ONE WAY DOPPLER EXTRACTOR VOLUME I

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ONE WAY DOPPLER EXTRACTOR

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by

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TABLE OF CONTENTS

N-a

TABLE OF CONTENTS (CONT'D)

TABLE OF CONTENTS (CONT'D)

v-c

APPENDICES

LIST OF ILLUSTRATIONS

v-e

LIST OF ILLUSTRATIONS (CONT'D)

LIST OF ILLUSTRATIONS (CONT'D)

LIST OF ILLUSTRATIONS (CONT'D)

LIST OF ILLUSTRATIONS (CONT'D)

TABLES

ABSTRACT

This report presents a feasibility analysis, trade-offs and implementation for a One Way Doppler Extractor system. A doppler error analysis is discussed which shows that quantization error is a primary source of doppler measurement error. Several competing extraction techniques are compared and a new "Vernier" technique presented which obtains high doppler resolution with low speed logic. Parameter trade-offs and sensitivities for this Vernier technique are discussed, leading to a hardware design configuration. A detailed design, operation and performance evaluation of the resulting breadboard model is presented which verifies the theoretical performance predictions. The breadboard model contains the circuitry to interface with an S-band transponder, to extract the doppler and time interval counts, to compute navigational parameters, by means of a microprocessor, from these counts and to display the results. Performance tests have verified that the breadboard is capable of extracting doppler, on an S-band signal, to an accuracy of less than 0.02 hertz for a one second averaging period. This corresponds to a range rate error of no more than 3 millimeters per second. Finally, a design for a flight hardware doppler extractor is presented, which can extract the doppler from any one of four S-band input frequencies. The flight hardware is projected at 410 cubic inches, 10.2 pounds and consuming 8 watts of prime power.

FOREWORD

This is a final report for NASA Contract NAS 9-13517 covering the period from 1 July 1973 to 1 November 1974. The program consisted of the following three phases:

1. Feasibility study and tradeoff analysis
2. Breadboard development
3. Feasibility study of digital VCO techniques

The overall program was conducted under the direction of Edward Nossen. Both feasibility studies were carried out by Eugene Starner. The breadboard development was directed by Seymour Klein; major contributors to the breadboard development were Richard Blasco, Daniel Hampel and John Yanosov. The preliminary design of flight hardware was also headed up by Seymour Klein.

Volume 1 of this report contains 3 parts:

Part 1 - The feasibility study and tradeoff analysis.

Part 2 - Breadboard development

Part 3 - Flight hardware design

Volume 2 of this report covers the feasibility study of digital VCO techniques.

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SYMBOLS AND ABBREVIATIONS USED IN THIS REPORT

AGC	Automatic Gain Control
APL/JHU	Applied Physics Laboratory/John Hopkins University
ARO	Anytime Readout
	Limiter Signal Suppression Factor
B_L, B_{LO}	Phase Lock Loop One Sided Bandwidth
B_{IF}	Intermediate Frequency Bandwidth
C, DC	Value of and Error in Measured Value of Speed of Light
CAD	
EXT FUN	External Function
EXT FUN REQ	External Function Request
EXT INT	External Internal
ECL	Emitter Coupled Logic
E_X	Error in X also ΔX
F_D	Doppler Off-set Frequency
F_τ, f_τ	S-Band Transmitter Frequency
F_B	Bias Frequency
$F_B + F_D$ or F_{B+D}	Bias Plus Doppler Frequency
F_o	Clock Reference Frequency (either primary frequency or a derivative of the master clock)
FPS, FT/SEC	Feet per second
G_τ, G_r	Transmit or Receive Antenna Gain
OWD	One Way Doppler
$N_B + D$	Counted Values of Bias Plus Doppler Frequencies ($F_B + F_D$)
N_o	Counted Values of the Clock Reference (F_o)
PLL	Phase Locked Loop
PLO	Phase Lock Oscillator
R	Range or Variable Multiplier
RF	Radio Frequency
RSS	Root Sum Squared Value
RMS	Root Mean Squared Value

RX	Performance to Receiver
RQ	Performance to Parameter
$\dot{R}$	Range Rate
ΔR	Change in Range
S_s, $\hat{S}_s$	Actual and One Sigma Values for that Short Term Oscillator Drift
S_L, $\hat{S}_L$	Actual and One Sigma Values for Long Term Oscillator Drift
S	Drift
S/N	Signal to Noise Ratio
SOW	Statement of Work
σ_χ	Standard Deviation of χ
τ, T, t	Doppler Integration or Averaging Period
t	Time as a variable
TX	Reference to Transmitter or Transmitter Parameter
USB	Unified S-band Transponder
VCO	Voltage Controlled Oscillator
VXCO	Voltage Controlled Crystal Oscillator
V_R	Range rate (same as $\dot{R}$)
W or ω	Phase Lock Loop Natural Frequency
WBD	(Section 4)

SECTION 1

INTRODUCTION AND SUMMARY

One way doppler navigation is a technique whereby an orbiting vehicle's position is inferred from a knowledge of the line of sight range rate history to a known reference point. The range rate history is determined by accurately measuring the doppler shift received from a stable transmitter located at the reference point. Figure 1-1 shows the geometrical relationships for a space vehicle receiver and a ground based transmitter. The advantages of one way doppler navigation are the ability of the space vehicle to determine positional and navigational data autonomously and eliminate the need for special application navigational aids. The feature of only requiring a one way RF link may also be desirable for certain applications where two way links are not always desirable or practicable.

One way doppler navigation requires very accurate measurements of the vehicle's range rate with typical values of 3 cm/sec being required over a one second integration interval. To obtain a range-rate accuracy of 3 cm/sec (0.1 ft/sec) using S-band frequencies, requires that the doppler frequency be measured to within 0.2 Hz. This requires the use of stable oscillators and accurate receivers as shown in the block diagram of Figure 1-2.

The S-band frequency must be controlled to within 0.2 Hz over the period of the doppler measurement. Also, other error sources such as caused by Gaussian noise, digital processes and propagation path variations should be controlled where practical to obtain the 0.2 Hz accuracy.

This report presents an error analysis of the one-way doppler measurement, and feasibility/trade-off evaluations for several doppler extractor and receiver concepts. The results of the error analysis show that the quantization error resulting from digitizing the doppler information can be the most significant source of error when conventional frequency counting techniques are employed. To reduce the quantization error the doppler

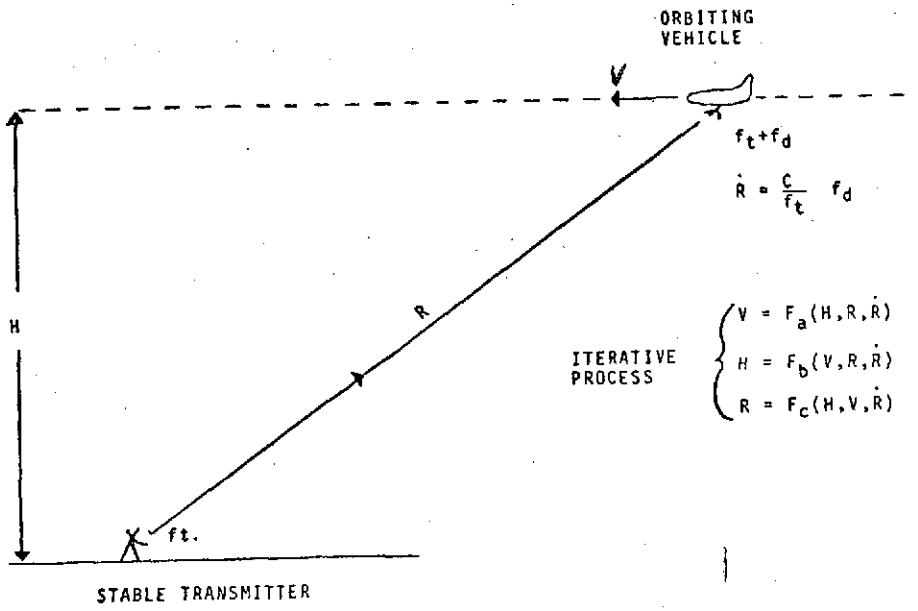


FIGURE 1-1 ONE-WAY DOPPLER GEOMETRY

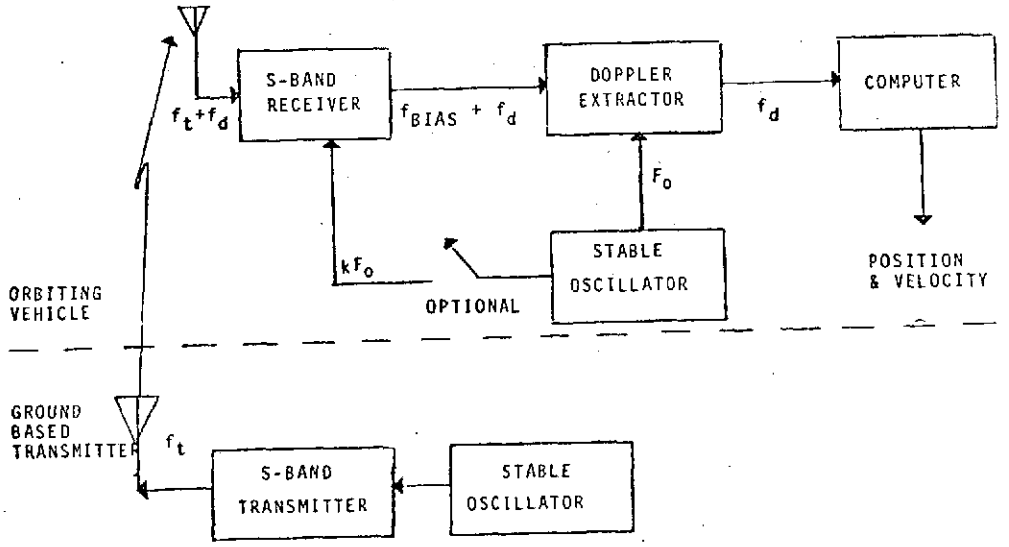


FIGURE 1-2 BLOCK DIAGRAM OF A ONE-WAY DOPPLER NAVIGATION SYSTEM

should have some means of determining fractional cycle counts in order that the total error budget is within the required 3 cm/sec(0.1 ft/sec) accuracy.

A new technique has been developed whereby fractional cycle counts are obtained within short integration periods. This technique which has been disclosed as new technology, employs a vernier approach in that the doppler frequency is compared with a stable reference oscillator frequency by means of a zero crossing coincidence detector. The technique offers low weight, low power consumption and simple construction without sacrificing accuracy or reliability. The analysis and breadboard test results show that this technique can supply range-rate resolution of at least 3 cm/sec(0.10 ft/sec) under all reasonable conditions of velocity (0-8230 m/sec., 0-27,000 ft/sec), acceleration (0-610 m/sec^2, 0-2000 ft/sec^2), loop signal-to-noise ratio ($\geq$ 10 dB) and for all integration periods of 0.5 seconds or more.

The breadboard one-way doppler extractor which was delivered to NASA, is shown in Figure 1-3. The functional features of this breadboard are tabulated in Table 1-1. The breadboard was interfaced with an Apollo USB transponder, specifically LM serial number 127, operating at a receive frequency of 2101.8 MHz. The breadboard was also provided with an interface for use with a Univac 1218 Computer. The breadboard doppler extractor, the S-band transponder and the associated test instrumentation are shown in Figure 1-4. The breadboard met or exceeded all the performance requirements called for in the Statement of Work as shown in Table 1-2. It was delivered with a 200 nanosecond time aperture setting which resulted in the performance listed in the last column of the table. As shown, even better accuracy performance can be achieved with a 15 nanosecond time aperture. However, this is at the expense of the delay time between a measurement command and command execution. In applications where the exact time of the measurement's execution is unimportant, this improved accuracy is readily available.

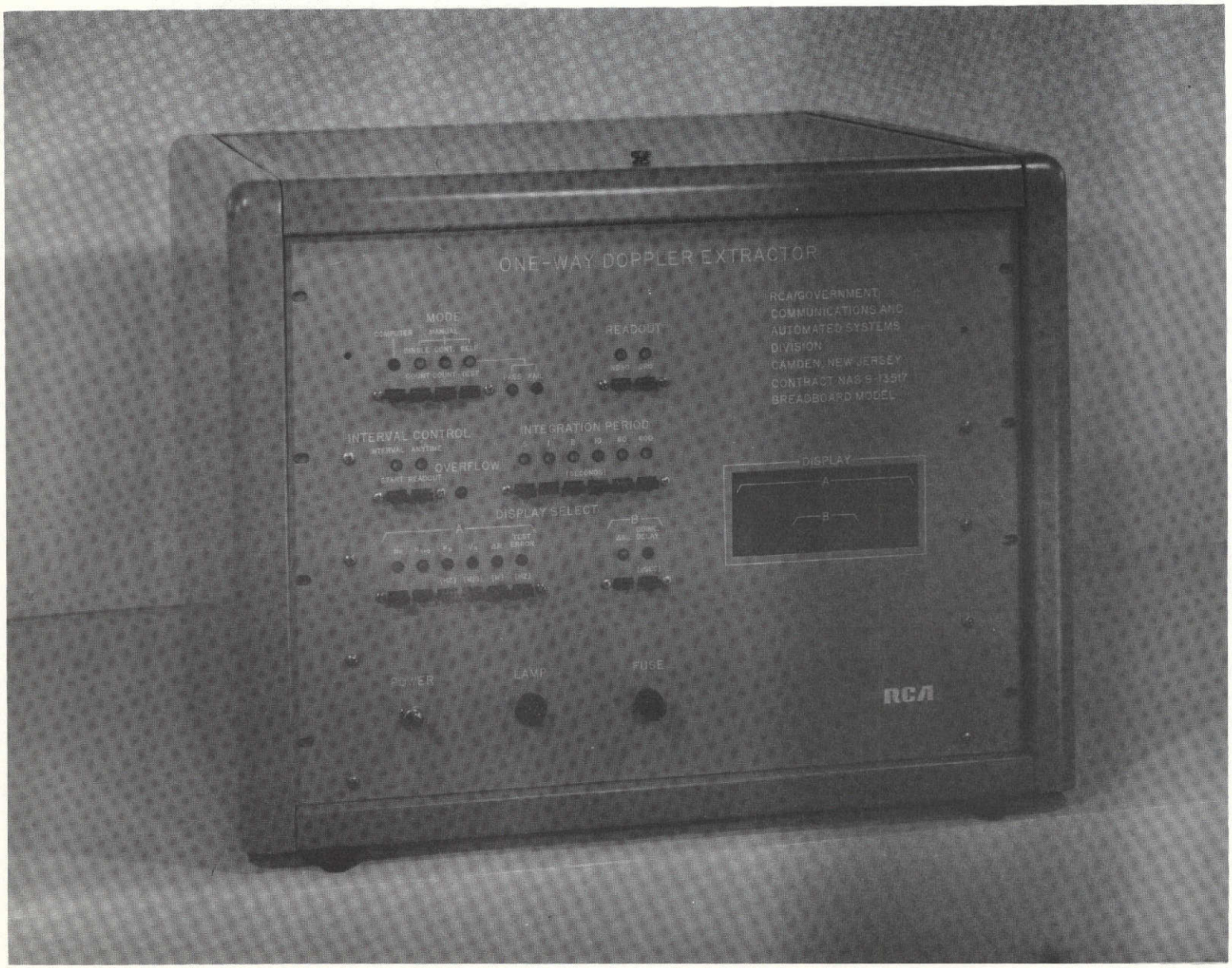


FIGURE 1-3 ONE-WAY DOPPLER EXTRACTOR BREADBOARD

TABLE 1-1 Breadboard Functional Summary

Parameter	Remarks
Non-destruction readout	Manual or Computer Selection. Counts continuously for up to 600 seconds with overflow indication.
Destructive readout	Manual or Computer Selection. Resets counters to zero at start of each new measurement interval.
Fixed integration periods of 0.5, 1,2,10,60 and 600 seconds.	Manual or Computer Selection of the period with automatic display of results.
Anytime readout	Manual or Computer control of the measurement interval from $\approx$ 0 to 600 seconds.
Self Test	Injects a known frequency near front end of extractor and checks the computed doppler for accuracy. Test is passed if error $\leq$ 0.3 Hz.
Displays Raw bias plus doppler or clock counts. Doppler frequency in Hertz. Range rate in meters/second. Slant range difference in meters	Any one of these results is displayed by push button switches.
Time delay between stop command and actual stop execution. Integration time variation in microseconds.	Switch selectable between either display.

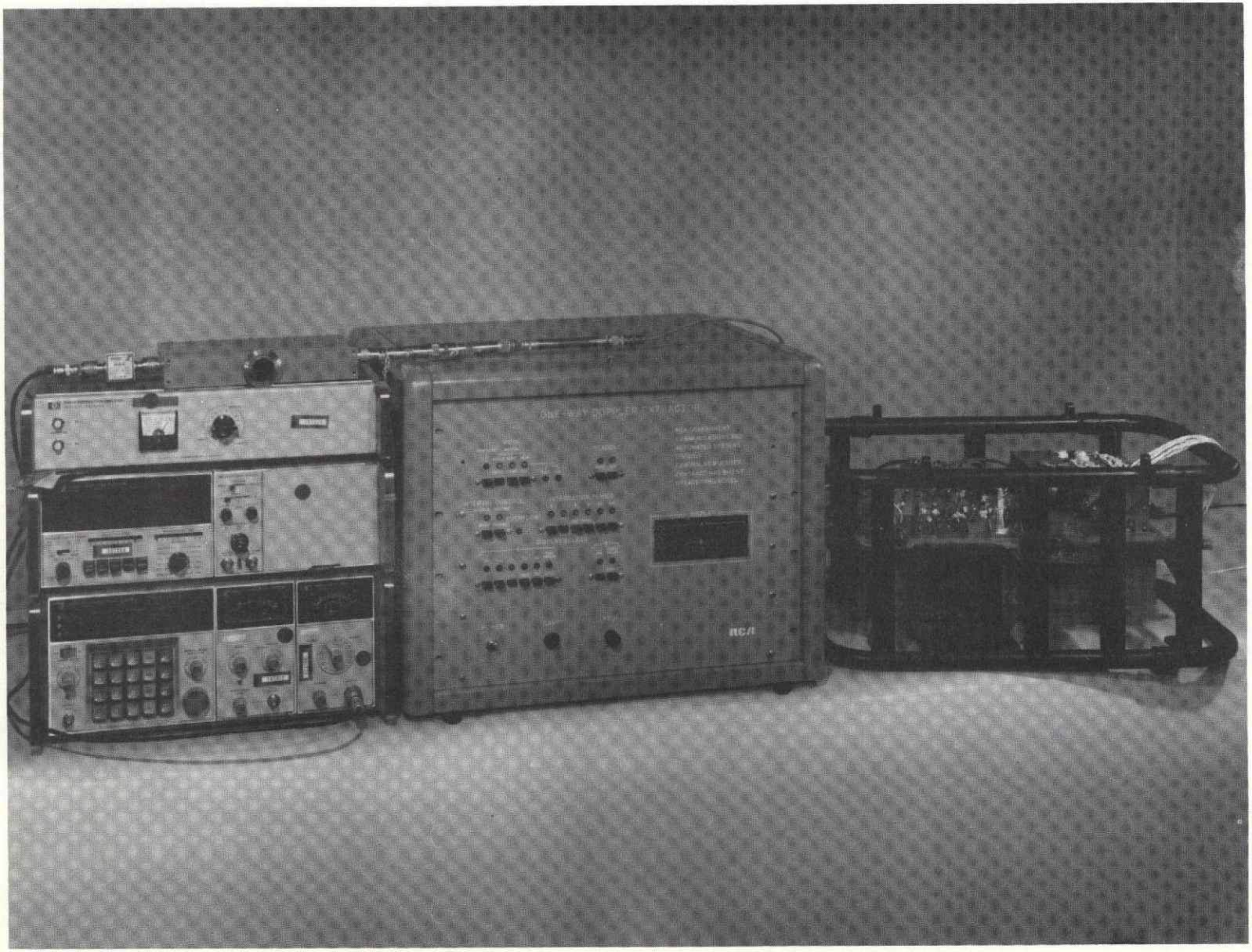


FIGURE 1-4 ONE-WAY DOPPLER EXTRACTOR TEST INSTRUMENTATION

A preliminary design configuration for flight hardware has been established, which satisfies the Rockwell International Space Shuttle requirements. The equipment necessary for doppler extraction from multiple carrier frequency receivers was estimated to be 5.6X6.9X10.6 inches, weighs 10.2 lbs and consumes no more than 8 watts of prime power.

TABLE 1-2 Breadboard Performance Summary

Parameter	SOW	Breadboard Performance	
		15 ns aperture	200 ns aperture
Noise error at the integration period.			
0.5 sec.	0.6 Hz	0.03 Hz	0.24 Hz
2 sec.	0.25 Hz	0.009 Hz	0.05 Hz
10 sec.	0.23 Hz	0.003 Hz	0.01 Hz
60 sec.	0.20 Hz	0.0025 Hz	0.002 Hz
600 sec.	0.20 Hz	0.0025 Hz	0.002 Hz
Maximum time Interval variation	100 us	60 ms	4 us

PART 1

FEASIBILITY/TRADE-OFF ANALYSIS

This part of the report includes a discussion of the Feasibility and Trade-off analysis of candidate one way doppler extractor systems. Major topics include a discussion of theoretical considerations, such as an error analysis and methods for error reduction, and implementation considerations, which include the trade-offs of various receiver and doppler extractor options.

A system is selected for a one-way doppler extractor breadboard and a performance sensitivity analysis is presented for this system. Major sections included in this part are:

2.0 THEORETICAL CONSIDERATIONS

3.0 IMPLEMENTATION

4.0 SYSTEM TRADE-OFFS AND OPTIMIZATIONS

SECTION 2
THEORETICAL CONSIDERATIONS

2.1 ERROR ANALYSIS

The error budget for a doppler measuring device consists of three types of errors; deterministic error, bias error and random error.

The deterministic errors are due to predictable effects such as refraction and multipath. These values can be predicted from estimates of satellite locations and only residual random errors result. It is assumed that these residual errors are independent between each doppler measurement and their contribution to the total error budget is discussed along with the other random error sources.

The bias error does not change significantly during a satellite pass or longer and is due to long term frequency drift of the stable oscillators and uncertainty in the measured value of the speed of light. Since these errors change only slowly with time, if at all, they cannot be removed by filtering (e.g., long averaging times) the individual doppler measurements. It may be possible to reduce the bias error in predicted range, however, by averaging the predicted location over many satellite passes.

The random errors change between each doppler measurement(fractions of a second) and are caused by short term oscillator instabilities, quantization error, phase lock loop tracking errors, noise induced errors in the doppler counter and residuals from the deterministic errors. These errors can be reduced by some form of filtering (e.g., long averaging times) of each doppler measurement.

Previous efforts in the area of ground to satellite one-way doppler measurement errors have been investigated. K. Bures and G. Smith of the Ames Research Center (reference 1) derive formulas for the error sources for a two way doppler measurement. Where applicable to the one-way doppler measurement these formulas have been used in this report for developing the error budget. RCA

describes (reference 2) the effects of ionospheric and tropospheric refraction on range measurements. W. Guier and G. Weiffenback of APL/JHU (reference 3) describe the errors resulting from ionospheric refraction. This section of the report summarizes the results of these references where applicable to the one-way doppler technique, and derives other error sources peculiar to one-way doppler.

2.1.1 DETERMINISTIC ERRORS

The deterministic errors have a mean value and a random component. As is generally assumed, the mean value can be predicted for each satellite pass so that only the random component enters into the error analysis. The resultant residual errors in range-rate are assumed to be independent for each doppler measurement and their contribution to the total error budget is discussed under the random errors.

2.1.2 BIAS ERROR

Reference (1) derives the bias error caused by uncertainty in the speed of light with the following result:

$$\boxed{\sigma_{\dot{R}} = \dot{R} \cdot \frac{\Delta C}{C}} = 3.33 \times 10^{-7} \quad R$$

Since $\dot{R}$ maximum = 8230 meters/sec. (SOW Specification)

$$\sigma_{\dot{R}} \text{ (max.)} = 2.75 \times 10^{-3} \text{ meters/sec}$$
$$= 9.0 \times 10^{-3} \text{ ft/sec.}$$

The range-rate error caused by long term oscillator instability is not defined in the references for the one-way doppler case. However, the resultant error is easily calculated by assuming the oscillator drifts by an amount $S_L \cdot f_t$; where S_L is the long term stability and f_t the transmitted frequency. The error in the doppler measurement is then:

$$\epsilon f_d = S_L \cdot f_t$$

$$\epsilon \dot{R} = \frac{C}{f_t} \cdot \epsilon f_d = C \, S_L$$

If $\hat{S}_L$ is the RMS frequency stability, then:

$$\sigma_{\dot{R}} = C \cdot \hat{S}_L \qquad C = \text{velocity of light.}$$

Since both the ground station and satellite oscillators will drift, the combined error due to long term instability is given by:

$$\sigma_{\dot{R}} = C \sqrt{\hat{S}_{LG}^2 + \hat{S}_{LS}^2}$$

where $\hat{S}_{LG}$ = ground oscillator drift
$\hat{S}_{LG}$ = satellite oscillator drift

If $\hat{S}_{LG} << \hat{S}_{LS}$ and $\hat{S}_{LS} = 10^{-9}$ (From discussions with NASA)

Then:

$\sigma_{\dot{R}} = 30$ CM/Sec. = 1.0 Ft/Sec.

The total RSS range rate bias error is then:

$$\sigma_{\dot{R}} = 30 \text{ CM/Sec} = 1.0 \text{ Ft/Sec.}$$

2.1.3 RANDOM ERRORS

The short term instability error is derived in the same manner as the long term factor. The resultant range rate error is:

$$\sigma_{\dot{R}_S} = C \sqrt{\hat{S}_{SG}^2 + \hat{S}_{SS}^2}$$

where $\hat{S}_{SG}$ is the short term RMS stability of the ground oscillator and $\hat{S}_{SS}$ is the stability of the satellite oscillator.

If $\hat{S}_{SG} << \hat{S}_{SS}$ and $\hat{S}_{SS} = 10^{-10}$

Then $\sigma_{\dot{R}_S} = 3.0$ CM/Sec = 0.10 Ft/Sec.

The quantization error contribution can be derived from the count error as follows:

$$\epsilon_{f_d} = \epsilon/T$$

where ϵ_{fd} is the doppler error, ϵ = fractional cycle lost in the quantization process, T = doppler averaging time.

The range rate error is uniformly distributed over the interval from zero to:

$$\epsilon_{\dot{R}\,(Max)} = \frac{c\,\epsilon}{f_t\,T}$$

and

$$\sigma_{\dot{R}_Q} = \frac{c\,\epsilon}{f_t\,T\sqrt{12}}$$

The quantization error can occur at both the beginning and ending of the counting period, and since these errors are independent, their variances add. Thus, the resultant quantization error is

$$\sigma_{\dot{R}_Q} = \frac{c\,\epsilon\sqrt{2}}{f_t\,T\sqrt{12}} = \frac{c\,\epsilon}{f_t\,T\sqrt{6}}$$

If doppler cycles are counted then ϵ has a maximum value of 1. For a 0.5 second counting period, (shortest value specified in SOW), the total quantization error is:

$$\sigma_{\dot{R}} = 12 \text{ CM/Sec.} = 0.41 \text{ Ft/Sec.}$$

Generally a phase lock loop (PLL) is used to track carrier plus doppler frequencies. The PLL introduces a timing jitter on the output frequency which results in a frequency error in the doppler counters. The range-rate error resulting from the use of a PLL is defined in Reference (1) as:

$$\sigma_{\dot{R}_J} = \frac{c}{2\pi\, f_t T \sqrt{(S/N)\,loop}}$$

If (S/N) loop = 10 dB
(A minimum requirement for accurate PLL track)

and T= 0.5 seconds
Then:

$$\sigma_{R_J} = 1.5 \text{ CM/Sec} = 0.050 \text{ Ft/Sec.}$$

The range rate error caused by noise at the input of the doppler counter is given in reference (4) as:

$$\sigma_{\dot{R}_N} = \frac{C}{2.6\, f_t T \sqrt{(S/N)\ \text{counter}}}$$

if $f_t = 2X10^9$, T = 0.5 sec.

$$\sigma_{\dot{R}_N} = \frac{11.5}{\sqrt{S/N}}\ \text{CM/Sec} = \frac{0.378}{\sqrt{S/N}}\ \text{ft./sec.}$$

if S/N = 60 dB, a typical VCO output value

$$\sigma_{\dot{R}_N} = 1.15X10^{-2}\text{CM/Sec} = 3.78X10^{-4}\text{Ft/Sec.}$$

Other random error sources - The residual errors from atmospheric effects will be root sum squared with the other random errors if they appear to be of significant value. Reference (4) shows that at 2 GHz, the doppler error due to ionospheric refraction has a maximum value of 0.25 Hz, or a range-rate error of .12 feet per second. However, since this is the maximum error the RMS error over the complete path will be significantly less than this value.

Likewise, from reference (2) a doppler error can be derived from range errors due to tropospheric scatter. Computing the standard deviation of the change in range for each degree change in elevation, and deriving the time required for each degree change results in a maximum random range-rate error of .16 meters per second for elevation angles greater than 5 degrees. This is the maximum error for a 100 mile orbit. At 300 mile altitude the range rate error caused by the ionosphere should be half this value and will be reduced even further at higher elevation angles.

The total root sum squared random error for the nominal parameters chosen is:

$$\sigma_{\dot{R}_{RSS}} = 12.8\ \text{cm/sec.} = .424\ \text{Ft/Sec.}$$

(The effects of the residual errors have been ignored in this summation)

The quantization error accounts for over 90% of this total error. Thus, techniques which reduce the quantization error would be of significant advantage in controlling the overall error budget for the doppler extractor.

The various errors encountered in the one way doppler measurements are summarized in Tables 2-1, 2-2 and 2-3.

TABLE 2-1 DETERMINISTIC ERRORS

ERROR SOURCE	ERROR MAGNITUDE/REMARKS
Ionospheric Refraction	Residual error random 1σ = 3.7 cm/sec(.12 Ft./sec)
Tropospheric Scatter	Residual error random 1σ = 6.1 cm/sec.(.2 Ft./sec)
Multipath	Requires knowledge of ground station environment.
Vehicle Acceleration	Depends on degree of data processing No error is Δ range computer.

TABLE 2-2 BIAS ERRORS

ERROR SOURCE	ERROR MAGNITUDE
Measured Velocity of Light	$1\sigma = 3.33 \times 10^{-7} \dot{R}$ $= 0.28$ CM/Sec (.009 Ft/Sec)
Long Term Oscillator	$1\sigma = C \cdot \hat{S}_{LS}$ $= 30$ CM/SEC (1 FT/SEC), $\hat{S}_{LS} \leq 10^{-9}$

TABLE 2-3 RANDOM ERRORS

ERROR SOURCE	RANDOM MAGNITUDE
Short Term Oscillator Stability	$1\sigma = C \cdot \hat{S}_S$ $= 3$ CM/Sec (.1Ft/Sec.), $(\hat{S}_S = 10^{-10})$
Quantization Error	$1\sigma = \frac{C \epsilon}{f_t T \sqrt{6}}$ $= 12.2$ CM/Sec (.41 Ft/Sec.), $\epsilon = 1$, T=0.5 Sec.
Jitter in Phase Lock	$1\sigma = \frac{C}{2\pi f_t T \sqrt{(S/N)_{loop}}}$ $= 1.5$ CM/Sec (.05 Ft/Sec.), $(S/N)_{loop} = 10$ dB
Noise on VCO Output	$1\sigma = \frac{C}{2.6 f_t T \sqrt{(S/N)_{VCO}}}$ $= .012$ CM/Sec (.0004 Ft/Sec.) $(S/N)_{VCO} = 60$ dB

2.2 METHODS OF ERROR REDUCTION

Several techniques have been investigated for reducing the measurement errors from the doppler extractor. Of the three primary random error sources, quantization error is the most significant and many techniques have been devised to reduce this error source. The other error sources (jitter and frequency stability) can only be reduced by brute force techniques, i.e., improved S/N ratio, increased averaging time or improved oscillator stability. These techniques are costly for significant error reduction and require a trade-off of desired accuracy vs cost to achieve that accuracy. The quantization error, however, can be reduced by proper hardware changes, and although these may add to the hardware cost, the resultant large improvement can be attained with only small changes in cost.

2.2.1 TECHNIQUES FOR REDUCTION OF QUANTIZATION ERROR

2.2.1.1 Averaging Time

For reduced quantization error in range-rate it is desirable to have long averaging times. However, if the Orbiting Vehicle is experiencing a changing range rate acceleration, long averaging times will result in a range rate error due to assuming constant acceleration. This error can be reduced to zero by computing change in range. As the following analysis shows, regardless of the length of the averaging time or the velocity history of the vehicle, the change in slant range is exactly proportional to the change in cycle count.

$$\Delta R_a = \int_o^t \dot{R}\, dt = \text{actual change in slant range.}$$

But:
$$\Delta N_d = \int_o^t f_d \, dt = \text{change in cycle count}$$

and,
$$f_d = \frac{\dot{R}}{C} f_t$$

$$\therefore \Delta Nd = \frac{ft}{C}\int_o^t \dot{R}\, dt = \frac{ft}{C} \Delta R_a$$

$$\Delta R_a = \frac{c}{f_t} \cdot \Delta Nd \quad \text{(independent of t)}$$

Thus, if changes in slant range are computed, no errors are introduced by using very long averaging times, regardless of the motion of the orbiting vehicle during the averaging period. The change in slant range from the ground transmitter is identically proportional to the change in doppler count.

Long averaging times will affect the total cycle count if the oscillator drift is significant over the averaging period. For short time intervals, the short term stability becomes worse as the interval becomes shorter. For many typical oscillators, the stability becomes constant, independent of the averaging time, when the averaging time is in the range of 1 to 100 sec. Figure 2-1 shows the results of all errors as a function of averaging time. Above 2.2 seconds averaging, S_S becomes the dominant error in R, if whole cycles are counted.

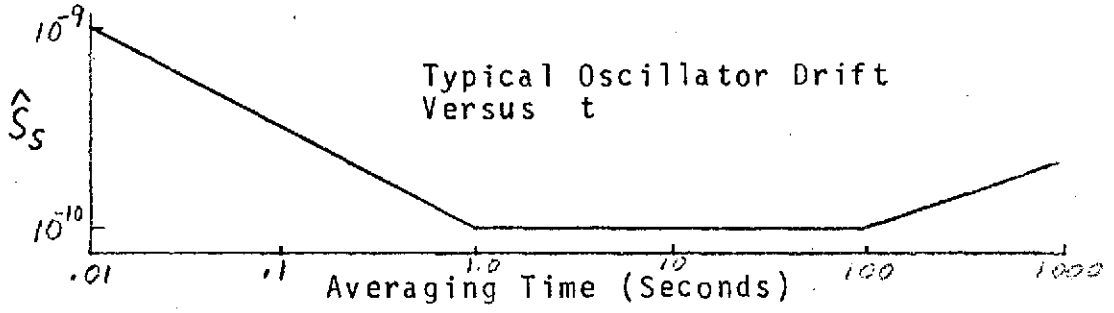
Below 2.2 seconds, quantization becomes the dominant error. If cycles are counted to a resolution of 0.1 cycles, the quantization error is only significant for averaging periods less than 0.1 seconds.

2.2.1.2 Period Measurement

W. H. Guier (et al) describes a technique (Reference 5) to reduce quantization error by the method of measuring the period between N cycles of the doppler frequency (or doppler + bias). This method is used by APL in the TRANET ground tracking system, and the technique is represented in Figure 2-2. The period of N cycles of bias plus doppler is measured by counting the clock cycles, with a resultant quantization on the clock cycle count.

The resultant range-rate error is developed in the figure and indicates that the error is reduced by the ratio of the bias to clock frequencies. Thus, for nominal 1 MHz bias and a 5 MHz clock the range rate error can be reduced by 2.4 cm/sec (0.08 ft/sec) in a 0.5 second averaging time.

This technique is attractive from the standpoint of simplicity, but the time interval over which the doppler count is made becomes a variable. This is due to the fact that N is generally



Resultant △ Range Error Versus Averaging Time

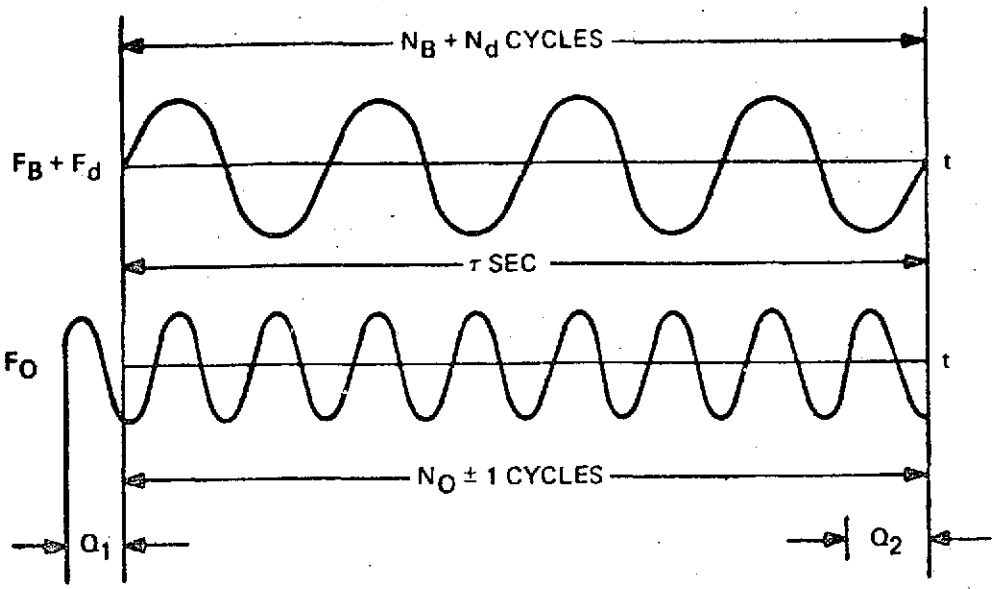
t	σ_R (Drift)	σ_R (Quant.)	σ_R (Jitter)	σ_{RMS}
0.1	0.95 CM	6.1 CM*	0.76 CM***	6.22 CM
0.5	2.10 "	6.1 "	0.76 "	6.50 "
1.0	3.00 "	6.1 "	0.76 "	6.84 "
2.0	6.00 "	6.1 "	0.76 "	8.59 "
5.0	15.00 "	6.1 "	0.76 "	16.21 "
10.0	30.00 "	6.1 "	0.76 "	30.62 "
0.1	0.95 "	0.61 "**	0.76 "	1.36 "
0.5	2.10 "	0.61 "	0.76 "	2.32 "
1.0	3.00 "	0.61 "	0.76 "	3.15 "
2.0	6.00 "	0.61 "	0.76 "	6.08 "
5.0	15.00 "	0.61 "	0.76 "	15.03 "
10.0	30.00 "	0.61 "	0.76 "	30.02 "

* Whole Cycle Count (ϵ = 1)

** Fractional Cycle Count (ϵ =0.1)

*** S/N = 10 dB

FIGURE 2-1 EFFECT OF AVERAGING TIME ON DELTA RANGE ERRORS



ERROR ANALYSIS

$$F_d = \frac{N_B + N_d}{\tau} - F_B = \frac{N_B + N_d}{N_0 (1 \pm 1/N_0)} F_0 - F_B$$

$$\epsilon F_d = \pm \frac{N_B + N_d}{N_0^2} F_0 \quad \left(\begin{matrix}\text{TRIANGULAR} \\ \text{DISTRIBUTION}\end{matrix}\right)$$

$$\tau = N_0/F_0$$

$$\epsilon F_d = \pm \frac{F_B + F_d}{\tau F_0}$$

$$\sigma F_d = \frac{1}{\tau\sqrt{6}} \cdot \frac{F_B + F_d}{F_0}$$

FIGURE 2-2 PERIOD MEASURING TECHNIQUE TO REDUCE QUANTIZATION ERROR.

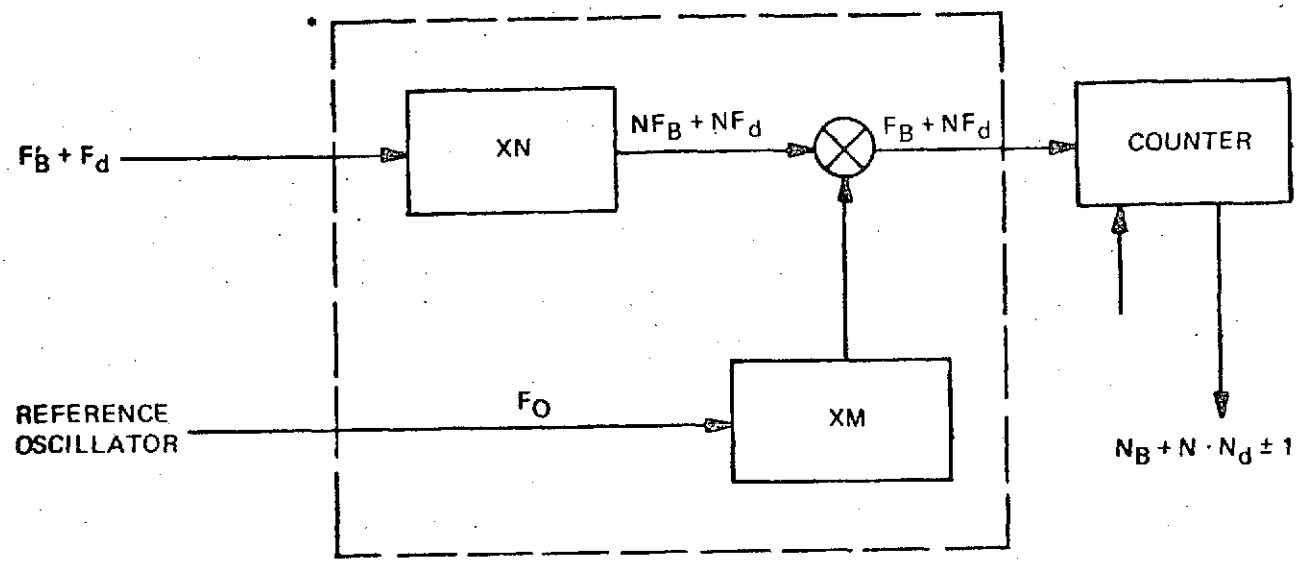
a fixed number and the time required for the doppler counter to reach depends on the doppler frequency. If the bias frequency is 1 MHz and the maximum doppler frequency is $\pm$ 60 kHz, then, for a 1 second nominal-averaging time ($N_o = 10^6$ nominal), the actual averaging time would range from 940 ms to 1060 ms.

It is possible to reduce the averaging time variation to no more than one period of the bias frequency by making N a variable number. For example, if doppler frequency is desired at regular intervals (t), the clock counter could output a stop command when the No count reaches a pre-determined value (based on t). Both counters would continue to run until the next bias plus doppler zero crossing. At this zero crossing both counters would be stopped. The bias plus doppler count would be an exact integer since its counter would count from exactly one zero crossing to another zero crossing. The clock count, however, would be in error by $\pm$ 1 count. The time interval variation would be no more than $\pm$ 1 cycle of the bias frequency.

If the bias frequency were 1 MHz, the time interval would vary no more than $\pm$ 1 us. However, a 10 MHz clock and counter would be required to achieve a one sigma doppler resolution of 0.08 Hz. A lower bias frequency could be used, however, it must be high enough to carry the full range of the doppler signal. A 100 kHz bias frequency could attain a doppler resolution of 0.13 Hz minimum (at $F_B + F_D = 160$ kHz) with a 1 MHz clock, but the time interval variation could then be as high as $\pm$ 25 us [$1/(F_B - F_D) = 1/40$ kHz].

2.2.1.3 Frequency Multiplication

Another technique to reduce the quantization error is to multiply the doppler frequency by some factor N. For the time interval there are N times as many counts but the quantization error remains at $\pm$ one count. In converting to doppler frequency, range rate, or change in range, the count must be divided by N. Thus, the net quantization error in range rate (for example) is reduced by a factor of N. This technique is represented in Figure 2-3



*MULTIPLIER STAGES CAN BE CASCADED TO KEEP NF_B LOW AT HIGH MULT.

ERROR ANALYSIS

$$Fd = \frac{\dfrac{N_B + N \cdot Nd \pm 1}{\tau} - F_B}{N}$$

$$\epsilon_{Fd} = \pm \frac{1}{N\tau} \quad \begin{pmatrix} \text{TRIANGULAR} \\ \text{DISTRIBUTION} \end{pmatrix}$$

$$\boxed{\sigma_d = \frac{1}{\tau\sqrt{6}} \cdot \frac{1}{N}}$$

FIGURE 2-3 ERROR REDUCTION BY FREQUENCY MULTIPLICATION, BLOCK DIAGRAM AND EQUATIONS.

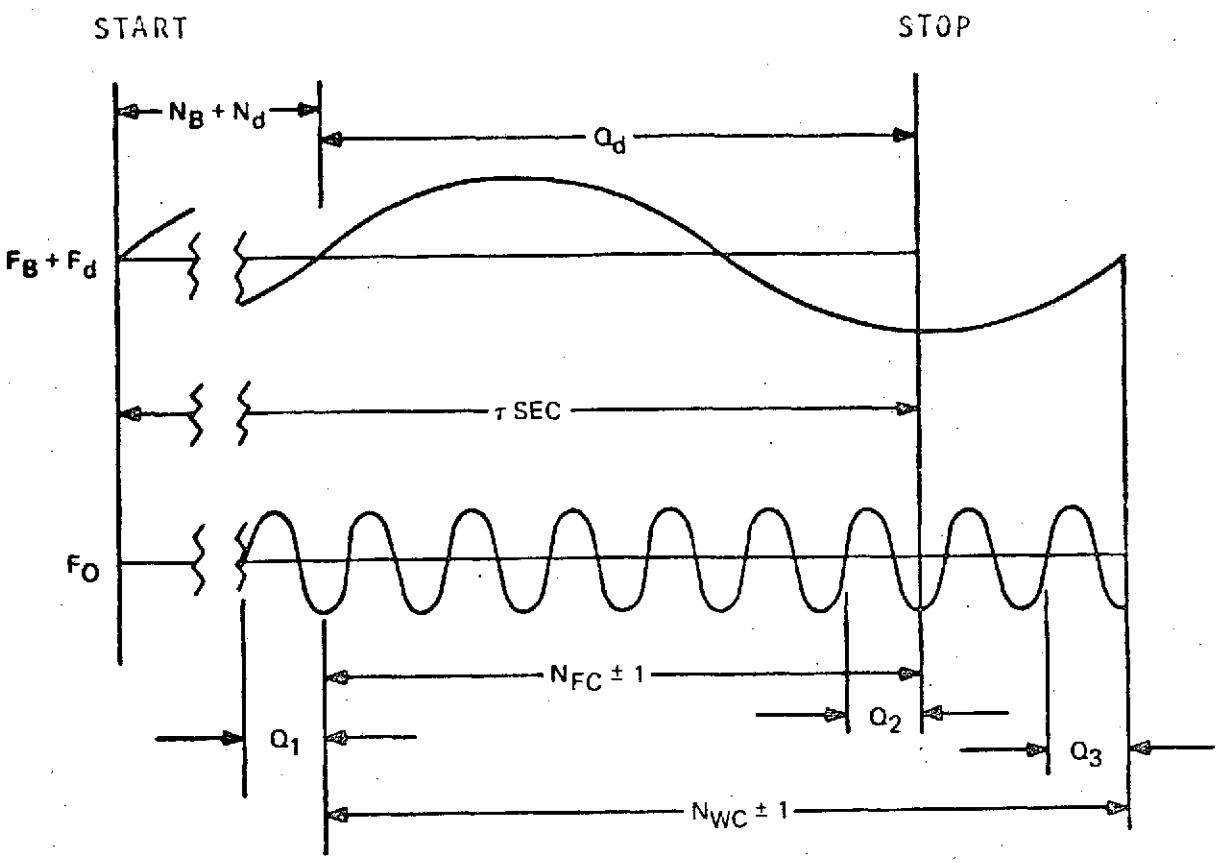
In the multiplication process the errors due to jitter and long and short term frequency instabilities are increased by the factor N. However, in computing range-rate or change in range the resultant count is divided by N. The errors also are divided by N so that the net result of the multiplication process is that the errors in range rate due to jitter and frequency instabilities are not affected, but the quantization error is reduced by a factor of N. The multiplication process decreases the signal to noise ratio by a factor of N^2. Thus, to obtain high resolution (high N), the S/N into the multiplier stage must be high, For example, if N=100, the S/N ratio into the multiplier should be greater than 50 dB if the S/N into the frequency counters is to be at least 10 dB.

The multiplication can be accomplished in alternate stages of multiplication and mixing to prevent the generation of high frequencies. Thus, two decade multipliers and two mixers with 9 MHz reference frequencies could be used to obtain a multiplication of 100 without generating frequencies in excess of 10 MHz (assuming a 1 MHz bias frequency).

2.2.1.4 Fractional Cycle Techniques

The fractional cycle technique employs a high frequency clock to divide the doppler cycle into many small fractions. The process is represented in Figure 2-4. The fractional cycle count is used to estimate the doppler quantization error to within the quantization error of the clock. The resultant improvement is equal to the ratio of the bias frequency to the clock frequency. The errors resulting from jitter and frequency instability are unaffected by this process.

This technique also causes an averaging time interval (t) variation of $\pm$ one bias frequency cycle. To simultaneously achieve high resolution and small time interval variations, the bias frequency must be large and the clock frequency must be even larger. Thus, a high speed clock counter must be employed to achieve doppler resolution improvements of more than about 10. If the bias frequency were chosen to be 1 MHz,



ERROR ANALYSIS

$$Fd = \frac{N_B + N_d + \dfrac{N_{FC} + (Q_2 - Q_1)}{N_{WC} + (Q3 - Q1)}}{\tau} - F_B$$

$$e_{Fd} = \pm \frac{1}{Nwc\,\tau} \begin{pmatrix} \text{TRIANGULAR} \\ \text{DISTRIBUTION} \end{pmatrix}$$

$$N_{WC} = Fo \quad \frac{1}{F_B + F_D} = \text{WHOLE CYCLE COUNT}$$

$$\sigma Fd = \frac{\sqrt{2}}{\tau\sqrt{6}} \cdot \frac{F_B + F_D}{Fo} \; ; \quad \left(\pm \frac{1}{Nwc} \quad \text{at } t = 0, \tau \right)$$

$$\sigma r_d = \frac{1}{\tau\sqrt{6}} \cdot \frac{(F_B + F_D)\quad \sqrt{2}}{Fo}$$

FIGURE 2-4 FRACTIONAL CYCLE TECHNIQUES TO REDUCE QUANTIZATION ERROR.

the clock frequency would need to be about 14 MHz to achieve a one sigma doppler resolution of 0.08 Hz. The time interval variation would be no more than about 1 us.

2.2.1.5 Vernier Technique by Coincidence Detection

The vernier technique is represented in Figure 2-5 and 2-6. This technique employs comparison of zero crossing coincidences between the bias plus doppler and clock frequencies to arrive at the doppler frequency. By counting both frequencies between coincidences, each counter is started and stopped on zero crossings. Thus, the $\pm$ 1 cycle count error is eliminated if the coincidence is defined with infinite precision. In practice, a coincidence would be declared whenever the two zero crossings are within some time interval which is small compared to the period of either frequency. The resultant error in doppler cycle count is distributed uniformly over the range $\pm$ P (where P is the time difference within which the two zero crossings are declared to be coincident). The resultant standard deviation of the doppler frequency error is:

$$F_D = \frac{1}{t\sqrt{6}} \cdot \frac{2P}{T_{(B+D)}} = \frac{1}{t\sqrt{6}} \cdot 2P(F_B+F_D)$$

Since $1/t\sqrt{6}$ is the nominal quantization error, the resultant error is reduced by a factor $2P\ (F_{(B+D)})$.

The vernier technique has the advantage that high resolutions can be obtained without the need for high speed counters, since all counted frequencies can be near one megahertz. The time interval variation occurs with the vernier technique as with some of the other techniques previously described. The time delay depends, in a non-linear fashion, on the selection of the bias and clock frequencies and the width of the coincidence aperture (2P). Typical values of delay are described and shown in a later section (Section 4.4)

2.2.1.6 Analog Technique

The analog technique employs an energy storing device to stretch the quantization interval and hence measure it with lower frequency clocks. Hewlett-Packard's computing (model HP 5360,

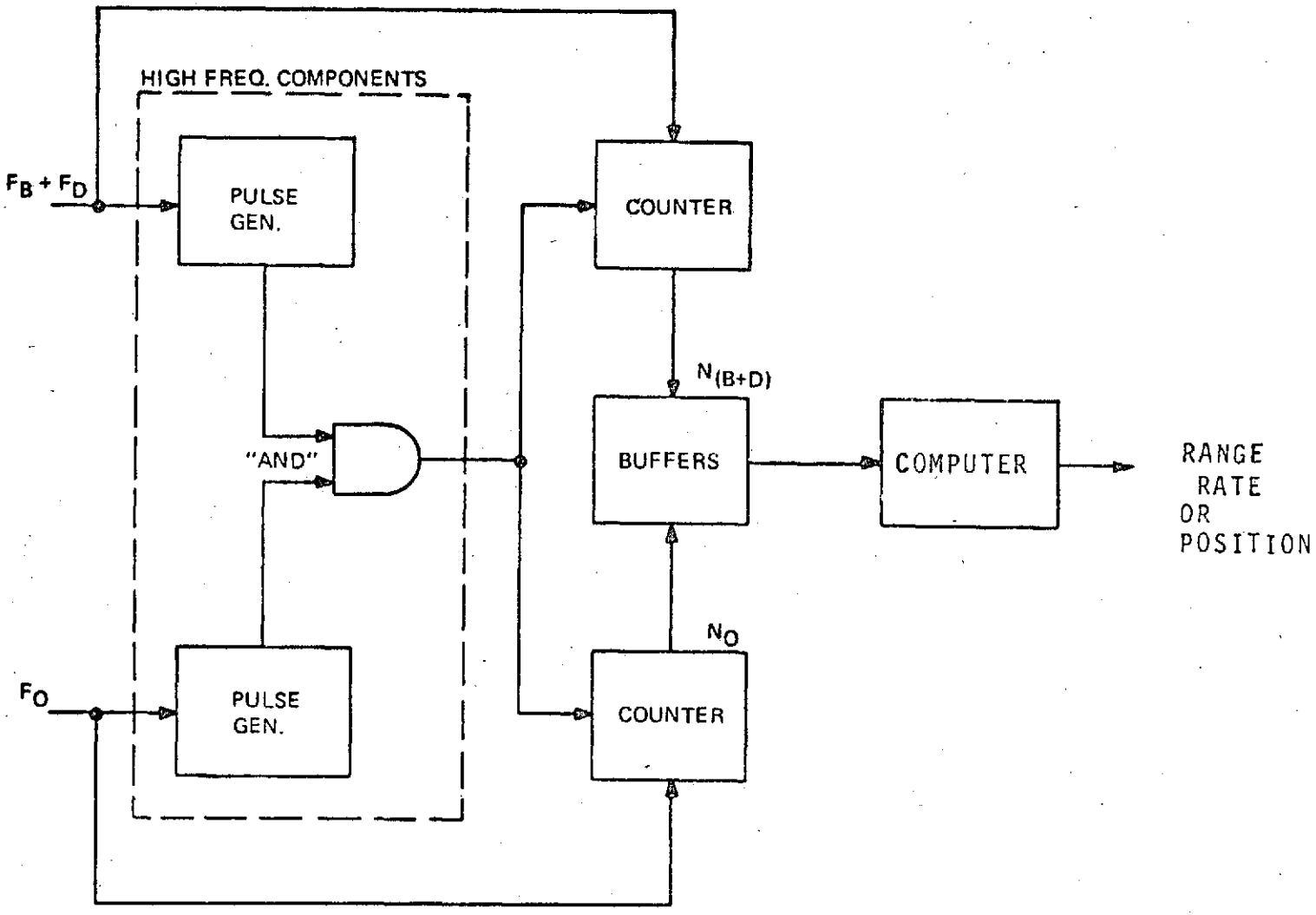
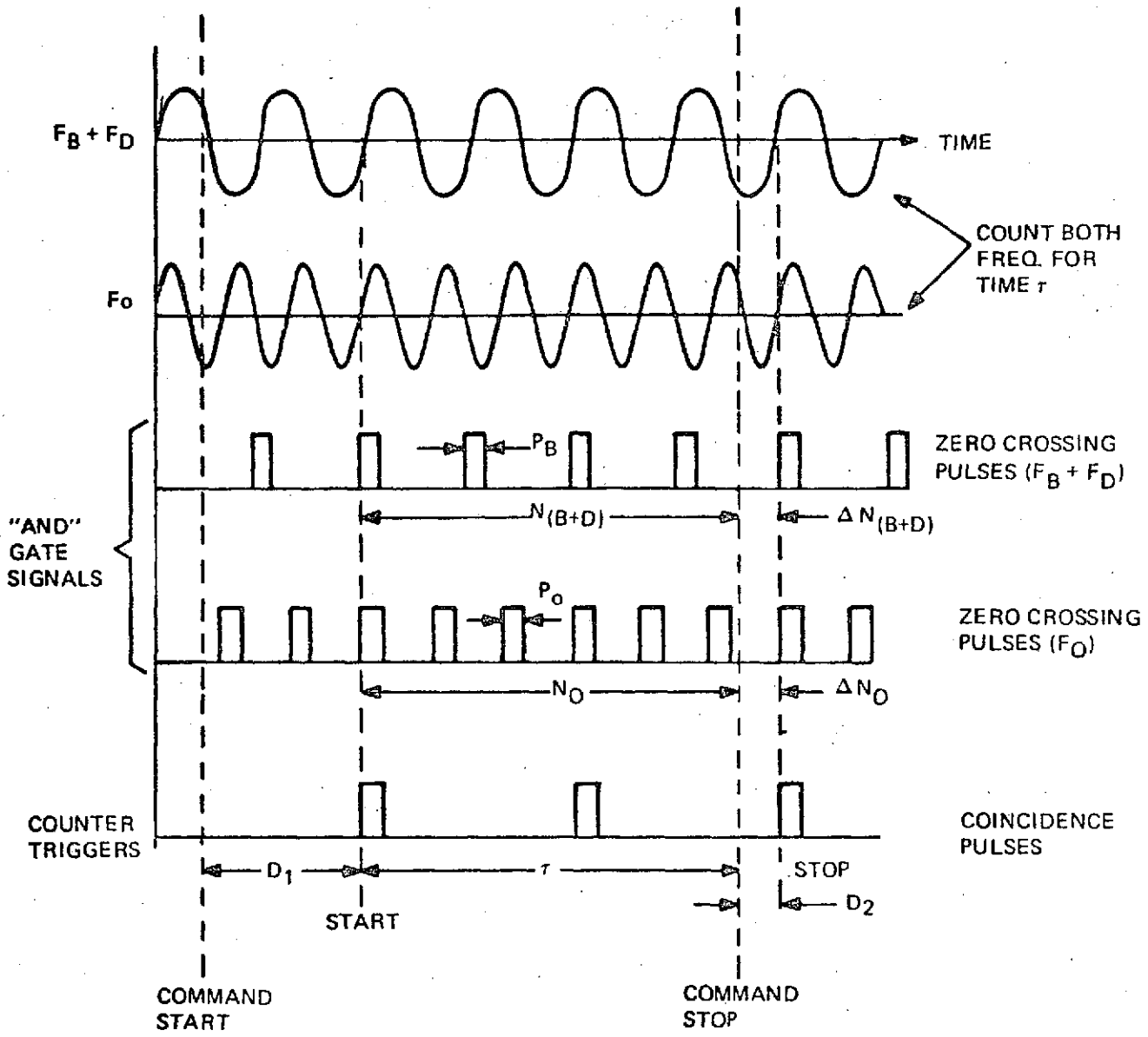


FIGURE 2-5 COINCIDENCE DETECTION DOPPLER EXTRACTOR, BLOCK DIAGRAM



$$\tau + D_2 = \frac{N_0 + \Delta N_0}{F_0}$$

$$F_D = \frac{N_{(B+D)} + \Delta N_{(B+D)}}{N_0 + \Delta N_0} \cdot F_0 - F_B$$

QUANTIZATION ERROR $= (P_0 + P_B)(F_B + F_D)$

FIGURE 2-6 TIMING SCHEME FOR COINCIDENCE DOPPLER EXTRACTOR.

Reference 6) employs this technique using a capacitor as the energy storing device. Figure 2-7 is a functional diagram of the technique. The quantization intervals (T_1 & T_2) are stretched by a factor of 1000 and the clock's frequency is counted over the stretched time intervals. The actual period for exactly $N_{(B+D)}$ whole cycles is then:

$$\tau = T_o + T_1 - T_2 = \left(N_o + \frac{N_1 - N_2 \pm 1}{1000}\right)\frac{1}{F_o}$$

and

$$F_B + F_D = \frac{N_{(B+D)}}{\tau} = \left(N_o + \frac{N_1 - N_2 \pm 1}{1000}\right)^{\frac{N_{(B+D)}}{}} \cdot F_o$$

The quantization error is

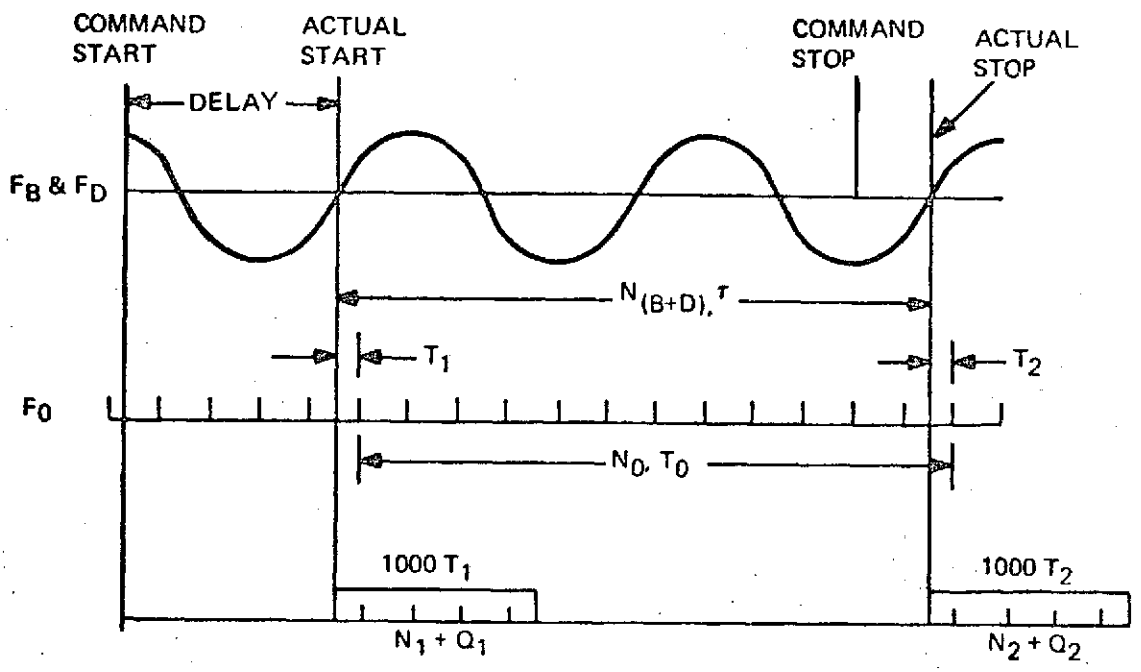
$$\epsilon_{F_D} = \pm\frac{N_{(B+D)}}{N_o} F_o \cdot \frac{1}{1000\, N_o}$$

but $N_o = F_o \tau$; $N_{(B+D)} = (F_B + F_D)\tau$

$$\therefore \epsilon_{F_D} = \frac{1}{\tau} \cdot \frac{F_B + F_D}{1000\, F_o}$$

$$\sigma_{F_d} = \frac{1}{\tau\sqrt{6}} \cdot \frac{F_B + F_D}{1000\, F_o}$$

The quantization error is reduced by a factor of 1000 relative to the nominal counting method. This technique requires that the bias frequency counter begins and ends on zero crossings of the bias frequency (since the technique is measuring the period of exactly N(B=D) cycles). The averaging time will vary by one bias frequency cycle resulting in a delay between the commands and the execution of the command similar to the other techniques described in this section. However, the delay will



$$\tau = T_0 + T_1 - T_2 = \frac{N_0 + \dfrac{N_1 + Q_1 - N_2 - Q_2}{1000}}{F_0}$$

$$F_B + F_D = \frac{N_{(B+D)}}{\tau} = \frac{N_{(B+D)} \cdot F_0}{\left(N_0 + \dfrac{N_1 - N_2 \pm 1}{1000}\right)}$$

FIGURE 2-7 ANALOG TECHNIQUE FOR REDUCED QUANTIZATION ERROR.

not exceed one cycle of F_B+F_D or 1 micro-second for a nominal 1 MHz bias.

An additional delay in calculating the doppler shift results from the 1000 times stretching of the clock quantization interval. With the 1000 times expansion, the doppler shift cannot be calculated until up to 1000 clock periods have elapsed. This could be as high as 1 millisecond if a 1 MHz clock is employed. It is not necessary in the one way doppler extractor to use a 1000 fold stretching and 10 would suffice. Thus, the delay in making a doppler calculation would then only be 10 us for a 1 MHz clock.

2.2.2 JITTER ERROR REDUCTION

The phase jitter from the VCO output results in a random doppler count error which is inversely proportional to the averaging time and the S/N ratio in the phase lock loop bandwidth. Thus, the jitter error can be reduced by increasing the S/N ratio (higher received power or lower receiver noise) and/or increasing the averaging time. Increasing the averaging time has the added advantage of reducing the quantization error, however, other total system errors may make it desirable to have short averaging times. This section is thus mainly concerned with the impact of methods to increase the receiver S/N ratio.

From the receiver design standpoint, the S/N ratio can be improved by decreasing either the receiver bandwidth or noise figure (noise temperature). Assuming the latter has been designed to its lowest practical limit, the bandwidth is the only receiver parameter which can be used to increase the S/N ratio. Since the receiver need only extract the carrier frequency (as far as doppler measurements are concerned), the receiver bandwidth could be made arbitrarily small if vehicle motion is uniform. Since doppler rates are expected, a minimum r receiver bandwidth is required to allow the PLL to maintain lock on the signal. Trade-off discussions of this minimum bandwidth are discussed in detail under Receiver Design Considerations (Section 3.1) and under System Trade-offs and Optimizations (Section 4.0).

The other parameters that can be varied to increase the S/N ratio (transmitter power and antenna gains) involve trade-offs in cost and complexity. Also, the reduction of jitter error must be weighed against other errors such as quantization and frequency drift errors.

SECTION 3

IMPLEMENTATION CONSIDERATIONS

3.1 RECEIVER DESIGN CONSIDERATIONS

An analysis of S/N levels and phase-lock loop bandwidths was conducted to determine receiver parameter requirements (bandwidth, acquisition time, tracking errors). Table 3-1 shows the link analysis and resultant signal-to-noise ratio for a typical S-band receiver. For this analysis it was assumed that the satellite was at a maximum range of 1000 nmi. ($2X10^6$ meters). This corresponds to a satellite at zero degrees elevation for a 100 nmi. orbit, or 5^o elevation for a 300 nmi. orbit. The other link parameters are actual values used in other analyses (e.g. an RCA Study Reference 7), or are USB equipment parameters (reference 6). The modulation loss (LM) is discussed in Section 3.1.3.

For the particular receiver of Table 3-1, the S/N level is seen to be 45 dB. This receiver has a threshold noise bandwidth of 800 Hz (USB parameter) and a bandwidth of 3000 Hz at a high S/N ratio. If a special receiver were built for the one-way doppler extractor, a different value of receiver bandwidth may be desirable. Narrower bandwidths increase the S/N ratio but will require longer acquisition times. Furthermore, there is a minimum bandwidth which will allow accurate tracking through the high doppler rate region.

3.1.1 DOPPLER LIMITS AND RATES

The receiver must be designed to acquire and track the transmitter signal under all practical circumstances. In particular, during acquisition the receiver must be designed to rapidly acquire the signal, even when the received frequency is at maximum off-set (doppler limit) and changing at a maximum rate (doppler rate). The receiver must also track the signal accurately in the region of maximum doppler rate. The maximum frequency off-set (for the acquisition analysis) is twice the maximum doppler limit ($\pm$ 60 kHz, reference SOW) plus possible frequency drifts. The maximum doppler rate

TABLE 3-1 LINK ANALYSIS (Range = 1,000 nmi.) (2000 km)

*TX Power	(P_t)	10	dBW
*TX Ant. Gain	(G_t)	43.5	dB
TX Losses	(L_t)	2	dB
Space Loss	(L_s)	164.4	dB
Polarization Loss	(L_p)	2	dB
Power at RX Ant.	(P_r)	-114.9	dBW
RX Ant Gain	(G_r)	10	dB
RX Losses	(L_r)	5	dB
Modulation Loss	(J_m)	7	dB
**Noise Figure/Temp.	(NF/t_0)	8	dB/1540^{ok}
**IF Bandwidth	(B_{IF})	16	kHz
**Loop Bandwidth (High S/N)	2 B_L	3000	Hz
Noise Power	(N)	-161.9	dBW
Loop S/N	$(S/N)_L$	45	dB
Min, Allowable Sweep Rate (=2 $\dot{F}_d$) ($\Delta \dot{F}$)		8000 Hz/Sec	

* From Technical Discussions with NASA Personnel

** USB Data

is $\pm$ 4000 Hz/sec also derived from the SOW.

3.1.2 ACQUISITION AND TRACKING LIMITS

The analysis used the parameter values of Table 3-1 with the loop threshold bandwidth as an independent variable. At a loop S/N ratio of 20 dB or more, the actual loop bandwidth is approximately 3 to 5 times the threshold bandwidth. Figure 3-1 shows the results of the analysis. The maximum acquisition time is inversely proportional to the threshold bandwidths. To determine the minimum bandwidth requirements it was assumed that the VCO was swept through a 200 kHz band at a rate of

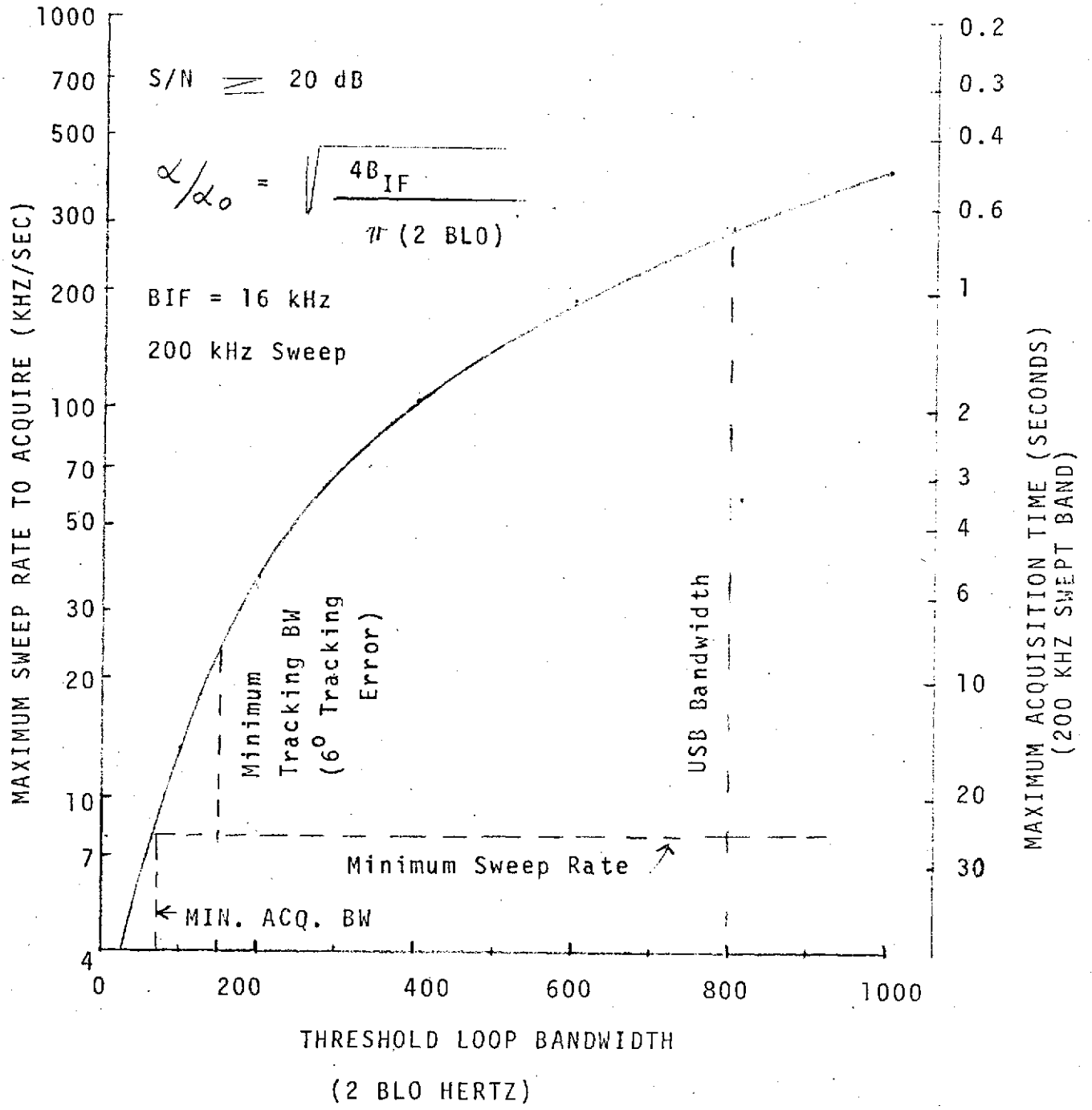


FIGURE 3.1 MINIMUM RECEIVER BANDWIDTH REQUIREMENTS

one-half the 90% probability of lock-on value (this value is suggested by Gardner in reference 9). This sweep rate depends on the threshold loop bandwidth through the expression:

$$\Delta \dot{F} \quad MAX = \left(\frac{1}{2}\right) \left\{ \frac{1-(S/N)L^{-1/2}}{2} \right\} (2\ B_{LO})^2\ (\alpha/\alpha_0)$$

where $2\ B_{LO}$ = threshold loop bandwidth.

α, α_0 = Limiter suppression factors at threshold and high S/N ratio.

With a high S/N level, this formula reduces to

$$\Delta \dot{F} \leq .08\ (2B_{LO})^2 \sqrt{\frac{4\ BIF}{\pi(2\ BLO)}}$$

BIF = IF Bandwidth prior to limiter.

The minimum sweep rate is determined by the maximum doppler rate expected since the sweep must be able to catch up to the signal. For this analysis, the minimum sweep rate is assumed to be twice the maximum doppler rate (4 kHz/sec. for an acceleration of 610 meters/sec.). The minimum sweep rate is then 8 kHz/sec.

Putting this value of sweep rate into the above equation results in a minimum acquisition bandwidth of 70 Hz and an acquisition time of almost 40 seconds. However, acquisition times of 1 or 2 seconds or less would be desirable. Thus, from the figure it is seen that the minimum bandwidth should not be less than 400 Hz for an acquisition time of 2 seconds.

The minimum allowable tracking bandwidth depends on the desired tracking error during the high doppler rate region. From formulas given in Reference 9, this minimum bandwidth can be derived as:

$$(2\ B_{LO})_{Min.} \geq \sqrt{\frac{2\pi \dot{f}_d}{\theta_a\ (\alpha/\alpha_0)}}$$

where $\dot{f}_d$ = max. doppler rate

α/α_0 = signal suppression ratio of the limiter

θ_a = tracking error for the loop

at high S/N ratio $\alpha/\alpha_0 = \sqrt{\frac{4 \cdot BIF}{(2\ BLO)}} = \sqrt{\frac{20,000}{(2\ BLO)}}$

for the receiver characteristics of Table 3-1. Thus, if the tracking error is desired to be less than .1 radians, then the minimum loop threshold tracking bandwidth must be at least 150 Hz.

The 70 Hz acquisition and 150 Hz tracking bandwidths are minimum values. Wider bandwidths would be desirable for both low tracking error and fast acquisition. The 800 Hz bandwidth of the present S-band transponders would provide a maximum acquisition of time of 0.7 second and a tracking error no larger than 0.01 radians ($.6^{o}$).

3.1.3 MODULATION EFFECTS

Since modulation is expected to be present on the carrier frequency, the receiver must be designed to extract a carrier reference frequency for the doppler extractor circuits. Assuming phase modulation, two techniques are generally used to extract the carrier reference. Each of these methods results in a loss of S/N ratio in the receiver loop bandwidth (this S/N loss is based on the link analysis assumption that all of the transmitter power is devoted to the carrier frequency).

The first technique uses a suppressed carrier from the transmitter to supply the receiver with a reference frequency. Using this technique the receiver can lock to the carrier reference, using a simple phase lock loop as shown in the block diagram of Figure 3-2. In order for the transmitter to devote as much power as possible to the sidebands, the transmitted carrier reference is suppressed by as much as 10 dB. As a result the receiver loop S/N ratio is reduced by the same 10 dB.

In addition to this loss, the modulation will cause sideband frequencies to be present which may increase the noise in the loop bandwidth and may also cause false locks to occur. The sideband noise in the loop bandwidth can be eliminated by using high repetition rate digital modulation (phase shift, frequency shift). This will displace the side lobe spectral lines outside

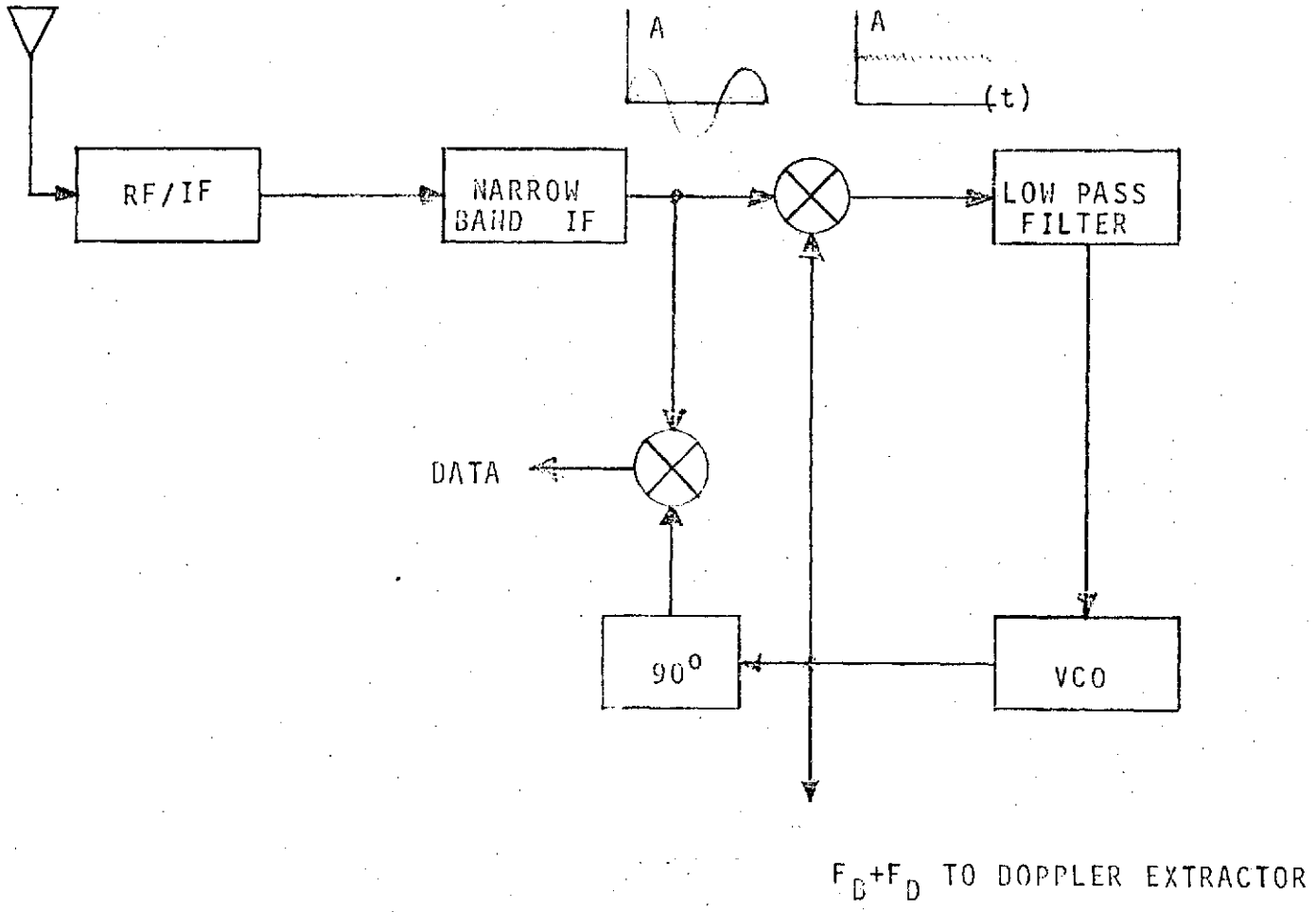


FIGURE 3-2 BLOCK DIAGRAM OF A RECEIVER USING RESIDUAL CARRIER AS A REFERENCE FREQUENCY.

the loop bandwidth when carrier lock is achieved. For this to occur, the repetition rate should be much greater than the strong signal loop bandwidth. This is generally the case for high speed digital communications so that the noise contributed by sideband energy is expected to be negligible. False locks can also be reduced by employing high repetition rates and allowing the VCO to sweep only in the vicinity of the expected carrier frequency.

A second technique to extract a carrier reference frequency, when bi-phase or quadra-phase modulation is employed, is to use a squaring loop or Costas loop. For quadra-phase modulation two square law devices would be used to quadruple the IF frequency or a dual Costas loop would be used. A receiver block diagram that extracts a carrier from bi-phase modulated signals, using the squaring loop, is shown in Figure 3-3. For similar modulation, Figure 3-4 shows a receiver which uses a Costas loop.

The main advantage to using a squaring loop or Costas loop is that the sidelobe information is removed leaving only a carrier reference frequency into the phase detector. Thus, no sidelobe signals will be present into the phase detector, resulting in less noise in the loop filter. Also, since no sidelobes are present the VCO cannot falsely lock on to a sidelobe frequency. Both of these loops have similar effects on the extracted carrier so that only the simpler squaring loop receiver will be discussed.

The transmitter suppresses the carrier frequency to a high degree resulting in primarily sideband information being transmitted. The square law device strips away the modulation resulting in a carrier reference frequency at twice the input IF frequency. As a result of the squaring device the loop S/N ratio is reduced by 6 dB. Other losses resulting from phase noise and the use of narrow band filters accumulate to less than one dB.

In the link analysis shown in Table 3-1 the effect of modulation was accounted for by assuming a total modulation loss of 7 dB. This assumes that either a squaring loop or Costas loop is

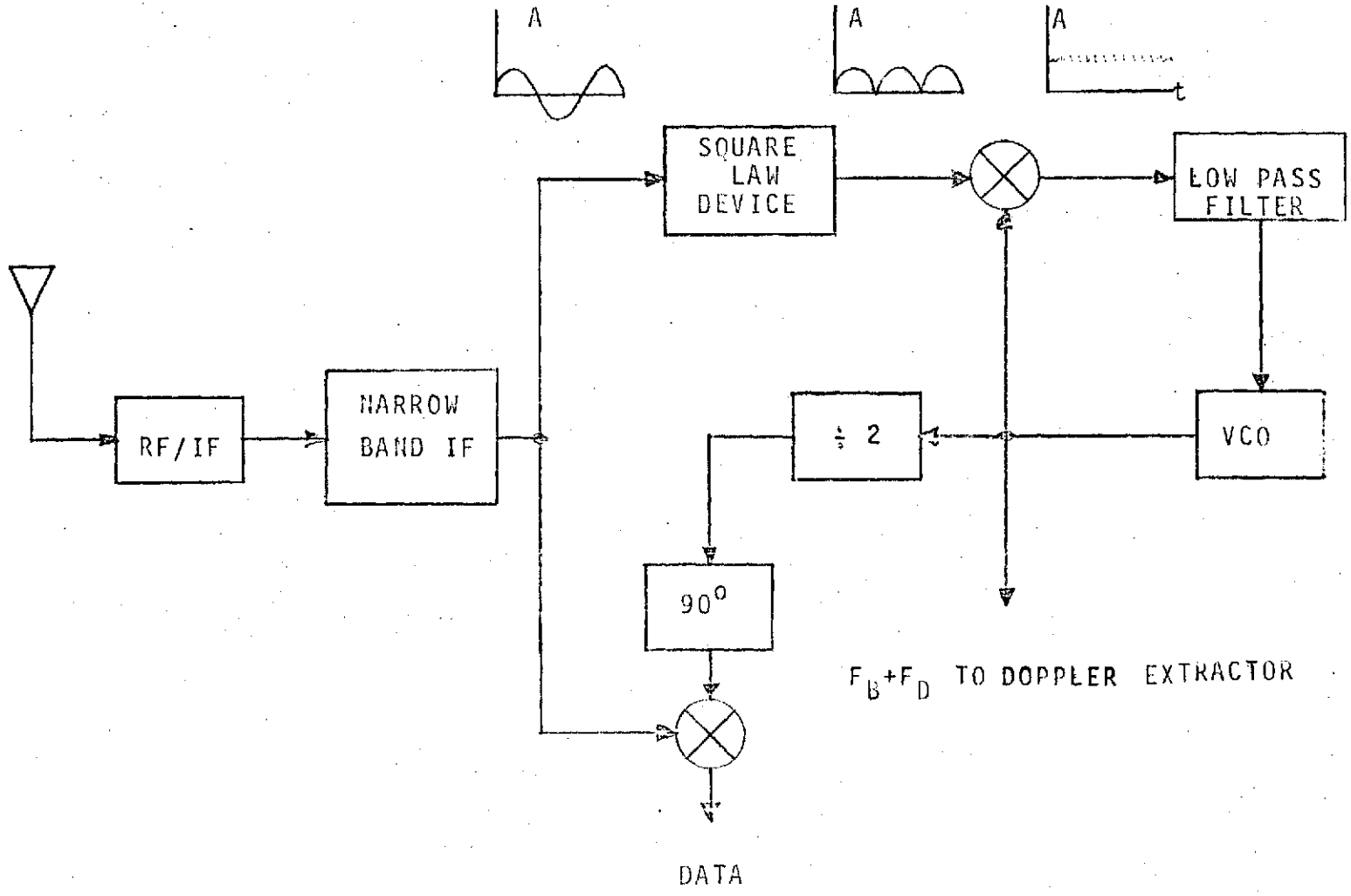


FIGURE 3-3 BLOCK DIAGRAM OF A CARRIER EXTRACTION RECEIVER USING A SQUARING DEVICE

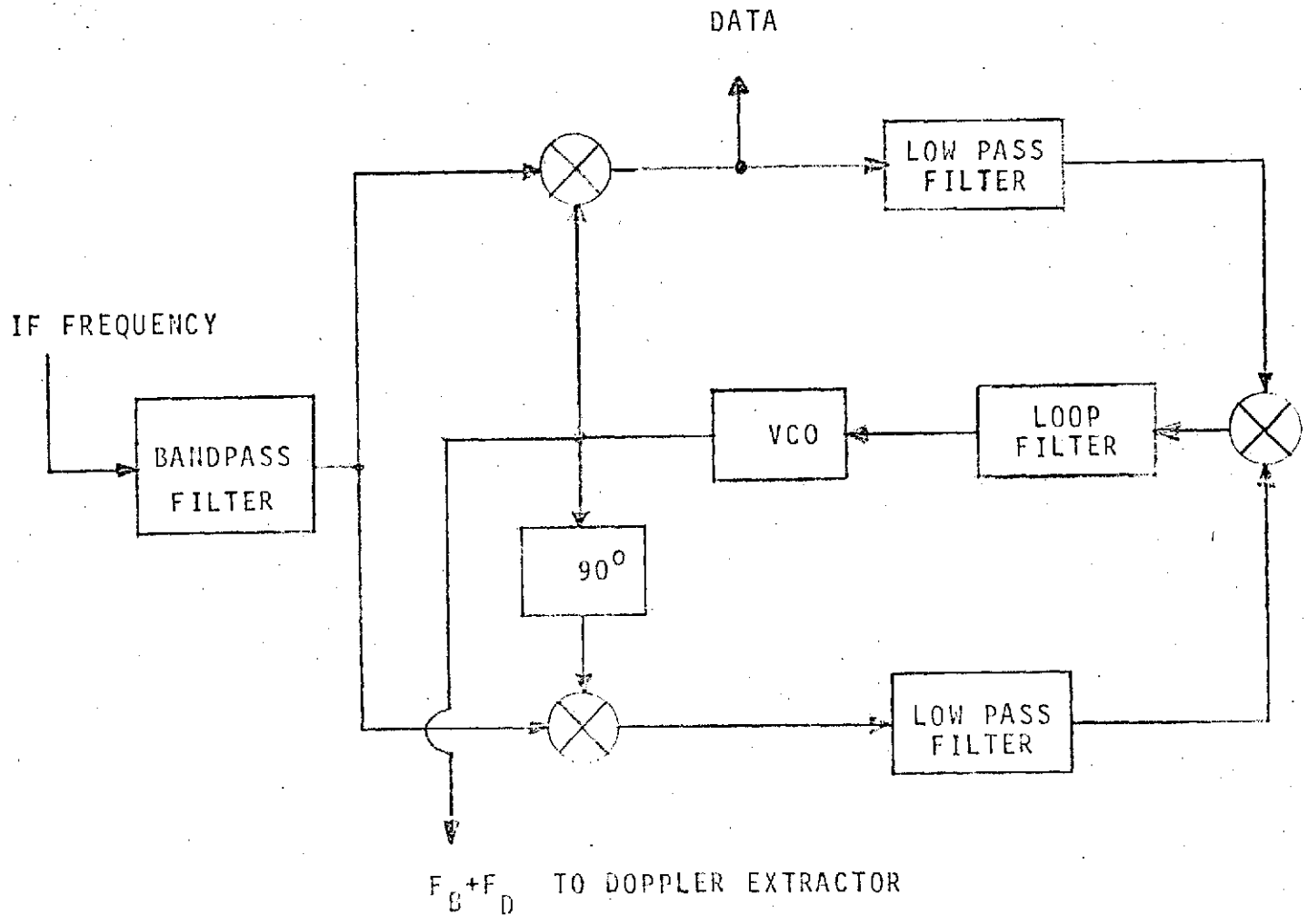


FIGURE 3-4 BLOCK DIAGRAM OF A CARRIER EXTRACTION RECEIVER USING A COSTAS LOOP

employed to extract the carrier or else a conventional PLL is employed with a carrier that is suppressed by no more than 7 dB.

3.1.4 OPTIONAL CARRIER FREQUENCY ACQUISITION TECHNIQUES

The present S-band transponders rely on passive acquisition in that the ground transmitter sweeps in frequency until a signal is received from the orbiting vehicle that acquisition is complete. This method has several disadvantages. The technique requires that two way communication is established before acquisition can be completed and it is difficult for more than one user to acquire and track the same transmitter. Further, if the receiver breaks lock or falsely locks to a sidelobe signal, two way communication must be re-established to repeat the acquisition phase.

A more attractive technique is to fix the ground transmitter frequency and provide for self acquisition in the S-band receiver. The receiver could have its own oscillator sweep in frequency and have means for detecting break lock or false locks. If these occur, the receiver can immediately revert to the acquisition phase without ground station cooperation. Further, many receivers could acquire and lock to the transmitter frequency without disturbing other communication links.

Two techniques are available for receiver acquisition of a stable transmitter frequency, namely; coherent and non-coherent acquisition. Coherent acquisition is the technique of sweeping the PLL oscillator. When the signal is present in the loop bandwidth, the PLL automatically acquires the signal, due to its feedback circuits, and the sweep is removed. For a given loop bandwidth there are maximum limits to the sweep rate which can be applied and still allow the PLL to automatically acquire the signal. This is the technique described briefly in section 3.1.2 where it was shown that acquisition could require several seconds to complete. Non-coherent acquisition time can be significantly less than this, especially for receiver bandwidths below one kilo-hertz and at high S/N ratio.

3.1.4.1 Non-Coherent Acquisition

Non-coherent acquisition is a technique of scanning the frequency band with a narrow bandwidth filter measuring the energy output and stopping the sweep when a desired energy threshold is achieved.

High sweep rates can be achieved by this technique. However, for a given filter bandwidth and signal power level, the faster the sweep, the lower is the signal energy that is coupled to the energy detector circuits. The energy loss, relative to a zero sweep rate, is dependent on the sweep rate and the filter bandwidth as shown in Figure 3-5.

From this figure it would appear that a wide bandwidth is desirable since this would result in the least amount of energy loss. However, as the bandwidth is increased the noise level increases.

Although the sweep loss decreases as the bandwidth is increased, if the bandwidth is sufficiently high the improvement in sweep loss becomes negligible compared to the increase in noise. Thus, for a given sweep rate, an optimum filter bandwidth exists which maximizes the swept S/N ratio into the energy detector. This optimum filter bandwidth is shown in Figure 3-6. In this figure signal power requirements are plotted against receiver bandwidth and acquisition times (inverse of the sweep rate) for constant S/N ratio into the detector. Figure 3-6 shows that in order to acquire in 0.1 seconds (2 MHz/sec sweep over 200 kHz band), a bandwidth of about 1 kHz makes optimum use of the available signal power. For other acquisition times, the optimum bandwidth can be selected from the figure by referring to the line of minimum power.

In order for the phase lock loop to lock to the signal, the sweep is stopped at the frequency of highest energy (or some similar other criteria). The PLL will be pulled into lock if its bandwidth is not too narrow relative to the sweep bandwidths. Assuming the VCO frequency, when sweep is stopped, does not differ from the signal frequency by more than the swept bandwidth, then the PLL pull in time will depend on the sweep bandwidth as shown in Figure 3-7.

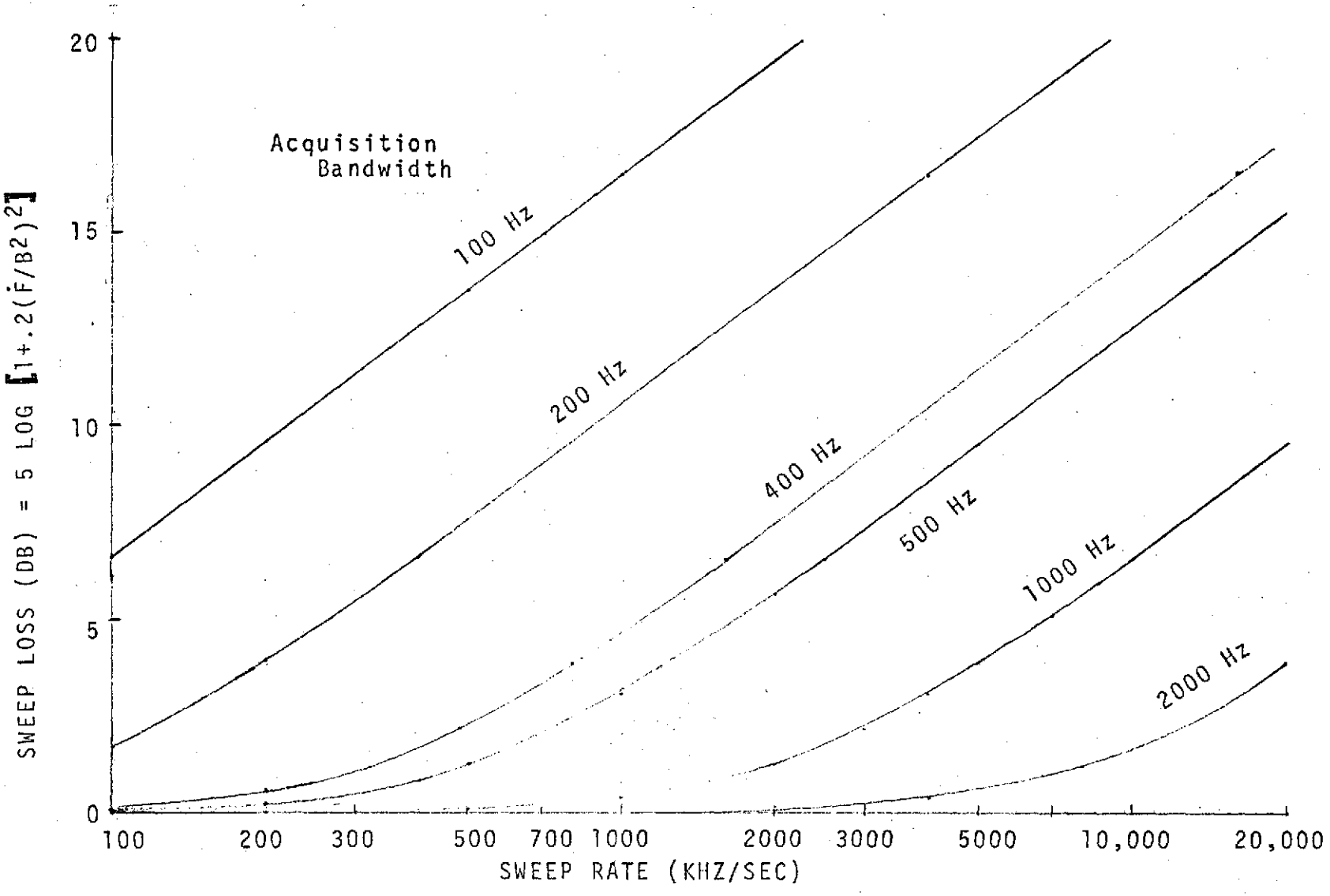


FIGURE 3-5 VARIATION OF SWEEP LOSS WITH SWEEP RATE & RECEIVER BANDWIDTH

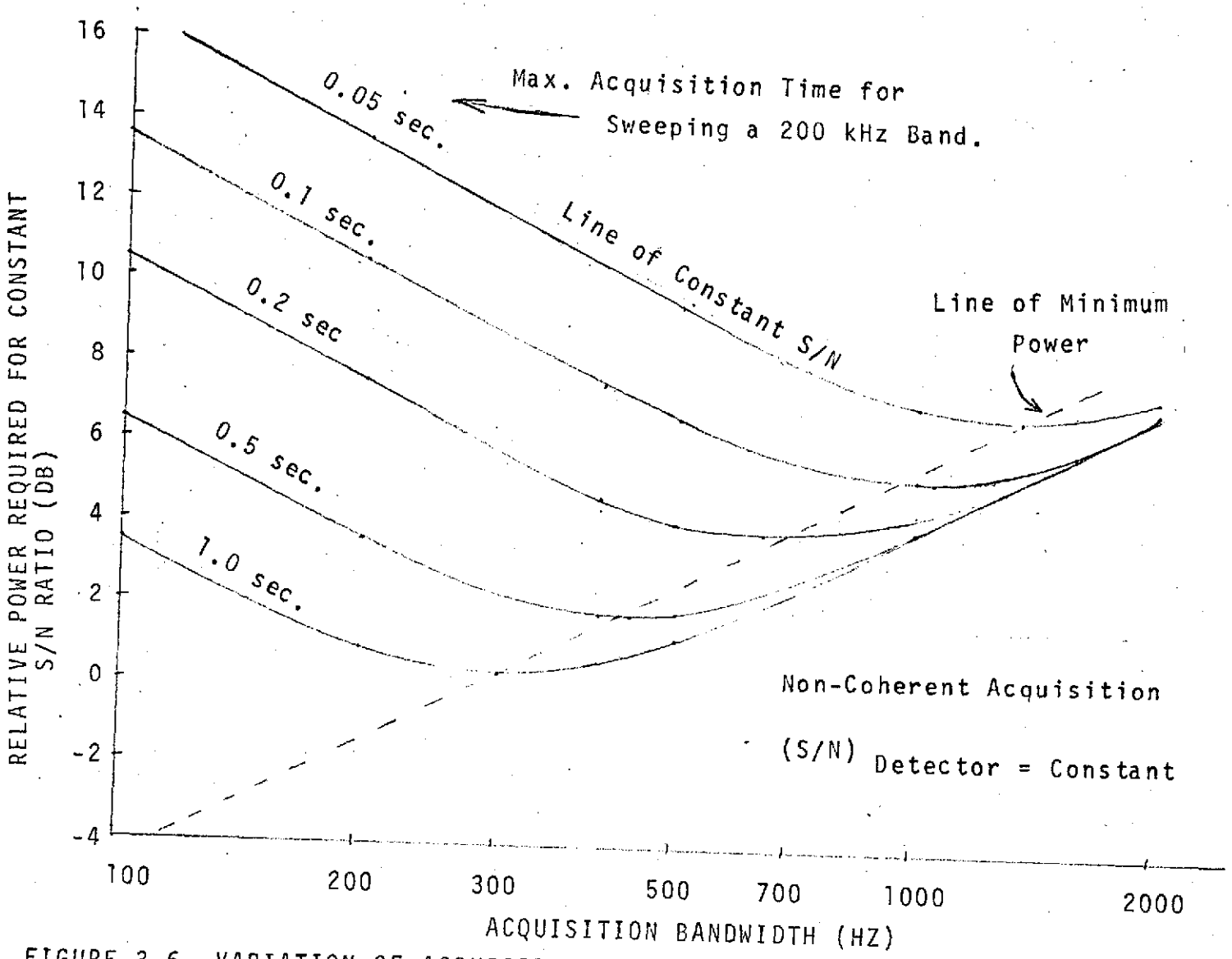


FIGURE 3-6 VARIATION OF ACQUISITION TIME WITH TRANSMITTED POWER AND RECEIVER BANDWIDTH

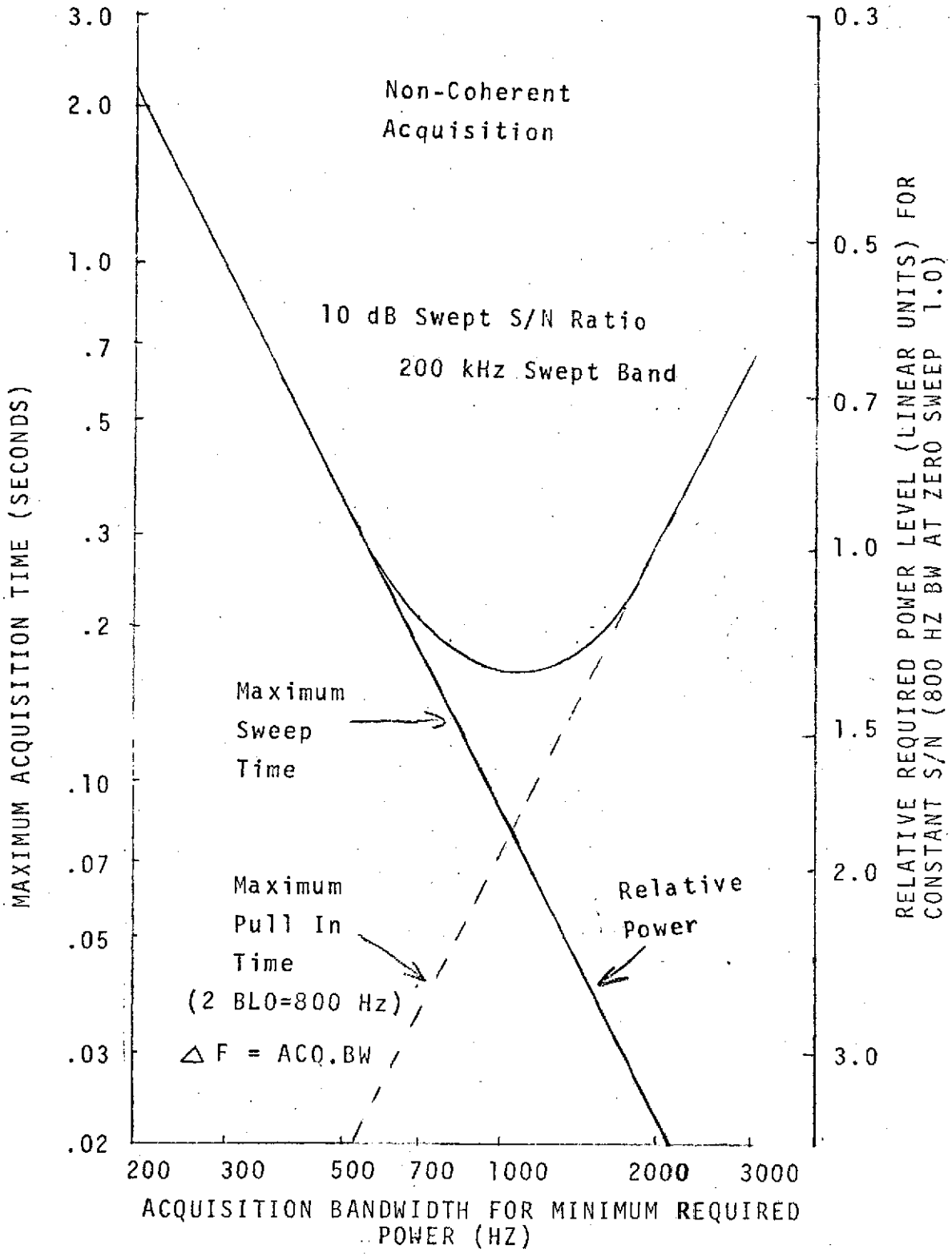


FIGURE 3-7 SENSITIVITY OF ACQUISITION TIME TO OPTIMUM RECEIVER BANDWIDTH

Since the pull in time increases as the sweep bandwidth increases (high $\triangle F$ uncertainty when VCO sweep is stopped) but the time to sweep the total band (200 kHz) decreases, there is an optimum sweep bandwidth that minimizes the total acquisition time. For the assumptions made (S/N = 10 dB, ζ = 0.5, swept bandwidth = 200 kHz, tracking bandwidth = 800 Hz) the optimum sweep bandwidth is about 1 kHz, resulting in a total acquisition time $\prec$ 0.2 seconds. At higher S/N ratios the acquisition time would be less than this value. Also, use of a higher PLL threshold bandwidth would result in acquisition times smaller than the above value.

3.1.4.2 Coherent Acquisition

Coherent acquisition was described briefly in section 3.1.2 assuming the received high signal to noise level shown in Table 3-1. This section expands on that analysis to include the effects of S/N ratio on the sweep rate and develops a trade-off of sweep rate (or acquisition time) for transmitter power requirements for direct comparison with non-coherent acquisition.

Coherent acquisition is the technique of sweeping the VCO frequency and allowing the phase lock loop to automatically acquire and track the signal. As in section 3.1.2, the maximum allowable sweep rate is assumed to be half of the desired rate for 90% probability of acquisition. That is:

$$\dot{F}_{max} \leq \frac{1}{4\pi}\left(1 - \frac{1}{\sqrt{S/N}}\right)\frac{\alpha}{\alpha_0}(2B_{LO})^2$$

Figure 3-8 shows the resultant acquisition times (200 kHz swept band) as a function of receiver threshold bandwidth, S/N level and transmitter power. From the figure it can be seen that the acquisition time is not very sensitive to S/N ratio (100 fold increase in signal level results in one third the acquisition time) but is sensitive to receiver bandwidth (doubling the bandwidth reduces acquisition time by a factor of three). Also, for a given acquisition time the transmitter power requirement is minimized at a S/N ratio of 10 dB.

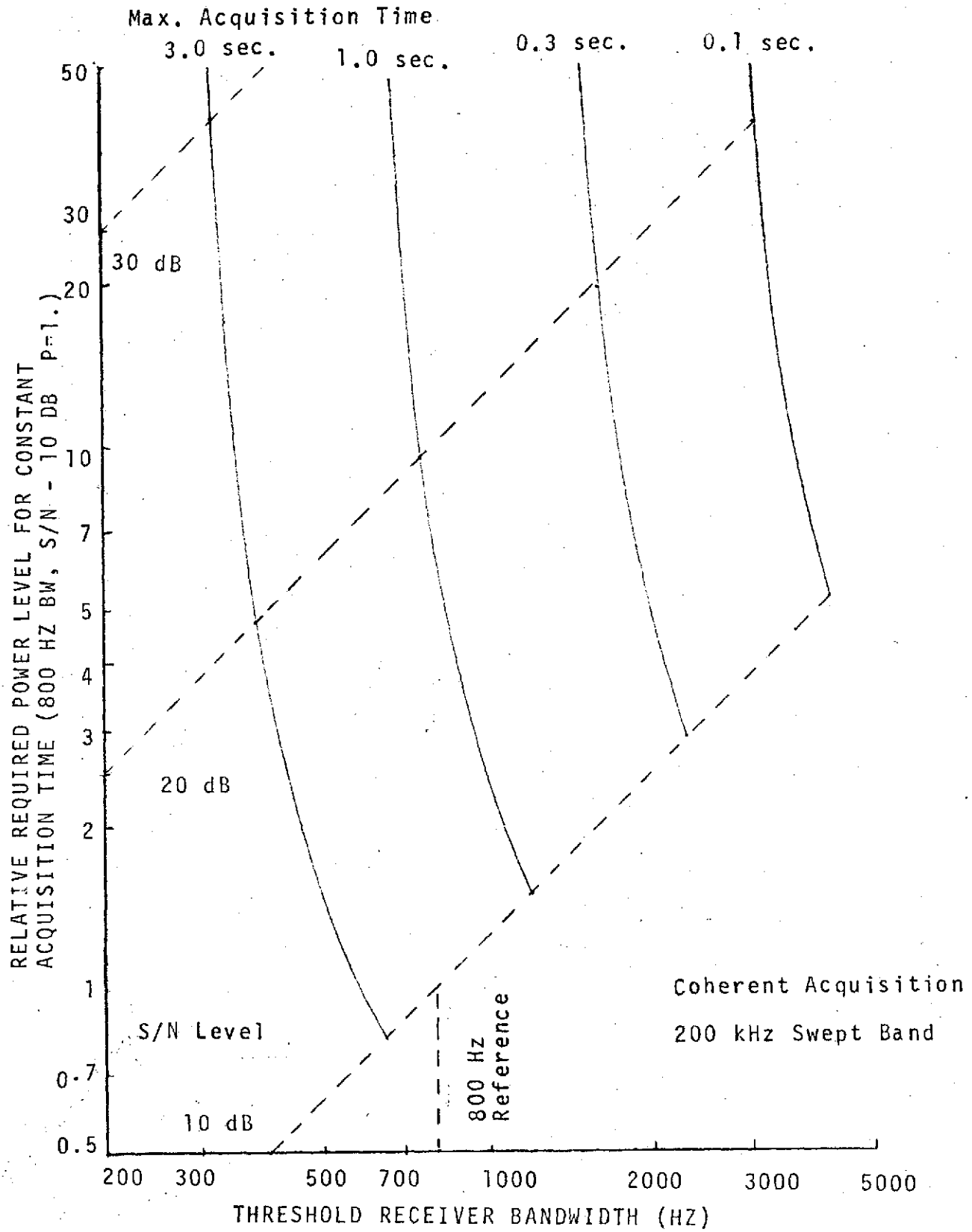


FIGURE 3-8 SENSITIVITY OF ACQUISITION TIME TO RECEIVER BANDWIDTH & S/N RATIO

Thus, during acquisition, the receiver bandwidth should be as wide as possible to produce a 10 dB signal to noise ratio in the loop.

Figure 3-9 shows the resultant acquisition times and relative transmitter power levels when the receiver bandwidth is maximized as defined above. The results show that the receiver bandwidth should exceed 1 kHz for coherent acquisition times less than one second.

Figure 3-10 compares the coherent and non-coherent acquisition times in terms receiver bandwidth and transmitter power requirements. The curves show for equivalent power requirements, the non-coherent technique acquires in about one-tenth the time for acquisition bandwidths of 1 kHz or less.

3.1.5 RECEIVER REQUIREMENTS

The results of this section have defined the following receiver parameters.

(1) Receiver tracking bandwidth

Threshold bandwidth should be no less than 150 Hz in order to track during the high doppler rate region. Higher bandwidths would be desirable both for tracking accuracy and acquisition.

(2) Acquisition bandwidth

In order to acquire the signal in a fraction of a second, it is necessary that the acquisition threshold bandwidth should also be above 300 hertz for non-coherent acquisition and above 1 kHz for coherent acquisition.

The above requirements are minimum values. Wider bandwidths would be desirable for both faster acquisition and accurate tracking of the signal. The S-band transponder, with its 800 Hz threshold bandwidth and 3,000 Hz strong signal bandwidth easily meets the minimum requirements. If VCO sweep is applied to this receiver, and non-coherent acquisition is employed, (with a 1,000 Hz bandwidth) it could acquire the carrier frequency in a few tenths of a second. For coherent acquisition the maximum acquisition time would be nearly 2 seconds

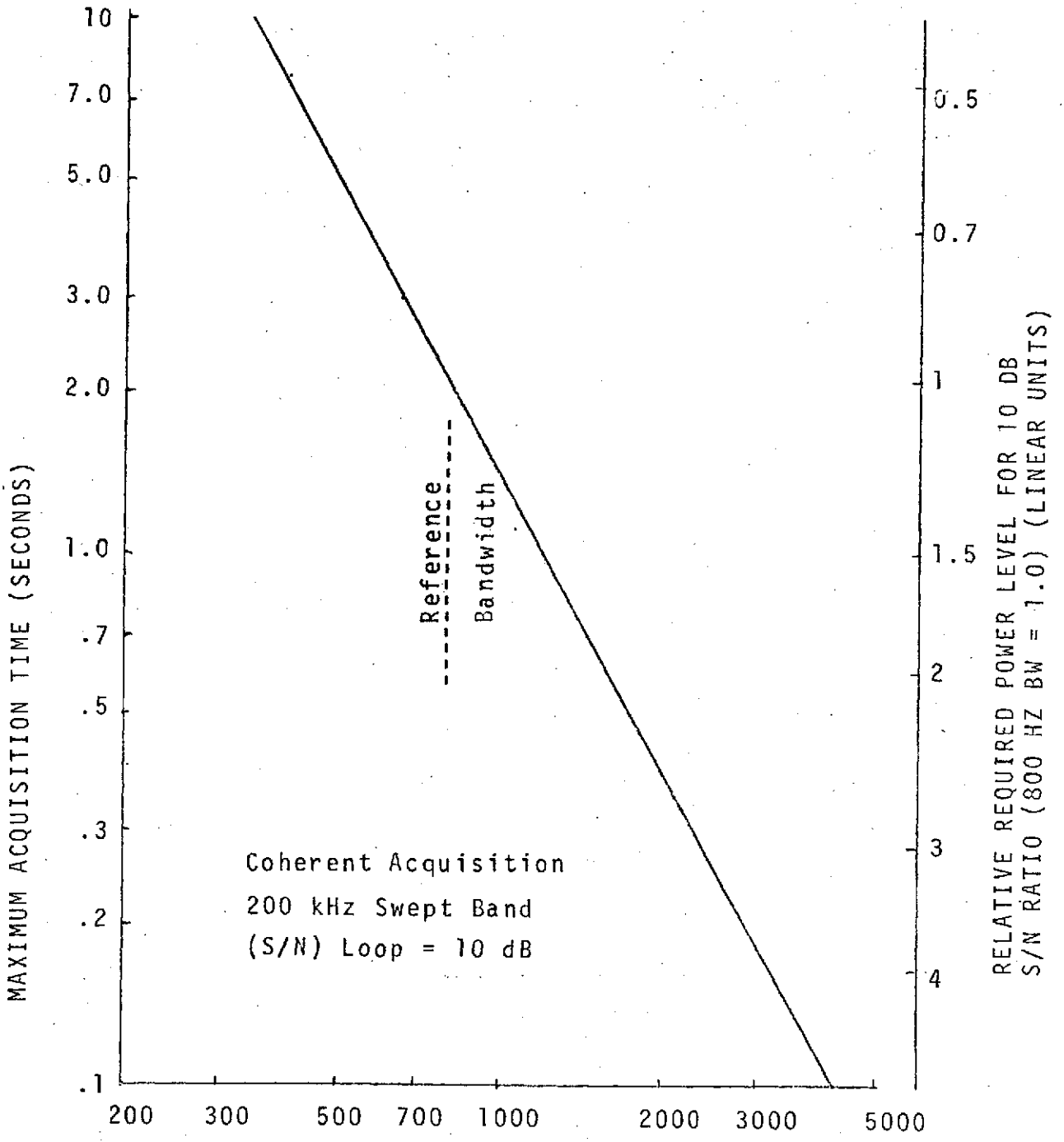


FIGURE 3-9 SENSITIVITY OF ACQUISITION TIME TO RECEIVER BANDWIDTH FOR LEAST TRANSMITTER POWER

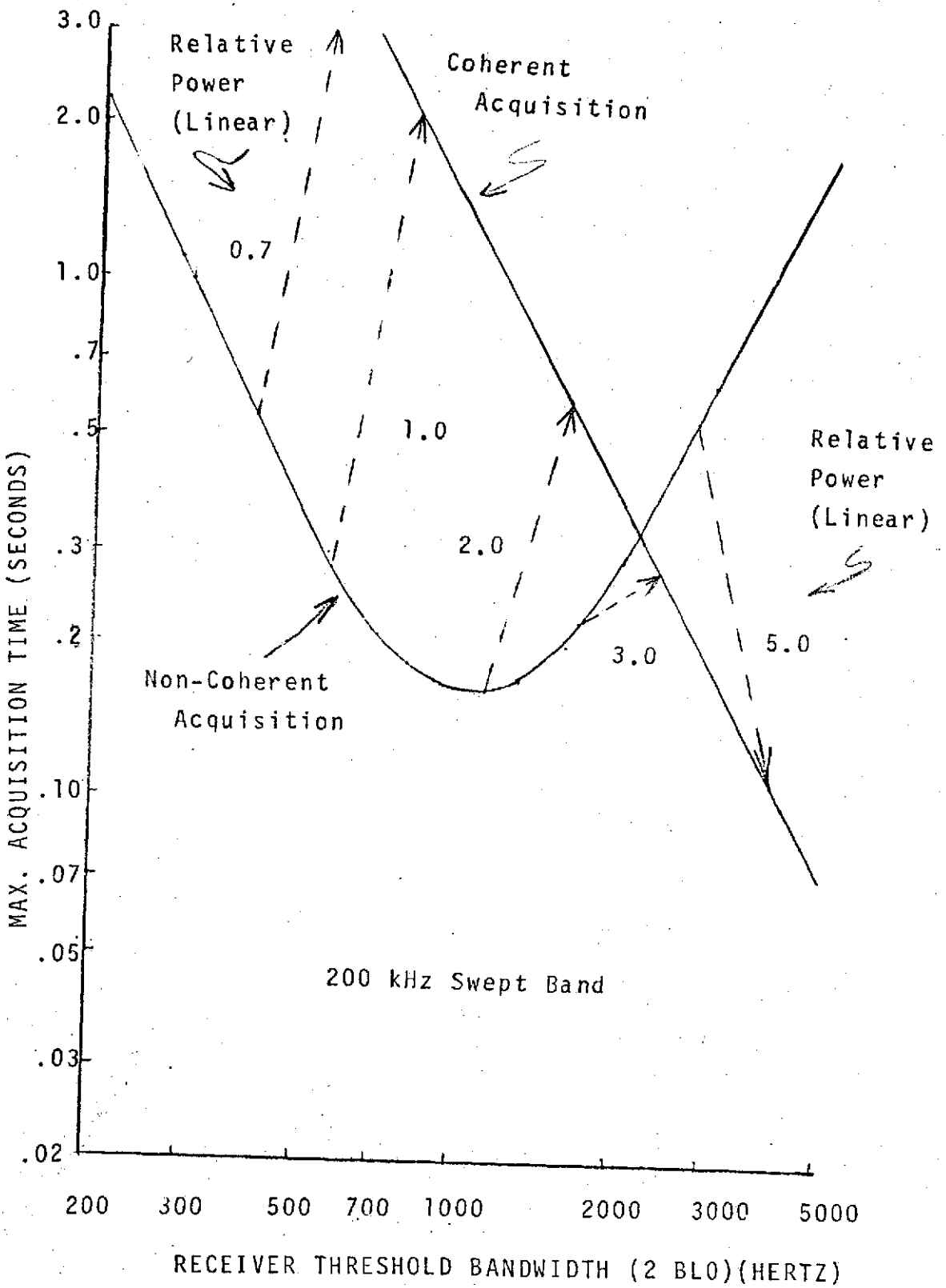


FIGURE 3-10 COMPARISON OF COHERENT AND NON-COHERENT ACQUISITION FOR EQUAL SIGNAL LEVELS

(since acquisition bandwidth would be 800 Hz). To reduce the coherent acquisition time to a few tenths of a second, the S-band transponder acquisition bandwidth would need to be increased above 2,000 Hz.

SECTION 4

SYSTEM TRADE-OFFS AND OPTIMIZATIONS

4.1 SYSTEM SELECTION CRITERIA

A shuttle doppler navigation system requires the use of high performance, low weight systems for the extraction of doppler information. The doppler extraction system most desirable for shuttle applications is one which can meet the performance requirements at least cost, weight, size and power consumption. The system should also be reliable in meeting the performance requirements under all expected conditions of velocity, acceleration and environmental factors.

The overall system accuracy is considered the prime performance measure for the candidate systems. From the Statement of Work (SOW) the required accuracy is (0.1 ft/sec) random error for 2 or more seconds of integration time and 30 cm/sec (0.98 ft/sec) maximum bias error per day. As a minimum the accuracy of the candidate systems will meet these requirements. Thus, the criteria for system selection will be to select the candidate system which can achieve the above accuracy requirements without sacrificing cost, weight, size or reliability.

4.2 CANDIDATE SYSTEMS

This section of the report describes various techniques to acquire, track and measure the doppler shifted carrier signal. The options involve various levels of cost and complexity but with resultant improvements in system performance. The candidate systems are divided into three classes of options that deal with specific and generally independent components of the total doppler extraction system. Three classes are, 1. Receiver options, 2. Quantization resolver options, and 3. Reference oscillator options. The following paragraphs discuss these options and their impact on the total system operation.

The data demodulation function of the receiver is not considered in the following discussions since it does not impact directly on the doppler extraction process. It is assumed that a phase lock loop receiver will be employed to remove the modulation and extract a carrier reference for injection into the doppler extractor.

4.2.1 RECEIVER OPTIONS

The requirements on the S-Band receiver are to accurately track the transmitter signal and supply highly accurate doppler signals to the doppler extractor. To achieve this goal, three receiver options have been considered as candidates for the total doppler extractor system. These include:

(1) Using an unmodified 5 band transponder transmit port to derive a signal for the doppler extractor.

(2) Modifying the transponder to obtain a VCO signal for the extractor,

(3) Designing a new receiver to optimize doppler extraction performance and carrier frequency acquisition.

Each of these three possibilities are discussed in the following sections.

4.2.1.1 Doppler Signal Obtained From S-Band Transponder Transmit Port

A technique for obtaining full doppler from the S-Band transponder would be to use the transmit port. A method for obtaining a doppler signal is shown in Figure 4-1. Since the S-Band signal into the doppler extractor could have down link data modulation present, a Costas loop (or similar demodulation circuit) would be necessary to extract the carrier reference frequency. Full doppler is obtained by using fixed reference oscillators for the mixer injection frequencies.

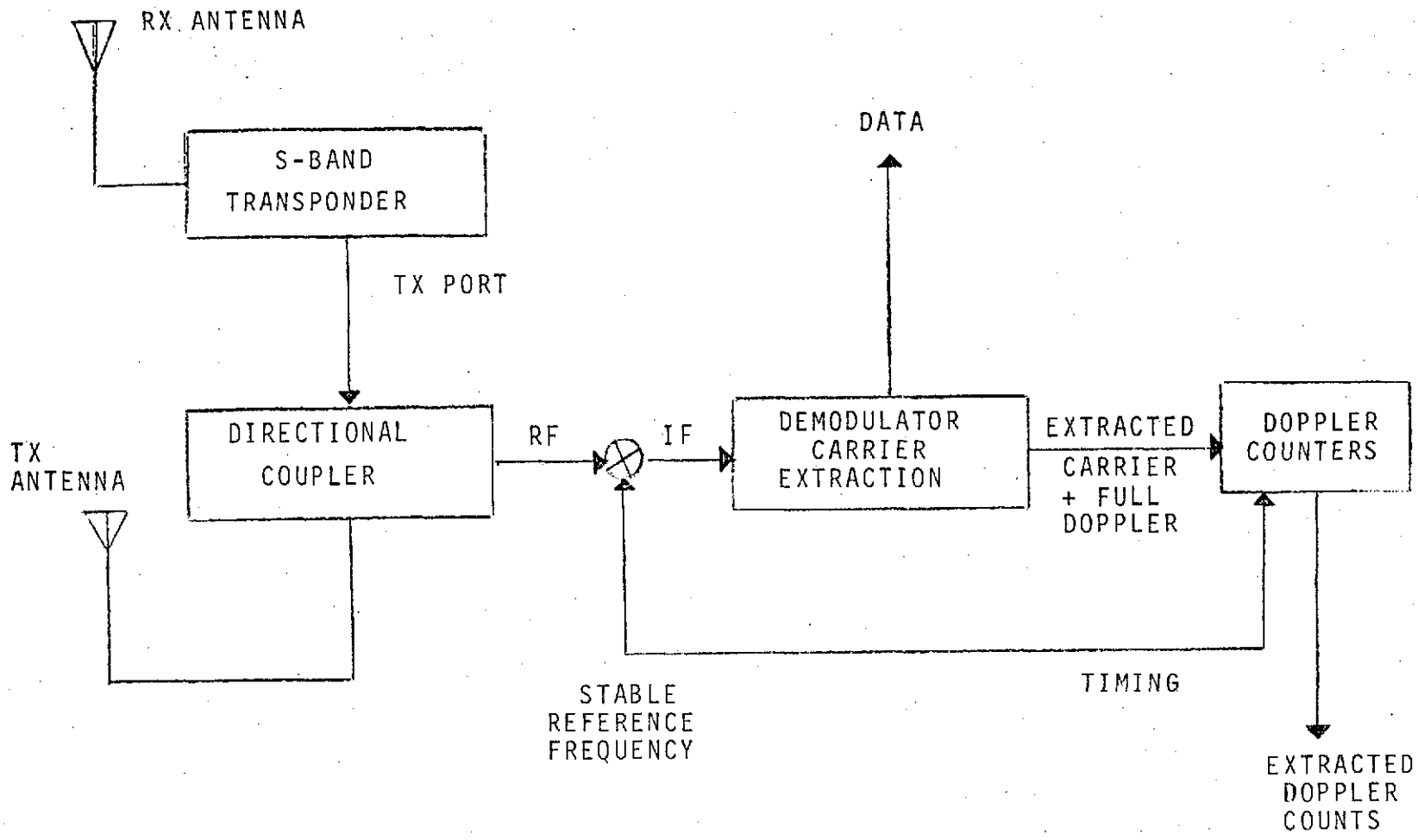


FIGURE 4-1 BLOCK DIAGRAM OF TECHNIQUE TO USE USB TRANSMIT PORT FOR DOPPLER EXTRACTION

Although full doppler is available to the counters, this technique has the disadvantage that the doppler extractor would contain an S-Band Receiver (including demodulators). This would make the extractor costly in both design and construction.

4.2.1.2 Doppler Signal Obtained from VCO Output

Figure 4-2 shows a block diagram of the S-Band transponder. The VCO output is available at a frequency of four times the VCO frequency (76.083 MHz), but only fractional doppler is available on this carrier. Since the S/N ratio from the VCO is high, frequency multipliers and mixers could be used to obtain full doppler on a low frequency carrier. Such a technique is outlined in Figure 4-3.

With this scheme, nearly full doppler can be obtained without employing demodulators and S-Band components. All frequencies are less than 100 MHz, allowing the use of lower cost, lower power and high reliability components in the doppler extractor.

4.2.1.3 New Receiver Designs

In order to achieve faster acquisition and higher accuracy doppler extraction, it may be desirable to design a new receiver optimized for doppler extraction. A new receiver could be designed to have a wide acquisition bandwidth and high VCO sweep rates. For an acquisition bandwidth of 5000 Hz, for example, the PLL could acquire the signal, coherently, in less than a tenth of a second. A new receiver could also be designed to acquire non-coherently, resulting in even faster acquisition times.

A new receiver could also be designed to achieve full doppler frequency or higher on the VCO output. This would simplify the circuits for the reduction of quantization error, since requirements for frequency multipliers and/or high frequency clocks would not be as critical.

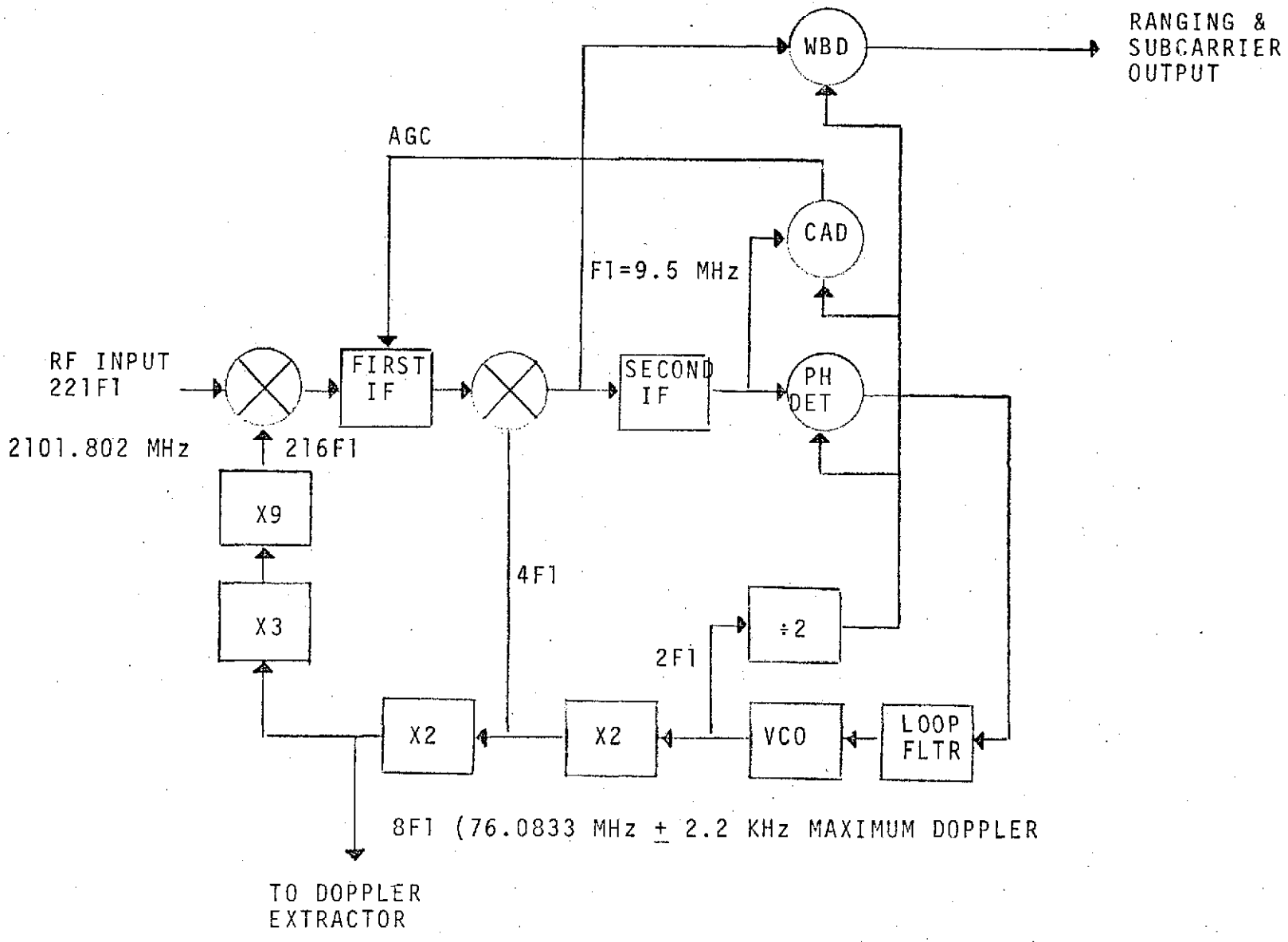


FIGURE 4-2 BLOCK DIAGRAM OF S-BAND TRANSPONDER

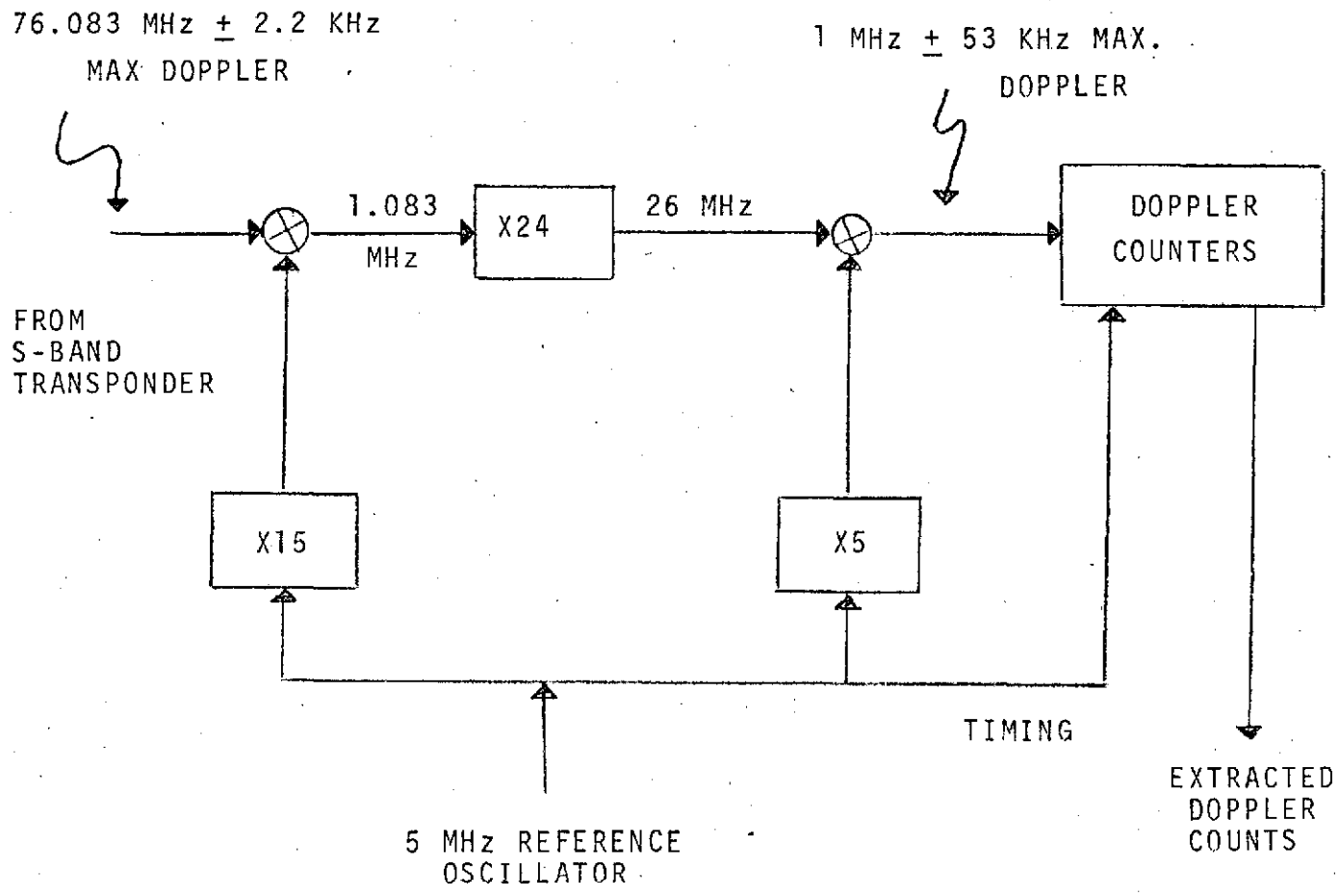


FIGURE 4-3 TECHNIQUE TO OBTAIN FULL DOPPLER FROM VCO OUTPUT

A new receiver could also be designed for multichannel operation, allowing selection of a clear channel by the user and allowing sequential tracking of several ground transmitters, on different frequencies, for triangulation measurements.

Four candidate receiver designs have been evaluated for this analysis. Each receiver design attempts to optimize one or more of the selection criteria parameters. Thus, System 1 attempts to minimize system cost, weight, and power requirements at the expense of system accuracy. Systems 2 and 3 trade-off low cost for increased accuracy. System 4 trades low cost and weight for increased utility.

The following pages discuss each system in detail and derives system trade-off data for each candidate.

4.2.1.3.1 System 1 Configuration

Shown in Figure 4.4 this system has a narrowband IF resulting from direct beating of a VCO harmonic with the RF signal. This receiver is relatively low cost but has the disadvantage that only a small fraction of the doppler frequency is injected into the extractor. This is representative of the Apollo USB receiver.

a. Frequency drift effects

$\Delta f_1 = f_1 S_1$; $\Delta F_o = F_o S_o$ $\quad$ S_o, S_1 = Random

$\Delta f_o = (f_d + S_1 f_1)/(N+1)$ $\quad$ Drift Factors

$$\dot{R} = \frac{(N+1)C}{f_1} \left[\frac{f_b + \Delta f_b}{1 + S_o} - f_b \right]$$

$$\dot{R} = \frac{(N+1)C}{f_1} \left[\Delta f_b - S_o (f_b + \Delta f_b) \right] \quad \text{SINCE } \frac{1}{1+S_o} = 1 - S_o$$

SINCE $\Delta f_b = (f_d + S_1 f_1)/(N+1) - F_o S_o$, THEN;

$$\dot{R} = \frac{(N+1)C}{f_1}\left[\frac{f_d}{N+1} + \frac{S_1 f_1}{N+1} + \frac{S_1 f_1}{N+1} - F_o S_o - S_o\left(f_b + \frac{f_d + S_1 f_1}{N+1} - F_o S_o\right)\right]$$

→ TRUE DOPPLER TERM

SINCE $f_b = f_o - f_o$, and $E_{\dot{R}} = \dot{R} - \dot{R}_{TRUE}$

$$\varepsilon_{\dot{R}} = \frac{(N+1)C}{f_1}\left[\frac{S_1 f_1}{N+1} - S_o f_o - \frac{S_o f_d + S_o S_1 f_1}{(N+1)} - F_o S_o^2\right] \quad (1)$$

$$E(\varepsilon_{\dot{R}}) = \frac{(N+1)C}{f_1} F_o S_o^2 < 10^{-11} \text{ FT/SEC} \quad 0$$

Neglecting 2nd Order Terms in S (Eq. 1)

$$\varepsilon_{\dot{R}} = \frac{(N+1)C}{f_1}\left[\frac{S_1 f_1}{N+1} - S_o f_o - \frac{S_o f_d}{N+1}\right]$$

$$\varepsilon_{\dot{R}} = C\left[S_1 - S_o \frac{(N+1)f_o}{f_1} - S_o \frac{f_d}{f_1}\right]$$

SINCE $(N+1)f_o = f_1$ and $f_d/f_1 << 1$

$$\varepsilon_{\dot{R}} = C\left[S_1 - S_o\right]$$

$$\varepsilon_{\dot{R}}^2 = C\left[S_1^2 + S_o^2 - 2 S_1 S_o\right]$$

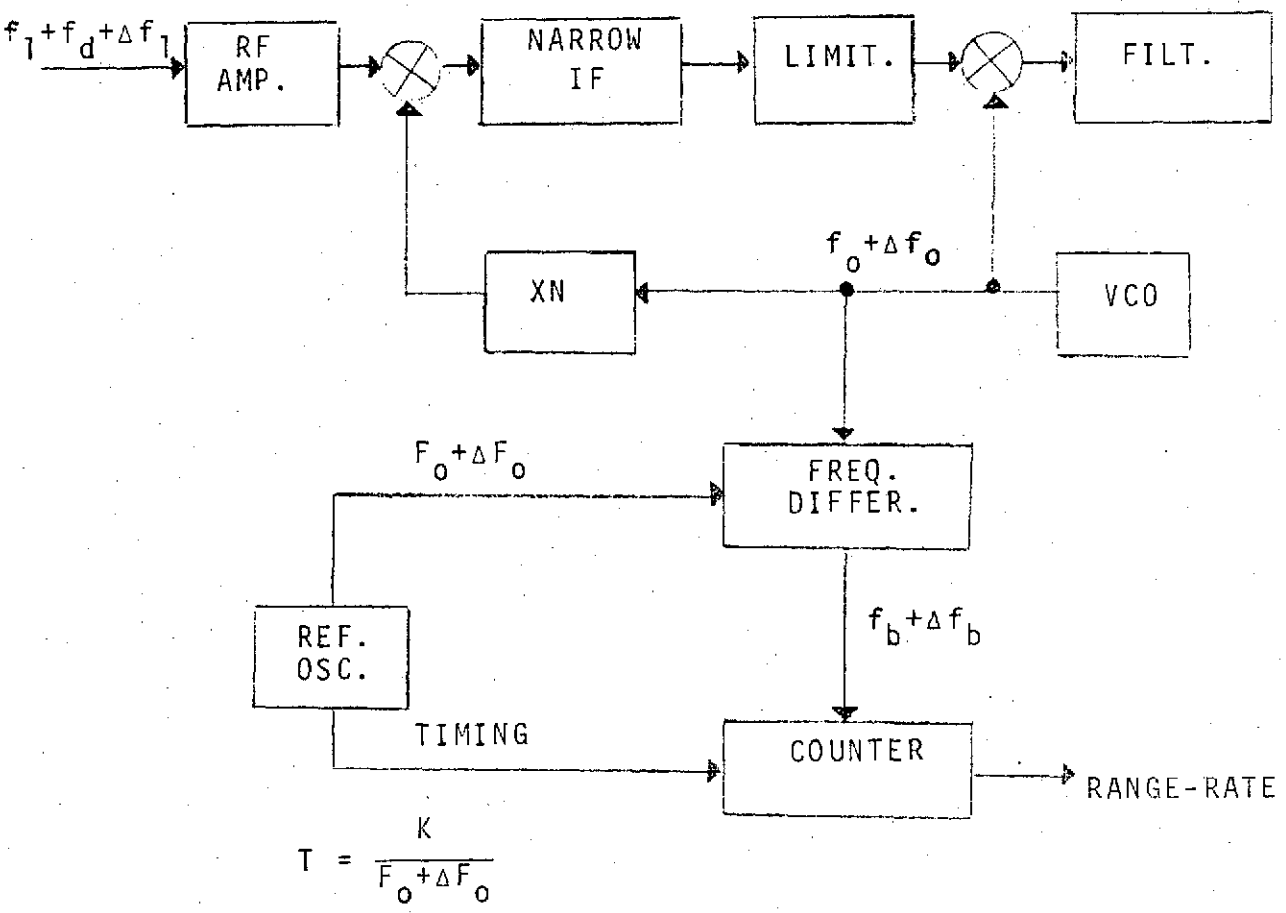
$$\varepsilon(\varepsilon_{\dot{R}}^2) = C^2 (\hat{S}_1^2 + \hat{S}_o^2) \qquad \text{WHERE } \hat{S} = S_{RMS}$$

$$\dot{R}^2 = E(\varepsilon_{\dot{R}}^2) - E^2(\varepsilon_{\dot{R}})$$

$$\therefore \boxed{\sigma_{\dot{R}_s} = C\sqrt{\hat{S}_1^2 + \hat{S}_o^2}} \qquad \text{DRIFT}$$

IF $\hat{S}_1 = \hat{S}_2 = \hat{S}$, THEN

$$\sigma_{\dot{R}} = C\hat{S}\sqrt{2}$$



FREQUENCY RELATIONSHIPS

$$f_1 = (N+1) f_o$$

$$f_b = f_o - F_o$$

DOPPLER & RANGE-RATE

$$\Delta f_b = \frac{f_d}{N+1} + \frac{\Delta f_1}{N+1} - \Delta F_o$$

$$\dot{R} = \frac{(N+1)C}{f_1} \left[\frac{\frac{K}{F_o + F_o(f_b+\Delta f_b)} - \frac{K}{f_o} f_b}{K/F_o} \right]$$

FIGURE 4-4 CONFIGURATION - SYSTEM 1

b. Quantization error

This error in the counted frequency of the VCO is

$$\varepsilon\Delta_f = \sqrt{2}\,\frac{\varepsilon}{T} \quad \text{WHERE} \quad \varepsilon = \text{FRACTION OF A CYCLE LOST}$$

$$\sigma\Delta_f = \frac{\sqrt{2}\,\varepsilon}{T\sqrt{12}}$$

SINCE $\dot{R} = \frac{(N+1)C}{f_1} \cdot f_d$, THEN;

$$\sigma_{\dot{R}} = \frac{(N+1)C}{f_1} \cdot \frac{\varepsilon}{T\sqrt{6}}$$

ε has the range from 0 to 1 cycle if full cycles are counted. Thus,

$$\boxed{\sigma_{\dot{R}_Q} = \frac{(N+1)C}{f_1 T \sqrt{6}}} \quad \text{QUANTIZATION}$$

Thus the quantization error is multiplied by the ratio of the received frequency to VCO frequency.

c. Jitter error

In the narrow band loop the frequency relationship are:

$$f_1 - (N+1)(f_o+\sigma_j) = \frac{1}{2\pi\, T\, \sqrt{(S/N)_{LOOP}}}$$

SINCE $f_1 = (N+1)f_o$

THEN:

$$\sigma_j = \frac{1}{2\pi\,(N+1)\,T\,\sqrt{S/N}}$$

AND:

$$\boxed{\sigma_{\dot{R}} = \frac{1}{N+1} \cdot \frac{C}{2\pi\, f_1\, T\, \sqrt{S/N}}} \quad \text{JITTER}$$

4.2.1.3.2 System 2 Configuration

Shown in Figure 4-5 this system beats a reference oscillator with the RF signal to produce a wideband IF. The VCO is phase locked to this IF frequency, with the result that full doppler is available on the VCO. A disadvantage of this system is that a low S/N ratio is injected into the limiter. Higher power transmitters may then be required if the loop bandwidth is narrow.

The minimum IF bandwidth to pass full doppler is 120 KHz. Even if the loop tracking bandwidth was as low as 200 Hz, then the S/N into the limiter would be -18 dB for a 10 dB loop S/N ratio. This is sufficient to be above the nominal phase detector threshold of -30 dB.

The addition of data modulation to the carrier signal will require that the IF be wider than 120 KHz. Thus, at a typical data modulation rate of about 80 Kbps the IF bandwidth should be increased by 160 KHz to 280 KHz. However, for accurate data demodulation the S/N ratio in this wider IF should be 10 dB or higher with the result that the limiter receives a S/N level higher than the -18 dB determined above.

a. Frequency drift effect

$$\Delta F_o = S_o F_o;\ \Delta f_1 = S_1 f_1$$

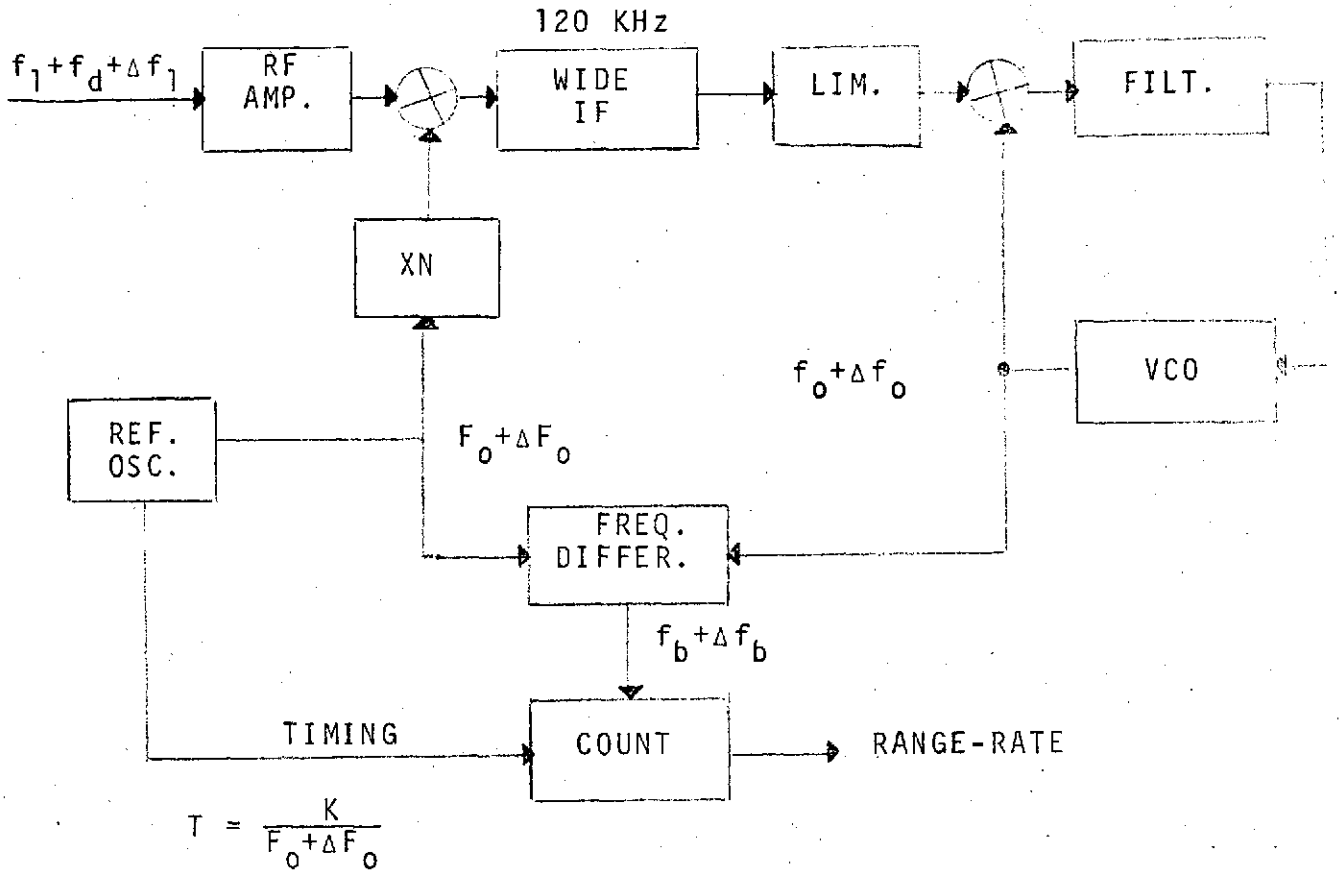
$$\Delta f_b = f_d + S_1 f_1 - (N+1) S_o F_o$$

$$\dot{R} = \frac{C}{f_1} \cdot \left[(1-S_o)\ (f_b + \Delta f_b) - f_b\right]$$

$$\dot{R} = \frac{C}{f_1} \left(\Delta f_b - S_o f_b - S_o \Delta f_b\right)$$

$$f_b = f_o - F_o$$

$$\therefore \dot{R} = \frac{C}{f_1} \cdot \{ \underbrace{f_d + S_1 f_1}_{\text{TRUE DOPPLER}} - (N+1) F_o S_o - S_o f_o + S_o F_o - S_o \left[f_d + S_1 f_1 - (N+1) F_o S_o\right] \}$$



FREQUENCY RELATIONSHIPS

$$f_1 = NF_o + f_o$$

$$f_b = f_o - F_o$$

DOPPLER & RANGE-RATE

$$\Delta f_b = f_d + \Delta f_1 - (N+1)\Delta F_o$$

$$\dot{R} = \frac{C}{f_1} \cdot \frac{F_o+\Delta F_o\ (f_b+\Delta f_b) - \frac{K}{F_o} f_b}{K/f_o}$$

FIGURE 4-5 CONFIGURATION - SYSTEM 2

subtracting out the true doppler, and neglecting second order terms in S, results in the range rate error:

$$\dot{\varepsilon}_R = \frac{C}{f_1}\left[S_1 f_1 - S_o(NF_o + f_o) - S_o f_d\right]$$

SINCE $Nf_o + f_o = f_1$

AND $f_d << f_1$, THEN;

$$\dot{\varepsilon}_R = C(S_1 - S_o)$$

$$\dot{\varepsilon}_R^2 = C^2 (S_1^2 + S_o^2 - 2S_oS_1)$$

$$E(\dot{\varepsilon}_R^2) = C^2(S_1^2 + S_o^2)$$

SINCE $E(\dot{\varepsilon}_R) = \dfrac{C\, S_o^2 (N+1)\, F_o}{f_1} < 10^{-11}$ FPS = 0

THEN:

$$\dot{\sigma}_R^2 = E(\dot{\varepsilon}_R^2)$$

thus, if $\hat{S}_1$ and $\hat{S}_o$ are the RMS stability factors for the oscillators, then:

$$\boxed{\dot{\sigma}_{R_S} = C\sqrt{\hat{S}_1^2 + \hat{S}_o^2}} \qquad \text{DRIFT}$$

If the frequency stabilities of the ground station and satellite oscillators are equal, then the range rate error due to drift becomes:

$$\sigma_R = C\,\hat{S}\,\sqrt{2}$$

b. Quantization error

The error in the counted frequency of the VCO, caused by quantization is:

$$\varepsilon\Delta_f = \sqrt{2}\ \varepsilon/T$$

$$\sigma\Delta_f = \varepsilon/T\ \sqrt{6}$$

AND

$$\sigma\dot{R} = \frac{C}{f_1}\ \sigma\Delta_f = \frac{C\varepsilon}{f_1 T\ \sqrt{6}}$$

If ε is uniform over 0 - 1 cycle

$$\boxed{\sigma\dot{R}_Q = \frac{C}{f_1 T\ \sqrt{6}}} \qquad \text{QUANTIZATION}$$

c. Jitter error

In the PLL narrowband filter the frequency relationships are:

$$(f_1 - NF_o) - (f_o + \sigma_j) = \frac{1}{2\pi T\ \sqrt{(S/N)_{LOOP}}}$$

BUT $f_1 = NF_o + f_o$

$$\therefore\ \sigma_j = \frac{1}{2\pi T\ \sqrt{(S/N)_{LOOP}}}$$

AND

$$\boxed{\sigma\dot{R}_J = \frac{C}{2\pi f_1 T\ \sqrt{(S/N)_{LOOP}}}} \qquad \text{JITTER}$$

4.2.1.3.3 System 3 Configuration

Shown in Figure 4-6 this system has both wideband and narrowband IF's, resulting from beating of a master reference oscillator with the RF signal. This receiver has full doppler on the VCO and also a high S/N ratio into the limiter.

a. Frequency drift effect

$$\Delta F_o = S_o F_o ; \quad \Delta f_1 = S_1 f_1$$

$$\Delta f_b = f_d + S_1 f_1 - (M+N+1) S_o F_o$$

$$\dot{R} = \frac{C}{f_1} \left[(1-S_o) \ (f_b + \Delta f_b) - f_b \right]$$

$$\dot{R} = \frac{C}{f_1} \left[\Delta f_b - S_o (f_b + \Delta f_b) \right]$$

$$f_b = F_o - F_o$$

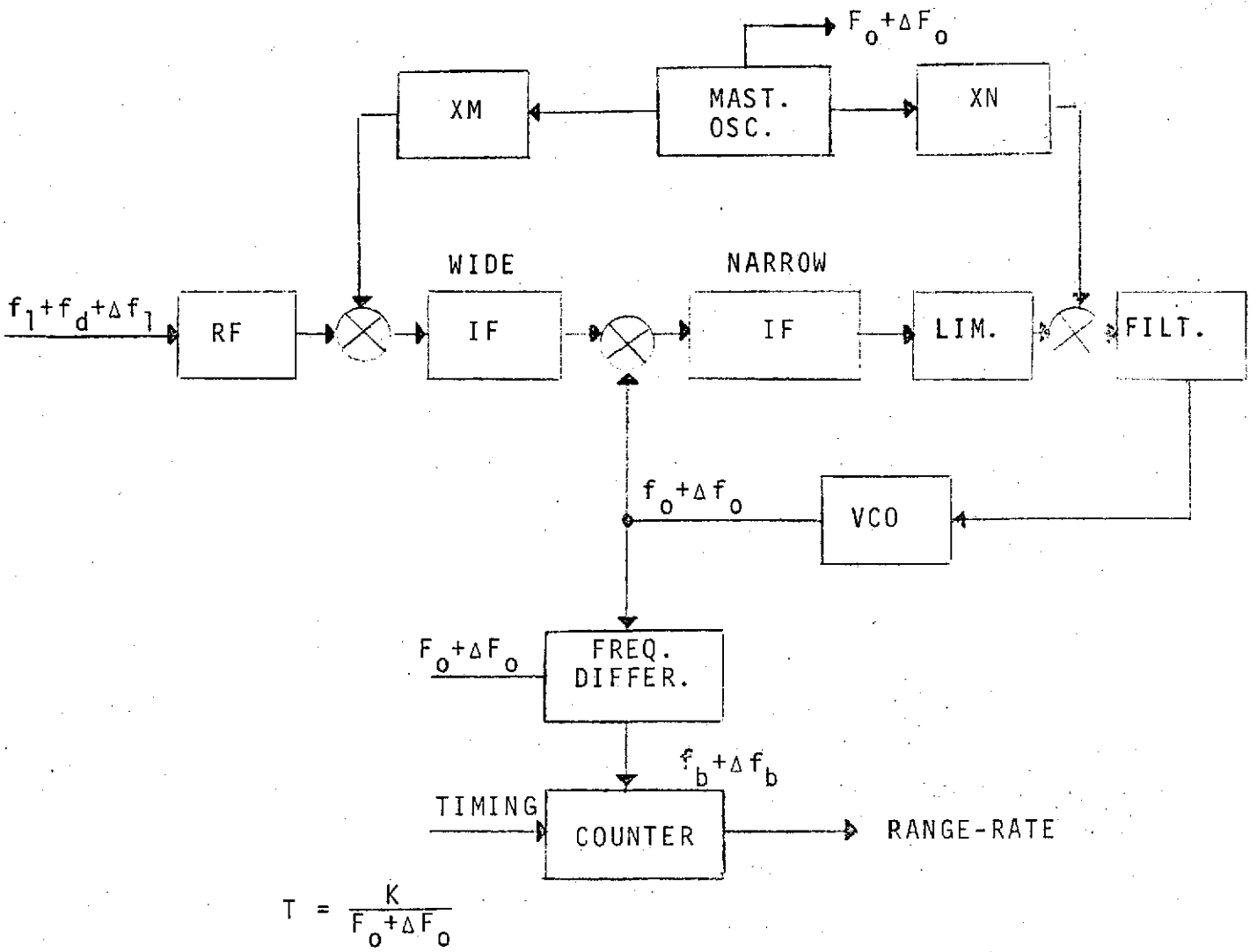
$$\ddot{R} = \frac{C}{f_1} \left\{ \begin{array}{l} f_d + S_1 F_1 - (M+N+1) S_o F_o - S_o f_o + S_o F_o \\ -S_o \left[f_d + S_1 f_1 - (M+N+1) S_o f_o \right] \end{array} \right\}$$

Subtracting out the true doppler and neglecting second order terms in S, the resultant error is:

$$\dot{\varepsilon}_R = \frac{C}{f_1} \left\{ S_1 f_1 - \left[(M+N) \ F_o + f_o \right] S_o - f_d S_o \right\}$$

SINCE $f_1 = (M+N) F_o + f_o$

AND $f_d << f_1$



$$T = \frac{K}{F_o+\Delta F_o}$$

FREQUENCY RELATIONSHIPS

$$f_1 = (M+N)\ F_o+f_o$$

$$f_b = f_o-F_o$$

DOPPLER & RANGE-RATE

$$\Delta f_b = f_d+\Delta f_1 - (M+N+1)\Delta F_o$$

$$\dot{R} = \frac{C}{f_1} \quad \frac{\left[\frac{K}{F_o+\Delta F_o}(f_b+\Delta f_b) - \frac{K}{F_o} f_b\right]}{K/F_o}$$

FIGURE 4-6 CONFIGURATION - SYSTEM 3

THEN:

$$\dot{\varepsilon}_R = C(S_1 - S_o)$$

$$\dot{\varepsilon}_R^2 = C^2 (S_1^2 + S_o^2 - 2S_1S_o)$$

$$E(\dot{\varepsilon}_R^2) = C^2 \left[E(S_1^2) + E(S_o^2) + 0\right]$$

SINCE: $E(\dot{\varepsilon}_R) < 10^{-11}$ FPS $\approx$ 0, THEN

$$\dot{\sigma}_R^2 = E(\dot{\varepsilon}_R^2)$$

If $\hat{S}_o$ and $\hat{S}_1$ are the RMS stability factors, then

$$\boxed{\dot{\sigma}_{R_S} = C\sqrt{\hat{S}_1^2 + \hat{S}_o^2}} \quad \text{DRIFT}$$

for equal stability factors

$$\dot{\sigma}_R = C\,\hat{S}\,\sqrt{2}$$

b. Quantization error

Since full doppler is available on the VCO, the quantization error is the same as for system (2). thus:

$$\boxed{\dot{\sigma}_{R_Q} = \frac{C}{f_1 T\sqrt{6}}} \quad \text{QUANTIZATION}$$

c. Jitter error

The frequency relationships in the PLL are:

$$(f_1 - MF_o) - (f_o + \sigma_j) - NF_o = \frac{1}{2\pi T\sqrt{(S/N)_{LOOP}}}$$

OR

$$f_1 - (M+N)F_o - f_o - \sigma_J = \frac{1}{2\pi T\sqrt{(S/N)_{LOOP}}}$$

BUT

$$f_1 = (M+N)F_o + f_o$$

$$\therefore \sigma\dot{R}_J = \frac{1}{2\pi T \sqrt{(S/N)_{LOOP}}} \qquad \text{JITTER}$$

4.2.1.3.4 System 4 Configuration (Multi-Channel Receiver)

Shown in Figure 4-7 this receiver uses wide bandwidth IF amplifiers and a fixed reference oscillator to obtain 20 channel capability. A variable multiplier stage in the 2nd mixer loop allows switch selectability of any one of the 20 channels. Since fixed reference oscillator frequencies are used for all but the final phase detector stage, full doppler frequency is available on the VCO output. Mixing of the VCO output with a 68 MHz reference oscillator frequency could be added to obtain the full doppler on approximately a 1 MHz bias frequency.

The error analysis for this receiver is similar to receiver types 2 and 3 previously described. That is:

a. Frequency drift error

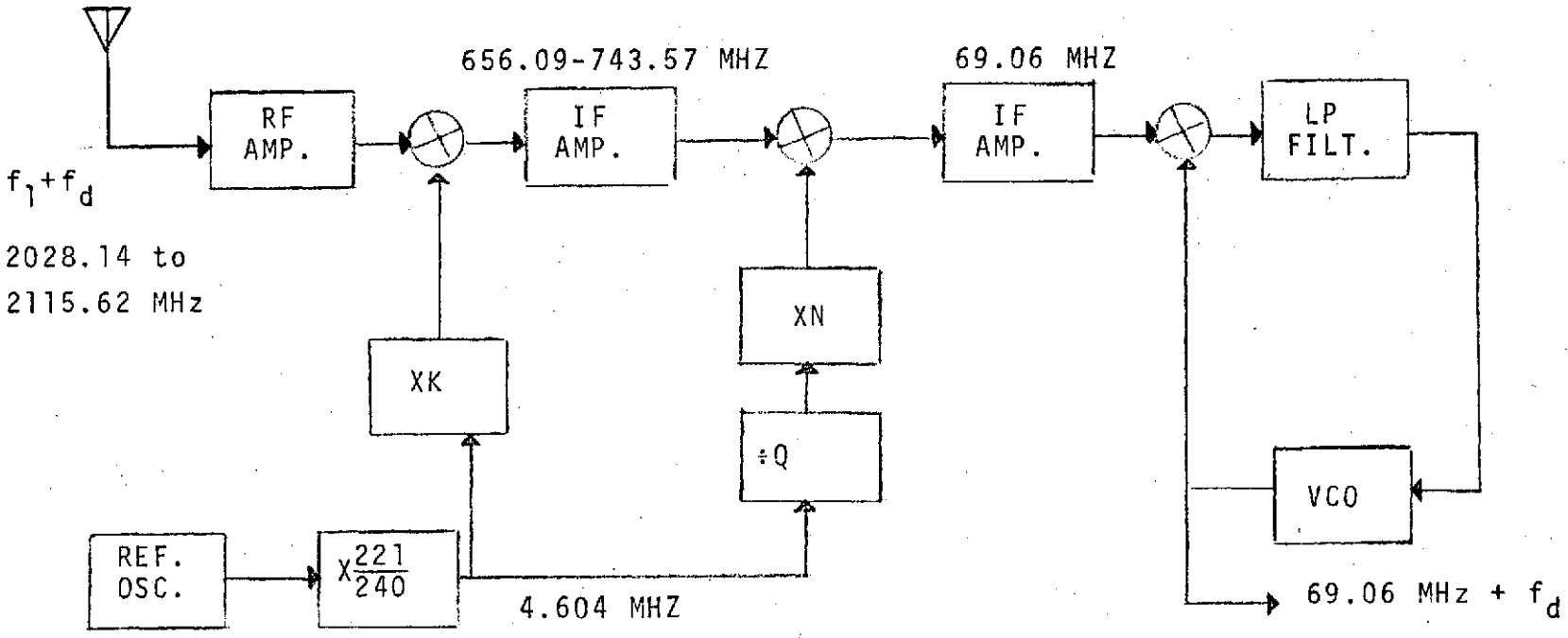
$$\sigma\dot{R}_S = C\sqrt{\hat{S}_1^2 + \hat{S}_2^2}$$

b. Quantization error

$$\sigma\dot{R}_Q = \frac{C}{f_1 T \sqrt{6}}$$

c. Jitter error

$$\sigma\dot{R}_J = \frac{C}{2\pi f_1 T \sqrt{(S/N)_{LOOP}}}$$



$$f_1 = (K+N/Q)\ (4.604) + 69.06 = (440.5+N)X\ 4.604$$

$$K = 298$$

$$Q = 2$$

$$N = 255 + 2n,\ (n=0\text{-}19)$$

$$\dot{R} = f_d \times \left[C \times \frac{48 \times 10^6}{(313+N/2).221}\right]$$

FIGURE 4-7 CANDIDATE MULTI-CHANNEL DOPPLER EXTRACTOR

4.2.2 QUANTIZATION ERROR REDUCTION OPTIONS

The various options for reducing quantization error have been discussed in Section 2.2.1. The method of using long averaging times is not considered here as a system option since the doppler extractor must operate at averaging times as short as 0.5 seconds. However, for instances where long averaging times are used, this technique does have impact on the other system options (such as oscillator selection, since long term oscillator drifts may be significant sources of error in the extraction process). Thus, long averaging times will be considered only for those systems that are affected directly by its use. The other five options discussed in Section 2.2 will be discussed in the system selection process.

4.2.3 CANDIDATE REFERENCE OSCILLATORS

The requirement to measure doppler frequencies accurately to a fraction of a hertz over a one second integration time requires short term oscillator stabilities of at least one part in 10^{10}. The long term bias error requirement of less than 2 Hz requires a long term stability of one part of 10^{9}. To meet these requirements, the oscillator could be of three types:

1. High stability ovenized quartz crystal oscillator
2. Rubidium gas oscillator
3. Cesium beam oscillator

Table 4-1 compares some of the parameters of these oscillators. The cesium beam standard is very desirable from the standpoint of stability and environmental effects. However, its size, weight and cost are prohibitive for Shuttle use and there is little hope that any of these characteristics will be significantly improved in the near future. Thus, the candidate oscillators for Shuttle use is limited to either quartz or rubidium gas.

TABLE 4-1 CHARACTERISTICS OF REPRESENTATIVE STABLE REFERENCE OSCILLATOR

TYPE	QUARTZ	QUARTZ	RUBIDIUM	RUBIDIUM	CESIUM
MANUFACTURER	HEWLETT-PACKARD	FREQUENCY ELECTRONICS	HEWLETT-PACKARD	EFRATOM	HEWLETT-PACKARD
MODEL NO.	HP 10543A	FE-1800DS	HP 5065A	FRK	HP 5062C
SHORT TERM STABILITY (1 SEC)	10^{-11}	10^{-12}	$5X10^{-12}$	$5X10^{-11}$	$7X10^{-11}$
LONG TERM STABILITY (MONTH)	$5X10^{-10}$	$<10^{-10}$	$1X10^{-12}$	$1X10^{-10}$	$1X10^{-11}$ (3 YRS)
OUTPUT LEVEL (50 Ω)	20 MW	20 MW	20 MW	20 MW	20 MW
POWER CONSUMPTION	24V, 3.5W	12.5V, 1.5W	24V,35W	24V,13W	24V,30W
WEIGHT	1.3 LBS	6.5 LBS	34 LBS	2.9 LBS	40 LBS
SIZE	30 IN^3	130 IN^3	1700 IN^3	73 IN^3	1700 IN^3
PRICE	$850	$12,000	$7,500	$6,400	$15,000

Of the quartz oscillators available, the characteristics of the Hewlett-Packard model HP 10543A, or Frequency Electronics model FE-1800D have characteristics desirable for Shuttle application. In terms of stability, weight and size, these units are representative of the state-of-the-art for quartz oscillators.

Of the rubidium oscillators, Frequency and Time Systems Inc., model FRK represents state-of-the-art development. This unit is low in weight and is suitable for airborne application. An evaluation of this unit has been made by NRL (reference 10) and several deficiencies noted. However, the reference suggests some design changes which may make the unit attractive for high stability airborne doppler measurements.

4.3 SYSTEM SELECTION

This section of the report discusses the system recommended for Shuttle applications and for breadboarding of a demonstration unit. The system is shown in a simplified block diagram in Figure 4-8. A more detailed description is included in Part II. The systems consists of an S-band transponder, a coincidence detection doppler extractor and either a quartz or rubidium reference oscillator (clock). This system was selected based on the criteria of high accuracy at minimum cost, weight, complexity and development effort.

Use of the S-band transponder VCO output offers an economical method of obtaining a carrier plus doppler reference frequency without adding significantly to total system weight, complexity or development effort. As Section 4.2 has shown, full doppler can be obtained by the addition of low frequency multiplier and mixer stages in the doppler extractor. Use of the S-band transponder in this manner will result in system accuracies equivalent to the other receiver options without the need to modify the RF or IF sections of the receiver. The transponder also

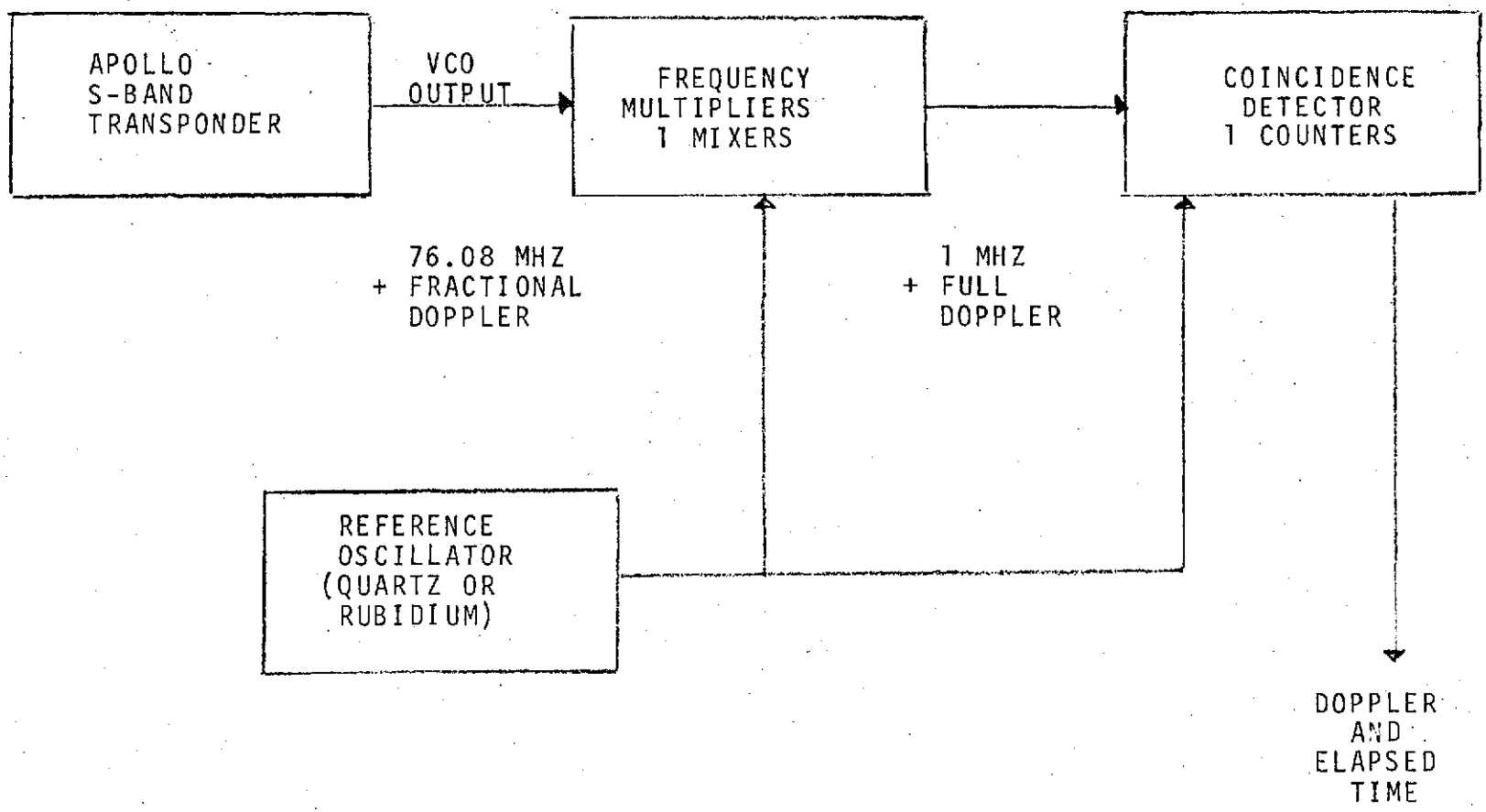


FIGURE 4-8 RECOMMENDED TECHNIQUE FOR DOPPLER EXTRACTION

offers the least technical risk since it has been flight proven in many lunar and orbital missions.

For Shuttle applications it would be desirable to modify the S-Band transponder to achieve a VCO sweep for rapid and autonomous acquisition. As shown in Section 3.1.4, the transponder could acquire the carrier reference frequency in one to two seconds coherently or about 0.2 seconds non-coherently.

The coincidence detection doppler extractor was selected to reduce the quantization error without the need for high speed counters. Even when full doppler frequencies are available to a conventional counter the desired range-rate accuracy of 3 cm/sec (0.1 ft/sec) can only be obtained with integration periods of 5 seconds or longer. Thus, a quantization resolving extractor would be desirable for reduced error at short integration times. The coincidence detection technique is recommended since this extractor can take advantage of low cost, low power and high reliability CMOS components, without sacrificing accuracy.

4.4 VERNIER DOPPLER EXTRACTOR ANALYSIS

This section analyzes the accuracy and time delays associated with the coincidence detection technique and shows the limiting effects of this delay on the extractor resolution capability. Also described is the effect of the time delay on the total system errors when the doppler extractor measurements are compared (or averaged) with other range rate measuring equipment (such as accelerometers).

4.4.1 EXTRACTOR ACCURACY ANALYSIS

The vernier doppler extractor uses narrow detection windows to define the coincidence of positive zero crossings of the desired doppler plus bias frequency and a known reference frequency (stable clock). The principle of operation is similar to the familiar vernier caliper measuring instruments

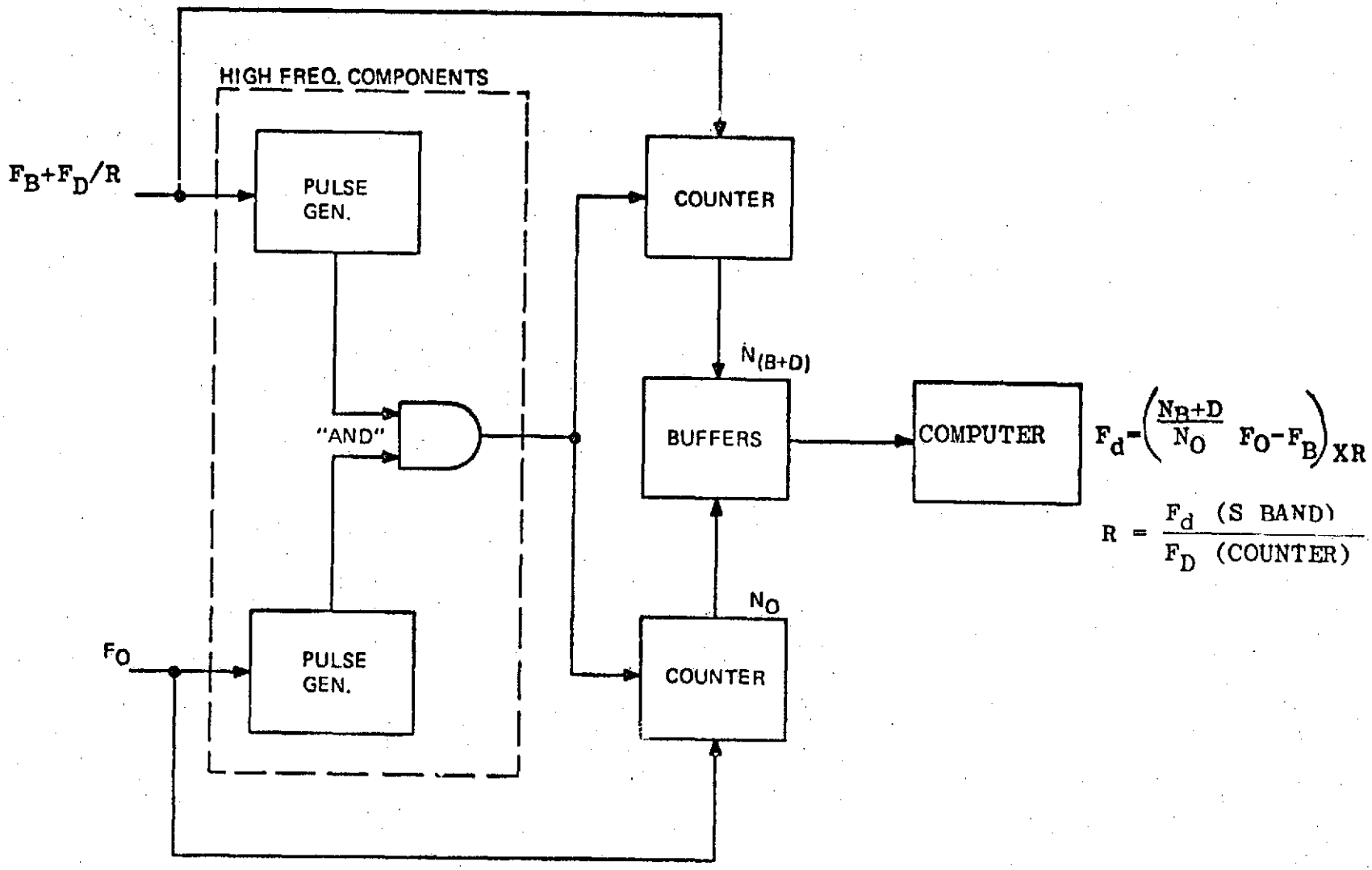
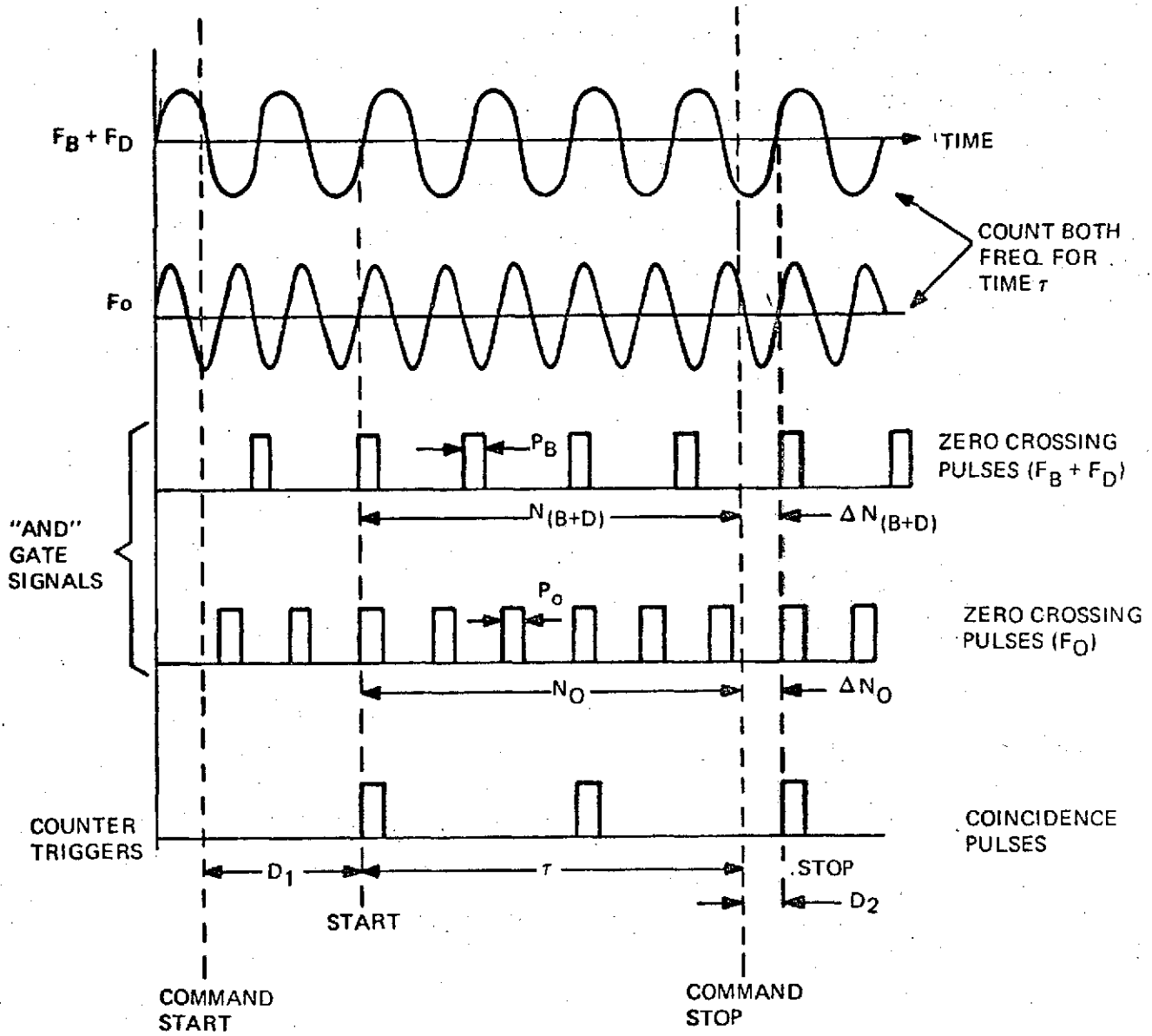


FIGURE 4-9 COINCIDENCE DETECTION DOPPLER EXTRACTOR, BLOCK DIAGRAM



$$\tau + D_2 = \frac{N_0 + \Delta N_0}{F_0}$$

$$F_D = R. \left[\frac{N_{(B+D)} + \Delta N_{(B+D)}}{N_0 + \Delta N_0} \cdot F_0 - F_B \right]$$

QUANTIZATION ERROR

$$= \left[\frac{(P_0 + P_B)(F_B + F_D)}{\tau} \right] \cdot R \text{ Hz}$$

FIGURE 4-10 TIMING SCHEME FOR COINCIDENCE DOPPLER EXTRACTOR

which can obtain a resolving power much greater than the smallest quantized measurement interval. In the vernier doppler extractor the positive zero crossings of the signals serve as reference marks and conventional frequency counters supply the measured cycle counts. If the known and unknown frequency counters are both simultaneously started and stopped on zero crossings the quantization is eliminated and the unknown frequency can be resolved to a very high accuracy. Figure 4-9 shows a functional block diagram of the implementation required to achieve the coincidence detection and control of the frequency counters, and Figure 4-10 shows the resultant signals and timing schemes.

In Figure 4-9, a zero crossing detector triggers a pulse generator to emit a very narrow and stable pulse at each zero crossing of the unknown and clock frequencies. An "AND" gate detects the coincidence of the pulses when they occur and emits a control pulse to start or stop counters which separately count the unknown and clock frequencies.

Figure 4-10 shows how the circuit would operate when discrete measurement intervals are desired. A command to start the counters is received from the computer.

The counters are actually started immediately following the next detected pulse coincidence. Thus, both the bias plus doppler and clock counters are started immediately after a zero crossing. After a defined measurement period (τ), both counters are commanded to read out the accumulated counts to the computer. The counters, however, continue to count until the next pulse coincidence at which time the desired counts are read into buffers. Since both counters were started and read at zero crossings, both counts are very accurate and the doppler frequency can be calculated with high precision. The doppler frequency is given by:

$$Fd = \left[\frac{N_{(B\ D)}}{N_o} F_o - F_B\right].R$$

where: $N_{(B+D)}$ = bias plus doppler count

N_o = clock count

F_o = clock frequency and

F_B = bias frequency

R = Doppler division ratio from the S-Band transponder.

An inaccuracy exists in the counts due to the finite widths of the pulses. Thus, the "AND" gate will respond to a near coincidence if the two pulses overlap to any degree. With reference to the clock count and the pulse rise times, the integer representing the bias plus doppler count could be in error by a fractional cycle count varying over the range $-P/T_{(B+D)}$ to $+P/T_{(B+D)}$ cycles, where P is the pulse width from the bias plus doppler pulse generator, and the clock pulse generator and $T_{(B+D)}$ is the period of the bias plus doppler frequency.

This error which occurs at both the start and stop times of the counters, is uniformly distributed over the interval $\pm P(F_B+F_D)$ and each error is independent if τ is much larger than the interval between coincidences. The combined error results in a maximum doppler error defined by:

$$\varepsilon F_d = \pm \frac{2P(F_B+F_D)}{\tau} \cdot R$$

and a standard deviation defined by:

$$\sigma F_d = \frac{2P(F_B+F_D)}{\tau \sqrt{5}} \cdot R$$

where R is the ratio of S-band doppler to counted doppler and τ is the measured period.

If the doppler extractor were only concerned with obtaining an accurate doppler measurement over a period of 1 second, say, with no regard to how much the 1 second time interval could vary, then P could be made arbitrarily small. A one nanosecond pulse, for example, and a 1 MHz bias frequency would result in a doppler error of 0.002 cycles or 0.002 Hz in a second period, provided full doppler is available into the doppler counters (R=1), Such a pulse width is feasible with stable rise times of 0.1 ns.

4.4.2 TIME DELAY ANALYSES

A coincidence of zero crossings occurs whenever the two pulses have some overlap into the "AND" gate. The probability of a coincidence depends on the pulse widths and the inter-pulse periods. The average period between coincidences can be shown to be given by:

$$\overline{T}_c = \frac{1}{(P_o+P_B)\ (F_B+F_D)F_o}$$

This formula assumes that the clock and bias plus doppler frequencies are not harmonically related, or if so, enough random variation in their frequencies is present to assure that the maximum period between coincidences is not excessive.

With random variations in pulse timing due to noise jitter, Figure 4-11 shows the sensitivity of obtaining at least one coincidence in 100 μs as a function of pulse width and bias frequency. The curves show that the highest probability of coincidence and the shortest pulse widths are obtained when the bias frequency is chosen as close as possible to the clock frequency. Since the doppler shift will shift the bias frequency closer to F_0, it is necessary that the bias frequency be at least 60 KHz (maximum doppler) less than F_0.

If a 100 kHz difference in the frequencies is more desirable to allow for drifts (etc.), Figure 4-12 shows the coincidence

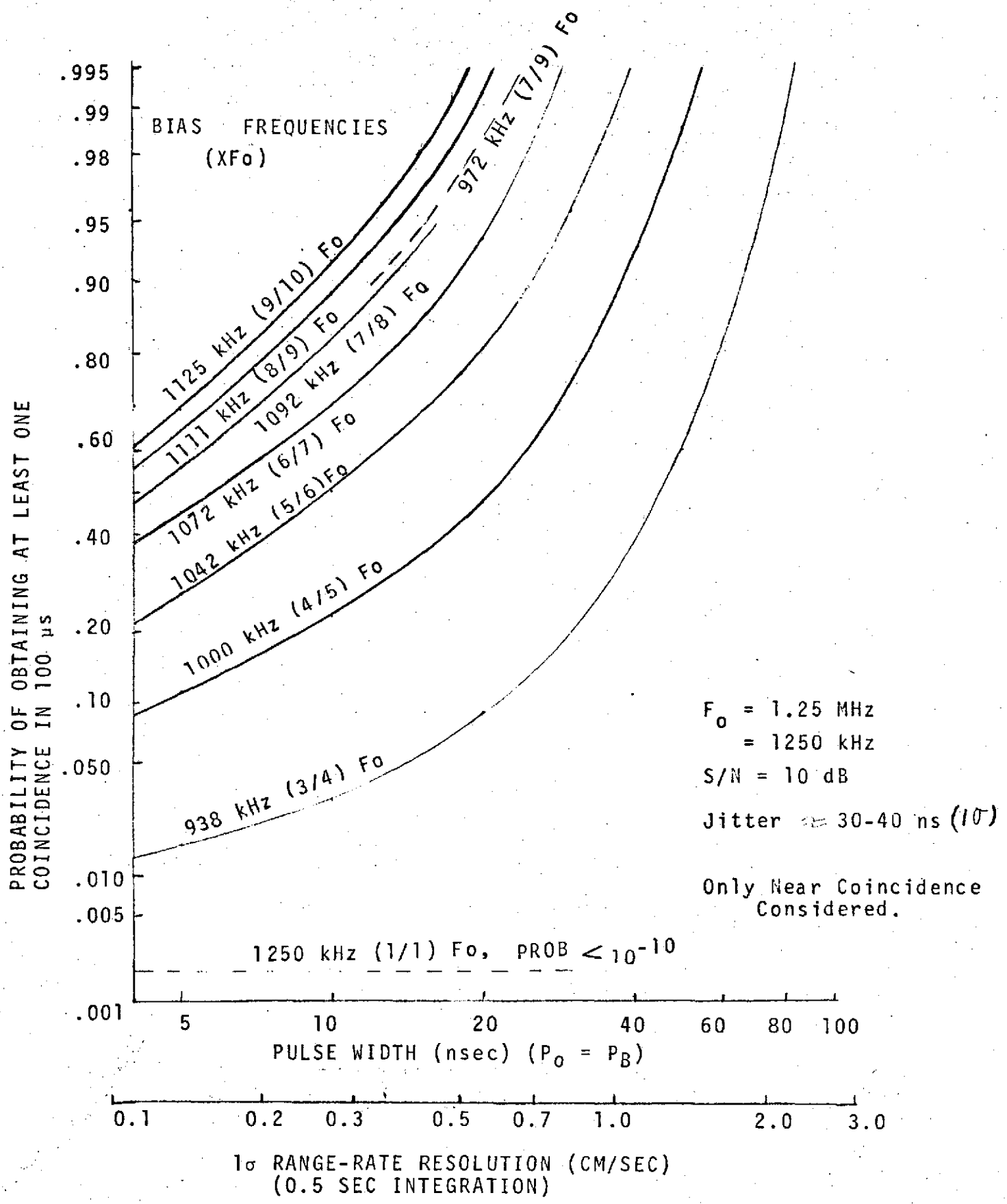


FIGURE 4-11 SENSITIVITY OF COINCIDENCE PROBABILITY TO PULSE WIDTH AND BIAS FREQUENCY AT RESONANCE

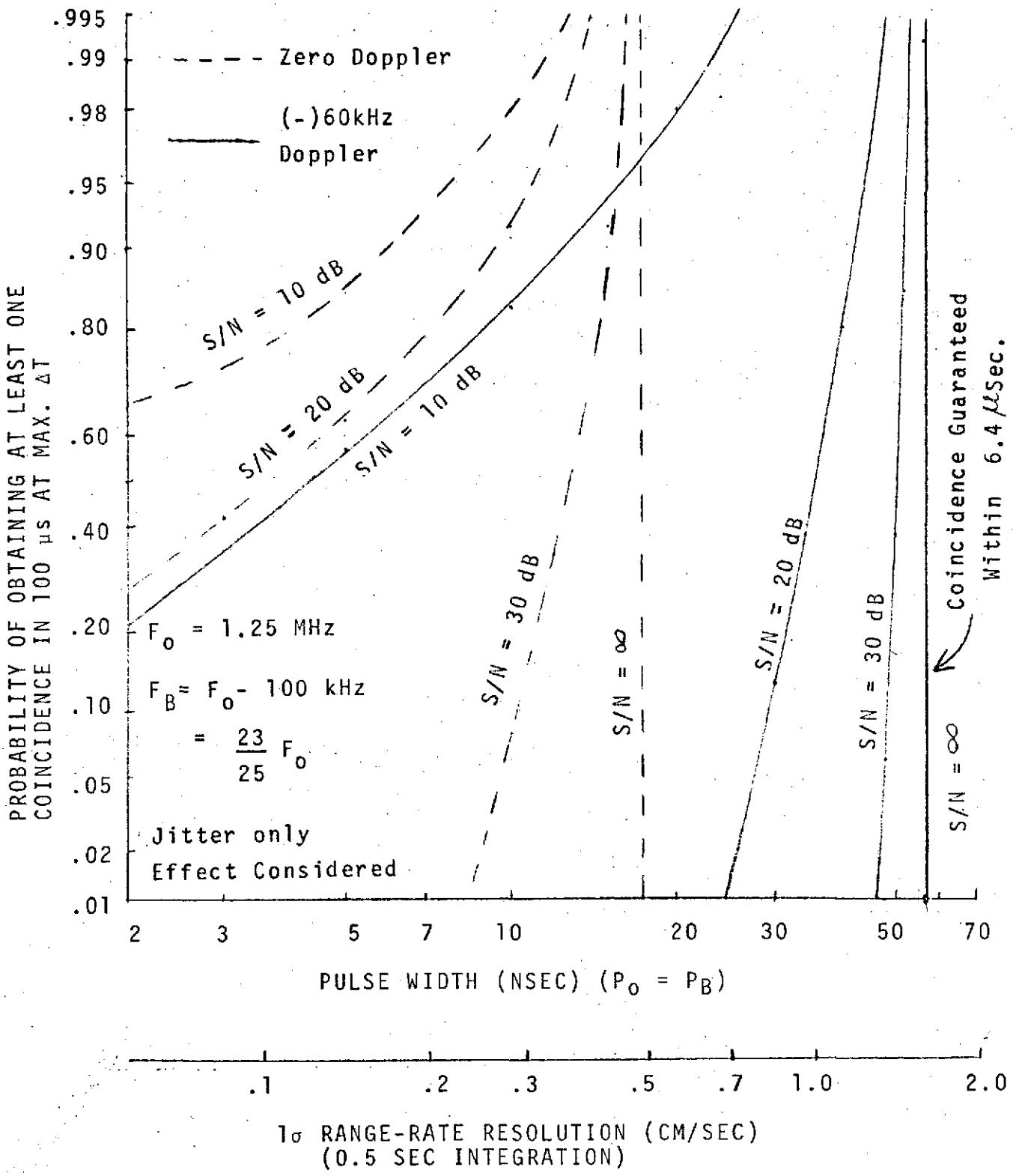
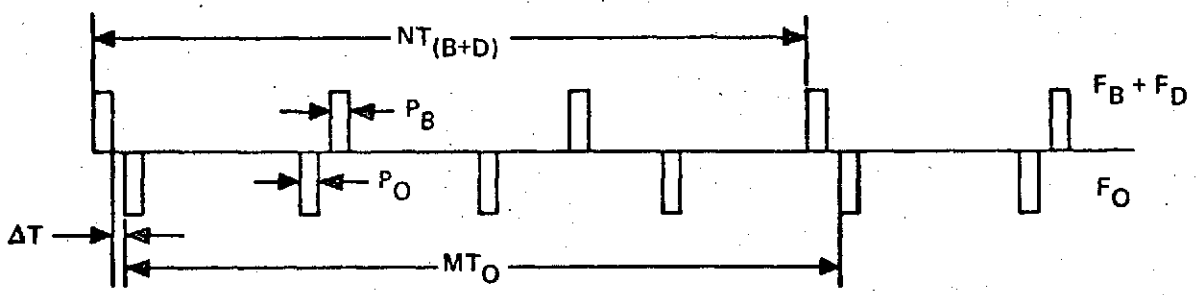


FIGURE 4-12 SENSITIVITY OF COINCIDENCE PROBABILITY TO DOPPLER AND S/N RATIO AT OPTIMUM BIAS FREQUENCY.



$M \approx N$; $M > N$; M &N Exact Integers

When:

$$\frac{F_B + F_D}{F_o} = \frac{N}{M}$$

Then:

$$T_{(B+D)} = \frac{M}{N} T_o \qquad \text{(M \& N have no common factors)}$$

Maximum possible separation at point of closest coincidence is given by

$$\Delta T \leq \frac{1}{2N} T_o - \frac{(P_o + P_B)}{2}$$

coincidence will occur in $M T_o$ seconds if

$$\frac{P_o + P_B}{2} \geq \frac{T_o}{2N}$$

FIGURE 4-13 EFFECT OF RESONANCES IN COINCIDENCE DETECTOR

probability when the bias frequency is 100 kHz less than F_0. The curves are plotted for the nominal (zero doppler) bias frequency and for the worst case harmonic relationship (near maximum negative doppler where $N/M = 7/8\ F_0$). The probability is also plotted as a function of S/N ratio (timing jitter). The results show that under worst case conditions (lowest possible harmonic ratio and zero timing jitter) pulse widths of 60 ns would be needed to guarantee a coincidence. At this pulse width $\Delta\tau \leq 0$ and a pulse coincidence is certain to occur in a maximum of eight clock periods (6.4 μs). The resultant range rate resolution is less than 1.8 cm/sec (0.06 ft/sec).

If the bias plus doppler frequency is an exact rational fraction of the clock frequency, a coincidence may never occur if the pulse width is made too narrow, or the S/N ratio is too high (random phase jitter too small for statistical treatment of time delay). This is shown in the diagram of Figure 4-13.

If the frequency ratio (F_B+F_D) is defined by the integers N/M (N/M is reduced to its lowest form and N M), a coincidence wil occur in MT_o seconds if the pulse width is greater than or equal to $T_o/2N$ (T_o = clock period). With $P - T_o/2N$, the doppler error equation becomes:

$$\varepsilon F_D = \pm \frac{2P(F_B+F_D)}{\tau}$$

but $2P = T_o/N$

and $F_B+F_D = \frac{N}{M} F_o$ (by definition)

$$\therefore \varepsilon F_D = \pm \left(\frac{T_o}{N}\right) \left(\frac{N}{M}F_o\right) = \pm \frac{1}{M\tau} \text{ since } T_o F_o = 1$$

M is the resolving power of the vernier extractor. The time delay has a maximum value of

$$td(MAX) - MT_o \text{ (td is uniformly distributed from zero to M } T_o$$

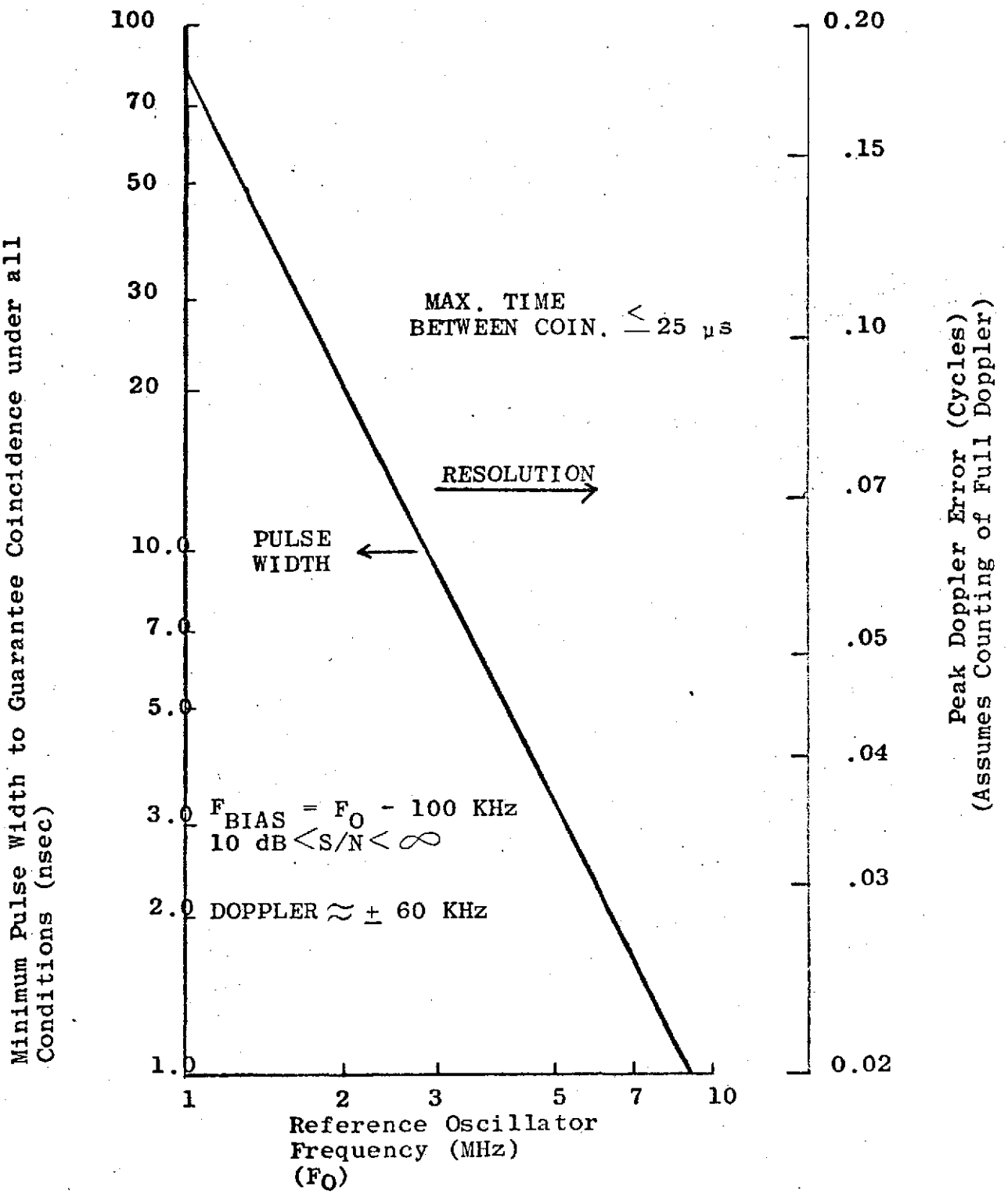


FIGURE 4-14 MINIMUM PULSE WIDTH TO GUARANTEE COINCIDENCE FOR ALL CONDITIONS

Since the time delay is random, the actual measurement interval can vary from $t-MT_o$ to $t+MT_o$. To keep the time interval variation small M should be small. But for high doppler accuracy M should be large. Thus, a compromise is required between acceptable time interval variations and desired doppler measurement accuracies.

If the time delay must be kept below some upper limit [(td(max.)], then M must not exceed a limit defined by:

$$M \leq \frac{td\ (MAX)}{T_o}$$

For example, if the clock period is 1 μs (F_o = 1 MHz) and the time delay must be less than 100 μs, then $M \leq 100$.

If the doppler shift varies, then the ratio N/M will vary, and the integer values of N and M will both vary. In this case the minimum allowable pulse width is defined when N is a minimum ($P \geq \frac{T_o}{2N_{min}}$) or when F_B+F_d is furthest from F_o. The maximum resolving power is also defined at this greatest separation of the two frequencies. If the doppler shift is too large, then the ratio $\frac{F_B-F_d\ max}{F_o} = \frac{N\ min}{M_{min}}$ will be small. N and M will also have small values. Thus, if M is to be large, then N must also be large and F_B-F_d max. F_o.

In summary, the vernier extractor can achieve high resolution only over a narrow bias plus doppler frequency range, if short time delays are required. Moderately high resolution can be achieved over a wider doppler range without increasing the time delays. To achieve the highest resoltuion and shortest time delays the clock and bias frequencies should be chosen as large as possible and the pulse widths as narrow as possible. Figure 4-14 shows the sensitivity of the doppler resolution to the clock reference frequency when the bias frequency is chosen to be off-set from the clock frequency by 100 kHz (full doppler is assumed into the

doppler counters). This off-set allows the bias plus doppler signal to remain always below the clock frequency and thus prevents long delays from occurring when $F_B+F_D=F_o$. As shown in the figure, doppler resolutions to 0.02 cycles can be obtained with a maximum possible delay of 25 μs, if the clock and bias frequencies are chosen at about 10 MHz. The pulse width, however, would need to be one nanosecond or less. The maximum delay can be shown to be 25 μs regardless of the clock frequency by the following analysis. With a 100 kHz nominal separation between F_o and F_B, the two frequencies can approach each other to within 40 kHz (with a maximum positive doppler of 60 KHz.) M will then have a maximum value given by:

$$\frac{N}{M} = \frac{M_{max}-1}{M_{max}} = \frac{F_B+F_{d(max)}}{F_o}$$

$$(M_{max}-1)\ F_o = M_{max}(F_B+F_{d\ max.})$$

or:

$$M_{max} = \frac{F_o}{F_o-(F_B+F_{d\ max})}$$

The maximum time delay is $M_{max.}(T_o)$, therefore:

$$td(max) = \frac{F_oT_o}{F_o-(F_B-F_{d\ max})} = \frac{1}{F_o-(F_B-F_{d\ max})}$$

With $F_o-(F_B+F_{d\ max.}) \geq 40$ kHz, the maximum time delay is less than or equal to 1/40 kHz - 25 μs.

If only fractional doppler is available (for example, on the 19 MHz VCO output the doppler could be 110 times lower than the S-band doppler), the resolution shown in the figure must be multiplied by the ratio of S-band doppler to counted doppler. However, with fractional doppler, it is not necessary to off-set the bias frequency by 100 kHz since the maximum doppler swing would only be about ± 600 Hz. The bias frequency could be placed within about 1 kHz of the

clock frequency. With a 1 MHz clock frequency, a 999 kHz bias frequency and ± 600 Hz of doppler, N/M would have a minimum value of $\frac{998400}{1{,}000{,}000} \geq \frac{624}{625}$.

The extractor could operate with pulse widths of 0.8 ns (T_o = 1 μs, 2N = 1248) and the resolution on the fractional doppler would be .0032 Hertz. When converted to S-band doppler, the resolution would be increased to 0.32 Hertz. The maximum delay would be 625 μs (MT_o). To reduce the requirements for narrow pulse widths and to decrease the maximum time delay it is desirable to have some large portion of the S-band doppler present on the counted bias frequency.

4.4.3 EXTRACTOR ACCURACY/TIME DELAY TRADE-OFFS

Narrow pulses or a low bias oscillator frequency reduce the quantization error; low values for these parameters will increase the average period between coincidences. Since measurements are taken at coincidence, narrow pulses or a low bias frequency will cause increased delay between the time when a measurement is desired and when it is actually obtained.

If the pulse widths are chosen to be at the minimum values to guarantee a coincidence ($P_o+P_B \leq T_o/N = \frac{1}{NF_o}$) then, as shown in the previous section, the maximum time delay will be given by

$$td\ (max) \leq \frac{1}{F_o-(F_B+F_{dmax})}$$

The worst case resolution (maximum error) of the extractor is defined when M is minimum. That is:

$$\sigma_R \leq \frac{C}{f_t \tau \sqrt{6}} \cdot \frac{1}{M_{min.}}$$

The minimum value of M occurs at maximum separation of the clock and bias plus doppler frequencies. At this maximum separation, M min. has a value given by:

$$\frac{M_{min}-1}{M_{min}} = \frac{F_B-F_{dmax}}{F_o}$$

or

$$M_{min} = \frac{F_o}{F_o-(F_B-F_{dmax})}$$

Therefore:

$$\dot{\sigma_R} \leq \frac{C}{f_t \tau \sqrt{6}} \cdot \frac{F_o-(F_B-F_{dmax})}{F_o}$$

Figure 4-15 shows the sensitivity of the extractor resolution and time delay to selected values of clock and bias frequencies. The curves show that the extractor resolution improves as the clock and bias frequencies are increased, and also improves as the bias frequency approaches the clock frequency.

The maximum time delay, however, is only dependent on the closeness of the bias plus doppler frequency and the clock frequency. Thus, in curve (b), the bias frequency is offset from the clock frequency by 100 kHz and the maximum time delay is 25 μs, independent of either the clock or bias frequency (as long as the two frequencies always differ by 100 kHz). However, as curve (b) shows, the resolution improves as the bias and clock frequencies are increased. The specification of 3 cm/sec maximum error can be met if the clock frequency is greater than about 1 MHz. The bias frequency would then be greater than about 900 kHz.

Combining the equations of time delay and resolution results in the relationship between resolution and time delay given by:

$$\dot{\sigma_R} = \frac{C}{f_t \tau \sqrt{6}} \cdot \frac{2F_{dmax}+1/td_{(max)}}{F_o}$$

Curves of the sensitivity of this maximum achievable resolution as a function of the maximum allowable time delay are shown in Figure 4-16. These curves show that the

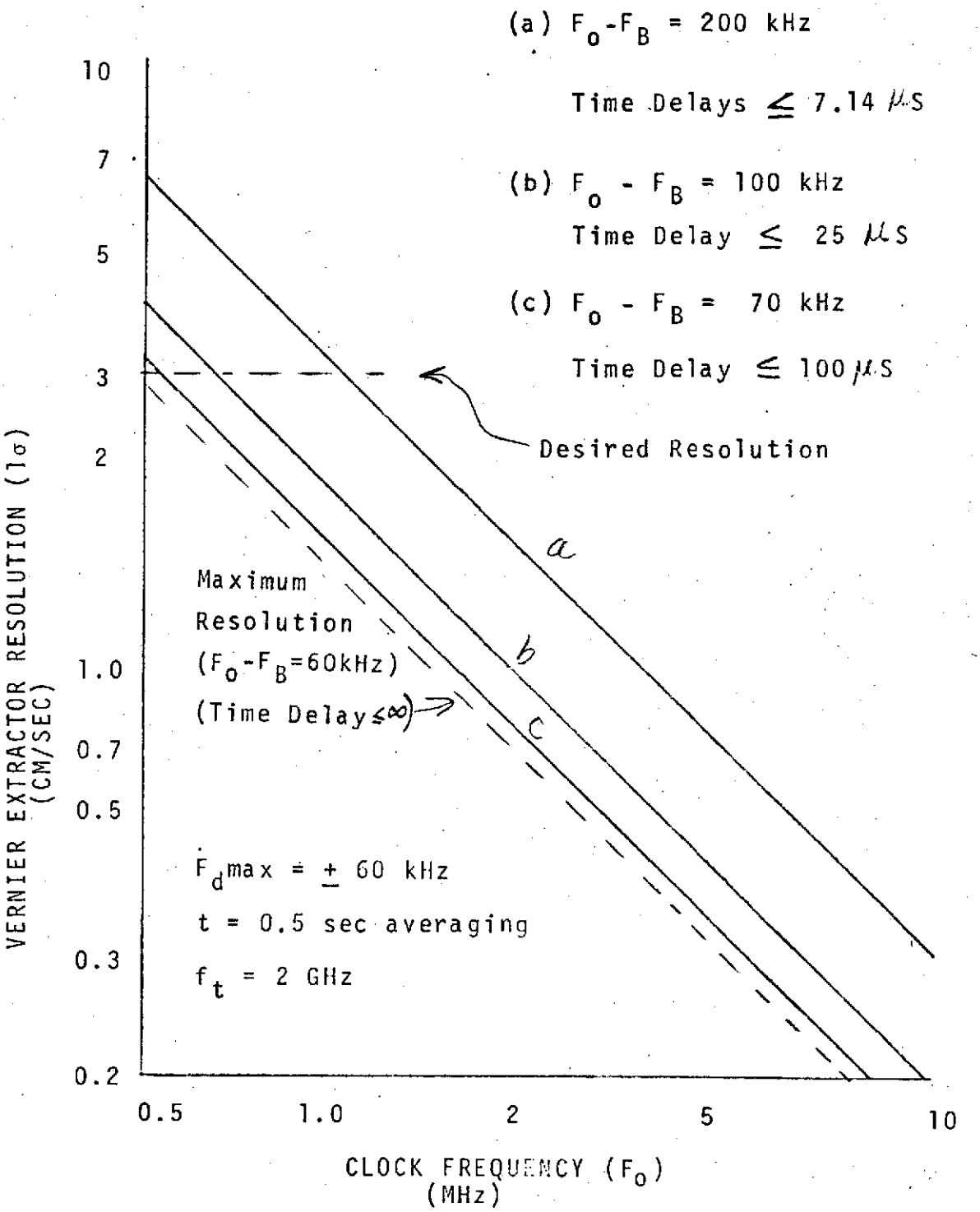


FIGURE 4-15 SENSITIVITY OF EXTRACTOR RESOLUTION AND TIME DELAY TO EXTRACTOR PARAMETERS

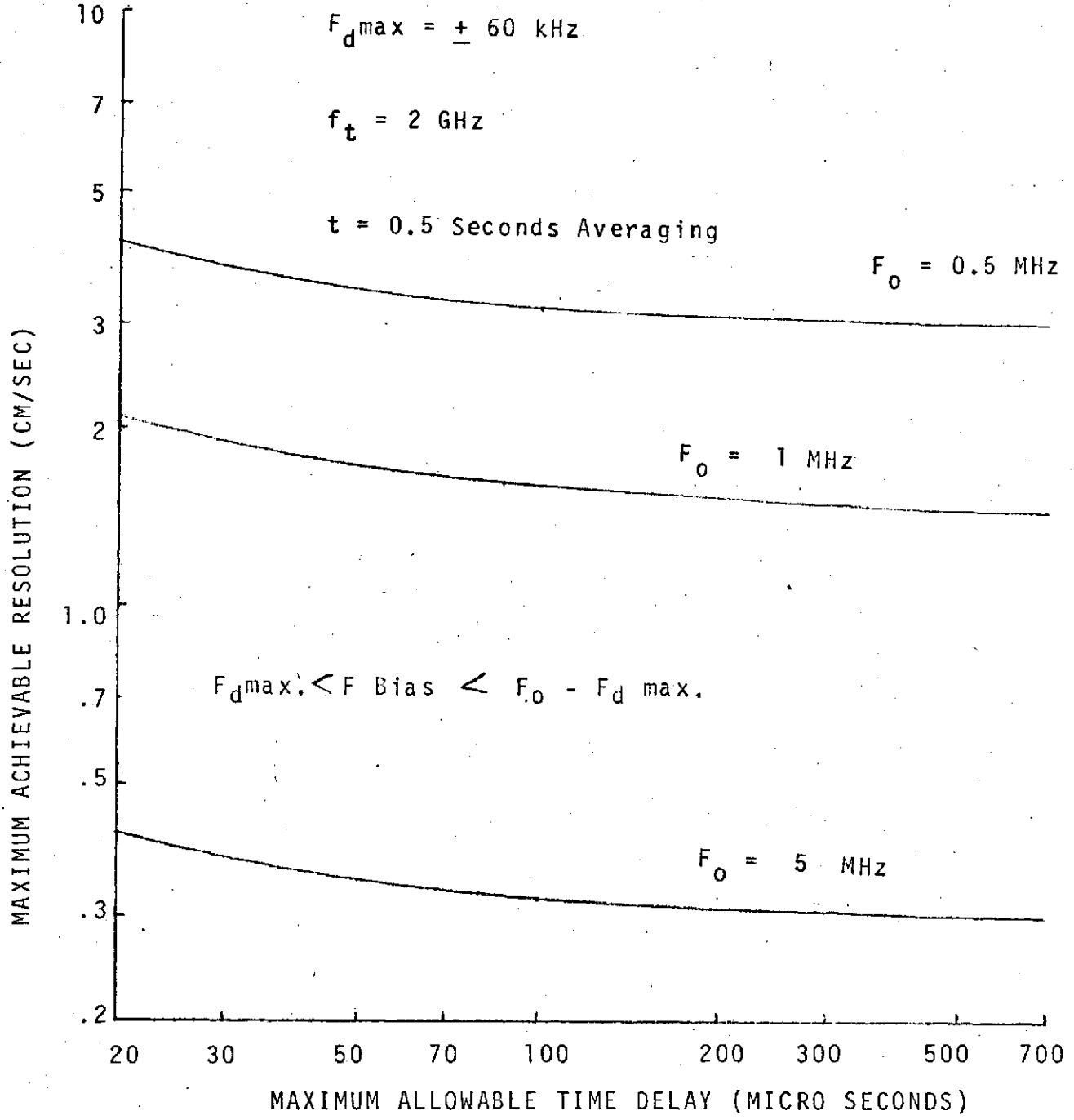


FIGURE 4-16 SENSITIVITY OF ACHIEVABLE RESOLUTION TO MAXIMUM TIME DELAY

resolution is not sensitive to time delay if the maximum time delay is allowed to be 100 μs or longer. Further, the extractor resolution is independent of the bias frequency, as indicated by the above equation, when the time delay must be kept below a maximum value.

4.4.4 EXTRACTOR IMPACT ON OTHER RANGE RATE MEASUREMENTS

This part of the report evaluates the sensitivity of total system error to values of pulse widths and counter frequencies when the doppler measurement is compared with other sensor data (e.g. accelerometers). The sensitivity to delays between the doppler and accelerometer measurements is evaluated and it is shown that delay times in excess of 100 μs are permissible without affecting the overall system accuracy.

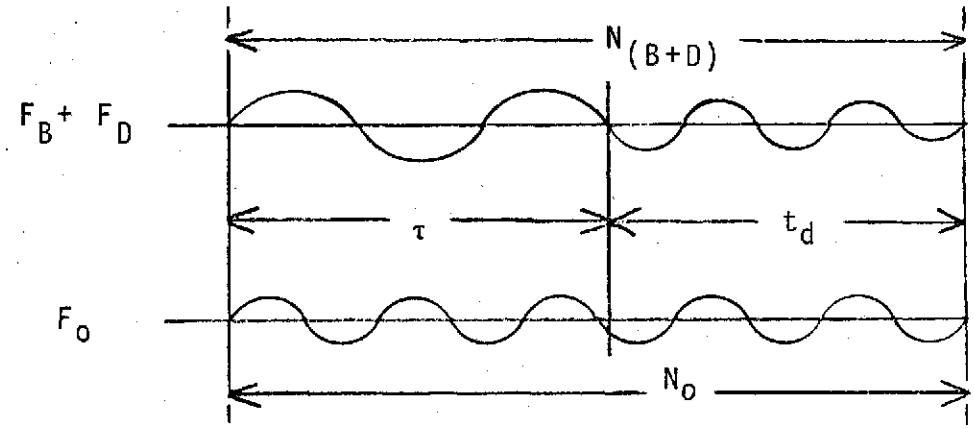
The effect of the time delay may be to cause an increase in the total error when the doppler measurement is compared with other sensor measurements taken over a slightly different time interval. Since the coincidence counter counts both the time interval and the doppler frequency the true time interval is known and only velocity changes occurring during the delay (which would not be included in the other sensor measurements) result in an actual error in the calculated doppler frequency. However, as the following analysis shows, the error increase resulting from the delay is negligible for pulse widths greater than about 0.5 nanoseconds (zero to 600 microseconds delay).

If it is assumed that the doppler frequency is constant for t seconds of integration, and the maximum acceleration occurs only during the delay interval (td seconds) then the maximum possible error caused by the delay is as shown in Figure 4-17. Assuming the shortest integration period of 0.5 seconds (highest error) and the maximum acceleration during the delay of 610 meters/second^2, the resultant range rate error caused by the delay is:

ASSUMPTIONS (WORST CASE)

NO ACCELERATION DURING INTEGRATION TIME (τ SEC)

MAXIMUM ACCELERATION DURING DELAY TIME (td)



$$F_D = \frac{N_{(B+D)}}{N_o} \quad F_o - F_B$$

$$F_D + \varepsilon F_D = \frac{(F_B + F_D)\ (\tau) + T_d \cdot \left[F_B + F_D + 1/2\ \dot{F}_D\ td\right]}{F_o(\tau + t_d)}\ F_o - F_B$$

$$F_D + \varepsilon F_D = F_B + F_D + \frac{1/2 \dot{F}_D td^2}{\tau + td} - F_B$$

$$\varepsilon F_D = \frac{\dot{F}_D\ td^2}{2(\tau + td)}$$

$$\dot{\varepsilon_R} = \frac{C}{f_t}\ \frac{\dot{F}_D\ td^2}{2(\tau + td)} \approx 1/2\ \frac{a\,td^2}{\tau}$$

FIGURE 4-17 EFFECT OF DELAY ON RANGE RATE ERROR MEASUREMENTS

$$\dot{\varepsilon}_R \text{ max.} = 61{,}000\ td^2 \text{ cm/sec}$$

$$= 2{,}000\ td^2 \text{ ft/sec}$$

where td = delay time in seconds

Even if the maximum likely delay time is less than one millisecond it is seen that the maximum possible error caused by the delay will not exceed 0.06 cm/sec (0.004 ft/sec). Figure 4-18 shows that for the nominal system parameters assumed throughout this report (i.e. $S_S = 10^{-10}$, S/N $\geq$ 10 dB and τ integration = 0.5 seconds) the effect of the delay on the total system error is negligible for time delays in the range from 100 to 1000 microseconds. At a maximum time delay of about 5000 μs, the range rate error from acceleration effects becomes as high as 1.52 cm/sec, making this a significant error source. Thus, as long as the time delay is less than 1000 μs, the errors caused by acceleration effects are small when compared with the other error sources.

If the clock stability is reduced to 10^{-11} the total RSS error is reduced by a factor of 2, as shown in Figure 4.19. At this clock stability the effect of the delay is still negligible for allowable time delays of 100 to 1000 microseconds. The quantization error becomes the most significant error if the S/N ratio > 10 dB.

Thus, it is seen that for the coincidence extractor that supplies both clock and doppler counts, the effects of the time delay on total error is negligible if the time delay is in the range from 100 to 1000 μs. For good range rate resolution (quantization error) the maximum time delay limitation should be no less than 100 μs.

4.4.5 CARRIER FREQUENCY ACCOMMODATION

In order to prevent resonances between the bias frequency and clock frequency in the coincidence detector, it is desirable to maintain a nearly constant bias frequency if the S-band frequency is changed. The S-band transponder

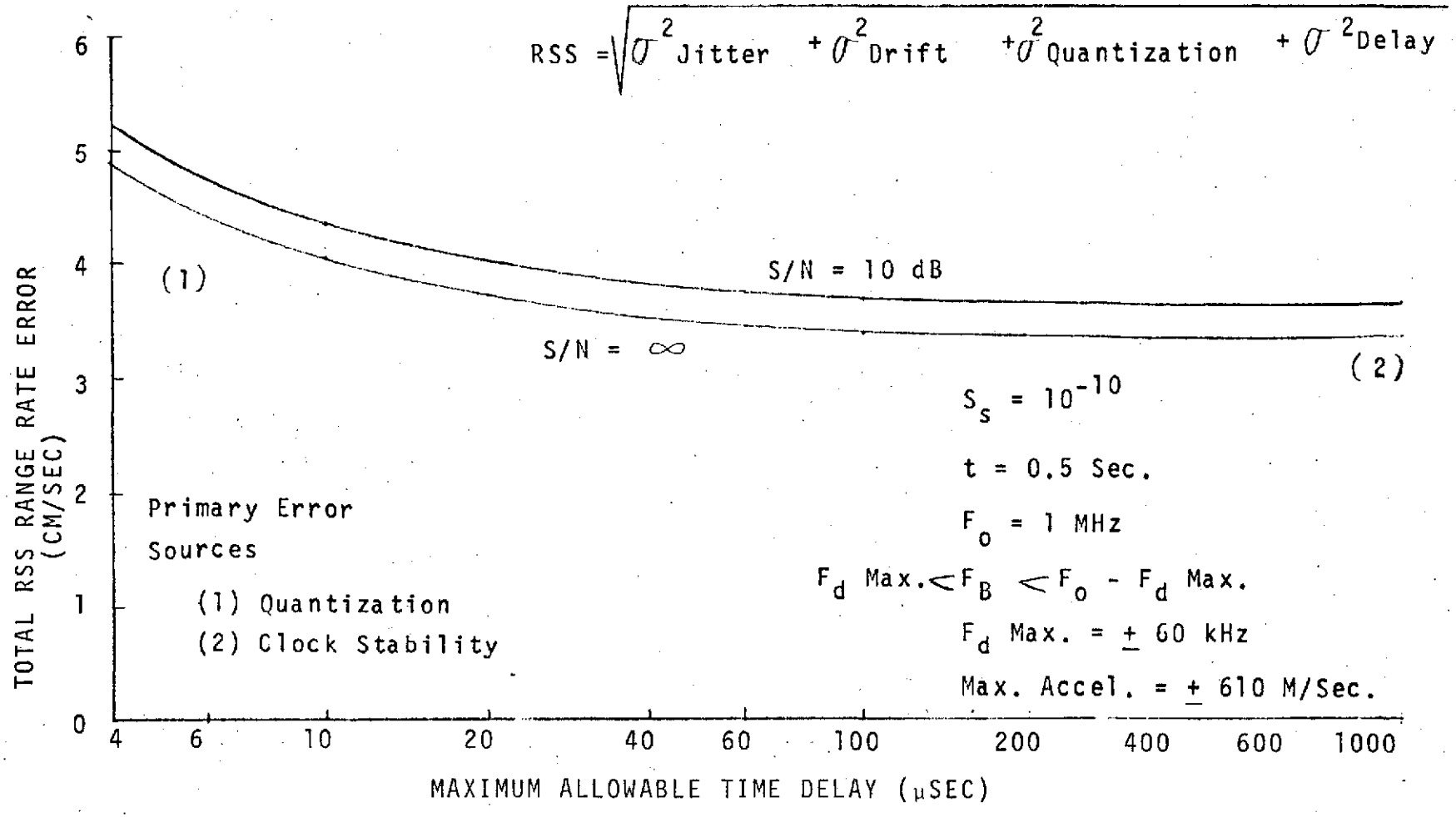


FIGURE 4-18 EFFECT OF TIME DELAY ON TOTAL SYSTEM ERROR

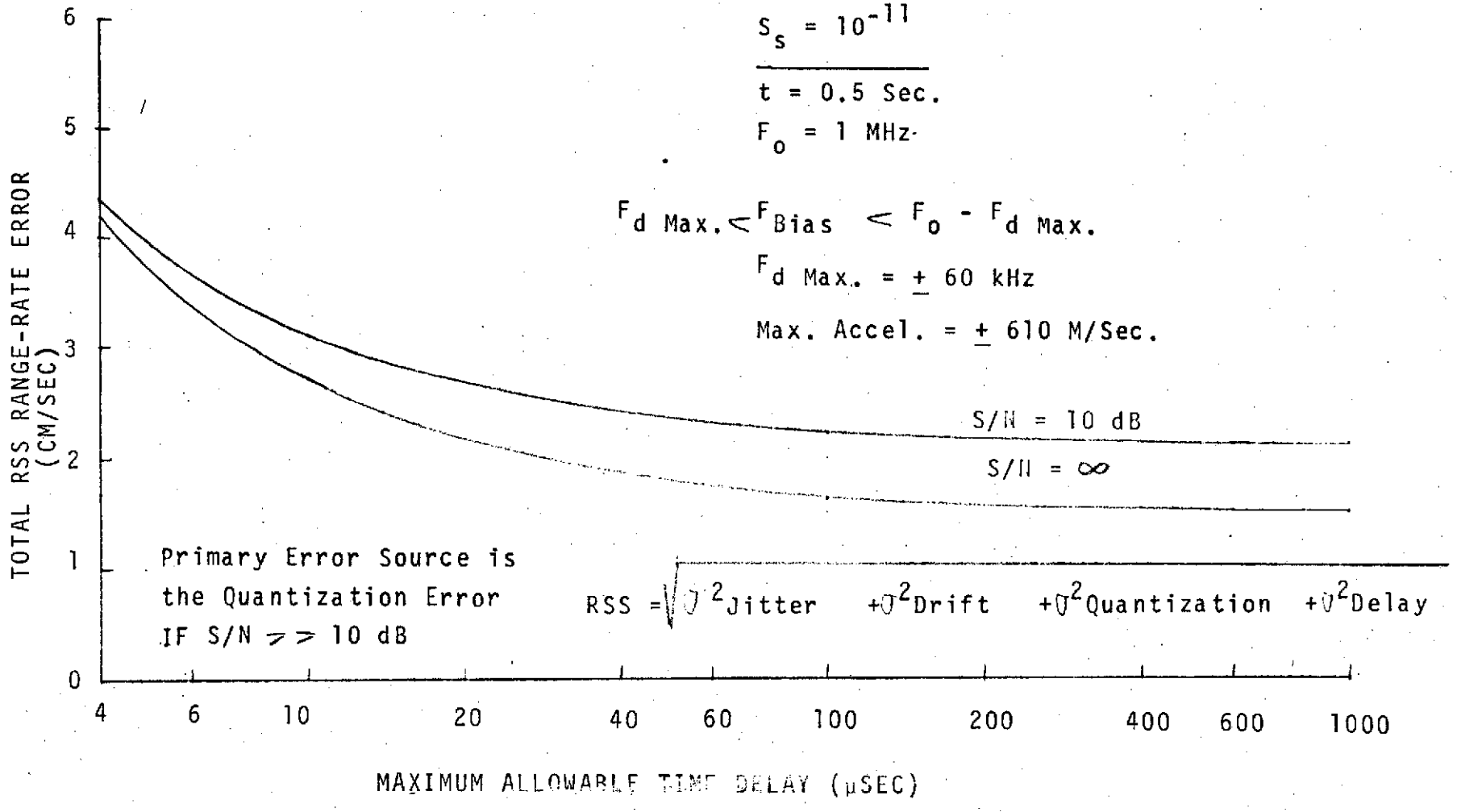


FIGURE 4-19 EFFECT OF TIME DELAY ON TOTAL SYSTEM ERROR

VCO frequency maintains a constant ratio to the S-band frequency, so that, if the S-band frequency is changed, the VCO injection frequency to the extractor also changes.

For example, if the S-band frequency is increased by 4.604 MHz, $\left[\frac{221}{240}\ (5\ \text{MHz})\right]$ the VCO output frequency increases by 1/6 MHz. If no changes were made in the extractor injection frequencies the bias frequency would increase from the nominal 1 MHz to 5.00 MHz (4 MHz change or 24 x 1/6).

To compensate for these changes and maintain a constant bias frequency, the reference oscillator injection frequencies should be changed by the same ratio as the VCO frequency.

A block diagram of a technique to accomplish this in the doppler extractor is shown in Figure 4.20. The fixed multiplier stage for the first mixer injection frequency (X 15 nominal), is replaced by divider and variable multiplier stages. The injection frequency is changed in 1/6 MHz steps as K is varied in unit steps, resulting in complete compensation of the change in the VCO output frequency, and a constant bias frequdncy of 1 MHz.

As the S-band frequency is increased, the doppler shift (for the same range rate) is increased proportionately. If the S-band frequency is changed over a 100 MHz range (5%), the maximum doppler shift on the bias frequency will change by less than 3 kHz. The extractor circuits can easily handle this increase without modification, but the software, which computes range rate (etc.), would need to compensate for the different proportionality between doppler and range rate.

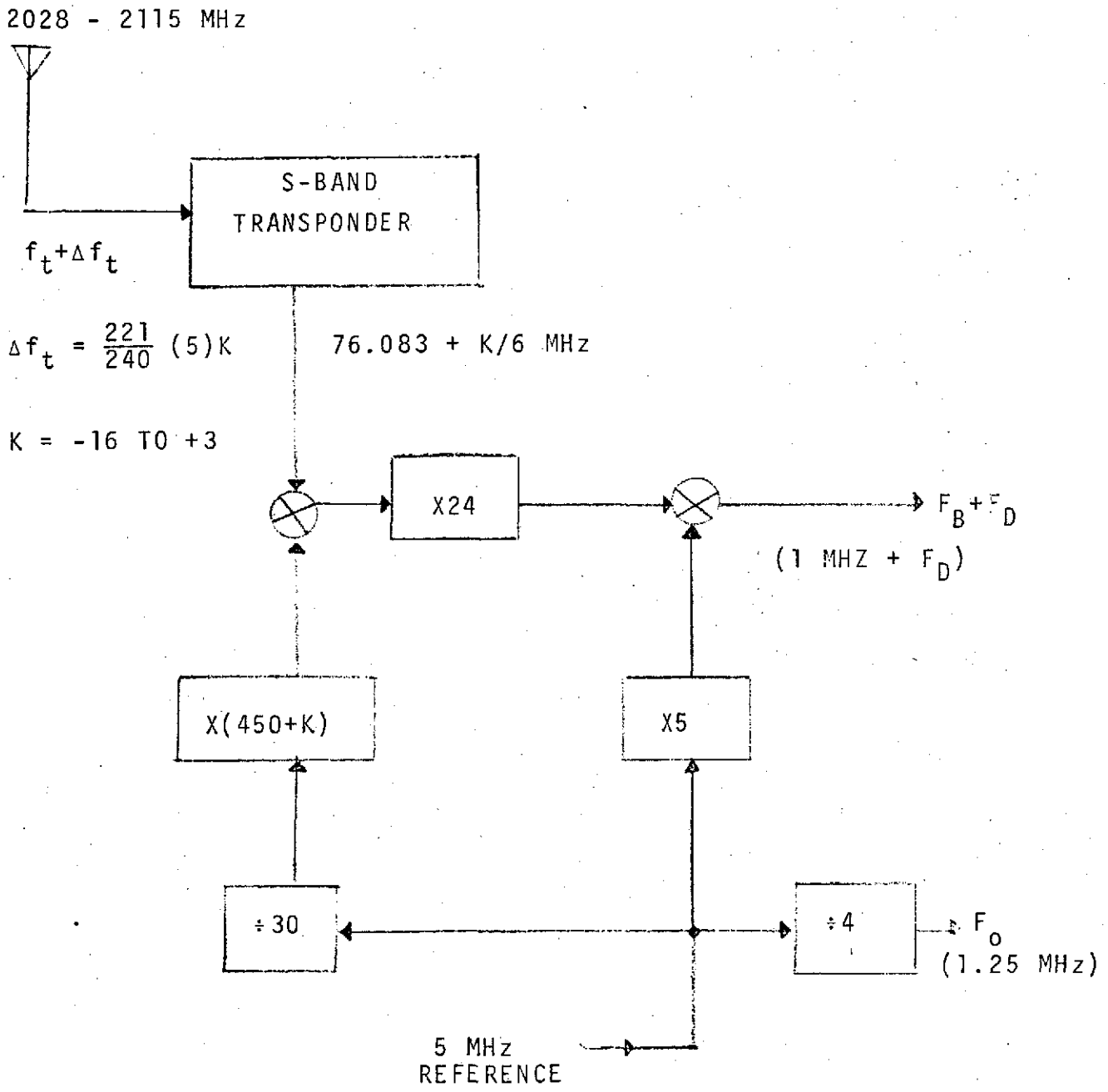


FIGURE 4-20 CARRIER FREQUENCY COMPENSATION TECHNIQUE

An alternate technique would be to use the multi-channel receiver described in Section 4.2.1.3. This receiver changes the reference oscillator injection frequencies and maintains a constant VCO output indepedent of the input S-band frequency. The doppler shift would still change with the input frequency so that software compensation would be required.

PART II

BREADBOARD DEVELOPMENT

This part of the report discusses the design, development and performance testing of the Vernier One Way Doppler Extractor. The operation of the breadboard unit and detailed schematics are also presented to aid the user in the operation and trouble shooting of the extractor. Major sections included in this part are:

SECTION 5

BREADBOARD REQUIREMENTS

The doppler extractor breadboard is required to meet specific performance and functional requirements as described in the Statement of Work and RCA proposals. A summary of these requirements are presented in this section.

5.1 PERFORMANCE REQUIREMENTS

The doppler extractor is required to measure and extract the doppler frequency from an S-band reference frequency derived from an S-band transponder. The accuracy and conditions under which the accuracy must be obtained is as shown in Table 5-1. As the table indicates, the doppler frequency must be measured to a fraction of a cycle. To achieve this precision requires that the S-band frequency and internally generated mixing frequencies be stable to at least one part in 10^{10}. Further, the error requirements prohibit the use of conventional frequency counting techniques since these techniques produce a quantization error of up to one whole cycle.

5.2 FUNCTIONAL REQUIREMENTS

In addition to the performance requirements, the breadboard model of the doppler extractor is required to provide the following functions.

1. Nondestructive doppler and time counters for periods up to 600 seconds shall be provided ,including an overflow indication when the 600 second period is exceeded.

2. Destructive doppler and time counters shall be provided, with the counters being reset to zero at the start of each new integration period.

3. Switch or computer selectable non-destructive and destructive counting modes shall be provided.

4. Switch selectable integration and readout periods of 0.5, 1, 2, 10, 60 and 600 seconds shall be provided with automatic display of each new measurement.

TABLE 5-1

BREADBOARD PERFORMANCE REQUIREMENTS

ERROR TYPE	INTEGRATION PERIOD (SEC)	MAXIMUM VALUE		
		CYCLES	FREQUENCY (Hz)	RANGE RATE (CM/SEC)
NOISE ERROR (RANDOM)	0.5	0.3	0.6	8.6
	2	0.5	0.25	3.6
	10	2.3	0.23	3.3
	60	12	0.20	2.9
	600	120	0.20	2.9
BIAS ERROR	24 HOURS	-	2.0	28.5

RANGE RATE: 0 to $\pm$ 8230 Meters/Sec

0 to $\pm$ 60,000 Hertz

LINE OF SIGHT ACCELERATION:

0 to $\pm$ 610 Meters/Sec^2

0 to $\pm$ 4300 Hz/Sec

MAXIMUM INTEGRATION INTERVAL VARIATION:

$\pm$ 100 Microseconds

MAXIMUM ERROR IN MEASURED INTEGRATION INTERVALS:

$\pm$ 100 Nanoseconds

5. A manual mode shall be provided with an anytime start command and an anytime stop command. The time between these successive commands shall be used as the integration period and the desired data shall be displayed after the stop command.

6. A computer controlled mode shall be provided with an anytime start command and an anytime stop command. Doppler and time count data shall be transferred to the computer after the stop command.

7. A computer controlled mode shall be provided where the computer selects a fixed integration time of 0.5, 1, 2, 10, 60 or 600 seconds. At the end of the integration period data shall be available for transfer to the computer.

8. Test points shall be provided for external monitoring of the readout time synchronization.

9. The breadboard model will be tested and test documentation prepared to verify that these performance/and functional requirements are met.

5.2.1 EXTRACTOR DISPLAYS

The doppler extractor breadboard shall include a microprocessor to calculate a number of parameters for display purposes. Any of the following parameters shall be switch selected for readout on a 9 decimal digit display.

a. Bias plus doppler frequency counts
b. Clock counts for the integration interval
c. Doppler frequency in Hertz
d. Velocity in meters/second based on the actual transponder frequency
e. Slant range difference in meters based on the actual transponder frequency.

A second 3 decimal digit display shall be provided which will show, by switch selection, either:

a. Time delay between the stop command and the actual stop execution, or
b. The difference between the nominal and the actual integration time for any of the fixed integration periods.

5.2.2 SELF TEST FUNCTION

The breadboard shall have an end-to-end self test capability which can be initiated either manually or under computer control. A known frequency shall be injected near the front of the doppler extractor. This frequency shall be measured and any of the parameters listed under 5.2.1 shall be displayed. In addition, a comparison against a stored reference value shall be performed. Agreement between the test signal and the reference shall result in lighting a "Data Good" light and providing a discrete output to the computer.

SECTION 6
BREADBOARD DESIGN DESCRIPTION

6.1 BREADBOARD CONFIGURATION

The doppler extractor breadboard implemented by RCA uses the vernier extraction technique to resolve the quantization error. The breadboard unit accepts a 76,083 MHz signal from an S-band transponder and contains the necessary circuitry to perform RF and digital processing to extract the doppler and doppler related information from the input.

The RF processor translates and multiplies the input frequency to obtain a suitable bias frequency containing approximately the full S-band signal. It also generates a self test signal for the self test modes. The digital processor performs the functions of coincidence detection, digital counting, timing, data processing and display, and interface formatting for a UNIVAC 1218 computer.

The photograph of Figure 6-1 shows the extractor as delivered to NASA. The unit measures 21 inches wide, 17 inches high and 18 inches deep. The front panel contains push buttons to select any of the functions described in Section 5. Computer control of the functions override the push buttons and is obtained through cable connectors at the rear of the unit. Multicolored LED lamps indicate whether the unit is in the manual mode (red LED's) or the computer mode (green LED's). A nine digit LED display indicates one of the following switch selectable quantities: raw doppler or time interval counts, computed doppler shift (Hertz), computed range rate (meters/second) or computed change in range (meters). An additional 3 digit LED display indicates the time interval delay in either raw clock counts or in microseconds.

A view of the extractor chassis is shown in the photograph of Figure 6-2. The RF and digital processing sub-chassis are indicated. The input and output connectors are shown in the rear panel photograph of Figure 6-3. Reading from left to right these connectors are computer input (from 1218 output),

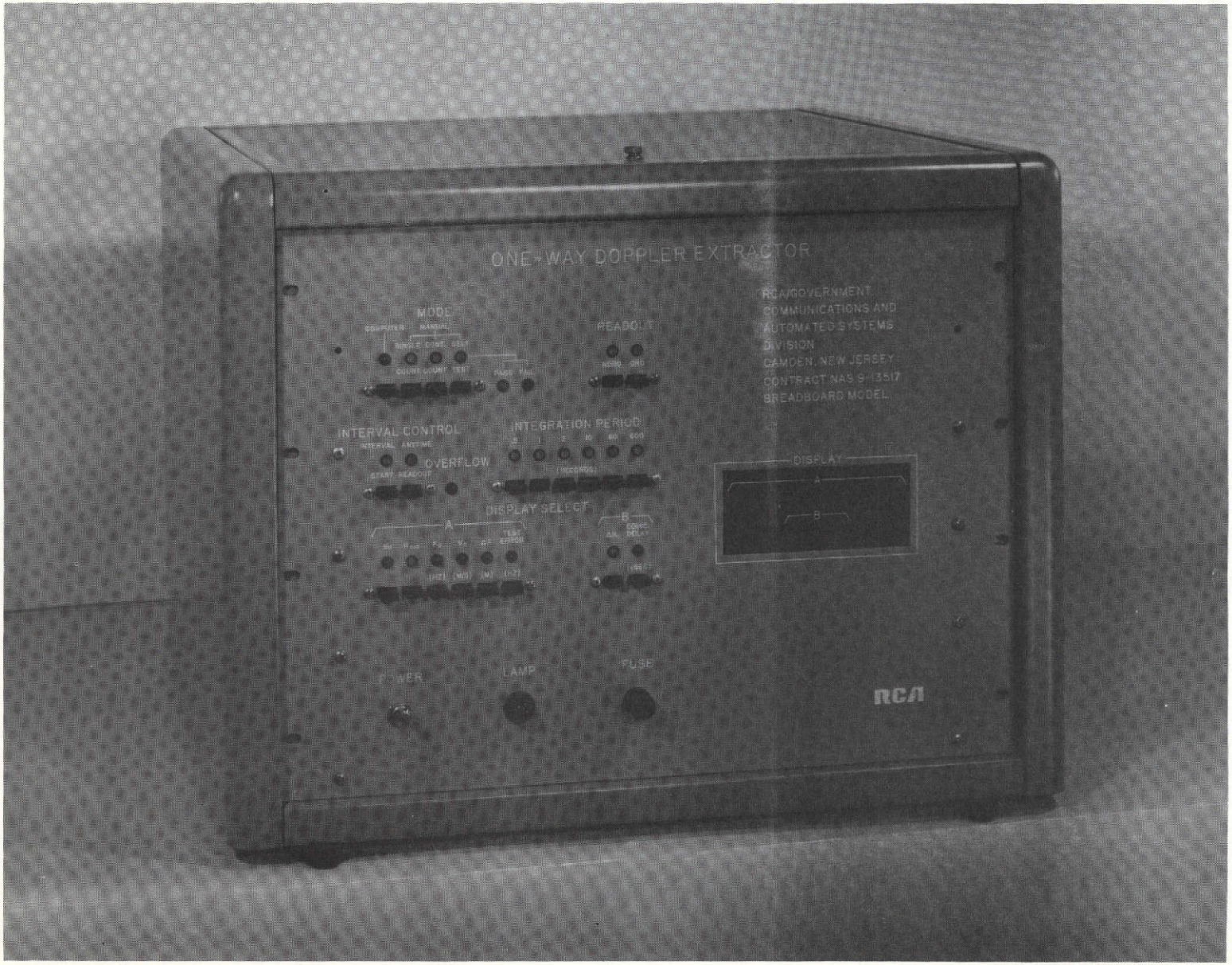


FIGURE 6-1 ONE-WAY DOPPLER EXTRACTOR BREADBOARD

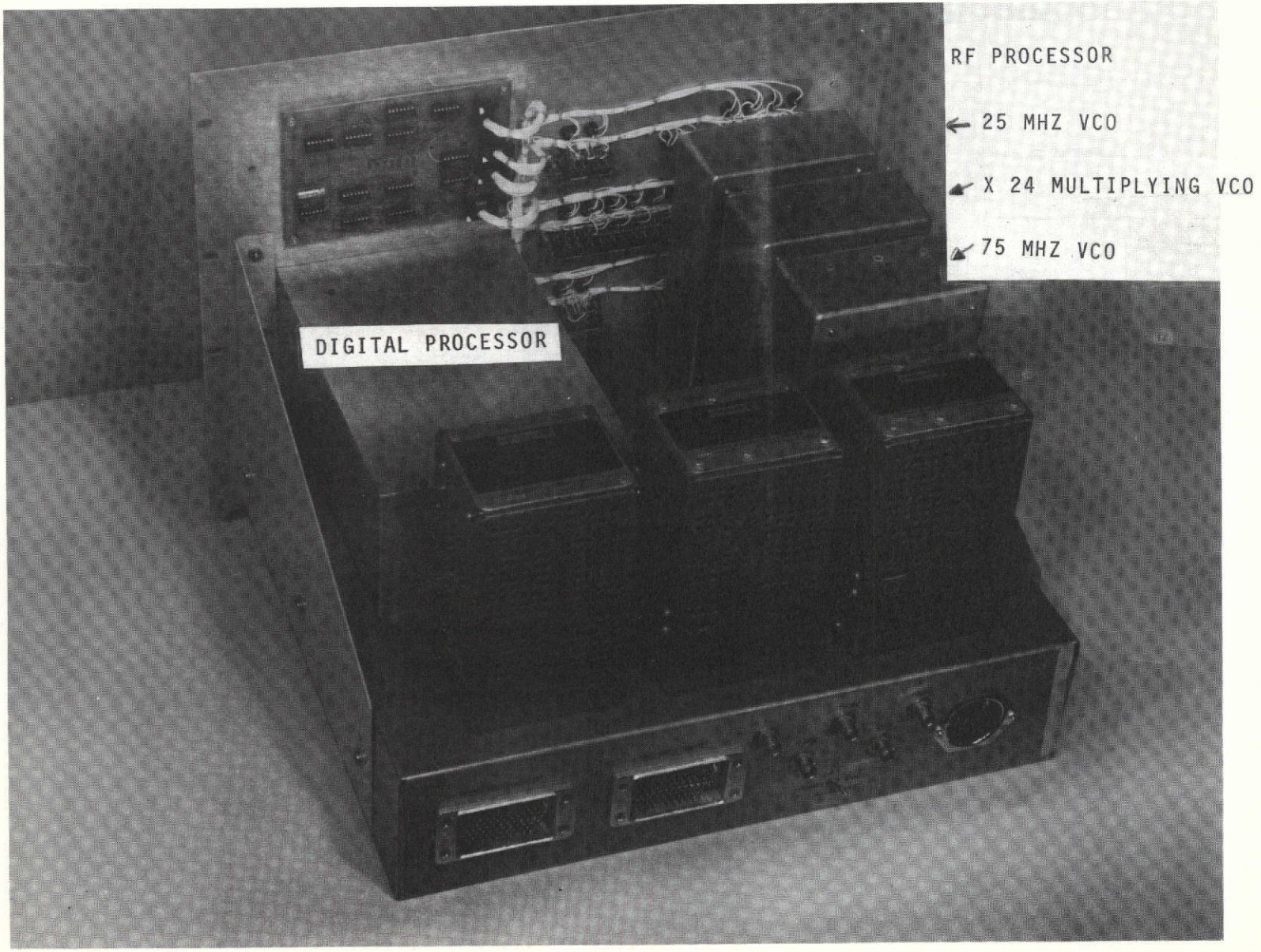


FIGURE 6-2 ONE-WAY DOPPLER EXTRACTOR CHASSIS

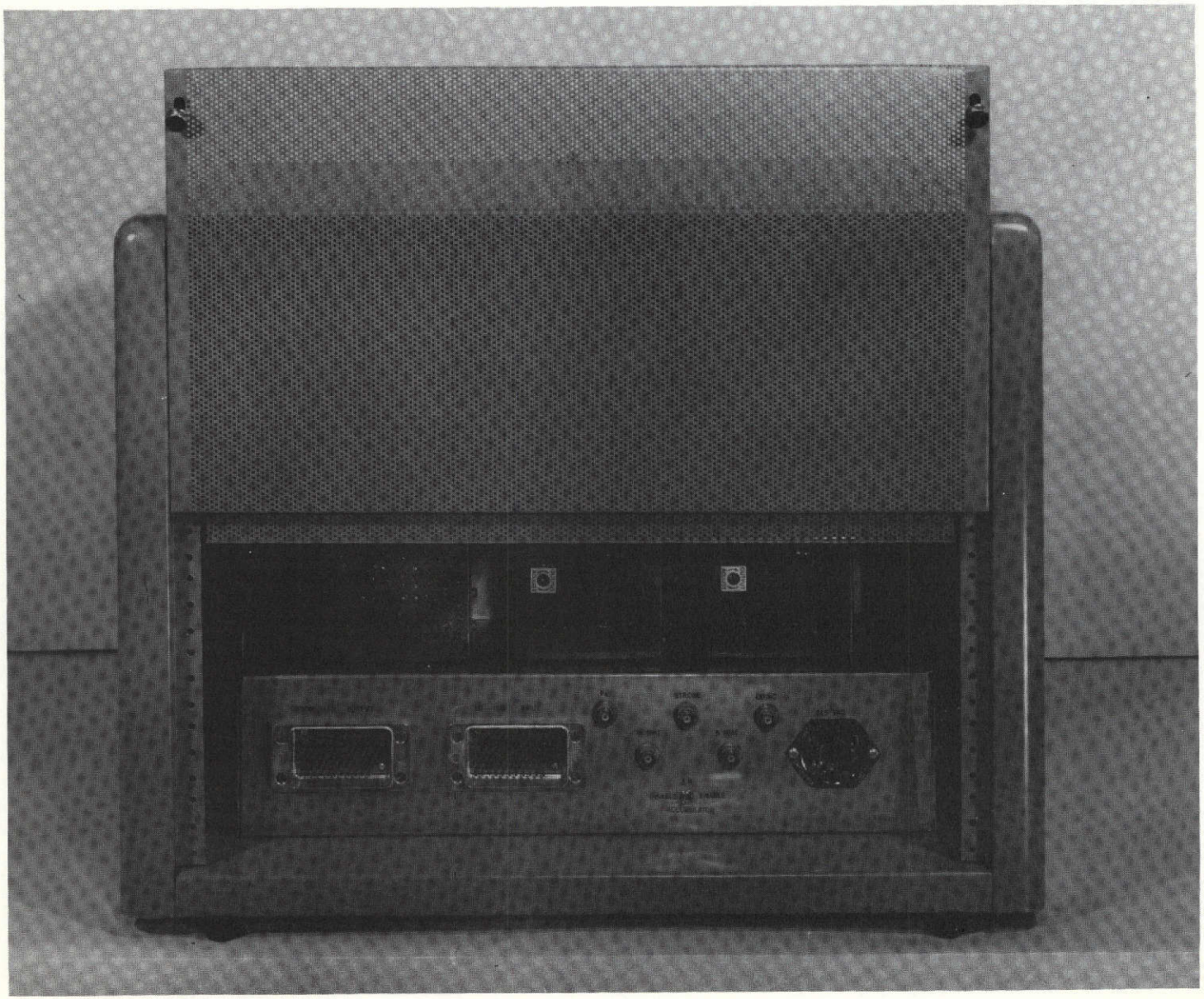


FIGURE 6-3 ONE-WAY DOPPLER EXTRACTOR INPUT/OUTPUT CONNECTORS

coincidence clock frequency input (F_o), S-band transponder frequency input (76 MHz), counter start/stop commands (STROBE), 5 MHz clock reference frequency (5 MHz), coincidence detector output (COINC) and 115V AC.

6.1.1 TECHNIQUE DESCRIPTION

A top flow diagram of the one-way doppler extractor environment is shown in Figure 6-4. The S-band transponder receives the doppler shifted transmitted frequency and outputs a 76.083 MHz reference signal containing 8/221 parts of the original S-band doppler. The doppler extractor performs RF processing to restore approximately full doppler on a 1 MHz bias frequency and performs digital processing to extract doppler counts, time interval counts, display data and computer interface logic to a UNIVAC 1218 computer. The timing circuits operate from an external 5 MHz frequency standard.

A block diagram of the extractor is presented in Figure 6-5 showing some of the internal functions performed by the RF and digital processors. As shown in the figure, the transponder signal enters the RF processor which performs frequency shifting and multiplication resulting in a doppler shift up to $\pm$ 60 kHz superimposed on a 1.00 MHz bias signal. The 76.083 MHz is mixed with a 75 MHz fixed injection frequency to obtain a 1.083 MHz plus fractional doppler (f_d/27.625) S-band reference signal. This frequency is then multiplied by 24, resulting in a 26 MHz output containing 192/221 parts of the original S-band doppler shift. The 26 MHz signal is then mixed with a 25 MHz fixed injection to obtain the desired 1 MHz containing nearly the full S-band doppler shift. The coincidence clock frequency (Fo) of 1.25 MHz is obtained by dividing the 5 MHz clock by a factor of 4.

The above frequencies were chosen for the breadboard unit for the following reasons:

1. The coincidence clock and bias frequencies should be approximately equal and at about 1 MHz for best utilization of CMOS logic and the coincidence technique.

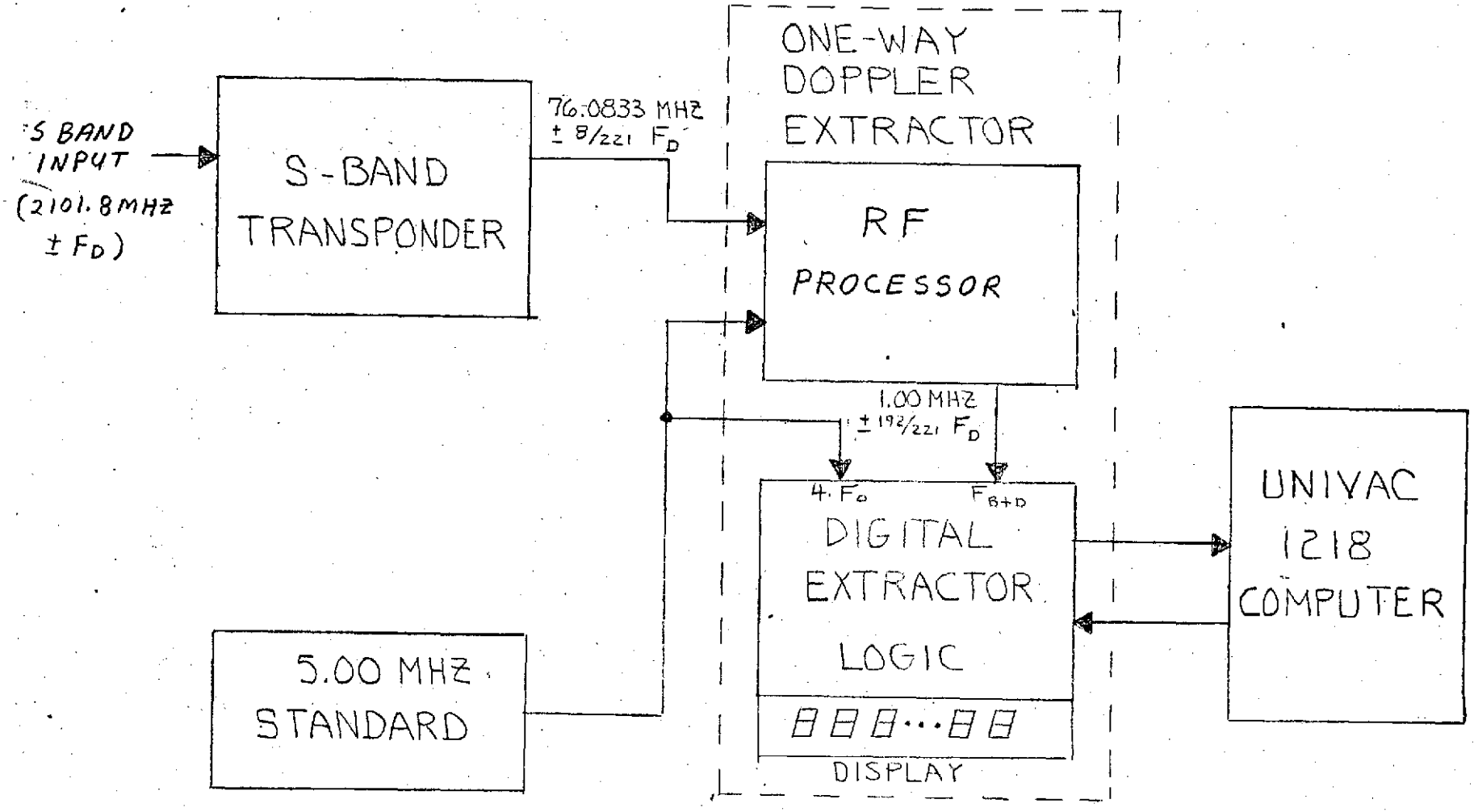


FIGURE 6-4 OWD EXTRACTOR ENVIRONMENT

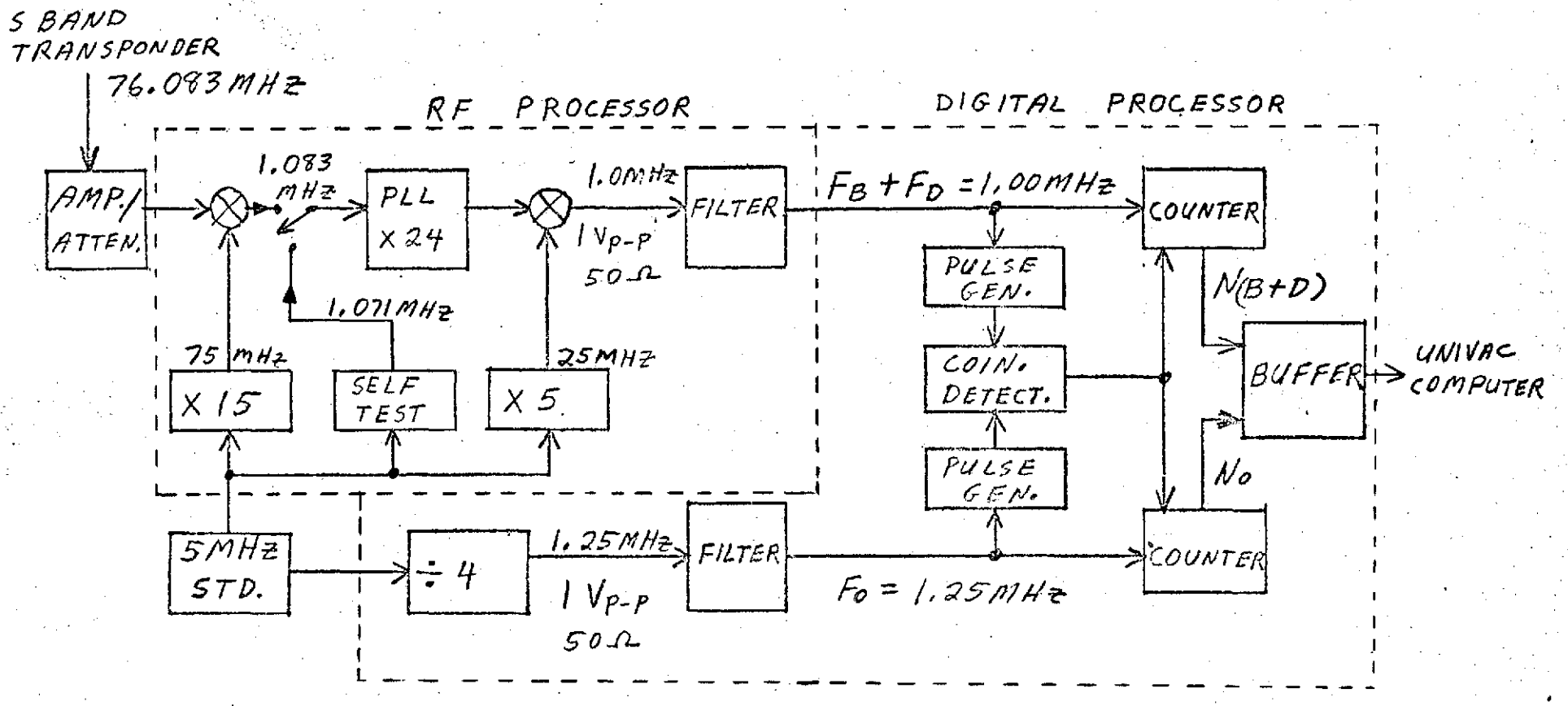


FIGURE 6-5 DOPPLER EXTRACTOR BREADBOARD BLOCK DIAGRAM

2. The injection frequencies should be low integer multiples of the clock for ease of generation and to obtain very clean injection frequencies.

3. The multiplying phase locked loop should have a multiplication factor that restores most of the original S-band doppler.

Other frequencies could be used in the extractor at the expense of increased circuit complexity.

The digital processor circuits of Figure 6-5 contain the pulse generators and coincidence detector required for the vernier extractor concept. The bias plus doppler and coincidence clock frequencies are converted to narrow pulses at each zero crossing and these pulses are fed to the coincidence detector. The coincidence detector responds to a pulse coincidence by generating a timing pulse. This pulse plus internal timing logic causes the counters to transfer their counts to the buffers at desired intervals. At coincidence, the quantization error is reduced to a small timing error due to a finite pulse width.

Two counters count zero crossings of the F_B+D and F_o signals. For non-destructive readout(NDRO), the counters run continuously. For destructive readout (DRO), the counters are reset at the beginning of each count interval. The two counter outputs ($N_{(B+D}$ and N_o) are stored in the buffers for computer sampling as desired. The buffer circuits also contain interface circuitry to convert the counts into coded words for the UNIVAC 1218 computer.

The self test function tests the operation of the doppler extractor from the output of the first mixer to the computer interface. A block diagram of the technique is shown in Figure 6-6. A test frequency is obtained from the 75 MHz first mixer injection oscillator by dividing this frequency by 70. Derivation of the test frequency from the 75 MHz oscillator is preferred over up converting from the 5 MHz standard, since the former technique also tests the lock condition of the

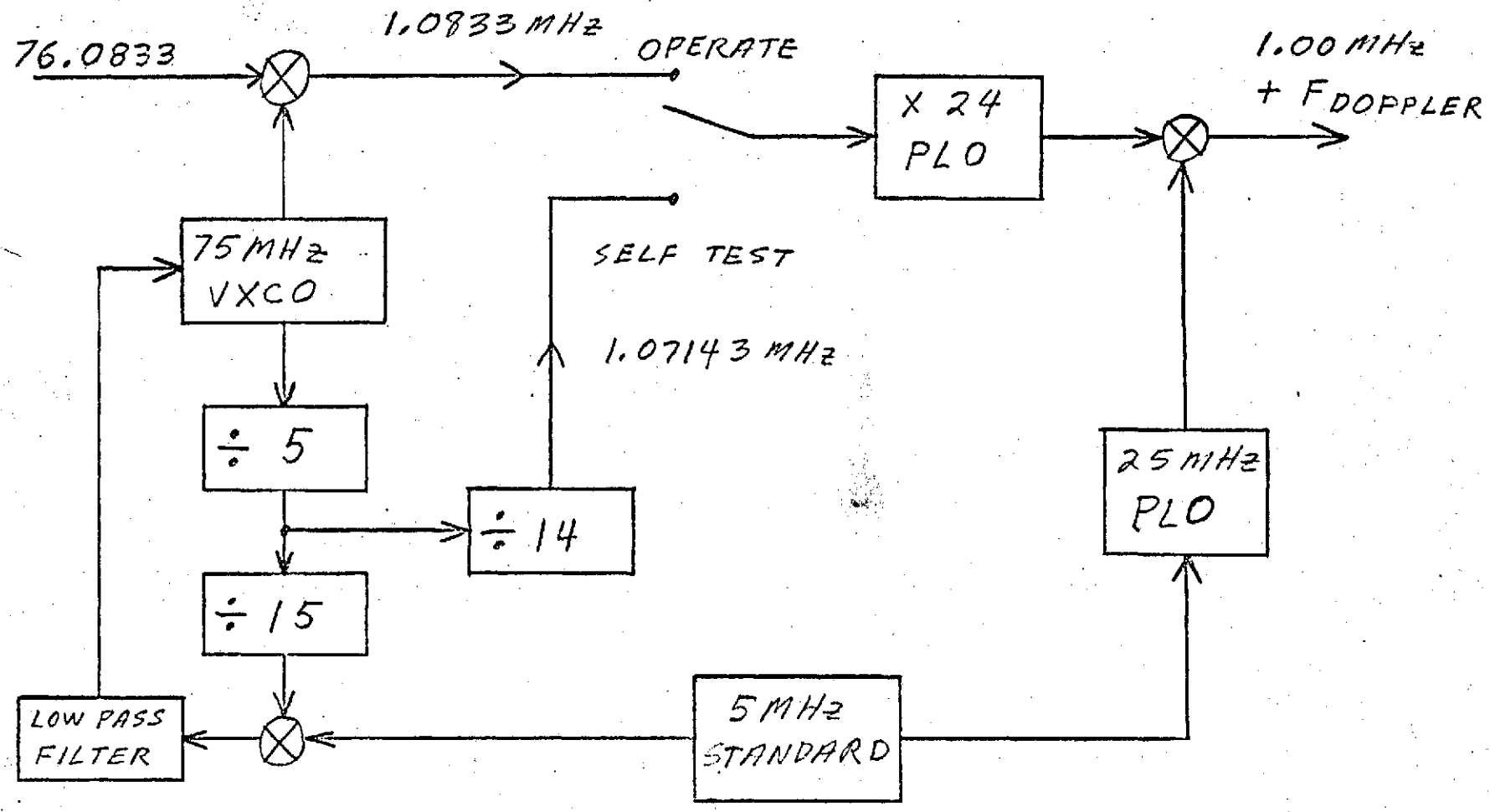


FIGURE 6-6 SELF TEST IMPLEMENTATION BLOCK DIAGRAM

75 MHz oscillator to the 5 MHz standard. The resultant frequency of 1,071,428.57 Hz is substituted for the nominal mixer output frequency of 1.083,333,33 Hz. After multiplication by 24 and differencing with the 25 MHz injection frequency, the resultant bias plus doppler frequency into the coincidence detector is 714,285.7 Hz. Since the nominal bias frequency is 1 MHz, the resultant equivalent doppler frequency at the extractor display will be -285,714.3 Hz when all components are working correctly. When converted to an equivalent S-band doppler shift (X $^{221}/_{192}$) the self test signal will represent a doppler shift of -328,869.05 Hz.

During the self test the extractor compares the actual measured doppler with a stored value of -285,714.3 Hz. If the two frequencies agree within a few Hertz a data good signal is sent to the 1218 computer and a "data good" indication lights on the front panel of the extractor.

The self test technique described above tests all components of the extractor with the exception of the first mixer. A highly stable test signal could have been injected at the input of the first mixer to also test this component. To obtain a test signal of adequate spectral purity and stability would require circuitry too complex to be incorporated into the present chassis. The test signal frequency must be within a few kilohertz of 76.083 MHz due to the bandwidth limitations of the X24 phase locked oscillator. The resultant increase in hardware to generate a stable test signal at the input was not worth the added advantage of testing the operation of a high reliability mixer.

6.2 RF PROCESSOR DESCRIPTION

The RF processor accepts the 76.083 MHz plus fractional doppler transponder signal and converts it to a 1 MHz bias frequency containing approximately the full S-band doppler shift. The RF processor generates the required injection frequencies, the doppler multiplication, the desired 1.25 MHz coincidence clock frequency and the self test injection frequency. A detailed

design description of each of these functions is included in the following paragraphs.

6.2.1 75 MHz PHASE LOCKED OSCILLATOR

The 75 MHz first injection frequency is generated from the 5 MHz reference using a phase locked oscillator and divider circuit. A block diagram of the 75 MHz phase locked oscillator is shown in Figure 6-7. The 5 MHz clock input is amplified by Q1 to obtain the TTL input requirement of the MC 4344L phase detector. The Q1 amplifier also served as isolation from other 5 MHz clock circuitry. In addition to a phase detector the MC 4344L also includes a charge pump and an amplifier circuit.

The output of the MC4344L is fed to the varactor tuned voltage controlled oscillator (VCO) which is nominally tuned to 75 MHz. Two stages of amplification and a seven pole 75 MHz low pass filter follow the VCO output. The output of the 75 MHz filter provides + 10 dBm at 50 ohms as an injection frequency to be mixed with the 76.083 MHz from the transponder. Spurious outputs and harmonic related signals at the 75 MHz port are greater than 60 dB below the output level. The output of the first amplifier following the VCO is an emitter follower which supplies drive to the $\div$ N circuitry associated with the phase locked loop. A divide by 5 (SP622B) and divide by 3 (S54H76J) counter are cascaded to provide the proper division in the $\div$ N circuitry. A level translator Q3 is used to obtain the TTL input requirement of the divide by 3 counter.

Figure 6-8 is a detailed schematic of the 75 MHz/1.0714 MHz phase locked oscillator. The 1.0714 MHz output is used for the self test function. The MC4344L is used as a second order low pass loop filter as shown in the diagram below.

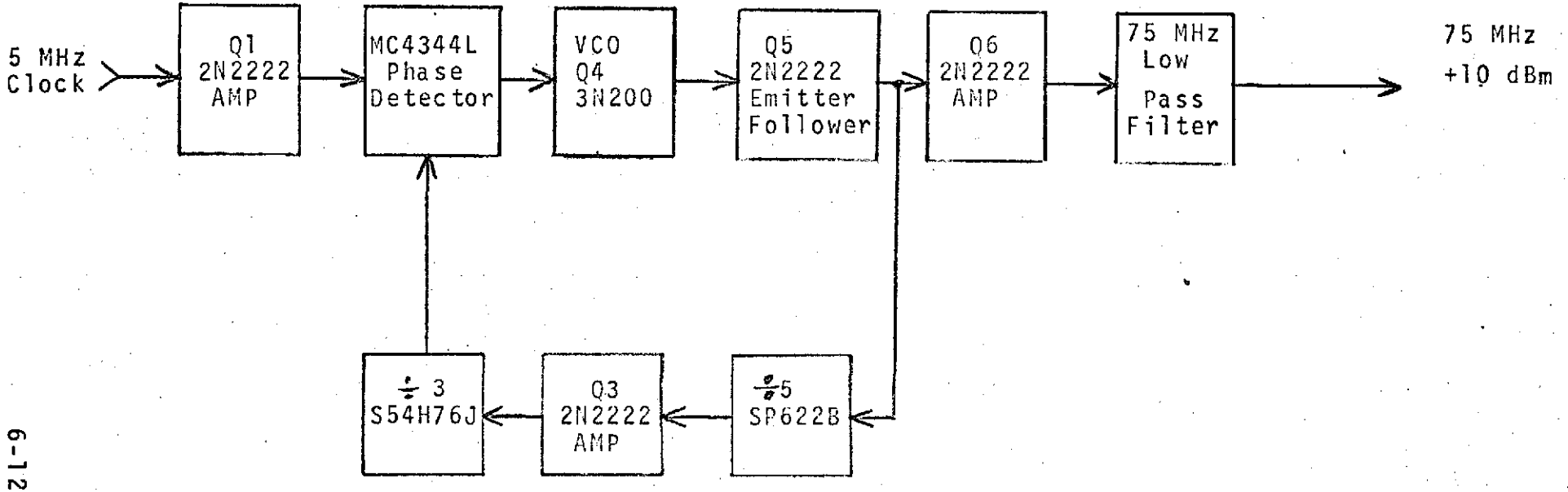


FIGURE 6-7 75 MHz PHASE LOCKED OSCILLATOR

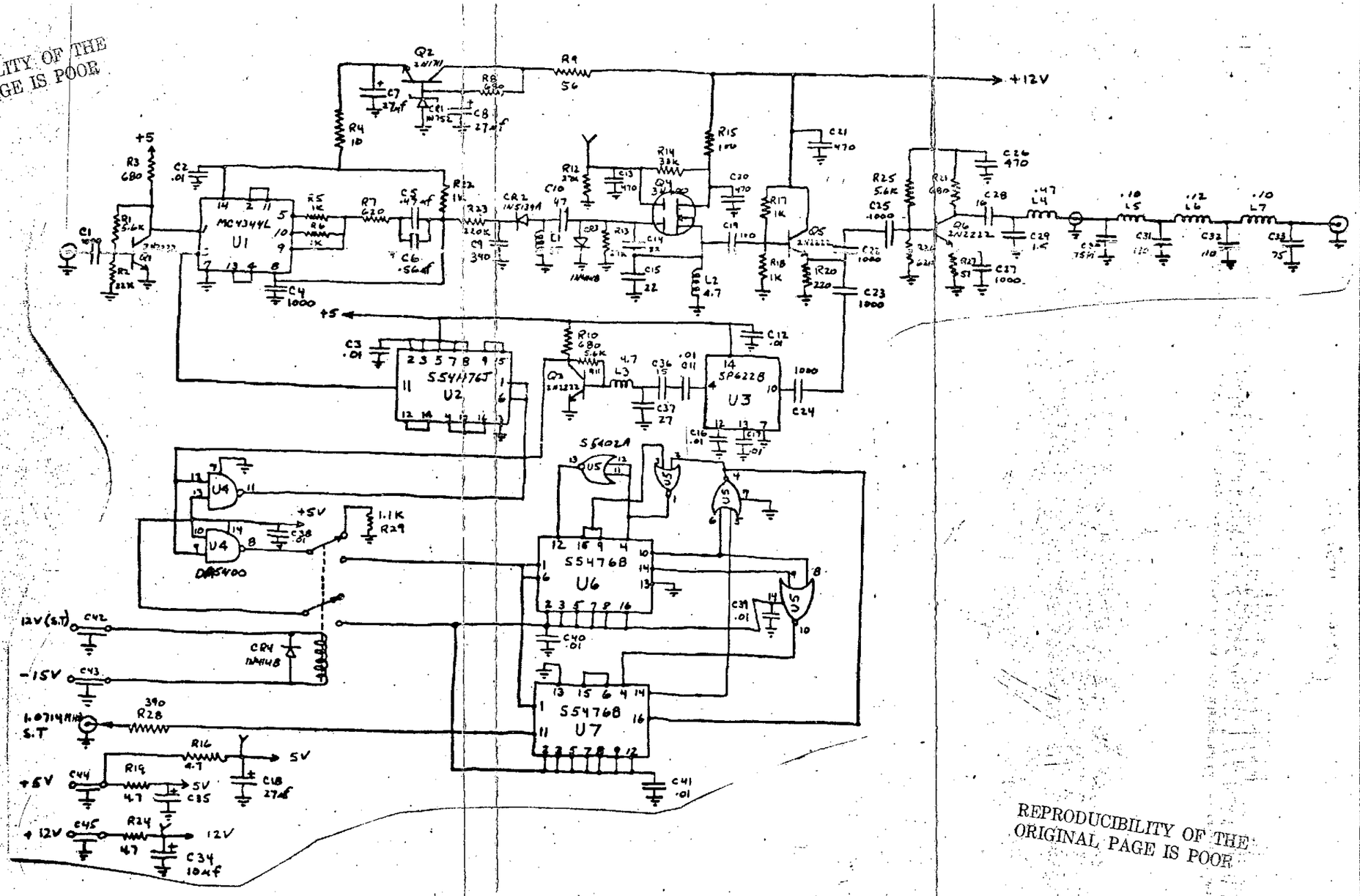
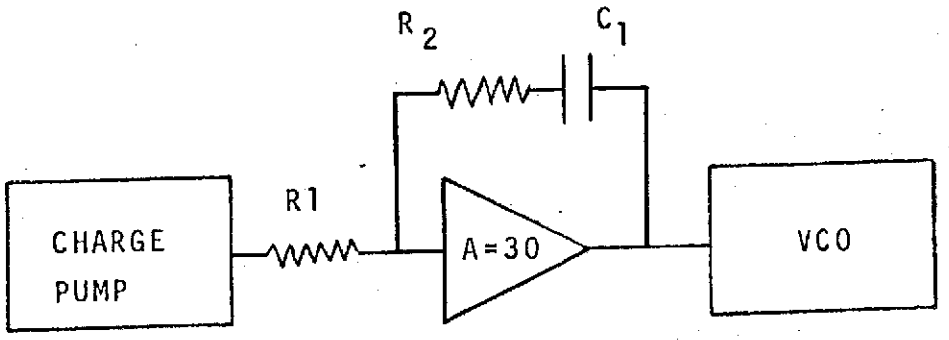


FIGURE 6-8: SCHEMATIC, 75 MHz PLL/1.0714 MHz SELF TEST GENERATOR



75 MHz Loop Filter Design

The loop transfer function for a second order system is given by

$$G(s)\ H(S) = K_p K_o K_n K_f$$

where

K_p = gain constant of phase detector in Volts/Radian (.1V/radian for MC 4344L)

K_o = K_v/S = gain constant of the VCO in radian/sec/volt
Measured as 1.4287×10^6 radian/sec/volt

K_n = Counter divide ratio = $\frac{1}{(5)(3)} = \frac{5}{15}$

K_f = Amplifier/Filter Gain

The K_f design is based on a maximum lock up time of 1.5 msec and a maximum overshoot of 15%. The amplifier in the MC 4344L has a gain of 30.

For a second order system with a dampening ratio of 1, a peak overshoot of less than 15% and settling to within 5% will occur at $W_n t = 4.5$.

$$W_n = \frac{W_n t}{t} = \frac{4.5}{1.5 \text{ msec}} = 3\ (10^3) \text{ rad/sec}$$

where W_n = loop bandwidth of the system

$$R_1 C_1 = \frac{k_p\, k_v}{W_n^2 N} = \frac{(.1)(1.4287)(10^6)}{\left[3(10^3)\right]^2 (15)} = 1.05 \quad (10^{-3})$$

With $R_1 = 1\ k\Omega$

$C_1 = 1\ \mu f$

$$R_2 = \frac{2\zeta}{C \cdot W_n} = \frac{2\ (1)}{(10^{-6}3)(10^3)} = 667\Omega$$

$$\therefore K_f = \frac{A\ (R_2 C_1 S+1)}{C_1\ (R_1+R_2 - A\ R_1)\ S+1}$$

$$K_f = 30\ \frac{\left(\frac{S}{1470}+1\right)}{\left(\frac{S}{35.31}+1\right)}$$

The loop transfer function is

$$G(s)\,H(s) = K_p K_o K_n K_f$$

$$= (.1)\left[\frac{1.43\ (10^6)}{S}\right]\left[\frac{1}{15}\right]\left[\frac{30\ \frac{S}{1470}+1}{\frac{S}{35.31}+1}\right]$$

$\therefore$ Gain = 109.13 dB

$\frac{1}{S}$ = - 20 dB/Decade @ W=1

$\frac{1}{S}$ = -20 dB/ Decade @ W=35.31

$\frac{1}{35.31}+1$

$\frac{S}{1470}+1$ = 20 dB/Decade @ W=1470

6.2.2 25 MHz PHASE LOCKED OSCILLATOR

A block diagram of the 25 MHz phase locked oscillator is shown in Figure 6-9. The block diagram and associated circuitry are similar to the 75 MHz phase locked oscillator with the exception of the $\div N$ circuitry which simply becomes a divide by 5 counter.

The output of the 25 MHz low pass filter provides +10 dBm into 50 ohms to be used as the injection signal when mixed with the output of the Doppler multiplier circuit.

A detailed schematic of the 25 MHz phase locked oscillator is shown in Figure 6-10. The loop transfer function is

$$G(s)\,H(s) = K_p K_o K_n K_f$$

$$= (.1)\left[\frac{5.049\ (10^6)}{S}\right]\left[\frac{1}{5}\right]\left[\frac{30\ \frac{S}{12255}+1}{\frac{S}{219}+1}\right]$$

The loop bandwidth is designed for $W_n = 4000$

$\therefore$ Gain = 129.63 dB

$\frac{1}{S}$ = -20 dB/Decade @ W = 1

$\frac{1}{\frac{S}{219}+1}$ = -20 dB/Decade @ W=219

$\frac{S}{12255} + 1$ = +20 dB/Decade @ W = 12255

6.2.3 DOPPLER MULTIPLIER PHASE LOCKED OSCILLATOR

The 76.083 MHz signal from the Transponder is mixed with 75 MHz from the phase locked oscillator and produces 1.083 MHz input signal to the Doppler multiplier phase locked oscillator. The

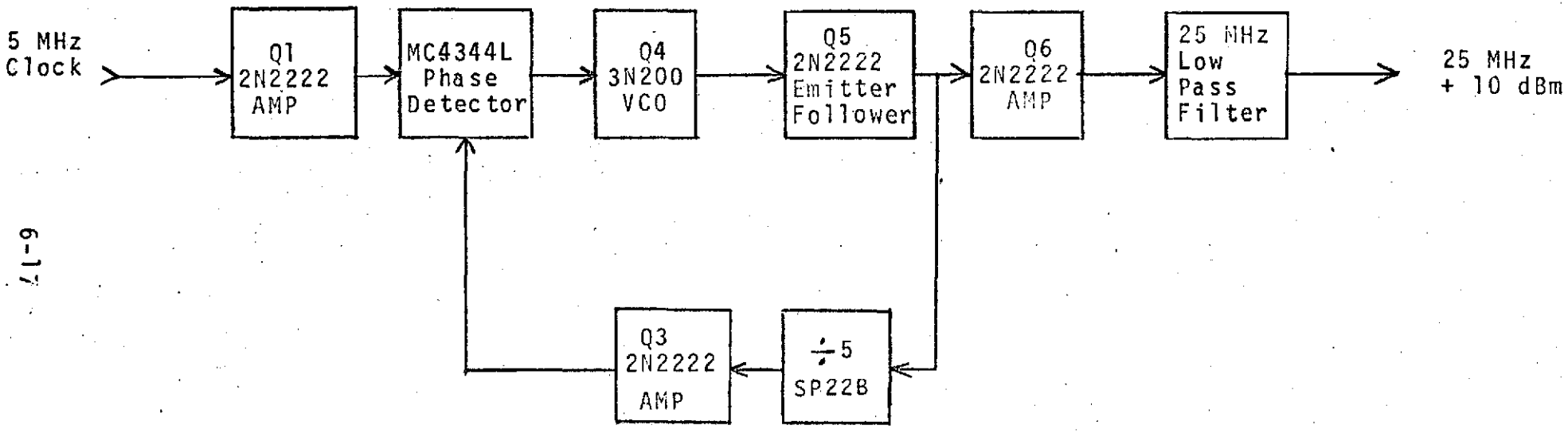


FIGURE 6-9 25 MHz PHASE LOCKED OSCILLATOR

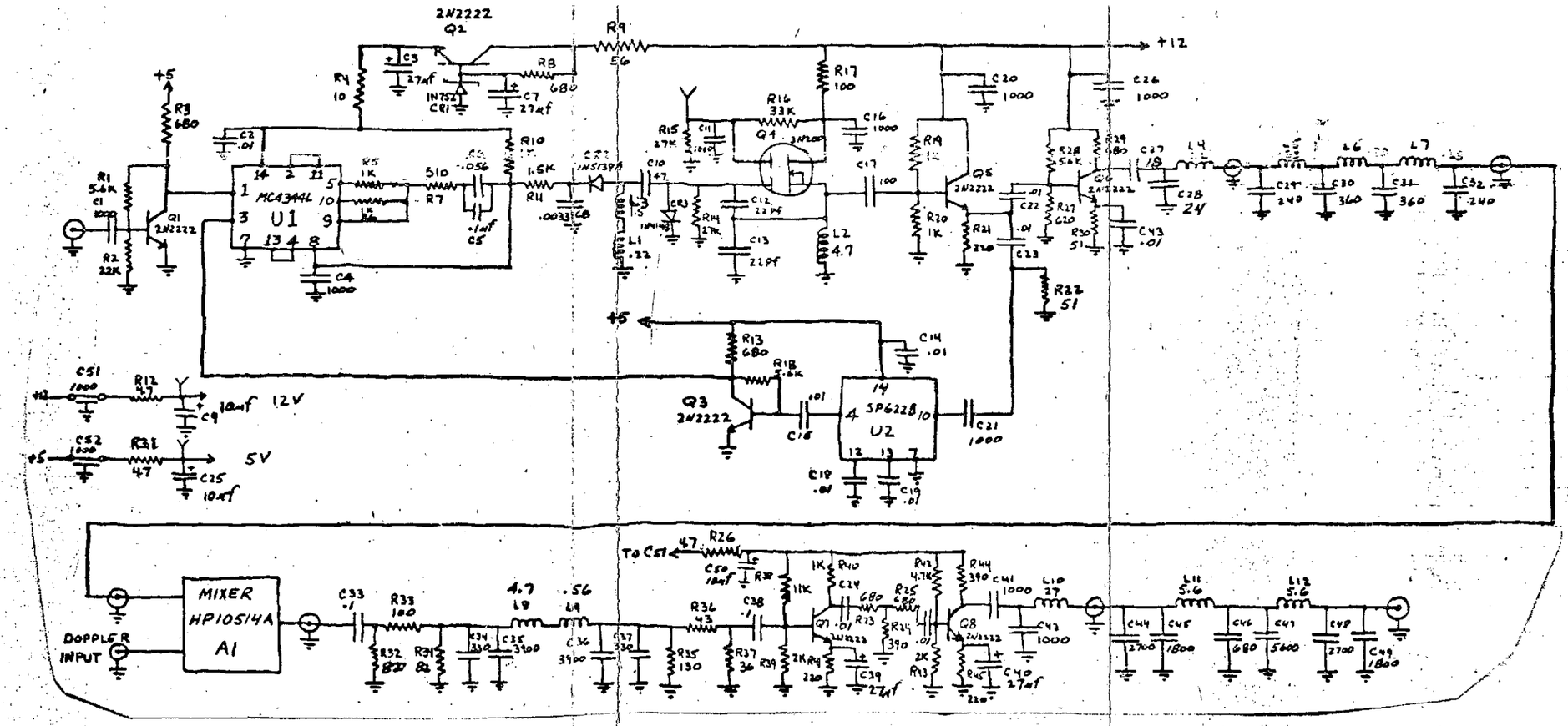


FIGURE 6-10: SCHEMATIC, 25 MHz PHASE LOCKED OSCILLATOR

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

FOLDOUT FRAME

FOLDOUT FRAME

1.083 MHz signal plus associated doppler frequency is then filtered and multiplied by 24 in the phase locked oscillator to produce a 26.0 MHz signal $\pm$ 24 times the doppler frequency present at the transponder 76.083 MHz port.

The emitter follower output of the doppler multiplier is fed to both a 5 pole 26 MHz low pass filter and the $\div$ 24 circuit of the loop. The divide by 24 circuit consists of a $\div$ 4 counter (MC 1232L) $\div$ 3 counter (S54H76J), and a $\div$ 2 counter (S8291A) cascaded to produce the proper division. Q6 translates the ECL output level of the $\div$ 4 to the TTL input level of the $\div$ 3 counter.

The output of the 26 MHz low pass filter provides 0 dBM at 50 ohms to be mixed with the 25 MHz phase locked oscillator to produce the 1.0 MHz bias plus doppler signal. This 1 MHz bias plus doppler frequency is filtered, amplified and again filtered to produce a 1.0 volt peak signal to the digital extractor circuit. A block diagram of the doppler multiplier is shown in Figure 6-11.

A detailed schematic is shown in Figure 6-12. The bandwidth of the Doppler Multiplier is 4 kHz. The transfer function is:

$$G(s)\,H(s) = K_p K_o K_n K_f$$

$$G(s)\,H(s) = \left[.1\right]\left[\frac{5.52(10^6)}{5}\right]\left[\frac{1}{24}\right]\left[\frac{30\left(\frac{S}{12561}+1\right)}{\frac{S}{1024}+1}\right]$$

Gain = 116.77 dB

$\frac{1}{s}$ = - 20 dB/Decade @ W=1

$\frac{1}{\frac{S}{1024}+1}$ = -20 dB/Decade @ W=1024

$\frac{S}{12561} + 1$ = +20 dB/Decade @ W=12561

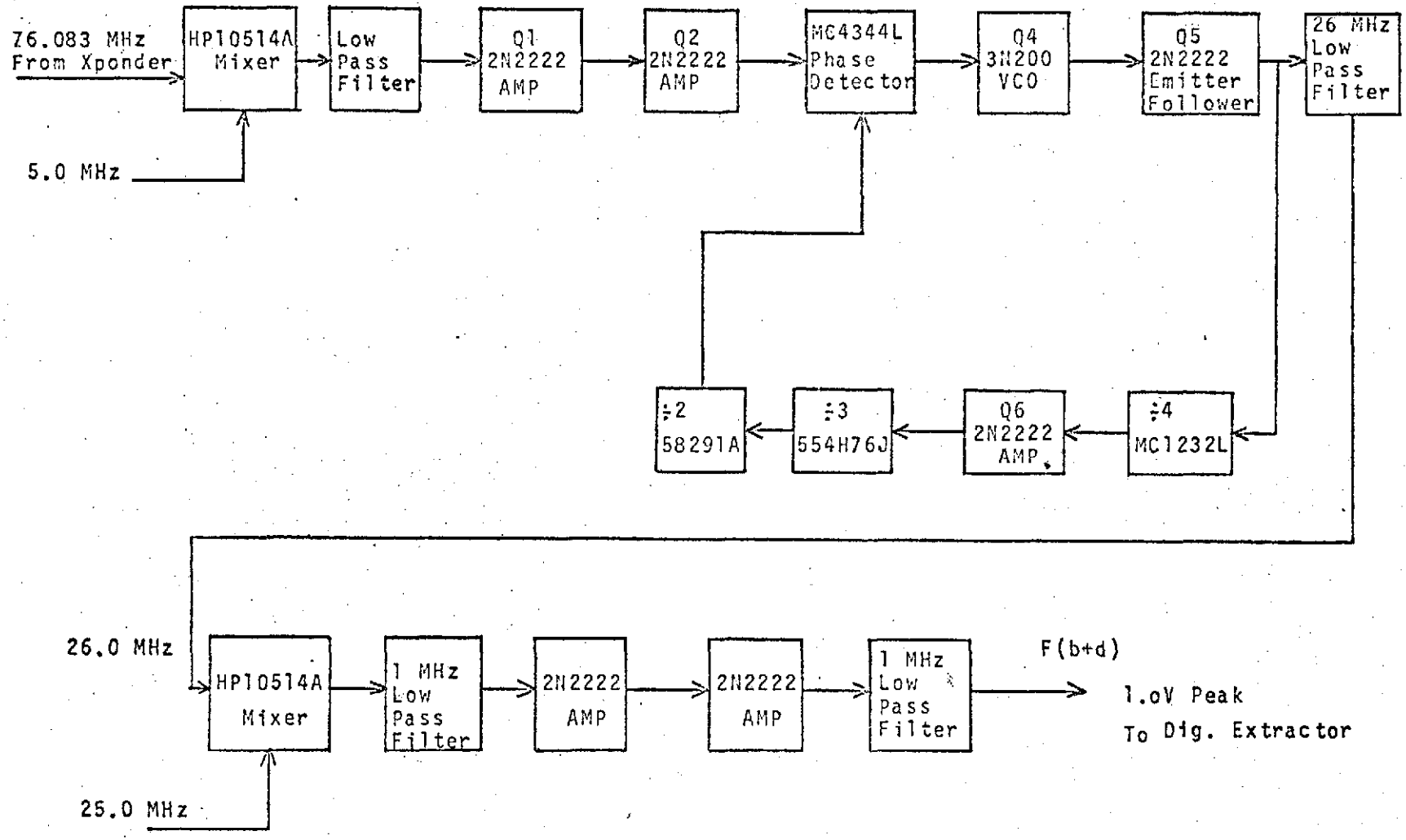


FIGURE 6-11 DOPPLER MULTIPLIER PHASE LOCKED OSCILLATOR

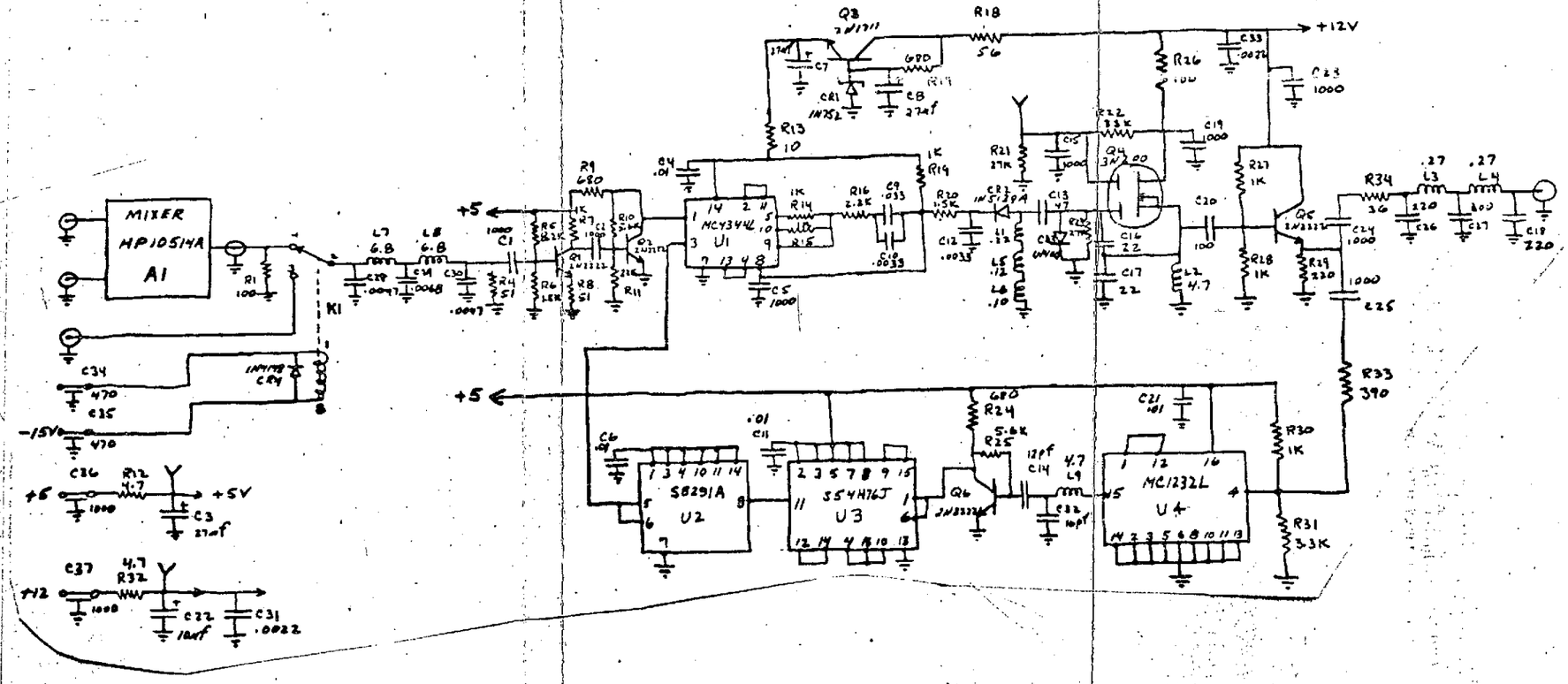


FIGURE 6-12: X24 DOPPLER MULTIPLIER PLL

6.2.4 SELF TEST SIGNAL

The self test frequency of 1.0714 MHz is generated in the 75 MHz phase locked oscillator circuit of Figure 6-8. In the self test mode, the 75 MHz divide by 5 counter, in addition to feeding the divide by 3 counter, also feeds a divide by 14 counter. The divide by 14 circuit is not part of the $\div N$ circuitry of the loop and does not affect the 75 MHz phase locked operation. The divide by 14 counter is activated by switching "ON" the 5 volts to the counter during self test operation. The 75 MHz signal, divided by 70 (or 1.0714 MHz), is then fed to the doppler multiplier input. Relay K1 in the doppler multiplier switches the input from the 1.083 MHz mixer output to the 1.0714 MHz self test frequency. The self test frequency is multiplied by 24 in the doppler multiplier producing a 25.714 MHz. This signal when mixed with the 25 MHz injection frequency, produces a 0.714 MHz bias plus doppler frequency input to the digital processor. The digital processor counts the self test frequency and makes a go-no go decision based on the computed equivalent doppler shift.

6.3 DIGITAL PROCESSOR

The digital processor accepts the 1 MHz plus doppler ($F_B + F_D$) signal from the RF processor and detects zero crossing coincidences between this signal and a clock reference frequency (F_0). The digital processor also includes the frequency counters, interval timing logic, micro-processor and computer interface logic necessary to supply the doppler and time counts to the UNIVAC 1218 computer. The micro-processor also computes navigational parameters for the extractor display. Figure 6-13 is a simplified block diagram of the digital extractor logic. A clock generator accepts the 5 MHz standard signal and generates clock frequencies required for operation of the digital logic.

A coincidence detector produces an output whenever zero-crossing coincidence of the RF processor signal (F_{B+D}) and the clock signal (F_0) occurs. An interval timer counts the 1.25 MHz (F_0) pulses to produce accurate interval markers. When an interval

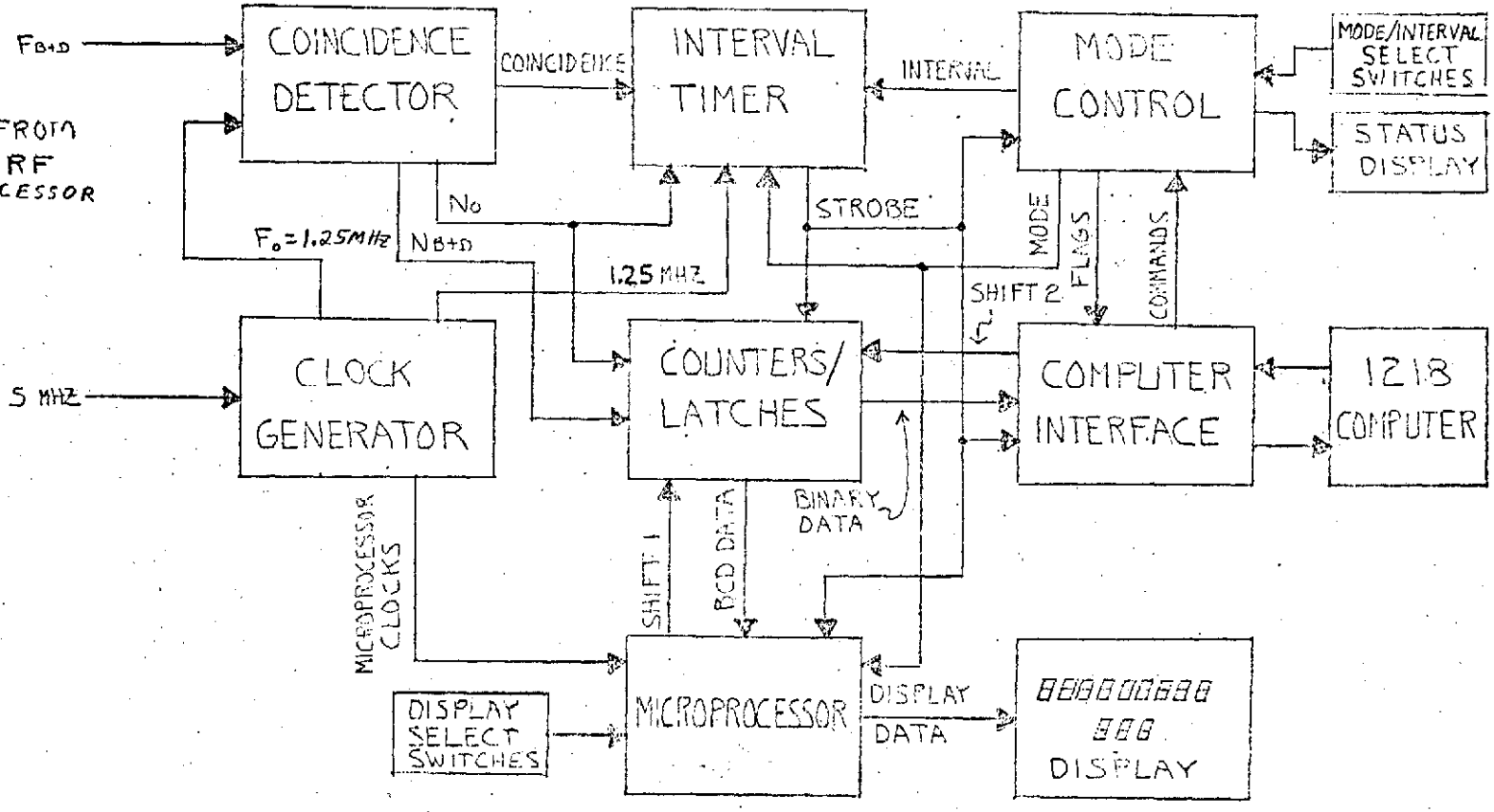


FIGURE 6-13 SIMPLIFIED BLOCK DIAGRAM DIGITAL EXTRACTOR LOGIC

marker is generated, a strobe pulse will be produced synchronous with the next coincidence pulse. This strobe is used to load the contents of the F_{B+D} and F_0 counters into latches and initiates the data transfer sequencers within the extractor.

Since the strobe is synchronized to the zero-crossings of the F_{B+D} and F_0 signals, the counters will always count an integral number of cycles of the two signals. In this way quantization error in the counts is reduced to the resolution of the coincidence detector. Separate binary and BCD counters produce data in the forms useful to the 1218 computer and to the display microprocessor.

Interval skewing (deviation of the actual measurement periods from their nominal positions) is principally caused by the delay between the interval marker and the following coincidence pulse. The intervals (or integration periods) will be slightly longer or shorter than nominal as a result of interval skew. Since the interval markers are independent of the coincidence pulses, however, the interval skew does not accumulate.

The interval timer will also generate readout strobes upon receipt of anytime readout (ARO) commands from the mode control logic. In this mode of operation the integration periods are established either by the operator or by the 1218 computer.

The extractor operates in several modes. Integration periods of 0.5, 1, 2, 10, 60 or 600-seconds may be selected. Integration periods may be contolled externally using the ARO mode. Readout from the F_{B+D} and F_0 counters may be destructive (DRO) wherein the counters are reset following each readout, or non-destructive (NDRO) wherein the counters are not disturbed by the readout strobe. The extractor can perform a single measurement and then stop (SINGLE COUNT), or it can produce continuous periodic output (CONTINUOUS COUNT). Several options are available when using the front panel display. Internal self-test of the extractor

circuits may be performed. The mode control logic provides the necessary internal control signals to implement the selected modes. (A complete description of extractor modes of operation is given in Section 7.)

The status of the mode control logic is displayed on the extractor front panel using LED indicators.

Computer interface logic receives binary data from the counter/latches and provides the formatting, level-shifting, and handshaking necessary to transfer this data to the 1218 computer.

A special-purpose microprocessor receives BCD data from the counter/latches and calculates key navigation parameters from this data. The microprocessor calculations are displayed on a front panel digital readout.

The digital logic uses a mixture of ECL, TTL, MOS, and CMOS integrated circuit components to achieve a balance between performance and total power dissipation. The 233 integrated circuits used in the digital logic are packaged on fifteen circuit boards. Fourteen of the boards are located in the digital nest, and may be unplugged for servicing. A card extractor is provided with the unit to permit probing of working circuits. By mixing technologies, high-speed performance is provided only where essential. The bulk of the logic is low-power CMOS. The CMOS logic provides excellent noise immunity, enhancing the reliability of the digital circuitry.

The design philosophy for the breadboard was to implement the desired functions with a minimum of development effort, consistent with reasonable design practice. Circuits within the breadboard, while functional, may not always, therefore, be optimal. With this caveat in mind, the breadboard circuts will now be described in detail.

6.3.1 DIGITAL CIRCUITS

Complete layout drawings for the fifteen digital logic boards are presented in Figures 6-21 through 6-26. The schematics for these boards are shown in Figures 6-30 through 6-41. These figures are grouped together at the end of this section for easy reference. Interconnection of the boards is detailed in Figure 6-27 while details of the front panel wiring are shown in Figure 6-28.

Every attempt was made to partition the digital logic so that each board is a functional module. While this is generally true, some functions do, nonetheless, overlap onto several boards. The circuits are described on a functional basis. The following notation is used:

> When a particular input or output pin is referred to, the format kXp will represent board k, package position X, and pin p. For example, 8G11 identifies pin 11 of package G on board 8 (the serial input of a CD4021 shift register in this case).
>
> When a package contains a single logic element, it will be identified as kX, where k is the board number and X is the package position. For example, 8G will identify the CD4021 shift register in position G of board 8.
>
> When a package contains more than one logic element (such as quad gates or dual flip-flops), the particular element will be identified as kXp, where k is the board number, X is the package position, and p is an output pin of the particular element. For example, 10L13 identified a flip-flop on board 10, while 10L2 identifies the other flip-flop in position L of board 10.

6.3.1.1 Coincidence Detector

The coincidence detector circuits are located on card number 1. A layout is shown in Figure 6-21 and the schematic is shown in Figure 6-30. The coincidence detector will produce an output

pulse whenever the zero-crossings of the F_{B+D} and F_0 signals coincide within a preset tolerance, or coincidence aperture.

High-speed comparators 1A and 1D accurately determine zero-crossings of the two input signals. The comparators produce ECL outputs which drive delay lines 1B and 1C, and gates 1E2 and 1E15. This combination results in precision one-shots, whose output pulse width is primarily a function of the 1B and 1C delay settings. Tapped delay lines are used to provide adjustable pulse width, high absolute accuracy (within 5%), and good stability (60ppm/°C). Pulse widths from 4 to 100 nanoseconds in 2-nanosecond increments are available by proper selection of delay line and tap. The coincidence aperture is the sum of the two delay line settings.

If the input zero-crossings coincide within the coincidence aperture, 1E2 and 1E15 will be low simultaneously, producing a positive pulse at 1G3. The one-shot pulses are ANDed in this way, establishing coincidence. 1G14 and 1G15 form a 1-microsecond one-shot, stretching the narrow coincidence pulses into pulses wide enough to operate the CMOS interval timing logic.

Level shifters 1H and 1F convert the ECL coincidence detector levels to 12-volt CMOS levels for use by the remaining digital logic. The N_{B+D} and N_0 signals are buffered by drivers 2Q and 2R and operate the counters on boards 4 through 8.

ECL-III logic and stripline circuit interconnection techniques are used to provide maximum commercially-available speed while maintaining waveform integrity. The use of 1-nanosecond logic insures that the coincidence aperture depends only on the delay lines (assuming the delay line settings are significantly greater than 1-nanosecond), and provides maximum resolution in the coincidence detector. Since the accuracy of the zero-crossing coincidence technique depends primarily on the accuracy of the coincidence detector, this approach results in breadboard performance closely approaching the theoretical limit of the technique. Performance may be hardware-limited as

the aperture is reduced to values much less than 20-nanoseconds.

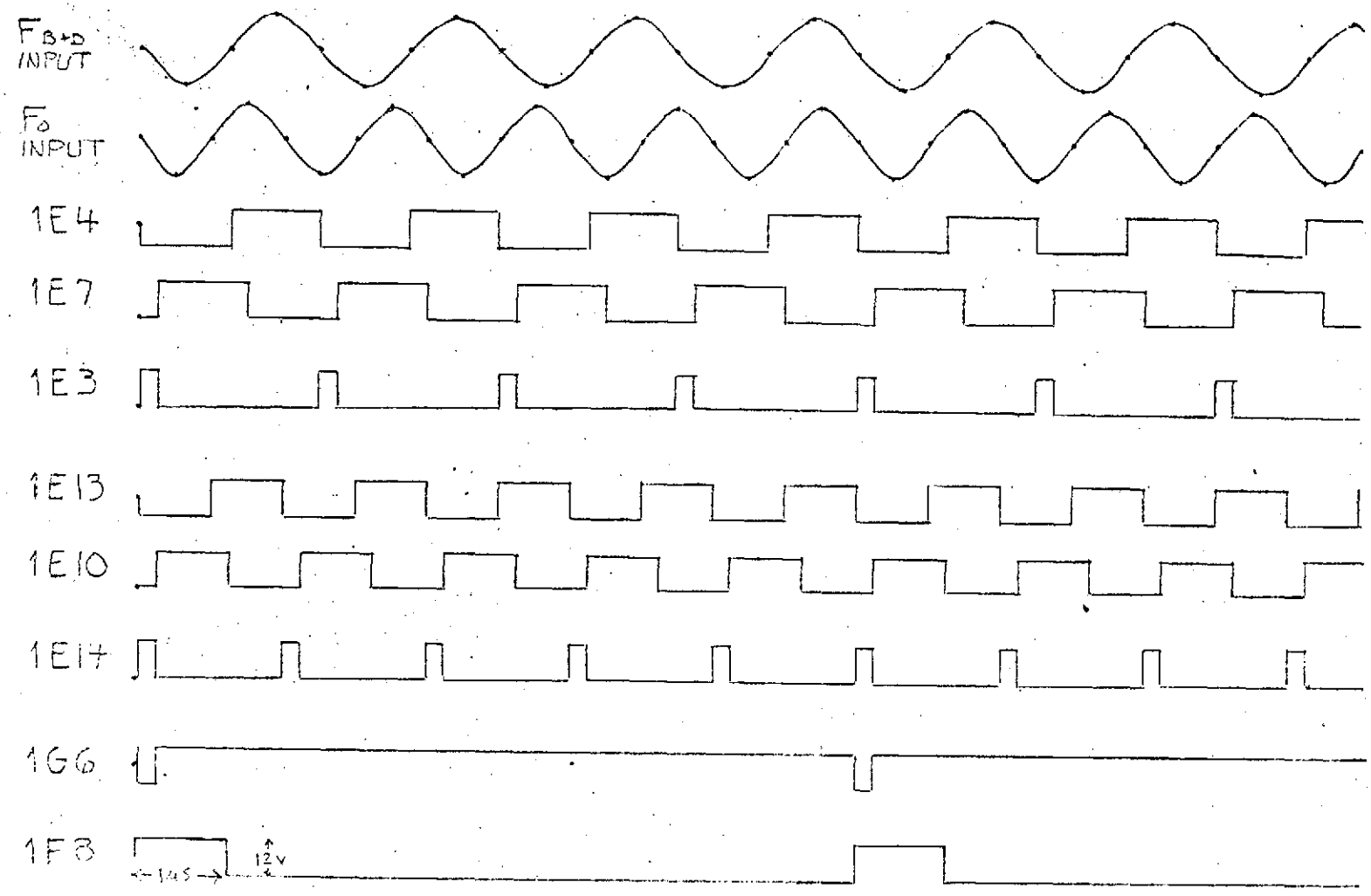
Three test-points, TPA, TPB and TPC enable monitoring of the precision ECL one-shot outputs and of the ECL coincidence pulses.

Figure 6-14 shows a timing diagram for the coincidence detector circuits.

6.3.1.2 Clock Reference Generator

The clock reference generator is located on card number 10 shown in Figure 6-24. A schematic is shown in Figure 6-36. The clock reference generator accepts the 5 MHz standard signal and generates clock signals for use by the digital logic circuits. A 20-dB attenuator at the digital nest '5 MHz' input connector provides isolation between the (sensitive) RF processor circuits and the (noisy) digital circuits. This pad is shown in Figure 6-27. Comparator 10S squares up the resulting low-level sinusoid, which is then amplified by 10T15 (operating as a "linear" amplifier) and further shaped by 10T12. High-speed divider 10U derives a 1.25 MHz reference clock and a 156-kHz display clock from this signal. The display clock is buffered by 10T4.

The breadboard design provides for the use of either the internal 1.25 MHz signal at 10U11 or an external 12-volt signal as the F_0 reference signal. The external signal is squared up by 10M6. The circuit at 10G6 detects the presence of the external signal as follows: With no signal present, 10M6 will be clamped high by the 620-ohm resistor. 10G6 will rise to a high level as the 300-picofarad capacitor is charged through the 47 K resistor. This enables gate 10G4, allowing the internal 1.25 MHz signal to operate gate 10G10. With a square-wave signal present at the external F_0 input, the 300-picofarad capacitor will be discharged through the diode as 10M6 goes low. The time constant is such that an external F_0 signal on the order of 1-MHz will readily keep 10G6 at a low level, disabling the internal 1.25 MHz reference. Gate 10G10 is then operated directly by 10M6. In this way the presence of the external reference is detected and switching of the F_0 input is accomplished. Buffer 10T6 drives the resistor network which provides a 50-ohm F_0 signal for use by



NOTE: COUNTER CLOCKS No AND N_B+D ARE INVERTED W.R.T. INPUT SIGNALS. COINCIDENCE CORRESPONDS TO POSITIVE TRANSITIONS OF THESE CLOCKS.

FIGURE 6-14 COINCIDENCE DETECTOR TIMING

the coincidence detector.

Inverters 10B2 and 10B12 form an 800-kHz multivibrator. The 800-kHz signal is divided by flip-flop 10H13 and buffered by 10T2 to provide a 400-kHz clock for the microprocessor. The microprocessor clock is generated in this way because the 311-kHz signal at 10U6 is too slow to enable the navigation parameter calculations to be completed in 2-seconds. The significance of this will be apparent when the microprocessor is described.

The internal 1.25 MHz signal is buffered by 10T10 and 10N2 to provide a "system" clock for the digital logic.

6.3.1.3 Interval Timer

The interval timer is located on board number 2 shown in Figure 6-21. A schematic is shown in Figure 6-31. The interval timer logic produces a STROBE pulse, which marks the start and stop of a measurement interval (or successive intervals in the CONTINUOUS COUNT mode). This strobe must be synchronized to the zero-crossing coincidence of the F_{B+D} and F_0 signals, and is initiated either by an internal marker generator or by external ARO readout commands. A COUNTER RESET pulse is also generated by the interval timer to reset the F_{B+D} and F_0 counters following readout in DRO operation.

The 1.25 MHz system clock is counted down by counters 2E, 2F, and associated logic to produce a 4 Hertz clock. Counter 2D will divide this 4-Hz signal by the appropriate 'N' to produce markers at the interval spacing indicated by the ABC interval select leads. The markers appear as an inverted interval strobe ($\overline{IS}$) at 2J4. The CLR TIMER lead clears the marker generator, permitting the markers to be synchronized by commands from the mode control logic. This lead also disables the markers, and is used to stop the doppler measurements when in the SINGLE COUNT mode.

The use of CMOS ripple counters for the marker generator results in a 10-microsecond worst-case delay from the INTERVAL START command to the output of the first marker. This delay contributes to the overall measurement delay of the extractor.

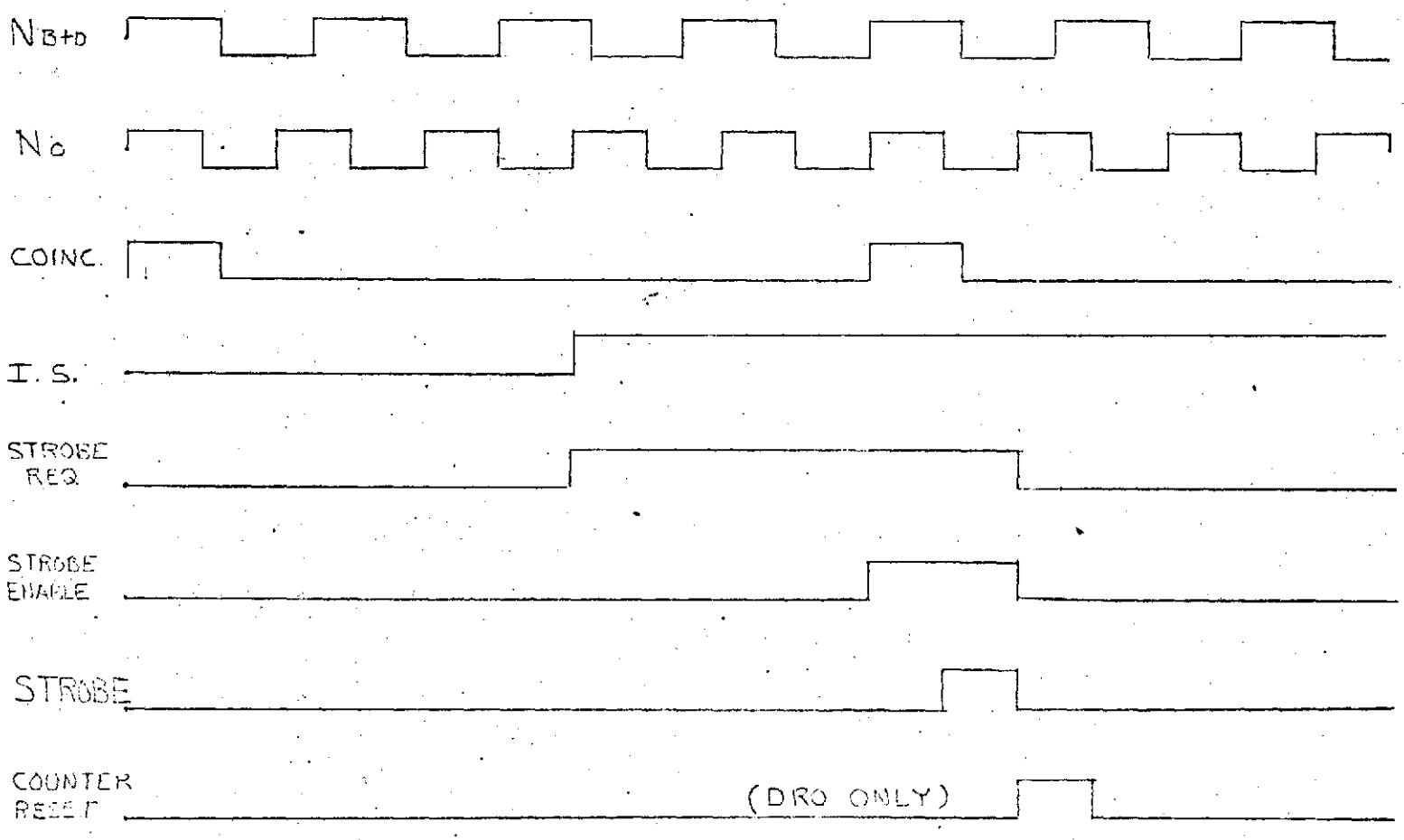
Gate 2N4 provides a marker at the start of a measurement, so that start-of-measurement data transfer can occur. The interval markers set the STROBE REQ flip-flop 2I13 when not in the ARO mode. Flip-flop 2I13 is set by the ARO STROBE REQ signal (produced by the mode control logic) in the ARO mode. When a strobe request has been given, the first COINCIDENCE pulse thereafter will set the STR ENABLE flip-flop 2I1. Gate 2K10 will then generate the STROBE pulse, synchronous with the N_0 clock. The strobe is buffered by 2N10 and drivers 2S and 2Q15. The strobe initiates counter readout and data transfer operations.

The strobe will set flip-flops 2H1 and 2G15. 2H1 will reset 2I1 and 2I13, ensuring that only one strobe results from each strobe request. In the DRO mode, gate 2K4 permits output 2H1 to produce a counter reset pulse. 2H1 is reset on the next N_0 transition, resulting in a reset pulse width of 400-nanoseconds. 2G15 produces a 10-microsecond PSEUDO RESET pulse which is used to clear a counter in the mode control logic.

The timing of the strobe and reset pulses (Figure 6-15) is quite critical. High-speed CMOS and CMOS/SOS components are used to reduce propagation delay effects. The strobe pulse is produced 400-nanoseconds after the final increment of the N_{B+D} and N_0 counters, but before readout. The reset pulse immediately follows the strobe in DRO operation. (The counters will "skip" the next count transition due to the reset pulse. They are therefore reset to a count of 1.) Any skewing of the strobe and reset pulses from the positions shown in Figure 6-15 will result in erratic operation of the counters. The output buffer circuits for the strobe, counter reset, N_0, and N_{B+D} circuits were matched to reduce pulse skew. Maximum pulse skew for the breadboard was measured as 40 nanoseconds. This skew permits the CMOS counters to operate reliably up to 1.5 MHz.

The strobe and reset pulses are based on the F_0 signal only. These signals are used to control both the N_0 and N_{B+D} counters. The N_{B+D} readout command skew will be tolerable as long as

$$\frac{2}{3} < \frac{F_{B+D}}{F_0} < 2$$



NOTE: COUNTERS INCREMENT ON POSITIVE N_{B+D} AND N_o TRANSITIONS, LATCHES STORE DATA ON POSITIVE TRANSITION OF STROBE.

FIGURE 6-15 TIMING OF STROBE AND COUNTER RESET

This limits the range of external F_0 frequencies for proper operation of the extractor. The lower bound is established by excessive skew of the reset pulse, while the upper bound is established by the strobe. Both F_{B+D} and F_0 must be kept below 1.5-MHz for proper operation of the readout sequence. (Observe that the 714.3-kHz self-test signal from the RF preconditioner is below the lower limit. For this reason the self-test measurement is NDRO to avoid possible trouble with the reset pulse skew.)

The STROBE and COINCIDENCE outputs are buffered and made available at the rear chassis lip of the breadboard.

6.3.1.4 Counter/Latch Circuits

N_{B+D} and N_0 pulses are counted by CMOS synchronous counters. Separate binary and BCD counters are provided for each signal to relieve the display microprocessor of the binary-to-BCD conversion otherwise necessary. This is in keeping with the design philosophy, wherein extra packages are provided to reduce the software development for the microprocessor. In a production unit, the conversion would be more efficiently performed in software.

The counters increment on the positive transition of the clock inputs. The counters will reset to 1 when the CTR RESET lead is high. The binary counters have a maximum capacity of 32 bits, while the BCD counters have a capacity of 9 digits. This capacity permits the counters to run more than 800-seconds before overflow (recycle through zero) occurs. The counters are found on boards 4 through 8, shown in the layout drawings of Figures 6-22 and 6-23. The schematic of the counters is shown in Figures 6-33 and 6-34. The counter arrangement is best seen in Figure 6-27.

LED readouts are provided on the counter boards to indicate proper operation of the binary counters. Operation of the BCD counters is indicated on the front panel digital display. The binary LEDs do not operate through latches. To enable the operator to interpret the readout, therefore, counter 8E controls the start and stop operation of the counters when the RUN/HOLD switch on board 8 is in the HOLD position. When this switch is

operated, 8E will ENABLE the counters for a single measurement interval (two successive strobes) and then DISABLE the counters. When in the SINGLE COUNT mode and using NDRO, the results of the BCD count will appear on the front panel display, while the binary results are available on the LED indicators.

The counter results are loaded into the CD4021 parallel-to-serial registers on the positive transition of the strobe. Due to the timing of the strobe pulse, the counters have approximately 400 nanoseconds to "settle" before the readout takes place. The registers are arranged in serial strings, one for each counter. Data are outputted in serial form, MSB first, upon clocking of the registers by the appropriate shift pulses. SHIFT 1 controls the BCD data, while SHIFT 2 controls the binary data. The shift bursts are generated in the microprocessor and computer interface logic, respectively. The data streams are concatenated, so that two successive shift bursts will output the N_0 count, followed by the N_{B+D} count, on a single lead.

Extractor flag bits, used to indicate extractor status to the 1218 computer, are inserted into the MSB positions of the binary data stream via register 8C and gate 8B4. Register 8A inserts zeroes into the binary stream to avoid conflicts with the flag bits. LEDs L1 throguh L4 on board 8 indicate the status of the flag bits.

6.3.1.5 Mode Control Logic

The mode control logic is located on board 3 shown in the layout drawing of Figure 6-22. A schematic is shown in Figure 6-32. The mode control logic receives extractor commands either from the 1218 computer or from an operator via the front panel push-buttons. The mode control logic interprets these commands and generates the internal control signals necessary to implement the commands. This logic was designed to be as "fail-safe" as possible, in that contradictory instructions (generated by pressing the wrong pushbutton, for example) are generally resolved in a known way.

Figure 6-28 shows the front panel wiring. Manual control instructions are produced by pressing pushbuttons on the front panel. The MODE, READOUT, and INTERVAL CONTROL instructions proceed directly to board 3, while the INTEGRATION PERIOD command is first encoded into the ABC format used by the interval timer. This encoding is accomplished by 15I, and helps reduce the number of leads into the crowded POWER/CONTROL connector. The ABC code is given on the diagram for board 2.

Control of the unit is accomplished using eight leads. The ABC leads determine the integration period. The COUNT lead indicates the continuous count mode when high, and single count operation when low. The ARO command is generated by a momentary-contact pushbotton and is de-bounced by 3Q9. Anytime readout is performed following the positive transition of this lead, and the unit becomes locked in the ARO mode (markers from the interval timer do not produce strobes) until the unit is reset using the interval start command. The unit is in the self-test mode when the TEST lead is high. A high on the DRO/NDRO lead indicates destructive readout, while a low on this lead indicates non-destructive readout. The INTERVAL START command is generated by a momentary-contact pushbutton, and is de-bounced by 3Q1. A negative transition on this lead will initialize the extractor, resetting all counters and producing a MASTER RESET pulse.

Interlocking push-buttons on the front panel enhance the fail-safe operation of the unit. Commands in contradiction to the current mode of operation are ignored (overridden) by the mode control logic.

The eight command leads produced by the front panel pushbuttons correspond directly to an eight-bit code used by the 1218 computer to control the unit. The computer command code is stored in latches 3T and 3U.

Depending on the status of the CONTROL lead, either the push-button commands are selected (when this lead is low) or the computer command word is selected (when this lead is high) by multiplexers 3S and 3M.

The integration period and readout mode are established by the

contents of 3R. This latch is updated upon receipt of a strobe, permitting the integration period and readout mode to change only at the end of a measurement interval. In this way the measurements are made self-completing. When self-test is selected, the unit is forced into a 2-second, NDRO readout mode by resetting 3R and activating gate 3D4.

The positive transition of the 1218 computer EXTERNAL FUNCTION lead is used to update latches 3T and 3U, and to simulate the momentary-contact action of the front panel INTERVAL CONTROL pushbuttons when under computer control. The external function signal is delayed a few microseconds to permit the latches to receive the concurrent command word, and then produces a negative transition at 3D10. If the interval start bit is up (3M13) a positive transition will be produced at 3D11, firing one-shot 3N1. If the ARO bit is up (3M10), a positive transition will result at 3B4, setting strobe request flip-flop 2I13 (which in turn produces a readout strobe).

In the manual control mode, the transition caused by pressing one of the interval control pushbuttons propagates through to 3B4 or 3D11.

Counter 3F and the interval timer combine to perform two basic extractor functions. Normally, counter 3F will produce the single count operation by activating the CLR TIMER lead upon receipt of two successive $\overline{IS}$ pulses from the interval timer. This will terminate the generation of interval markers (and thus strobes). The counter is initialized by the master reset pulse (via 3A10) to produce a new measurement when the INTERVAL START command is given. The single count operation depends on gate 3A9, which will inhibit the clear timer pulses if in the ARO mode or if in the continuous count mode.

In the ARO mode, the interval timer is used to determine when the duration between ARO commands exceeds the setting of the timer. Two successive $\overline{IS}$ pulses into 3F indicates that the present maximum duration has been exceeded, and an OVERFLOW indication is given via 3E11 and 3E2. The overflow indication is harmless, and merely lights a lamp and produces a flag bit

at the computer interface to indicate that something has gone amiss. When an ARO command is given, the PSEUDO RESET pulse is produced. In the ARO mode, gate 3E4 permits this pulse to reset the interval timer via 3A6 and to reset counter 3F via gate 3A10. This resets the overflow indication and starts a new overflow count. Since the pseudo reset pulse occurs after the strobe, the overflow flag is loaded into register 8C for transfer to the computer before the flag is taken down.

Once an ARO command is given, the unit is locked into the ARO mode by setting flip-flop 3Q10. This flip-flop is reset by the master reset pulse (produced by the INTERVAL START command).

The SELF-TEST command forces the unit into a 2-second, NDRO read-out mode, as described earlier. Gate 3E10 forces the unit into SINGLE COUNT operation, while gate 303 inhibits any erroneous ARO commands. The self-test command is buffered by 11G12 and 11G15, and operates the self-test relays in the RF processor (which cause the generation of the precise test signal) via driver transistor 11H.

Flip-flops 3J and 3K form the self-test sequencer. One-shot 3K13 is triggered by the self-test command. A 1.4-second period is used to provide a lamp test (via 3C10, 14AA3, and 3B3) while the RF processor PLLs are allowed to stabilize. A MASTER RESET signal is generated via 3B11 to initialize the unit (the master reset is also produced by one-shot 3N1 when an interval start command is given).

When 3K13 times out, the unit performs a single 2-second NDRO count of the test signal. Upon completion of the measurement, 3F12 will go high, triggering one-shot 3J1. After 3.5 seconds elapse (permitting the microprocessor to complete its calculations) 3J1 times out, setting 3J13 and 3K2. Flip-flop 3K2 enables the pass-fail result via gates 10P3 and 10P4. The appropriate pass or fail lamp is lit, and the pass-fail bit is jammed into the computer output data word via 9A13. Flip-flop 3J13 raises the EXTERNAL INTERRUPT lead to alert the 1218 computer that the pass-fail result is available at the interface. 3J13 is reset by an INPUT ACKNOWLEDGE from the computer

(adhering to the 1218 handshaking format), while 3K2 resets when the unit is taken out of the self-test mode.

6.3.1.6 Status Indicators

The status of the extractor mode control logic is indicated by seventeen multicolored LEDs on the front panel.

The mode status bits are loaded into registers 3P and 3V. The ABC integration period code is decoded by 3W to operate the integration period indicators. Gate 3D3 forces a continuous count indication when in the self-test mode. The other status leads are available on board 3.

A logic 1 in the 3P and 3V registers will light a corresponding lamp on the extractor front panel. Gate 3B3 forces all indicators to light during the lamp test portion of the self-test sequence.

Counter 3G and flip-flops 3H13 and 3N9 produce 16-cycle bursts of the N_0 clock (via 3B10 and following buffers) to transfer the status information to registers 15B and 15J. During this data transfer the indicators are blanked by taking down the PANEL DISPLAY ENABLE lead. At the completion of the transfer, one-shot 3H1 is fired to energize the indicators.

The serial data transfer is necessary due to pin limitations on board 3. The transfer sequence provides a 1-kHz display update rate, with an indicator duty cycle of 98.7%. The resistor-diode networks at pins 28, 29, 40 and 42 of board 3 provide TTL-compatible output levels (the board 3 logic operates at 12-volts).

Drivers 15A, 15C, 15E, 15L, 15K, 15G and 15H (Figure 6-41) energize the LED indicators by sinking the LED current. The position of switch S_{1A} is used (see Figure 6-28)by gates 15D to determine whether the red or green segments of the multicolored diodes should be lit. The color is changed by reversing the current flow through the diodes. Green is used to indicate computer-controlled operation.

The red portions of D_2, D_3, and D_4 are energized directly when the corresponding button of S_1 is pressed. The green portions of these diodes are energized via the board 15 drivers. D_1 is energized directly by S_{1A}.

6.3.1.7 Computer Interface

The computer interface circuits are located on boards numbered 9 and 10 shown in Figures 6-23 and 6-24. Schematics of these boards are shown in Figures 6-35 and 6-36. The computer interface logic performs the data formatting, level-shifting, and handshaking required to interface with a 1218 computer port.

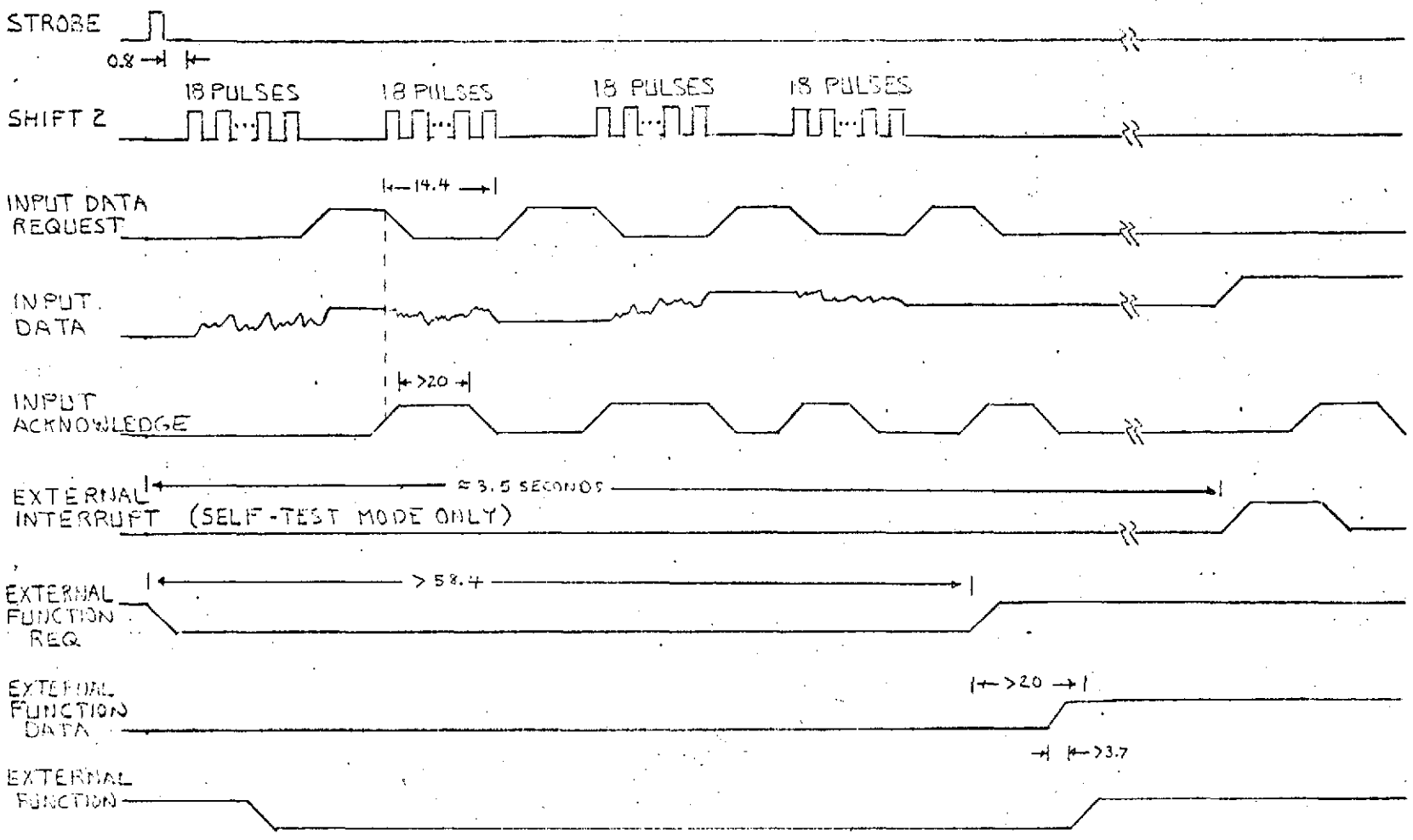
Figure 6-16 shows the timing of the interface leads. A strobe indicates that new data are available in the extractor registers (boards 4-8), and initiates a burst of 1.25 MHz clock to shift the first word into the serial-to-parallel registers on board 9. Once the data is loaded (and stable), the INPUT DATA REQUEST lead is raised. The computer responds with an INPUT ACKNOWLEDGE, which initiates another SHIFT 2 burst to load the second word. The exchange continues until four 18-bit words are sent to the computer, completing the sequence.

If the extractor is performing a self-test, the EXTERNAL INTERRUPT lead will be raised after 3.5-seconds to alert the computer that the pass-fail flag bit is available. The computer responds with another INPUT ACKNOWLEDGE, completing the sequence.

The EXTERNAL FUNCTION lead must be toggled to access new commands from the 1218 computer. During data transfer from the extractor to the computer, this lead is taken down, preventing a command from being given. The positive transition of the EXTERNAL FUNCTION REQUEST lead following the transfer allows the computer to transmit a new command to the extractor. The EXTERNAL FUNCTION lead is raised by the computer to indicate that a new command is present on the data lines.

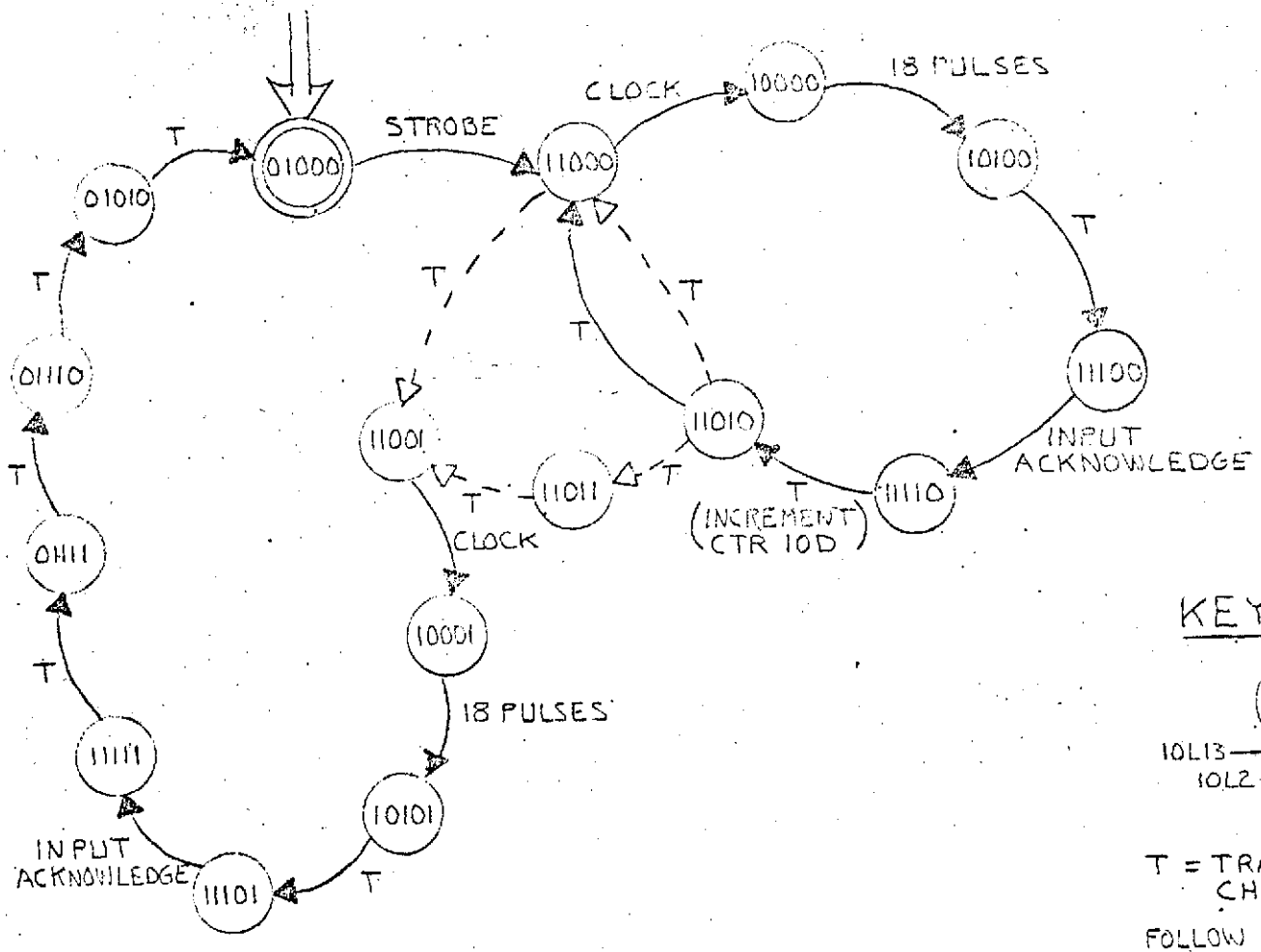
The timing of Figure 6-16 meets the requirements specified in the 1218 computer technical manual. Risetimes and falltimes are approximately 5-microseconds on all extractor-generated leads.

Counters and flip-flops 10L, 10K, 10J, 10C, 10D, and associated gates (card layout Figure 6-24) form a high-speed synchronous burst generator, producing the SHIFT 2 bursts. Operation of this burst generator is illustrated by the state diagram of Figure 6-17. Flip-flop 10L13 is set while the data transfer sequence is in progress. Shift pulses are enabled when 10L2 is

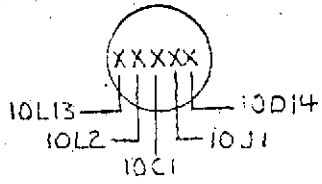


NOTES: TIMES IN MICROSECONDS UNLESS OTHERWISE INDICATED
RISE-AND FALL-TIMES APPROXIMATELY 5 MICROSECONDS
SEE ALSO FIGURES 4-38 AND 4-39 IN 1218 COMPUTER MANUAL.

FIGURE 6-16 COMPUTER INTERFACE TIMING



KEY:



T = TRANSIENT STATE CHANGE

FOLLOW DASHED PATH WHEN 10D INCREMENTS FROM 3 TO 4.

BURST IS ENABLED WHEN 10L2 = 0.

FIGURE 6-17: STATE DIAGRAM FOR SHIFT 2 BURST GENERATOR

low. 10C1 will become a high when an 18-pulse burst has been completed. 10C1 provides the INPUT DATA REQUEST signal, while 10L12 is used to produce the EXTERNAL FUNCTION REQUEST signal.

The SHIFT 2 bursts transfer data from the binary data registers on boards 4 through 8 into registers 9A, 9B and 9C. The 18-bit parallel data are then transferred to the computer. Self-test results are inserted in the data word via 9A8 or 9A10.

Level shifters/line drivers are provided on the extractor output leads. As shown in Detail A for board 9, a zener diode and resistor shifts the 0-12 volt CMOS levels to (-15)-0 volt 1218 computer levels. The CD4050 buffers drive R-C networks (which limit the rise and fall times) and emitter followers. The emitter followers drive the computer input cable.

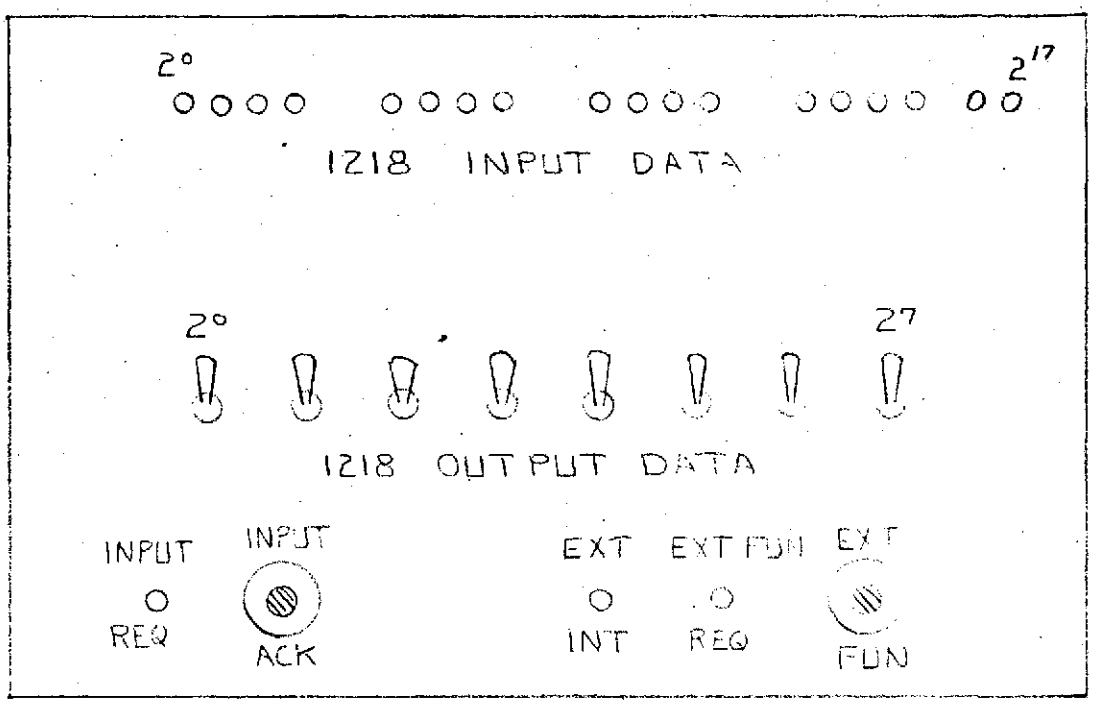
Detail B shows the line receiver circuit. Incoming computer levels are shifted to CMOS levels by the zener diodes and resistors. R-C networks filter high-frequency noise which may be present on the line. A CD4050 functions as buffers. Positive feedback, via the 180 K resistors provies 2.5 volts of hysteresis, improving the noise immunity of the line receivers. The line receivers are located on boards 9 and 10.

Table 6-3 details the wiring of the computer interface connections.

A computer interface test unit was shipped with the extractor to provide rapid verification of the interface logic when a 1218 computer is not available. The front panel layout of this unit is shown in Figure 6-18. The test unit plugs into the computer connectors at the rear of the extractor and is powered from the extractor. Use of the test unit is discussed in the section "Breadboard Operation."

6.3.1.8 Microprocessor Hardware

The microprocessor circuits perform calculations on the BCD counter data to provide direct display of doppler frequency (F_D), range rate ($\dot{R}$), change in range ($\triangle R$), self-test error, and coincidence delay. The following paragraphs describe the hardware implementation of the microprocessor. The microprocessor



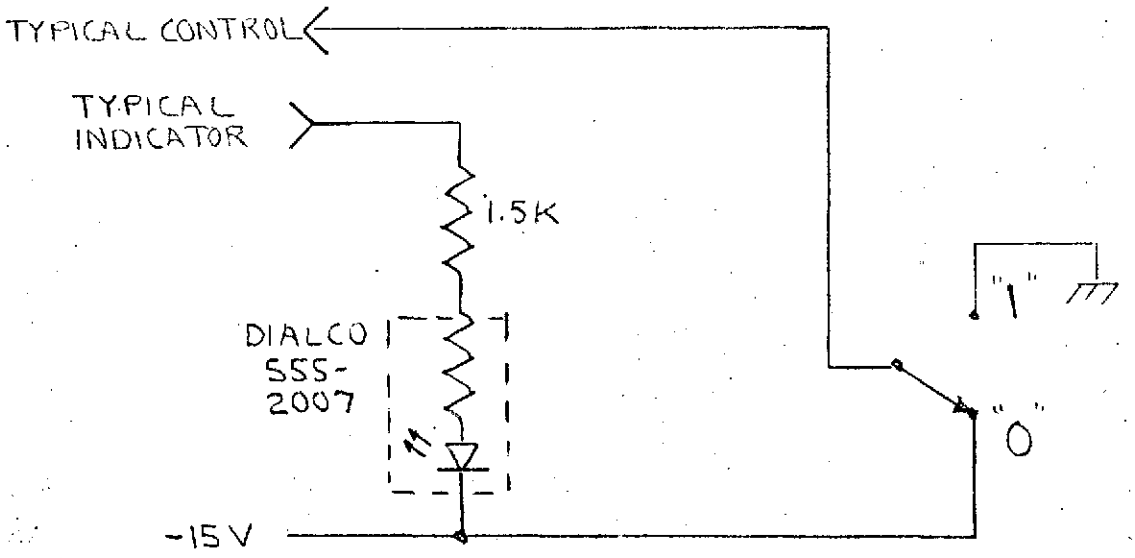


FIGURE 6-18 COMPUTER INTERFACE TEST UNIT

algorithms are discussed later under microprocessor software. New and powerful microprocessor chip sets were appearing on the market during the design period of the extractor. These general-purpose chips were relatively expensive, difficult to program, and difficult to interface. The Texas Instruments TMS-0117 calculator chip provided the computational capability required for the extractor display, while at the same time being easy to program, easy to interface, readily available, and very low cost. With the design philosophy to mind, the TMS-0117 was selected as the central processing element in a special-purpose microprocessor arrangement.

Figure 6-19 shows the microprocessor and display approach. The TMS-0117 functions as a central processing unit. A random-access memory (RAM) provides storage of intermediate and final calculation results. A programmable read-only memory (PROM) holds a series of instructions referred to as a microsequence or microprogram. The microsequence is the detailed set of data transfers and instructions required to compute the navigation parameters for display. The microsequence timing logic generates clock bursts used to operate the central processor, transfer data, and increment the microsequence memory. Input and output gating logic provides the multiplexing and serial-parallel conversion required to interface the TMS-0117 with the RAM, ROM, and extractor data registers.

This microprocessor approach has a speed disadvantage. Computation time for the navigation parameters is on the order of 1.8 seconds. Holding a number in the output registers of the TMS-0117 calculator chip would permit display of the output, but would "tie up" this chip during the display period. For this reason, the internal display scanning and blanking circuitry of the TMS-0117 was not utilized, permitting the chip to be used full time as a processor.

As shown in Figure 6-19, separate display timing, formatting and zero-suppression circuits are provided. The display logic shares the RAM with the microprocessor. In operation, the display circuits select and access the multiplexed display data by stepping through the appropriate block of RAM addresses.

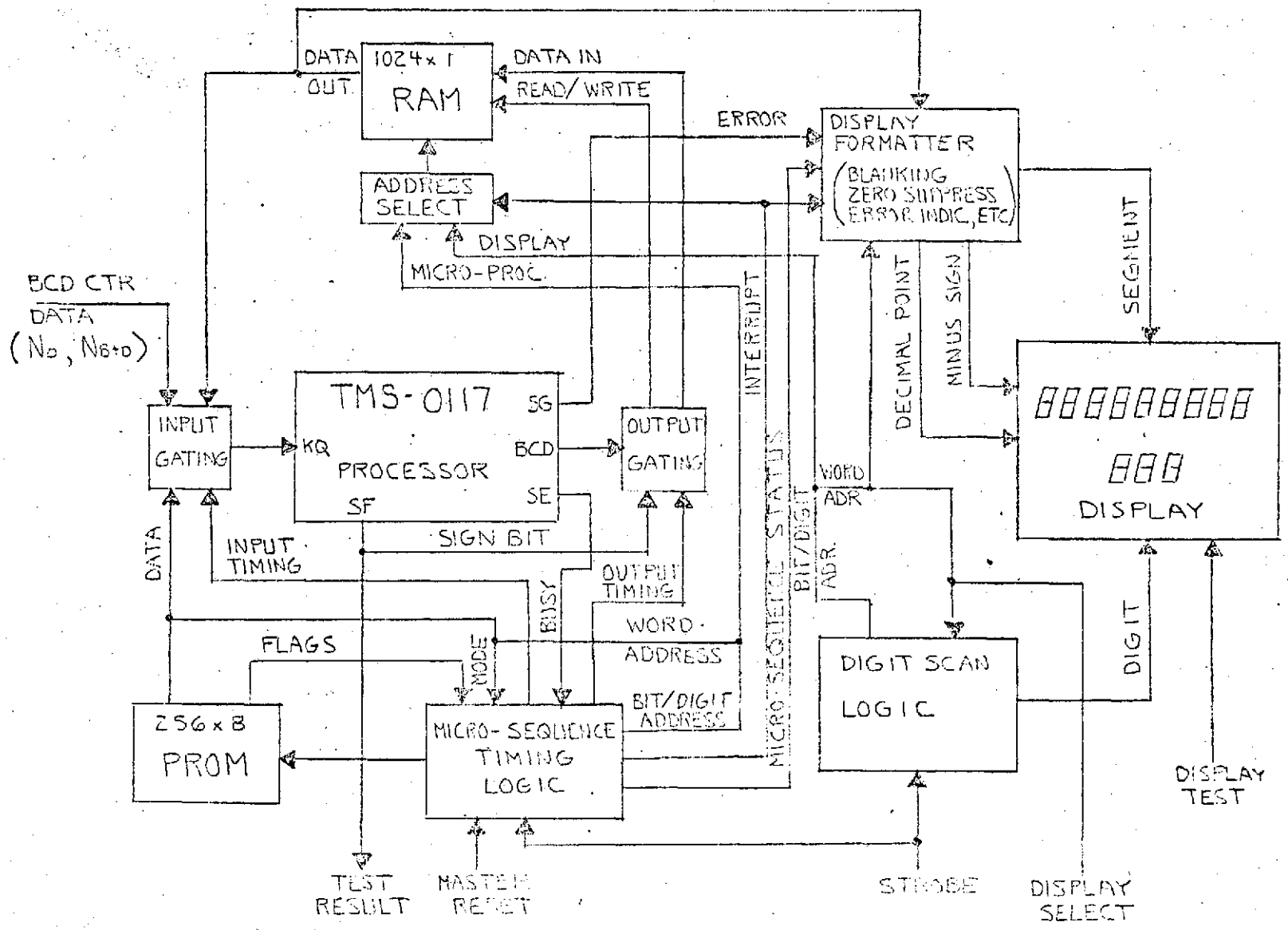


FIGURE 6-19 OWD DISPLAY APPROACH

The microprocessor accesses the RAM on an interrupt basis, "stealing" the address and data leads to read or write a data word. The display is blanked during this interrupt. Upon completion of the interrupt, the RAM address and data leads are switched back to the display control circuits, where display scanning is resumed. Due to the low duty cycle of the interrupt action, the display appears undisturbed to the eye.

The RAM addressing is organized such that the microprocessor accesses one portion of the memory while the display logic accesses another. Intermediate calculations and new parameter results are stored in one half of the memory. Previously calculated results are stored in the other half. The display logic only accesses previous results, while both current and previous results are used by the microprocessor.

A strobe from the interval timer initiates the microsequence. Upon receipt of the strobe, the microprocessor will access the BCD data from the extractor and calculate all navigation parameters, storing the results in the RAM. At the completion of the microsequence, a bit of the RAM address will be inverted. This inversion has the effect of interchanging the new and old data within the RAM, so that the just-completed calculations appear on the display, while the other half of the memory becomes available for the next set of calculations.

This approach provides a sample-and-hold type of display, and permits viewing of previous calculations while new parameters are being calculated. With integration periods under 2-seconds, the microprocessor will be constantly calculating, necessitating the sample-and-hold display.

If the extractor is operating with integration periods under 2-seconds, the microsequence will not be completed before the next strobe occurs. The current microsequence is aborted, allowing the new sequence to begin. In this way the new data cannot be lost, and will be available for display as long as the integration period exceeds 0.5 seconds. The navigation parameters are calculated in sequence, with F_D, R_C, $\triangle R$, test error, and

coincidence delay progressively available as the integration period is increased from 0.5 to 2-seconds.

Flag bits are provided in the PROM at the completion of each parameter calculation. A counter in the microsequence timing logic counts these flags to determine the status of the microsequence. The output of this counter is used to determine the completion of the sequence, causing the display to be updated. If the sequence is aborted, the sequence status information is used by the display control logic to blank the display of uncalculated parameters.

Digit-scan multiplexing is used to reduce the latch/decoder/driver package count for the 12-digit readout. This multiplexing approach is compatible with the digit-scanned input/output multiplexing of the TMS-0117 data.

The microsequence is implemented whithout branching. Address registers and logic normally provided for this function are not required for this microprocessor.

The central processor and associated logic are contained on board II. The layout for board II is shown in Figure 6-24. A schematic is shown in Figure 6-37. This processor operates in four modes:

Mode 1 - Instructions or data are read directly from the PROM into the TSM-0117 processor chip.

Mode 2 - Data are transferred from the extractor shift registers to the processor chip.

Mode 3 - Data are read from the RAM and transferred into the processor chip.

Mode 4 - Data in the processor chip output register are written into the RAM.

The data transfer is one digit per Mode 1 instruction, and one block of digits, or word, per Mode 2, 3 or 4 instruction. The basic data word consists of a sign and ten significant digits, for a total of eleven digit positions. The extractor data does not carry a sign bit. A Mode 2 transfer therefore consists of 10 digits from the extractor registers. The most significant digit (MSD or sign) is made zero by 8I and 8G.

The TMS-0117 NO-OP Code (control bit followed by 1111) is used to indicate a positive number, while negative numbers are preceded by the TMS-0117 SUBTRACT code (control bit followed by 0110). The processor chip interprets these codes as a sign bit when properly used in the microsequence. Decoding is provided in the display logic to detect the minus sign code.

The interfaces and operation codes for the TMS-0117 are described in Appendix C. Processor 11J operates with ± 7.6 volt supplies, provided by series regulators 11T and 11I. Buffers 11Q convert 0- to 12-volt CMOS logic levels to the ± 7.6 volt levels for the processor chip. Networks, each consisting of 3.9K resistor, a 5.1 volt zener diode, and a 47K resistor, restore the 11J output signals to CMOS levels.

The input/output format and timing for 11J are described in Appendix C. Input words consist of a control bit followed by a four-bit code. A zero in the control bit position indicates the presence of a BCD digit, while a one in the control bit position indicates a control operation, such as add, subtract, etc.

Chip 11J uses a bit-serial input format and a bit-parallel output format. Register 11R provides parallel-to-serial conversion, so that the processor input and output are both bit-parallel. Parallel data are entered into 11R by raising 11R9 to a high. Returning 11R9 to a low permits the serial input clock to shift the 11J input data out of 11R3. The serial input clock is produced by wire-ORing digit scan leads available on 11J.

The 11J multiplexing scheme is described in the appendix. A DIGIT CLOCK is used to indicate the center of the digit-scan positions. 11J output data are valid on either transition of the digit clock. Time slot D11 is used for access of the sign bit and other flag bits available at 11J. D10 through D1 indicate access (on output) to the MSD through LSD, respectively, of the output register. The output digits appear in parallel form on the SA, SB, SC, and SD leads, with the MSB of the BCD formatted digit appearing on the SA output.

The input control bit, followed by the input word (MSB first) are accessed during time slots D10, D7, D5, D3, and D1 respectively. With the positive transition of each of these indicators, a new bit is shifted out of 11R. Since the TMS-0117 scans in the order D11, D10, D9,...D1, data are handled MSD and MSB-first. This order of data flow is maintained throughout the microprocessor and display circuits.

RAM 12K is organized as 1024 x 1 -bits. This organization implies bit-serial transfer of RAM data. 11A provides the conversion from the parallel format of 11J to the serial format required by 12K.

The bit-parallel interface provided by 11R permits the use of an independent clock for serial data transfer into the microprocessor. Register 12I converts serial extractor and RAM data to parallel form using the external transfer (BURST) clock. The PROM data are in parallel form, and do not pass through 12I.

Table 6-1 shows the assignment of the RAM address leads. This assignment minimizes the external logic required to generate the RAM addresses, at the expense of unused bit positions within the RAM. The MSD/MSB-first ordering of data is reflected in the address assignments. The assignment of word blocks is the order in which the navigation parameter calculations are made. The N/O bit indicates the access of new or old (previously calculated) data from the RAM.

Chip 11J provides four flag bits. These flag bits are active during time D11, and indicate the status of the processor. The SE output indicates that the processor is busy (data in the output register are not valid) when it is high during D11. SF represents the sign of the output number, a high indicating a negative number. SG will be high if the processor is latched in an error condition. The SH flag can be used to provide leading zero suppression of the output data. The leading zero suppression function is provided by separate hardware in the display control logic, and the SH output is not used.

TABLE 6-1 RPM LOCATION ASSIGNMENTS

N/O	WORD			DIGIT				BIT	
A9	A8	A7	A6	A5	A4	A3	A2	A1	Ao
0 = Previous Value.	0	0	0 = N_o	0	0	0	0 = Sign	0	0 = MSB
1 = New Value	0	0	1 = N_{B+0}	0	0	0	1 = MSB	0	1 "
	0	1	0 = F_o	0	0	1	0 "	1	0 "
	0	1	1 = V_R	0	0	1	1 "	1	1 = LSB
	1	0	0 = Δ R	0	1	0	0 "		
	1	0	1 = Test Error	0	1	0	1 "		
	1	1	0 = Spare	0	1	1	0 "		
	1	1	1 = Coinc Delay	0	1	1	1 "		
				1	0	0	0 "		
				1	0	0	1 = LSB Display		
				1	0	1	0 = LSB		
				1	0	1	1 }		
				1	1	0	0 } NOT		
				1	1	0	1 } USED		
				1	1	1	0 }		
				1	1	1	1 }		

Gate 11P11 provides a transition used to latch the pulse-type flag outputs. The SE flag is latched by 10H2, and SG is latched by 11D13. The SF flag is converted into a NO-OP or SUBTRACT code by 11C4, and is inserted into the bit-parallel output data stream by multiplexer 11B. The SF flag is also used on board 10.

The KO input lead of 11J provides a master reset for the chip, and must be exercised to unlatch the processor from an error condition. The KO lead is activated by the STROBE, clearing the processor at the start of each sequence of calculations. The 400-nanosecond strobe pulse from board 2 is stretched by one-shot 10Q1 to ensure proper clearing of processor 11J. This stretched pulse is used to reset the sequencers on boards 11, 12, and 13, re-initializing the microsequence and display control logic with each new strobe.

The KP lead is used to indicate that data are being read into 11J via the KQ(input data) lead. KP is activated either by flip-flop 11K9 (in Mode 1) or by 11K2 (in Modes 2 or 3) when a new word is strobed into register 11R. The 11K outputs are combined by 11P4. The 11J input is inhibited in Mode 4.

Bit counter 11E, digit counter 11U, and associated gating form an address counter/burst generator for the microprocessor. These counters operate in Mode 2 to produce a series of 4-bit bursts to shift a BCD word from the counter/latch boards into 11J via register 12I and surrounding multiplexer logic. In Mode 3, these counters increment the address of 12K to access a serial word from memory, and provide the BURST pulses to shift this word, one digit at a time, into 12I. In Mode 4 the RAM address is again incremented while the BURST pulses operate through 12D9 to exercise 12K3, writing data bits into the RAM. The burst counters are not used in Mode 1, since data are transferred in parallel in this mode.

One-shots 1202 and 12012 produce a MICRO-INSTRUCTION CLOCK which increments microsequence counter 12G and triggers the board 11 burst generators when required.

A special mode is provided with the TMS-0117 wherein data input is accelerated by activating the KP lead for the duration of a number entry. In this mode, input data are changed upon the positive transition of the SR lead. The control logic surrounding the burst generator and micro-instruction clock generator implements this special mode. It is interesting to note that, even with the special mode of data entry, the time required to enter data into the processor consumes 1.5 seconds out of the 1.8-second total microsequence execution time.

Mode 1. In this mode, data are transferred directly from PROMs 12M, 12N into processor 11J. The data are in a parallel format consisting of a control bit and a four-bit code. The data are level shifted by 12U and 12L from the 5-volt PROM levels to 12-volt CMOS levels. The control bit pulses through 11S3 to 11R15. The four-bit code passes through multiplexer 12Q to the 11R parallel inputs.

The mode 1 instruction is accessed on the positive transition of MICRO-INSTRUCTION CLOCK by advancing counter 12G. The PROM address is incremented, level shifted by buffers 12E and 12F, and is applied to 12M, 12N to access the instruction. The MICRO-INSTRUCTION CLOCK disables the bit counter 11E by setting flip-flop 11D1 via 11S13. The digit counter will be disabled with 11U5 at a high level in Mode 1. Burst generation is therefore inhibited in this mode.

One shots 120 are allowed to time out, permitting the PROM data to stabilize. Gates 11L10 and 11L4 will then become active, permitting the next SF STROBE to read the data into 11R and to set flip-flop 11K9 via 11L3.

This action initiates a data entry into 11J, with the data bits shifted out of 11R.

With data entry in progress, a positive transition will occur on the CHIP BUSY latch output 10H1. One-shot 1202 is fired, producing a MICRO-INSTRUCTION CLOCK pulse, incrementing 12G.

If the newly-accessed instruction also calls for a Mode 1 operation, 11L10 will again permit the instruction to be loaded into 11R via the action of 11L3. Flip-flop 11K12 will remain set as long

as Mode 1 instructions are received, permitting the Mode 1 data to be rapidly entered into the processor. When a Mode 2, 3 or 4 instruction is received, 11K12 will be reset and 11L10 disabled, terminating the data entry.

Mode 2. This mode provides data entry into the processor chip from the registers on boards 4 through 8. These registers are concatenated, providing N_0 followed by N_{B+D} with two successive Mode 2 instructions. The data format is bit-serial BCD, with MSD/MSB appearing first in the data stream. The MSD of each number is made zero by 8G and 8I. Nine additional digits are provided by the BCD counters. This provides ten digits of data per count, compatible with the microprocessor data format. While a bit-parallel format would have been preferred for the counter data, the bit-serial format permitted the use of previously-built counter/latch boards in the extractor.

The BCD data stream appears at 8I3 and passes through 12T4, 12T11 to 12I15. A BURST of four pulses loads a digit into 12I, where the parallel BCD data passes through 12Q to register 11R.

The counter data represents numerical information. The control bit is correspondingly a zero, with 11S1 and 11S2 both high in this mode.

Counters 11E and 11U are self-completing. Once triggered, these counters will produce a complete burst sequence, and "hang up", with gates 11S10 and 11C11 activating count inhibit leads 11E5 and 11U5. The burst generators are triggered by resetting 11E and 11U.

In Mode 2, counter 11U will initially be hung up at a count of 12 via 11S10. The MICRO-INSTRUCTION CLOCK will hold 11E at a count of zero via 11S11 and 11D1. The PROM instruction is allowed to stabilize while one-shoot 120 times out.

When the MICRO-INSTRUCTION CLOCK goes low, 11N5, 11N3, and 11N4 will be low. The CHIP BUSY lead is monitored to ensure that the processor is ready to accept new data. When this lead goes low, all inputs to 11N1 will be low, activating 11U1. Digit counter 11U is preset to a count of one due to the wiring of jam lead 11U4. 11010 will now go low, enabling the digit counter. The

bit counter is enabled via 11C11 and 11015. Flip-flop 11D1 is reset via 11P3, triggering a burst sequence. Observe that 11P10 and 11M10 are always low in Mode. 2.

Gates 11M3 and 11M4 form a set-reset flip-flop. 11M3 provides a gate for the four-pulse bit-clock bursts. 11M3 is set low when counter 11E counts to four, providing guard time to avoid any spikes in the burst. The 156-kHz clock is gated by 11L11 to produce the BURST signal. The BURST is gated by 11V9 and allowed to produce SHIFT 1 pulses in Mode 2. The SHIFT 1 pulses shift four bits of data (one BCD digit) out of the counter/latch registers. The BURST signal clocks these bits into register 12I.

When bit counter 11E counts to eight, the burst is complete. Gate 11C11 will inhibit 11E, while 11M3 will go high. Gate 11L10 is low in Mode 2, so 11L4 will go low, permitting the SF STROBE to clock the BCD digit into 11R and set flip-flop 11K2 via gate 11L3. As in Mode 1, this action initiates the TMS-0117 input sequence, entering the digit into the processor. 11K2 will remain low for the remainder of the burst sequence, providing the special fast data entry operation of processor 11J. The positive transition on 11E2 increments counter 11U.

A positive transition on the CHIP BUSY lead will set 11D1, which in turn resets 11E. Gate 11C11 goes low, enabling counter 11E and resetting 11D1 via 11P3. A new four-bit burst is generated.

In this way bursts are produced and digits are read into 11J. Data are updated with positive transitions of the CHIP BUSY 1 lead, in keeping with the special mode of data entry. When 11U counts to eleven, 11V6 will go low, disabling SHIFT 1 pulses via 11V9. Ten digits of valid data are shifted out of the counter/latch registers.

Since the BURST is still enabled when 11V6 goes low, invalid data will be shifted into 12I. Completion of the final burst will jam the invalid data into 11R. However, gate 11S10 detects that 11U has incremented to twelve, and that the burst sequence is therefore complete. Flip-flop 11K2 is immediately reset, taking down the 11J KP lead and causing the processor to ignore the invalid data on the KG lead. Counter 11U is disabled via 11010,

and 11E is inhibited via 11C11 and 11015.

The positive transition at 11010 fires one-shot 12012, accessing the next micro-instruction.

Mode 3. This mode allows an eleven-digit word to be read from the RAM into the processor. The address of the desired word location is contained in the micro-instruction requesting the transfer. The microprocessor timing logic must provide a series of eleven four-bit bursts to access the bit-serial RAM data one digit at a time. The bit and digit addresses within the desired word block are provided by the microprocessor timing logic.

The MICRO-INSTRUCTION clock will set 11D1, holding 11E at zero. 11U5 will be locked in a high state, as in the other modes. When one-shot 120 times out, 11N1 will go high as soon as CHIP BUSY goes low. Counter 11U is preset to zero, causing 11010, 11015, and 11D1 to go low, initiating the burst sequence.

The BURST signal is generated in the same way as Mode 2. SHIFT 1 pulses are inhibited by 11V9 in Mode 3. 11U is preset to zero instead of one, producing eleven valid bursts instead of ten. RAM data from 12K12 passes through 12A3, 12D6 and 12T11 to 12I15. The data are clocked into 12I with the BURST pulses, and loaded into 11R when 11E2 goes high. 11K2 activates the KP lead of 11J, providing the special rapid data entry in this mode also. The data are loaded into 11J. A twelfth data burst is produced, representing invalid data at the end of the sequence. The invalid data are ignored by resetting 11K2 when 11010 goes high.

The first "digit" of the RAM data represents the sign of the incoming number. The sign is presented to the TMS-0117 as either a NO-OP or SUBTRACT code, causing the processor to handle the number properly. The RAM does not store the control bit. Instead, 11N13 detects when the sign is being entered into 11J, and forces the control bit to a one via 11S4 and 11S3.

The RAM address and data leads are normally accessed by the display control logic. When a Mode 3 sequence is in progress, 11C11 will be high, producing an INTERRUPT signal (inverted) at 11F4. The INTERRUPT signal causes multiplexers 11R, 11S, and 11T to

switch the RAM address inputs and data leads to the microprocessor logic. The RAM is thus "stolen" for about 0.5 milliseconds. The display is blanked by the INTERRUPT signal.

The most significant bits of the RAM address, representing the word block address, are provided directly by PROM 12M. The RAM address assignment of Table 6-1 permits the 11E and 11U outputs to be used directly as the bit and digit address leads.

Gating is provided on board 12 to force RAM data to zero under certain conditions. When the mode control logic of board 3 produces a MASTER RESET signal, the RAM must be cleared. Since the 2602 does not provide a clear lead, this function is provided indirectly. Flip-flops 12C are cleared by the MASTER RESET signal. Immediately following the MASTER RESET, 12C13 will be low. Whenever previously calculated RAM data are addressed, represented by a low at 12R13, 12A10 will go high, forcing 12A3 to zero. Data entered into the RAM during the current micro-sequence are not affected, since 12R13 will be high when this data are accessed. The RAM data appears exactly as if the RAM had been cleared directly by the MASTER RESET pulse.

At the completion of each series of calculations, a positive transition is produced on the N/O lead by the board 10 logic. The toggling action of 12C2 inverts the new/old address lead via gate 12J10. This provides the effect of interchanging new and old data without actually moving bits. With the completion of the initial calculations, the first N/O transition will set 12C13, enabling previously calculated RAM data, which is valid from that point on.

When the extractor is in the DRO readout mode, the counters are reset following each STROBE. A branch would normally be required in the micro-program, subtracting previous N_{B+D} and N_O values from current values to obtain a net count for the just-completed interval in NDRO operation, while directly using the new values (without subtracting) as the net interval count in DRO operation. This branch (and corresponding branch hardware) is avoided by setting 12H13 in the DRO mode, causing gates 12B4 and 12D5 to zero the RAM data when 12A4 detects that previous N_{B+D} or N_O data are being

addressed. The microprocessor subtracts the previous values from current values, regardless of the DRO/NDRO setting, with the DRO subtraction rendered harmless by the above gates.

The micro-program provides for accumulation of ΔR by adding the previous ΔR value to the new ΔR result. The accumulator action can be disabled in hardware, once again avoiding a branch in the micro-program. When the DISABLE ΔR ACCUM lead is high, 12D10 will go low whenever the ΔR address is detected via 12A11, forcing previous ΔR data to zero via 12D6.

Logic on board 2 provides the DISABLE ΔR ACCUM signal. Pin 2C6 will disable the accumulator when in the DRO mode or when the rear chassis lip switch is set to the DISABLE position. In certain cases, the accumulator can overflow, exceeding the capacity of the processor. This would cause the processor to lock up in an error condition, disrupting other calculations until the next STROBE cleared 11J.

A test is provided in the micro-program to detect when the ΔR accumulator is about to overflow. When the accumulator contents exceed 4,000,000 meters, this test will produce a positive number in the 11J output register. The SF lead of 11J is sampled by a ΔR STROBE, generated when the test result is in the output register. If the output register contents are positive, 2G2 will go low, disabling the accumulator to prevent the overflow. Gate 3E3 will produce an OVERFLOW indication when this happens. The overflow condition is cleared by resetting 2G2 whenever the accumulator is cleared. Gate 2K11 provides the proper pulse to clear 2G2, since the accumulator is cleared either by a MASTER RESET or by a DRO readout.

When the Mode 3 sequence has been completed, one-shot 12012 will fire, accessing the next micro-instruction.

Mode 4. This mode permits the contents of the 11J output register to be written into RAM 12K. Burst generators 11E and 11U are again used. Since the write sequence must be synchronized with the 11J digit scan leads, however, the bursts are triggered in a different manner than in the other modes.

The MICRO-INSTRUCTION CLOCK will initially force 11D1 to a high. Unlike the other modes, 11D1 is not cleared when the MICRO-INSTRUCTION CLOCK goes low. 11V10 will hold 11D1 high while the DIGIT CLOCK from 11J is high. Gate 11P10 will reset 11D1 when the DIGIT CLOCK goes low. In this way BURST pulses are triggered by the DIGIT CLOCK.

Digit counter 11U must be synchronized with the 11J digit scan leads. When the MICRO-INSTRUCTION CLOCK goes low, 11N3 and 11N5 will be low. 11N2 will be low when the 11J register contents are valid. Gate 11M10 will produce a low output when the SF STROBE is active. Thus the positive transition of 11N1, which initiates the Mode 4 sequence by resetting 11U, is synchronized with the D11 clock.

The eleven-digit BURST is generated in a manner similar to Mode 3, except that each four-bit burst is initiated by a negative transition on the DIGIT CLOCK. With the output of each new digit, indicated by the DIGIT CLOCK, the BURST loads this digit into the RAM.

Since the bit and digit counters are synchronized to the 11J digit scan leads, these counter outputs are used directly as the bit- and digit- address locations for the RAM. Gate 11F4 provides the INTERRUPT signal while the write operation is in progress, causing the board 12 multiplexers to switch the RAM to microprocessor control. The word block address is stored in PROM 12M, as an integral part of the write instruction.

Gate 12D9 activates the read/write lead of RAM 12K, so that the BURST pulses cause the data to be shifted out of 11A and written into the RAM. Multiplexer 11B inserts the sign code into the data stream, as previously described. Register 11A is loaded with the DIGIT CLOCK.

At the completion of the Mode 4 sequence, 12012 will fire, accessing the next micro-instruction. Since this causes the MICRO-INSTRUCTION CLOCK to go high, 11N1 will be disabled, providing a single write burst. The sign code is actually written twice (at the beginning and end of the sequence), but this is harmless.

NOTE: ALL BITS EXCEPT CONTROL BIT ARE INVERTED IN PROMs.

Figure 6-20. MICRO-INSTRUCTION Format

The micro-instruction format is shown in Figure 6-20. The two-bit op-code specifies the microprocessor mode, and is decoded by gates 12P and 12J4. The flag bit is latched by 12H1 to prevent spikes, and increments sequence counter 10R. The remaining five bits provide Mode 1 data or Mode 3 and 4 address information.

Sequence counter 10R is initialized either by MASTER RESET or STROBE. The flag bits from PROM 12N are placed at the completion of each calculation, incrementing 10R. When 10R counts to eight, the micro-sequence is complete. 10M2 will activate the STOP lead, which inhibits further advancing of the micro-sequence. The eighth flag is coincident with a Mode 4 instruction. This instruction is executed, the next instruction accessed (a NO-OP instruction), 12H2 will then go high, allowing 12B3, 12V4 and 12V3 to freeze the sequence.

A new STROBE will reset 12G, 12H1, 12O, and 10R, initializing the micro-sequence for a new series of calculations. Gate 10G3 generates the N/O signal, indicating when a new sequence has begun. When the integration period of the extractor is less than 2 seconds, the STROBE will occur before the previous micro-sequence is complete. In this case register 10A stores the count of 10R at the time of the STROBE. This information is used to blank the display should non-calculated parameters be selected.

Flip-flop 10Q13 latches the ERROR signal from the TMS-0117. This signal produces a special code on the display and sends a flag to the computer to indicate the error condition. The presence of this signal will force a self-test to fail by setting 1001 and 10013.

Three tests are provided in the micro-program. These tests are used to check the ΔR accumulator for overflow, as described earlier, and to produce the self-test pass/fail indication. The sign of the 11J output is sampled (SF lead) to indicate the results of the tests. Flag bits are placed in the micro-program when the

test results are available. With a flag present and the 11J data valid (10H2 high), 10G13 is high, allowing the SF STROBE to produce a negative pulse at 10G11.

Should the flag represent the presence of ΔR accumulator test data, 10F6 will be low, resulting in a ΔR STROBE at 10E4. Should the result of the self-test frequency error check be present, 10F10 will be low, causing the 11J sign information to be latched by 10013. 10M2 permits the coincidence delay test result to be stored in 1001. The R-C filter at 10G13 allows the sequence counter to stabilize before the flag bit is recognized.

The self-test results indicate a pass condition when the signs of the two test numbers are both negative. Should this be the case, the P/F ENABLE lead, activated by the board 3 logic, will produce a PASS indication at 10P4. Otherwise a FAIL indication will be given at 10P3.

Buffers 12E and 12F provide level shifting from CMOS to TTL levels to operate the PROM and RAM chips.

6.3.1.9 Microprocessor software. The microprocessor software is the set of instructions stored in the PROMs, which when executed produce the navigation parameter calculations.

The development of the microprocessor hardware and software was done simultaneously, and the two are very closely linked. This minimized the total development time. The software was written to provide maximum possible accuracy, eliminate branching, to provide test result indicators where required, and to handle the quirks of the microprocessor hardware.

The instruction format of the TMS-0117 is presented in Appendix C. The TMS-0117 performs fixed-point arithmetic operations to ten-digit accuracy. Calculation results are truncated to ten digits. The contents of the output register may be shifted left or right, and operands may be interchanged with proper commands. An implied constant feature reduces the number of data entries.

The features of the TMS-0117 are expanded by the microprocessor hardware to implement the micro-instruction set summarized in Table 6-2. This micro-instruction set results in a relatively simple and straightforward micro-program.

The micro-program is designed to operate without branching. The complete sequence is executed, regardless of extractor mode of operation. Gating is provided to avoid branching based on DRO/NDRO operation. The shift-left/shift-right instructions possess a characteristic which is exploited to avoid other branch decisions. If the TMS-0117 contents are shifted left and then right, a zero will result in the MSD position. Similarly, a shift right followed by a shift left results in a zero in the LSD position. Zeroes may be placed in MSD or LSD positions by proper combinations of left- or right- shift instructions. This characteristic permits manipulation of a portion of the register contents by selectively setting the remaining digits to zero.

The microprocessor hardware fixes the decimal point for all calculations to the right of the MSD. This decimal position provides the maximum dynamic range for the fixed-point multiplications and divisions. Scaling is provided within the software to avoid overflow during these operations. Scaling is accomplished with shift left or right commands.

During software development, a breadboard TMS-0117 calculator was built to test the algorithms. Work with the breadboard uncovered a "bug" in the TMS-0117 internal program. Certain combinations of multipliers and multiplicands will result in erroneous overflow. In particular, if the multiplicand (first number) is between 1 and 10, and the multiplier is between 1.4 and

TABLE 6-2. MICRO-INSTRUCTION SUMMARY

Instruction	Mode	Code[1]	Execution Time (mSec)	Description
ENT (Y)	1	00-0YYYY	3.25	Enter BCD Digit Y into Processor.
DOPP	2	01------	35.75	Enter Ten Digits from Extractor Registers into Processor.
READ (Y)	3	10-0YYYY	40.06	Read Ten Digits and Sign from RAM Word Location Y into Processor.
WRITE (Y)	4	11-0YYYY	2.15	Write Contents of Processor Output Register (Ten Digits and Sign) into RAM Word Location Y.
CLR	1	00-10000	5.39	Clear Processor Output Register.
EQ	1	00-10001	4.31 + T_{INSTR}	Execute Instruction[2].
MULT	1	00-10010	48.06	Multiply Register Contents by Following Entry.
DIV	1	00-10011	54.31	Divide Register Contents by Following Entry.
ADD	1	00-10100	9.68	Add Following Entry to Register Contents.
INC	1	00-10101	6.44	Increment Register Contents by 1-LSD.
SUB	1	00-10110	9.68	Subtract Following Entry from Register Contents.
DEC	1	00-10111	6.44	Decrement Register Contents by 1-LSD.
ADOVF	1	00-11000	4.13 + 1.075 (10^{10} - REG)	Increment Register Contents to Overflow.
DEZRO	1	00-10001	4.13 + 1.075 (REG)	Decrement Register Contents to Zero.

TABLE 6-2. MICRO-INSTRUCTION SUMMARY (Cont'd)

Instruction	Mode	Code[1]	Execution Time (mSec)	Description
SR	1	00-11010	5.39	Shift Register Contents to Right.
SL	1	00-11011	5.39	Shift Register Contents to Left.
EXO	1	00-11100	7.56	Exchange Operands.
NO-OP	1	00-11111	4.31	No Operation.

NOTES:

1. See Figure 6-20 for MICRO-INSTRUCTION format.
2. Implied Constant (Last Instruction and Operator) Available by Using this Operator.

1.7, an overflow occurs, even though the product is less than ten. The software is written such that the multiplier is always less than 1, avoiding the "bug". The only penalty paid is the loss of one significant digit in the ΔR calculations.

Display of meaningless calculations, such as TEST ERROR when not in the self-test mode, or COINCIDENCE DELAY when in the ARO mode, is inhibited by the extractor hardware.

The micro-program is detailed in Figures 6-42 through 6-51. The following sequence of operations is performed:

1. Read and store new N_0 count.
2. Calculate and store new ΔN_0 for the interval.
3. Read and store new N_{B+D} count.
4. Calculate and store ΔN_{B+D} for the interval.
5. Calculate and store F_D, where

$$F_D = \left[\frac{\Delta N_{B+D}}{\Delta N_0} \times 1.25\times10^6 - 10^6\right] \times \frac{221}{192}$$

6. Calculate and store V_R, where

$$V_R = -\lambda_t \bullet F_o = \left[\frac{\Delta N_{B+D}}{\Delta N_0} \times 1.25\times10^6 - 10^6\right] \times \left(-\frac{221}{192}\lambda_t\right)$$

and $\frac{221}{192}\lambda_t = 0.1641799015$ meters

7. Calculate and store ΔR, where

$$\Delta R = -\left[\Delta N_{B+D} - \frac{F_b}{F_o}\Delta N_0\right] \times \frac{221}{192}\lambda_t$$

and $\frac{F_b}{F_o} = 0.8$

8. Test the ΔR value for magnitude greater than 4,000,000 meters, and allow sign of test to be picked up by micro-processor hardware.
9. Calculate and store the TEST ERROR, which is the difference between F_D and its nominal self-test value of -328.8690477 kHz (translated to equivalent transponder

input shift).

10. Determine whether the TEST ERROR magnitude is greater than 0.3 Hz, and allow sign of this check to be picked up by microprocessor hardware.

11. Calculate and store the COINCIDENCE DELAY associated with the strobe initiating the calculations.

12. Test the COINCIDENCE DELAY for values greater than 100-microseconds. Allow the sign representing this test result to be picked up by microprocessor hardware.

Micro-instruction 0 provides a "dummy" write, permitting the self-completing burst generators to time out in case a sequence abortion occurred during a Mode 2, 3 or 4 operation.

The calculation of ΔN_0 and ΔN_{B+D} must take into account the overflow of the extractor counters. This is done by incrementing the new counts as if overflow had occurred. The MSD of the data was made zero by the hardware. Adding a 1 in the MSD position provides the assumed overflow result. The net counts for the interval are calculated, using the actual previous counts. If overflow occurred in the counters, the result is correct. If not, the result is in error by a 1 in the MSD position. Selectively zeroing the MSD through the shift left--then right-- operation produces the correct net count, whether or not the overflow actually occurred.

The scaling operations are illustrated by the input-output format entry to the right of the micro-instruction listing. The correlation between digits in the 11J output register, the RAM, and the display is shown in Figures 6-42 through 6-49 to indicate the effect of shifting operations on the RAM and display contents.

The three software tests are performed as follows: The ΔR result is shifted right and multiplied by itself to provide ΔR^2 with as many significant digits as possible without overflow. The maximum allowable ΔR^2 is subtracted. The sign of the difference will be negative if the ΔR value is within limits.

Similarly, the TEST ERROR is shifted left and right to retain only the five LSDs. The result is multiplied by the unmodified TEST

ERROR to provide a number which corresponds to the square of the TEST ERROR. This approach provides full test accuracy for small errors up to 9.9999 Hz, while at the same time detecting large errors which may have zeroes in the LSD positions. The resolution of the test is thus ten digits, while at the same time overflows are avoided.

The COINCIDENCE DELAY test simply subtracts 100 microseconds from the always-positive delay value.

The delay calculation itself is based on nominal counts for the integration period. Six integration periods are possible, normally requiring a branch. However, all integration periods are multiples of 100-milliseconds. The six LSDs only may be used to calculate the delay, independent of the integration period. This places an upper bound of 100-milliseconds on the range of delays handled by this algorithm. Since the capacity of the display is only 100-microseconds, the limit is of no consequence. This approach does not work in ARO operation, since in the ARO mode the nominal integration period is not known. The COINCIDENCE DELAY display is blanked in the ARO mode for this reason.

Since the extractor counters are reset to one instead of zero, the minimum delay appearing on the display will be 1-microsecond. The display indicates an actual delay between the displayed value and that value minus 1-microsecond. Resetting the extractor counters to one avoids division by zero in the micro-sequence.

Calculation results are truncated to ten digits by the TMS-0117. Inaccuracies resulting from truncation are partially corrected by adjusting the values of the micro-program constants.

6.3.1.10 Display. The display logic provides simultaneous display of up to two parameters stored in the RAM. The displays are digit-scanned, with the display logic providing the address information to step through the RAM. Leading zero suppression is provided to enhance display readability. The display is blanked should uncalculated or invalid parameters be selected. An error symbol is provided in the event of a microprocessor error.

The display logic layout is shown in Figures 6-25 and 6-26. Schematics are shown in Figures 6-39 and 6-40.

Gates 15F encode the selection for Display A into a 3-bit binary number. This number corresponds to the sequence count representing the calculation of the desired parameter. The representation of the Display B selection is either zero or seven, and the encoding is done directly.

The A and B displays are alternately scanned, based on the toggling action of 13J12. Multiplexer 13N selects the code for the display word to be scanned, and provides the word-block address information to the RAM. The MSB of the address is always zero, causing only previously-calculated results to be displayed.

The SEQUENCE STATUS is ones-complemented by register 10A. When the DISPLAY WORD is added to the complemented SEQUENCE STATUS in adder 13M, the result represents the difference of these numbers minus one. 13M14 will be high if the SEQUENCE STATUS is less than the DISPLAY WORD plus 1, and low otherwise. Since the sequence counter increments following the calculation of each parameter, 13M14 indicates whether or not the selected parameter was calculated. If 13M14 is high, the display is blanked.

The bit- and digit- scanning of the RAM is provided by 13X and 13W, respectively. A 156-kHz clock increments the bit counter on positive transitions. The RAM data enters 13H via gate 12A3, which zeroes the display data at the start of a measurement sequence.

The correspondence between display digit and RAM address is not always one-to-one, as indicated on Figures 6-42 through 6-49. This condition arises because a previously-built 9-digit display is used to display the ten-digit-plus-sign RAM contents.

When displaying the N_0, N_{B+D}, and COINCIDENCE DELAY parameters, the display digit and RAM address agree. Addresses 1 through 9 correspond to the nine MSD positions in memory. These parameters do not carry a sign.

The remaining parameters carry a sign, which occupies digit position 1 of the display. Display digits 2 through 9 correspond to RAM addresses 1 through 8, the eight MSDs of the RAM word.

Counters 13R, 13T and 14BB scan the display. 13R scans the B

display, while 13T and 14BB scan the A display. Counter 14BB is functionally identical to 13T, and was provided to reduce the number of output leads on pin-limited board 13. The display and RAM address counters increment on the positive transition of the 156-kHz clock. The resulting serial data at 13H7 are clocked into 13H on the negative transition of the 156-kHz clock. On the next positive 156-kHz transition the parallel BCD data are clocked into register 13G, where the data are held for display. Observe that 13R and 13T increment on this second positive transition, and that these counters energize the digit scan for data corresponding to the previous count of 13W. The correct synchronization for the display of signed parameters is obtained by setting the digit scan and RAM address counters to the same value.

Decoding gates 13O, 13P6, 13I11, and 13I4 detect the selection of a signed parameter and place a zero at 13U6, leaving the DISPLAY DIGIT address at the 13U outputs unchanged.

When N_0, N_{B+D}, ΔN_0, or COINCIDENCE DELAY is selected, 13U6 will be high. Adder 13U will increment the 13W count by one to form the correct DISPLAY DIGIT address.

Observe that the RAM will always carry at least one significant digit more than will appear on the display. This provides maximum accuracy when multiple calculations are made.

The A and B displays are alternately scanned, with the A or B digit counter enabled and the corresponding display select code accessed depending on the state of 13J13. When operating in synchronization, one of counters 13R and 13T will be enabled via 13L13 and count through to zero, whereupon 13J13 toggles and the other counter will be enabled. The use of 13L13 allows the counters to count to zero before being disabled. One of 13R or 13T will be counting, with the other counter disabled in the zero state. Should the counters lose synchronization (both counters out of the zero state), 13L1 will be set, re-synchronizing them. The STROBE is also used to set 13L1, synchronizing the counters with each new data readout.

The decoded outputs of 13R and 14BB drive the digit scan circuits on board 14. When activated by a high input level, the digit

drivers (detail YY on board 14) place about 4.4-volts on the corresponding LED display digit anodes, activating them. Counter position 0 is used for synchronization, as just described. Positions 1 through 9 are used to scan the 9-digit A display, while positions 7 through 9 (corresponding to the three LSDs of the full display word) are used to scan the 3-digit B display. The 12-digit display is scanned every 0.512-milliseconds.

Display data held in 13G normally passes through multiplexer 13F and 12- to 5-volt level shifters 13E to decoder 14AA. The resulting decoded outputs operate the segment drivers (detail XX on board 14). These drivers ground the cathodes of the LED displays, causing the appropriate segments of the activated digit to light.

The decimal points on the two LSDs of Display A are used. When ΔR is displayed, 13A4 will be low, causing driver 13V to activate the LSD decimal point. When F_D, V_R, or TEST ERROR are displayed, 13A6 will be low, causing driver 13S to activate the other decimal point.

The Display A sign is generated as follows: When one of the signed parameters is selected, 13I11 will be high. When the Display A scan counters are in the digit 1 (sign) position, 13B4 will go low, activating the blanking input of decoder 14AA. This input forces the 14AA open-collector outputs to be "off" (high level), regardless of the levels at any other inputs. The sign is stored as a TMS-0117 NO-OP code (1111) if positive, and as a SUBTRACT code (0110) if negative. If a positive sign is present, the sign display is left blank. If a negative sign is present, decoder output 13D7 will go high, grounding the segment g cathode via driver 13A2 and the diode. This will cause the minus sign to appear on the display. Since segment g is also lit when decimal 6 (also coded 0110) appears on the display, the OR arrangement formed by the open-collector 14AA output and the diode provides proper operation of the segment g driver.

When 10Q12 indicates a microprocessor ERROR, multiplexer 13F will force 1100 onto the display data lines, causing the error symbol (␣) to appear on the display. This symbol will not appear in the sign position, since the blanking action of the 14AA4 input will

override it.

When flip-flop 3K13 provides the DISPLAY TEST signal, this signal is level-shifted by 3C10 and the associated resistor-diode network and activates 14AA3. This action lights all of the display segments (with the exception of the Display A sign position, where the 14AA4 input again overrides). The sign position may be tested by selecting one of the unsigned parameters.

The extractor display must be blanked under certain conditions. If the display parameter was not calculated, or if the TEST ERROR parameter is selected when not in the self-test mode, or if the COINCIDENCE DELAY parameter is selected when in the ARO mode, or if the display logic receives an INTERRUPT from the microprocessor, the display is blanked. Leading zeroes of displayed parameters are blanked. These blanking operations are provided by logic on board 13.

If the display parameter was not calculated, 13Q4 will be low. If the TEST ERROR parameter is improperly selected, 13I10 will be low. When the microprocessor provides an INTERRUPT, input pin 18 of board 13 will be low. A low at any of these points will cause 13C10 to go high, causing 13A15 to go low.

If the COINCIDENCE DELAY parameter is improperly selected, 13I3 will be low. When the two display counters are in the initial position (representing the start of a new scan) 13B11 will be low. If any of 13A15, 13I3 or 13B11 are low, 13C9 will be high, blanking the display through 13K4, 13E4 and 14AA5. The 14AA5 input will not blank the display unless the BCD lines are zero. Gates 13Q3 and 13Q11 disable multiplexer 13F, forcing the BCD lines to zero.

Output 13C9 will set flip-flop 13J2. Due to the feedback through gate 13P10, 13J2 will remain set until either 13K3 or 13C6 go high. Output 13K3 will be high when a non-zero/non-sign digit is present on the BCD lines. Output 13C6 will be high when the last display digit (least-significant) is being scanned or when the digit preceding a decimal point is being scanned. With 3P10 high, the display remains blanked until one of these conditions is met. Leading-zero blanking is thus provided, with the display blanked

at the start of each new scan, and unblanked either by a non-zero digit or by the scan of the "units" display position.

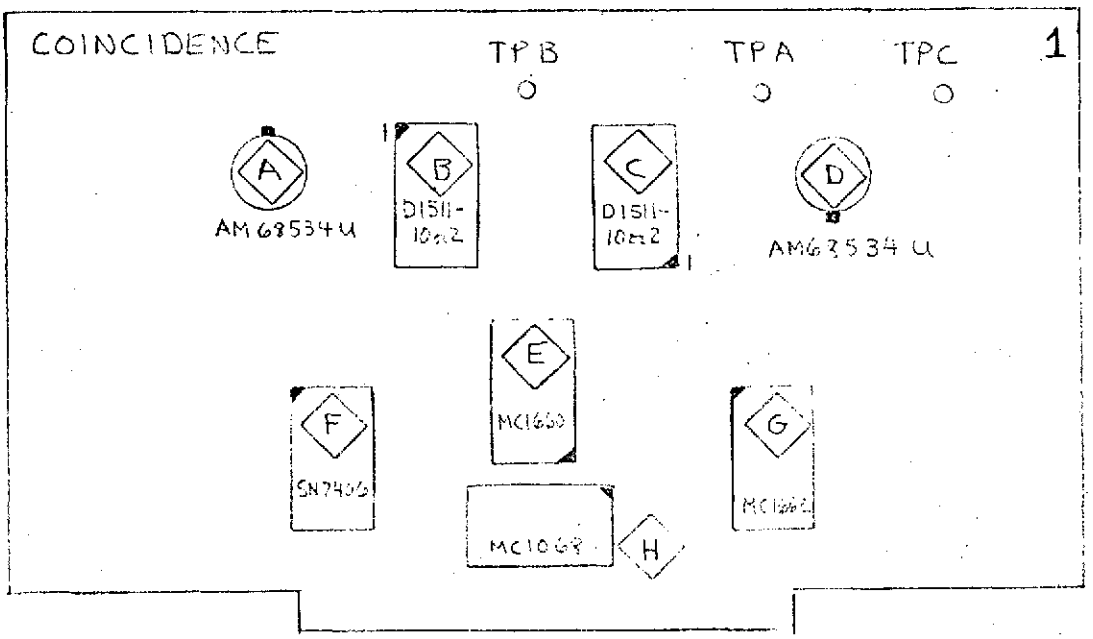
The minus sign display is not blanked. The microprocessor error indication and the display test will override the blanking of leading digit positions.

Due to the storage in registers 13H and 13G, these registers must be lceared to prevent data from INTERRUPT operations or data representing uncalculated parameters from improperly unblanking the display. At the same time, register 13H must be allowed to store the sign of a valid word (which is available while 13B11 is low). Output 13C10 is therefore used to clear the data registers.

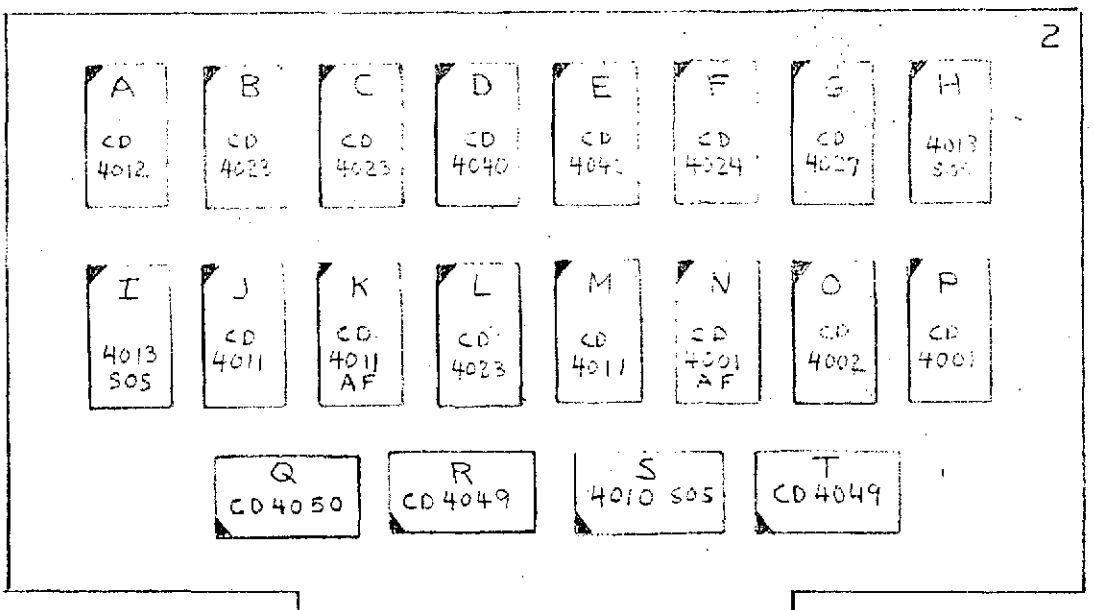
The zero-blanking circuits will not unblank the display following an INTERRUPT until the start of a new scan. The display scan rate is a compromise between noticeable disturbance caused by the blanking action (scan rate too slow) and background "noise" caused by the relatively slow display driver switching (scan rate too fast).

The display drivers introduce excessive noise on the display power input leads. This noise is decoupled from the other extractor circuits by the filters shown in Figure 6-29.

Table 6-4 details the wiring of the display drivers.

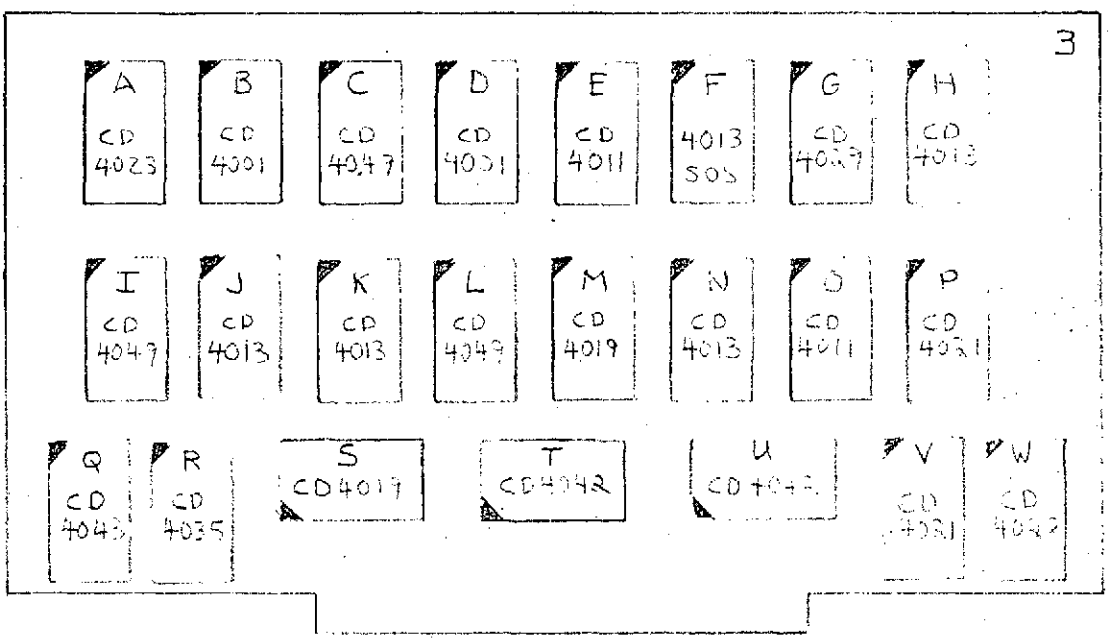


BOARD 1- COINCIDENCE DETECTOR

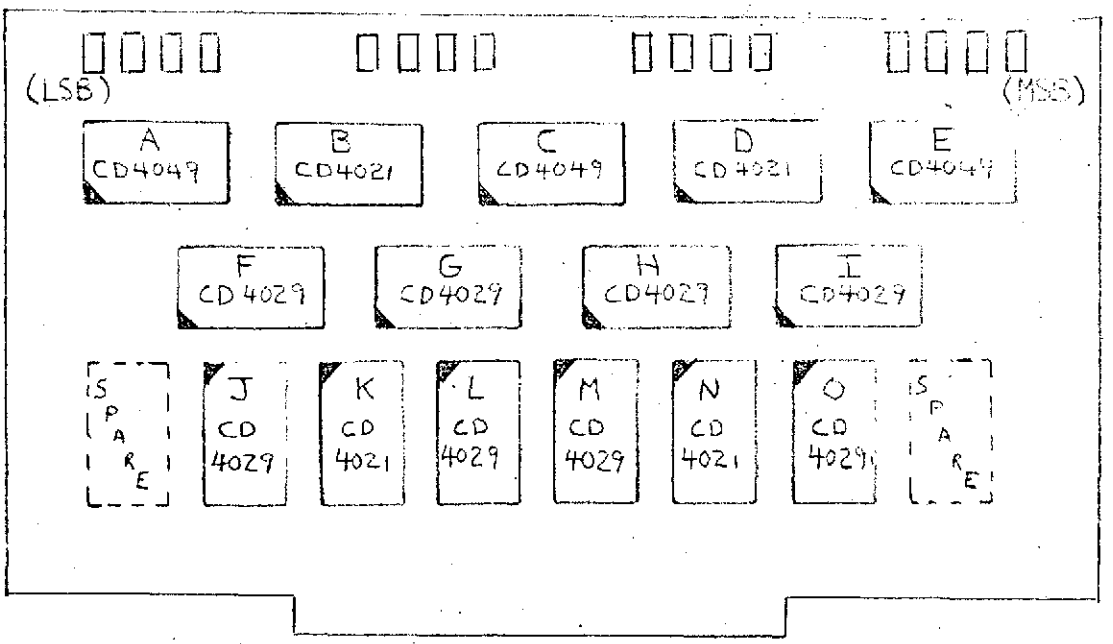


BOARD 2- INTERVAL TIMER

Figure 6-21. Layouts, Board Numbers 1 and 2

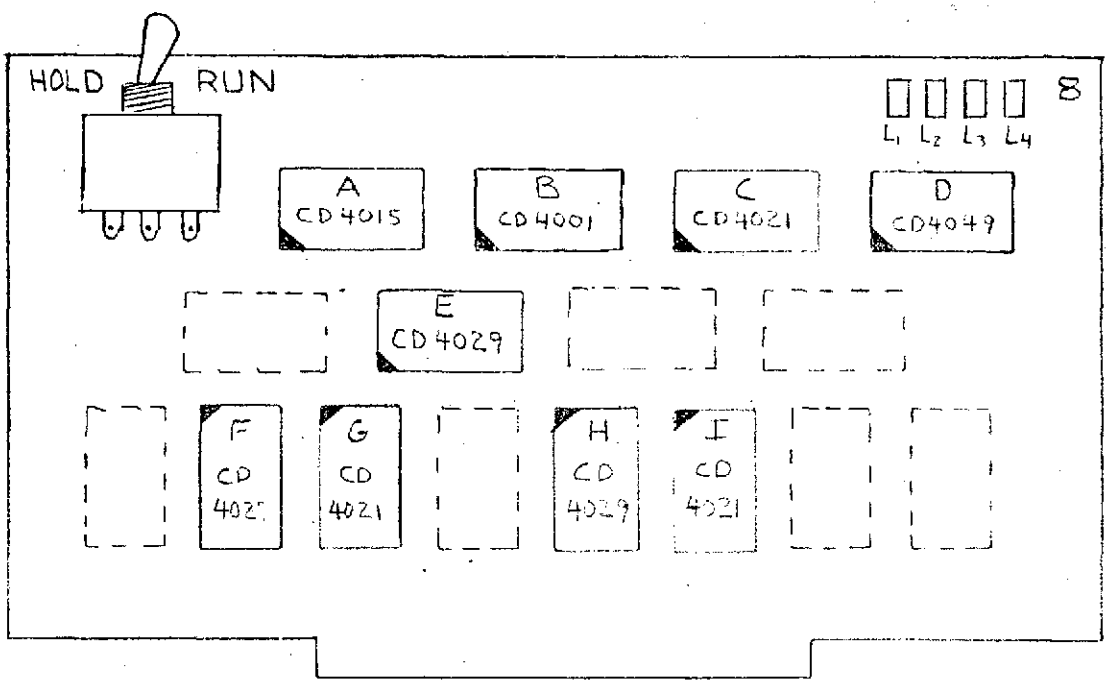


BOARD 3 - MODE CONTROL

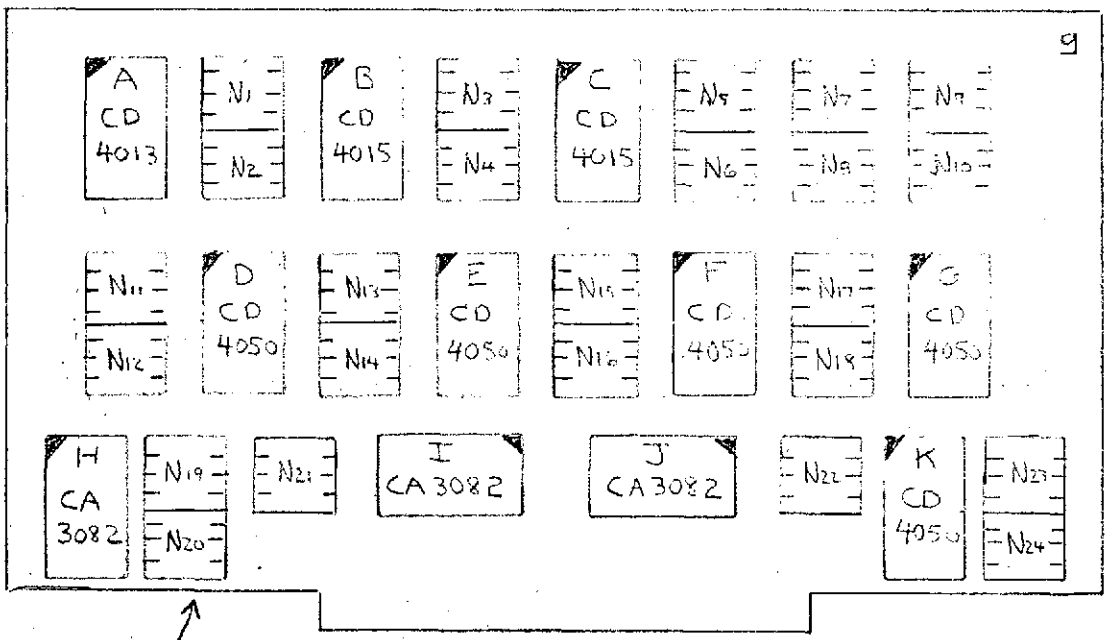


BOARDS 4,5,6 & 7 - COUNTER/LATCH

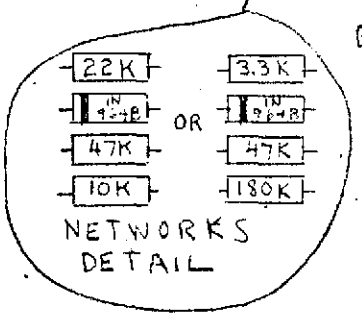
Figure 6-22. Layouts, Board Numbers 3 through 7



BOARD 8- MISCELLANEOUS COUNTER

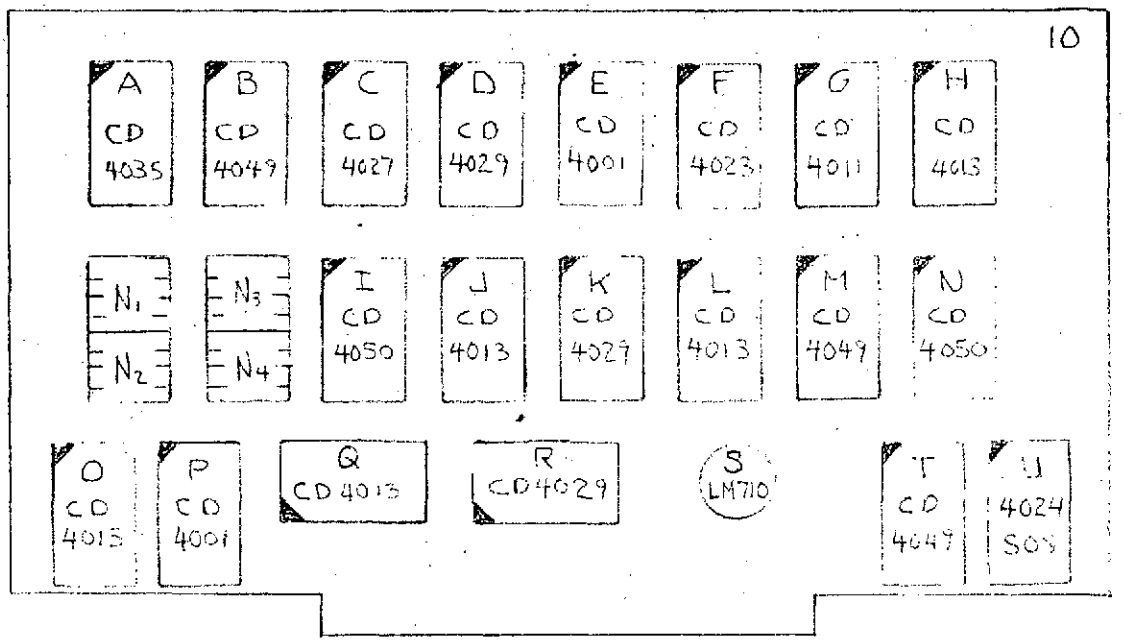


BOARD 9 - COMPUTER INTERFACE



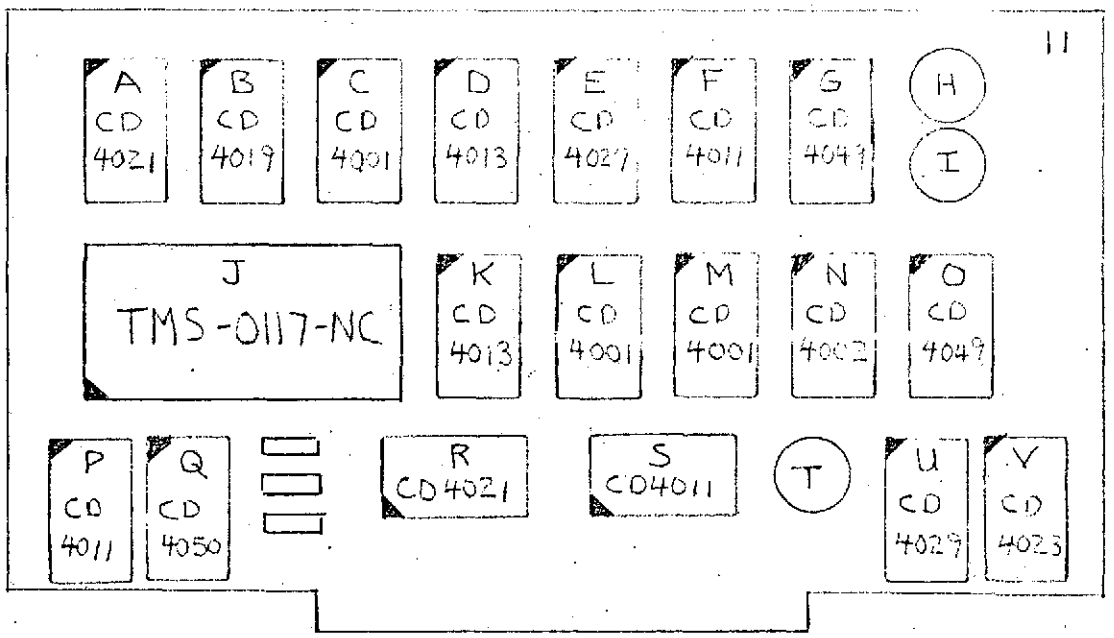
Note: Exact Placement of Network Components May Vary from Detail.

Figure 6-23. Layouts, Board Numbers 8 and 9



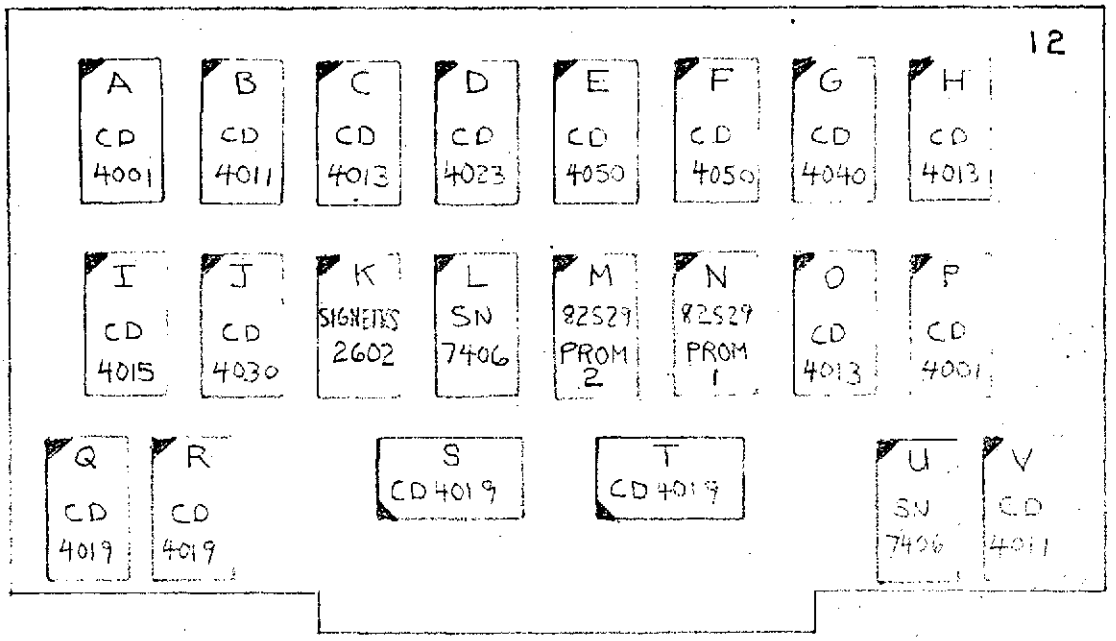
BOARD 10 - MISCELLANEOUS

NOTE: ORIENTATION OF LM710 NOT RECORDED - TAB SHOULD BE ALIGNED WITH CLOCKWISE EDGE OF [illegible] IN SOCKET

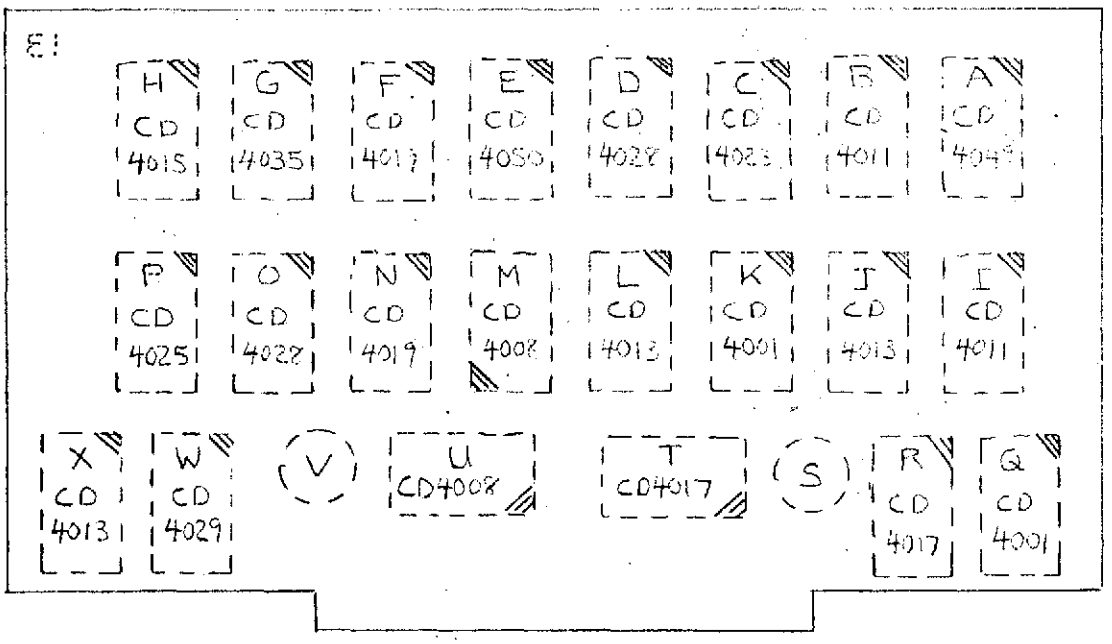


BOARD 11 - MICROPROCESSOR

Figure 6-24. Layouts, Board Numbers 10 and 11

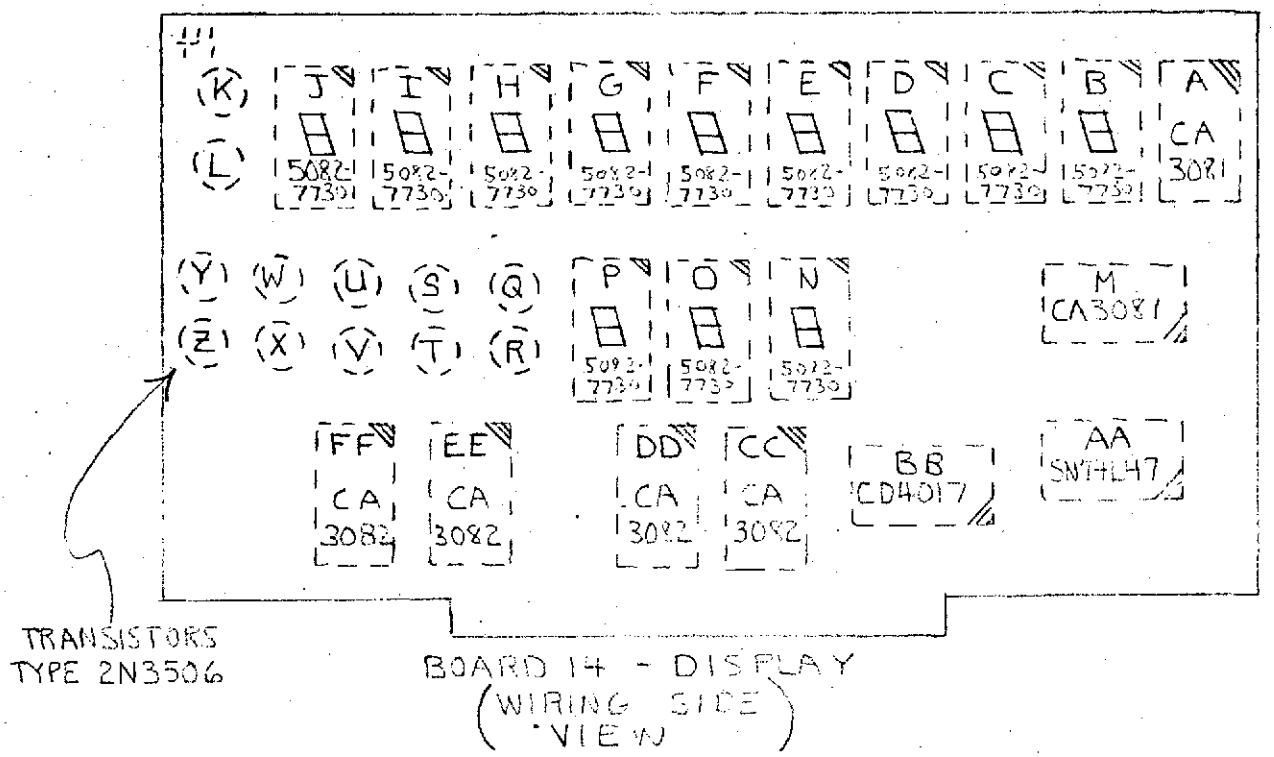


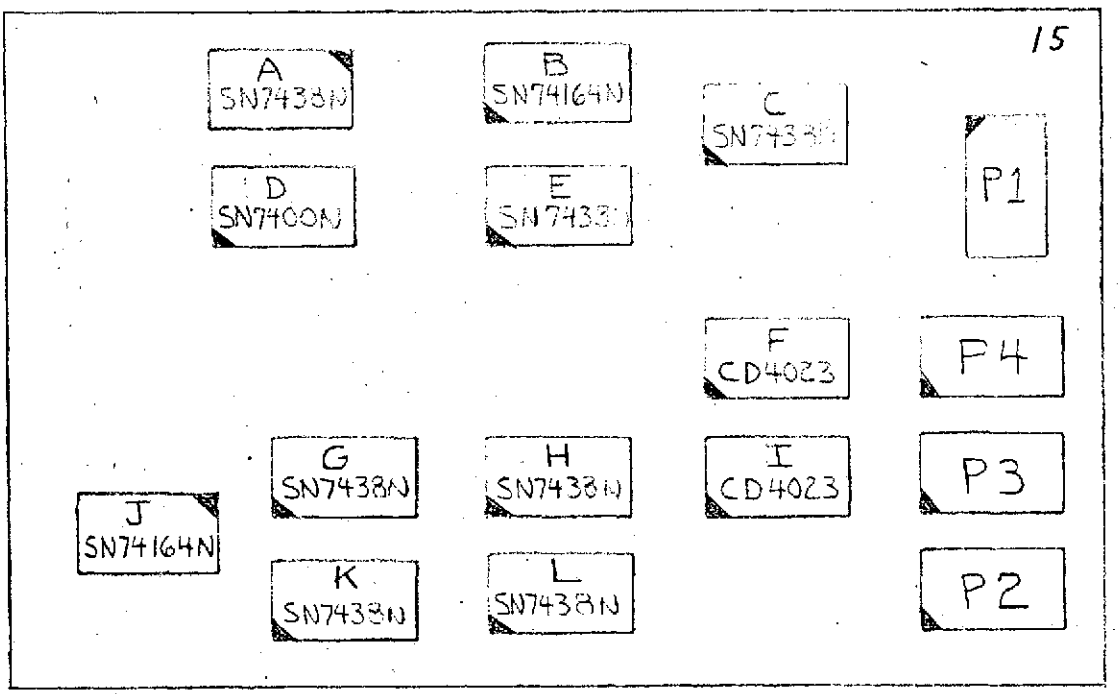
BOARD 12- MEMORY
(TOP VIEW)



BOARD 13 - DISPLAY CONTROL
(WIRING SIDE VIEW)

Figure 6-25. Layouts, Board Numbers 12 and 13





BOARD 15 - PANEL INDICATOR DRIVERS
(MOUNTED ON INSIDE SURFACE OF FRONT PANEL ABOVE DIGITAL NEST
TOP VIEW

Figure 6-26. Layouts, Board Numbers 14 and 15

ONE-WAY DOPPLER DIGITAL NEST WIRING

FOLDOUT FRAME 1

FOLDOUT FRAME 2

Figure 6-27. One-Way Doppler Digital Nest Wiring

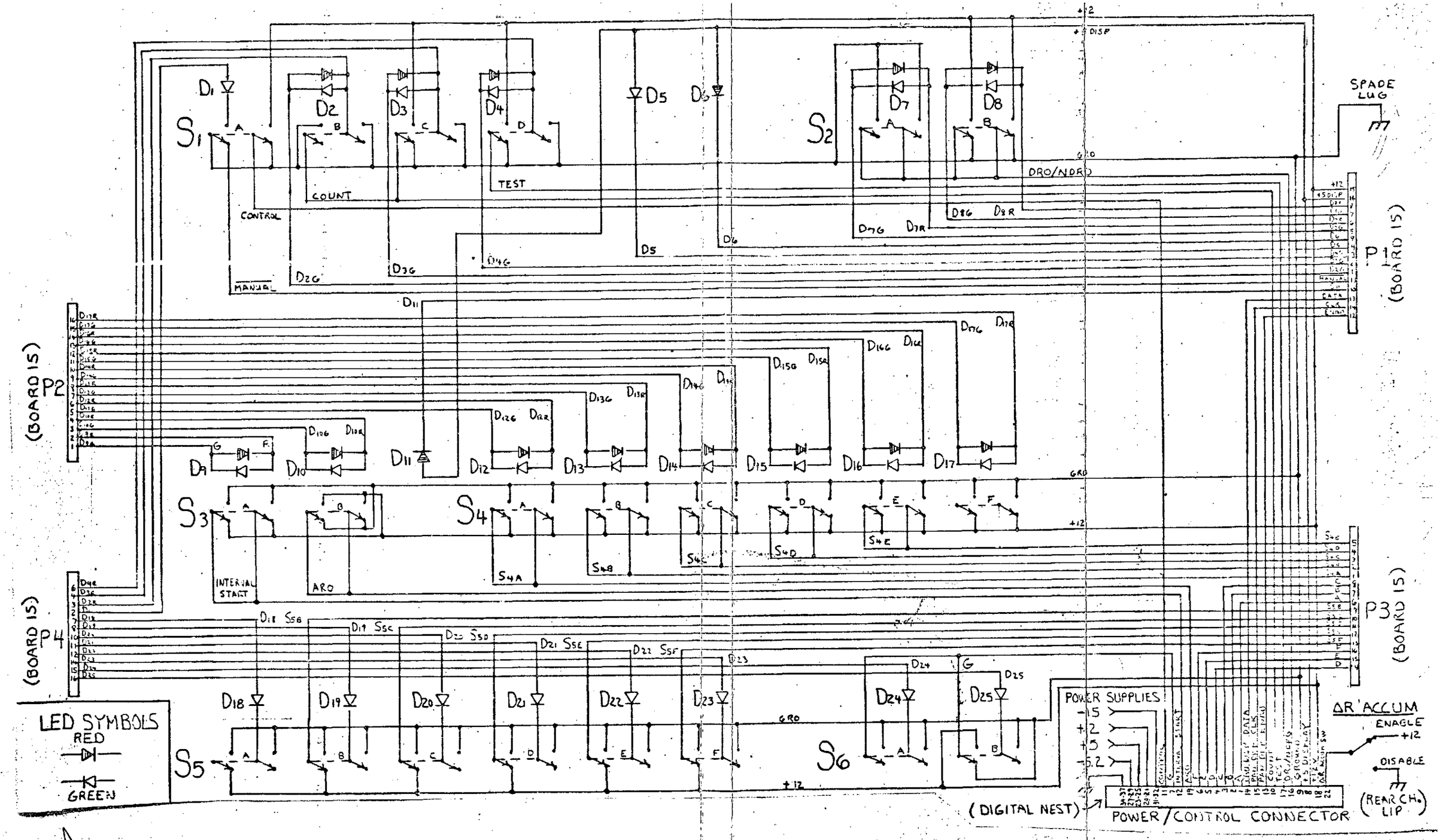


Figure 6-28. Front Panel Wiring

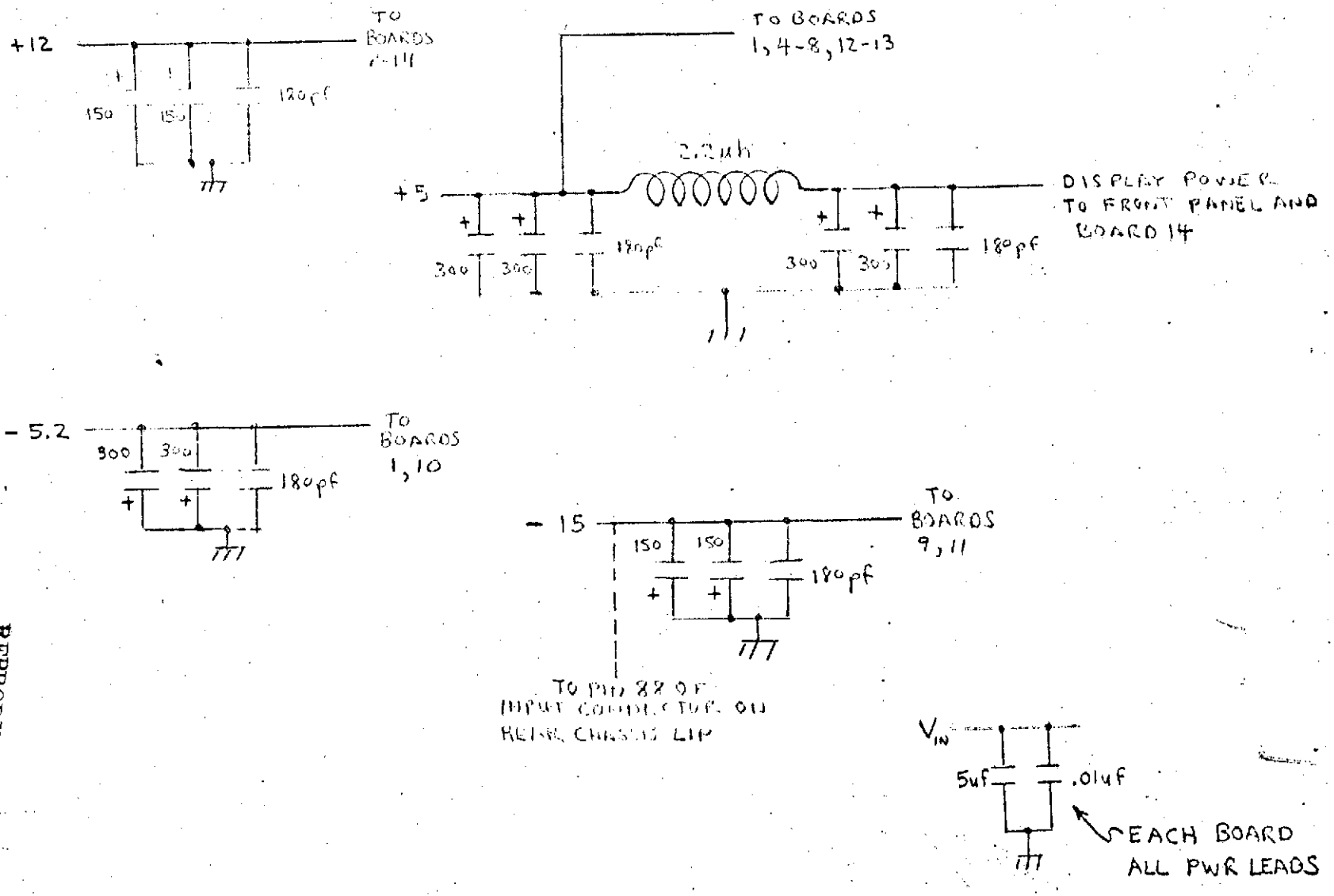


Figure 6-29. Power Wiring Detail

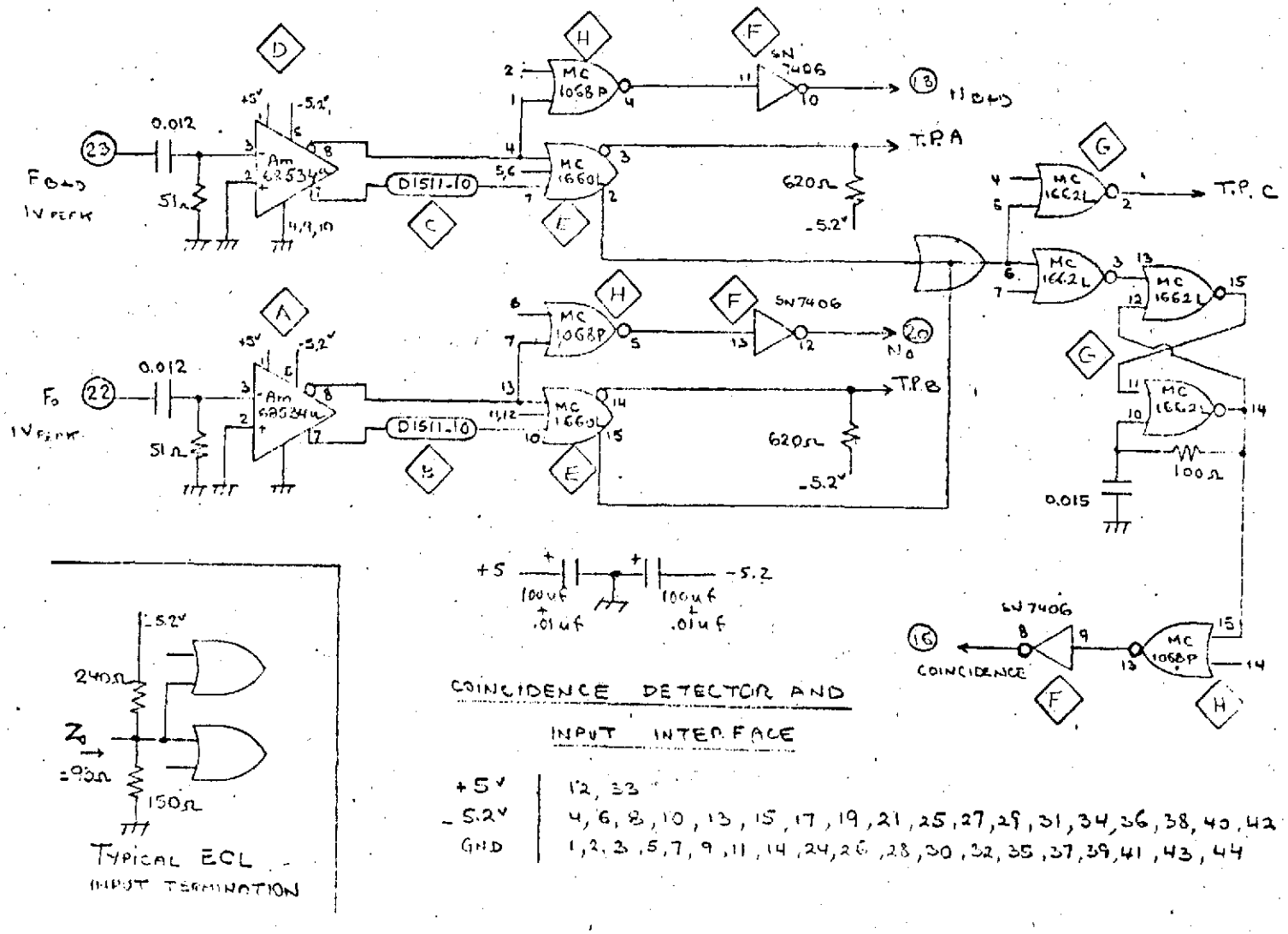


Figure 6-30. Schematic, Board 1, Coincidence Detector

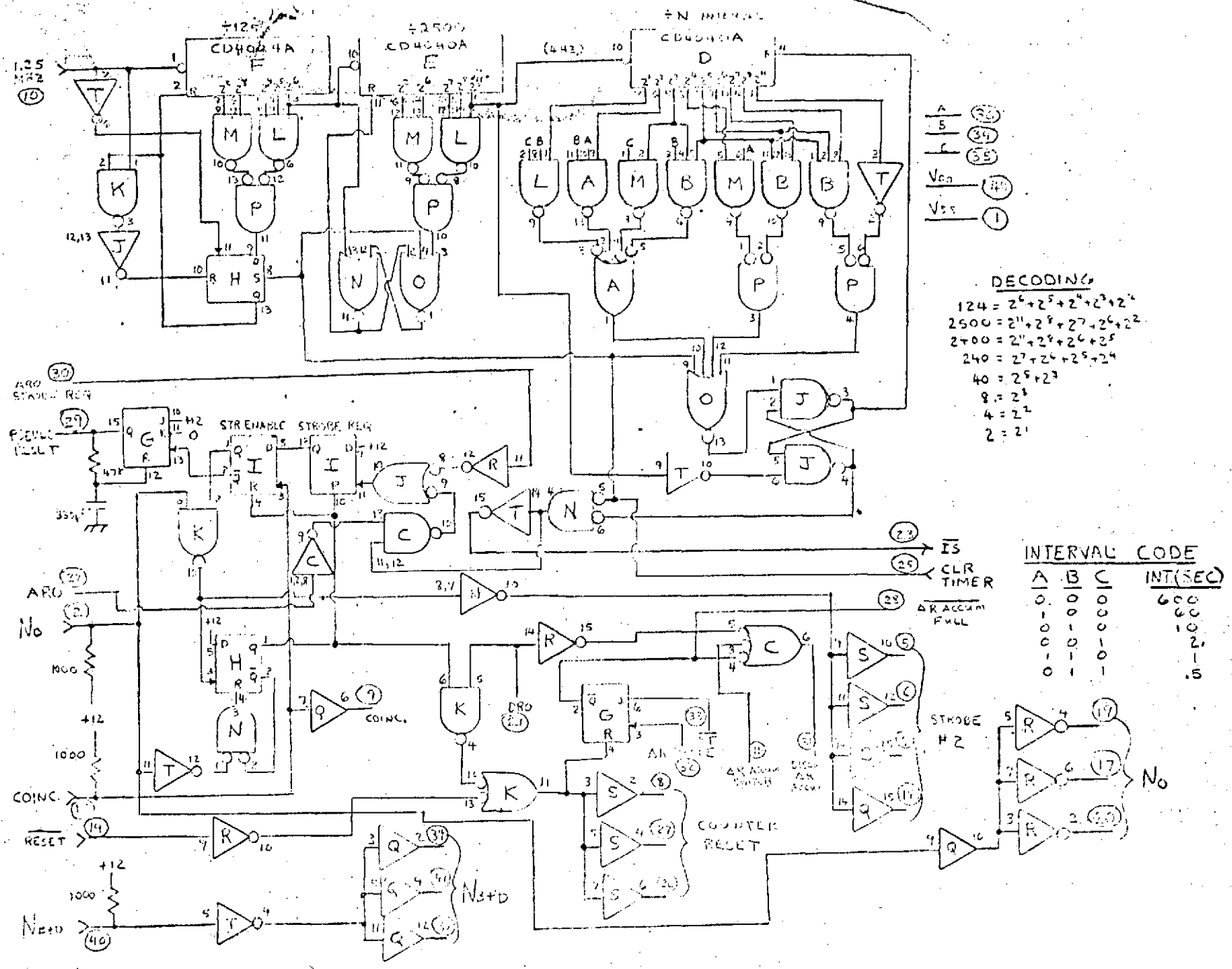


Figure 6-31. Schematic, Board 2, Interval Timer

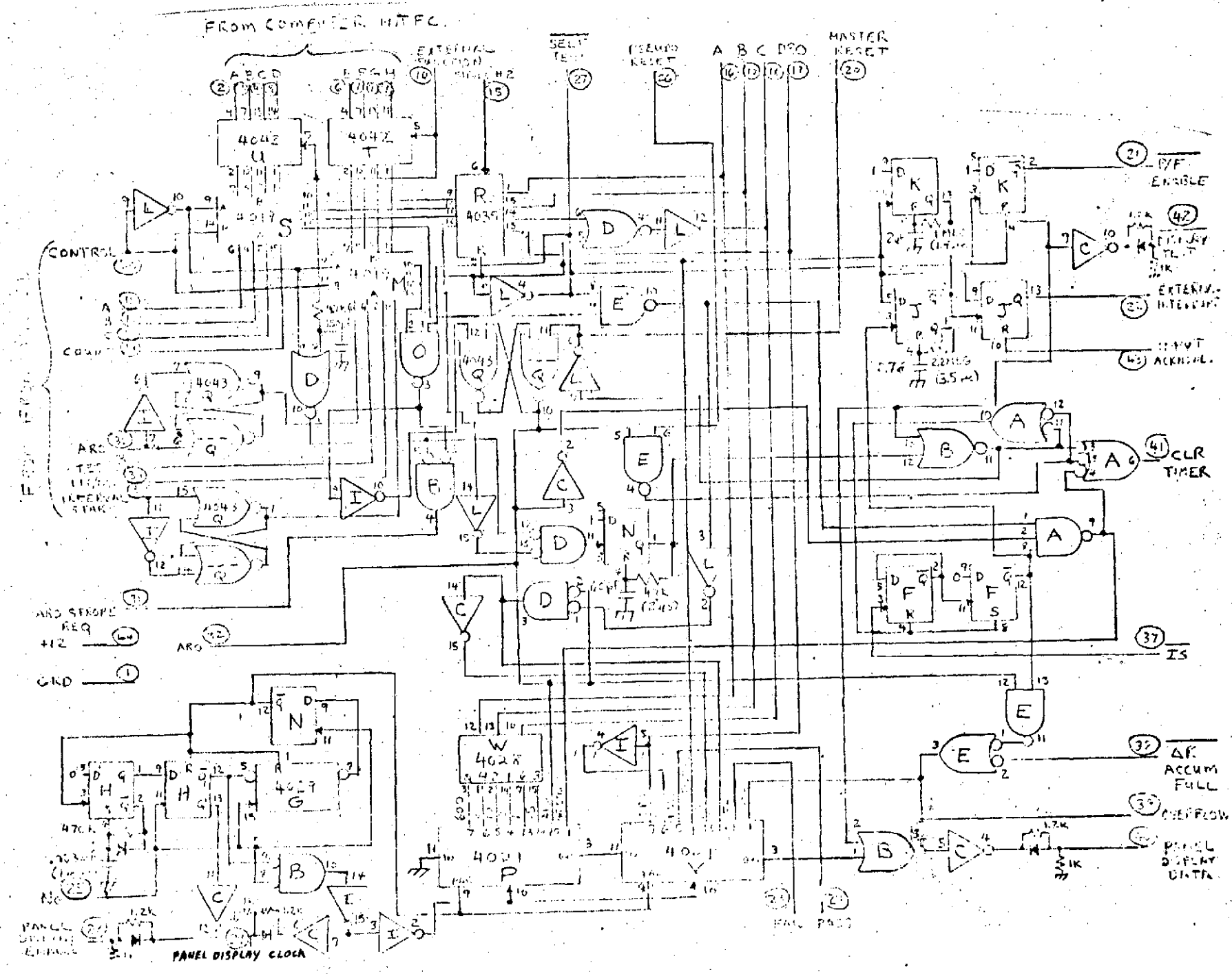


Figure 6-32. Schematics, Board 3, Mode Control

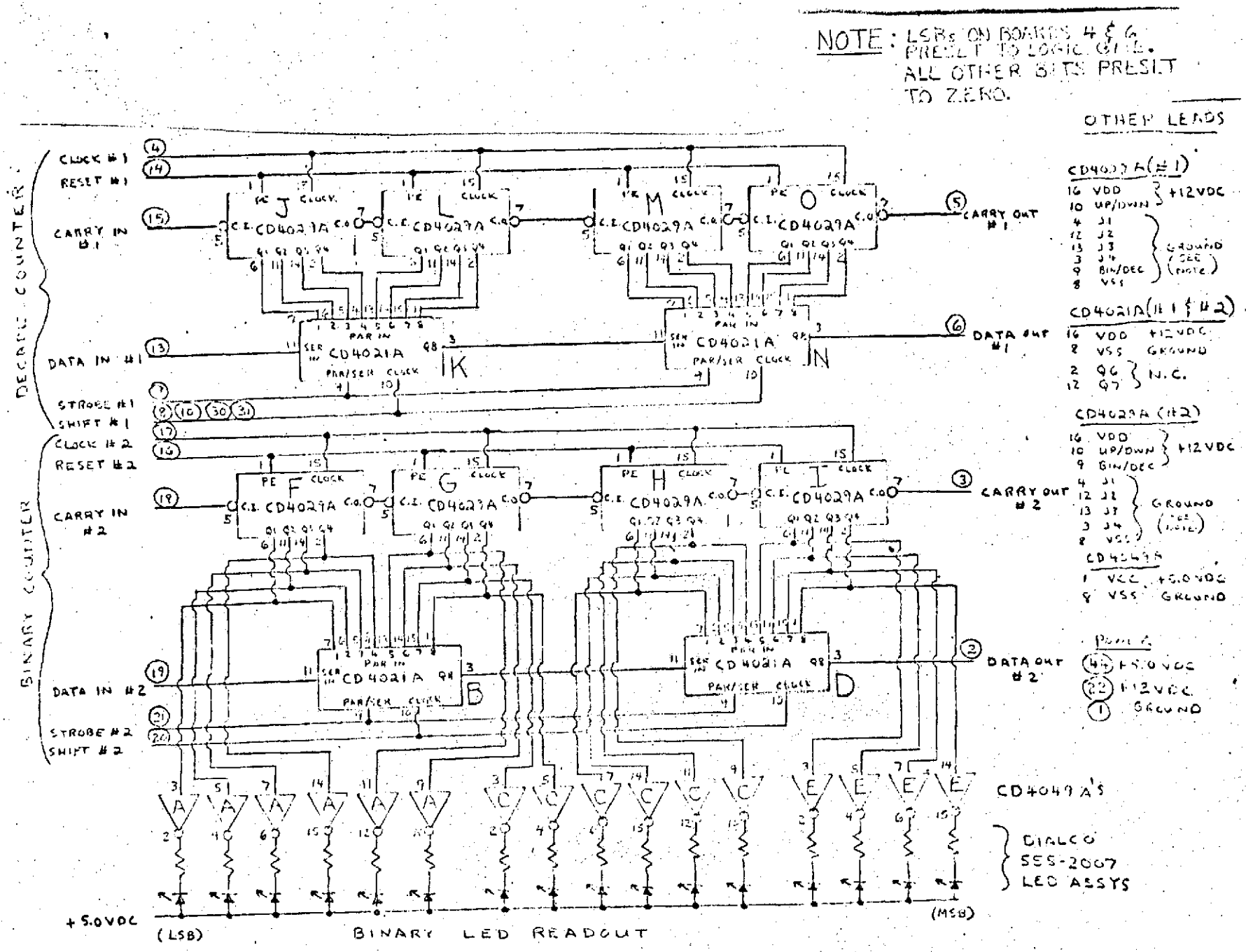


Figure 6-33. Schematics, Boards 4, 5, 6, 7, One-Way Doppler Counter/Latch Boards

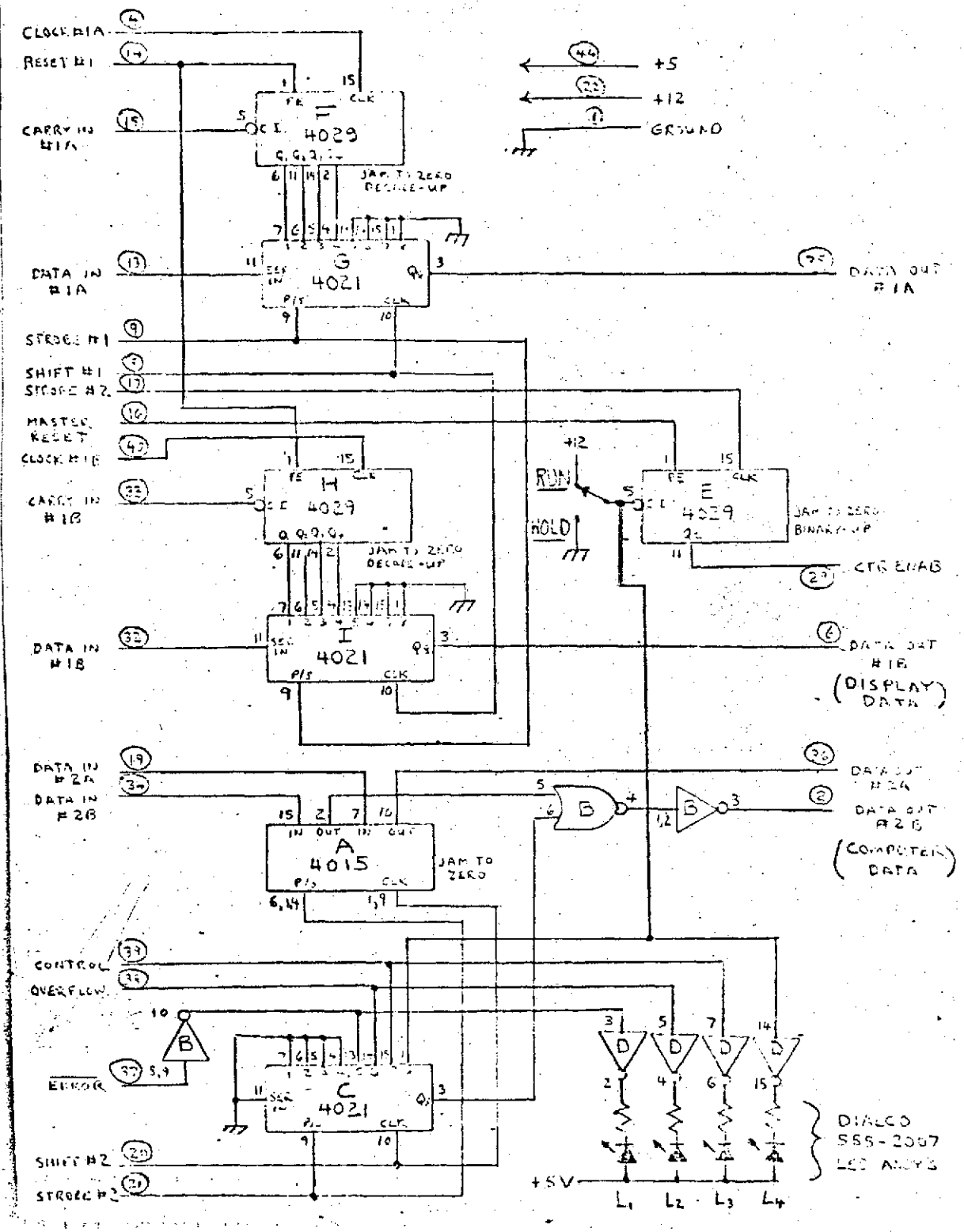


Figure 6-34. Schematics, Board 8, Miscellaneous Circuits

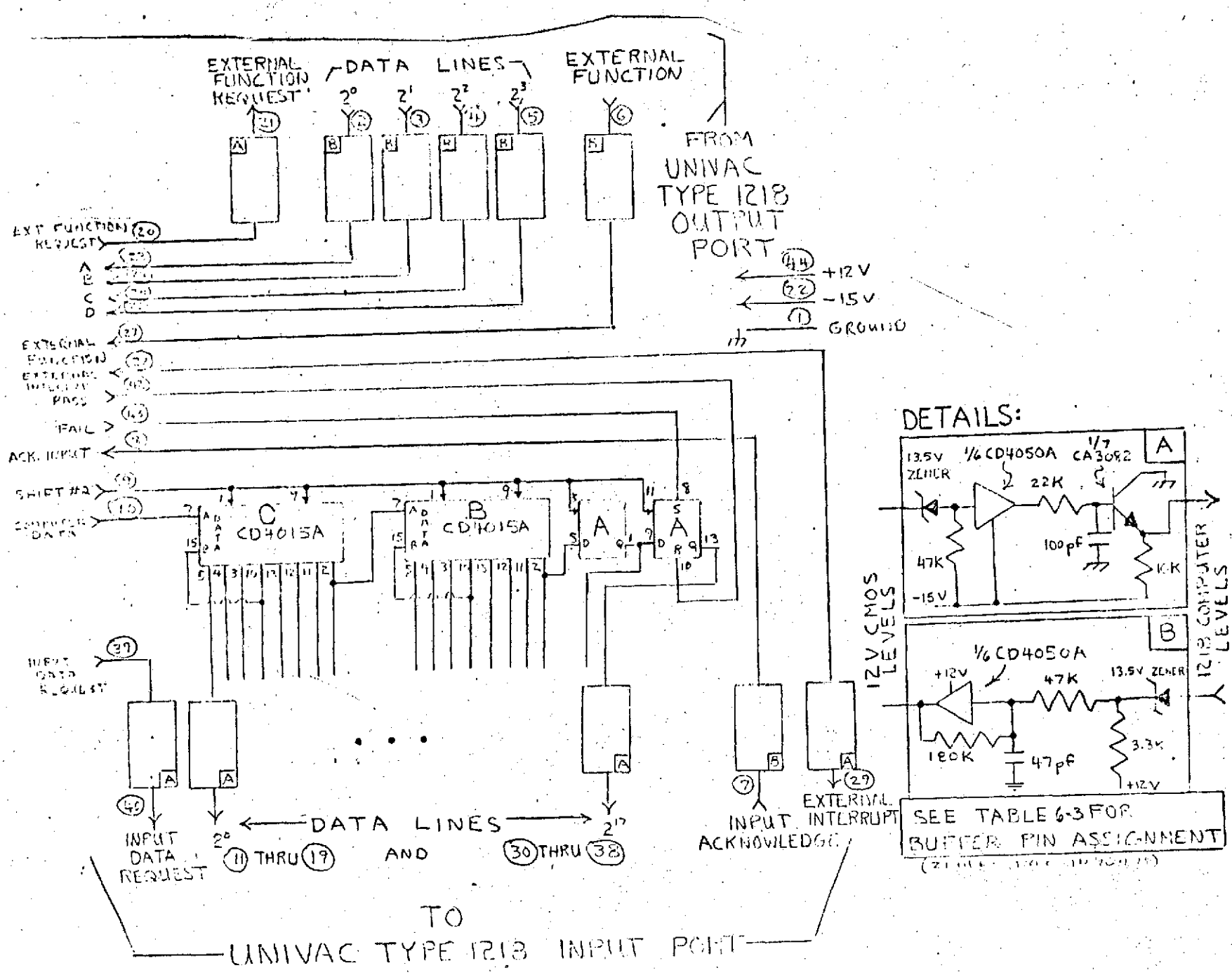


Figure 6-35. Schematics, Board 9, Computer Interface

TABLE 6-3. COMPUTER INTERFACE CONNECTIONS

DESIGNATION 1218 INPUT	COMPUTER CONNECTOR PIN	DIGITAL NEST CONNECTOR PIN	BOARD CONNECTOR PIN	BUFFER (INPUT/OUTPUT)	DRIVER (INPUT/OUTPUT)	NETWORK
INPUT REQUEST	1	19	9:40	K: 7/6	J:16/1	*
INPUT ACKNOWLEDGE	2	20	7	G:14/15	---	N_9
EXTERNAL INTERRUPT	3	30	29	K: 5/4	J:13/14	*
2^0	9	18	11	F: 7/6	J:11/12	N_{22}
2^1	10	17	12	F: 9/10	J: 8/7	N_{18}
2^2	22	16	13	F:11/12	J: 6/4	N_{17}
2^3	23	15	14	F:14/15	J: 3/2	N_5
2^4	24	14	15	F: 3/2	J:10/9	N_6
2^5	25	13	16	F: 5/4	I:13/14	N_{15}
2^6	26	12	17	E: 9/10	I:16/1	N_{16}
2^7	27	11	18	E:14/15	I:10/9	N_3
2^8	28	10	19	E:11/12	I:11/12	N_4
2^9	29	9	30	E: 7/6	I: 8/7	N_{21}
2^{10}	30	8	31	E: 5/4	I: 6/4	N_{14}
2^{11}	31	7	32	E: 3/2	I: 3/2	N_{13}
2^{12}	32	6	33	D:11/12	H:11/12	N_{19}
2^{13}	47	5	34	D: 9/10	H: 8/7	N_{20}
2^{14}	48	4	35	D: 7/6	H: 6/4	N_{12}
2^{15}	49	3	36	D: 5/4	H: 3/2	N_{11}
2^{16}	50	2	37	D:14/15	H:13/14	N_2
2^{17}	51	1	38	D: 3/2	H:16/1	N_1

TABLE 6-3. COMPUTER INTERFACE CONNECTIONS (Cont'd)

DESIGNATION	COMPUTER CONNECTOR PIN	DIGITAL NEST CONNECTOR PIN	BOARD CONNECTOR PIN	BUFFER (INPUT/OUTPUT)	DRIVER (INPUT/OUTPUT)	NETWORK
-15 VDC	88	Wired Directly to Power Supply				
Returns	11-13,19-20 33-43,58-62	32-37	Wired to Ground at Digital Nest Input			
Shield	45,69	Grounded at Computer Connector				
1218 OUTPUT						
Ext. Function	3	25	9:6	G:11/12	-----	N_{10}
Ext. Function Req.	4	26	21	K: 3/2	H:10/9	*
2^0	9	24	2	G: 3/2	-----	N_7
2^1	10	23	3	G: 5/4	-----	N_8
2^2	22	22	4	G: 7/6	-----	N_{24}
2^3	23	21	5	G: 9/10	-----	N_{23}
2^4	24	27	10:40	I:11/12	-----	+
2^5	25	28	41	I: 9/10	-----	+
2^6	26	29	42	I: 7/6	-----	+
2^7	27	31	43	I: 5/4	-----	+
Returns	13-14,19-20 33-38	32-37	Wired to Ground at Digital Nest Input			
Shield	45,69	Grounded at Computer Connector				

* Network Components Wired Point-to-Point on Wiring Side of Board

+ Network Assignment Not Documented for Board 10.

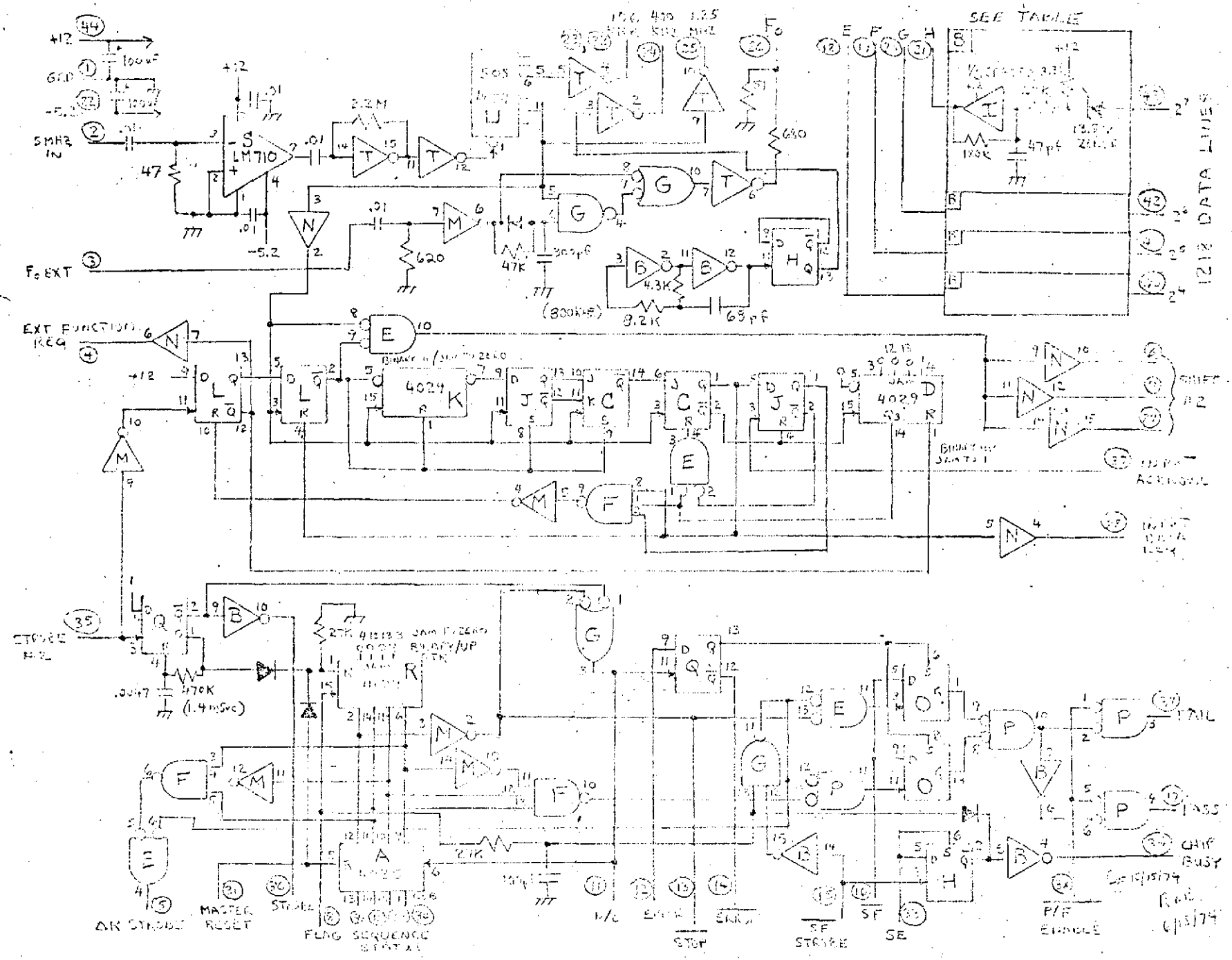


Figure 6-36. Schematics, Board 10, Miscellaneous

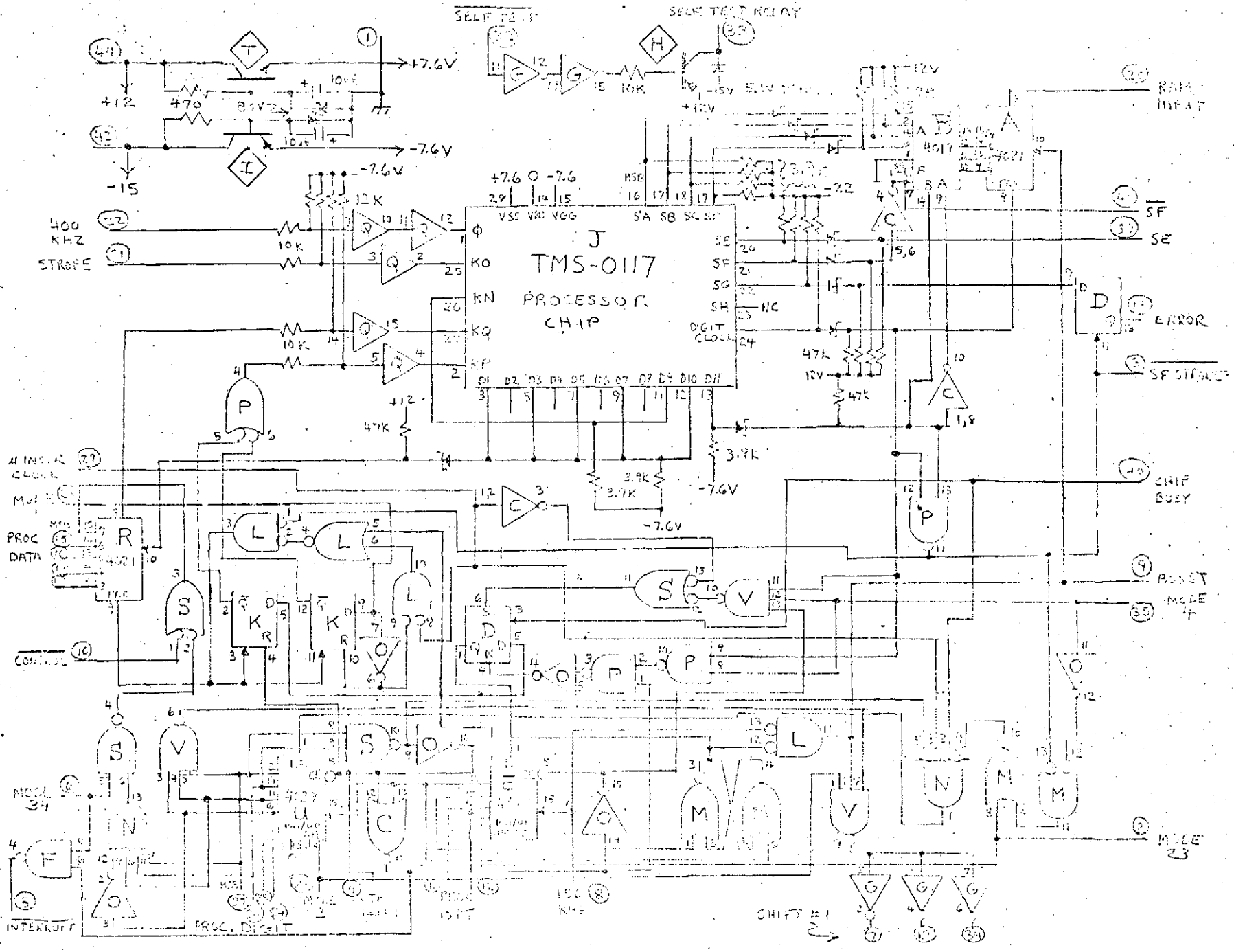


Figure 6-37. Schematics, Board 11, Microprocessor

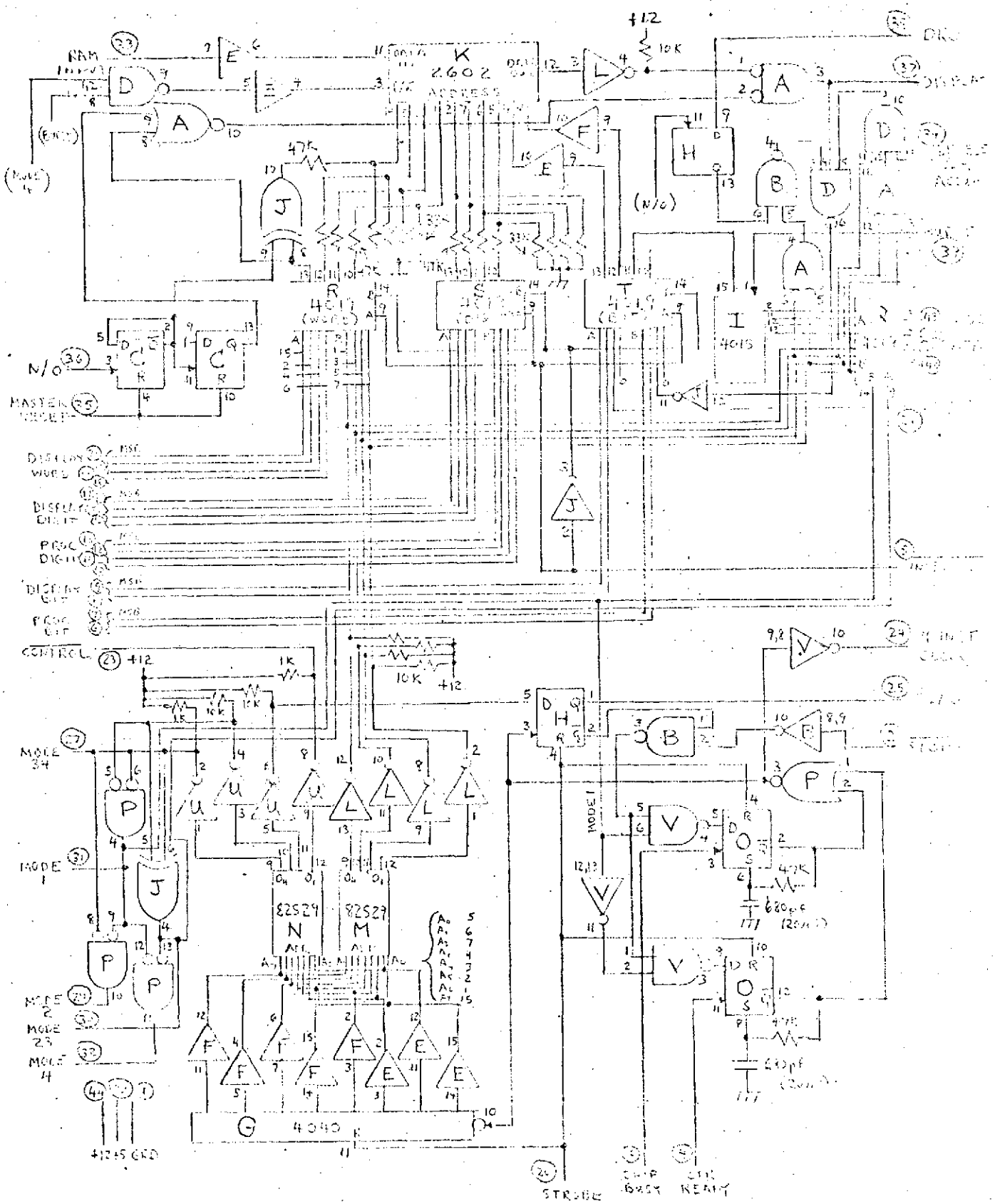


Figure 6-38, Board 12, Memory

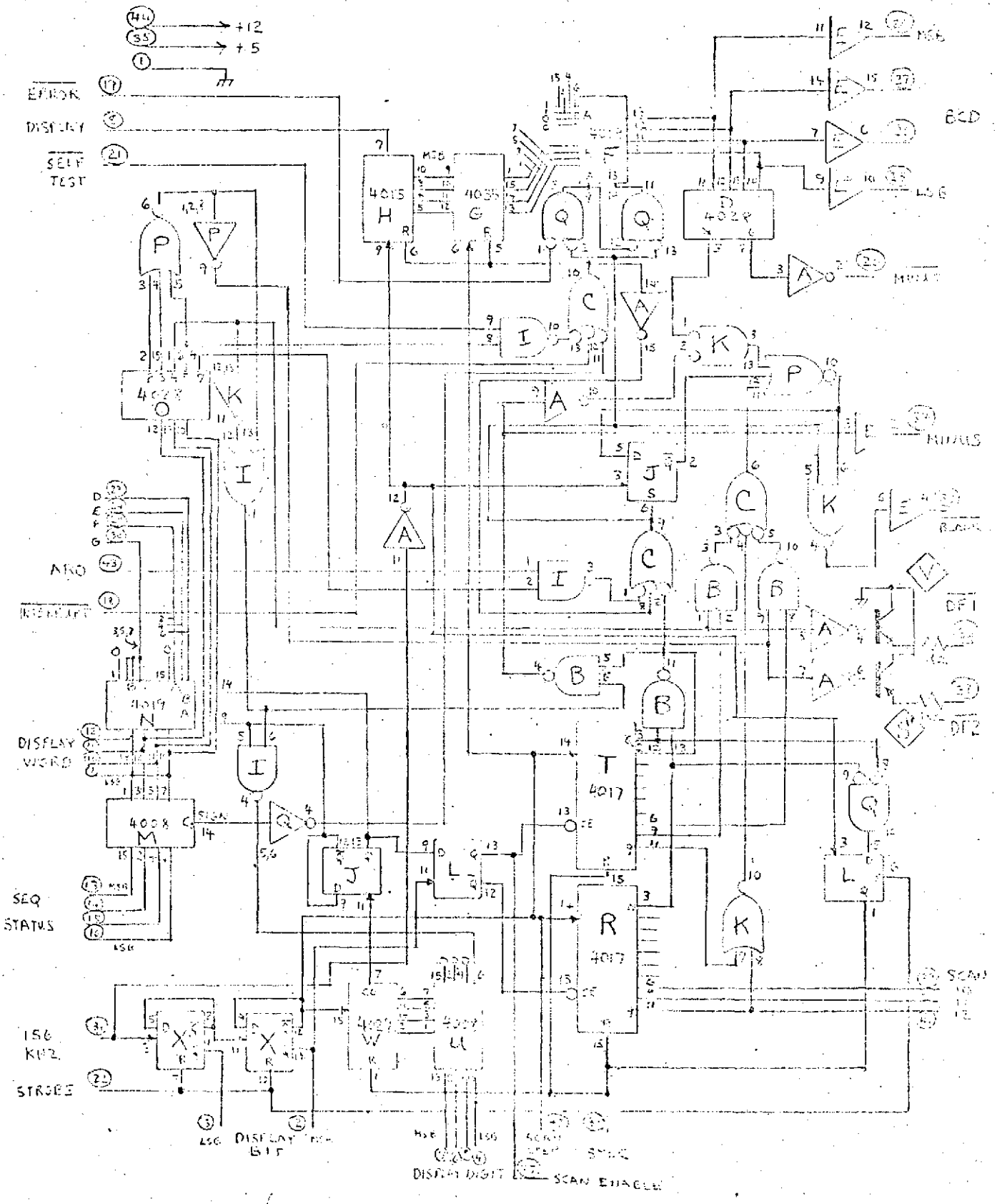


Figure 6-39. Schematic, Board 13, Display Control

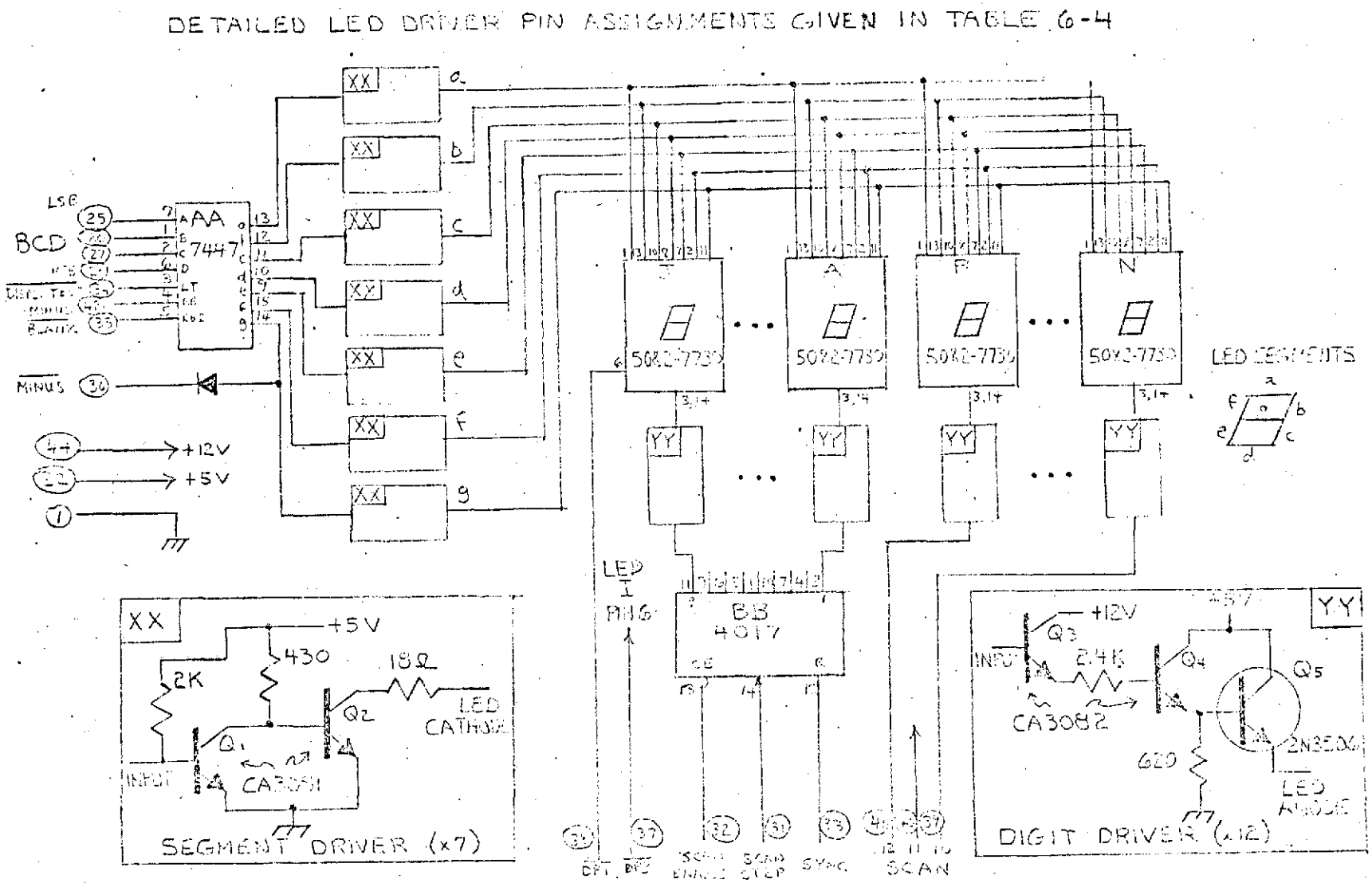


Figure 6-40. Schematic, Board 14, Display

TABLE 6-4

LED DRIVER PIN ASSIGNMENTS

BOARD 14

SEGMENT DRIVERS

SEGMENT	Q_1 (B/C)	Q_2 (B/C)	LED CATHODE
a	A: 13/14	M: 13/14	B-J, N-P : 1
b	11/12	11/12	13
c	6/4	6/4	10
d	3/2	3/2	8
e	16/1	16/1	7
f	10/9	10/9	2
g	8/7	8/7	11

DIGIT DRIVERS

DIGIT	Q_3 (B/E)	Q_4 (B/E)	Q_5	LED ANODE
DISPLAY A:MSD	DD: 16/12	FF: 11/12	S	B: 3, 14
	6/4	6/4	V	C
	10/9	10/9	U	D
	CC: 16/1	EE: 16/1	X	E
	3/2	3/2	W	F
	13/14	13/4	Z	G
	11/12	11/12	Y	H
	6/4	6/4	L	I
	10/9	10/9	K	J
DISPLAY B:MSD	DD: 16/1	FF: 16/1	R	N
	3/2	3/2	Q	O
	13/14	13/14	T	P

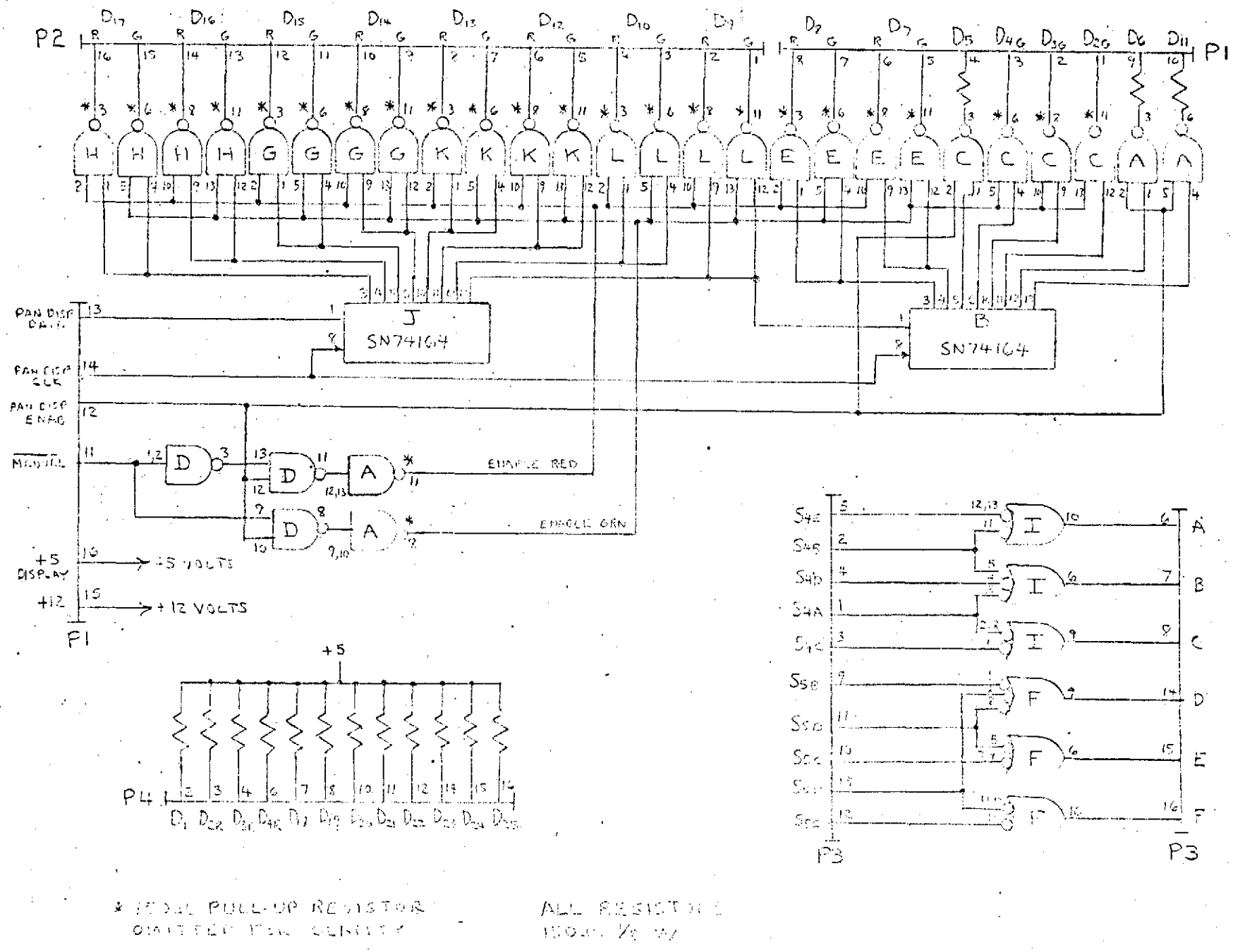
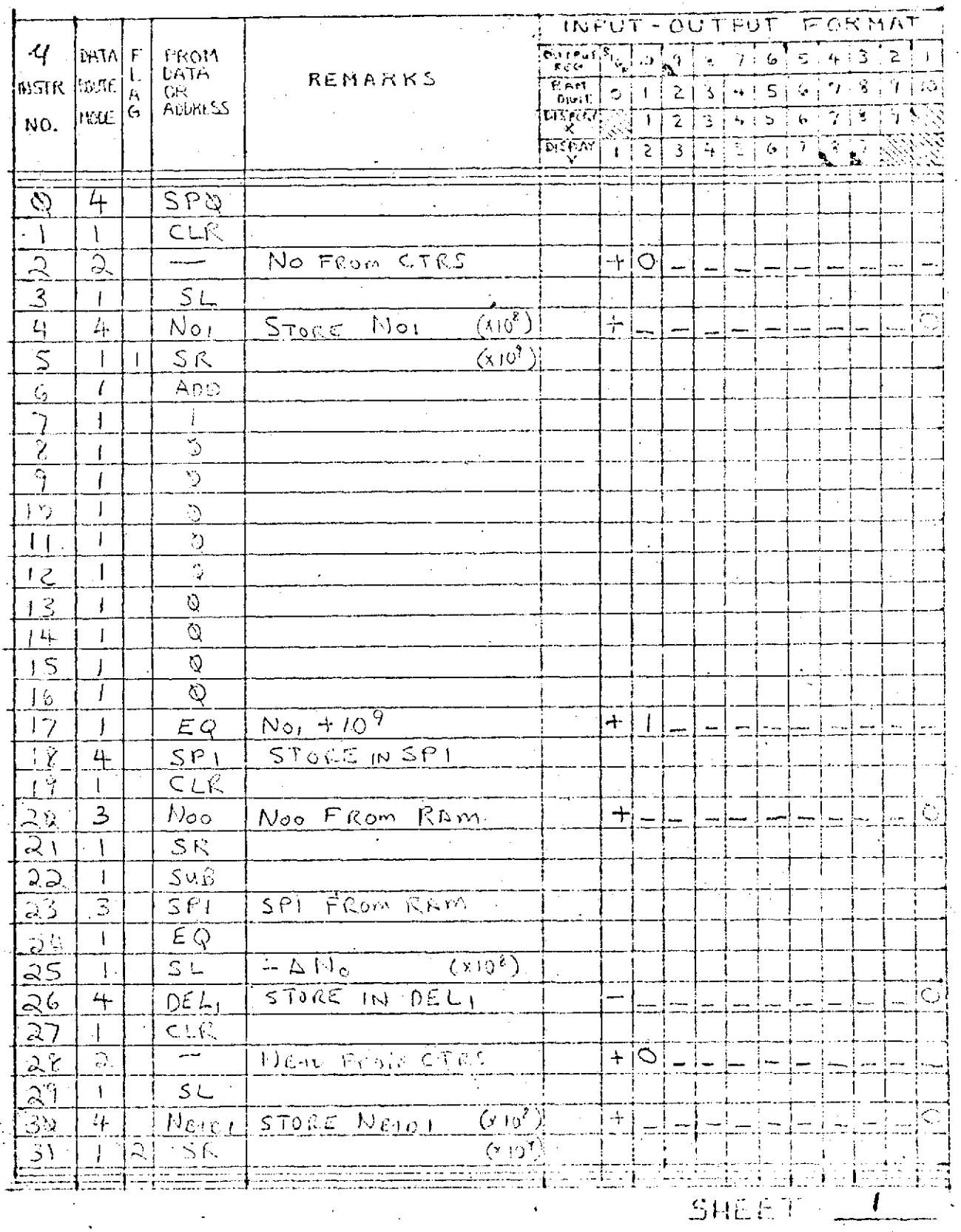


Figure 6-41. Schematics, Board 15, Panel Indicator Drivers



4 INSTR NO.	DATA ROUTE MODE	FLAG	FROM DATA OR ADDRESS	REMARKS	INPUT-OUTPUT FORMAT
0	4		SP0		
1	1		CLR		
2	2		—	No FROM CTRS	+ 0 — — — — — — — —
3	1		SL		
4	4		No1	STORE No1 ($\times 10^8$)	+ — — — — — — — — — 0
5	1	1	SR	($\times 10^9$)	
6	1		ADD		
7	1		1		
8	1		3		
9	1		5		
10	1		0		
11	1		3		
12	1		2		
13	1		0		
14	1		0		
15	1		0		
16	1		0		
17	1		EQ	No1 $+10^9$	+ 1 — — — — — — — —
18	4		SP1	STORE IN SP1	
19	1		CLR		
20	3		Noo	Noo FROM RAM	+ — — — — — — — — — 0
21	1		SR		
22	1		SUB		
23	3		SP1	SP1 FROM RAM	
24	1		EQ		
25	1		SL	$\div \Delta$ No ($\times 10^8$)	
26	4		DEL1	STORE IN DEL1	— — — — — — — — — — 0
27	1		CLR		
28	2		—	DEM FROM CTRS	+ 0 — — — — — — — —
29	1		SL		
30	4		Ne1e1	STORE Ne1o1 ($\times 10^9$)	+ — — — — — — — — — 0
31	1	2	SR	($\times 10^1$)	

SHEET 1

Figure 6-42. MICRO-PROGRAM Coding Sheet

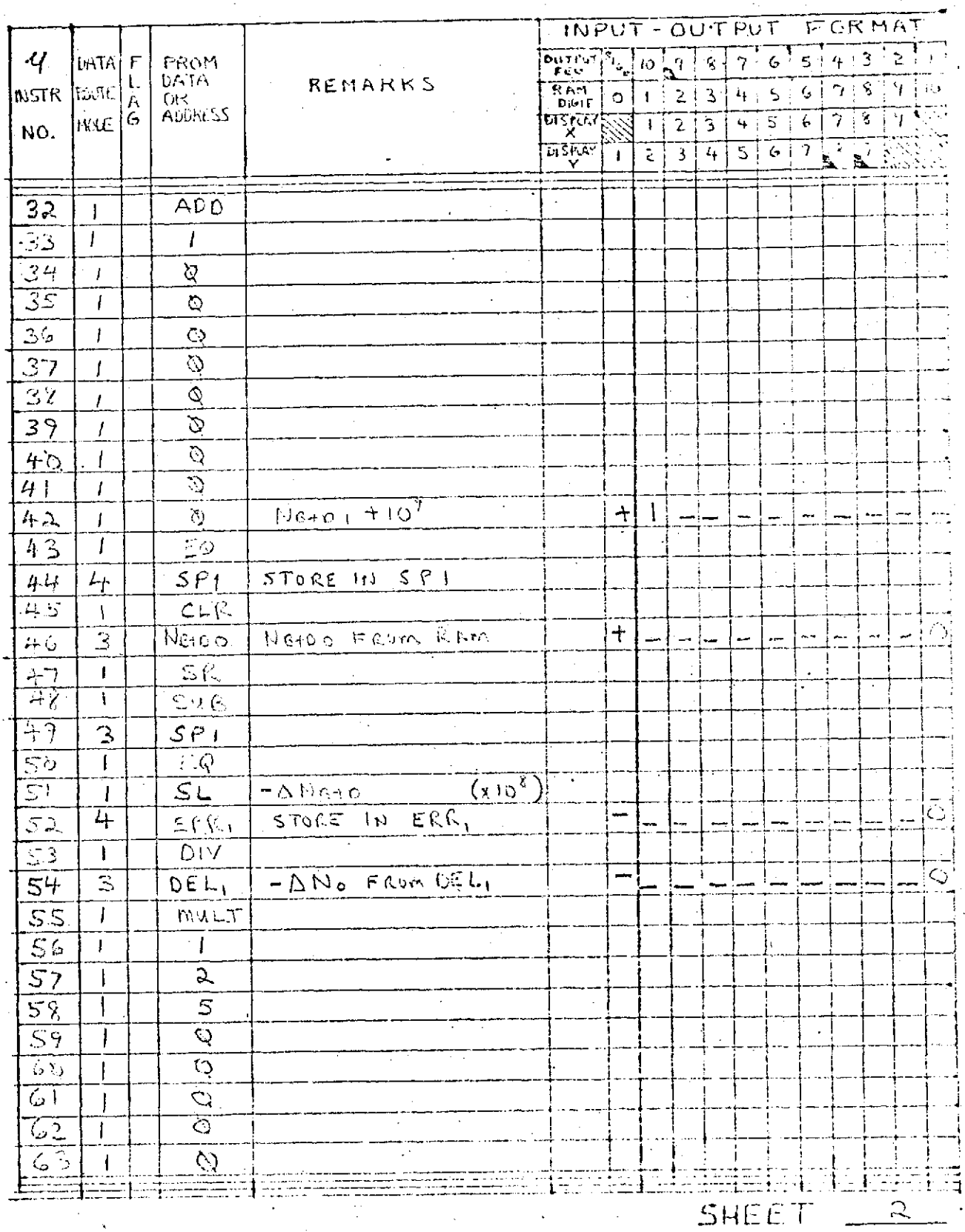
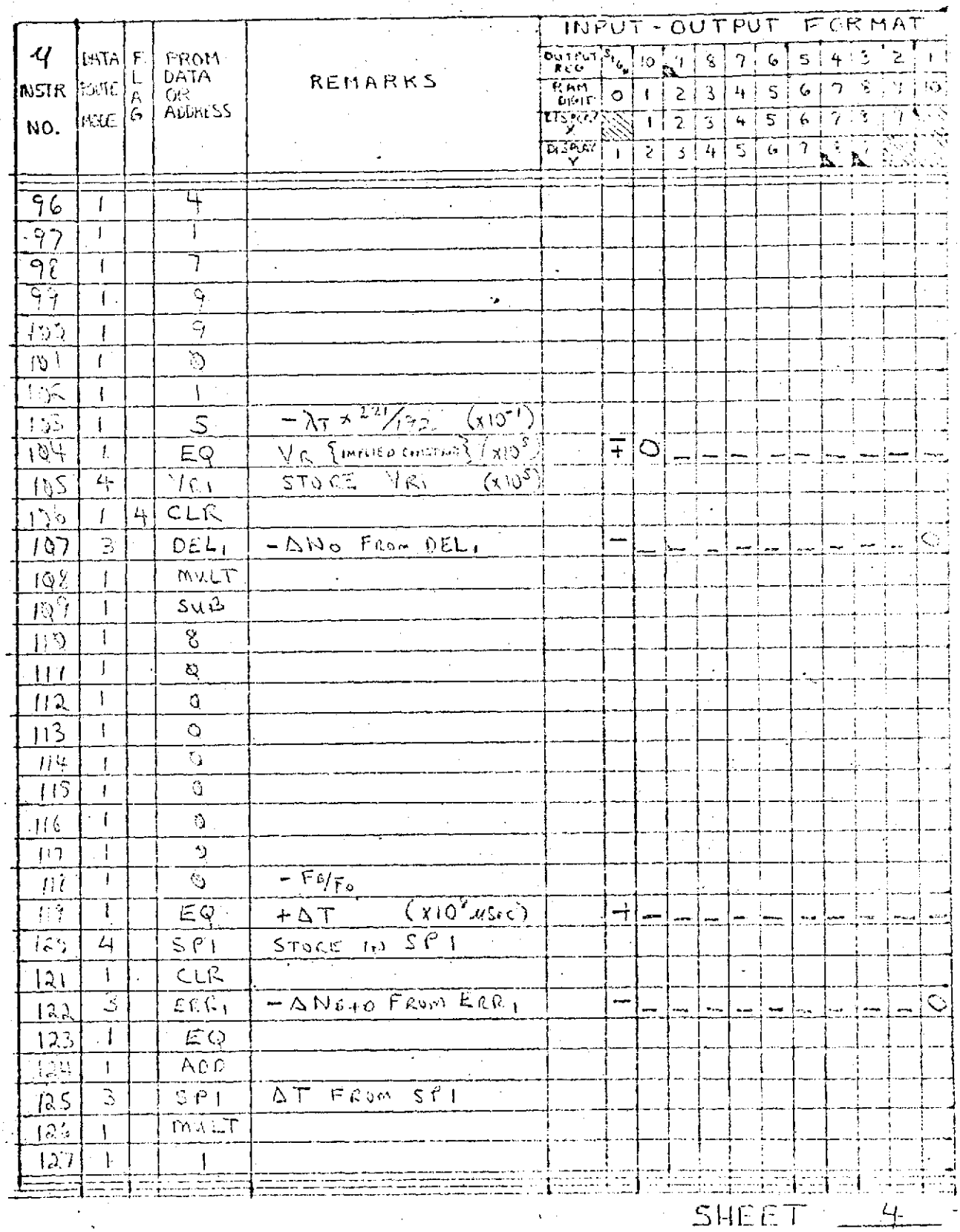


Figure 6-43. MICRO-PROGRAM Coding Sheet

4 INSTR NO.	DATA SOURCE MODE	F L A G	FROM DATA OR ADDRESS	REMARKS	INPUT-OUTPUT FORMAT
					OUTPUT REG: S 10 9 8 7 6 5 4 3 2 1
					RAM DIGIT: 0 1 2 3 4 5 6 7 8 9 10
					DISPLAY X: 1 2 3 4 5 6 7 8 9
					DISPLAY Y: 1 2 3 4 5 6 7 8 9
64	1		0		
65	1		1		
66	1		EXO		
67	1		SUB		
68	1		1		
69	1		0		
70	1		0		
71	1		0		
72	1		0		
73	1		0		
74	1		0		
75	1		0		
76	1		0		
77	1		0	$\left(\frac{\Delta \text{freq}}{\text{freq}}\right) \cdot F_0 - F_6) \times 10^6$	
78	1		MULT		
79	1		1		
80	1		1		
81	1		5		
82	1		1		
83	1		0		
84	1		4		
85	1		1		
86	1		6		
87	1		6		
88	1		7	221/192	
89	1		EXO		
90	1		EQ	F_0 $(\times 10^6)$	
91	1		SL	$(\times 10^5)$	
92	4		F_{01}	STORE F_{01} $(\times 10^5)$	I - - - - - - - - - 0
93	1	3	SUB		
94	1		1		
95	1		6		

SHEET 3

Figure 6-44. MICRO-PROGRAM Coding Sheet



4 INSTR NO.	DATA ROUTE MODE	FLAG	FROM DATA OR ADDRESS	REMARKS	INPUT-OUTPUT FORMAT
96	1		4		
97	1		1		
98	1		7		
99	1		9		
100	1		9		
101	1		0		
102	1		1		
103	1		5	$-\lambda_T * 221/192$ (x10⁻¹)	
104	1		EQ	V_R {IMPLIED CONSTANT} (x10⁵)	∓ 0
105	4		YR1	STORE Y_{R1} (x10⁵)	
106	1	4	CLR		
107	3		DEL1	-ΔNo FROM DEL1	− 0
108	1		MULT		
109	1		SUB		
110	1		8		
111	1		8		
112	1		0		
113	1		0		
114	1		0		
115	1		0		
116	1		0		
117	1		0		
118	1		0	$-F_0/F_0$	
119	1		EQ	$+\Delta T$ (x10⁵ μsec)	+
120	4		SP1	STORE IN SP1	
121	1		CLR		
122	3		ERR1	-ΔN640 FROM ERR1	− 0
123	1		EQ		
124	1		ADD		
125	3		SP1	ΔT FROM SP1	
126	1		MULT		
127	1		1		

SHEET 4

Figure 6-45. MICRO-PROGRAM Coding Sheet

4 INSTR NO.	DATA ROUTE MODE	FLAG	FROM DATA OR ADDRESS	REMARKS	INPUT - OUTPUT FORMAT
					OUTPUT REG: S/C 10 9 8 7 6 5 4 3 2 1
					RAM DIGIT: 0 1 2 3 4 5 6 7 8 9 10
					DISPLAY X: 1 2 3 4 5 6 7 8 9
					DISPLAY Y: 1 2 3 4 5 6 7 8 9
128	1		6		
129	1		4		
130	1		1		
131	1		7		
132	1		9		
133	1		7		
134	1		5		
135	1		1		
136	1		6	$+\lambda T \times 2.21/192$ (x15')	
137	1		EXP		
138	1		EQ	ΔR (x10⁹ M)	± 0
139	1		SL	(x10⁶)	
140	4		DEL1	STORE IN DEL1	
141	1		CLR		
142	3		ΔR_0	ΔR_0 FROM RAM	± 0
143	1		EQ		
144	4		ERR1	STORE IN ERR1	
145	1		CLR		
146	1		ADD		
147	3		ERR1	ΔR_0 FROM ERR1	± 0
148	1		EQ		
149	3		DEL1	ΔR FROM DEL1	± 0
150	1		EQ		
151	4		ΔR_1	STORE ΔR_1 (x10⁶)	± 0
152	1		SR		
153	4		DEL1	STORE IN DEL1	± 0
154	1		MULT		
155	3		DEL1		
156	1		SUB		+ 0
157	1		1		
158	1		6		
159	1		0		

SHEET 5

Figure 6-46. MICRO-PROGRAM Coding Sheet

4 INSTR NO.	DATA ROUTE MODE	FLAG	PROM DATA OR ADDRESS	REMARKS	INPUT - OUTPUT FORMAT
					OUTPUT REG: S/N 10 9 8 7 6 5 4 3 2 1
					RAM UNIT: 0 1 2 3 4 5 6 7 8 9 10
					DISPLAY X: 1 2 3 4 5 6 7 8 9
					DISPLAY Y: 1 2 3 4 5 6 7 8 9
160	1		Q		
161	1		Q		
162	1		Q		
163	1		Q		
164	1		Q		
165	1		Q		
166	1		EQ	TEST FOR ΔR ACCUM FULL - OR IF NEG	
167	4	5	SPR	WRITE TO ACCUM PICK UP SIGN	
168	1		CLR		
169	3		F_{01}	F_{01} FROM RRM	± _ _ _ _ _ _ _ _ _ 0
170	1		EQ		
171	1		ADD		
172	1		3		
173	1		2		
174	1		8		
175	1		8		
176	1		6		
177	1		9		
178	1		Q		
179	1		4		
180	1		7		
181	1		7	$-F_{TEST} \times 221/192$	
182	1		EQ	TEST ERROR ($\times 10^5$)	
183	4		ERR_1-	STORE ERR_1 ($\times 10^5$)	± _ _ _ _ _ _ _ _ _ _
184	1		CLR		
185	3		F_{01}	F_{01} FROM RRM	± _ _ _ _ _ _ _ _ _ 0
186	1		EQ		
187	1		SR		
188	1		SR		
189	1		SR		
190	1		SL		
191	1		SL		

SHEET 6

Figure 6-47. MICRO-PROGRAM Coding Sheet

4 INSTR NO.	DATA MODE INDEX	FLAG	PROM DATA OR ADDRESS	REMARKS	INPUT - OUTPUT FORMAT
					OUTPUT REG: S 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
					RAM DIGIT: 0 1 2 3 4 5 6 7 8 9 10
					DISPLAY X: 1 2 3 4 5 6 7 8 9
					DISPLAY Y: 1 2 3 4 5 6 7 8 9
192	1		SL		± _ _ _ _ _ _ _ 0 0 0
193	1		ADD		
194	1		3		
195	1		2		
196	1		8		
197	1		8		
198	1		6		
199	1		9		
200	1		0		
201	1		4		
202	1		7		
203	1		7		
204	1		EQ		
205	4		DEL1	STORE TO DEL1	± _ _ _ _ _ _ _ 0 0 0
206	1		SL		
207	1		SL		
208	1		SL		
209	1		SL		
210	1		SL		
211	1		SR		
212	1		SR		± 0 0 _ _ A_5 A_2 A_1 0 0 0
213	1		MULT		
214	3		DEL1	ERROR FROM DEL1	± _ _ _ _ _ _ _ A_5 A_2 A_1
215	1		EXO		
216	1		SUB		
217	1		9	$(.3\ Hz)^2$ NO ROLES	
217	1		EQ	ERROR CHECK - PASS IF NEG.	± 0 X X X X X X X X X
219	4	6	SPQ	WRITE TO RAM W/ SIGN	
220	1		CLR		
221	3		DEL0	DEL0 FROM RAM	+ _ _ _ _ _ _ _ _ _ _
222	1		ADD		
223	3		SP1	ΔT FROM SP1	+ _ _ _ _ _ _ _ _ _ _

SHEET 7

Figure 6-48. MICRO-PROGRAM Coding Sheet

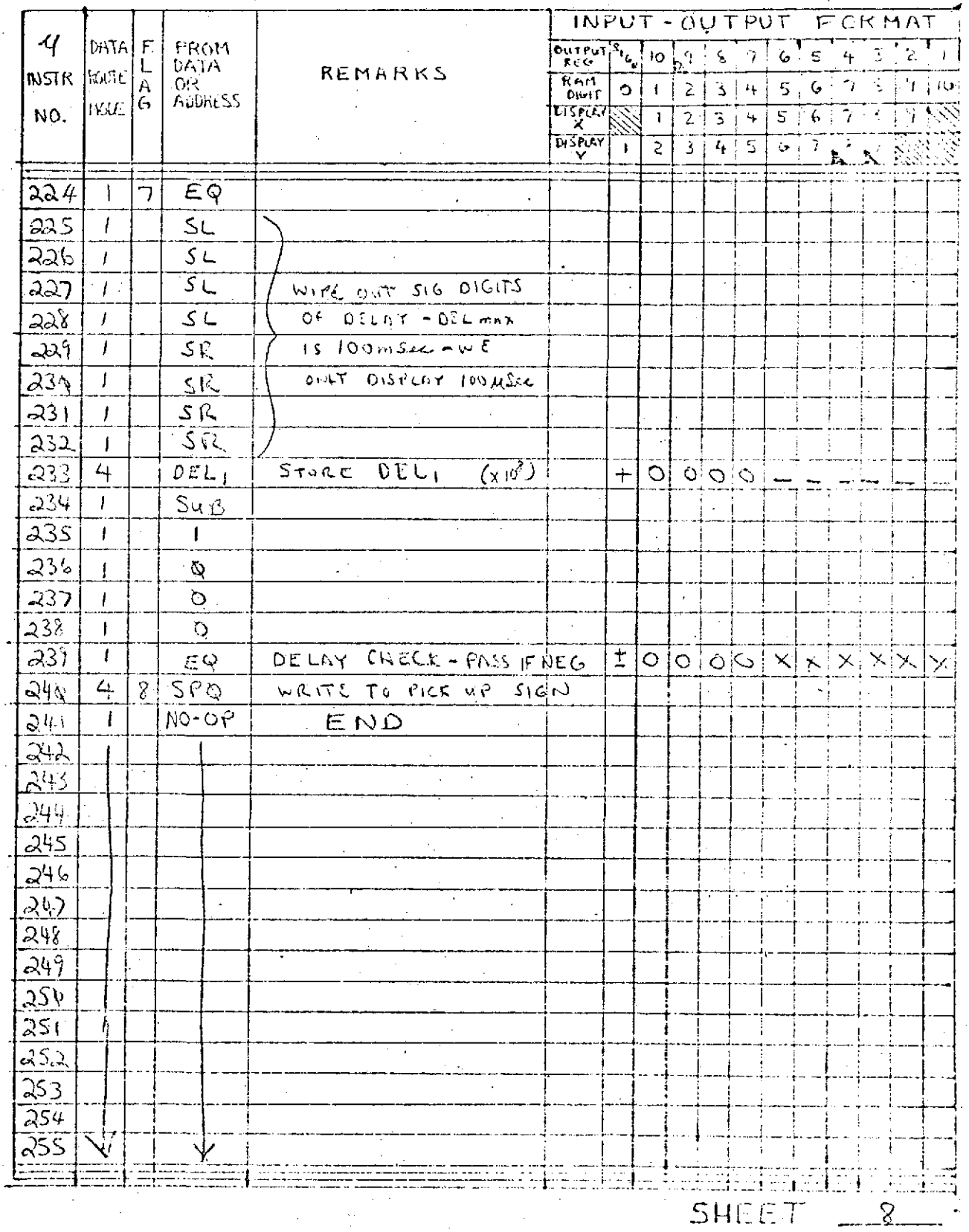


Figure 6-49. MICRO-PROGRAM Coding Sheet

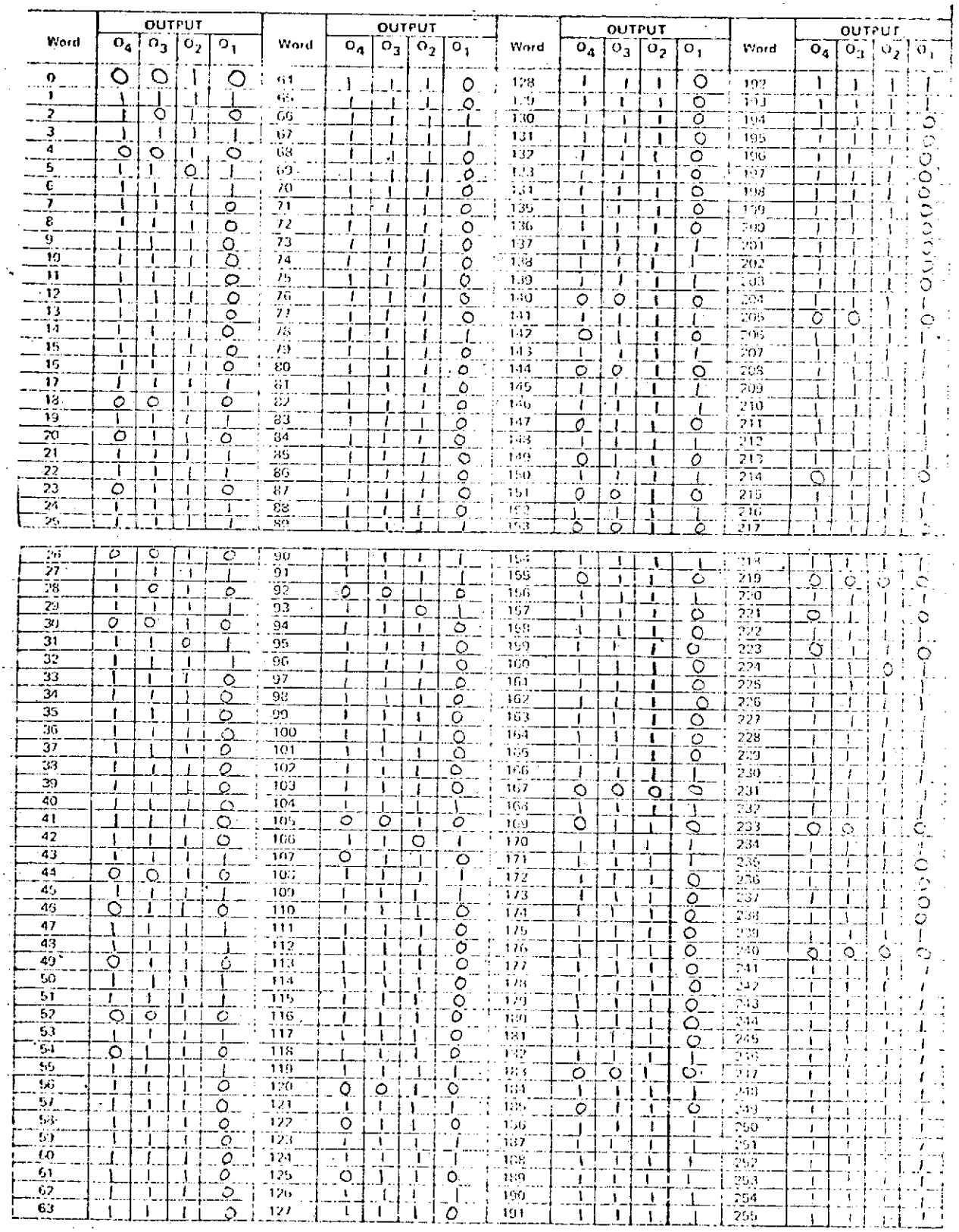


Figure 6-50. PROM Instructions

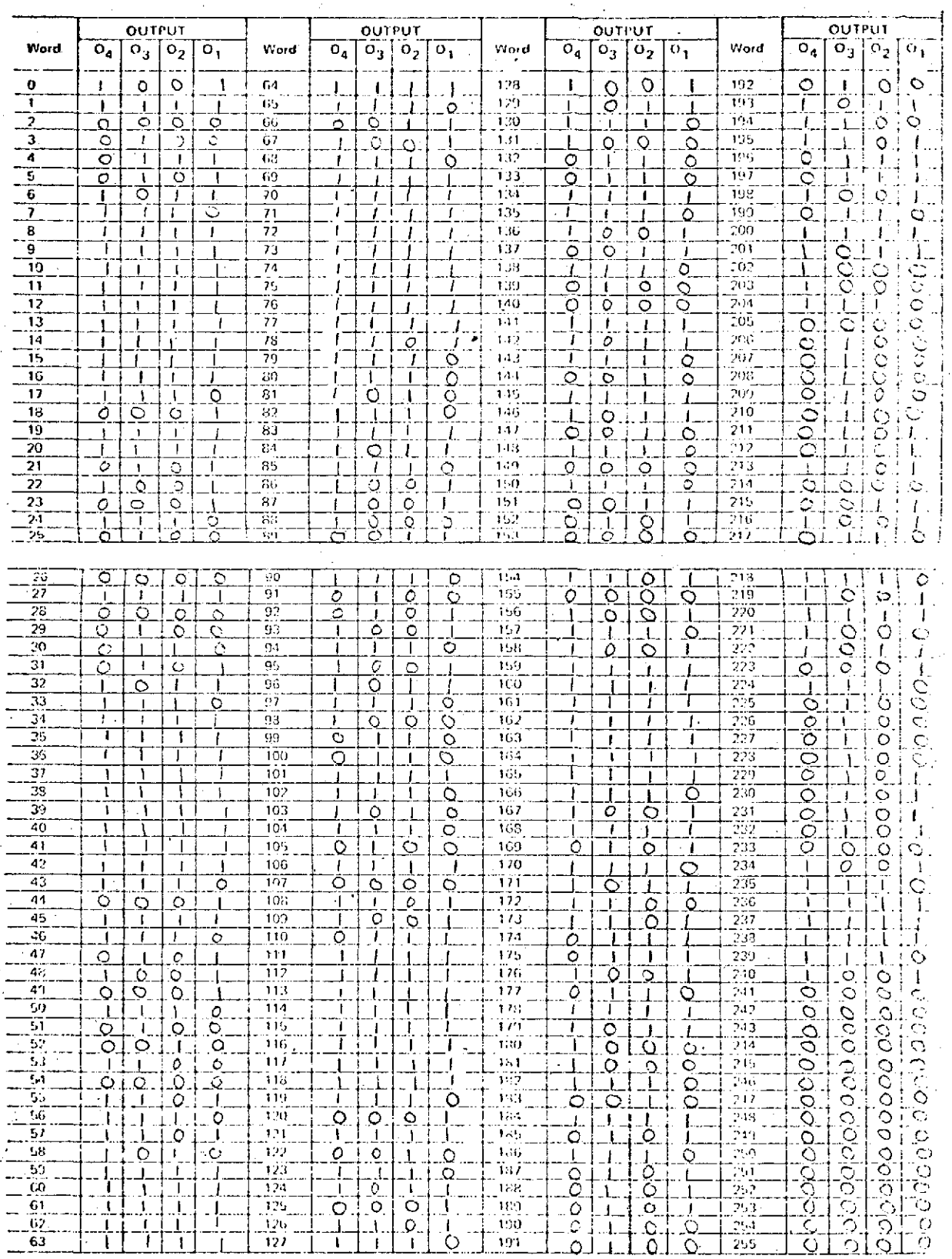


Figure 6-51. PROM Instructions

SECTION 7

BREADBOARD OPERATION

7.1 GENERAL DESCRIPTION

The breadboard model of the vernier doppler extractor contains the analog circuitry required to obtain a 1 MHz bias frequency containing approximately the full S band doppler shift. This is accomplished by translation and multiplication of the 76.083 MHz transponder output frequency. The transponder output contains 8/221 of the S band doppler shift and after translation and multiplication by 24, the bias frequency contains 192/221 of the S band doppler shift.

The digital portion of the one-way doppler extractor recovers the doppler shift information from the 1 MHz bias frequency and passes this information to the spacecraft computer via a suitable interface, and to an operator via a visual display.

Doppler extraction is accomplished using the zero-crossing coincidence technique. Simultaneous zero-crossing of the 1 MHz input signal and a 1.25 MHz reference signal is used to define the start and stop of each measurement interval. In this way the quantization error in the measurement is reduced to the resolution of the coincidence detector. High-resolution is obtained without the use of high clock frequencies.

Two counters count zero crossings of the input signal (F_{B+D}) and the reference signal (F_0), respectively. Since the counts of both counters always contain an integral number of zero crossings, the ratio of the two counts will be proportional to the ratio of the two input frequencies. The doppler shift on F_{B+D} can be obtained by solving:

$$F_D = \frac{N_{B+D}}{N_0} \times F_0 - F_B$$

WHERE: F_D = input doppler shift,

F_0 = reference frequency (1.25 MHz),

F_B = input bias frequency (1.00 MHz),
N_{B+D} = count of input signal counter and,
N_0 = count of reference signal counter

Once the input doppler shift is obtained, other navigation parameters (such as range rate and change in range) may be derived using standard formulas.

The counter outputs N_{B+D} and N_0 are sent directly to the spacecraft computer, which uses these numbers to obtain the navigation parameters desired. To provide a useful display to the operator, the digital extractor contains a microprocessor which calculates and displays the navigation parameters.

The extractor may be controlled either from computer commands or from push-buttons located on the front panel.

7.2 FUNCTIONAL CHARACTERISTICS

The breadboard extractor meets or exceeds the following performance characteristics:

1. The coincidence aperture (resolution) adjustable from 8 to 200 nanoseconds in 2 nanosecond increments. Adjustment is made by using plug-in tapped delay lines and movable straps. Absolute accuracy of the coincidence aperture is $\pm$ 10%.

2. The input (F_{B+D}) and reference (F_0) frequencies may be varied, as long as F_{B+D} and F_0 are less than 1.5 MHz and $2/3 < \frac{F_{B+D}}{F_0} < 2$. (Front panel display of navigation parameters is accurate only for F_B = 1.00 MHz and F_0 = 1.25 MHz.)

3. The reference frequency (F_0) is internally generated using an external 5.00 MHz standard. A rear panel connector is provided for an external F_0 input which can be different from the internal 1.25 MHz. The external source should provide a 12-volt square wave into a 600-ohm load.

4. The 5.00 MHz standard input level should be from 1-2 volts peak into a 50-ohm load.

5. The Integration (measurement) time can be fixed or adjustable. Fixed integration periods of 0.5, 1, 2, 10, 60, or 600 seconds are internally generated from the 5.00 MHz standard. Integration periods are synchronized to an external command and to zero-crossing coincidence. Anytime readout commands may be given to provide externally-generated integration periods from 0.5 seconds to 600 seconds.

6. The measurement delay (from external command to actual start or stop of the integration period) is less than 100 microseconds for coincidence apertures of 180 ns or more.

7. The doppler frequency resolution is better than 0.25 Hz for a 200 nanosecond coincidence aperture and a 1-second integration period.

8. The actual integration period is known to 10^{-7} seconds or better.

9. Computer interface: compatible with Univac Type 1218 computer "single port" mode.

10. Control - either via computer interface or via manual push-button.

11. Test points are provided for external monitoring of zero-crossing coincidence and readout time synchronization. Test point levels are 0 and 12-volts into a 600-ohm load.

12. The maximum doppler shift is $\pm$ 60 kHz at the 1.00 MHz input frequency. This corresponds to greater than $\pm$ 8230 meters/second range rate.

13. Power requirements: 115 VAC 60 cycles.

14. Self test: a reference test frequency of 5/7 MHz is generated from the 5.00 MHz standard. A fixed 2-second doppler count is performed and F_D is extracted. F_D is transformed to the transponder input frequency and checked for accuracy. A go-no go signal is generated and will indicate a "pass" condition if the transformed F_D is within

0.3 Hz of its nominal value, and if the measurement delay is less than 100 microseconds.

15. The counter readout is either destructive or non-destructive.

16. Front panel display:

    a. Light-emitting diodes (LEDs) indicate mode, self-test results, counter readout, interval control, integration period of the unit and navigation parameters selected for visual display. The LEDs are multi-colored, and will be green when the unit is operating normally under computer control. Red LEDs will light whenever an error condition occurs or when the unit is under manual control.

    b. A 9-digit decimal readout displays the following:

        1) N_0, the period count

        2) N_{B+D}, the bias plus doppler count.

        3) F_D (doppler shift transformed to transponder input frequency) in Hertz, displayed to .01 Hz. Accuracy better than 0.25 Hz.

        4) V_R (range rate) in meters per second, displayed to .01 meters/sec. Accuracy better than .04 meters/sec.

        5) ΔR (range change) in meters, displayed to 0.1 meters, either for given integration period (DRO) or optional cumulative measurement in NDRO mode selected by rear panel switch. The accumulator capacity is $\pm$ 4 x 10^6 meters. Accuracy of non-cumulative display is better than 0.2 meters. Accuracy of cumulative display depends on the number of integration periods accumulated and is approximately 0.1 meters per period plus 0.1 meters fixed error.

        6) Self-test error in Hz displayed to .01 Hz. The accuracy is .01 Hz.

c. A 3-digit decimal readout displays the following:

1) Three least-significant digits of N_0.

2) Measurement delay in microseconds, displayed to 1 us accuracy.

Leading zero suppression is provided on the decimal displays. The display will be blanked if the parameter selected has not been calculated by the microprocessor. An error symbol (half size U's) will appear on the display if the microprocessor produces an error signal during the calculation of the navigation parameters.

17. Measurements are either repetitive (successive integration periods) or non-repetitive (single integration period).

18. An overflow indicator is provided to indicate when the time between anytime readout commands exceeds 0.5, 1, 2, 10, 60, or 600 seconds (computer or manually selected) or when the ΔR accumulator is full.

19. Flag bits are sent through the computer interface to alert the computer when the unit is under manual control, when an overflow condition occurs, or when the display microprocessor produces an error signal.

20. Self-test pass/fail results are sent to the computer using an external interrupt command.

21. Measurement data are sent to the computer regardless of mode or manual/computer control selection. The computer must acknowledge all data to enable subsequent data output.

7.3 OPERATION OF THE BREADBOARD

7.3.1 MANUAL OPERATION

The extractor may be manually operated by using the push-button switches on the front panel as shown in Figure 7-1. The unit is connected to a 115-volt, 60 Hertz power source and is turned on using the POWER switch on the front panel. The lamp adjacent to the power switch indicates the presence of power into

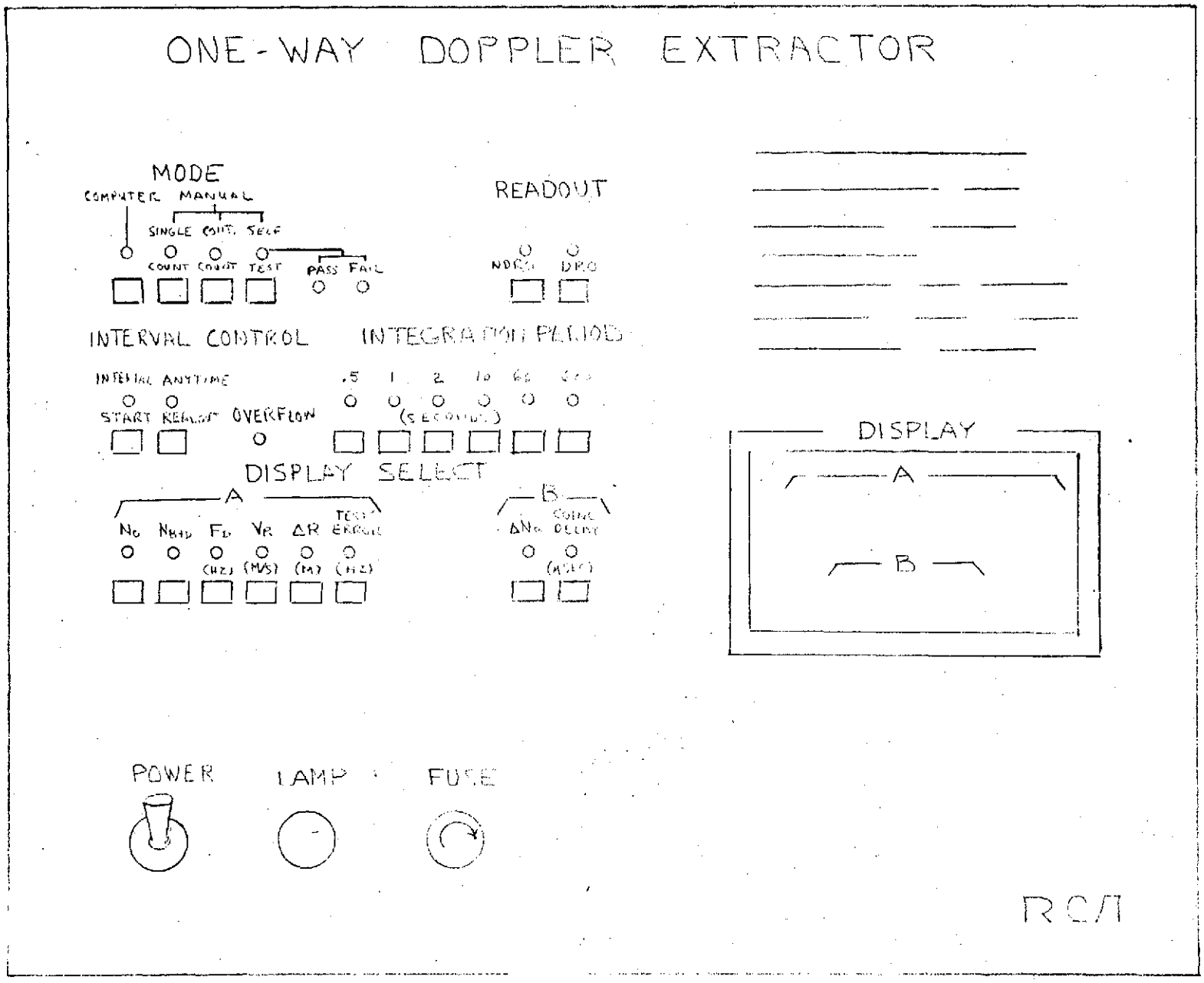


FIGURE 7-1. FRONT PANEL LAYOUT

the unit. The fuse located next to the power lamp protects the circuits at the 115-volt input. It should be replaced with a 3-Ampere fuse when required.

The extractor MODE is selected by operating the proper push-button:

COMPUTER - places the unit under computer control (see Section 7.3.3 on "computer controlled operation" for more information). When pressed, this button disables all of the remaining push-buttons on the panel, except for the "display select" buttons, which are always manually operated. When released the extractor is in the manual mode and all the other push-buttons are activated.

SINGLE COUNT - will cause the unit to perform a non-repetitive measurement. The unit will perform a single count of the doppler frequency and will stop. This mode is useful when manually recording measurements from the visual display, since the measurement results are "held" until the unit is reset.

CONTINUOUS COUNT - will cause the unit to perform repetitive measurements. The unit will produce an output every N seconds, where N is the selected integration period. The unit will be stopped and the display cleared if the reset button or the "self-test" button is pressed. The unit may be stopped and the latest results held in the display by pressing the "single count" button after the completion of at least one count. The counting will then stop immediately.

SELF-TEST - initiates the self-test sequence. This sequence will be described later in this section.

The type of counter READOUT is selected by operating the proper button:

NDRO - When pressed, the N_{B+D} and N_0 counters will be read out non-destructively. Both counters have sufficient capacity to accommodate a single 600-second integration period

without overflow (in the continuous count mode) this condition is detected and corrected by the computer and the display microprocessor.

DRO - Pressing this button causes the N_{B+D} and N_0 counters to reset after each measurement.

Readout may be changed in the course of a series of continuous counts. When the readout is changed by pressing the proper READOUT button, the readout operation will change with the start of the next integration period. The measurement in progress when the buttons are changed is undisturbed.

The INTEGRATION PERIOD is selected by operating the appropriate button (0.5, 1, 2, 10, 60 or 600 seconds). When using the unit in the "anytime readout" function, the "integration period" buttons select the maximum time lapse between anytime readout commands before an overflow condition is indicated. The integration period will self-complete) and the period will change with the start of the next measurement. In this way integration periods may be concatenated to form a net integration period anywhere from 0.5 to 600 seconds in 0.5 second increments. The period may be changed to speed up the display update (such as when landing or docking) or to slow down the display update (for best measurement accuracy).

Note that when the integration period is changed from .5 second or 1-second to 2, 10, 60 or 600-seconds the ΔR cumulative readout and coincidence delay readout may be in error. The operator will <u>not</u> receive an indication of the erroneous readouts in this instance.

The INTERVAL CONTROL buttons are momentary-contact types which function as follows:

INTERVAL START - Pressing this button causes a master reset to be given. All counters and registers within the unit are initialized. The unit does not contain power-on initialization circuits. The interval start button must therefore be operated when power is turned on. This button is used:

a. To initialize a single count measurement.

b. To reset the N_{B+D} and N_0 counters when using NDRO.

c. To stop a continuous count measurement destructively.

d. To synchronize the integration period with external events.

ANYTIME READOUT (ARO) - this button is pressed after a count has begun to cause an anytime readout. The overflow timer is set by selecting the proper integration period button. The count is initiated by pressing the interval start button. Anytime readout is accomplished by pressing the anytime readout button before the integration period timer times out. Once an anytime readout is requested, the unit is forced into a continuous count mode (regardless of the setting of the mode buttons) and readouts will occur only when the anytime readout button is pressed. An overflow indication will be given if the time between ARO commands exceeds the setting of the integration period timer. The integration period timer is reset with each new ARO command. This overflow indication is harmless, and only warns the operator that the display data may be invalid. The unit remains in ARO operation until the interval start button is pressed to reset it.

7.3.2 SELF-TEST OPERATION

The self-test sequence is initiated by transfer of the proper code from the computer or by pushing the "self-test" button on the front panel. The sequence is as follows:

1. Initialization phase - The digital circuitry is held in a master reset condition while the phase-locked loops are allowed to lock to the self-test frequency of 714,285.7 Hz. During this phase a "lamp test" signal is given and all segments of the digital readouts will be lit, along with all of the status indicator lamps (except the mode lamps if the test was manually initiated). The color of the status lamps will depend on whether the self-test was initiated manually or by the computer. This phase will

last approximately 1.5 seconds.

2. Measurement phase - The unit makes a single count, NDRO, fixed 2-second measurement of the self-test signal. The microprocessor will then calculate all parameters and load appropriate latches if the accuracy and delay tests are passed. The digital self-test data will appear on the display as soon as the micro-sequence is complete. Data from the start of the measurement will be displayed in a manner similar to normal unit operation. Raw data is provided to the computer in the normal manner during this phase.

3. Decision phase - A 3.5 second timer is started upon completion of the 2-second fixed measurement. When this times out, the contents of the pass/fail latches will appear on the front panel and will be sent to the computer via an interrupt signal. The "pass" indication will be given only if both the accuracy and delay tests are passed and the display microprocessor has successfully completed its operations without an error indication.

The self-test results will remain on the display until the unit is returned to either the single or continuous count modes or the self-test is repeated.

The measurement phase of the self-test sequence may be repeated by pressing the "interval start" button. The pass-fail indication will appear immediately. This is a non-standard use of the self-test mode, and is provided only as a convenience to a manual operator. When under computer control, the self-test should be repeated only by leaving and then re-entering the self-test mode.

7.3.3 COMPUTER-CONTROLLED OPERATION

Control of the OWD extractor by the 1218 computer may be accomplished by pressing the COMPUTER mode button on the extractor front panel. Operation is functionally identical to operation in the manual mode. All front panel buttons (except the display

select buttons) are disabled.

7.3.3.1 Output Format

The format of the 1218 output used to control the extractor is as follows. A logic one on the EXTERNAL FUNCTION REQUEST lead indicates that the extractor is ready to accept a control command. The 2^0 through 2^7 data leads define the command, according to Table 7-1. The command is read into the extractor on the positive transition of the EXTERNAL FUNCTION lead. The positive transition of the external function lead is used to start and stop measurements when using "interval start" or "ARO" commands.

7.3.3.2 Input Format

The extractor will provide data to the computer input in the form of four 18-bit words. The format is as follows:

Word 1 - Bits 2^0 through 2^{13} equal bits 2^{18} through 2^{31} of N_0, respectively.

Bit 2^{14} will be a "1" if the display microprocessor has made an error.

Bit 2^{15} will be a "1" if the overflow lamp was lit during the measurement interval.

Bit 2^{16} will be "1" if the extractor is under computer control. This bit will be "0" if the unit is under manual control.

Bit 2^{17} will be a "1" if the RUN/HOLD switch on Board 8 of the digital logic is in the run position. This bit will be "0" if the switch is in the hold position. Data is invalid if this bit is "0".

Word 2 - Bits 2^0 through 2^{17} equal bits 2^0 through 2^{17} of N_0, respectively.

Word 3 - Bits 2^0 through 2^{13} equal bits 2^{18} through 2^{31} of N_{B+D}, respectively. Bits 2^{14} through 2^{17} should be "0".

TABLE 7-1. OWD EXTRACTOR COMMAND FORMAT

COMPUTER OUTPUT BIT	2^0 2^1 2^2	2^3	2^4	2^5	2^6	2^7
FUNCTION	INTEGRATION PERIOD	COUNT	ARO	SELF-TEST	READOUT	INTERVAL START
INTEGRATION PERIOD						
0.5 Sec	0 1 1	1 = Contin. Count	1 = Anytime Readout	1 = Self-Test Mode	1 = DRO	1 = Interval Start
1 Sec	1 1 0				0 = NDRO	
2 Sec	0 0 1	0 = Single Count				
10 Sec	0 1 0					
60 Sec	1 0 0					
600 Sec	0 0 0					

Bit 2^5 = 1 will override all other bits except bit 2^7.

Bit 2^4 = 1 will override bit 2^3. Bits 2^4 and 2^7 must never be 1 simultaneously.

Word 4 - Bits 2^0 through 2^{17} equal bits 2^0 through 2^{17} of N_{B+D}, respectively.

The INPUT DATA REQUEST lead will be high when valid data is at the input cable connector. All four input words must be read and acknowledged using the INPUT ACKNOWLEDGE lead. The input data request lead will toggle to zero and back to logic one when a new data word is at the interface. The input words must be acknowledged whether they are used or not, otherwise subsequent data will not be valid. Input data is present at the start and completion of each measurement interval, in both computer-controlled and manual operation.

The EXTERNAL FUNCTION REQUEST lead on the output cable will be a "0" while input data is being read into the computer, and will return to the "1" level when all four input words have been acknowledged. This prevents new control commands from being given to the extractor until the data from the previous command has been acknowledged.

Self-test results are provided to the computer using the EXTERNAL INTERRUPT lead. When this lead is a "1", the 2^{17} data bit will indicate the results. A "1" at the 2^{17} bit position indicates the self-test has FAILED; a "0" indicates that the self-test was PASSED. All other data bits should be ignored by the computer. The external interrupt lead will return to a "0" when the computer acknowledges the self-test result. To obtain subsequent data from the extractor, the unit must be taken out of the self-test mode.

Input data in the four-word format described above will be present at the start and completion of the self-test measurement interval, and must be acknowledged as described earlier. The raw data may be used by the computer to independently check the self-test results.

7.3.3.2 Computer Interface Test-Unit

An interface test-unit is supplied with the extractor for two purposes: 1) to allow the user to empirically determine effects

of various command sequences on the extractor; and 2) to verify the operation of the interface logic. The unit is plugged into the input and output connectors at the rear of the extractor, and is powered via pin 88 of the input connector. LEDs indicate the status of bits from the extractor to the computer. Switches control bits from the computer to the extractor.

Command codes may be set up using the eight toggle switches, as shown by the front panel layout of Figure 7-2, and read into the extractor using the EXT FUN button. The INPUT ACK button is pressed to acknowledge data from the extractor. Refer to Table 7-1 for the conversion of computer commands to the appropriate toggle switch positions.

Operation of the computer interface logic in the extractor may be verified with the test unit in the following manner:

1) Remove the cover from the digital nest.

2) Throw the switch on Board 8 to the HOLD position.

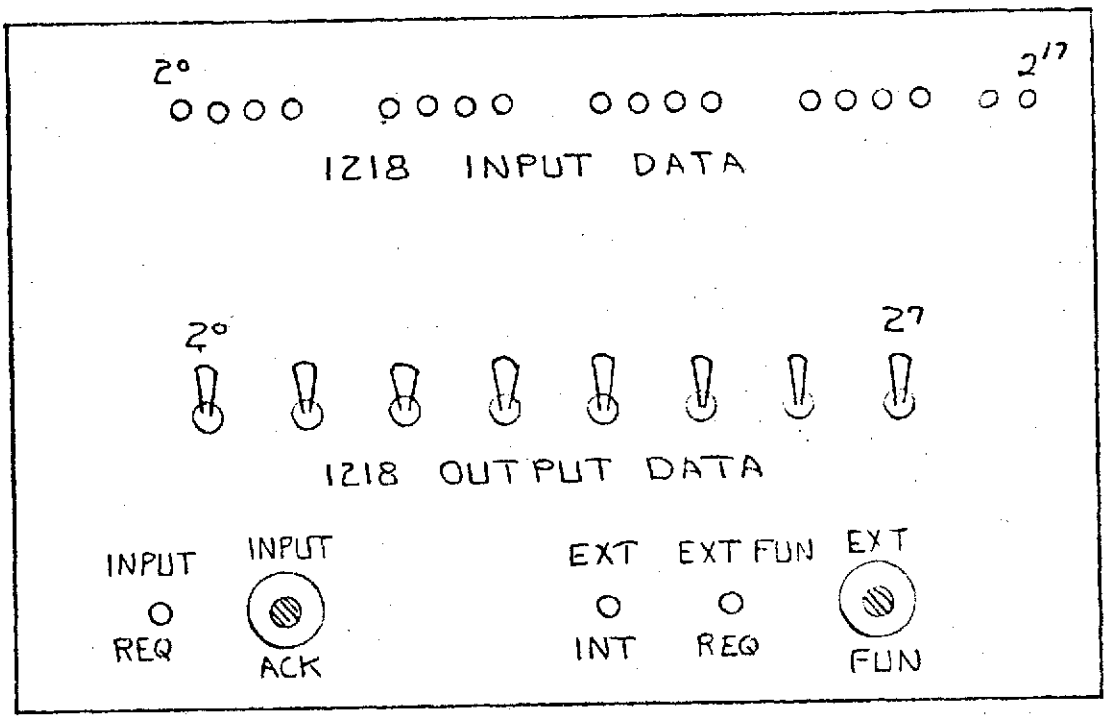
3) Push the COMPUTER button on the front panel.

4) Set up a command word for a SINGLE COUNT, NDRO measurement. A self-test command may be used.

5) Press the EXT FUN button and then immediately press the INPUT ACK button four times. The EXT FUN REQ lamp should now be lit.

6) Permit the selected interval to time out. The INPUT DATA REQ lamp should now be lit. Input word 1 will appear on the LEDs in the test unit. Pressing the INPUT ACK button should access words 2, 3, and 4 in succession. The EXT FUN REQ lamp should be extinguished during this period. This lamp should once again be lit after INPUT ACK is pressed for the fourth time.

7) Compare the data words at the test-unit with the extractor data. There should be a one-to-one correspondence between the test-unit indicators and the LED indicators on Boards 4-8 as shown in Figure 7-3. The data should represent the



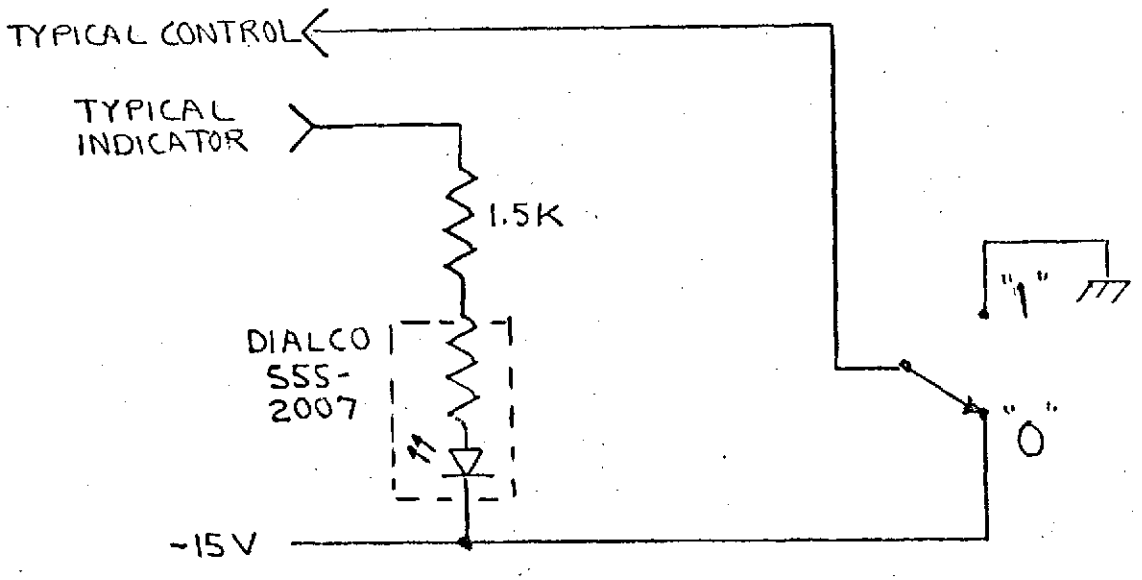


FIGURE 7-2. COMPUTER INTERFACE TEST UNIT

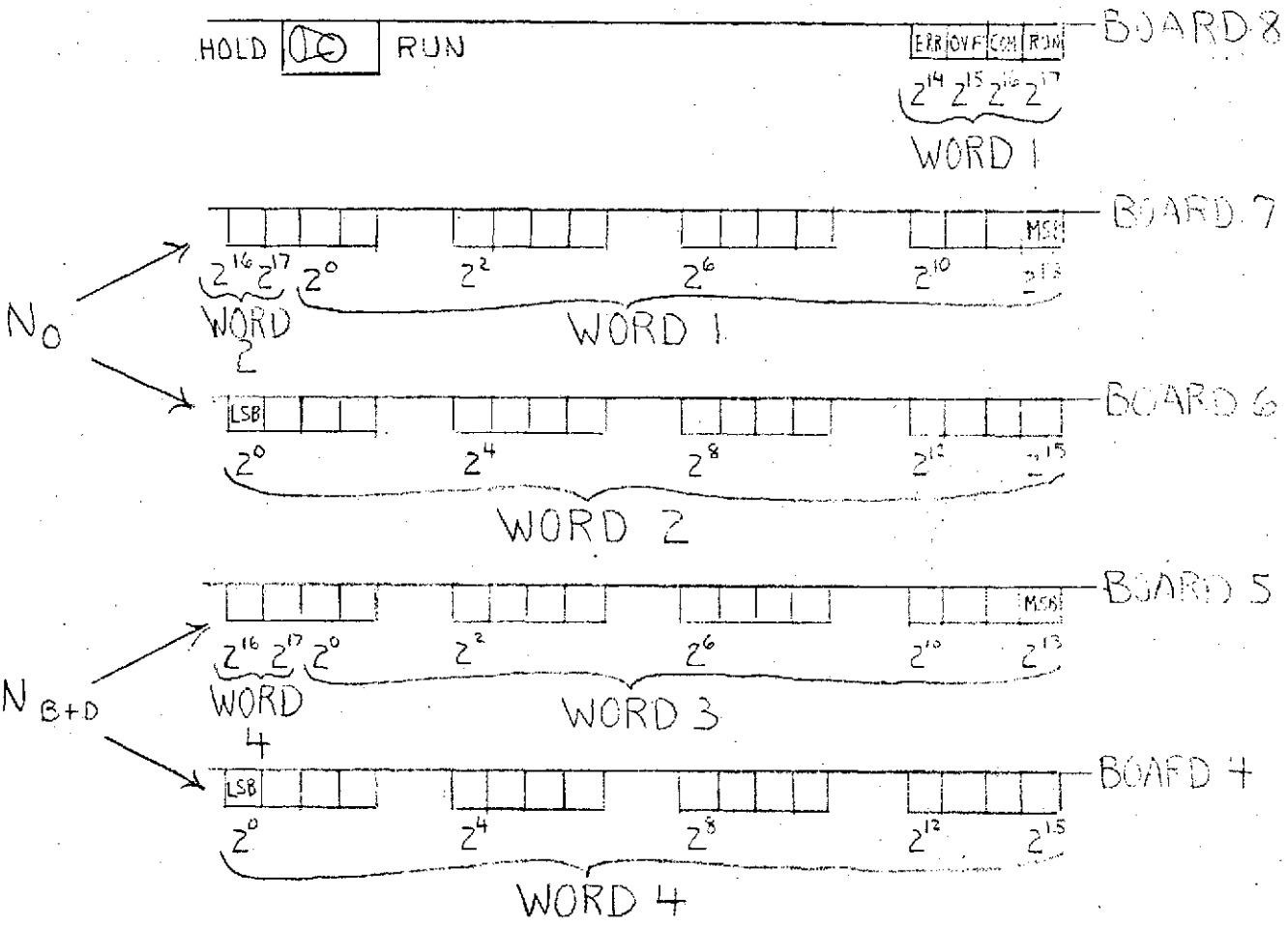


FIGURE 7-3. EXTRACTOR DATA WORD INDICATORS

binary equivalent of the corresponding raw data appearing on the front panel decimal display.

8) If a self-test was used for (4) wait for the self-test result. The EXT INT lamp should be lit when the front panel pass/fail indication is given. The 2^{17} indicator should indicate the proper result. Pressing the INPUT ACK button should extinguish the EXT INT lamp.

9) This completes the interface logic validation. BE SURE to return the switch on Board 8 to the RUN position before replacing the digital nest cover.

7.4 STATUS INDICATORS

LED indicators are provided to indicate the status of the unit. These indicators are associated with the appropriate control buttons, and indicate the actual status. If the control buttons are overridden (when under computer control, during a self-test, when using ARO, or when the integration period is changed and the current period is not complete) the indicators show the current status of the unit, regardless of the overridden button settings. (Exception: the single/continuous count indicators are not overridden in manual operation, although the push-buttons are overridden.)

When the unit is under computer control, the status indicators will be GREEN. When the unit is under manual control, the status indicators will be RED.

LEDs display the results of a self-test when in the self-test mode, and indicate an overflow condition when the ΔR accumulator is full or when the ARO interval timer has timed out. The PASS indicator is GREEN, while the FAIL and OVERFLOW indicators are RED.

The overflow indicator warns that the display data may be invalid. If it was set due to an ARO time-out, it will be reset with the next ARO command. If it was set because the ΔR accumulator is full, the LED will remain on to indicate that the ΔR accumulator has been disabled. (The readout for ΔR will be

forced back to indicating the change in range for the given integration period only.) In this latter case the overflow indicator will be reset only when the counters are reset either by use of the interval start button or by changing to DRO. This indicator is "harmless", in that other measurements are not disturbed when it is set.

The "interval start" indicator will be lit when counting is in progress. The ARO indicator will be on when the unit is "locked" in the ARO mode.

Integration period indicators display the actual integration period of the unit.

7.5 DIGITAL DISPLAYS

A dual display is provided on the unit to allow direct readout of important parameters.

A 9-digit display (designated display A) displays one of the following, depending on the DISPLAY SELECT button pushed:

a) N_0 - 9 digits

b) N_{B+D} - 9 digits

c) F_D (in Hz) - sign, 8 digits, and decimal point

d) V_R (in meters/sec) - sign, 8 digits, and decimal point

d) ΔR (in meters) - sign, 8 digits, and decimal point

f) TEST ERROR (in Hz) - sign, 8 digits, and decimal point

A 3-digit display simultaneously displays one of the following, depending on the DISPLAY SELECT button pushed:

a) ΔN_0 - last 3 digits of N_0

b) COINCIDENCE DELAY (in microseconds) - 3 digits

Green LEDs above the display select buttons indicate the parameters appearing on the displays.

An option is provided when using NDRO and viewing ΔR. By throwing the ΔR ACCUMULATOR switch, located on the rear lip, to the ENABLE position, the ΔR display will be the cumulative

total change in range since the last master reset. The accumulator capacity is $\pm$ 4 x 10^6 meters. If this capacity is exceeded, the accumulator will be disabled by the digital logic, and the overflow lamp will be lit. With the accumulator disabled, the display ΔR will indicate the change in range for a given integration period only, and not the cumulative total. The accumulator may be reset in one of two ways:

a) Depressing the INTERVAL START button (resets all counters).

b) Selecting DRO, and then returning to NDRO operation (this maintains the synchronization of the integration period timer).

The overflow indicator will be extinguished when the accumulator has been reset.

The TEST ERROR display will be blanked unless the self-test mode is selected. The COINCIDENCE DELAY display will be blanked in the ARO operation, since coincidence delay calculations depend on a priori knowledge of the nominal integration period.

Leading zeroes (except for zeroes in the last digit position or immediately preceding a decimal point) are blanked on both displays. An error symbol (␣) will appear on both displays if the microprocessor gives an error indication during the calculation of the parameters that otherwise would have appeared on the display. This error may be caused by erroneous input to the microprocessor from the counters or from the microprocessor memory, or by a malfunction of the microprocessor itself.

The display microprocessor may not complete all of the parameter calculations before the data for the next calculations are ready. This condition occurs when the integration period is less than 2 seconds, and continuous measurements are being made. In this case, the microprocessor will reset with the receipt of the new data, and abandon the remainder of the microsequence. The display will be blanked for those parameters

which were not calculated when the micro-sequence was aborted. The blanking function overrides the microprocessor error indication. Error symbols will appear only for those parameters calculated before the error occurred. The parameter calculation where the error occurred may thus be isolated.

The displays will occur in the following sequence:

1) The display will initially be blanked following an interval start command.

2) The display will then indicate the results for the start of the first interval, either when the microprocessor has completed the micro-sequence for the initial data, or when the micro-sequence is aborted due to the receipt of new data (representing the completion of the initial count).

3) The display will next indicate the results for the completion of the first integration period, either when the micro-sequence is completed or aborted only if continuous measurements are being made.

4) If continuous count measurements are being made, the display will indicate the results of subsequent measurements, in a manner similar to (3).

The delay from the completion of a measurement to the completion of the micro-sequence (when the results of that measurement are displayed) is approximately 1.8 seconds. When using the unit in the 0.5 second continuous count mode, only N_{B+D} and N_0 will be displayed. When using the unit in the 1-second continuous count mode, N_0, N_{B+D}, F_D, and V_R will be calculated. When using larger integration periods, or when in the single count mode, all parameters are calculated.

When in the single count mode with a 0.5- or 1-second integration period, the ΔR and coincidence delay calculations are not made on the data at the start of the measurement. The data appearing after the completion of the integration period will always be invalid for the coincidence delay, and will be invalid for the ΔR display if the ΔR accumulator was in use.

Since no indication of this erroneous condition is given to the user, data should not be used. Similarly, ignore the ΔR accumulator and coincidence delay data if the integration period was extended from the 0.5- or 1-second periods in the continuous count mode.

The microprocessor calculations should be the same whether in the DRO or NDRO modes of operation, with the exception of the ΔR accumulator display. Only the change in N_0 and N_{B+D} over the given integration period is used in the calculations. The resolution of the displayed navigation parameters will not improve with subsequent continuous measurements. The NDRO raw data is, of course, available to the 1218 computer, and improved resolution may be obtained with appropriate algorithms in the computer software. The improvement in resolution by using the NDRO mode of operation may be observed by comparing the computer results to the OWD extractor display.

When comparing the extractor display to external parameter measurements, the following parameters are to be used:

F_B - input bias frequency = 1.00 MHz

F_0 - input reference frequency = 1.25 MHz

F_D (at transponder input) = F_D (at digital input) x 221/192

F_D (at transponder input) appears on the extractor display.

λ_T - transponder input wavelength = 0.1641799015 meters

Nominal self-test equivalent doppler off-set frequency = -328,869.0477 Hz (at transponder input)

7.6 EXTERNAL CONNECTIONS

Connection of the extractor unit is illustrated in Figure 7-4. Input and output cables for the 1218 computer plug into the appropriately marked connectors at the rear of the extractor. The AC power cable is plugged into the 115 VAC connector.

The 76.0833 MHz transponder intermediate frequency output is connected to the "76 MHz" input. A 5-MHz precision frequency standard should be connected to the "5 MHz" input. The 5 MHz input levels are sensitive, and should be no less than 1-volt peak and no more than 2-volts peak into a 50 ohm impedance. Input levels outside of this range will cause erroneous operation of the extractor.

The 1.25 MHz F_0 signal is internally generated in the extractor. If a different F_0 is desired, such as when making resonance or accuracy tests, a 12-volt square wave signal (never greater in frequency than 1.5 MHz) may be connected to the "F_0" connector. The connector input impedance is 600 ohms. The extractor will automatically detect the presence of the signal at the F_0 input and switch to the external reference. The extractor will switch back to the internal 1.25 MHz signal upon loss of signal at the F_0 input. Remember that the display microprocessor assumes a 1.25 MHz reference frequency, and displayed parameters will be correspondingly in error when using different reference frequencies.

Two other connectors are provided at the rear of the extractor. The COINCIDENCE output provides a 12-volt, 1 - microsecond positive pulse whenever zero-crossing coincidence of the F_0 and F_{B+D} signals occurs (within the aperture of the coincidence detector). This output is useful when observing measurement delays and resonance effects.

The STROBE output provides a 12-volt, 300 nanosecond, positive pulse at the beginning and end of the actual integration periods. The positive transition of this pulse may be used to measure the actual integration period length, or to synchronize the measurement period of an external counter (such as the HP

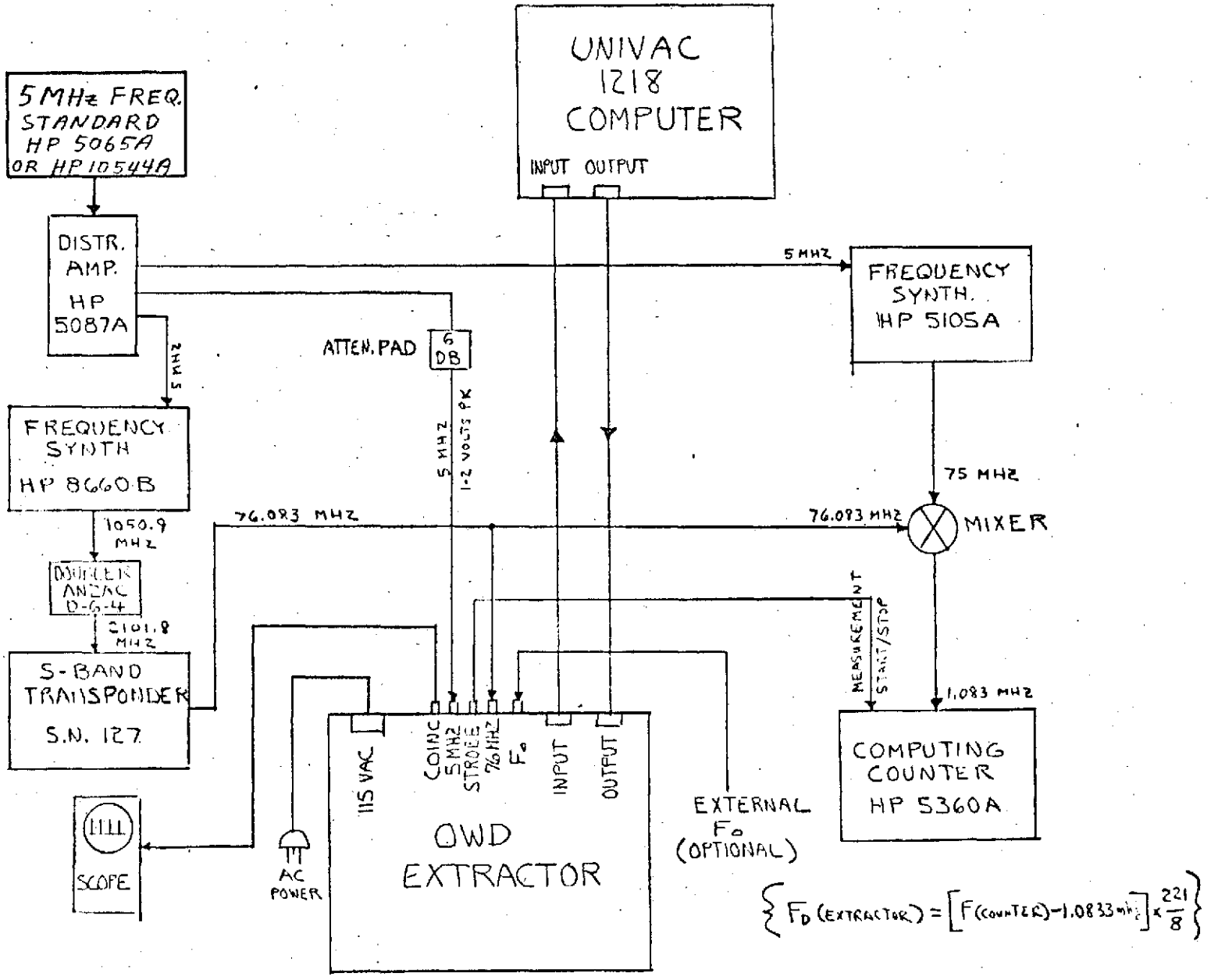


FIGURE 7-4 TYPICAL TEST SET-UP

computing counter) to the extractor measurement period. In this way accurate comparisons may be made when sweeping the transponder input frequency.

The coincidence and strobe outputs are capable of driving a 600-ohm load.

7.7 CHANGING COINCIDENCE APERTURE

The coincidence aperture may be changed by moving the straps located on the coincidence detector board (Board 1). Remove Board 1 from the digital nest, and set the straps as desired. The straps (one per delay line) are located on the wiring side of the board in back of the delay lines. From the wiring side, the delay line to the left controls the N_{B+D} pulse width, while the delay line to the right controls the N_0 pulse width. Strap Positions 1 through 10 correspond to 10% through 100% of the total delay (in nanoseconds) stamped on the delay line. The straps are run from the desired delay line tap to the path running between the taps.

The coincidence aperture is the sum of the N_{B+D} and N_0 pulse widths. It is preset at 200 nanoseconds, the minimum aperture to eliminate resonance effects over the doppler range. Smaller apertures will result in greater frequency resolution at the expense of increased time delays. The test points on the coincidence board may be used to verify board operation. Test point A corresponds to N_{B+D} and the width of the pulse at this point should match the delay line setting. Test point B corresponds to the N_0 pulses. Test point C represents the coincidence of the pulses at points A and B. The test point signals are standard ECL level outputs.

100-nanosecond delay lines are normally used on the coincidence board. 20-nanosecond delay lines are also supplied with the unit. These delay lines may be plugged in the desired delay line sockets to obtain very narrow pulse widths.

SUB-MINIATURE DELAY LINE

DUAL IN-LINE CONFIGURATION
10 DELAY POINTS

Each Delay Line has ten tap delays spaced at equal intervals with accuracy of ±5%.

Attenuation is less than 1 db.

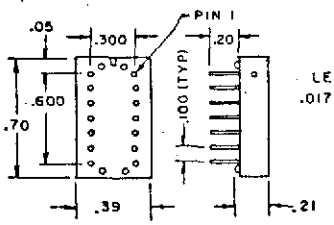
Temperature coefficient is less than 60 PPM/°C.

Maximum operating voltage is 25 V.

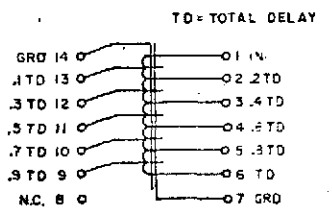
Encapsulated in epoxy resin.

Meets all applicable military specifications.

MODEL D1511 SERIES			
MODEL NO.	DELAY	RISE TIME	IMPEDANCE
D1511-1	10 NANOSECS	3 NANOSECS	100 OHMS ±5%
D1511-2	20	6	
D1511-4	40	13	
D1511-6	60	20	
D1511-8	80	26	
D1511-10	100	33	

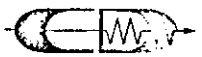


PHYSICAL DIMENSIONS



SCHEMATIC DIAGRAM

Other delays, rise times and impedance can be furnished.



COMPUTER DEVICES CORP.
63 AUSTIN BOULEVARD COMMACK, N. Y. 11725

FIGURE 7-5 DELAY LINE DATA SHEET

When using the 20-nanosecond delay lines, do not set the taps below 4-nanoseconds (Tap 2), since the 1-nanosecond propagation delay and rise time of the coincidence logic will severely distort the coincidence pulses.

A data sheet for the delay lines is shown in Figure 7-5 for the users information.

SECTION 8

PERFORMANCE RESULTS

8.1 PERFORMANCE TEST PROCEDURE

The vernier doppler extractor breadboard was tested to verify that required specifications were met and that the performance analysis of Part I was valid. The test procedure included five separate tests of accuracy and time delay under various conditions of coincidence aperture width (coincidence pulse width into the "AND" gate), doppler off-sets, doppler rates, integration period length and S-Band signal level.

The test procedure used the test equipment configuration of Figure 8-1. The Hewlett-Packard L-Band frequency synthesizer was used, along with a frequency doubler, to generate a reference S-band signal for the S-band transponder. The extractor breadboard obtained the doppler measurement from the 76.083 MHz transponder output (J7 of Chassis Sub-Assembly A1). The Hewlett-Packard computing counter supplied a comparison doppler measurement from the one megahertz bias frequency in the extractor. A common quartz oscillator supplied clock and synthesizer reference signals to all units through the distribution amplifier. Since a common oscillator was used the tests did not include frequency drift effects in the measured results. The purpose and procedure for obtaining the five extractor sensitivity tests follows:

8.1.1 TEST #1 - COINCIDENCE APERTURE SELECTION

Purpose:

To initially define an operational coincidence aperture which will produce the greatest doppler measurement accuracy for a maximum time delay (skewness) of 100 μs.

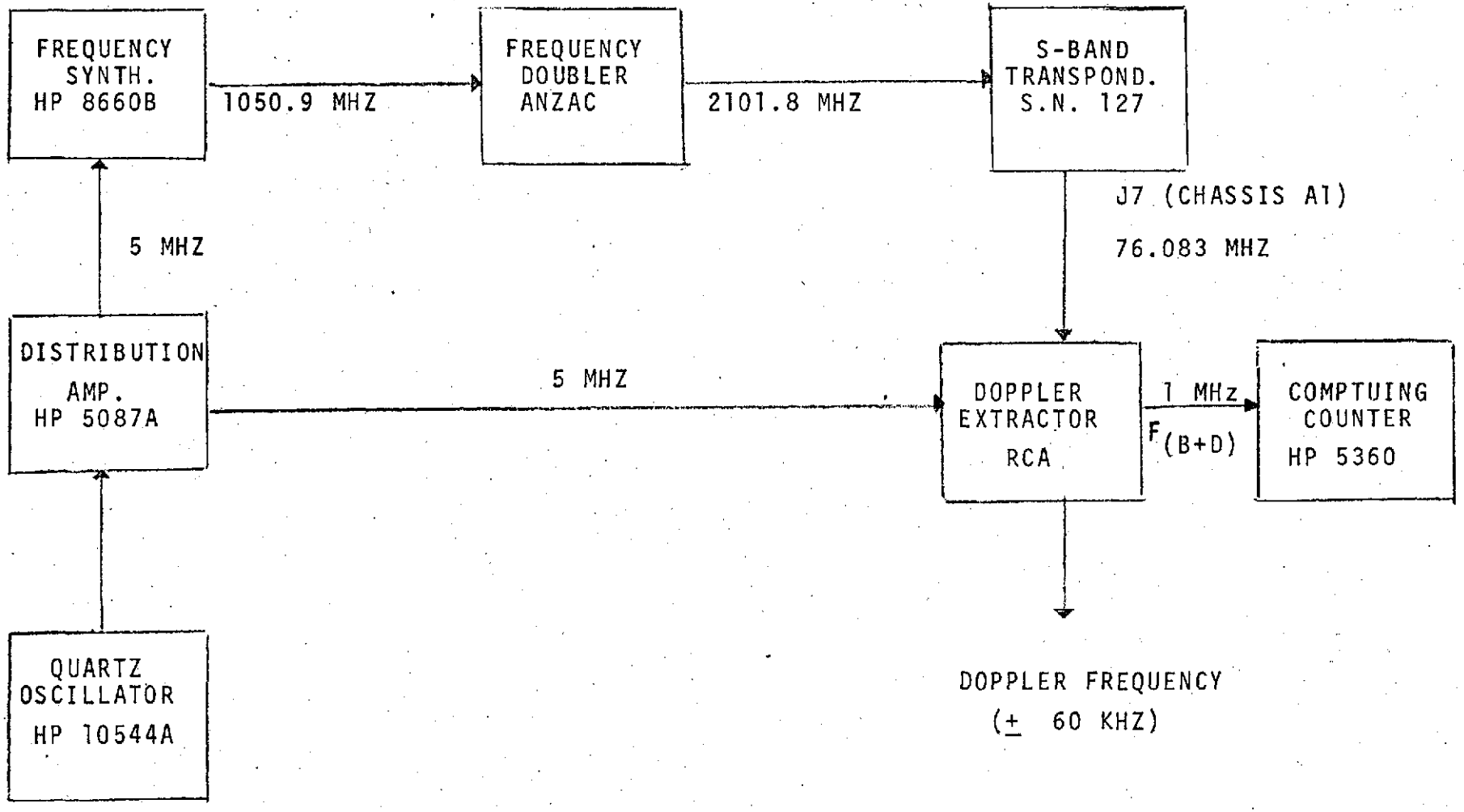


FIGURE 8-1 TEST SET UP FOR DOPPLER EXTRACTOR PERFORMANCE TESTS

Procedure:

The time delay (skewness) statistics depend on the coincidence aperture and the ratio of the bias plus doppler frequency to the clock frequency. At the clock frequency of 1.25 MHz the maximum delay occurs at zero doppler where $F(B+D)/F_0 = 4/5$. Thus, at zero doppler about 100 measurements of time delay will be made to determine the delay statistics for coincidence aperture (sum of the two pulse widths) of 50, 70, 90 and 100 ns. From these measurements the expected time delay and 95 and 99 percentiles will be computed. From these computations a minimum aperture will be selected which produces a 99 percentile time delay of less than 100 μs. The selected aperture will then be used for all other accuracy measurements of the doppler extractor.

At the selected aperture, about 400 additional measurements of the time delay will be made to construct detailed statistics of the time delay such as histograms, cummulative probability curves as well as mean and percentile levels of time delay.

8.1.2 TEST #2 - DOPPLER SENSITIVITY TESTS

Purpose:

To verify the extractor accuracy at various values of doppler off-set.

Procedure:

The doppler accuracy measurements will be made using an integration time of 0.5 seconds and a S/N ratio into the S-band transponder of about 30-40 dB.

Approximately 30 measurements will be made at doppler off-sets of approximately 0, 30,0-0 and 60,000 Hz.

8.1.3 TEST #3 - SENSITIVITY OF DOPPLER ACCURACY TO SIGNAL LEVEL

Purpose:

To determine the range of signal levels over which the doppler extractor is capable of meeting the accuracy requirements.

Procedure:

The S-band transponder threshold signal level which maintains continuous lock will be determined. Approximately 30 measurements of doppler accuracy will be made at signal levels of 3 dB, 10 dB and 30 dB above this threshold level, using an integration period of 0.5 seconds and a nominal doppler off-set value.

8.1.4 TEST #4 - SENSITIVITY OF DOPPLER ACCURACY TO INTEGRATION PERIOD

Purpose:

To verify that the doppler extractor can meet the accuracy requirements at integration periods of 0.5, 2, 10, 60 and 600 seconds.

Procedure:

Using a nominal signal level 30 dB above threshold and a nominal doppler off-set, approximately 30 measurements of doppler accuracy will be made at integration periods of 0.5, 2 and 10 seconds. At integration periods of 60 and 600 seconds approximately 10 doppler measurements will be made.

8.1.5 TEST #5 - SENSITIVITY OF DOPPLER ACCURACY TO DOPPLER RATES

Purpose:

To verify that the extractor can meet the accuracy requirements at the maximum doppler rate of about 4000 Hz/second.

Procedure:

The L-Band synthesizer will be frequency swept at approximately 2000 Hz/sec (4000 Hz./sec at S-Band). S-band signal level about 30 dB above threshold and a doppler integration period of 0.5 seconds will be used. Doppler measurements will then be obtained simultaneously using both the OWD extractor and the computing counter. The computing counter will be used to define the actual average value of doppler over the integration period. These values will be compared to the extractor values to determine the measurement errors.

Since it is important to have a small time delay for good doppler accuracy, when a doppler rate is present, the initial and final time delays will also be measured. With the time delay measurements, any large doppler errors can be analyzed to determine if they were caused by large time delays.

8.2 PERFORMANCE RESULTS

8.2.1 DOPPLER EXTRACTOR ACCURACY

Figure 8-2 shows the results of the sensitivity of doppler accuracy to integration time and coincidence detector aperture (twice the pulse width). The results indicate that the extractor is capable of measuring the S-band doppler to an accuracy of 0.03 Hz or better if aperture widths of 15 ns are used. This error is primarily caused by the quantization error for short averaging intervals as shown by comparison with the expected quantization error. At long averaging intervals (>5 seconds), the error is greater than the expected quantization error primarily due to clock and reference frequency instability. With an aperture of 180 ns, the accuracy degrades to about 0.3 Hz in a 0.5 second averaging period. This can be compared to a conventional zero crossing counter which would normally have a peak error of 2 Hz in a 0.5 second averaging period. Measurements of doppler accuracy with apertures less than 15 ns were not made although the breadboard was designed to operate with an aperture as low as 2 ns. Had this aperture been used in the measurements the expected peak quantization error would be 0.008 Hz in a 0.5 second averaging period.

8.2.2 TIME DELAY STATISTICS

As described in Part I, the peak time delay between a command and actual start of the counters, or time between coincidences, is sensitivie to the aperture width and the ratio of the bias frequency to clock frequency (N/M).

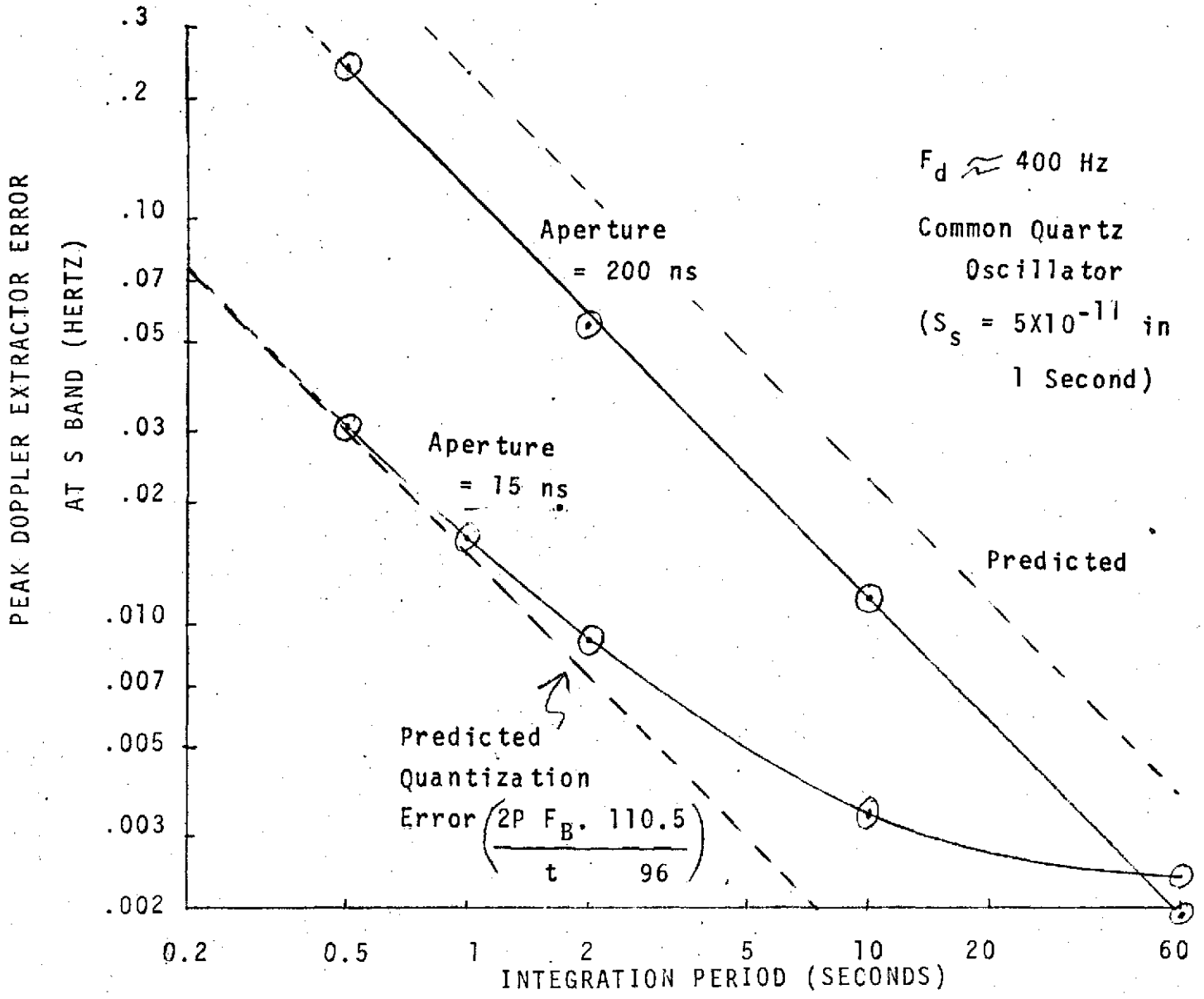


FIGURE 8-2. OWD EXTRACTOR MEASUREMENT ERROR

If the aperture width (2P) is made shorter than T_o/N(T_o=1/F_o = clock period) the time delay could be infinite. That is, a coincidence will never occur and the logic circuits would receive no command to start the counters. In a practical system, however, phase jitter will eventually cause a coincidence to occur.

If the aperture width is made less than T_o/N, the maximum delay will occur when N is a minimum value. Over the doppler range of $\pm$ 60 KHz, N is a minimum at zero doppler [$(F_B + F_d)/F_o$ = 1.00/1.25 = 4/5] and has a value of 4. Therefore, large delays can be expected whenever the aperture is less than 200 ns (T_o/N = 800 ns/4).

Figures 8-3, 8-4 and 8-5 show the statistics of the time delay for apertures of 200 ns, 180 ns and 15 ns, respectively. With an aperture of 200 ns the delay is uniformly distributed with a maximum delay of four microseconds. As the aperture is decreased to 180 ns the distribution of delays appears to follow a Rayleigh distribution with large values of delay occurring occasionally. At an aperture of 15 ns very large delays are common. With this aperture delays above 30 milliseconds occur half of the time.

Figure 8-6 shows the sensitivity of the 95 percentile value of time delay to the aperture width. The results show a nearly linear relationship between the logarithm of the time delay and the value of the aperture width.

As the doppler shift changes from the highly resonant condition of zero doppler the time delays decrease rapidly. For example, at an aperture of 15 ns, the 95 percentile time delay is about 50 μs at zero doppler. However, at a doppler off-set of less than 500 Hertz, the 95 percentile delay decreases to only 300 μs.

If there would be a range rate when the doppler shift is near zero, the zero doppler resonant condition would be short lived. For example, a doppler rate of 1 KHz/second

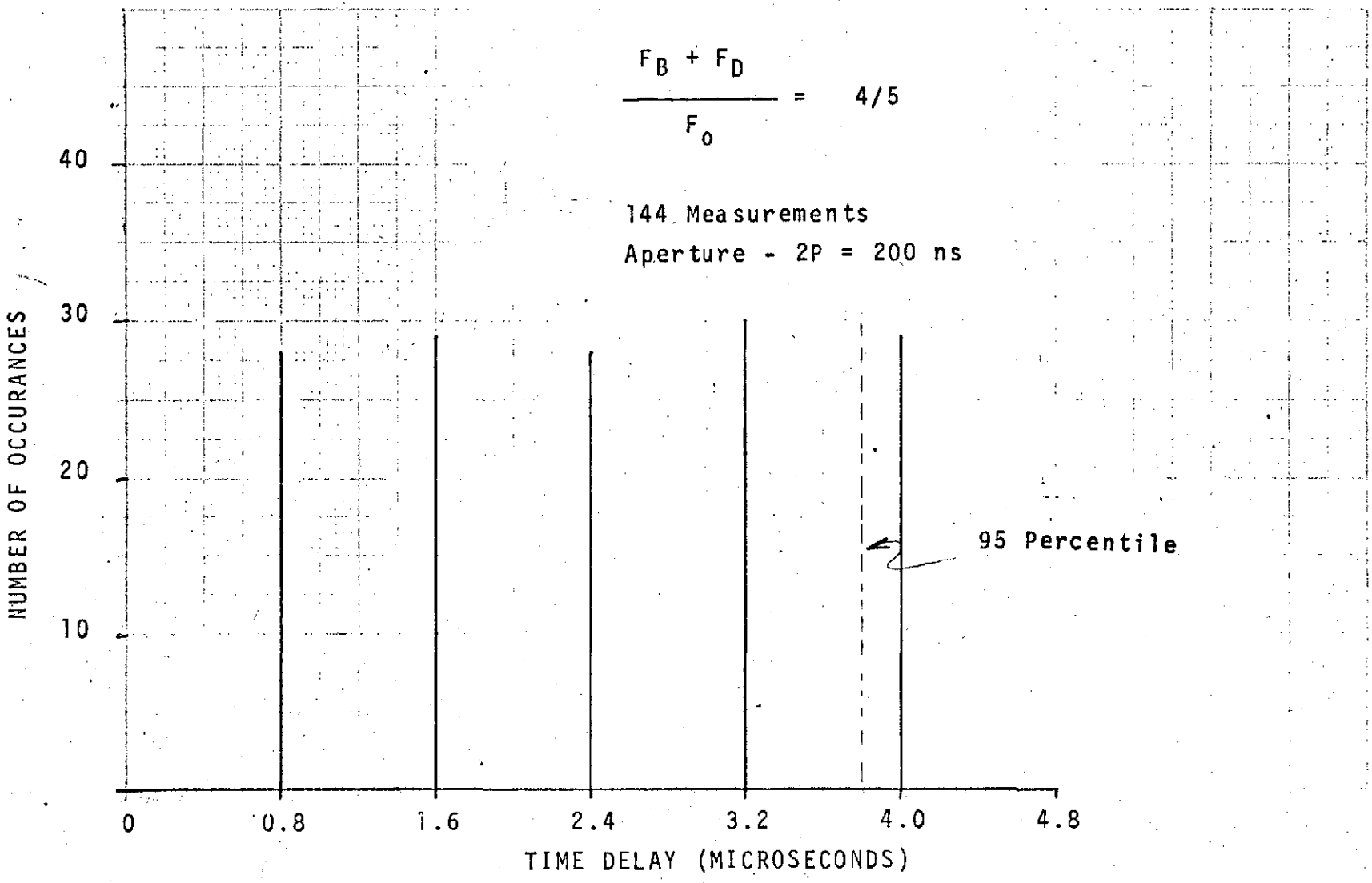


FIGURE 8-3. DISTRIBUTION OF DELAY TIME

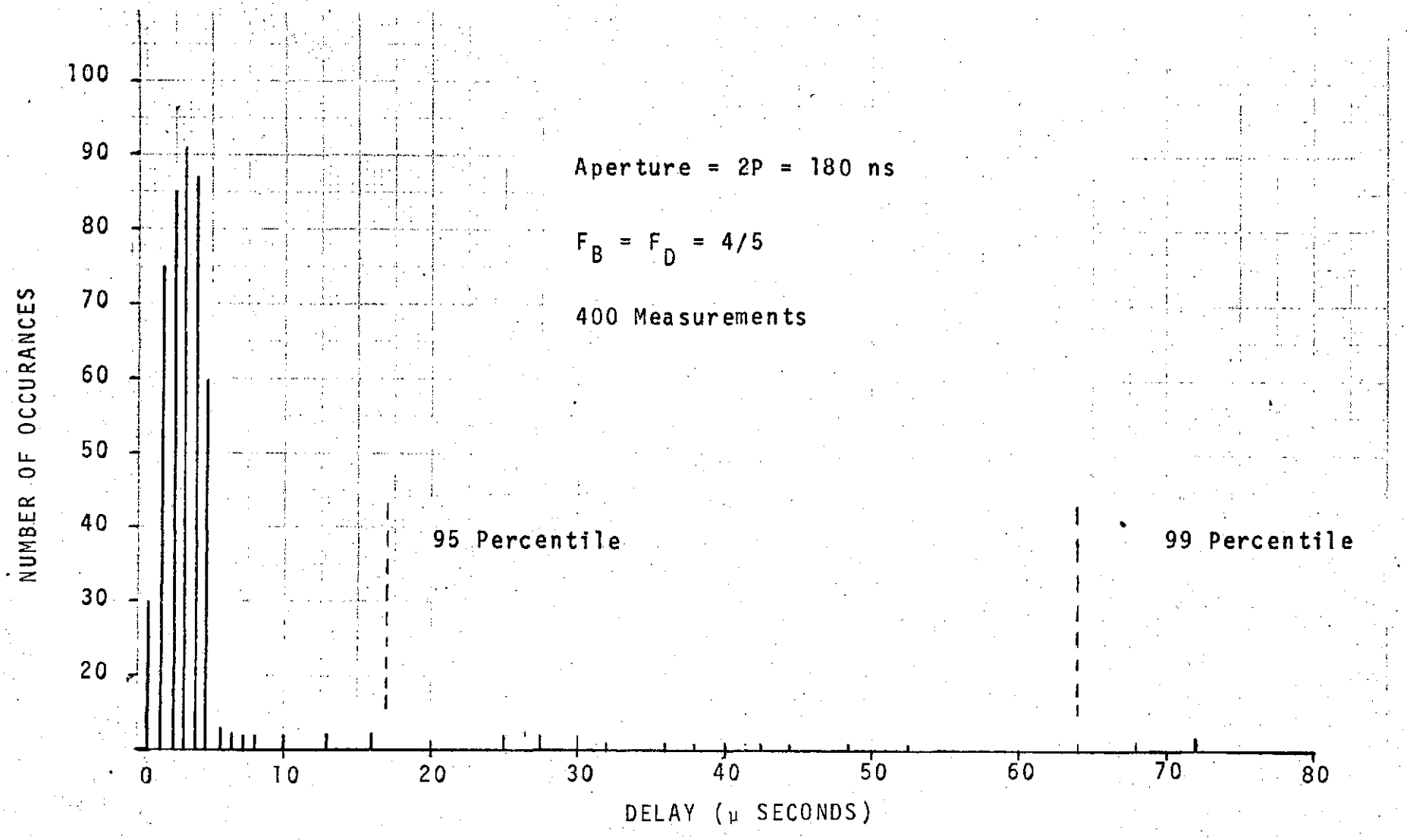


FIGURE 8-4. DISTRIBUTION OF TIME DELAY

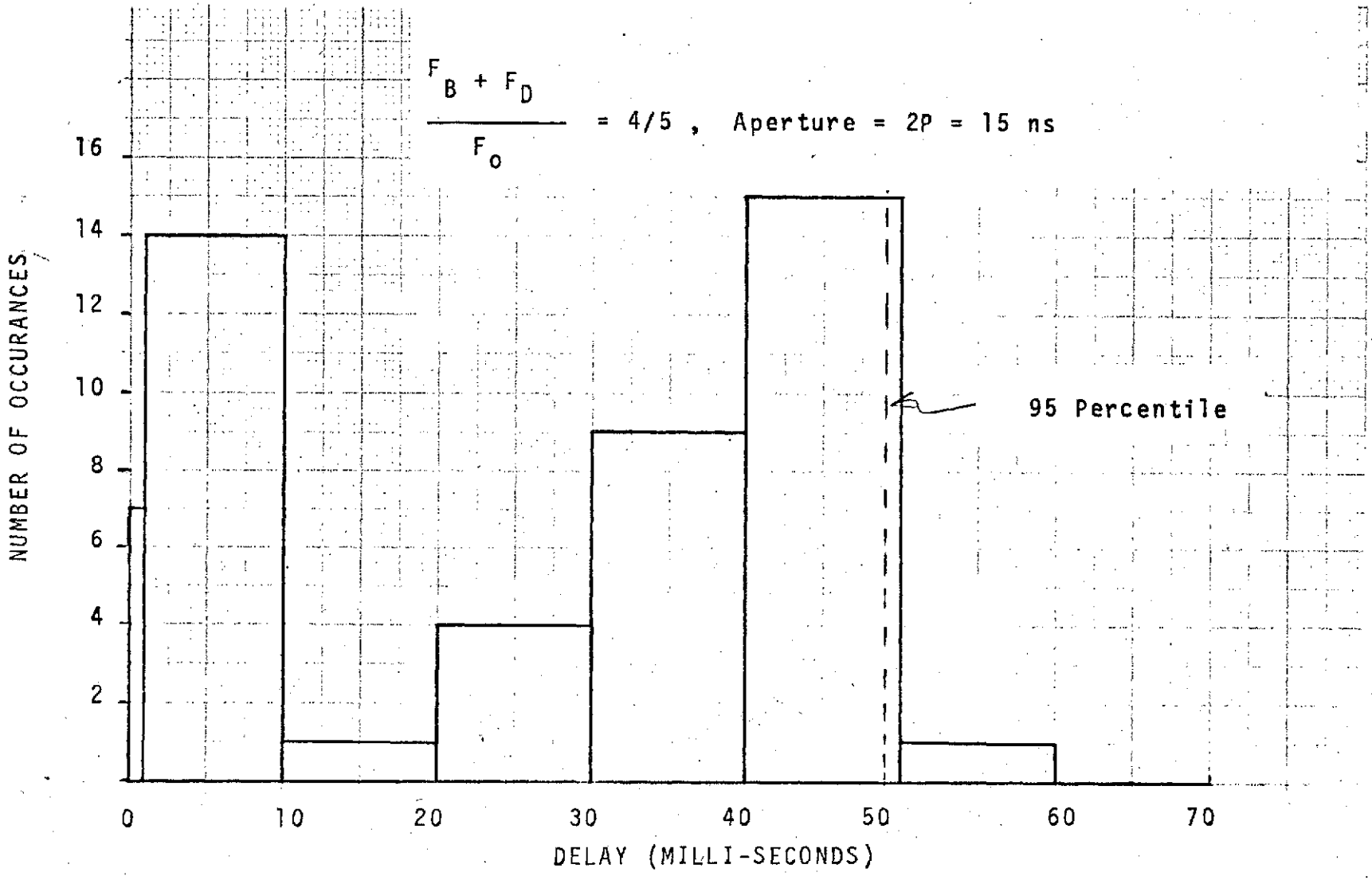


FIGURE 8-5. DISTRIBUTION OF TIME DELAY

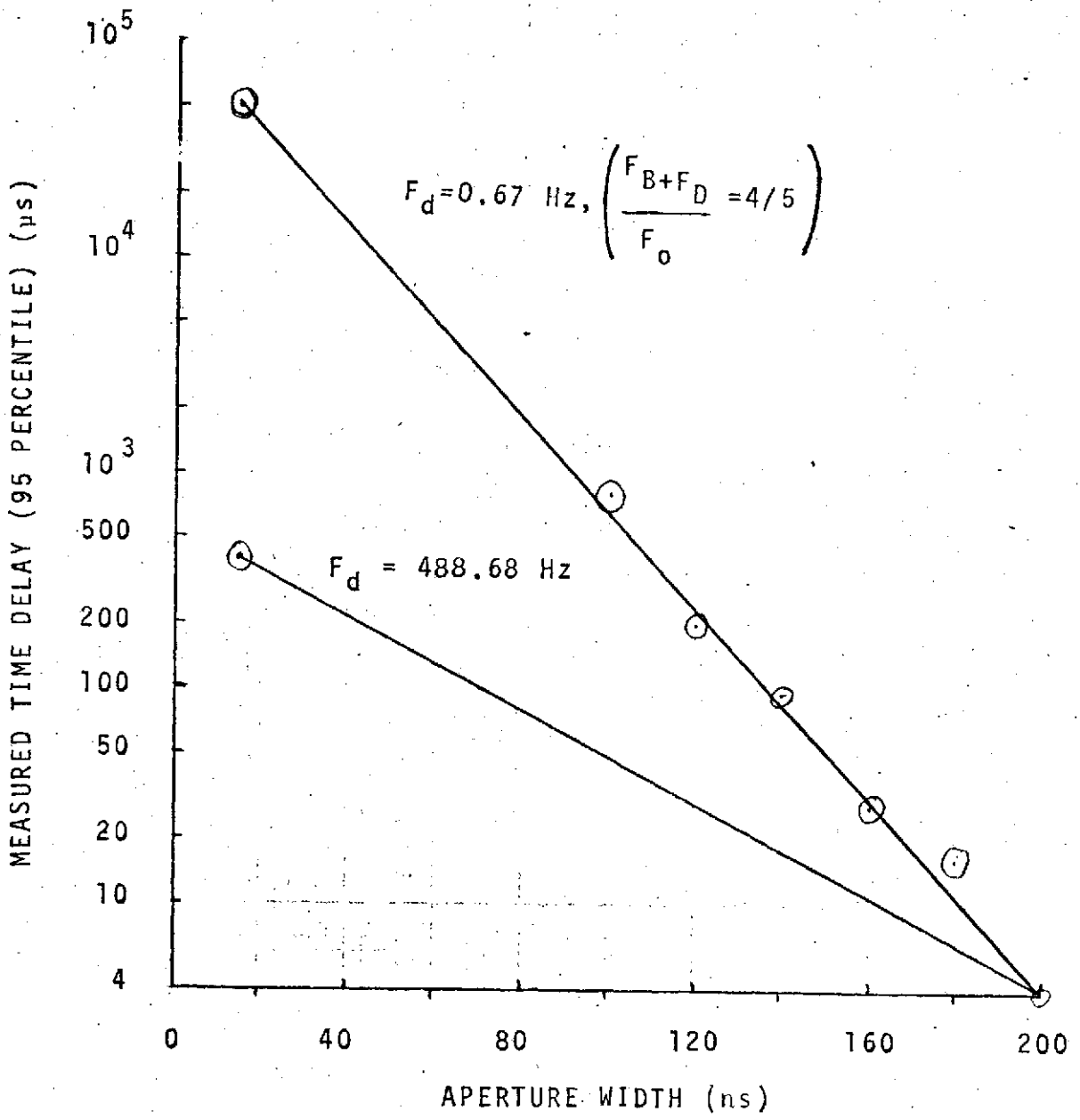


FIGURE 8-6. SENSITIVITY OF TIME DELAY TO COINCIDENCE APERTURE AND DOPPLER OFF-SET

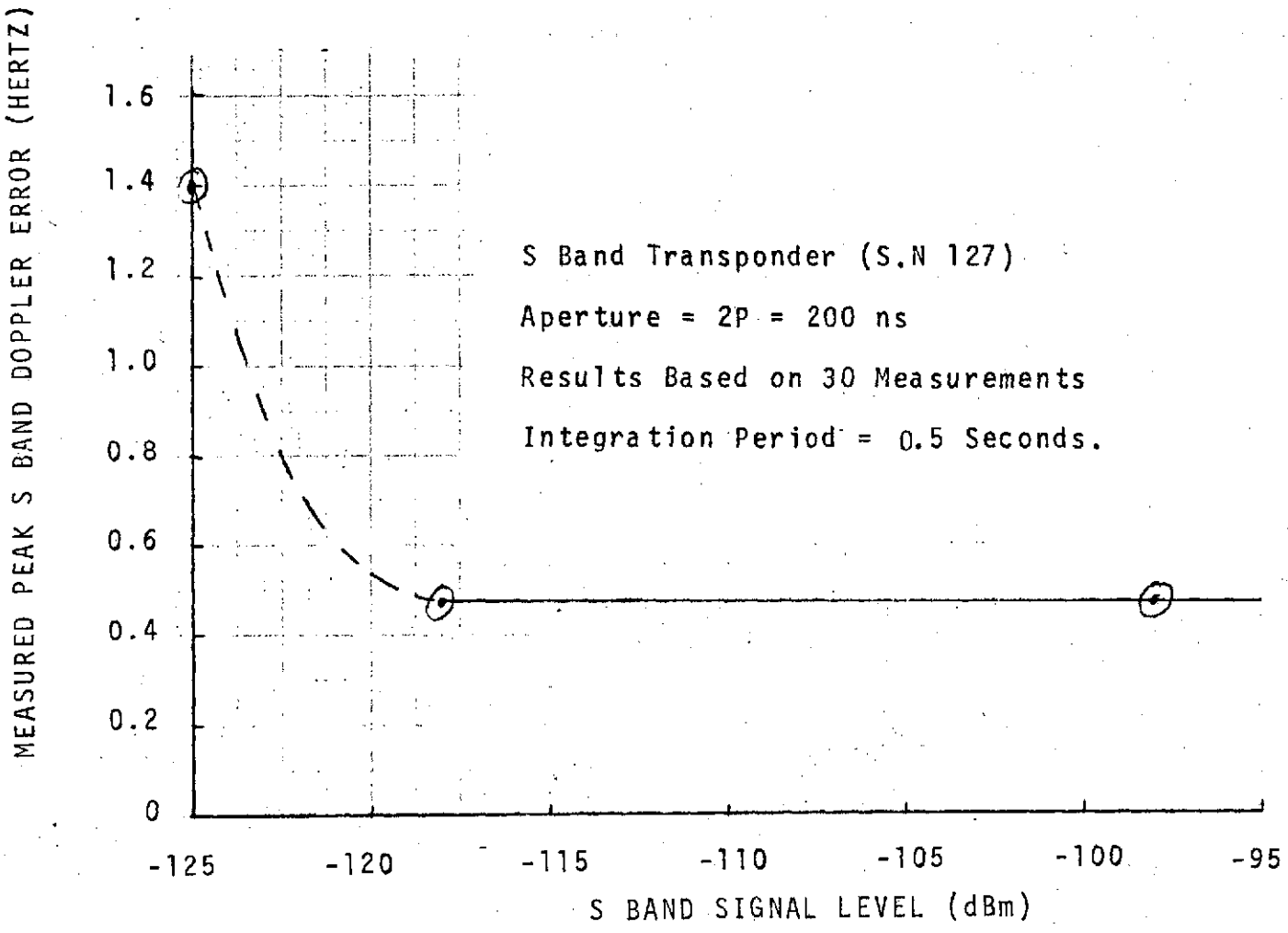


FIGURE 8-7. SENSITIVITY OF EXTRACTOR ERROR TO S BAND SIGNAL LEVEL

would cause a shift from +500 Hz of doppler to -500 Hz in 1 second. Thus, the resonance would not last more than one second and time delays in excess of 300 microseconds would occur only rarely even with aperture widths of 15 ns.

8.2.3 SENSITIVITY TO S-BAND SIGNAL LEVEL

The results of the error sensitivity tests to S-band signal level are shown in Figure 8-7. These results show that the error is constant(primarily due to quantization error at the wide aperture of 200 nanoseconds) at less than 0.5 Hertz as long as the signal level is about -118 dBm or larger. These measurements were made at an integration period of 0.5 seconds. The threshold signal level of the S-band transponder (serial number 127) was determined to be about -128 dBm. This is the signal level at which phase lock was sporadic. Thus the doppler extractor is capable of resolving the S-band doppler offset to an accuracy of 0.5 Hertz with S-band signal levels only 10 dB above the transponder threshold signal level.

8.2.4 SENSITIVITY OF EXTRACTOR ACCURACY TO DOPPLER OFFSET

The extractor accuracy was determined for three different doppler offsets (10,30,000 and 60,000 Hertz) at a constant integration period of 0.5 seconds. These results are presented in Figure 8-8 along with the predicted variation. The predicted variation is $\frac{2P}{\tau}(F_B+F_d)$. Since a 60 KHz variation in F_d varies $F_B + F_d$ by 6%, a 6% variation in the doppler error is expected. The actual variation was observed to be about 30%. These results, however, agree within the statistical accuracy of the tests. With 50 measurements at each doppler offset, the actual error could differ from the measured error by as much as 20%. The curves of Figure 2.6 show that no large deviation from the predicted results is present.

The curves also show that the measured error is less than the predicted error for all doppler offsets. This could

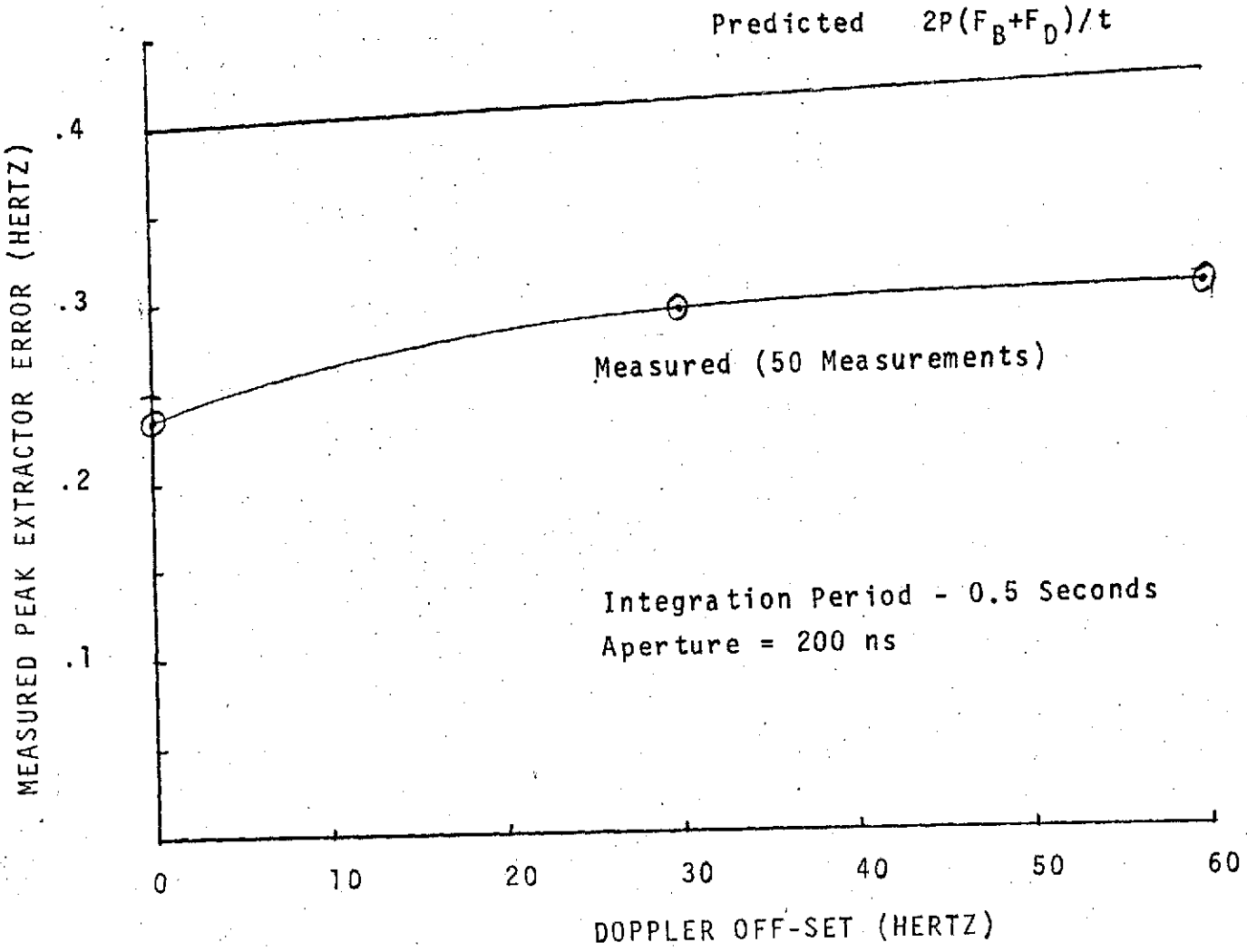


FIGURE 8-8. SENSITIVITY OF EXTRACTOR ERROR TO DOPPLER OFF-SET

be due to an actual coincidence aperture different from the 200 ns assumed in the tests. The aperture results from a tap on a 200 ns delay line and the actual delay was not measured.

8.2.5 SENSITIVITY TO DOPPLER RATES

The accuracy of the doppler extractor was also tested with doppler sweep rates of 4600 Hz/sec. The doppler extractor measured the net doppler shift over a period of 0.5 second in the range of zero doppler. That is, the extractor began counting when the doppler shift was in the range of $\pm$ 10 KHz and was stopped 0.5 seconds later. The Hewlett-Packard computing counter was simultaneously (within the time delay statistics) started and stopped over the same time intervals. The peak averaging time difference between the two counters could have been as high as 11.6 μs. ($\pm$4.8 μs variation for the extractor time interval and $\pm$ 1 μs for the computing counter). At a sweep rate of 4600 Hz/sec and an 11.6 μs time skewness, the peak error caused by the time interval skewness should not exceed 10^{-6} Hz. Thus, the extractor error should not increase with a sweep rate of 4600 Hz/sec.

Based on 50 measurements of doppler, the peak extractor error was 0.409 Hz when compared to the computing counter. The standard deviation was 0.185 Hz. This compares with predicted values of 0.4 Hz peak error and 0.163 Hz for the standard deviation. These predictions are based on an averaging time of 0.5 seconds and a coincidence aperture of 200 ns. Thus, even with the high sweep rates the vernier extractor is able to measure the doppler to within $\pm$ 0.4 Hz peak error over an integration period of 0.5 seconds. This corresponds to a peak cycle count error of $\pm$ 0.2 cycles regardless of the averaging time.

PART III

FLIGHT HARDWARE DESIGN

This part of the report discusses a preliminary flight hardware design of the vernier doppler extractor. This design was in response to a Rockwell International specification for an extractor to interface with STDN and SGLS transponders and extract doppler to an accuracy of 0.3 cycles. Additional extractor specifications and a design approach are discussed. A description of the preliminary design is presented showing both the electrical and mechanical designs. Topics discussed in this part include:

SECTION 9

EXTRACTOR SPECIFICATIONS

9.1 SPECIFICATIONS FOR A FLIGHT MODEL DOPPLER EXTRACTOR

A preliminary design of a flight hardware vernier doppler extractor has been made in response to a Rockwell International specification. The specification calls for an extractor capable of obtaining doppler measurements to an accuracy of approximately 0.3 cycles (9 cm/sec in a half second averaging period) referenced to the S-band frequency. The extractor is required to interface with STDN or SGLS transponder output frequencies. Two output frequencies are specified which could have lowest values of 18.47917 and 19.0625 MHz, respectively. Additional Rockwell specifications which directly affect the doppler extractor performance and design are shown in Tables 9-1, 9-2 and 9-3. These specifications include extractor performance requirements (Table 9-1), extractor interface requirements (Table 9-2) and environmental conditions in which the extractor must operate (Table 9-3).

The extractor is further specified to perform the functions of RF mixing and translation, frequency synthesis, control logic and timing, digital counting, storage, buffering and digital input/output. These functions are to be performed with the following requirements:

a) Receive and select from one of two inputs the RF output signal from the associate energized S-Band receiver from which doppler is to be determined.

b) Receive from an external frequency standard a 4.608 MHz reference signal.

c) Generate, in synchronization with the 4.608 MHz reference, the internal frequencies and timing signals required for the functional operation.

TABLE 9-1

PERFORMANCE REQUIREMENTS

OPERATING RANGE	RANGE RATE: 0 to ± 8230 mtrs/second (± 60 kHz) ACCELERATION: 0 to ± 610 mtrs/second^2 (± 4500 Hz/sec)		
ACCURACY	INTEGRATION INTERVAL (SEC.)	3 SIGMA MEASUREMENT ERROR (CYCLES)	3 SIGMA MEASUREMENT ERROR (HERTZ)
	0.1	0.3	3 Hz
	0.5	0.3	0.6 Hz
	1.0	0.4	0.4 Hz
	2.0	0.5	0.25 Hz
	10.0	2.3	0.23 Hz
	30.0	6.0	0.20 Hz
	60.0	12.0	0.20 Hz
	600.0	120.0	0.20 Hz
	The maximum bias error of the doppler shall not exceed the effect of a 2 Hz drift of the stable reference frequency (at S-band) per day.		
MEASUREMENT TIME CORRELATION	The start time of the doppler and time interval counts shall be synchronized to within 100 microseconds of the initiation of the start interval time discrete. The data output from the doppler extractor shall be the actual time interval specified to an accuracy of 100 nanoseconds. The doppler and interval counter shall start within 1.0 nanoseconds of each other, and shall be outputted within 1.0 nanoseconds of each other.		

TABLE 9-2

INTERFACES

S-BAND TRANSPONDER - EXTRACTOR INTERFACE FREQUENCIES (ZERO DOPPLER)

MODE	S-BAND FREQ.	F_{VCO}
SGLS-LO	1775.733 MHz	18.479166 MHz
SGLS-HI	1831.787 MHz	19.062500 MHz
STDN/TDRS-LO	2041.947 MHz	18.479166 MHz
STDN/TDRS-HI	2106.406 MHz	19.062500 MHz

TRACKING STATION FREQUENCY UNCERTAINITY

	TDRS	STDN	SCF
SHORT TERM (ONE SEC.)	2×10^{-12}	2×10^{-12}	TBD*
LONG TERM (ONE YEAR)	5×10^{-12}	5×10^{-12}	TBD*

* NOTE: THOUGHT TO BE COMPARABLE TO TDRS AND STDN

MASTER TIMING UNIT (MTU)

FREQUENCY 4.608×10^{6} Hz

STABILITY (1 SECOND) 1×10^{-10}

(24 HOURS) 1×10^{-9}

AFTER FULL MTU STABILIZATION

IMPEDANCE

MTU OUTPUT = 75 OHMS PLUS OR MINUS 7 OHM

EXTRACTOR INPUT = 75 OHM PLUS OR MINUS 7 OHM

POWER LEVEL (INPUT TO EXTRACTOR) 6 DBM OR MINUS 3 DB

TABLE 9-3

ENVIRONMENTAL CONDITIONS

Performance shall be within specification under the operational conditions, and subsequent to the nonoperational conditions, given below:

Operational

Temperature: Mounting surface from 35° to 120°F

Pressure: 12 to 18 psia

Humidity: 8 to 100 percent relative

Lightning: In accordance with MF004-002 for indirect effects

Random Vibration (Qualification)

20 - 150 Hz, +6 dB/oct. to 0.09 g^2/Hz

150 - 900 Hz, 0.09 g^2/Hz

900 - 2000 Hz, -9 dB/oct.

Duration, 48 minutes/axis

Random Vibration (Acceptance)

20 - 80 Hz, +3 dB/oct. to 0.067 g^2/Hz

80 - 350 Hz, 0.067 g^2/Hz

350 - 2000 Hz, -3 dB/oct.

Duration, TBD minutes/axis

Acceleration: ± 5 g, all axes

Nonoperational (Packaged)

Temperature: -65 to +150°F

Pressure: 3 to 16 psia

Sand and Dust: Desert and ocean beach area conditions; also suspended dust

Shock: 20 g terminal sawtooth shock pulse of 11 ms duration in all axes.

Other: Sun, rain, hail, snow, ozone, fungus. Detailed requirements are TBD.

d) Provide RF mixing and frequency translation as required to obtain a known bias frequency upon which a known fraction of the S-band doppler shift is impressed.

e) Provide continuous digital counting capability to simultaneously count both the bias frequency plus doppler shift and some multiple of the stable reference frequency. Both counters shall operate for a continuous period of time of not less than 10 minutes before counter recycle and the counting process shall not be disturbed or interrupted by the data read out process. The counter which counts bias frequency plus doppler shift hereafter shall be referred to as the doppler counter and the counter which counts some multiple of the stable reference frequency shall be referred to as the interval counter. The interval counter shall be continuous and have the same type recycle characteristics as the doppler counter.

f) Provide two modes of counter operation:

1. Continuous counting of bias frequency plus doppler and continuous counting of the multiple of the reference stable frequency with independent automatic recycle to zero when either register is full without stopping continuous count.
2. Continuous counting of bias frequency plus doppler and continuous counting of the multiple of the reference stable frequency after the doppler counter has been reset to zero at computer command. The interval counter shall be reset to zero when the doppler counter is reset to zero at computer command.

g) Provide for transfer of the count number from the doppler and interval counters to temporary digital storage upon receipt of an externally computer generated transfer pulse or an internally generated transfer, pulse discrete, without interrupting the continuous doppler and interval count.

h) Provide for generation of the doppler counter transfer pulses at precise intervals of time as commanded in advance by receipt and storage of digital command words from the computer. Measure the required command time interval by counting cycles from a clock synchronized to the external frequency standard input signal.

i) Initiate the start of the time interval measurement upon receipt of a "start interval time" discrete signal from the computer interface.

j) Temporarily store the doppler counter measurements along with any required auxiliary digital measurements in input/output buffers within the extractor.

k) Accept input digital command read out digital data from/to the external computer as specified herein.

l) Accept digital and discrete mode status information from each of the two associated S-band receivers. Adjust mode operation within the extractor to the proper operational mode to match the S-band receiver mode in use. Output the mode status to the computer along with each associate doppler data digital readout. The receiver mode status shall identify SGLS, STDN, or TDRS mode, high or low frequency in use, and VCO coherency condition.

m) Receive and select from one of two inputs the digital signal containing ground station identification data and clock from the associate energized Network Signal Processor (NSP).

n) Temporarily store the inputted eight bits of digital ground station data which shall be updated at a 9 Kbps rate at successive 20 milliseconds time intervals from the network signal processor.

o) Provide for transfer of the eight bits of ground station data to the input/output buffers within the extractor to permit readout of this data to the external computer along with the doppler, time interval, and discretes block of words.

p) Initiate the start time of the transfer of the eight bit ground station data from temporary input storage to the extractor computer input/output buffers as follows:

   1. Monitor the 8-bit input ground station data and the start ΔT discrete signal from the computer as input to logic.
   2. Logic shall initiate data transfer pulse within one millisecond following conclusion of the 8-bit read-in period provided that a start ΔT discrete has been received from the computer.

q) Provide two instrumentation outputs.

r) Perform an end-to-end self-test of all functional paths within the unit upon receipt of a test mode discrete.

s) The extractor shall operate from main DC power in accordance with MF0004-002. The maximum power shall not exceed 10 watts at 28 volts DC main bus. The extractor shall be designed for continuous operation.

SECTION 10

DESIGN APPROACH

10.1 VERNIER DOPPLER EXTRACTOR REQUIREMENT

The transponder output frequencies contain only a fraction of the S-band doppler frequency (less than 1% typical). Thus, to achieve a 0.3 cycle accuracy for the S-band doppler frequency, the extractor must be capable of measuring the transponder output doppler to an accuracy up to 100 times better than 0.3 cycles (i.e., up to 0.003 cycles). Further, if the transponder VCO loop S/N ratio is 10 dB, then VCO phase jitter will contribute about .0015 cycles (3σ) to the total error at the VCO output frequency or .15 cycles referenced to S-band. To maintain a total error of 0.003 cycles on the VCO reference frequency the vernier extractor quantization error must be less than .0026 cycles. The time delays associated with the doppler measurements are not to exceed 100 μs. The selected vernier extractor approach is capable of meeting the accuracy requirement by obtaining a 1 MHz bias frequency containing the partial doppler, and using "AND" gate apertures of 2.6 nanoseconds. However, the time delays associated with this narrow aperture would result in measurement delays of as much as 714 microseconds. This is obtained from the relationship between doppler accuracy and time delay discussed in Part I. That is:

$$\epsilon_N = \frac{2F_{dmax} + \frac{1}{td_{max}}}{F_o} = \leq .0026 \text{ cycles}$$

where ϵ_N is the cycle count error ($\leq$.0026 cycles), $F_{d\ max}$ is the maximum doppler shift on the bias frequency (600 Hz maximum), $t_{d\ max}$ is the maximum time delay, and F_o is the clock reference frequency.

Re-arranging the above equation and using a clock reference frequency of 1 MHz results in the following relationship.

$$t_{d\ max} = \frac{1}{\epsilon_N F_o - 2 F_d}$$

or

$$t_{d\ max} = \frac{1}{1400} \leq 714\ \mu s$$

It is possible to obtain the required resolution within the required time delay limits by operating the extractor with higher clock and bias frequencies and shorter coincidence apertures. However, from the above expression, the clock frequency (and hence the bias frequency) would need to have a value of about 4.3 MHz, and the coincidence aperture would need to be 0.6 nanoseconds. These requirements would place extreme demands on circuit power, complexity and reliability for a flight hardware extractor. To relax the requirements for high clock and bias frequencies and short coincidence apertures, the transponder doppler reference frequency could be multiplied to achieve a doppler signal closer to the true S band doppler. With such a multiplied doppler reference, the extractor resolution (quantization) requirements could be increased above the required 0.0026 cycles, resulting in less time delay for the same clock frequency. For example, if the doppler frequency were multiplied by 10, then the maximum time delay would be decreased by 10. That is:

$$t_{dmax} = \frac{1}{(.0026)(10)(1 \times 10^6\ Hz) - 2(10)600} \leq 71\ \mu s$$

for a 1 MHz clock frequency.

This delay assumes that the bias frequency is carefully chosen very close to the clock frequency. In practical systems with small integer frequency multipliers and dividers it is not always possible to select the optimum bias frequency. Thus, additional doppler multiplication may be required to simultaneously obtain the resolution and time delay requirements.

In addition to operating with a preferred bias frequency no greater than about 1 MHz, the flight hardware vernier extractor should operate with coincidence apertures that do not impose severe hardware constraints on the coincidence circuits.

Pulse widths of about 5 to 10 nanoseconds, which result in coincidence apertures of 10 to 20 nanoseconds, would not be difficult to obtain for a high reliability low power extractor. A pulse width of 5 nanoseconds (aperture = 10 nanoseconds) would limit the vernier extractor resolution to about 0.01 cycles with a 1 MHz bias frequency. These restrictions would thus require a doppler multiplication of about 4 to achieve the desired S-band doppler resolution of 0.26 cycles.

10.2 DESIGN DESCRIPTION

A response to the Rockweell specification is shown by the general circuit configuration of Figure 10-1. The objectives of this circuit will be to obtain a suitable injection frequency which will allow high multiplication and obtain the multiplied doppler on approximately a 1 MHz bias. If the vernier extractor is to obtain the required doppler resolution of about 0.2 cycles (so that the RMS error $\leq$ 0.3 cycles) with pulse widths of 10 ns or more, then the required multiplication must be at least the following:

$$\epsilon F_D = \frac{110.5}{K} \cdot (2PF_B) \leq 0.2 \text{ cycles}$$

or $K \geq 1.105P$ where P is in nanoseconds and F_B = 1 MHz.

with P = 10 ns

$K \geq 11$

To obtain high multiplication (of 11 or more) the frequency output of the first mixer should be nearly the same regardless of which VCO input frequency is selected, to allow the multiplying loop to easily acquire the signals with narrow bandwidths. A system which meets the desired goals and can obtain doppler resolutions of 0.2 Hz or better with $\approx$1 MHz counters is shown in Figure 10.2 A variable

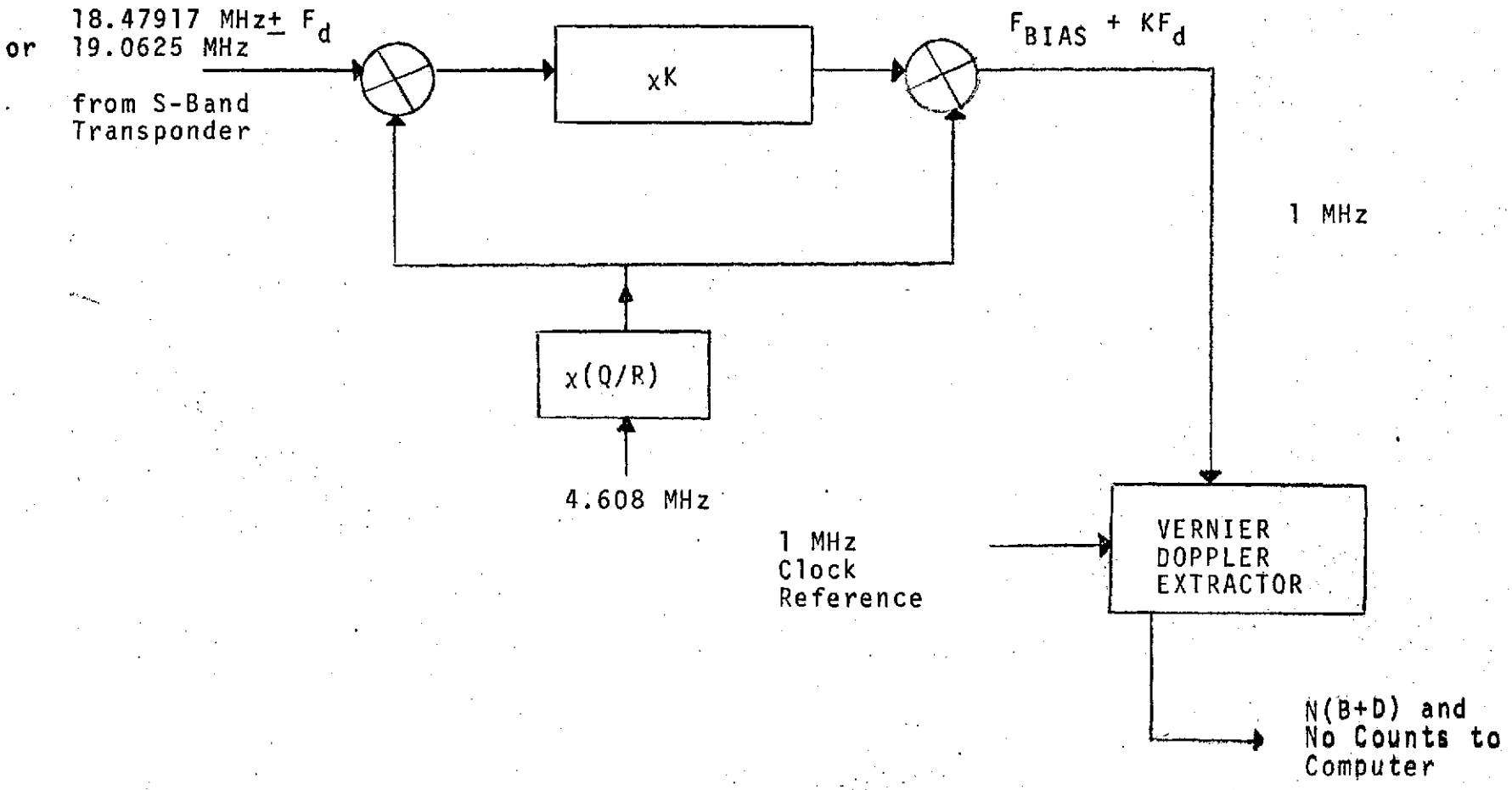


FIGURE 10-1 PROPOSED DOPPLER EXTRACTION - (GENERAL BLOCK DIAGRAM)

multiplier is used in the circuit to obtain nearly identical multiplied output frequencies. Thus, the multiplier VCO loop can use a very stable VXCO allowing the use of relatively narrow loop bandwidths. The bias frequency output to the vernier extractor is approximately 1.4 MHz containing approximately 1/2 to 3/4 of the full S-band doppler. To obtain the required resolution of 0.2 Hz, the vernier extractor must provide an additional resolution improvement factor of at least 9. From the accuracy/time delay trade-offs of Part I, M must be at least 9, so that the ratio N/M (the ratio of bias plus doppler to clock frequencies) cannot be less than 8/9. Thus, the clock frequency must be no more than 9/8 of the minimum bias plus doppler frequency (9/8 of 1.357 = 1.515 MHz) if the clock reference frequency is chosen greater than the bias frequency. If the clock reference is chosen below the bias plus doppler frequency, it must be no smaller than 8/9 of the maximum bias plus doppler frequency. That is, the clock frequency must be greater than or equal to 1.286 MHz (8/9 of 1.447 MHz).

In the system of Figure 10-2, a clock reference frequency greater than the bias frequency was chosen since a convenient ratio of the available clock frequency could be obtained which nearly meets the restrictions described above. The chosen clock reference frequency of 1.536 MHz is slightly above the maximum allowed frequency of 1.515 MHz, however, this simply means that the extractor error will be slightly more than the desired 0.2 cycles (0.26 cycles is the maximum allowable quanitzation error). With the selected clock frequency, the following paragraphs will show that the extractor quantization error will be no greater than 0.216 cycles. Thus, selection of a more desirable clock reference (for improved accuracy) is probably not worth the added circuitry required to generate the more desirable frequency.

With a clock reference frequency of 1.536 MHz, the ratio of the bias plus doppler to clock frequency (N/M) will vary over the limits from 0.87695 to 0.94206. In terms of the

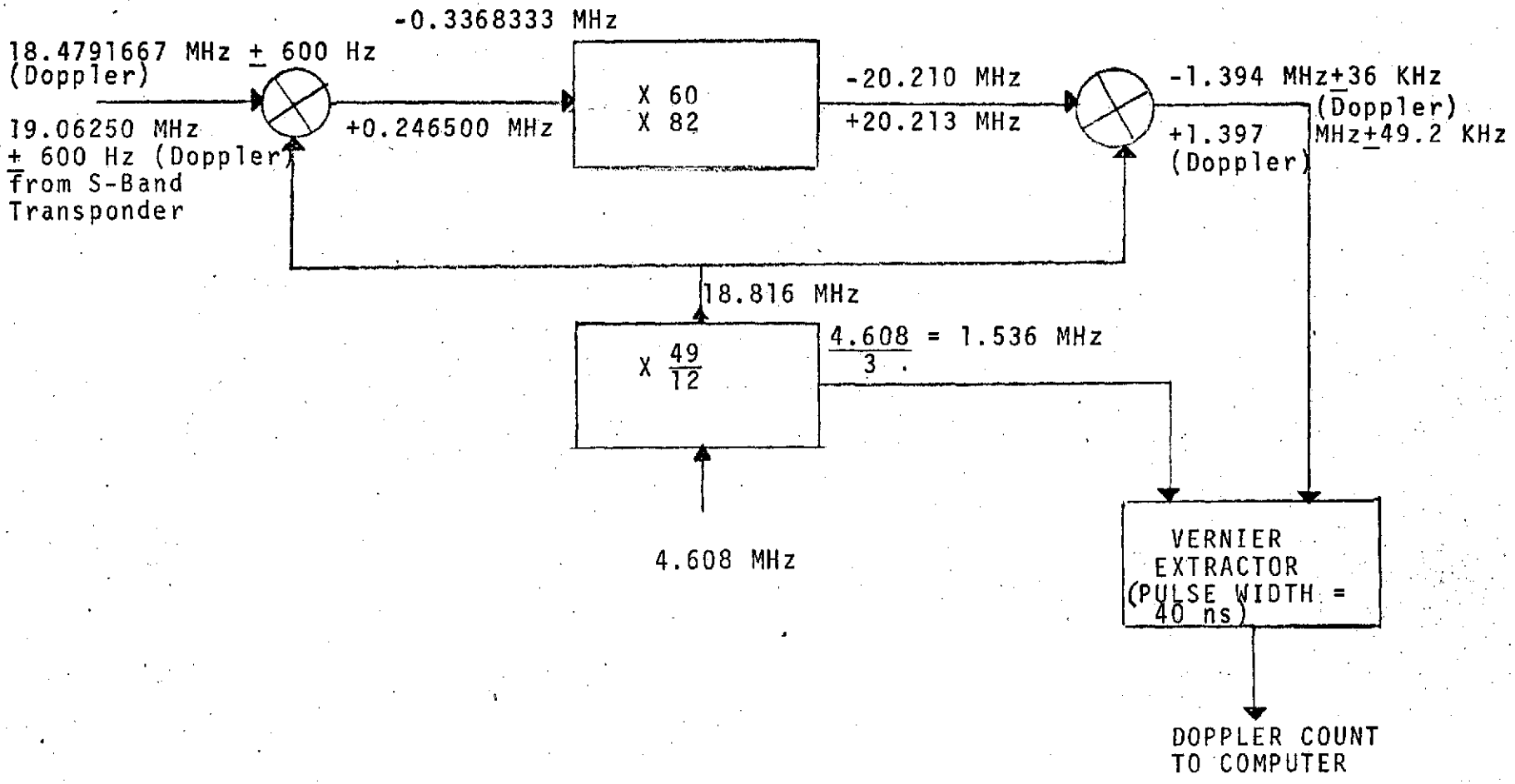


FIGURE 10-2 PROPOSED DOPPLER EXTRACTOR (DETAILED BLOCK DIAGRAM)

ratio of the smallest integers for N and M, the ratio N/M will not exceed the range from 8/9 to 16/17. Thus, N has a minimum value of 8, and the minimum pulse width in the vernier extractor (to allow short time delays) must be 40.7 ns ($P \geq T_0/2N$, T_0=651ns and N=8). Since M ranges from 9 to 17, the maximum possible delay will be less than 11 μs (MT_0).

10.3 DOPPLER EXTRACTION ACCURACY

Selecting a pulse width of 41 ns, the quantization errors of Table 10-1 will result. It is seen that the maximum quantization error will not exceed 0.216 cycles. The combined quantization error and noise induced jitter error is also shown in the table. This total error will be no greater than 0.27 cycles which is below the required maximum value of 0.3 cycles. The error resulting from the clock oscillator drift is not included in the table since this error depends on the selected clock oscillator. If the clock is only stable to one part in 10^{10}, the maximum oscillator drift error (3σ) could be as high as 0.6 cycles in a one second averaging period (0.6 Hz for all averaging periods). This error alone would exceed the specifications, so that it is assumed that either the clock stability error is not part of the total error specification or a better oscillator will be selected. An oscillator stability of about $2X10^{-11}$ would be required to obtain a maximum (3σ) root mean squared error of 0.3 cycles or less.

TABLE 10-1

MAXIMUM ONE WAY DOPPLER EXTRACTOR ERRORS

INPUT FREQUENCY FROM S-BAND TRANSPONDER	RATIO OF S-BAND DOPPLER TO COUNTED DOPPLER (R/K)	RESULTANT PEAK QUANTIZATION ERROR FROM COMPUTER DOPPLER ($\epsilon = \pm 2P(F_B+F_D)\frac{R}{K}$*)	MAXIMUM NOISE INDUCED JITTER ERROR (S/N = 10 dB)	COMBINED ROOT SUM SQUARED ERROR
18.479167 MHz	$\frac{110.5}{60} \leq 1.842$	$\leq$0.216 Cycles	$\leq$0.158 Cycles	$\leq$0.268 Cycles
19.0625 MHz	$\frac{110.5}{82} \leq 1.348$	$\leq$0.160 Cycles	$\leq$0.158 Cycles	$\leq$0.225 Cycles

*P=41 ns (82 ns APERTURE)

SECTION 11

PRELIMINARY DESIGN

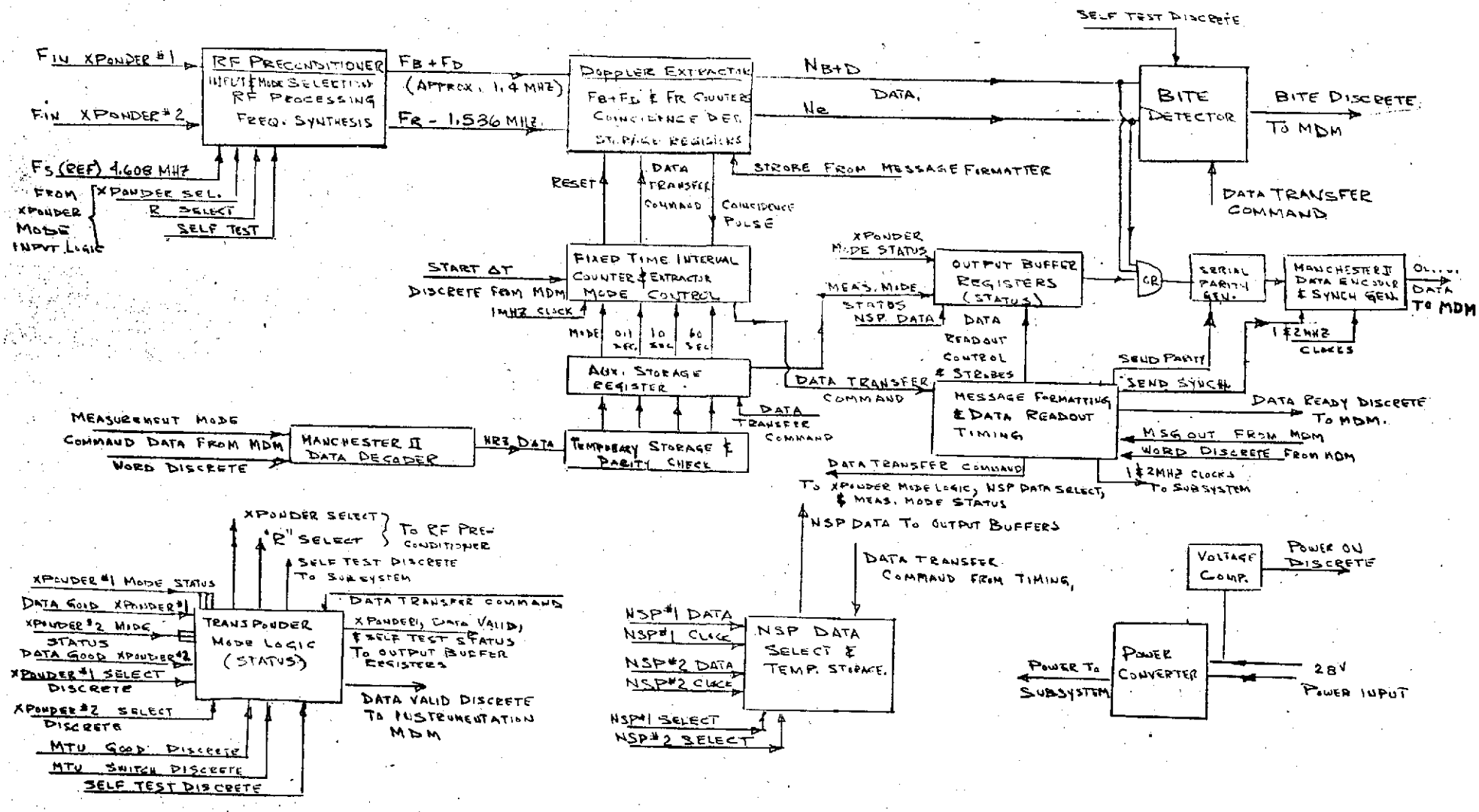
11.1 ELECTRICAL DESIGN

The doppler extractor illustrated in Figure 11-1 contains the circuitry necessary to perform the following functions:

a. RF preconditioning and frequency synthesis
b. Doppler extraction
c. Control and output data formatting

The RF preconditioner selects the appropriate transponder VCO signal upon command of the transponder mode logic. It provides the appropriate frequency translation and multiplication required to produce the bias and scaled doppler frequency necessary to meet the specifications as outlined in the previous sections. The multiplication ratio is modified to produce the desired doppler frequency scale factor for the various transponder modes. In addition, the unit derives the reference frequency for the doppler extractor and the injection frequency required to perform the end-to-end self test function.

The doppler extractor utilizes the coincidence detection technique developed by RCA. This technique has the advantage in that it achieves the required precision at relatively low counting rates (approximately 1.54 MHz). The doppler extractor circuitry consists of the doppler plus bias frequency and reference frequency counters, associated parallel to serial shift registers, and coincidence detector. The fixed time interval counter provides the selectable time intervals of 0.1 second, 10 seconds, and 60 seconds, required in the fixed time interval readout mode. The extractor mode logic provides the necessary configuration modification required, in order that the extractor may operate in either the Computer Command or the Fixed Time Interval mode.



11-2

S-11

FIGURE 11-1 SPACE SHUTTLE DOPPLER EXTRACTOR BLOCK DIAGRAM

The transponder mode logic accepts the transponder #1 and #2 mode discretes which define the transponder frequency and associated receiver circuit ratio "R". The transponder #1 Data Good and transponder #2 Data Good discretes indicate the phase coherency of the phase-lock loop receivers. The transponder select discretes #1 and #2 selects the associated transponder mode status and data good discrete to control the RF preconditioner, and provides the mode and status conditions to the output buffer registers. The MTU good discrete and the selected Data Good discrete are combined to provide a Data Valid discrete to the instrumentation MDM. The MTU Oscillator Switch discrete is strobed as a status condition to the serial data output buffers. The self test discrete input to the transponder mode logic places the system in the self test mode, and the status is indicated to the output buffers for transmission to the MDM interface.

Selection of the NSP #1 or the NSP #2 ground station data and associated clocks is accomplished by the presence of either the NSP #1 or NSP #2 select discretes in the NSP select logic. The ground station data is temporarily stored for subsequent readout to the MDM interface.

The measurement mode command data is demodulated in the Manchester II data decoder and transferred to the auxiliary storage register after a parity check is performed. The command data indicates whether the measurement is to be made in the Computer Command Mode or in the Fixed Time Interval Mode. The Fixed Time Interval Mode command indicates the integration period.

In the Computer Command Mode, the data is read out at time intervals determined by the computer. The Start $\Delta\tau$ discrete from the MDM initiates the readout cycle. The first doppler extractor coincidence pulse after the receipt of the Start $\Delta\tau$ transfers the data in the FB+FD and FR counters to the parallel to serial shift register for temporary storage and initiates the data transfer cycle. The maximum delay

of the first coincidence pulse with respect to the Start $\Delta\tau$ discrete is 11 microseconds.

Upon receipt of the data transfer command, the message formatting and data readout timing logic initiates the transfer of the transponder and measurement mode status and the selected NSP data to the output buffer registers. Transfer of the status data to the output buffers results in a data ready discrete. Receipt of the MSG out and word discretes initiate the transfer of data to the MDM. Upon receipt of the word discrete, the message formatter initiates the generation of the Manchester II Synch. pattern and the necessary strobes to transfer the extractor mode and status from the output buffers to the MDM at a 1 MHz rate. The data word is encoded in the Manchester II data format, and the 1 bit parity is generated by the serial parity generator at the appropriate time. This results in a 20 bit data word.

Subsequent word discretes transfer the NSP ground station data and the contents of the doppler FB+FD and FR counters in a similar fashion.

In the Fixed Time Interval Mode, the data is repeatedly read out at the specified time intervals. The Start $\Delta\tau$ discrete resets the doppler extractor fixed time interval counter and the FB+FD and FR counters. The first coincidence pulse following the Start $\Delta\tau$ discrete initiates the fixed time interval counter.

At the selected time interval, the fixed time interval counter initiates the mode logic readout cycle. The first extractor coincidence pulse following the termination of the integration period transfers the data in the FB+FD and FR counters to the parallel to serial shift registers for temporary storage, and indicates the data transfer cycle. The data transfer cycle is the same as in the Computer Command Mode. The fixed time interval counter continues to initiate the readout cycle until the mode is changed.

The computer has the capability of changing the doppler extractor measurement mode at any time except when the FB+FD and FR registers are being updated by an internally generated read command. In this condition, the mode change is delayed by 100 nanoseconds.

The presence of the self test discrete places the extractor in the self test mode. The measurement mode logic is placed in the Fixed Time Interval Mode with an integration period of 1 second, and the BITE detector is activated. A synthesized frequency is injected at the input to the RF preconditioner to simulate a transponder signal. Data is read out to the MDM in the normal manner, and the mode status word indicates that the system is in the self test mode. The BITE detector provides the necessary logic to perform a GO/NO-GO test and provides a BITE discrete to the MDM interface.

The doppler extractor contains a power converter which derives the required voltages from the 28 volt supply. A voltage comparator provides an ON/OFF discrete to the instrumentation MDM and a Power ON discrete to the MDM when the input voltage exceeds 24 volts.

11.1.1 RF PRECONDITIONER

The RF preconditioner provides the necessary signal processing for the doppler circuitry. It translates the transponder VCO RF signal to a suitable frequency range which makes the use of low power CMOS logic in the extractor design feasible. The RF signal is multiplied so that the doppler scale factor approaches its S-band value and reduces the resolution requirements of the extractor logic. To perform the necessary translations, a local oscillator signal is generated by frequency synthesis from a frequency standard. The reference clock signal for the doppler extractor is also derived from the same source. A self test feature is included. Figure 11-2 is a block diagram of the RF preconditioner.

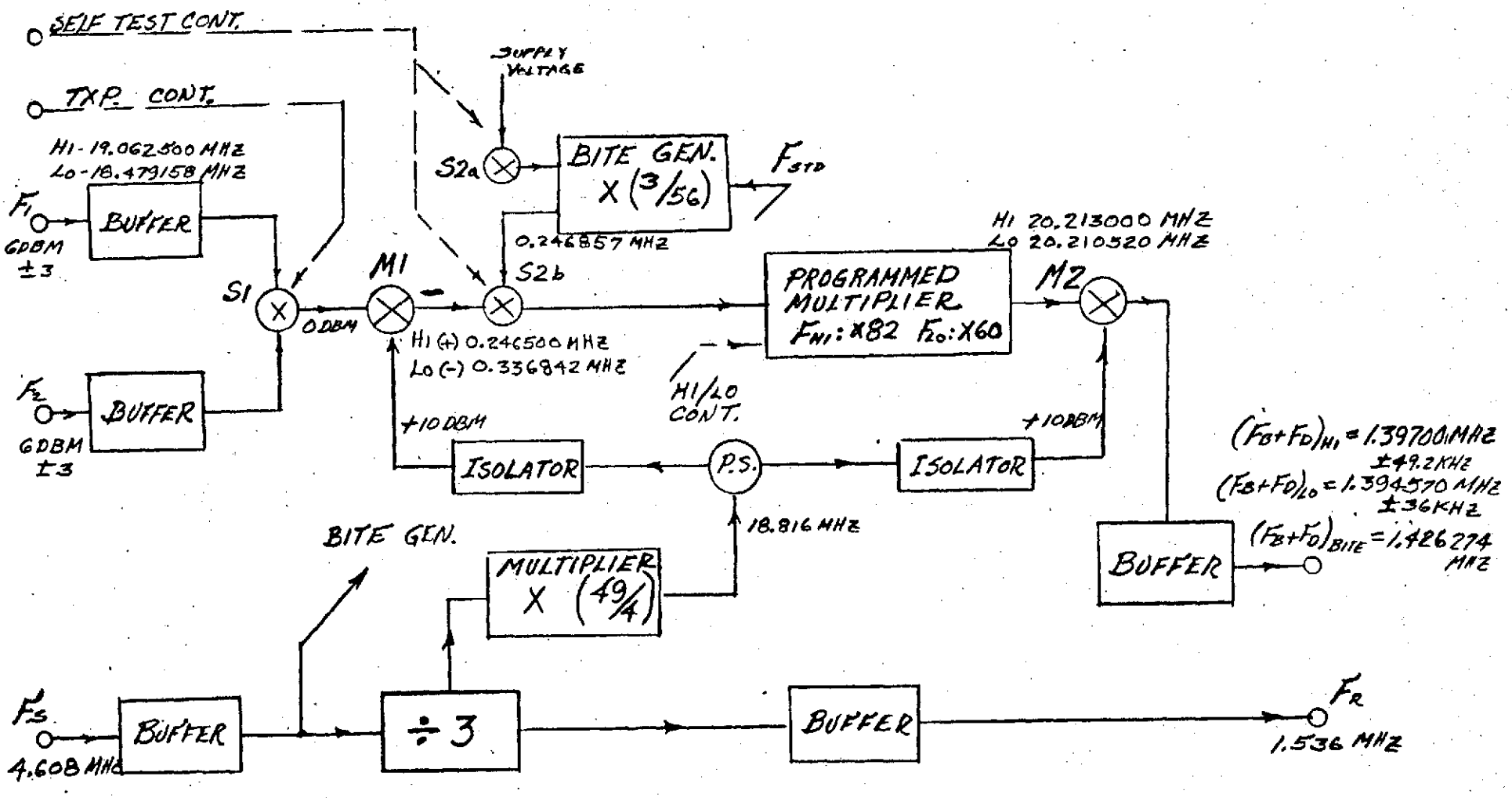


FIGURE 11-2. RF PRECONDITIONER

As shown in the Figure 11-2 the RF input signals from the transponders are buffered prior to the first translation. Selection is accomplished by a switch, S1, which is under control of the Transponder Mode Logic. The first translation with mixer, M1, develops a down-conversion. Following this conversion, the signal frequency is multiplied by a programmable multiplier. After this process, the signal is down-converted again, and provided as a buffered output signal to the doppler extractor unit. Both conversions are developed by injections from a common local oscillator with adequate isolation between mixers. The local oscillator frequency is established by frequency synthesis related to a reference standard.

The doppler extractor reference clock signal is also derived from this standard and provided as a buffered output to the extractor.

A self test signal (normally disabled) is provided by the BITE generator which is synthesized from the reference standard. When the Self Test Mode is initiated, a switch S2, immediately following the first mixer, M1, interrupts the normal signal path. This test checks the operational integrity of all the networks, except for the first mixer and input buffers which are regarded as reliable circuits. The test has been implemented in this manner and provides the most cost-effective approach.

When, for example, the transponder mode logic selects the TDRS/STDN signals, the first translation converts the high signal to HI (+) 0.246500 MHz and the low signal to LO (-) 0.336842 MHz (the negative sign indicates a sideband inversion). The programmable multiplier multiplies these frequencies by a factor of 82 or 60 respectively, depending on whether a HI or a LO RF signal is being processed. The resulting frequencies at the input to the second mixer are:

HI	20.213000 MHz
LO	20.210520 MHz

After the second conversion, the output signals have the following frequencies:

$$(F_B + F_D)_{HI} = 1.397000 \text{ MHz } (+)$$

$$\pm 49.2 \text{ kHz}$$

and

$$(F_B + F_D)_{LO} = 1.394570 \text{ MHz } (-)$$

$$\pm 36 \text{ kHz}$$

The designation, F_B, indicates the bias frequency which develops in each instance in the presence of zero doppler. To positive and negative deviations indicate the values of the respective multiplied dopplers, F_D.

The BITE test signal of 0.246857 MHz is synthesized from the 4.608 MHz reference. The unit is placed in the HI mode, and the above signal is injected into the programmable multiplier. The resultant BITE test signal is:

$$(F_B + F_D) \text{ BITE} = 1.426274 \text{ MHz}$$

The above design utilizes a single injection frequency for down and up-conversion and results in a relatively narrow bandwidth programmable multiplier.

11.1.1.1 Input Selector Buffers and Mixers

The input buffers are used to isolate one RF channel from the other, and provide the required attenuation to develop a signal level of 0 dBm at the mixer. The presence of the synthesized local oscillator at either RF port is significantly reduced to acceptable levels.

Output buffering is also provided for the signals to the extractor which include (FB+FD), the bias-doppler signal, and FR, the reference clock signal. In the latter instance, special precautions are taken to ensure that operations in the

extractor will not be reflected as virtual in-band components with recirculation in the multiplier chain.

The choice for the mixer networks in the present application favors a conventional ring-diode arrangement, using Schottky-barrier type diodes. Typical operation prescribes an oscillator injection of +10 dBm to ensure adequate linearity when related to the signal level of 0 dBm. Variations of ± 3 dB for the RF signal are of little consequence since the IF signal is developed well above the threshold of a logical conversion in a digitally controlled phase-locked loop, corresponding to the 82/60 multiplier chain.

11.1.1.2 Programmable Multiplier

Following the low pass filter, the translated signal is limited, and frequency multiplication is accomplished by the programmable multiplier. In one mode, conforming to the conditions that the HI signal is selected or the self test mode is initiated, the multiplier network operates with a factor 82. In its other mode, when the LO signal is selected, it operates with a factor, 60.

Figure 11-3 shows a block diagram of the programmable multiplier which is devised as a phase lock loop. The phase lock loop consists of a phase-frequency detector, loop filter, VCO, a programmable divide-by-N counter, and a divide-by-2 prescaler.

The phase-frequency discriminator alleviates the need for acquisition circuitry. The bandwidth of the loop is approximately 5 KHz and therefore, the multiplier does not impair the overall system accuracy.

The VCO signal, which operates nominally at 20.213 MHz, would normally include undesirable modulation sidebands corresponding to the input signal to the phase discriminator. These sidebands are very effectively eliminated by including two resonant traps.

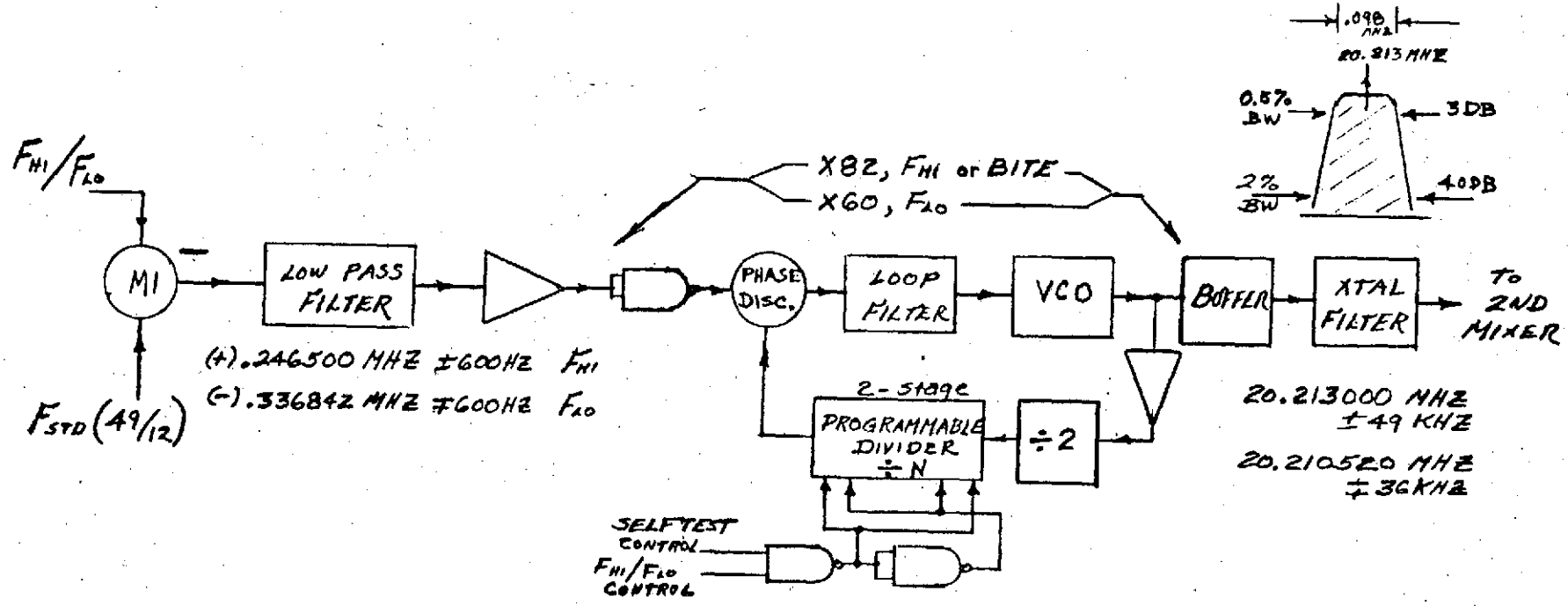


FIGURE 11-3. PROGRAMMABLE MULTIPLIER

11.1.1.5 Bite Generator

The self test feature of the preconditioner provides an equivalent 1st IF signal which is normally disabled by switch, S2, as previously described. This signal is synthesized from the reference standard by the following relationship.

$$F_{BITE} = F_S \left(\frac{3}{56}\right)$$

$$F_{BITE} = 0.246857 \text{ MHz}$$

The divide-by-56 operation is implemented by a digital divider and a conventional x3 multiplier.

11.1.2 DOPPLER EXTRACTOR CIRCUITRY

The doppler extractor circuitry counts cycles of the analog doppler-plus bias (F_{B+D}) and reference (F_R) signals from the RF preconditioner in such a way as to permit accurate recovery of doppler information from the analog signals. The resulting counts (N_{B+D} and N_R) are held in buffer registers for insertion into the output data stream. The spacecraft computer operates on the doppler and reference counts to recover the desired doppler shift information.

11.1.2.1 Coincidence Detector

The coincidence detector accepts the analog signals from the RF preprocessor and outputs a pulse whenever the zero-crossings of the two signals are coincident within a predetermined resolution or coincidence aperture. This pulse can then be used to start and stop the doppler and reference counters at or near the zero crossings of the respective input signals. In this way, the quantization error in the N_{B+D} and N_R counts is reduced to the resolution of the coincidence detector.

It was shown in Section 10 that a coincidence aperture of 41 nanoseconds is required to meet the accuracy and delay requirements of the specification. This aperture must be

The multiplier is terminated in a bandpass crystal filter with a passband of about 0.5%. This assures that the doppler signal with full deviation for both channel selections will be faithfully transferred to the 2nd mixer. The corresponding band limits for the filter are:

20.262200 MHz
20.164200 MHz

The filter is also characterized by a 40 dB rejection bandwidth of less than 2%, a condition which virtually eliminates all reference-rate sideband components.

11.1.1.3 Extractor Reference Clock

The extractor reference clock signal is generated very simply by dividing the reference standard frequency by three. Thus, $F_R = F_S/3 = 1.536$ MHz.

This signal is supplied as an output to the extractor via several stages of isolation.

11.1.1.4 Local Oscillator

The local oscillator signal is developed at 18.816 MHz and is derived by the following rational operations, relating to the reference standard:

$$F_{LO} = \left(\frac{F_S}{3}\right) \cdot \left(\frac{1}{4}\right) \cdot (49)$$

Since the first factor is also developed as the extractor reference clock, the latter signal is made common to the synthesis chain for the LO. This process is also implemented by TTL logic, and after division by 4, the fixed multiplicative factor, 49, is evolved in a manner similar to that used for the programmable multiplier with a PLL. The LO signal, however, is developed as a single spectral line, so that the terminating crystal filter is designed with a very narrow bandwidth. Otherwise, the PLL with the phase-frequency digital discriminator and a fixed divide-by-49 feedback loop operating with a reference signal of 384 KHz is quite similar.

maintained within a few nanoseconds under all conditions.

Figure 11-4 is a functional diagram of the coincidence detector. Two high-speed comparators square up the analog signals. The comparator outputs drive the doppler and reference counters, and also trigger two one-shots on negative transitions. The one-shots produce precise output pulses. Coincidence is declared when the two pulses coincide, setting the output flip-flop. The output flip-flop is reset on the positive transition of the reference signal. In this way, a coincidence pulse is produced whenever the negative zero-crossings of the input signals are within the coincidence aperture. The output pulse width is one-half of the F_R period and is readily handled by the mode control logic.

High-speed logic is required in the coincidence detector to insure that component and temperature variations in the logic propagation delays do not produce a coincidence aperture outside acceptable limits. Logic rise time must be fast compared to the coincidence aperture so that the aperture is not disturbed by threshold variations.

Worst-case analysis has revealed that ECL logic is required to meet the above standards. ECL comparators and ECL 10,000 series devices are proposed. The ECL 10,000-series has relatively low power dissipation, 2 nanosecond rise time, and less than 0.2 nano second variation in propagation delay (per gate) over the specified ambient temperature range.

The precision one-shots are implemented using the standard ECL delay-line technique. Availability of precision delay lines with 60 ppm/°C temperature coefficients make this approach feasible. The delay lines will contribute less than 0.5 nanosecond variation to the coincidence aperture over the specified temperature range. Coupled with the propagation delay and threshold characteristics of the ECL 10,000 logic, this guarantees that the aperture can be held within a few nanoseconds of its nominal value under worst-case conditions.

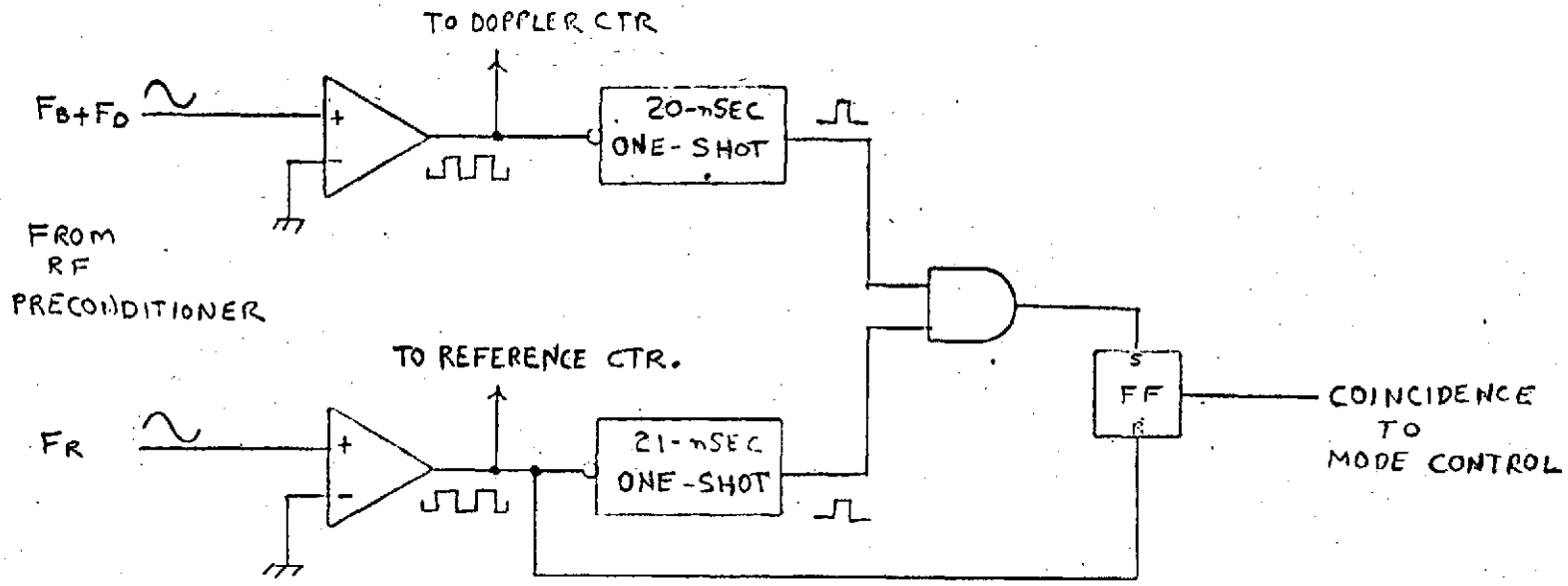


FIGURE 11-4. COINCIDENCE DETECTOR

The ECL logic, with its inherently low output impedance, readily drives the delay lines (which have nominal impedances on the order of 100 ohms).

The width of the coincidence output pulse is approximately 325 nanoseconds with a 1.536 MHz F_R. This pulse width is sufficient to operate TTL logic or CMOS logic operated at 12 volts.

11.1.2.2 Doppler and Reference Counters and Data Storage

Figure 11-5 depicts the counting and data storage arrangement for the doppler and reference frequencies. Square wave signals from the coincidence detector drive two 32-stage synchronous counters. This counter capacity will result in an overflow period in excess of 46 minutes.

The counters increment on the positive transition of the input signals. A strobe is generated in the mode control logic corresponding to the second half-cycle of the input signals. This strobe will operate the parallel/serial control on the parallel to serial shift registers, causing the counter results to be stored in these registers. Circuit parameters are adjusted to guarantee that the storage registers are latched before the counter outputs change due to subsequent zero crossings.

The message formatter circuit will access the counter data in the form of four 16-bit serial words, as shown in Figure 11-5. The message formatter will produce four bursts of 1 MHz clock, 16 cycles per burst. A word selector in the formatter circuit will insert the desired word into the output data stream, while the remaining registers will simply recirculate. In this way, the counter data is held in the parallel/serial registers until it is inserted in the output data stream.

The timing arrangement described above permits nearly a full cycle (651 nanoseconds at the 1.536 MHz reference frequency) to elapse before the data storage registers latch the counter outputs. This represents the minimum acceptable worst-

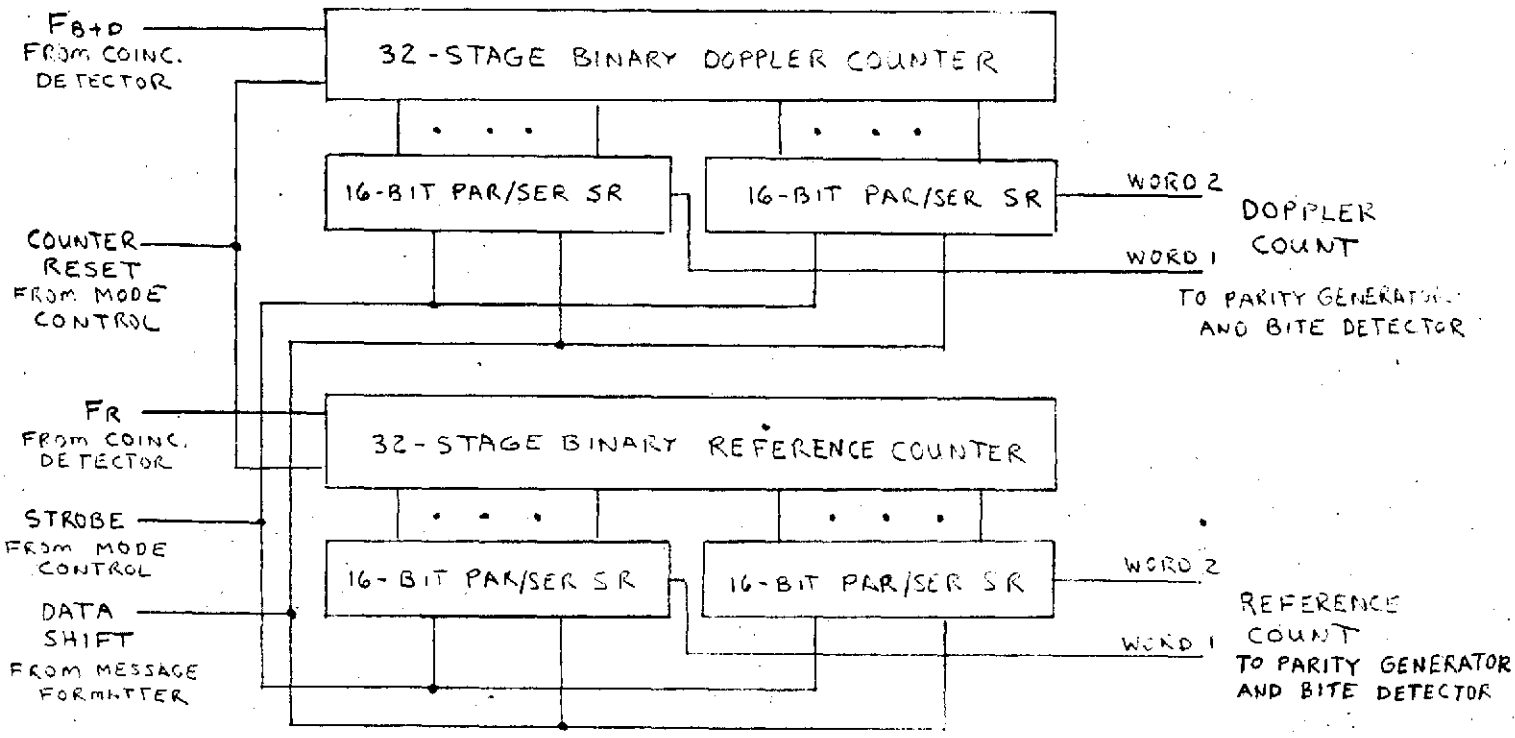


FIGURE 11-5. F_{B+D} & F_R COUNTERS

case driver plus counter propagation delay plus register set-up time requirement. Worst-case specifications for CMOS components indicate that CMOS counters and registers (operated at 12 volts) can be used for most stages.

The standard CMOS counters are not quite fast enough (worst case) to operate synchronously at 1.536 MHz. It is, therefore, proposed to use high-speed CMOS or low-power Schottky TTL components for the initial (high-speed) counter stages, implementing the remaining stages with standard CMOS. A technology mix is feasible due to the ready availability of TTL/CMOS level shifters. Power and package count estimates for this proposal were based on the use of TTL counters and appropriate level shifters for the initial counter stages. The mixed-technology approach results in a substantial power dissipation saving (compared to an all-TTL approach) at the expense of two packages for level shifters.

Observe that the approach of Figure 11-5 extracts counter data non-destructively. The counters are unaffected by the readout strobe.

11.1.2.3 Fixed Interval Timer and Mode Control

The mode control logic and interval timer are functionally illustrated in Figure 11-6. There are two basic modes of operation: Mode a -- computer commanded readout, and Mode b -- fixed time interval readout.

In Mode a, the positive transitions of the $\Delta\tau$ discrete from the MDM will set a "Strobe Request" flip-flop. The first coincidence following the strobe request will set a "Strobe Enable" flip-flop. The strobe enable output will reset the strobe request flip-flop (insuring that only one readout strobe is produced for each positive $\Delta\tau$ transition) and allow the generation of the readout strobe.

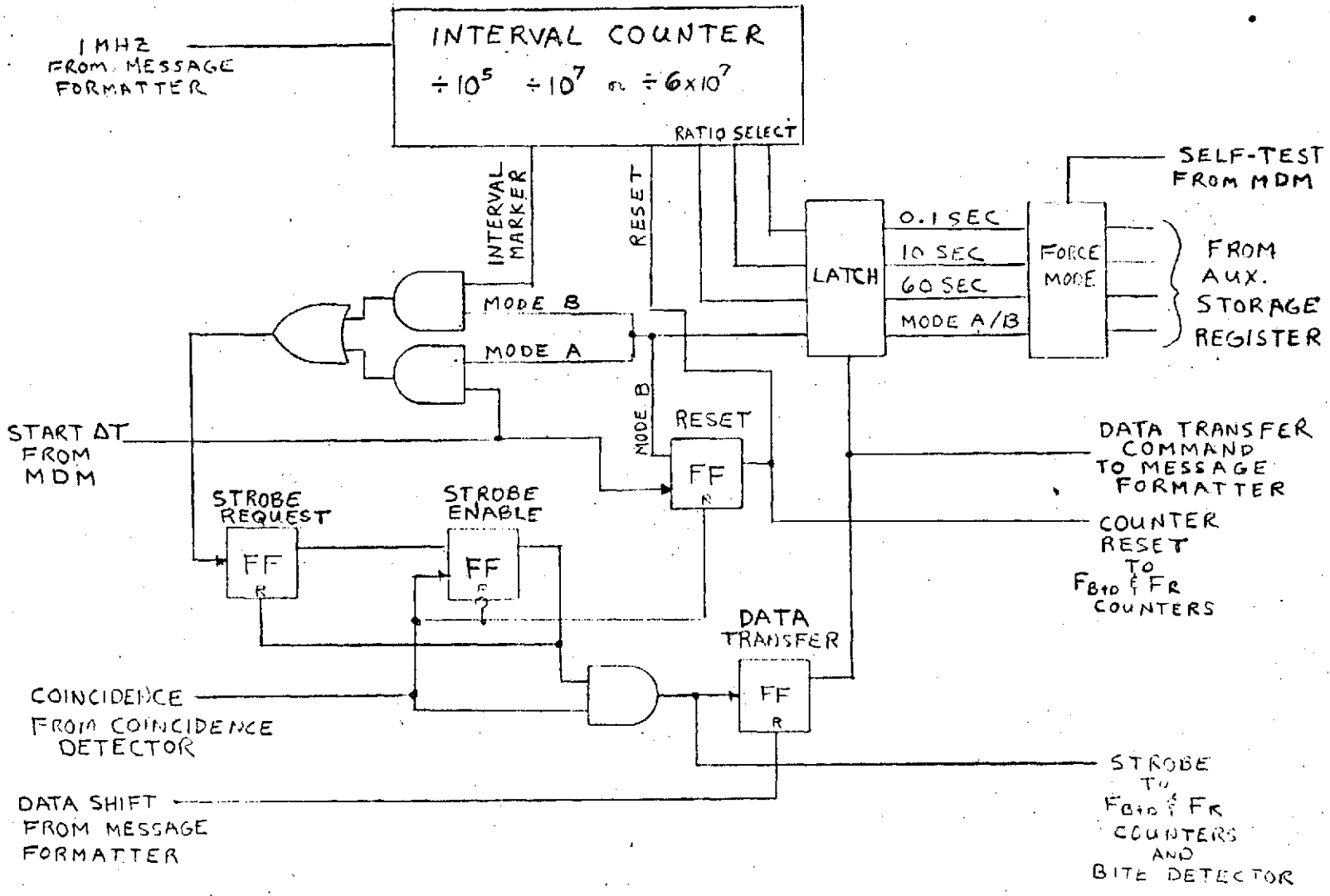


FIGURE 11-6. FIXED INTERVAL TIMER AND MODE CONTROL

The readout strobe is used to latch the doppler and reference counts and to activate the BITE detector in the self-test mode. The readout strobe also sets a "Data Transfer" flip-flop, which generates the data transfer command to the message formatter. The data transfer command is reset upon receipt of data shift pulses from the message formatter.

In Mode b, strobe requests are generated by markers from an interval counter. The interval counter counts cycles of a precision 1 MHz clock from the message formatter. Markers are produced every 10^5, 10^7 or 6×10^7 cycles, depending on the ratio select leads. The resulting 0.1-, 10-, or 60-second markers activate the strobe request flip-flop, initiating strobe generation as in Mode a.

A "Reset" flip-flop is set in Mode b with each positive transition of the $\Delta\tau$ discrete. This action will reset and hold the doppler, reference, and interval counters until receipt of the next coincidence pulse, when the counters are again permitted to count. In this way, all counting is synchronized to zero-crossing coincidence of the extractor input signals, reducing quantization error as described in Part I.

A latch is provided to hold the mode select and fixed interval select leads constant while data is being transferred to the message formatter. The latch is activated by the data transfer command. At other times, changes in mode or fixed interval length select leads are allowed to pass through the latch.

Logic is provided to force the mode control logic to a 1 second fixed readout mode when the self-test command is given.

Propagation delay requirements for generation of the readout strobe dictate the use of low-power Schottky TTL components in the strobe logic. The remaining portions of the interval timer and mode control are implemented with CMOS logic.

CMOS ripple counters are used to generate the interval markers. These devices readily operate at a 1 MHz clock rate

(under worst case conditions). The skewing of the interval markers with respect to $\Delta\tau$ transitions will be less than 13 microseconds (worst case) due to ripple delay in the counters.

It was shown in Section 10 that the worst-case delay for the coincidence pulses is 11 microseconds. The coincidence delay will cause skewing at the start of a measurement and at each readout. Since the interval timer functions independently of the coincidence pulses, however, the readout skew is not cumulative. The total worst-case skew due to interval timer ripple delay and coincidence is 35 microseconds, well within the specifications.

11.1.2.4 Doppler Extractor Package Count

A preliminary design (based on the design of the NASA bread-board unit) was prepared for worst-case analysis and to obtain accurate package count and power dissipation estimates.

The preliminary design results indicate that the doppler extraction circuits will require 5 ECL, 7 TTL, and 39 CMOS packages. Of the 51 total packages, 5 are required for shifting between the various logic levels

The mixing of technologies results in a substantial reduction in total power dissipation.

11.1.3 INPUT DATA PROCESSING AND CONTROL

The input data processing and control logic must monitor the S-Band Transponder status, the NSP status, the MTU status, and the 28 VDC extractor power input. It must generate signals to select the proper transponder and Network Signal Processor (NSP) inputs and generate status data for subsequent transmission to the computer. The input data processor and control must also accept serial data from the computer through the Multiplexer/Demultiplexer (MDM). The data must be decoded and checked for proper parity. The decoded signals are then used to select measurement mode and in Mobe b, select the measurement interval.

11.1.3.1 Input Status Monitoring

The extractor must receive and select one of two RF output signals from two-S-band transponders and accept digital information concerning the transponder operating mode. In addition, it must monitor the transponder Data Good line to insure that a valid signal is being received from the transponder over the entire measurement period. If the transponder Data Good signal goes low for a period of greater than 10 μsec., the measurement must be considered invalid.

In addition, the Master Timing Unit (MTU) status and NSP status must be monitored in a similar manner. If both the Data Good and MTU status are high during the entire measurement period, the measurement is valid and a Data Valid signal is generated and sent to the instrumentation MDM. The mode status truth table is shown in Table 11-1. The mode status is decoded and used to control the mode of the RF preconditioner. Outputs A, B, and C are sent to the message formatter where they are strobed at the proper time and transferred to the computer via the MDM.

11.1.3.2 Computer Input Data Processing

Computer input data processing includes message synch. detection, Manchester II decoding, parity checking, data storage and decoding. The decoded data selects the measurement mode and the measurement interval in the fixed time interval mode. The measurement mode status and time interval are also sent to the message formatter for transmission to the computer.

The computer data processing circuits consist basically of an input register, parity checker, auxiliary storage and time interval decode. The input register is an 18-bit shift register. Seventeen bits are used to receive data, one bit for parity, and one locally generated control bit. When the Word Discrete goes high, an initialization pulse is generated. This sets the control bit to a logic one and resets the rest of the register bits to logic zeros. Data and a clock are

TABLE 11-1

TRANSPONDER MODE STATUS TRUTH TABLE

MODE OUTPUTS			PRIME MODE	FREQ. MODE
A	B	C		
0	0	0	X	X
0	0	1	X	X
0	1	0	SGLS	LOW
0	1	1	SGLS	HIGH
1	0	0	STDN	LOW
1	0	1	STDN	HIGH
1	1	0	TDRS	LOW
1	1	1	TDRS	HIGH

received from the Manchester decoder. The clock pulses shift in the data. When the logic one control bit reaches the last stage of the shift register, a pulse is generated which samples the output of the parity checker. If parity is correct, a store pulse is generated. This transfers the three bits of data defining the measurement mode and time interval to the auxiliary storage register. The stored bit defines the measurement mode. The other two bits are decoded to specify the measurement interval for the fixed time interval mode. The contents of the auxiliary storage register are sent to the message formatter output buffers for serial transmission to the computer. The measurement mode status is used in the mode control circuitry to set up the desired time interval.

Measurement mode commands that arrive during a doppler count transfer are not read into the auxiliary storage register until after the doppler transfer is complete. Therefore, a one-shot, uses the Data Transfer signal to generate a 200 nanosecond pulse that delays transfer to the auxiliary storage register until after the doppler count is transferred.

11.1.3.3 Output Data Transfer

The message formatting and data readout timing logic must assemble the extractor status data into two 16-bit words. Upon command from the computer, the status words and doppler count words are encoded and serially transferred to the computer MDM. Each 16-bit word must be preceded by a synch. pattern and followed by a parity bit.

Transponder status data is formatted into two 16-bit words. The last 8 bits of word 2 are used for NSP ground station data while the remaining 24 bits are used for status data. Status data will include measurement mode, time interval, MTU Good, MTU switch, Data Good, Data Valid, transponder mode, self-test mode. This is only a tentative list of status data to be reported out. Additional outputs will be added as required.

11.1.4 SELF TEST MODE

Self test is initiated upon receipt of a self test discrete from the MDM. A precise, known frequency is synthesized by the RF preconditioner. The doppler extractor is switched to the fixed time interval mode with a 1 second integration period. The doppler and reference counts are outputted in the normal manner to the spacecraft computer, where frequency and delay information is recovered.

The self test approach verifies the operation of all extractor circuits with the exception of the RF preconditioner first mixer and certain control inputs.

Verification of the extractor performance is made by the spacecraft computer. It is also desirable to have a stand alone self-test capability within the extractor. This stand alone capability is provided by the BITE detector circuit.

The BITE detector monitors the doppler and reference count outputs and determines whether these outputs represent reasonable counts. A BITE discrete is generated to indicate the GO/NO-GO results of the BITE test.

Both the doppler and reference frequencies are fixed in the self test mode. The only variations in the doppler and reference counts result from skewing of the actual measurement intervals. The maximum intervals skew is 35 microseconds.

The 35 microsecond maximum skew indicates that a valid N_R count should deviate no more than 54 counts from its nominal 1,536,000 value. The N_{B+D} count should deviate no more than 51 counts from its nominal 1,426,274 value. Since the interval skew affects both counts in the same way (both counts will increase in porportion to the actual interval length), an effective indicator is the difference between the two counts (nominally 109,726). This difference will deviate no more than 4 counts from its nominal value as a result of interval skew. These numbers are based on a nominal 1 second integration period.

The BITE decoder will, therefore, perform the following two tests on the counter output data:

a. Verify the N_R is within 54 counts of its nominal value.

b. Calculate $N_R - N_{B+D}$ and verify that this difference is within 4 counts of its nominal value.

These two tests will verify that interval skew is less than 35 microseconds, and that the doppler frequency, as synthesized by the RF preconditioner and counted by the doppler counters, is within 11.5 hertz of its nominal value. This provides a reasonable check of the extractor performance.

The BITE tests are repeated at 1 second intervals as long as the unit receives the self test discrete. The use of latches to sample the test results at the proper time results in a BITE discrete output that will change at 1 second intervals, depending on the results of each BITE test.

The BITE detector is implemented entirely with CMOS components. It is estimated that 16 packages are required to implement the circuit.

An alternate BITE detector approach would use a small dedicated microprocessor to precisely calculate the interval skew and frequency error. This approach was used in the NASA breadboard, primarily because the microprocessor was required for display of the navigation parameters. The microprocessor self-test was essentially free in that case.

It is estimated that 25 packages would be required to implement a microprocessor BITE detector. This approach would involve the use of read-only-memories and a calculator chip. The availability of these components tested to MIL-STD-833 levels is not known. The use of the microprocessor approach would require software development, increasing cost by a modest amount. The microprocessor would provide an exact result. It is not felt that this precision is required.

11.1.5 POWER SUPPLY

The doppler extractor circuitry, including the RF pre-conditioner, coincidence detector and counters and control and output formatters, have been estimated to require approximately 8 watts of DC power. Table 11-2 shows the characteristics of the power supply which generates the required voltage levels at a combined output power of 8 watts.

11.2 MECHANICAL DESIGN

The objective of the mechanical design effort on the doppler extractor is to provide an equipment that will functionally meet the specified requirements. To achieve this objective, the mechanical design must provide the necessary environmental protection to the electronic circuits during the entire 12-year equipment life. The equipment life includes the manufacturing process, earth transportation and storage, checkout, launch pad environment, launch boost, flight, operation, and return.

A pressurized case is used to provide a controlled environment for the electronics. Thermal control is provided by conduction cooling to the cold plate on the spacecraft. The methods employed for pressure control (Parker Seal) and thermal control have been space qualified and proven on such programs as the CM VHF Transceiver, LCRU, and CSAR. Special consideration has been given to the vibration and stringent shock requirements.

The packaging design for the Doppler Extractor equipment has the following characteristics:

a. Size: 5.6 inches wide, 6.9 inches high, 10.6 inches long.

b. Weight: 10.2 pounds

c. Center of Gravity: The C.G. is located approximately in the geometric center of the package.

TABLE 11-2

POWER SUPPLY REQUIREMENTS AND SPECIFICATIONS

CHARACTERISTICS	REQUIRED LEVEL
Input voltage:	24-32 volts
Outputs:	+12 V ±2% +5 V ±5% -5.2V ±5%
Ripple:	5 mV PP max.
Input Power:	Less than 8 watts
Efficiency:	80%
DC isolation:	Input power leads to outputs 1 megohm min.
Reverse polarization:	No performance degradation after application of reverse polarity voltages up to 32 volts

d. Type of Construction: Unitized chassis with modular subassemblies.

e. Thermal Interface: Heat transfer by conduction from subassemblies to the base of the case. Heat transfer by conduction from its mounting base by conduction to the cold plate in the spacecraft.

The packaging concept for the Doppler Extractor represents the implementation of the following design objectives:

Minimum weight	No special tools required for installation
Minimum volume	Optimized thermal design
Minimum cost	Optimized structural design
Maximum reliability	Short delivery cycle
Withstand environmental extremes.	

The outline drawings for the Doppler Extractor is shown in Figure 11-7.

The Doppler Extractor units are divided into the following major elements:

Case	Modules
Pressure case	DC/DC Converter
Pressure cover	RF Preconditioner
Wiring and connectors	Doppler Extractor/Control
Hardware	Data Processor/Control

The Doppler Extractor case is fabricated from aluminum alloy 6061 because of its ease of machinability, good strength characteristics, and its superior ability to withstand corrosion. The case will be machined from a solid block of material as opposed to other types of fabrication such as forming and welding, to obtain the following advantages:

- Better packaging efficiency through the elimination of lap joints, radius and weld or braze fillets.

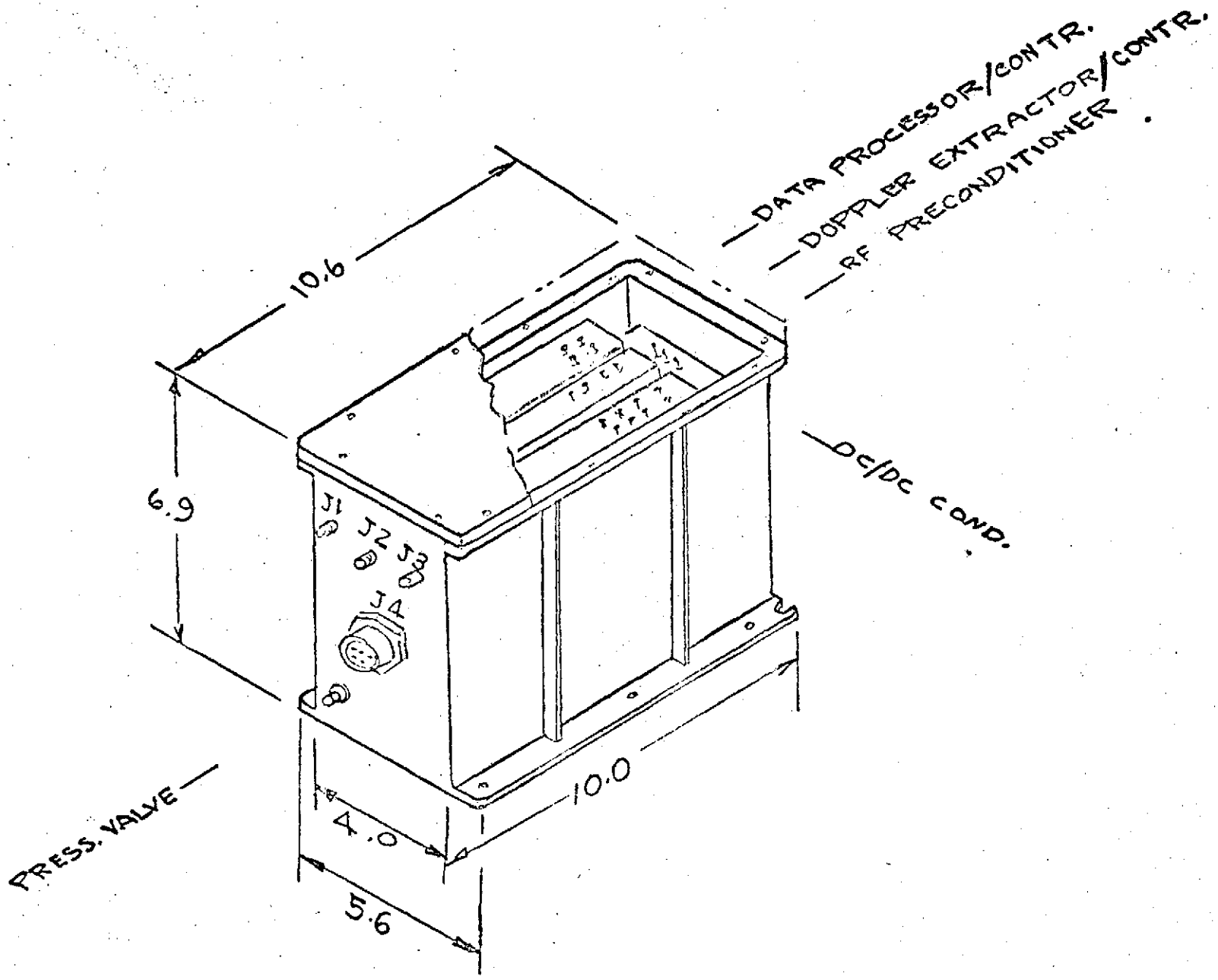


FIGURE 11-7. DOPPLER EXTRACTOR

- o Better structural integrity - the continuous and homogenous nature of the material provides a stronger and more predictable structure.
- o Closer control of tolerances effecting the positioning of components.
- o Almost limitless possibilities for partitioning and cavities as required by the electrical design.
- o Excellent shielding characteristics through the continuous nature of the enclosure.
- o Better thermal characteristics through continuous walls, and flatter interface surfaces.
- o Homogenous wall characteristics eliminate potential leak sources.

The shock and vibration spectrum that is imposed on the Extractor will be given special consideration in the packaging design. The shock pulse will be transmitted through the mounting of the case to the subassemblies, and in turn to the individual electronic components. The level of shock that will actually reach the individual components is a function of the input shock pulse spectrum and the combined natural frequencies of the series of mounting interfaces from the equipment mounting to the component. The mechanical system, in effect, behaves as a series of cascaded amplifiers, each amplifier being a mechanical interface with its own frequency response characteristic. In general, mechanical systems of this nature have a tendency to attenuate all frequencies above the natural frequency. This behavior is favorable since by the time the shock pulse reaches the electronic components the higher levels will be attenuated. By proper control of the design of the interfa ces and structures from the case to the component, the levels that the components see can be brought within safe limits.

The natural frequency of the case and other structural members will be below 1000 Hz. Since the G level increases with increasing frequency, the high peak shock levels will not be transmitted and the equipment will be capable of withstanding the imposed vibration and shock levels.

APPENDICES

Appendix A discusses the errors associated with the conventionally used linear relationship between doppler off-set and range rate, when the receiver is moving at orbital velocities. The exact, relativistic relationship is also discussed and it is shown that errors in range rate as high as 13 cm/sec can result from the linear approximation. A second order approximation to the exact formulation is also presented. It is shown that this second order approximation results in an error no greater than 10^{-7} cm/sec, at velocities as high as 100,000 ft/sec.

Appendix B is a brief description of the Vernier doppler extraction system as presented in the New Technology Disclosure to NASA.

Appendix C is a reproduction of Texas Instrument's data sheet on the 10 digit processor which was used in the one way doppler extractor micro-processor.

A-v

APPENDIX A

EFFECTS OF RELATIVISTIC VELOCITIES ON DOPPLER ACCURACY

The breadboard of the vernier extractor contains a microprocessor to compute the range rate and change in range from the measured doppler shifts. The processor computes these quantities based on the conventionally used linear relationship between doppler and range rate.

That is:

$$\dot{R} = \frac{C}{f_t} \cdot f_d = \lambda_t \cdot f_d$$

where f_t is the S-band frequency, λ_t is the S-band wavelength,

C is the velocity of light

f_d is the measured doppler and

$\dot{R}$ is the computed range rate.

The change in range is computed from the doppler count (Nd) over the measured time interval. That is:

$$\Delta R = \frac{C}{f_t} \cdot Nd = Nd \cdot \lambda_t$$

These formulas assume that the actual velocity of the S-band receiver is sufficiently small that the relativistic effects can be neglected. However, for a vehicle moving at velocities approaching 30,000 ft/sec the relativistic effects can be significant when doppler accuracies to a fraction of a Hertz (or range rate accuracies to a few centimeters per second) are desired.

Considering the effects of relativistic velocities, the true received frequency, as given in Reference (1) is:

$$f_R = f_t + f_d = \sqrt{\frac{C+\dot{R}}{C-\dot{R}}} \cdot f_t$$

where f_R is the received S-band frequency and the other parameters are defined above.

The doppler shift is:

$$f_d = f_t\left[\sqrt{\frac{(1 + \dot{R}/C)}{(1 - \dot{R}/C)}} - 1\right] \quad \text{eq. (A-1)}$$

Expressing the range rate in terms of the doppler shifts results in the equation:

$$\dot{R} = C \cdot \frac{(1 + f_d/f_t)^2 - 1}{(1 + f_d/f_t)^2 + 1} \quad \text{eq. (A-2)}$$

Expanding the terms in parenthesis results in:

$$\dot{R} = \left(C \cdot \frac{f_d}{f_t}\right) \cdot \left[\frac{2 + f_d/f_t}{2 + 2(f_d/f_t) + (f_d/f_t)^2}\right]$$

Neglecting the third order effect of the term $(f_d/f_t)^2$, and noting that $1/(1+X) \approx (1-X)$ if $x \ll 1$, then the above equation can be simplified to:

$$\dot{R} = \left(C \cdot \frac{f_d}{f_t}\right) \cdot \left(1 - \frac{f_d}{2 f_t}\right) \quad \text{eq. (A-3)}$$

The first term in parenthesis is the conventional linear relationship between doppler and range rate. The second term is a 2nd order correction to the linear approximation. The above expression is a second order approximation to the actual relativistic equation (equation A-2) and is in error from the true value by no more than $(C/4)\,(f_d/f_t)^4$. Even if (f_d/f_t) is as high as $1X10^{-4}$ (corresponding to a range rate of about 100,000 ft/sec), the error in equation (A-3) is no more than 1×10^{-6} cm/sec.

Table A-1 compares the calculations of range rate from

TABLE A-1

EFFECTS OF RELATIVISTIC DOPPLER ON COMPUTED RANGE-RATE

Measured Doppler Shift Hz	Linear Computation of Range-Rate Meters/sec	2nd Order Computation Meters/sec	True Range-Rate Meters/sec	Error in Linear Approximation cm/sec	Error in 2nd Order Approximation cm/sec
20,000	3,000	2,999.9850	2,999.9850	1.5	$\leq 7.5 \times 10^{-11}$
40,000	6,000	5,999.9400	5,999.9400	6	$\leq 1.2 \times 10^{-9}$
60,000	9,000	8,999.8650	8,999.8650	13.5	$\leq 6.0 \times 10^{-9}$
80,000	12,000	11,999.7600	11,999.7600	24.0	$\leq 1.92 \times 10^{8}$
100,000	15,000	14,999.6250	14,999.6250	37.5	$\leq 4.7 \times 10^{-8}$
Equations for doppler/error	$\dot{R}=C \cdot (f_d/f_t)$	$\dot{R}=C(f_d/f_t) \cdot (1-1/2\ f_d/f_t)$	$\dot{R}= C \cdot \frac{(1+F_d/F_t)^2-1}{(1+F_d/F_t)^2+1}$	$\epsilon \leq \frac{c}{2} \cdot (f_d/f_t)^2$	$\epsilon \leq \frac{c}{4} \cdot (f_d/f_t)^4$

NOTE: $f_t = 2 \times 10^9$ Hz

C assumed equal to 3×10^8 meters/second for simplicity of the calculations

measurements of the doppler shift, when the conventional linear formula is used, as well as the result of applying the 2nd order approximation (equation A-3) and the true expression (equation A-2). The results shown in the table indicate that for doppler shifts of 60,000 Hertz (corresponding to range rates of about 9000 meters/sec or 30,000 ft/sec) the linear approximation can be in error by 13.5 cm/sec. The 2nd order approximation, however, is in error by no more than $6X10^{-9}$ cm/sec. The linear approximation can give errors significantly greater than the desired maximum range rate error of 3 cm/sec. The 2nd order approximation, however, produces an error well below the desired bounds, even for range rates as high as 15,000 meters/sec (50,000 ft/sec). It is recommended that the 2nd order approximation be used for all range rate computations requiring knowledge of range rate to within about 15 cm/sec (0.5 ft/sec) of the actual value at orbital velocities.

APPENDIX B
NEW TECHNOLOGY DISCLOSURE

B.1 INTRODUCTION

In many electronic systems employing digital techniques to measure frequency or range rate (radar, collision avoidance systems, navigation aids, etc.) the primary source of error is very often the quantization (± 1 cycle) resulting from the digitizing process. In measuring frequency using conventional counters, for example, the unknown frequency zero crossings are counted for a time period determined by simultaneously counting a known stable reference frequency. If the measurement period is one second, the frequency error will be ± one Hertz.

Several techniques have been developed to reduce the quantization error but most are either time consuming, do not offer sufficient improvement, may increase other error sources, require high frequencies and/or require high power, high speed counters. The technique described in this report can achieve a quantization error reduction of 1000 or more without the use of high speed counters and the majority of circuit elements can employ low power, low cost, high reliability CMOS circuitry. The technique has been implemented in a breadboard model and measurements made with the breadboard indicate that frequency can be resolved to at least .02 Hertz over a one second counting period. Higher resolutions are achievable with the breadboard but the ultimate resolution capability has not yet been measured.

B.2 SYSTEM DESCRIPTION

The RCA developed technique to achieve high resolution measurements of frequency uses an electronic equivalent to the mechanical vernier caliper. In the mechanical version, the measurement precision is expanded by means of reading the coincidence of the scale markings of two nearly equal scales. The RCA developed technique employs the zero crossing of a known stable frequency and the unknown frequency as the scale markings, and a coincidence detector circuit to determine when a zero

crossing coincidence has occurred between the two frequencies. A simple block diagram of the technique is represented in Figure B-1.

A timing scheme to control the start and stop times of the counters is shown in Figure B-2. The unknown frequency is represented by (F_B+F_D) or F (B+D) for convenience, since it often develops from a known bias frequency shifted by an unknown frequency (e.g. doppler). From Figures B-1 and B-2, the unknown frequency and the known clock frequency are compared for a zero crossing coincidence by means of an "AND" gate. Since the input frequencies are typically sine waves, pulse generators are used to generate very narrow zero crossing markers so that the "AND" gate can precisely measure the time of coincidence. The counters are started and stopped at coincidence signals from the "AND" gate. At the end of the counting period, the reference frequency counter contains a precise measure of the measurement time interval since this counter counted from one zero crossing to a later zero crossing. The unknown frequency counter contains a precise measure of the unknown frequency since it is counted from one zero crossing to a later zero crossing. Since both counters were started and stopped on zero crossings, and were started and stopped simultaneously, the quantization error is virtually eliminated. A small quantization error does remain, however, due to the fact that the "AND" gate will trigger on any amount of overlap between the unknown and reference signal pulses. The residual quantization error is given by:

$$\epsilon_Q = \pm \frac{(P_o+P_B)\ (F_B+F_D)}{2} \text{ cycles}$$

where ϵ_Q = residual quantization error

P_o, P_B are the pulse widths for the reference and unknown signals, respectively.

(F_B+F_D) is the unknown frequency

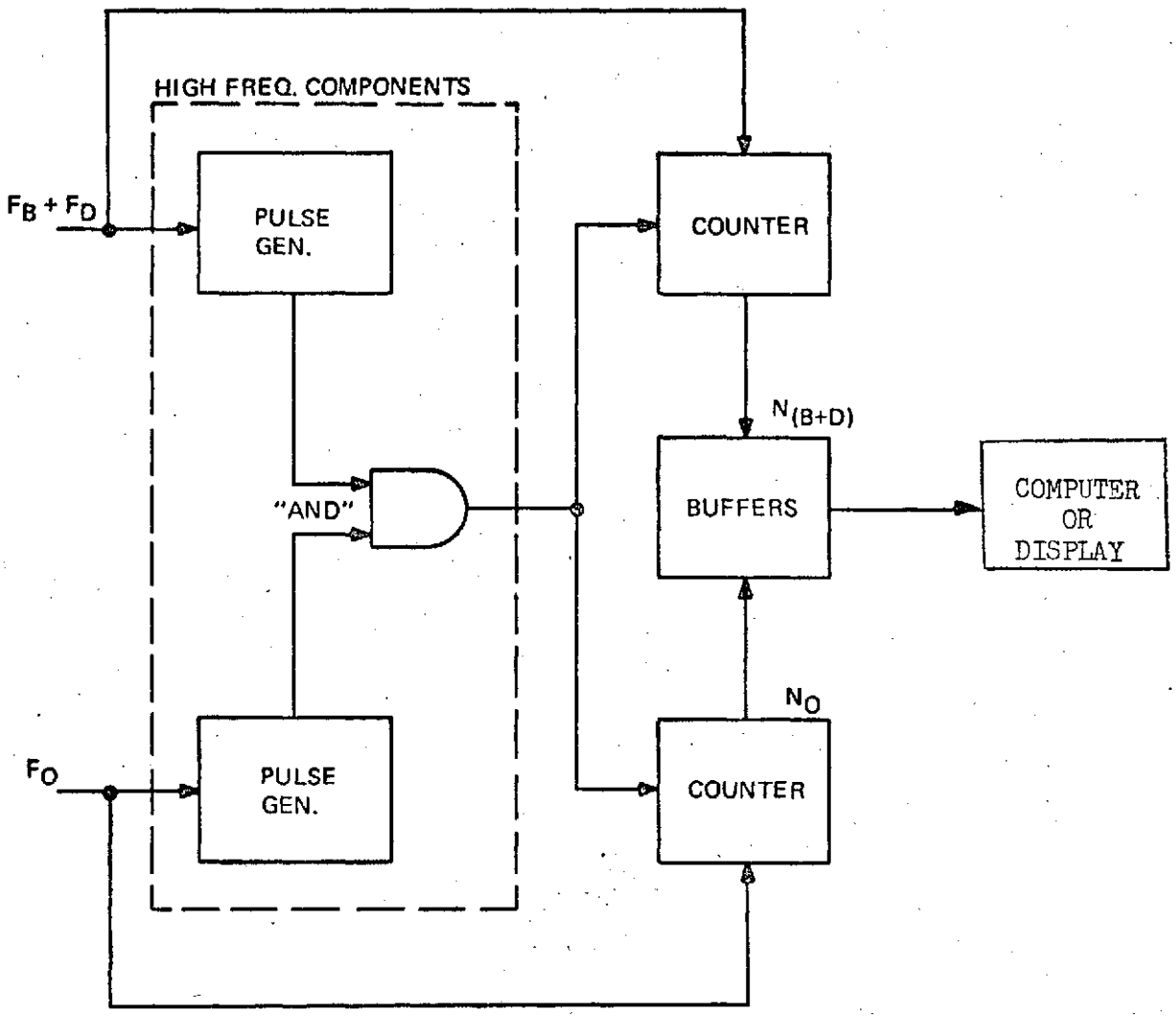
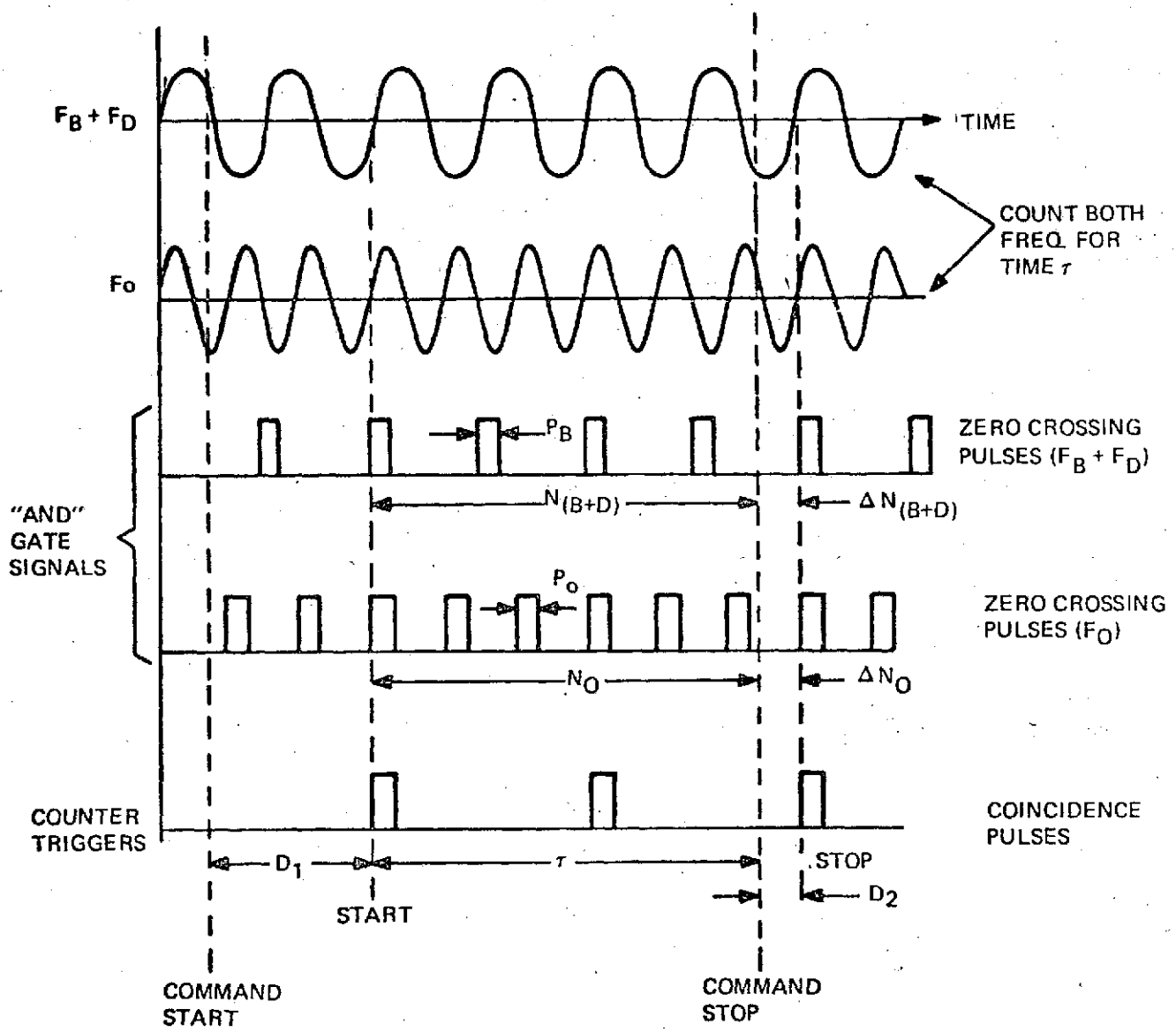


Figure B-1. Coincidence Detection Doppler Extractor, Block Diagram



$$\tau + D_2 = \frac{N_0 + \Delta N_0}{F_0}$$

$$F_D = \frac{N_{(B+D)} + \Delta N_{(B+D)}}{N_0 + \Delta N_0} \cdot F_0 - F_B$$

QUANTIZATION ERROR = $(P_0 + P_B)(F_B + F_D)$

Figure B-2 Timing Scheme For Coincidence Doppler Extractor

Since the quantization error occurs at both the beginning and end of the measurement period, the total quantization error over the measurement period is distributed over twice the above range. The standard deviation of the quantization frequency error assuming a uniform distribution, is given by

$$\sigma_{F_Q} = \frac{(P_D+P_B)\ (F_{B+}F_D)}{\tau\sqrt{6}} \text{ HERTZ}$$

where τ is the measurement period.

B.3 BREADBOARD PERFORMANCE

The technique described in this report has been implemented by RCA under a contract with NASA (contract number NAS 9-13517). Measurements have been made using an unknown frequency of 1 MHz (down converted from about 2 GHz) which had a 1 second short term stability of about .01 Hertz.

The pulse widths into the "AND" gate were 7.5ns (15ns aperture). The resultant standard deviation of the measurements is shown in Figure B-3. These results indicate that the breadboard unit performed as expected and could measure the unknown frequency to within .02 Hertz over a one second measurement period. Higher accuracies could be achieved with shorter pulse widths into the "AND" gate. The breadboard unit is capable of operating with pulses as short as one nanosecond, which should result in frequency resolutions of less than .001 Hertz over a one second measurement period. Measurements of this small a quantization error is difficult, since oscillator drift and noise jitter will now become predominant system errors.

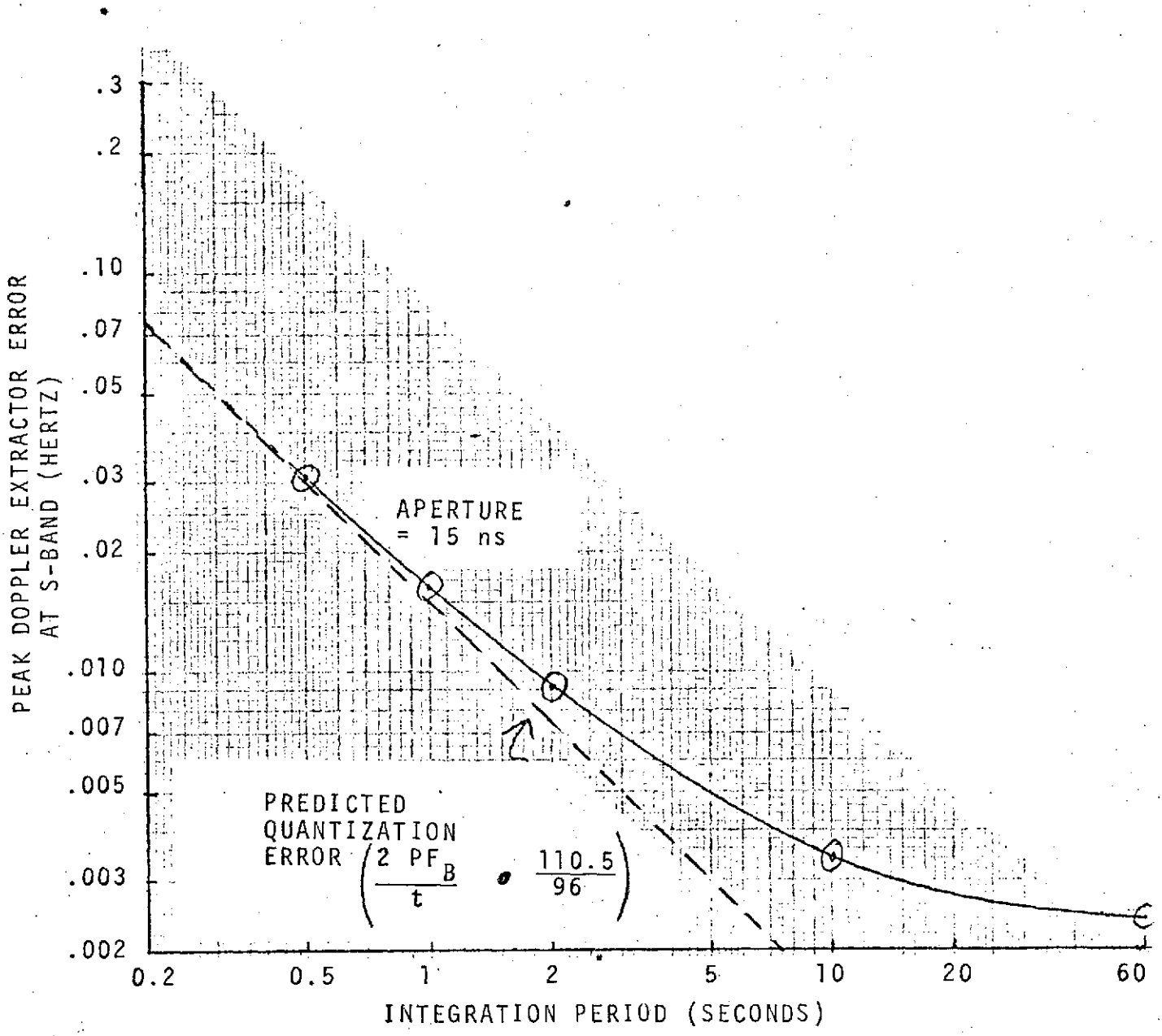


FIGURE B-3. OWD EXTRACTOR MEASUREMENT ERROR

MOS
LSI

TMS 0117 NC
10-DIGIT DECIMAL ARITHMETIC PROCESSOR

FEBRUARY, 1973

- 10 Digits, 3 Registers
- BCD Input and Output
- Direct Add, Subtract, Multiply, Divide
- Implied Constant in 4 Basic Modes
- Add to Overflow, Subtract to Zero
- Shift Left, Shift Right
- Exchange Registers
- Busy/Ready Interlocks
- On-Chip Digit Clock
- 100 ms Maximum Operation Time
- TTL Compatibility

description

The TMS 0117 NC is an MOS/LSI digital building block designed to process numerical data in BCD format. The device performs the most commonly required arithmetic operations, and numbers of up to ten digits can be processed in under 100 milliseconds.

Even when only partially utilized, the TMS 0117 provides a considerable cost saving when compared with more conventional arithmetic techniques. Its applications include automatic control systems, on-line data analysis, digital correlators, weighing machines, and computing counters/frequency meters. The device requires a minimal amount of external control logic, and complex problems may be solved by using it as a 'mini' central processor unit (CPU) in conjunction with SN74188 bipolar integrated circuit Programmable Read Only Memories (PROMs) as the microprogram store.

In addition to the four basic processes (Add, Subtract, Multiply, Divide), the TMS 0117 performs operations such as Increment, Decrement, Shift Left, Shift Right, Exchange Operands, Add to Overflow, and Subtract to Zero.

A BUSY/READY signal generated on the chip discriminates between the BUSY condition (output data invalid, no data can be entered) and the READY condition (output data valid, data can be entered).

Data input and output are in serial form.

An output clock generated on the chip can be used to off load the output data into a memory.

operation

Functions that the processor will perform may be classified into three types — arithmetic, register, and internal control ('housekeeping'). Register and simple arithmetic operations, such as data interchange and add/subtract 1, require a minimal amount of internal microprograms and are rapidly executed. More complex arithmetic operations, such as multiplication and division, use a considerable portion of the program space and take proportionately longer to execute. The time taken to carry out housekeeping instructions, e.g. reset after error flag, is variable, being dependent on the state of the internal program.

The operations are defined as follows:

- Multiply

  Multiply the contents of the output register (multiplicand) by the last data entry (multiplier) and transfer the product to the output register.

— continued

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

TEXAS INSTRUMENTS
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operation (continued)

- Divide
  Divide the contents of the output register (dividend) by the last data entry (divisor) and transfer the quotient to the output register.
- Add
  Add the last data entry to the contents of the output register.
- Subtract
  Subtract the last data entry from the contents of the output register.
- Increment
  Add 1 to the contents of the output register. (Decimal point and sign are ignored in this operation.)
- Decrement
  Subtract 1 from the contents of the output register. (Decimal point and sign are ignored.)
- Add to Overflow
  Continuously increment at the rate of 1 per D scan, the contents of the output register until overflow is reached.
- Subtract to Zero
  Continuously subtract 1 at the rate of 1 per D scan from the contents of the output register until zero is reached.
- Equal
  Execute instruction. Causes the processor to carry out the last stored instruction. Equal also sets up implied constant (last data entry and last function).
- Right Shift
  Move the contents of the output register one place toward the least significant digit (LSD).
- Left Shift
  Move the contents of the output register one place toward the most significant digit (MSD).
- Exchange Operands
  Interchange the last pair of numeric entries, e.g. $a \div b$ becomes $b \div a$.
- Clear
  Clear all stored instructions and data registers.
- Reset
  Reset is a master clear and will operate under all conditions. It is used when the processor has entered a locked state, i.e. error flag, and it resets the internal programs.

timing

The basis for the timing is an external clock applied to the device. Nominal frequency of the clock is 250 kHz. An internal state time is equivalent to 3 external clock cycles. A digit time is equivalent to 13 internal state times or 39 clock cycles or nominally 156 microseconds. A digit time (D-time) corresponds to the time during which each digit is displayed. A blanking of one state time is on the leading and trailing edge of each D output signal. Eleven digit terminals are used to scan the data entry logic and to multiplex a display. Only one digit time is high at any given point.

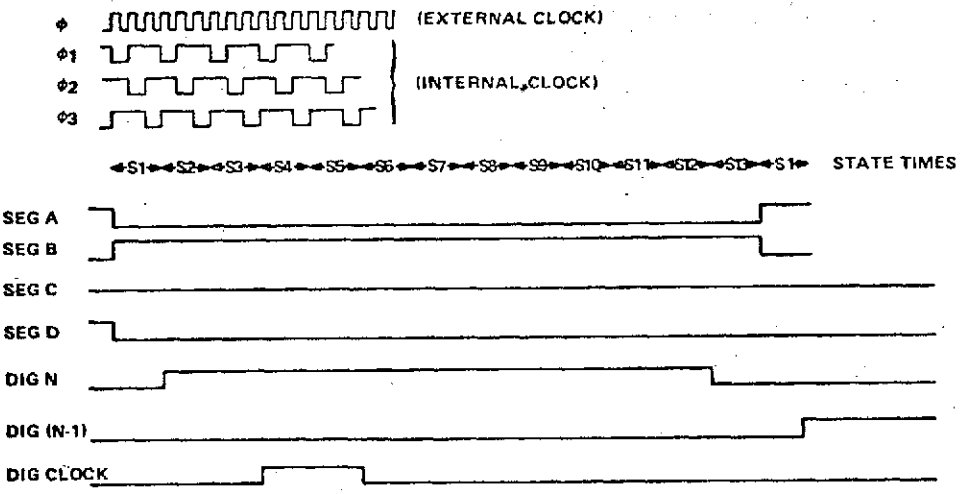
Digits are displayed in scanning mode, thus any digit is displayed for one D-time and displayed again one D-cycle later. (A D-cycle is equivalent to 11 D-times – i.e. 1.72 milliseconds.)

A digit clock is brought out on SP (pin 24) to be used for clocking data to be stored from the TMS 0117 to a memory. The clock pulse is two state times wide (S_4 and S_5 out of 13 state times) and the data is valid on either edge of the clock as shown below. The period of the clock is one digit time (13 state times).

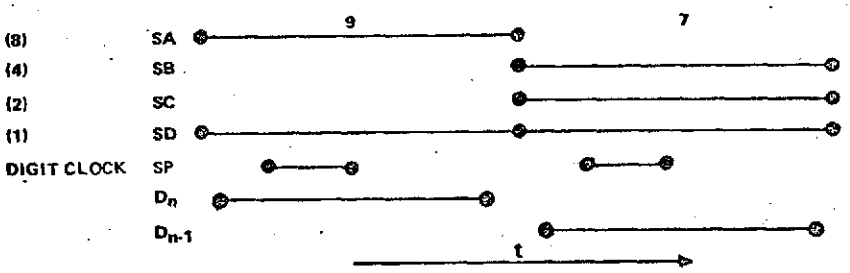
– continued

timing (continued)

TIMING DIAGRAM
One Digit Time



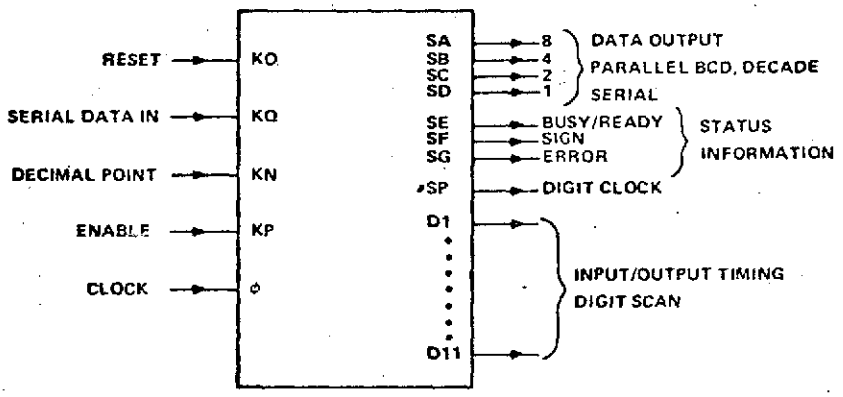
Two Digit Times, Displaying Number 97



The table below shows the time required to complete the functions indicated for a nominal 250-kHz clock rate.

FUNCTION	TIME
Numer entry, single digit	5.2 ms maximum
Operation instruction entry	6.9 ms maximum
Shift left or right	1.72 ms
Increment or decrement	3.4 ms
Exchange operands	5.2 ms
Add, subtract	8.6 ms
Multiplication	70 ms (worst-case numeric inputs)
Division	80 ms (worst-case numeric inputs)
Digit cycle time	1.72 ms
Digit time	156 μs

TMS 0117 INPUTS, OUTPUTS, CONTROL TERMINALS



There are two types of data input, both of which are entered on the KQ terminal. They are:

- Numerical data
- Operation commands

data input

The serial data input line requires its information in the form of a serial five-bit word. Four bits are used as a data/instruction code and the fifth bit as a control. The control determines whether the four-bit code is interpreted as data or as an instruction.

INPUT CODING

CONTROL BIT				INPUT NOTATION			
2^3	2^2	2^1	2^0				
A5	A4	A3	A2	A1			
0	0	0	0	0	0	Numeric Data	
0	0	0	0	1	1		
0	0	0	1	0	2		
0	0	0	1	1	3		
0	0	1	0	0	4		
0	0	1	0	1	5		
0	0	1	1	0	6		
0	0	1	1	1	7		
0	1	0	0	0	8		
0	1	0	0	1	9		
1	0	0	0	0	Clear	Instruction Codes	
1	0	0	0	1	Equals		
1	0	0	1	0	Multiply		
1	0	0	1	1	Divide		
1	0	1	0	0	Add		
1	0	1	0	1	Add 1		
1	0	1	1	0	Subtract		
1	0	1	1	1	Subtract 1		
1	1	0	0	0	Add 1 to overflow		
1	1	0	0	1	Subtract 1 to zero		
1	1	0	1	0	Shift right		
1	1	0	1	1	Shift left		
1	1	1	0	0	Exchange operands		
1	1	1	0	1	No operation	Not Used	
1	1	1	1	0	No operation		
1	1	1	1	1	No operation		

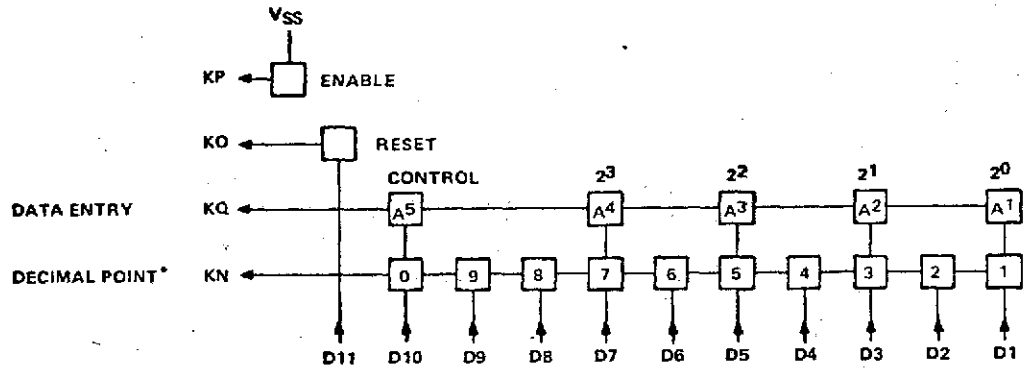
— continued

data input (continued)

In order to reduce the number of package pins required for data entry, the five-bit code is serialized. The processor generates sequential digit strobes, D1 to D11, that enable the input data to be serialized.

The data input lines are KN, KO, KP and KQ. The boxes represent a logical or direct switch connection between the digit lines D1 to D11 and K inputs.

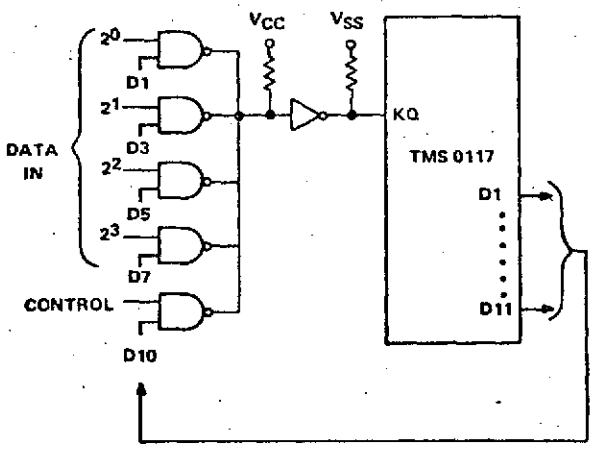
DATA INPUT AND DIGIT LINES



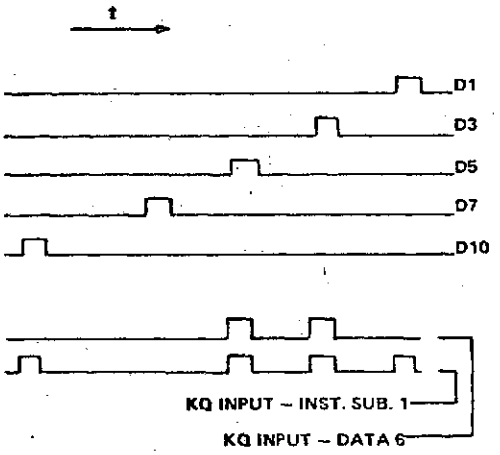
*Decimal point – one switch and only one switch permanently closed.

A gate implementation of the entry function and a simplified timing diagram are shown below.

ENTRY FUNCTION



TIMING DIAGRAM



The data entries are controlled by the enable input, as described under Input Coding. Numeric entries are limited to ten digits. Any zeros that are required to fill the unused most-significant-digit positions preceding number entry (leading zeros) need not be entered; but if, from a systems point of view, it is necessary to enter them, they will be ignored by the processor. Data are entered most-significant-digit first.

– continued

data input (continued)

The RESET terminal is an interrupt signal. It will clear all registers and status information under any conditions. This is the only key operational after the machine enters a locked state. The CLEAR opcode clears in the same manner but cannot be used once in the locked state (overflow). RESET operates independently and does not need to be followed by an ENABLE.

data output

The TMS 0117 has two types of data output — numeric and status.

numeric data

Numeric data is presented as digit serial, bit parallel, Binary Coded Decimal (BCD) during digit times D10 (MSD) to D1 (LSD) on outputs SA to SD. This serial information repeats after 11 digit times, i.e. once every digit cycle. Outputs D1 to D10 can be used to strobe an external display or indicate the beginning and end of the output data word. An output digit clock is provided on output SP to enable the user to clock output data into an external register. The digit clock timing is arranged such that output data is valid on either edge of the digit clock. Similarly digit strobes D1 to D11 also inset the data outputs.

	SA	SB	SC	SD	SE	SF	SG	DIGIT
DATA	0	0	0	0	0	0	0	0
	0	0	0	1	0	0	0	1
	0	0	1	0	0	0	0	2
	0	0	1	1	0	0	0	3
	0	1	0	0	0	0	0	4
	0	1	0	1	0	0	0	5
	0	1	1	0	0	0	0	6
	0	1	1	1	0	0	0	7
	1	0	0	0	0	0	0	8
	1	0	0	1	0	0	0	9

NOTE: Data is extracted from MSD (D10) first to LSD (D1) last.

status information

Status information, i.e. the internal state of the processor (housekeeping), is available on outputs SE to SG during D11 time. Output D11 may be used to clock outputs SE to SG into an external register.

STATUS CODING

SA	SB	SC	SD	SE	SF	SG		
0	0	0	0	1	X	0	Busy	INTERPRETATION (where X represents a don't-care condition)
0	0	0	0	0	X	0	Ready	
0	0	0	0	0	0	0	Sign Positive	
0	0	0	0	0	1	0	Sign Negative	
0	0	0	0	X	X	1	Error	

OUTPUT: Error, Sign, Busy/Ready

— continued

data output (continued)

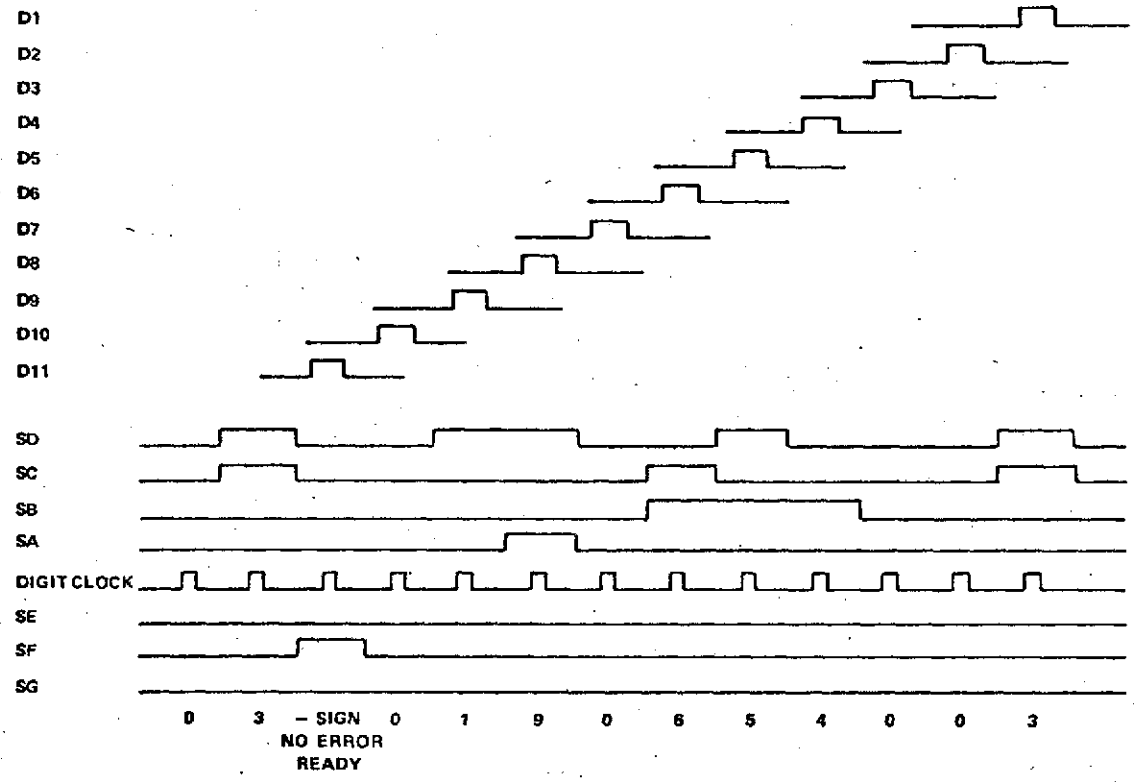
During D11 time, outputs SA to SD are zero. Output SG indicates an error, such as numeric overflow or an invalid operation. Status outputs have the following priorities:

1) Error output SG invalidates all other numeric and status outputs. If an error indication occurs, the processor enters a locked state and must be reset.

2) Busy/ready output SE invalidates numeric and sign data, unless it indicates that the processor is ready to accept new data or instructions, i.e. only when there is no error and the ready signal is present are the sign and numeric outputs valid.

An example of the data output timing is shown below.

DATA OUTPUT TIMING EXAMPLE



As shown, the serial output data represents –0190654003. The numeric and sign outputs are valid since the processor indicates that it is READY and there is no ERROR during D11 time.

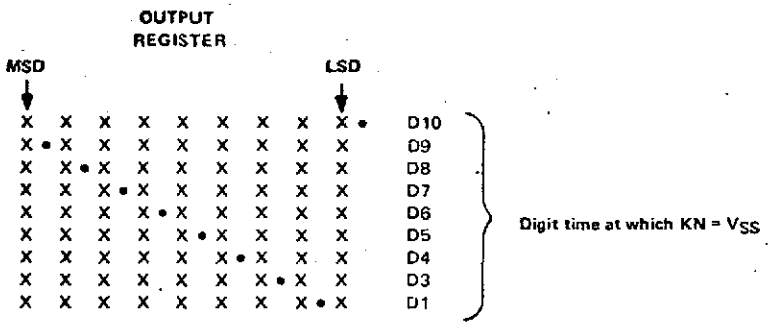
decimal point (DP)

The processor operates in fixed-point mode on input and output. The point is not interposed between input digits, i.e., there is no input or output data code representing DP. DP is, in fact, implied by the digit time at which input KN is taken to a logic High. Decimal-point format is shown below.

– continued

decimal point (DP) (continued)

DECIMAL POINT FORMAT



KN may be taken to a logic High by means of a fixed link with the required digit output D1 to D10. If the position is to be determined by means of logic inputs, then open collector gates can be used to determine the KN-digit connection in a manner similar to data entry.

The decimal point is not input in the normal flow of entering numbers but is set for any calculation by a switch. The position of the switch does not affect an addition or subtraction problem, but it does affect multiplication and division (see the problem set below). The decimal is not stored internally; therefore, erroneous answers will result if the decimal switch is changed while performing a series of calculations. To prevent errors, RESET or CLEAR the chip after changing the decimal-point switch.

PROBLEM SET

NUMBER ENTRY	DISPLAY		
	DECIMAL POINT AT POSITION:		
	0	2	4
500000	500000.	5000.00	50.0000
+	500000.	5000.00	50.0000
400	400.	4.00	0.0400
X	500400.	5004.00	50.0400
30000	30000.	300.00	3.0000
÷	(OVF) 0.	1501200.00	150.1200
400	(OVF) 0.	4.00	0.0400
=	(OVF) 0.	375300.00	3753.0000
RESET	0.	0.00	0.0000
1	1.	0.01	0.0001
÷	1.	0.01	0.0001
3	3.	0.03	0.0003
=	0.	0.33	0.3333
90	90.	0.90	0.0090
=	30.	30.00	30.0000
4	4.	0.04	0.0004
EXCH OP	3.	0.03	0.0003
=	0.	0.75	0.7500

NOTES: 1. Decimal point is external to chip.
2. For clarity, insignificant leading zeros are not shown.

overall operation

The timing of the data entry and control is determined by the enable input in conjunction with the status outputs. It is best expressed in 'digit times', i.e. the time between leading edges of successive digit pulses, and 'digit cycles', i.e. the time between leading edges of successive D1 pulses.

To initiate a data entry cycle, the enable input KP is taken to a logic High (V_{SS}). After a variable delay, the status outputs will indicate that the processor is in the BUSY mode. Data entry will be possible during the READY mode only. The TMS 0117 will ignore inputs when performing an operation. The entry cycle will last 14 to 23 D-times, depending on which digit is On when the enable connects to V_{SS}. Enable must be released within 5 D-times from BUSY signal unless a special mode of operation is desired. In the special mode the enable is kept High throughout the operation. Data inputs are changed each time the processor goes from the READY to the BUSY state until the entire sequence is completed. This speeds up data input since the processor may be ready internally to accept new data, but, because of the multiplexed output, the READY output cannot be given until D11 time. Since data entry and some operations, such as Add 1, Shift Right, etc., are short, the BUSY time will only be 1 to 3 digit cycles.

Data and instructions are entered in the same order as with a +, −, = type of keyboard. In addition to chain operations, e.g. 2 x b x c =, *there is an implied constant. The processor retains the last operator and number entry before an* Equal operation, as a constant.

The + and − code is interpreted as a sign after a Multiply or Divide operation, and as an operation at any other time. Successive Equal operations cause multiple executions of the previously stored instructions and the associated data, i.e. constant mode operation.

Examples:

	Entry	Display	Comments
1)	100	100	Display entry
	−	100	Stored as instruction
	3	3	Display entry
	=	97	Executes previous instruction
	=	94	Constant mode, instruction is sub 3, executes and displays
	−	94	Stored as instruction
	50	50	Display entry
	=	44	Executes previous instruction
	=	−6	Constant mode instruction is sub 50
	=	−56	Constant mode instruction is sub 50
2)	100	100	Display entry
	−	100	Stored as instruction
	3	3	Display entry
	+	97	Causes previous instruction to be carried out and stores current instruction.
	10	10	Display entry
	+	107	Previous instruction carried out and stores current instruction
	3	3	Display entry
	−	110	Executes previous instruction and stores current instruction
	99	99	Display entry
	−	11	Executes previous instruction and stores current instruction
	12	12	Display entry
	=	−1	Executes previous instruction and displays result

	Entry	Display	Comments
3)	−	0	Stored as sign/instruction
	5	5	Display entry
	X	−5	Enters instruction and interprets − as sign and displays
	3	3	Display entry
	=	−15	Executes previous instruction and displays result
4)	−	0	Stored as sign/instruction
	5	5	Display entry
	X	−5	Enters instruction and interprets − as sign and displays
	−	−0	Enters sign and displays
	5	−5	Enters data and displays with associated sign
	=	25	Executes previous instruction and displays result
5)	100	100	Display entry
	+	100	Enters add instruction
	−	200	Enters sub instruction and executes previous instruction
	3	3	Display entry
	=	197	Executes previous instruction and displays result
6)	100	100	Display entry
	−	100	Enters sub instruction
	−	0	Enters sub instruction and executes previous instruction
	5	5	Display entry
	=	−5	Executes previous instruction and displays result

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−20 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−20 V to 0.3 V
Clock input voltage range (See Note 1)	−20 V to 0.3 V
Data input voltage range (See Note 1)	−20 V to 0.3 V
Applied output voltage range (See Note 1)	−20 V to 0.3 V
Operating free-air temperature range	0°C to +70°C
Storage temperature range	−55°C to +150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

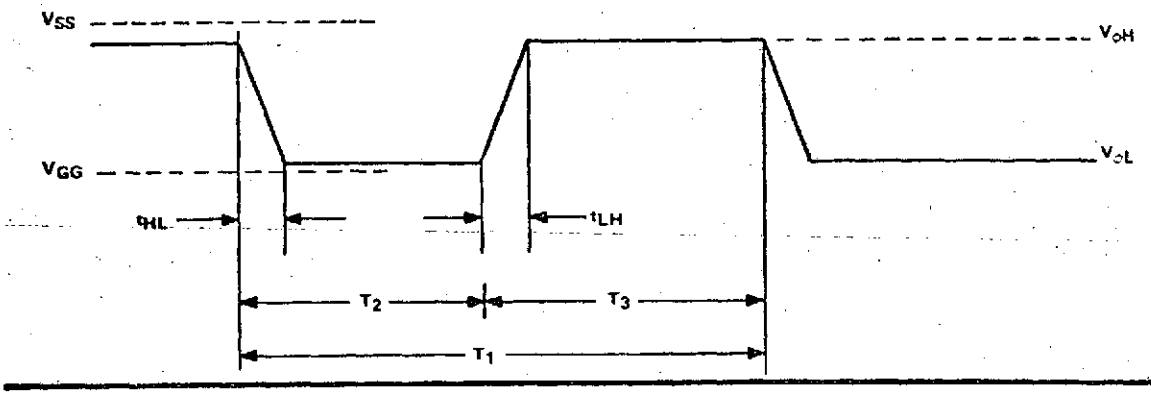
recommended operating conditions

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNIT
Operating Voltages (See Note 2)					
Drain supply V_{DD} (See Note 3)		0	0	0	V
Substrate supply V_{SS}		6.6	7.2	8.1	V
Gate supply V_{GG}		−8.1	−7.2	−6.6	V
Clock Levels					
Clock high level $V_{\phi H}$		V_{SS} −1.5	V_{SS} −0.5	V_{SS}	V
Clock low level $V_{\phi L}$		V_{GG} −1	V_{GG}	V_{GG} +1	V
Applied Output Voltage		−0.3		18	V
Clock Timing (See Clock Timing Diagram)					
Frequency		100	250	400	kHz
Period T_1		2.5	4	10	µs
Half-period T_2		1.25	2	5	µs
Half-period T_3		1.25	2	5	µs
Clock T_r and T_f	f clock = 100 kHz	30		1000	ns
Clock T_r and T_f	f clock = 250 kHz	30		650	ns
Clock T_r and T_f	f clock = 400 kHz	30		300	ns
Input Level K Lines					
Low		V_{GG}	V_{DD}	V_{SS} −6	V
High		V_{SS} −1.5	V_{SS} −0.5	V_{SS}	V

NOTES: 2. Effective zero suppression depends on a transient free rise of V_{SS} and V_{GG} during power-up. With certain supply systems it may be necessary to capacitively damp the supplies to ensure zero suppression.

3. V_{DD} is voltage reference.

CLOCK TIMING DIAGRAM



electrical characteristics at nominal conditions over 0°C to 70°C temperature range

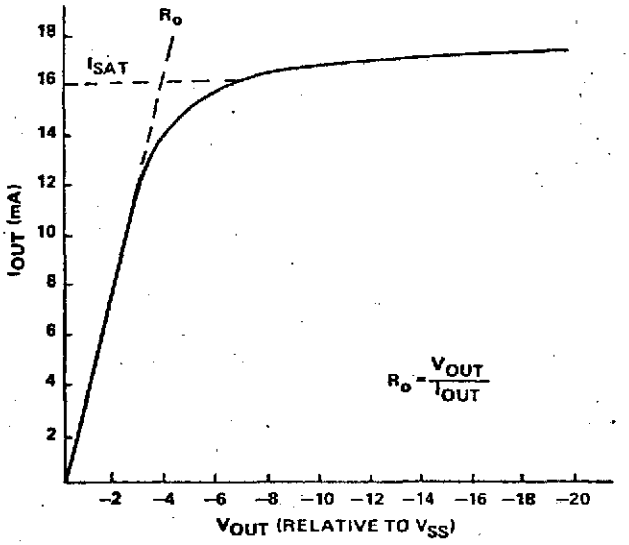
CONDITION	MIN	TYP†	MAX	UNIT
Input current on K lines (K input low) (All other pins GND)		0.1	10	μA
Input pull-up resistance		30		kΩ
Output leakage (off state with $V_{OUT} = V_{SS} - 10$ V) (See Note 4)		0.1	100	μA
Output resistance R_O (on state with $V_{OUT} = V_{SS} - 0.5$ V) (See Typical Output Buffer Characteristics)		250	500	Ω
Output saturation current I_{SAT}		15		mA
Clock leakage (Low Level)		0.1	100	μA
K line input capacitance ($V_K = V_{SS}$, f = 100 kHz)		2.5	5	pF
Output capacitance (f = 100 kHz)		2.0	5	pF
Clock capacitance (f = 100 kHz)		10	20	pF
Average supply current I_{GG} (See Note 4)		10	15	mA
Average supply current I_{DD} (See Note 4)		17	25	mA
Power dissipation (See Notes 4 and 5)		265	400	mW

NOTES: 4. At 25°C. Output leakage cannot be measured with a curve tracer because capacitive coupling will turn on the output.

5. Power saving techniques, including pulsing of power supplies and reduction of clocking cycle may reduce power to 100 mW. These techniques involve special screening of the device.

†All typical values are at $T_A = 25°C$.

TYPICAL OUTPUT BUFFER CHARACTERISTICS



computation times (see timing section)

TTL interface

The K inputs will interpret as a logic High a voltage that lies between the substrate supply voltage V_{SS} and $V_{SS} - 1.5$ V, and as logic Low a voltage between the gate supply voltage V_{GG} and drain supply voltage $V_{DD} + 1.2$ V. The simplest input interface may be a TTL open-collector gate with a pull-up resistor to V_{SS}.

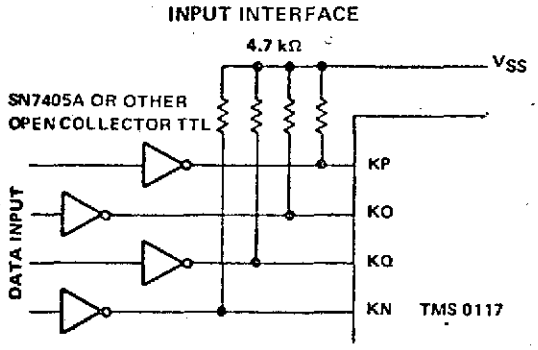
All data and control inputs have an internal pull-up resistor to V_{DD}. The load presented to an external driver is the internal resistor (30 kΩ) and the capacitance of the gate clamp protection diode.

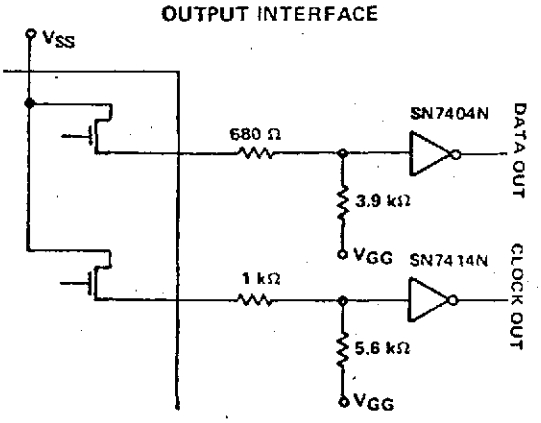
— continued

TTL interface (continued)

All outputs, D1 to D11 (data and status) are open-drain buffers. The output buffers have a typical channel resistance $r_{DS(on)}$ of 250 Ω and can supply in excess of 5 mA to V_{SS}. An economical output interface compatible with TTL is shown below.

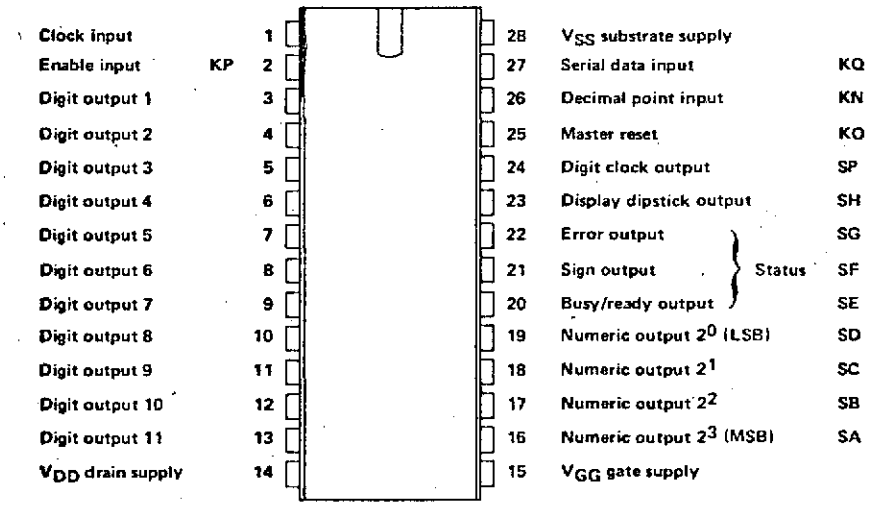
Any output, e.g. digit clock, that is required to drive a TTL clock input should be interfaced with a Schmitt trigger, such as the SN7414N integrated circuit. The Schmitt trigger is required because the fall time of the open-drain output is of the order of 150 nanoseconds and is not directly compatible with edge-triggered TTL inputs.





mechanical data

The TMS 0117 NC is mounted in a 28-pin plastic dual-in-line package, designed for insertion in mounting-hole rows on 0.600-inch centers.



NOTES:
1. Digit outputs D1, D3, D5, D7 and D10 are used to serialize input data.
2. Digit outputs D1 – D10 are used as digit enable for numeric display.
3. Status outputs are valid during D11 time.
4. K input and S output notation per TMS 0100 NC specifications.
5. Display dipstick SH indicates the number of digits displayed in the output register by being at logic High for the relevant portion of the digit cycle. It acts as a zero suppress latch.

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