TO:       KSI/Scientific & Technical Information Division  
          Attn: Miss Winnie M. Morgan

FROM:    GP/Office of Assistant General  
          Counsel for Patent Matters

SUBJECT: Announcement of NASA-Owned U.S. Patents in STAR

In accordance with the procedures agreed upon by Code GP and Code KSI, the attached NASA-owned U.S. Patent is being forwarded for abstracting and announcement in NASA STAR.

The following information is provided:

U.S. Patent No. : 3,857,045

Government or Corporate Employee: Lockheed Missiles & Space Co., Sunnyvale, CA

Supplementary Corporate Source (if applicable):

NASA Patent Case No.: MSC-14,240-1

NOTE - If this patent covers an invention made by a corporate employee of a NASA Contractor, the following is applicable:

YES ☑  NO ☐

Pursuant to Section 305(a) of the National Aeronautics and Space Act, the name of the Administrator of NASA appears on the first page of the patent; however, the name of the actual inventor (author) appears at the heading of column No. 1 of the Specification, following the words "...with respect to an invention of ..."

Bonnie L. Woerner  
Enclosure
FOUR-PHASE LOGIC SYSTEMS

Inventors: George M. Low, Administrator of the National Aeronautics and Space Administration, with respect to an invention of; Howard L. Petersen, 13192 Paramount Drive, Saratoga; Donald K. Kinell, 2420 Whitney Drive, Mountain View, both of Calif.

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ABSTRACT

A four-phase logic system is provided which includes at least four logic networks connected in parallel between a single power line and a reference potential. A four-phase clock generator generates four distinct clock signals from a single-phase clock input at data rate. Each logic network comprises a pair of complementary metal-oxide-semiconductor integrated transistors (CMOST). Each metal-oxide-semiconductor transistor (MOST) in the pair is responsive to a clock signal which turns the transistor ON or OFF. In each network there is also at least one MOST which is responsive to a logic signal. The logic transistor is connected in cascade with the pair of CMOSTs. A stray capacitance which serves as a storage capacitor between the junction of the pair of transistors and a reference potential provides an output signal dependent upon the applied clock signals and the incoming logic signal.

3 Claims, 11 Drawing Figures
FIG. 4.

FIG. 5.

FIG. 6.

FIG. 7.

FIG. 8.
FIG. 9.

\[
\begin{align*}
S_1 &: V_{dd} - 0 \\
\phi_1 &: V_{dd} - 0 \\
\phi_2 &: V_{dd} - 0 \\
\phi_3 &: V_{dd} - 0 \\
\phi_4 &: V_{dd} - 0
\end{align*}
\]

PROPAGATION DELAY TIME

TIME \rightarrow

FIG. 10.

\[
\begin{align*}
S_1 &\rightarrow \overline{S_1} * S_1 = \phi_1 \\
S_2 &\rightarrow \overline{S_2} * S_2 = \phi_2 \\
\overline{S_1} &\rightarrow \overline{S_1} * S_2 = \phi_3 \\
\overline{S_2} &\rightarrow \overline{S_2} * S_3 = \phi_4
\end{align*}
\]

SYMMETRICAL
ONE PHASE INPUT
FOUR-PHASE LOGIC SYSTEMS

ORIGIN OF THE INVENTION

The invention described herein was made in the performance of work under a NASA contract and is subject to the provisions of Section 305 of the National Aeronautics and Space Act of 1958, Public Law 85-568 (72 Stat. 435; 45 U.S.C. 2457).

BACKGROUND OF THE INVENTION

MOS integrated micro circuits are highly desirable because they allow high-component packing density on a single chip. P-channel, MOST, four-phase logic networks are known. Such prior art four-phase logic networks require for their operation a four-phase clock generator driven by at least two, single-phase, clock signals at the data rate. Consequently, such prior art four-phase circuits cannot be used as sub-assemblies in such logic systems which cannot accommodate a four-phase clock generator requiring two or more clock inputs. Known, P-channel, four-phase logic circuits also have the further disadvantage of requiring two distinct power supply voltages. Since bi-polar logic employs only a single supply voltage, it is apparent that the requirement for two power supply voltages makes it rather difficult to interface conventional bi-polar logic systems with four-phase logic systems.

It is therefore an object of the present invention to overcome the above-described and other apparent drawbacks of known four-phase MOST logic systems.

SUMMARY OF THE INVENTION

The objects of the invention are accomplished by generating the required four-phase on a single chip from a single phase clock at the data rate. Accordingly, this invention makes possible CMOST logic implementation with a single standard bi-polar logic voltage supply. Hence, the invention can be easily interfaced with bi-polar logic, MOST static logic, and MOST two-phase logic. The invention can also be used to replace directly logic sub-assemblies in systems designed for other logic types. In the invention, the CMOST semiconductor devices act as switches to charge and discharge their storage capacitors in the desired sequence of operation.

In a preferred embodiment, the four-phase logic system itself includes at least four logic networks connected in parallel between a single power line and a reference potential. A four-phase clock generator generates four distinct clock signals from a single-phase clock input at data rate. Each logic network comprises a pair of CMOSTs. Each MOST in the pair is responsive to a clock signal which turns it ON or OFF. In each network there is also at least one additional logic MOST, responsive to a logic signal, which is connected in cascade with the pair of CMOSTs. A storage capacitance between the junction of the pair of CMOSTs and a reference potential provides an output signal dependent upon the applied clock signals and the incoming logic signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a four-phase logic system including four distinct types of logic networks; FIG. 2 shows a modified embodiment of a logic network; FIG. 3 is a block representation of a four-phase clock generator; FIG. 4 represents typical wave forms of the four phases obtained from the generator of FIG. 3; FIG. 5 shows a preferred embodiment of a clock generator for producing the desired phases; FIG. 6 shows a typical CMOST inverter of a type which can be used in the generator shown in FIG. 5; FIG. 7 depicts the input and output waveforms of the generator shown in FIG. 5; FIG. 8 is a logic gate network with the generator shown in FIG. 5 for producing the desired phase signals from the clock signals; FIG. 9 depicts the input and output waveforms from the gate network shown in FIG. 8, and FIGS. 10 and 11 are, respectively, similar to FIGS. 8 and 9 but for a different input clock signal.

Referring now to FIG. 1, there is shown a four-phase logic system employing MOSTs and CMOSTs. The phases or clock pulses are herein referred to as the $\phi_1$, $\phi_2$, $\phi_3$, and $\phi_4$ phases. The present invention is particularly concerned with a system 10 using four basic logic networks or elements 12-15, each logic element employing a pair of opposite polarity MOST's known as P-channel and N-channel. Networks 12-15 are herein referred to as TYPES 1-4, respectively. Each of the logic elements 12-15 comprises at least three MOSTs $Q_1$, $Q_2$, and each logic element stores its information in the stray capacitances of the MOSTs which are lumped for the sake of the drawing into a single storage capacitor designated as C and followed by an appropriate subscript corresponding to the number of the particular TYPE of logic element.

Logic systems of the kind to which this invention relates are particularly adapted for integrated circuits in which a considerable number of logic functions can be performed by a single integrated circuit unit or chip. As previously mentioned, this invention makes it possible to provide four-phase logic systems on single chips and such chips can then be interconnected with different kinds of logic elements or systems mounted on other chips in which capacitors are used as the memory storage elements.

Each logic TYPE comprises a logic MOST connected in series with a pair of MOSTs of opposite polarity, that is with a pair of complementary MOSTs herein called CMOSTs. Each CMOST receives one clock pulse or phase and each consecutive pair of CMOST's receives the same phase. As previously mentioned, there are four phases $\phi_1$-$\phi_4$, and the junction between the two CMOSTs can provide on an output lead an output pulse for each logic TYPE. The stray capacitance of the chip between the output lead and ground store the logic information in the logic TYPE.

More specifically, TYPE 2 logic element comprises in a simplified embodiment three MOSTs $Q_1$, $Q_2$, with $Q_1$, $Q_2$ forming the CMOST pair and $Q_2$, receiving a LOGIC input at 9. The TYPE 2 logic element is connected between a reference potential $V_0$, typically ground, and a power supply bus 7 maintained at $+V_0$.

The stray capacitance 8 is represented as a capacitor $C_1$ connected between ground and the output lead OUT, at the junction of the CMOST pair. MOST $Q_2$ receives a phase or clock pulse $\phi_2$ at 4 and MOST $Q_2$ receives a clock $\phi_1$ at 3.
The TYPE 3 logic element similarly includes three MOSTS Q₁₋₂₅ with the logic receiving MOST being Q₂. It will be noted that Q₁ in TYPE 2 and Q₂ in TYPE 3 receive the same clock φ₁. In the TYPE 4 logic element, the logic receiving MOST is Q₂, and in the TYPE 1 the logic receiving MOST is Q₅. With one logic receiving MOST, a logic input A becomes an output A.

In FIG. 2 is shown a variation of the TYPE 2 logic element in which three transistors Q₁₋₂₅ are substituted for the single logic transistor Q₁. Transistors Q₁₋₂₅ respectively receive logic inputs C, A, and B and provide an output AB+C. It will therefore be apparent that more than three MOSTs can substitute for each logic transistor to accommodate more complex logic inputs.

Referring now to FIGS. 3 and 4, there is shown a four-phase clock generator 20 receiving a one-phase clock input on line 22 and providing four output clocks or phases φ₁₋₄ such as are needed for the logic system 10 of the invention shown in FIG. 1. A one-phase clock input is illustrated in FIG. 4 as being a repetitive rectangular wave which starts at T₁. The clock φ₁ is at the supply potential at time T₁ at which time it changes to zero potential and remains at zero potential until time T₂ at which it returns and remains at the supply potential for the duration of the period of the one-phase clock input. The clocks φ₂₋₄ relative to the clock φ₁ are depicted in FIG. 4. The width of each clock is such as to allow sufficient time for charging and discharging of capacitors C₁₋₄ (FIG. 1). The total width of all four clocks in the time domain is less than the time period of the one-phase clock input on line 22. Also the clock pulses are displaced in the time domain so as not to overlap. It should now be apparent that since the four required phases are generated from a single one-phase clock input, the clock generator 20 and the four-phase logic system 10 can be fabricated on a single chip.

In FIG. 5 are shown seven CMOST inverters connected in cascade. The input signal is designated as S₁ and each output signal is designated with an appropriate subscript to indicate its position in the chain. An asterisk following an output designates that the output is potential. A ZERO logic input which effectively holds Q₁ at ground potential. Depending on the logic input, the clock generator 20 and the four-phase clock generator 20 on the same chip with the logic system 10 (FIG. 1), there will now be described the operation of system 10 together with the waveforms depicted in FIG. 4.

Capacitor C₄ is charged and discharged through CMOSTs Q₄₋₅ during time interval T₆-T₇, the application of clock φ₂ causes Q₅ to switch ON since φ₂ is at ground potential, while Q₄ remains OFF. Capacitor C₅ charges to the supply potential Vᵈ through MOST Q₅. After time T₇, MOST Q₅ is switched OFF by φ₃ and capacitor C₅ stores its potential. During time interval T₆-T₆, is switched ON by φ₇. Depending on the LOGIC input, MOST Q₃ will be switched either ON or OFF. If the logic input is a ONE, Q₃ will turn ON thereby completing a path to ground through Q₂, and capacitor C₃ will discharge to ground potential. On the other hand, if the logic input is a ZERO, Q₃ will switch OFF, and capacitor C₃ will remain charged. The stored information in capacitor C₃ is available for readout from time T₃ to time T₆.

Thus it will be appreciated that C₃ in the TYPE 2 logic element is precharged during clock φ₂; it is evaluated, that as it can be modified or allowed to remain the same during clock φ₃, and it is available for readout during φ₄ and φ₅. Q₃ will again be precharged at the next φ₂, etc. It can be stated therefore that the TYPE 2 logic element operates as an inverter which is precharged during time interval T₃-T₅, evaluated during interval T₅-T₆, and valid during interval T₆-T₇.

The TYPE 3 logic element operates in a similar manner: capacitance C₅ is charged and discharged through CMOSTs Q₅₋₆ during time interval T₆-T₇. Q₅ is switched ON by φ₇ at +Vᵈ, while Q₆ remains OFF since φ₇ is also at +Vᵈ. Thus C₅ is charged to ground potential.

After time T₆, Q₄ is switched OFF and C₃ stores its ground potential. During time interval T₉-T₁₀, Q₄ is switched ON by φ₈ at ground potential. Depending on the LOGIC input to Q₃, C₃ will remain at ground potential for a ONE input which effectively holds Q₃ OFF, or C₃ will charge to +Vᵈ for a ZERO logic input which turns Q₃ ON and completes a path to +Vᵈ through Q₃ and Q₆.

The potential on C₃ provides OUTPUT₃, and from time interval T₉-T₁₀, both Q₃ and Q₄ are OFF, thereby isolating the information on C₃. OUTPUT₃ is valid for readout during T₆-T₇. Thus, the TYPE 3 network also operates as an inverter which is precharged during interval T₆-T₇, evaluated during interval T₅-T₆, and valid during interval T₆-T₇.

It will be noted that the TYPE 4 logic element is similar to the TYPE 2 logic element. The TYPE 4 logic element operates as an inverter which is precharged during time interval T₆-T₇, evaluated during interval T₅-T₆, and valid during interval T₆-T₇. It will also be noted that the TYPE 1 and TYPE 3 logic elements are similar. TYPE 1 operates as an inverter which is precharged during interval T₅-T₆, evaluated during interval T₆-T₇, and valid during interval T₆-T₇.
While the logic networks 12–15 shown in FIG. 1 operate as simple inverter circuits, they are also capable of performing more complex logic functions by replacing the single logic MOST such as Q1 or Q2, etc., in each of the logic networks 12–15 with a more complex MOST logic circuit, for example as depicted in FIG. 2, wherein is shown a TYPE 2 logic element for generating an output AB+C.

As shown in FIG. 2, C2 is charged to the supply voltage $V_{dd}$ during the time interval $T_{1} - T_{2}$. Depending on the state of the logic inputs A, B and C during time interval $T_{2} - T_{3}$, Q13, Q14, and Q15 will be switched either ON or OFF. To discharge C2, either Q13 alone must be ON or Q14 in series with Q15 must be ON. All three MOST's Q13–Q15 are operative during the evaluation interval $T_{3} - T_{4}$ when Q2 is ON. In sum, capacitor C2 discharges for AB+C and a ZERO output represents the complement of AB+C that is AB–C.

Other logic functions may be synthesized using combinations of MOSTs as necessary. It will be noted that the combination shown in FIG. 2 produces the NOR function as well as the NAND function. Extensions of the simple circuit of FIG. 2 can produce most logic functions which may be desired in practice.

It will be appreciated that in using complementary MOST four-phase logic, successive phase intervals are used to precharge and evaluate a logic element TYPE.

The output of a particular logic element TYPE is valid for the next two clocks. The clocks are so arranged that only one logic element is evaluated during each phase.

The TYPE 1 logic element is evaluated during $\phi_1$, TYPE 2 during $\phi_2$, TYPE 3 during $\phi_3$, and TYPE 4 during $\phi_4$.

Thus the output of a specified logic element TYPE can be applied to the inputs of two logic element TYPES. For example, a TYPE 1 logic element can be used to provide an input to a TYPE 2 or a TYPE 3 logic element. A TYPE 2 can be used to provide an input to a TYPE 3 or a TYPE 4. A TYPE 3 can be used to provide an input to a TYPE 4 or a TYPE 1, and a TYPE 4 can be used to provide an input to a TYPE 1 or a TYPE 2.

Referring to the operation of the inverter network shown in FIG. 5 and the phase generating logic of FIG. 8 and for an asymmetrical 1-phase input clock, $S_1$, $\phi_1$ is generated from this single phase input by the logic function $\phi_1 = S_1 S_1^*$, where $S_1$ and $S_1^*$ are slightly delayed by the propagation time of the input clock. Clock $\phi_1$ is false only if both $S_1$ and $S_1^*$ are true, a condition which exists only during the delay interval after $S_1$ becomes true. Similarly, $\phi_2 = S_2 S_2^*$ and $\phi_3 = S_3 S_3^*$ is true only during the delay interval after $S_2$ becomes true.

Similarly, $\phi_4$ is false only during the delay interval after $S_3$ becomes true. FIG. 9 shows the waveforms of the input and outputs.

For a symmetrical one-phase input clock and the phase generating logic as shown in FIG. 10, the logic functions for $\phi_1$ and $\phi_2$ are the same as previously described. However, $\phi_3$ and $\phi_4$ are now generated for the other half cycle of the one-phase input by functions $\phi_3 = S_1 S_2^*$ and $\phi_4 = S_2 S_3^*$.

In this case, $\phi_3$ is false only for the delay interval after $S_1^*$ becomes true. Also, $\phi_4$ is true only for the delay interval after $S_2^*$ becomes true. FIG. 11 shows the waveforms of the input and output for the symmetrical one-phase input.

It will be appreciated that the above described embodiments are for specific logic implementation and are only illustrative of the principles of the invention. Persons skilled in the art may effect various modifications without departing from the spirit and scope of the invention as defined in the claims attached hereto.

What is claimed is:

1. A four-phase logic system comprising:
   - at least four logic networks connected in parallel between a voltage source and a reference potential;
   - each said logic network including a pair of CMOSTS, and a logic MOST circuit connected in series with the pair of CMOSTS, and wherein each said pair comprises a P type conductivity transistor and an N type conductivity transistor with their conductive paths in series connection adjacent series CMOST pairs and logic MOSTS alternating in position in said series between said voltage source and said reference potential;
   - a four-phase clock generator adapted to generate a four-phase clock waveform signal from a single phase input clock waveform signal, each said CMOST in each pair of CMOSTS being respectively coupled to adjacent phases of said clock generator which turns it ON and OFF;
   - each said logic MOST circuit being responsive to a logic input signal, and each junction terminal between each pair of CMOSTS constituting an output terminal for its associated logic network with the stray capacitance between said junction terminal and the reference potential constituting a storage means for storing the desired logic output of said associated logic network where it is available for readout from said output terminal.

2. A four-phase logic system as defined in claim 1 wherein first and second phases of said clock generator output are coupled to different control electrodes of the pair of said CMOSTS in the first of said logic networks, second and third phases of said clock generator output are coupled to different control electrodes of the pair of said CMOSTS in the second of said logic networks, third and fourth phases of said clock generator output are coupled to different control electrodes of the pair of said CMOSTS in the third of said logic networks, and said first and fourth phases of said clock generator output are coupled to different control electrodes of the pair of said CMOSTS in the fourth of said logic networks.

3. A four-phase logic system as defined in claim 2 wherein an electrode of the serially connected pair of CMOSTS of said first logic network and said third logic network are coupled directly to said voltage source in a conductive path therewith and said voltage source is coupled directly to an electrode in the conductive path of a logic MOST in the logic MOST circuit of said second logic network and to an electrode in the conductive path of the logic MOST circuit of said fourth logic network.