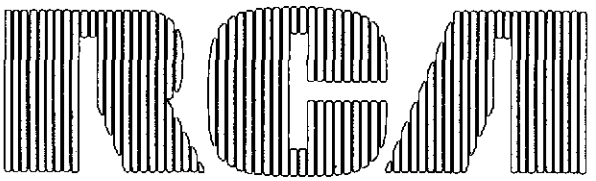


Contract No. NAS 9-13576

Tracking Techniques for Space Shuttle Rendezvous

FINAL REPORT

Prepared for

NASA Lyndon B. Johnson Space Center
Houston, Texas

RCA | Government and Commercial Systems
Government Communications and Automated Systems Division
Burlington, Massachusetts

Contract No. NAS 9-13576
FINAL REPORT

Tracking Techniques for Space Shuttle Rendezvous

Prepared for

NASA Lyndon B. Johnson Space Center
Houston, Texas

RCA | Government and Commercial Systems
Government Communications and Automated Systems Division
Burlington, Massachusetts

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont.)

TABLE OF CONTENTS (Cont.)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont.)

FOREWORD

This final report is submitted under Contract NAS9-13576 from National Aeronautics and Space Administration, Lyndon B. Johnson Space Center, Houston, Texas. This report supersedes the interim report TTR No. 1 dated July 1974, since both the work reported there and the work performed subsequent to that date are covered in this report.

PART I

INTRODUCTION

1.1 OBJECTIVE

The purpose of this effort was to study the system approach, and implement and evaluate the changes necessary to add the non-cooperative mode capability with frequency diversity to the Apollo Rendezvous Radar while retaining the cooperative mode capability.

1.2 BACKGROUND

Shuttle rendezvous operations involving spacecraft such as scientific satellites, space stations, and disabled or powered-down spacecraft will require an on-board rendezvous tracking system. The rendezvous tracking system must have the capability of tracking both non-cooperative and cooperative targets. When it is determined that regularly scheduled rendezvous operations with any given orbiting spacecraft will be required, a transponder would be attached to enhance the range and accuracy capabilities of the system. The tracking system must be capable of supplying range, range rate, and angular information of the target to the on-board Shuttle Guidance and Navigation System.

1.3 CONCLUSIONS

The space-proven Apollo-type Rendezvous Radar has been modified to operate in both a cooperative and a non-cooperative mode, with frequency diversity in the latter mode. Tests have shown that the system performs as intended, and in particular that the concepts of range measurement by tone modulation, coherent ICW operation at a high prf to provide transmitter-receiver isolation, and frequency diversity all are compatible and operate together without interference, as the analysis has indicated. This program has been

successfully completed at a very modest cost by avoiding a number of investigations, system optimizations and system modifications which eventually must proceed, but which are not essential to this basic feasibility demonstration.

1.4 RECOMMENDATIONS

In order that the Space Shuttle program can take full advantage of the desirable features which this type of radar can provide, futher work is recommended along several lines. These include further testing and possible minor modifications using the radar in its present form, addition of features which better optimize the performance in the non-cooperative mode, testing under more realistic simulated target conditions, and system analysis with computer simulation of critical system operations. The following paragraphs list these items.

Items which are very desirable to facilitate system testing are as follows.

- Variable doppler sweep limits — this will prevent the frequency search from sweeping through the clutter band at zero doppler, thus aiding system testing in a clutter environment, and still permit testing at zero doppler in a non-radiating setup.
- Display and recording of control logic — permitting monitoring of the various steps in the target detection, acquisition, and tracking sequences, which although not important in the final application is of interest in developmental testing.
- Manual target designator — an optical sight with suitable angle pickoffs and interface with the radar will provide a necessary means of pointing the radar beam or the scanned sector at any desired direction or target, including moving targets.
- Acquisition display — a two dimensional display of angle coordinates permits an indication of the target direction (obtained from the above manual target designator) and the actual radar beam as it proceeds through the scan pattern. This is

necessary to be able to effectively control and monitor the acquisition of a stationary target, and is essential if the target is moving, or if a short range target is to be acquired and detection is possible in a side lobe.

- Fluctuating target simulator — a target simulator with provision for target area fluctuation and for the effects of frequency diversity is very desirable. Simulation of the target extended in the range direction is also desirable, but less important.

Items which accomplish system performance improvements related to the modifications already made are as follows. These items are related to the conversion of the radar to provide the non-cooperative target capability, but were deferred in the interest of proving concept feasibility at low cost. The evaluation of tests on the equipment in its current form, which does not include these items, should recognize corresponding limitations in areas related to these items.

- Servo loops — the moments of inertia on the two gimbals were altered, without changing the servo loop compensation. Speed of response and stability can therefore be improved.
- Angle scan parameters — preliminary calculations suggest that more uniform acquisition performance can be obtained if the raster line spacing is reduced, at the cost of reduced coverage. Test conditions should be reviewed to determine if it is desirable to alter the scan parameters.
- Data-good logic — the existing logic was developed for the cooperative mode, so some revision is to be expected to obtain proper operation with the target fluctuations present in the non-cooperative mode.
- AGC — this also was designed for the cooperative mode, and some improvement in system performance can be obtained by adjusting its parameters and characteristics to operate with a fluctuating target, with frequency diversity, and with a short range mostly-eclipsed target.

- Optimization using target simulator - all of the above system design items should be optimized in the laboratory, and the performance verified, on a fluctuating target simulator such as was mentioned in the preceding list related to system testing.

Items consisting of added features which, although not essential to proving feasibility, are required in an eventual implementation, are listed as follows. All of these items have a strong potential for expanding system performance, so that although no large development risk is involved it is very worth while to proceed on them to pave the way for optimum design of the eventual system.

- Doppler filter bank - providing a bank of detection filters, rather than a single swept-frequency filter as currently implemented, will greatly speed the search process. This affects the frequency lock on logic.
- Low PRF in search mode - this eliminates eclipsing loss in the search mode for nominal maximum range targets. It has a minor impact on the acquisition logic due to operation in the ambiguous doppler condition.
- Multiple-tone usage in range tracker - the present logic for controlling the use of the several range tones is adapted with minimum change from the cooperative-mode configuration. A few instances have been observed where an improper range lockup has occurred. The different conditions connected with signal fluctuation and a different signal demodulation method dictate that the tone usage logic should be reviewed to select the best techniques.
- Positive PRF control during tracking - for expediency the present method is to cycle through PRF's whenever the signal level drops below a programmed threshold, so that tracking of a fluctuating target can be significantly improved by selecting the PRF on the basis of measured range.

PART II

ABSTRACT

The space shuttle rendezvous radar has a requirement to track cooperative and non-cooperative targets. For this reason the Lunar Module (LM) Rendezvous Radar has been modified to incorporate the capability of tracking a non-cooperative target. The modifications include the following.

Radar

(1) Addition of a higher power pulsed transmitter at the transponder transmit frequency 9792 MHz.

(2) Gating off the receiver during the transmitter on time.

(3) Additional processing of the received signal to extract the ranging tones and to frequency lock the receiver to the received signal from a fluctuating target in the non-cooperative mode.

(4) Providing frequency diversity by generating additional transmitter and local oscillator frequencies, thus minimizing the effects of target fluctuation.

(5) Provide a scan generator to scan the radar through the volume of uncertainty of target location.

Special Test Equipment

(1) Pulse modulation of simulated target signal with time delay corresponding to simulated target range.

(2) Frequency diversity simulation.

The radar modifications were done in two phases. In the first phase all modifications except those relating to frequency diversity were completed, and system tests were performed to confirm proper performance in the non-cooperative mode. In the second phase frequency diversity was added to the radar and to the special test equipment, and then system tests were performed. This last set of tests included re-running the tests of the non-cooperative mode without frequency diversity, followed by tests with frequency diversity and tests of operation in the original cooperative mode.

PART III

EQUIPMENT MODIFICATIONS

1.0 INTRODUCTION

The Rendezvous Radar herein described is an extension of the unit designed for the Apollo Mission. It differs from the original design in that a non-cooperative target mode with frequency diversity has been added. Figure III-1 is a block diagram of the modified radar.

The Rendezvous Radar (RR) is a lightweight, highly reliable, accurate, space stabilized, coherent tracking radar which operates in either the Transponder Mode where it acquires its associated Transponder located on board the target vehicle, or it coherently skin tracks a non-cooperative target. After acquisition it automatically tracks while supplying angle, angle rate, digital range data, and range rate data to the guidance computer and/or the astronauts displays.

In the cooperative mode the RR and the Transponder (T) each utilize solid state varactor multipliers as transmitters, with the transmission and reception on a CW basis.

In the non-cooperative mode the radar uses a TWTA as a final output transmitter stage. This provides the higher power required for skin tracking. Since reception and transmission are at the same frequency. The receiver is gated off during the transmit time. Transmission is performed at the five different PRFs to minimize eclipsing losses. Transmitter duty cycle is approximately 40 percent. Five transmit frequencies are used to minimize the effects of fluctuating targets.

Gyros which are located on the RR antenna stabilize the line-of-sight (LOS) against the effects of body motions, and permit accurate measurements of LOS angular rate.

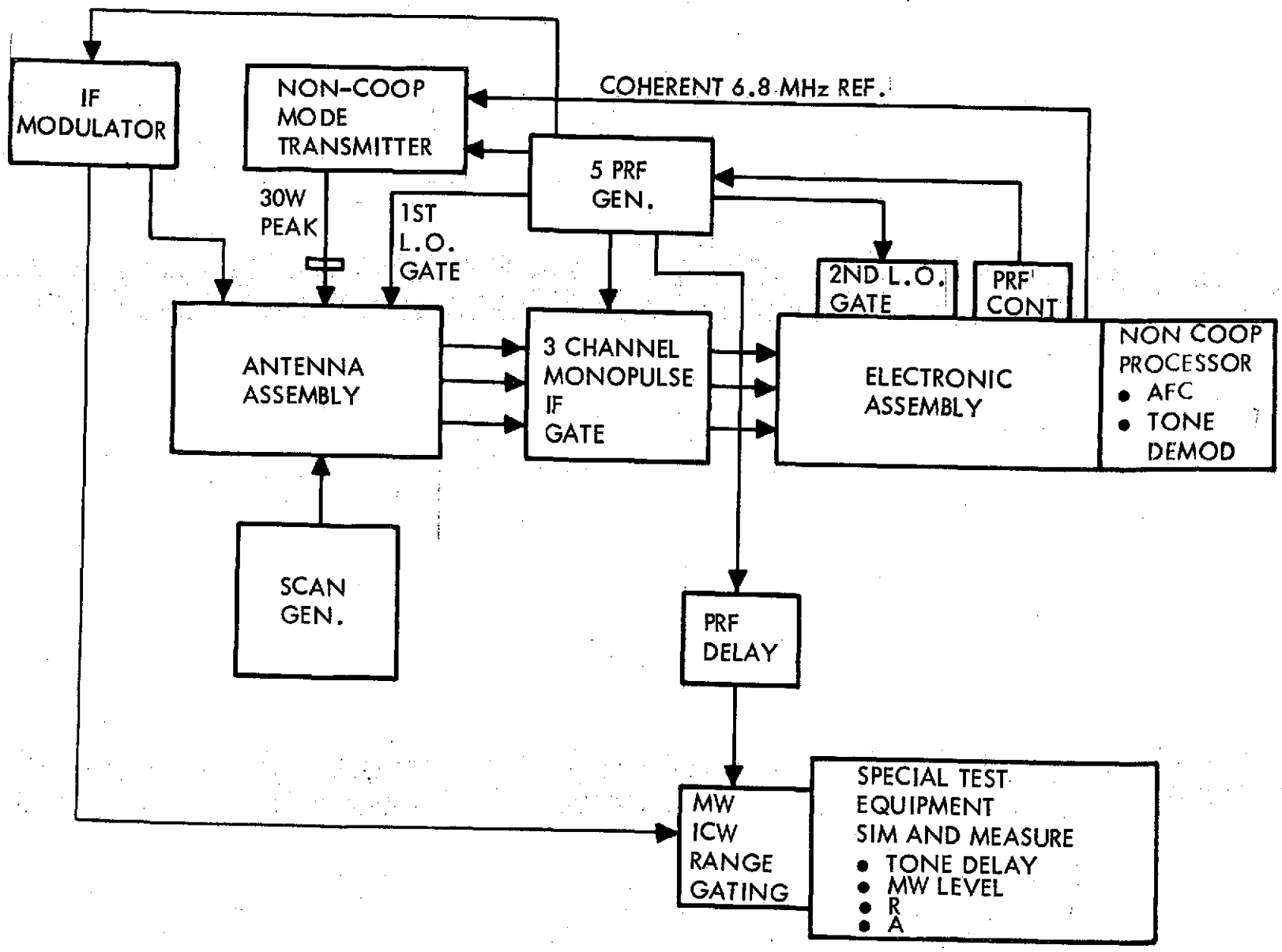


Figure III-1. Simplified Block Diagram, LM Radar Modified for Non-Cooperative Tracking

Angle tracking is accomplished by using the technique of amplitude comparison monopulse (or simultaneous lobing) to obtain maximum angular sensitivity and boresight accuracy. Range Rate is determined by measuring the two-way doppler frequency shift on the signal received from the target. Range is determined by measuring the time delay between the transmitted signal modulation waveform and the received signal waveform utilizing a multi-tone phase modulation.

2.0 MODIFICATIONS TO EQUIPMENT

2.1 RADAR MODIFICATIONS

The transmitter consists of a gated 30 watt gridded TWTA driven by a coherent, pregated, exciter center frequency of 9792 MHz, the other frequencies are ±50 MHz and ±100 MHz. The transmitter is located off the antenna gimbals. Its output is routed to the antenna feed horns using waveguide and rotary joints which have been added at the shaft and trunnion axes. The new transmitter is shown in Figure III-2. This figure also shows the PRF generator which controls the receiver and transmitter on times and the transmit and local oscillator frequencies. The modified antenna assembly, including the added waveguide and joints are shown in Figure III-3. The coupling to the antenna microwave is shown in greater detail in Figure III-4.

Receiver gating was added to prevent the radar from locking to the transmit signal. The receiver is gated off in three steps. The X band local oscillator is turned off using a SPDT PIN diode switch, shown in Figure III-5. This reduces the transmitter leakage by approximately 40 dB and prevents saturation of the mixer preamp. With frequency diversity the local oscillator is stepped in synchronous with transmitter to maintain the IF at 40.8 MHz. The preamp outputs, at 40.8 MHz, can then be gated with phase and amplitude tracking gates to provide further isolation prior to the high gain first IF amplifiers. Finally the second L.O. at 34 MHz, is gated. This combination is adequate to reduce the 6.8 MHz second IF to a level below the receiver sensitivity.

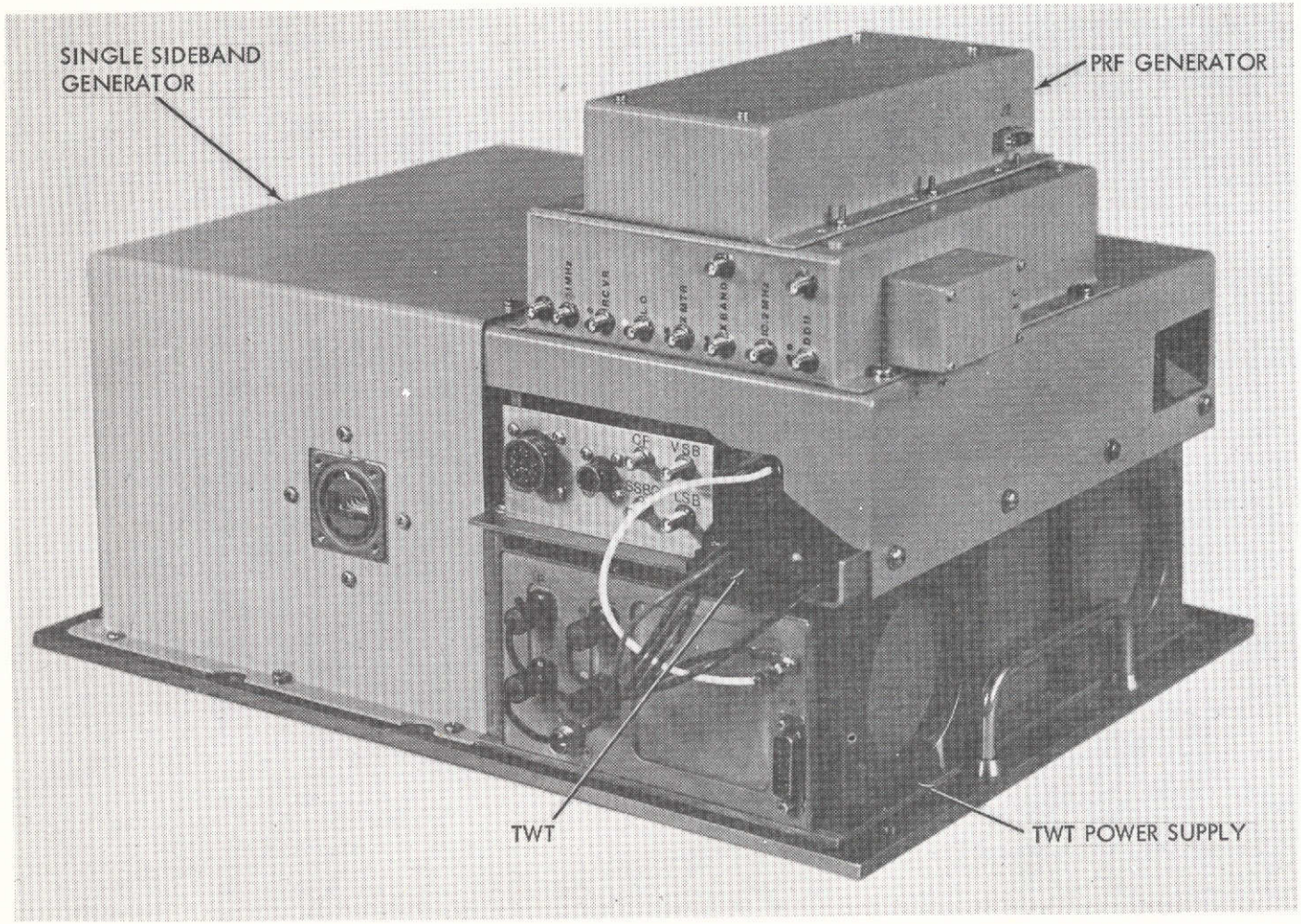


Figure III-2. Non-Cooperative Mode Transmitter

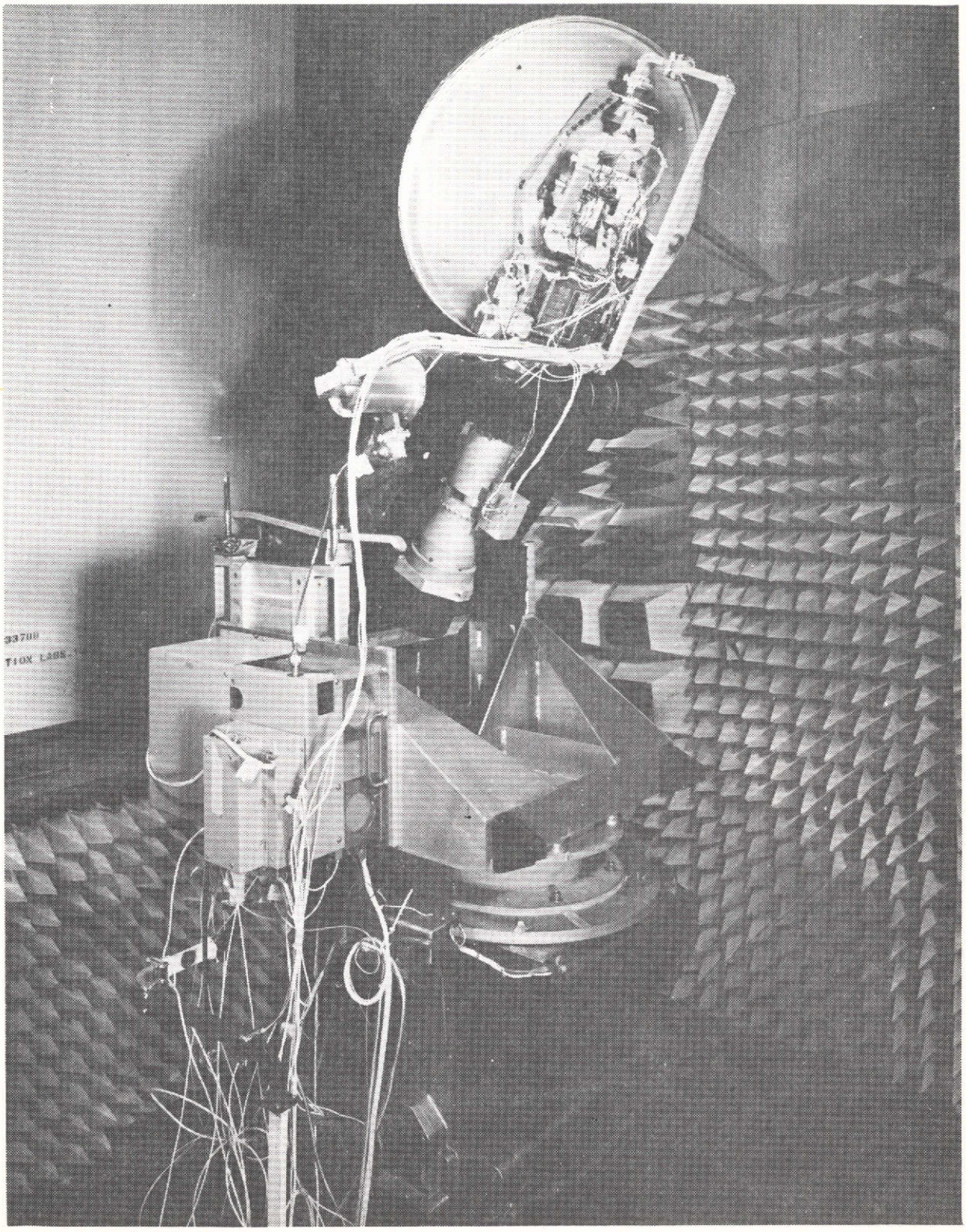


Figure III-3. Modified Antenna Assembly

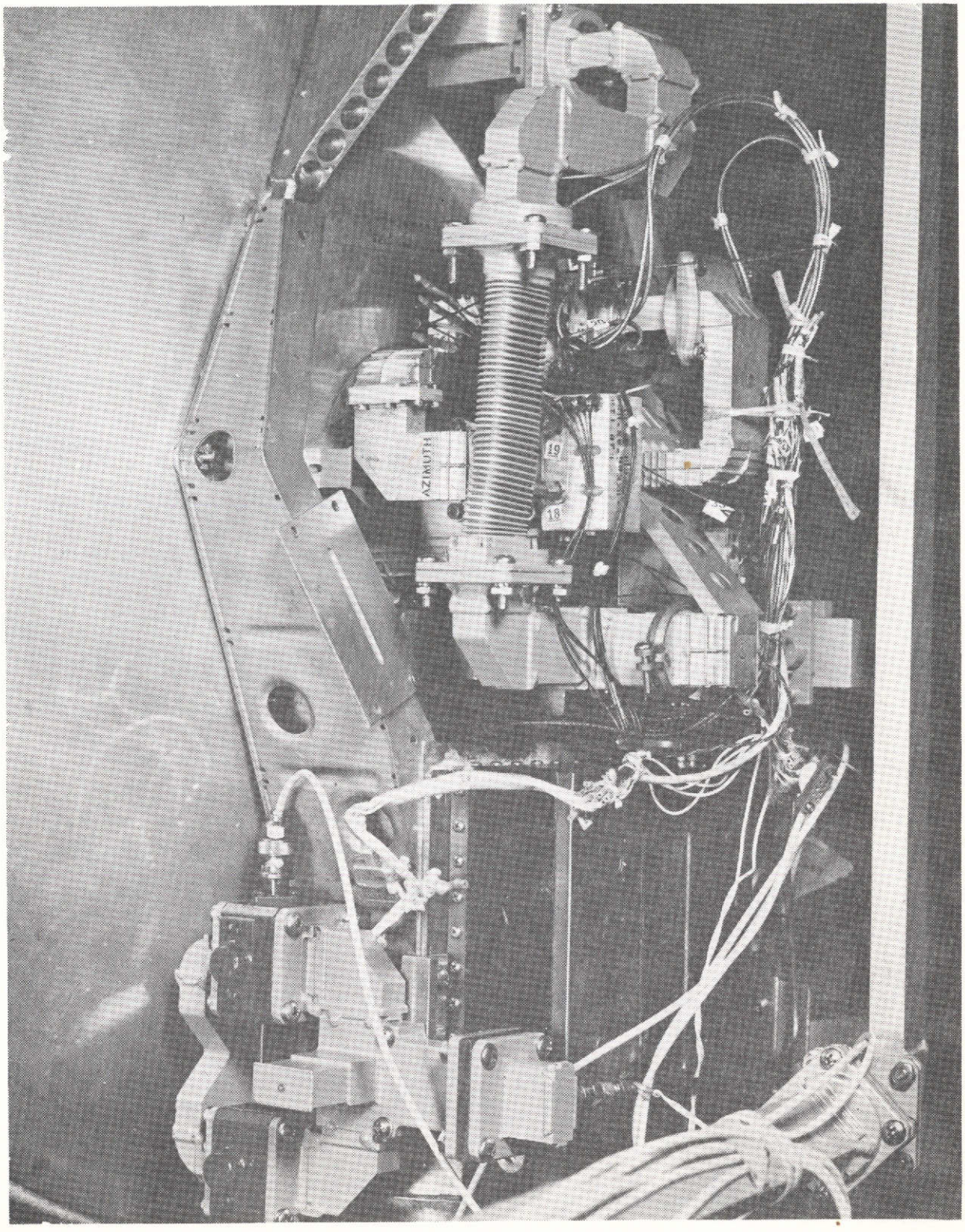


Figure III-4. Waveguide Routing

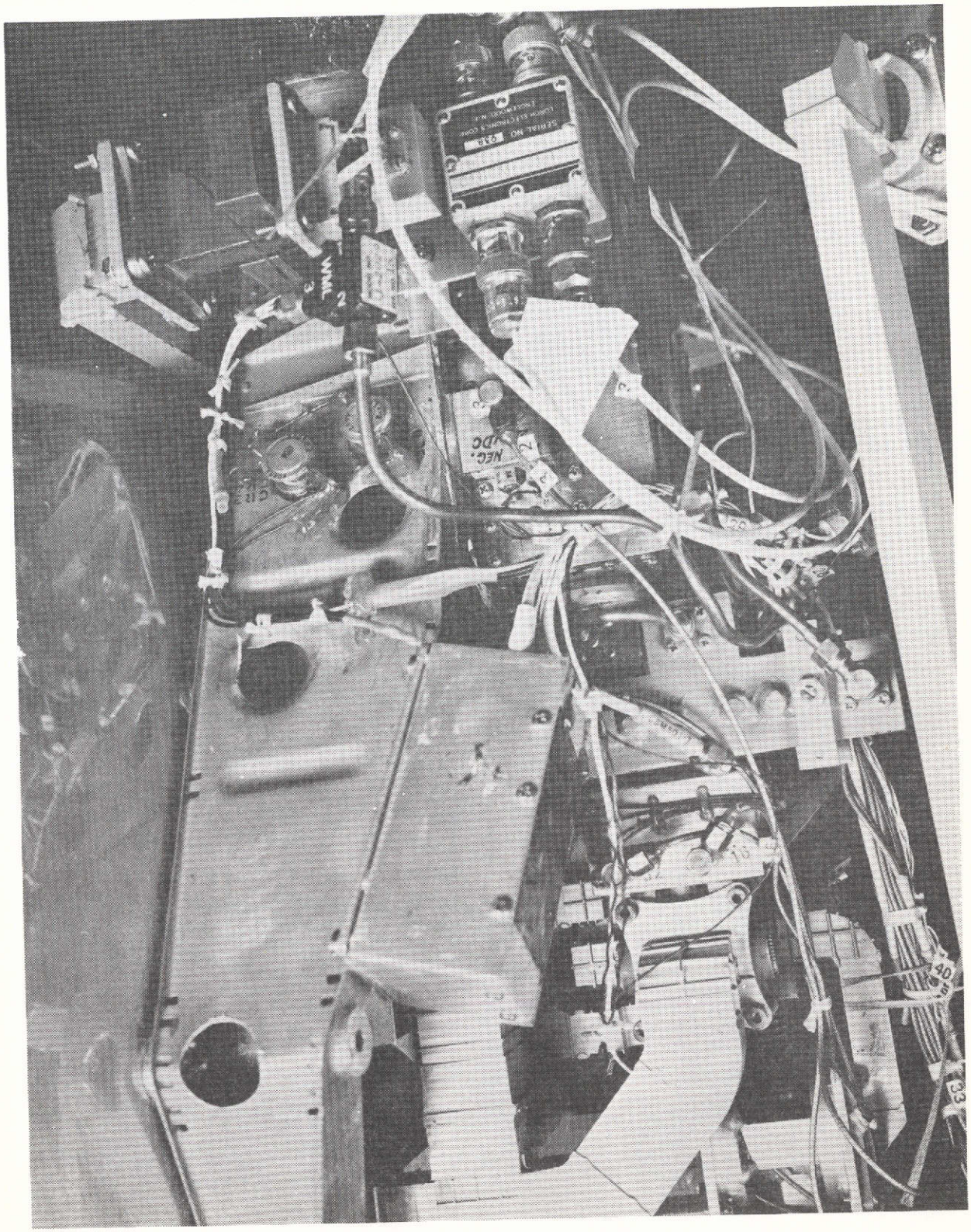


Figure III-5. Pin Diode Switch Location

The signal processor accepts the wideband 6.8 MHz, 2 MHz bandwidth, from the receiver and extracts the ranging tones and an error signal for control of the doppler measuring VCO. The received 6.8 MHz signal is applied to five narrow band filters. The center filters passes the carrier and the low frequency, 200 Hz, tone sidebands. Two additional filters pass the upper and lower sideband associated with the mid frequency, 6.4 kHz, tone while the final two pass the high frequency, 204.8 kHz, tone upper and lower sidebands. The filtering increases the signal to noise ratio and removes unwanted modulation sidebands created by the PRF switching. After filtering, the mid and high frequency sidebands are recombined with the carrier to create two tone channels. The channels are limited to remove the unwanted amplitude modulation and applied to two discriminators. The high frequency discriminator extracts the high frequency tone and the mid frequency discriminator extracts the low and mid frequency tones. The tones are then amplified and phase shifted to a level required by the range tracker. The carrier filter output is also limited and applied to a discriminator to produce a frequency error signal. The resultant error signal, after compensation, is applied to the VCO to frequency lock the receiver.

Figure III-6 is a picture of the electronic assembly showing the added assemblies.

The scan generator forces the radar to scan the target uncertainty volume by applying a fixed bipolar voltage to the manual slew inputs of shaft and trunnion. The scan pattern starts from the upper left corner of the volume of uncertainty. After a fixed period of time (approximately 20 degrees) the antenna is stepped down in shaft and the direction of trunnion motion is reversed. This procedure is repeated until the total volume is scanned. The antenna then reverses and scans up from lower right hand corner.

2.2 SPECIAL TEST EQUIPMENT (STE) MODIFICATIONS

In order to test the modified radar it was necessary to provide a simulated target delayed in time relative to the transmit signal. The existing STE was capable of delaying the ranging tones. A digital delay unit was added which delayed the transmit pulse, to simulate range delay. This delayed pulse gated the simulated signal in the STE to simulate the target

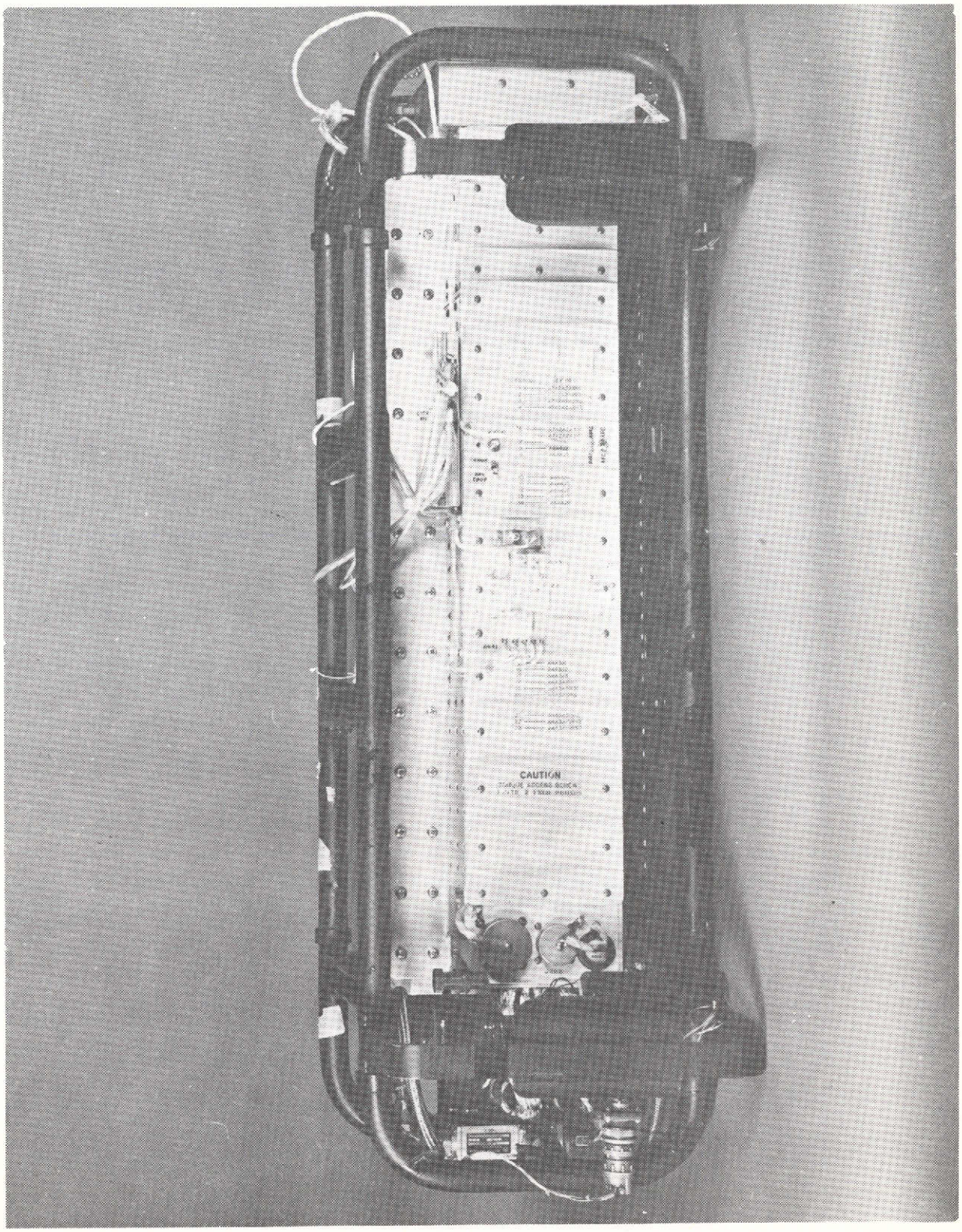


Figure III-6. Electronic Assembly

return. The simulated target was modified to provide the 5 frequency diversity signals at the same frequency as transmitted plus doppler which are used for target return signals.

2.3 PERFORMANCE

Radar performance was verified using the simulated target at various ranges from 100 ft to 7 nautical, with the transmitter active. Since reflected targets in the area interferred with the simulated signal, the synthetic target signal was injected using the RR hat coupler. The radar also tracked the reflected signal from an aluminum coated cube located 100 feet from the radar. The radar also tracked several reflected targets in the area. The ability of the radar to acquire the simulated target from the scan was also verified. For further details of the test results see section 4.0 pages 23 through 48.

3.0 GENERAL EQUIPMENT DESCRIPTION

The radar consists of five main assemblies: Antenna Assembly, Electronic Assembly, Transmit-Exciter/Control, Transmitter Assembly and scan generator. A brief description of the major functions follows, and reference should be made to the detailed block diagram Figure III-7.

3.1 ANTENNA ASSEMBLY

The RR Antenna assembly includes the usual microwave radiating and gimballing elements in addition to internally mounted gyros, resolvers, multiplier chains, frequency diversity single side band generator, modulators and mixer preamplifiers. Except for the waveguide required for the high power transmitter in a non-cooperative mode, flexible low frequency coaxial cables are used to connect the outboard antenna components to the inboard electronics assembly. A flexible cable wrap-up system is used to achieve rotation about each axis.

The Antenna is a four-horn amplitude comparison monopulse type. The Cassegrain configuration is used to minimize the total depth. The antenna transmits and receives

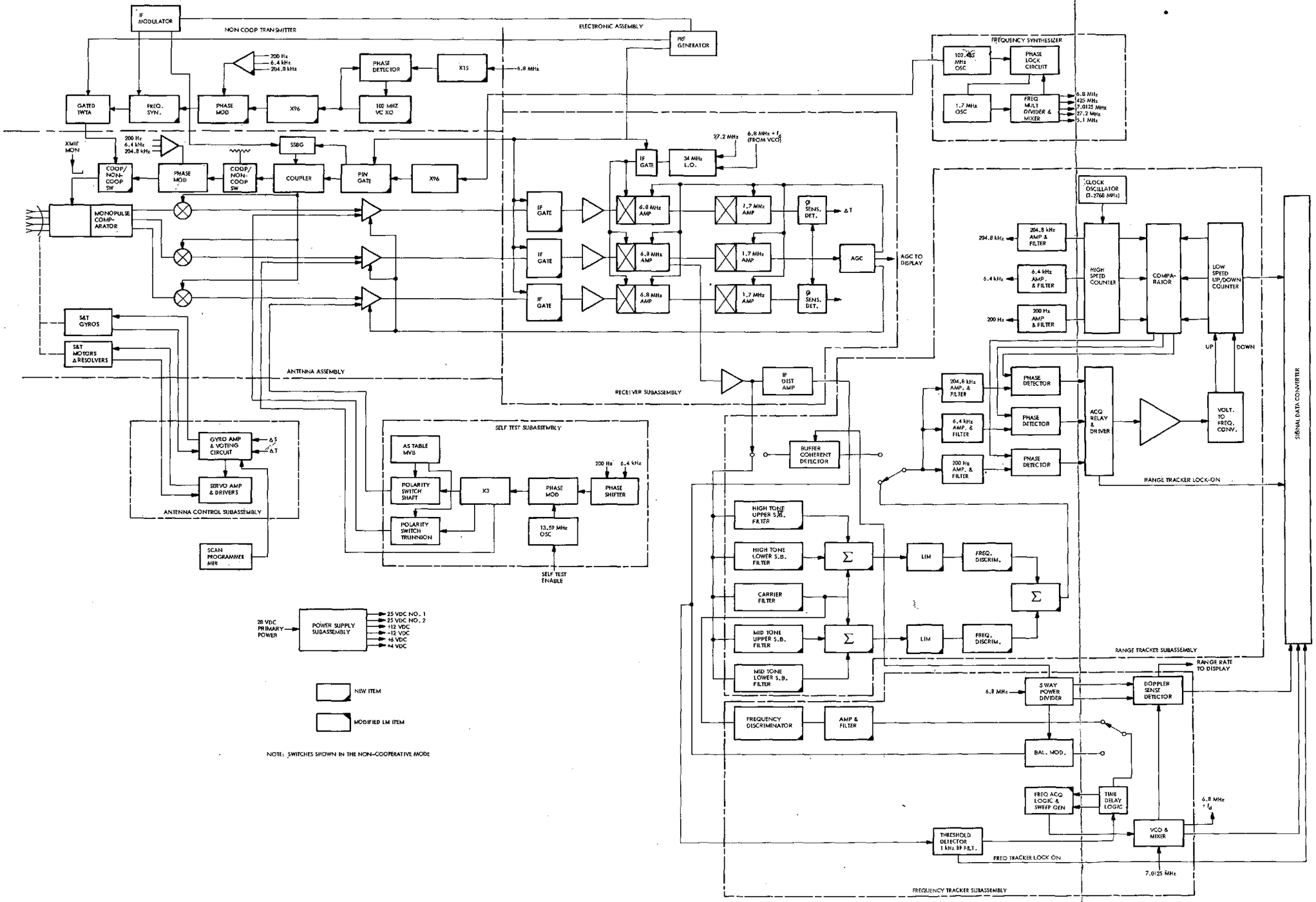


Figure III-7. Block Diagram, Shuttle Radar

circularly polarized radiation to minimize signal variations resulting from attitude changes of the linearly polarized Transponder Antenna. Components are distributed inside the antenna to achieve balance around each axis. Each axis is controlled by a brushless servo motor which is driven by pulse-width modulated drive signals.

Four rate integrating gyros are used for LOS space stabilization and LOS angle rate measurement. These are located in the lower section of the trunnion axis and act as a counterweight. Only two of the gyros are used at any one time and a voting logic system (located in the Electronic Assembly) is utilized to transfer control to the other two gyros in the event of a failure in either of the two gyros being used. The voting logic compares the two active and one of the redundant gyro outputs. A two speed resolver is mounted on each axis for high accuracy angle data pickoff for the computer and for display.

The multiplier chain, phase modulator, and mixer preamplifiers are mounted internally behind the antenna dish. In the cooperative mode the multiplier chain supplies X-band power for radiation and for local oscillator excitation. This is feasible, since the Transponder replies with a frequency side-step equal to the radar first IF frequency. In the non-cooperative mode a separate transmitter displaced from the LO by the IF frequency is provided. The heat dissipated by the multiplier chain is radiated back into space by the dish. The phase modulator utilizes a ferrite rod inside a waveguide and a solenoid for varying the magnetic field inside the rod. The ranging tone signals are applied to the solenoid, which varies the electrical length of the rod, and provides phase modulation of the X-band carrier. Three balanced mixers and three preamplifiers are included, one for each of the three channels (reference, shaft error, and trunnion errors).

3.2 ELECTRONIC ASSEMBLY

The Electronic Assembly includes the following functions.

3.2.1 Receiver

The receiver is a highly stable three channel, triple conversion superhetrodyne. It has intermediate frequencies of 40.8 mc, 6.8 mc, and 1.7 mc. The bandwidth of the first IF amplifier is 10 mc and the second IF amplifier is 2.7 mc and the bandwidth of the third IF is approximately 1 kc. Two channels are provided for amplifying the shaft axis and trunnion axis error signals and one channel is provided to amplify the reference or sum channel.

The receiver also includes phase sensitive detectors for generating angle error signals, an AGC circuit for controlling the Gain of the three receiver channels, an IF distribution amplifier unit for supplying reference channel signal to the range and frequency trackers, and a gated local oscillator signal. The second local oscillator frequency is obtained by beating the frequency tracker VCO output with a reference frequency exactly 6.8 mc lower than the incoming 40.8 doppler shifted frequency. After the second mixer, the doppler frequency shift is removed and all subsequent signal processing is accomplished at fixed carrier frequencies.

3.2.2 Frequency Synthesizer

The Frequency Synthesizer generates all of the fixed frequencies required for coherent signal transmission and reception. A single 1.7 mc oscillator and a system of multiplication, division, and mixing are used to produce the required frequencies. The synthesizer also generates the receiver local oscillator frequency, and various clock and reference frequencies used by the receiver, signal data converter, and trackers.

3.2.3 Frequency Tracker

In the cooperative mode the Frequency Tracker tracks the coherent narrow-line spectra received from the Transponder. The Frequency Tracker is switched in order to phase-lock the VCO with the incoming narrow-line spectrum. The phase detector for the phase-locked loop uses a 6.8 signal, from the frequency synthesizer, as a reference. In the non-cooperative mode a discriminator is used to derive the error signal. The error signal

drives the VCO to a frequency that when it is used as a local oscillator signal for the second IF mixer after being mixed with a 27.2 mc synthesizer signal, it removes the doppler frequency shift from all signals in succeeding IF stages, and assures passage of the signal through the 1.7 mc filters. These filters have a bandwidth of 1 kc. The tracker utilizes a frequency sweep circuit to sweep the VCO frequency across the doppler frequency range (±100 kc in cooperative mode and 0 to +10 kc in non-cooperative mode) while searching for the received signal. A threshold circuit senses the presence of carrier signal within locking range, stops the sweep, and permits the VCO to phase lock.

3.2.4 Transponder Mode Range Tracker

The Transponder Mode Range Tracker determines the range to the Transponder by measuring the phase angle between the transmitted tones and the received tones. Operation is as follows. The signal received from the Transponder in cooperative mode is demodulated (at 6.8 mc) in a coherent product detector which uses a 6.8 mc quadrature reference or tone discrimination non-cooperative mode. The individual sinewave tones are extracted from the receiver noise by using bandpass filters at the tone frequencies. Range phase delay is measured independently on each of the three tones in a closed tracking loop. Three reference square waves are locally generated, each having variable phase with respect to the transmitted tones. This phase delay is adjusted until the phase of each reference square wave matches the respective received tone. These reference square waves are produced digitally by comparison of a running high-speed counter with a low-speed forward-backward range counter. The low-speed range counter is driven forward or backward until phase null is achieved in each of the three phase detectors. The range counter is driven by incremental range pulses from a dc to PRF Converter, which is controlled by weighted integration of the three phase detector error signals.

3.2.5 Signal Data Converter

The Signal Data Converter accepts the range and range rate data from the Range and Frequency Trackers and converts it to the 15 bit serial format required by the Guidance Computer. Data is shifted out to the computer on range and range rate lines as requested

by the computer. It also sends various discrete radar status indications to the computer, select radar mode, and processes display data for activation or the astronaut display panels.

3.2.6 Antenna Control Amplifiers

The Antenna Control Amplifier contains amplifiers, for driving the antenna shaft and trunnion axis servo motors, for driving the gyro torquer coils, and the voting logic for selecting the correct gyro pair. The servo control amplifier, in connection with the antenna components and radar receiver, form an inner and outer closed loop for each axis. The inner or stabilization loop establishes the antenna boresight axis to a fixed point in inertial space even in the presence of body motions. The outer or tracking loop maintains the antenna boresight on the target based upon tracking error signals from the monopulse receiver. In the designate or search mode this loop is open and accepts the computer designate data. In the automatic mode, the Guidance Computer will designate the antenna boresight to the target supplying an automatic track enable signal for the RR when within 1 degree of the computed target LOS. This together with frequency lock-on causes the tracking loop to close. The antenna will then continuously track the target by maintaining the monopulse receiver angle error signals at null. The antenna may be manually slewed at fixed inertial rates. The "enable" signal necessary to close the auto track loop is supplied by a manual switch in manual mode.

The antenna shaft and trunnion motors are 32 pole, brushless, permanent-magnet rotor types driven by pulse-width modulated drive signals applied to sine and cosine windings of each motor. Reversal of the direction of rotation is accomplished by reversing the motor windings across the pulse width modulated drive voltage obtained by ON/OFF switching of the 25 volt ac power at a 1.8 kc rate. The voting logic, consisting of performance comparison and logical switching circuit, is used to automatically detect and remove a malfunctioning gyro. Of the four gyros, two are used to stabilize the antenna. Each pair can perform a comparison or a control function. The voting logic determines whether the active pair contains a failed gyro by comparing the output of each gyro of the active pair and one gyro of the redundant pair. If a failure or degradation occurs the other pair is switched in to stablize the antenna.

3.2.7 Self Test

Radar self test circuit permits testing of the radar without the presence of a cooperating Transponder. The self test checks transmitter power, phase lock in minimum signal level, angle error detection, AGC action, and range and range rate measurement. Insertion of single values of range and range rate permit quantitative checking via the displays. The self test circuit is disabled when the radar is in the operate modes.

3.2.8 Power Supply

The RR power supply is basically, a highly efficient dc-dc converter which provides six regulated dc output voltages. The circuit utilizes the method of switched-tap modulation for input regulation. After chopping, rectification and filtering, series regulators are used at each output. A chopping frequency of 20 kc is used to minimize the weight of transformer and ripple filter component. Short circuit protection circuits sense overload current conditions on any of the output lines and de-activate the 20 kc chopping oscillator for a preset peiod of time. If the overload has been removed after this time, nominal operation is resumed, if not, the de-activation cycle will continue until the overload is removed.

3.3 TRANSMITTER ASSEMBLY

The cooperative mode transmitter consists of a X96 multiplier chain, located on the antenna assembly, driven by a coherent 102.425 MHz crystal oscillator located in the frequency synthesizer. The resultant 9832.8 MHz signal at a level of 240 mw, is phase modulated by the ranging lines and then radiated by the antenna.

The non-cooperative transmitter is located off the antenna assembly. It contains a second X96 multiplier driven by a 102 MHz signal. The resultant 9792 MHz signal is mixed with ±50 MHz or ±100 MHz in the single side band generator (SSBG) to generate the transmitter signal which is gated at the PRF frequency and phase modulated by the ranging tones. It is then routed to a gated travelling wave tube amplifier where it is amplified to a nominal 30 watts peak power. The signal is then routed to the antenna via two rotary joints.

4.0 SYSTEM PERFORMANCE DEMONSTRATION

The performance of the modified radar was demonstrated to NASA JSC from 26 March 1974 to 28 March 1974 and from 19 November 1974 to 22 November 1974. The former tests were conducted prior to the inclusion of frequency diversity and verified the performance for the frequency track and range track loops. The second series was a test of the frequency diversity modification.

4.1 DESCRIPTION OF TESTS

The test procedures for the two series of tests were essentially identical. The major difference was that the latter tests were performed with and without frequency diversity and the former performed without frequency diversity.

Three basic tests were conducted to exercise and evaluate the modified rendezvous radar in its non-cooperative mode. The testing consulted of:

(a) Clutter Free Tests. When the radar is allowed to radiate into free space, clutter, returns from the area mask the simulated target return. Since ground clutter will not be a problem during the actual mission, the effect of ground clutter returns on radar performance must be properly separated from the basic radar operation. The radar hat coupler permits this type of testing. The transmit energy is routed by the hat coupler to the test equipment where it is absorbed. In addition, a simulated radar return signal is coupled into the radar. The servo performance can not be evaluated in this configuration. Servo performance is verified in other tests. During this tests, the return signal was processed to accurately simulate targets at 7 nautical miles, 3.5 nmi and 100 ft.

(b) Radar Search and Acquisition Tests. The ability of the radar to search the volume of uncertainty and to acquire and track the target is verified during these tests. During these tests, the transmitter is deactivated and the simulated target, representing a target at 7 nmi, is radiated across the test range from a moving

target horn. The radar searches the area of uncertainty, acquires the moving target and tracks it in angle, range and doppler.

(c) Radiation Tests. During these tests, the radar's ability to track the transmitter signal was verified. The following tests were performed.

(1) The transmit signal was routed to the target horn and radiated back to the radar. This verified short range performance against a known non-sintillating target. Range and range rate biases were also checked.

(2) The transmit signal illuminated an aluminum coated balloon and the radar tracked the reflected signal.

(3) The radar tracked the clutter returns.

Appendix 1 gives the detailed step by step operation involved in accomplishing the testing.

4.2 RESULTS OF DEMONSTRATION TESTS

4.2.1 Performance Demonstration of Interim Configuration

The performance of the radar in the non-cooperative mode was demonstrated to NASA JSC on 26 March 1974 to 28 March 1974. The demonstration procedure is shown in Appendix I.

When the transmitter was allowed to radiate into space, reflected signals from buildings in the vicinity completely masked the simulated target. For this reason, the RF silencer was attached to the horn feed for the first series of tests. The hat coupler reduces the radiated signal significantly, allowing the insertion of a full range of simulated signals. The RF silencer absorbs the energy from three of the four horns and loosely couples a signal from the fourth horn. A test signal may also be inserted into the horn. An attenuation of 30 dB is exhibited in the RF silencer. The first series of test were performed with the RF silencer. Several acquisitions were made at each of three simulated ranges, 7 nmi, 3.5 nmi and 319 ft. The results of these acquisitions are shown in the data sheets attached.

Table A (page 33) gives the data analysis for the test at 7 nmi setting. The test equipment range setting is tabulated in the first two columns. The conversion from WORD to FEET involves a multiplication by the bit size (4.69 ft/bit) and subtraction of 150 feet due to calibration of the range simulation setup, used in all tests. The third and fourth columns give the radar output data, where the conversion from WORD to FEET uses the bit size of 9.38 ft/bit. The difference in feet is listed in the fifth column. Corresponding columns of Tables B and C (pages 34 and 35) cover tests at about 3.5 nmi and at 319 ft.

Columns 6 to 10 summarize the range rate data. The test equipment available from LM program was designed to test range rate in the cooperative mode using a transponder, but did provide a method of checking system operation without a transponder. This latter test function is used in the tests reported here, but since the test equipment in this mode does not have a locked-in r-f source, there is a variable offset in the doppler data due to oscillator frequency variations.

The test equipment displays half the doppler frequency ($f_d/2$ in column 6) and the range rate in feet per second to which this corresponds (column 7) is given by the following relation, including the offset mentioned above.

$$\text{Simulated Range Rate} = \frac{1}{10}\,(f_d/2 + \text{OFFSET})$$

The following relation shows the conversion from the range rate word generated by the radar (column 8) and the measured range rate in feet per second (column 9).

$$\text{Measured Range Rate} = \frac{1}{2}\,(\text{RANGE RATE WORD} - 21250)$$

The difference between simulated and measured values is tabulated in column 10. The value for OFFSET was assumed to be constant for each set of five tests, and was set so the difference (in column 10) is zero for the first test. The variation in the following four tests therefore includes the changes in radar error and the test equipment instability.

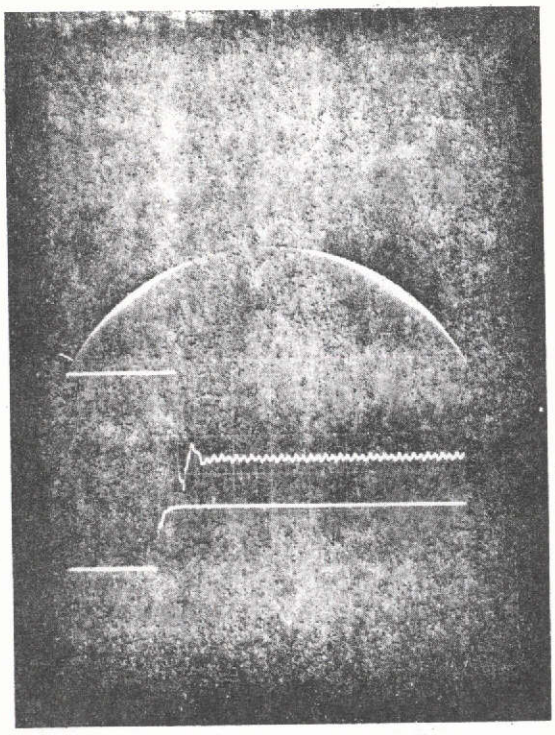
Column 11 gives the AGC and column 12 the time to achieve acquisition and a data good indication for each test.

During these tests selected points were monitored and photographed. Photographs 1 and 2 show the relationship between the receiver and transmitter on times. The upper trace, in both cases, is the LO gate drive signal and the lower trace is the detected transmitter output. In both cases, a low level represents an ON condition and a high level represents an OFF condition. Photographs 3 shows the 6.8 MHz wideband signal to the signal processor for a 7 nmi simulated signal. The return signal is not readily visible due to the low signal to noise ratio. Photographs 5 and 6 show the high and mid tone respectively under this low signal to noise ratio. Photographs 4 and 7 show the high frequency and low frequency signal for a 40 dB increase in signal to noise 4000 feet simulated range.

Photographs 8, 9 and 10 are spectral photographs of the mid, low and high frequency tones respectively. These spectrums were measured at the output of the signal processor. Photograph 11 shows the signal processor input with strong signal and maximum eclipsing. The signal can easily be observed at the instant the receiver is turned on.

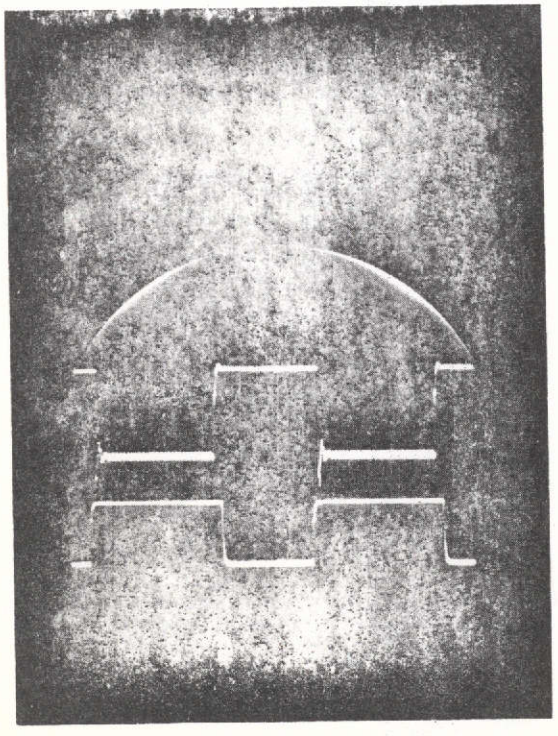
Following these tests, the RF silencer was removed. Reflected energy from various fixed targets in the area were observed and tracked, including buildings, towers, and an aluminum coated block.

The transmitter was then de-activated and the radar ability to acquire and track a moving target from a scan pattern was demonstrated using simulated signal.



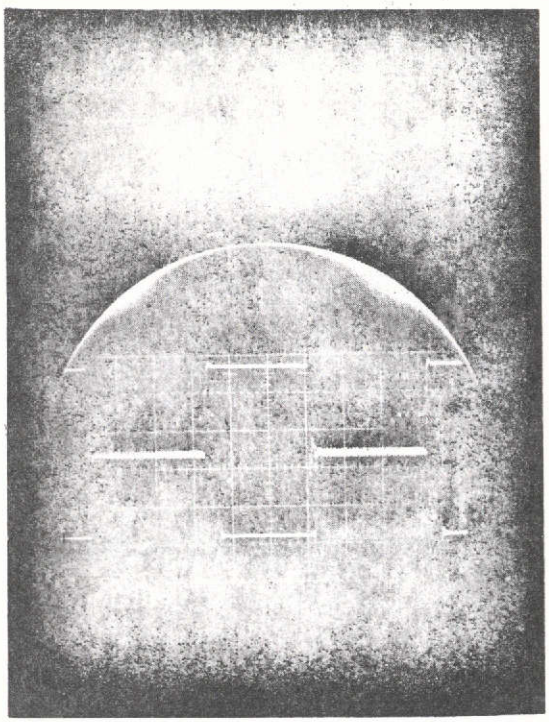
Photograph No. 1

Receiver Gating (0.5 μSec/Div)
Upper Trace - Receiver Gate
(Low = Receiver On)
Lower Trace - Transmit Pulse
(Low = Transmitter On)



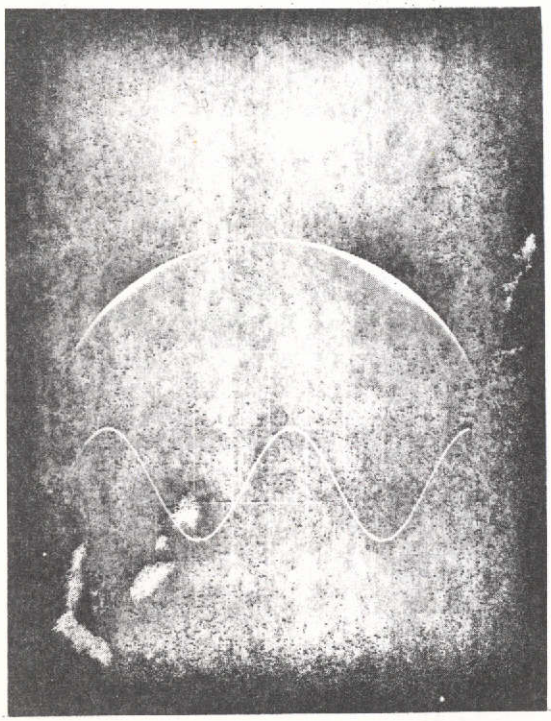
Photograph No. 2

Receiver Gating (2 μSec/Div)



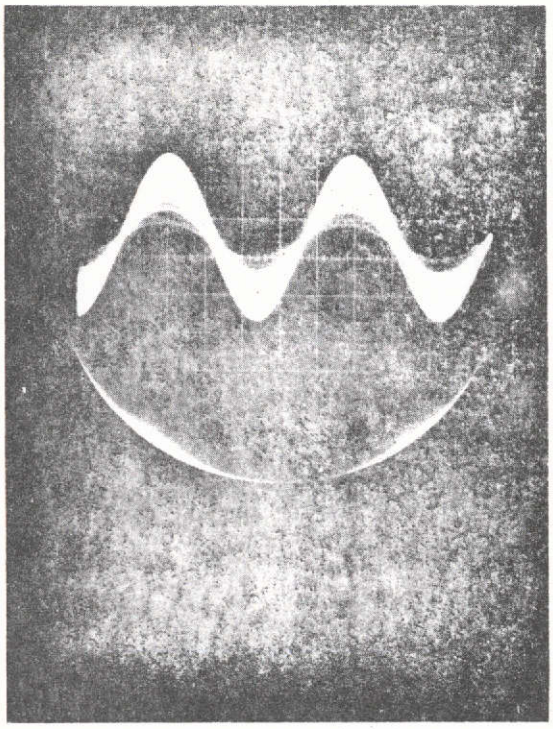
Photograph No. 3

Received Signal - Maximum Range
(2.0 μSec/Div)
Upper Trace - Receiver Gate
(Low = Receiver On)
Lower Trace - 6.8 MHz Wideband
(1V/Div)



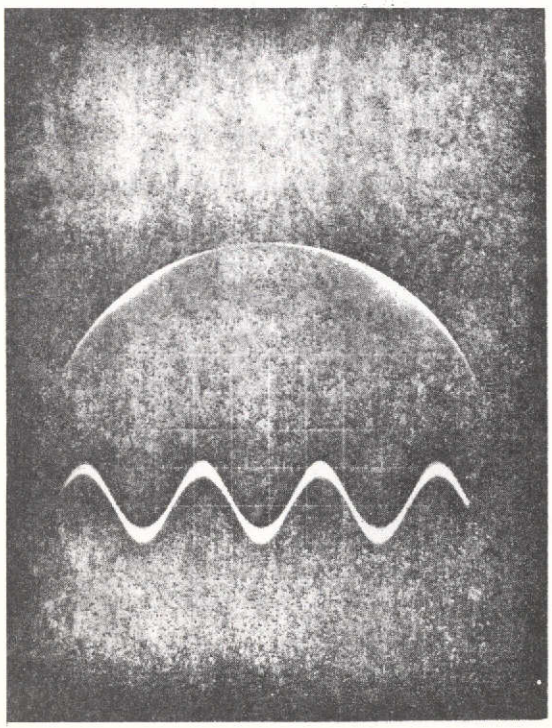
Photograph No. 4

HF Receive Tone - Strong Signal
(Time Base = 1 μSec/Div)
(Sensitivity = 2 Volts/Div)



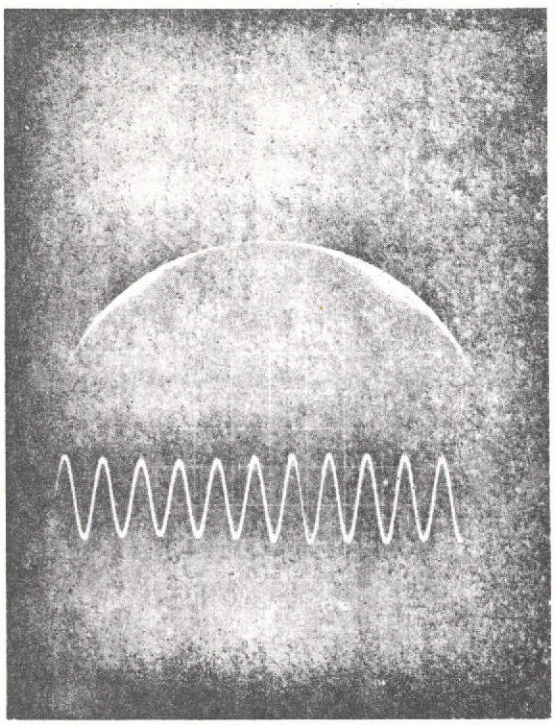
Photograph No. 5

HF Receive Tone - Weak Signal



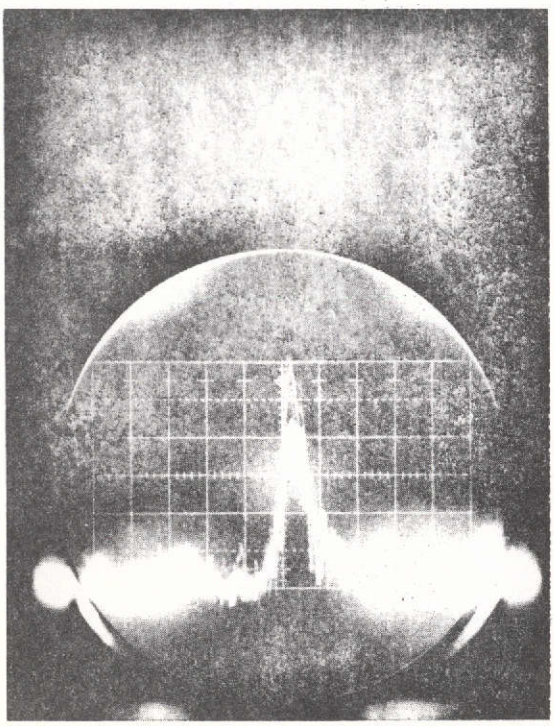
Photograph No. 6

MF Receive Tone - Weak Signal
(Time Base = 50 μSec/Div)
(Sensitivity = 5V/Div)



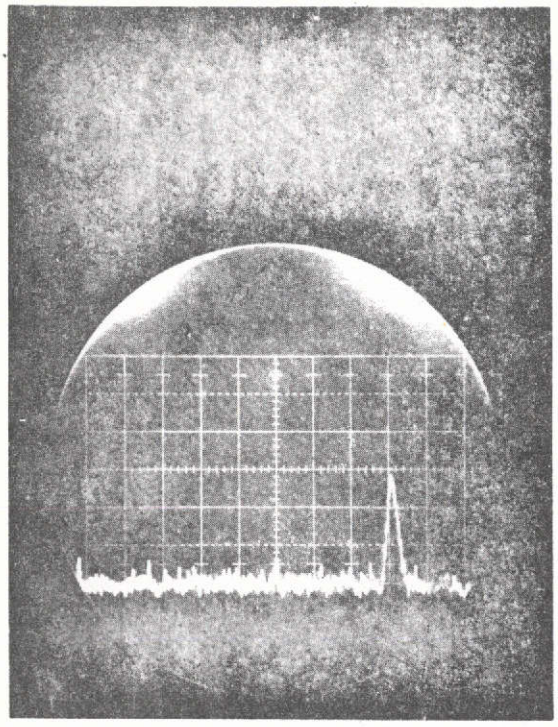
Photograph No. 7

LF Receive Tone - Strong Signal
(Time Base = 5 msec/Div)
(Sensitivity = 5V/Div)



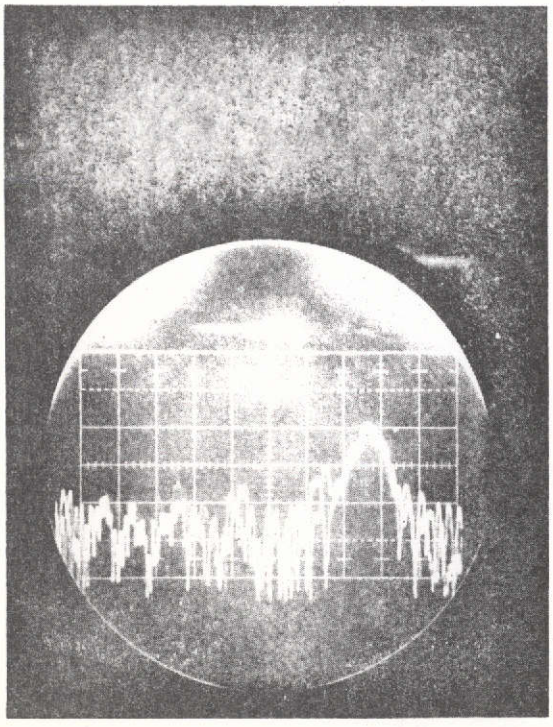
Photograph No. 8

Spectrum - MF Receive Tone
Dispersion - 1 kHz/Div
Bandwidth - 1 kHz



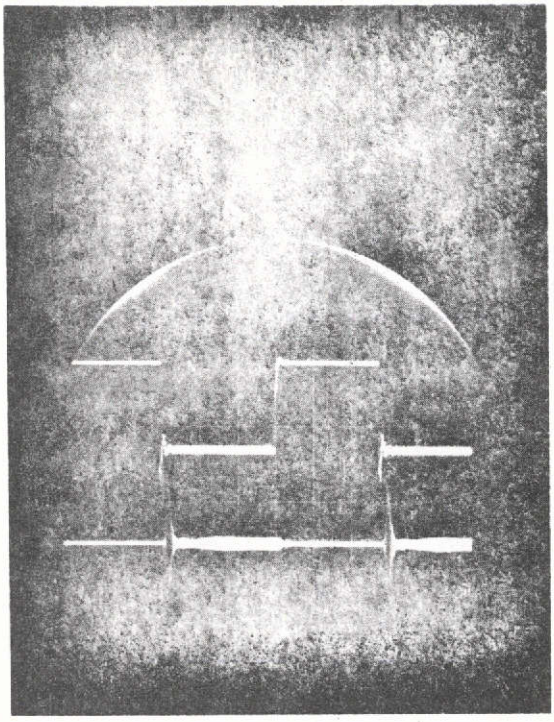
Photograph No. 9

Spectrum - LF Receive Tone
Dispersion - 20 Hz/Div
Bandwidth - 20 Hz



Photograph No. 10

Spectrum - HF Receive Tone
Dispersion - 1 kHz/Div
Bandwidth - 1 kHz



Photograph No. 11

Receive Signal - Minimum Range
(2 μSec/Div)
Upper Trace - Receiver Gate
(Low = Receiver On)
Lower Trace - 6.8 MHz Wide Band
(1V/Div)

Table A. Tracking Technique Radar Test Data
Interim Configuration

RREA 42 AA-17 W/HAT COUPLER

Digital Delay Unit Setting: 7 nmi

T-RR Path Attenuation Setting: 64 dB

Column Number	1	2	3	4	5	6	7	8	9	10	11	12
	Range					Range Rate					AGC VDC	ACQ Time Sec
	T/E Input Word	T/E Input Ft	Radar Output Word	Radar Output Ft	Delta Ft	T/E Input $f_d/2$	T/E Input Ft/Sec (1)	Radar Output Word	Radar Output Ft/Sec	Delta Ft/Sec		
1	9074	42407	4520	42397	-10	-1001 Hz	501.5	22253	501.5	0	+0.8	9.1
2	9074	42407	4520	42397	-10	-1001 Hz	501.5	22253	501.5	0	+0.8	8.3
3	9074	42407	4520	42397	-10	-1001 Hz	501.5	22253	501.5	0	+0.78	10.3
4	9074	42407	4520	42397	-10	-1001 Hz	501.5	22252	501	-0.5	+0.8	9.4
5	9074	42407	4520	42397	-10	-1001 Hz	501.5	22253	501.5	+0.5	+0.8	9.5
						(2) ⟶						
6	9074	42407	4520	42397	-10	-3003 Hz	296.5	21843	296.5	0	+0.78	9.3
7	9074	42407	4520	42397	-10	-3003 Hz	296.5	21843	296.5	0	+0.8	10.7
8	9074	42407	4520	42397	-10	-3004 Hz	296.5	21821	285.5	-11	+0.8	0.2
9	9074	42407	4520	42397	-10	-3005 Hz	296.5	21820	285	-11.5	+0.8	9.5
10	9074	42407	4520	42397	-10	-3005 Hz	296.5	21820	285	-11.5	+0.8	9.4

(1) Corrected for T/E Bias
(2) Changed Doppler Selector Ft/Sec Setting

Table B. Tracking Technique Radar Test Data
Interim Configuration

RREA 42 AA-17 W/HAT COUPLER

Digital Delay Unit Setting: 3.5 nmi

T-RR Path Attenuation Setting: 52 dB

Column Number	1	2	3	4	5	6	7	8	9	10	11	12
	Range					Range Rate					AGC VDC	ACQ Time Sec
	T/E Input		Radar Output		Delta	T/E Input		Radar Output		Delta		
	Word	Ft	Word	Ft	Ft	$f_d/2$	Ft/Sec[1]	Word	Ft/Sec	Ft/Sec		
1	4540	21143	2253	21133	-10	-3004 Hz	239.5	21729	239.5	0	+0.92	9.7
2	4540	21143	2254	21142	-1	-3004 Hz	239.5	21729	239.5	0	+1.23	8.9
3	4540	21143	2254	21142	-1	-3004 Hz	239.5	21733	241.5	+2	+1.29	10.7
4	4540	21143	2255	21152	+9	-3004 Hz	239.5	21728	239	-0.5	+1.23	9.0
5	4540	21143	2255	21152	+9	-3002 Hz	239.5	21733	241.5	+2	+1.23	8.9
						(2) ⟶						
6	4540	21143	2255	21152	+9	-1001 Hz	443.5	22137	443.5	0	+1.34	8.9
7	4540	21143	2255	21152	+9	-1001 Hz	443.5	22140	445	+1.5	+1.33	9.0
8	4540	21143	2255	21152	+9	-1001 Hz	443.5	22143	446.5	+3	+1.23	8.9
9	4540	21143	2255	21152	+9	-1001 Hz	443.5	22144	447	+3.5	+1.34	9.3
10	4540	21143	2255	21152	+9	-1001 Hz	443.5	22145	447.5	+3.5	+1.29	8.3

(1) Corrected for T/E Bias

(2) Changed Doppler Selector Ft/Sec Setting

Table C. Tracking Technique Radar Test Data
Interim Configuration

RREA 42 AA-17 W/HAT COUPLER

Digital Delay Unit Setting: 94 Ft.

T-RR Path Attenuation: 7 dB

Column Number	1	2	3	4	5	6	7	8	9	10	11	12
	Range					Range Rate					AGC VDC	ACQ Time Sec
	T/E Input		Radar Output		Delta	T/E Input		Radar Output		Delta		
	Word	Ft	Word	Ft	Ft	$f_d/2$	Ft/Sec[1]	Word	Ft/Sec	Ft/Sec		
1	100	319	34-35	319-328	0-9	-1701	347.5	21945	347.5	0	+2.44	8.7
2	100	319	34-35	319-328	0-9	-1701	347.5	21945	347.5	+0.5	+2.43	8.9
3	100	319	34-35	319-328	0-9	-1701	347.5	21946	348	+0.5	+2.43	9.7
4	100	319	34-35	319-328	0-9	-1701	347.5	21946	348	+0.5	+2.44	8.9
5	100	319	34-35	319-328	0-9	-1702	347.5	21949	348.5	+1	+2.44	8.7
						(2) ———						
6	100	319	34-35	319-328	0-9	-3004	221	21692	221	0	+2.43	9.3
7	100	319	34-35	319-328	0-9	-3004	221	21692	221	0	+2.43	8.8
8	100	319	34-35	319-328	0-9	-3004	221	21692	221	0	+2.44	8.8
9	100	319	34-35	319-328	0-9	-3004	221	21694	222	+1	+2.44	9.3
10	100	319	34-35	319-328	0-9	-3004	221	21694	222	+1	+2.43	8.7

(1) Corrected for T/E Bias
(2) Changed Doppler Selector Ft/Sec Setting

4.2.2 Performance Demonstration of Final Equipment Configuration

The performance of the radar in the final equipment configuration was demonstrated to NASA-JSC on 19 November 1974 to 22 November 1974. The procedure was essentially identical to the interim test procedure shown in Appendix I. The main difference was that the tests were performed with and without frequency diversity.

Tables D, E, F, and G give data analysis for the tests without frequency diversity at simulated ranges of 7 nmi, 3.5 nmi, 1.75 nmi and 469 feet respectively. The format is the same as before. Correspondingly, Tables H, I, J, and K give the data analysis for the frequency diversity tests at 7 nmi, 1.75 nmi, 3.5 nmi and 469 feet respectively.

As was noted in the discussion of the interim configuration tests, the r-f source in the test equipment is not locked to the radar r-f source. Therefore any frequency difference between these separate sources shows up as an apparent doppler shift, and therefore causes an apparent error in target velocity.

In correcting for this test equipment error, the value of ft/sec for the test equipment input (column 7) was offset by an amount to make the DELTA Ft/Sec value zero for the first of each set of five points, as was done in the interim configuration tests. In addition, in the final configuration tests, the frequency of the 102 MHz oscillator in the test equipment was measured, and then if the measurement changed within a set of five points, this change was used to correct the following four points. Perfect correction was not expected, since the resolution of the frequency measurement was not as good as desired (5 ft/sec) and changes in the 102 MHz oscillator in the radar were not measured. The apparent changes of target velocity measurement observed are consistent with the errors inherent in this process.

The ability of the radar to acquire a moving target from the scan pattern and to track the target once acquisition was achieved was demonstrated. The data measured is shown in Table L. This data indicates acquisition with and without frequency diversity and at angular rates of 3 mr/sec and 14 mr/sec. It should be noted that the simulated range was increased by 150 feet to account for the longer range to the target horn relative to the hat coupler.

Table D. Tracking Technique Radar Test Data
Final Configuration

RREA 42 AA-17 W/HAT COUPLER

Digital Delay Unit Setting: 7 nmi

T-RR Path Attenuation: 64 dB

Fixed Frequency

Column Number	1	2	3	4	5	6	7	8	9	10	11	12
	Range					Range Rate					AGC Volts	ACQ Time Sec
	T/E Input		Radar Output		Delta	T/E Input		Radar Output		Delta		
	Word	Ft	Word	Ft	Ft	$f_d/2$	Ft/Sec(1)	Word	Ft/Sec	Ft/Sec		
1	9074	42557	4535	42538	-19	- 800 Hz	221	21692	221.0	0.0	0.82	10.4
2	9074	42557	4535	42538	-19	- 800 Hz	221	21689	219.5	-1.5	0.82	9.8
3	9074	42557	4535	42538	-19	- 800 Hz	221	21688	219.0	-2.0	0.82	10.7
4	9074	42557	4535	42538	-19	- 800 Hz	221	21683	216.5	-4.5	0.82	10.7
5	9074	42557	4535	42538	-19	- 800 Hz	221	21683	216.5	-4.5	0.82	9.8
						(2) ⟶						
6	9074	42557	4535	42538	-19	-1700 Hz	125	21500	125.0	0.0	0.82	11.8
7	9074	42557	4535	42538	-19	-1700 Hz	125	21499	124.5	-0.5	0.82	9.7
8	9074	42557	4535	42538	-19	-1700 Hz	125	21499	124.5	-0.5	0.82	10.0
9	9074	42557	4535	42538	-19	-1700 Hz	125	21498	124.0	-1.0	0.82	10.3
10	9074	42557	4535	42538	-19	-1700 Hz	125	21500	125.0	0.0	0.82	10.1

(1) Corrected for T/E Bias
(2) Changed Doppler Selector Ft/Sec Setting

Table E. Tracking Technique Radar Test Data
Final Configuration

RREA 42 AA-17 W/HAT COUPLER

Digital Delay Unit Setting: 3.5 nmi

T-RR Path Attenuation: 52 dB

Fixed Frequency

Column Number	1	2	3	4	5	6	7	8	9	10	11	12
	Range					Range Rate					AGC Volts	ACQ Time Sec
	T/E Input		Radar Output		Delta	T/E Input		Radar Output		Delta		
	Word	Ft	Word	Ft	Ft	$f_d/2$	Ft/Sec(1)	Word	Ft/Sec	Ft/Sec		
1	4540	21293	2267	21264	-29	- 800 Hz	242.5	21735	242.5	0.0	1.41	9.1
2	4540	21293	2267	21264	-29	- 800 Hz	242.5	21730	240.0	-2.5	1.42	9.1
3	4540	21293	2267	21264	-29	- 800 Hz	237.5	21725	237.5	0.0	1.36	9.1
4	4540	21293	2267	21264	-29	- 800 Hz	237.5	21722	236.0	-1.5	1.38	9.0
5	4540	21293	2267	21264	-29	- 800 Hz	237.5	21718	234.0	-3.5	1.41	9.1
						(2) ⟶						
6	4540	21293	2267	21264	-29	-1700 Hz	257.5	21565	257.5	0.0	1.39	10.0
7	4540	21293	2267	21264	-29	-1700 Hz	257.5	21570	260.0	+2.5	1.42	9.1
8	4540	21293	2267	21264	-29	-1700 Hz	257.5	21570	260.0	+2.5	1.36	9.1
9	4540	21293	2267	21264	-29	-1700 Hz	252.5	21568	259.0	+7.5	1.38	10.0
10	4540	21293	2267	21264	-29	-1700 Hz	272.5	21586	268.0	-4.5	1.42	9.2

(1) Corrected for T/E Bias

(2) Changed Doppler Selector Ft/Sec Setting

Table F. Tracking Technique Radar Test Data
Final Configuration

RREA 42 AA-17 W/HAT COUPLER

Digital Delay Unit Setting: 1.75 nmi

T-RR Path Attenuation: 40 dB

Fixed Frequency

Column Number	1	2	3	4	5	6	7	8	9	10	11	12
	Range					Range Rate					AGC Volts	ACQ Time Sec
	T/E Input Word	T/E Input Ft	Radar Output Word	Radar Output Ft	Delta Ft	T/E Input $f_d/2$	T/E Input Ft/Sec(1)	Radar Output Word	Radar Output Ft/Sec	Delta Ft/Sec		
1	2270	10646	1134	10637	-9	-1700 Hz	134.0	21518	134.0	0.0	1.73	11.8
2	2270	10646	1134	10637	-9	-1700 Hz	134.0	21516	133.0	-1.0	1.58	12.1
3	2270	10646	1134	10637	-9	-1700 Hz	134.0	21514	132.0	-2.0	1.67	14.4
4	2270	10646	1134	10637	-9	-1700 Hz	134.0	21510	130.0	-4.0	1.58	12.9
5	2270	10646	1134	10637	-9	-1700 Hz	129.0	21509	129.5	+0.5	1.58	10.7
						(2) →						
6	2270	10646	1134	10637	-9	- 800 Hz	216.5	21683	216.5	0.0	1.58	9.7
7	2270	10646	1134	10637	-9	- 800 Hz	216.5	21677	213.5	-3.0	1.67	14.0
8	2270	10646	1134	10637	-9	- 800 Hz	216.5	21676	213.0	-3.5	1.73	11.1
9	2270	10646	1134	10637	-9	- 800 Hz	216.5	21672	211.0	-5.5	1.73	11.0
10	2270	10646	1134	10637	-9	- 800 Hz	211.5	21670	210.0	-1.5	1.73	9.6

(1) Corrected for T/E Bias

(2) Changed Doppler Selector Ft/Sec Setting

Table G. Tracking Technique Radar Test Data
Final Configuration

RREA 42 AA-17 W/HAT COUPLER

Digital Delay Unit Setting: 94 ft

T-RR Path Attenuation: 0 dB

Fixed Frequency

Column Number	1	2	3	4	5	6	7	8	9	10	11	12
	Range					Range Rate					AGC Volts	ACQ Time Sec
	T/E Input		Radar Output		Delta	T/E Input		Radar Output		Delta		
	Word	Ft	Word	Ft	Ft	$f_d/2$	Ft/Sec(1)	Word	Ft/Sec	Ft/Sec		
1	100	469	51-52	478-488	+9-19	800 Hz	332.5	21915	332.5	0.0	2.45	10.2
2	100	469	51-52	478-488	+9-19	800 Hz	332.5	21909	329.5	-3.0	2.45	10.8
3	100	469	51-52	478-488	+9-19	800 Hz	332.5	21906	328.0	-4.5	2.45	9.7
4	100	469	51-52	478-488	+9-19	800 Hz	327.5	21905	327.5	-0.0	2.45	9.7
5	100	469	51-52	478-488	+9-19	800 Hz	327.5	21898	324.0	-3.5	2.45	10.0
						(2)→						
6	100	469	51-52	478-788	+9-19	1700 Hz	229.5	21709	229.5	0.0	2.45	9.4
7	100	469	51-52	478-488	+9-19	1700 Hz	229.5	21706	228.0	-1.5	2.45	9.7
8	100	469	51-52	478-488	+9-19	1700 Hz	229.5	21703	226.5	-1.5	2.45	9.7
9	100	469	51-52	478-488	+9-19	1700 Hz	224.5	21688	219.0	-5.5	2.45	9.6
10	100	469	51-52	478-488	+9-19	1700 Hz	224.5	21683	216.5	-8.0	2.45	9.8

(1) Corrected for T/E Bias
(2) Changed Doppler Selector Ft/Sec Setting

Table H. Tracking Technique Radar Test Data
Final Configuration

RREA 42 AA-17 W/HAT COUPLER

Digital Delay Unit Setting: 7 nmi

T-RR Path Attenuation: 63 dB

Frequency Diversity

Column Number	1	2	3	4	5	6	7	8	9	10	11	12
	Range					Range Rate					AGC Volts	ACQ Time Sec
	T/E Input		Radar Output		Delta	T/E Input		Radar Output		Delta		
	Word	Ft	Word	Ft	Ft	$f_d/2$	Ft/Sec(1)	Word	Ft/Sec	Ft/Sec		
1	9074	42557	4535	42538	-19	-800 Hz	342.5	21935	342.5	0.0	0.82	10.4
2	9074	42557	4535	42538	-19	-800 Hz	347.5	21948	349.0	1.5	0.82	10.1
3	9074	42557	4535	42538	-19	-800 Hz	347.5	21953	351.5	4.0	0.82	9.9
4	9074	42557	4535	42538	-19	-800 Hz	352.5	21959	354.5	2.0	0.82	10.8
5	9074	42557	4535	42538	-19	-800 Hz	352.5	21965	357.5	5.0	0.82	10.4
						(2) →						
6	9074	42557	4535	42538	-19	-1700 Hz	129.0	21508	129.0	0.0	0.82	13.6
7	9074	42557	4535	42538	-19	-1700 Hz	129.0	21510	130.0	1.0	0.82	12.3
8	9074	42557	4535	42538	-19	-1700 Hz	129.0	21512	131.0	2.0	0.82	13.4
9	9074	42557	4535	42538	-19	-1700 Hz	129.0	21515	132.5	3.5	0.82	16.8
10	9074	42557	4535	42538	-19	-1700 Hz	134.0	21520	135.0	1.0	0.82	12.8

(1) Corrected for T/E Bias
(2) Changed Doppler Selector Ft/Sec Setting

Table I. Tracking Technique Radar Test Data
Final Configuration

RREA 42 AA-17 W/HAT COUPLER

Digital Delay Unit Setting: 3.5 nmi

T-RR Path Attenuation: 52 dB

Frequency Diversity

Column Number	1	2	3	4	5	6	7	8	9	10	11	12
	Range					Range Rate					AGC Volts	ACQ Time Sec
	T/E Input		Radar Output		Delta	T/E Input		Radar Output		Delta		
	Word	Ft	Word	Ft	Ft	$f_d/2$	Ft/Sec(1)	Word	Ft/Sec	Ft/Sec		
1	4540	21293	2267	21264	-29	-1700 Hz	175.5	21601	175.5	0.0	1.41	8.9
2	4540	21293	2267	21264	-29	-1700 Hz	175.5	21599	174.5	-1.0	1.42	9.1
3	4540	21293	2267	21264	-29	-1700 Hz	170.5	21593	171.5	+1.5	1.41	9.1
4	4540	21293	2267	21264	-29	-1700 Hz	170.5	21588	169.0	-1.5	1.36	9.3
5	4540	21293	2267	21264	-29	-1700 Hz	170.5	21584	167.0	-3.5	1.41	9.0
						(2)→						
6	4540	21293	2267	21264	-29	-800 Hz	255.0	21760	255.0	0.0	1.38	9.1
7	4540	21293	2267	21264	-29	-800 Hz	255.0	21760	255.0	0.0	1.39	9.4
8	4540	21293	2267	21264	-29	-800 Hz	255.0	21757	258.5	+3.5	1.36	10.1
9	4540	21293	2267	21264	-29	-800 Hz	255.0	21757	258.5	+3.5	1.38	9.3
10	4540	21293	2267	21264	-29	-800 Hz	255.0	21755	257.5	+2.5	1.38	10.0

(1) Corrected for T/E Bias
(2) Changed Doppler Selector Ft/Sec Setting

Table J. Tracking Technique Radar Test Data
Final Configuration

RREA 42 AA-17 W/HAT COUPLER

Digital Delay Unit Setting: 1.75 nmi

T-RR Path Attenuation: 40 dB

Frequency Diversity

Column Number	1	2	3	4	5	6	7	8	9	10	11	12
	Range					Range Rate					AGC Volts	ACQ Time Sec
	T/E Input		Radar Output		Delta	T/E Input		Radar Output		Delta		
	Word	Ft	Word	Ft	Ft	fd/2	Ft/Sec(1)	Word	Ft/Sec	Ft/Sec		
1	2270	10646	1134	10637	-9	-800 Hz	244.0	21738	244.0	0.0	1.74	11.0
2	2270	10646	1134	10637	-9	-800 Hz	244.0	21736	243.0	-1.0	1.61	10.6
3	2270	10646	1134	10637	-9	-800 Hz	239.0	21732	241.0	+2.0	1.61	13.7
4	2270	10646	1134	10637	-9	-800 Hz	239.0	21727	238.5	-0.5	1.61	11.8
5	2270	10646	1134	10637	-9	-800 Hz	239.0	21725	237.5	-1.5	1.61	11.1
						(2) →						
6	2270	10646	1134	10637	-9	-1700 Hz	142.5	21535	142.5	0.0	1.74	12.8
7	2270	10646	1134	10637	-9	-1700 Hz	142.5	21534	142.0	-0.5	1.69	9.7
8	2270	10646	1134	10637	-9	-1700 Hz	142.5	21530	140.0	-2.5	1.74	10.0
9	2270	10646	1134	10637	-9	-1700 Hz	142.5	21528	139.0	-3.5	1.74	13.8
10	2270	10646	1134	10637	-9	-1700 Hz	142.5	21525	137.5	-5.0	1.61	11.1

(1) Corrected for T/E Bias
(2) Changed Doppler Selector Ft/Sec Setting

Table K. Tracking Technique Radar Test Data
Final Configuration

RREA 42 AA-17

Digital Delay Unit Setting: 0

T-RR Path Attenuation: 0 dB

Frequency Diversity

Column Number	1	2	3	4	5	6	7	8	9	10	11	12
	Range					Range Rate					AGC Volts	ACQ Time Sec
	T/E Input		Radar Output		Delta	T/E Input		Radar Output		Delta		
	Word	Ft	Word	Ft	Ft	$f_d/2$	Ft/Sec (1)	Word	Ft/Sec	Ft/Sec		
1	100	469	51-52	478-488	9-19	-800 Hz	289	21828	289.0	0.0	-2.48	9.8
2	100	469	51-52	478-488	9-19	-800 Hz	289	21822	286.0	-3.0	+2.48	9.6
3	100	469	51-52	478-488	9-19	-800 Hz	289	21820	285.0	-4.0	+2.48	9.1
4	100	469	51-52	478-488	9-19	-800 Hz	279	21810	280.0	+1.0	+2.48	9.3
5	100	469	51-52	478-488	9-19	-800 Hz	279	21810	280.0	+1.0	+2.48	10.0
						(2)→						
6	100	469	51-52	478-488	9-19	-1700 Hz	210	21670	210.0	0.0	+2.48	9.5
7	100	469	51-52	478-488	9-19	-1700 Hz	210	21670	210.0	0.0	+2.48	9.7
8	100	469	51-52	478-488	9-19	-1700 Hz	205	21662	206.0	+1.0	+2.48	9.6
9	100	469	51-52	478-488	9-19	-1700 Hz	205	21659	204.5	-0.5	+2.48	10.0
10	100	469	51-52	478-488	9-19	-1700 Hz	205	21654	202.0	-3.0	+2.48	9.9

(1) Corrected for T/E Bias

(2) Changed Doppler Selector Ft/Sec Setting

Table L. Tracking Technique Radar Test Data Final Configuration

RREA 42 AA-17 W/O HAT COUPLER

Digital Delay Unit Setting: 7 nmi

T-RR Path Attenuation: 53 dB

Column Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14
	Range					Range Rate					AGC Volts	ACQ Time Sec	Target Rate	Fixed/ Diversity
	T/E Input		Radar Output		Delta	T/E Input		Radar Output		Delta				
	Word	Ft	Word	Ft	Ft	$f_d/2$	Ft/Sec[1]	Word	Ft/Sec	Ft/Sec			Mr/Sec	
1	9076	42725	4550	42679	-46	-700 Hz	292	21834	292.0	0.0	+1.19	22.8	3	Diversity
2	9076	42725	4550	42679	-46	-700 Hz	292	21835	292.5	+0.5	+1.19	17.3	3	Diversity
3	9076	42725	4550	42679	-46	-700 Hz	292	21835	292.5	+0.5	+1.16	17.2	3	Diversity
4	9076	42725	4550	42725	-46	-700 Hz	292	21836	293.0	+1.0	+1.19	17.3	3	Fixed
5	9076	42725	4550	42679	-46	-700 Hz	303	21856	303.0	0.0	+1.28	16.9	14	Diversity
6	9076	42725	4550	42679	-46	-700 Hz	303	21854	302.0	-1.0	+1.30	18.1	14	Diversity
7	9076	42725	4550	42679	-46	-700 Hz	303	21854	302.0	-1.0	+1.32	17.7	14	Diversity
8	9076	42725	4550	42679	-46	-700 Hz	303	21851	300.5	-2.5	+1.35	31.8	14	Fixed
9	9076	42725	4540	42679	-46	-700 Hz	303	21855	302.5	-0.5	+1.28	19.5	14	Fixed
10	9076	42725	4550	42679	-46	-700 Hz	303	21854	302.0	-1.0	+1.29	34.6	14	Fixed

(1) Corrected for T/E Bias

Two additional tests were performed using the non-cooperative mode transmitter. First, the transmitter output was connected to range target horn and radiated across the test range to the radar. Second, the transmitter output, at the target tower, illuminated an aluminum coated balloon which was tracked by the radar. During both test the range rate readout indicated a stationary target, zero doppler shift, at a range of 375 feet, range word equals 40. This indicated a bias error of 125 ft due to the tone alignment of the transmitter. The transmitter will be realigned to remove this bias error.

The radar was then converted to the cooperative mode and proper operation was verified.

The radar was reconfigured to the non-cooperative mode. Data was taken indicating AGC readings at various attenuator settings at each of the 5 PRF's in the frequency diversity mode. This data is summarized in Tables M, N, and O.

Table M. AGC Versus Attenuation
2.8 nmi Delay

PRF / Attenuation	1	2	3	4	5
60	—	—	—	—	0.97V
50	—	—	1.1V	1.28V	1.32V
40	0.87V	1.3V	1.41V	1.51V	1.62V
30	1.32V	1.52V	1.77V	1.90V	1.98V
20	1.55V	1.92V	2.09V	2.19V	2.25V
10	1.94V	2.21V	2.33V	2.40V	2.42V
0	2.21V	2.41V	2.46V	2.48V	2.49V

— = Receiver not locked.

Table N. AGC Versus Attenuation
3.2 nmi Delay

PRF / Attenuation	1	2	3	4	5
60	1.38V	1.42V	1.42V	1.36V	1.27V
50	1.72V	1.73V	1.74V	1.72V	1.69V
40	1.87V	1.88V	1.89V	1.87V	1.85V
30	2.14V	2.15V	2.15V	2.12V	2.09V
20	2.35V	2.37V	2.37V	2.35V	2.32V
10	2.45V	2.45V	2.46V	2.45V	2.44V
0	2.49V	2.49V	2.49V	2.49V	2.49V

Table O. AGC Versus Attenuation
4.2 nmi Delay

PRF / Attenuation	1	2	3	4	5
60	1.27V	1.25V	1.19V	1.08V	0.88V
50	1.49V	1.48V	1.43V	1.39V	1.31V
40	1.88V	1.87V	1.81V	1.72V	1.58V
30	2.18V	2.17V	2.12V	2.06V	1.96V
20	2.38V	2.38V	2.35V	2.30V	2.23V
10	2.47V	2.48V	2.46V	2.44V	2.41V
0	2.51V	2.51V	2.51V	2.50V	2.48V

PART IV

DETAILED EQUIPMENT DESCRIPTION

1.0 DESCRIPTION OF OPERATION

The following is a detailed discussion of the operation of the functional subassembly.

1.1 ANTENNA ASSEMBLY

1.1.1 General

The Radar Antenna consists of an antenna pedestal and base mounted on the outside structural members of the LM. The antenna pedestal includes rotating assemblies which contain various radar components. The rotating assemblies are balanced about a shaft axis and a trunnion axis. The trunnion axis is perpendicular to, and intersects, the shaft axis. The antenna reflector together with the microwave and r-f components are assembled at the top of the trunnion axis. This assembly is counter-balanced by the trunnion axis rotating components such as the gyros, resolvers, and drive motors which are mounted below the shaft axis. Both groups of components, which are opposite each other, revolve about the shaft axis. This balanced arrangement requires less driving torque and reduces the overall antenna weight.

The Rendezvous Radar is an amplitude comparison monopulse (simultaneous lobing) system. The Radar Antenna uses a 24-inch diameter parabolic reflector with a Cassegrainian feed. In this system, a conventional four horn feed illuminates a hyperboloidal sub-reflector which is located to reflect the r-f energy back to the main parabola. The parabolic reflector collects this r-f energy and forms a directional beam. The radar antenna operates in the X-band region with a gain exceeding 32 dB. The output signal radiated from the antenna is circularly polarized in order to minimize signal losses due to variations in attitude between

the radar and the target. A ferrite phase modulator excited by three different sub-r-f frequencies varies the phase characteristics of the r-f energy so that accurate, nonambiguous range tracking is obtained.

The antenna assembly was modified to incorporate the non-cooperative target tracking mode and frequency diversity. The modifications are shown in Figure IV-1. The phase modulator was removed and the directional coupler output port was terminated. The TWT signal was routed via the shaft and trunnion rotary points to the antenna hybrid. A SPDT diode switch has been added at the chain output to gate the first LO and to select the proper L.O. frequency. Operation of the PIN diode is discussed in Section 1.2.1.

Each antenna axis is controlled in angle by a servo system that has a bandwidth of 1 cycle. The main radar servo tracking loops enclose secondary gyro stabilization loops. Rate integrating gyros are used in an integrating configuration so that inertial space conditions can be designated and held despite vehicle body movement. A cluster of four gyros are used for greater reliability. The outputs of the gyros are monitored by a voting amplifier

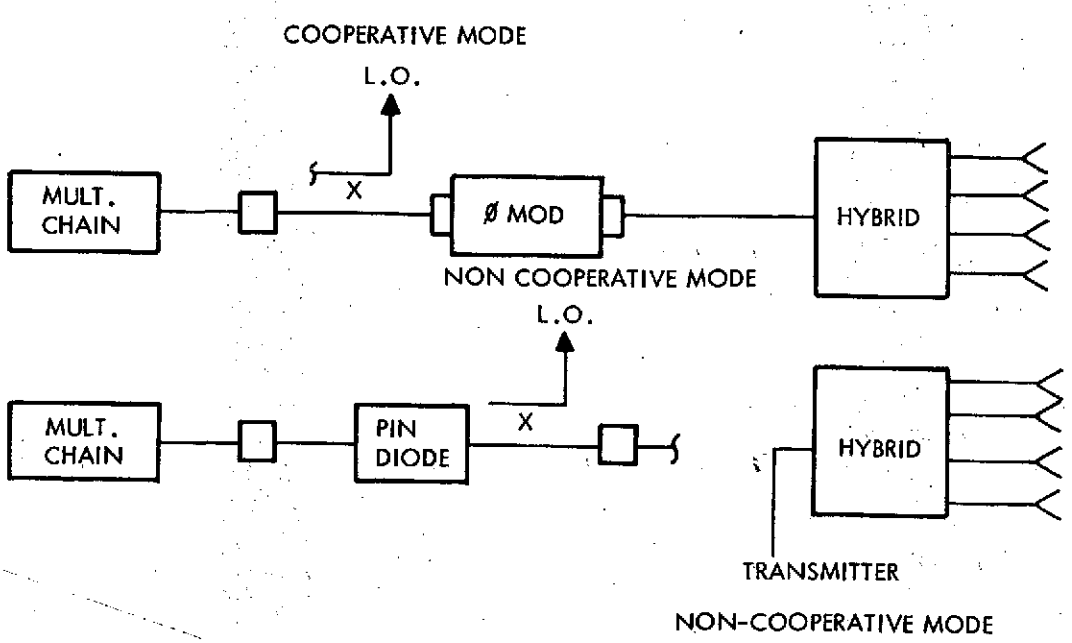


Figure IV-1. Antenna Assembly Modification

which weighs the gyro information and, if necessary, performs a switching function to provide the gyro stabilization loops with optimum control signals. In this manner, compensation is made for excessive gyro drift or complete failure of a gyro or component of an associated stabilization loop. Each servo is capable of being slewed at an inertial rate of 3 degrees per second. Direct drive brushless motors are used in each axis.

With the waveguide run required for the non-cooperative mode, coverage is provided from +25 degrees to +180 degrees from the horizontal. The antenna trunnion axis provides antenna travel of 70 degrees to either side of all shaft axis positions.

1.1.2 Microwave Subassembly

The Microwave Subassembly consists of an Antenna Subassembly Four Horn Feed, Polarizer, Dual Mode Transition, Phase Shifters, Comparator, Transmitter Distribution Network, and Local Oscillator distribution network, shown in Figure IV-2. This subassembly (1) transmits the output of the high-power multiplier chain or the noncooperative mode transmitter to the feed horn; (2) accepts the received r-f signals coming through the feed horn and directs these signals through the comparator to the mixers; and (3) distributes a portion of the r-f energy from the high power multiplier chain as a local oscillator signal to the three mixers.

The Antenna Subassembly is a Cassegrainian type and consists of a parabolic primary reflector and a hyperbolic secondary reflector. The secondary reflector is located in front of the focal point of the paraboloid. It reflects the r-f energy radiated from the feed horn back to the parabolic reflector. The energy is formed into a narrow beam by the parabolic reflector and radiated into space. The choice of focal length for a parabolic antenna reflector depends upon the radiation pattern of the feed for the antenna. A paraboloid of given diameter may use a short focal length, with the feed assembly mounted inside the mouth of the reflector, or a long focal length, with the feed assembly located far in front of the parabolic reflector. A short focal length will result in non-uniform illumination of the paraboloid due to the directivity of the feed assembly. This will reduce the useful diameter of the reflector and lower the antenna gain. A long focal length provides essentially uniform illumination of the paraboloid but allows some of the radiated r-f energy from the

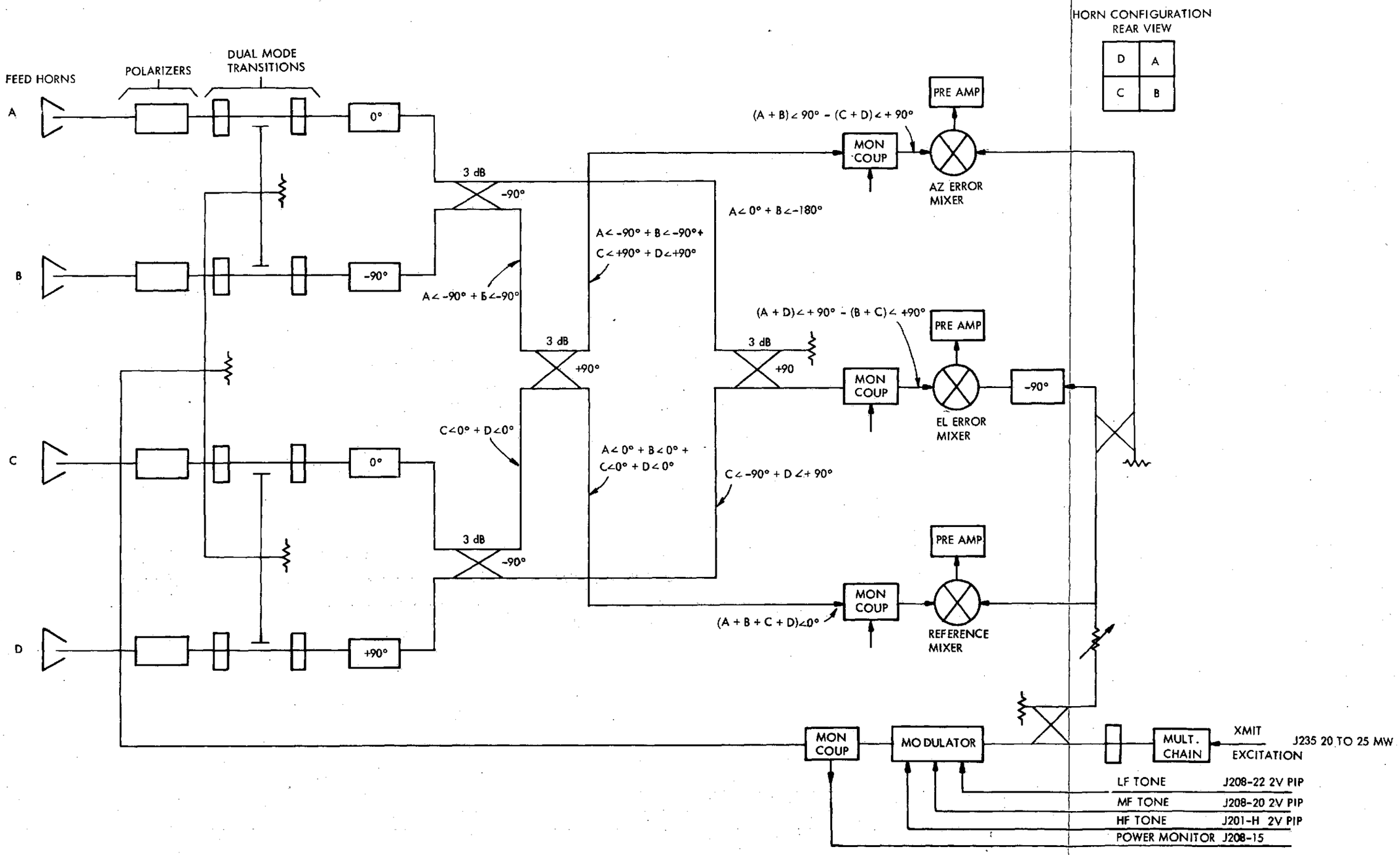
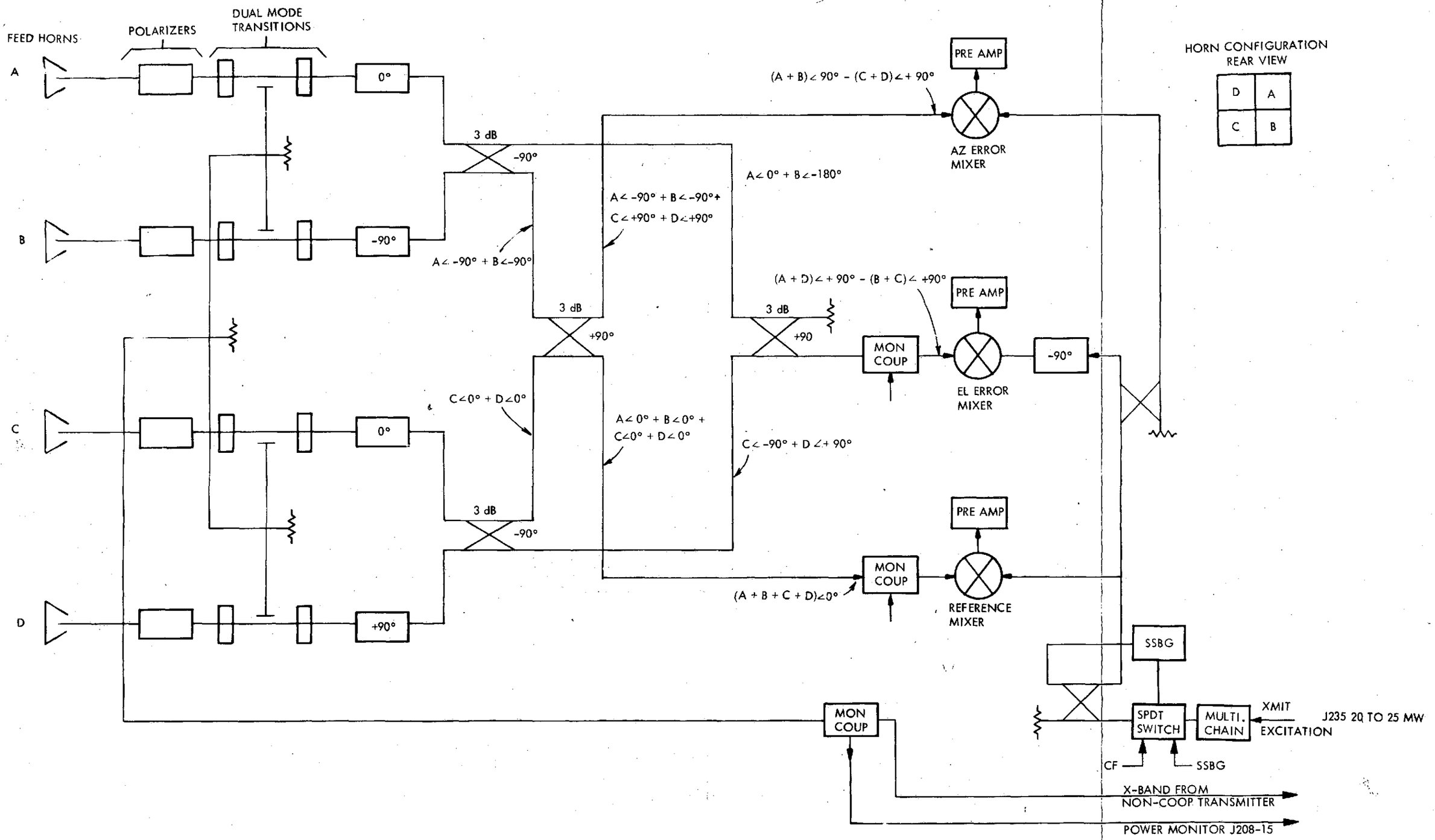


Figure IV-2. Microwave Subassembly Functional Block Diagram Cooperative Mode



FOLDOUT FRAME 1

ORIGINAL PAGE IS
OF POOR QUALITY

Figure IV-2A. Microwave Subassembly Functional Block Diagram Non-Cooperative Mode

FOLDOUT FRAME 2

feed to spill over the edge of the reflector. Also, as focal length is increased, the overall beam angle of the main lobe is narrowed, but an increase in secondary side and back lobes will lower antenna gain. A ratio of focal length to diameter of approximately 0.35 is an effective compromise between the various factors.

The Cassegrainian technique employed allows a short focal length (F/D ratio of 0.375) to minimize side lobes that would result from a spill-over of r-f energy. In addition, the main lobe beam width is narrowed to less than four degrees because the parabola receives a more uniform illumination provided by the divergent reflection characteristics of the hyperbola. Additional considerations affecting the selection of an F/D ratio for this application are strength-to-weight ratio, and overall dimensions of the Cassegrainian design that will permit the antenna assembly to perform within the allotted space. The gain of the antenna assembly is greater than 32 dB. The following is a list of antenna characteristics:

Gain	Greater than 32 dB
Polarization	Circularly Polarized
Polarization Ratio	Within 2 dB over Half Power Beamwidth
Transmission Beamwidth	4 Degrees at Half Power Points (Nominal)
Receiver Reference Pattern Beamwidth	4 Degrees at Half Power Points (Nominal)
Sidelobe Level	15 dB Minimum
Transmitter-Receiver Isolation	30 dB Minimum
Error Pattern Null Depth	30 dB Minimum
F/D	0.375
Parabolic Reflector Diameter	24 Inches
Hyperbolic Reflector Diameter	4.65 Inches
Hyperbola Position	7.58 Inches (Nominal)
Hyperbola Edge Angle	35 Degrees

The feed horn radiates and receives r-f energy and provides the proper amplitude taper (distribution) of energy across the parabola to achieve the required gain and beamwidth characteristics of the antenna. The feed consists of a cluster of four square apertures 0.75 wavelengths on each side and is located at the center of the parabolic reflector.

The Polarizer converts linearly polarized signals to circularly polarized signals. This faculty is achieved in both directions. During transmission, the polarizer converts the linearly polarized signal from the transmitter section of the radar to a circularly polarized signal suitable for radiation from the feed horn. A linearly polarized signal (beacon return) may arrive with its wave front oriented in any direction. The Polarizer converts this received signal to a circularly polarized signal. The vertical component of the circularly polarized signal is coupled to the receiver section. By converting the incoming linearly polarized signal to a circularly polarized signal, the Polarizer will assure a uniform transfer of energy between the beacon transponder and the radar receiver regardless of the orientation of the incoming linearly polarized signal.

The Dual Mode Transition acts in conjunction with the Polarizer to provide the required 30 dB of isolation between the transmit and receive channels. It is a three port device. Two ports carry linearly polarized signals and both are coupled to the third port which will support the combination or orthogonal linearly polarized signals. One of the linear ports is connected to the transmitter section, and the other linear port is connected to the receiver section. The orthogonally polarized port connects to the feed horn through the polarizer. Each linearly polarized port is orthogonally polarized with respect to the other linearly polarized port, thus providing a high degree of isolation between the two. This arrangement will decouple the receiver from the high power r-f energy during transmission.

The comparator used in the microwave Subassembly requires a plus and minus 90 degree phase shift of the signal applied to two of its four input channels in order to properly process the r-f signals. Two Phase Shifters are used for this purpose, one capacitive and the other inductive. The r-f signals received from the Dual Mode Transition are delayed 90 degrees by the capacitive type Phase Shifter and advanced 90 degrees by the inductive type Phase Shifter. These phase shifted signals, in conjunction with the two unaffected (0 phase) signals are applied to the Comparator.

The Comparator is an r-f signal processing network. Within this network the proper amplitude and phase relationships are established (in conjunction with the external phase shifters) so that addition and subtraction of various combinations of the four input signals develops the monopulse reference and error outputs required to drive the antenna positioning system. The input signals pass through a tandem pair of 3-dB topwall hybrid junctions, and then through two 3-dB sidewall hybrids which are folded back on themselves. One of the four output ports of the Comparator is terminated in a matched load. The other three comparator output ports feed the reference, azimuth error, and elevation error signals to their respective mixers.

The Transmitter Distribution Network divides the high power transmitter energy into four equal parts suitable for application to the transmitter input port of the Dual Mode Transition.

The Local Oscillator Distribution Network divides the portion of the chain energy obtained from a directional coupler or from the single sideband generator into three equal parts. This r-f energy is distributed to the three (azimuth, elevation, and reference) pre-amplifiers as the local oscillator signal. A single pole double throw pin diode switch is used to select the proper signal.

The SPDT PIN diode switch consists of a waveguide Tee with a PIN diode mounted in the two output arms. When one diode is energized, the chain output is routed to the L.O. power divider via the directional coupler. If the second diode is energized, the chain output is routed to the single sideband generator. After translation in frequency, the signal is applied to the L.O. power divider directly. The single sideband generator, shown in Figure IV-3 consists of two varactor modulators which allow generation of upper and lower sidebands about the carrier frequency. The sideband outputs from the modulators are so phased that when combined one of the sidebands is rejected and a single sideband output results. The other sideband may be selected by feeding the modulating signal into a different port of the IF quadrature hybrid.

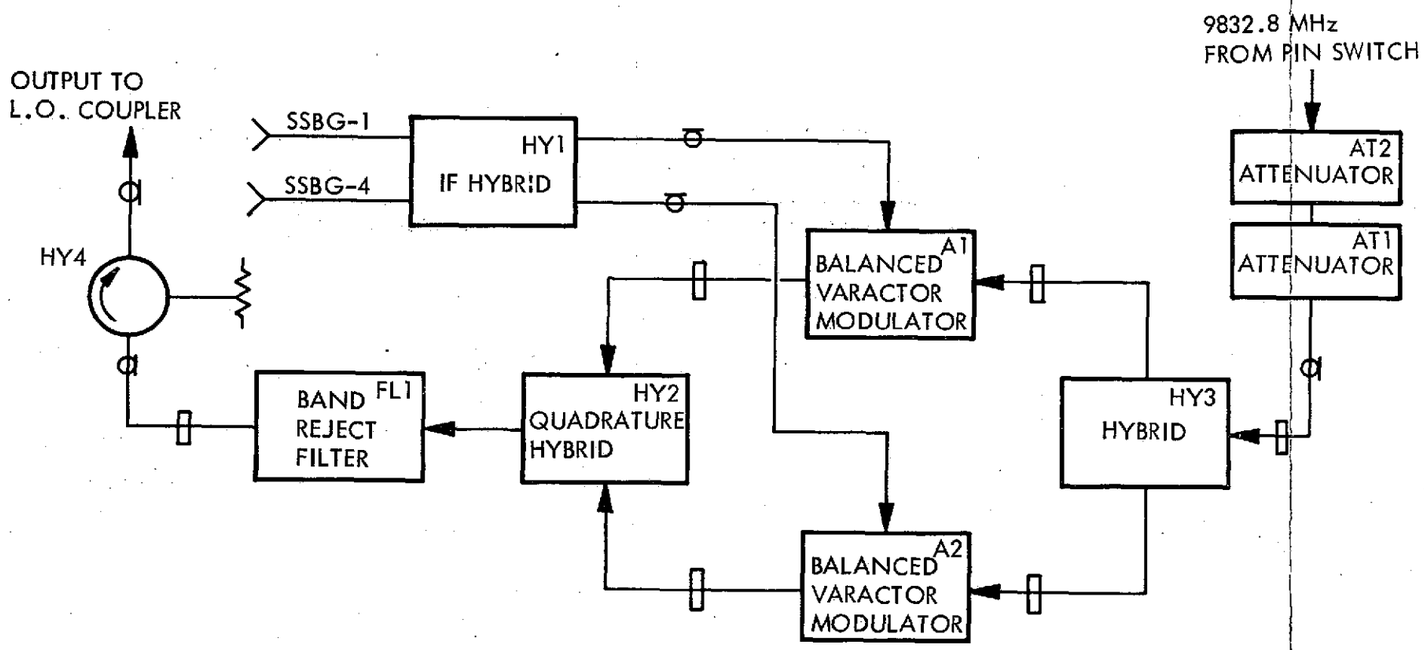


Figure IV-3. L.O. Single Sideband Generator

For the LO sideband generator the microwave input is fed to the two varactor modulators in phase by means of a waveguide hybrid. The modulating signal is fed to modulators 90° out of phase using an IF quadrature hybrid. The modulators are balanced units each using two varactors and thus providing carrier rejection of at least 20 dB. The resulting sidebands from one modulator will be 90° out of phase with respect to those from the other modulator. In addition, using the output of one modulator as reference, the two upper sidebands will have a different phasing than the lower sidebands; if one is leading by 90° the other will be lagging by 90°. These sidebands are then fed into a waveguide quadrature hybrid. Because of the phasing of the sidebands one will appear at one hybrid output while the other sideband will appear at the other output. For this particular application, one hybrid output is terminated. The other sideband is obtained by changing the phase relationship of the modulating signals to the varactor modulators. This is accomplished by feeding the modulating signal to a different port on the IF quadrature hybrid.

A band reject filter is used following the waveguide quadrature hybrid to provide additional carrier rejection. The output from the L.O. single sideband generator is sent through a coaxial circulator and a short piece of hardline into the former terminated port of the coupler in the antenna microwave assembly.

1.2 ELECTRONICS ASSEMBLY

The electronic assembly consists of the functions described below.

1.2.1 Receiver Subassembly

The Receiver shown in Figure IV-4 is an amplitude comparison type with a triple conversion 3 channel IF which provides azimuth and elevation errors. Receiver signals from the preamps on the antenna (two differences and one reference) at a frequency of 40.8 mc, are the IF inputs to the receiver. In each channel the 40.8 mc signal is amplified in the first IF and converted to 6.8 mc in the second mixer. The signal is then amplified and fed to the third IF, which converts it to a 1.7 mc signal, and then amplifies it to provide an output at this frequency.

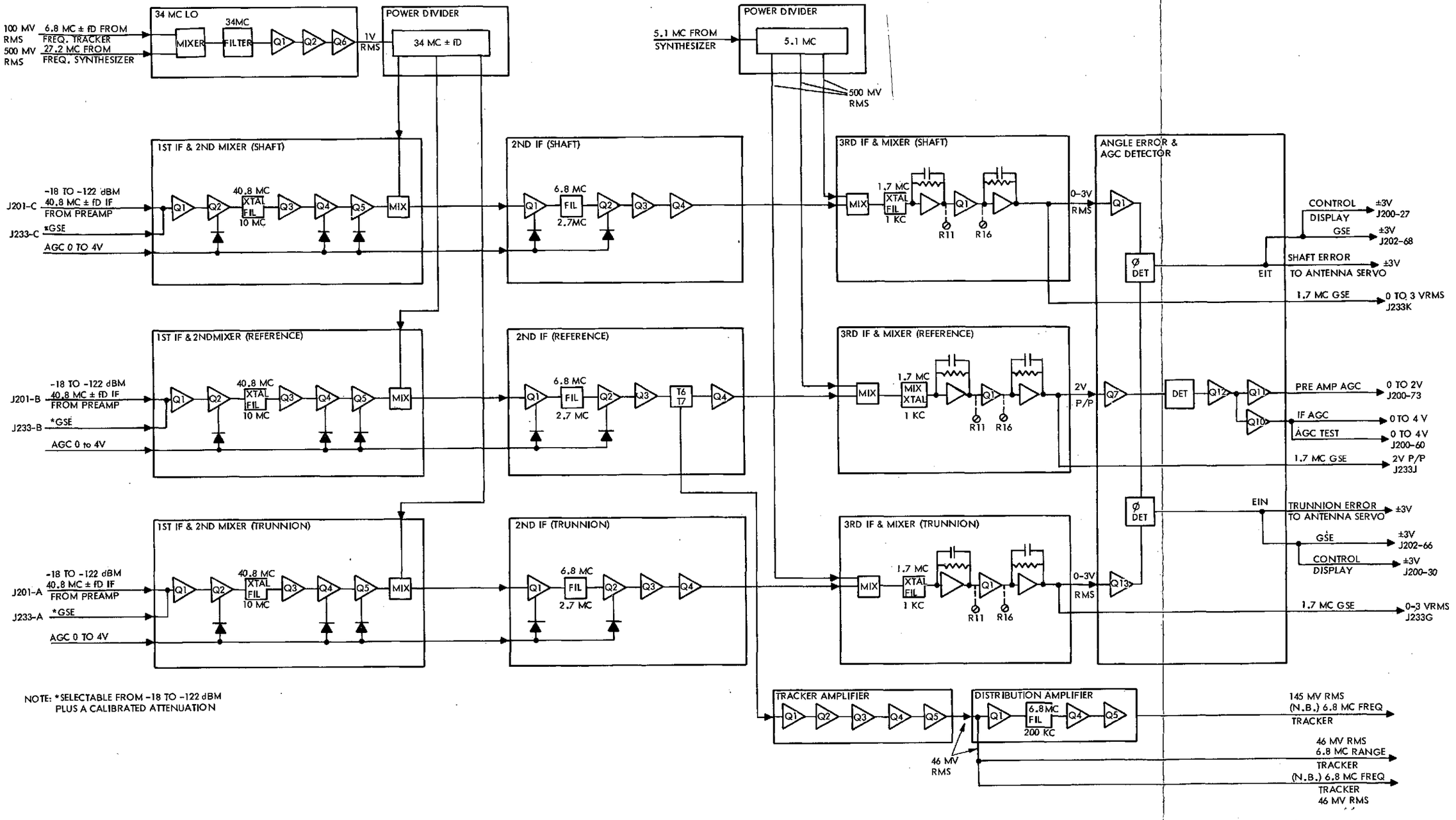


Figure IV-4. Receiver Subassembly Functional Block Diagram

Each IF difference channel output drives a separate input to an angle error detector, and the sum channel provides a reference for the angle error detectors and the AGC Detector and Amplifier.

Angle error outputs feed the servo loops for antenna control.

The AGC output is a dc voltage controlling the gain of the first and second IF's of all three channels as well as that of each pre-amp in the antenna.

The Receiver also provides a 6.8 mc output from the second IF of the reference (sum) channel to the Tracker Amplifier. This in turn feeds a distribution amplifier whose outputs go to the Frequency Tracker and the three tone Range Tracker.

Inputs are supplied to the Receiver from the Frequency Synthesizer and Frequency Tracker. The Frequency Synthesizer provides a 27.2 mc reference signal to the mixer of the 34 mc Gated LO and a 5.1 mc input (via a Power Divider) to the third mixer in each of the third IF amplifiers. The Frequency Tracker provides an input to the mixer of the 34 mc Gated LO at a nominal 6.8 mc but deviates from this value by the frequency of the doppler.

In the non-cooperative mode, the receiver is gated off during the transmit time. Figure IV-5 is a simplified block diagram of the receiver showing these gating functions.

The initial gating is achieved by switching the first L.O. with a SPDT PIN diode switch. The PIN diodes attenuate the L.O. signal by approximately 40 dB when the diodes are cut off and passes the L.O. signal with less than 1 dB insertion loss when either diode is conducting. The PIN diodes are controlled by two PIN diode driver shown in RCA Drawing No. 2378757. A low level at the input of the driver will apply -50v to the PIN, thereby shutting it off, and attenuate the L.O. drive. A high, 5 vdc, at the input applies a positive level to the diode turns it on and passes the L.O. signal to the mixer.

Gating of the IF signal and the second L.O. are accomplished using identical circuits. A simplified block diagram for the second L.O. gate is shown in Figure IV-6. The L.O. signal

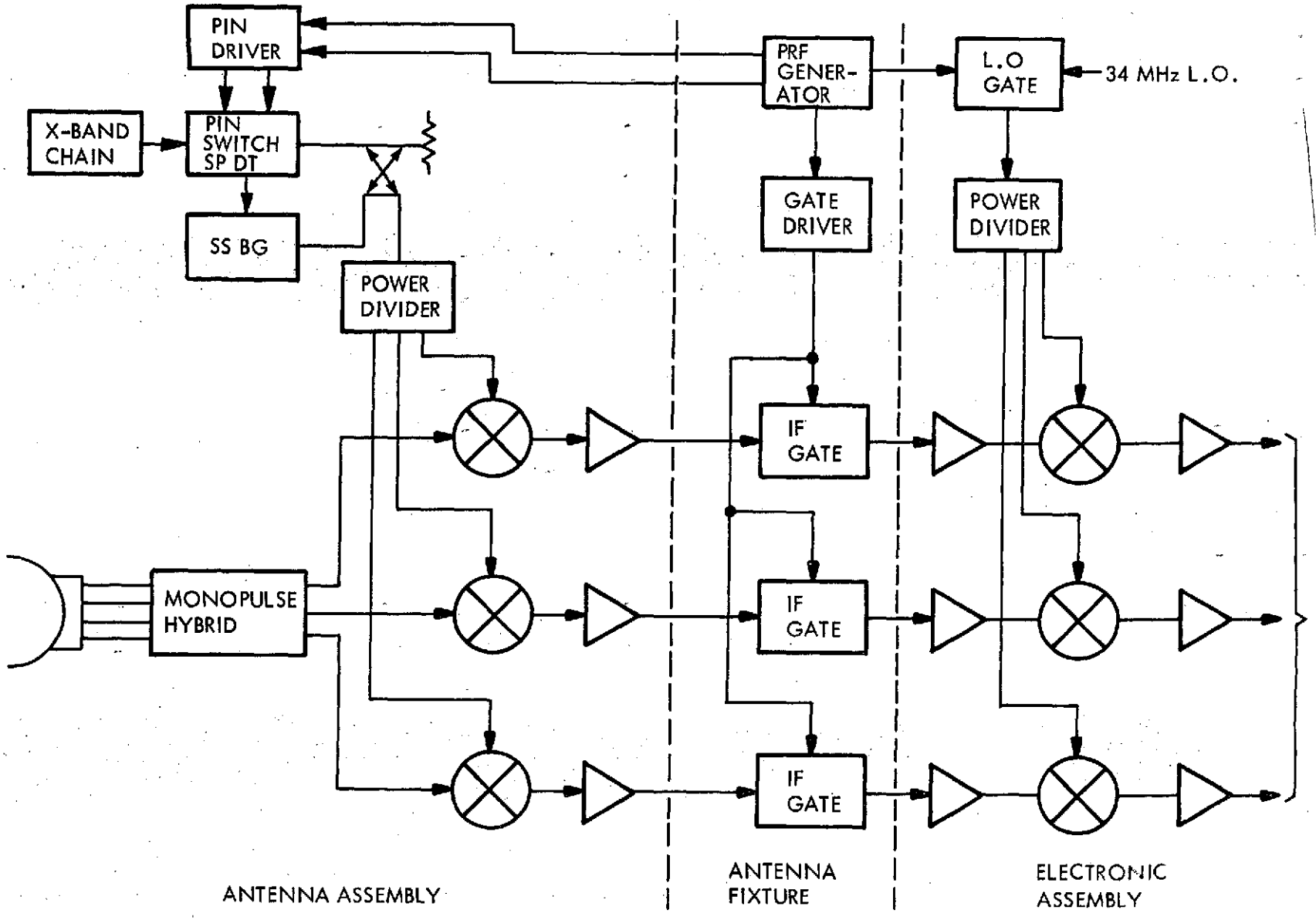


Figure IV-5. Block Diagram, Receiver Gating

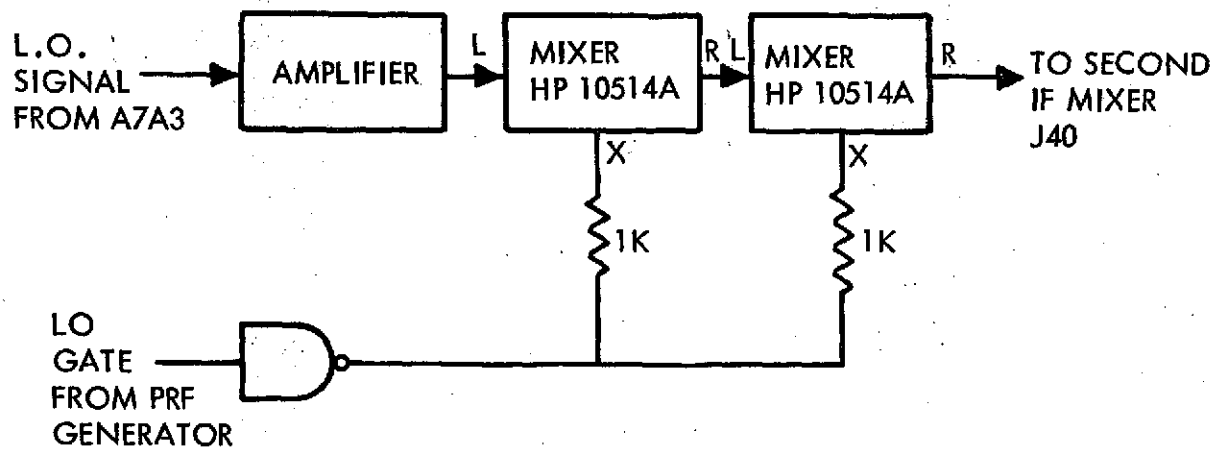


Figure IV-6. Block Diagram, L.O. Gate

is amplified and applied to the L input of an HP 10514A mixer. The R port is the output port. This is followed by a second mixer connected in the same manner. The L.O. gate is applied to an uncommitted collector gate. The output collector is connected to a 12v source and, via a 1K resistor to the X port resulting in minimum insertion loss. When the L.O. gate is high the input is 0 ma, resulting in maximum attenuation of the applied signal.

The IF gates shown in Figure IV-7 are identical in construction. One amplifier/mixer pair is used for each receiver channel. One additional driver gate has been provided to drive the three channels. The logic input to the IF gate is the inverse of the L.O. gate, i.e., the gate is "ON" with a high input and OFF with a low input.

The first IF amplifier in each channel is identical and uses matched transistors and diodes. A 10 MHz bandwidth lumped filter sets the bandwidth for the first IF, the AGC stage, and the second mixer. The filters are fixed tuned, hermetically sealed LC filters. Grounded base

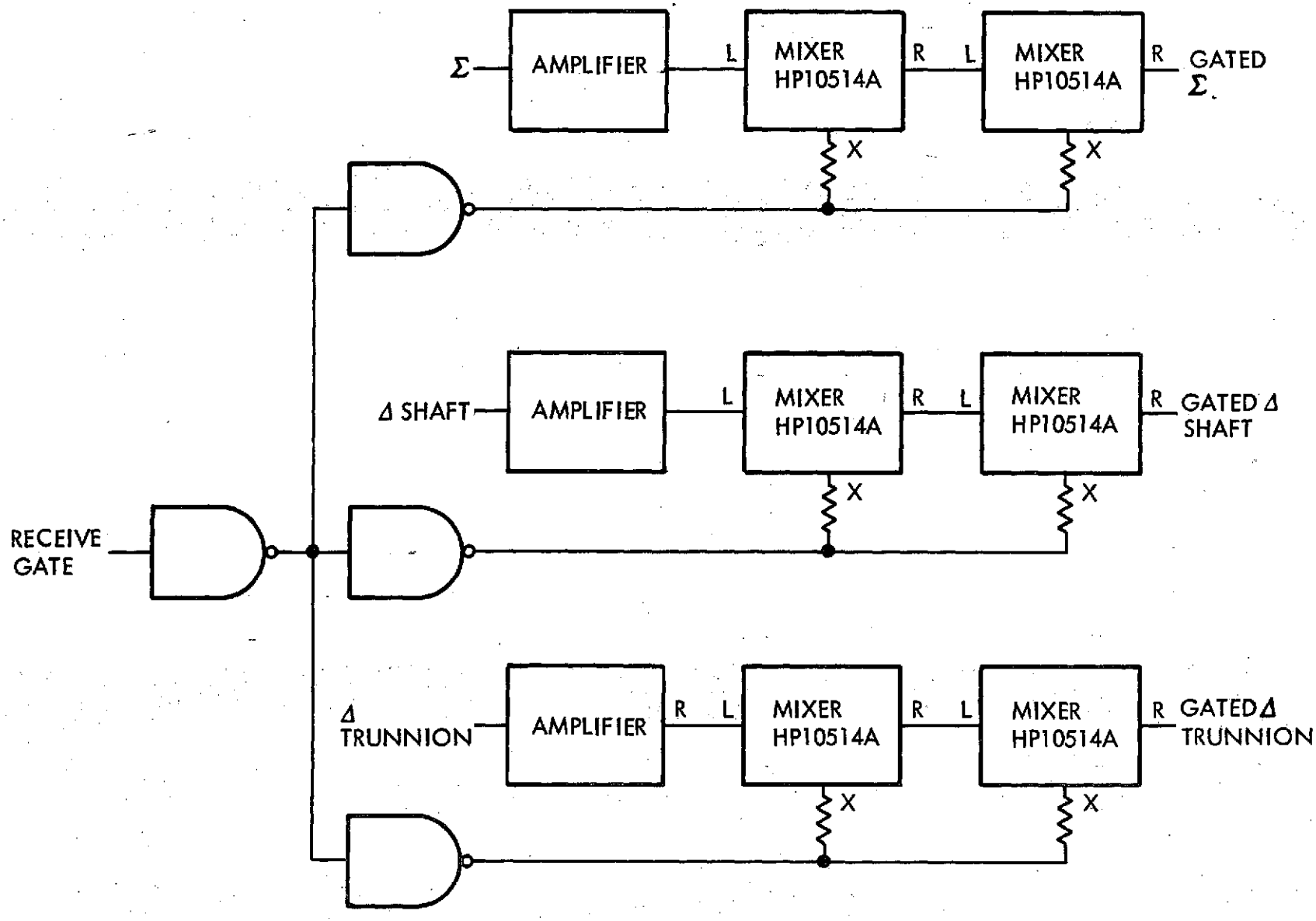


Figure IV-7. Block Diagram, IF Gate

amplifiers are used due to the phase tracking requirements. The 40.8 MHz signal is applied to a double balanced mixer which provides high isolation to prevent cross coupling between channels via the L.O. and, also, the rejection of spurious frequencies on the L.O. The other signals applied to the mixer is 34 MHz from the 34 MHz Gated L.O. This signal is applied only when radar returns are being received. During transmit the 34 mc signal is cut off. The 34 MHz L.O. has inputs of 27.2 MHz from the Frequency Synthesizer and 6.8 MHz ± the doppler contained in the 6.8 MHz coming from the Frequency Tracker. The 27.2 MHz and 6.8 MHz signals are mixed and passed through a filter to allow the 34 MHz to pass and attenuate the other mixer products. The bandwidth of the filter passes all doppler variations contained in the LO signal. It is amplified by two grounded base stages and applied to a power divider via the LO gate which gates the 34. The signal is now divided by a power splitter and passed to the mixer in the first IF. The output of the first IF is 6.8 mc which is applied to the second IF.

In the second IF amplifier the 6.8 MHz signal is amplified and passed to a single pole 2.7 MHz filter to provide the predetection bandwidth for the trackers. The filter is a shunt parallel tuned circuit. The signal is amplified and passed to the third IF. The reference channel also drives the tracker amplifier. The output to the tracker amplifier is constant for all signal levels in the dynamic range of the receiver because the remaining gain on the receiver ahead of the AGC detector is fixed. This output is fed to an emitter follower which lightly loads the second IF reference channel so that it will maintain tracking with the difference channels. The signal is amplified by four common base stages and applied to the distribution amplifier. It is then coupled through an emitter follower to a 200 kc bandwidth filter to isolate the frequency tracker channel.

The output of the second IF (that goes to the third IF) is 6.8 MHz. This is fed to a mixer which has input of 5.1 MHz from the Frequency Synthesizer. The output of this mixer is a 1.7 MHz signal which is passed through a 1 kHz crystal filter to remove the undesired mixer products. In addition to this rejection the filter also reduces the amount of broadband noise at the output. After the filter there is a gain control and a phase shift network. The purpose of the gain control is to provide a means of adjusting and equalizing the overall gain of each channel which includes the first, second, and third IF amplifier. The gain control

allows trimming to take up small variations in gain which may occur in any of the units when the system is boresighted. The phase shifting network is also used in boresighting to equalize any variations in phase which may occur in each channel from the pre-amplifiers through the third IF.

The outputs of the third IF amplifiers are applied to the angle error detectors to provide the necessary AGC control voltages to the pre-amplifiers, the first IF and the second IF amplifiers and to normalize the three channel gains with respect to the sum channel. It, also, provides a DC output voltage to the servo amplifiers which is proportional to the output signal level of the shaft and trunnion axis third IF amplifiers.

The shaft and trunnion error signals for the servos driving the antenna are obtained by phase sensitive peak detectors. The output of each error channel is buffered by two common emitter amplifiers and applied to a transformer which provides two signals 180 degrees out of phase. The reference channel signal is summed with the transformer output of each error channel and the sum and difference signal is applied to peak detectors. The signal is then applied out to the servo control amplifiers.

The AGC voltage is derived by the reference channel output. This output is applied to a peak detector, and then passed through a low pass filter and compared to a reference voltage. The difference is amplified and frequency compensated to provide the required AGC frequency response. The resultant DC output is then applied directly as the AGC voltage to first and second IF amplifiers.

The AGC voltage for the pre-amplifier is obtained by tapping off a portion of the first IF AGC voltage and amplifying it in a non-inverting amplifier. This output is delayed in level from the IF AGC.

The outputs of the third IF amplifiers are monitored by the GSE. The shaft IF output, has a variable amplitude of 0 to 3 vrms. The trunnion IF output, has a variable amplitude of 0 to 3 vrms. The reference IF output, has a constant 2v peak-to-peak amplitude. These signals are at 1.7 MHz.

The shaft error and trunnion error outputs of the angle error and AGC Detector are monitored by the GSE. The signals are DC voltages with limits of +3 volts to -3 volts. These same signals are applied to a metering circuit for readout in the Control and Display Assembly.

The AGC Test output is supplied to a metering circuit for readout in the Control and Display Assembly. The signal is variable from 0 volts DC to +4 volts DC.

1.2.2 Frequency Synthesizer Subassembly

The basic operating frequency of the synthesizer is 1.7 mc which is derived from a voltage controlled crystal oscillator. The output of the oscillator is used to drive multiplier chains and a divider network. The 1.7 mc is applied to a multiplier chain which employs a tripler and a double tuned amplifier that generates a 5.1 mc signal which is used in the Receiver as the third IF mixer excitation. The output of this multiplier chain is 5 mw. The second multiplier chain (X16) is used to generate the 6.8 mc and the 27.2 mc signals. This multiplier uses a pair of quadruplers. The output of the first quadrupler is 6.8 mc at a 5 mw level. The 6.8 mc is then amplified and supplied to the Frequency Tracker and Range Tracker, to the GSE Connector, as a 6.8 mc Test signal, and to the non-cooperative mode transmitter. The 6.8 mc is also supplied to a second quadrupler which generates the 27.2 mc signal that is applied to an amplifier at a 10 mw level. The output of the amplifier is sent to the receiver as the Gated LO mixer excitation. The 27.2 mc is also applied to a crystal filter for sideband rejection. A filter output of 27.2 mc is supplied to another multiplier which uses a tripler to generate the 81.6 mc signal for the mixer. The other input (20.825 mc) to the mixer is derived from the basic 1.7 mc oscillator which is supplied to a divider network where it is divided by two using varactor diodes with tuned circuits in the input and output. Following a second "divide by two network" the frequency is 425 kc at a 5 mw level, which is sent to a X49 mulitplier which generate the 20.825 mc mixer input signal. The 20.825 mc and 81.6 mc signals are mixed in crystal mixer, amplified, filtered.

The resultant 102.425 MHz signal is sent to a phase detector where it is compared to a 102.425 MHz reference signal from a crystal controlled oscillator. The resultant error signal controls the 1.7 MHz VCXO. In this manner, all synthesized signals are interrelated.

The reference 102.425 signal, after amplification is used to drive a multiplier chain in the antenna. Other outputs from the divider network are applied to a X33 multiplier and a 425 kc amplifier. The input to the X33 multiplier chain is applied to a transistor whose collector is tuned to 212.5 kc, effectively dividing the 425 kc by two. It is next applied to a tripler and then to a times eleven multiplier amplifier and sent out as a 7.0125 mc signal which is used as a doppler bias mixer excitation in the Frequency Tracker. The other 425 kc output of the divider is amplified and sent out as 425 kc range readout clock excitation. A separate 12 v regulator is used for the 102.425 MHz reference crystal oscillator.

The multiplier stages consist of a Class A transistor stage which is biased in such a manner, that a small amount of input power will drive the stage into the nonlinear Class AB state. Thus harmonics are generated, and the capacitor coupled, double tuned circuit is used for filtering at the desired harmonic. Power Gain can ordinarily be obtained from this type of circuit for the harmonic number of five or less.

In the Divider circuits the input LC network contains a series tuned circuit and a parallel tuned tank circuit. The series tank is tuned to half the input frequency (850 kc) and the parallel tank is tuned to the input frequency (1.7 mc). This combination effectively divides the input frequency in half and prevents the 850 kc signal from getting back to the 1.7 mc oscillator.

The output LC network also has a series tuned circuit in addition to a parallel tuned tank. The series tank is tuned to 850 kc to allow passage of the signal generated by the varactor circuitry. The parallel tank is tuned to 1.7 mc which assures that none of the input signal (1.7 mc) will find its way into the load.

The block diagram of the Frequency Synthesizer is shown in Figure IV-8.

1.2.3 PRF Generator

The PRF generator provides all gating functions required by the radar in the non-cooperative mode of operation. Five different PRFs are provided in order to minimize the eclipsing

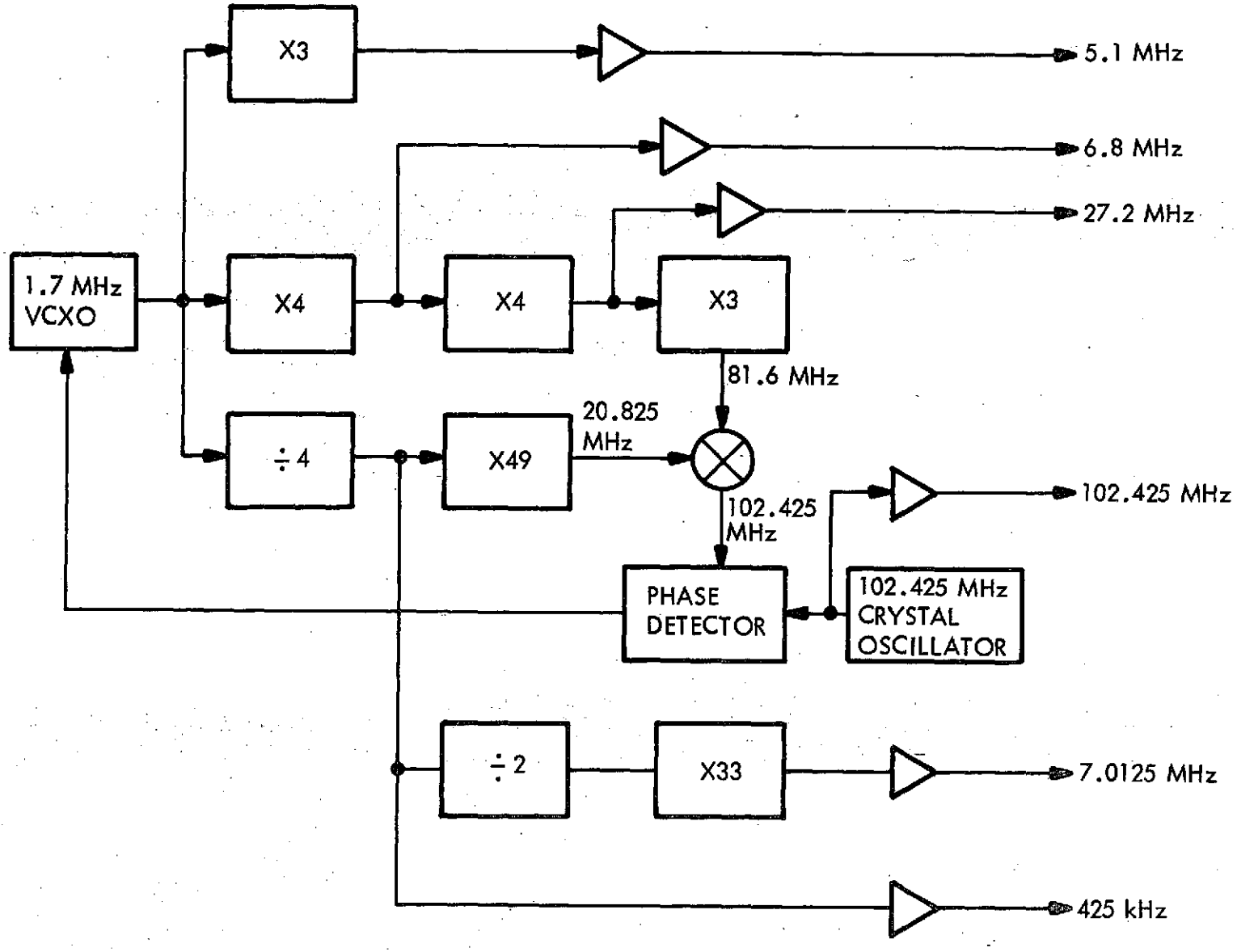


Figure IV-8. Block Diagram, Frequency Synthesizer

losses. A simplified block diagram is shown in Figure IV-9. Timing diagrams are shown in Figure IV-10.

Timing for the PRF generator is 10.15 MHz derived from an internal oscillator. A counter is incremented at a 10.15 MHz rate. The count is monitored for predetermined values, which determine the pulsewidth and the pulse recurrence frequency. The PRF control monitors the counter contents for a prewired count. When this count is achieved, the PRF control output goes high. On the next positive going edge of the 10.15 MHz clock, the counter is cleared and the PRF control output goes low. This results in a pulse at an interval determined by the prewired value. Five values are prewired to obtain the five PRFs desired (120, 118, 116, 114, 112). This results in the PRF's of 85 Kpps, 86.4 Kpps, 87.5 Kpps, 89.5 Kpps and 91 Kpps.

Simultaneous with the clearing of the counter, three flip flops, the transmit gate, the X-band gate and the receive gate are set. These gates turn on the transmitter and deactivates the receiver. After 49 clock pulses the pulse-width control output goes high. On the succeeding positive going edge of the clock the transmit gate is reset, turning off the transmitter. One clock period later, the X-band gate is reset, turning on the first LO. After an additional three clock periods, the receiver gate is reset, turning on the receiver.

The X-band LO gate is delayed one clock pulse, 100 nanosecond, relative to the transmit gate to compensate for delays in transmitter turnoff. An additional 300 nanosecond delay is introduced in the receiver gates to allow settling of transients created by the X-band gate.

One PRF is transmitted for 176 pulses. The PRF select is then incremented and a second PRF is transmitted. The PRF select is not incremented if the inhibit line is low. The inhibit line is controlled by the PRF controller located at the radar electronic assembly.

Operations of the PRF controller is separated into three phases, search, acquisition and track. During the search phase, indicated by the lack of frequency tracker lock, the inhibit line is high and all PRFs are continuously scanned. The acquisition phase extends from frequency tracker lock-on until track is initiated as indicated by the presence of the data

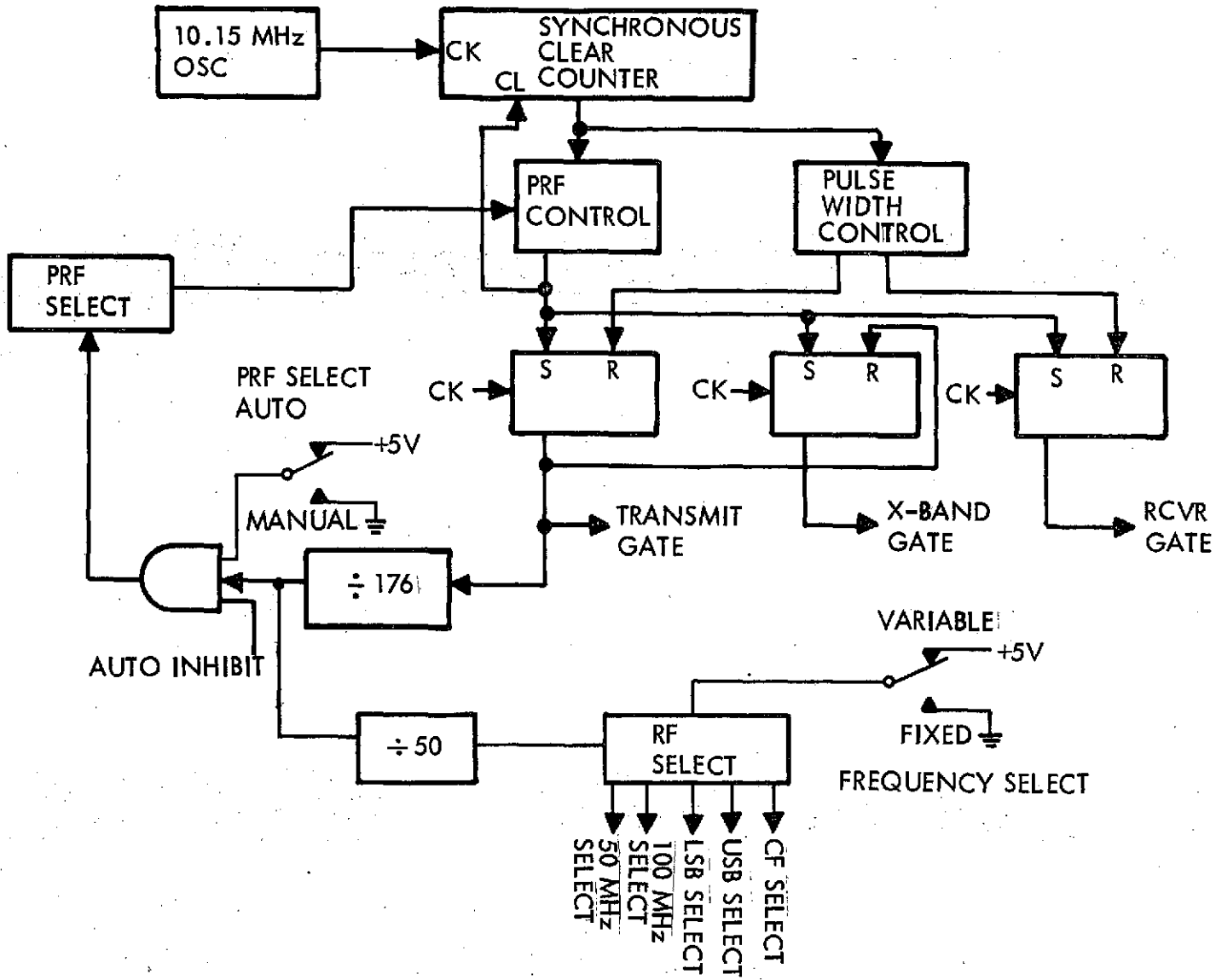


Figure IV-9. Block Diagram, PRF Generator

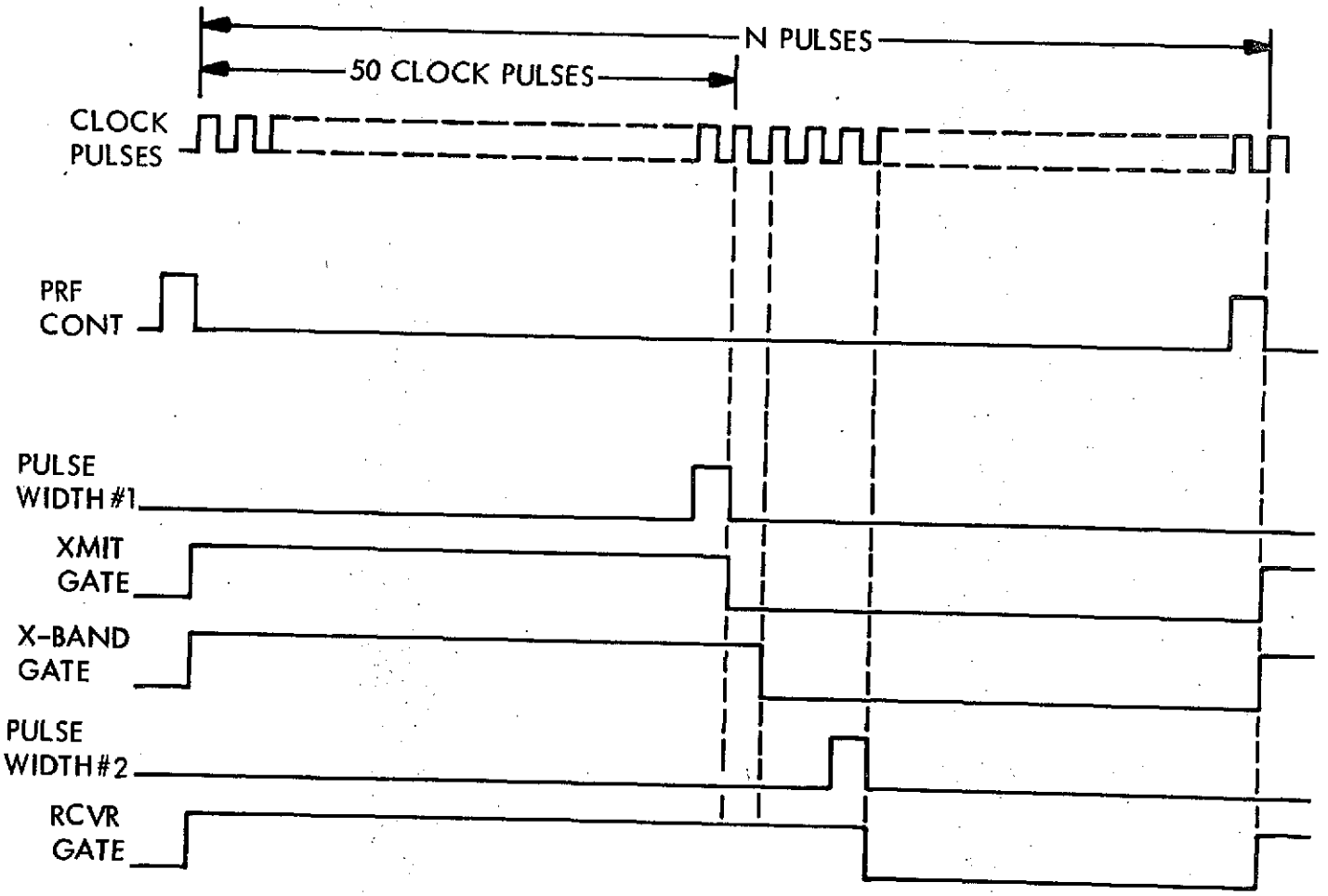


Figure IV-10. Timing Diagram, PRF Generator

good discrete. During this phase PRF sequencing is inhibited. The track phase is initiated by the presence of the data good discrete. During the track phase, target range is known. A PRF is selected which produces an AGC in excess of a reference voltage. The reference voltage is a function of target range and is given in Table IV-A.

Table IV-A.

Range (nmi)		AGC Reference	Adjustment
From	To		
6.32	Max. Range	0.8 v	R2
3.16	6.32	1.3 v	R3
1.58	3.16	1.7 v	R4
0	1.58	2.4 v	R5

The desired PRF may also be selected manually by placing the PRF select switch to manual.

During frequency diversity operation, one RF frequency is transmitted for 8800 pulses (50 x 176) as determined by the divide by 8800 counter. The counter output increment a three stage, divide by five counter. The first stage select the offset frequency, 50 MHz of 100 MHz. The second stage selects the upper or lower sideband. The third stage, the most significant bit, selects the center frequency. When the center frequency is selected all other select lines, 50 MHz, 100 MHz, upper sideband and lower sideband, are at a low. Center frequency is also selected by placing the frequency select switch into the fixed position.

1.2.4 Frequency Tracker Subassembly

1.2.4.1 General

The Frequency Tracker, shown in Figure IV-11 operates in acquisition and track modes. The acquisition mode is an unlocked searching condition prior to lock-on to the target reply during which time the radar receiver is swept ±121 kHz about a center frequency of 9832 MHz. Upon detection of the signal, the frequency tracker stops sweeping and acquires phase lock of its VCO with the incoming signal. In the non-cooperative mode, the receiver is swept 0 to 10 kHz relative to 9832.8 MHz.

The Frequency Tracker provides for phase locking the signal to the synthexiser reference so that the coherent detector may recover the FM tone data or phase data from the incoming signal. Doppler velocity is obtained by measuring the absolute frequency difference between the received signal and the frequency reference of the synthesizer. Frequency lock is used in the non-cooperative mode.

1.2.4.2 Acquisition Mode

When the Frequency Tracker is first turned on it is in the acquisition or searching mode. Assuming there is no receiver input (no lock on), the sweep generator provides a sawtooth voltage at ±121 kHz, 0 to 10 kHz in the non-cooperative mode. This voltage is applied to the VCO causing it to sweep in frequency, linearly with time. The VCO output frequency is mixed with 27.2 MHz in the receiver to produce a frequency of near 34 MHz.

The 34 MHz signal is the LO input to the receiver and when it is mixed with the 40.8 MHz return signal it gives an output IF signal of 6.8 MHz. If there is no 40.8 MHz signal, there is no 6.8 MHz output signal from the Receiver to the Frequency Tracker and the VCO will continue to sweep. Assume a 40.8 MHz signal is applied to the receiver. The Threshold Detector senses the incoming noise for presence of a signal by comparing a narrow band frequency window with the wideband noise level. Until detection of a narrow band signal,

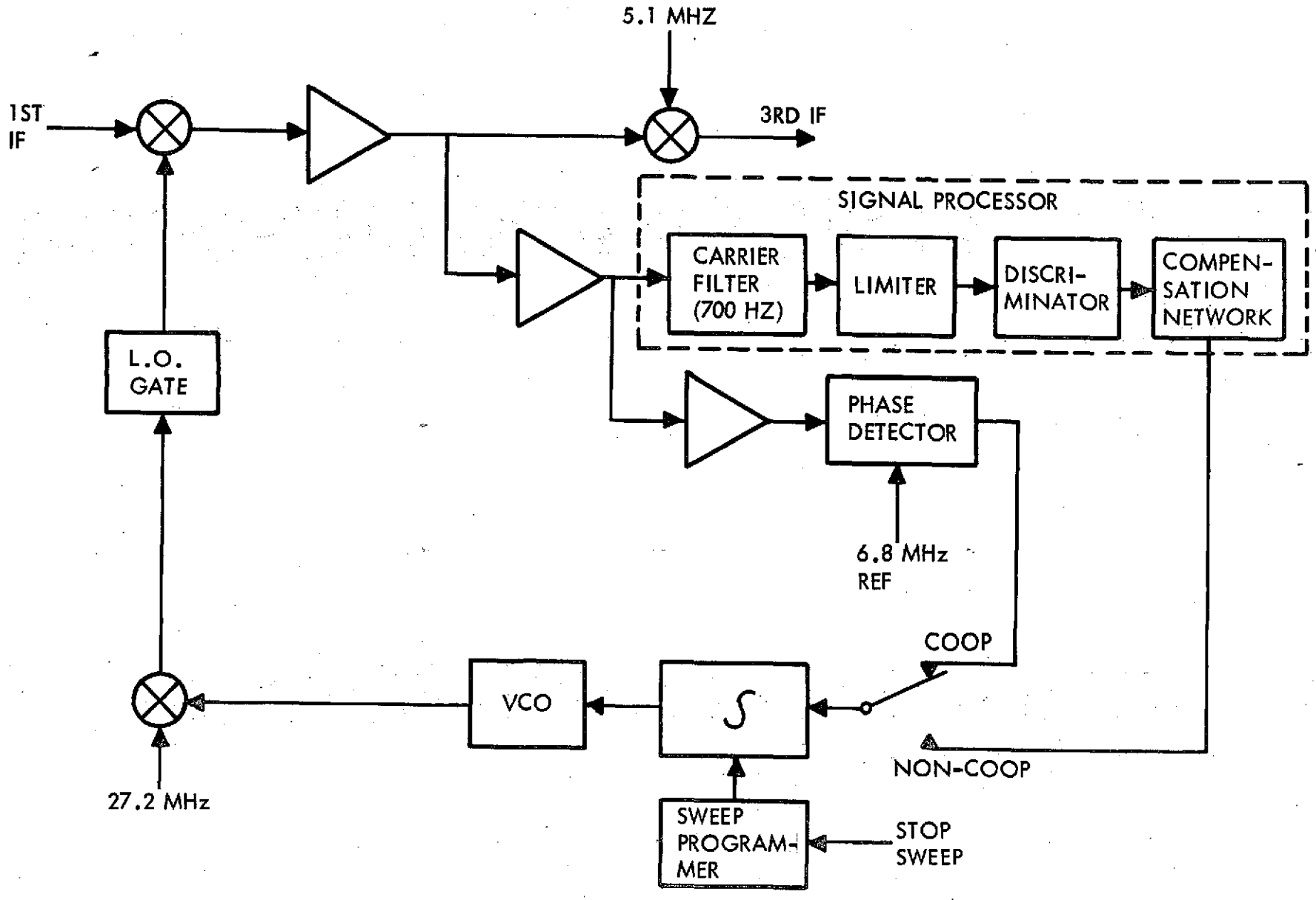


Figure IV-11. Block Diagram, Frequency Track Loop

the VCO continues to sweep. Upon detection, by a preset difference, the detector stops the sweep. The stop sweep signal is also connected to the Control Display Assembly as a frequency lock or PLO signal. The frequency of the VCO is now controlled by the output of the Filter. This dc voltage output changes the VCO frequency until frequency coincidence is attained.

The VCO is now locked to the incoming signal. The particular frequency of the VCO indicates range rate (velocity). This frequency is sent to the data processor as range rate output for processing and finally for display. The VCO output is also applied to the Doppler Sense Detector. The Doppler detector determines that the doppler frequency return signal is associated with an opening or closing target and removes the IF bias frequency of 6.8 mc and provides a pulse train with a recurrence frequency equal to the doppler frequency. In phase and quadrature components of the 6.8 mc references are applied to identical mixers. The second input is the 6.8 mc ± fd signal. The output of the mixer consists of in-phase and quadrature stripped doppler. These are applied to Schmitt trigger circuits. The doppler square wave outputs are applied to a quadrature detector whose output consists of a train of pulses equal to the doppler frequency, and are applied to a f/f consisting of a cross coupled dual gate. The logic outputs of the detector indicate the sense of the doppler signal. The square wave signal is also coupled to the Control Display Assembly Interface as a pulse 3 μsec pulse for each cycle of doppler.

1.2.4.3 Track Mode

Operating in the cooperative mode the input signal from the receiver is 6.8 mc and is compared with a 6.8 mc reference from the Synthesizer. The reference is shifted by 90 degrees (in a power divider) and applied to the balanced modulator. The output of the balanced modulator is a dc voltage, when the two inputs are at the same frequency. This dc voltage is a measurement of the phase difference between the two signals. If the two inputs are in phase, the balanced modulator output is zero. Any change in phase causes a dc voltage, whose polarity depends upon which input is leading the other.

In the non-cooperative mode the input 6.8 MHz signal is filtered to remove unwanted tone and PRF lines. The filtered signal is limited to remove AM caused by PRF switching and provide a constant signal to the discriminator. The discriminator output is a measure of the frequency error. After loop compensation, the discriminator is supplied to an integrator and then to the VCO. This is type 1 system which results in no frequency error for a constant doppler.

1.2.5 Range Tracker Subassembly

1.2.5.1 Tone Generation (Reference Figure IV-12)

The 3.2768 MHz clock generator, generates the basic reference frequency that the three coherent tone frequencies are derived from, in the high speed counter. The three selected outputs of the high speed counter are then fed as square waves into three tone calibrator circuits where the signals are converted to sine waves of fixed amplitude and phase relationship. The tone signals are then routed out and used to modulate the transmitted signal.

The 3.2768 MHz clock generator consists of a reference oscillator followed by a pulseshaper and generator. The oscillator provides an output of 5 MW at a frequency of 3.2768 MHz. The pulse generator is a five stage unit which amplifies and squares the sine wave oscillator output and shapes a 100 nanosecond pulse capable of driving the high speed counter. Stage one and two amplify and square the input sine wave. The third stage is an emitter follower which drives a 50 nanosecond delay line. The output of the emitter follower travels to the end of the shorted delay line arriving in 50 nanoseconds. The polarity is reversed and the pulse reflected, arriving at the original end 100 nanoseconds after it was initiated. A portion of the reflected pulse (all but the last 100 nanoseconds) cancels with a portion of the original pulse (all but the first 100 nanoseconds) to form two pulses, each of 100 nanoseconds duration, a positive pulse followed by a negative pulse. The positive pulse turns on Q4. Q4 is a pulse shaper and a driver stage for the output stage. When Q4 is turned off Q5 conducts to raise the output level and allow a rise time of less than 30 nanoseconds. When Q4 turns on, Q5 turns off and the output is clamped to ground by CR3 allowing a fall time of less than 30 nanoseconds. The output of the pulse generator and shaper is coupled to the high speed counter.

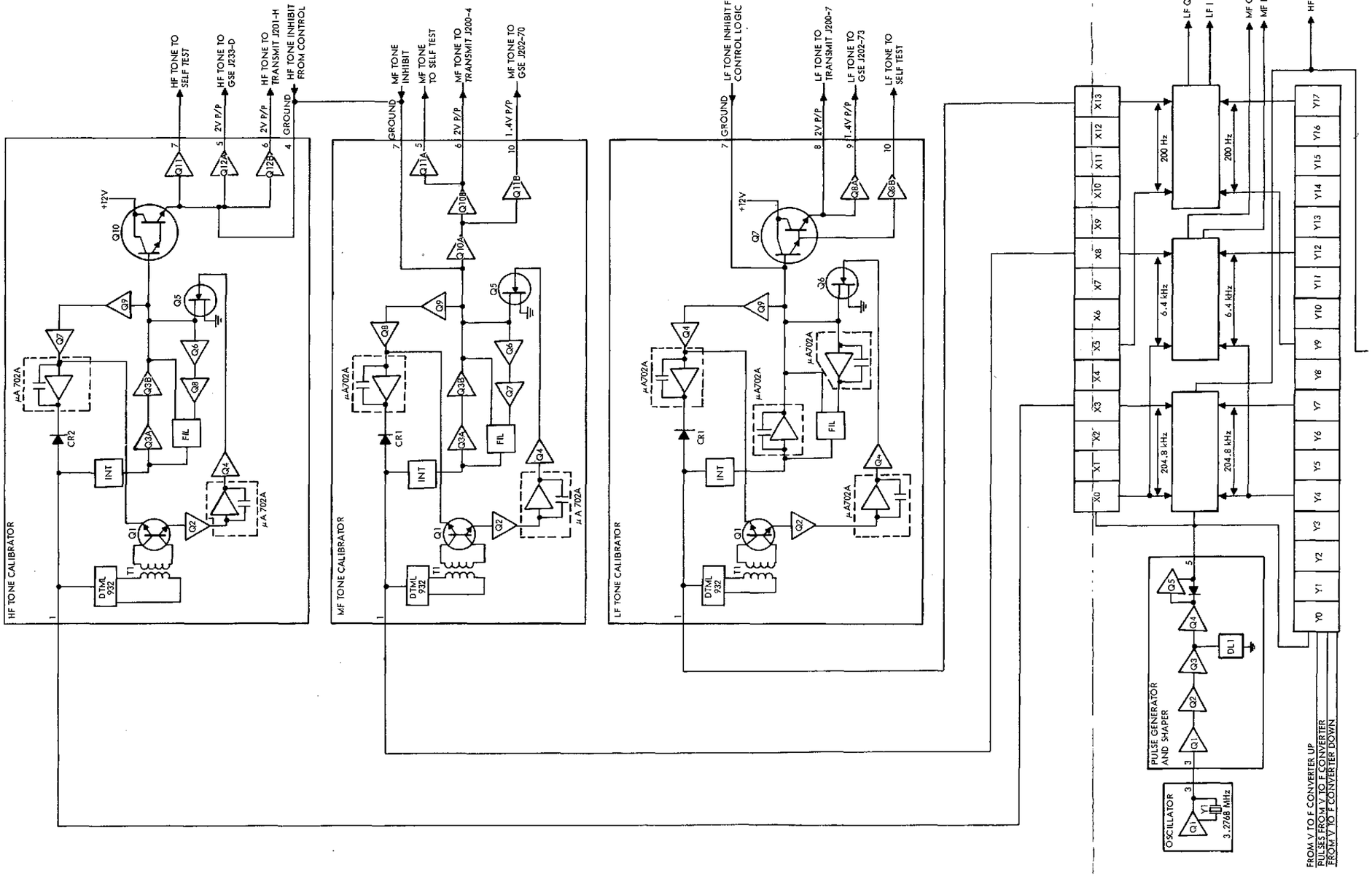


Figure IV-12. Tone Generation, Functional Block Diagram

The high speed counter is a 14 bit synchron combination parallel carry type, straight binary counter. It is used to provide the basic tone base for the ranging unit. Submultiple square waves of the 3.2768 mc clock, at 200 cps, 6.4 kc, and 204.8 kc are derived from the counter. These square waves are fed to the tone calibrators and converted to sine waves (tones) having a variable phase adjustment. Logic in the calibrator can inhibit the tones in conjunction with the control logic when required.

The tone calibrator converts a square wave input between 2.5 volts and 4.5 volts peak to a sine wave of fixed amplitude and phase error. The square wave input is limited (clipped) and controlled before integration to allow for a low distortion output. The input, after limiting, is applied to an integrator which reduces the harmonic content and is then applied to a bandpass amplifier, Q3A which has a tunable parallel tee network in the feedback path. The output of Q3B is used to drive the control circuits, Q9, Q8, and an uA702A as well as being the output of the unit. Tuning for the filter is accomplished by T1 which couples the tone input to a chopper Q1, which has as its other input the output of Q8, in the amplitude control circuitry. This square wave is chopped and applied through Q2 an isolation amplifier to a uA702A. The uA702A is used for voltage and temperature stability. This signal is now coupled to Q5, a unijunction transistor. The unijunction is used due to its variable impedance. This gives the required attenuation for the filter. The tone outputs are inhibited by the control logic until the frequency tracker has locked up. The H.F. and L.F. Tone Calibrator operation is essentially the same even though different circuit components are used.

The high speed counter has an output to the binary comparator. The comparator also has an input from the up-down counter. The binary comparator generates a square wave whose phase relationships with respect to a similar square wave derived from the reference counter is determined by the number in the up-down (range) counter. The lower frequencies, 200 Hz (LF) and 6.4 kHz (MF), have both an "I" output (in phase) and a "Q" output (90 degree out of phase) with respect to the associated transmitter frequency. The H.F. frequency (204.8 kHz) has only the "Q" output. The comparator is used to decode the three tones. In the case of the 204.8 kHz tone the first four least significant bits of the referenced counter

and the corresponding bits of the up-down counter are compared. For the 6.4 kHz tone the first nine least significant bits are compared. For the 200 Hz tone the nine most significant bits are compared.

When commonality exists (in a bit position or positions) in the decoding of two different tones, the decoders are combined into one and the resulting output is shared by each tone.

The 6.4 kHz and 200 Hz "Q" and "I" tones (square waves) are sent directly to the phase detector where they are compared with the incoming signal from the receiver. The 204.8 kHz "Q" tone (square wave) is applied to a delay line phase shifter using a tapped delay line to accomplish a vernier phase shift. The delay line has 15 tones of equal delay and the appropriate tap is selected digitally from the four least significant bits of the range converter. The input square wave is applied to an amplifier Q1, Q2 which drives the delay line. The logic signals are applied to a decoder whose output will energize only 1 of 16 switches. The energized switches passes the delay line signal to an isolation amplifier that drives the output amplifier Q7. The output signal is sent to the 204.8 phase detector for comparison with the received tone. Each tap of the delay line has a delay of 19 nanoseconds.

1.2.5.2 Range Computation (Ref. Figure IV-13)

In the cooperative mode, the received signal, along with a reference signal, is applied to the coherent detector, which is basically two 6.8 mc amplifiers driving a diode bridge phase detector. The reference input at 400 mv rms is amplified 20 volts peak-to-peak to provide the bias current for the bridge. The input signal, at 46 mv rms and 600 mv rms noise, is driven into the bridge by push-pull emitter followers. The detected output is then fed to the filter for each tone. The detected tone output level is 60 mv rms.

In the non-cooperative mode the received signal is applied to the Signal Processor shown in Figure IV-14.

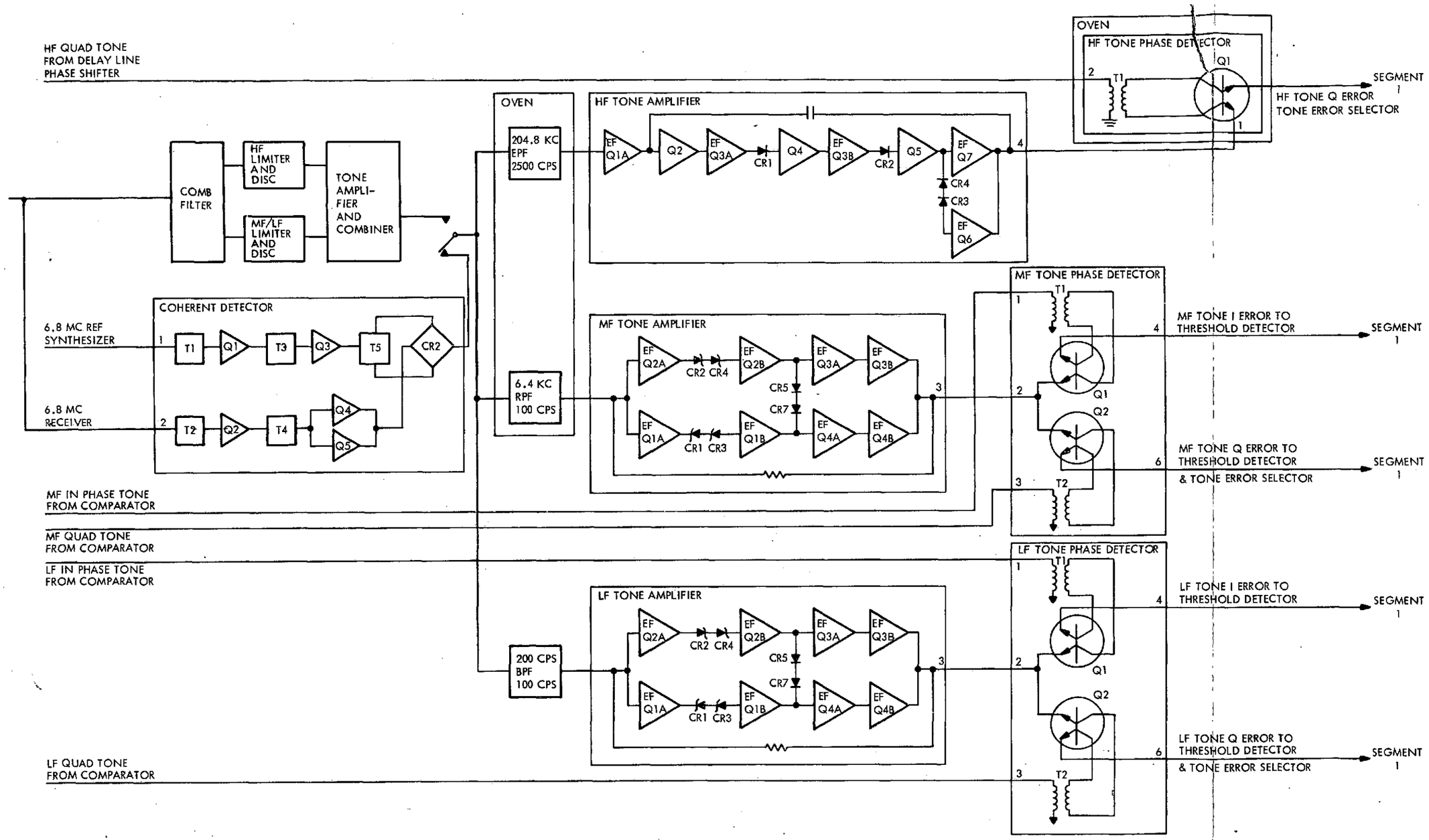


Figure IV-13. Range Tracker, Functional Block Diagram

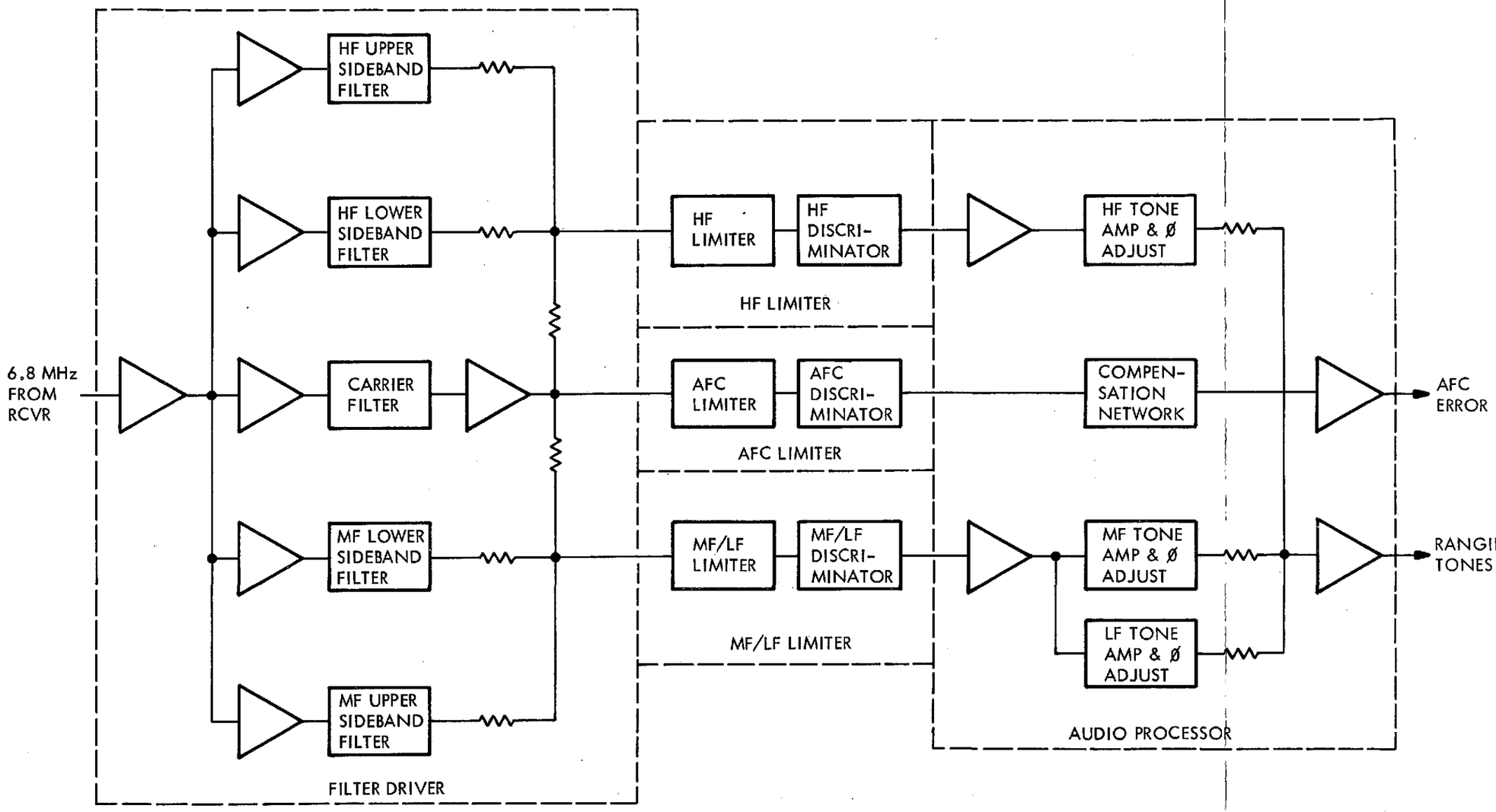


Figure IV-14. Block Diagram, Signal Processor

After buffering, the signal is processed by a bank of filters to extract the desired sidebands and remove unwanted modulation sidebands. The LF carrier sidebands are extracted by the carrier filter. The signals are recombined to form an HF channel and a MF/LF channel. Since each channel is the composite of three filters, each having a bandwidth of 700 Hz, the noise bandwidth in each channel is reduced to 2.1 kHz for a 50 dB signal/noise improvement.

The signals are then limited to remove unwanted AM modulation introduced by varying PRF's. Tones are extracted by the HF and the MF/LF discriminator. The tones are adjusted in amplitude and phase for proper system operation. The tones are combined and transmitted to the range filters for processing.

The filters are active bandpass filters with the following characteristics. Center frequencies of 200 Hz ± 0.1 Hz, 6.4 kHz ± 0.1 Hz, and 204.8 kHz ± 1 Hz. The bandwidths are 100 ± 10 Hz for the 200 Hz, and 6.4 kHz filters and 2000 Hz maximum for the 204.8 kHz. The outputs from the filter are 200 Hz, 6.4 kHz, and 204.8 kHz, which are fed to the tone amplifiers.

The tone amplifiers are used to amplify the output of the tone filters to a level that is adequate to drive the phase detector. The Low Frequency (200 Hz) and Medium Frequency (6.4 kHz) amplifiers are identical and the High Frequency (204.8kHz) amplifier is different. The LF and MF amplifiers will be covered first. The amplifiers are used to amplify the input to a 10V peak-to-peak level. The circuits are basically a single stage push-pull amplifier, with emitter follower input, and a Darlington configured output. The HF amplifier is used to amplify the input to a 6.8 volt peak-to-peak level. The amplifier is a three stage operational amplifier, with emitter follower input, and emitter follower output. The signals from three tone amplifiers are fed to the phase detectors. There is a phase detector for each of the three tone frequencies. Each contains a demodulation channel in which the received tone is chopped with a square wave which is 90° out of phase with the transmitted reference tone. These channels are used as nulling devices for range measurement and referred to as the quadrature channel. The 200 cps and 6.4 kc phase detectors contain a second channel in which the same input tone is chopped with a square wave which is in phase with the transmitted reference tone. These channels serve to indicate tone and null points and are referred to as the in-phase channel. In its nulling process, involving the quadrature

channel, the reference square wave is shifted in-phase until the dc output of the channel is zero. The amount of phase shift required is the measure of range. The in-phase channel reference gate is shifted along with the quadrature channel reference gate, and the dc output of the in-phase channel is maximum when that of the quadrature channel is zero. The in-phase channel output supplies the threshold detector with information for determining an input tone signal present condition, and in combination with the quadrature channel output, for determining the proper null point.

Operation of the quadrature channel is as follows. The integrated chopper Q2 is used for demodulation. Turned on by applying a drive current from base to collector, during which time, a short circuit appears between emitter one and emitter two. The drive current is supplied by the reference square wave which is coupled through T2 into the base collector circuit. The received tone is applied to Q2 emitter. The chopped tone which appears on the other emitter is the output of the phase detector. The output dc level is maximum when the received tone and the gate are in phase and zero when they are 90 degree out of phase. The in phase channel operates in a identical manner to the reference channel. The outputs from the in phase channels (referred to as "I" error signals) are now applied to threshold detectors along with the "Q" errors. The "Q" error signal is also applied to the Tone error selector. The purpose of the threshold detector is to provide modifying inputs to the acquisition logic for reducing range acquisition time by means of associated logic elements in the acquisition logic. The 200 cps threshold detector provides an on target signal when the range counter has been slaved to within 30 degrees on null. The signal is used to imitate a timing delay, sufficient for the loop to settle to a true null, prior to removing the range counter fast slew signal and releasing the acquisition relays. In this way, delay timing is employed only when the tracking loop has settled to a linear error slope region. Circuit operation is as follows (Ref. Figure IV-15).

The input to Q1 is from the phase detector. The input is applied to two comparator circuits (uA702A), one of which is referenced to a positive DC level, and the other to an equal value but of negative polarity. The comparators are so arranged so that the two outputs when fed to a two input NAND gate (in the acquisition logic) represents an acceptance "window" of approximately 40 degrees in width centered about the null. The other Comparator shown

C-2

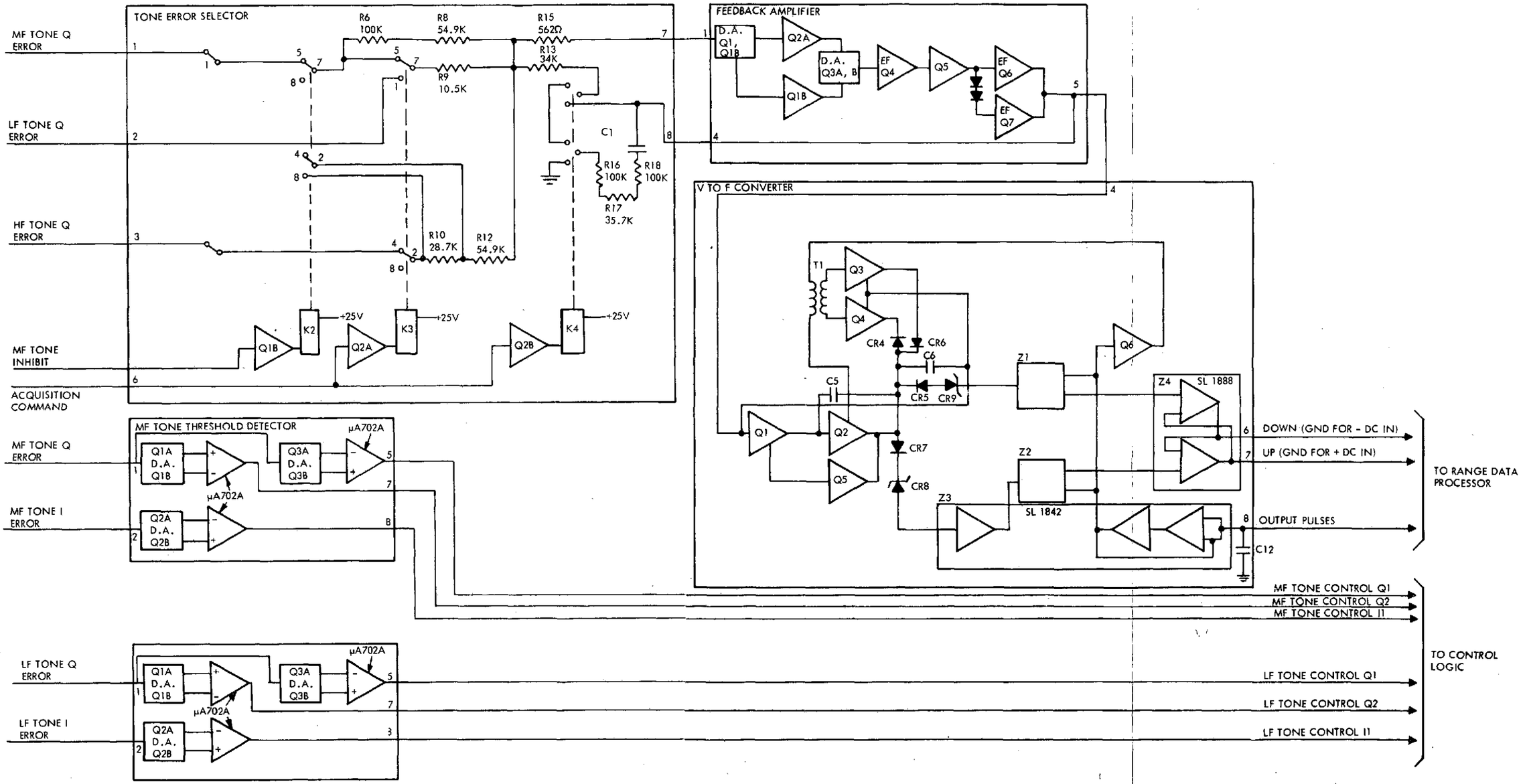


Figure IV-15. Transponder Mode Range Tracker, Functional Block Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

has its input from Q2 which is the "I" error from the phase detector and is in quadrature with the input to Q1. This is used to differentiate between a true "on target" signal and a false null, represented by the point where the phase detector output is at or near null but the polarity is incorrect for the tracking loop. The output of this Comparator is NANDED with "Q" Comparator outputs to generate the On-Target signal while the inverse "I" signal is NANDED with the "Q" outputs represent a false null. The NANDING is done in the acquisition logic circuitry. The 6.4 kHz threshold detector is identical to the 200 Hz, explained here, except that only the ON-TARGET condition is used in the acquisition logic.

The "Q" outputs of the phase detectors are applied to the tone error selector which is used to control the gain and frequency dependent characteristics of the feedback amplifier in the acquisition and tracking modes. The unit also receives inputs from the acquisition logic. From the input, the tone phase errors are selected and mixed as required for the various operations of the feedback amplifier. When the acquisition command is received from the acquisition logic, relays K3 and K4 are energized. Contacts of K3 inject the 200 Hz phase detector output into the feedback amplifier inputs (R6, R8, and R9 are selected) so as to mix the magnitude of the 200 Hz and 6.4 kHz phase errors in a 16:1 ratio. Contacts of K4 cause K3 to be connected between the output and input of the feedback amplifier so that an inverting gain with flat frequency response is obtained. Since the 6.4 kHz input is scaled down by 16 times, but the tone frequency ratio is 32 to 1, the resulting error slope to the 6.4 kHz tones (as seen at the amplifier input) is twice that of the 200 Hz error. One end of R16 is grounded through contacts of K4 so that C1 becomes charged to the output voltage of the feedback amplifier. As the tracking loop settles to a null, this voltage represents the velocity of the target since the voltage to frequency error pulses into the range counter are directly proportional to the voltage. During acquisition the HF tone error is removed by contacts of K3. When the acquisition command is removed the 200 Hz is removed from the input of the feedback amplifier and the amplifier is converted to an integrator. The normally closed contacts of K4 are used to select a portion of the 204.8 kHz tone error for mixing with the 6.4 kHz tone error. With an input tone error ratio of 16 to 1 the composite error slope resulting from the mixing gives an equivalent gain function of three times the value resulting from the 6.4 kHz tone. Only K2 is energized by the acquisition logic when the range is below 50 n mi. At this time contacts of K2 remove the tone and scale the 204.8 kHz tone error input

to the feedback amplifier. The only input to the feedback amplifier is the 204.8 kHz tone error. The transistors shown are relay drivers. The output from the tone error selector is applied to the feedback amplifier.

The Feedback Amplifier consists of four stages, the first, Q1B, Q1A is a differential amplifier followed by emitter follower buffers Q2A, Q2B is used to provide improved isolation, the second stage, Q3A, Q3 is a differential amplifier with an emitter follower Q4 buffering the input, the third single ended stage Q5. The output stage Q6, Q7 is a complimentary Symmetry driver. Feedback for the amplifier is through the tone error selector. The output of the Feedback amplifier is applied to the voltage to frequency converter. (V-F)

The V-F converter develops the necessary signals required by the up-down counter. It supplies pulses of 6 μs duration whose frequency is proportional to the absolute value of the input voltage. The converter also controls the up down lines of the up down counter. These lines should be at 4V and OV or vice versa, depending on the polarity of the input voltage. The up down counter requires no other signals in performing its counting operation. The input signal is applied to Q1 and integrated. The output of Q1 is applied to CR5 and CR7 (via C5) which will conduct at a prescribed level, established by CR9 and CR8 respectively, and trigger either Z1 or Z2 which are one shot multivibrators. The output of either multivibrator will be coupled through Q6 and energize the dump circuit consisting of T1, Q3, Q4, CR4 and CR6, which will cause C6 to discharge through the diode transistor network that is biased on. The output pulse is developed by inverting the output of the multivibrator Z1 or Z2. Note that Z1 is triggered by a negative input voltage and vice versa. An output from either Z1 or Z2 will trigger one of the input lines of the flip-flop Z4. The position of the flip-flop, therefore is governed by the polarity of the input signal. Transformer T1 is a pulse transformer which will couple the output pulse to transistor Q3 or Q4 depending on polarity and bias diodes CR4 or CR6 on allowing C6 to discharge in the prescribed time. If C6 doesn't discharge 20 ms after a pulse has been received by T1 the output of the integrator will remain high and the multivibrator will not reset and the output pulse will disappear. The

"hang up" is corrected by C12. If the output pulse is grounded for more than 1000 ms, C12 will discharge lowering the input to Q6 within 1 volt of ground. Now the output will rise again causing C12 to recharge. Q5 is used for constant current source for Q1 and Q2. It also maintains CR5 and CR7 at the proper current level.

A tapped delay line, shown in Figure IV-16, is used to accomplish a linear phase shift of the 204.8 kHz (HF) tone. The delay line consists of 15 taps each having a delay of 19 nanoseconds or an overall delay of 285 nanoseconds for the entire delay line. The delay is used to increase the resolution of the system from a basic resolution of 150 feet to 9.38 feet.

The inputs to the unit are the 204.8 kHz (HF) tone to be delayed and the logic levels (4 lines) from the four least significant bits of the range counter. These govern the amount of delay for the tone. The 204.8 kHz (HF) tone is applied through Q1 and Q2 to the delay line as drive.

The logic levels are applied to a decoder network whose output will energize one of sixteen diode switches. The energized switch will pass the delay line drive signal to an isolation amplifier, (Q3, Q4, Q5 or Q6) that drives the output amplifier Q7. The output signal is applied to the HF phase detector for comparison with the demodulated received tone.

The decoder consists of Z1 through Z14 and operation is as follows:

Z4 and Z10 receive the logic levels from the range counter and apply them to the dual input gates. The eight dual input gates receive all possible combinations that can be derived from the four outputs of the range counter. Only one of these gates can be enabled at any time, because at any one time the four inputs can be in only one combination. The enabled gate will apply a logic level to the four inverters that are employed in Z5, Z8, Z12 and Z14. The inverter will invert the logic level and turn on diode switch. The switch that is energized will pass the delayed tone to the isolation amplifier and then to the output driver and out to the phase detector.

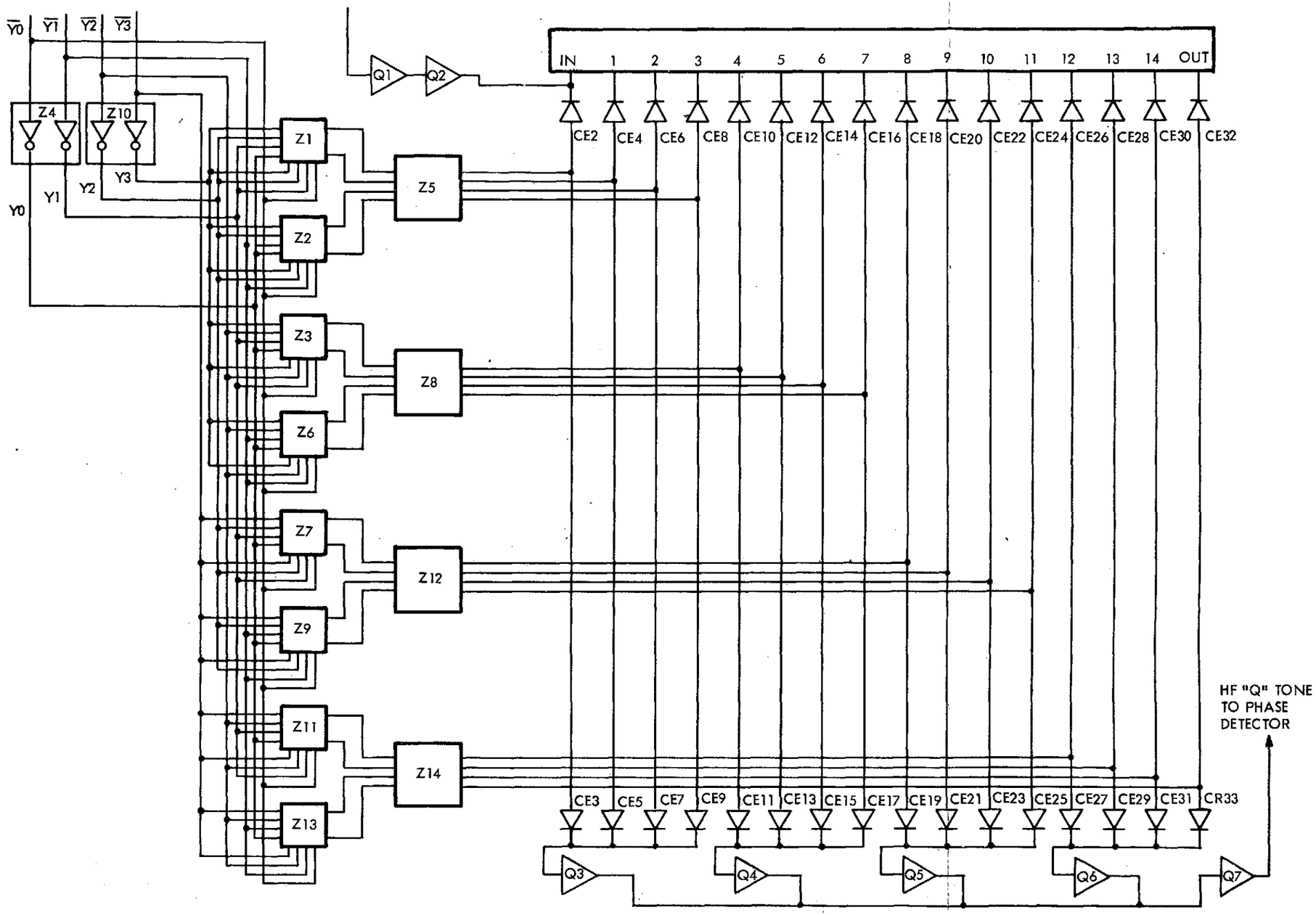


Figure IV-16. Delay Line Phase Shifter, Functional Diagram

1.2.6 Signal Data Converter Subassembly

1.2.6.1 Control Logic

The timing reference for the acquisition control logic is derived from the 200 Hz square-wave output from the high-speed reference counter. A ten-stage binary counter is used to generate timing intervals which are conditioned by the logic inputs. These ten stages provide for timing intervals up to 5.12 seconds. The control logic for the range tracker is shown on Figure IV-17. Timing waveforms at several points within the counter and at the output of various storage flip-flops are shown on Figures IV-18 and IV-19.

Acquisition commences at time t = 0, when the Frequency Tracker lock-on signal, the Auto Track Enable and Transponder Mode Select signals are received (all logic "1"). The receipt of these three signals causes the conditioning circuits to set the Flip-Flops to a known condition before the start of actual counting. The output of (1) is now 'down' (and will remain in this condition as long as the three inputs are present). It is applied to (2) for inversion, and then to the inverters (3) and (4). This output (down) is applied to the Up/Down counter as a reset which clears out the counter. The 'down' output of (1) is also sent to an inverter (5) whose 'up' output is applied to FF1 to remove the direct reset signal. The output of (5) is also applied to (6) where it is inverted and goes to the Track Delay F/F as a conditioning signal. The output of (6) is also inverted by (7) and sent to the Track Delay F/F to remove the direct reset signal. The output of (7) also goes to all ten stages of the counter to remove the direct reset signal. The 'up' output of (5) is applied to the Clock Control F/F, the Acquisition Hold F/F, and the Track enable F/F, to remove the direct reset signal and allows the F/F's to settle. The Track Delay, Track Enable, Acquisition Hold, Clock Control, FF-1 flip-flops and the counter are now conditioned to start counting.

The 'down' output from (1) goes to an inverter (8) which is sent to both the H.F. and M.F. Tone calibrator to enable the tone for transmission. The output (1) also goes to another inverter (9) and is further applied to gates (10) and (11). The second input to gate (11) is

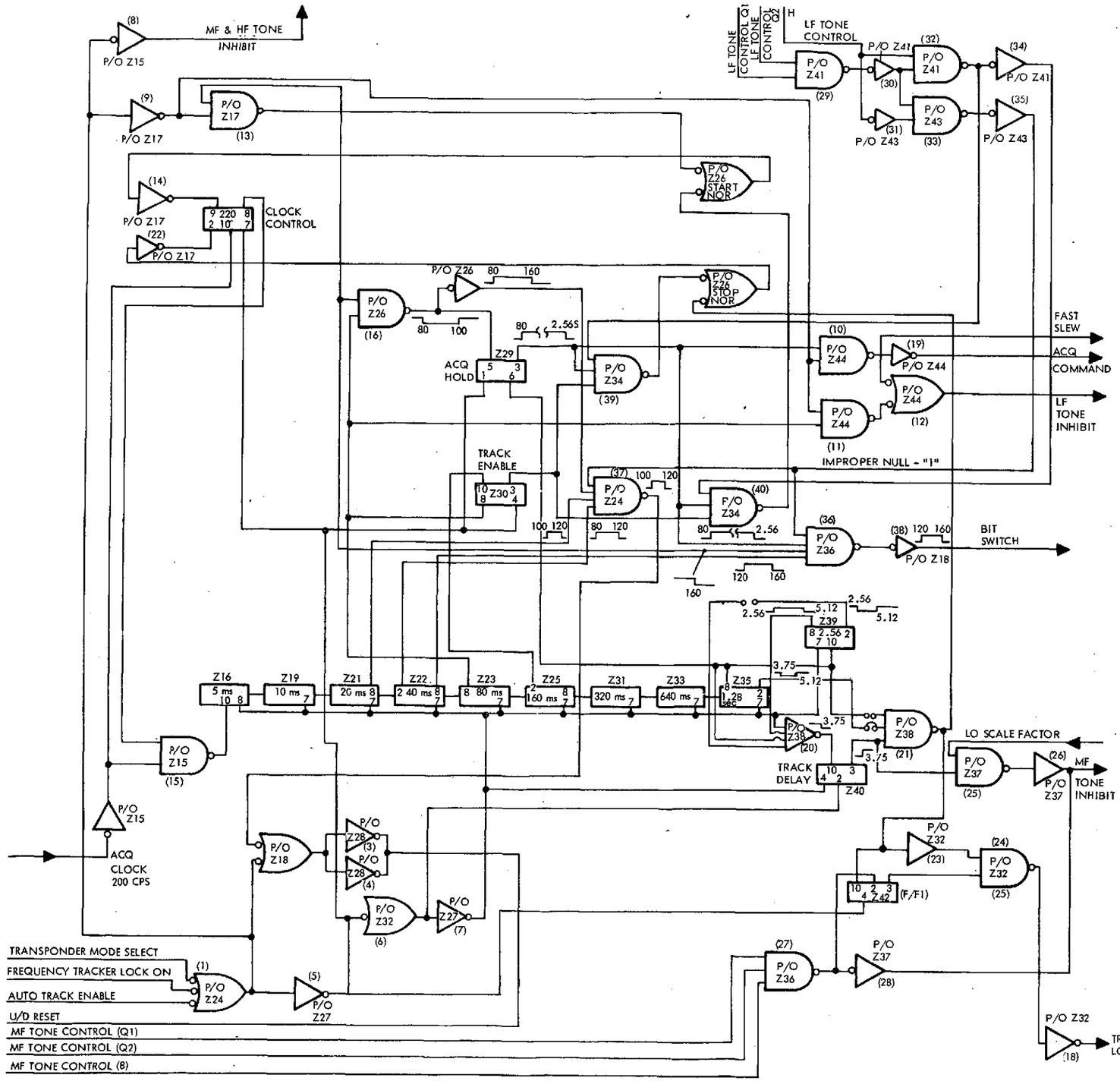


Figure IV-17. Signal Data Converter Control Logic

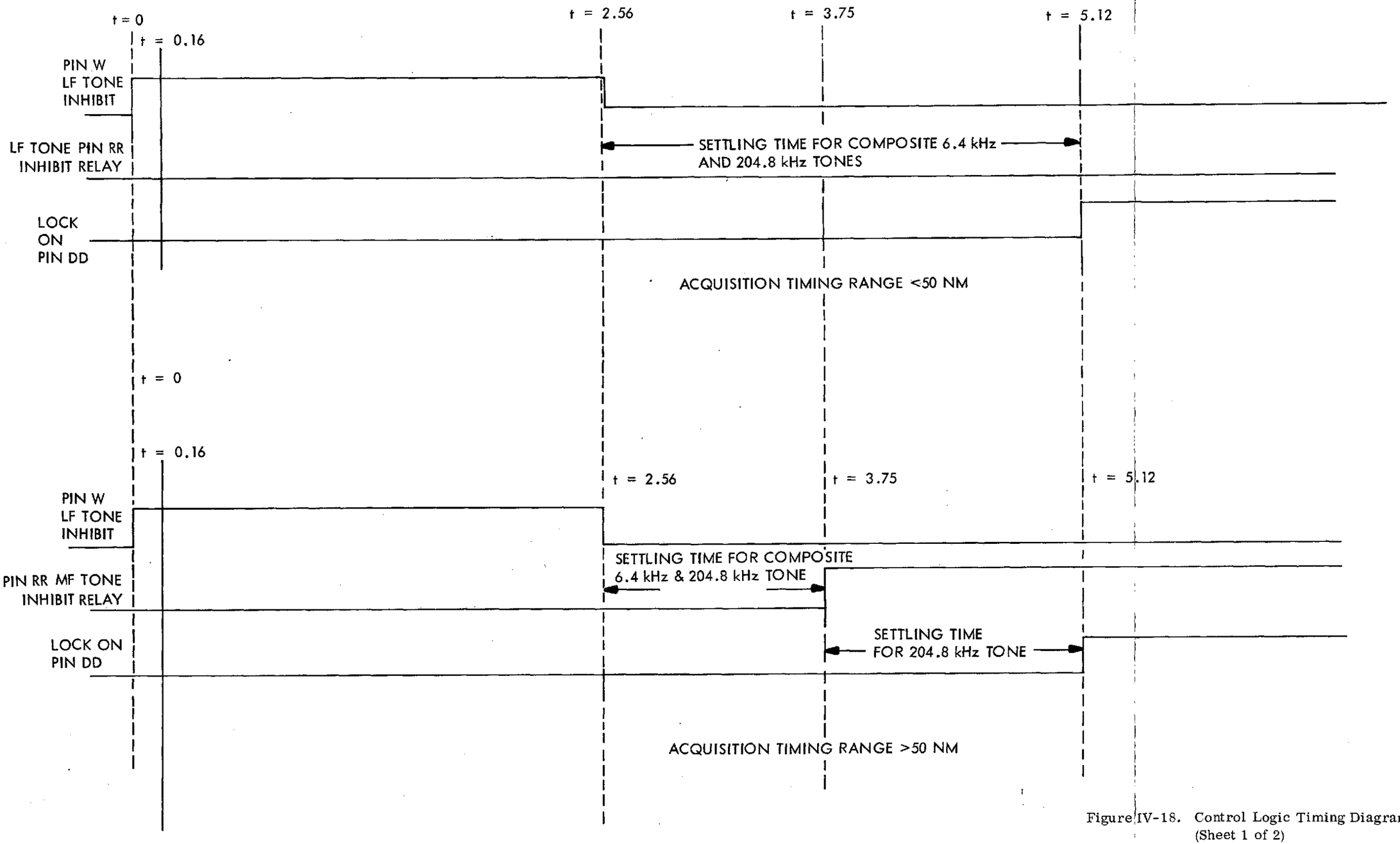


Figure IV-18. Control Logic Timing Diagram
(Sheet 1 of 2)

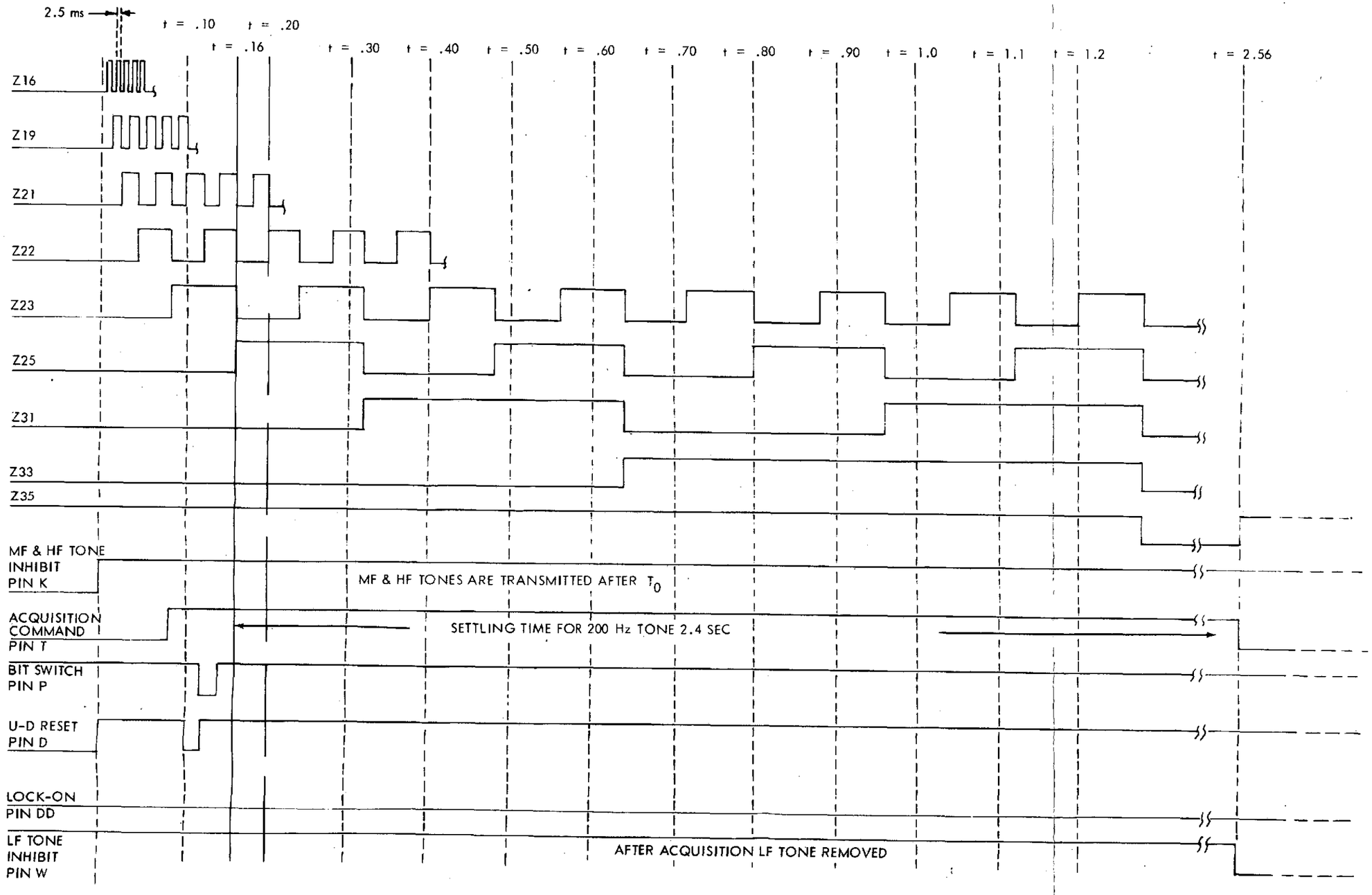


Figure IV-18. Control Logic Timing Diagram (Sheet 2 of 2)

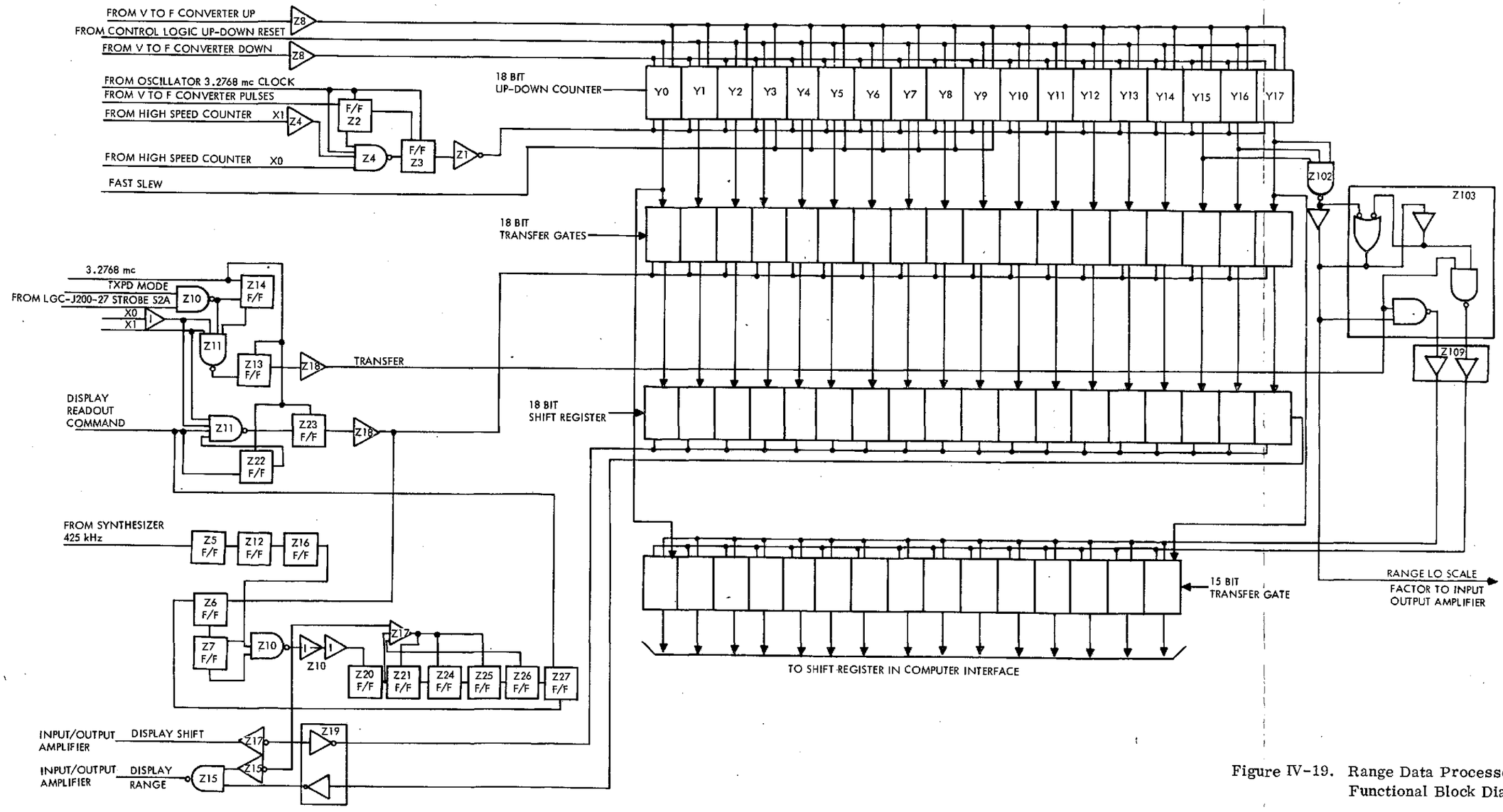


Figure IV-19. Range Data Processor, Functional Block Diagram

one of the outputs of the Track Enable F/F (which has been conditioned) and causes a 'down' output to go to gate (12) and out to the LF Tone Calibrator which enables the LF tone for transmission.

The output of inverter (9) in conjunction with the "conditioned" output of the Track Enable F/F causes the output of gate (13) to be down and its output is applied to Z11, the Start NOR gate. The output of Z11 is inverted by inverter (14) and sent to the Clock Control F/F which causes an 'up' output to be applied to gate (15) whose other input is the Acquisition Clock, 200 cps input. Gate (15) now applies 200 cps pulses to the counter.

The counter now starts counting the 200 cps clock signal for generation of the first set of delays. The control logic is now in a state which will allow the start of Range acquisition, and Range Tracker Lock-on.

The first event, occurring at t = 80 milliseconds, is the setting of the Acquisition Hold flip-flop (Z21). Z21 is set when gate (16) output goes 'down'. The inputs to gate (16) are the "conditioned" output, the Track Enable F/F, and the output of the fifth stage of the counter (80 ms). When the Acquisition Hold F/F sets gate (10) whose other input has already been conditioned) a down output is provided, which causes the fast slew line to the range counter to be enabled. A second output from gate (10) goes out as the Acquisition Command Signal, after being inverted by an inverter (19), and causes the acquisition relays in the Tone Error Selector to be energized. The latter event causes the acquisition relays kHz tone errors to be summed into the feedback amplifier with the proper scaling (16:1) for producing a composite error characteristic. Closure of this relay also inhibits the 204.8 kHz tone error from the feedback amplifier at this time, and causes the amplifier to function as a straight gain device with resistive feedback. The loop now starts to slew toward a null on the composite 200 Hz and 6.4 kHz tone.

During normal operation the fast slew and the tone signals are turned off after 2.56 seconds. This is accomplished as follows: The last stage of the counter provides a 2.56 second signal output to the Acquisition Hold F/F causing the output to age (10) to go 'down' which

opens gate (10) and removes the signal on the Acquisition Command and fast slew lines. Opening gate (10) also removes one input to NOR gate (12) whose other input was removed at 160 ms by the loss of output from the Track Enable F/F. With no signal output from gate (12) the LF tone enable signal disappears. At this time the fast slew signal is removed, the output of the L.F. tone calibrator is inhibited (removing the 200 Hz tone from the transmitter) and the acquisition relay is de-energized. This latter event causes the 204.8 kHz tone error to be mixed with the already present 6.4 kHz tone error in the Feedback Amplifier. The proper mixing ratio (16:1) is again established for forming a composite error characteristic. In addition the 200 Hz tone error is disconnected at this time. When this sequence is completed, the Track Delay flip-flop is set and the first phase of acquisition is complete.

The Track Delay F/F is set at time t = 3.75 seconds by an output from gate (20). The inputs to gate (20) are pre-set times and are wired in the factory to give a setting time of t = 2.56 until t = 3.75 seconds, and an output from t = 3.75 seconds until t = 5.12 seconds.

In order to simplify the following discussion, it will be assumed that t_x is equal to zero. The total time from tome t = 0 before the 200 Hz tone is removes is then 2.56 seconds. After the 200 Hz tone has been removed, either one of two sequences will follow, depending on the target range. The waveforms for these sequences are shown in Figure IV-18.

If after t = 2.56 seconds the target range is above 50 nmi the composite 6.4 kHz and 204.8 kHz tone errors will be allowed a settling time of 2.56 seconds. When this event is completed at t = 5.12 seconds the range tracker will give a locked on indication.

If after t = 2.56 seconds the target range is below 50 nmi, the composite error is allowed 1.28 seconds to settle. After this time the 6.4 kHz tone phase detector will be disconnected from the tracking loop leaving only the 204.8 kHz tone error in the loop. In addition, the tracking loop gain will be rescaled in order to maintain the same loop gain as obtained during composite tracking.

A shorter settling time is permissible for the composite 6.4 kHz and 204.8 kHz tone error below 50 nmi, due to the lower noise bias values at this range. This results in a corresponding decrease in the probability of an ambiguous acquisition. After removal of the 6.4 kHz tone error, an additional settling time of 1.28 seconds is allowed for the 204.8 kHz tone error before the Range Tracker On-Target signal is sent out. This additional settling time is required below 50 nmi. Where small range bias errors on the 204.8 kHz tone might prove significant especially for ranges below 1 nmi.

In either case a tracker Lock-on signal is developed at 5.12 seconds as follows: Gate (21) provides an output at 5.12 seconds because both of its inputs go 'up' at that time. The output is applied to the stop NOR gate (Z26) whose output causes the Clock Control F/F to change state which removes its output going to gate (15) and stops the clock pulses from entering the counter. The output of gate (21) also goes to inverter (23) and F/F1, which causes F/F1 to change state and its output and the output of inverter (23) are applied to gate (24). Both inputs to gate (24) being 'up', cause its output to be low, which is sent to inverter (18), and results in Range Tracker Lock-on indication.

Gate (25) is used to turn off the MF tone when range is less than 50 nmi. The output of the Track Delay F/F (at 3.75 seconds) is applied as one input to gate (25). The second input is called "Low Range Scale Factor" and comes from the Range Counter. If both inputs are 'up' then the MF tone will be removed. Gate (27) is provided as a "Fail Safe" device by monitoring the MF tone (which is used in both Acquisition and Tracking).

Precautions have been taken to assure that a lock-on signal will occur even if operating at or near null but 180° out of phase and that, if required, the counting cycle is momentarily interrupted (at t = 0.16 seconds) to allow the 200 cps error to cross into the 30° threshold limit.

After t = 80 ms and during the next 80 ms (t = 80 ms through t = 160 ms), an operation takes place which deals with the problem of ensuring rapid acquisition, in the event the initial 200 Hz tone error happens to be at or near null, but with an incorrect error slope. This is

accomplished as follows: The Q_1, Q_2 and I control signals coming from the LF Threshold Detector are gated through gate (29), inverters (30) and (31) and (31) and gates (32) and (33). The 'down' output of gate (33) is inverted by inverter (35) and goes to gates (36) and (37) as an improper null signal. Gate (36) has as its other inputs, the output of the Acquisition Hold F/F which is now 'up'; the output of the Track Enable F/F which is 'up'; and the output of the fourth stage of the counter which is also "up" at this time. All 'up' inputs to gate (36) result in a 'down' output which is inverted by inverter (38) and goes out as an 'up' signal on the Bit Switch line. This signal causes the UP/DOWN counter to be shifted 100 nmi towards the target, thus removing the loop from the incorrect null point. Before the injection of the Bit Switch signal the UP/DOWN counter is reset (between t = 100 ms and t = 120 ms). This is necessary to prevent the UP/DOWN counter from moving in the wrong direction before the occurrence of the Bit Switch. Resetting is done by gate (37) whose inputs are improper null signal; an inverted output of gate (16); and an output from the third and the fourth stage of the counter. When all inputs to gate (37) are 'up', its output is down and is fed to gate (2), then through inverters (3) and (4), and is sent out as UP/DOWN reset.

At t = 160 ms an output from the sixth stage of the counter is applied to the Track Enable F/F, whose 'up' output is sent to gates (39) and (40). Both gates (39) and (40) have a second input which is an "up" from the Acquisition Hold F/F. The third or controlling input to gate (39) comes from gate (32) which will be 'up' if not within the 30 degrees threshold limit. The output of gate (39) is coupled to Z11 which stops the counter by resetting the Clock Control F/F.

When the 200 cps error crosses into the 30 degrees threshold "window", with the proper error slope, the output of gate (32) goes from 'up' to 'down', is then inverted by inverter (34) and then applied as an "up" control signal to gate (40). The output of gate (40) is now a 'down' signal which is applied to Z26 start NOR Gate. The NOR gate output is applied to an inverter whose output sets the Clock Control F/F and causes the continuation of the counting cycle. In the event the error signal is already within the "window" zone of the acquisition threshold detector, the clock control does not reset ($t_x = 0$) and counting continues uninhibited. In either case, the counter will then operate until a total time delay, referenced from time zero of 5.12 seconds, plus t_x has accumulated.

1.2.6.2 Computer Interface

The Range Data Processor processes the Transponder mode range data into the correct format for the LGC.* Other functions include generation of an 18 bit serial binary number for display purposes and to provide a range counter state for the three tone range tracker. The schematic diagram is shown in Figure IV-19.

The output of the three tone range tracker is an 18 bit binary number accumulated in the up-down counter. The state of the counter is continuously updated; therefore at any instant, the binary number present in the counter represents the measured radar range. Data is transferred in parallel out of the up-down counter to a 18 bit shift register. Transfer pulses are applied via the timing circuitry. Transfer logic assures that transfer takes place during the quiescent state of the counter, which exists between range up dating pulses. Thus inhibiting of the range tracker during readout is eliminated. After transfer the display shift register is read out by 18 pulses which are generated in the timing circuits. The read-out command however originates in the display assembly. The range request from the Computer interface, transfers the range binary number to a 15 bit shift register. Since the computer register has a capacity of 15 bits, the most significant 15 or least significant 15 bits are transferred from the up-down counter. A scale factor logic signal is applied to the LGC to indicate high or low scale factor. The three most significant stages of the up-down counter are monitored. When any of these stages is a binary "1", a high scale factor indicator is sent to the LGC and the 15 most significant bits (4-18) are transferred, upon request, to the output shift register. When the last three stages are all binary "0", a low scale factor indication is sent to LGC and the 15 least significant stages (1-15) are transferred. The timing circuit takes advantage of the fact that the range counter can only be updated in range data on a specific combination of X0 and X1 (the first two bits of the reference counter). Knowing when the range counter is being updated, can permit the transfer of data from the range counter to the displays.

*The term LGC, LM guidance computer, was the interrogation source in the original system. For lack of a new term for the interrogation source, this name has been retained.

Included in the timing circuitry is a counter which generates the 18 bit shift pulses needed to shift the display data to the display assembly. 425 kc is counted down by three flip flops to a 53 kc rate which will count 18 pulses of the 53 kc and then shut off. The counting of the 18 pulses is accomplished by starting the count on the trailing edge of the first pulse and using this to feed to a F/F delay network. The double inversion needed for driving purposes in the F/F network will count exactly 18 pulses and then an output from the last flip flop will inhibit the input to the counting network. The transfer pulses are inverted and used to shift the range number out of the register. The shift pulses are also used to prepare a gate which will pass the range number to the displays.

1.2.6.3 Input/Output Timing

The Input/Output Timing Unit shown in Figure IV-20 accepts binary outputs from the Range Tracker and range rate doppler frequency. The range rate frequency goes from 114.74 kc for a maximum opening rate of 4900 fps to 310.25 kc which represents a closing velocity of 4900 fps. The function of the unit is to transform radar outputs into computer language. The LGC requests the data by applying a 3.2 kc strobe pulse to the unit. One pulse train (strobe) referred to as S-1, is supplied continuously as a train of reset pulses. The second pulse train, S2, consists of a burst of pulses to "read" the RR data. The duration of this burst is 80 milliseconds for range and range rate. After the range and range rate has been transformed to digital information, the LGC "reads out" this data by means of a burst of fifteen 3.2 kc interrogate pulses. When the computer requests range data from the radar the Range Gate Strobe S2B is applied to T3 then through two inverters (to insure enough drive and impedance matching) to a F/F which has the reset strobe S1 applied as a clock frequency. This F/F drives another F/F whose output is fed to a NAND gate along with the output of the first F/F. The output of the NAND gate is applied to a NOR gate whose other input is Range Rate Gate Strobe (which is not present at this time). The NOR Gate output is inverted and applied to counter. The output of the F/F circuitry is also applied to another NOR Gate which will generate the transfer pulse following the termination of the 100 millisecond data strobe interval. The transfer pulse is generated by dividing two stages of a three stage timing counter. After transfer of data from the binary counter to the shift register the binary counter is cleared by a pulse generated in the timing counter.

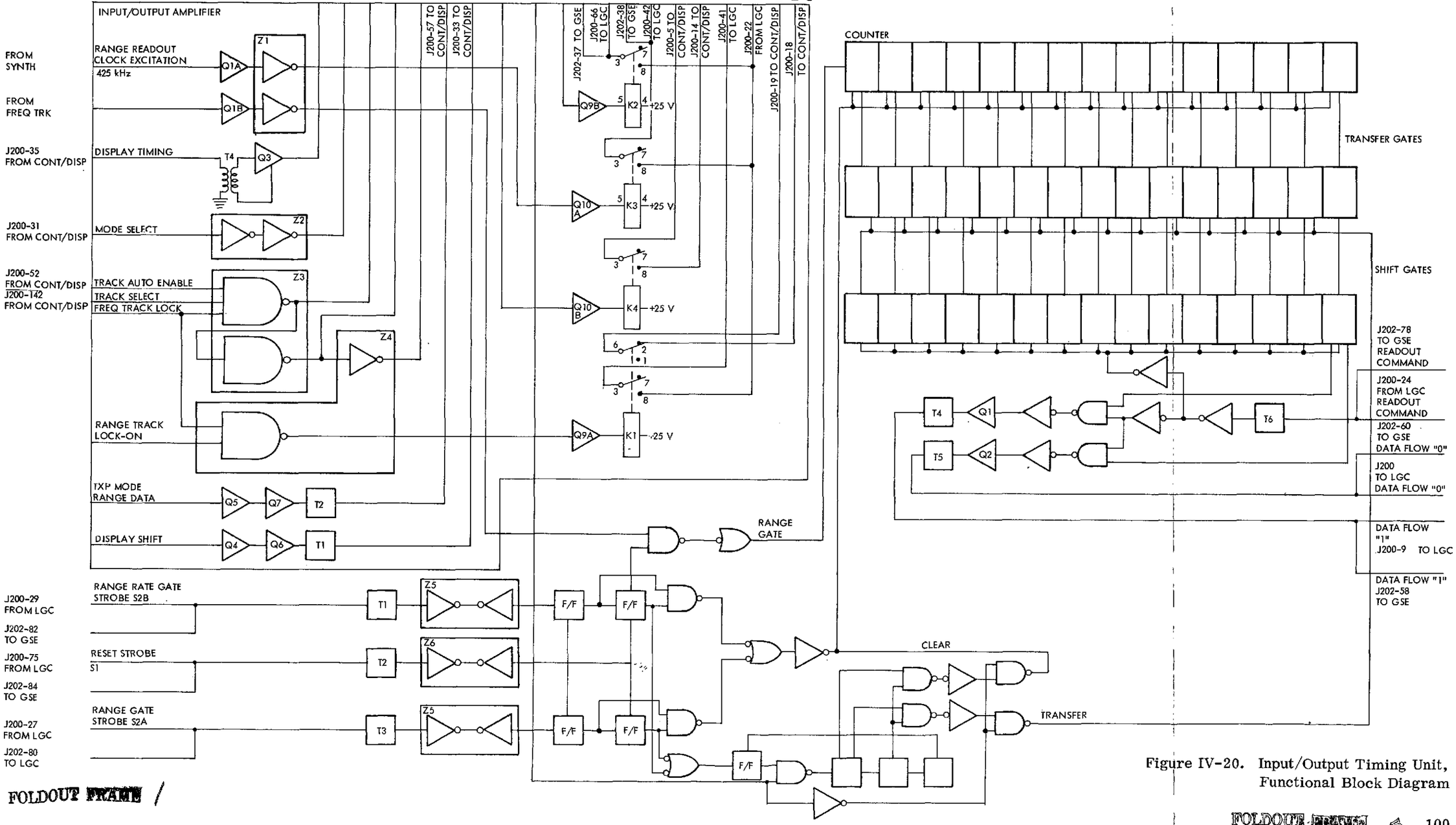


Figure IV-20. Input/Output Timing Unit, Functional Block Diagram

FOLDOUT FRAME /

FOLDOUT FRAME

When range rate is requested by the LGC, strobe pulses (S2B) are applied through T1, (double inverted for drive and impedance matching) into a F/F which in turn drives another F/F. The output of both F/F are applied to a NAND gate and then fed to a NOR gate whose other input is Range Strobe (which is not present at this time). This pulse is then applied to the range counter. Also applied to the counter is the range rate information. This information is applied through a NOR gate being fed by a NAND gate whose inputs are strobe pulse S2B and biased range rate at 212.5 kc rate. The counter data gates are open for 80 milliseconds and this range rate information is read directly into the counter. Since the frequency variation is directly proportional to range rate, no conversion is necessary. Once again after 80 milliseconds a transfer pulse is generated and the information transferred to the shift register. The transfer pulse is generated in the same manner as for range information.

The transfer and clear pulses are generated in the following manner. When the range or range rate strobe has completed 80 millisecond count the data must be transferred to the shift register and be cleared before receiving new data. The transfer and clear pulses are generated in a 3 stage binary counter. The counter receives as a clock a 425 kc pulse from the input/output amplifier. The 3 stage counter is permitted to start at the conclusion of the 100 millisecond data strobe. The first count (01) nothing happens and the time is ended to allow the counter to ripple to a strobe state. On the next count (10) a transfer pulse is decoded and sent to the transfer gates. The next count (11) a clear pulse is decoded and sent to the binary counter clearing the counter awaiting the next strobe pulse. On a count of (100) the counter shuts off. The clear pulse is used to clear the counter to (000). Either strobe pulse will initiate the above sequences.

After the range, or range rate data has been read into the shift register, it is shifted left to right under control of a 15 pulse burst of 3.2 kc with a pulse duration of 3 ± 0.5 msec. For each clock pulse the binary information is shifted one place to the right. After 15 clock pulses, all stages of the shift register are in the Zero state. The information is shifted out on data flow "0" and data flow "1" lines via transistor drivers Q1, and Q2 and output transformer T4 and T5.

The other portion of the computer interface is the Input/Output Amplifier. This unit processes display signals between the Control panel and the Rendezvous Radar, transforms logic signals to discrete signals for LGC, and accepts switched inputs from the control panel and LGC which perform mode switching among the Rendezvous Radar subassemblies.

The discrete circuitry is made up of Q9A, Q9B, Q10A and Q10B along with relays K1-K4. When any of the discretes are a logic "1" the transistor is turned on and a 28v discrete is supplied to the LGC. Relay K2, K3, K4 use only one set of contacts while Relay K1 uses two. K1 is energized when the Frequency Tracker and Range Tracker are locked on. Before lock on, or if either tracker loses lock on, normally closed contacts of K1 will send a data no good signal to the display and to telemetry. Once lock has occurred K1 is energized, the data no good signal is removed, and a data good discrete is now sent to the LGC.

The Input/Output Amplifier accepts the 425 kc clock excitation and the biased range rate at 212.5 kc and transforms the sine waves into square waves. These signals are accepted by Q1A and Q1B respectively. Both transistors are in the "off" state and saturate when the inputs go positive. Z1 contains dual drivers which improve the rise time of the square wave inputs and provide buffering to the various circuits where these signals are read. The Display timing signal is applied through T4 to Q3 which operates in a switching mode, providing the drive to the display processing circuits. Range display shift pulses are applied to Q4 which normally conducts and keeps Q6 in the off condition. When a pulse is applied to Q4 the base goes negative and it turns off causing Q6 to turn on (for the duration of the pulse). The output of Q6 is coupled to the Display Assembly via transformer T1. The range data is sent out in an identical fashion.

The mode logic section Z2, Z3 and Z4 provides switching among various Rendezvous Radar subassemblies. The circuits accept logic levels from the Control Assembly, LGC, and the Rendezvous Radar. Depending on the state of the inputs, the mode logic generates command signals to initiate Data Good, angle track to Antenna Servo Amplifier, three tone range tracking, and slew signal for the antenna servo voting amplifiers.

The inputs from the Control Assembly originate from three interconnected switches which supply "1" or "0" logic levels. The signals from the Computer and Radar are identical levels, however, they originate from logic circuitry rather than switches. The Radar On/Auto switch will determine the switched position of the mode logic by mechanical coupling. Mode select input commands the radar operating mode. The signal is a "1" when the Manual/LGC switch is in LGC position and transponder mode is selected after double inversion, it is applied to the range tracker indicating transponder mode has been selected. The track select signal also selects radar operating modes, the track select signal is a "1", to enable auto angle tracking. The auto track enable signal will be a "1" when in LGC mode of the auto track position. The logic level from the Range Tracker and Frequency Tracker are a "1" when lock on is accomplished. The slew mode select output of Z3 to the antenna servo is a "0". The output of Z3 is inverted by Z3 is a "1" to the antenna servo as gyro torque Gain Control. The other output from Z3 is inverted by Z4 and is a " 0" and is called Auto Track Command to the Servo.

The inputs to the logic gate of Z4 are "Frequency Tracker Lock On" and "Range Tracker Lock On." Both "1's" (if locked on) are inverted and a "0" is fed to Q9A to energize K1 to give a data good indication.

Any "0" on the logic gate will make the output go to the "1" state and cause a failure indication.

1.2.7 Antenna Control Amplifier Subassembly

1.2.7.1 Servo Control

The servo control section receives positive or negative d-c error signals from the Radar Receiver and combines this information with the gyro stabilization information to develop a resultant tracking direction and rate signal for both the X and Y axes of the antenna. The gyro stabilization loops prevent vehicle body motions from affecting antenna position so that target tracking accuracy of the radar antenna is maintained. Figure IV-21 is a functional block diagram of the subassembly.

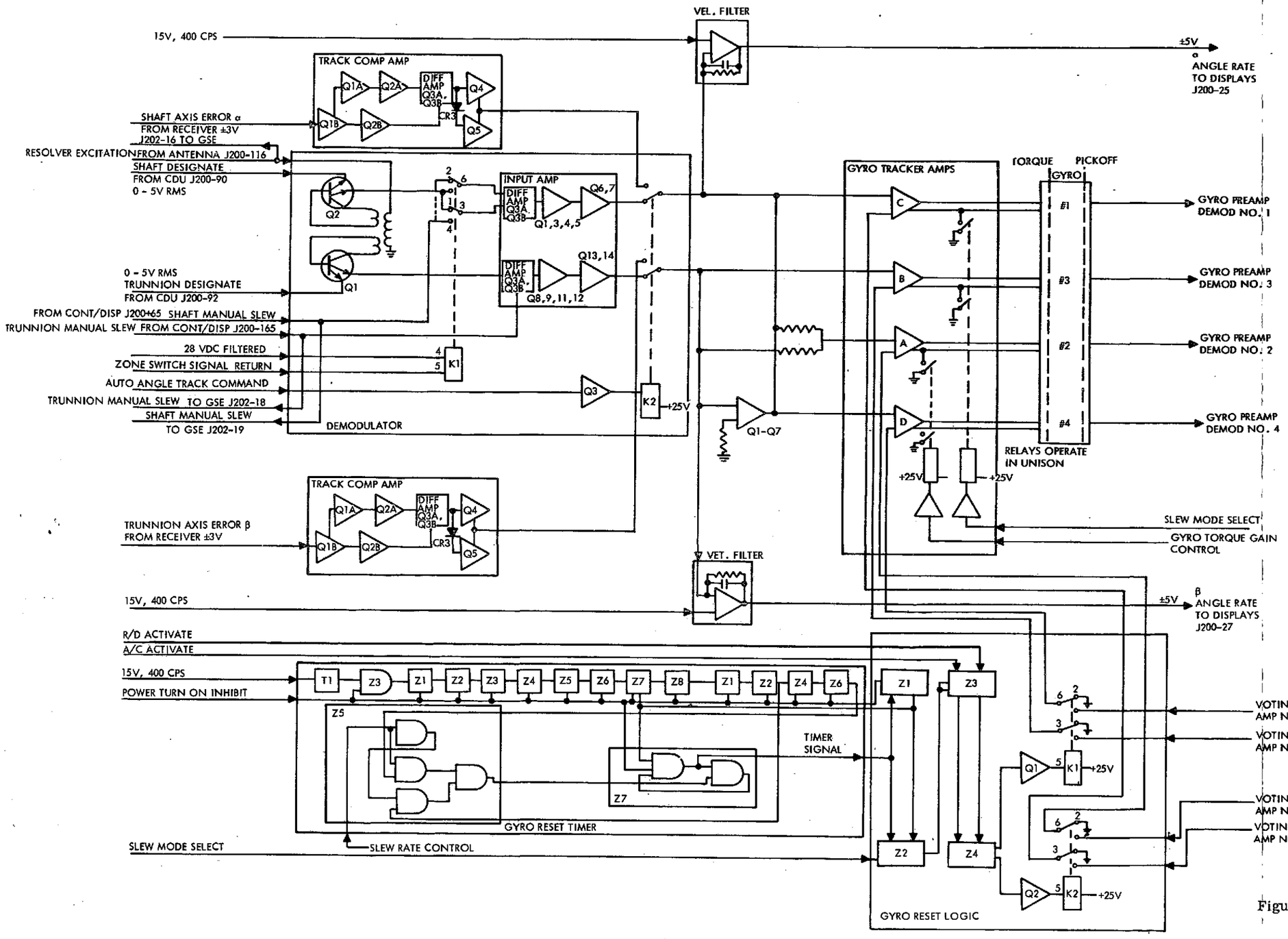


Figure IV-21. Servo Control, Functional Block Diagram (Sheet 1 of 3)

FOLDOUT FRAME 1

FOLDOUT FRAME 2

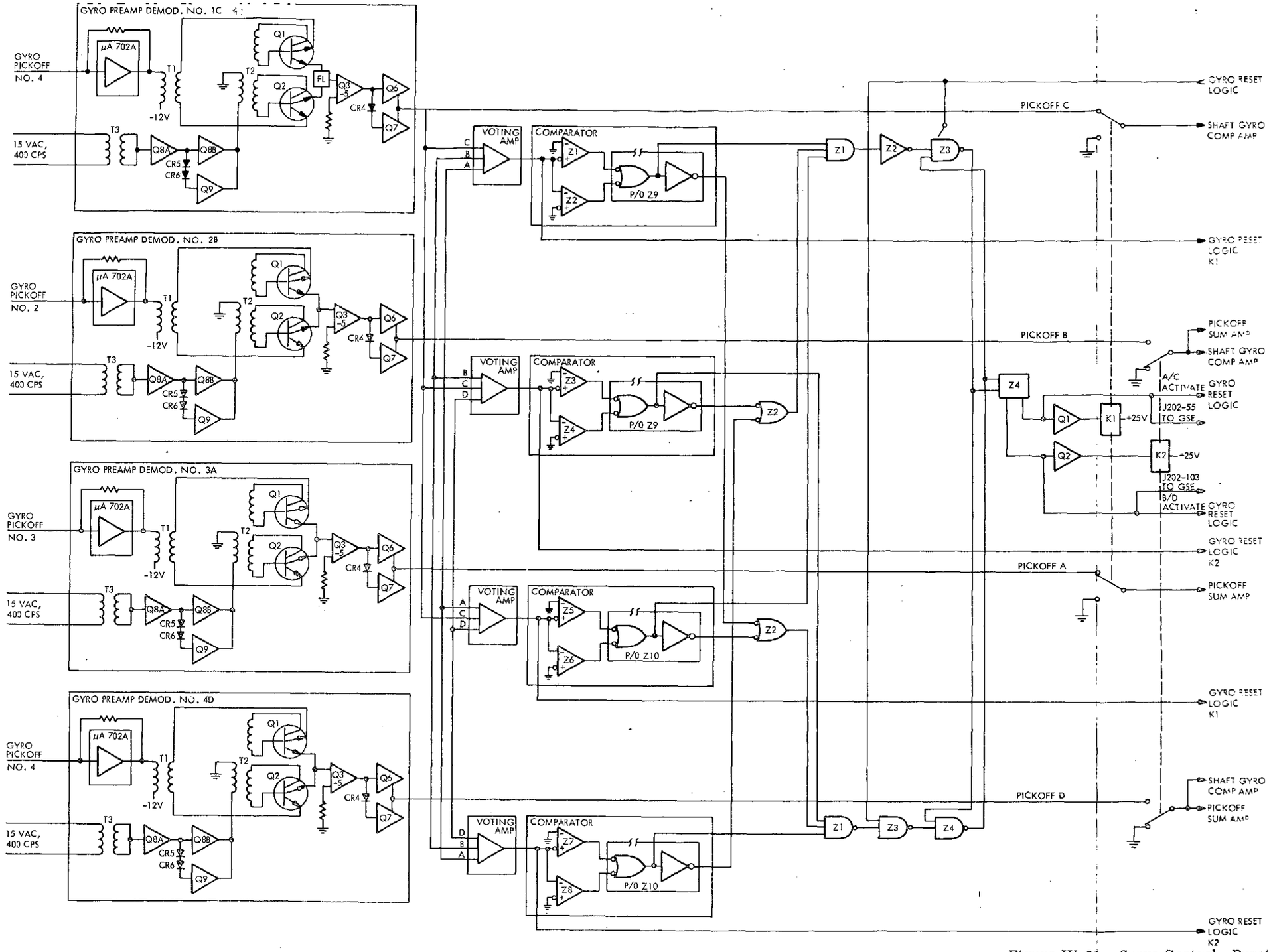


Figure IV-21. Servo Control, Functional Block Diagram (Sheet 2 of 3)

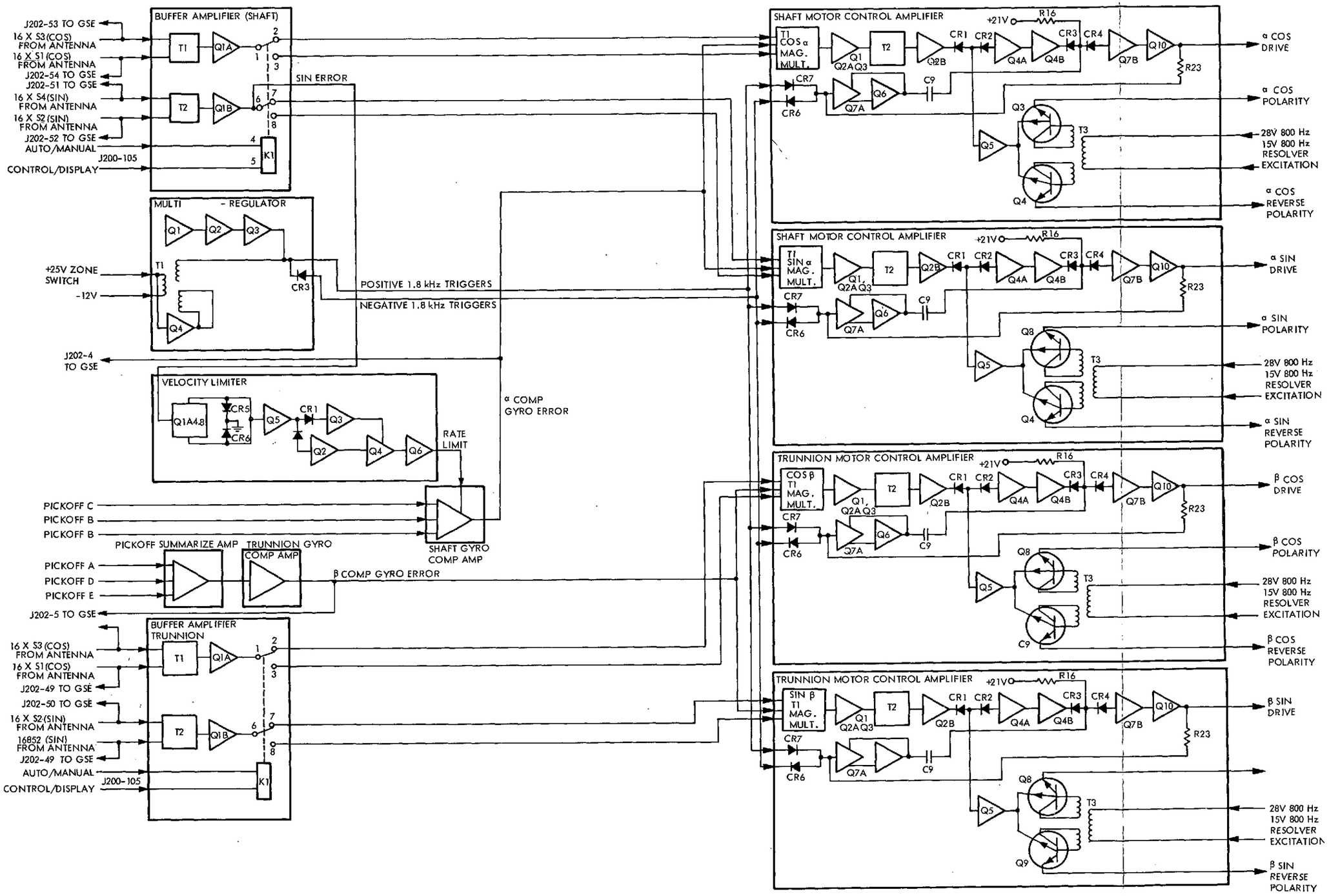


Figure IV-21. Servo Control, Functional Block Diagram (Sheet 3 of 3)

During the following discussion the shaft (Y) axis will be described. Since the trunnion (X) axis circuitry is essentially the same as the shaft axis, the discussion also serves to explain its operation.

The Y error signal is applied to the input of the track compensation amplifier. The track compensation amplifier in common with other amplifier circuits in the servo control section, uses a standard d-c operational amplifier. The input and feedback networks for the d-c operational amplifier are selected to provide for the proper gain and bandwidth characteristics for each amplifier circuit. The d-c gain of the track compensation amplifier is approximately 100. A gain control at the amplifier output adjusts the amplitude of the compensated error signal applied to the torque driver amplifier input.

The velocity filter receives the compensated d-c error voltage from the track compensation amplifier. This error voltage represents the line of sight tracking direction and rate of the radar antenna. Two velocity filters are used, one for each axis. The velocity filter is a d-c amplifier with a response characteristic that will suppress noise voltage and system transients. As a result, the rate voltage supplied to the angle rate display will describe the true physical movement of the antenna.

The torque driver amplifier drives a current through the torque of gyro No. 1. The positive or negative error signal of varying amplitude that is applied to the input of the torque driver amplifier will cause a torque to be developed within the gyro in a specific direction and of a certain strength. The direction and strength of the torque is determined by the polarity and amplitude of the d-c error voltage. This developed torque will tend to drive the spin axis of the gyro away from its initial reference position.

A cluster of four gyros is used in the antenna. Two gyros, one for each axis, are in use at any one time. Figure IV-22 shows the orientation of the spin axis of each gyro with respect to X, Y, and Z axes of the LM. The two gyros shown parallel to the X and Y axes are the on-axis gyros, whereas the two gyros shown at 45-degree angles to the X and Y axes are the off-axis gyros. In the considered mode of operation, gyro No. 1 (letter designation C)

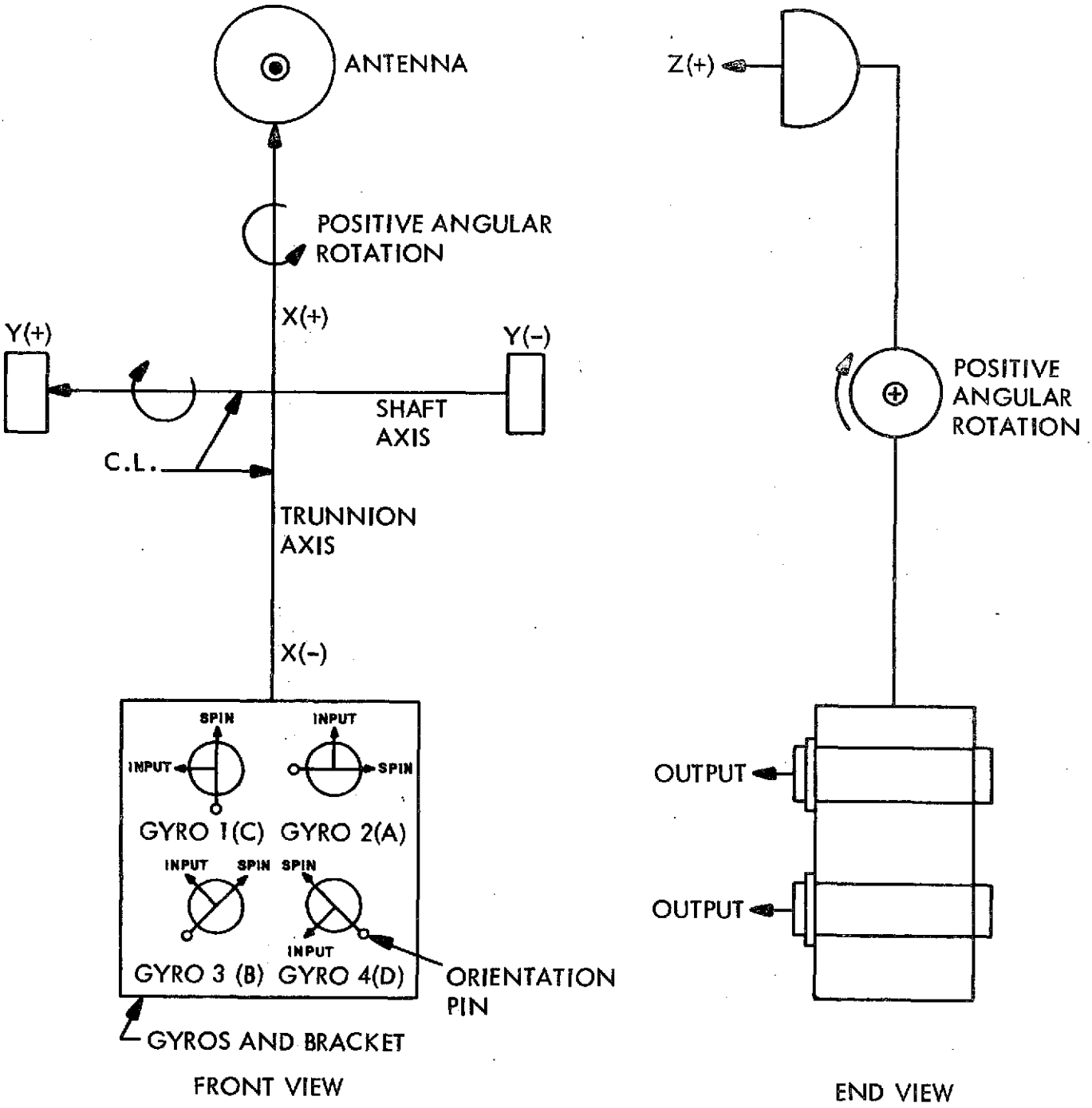


Figure IV-22. GYRO Orientation Relative to LM, X, Y, and Z Axis

controls antenna operation about the Vehicle Y or shaft axis. Gyro No. 2 (letter designation A), the other on-axis gyro, controls antenna operation about the X or trunnion axis.

Initially, the spin of the gyro rotor will establish a reference orientation for control of the Y-axis. The output signal from the pickoff of the gyro unit will be at a minimum or null at this time. Since the pickoff output is electronically amplified to develop a drive signal for the antenna shaft axis motor, the antenna will remain stationary with respect to the established inertial space coordinates. When the spin axis of the gyro is driven away from the spin reference position by the error signal, the output signal of the gyro pickoff will increase and cause the antenna shaft axis motor to rotate the antenna at some constant angular velocity. The gyro rotor responds to this angular velocity by applying a torque to its mounting gimbal in a direction that tends to return the spin axis back in alignment with the spin reference axis. System equilibrium is established when this alignment is reached and the pickoff output signal is at its minimum level. This means that the angular velocity of the antenna with respect to the inertial space coordinates is directly proportional to the torque developed within the gyro torquer by the error signal. An integral of the error signal with respect to time is a direct measure of the angular displacement of the antenna with respect to the inertial space coordinates. For this reason, the gyro control system is a rate integrating type.

Vehicle body motions will also tend to displace the spin axis of the gyro from the spin reference position. The resulting pickoff signal will drive the antenna in a direction opposite to that of the body motion. This causes a torque to be applied to the gyro rotor in a direction that will return the spin axis to the spin reference position. The effect will be to keep the orientation of the antenna constant with respect to the inertial space coordinates. If a torque is applied to the gyro rotor by the gyro torquer, as a result of an error signal (during the time a torque is developed as a result of the Vehicle body movement) the displacement of the gyro rotor and the corresponding pickoff signal will cause antenna movement with respect to the inertial space coordinates proportional only to the error signal. This will occur because the Vehicle body movement is effectively cancelled. The torque developed by the Vehicle body movement may either add to, subtract from, or even equal

the torque developed by the error signal. The amplitude of the pickoff signal and the resulting angular velocity of the antenna with respect to the Vehicle will vary accordingly.

The output of the gyro pickoff is an 400-Hz signal of a certain amplitude and phase. The signal amplitude is determined by the degree of gyro rotor displacement. The signal phase is determined by the direction of gyro rotor displacement, and will be approximately in phase or approximately 180 degrees out of phase with the system 400-Hz reference. The pickoff signal is applied to the pre-amp demodulator. Within the pre-amp demodulator, the pickoff signal is applied to the input emitter of transistor Q1 and Q2 through transformer T1. The 400 Hz reference signal is fed via transformer T3, buffers Q8 and Q9, and transformer T2, to the collector and base of transistors Q1 and Q2. Transistor Q1 receives operating voltages of the proper polarity, every half cycle of the 400 cps reference voltage. If the pickoff input a-c signal is positive (during the conduction time of Q2) a positive half cycle of output voltage is produced. If the pickoff input a-c signal is negative (during the conduction time of Q1) a negative half cycle of output voltage is produced. The 400-Hz component of the positive or negative pulsating d-c output signal is removed by the 400-Hz parallel T filter, and a positive or negative d-c voltage is applied to the input of the d-c amplifier portion of the pre-amp demodulator. The d-c amplifier output voltage (pickoff C) is fed to the voting amplifier.

The voting amplifier weighs this gyro output information and, if the information is judged acceptable, when compared with the output information of the other gyros, an equivalent d-c output signal (shaft error) will appear at the output of the voting amplifier. The shaft error signal is applied to the input of the gyro compensation amplifier.

The voting amplifier also uses the compensated shaft error voltage obtained at the output of the track compensation amplifier to generate torque voltages (torquer B' and torquer D') for application to the torque drivers of the off-axis gyros. These torque voltages will control the off-axis gyros in order to maintain the same relationship between the spin axes of the on-axis gyros (in use) and the off-axis gyros (in standby) during periods of antenna rotation due to target track error voltages. Each torque driver also has a caging input.

The caging input signal is supplied by the voting amplifier as torque drive A, B, C, and D signals. When a gyro is in use, such as gyro No. 1 in this example, no caging input signal is provided by the voting amplifier for that gyro. When a gyro is in standby, such as both off-axis gyros in this example, a caging signal, which is a short duration pulse occuring every ten seconds, will be generated by the voting amplifier for that gyro. The purpose of the caging signal is to correct for possible differences in the drift rate between the gyros in use and the gyros in standby, so that the drift rates are equalized at the start of the next ten-second comparison period. The caging signals for the off-axis gyros are derived from the pickoff B and pickoff D signals supplied to the voting amplifier by the pre-amp demodulators of the off-axis gyros. In the event that the output information from either on-axis gyro channel in use becomes faulty for any reason, i.e., disappears or drifts excessively, antenna control is switched from the on-axis gyros to the off-axis gyros by the voting amplifier. When this happens, the pickoff C signal at the output of the pre-amp demodulator of gyro No. 1 will no longer be used to develop a shaft error signal. The voting amplifier now converts the pickoff C signal to the torque drive C (caging) signal and applies this signal to the caging input of the torque driver for gyro No. 1.

To continue the discussion of the shaft axis servo section under control of gyro No. 1, the shaft error signal at the output of the voting amplifier is applied to the shaft gyro compensation amplifier. The shaft error signal is amplified by the gyro compensation amplifier, the response of which is designed to compensate for the characteristics of the signal at this point. The output voltage of the amplifier is adjustable by a gain control and is fed to the shaft motor control amplifier.

The positive or negative d-c error voltage applied to the input of the shaft motor control amplifier will control the output a-c signal in two ways. First, the amplitude of the a-c output signal is varied in proportion to the amplitude of the input d-c voltage. For a zero voltage input level, the a-c output voltage will also be zero. Second, the phase of the a-c output voltage will be determined by the polarity of the d-c error input voltage, i.e., in phase with the resolver input excitation voltage when the variable amplitude d-c error voltage is positive, and 180 degrees out of phase when the variable amplitude d-c error voltage is negative. The analogue a-c output voltages of the shaft motor control amplifier

which are derived from the sine and cosine outputs of the shaft axis resolver, are supplied to the pulse width modulator. The sine and cosine output voltages of the angle multiplier are 800 cycle sinusoidal voltages which sense rotor angle position. Pulses are formed by the pulse width modulator and the output pulse widths are proportional to the amplitude of the demodulated error voltage input. The variable width pulses are fed to the motor sine and cosine windings through the servo drive amplifier.

The developed motor torque will be proportional to the magnitude of the d-c error signal. If the antenna load torque is constant, then motor speed will be approximately proportional to the d-c error. The direction of motor rotation is reversed when the polarity of the d-c error signal is reversed. While the motor is turning, its excitation is a sinusoidally changing d-c current (equivalent to a-c), the frequency of which is determined by motor speed and the number of motor poles. The rotor of the drive motor is a permanent magnet type containing 16 pole pairs, a number equal to the sinusoidal output voltage variations obtained for one revolution of the 16 speed resolver.

If the motor is stalled at a given location, motor current will be d-c the magnitude and polarity of which is governed by the position of the rotor. An infinite number of current combinations is possible through the sine and cosine windings of the motor.

The amplitude component of the magnetic multiplier output is used to establish a turn off voltage for the pulse width modulator.

The pulse width modulator will generate output pulses only when a positive signal is applied to the input. No output pulses are generated when a negative signal is applied to the input. The width of the generated output pulses is proportional to the value of the positive d-c input voltage.

Normally, the transistors in the multivibrator section of the pulse width modulator are in the following states; transistor Q7B is conducting, and, because the voltage on the base of transistor Q7A is not sufficiently positive, transistors Q7A and Q6 are cut off. With

transistor Q6 cut off, capacitor C9 charges to a value determined by the voltage developed between the base of transistor Q4B and the +21 vdc power supply voltage. The charge path (conventional current) is through capacitor C9, diode CR3 and the emitter-collector of transistor Q4B. Diode CR4 is reverse-biased at this time and capacitor C9 quickly charges to its maximum value.

The astable multivibrator generates a square wave at a frequency of 1.8 kc. The square wave is used to time the operation of the pulse width modulators. The incoming square wave is applied to the base of transistor Q7A through diode CR7. A positive pulse will trigger transistor Q7A and turns transistor Q6 into conduction, thus starting a cycle of operation. One side of capacitor C9 will be effectively grounded through transistor Q6, causing the opposite side of capacitor C9 to become a negative with respect to the voltage at the emitter of transistor Q4B and the voltage at the base of transistor Q7B. Consequently, diode CR3 will be reverse-biased and diode CR4 will be forward-biased. The increased negative voltage now applied to the base of transistor Q7B through diode CR4 will cut off the transistor and cause the output voltage of the multivibrator to rise to a positive value. This positive voltage is coupled back through resistor R23 to maintain transistors Q7A and Q6 in their conducting states. Capacitor C4 will now start to discharge. When the voltage across the capacitor drops sufficiently, transistor Q7B will again conduct. The amount of time required for this to occur and the corresponding output pulse width, is determined by the value of the original charge on capacitor C9. When transistor Q7B conducts, transistors Q7A and Q6 are cut off, returning the multivibrator circuit to the original condition. The cycle of operation is repeated when the following positive pulse is applied to the base of transistor Q7B. The positive output pulses from either pulse width modulator, varying in width from zero to 450 microseconds, are applied to the drive motor amplifier.

The phase component of the output of the shaft motor control amplifier is applied to switch Q5. When a signal is applied, Q5 will conduct and pass the signal to transistors Q8 and Q9. The reference voltage is applied to T3. The secondaries of T3 supply this reference voltage to Q8 and Q9. When the input signal is in phase with the reference signal, Q9 will have a positive dc output while Q8 will have a negative dc output due to the phase reversal of T3.

When the incoming signal is out of phase with the reference, Q8 will have a positive output and Q9 will have a negative dc output. These signals (polarity and reversed polarity) are applied to a multivibrator in the Servo Drive Amplifier and are used to bias the multivibrator.

1.2.7.2 Servo Drive

The servo drive section develops drive power for the shaft axis and trunnion axis drive motors. Direct drive, brushless, torque type motors are used for each axis. Each motor has a sine and cosine drive winding. The proper phasing of the excitation currents through both windings is determined by the sine and cosine output signals of a resolver attached to the motor shaft. The effect is to electrically commutate the drive currents and produce a motor with dc operational characteristics without using brushes. The instantaneous phasing and amplitude of the drive currents, which determine motor speed and direction of rotation is obtained by controlling the phase and amplitude of the original resolver commutation signals. The resolver signals are fed back to the angle multiplier where the product of each sine and cosine resolver signal, and the dc error voltage developed in the servo control section, produces an ac analog output voltage of a specific phase and amplitude.

Figure IV-23 shows a functional block diagram of the Motor Drive amplifier. The inputs are from the Motor Control Amplifier and are pulses for drive, and (+) and (-) dc for polarity signals. Each pulse drive from the pulse width modulator is applied to the multivibrator (Q1A, Q1B) as well as transistor switches Q10 and Q5. The amplifier is divided into two drive channels. One channel is associated with power transistors Q16 and Q20 and the other channel with Q18 and Q19.

Assume that positive pulses are applied to the multivibrator Q1A and Q1B in addition to Q5 and Q10. If the polarity inputs are such as a (+) dc is applied to Q1B collector and a (-) dc is applied to the collector of Q1A, Q1B will pass the positive signal through CR2 to transistor Q2 and turn it on which in turn turns on Q3 and Q19. The absence of an output from Q1A (when Q1B is conducting) lowers the bias on the base of Q7 turning it off. This will

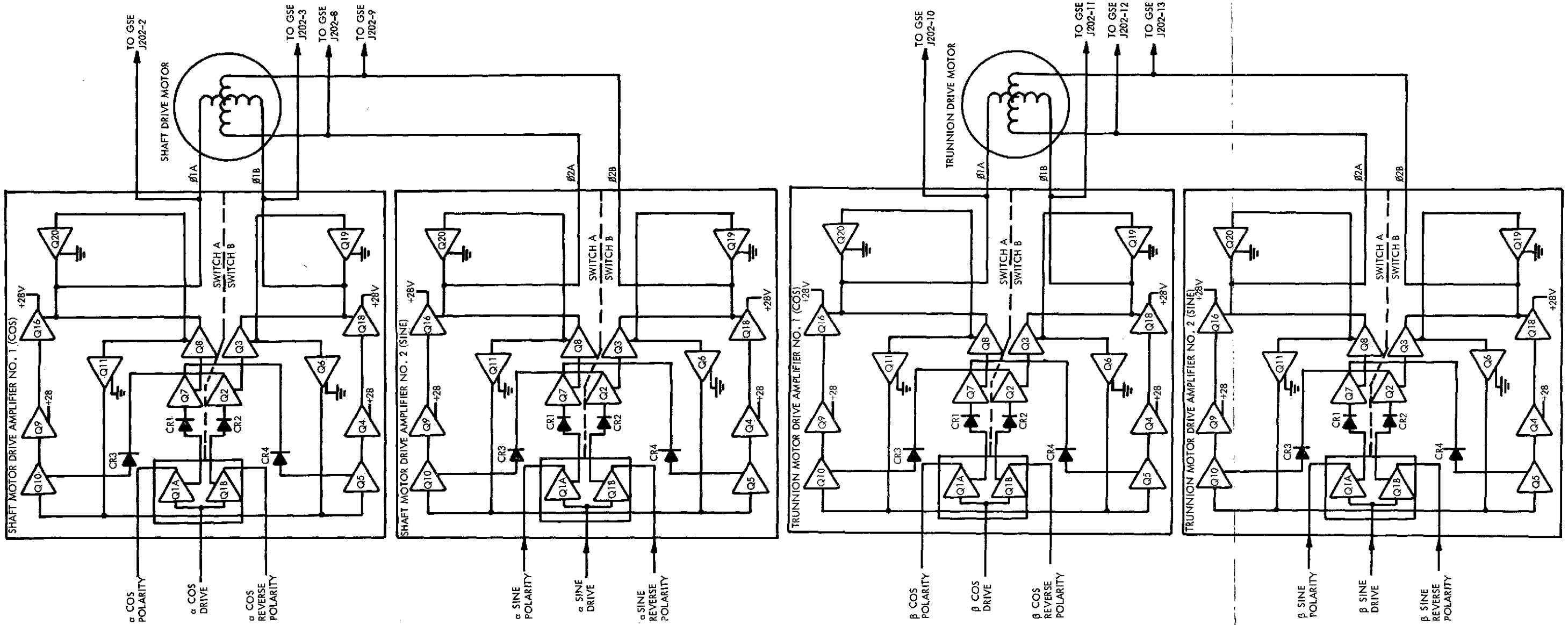


Figure IV-23. Servo Drive, Functional Diagram

in turn shut off Q8 and Q20. The multivibrator is now in a known condition. The next pulse that comes in has no effect on the multivibrator circuitry. The pulses are fed into the collectors of Q11 and Q6. At this time Q6 is turned on by Q3 being turned on, and applies a ground to the base of Q5 turning it off. Turning Q5 off effectively places the base of Q4 at 28 volts turning it off. This in turn turns Q18 off. The same pulse applied to Q11 goes to the base of Q10. Q11 is cut off at this time due to Q4 being cut off. The pulse of Q10 turns it on and this turns on Q9. Q9 turns on Q16 allowing current to flow through the motor winding from ground through Q19, the motor winding, Q16 to +28 volts. The length of time that current flows through the transistor switches is determined by the width of the input pulse from the pulse width modulator. When the pulse is removed, the back EMF of the motor coil inductance tries to maintain the flow of current through the motor coil at previous peak level. The motor inductance now acts as a voltage source and maintains current flow. This limits the amplitude of the surge voltage. Thus a large amount of stored energy is cycled through the motor windings during the periods between pulses. When the polarity input reverses the multivibrator is reset and Q1A passes the positive pulse and turns on Q7 which turns on Q8, Q20, and Q11, while Q18 turns off Q2, Q3, Q19 and Q6. When the next pulse appears the multivibrator remains in this state but now the input drive pulse is applied to Q5 turning it on. This turns on Q4 which turns on Q18. The pulse cannot be applied to Q10 due to Q11 being turned on grounding the input line to the base. Q11 being turned off turns off Q9 which turns off Q16. Conduction for the motor coil winding is now from ground through Q20, the motor coil, Q18, to +28 volts. This now is in the opposite direction. The motor will run in one direction as long as the polarity input to Q1A and Q1B remain the same.

The circuitry of Q5 and CR4 and Q10 and CR8 is used as an interlock to insure that the output of the multivibrator will not change states during a driving cycle of the input pulse. The power switching transistor Q16, Q18, Q19 and Q20 are external to the subassembly. They are mounted on the chassis due to the heat dissipation.

1.2.7.3 Scan Programmer

The scan programmer forces the radar antenna to scan an angular sector of uncertainty of 20° in shaft and 20° in trunnion. The sector location is determined by the antenna pointing angle when the function switch is moved from normal to scan.

Figure IV-24 shows the interconnection of the scan programmer at the RCA test facility.

In the normal position of the function switch, the antenna may be positioned using either the manual slew switch or the designation resolvers. In order to simulate the astronauts control panel, the shaft and trunnion slew signals are disabled in the computer mode. This is accomplished in the STE. No similar switching is present in the designate resolver loop. However, provisions have been made to independently disconnect the resolver error signals. It should be noted that if the slew signals and designate signals are applied simultaneously to the radar, both functions will operate and the antenna will move until the slew and designate signals are equal in amplitude and opposite in sense.

In order to provide greatest flexibility, the scan programmer has bypassed all inhibit signals. Therefore the scan programmer is operable in both the manual and computer modes. Internal switching removes the designate and slew signals during the scan mode.

In the scan mode, a bipolar signal is applied to the radar shaft and trunion slew inputs. The timing of these signals is shown in Figure IV-25. A negative signal is applied to the trunnion slew input. The antenna will then slew to the right. After approximately 2.75 seconds, the polarity is reversed. This will cause the antenna to reverse direction. Simultaneously, a .25 second pulse is applied to the shaft slew input. This causes the antenna to step down. The procedure is continued until the sector search is complete. The scan direction is then reversed and the antenna will repeat the scan.

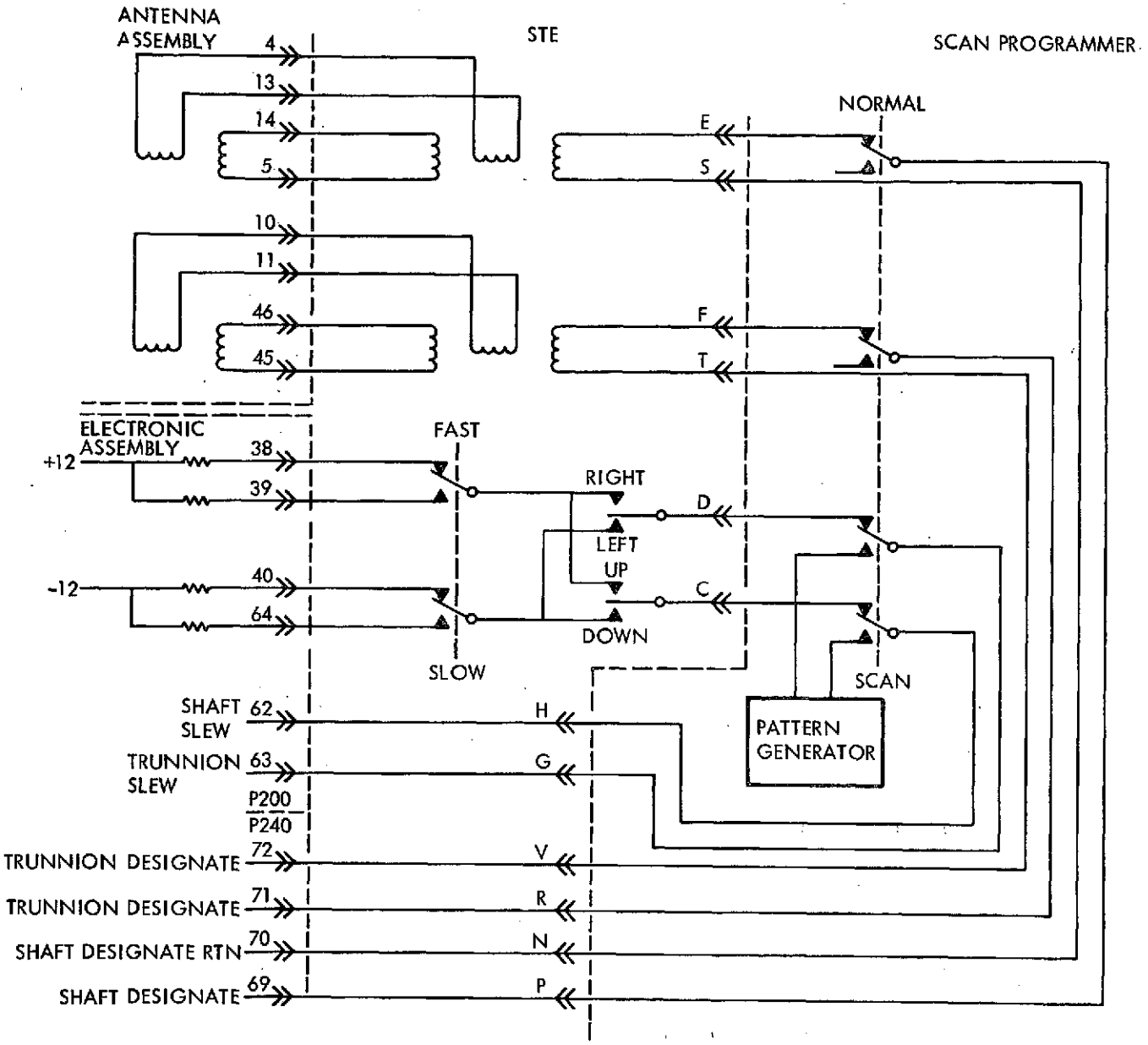


Figure IV-24. Functional Block Diagram - Scan Programmer

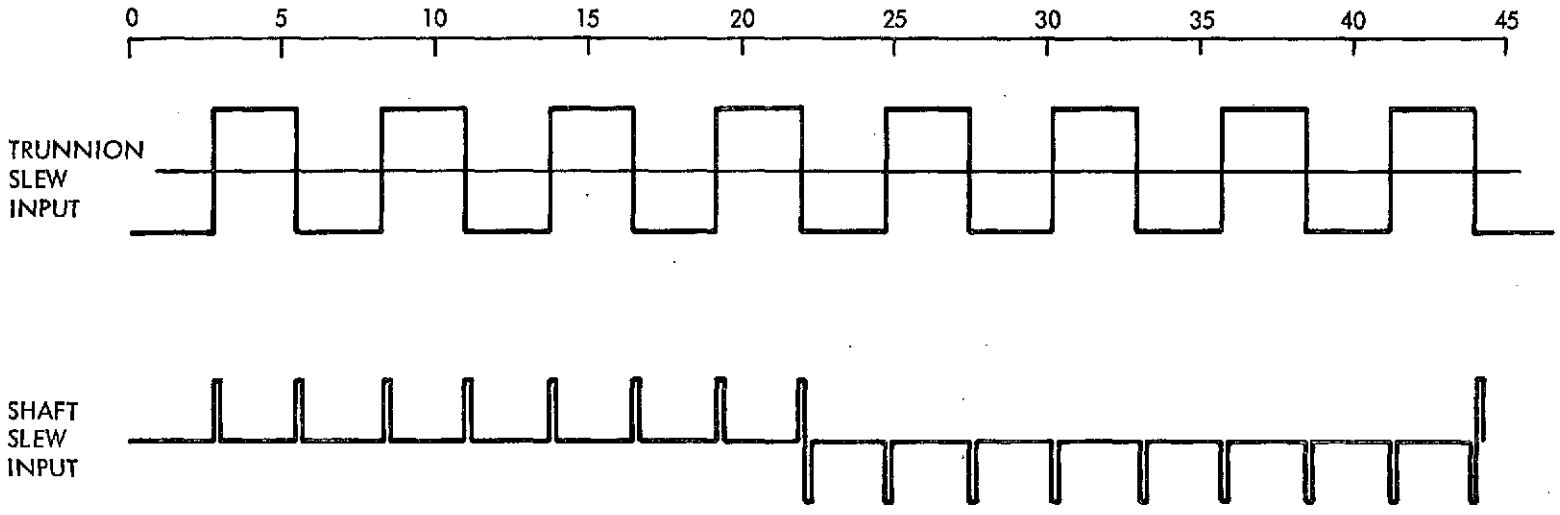


Figure IV-25. Timing Diagram Scan Programmer

The high angular rates applied to the radar servo, and the transients created at reversals by the scan generator, causes frequent switching between the primary and redundant gyros. This switching perturbates the servos and distorts the scan pattern. It is therefore necessary to inhibit voting when the scan generator is in use. The circuit shown in Figure IV-26 will force the selected gyro set on and will inhibit voting. Switch S1 should be a double pole double throw, center off toggle switch.

1.2.8 Power Supply Subassembly

The Power Supply is a switched tap converter type which produces regulated +25 vdc, +12 vdc, -12 vdc, +6 vdc, and 4.3 vdc. The regulated voltages are used throughout the Electronics Assembly, supplied to the Antenna Assembly, and also monitored in the GSE. A functional block diagram of the power supply is shown in Figure IV-27.

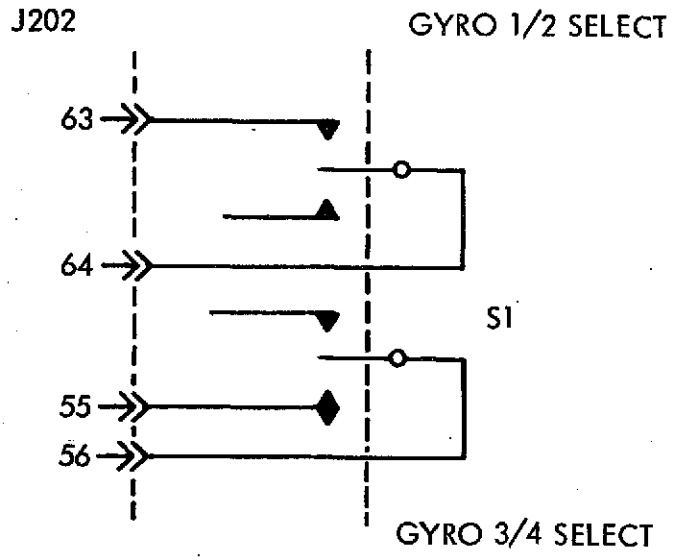


Figure IV-26. Gyro Switching Inhibit Schematic

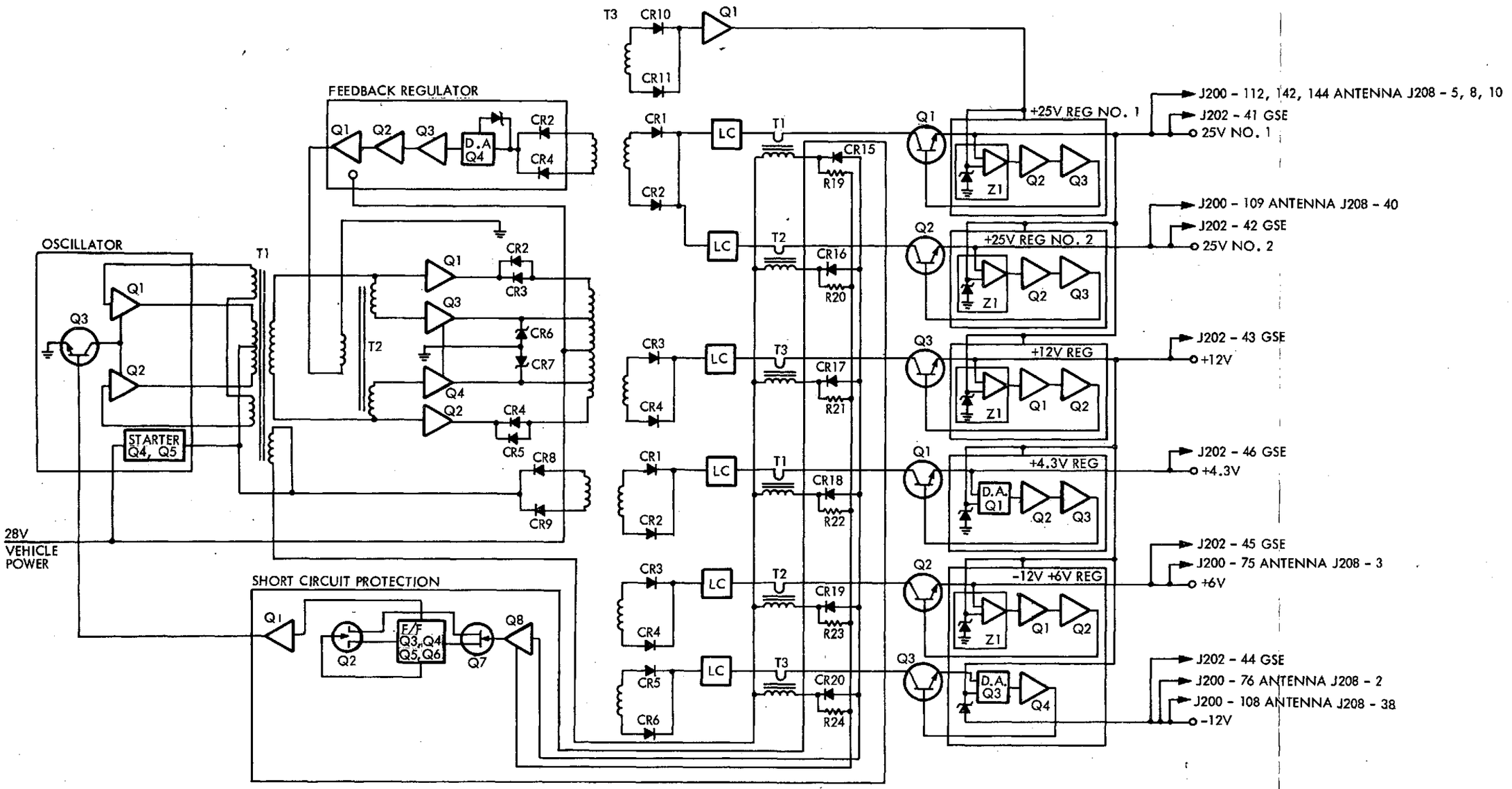


Figure IV-27. Power Supply, Functional Block Diagram

The 28 vdc input, from the battery to the power supply, is fed to a starter circuit, the center tap of the primary of power transformer T3, and to the feedback regulator as an operating voltage. Initially the voltage for the oscillator is applied through the starter circuit to the saturable transformer T1 in the oscillator. This starts the oscillator Q1 and Q2 to operate. The transistors receive their feedback through windings of the transformer T1. The current increases in the transformer until saturation occurs. At this time the current in the secondary decreases and the current in the feedback winding reverses direction, which reverses the bias condition of Q1 and Q2 causing current to flow in the opposite half of T1 primary. The rate of which this occurs is a function of the saturation point of the transformer and the supply voltage.

When the switch tap converter is running normally, the voltage to run the square wave oscillator comes from a regulated supply obtained from a winding on the power transformer T3. However, when the converter is first turned on, this supply is not yet available. As the voltage increases in the power transformer the starter circuit is disabled and full oscillator power is delivered from the power transformer. During normal operation little power is drawn from the starting circuit. The square wave oscillator drives the switch tap converter consisting of transistors Q1, Q2, Q3, Q4. During the positive half of the drive cycle, transistor Q1 is first driven into conduction, grounding one end of the power transformer T3 and converting the supply voltage across half the primary of T3. The voltage induced in any secondary winding of T3 during this period is the supply voltage times the corresponding turns ratio. At some time during the positive half of the drive cycle the controlled saturable reactor T2 saturates. This time is controlled by the amount of feedback regulator. The current increases until the back bias threshold established is exceeded.

Current now flows through T2 causing Q3 to conduct. The inboard tap of power transformer T3 is now grounded and the supply voltage connected between the inboard tap and the center of T3 causes the out board tap to go below ground back biasing the divider CR2 - CR3, cutting off Q1. The voltage induced in any secondary of T3 is now greater because the turns ratio is larger. The voltage on any secondary, therefore has a stepped appearance. Transistors Q2 and Q4 are driven into conduction in an exact fashion during the negative half of the drive cycle. Simultaneous conduction of inboard transistor Q3 and the opposite outboard transistor Q1 is accomplished by delaying (3 sec.) the turn on of the outboard transistor Q1. This delay allows the inboard transistor Q3 to be fully turned off.

The average value of the voltage induced in any secondary winding of T3 is closely regulated by the feedback regulator. This regulation is maintained by comparing a portion of the rectified voltage from a winding of T3 with a zener reference voltage in differential amplifier Q4. The voltage difference is amplified and a feedback current, proportional to the amplified difference, is supplied to the controlled saturable reactor, T2, in the switch tap converter. The feedback current controls the time of transistion between the two induced secondary voltage levels in such a way, that the average value of the voltage induced in the secondary of T3 is held relatively constant.

The step modulated voltage induced in any secondary winding of T3 is rectified, smoothed and filtered by the LC network. Due to the high operating frequency of the converter (20 kHz) the rectifier diodes are high current, first recovery type. The LC product is chosen to maintain the ripple across the capacitors at less than 40 mv rms.

The rectified and filtered voltage is applied to a series regulator which is controlled by a pre-regulator. The pre-regulator compares the output of the series regulator, with a reference established by a zener diode network in the pre-regulator, which in turn causes the series regulator to operate with a low voltage drop across them (1 volt) thus achieving a reasonable efficiency even at relatively high currents.

Short circuit protection is provided by sensing the current at the output of the LC network on each output line. The short circuit protection circuitry consists of a five diode network called a "but of networks," unijunction diodes, a triggerable flip-flop and a oscillator control switch. When a overload is sensed in any output, the current in Q8 increases causing the unijunction Q7 to trigger flip-flops Q3, Q4, A5, and Q6. The flip-flop turns on Q1 which in turn shuts off the oscillator control switch (Q3) located in the oscillator. Q3 now turns off the oscillator, shutting down the power supply.

The flip-flop reset is determined by the firing potential of unijunction transistor Q2. The flip-flop will reset in 350 milliseconds, which is established by an RC network in the unijunction circuitry. The reseting of the flip-flop will cause Q1 to turn off which allows the oscillator control switch Q3 to turn on and the oscillator start to go into oscillation. If this overload has been removed in the time, normal operation will resume, of not, the flip-flop will continually recycle until the short is removed.

1.2.9 Self Test Subassembly

The self test circuitry permits radar testing without the need of a Transponder. The circuits check transmitter power, phase lock at minimum signal level, angle error detection, AGC action, and range and range rate measurements.

The self test circuitry is enabled by supplying a self test enable signal from the Control/ Display Assembly. This signal is +12 volts and is supplied to relay K1. When energized the relay contacts supply the +12 volts and -12 volts to the subassembly.

The three tone signals are applied to phase shifters in the subassembly. The phase shifters contain passive R-C networks with impedance matching emitter followers. The emitter followers keep the total phase shift to within $+1^0$ over the temperature range. The modulating signals are phase shifted before insertion into the phase modulator. The outputs of the phase shifters are supplied to the phase modulator in addition to the other input which is 13.59 mc. This signal is derived from a crystal controlled oscillator. The phase modulator is a common base, tuned collector amplifier using varactor diodes in the resonant circuit.

The modulating voltage or tone input is applied across the varactor diodes. This causes the effective capactance to change as a direct function of the applied modulating signal. As the center frequency varies, the carrier signal (13.59 mc) will encounter a phase shift. Therefore, the phase shift is related to the modulating signal. Each tone input is driven from a low impedance source into a set of varactors. In this manner other tones cannot cross modulate one tone because of the shunting effect of the coil. The three tones are summed directly in the resonant circuit. The output of the modulator is applied to a buffer to build up the carrier to a required level to drive the multiplier circuit. The multiplier is tuned to the third harmonic of the carrier and is supplied as a 40.77 mc carrier with the tone modulation appearing on it to the power divider network. The power divider is an active power splitter because it is necessary to phase shift and attenuate each channel separately. The active power splitter provides adequate separation between channels. The output of the power splitter is supplied to difference channel 0-180 phase shifters. Each difference channel is square wave phase modulated by the phase shifter. Two signal polaraties are obtained from an auto transformer. Each polarity is, in turn, fed to a summing network by the proper switching. A positive voltage is applied to the switching logic input, forward biasing a diode and a positive potential exists at the emitter of the transistor, this cuts off the transistor. When the DC return signal is applied to the switching logic input the transistor is turned ON. This action causes a 0 degree or 180 degree phase shift and is supplied to the antenna assembly along with the signal from the reference channel output.

The outputs of the self test subassembly causes readings from the RR to be as follows:

200 n miles of range, 30 kHz of doppler shift, angle error of 0 degree or 180 degree and the AGC action on the receiver and pre-amplifier on the Antenna Assembly.

1.3 IF MODULATOR

Each single sideband generator within the system requires an IF drive signal, at 50 MHz or 100 MHz, applied to the proper part; upper sideband or lower sideband. The IF modulator, shown in Figure IV-28, provides this signal under control of the PRF generator. A block diagram of the IF modulator is shown in Figure IV-29. The frequency select switch selects either the 50 MHz or 100 MHz oscillator output and applies the unselected source to an internal load. Correspondingly the sideband select switch routes the selected signal to either the upper or lower sideband amplifier. After amplification, the signal is applied to a three way power divider where it is divided equally to each of the sideband generators. The output level is +10 dB m ± 1 dB. When the center frequency is selected by the PRF generator, all selects lines are low. Therefore, both oscillators are loaded and the input of each amplifier is loaded. In this manner, no signals are routed to the sideband generator.

1.4 TRANSMITTER

1.4.1 Cooperative Mode Transmitter

The Frequency Multiplier Chain is an all solid state amplifier and frequency multiplier, composed of transistors, varactors, and matching resonator networks. The unit has a waveguide RF output terminal, two dc pin input terminals, and a miniature coaxial RF input terminal. The Chain supplies microwave transmitter power for the Rendezvous Radar in the cooperative mode. It also supplies local oscillator power for the pre-amp mixers in the Microwave Subassembly in both modes. It receives its input from the wide band amplifier in the Frequency Synthesizer Subassembly at a frequency of 102.425 mc at a nominal power level of 20 to 25 mw. This is applied to a transistor amplifier that increases the power to 16 watts which drives the multiplying part of the chain.

The multiplier part of the chain consists of a quadrupler, tripler, and three doublers. Since the multiplier used is a microwave system, varactors are used as harmonic generators. A varactor operates in the region in which a conventional diode is cut-off, and has a nonlinear relationship between its voltage and capacitance. Thus, distortions occur in the

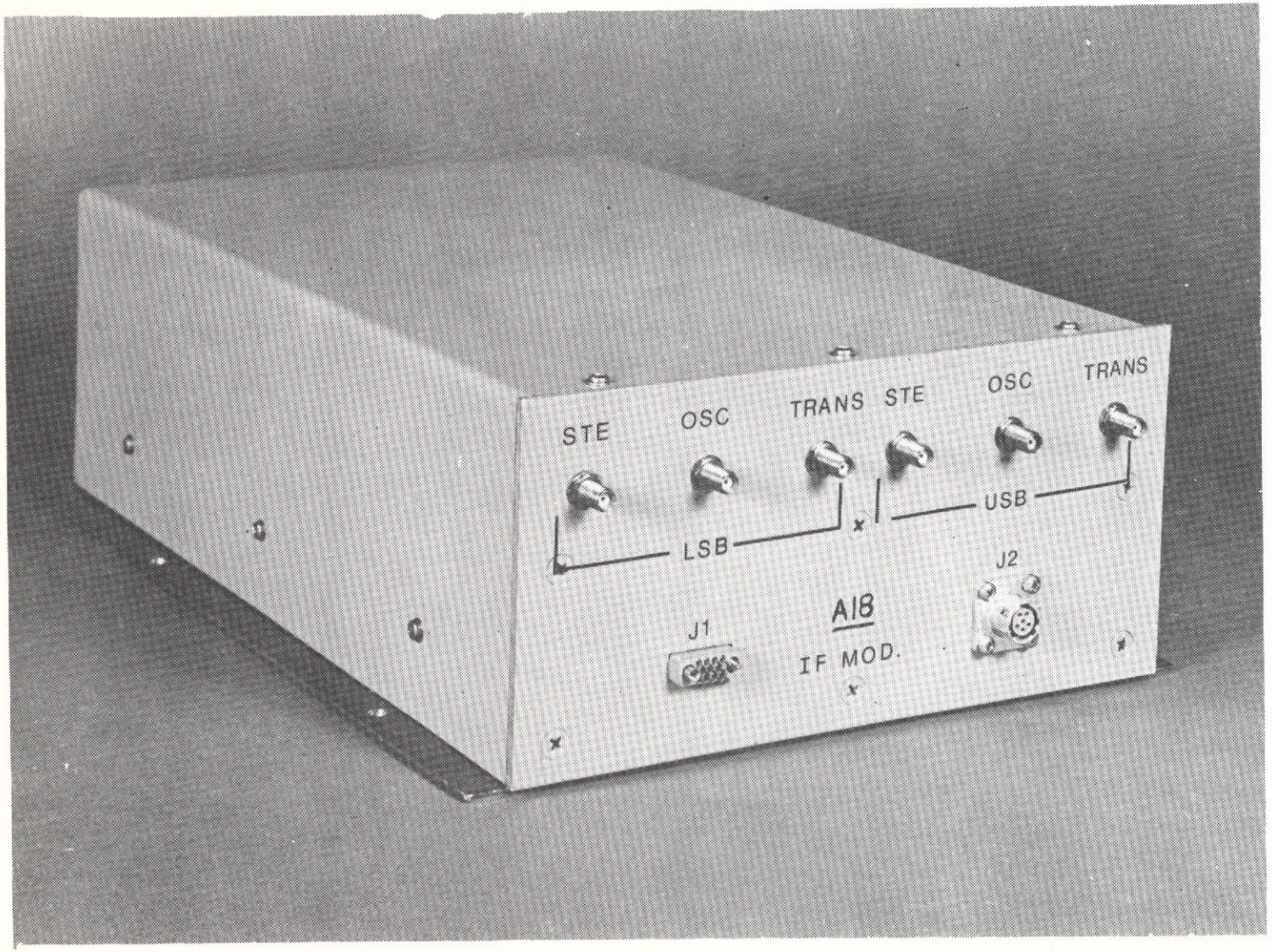


Figure IV-28. IF Modulator

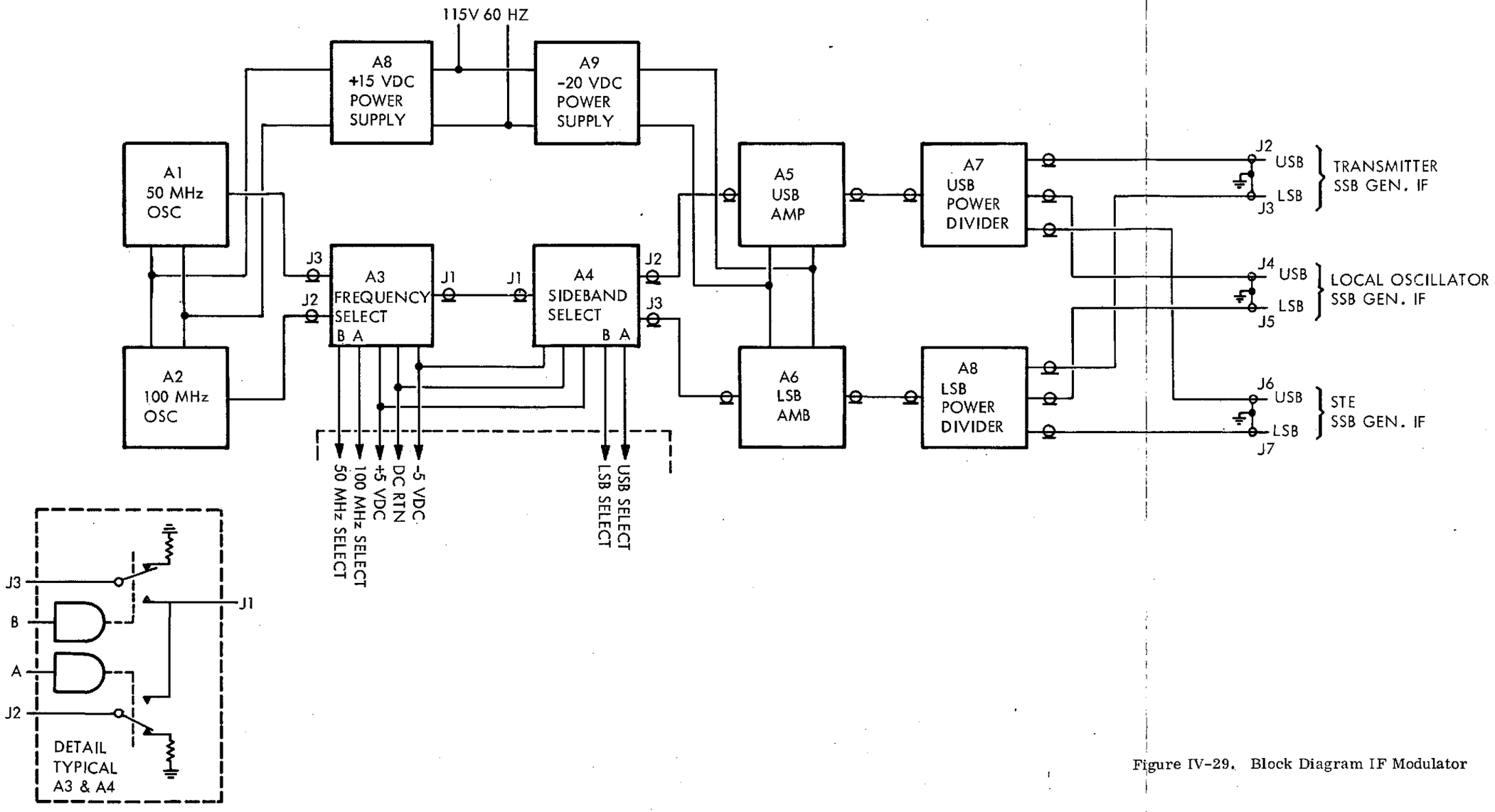


Figure IV-29. Block Diagram IF Modulator

signals applied to a varactor, which encourages the generation of harmonic frequencies. The basic premise of a varactor multiplier is to convert a source signal into a harmonic current, through a load, by means of a varactor. If the output of the multiplier is to be the second harmonic, then the input filter is tuned to the fundamental frequency and the output filter is tuned to the second harmonic. If the output is to be the third or fourth harmonic then the input is tuned to the fundamental frequency and an idler circuit is tuned to the second harmonic. This permits fundamental and second harmonic current flow to mix in the varactor and provide voltage components of the (1) fundamental frequency, (2) second harmonic, (3) fundamental plus second harmonic, and (4) two times the second harmonic, across the varactor. The output filter then is tuned to the desired third harmonic, item (3) above, or to the fourth harmonic, item (4) above. Then the output filter allows only the third or fourth harmonic to pass through to the load.

Combinations of the foregoing are used to provide the described output frequency of 9832.8 mc, from the input frequency of 102.425 mc. The power level of the output is a nominal 240 mw. The operating voltage for the multiplier chain is supplied from the power supply in the Electronic Assembly and is at a +25 vdc level.

The output of the multiplier chain is phase modulated by two of the three tones from the range tracker at a modulation index of 0.3 radians each.

1.4.2 Non-Cooperative Mode Transmitter

In the non-cooperative mode a separate transmitter shown in Figure IV-30 provides a 4.6 microsecond transmit pulse upon command of the PRF generator. A simplified block diagram of the transmitter is shown in Figure IV-31. The exciter multiplies the 102 MHz VCXO output, which is phase locked to the 6.8 MHz signal from the synthesizer, to the desired X-band frequency of 9792 MHz at an output level of 240 mw. The signal is pre-gated phase modulated and routed to the frequency synthesizer. The frequency synthesizer generates the five transmit frequencies for frequency diversity. After additional gating and amplification, to a level of 30 W peak, by the TWTA the signal is routed to the antenna for transmission. The system has been calibrated using a 21 ±0.5 feet run of waveguide between the phase modulator and the transmitter assembly. If this length is changed, the range tracker will be in error proportional to the difference in length.

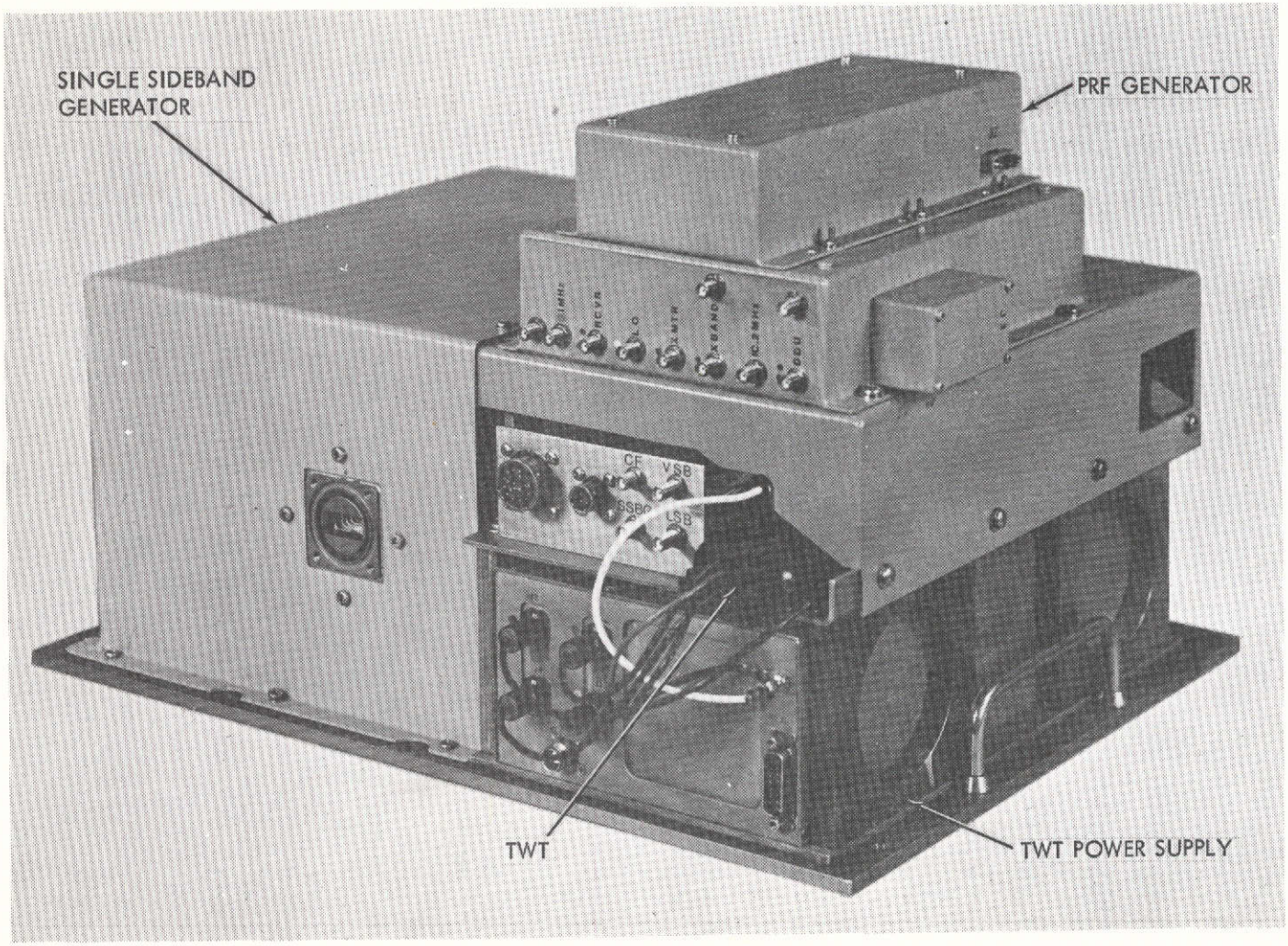


Figure IV-30. Non-Cooperative Mode Transmitter

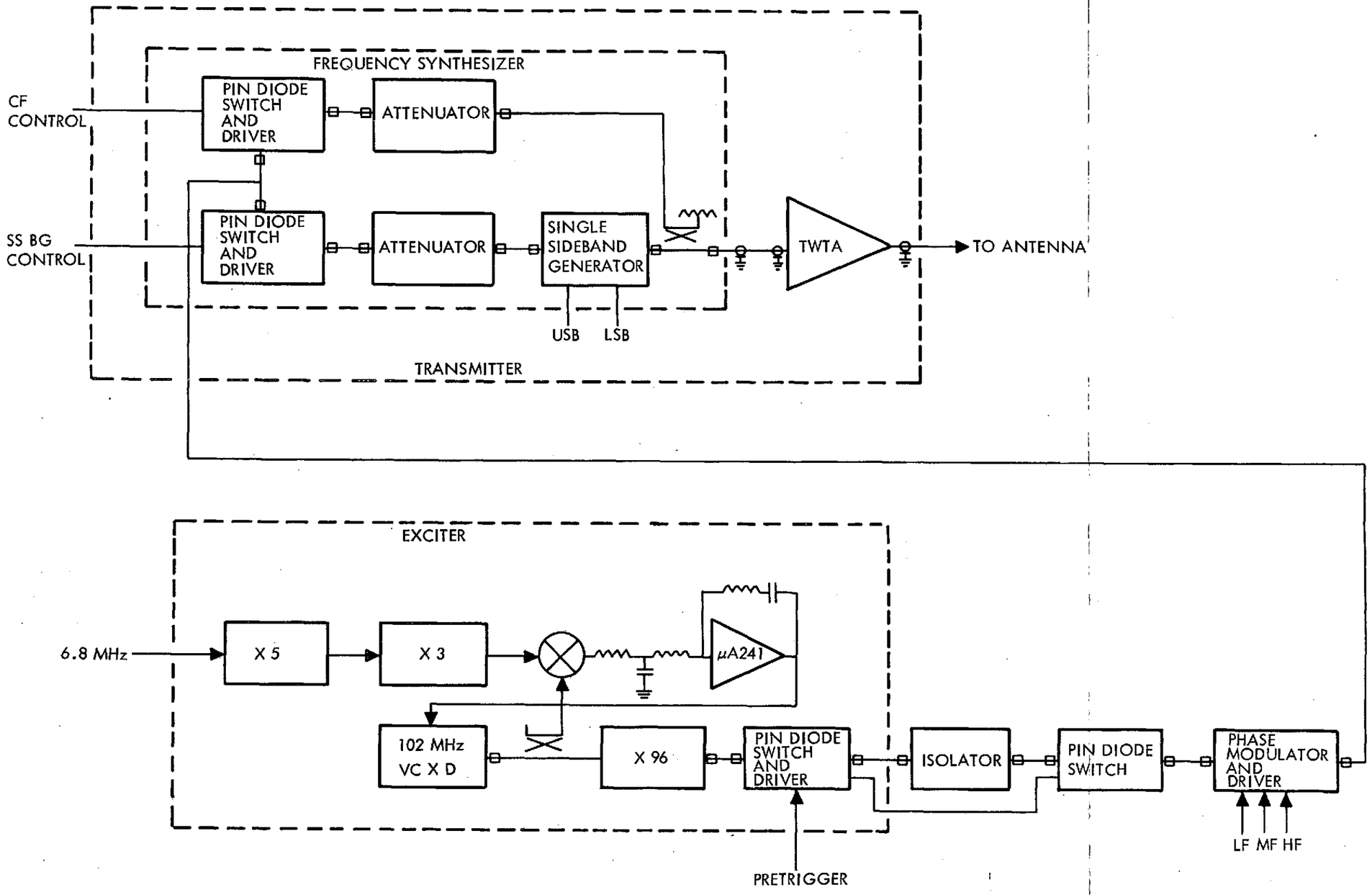


Figure IV-31. Block Diagram - Non-Cooperative Mode Transmitter

The frequency synthesizer for the transmitter shown in Figure IV-32 consists of a single pole double throw waveguide diode switch, a single sideband generator and a waveguide coupler. The switch and coupler are used to bypass the sideband generator when center frequency operation is desired.

The transmitter single sideband generator consists of two varactor modulators which allow generation of upper and lower sidebands about the carrier frequency. The sideband outputs from the modulators are so phased that when combined one of the sidebands is rejected and a single sideband output results. The other sideband may be selected by feeding the modulating signal into a different part of the IF quadrature hybrid.

The modulators used in the transmitter single sideband generator are single varactor single ended devices. The center frequency signal is fed to the modulator through the difference port of a waveguide hybrid. The path length from the hybrid junction HY2 to one modulator, A1, is 45° shorter than the other. The modulating signal is directed to the two modulators by means of an IF quadrature hybrid, HY1. The generated sidebands propagate back to the hybrid junction through the 45° differential path length. The resulting phasing at the junction is such that one sideband (upper or lower) is in phase and exits through the sum port of the hybrid, HY2 and to the output of the sideband generator. The other sideband is 180° out of phase and therefore exits through the difference port and is absorbed in the input isolator. The relative phasing of the sidebands can be reversed by feeding the modulating signal into the other port on the IF hybrid.

The output from the single sideband generator is fed through the band reject filter, to provide carrier rejection, through the coupler to the input of the TWT.

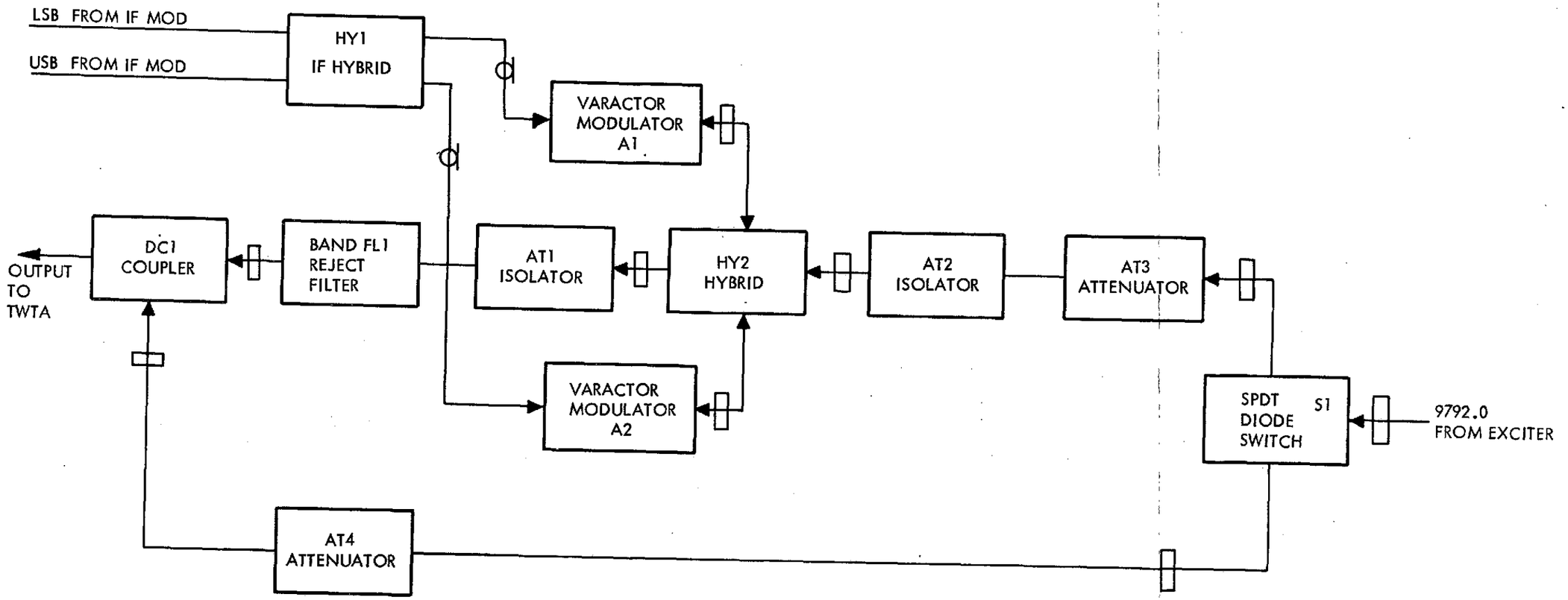


Figure IV-32. Transmitter Frequency Synth.

FOLDOUT [redacted] 1

FOLDOUT [redacted] 2

The transmitter is activated by the transmitter control, shown in Figure IV-33. Three phase 400 Hz power is applied to the transmitter power supply via a 5 amp circuit breaker and a power switch. A separate one phase ON/OFF switch is provided for the TWT cooling fan. The fan switch interlocks the TWT power supply by grounding the operate/standby line. In this state the power supply will not be activated.

A time out circuit is provided which activates the power supply three minutes after turning on the 3 ϕ power switch, the fan switch and placing the operate switch to operate. The time out is not started until all switches are activated. However, once elapsed, the operate switch may be placed in the standby position without resetting the timer. Power is then present as soon as the switch is returned to the operate position. The fault light is illuminated whenever the operate switch is in the standby position.

The transmitter power supply monitors the current to the TWT helix. If this current is found to be excessive, the power supply is transferred to standby and a fault signal is sent to the control unit. A momentary closure of the fault reset switch will return the power supply to the operate mode.

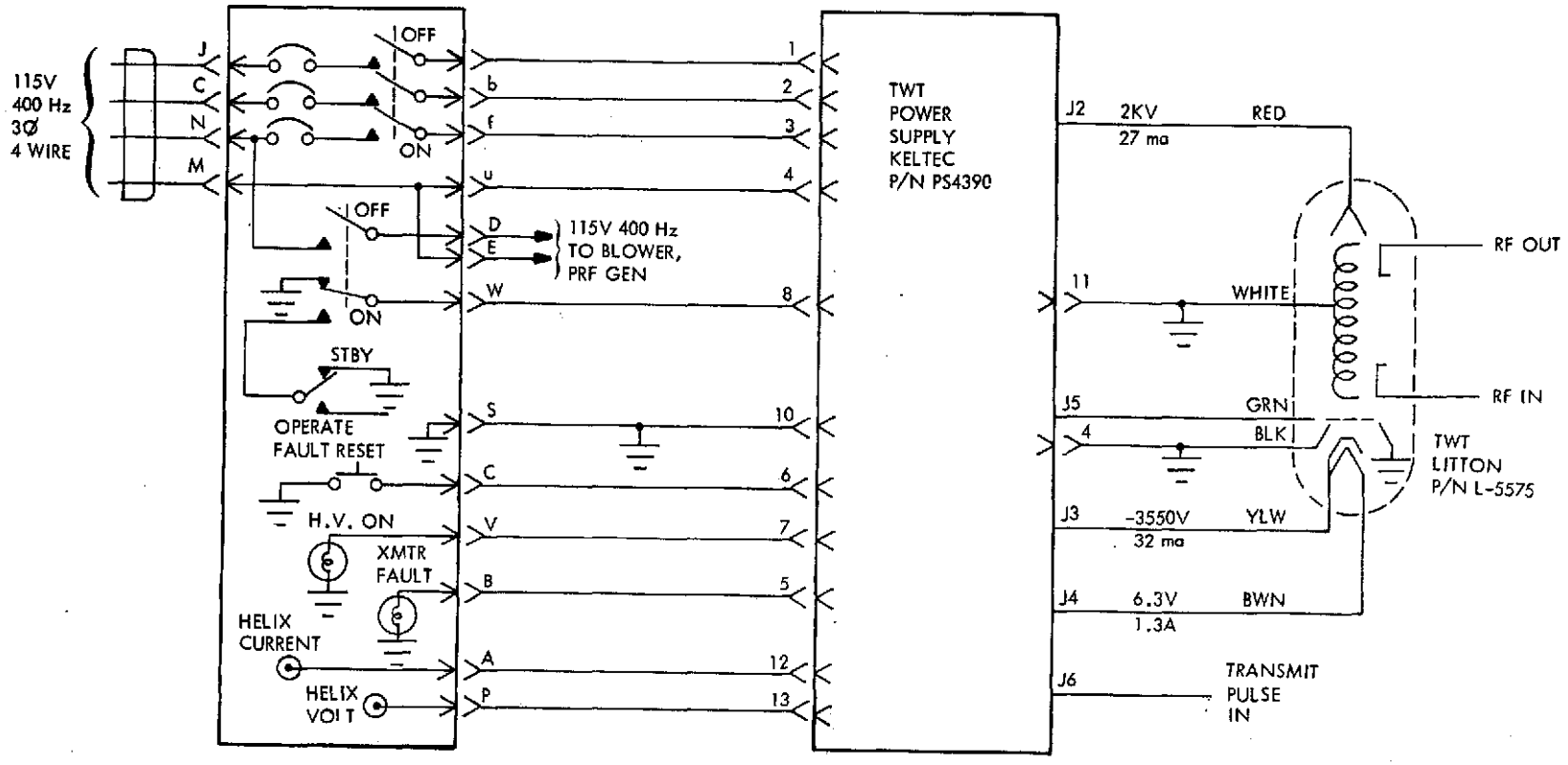


Figure IV-33. Non-Cooperative Mode Transmitter Control

2.0 STE MODIFICATION

Testing of the radar in the non-cooperative mode requires the generation of a simulated target return. This return must be capable of simulated round trip delay in range and varying doppler shift. The simulated round trip delay must include the time delay in both the pulse and the phase delay of the modulated tones. The STE, used for cooperative testing, was modified to provide this capability.

A block diagram of the STE components is given in Figure IV-34. An overall view of the test facility, showing the interrelationship of the various components, is shown in Figure IV-35. Operation of the STE is as follows. A 102 MHz crystal oscillator is multiplied up to X-band, 9792 MHz, to create a synthetic target signal. This signal is then shifted to simulate target doppler shift and the tone phase modulation is added.

Frequency shift of the X-band source is accomplished in two steps. First, the signal is shifted up in frequency by a fixed 40.8 MHz to 9832.8 MHz. The signal is then shifted down by a 40.8 MHz ± 90 kHz. The phase modulation for tone ranging is introduced in the doppler generator using delayed ranging tones.

Delay of the ranging tones is accomplished by the tone delay simulator where three geared phase shifters are varied an amount commensurate with the range. The resultant phase modulated X-band signal is amplified by locking a gunn oscillator. The gunn oscillator output is 10 milliwatts independent of the drive level. The gunn oscillator output is gated by the delayed transmit pulse. The delay introduced by the digital delay unit simulates the target range delay. The signal is routed to the frequency synthesizer where frequency diversity is introduced. The resultant signal is then attenuated to simulated round trip path loss and routed, via waveguide to either the target tower or the antenna shack.

The signal can therefore be coupled to the radar antenna in two ways. The signal may be radiated from the tower by target horn and captured by the radar antenna or the signal in the antenna shack may be directly coupled to the antenna horns via the antenna hat coupler.

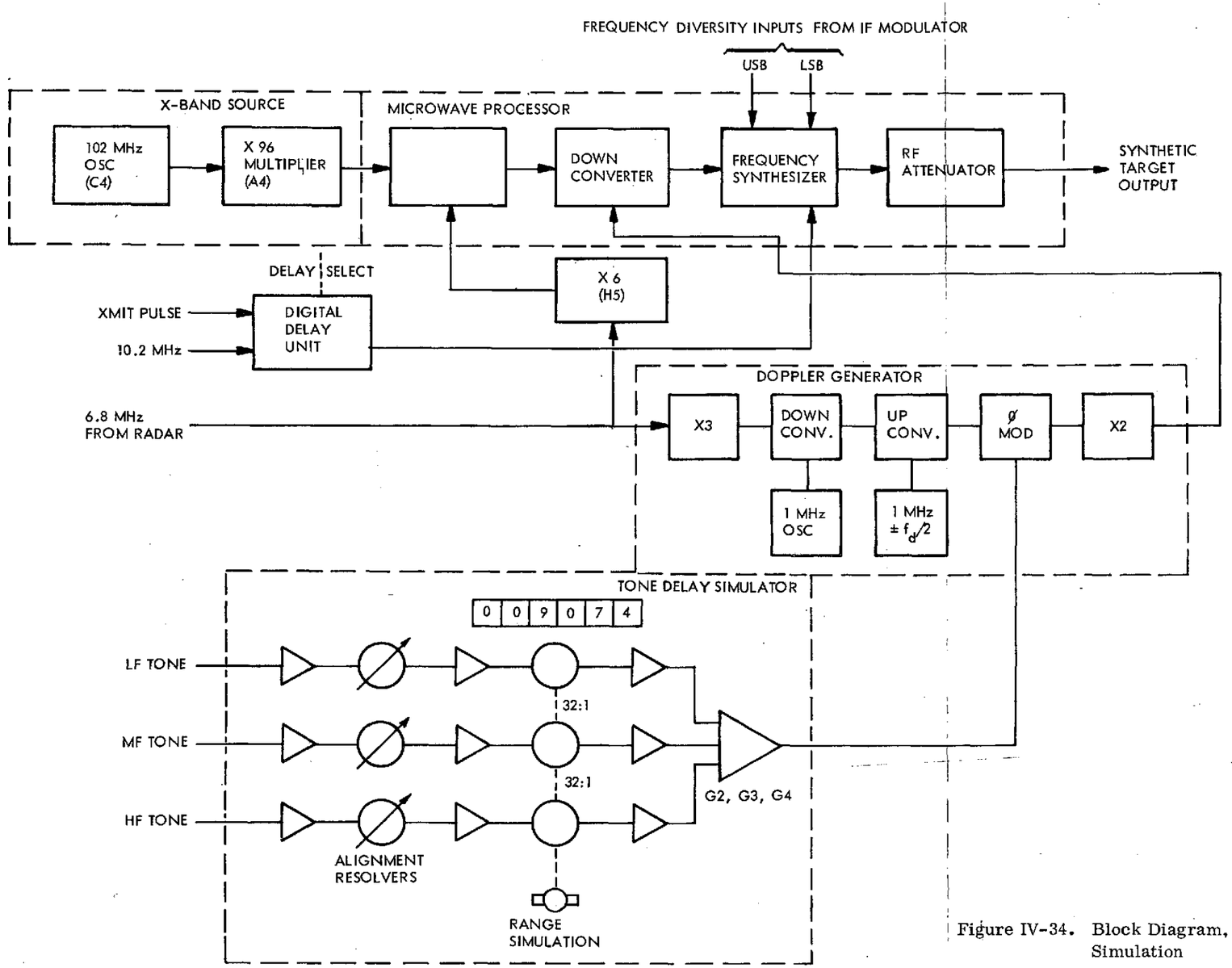


Figure IV-34. Block Diagram, Target Simulation

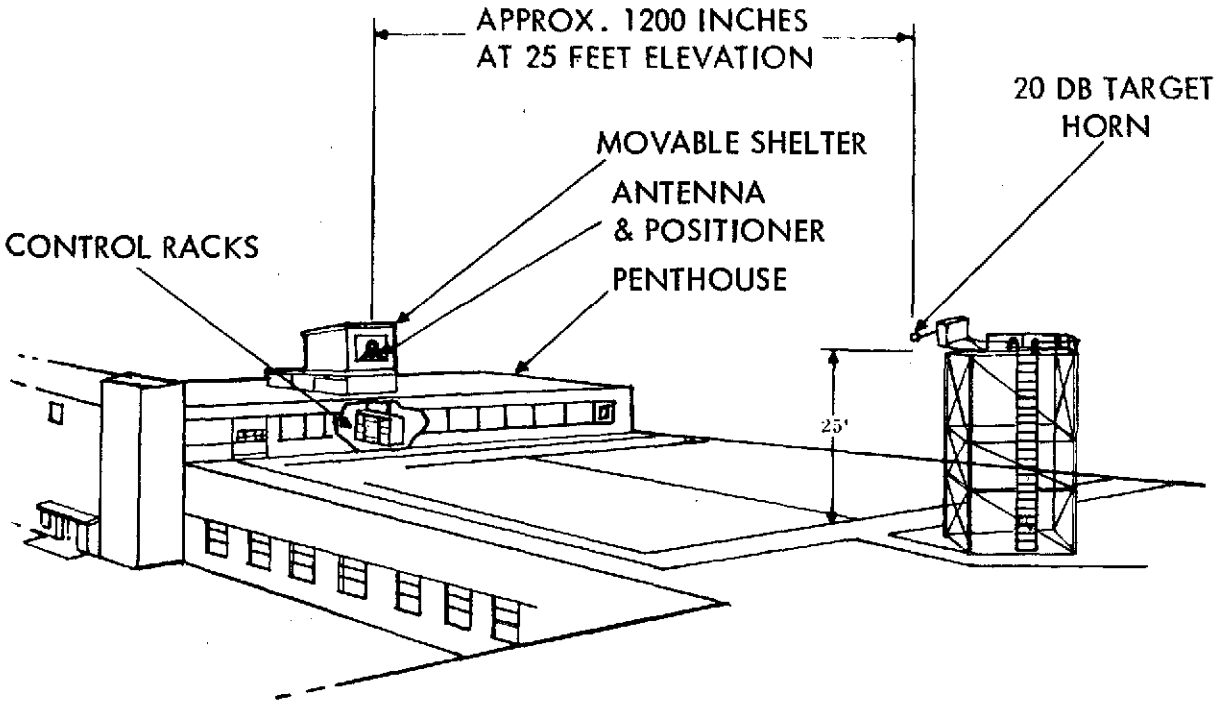


Figure IV-35. Overall Arrangement of Test Facility

The former technique allows testing of the radar's ability to angle track a moving target. However, reflections from surrounding buildings, towers, etc., preclude its use with the transmitter full on. The latter precludes angle tracking since angle information is not available from the hat coupler. However, radar performance in range and doppler may be tested with the transmitter active.

To reduce the effects of the reflections from the surrounding buildings, towers, etc. the radar transmitter signal can be routed to the target horn utilizing the two waveguide runs available from the microwave rack. With minor changes, these two runs may be connected in series, thereby providing a waveguide connection from the antenna shack to the target tower. This allows a portion of the radar transmit energy to be radiated from the target horn as a test signal. It is also possible to connect an auxiliary horn to the waveguide. This horn can then illuminate a fluctuating target. Reflections from this target can be tracked by the radar.

APPENDIX 1

DEMONSTRATION PROCEDURE

APPENDIX 1

DEMONSTRATION PROCEDURE

For No. I, Hat Coupler Tests

Test 1 - Max Detection and Acquisition Range

Step 1. Verify that servo's are off (i.e. 400~ and 800~ Pwr supplies)

Step 2. RF Sources Program Set @

A2, A4
C1, C4
D1, D5
E4 RF level to 64 dB. T to RR path (7 nmi)
F5
G2, G3, G4
H5

Note: Range readouts will be short by ≈ 100 ft unless test equipment re-zero'd

Step 3. Set "Digital Delay Unit" to 7 nmi

Step 4. Set TMRS to 9074 (7 nmi)

Step 5. Set Doppler Simulator to chosen value

Step 6. De-activate simulated target by DEPRESSING G1

Step 7. Switch mode select to "auto track"

Step 8. After AGC ≈ -0.4 re-depress G1

Step 9. Observe and record R, Range, AGC and fd/2 or acquisition time

ACQ time set controls to 1, 0
Time B-A 10^{-3} time base

Simulated doppler fd/2 = 3, 3

Rate C and 1 sec time base

Step 10. Make several acquisitions and record data.

Step 11. Make several acquisitions at different range rates and record data.

Step 12. Take scope photos.

No. 1

No. 2

No. 3 TP's referenced on block diagram

No. 4

No. 5

Test 2 - Min Range Operation

Step 1. Verify that servo's are off.

Step 2. RF Sources Program set @

A2, A4

C1, C4

D1, D5

E4 Set RF level to max (0 dB) in T to RF path for min range

F5

G2, G3, G4

H5

Step 3. Set Digital Delay Unit to 94 feet.

Note: Range readouts will be short by ≈ 100 ft. unless test equipment is re-zero'd.

Step 4. Set TMRS to 100 (i.e. 500 ft used because of above note)

Step 5. Set doppler simulator to chosen value.

Step 6. De-activate simulated target by DEPRESSING G1

Step 7. Switch mode select to auto track.

Step 8. After AGC ≈ -0.4 re-DEPRESS G1.

Step 9. Observe and record R, Range, AGC, and f/2 or acquisition time.

Note: ACQ time = 10 on counter set time B-A, 10^{-3} time base SIM DOPPLER fd/2 = 33, Rate C, and 1 sec time base.

Step 10. Make several acquisitions and record data.

Step 11. Make several acquisitions at different range rate and record data.

Step 12. Observe scope readouts at test points, and photograph scope display of wide-band IF and receiver tones after filters.

For No. II, Demo of Clutter Return Signals

Step 1. Observe scope display.

Step 2. Vary antenna pointing angles over range of clutter targets - observe AGC and scope display.

Step 3. Track strong simulated target in presence of clutter.

Step 4. Reduce TWT output level and track simulated target at lower power levels.

For No. III, Demo of Acq and Track @ 7 nmi

Step 1. RF Sources Program

A2, A4
C1, C4
D1
E4 — RF level 53 dB (≈ 7 nmi) atten T to RR (AGC (1.0) W PRF ±0.2)
F5
G2, G3, G4
H5

Step 2. TMRS @ 9076 (7 nmi)

Step 3. Doppler simulator to chosen value.

Step 4. Digital delay unit to 7 nmi.

Step 5. Target to center position.

Step 6. Go to manual designate and have antenna designated to

349.5° shaft
190.0 trunnion } Upper left of Vol uncertainty

(target @ center = 000 shaft and 181. trunnion)

Step 7. Move mode select to auto track.

Step 8. Switch scan programmer to "scan" - observe and record R, Range and AGC.

Step 9. Turn on moving target @ rate "1" (3 mr/sec)

Step 10. Recycle and re-acquire the moving target.

recycle
(1) Set scan programmer to "normal"
(2) Set mode select to manual

reacquisition
(3) Mode select to auto after AGC goes to -0.4
(4) Set scan programming to "scan"
Observe and record R, Range and AGC.

Step 11. Turn up moving target rate to No. ($\approx 0.8°$/sec)

Step 12. Recycle and reacquire the fast moving target.
Observe and record R, Range and AGC.