JSC-09285
[EE2-74-026-(U)]
Revision A

NASA CR-141611

SHUTTLE EXTRAVEHICULAR ACTIVITY SIGNAL PROCESSOR PULSE AMPLITUDE MODULATION DECOMMUTATOR

Job Order 11-229

(This revision supersedes LEC-3649 issued May 1974.)

Prepared By

Lockheed Electronics Company, Inc.
Aerospace Systems Division
Houston, Texas

Contract NAS 9-12200

For

FLIGHT TELECOMMUNICATIONS BRANCH
TRACKING AND COMMUNICATIONS DEVELOPMENT DIVISION

National Aeronautics and Space Administration

LYNDON B. JOHNSON SPACE CENTER

Houston, Texas

December 1974

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ACKNOWLEDGEMENT

This is to acknowledge the contributions of K. Duane McLain in the design and development work on the pulse amplitude modulation decommutator. This work was a joint effort of Lockheed Electronics Company, Inc., and National Aeronautics and Space Administration personnel. Mr. McLain was responsible for the work on the digital automatic scaler and for preparation of the material of section 4.2 of this report.

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ABBREVIATIONS, ACRONYMS AND SYMBOLS

ADC	Analog-to-Digital Converter
ADS	Audio Distribution System
AMP	Amplifier
BP	Band Pass
CNR	Carrier-to-Noise Ratio
CTR CLK	Counter Clock
DC	Direct Current
DEL CLK	Delayed Clock
EKG	Electrocardiogram
ESP	Extravehicular Activity Signal Processor
EVA	Extravehicular Activity
EVC	Extravehicular Communications
FM	Frequency Modulation
IRIG	Interrange Instrumentation Group
LP	Low Pass
MDM	Multiplexer Demultiplexer
NRZ	Nonreturn-to-Zero
PAM	Pulse Amplitude Modulation
PAM-RZ	Pulse Amplitude Modulation-Return to Zero
SIM	Simulator
S/R	Shift Register

SNR	Signal-to-Noise Ratio
TM	Telemetry
UHF	Ultra High Frequency
VCO	Voltage Controlled Oscillator
VDC	Volts Direct Current
XMTR	Transmitter
decom	Decommutator
rms	Root-Mean-Square
sync	Synchronizer

SHUTTLE EXTRAVEHICULAR ACTIVITY SIGNAL PROCESSOR PULSE AMPLITUDE MODULATION DECOMMUTATOR

1.0 SUMMARY

The Pulse Amplitude Modulation (PAM) decommutator (decom) portion of the Shuttle Extravehicular Activity Signal Processor (ESP) receives a Pulse Amplitude Modulation-Return to Zero (PAM-RZ) signal and has the capability of correctly processing the data for the Multiplexer Demultiplexer (MDM) interface, even though the received wavetrain varies significantly from normal.

The PAM decom fulfills the goal of providing data with long-term stability and accuracy. This was achieved by synchronizing the PAM decom to the PAM-RZ wavetrain and by sampling each channel with a common sample and hold circuit before digitizing the data sequentially. The digital value of each channel is then scaled by the digital value of the calibration channels. The corrected digital value of each channel is then provided as an output signal and is included in a block of serial digital data.

2.0 INTRODUCTION

The Extravehicular Activity system for the Shuttle includes two EVA signal processor systems which in turn include PAM decommutators.

The PAM decommutator was developed to identify and digitize each analog channel of the input signal, and to present the digital data in proper format for an MDM interface unit. The decom is designed for laboratory test use and for use in establishing specification requirements for flight hardware.

3.0 SYSTEM DESIGN CONCEPT

The overall onboard Extravehicular Activity system block diagram for Shuttle is shown in figure 3-1. This diagram shows redundancy, and therefore two EVA signal processors are shown. Figure 3-2 shows the system frequencies. The 7.35- and 10.50-kHz subcarriers contain the PAM wavetrain which the PAM decommutators receive.

The design approach taken for the PAM decommutator development is to provide data with long-term stability and accuracy. To fulfill this philosophy, the PAM decommutator is synchronized to the PAM-RZ wavetrain, and each channel is sampled with a common sample and hold circuit and digitized sequentially. The digital value of each channel is then scaled by the digital value of the calibration channels. The corrected digital value of each channel is stored for one complete frame and then transferred to the MDM at a high rate in one block of serial digital data. A block diagram of the decommutator is shown in figure 3-3.

This approach was chosen over an all analog approach of sampling and holding each channel, performing a correction of the value using an analog scaler and then buffering some 50 to 60 analog channels to the MDM where the values would be sampled and digitized. One drawback of such a system is the inaccuracies that can occur after scaling has been performed. Also, the linearity of each channel would have to be checked and the stability maintained. The number of interface wires to the MDM in this approach is at least double the serial digital interface requirement.

The PAM decom specifications are presented in table I and the PAM waveform is identified in figure 3-4.

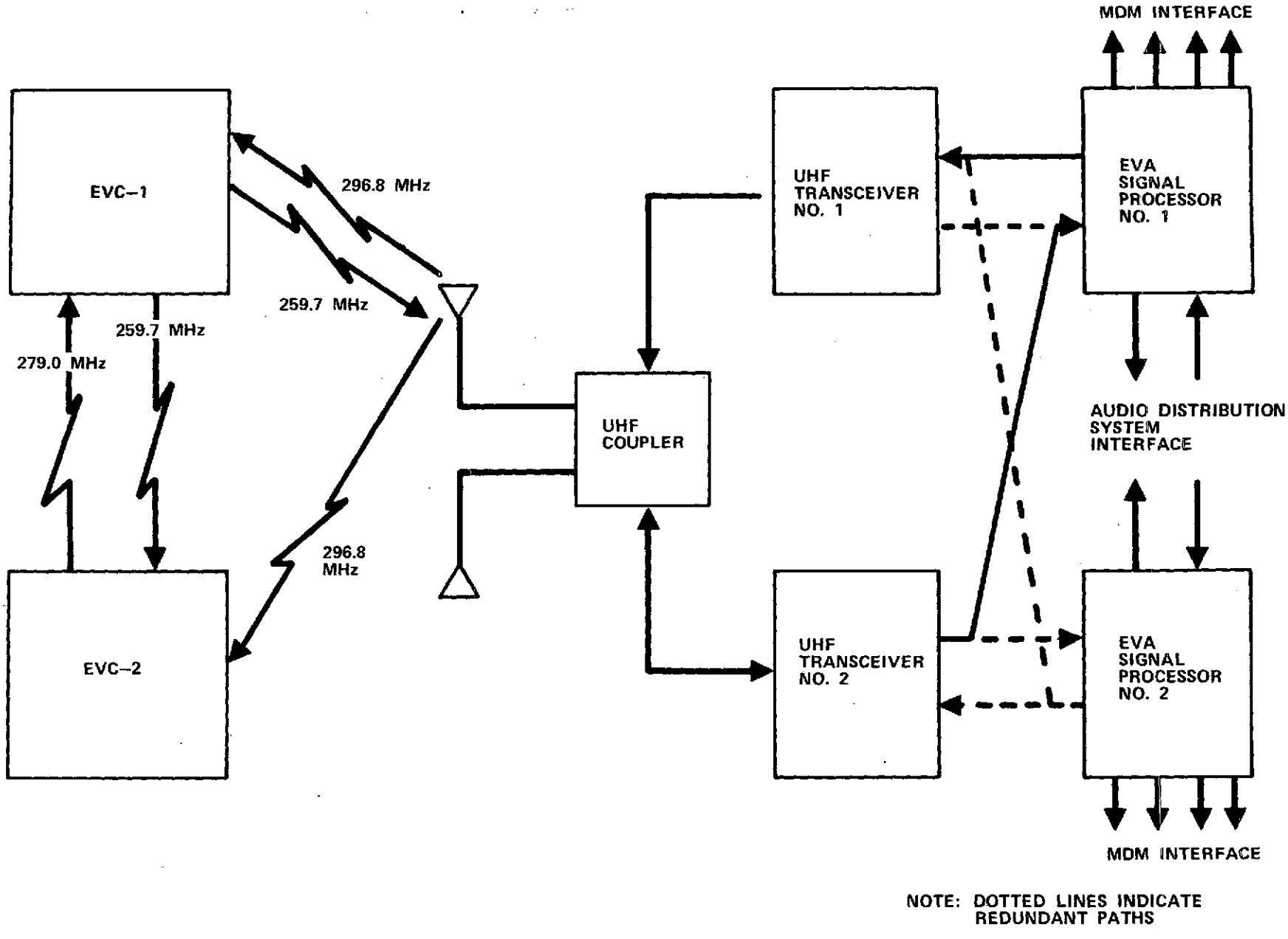


Figure 3-1. – System configuration.

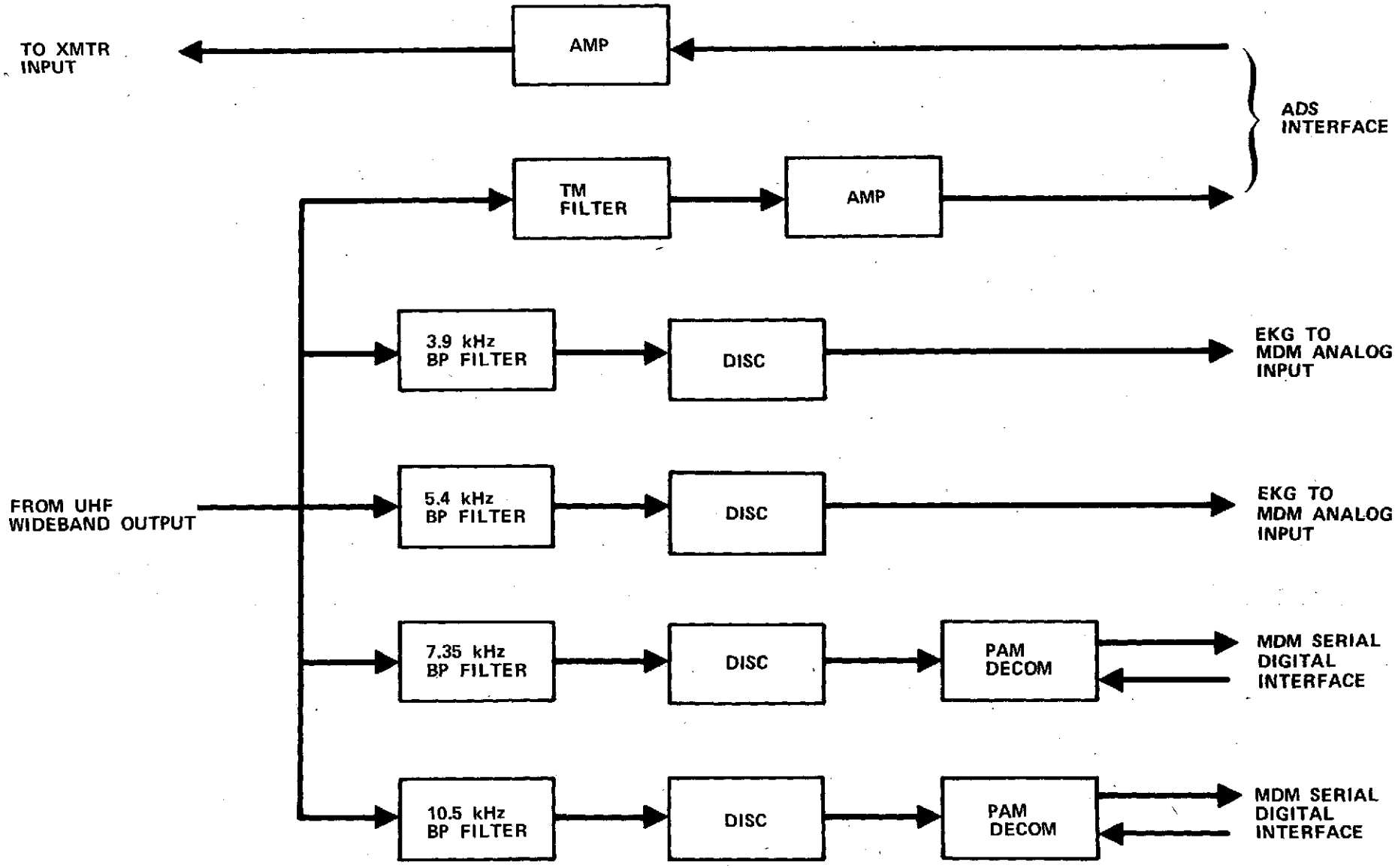


Figure 3-2. – EVA signal processor.

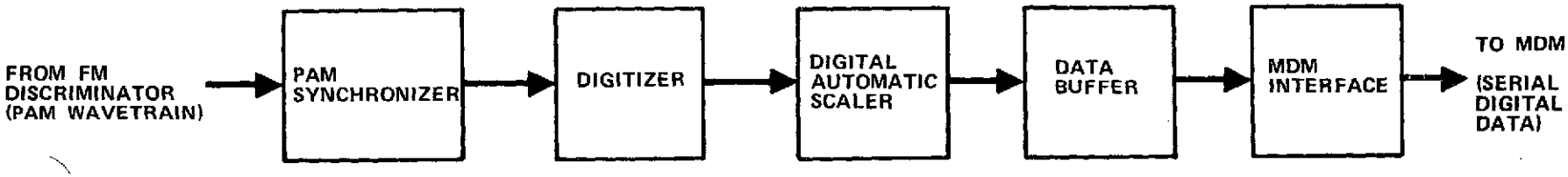


Figure 3-3. – PAM decommutator block diagram.

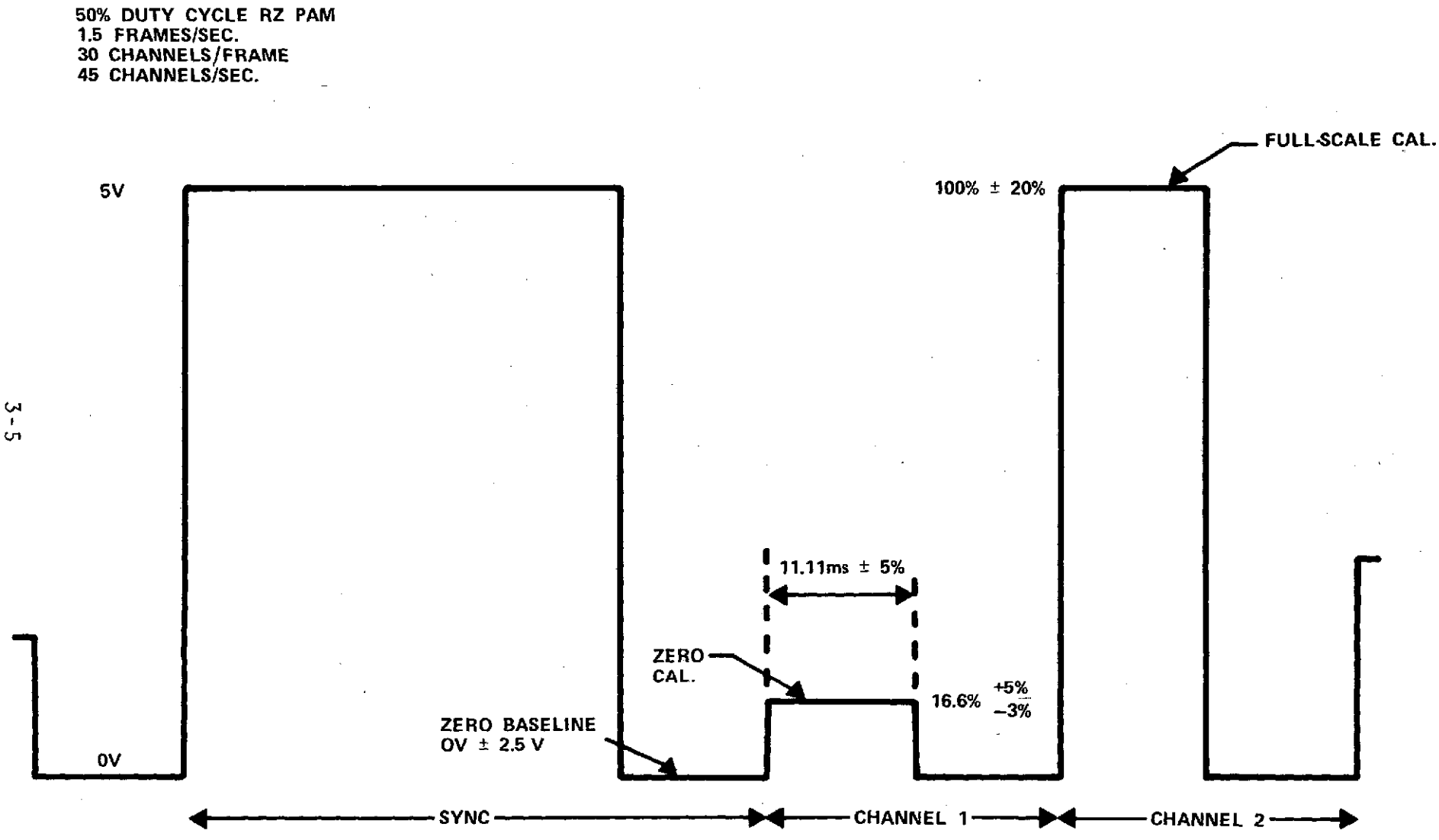


Figure 3-4. – PAM waveform.

TABLE I.- SHUTTLE EVA SIGNAL PROCESSOR,
PAM DECOM SPECIFICATIONS.

Input Characteristics	(Refer to fig. 3-4).
Amplitude	PAM-RZ: Nominal 5 V peak-to-peak ±20 percent.
Baseline Direct Current (DC) Offset	Baseline at ground ±2.5 V.
Polarity	Positive for increasing percentage.
Input Impedance	5000 ohm (discriminator requirement).
Input Overload	±14 V at the input will not damage the equipment.
Pulse Rate	PAM-RZ: 45 pulses per second ±10 percent.
Duty Cycle	PAM-RZ: 50 percent ±5 percent of channel period.
PAM-RZ Pedestal	16 percent of peak-to-peak amplitude +5 percent, -3 percent of peak-to-peak amplitude.
Frame Format	The system will operate with Interrange Instrumentation Group (IRIG) two-channel synchronization pulse format for PAM-RZ. There will be 30 channels with 26 channels for data, two channels for calibration and two channels for sync. The frame rate will be 1.5 frames per second ±10 percent.
Channel Calibration Location	As suggested in IRIG telemetry standards: Channel number 1 is 0 percent of full scale. Channel number 2 is 100 percent of full scale.

TABLE I.- SHUTTLE EVA SIGNAL PROCESSOR,
PAM DECOM SPECIFICATIONS. - Continued

System Accuracy	
Accuracy	The output accuracy of any amplitude of any channel must be within ±0.5 percent of full scale.
Nonlinearity	Within ±0.5 percent of full scale from the best fit straight line through the transfer function plot.
Overrange	Any one data channel may be any value from baseline to +150 percent of peak-to-peak of the input signal without causing degradation of performance of any other channel.
Synchronization	
Signal-to-Noise Ratio (SNR) Measurement Method	Frequency modulate a 7.3-kHz signal to obtain a delta frequency ±7-1/2 percent with a 45-Hz sine wave. Sum the frequency modulated signal with white Gaussian noise. Connect the summed signal and noise into a channel 11 proportional-bandwidth ±7-1/2 percent frequency modulated (FM) discriminator with a constant delay 110-Hz output filter. Measure the root-mean-square (rms) signal to rms noise ratio at the discriminator output filter output. Replace the 45-Hz modulating sine wave frequency with an equal peak-to-peak voltage PAM-RZ 45 channel per second wavetrain. The data channels should have random amplitudes except that their arithmetic average should equal 50 percent of full scale.

TABLE I.- SHUTTLE EVA SIGNAL PROCESSOR, PAM DECOM SPECIFICATIONS. - Concluded

Signal-to-Noise Ratio	The unit will acquire and maintain channel lock with an average change in phase error of less than ±10° when the rms signal to rms noise ratio (not CNR) is 50 percent of the FM discriminator threshold rms signal to rms noise ratio. The unit will acquire and maintain at least 99 percent frame synchronization when the rms signal to rms noise ratio (not CNR) is 85 percent of the FM discriminator threshold rms signal to rms noise ratio. The signal with noise is to be obtained through an IRIG proportional-bandwidth ±7-1/2 percent channel 11 FM discriminator, the output filter to be a nominal frequency response constant delay filter. The channel 11 filter is 110 Hz.
Channel Amplitude	Synchronization will be maintained with normal sync channels but all other channels at 0 percent, provided the input pulse rate is constant and noise and jitter are not present.
Channel Jitter	Synchronization will be maintained with up to ±10 percent channel-to-channel jitter.
Power In	28 VDC ± 4 V

4.0 GENERAL CIRCUIT DESCRIPTION

The PAM decommutator consists of three principal sections. These are the synchronizer (sync) and digitizer section, the digital automatic scaling section, and the data buffer and MDM interface section. These sections are wire-wrapped on plug-in boards. The plug-in board card cage is attached to a display panel and is rack mountable.

4.1 SYNCHRONIZER AND DIGITIZER SECTION

The synchronizer and digitizer section has three main branches. They are the channel synchronizer branch, the frame synchronizer branch, and the digitizer branch. The block diagram of the three branches is shown in figure 4-1.

4.1.1 Channel Synchronizer Branch

After the incoming signal is buffered and direct current restored, the signal enters the channel synchronizer branch. The schematic of this branch is shown in figure 4-2. The signal is prepared for the phase locked loop by being passed through a 55-Hz low pass filter. The signal is limited near 80 percent and then passed through a squaring amplifier. The aim of the limiter and squaring amplifier is to increase the weight of middle amplitude signals where impulse noise is least severe. The signal then enters the phase locked loop where clocks are generated at the channel rate of 45 Hz and 20 times the channel rate or 900 Hz. The 45-Hz channel rate clock is used to increment the channel number counter. The 900-Hz (channel rate times 20) clock is decoded and used to time events during each channel period.

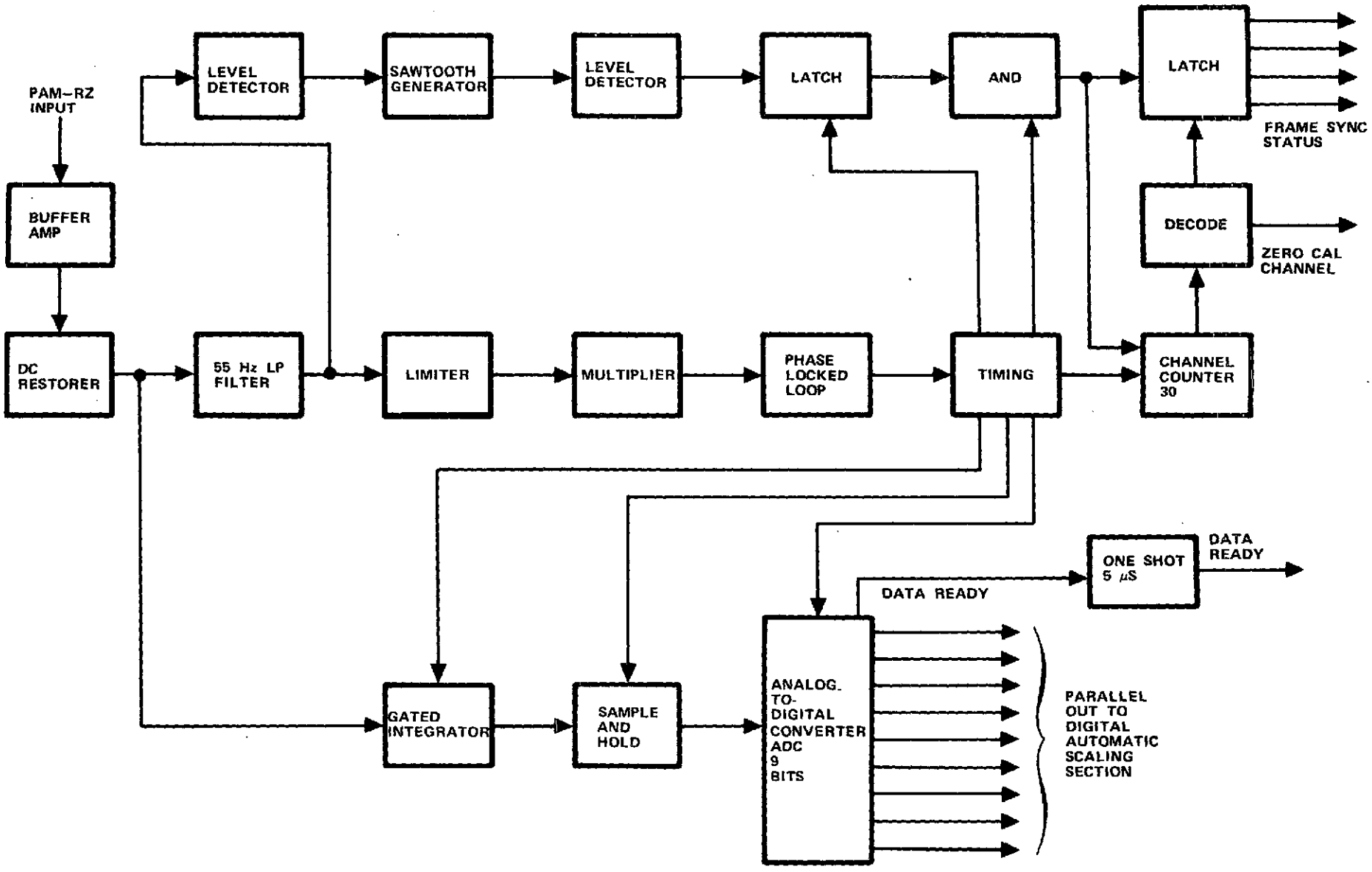


Figure 4-1. – Synchronizer and digitizer block diagram.

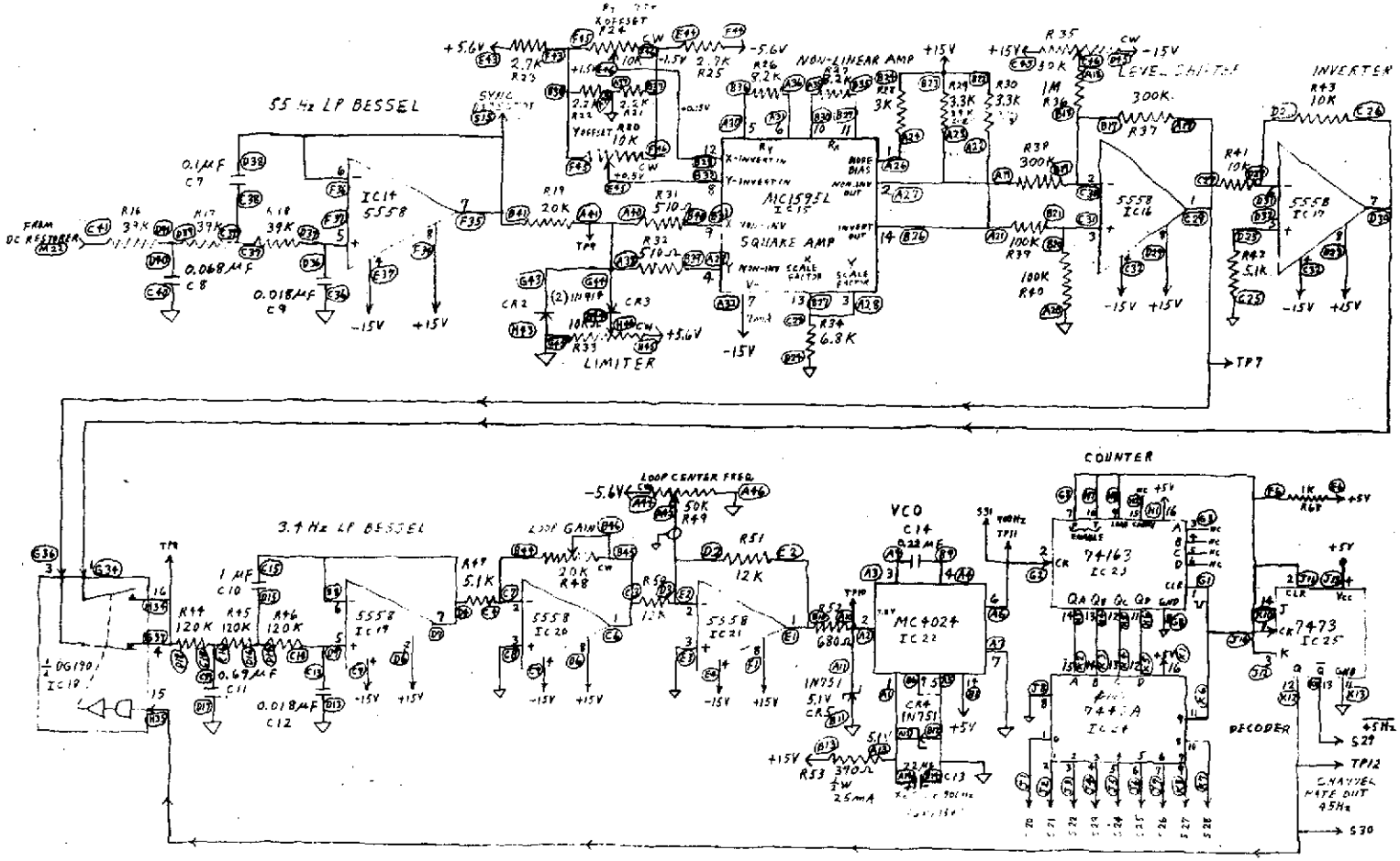


Figure 4-2. — Channel rate phase locked loop schematic.

4.1.2 Frame Synchronizer Branch

The frame synchronizer accepts the signal after it passes through the 55-Hz low pass filter. The schematics of this section are shown in figures 4-3 and 4-4. A gate is turned on when the wavetrain level reaches 80 percent and turns off at 20 percent. The large hysteresis reduces the effect of impulse noise on the sync pulse. The first gate starts a ramp. If the ramp lasts as long as a sync pulse, the next gate is turned on, and a sync pulse is identified. In order to obtain test data, four sync status indication signals are used. Each signal is displayed and any one of the four, as selected by a front panel switch, may be routed to the MDM data buffer to indicate sync in the status word.

Sync status "A" is true after the first sync pulse is recognized. It becomes false after 30 channel periods without a new sync pulse identification.

Sync status "B" is true when sync status "A" is true and the channel counter is synchronized.

Sync status "C" becomes true if the sync pulse is recognized after sync status "B" becomes true. It becomes false after two consecutive sync pulses are not recognized.

Sync status "D" is true when either sync status "B" or sync status "C" is true.

The channel counter is reset by each recognized sync pulse when sync status "C" is false.

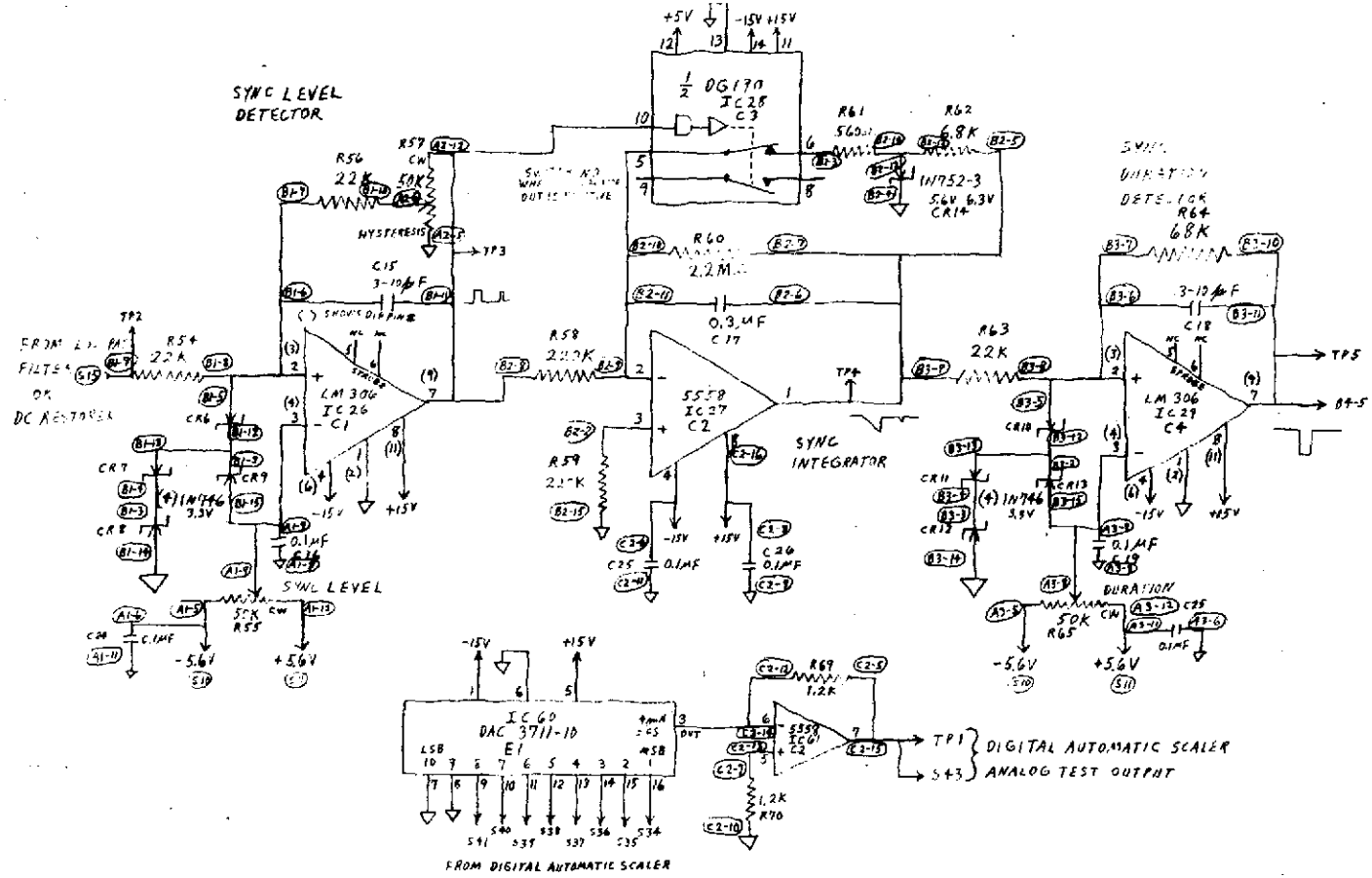


Figure 4-3. – Synchronization detector schematic.

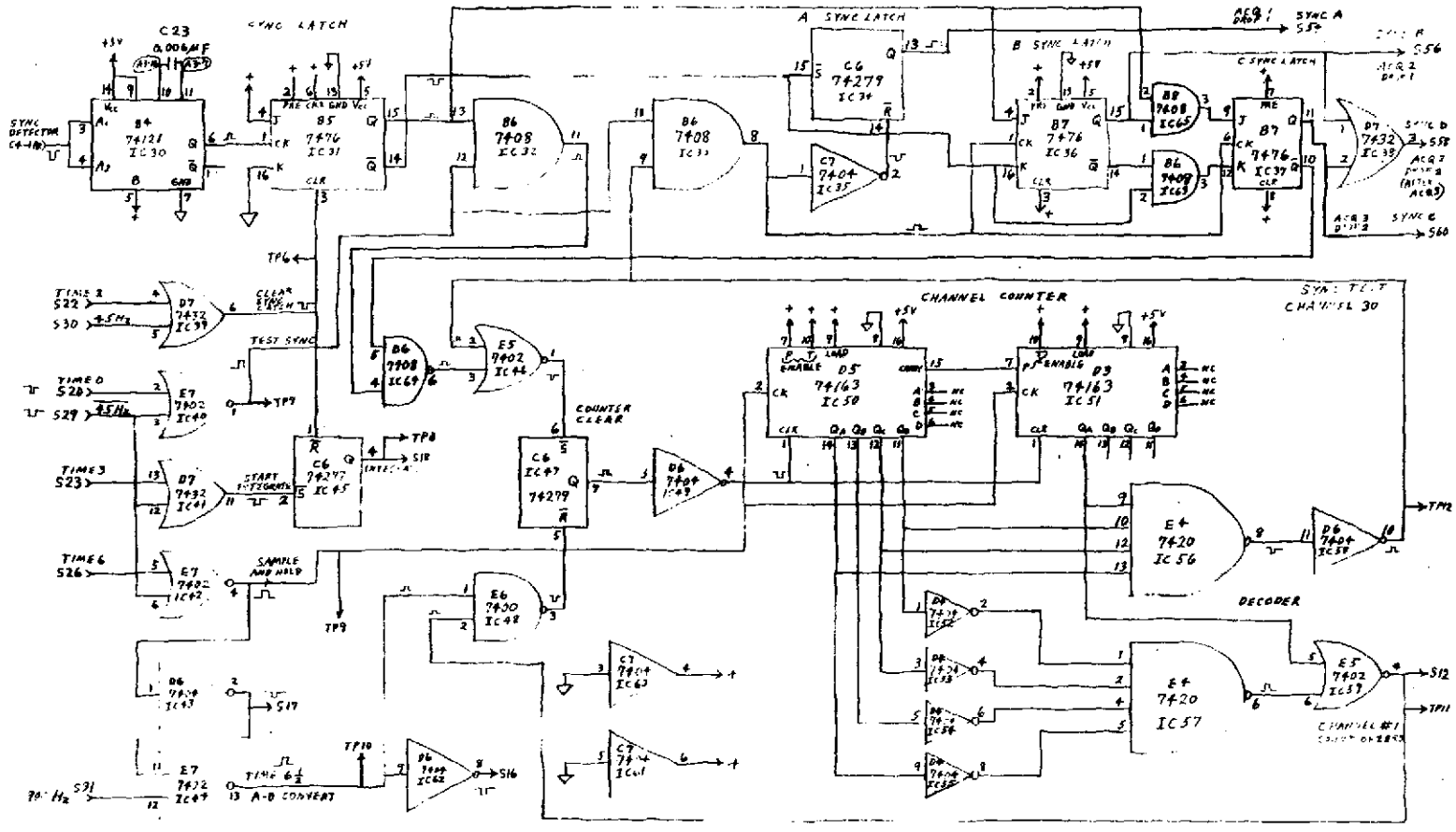


Figure 4-4. — Timing and synchronization status schematic.

4.1.3 The Digitizer

The digitizer section receives the PAM-RZ waveform after the DC restorer has removed any DC level shift. The schematic is shown in figure 4-5.

A gated integrator is used so that after each channel reaches full amplitude, the top flat portion is integrated to average out noise.

After integration, a sample and hold circuit maintains a constant voltage for a 12-bit analog-to-digital converter (ADC). It is necessary to use at least 9 bits of the analog-to-digital converter to obtain the specified accuracy of ± 0.5 percent of full scale when the maximum input amplitude may vary ±20 percent of full scale. A 12-bit analog-to-digital converter is used because of the better linearity specification normally available in 12-bit analog-to-digital converters as compared to 9-bit analog-to-digital converters.

The output of the analog-to-digital converter is sent to the digital automatic scaling section for scale correction.

4.2 DIGITAL AUTOMATIC SCALER

The function of the digital automatic scaler is to give each data channel its correct digital value by comparing its amplitude relationship to the 0 percent and 100 percent calibration channels. The block diagram of the digital automatic scaler is shown in figure 4-6. The schematics are shown in figures 4-7 and 4-8. A flowchart is shown in figures 4-9. The signal inputs to the scaler are: the zero calibration

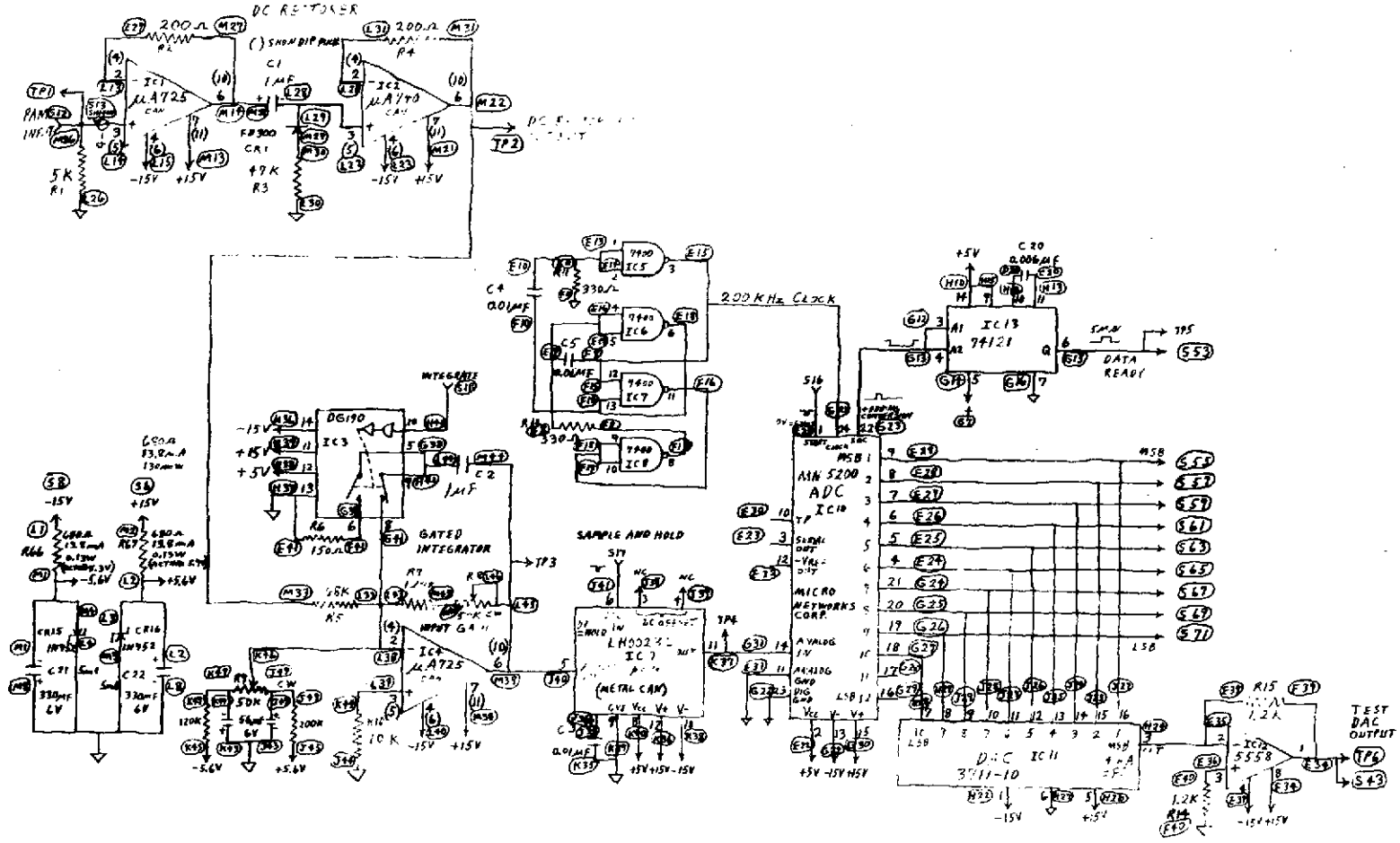


Figure 4-5. – Analog-to-digital converter schematic.

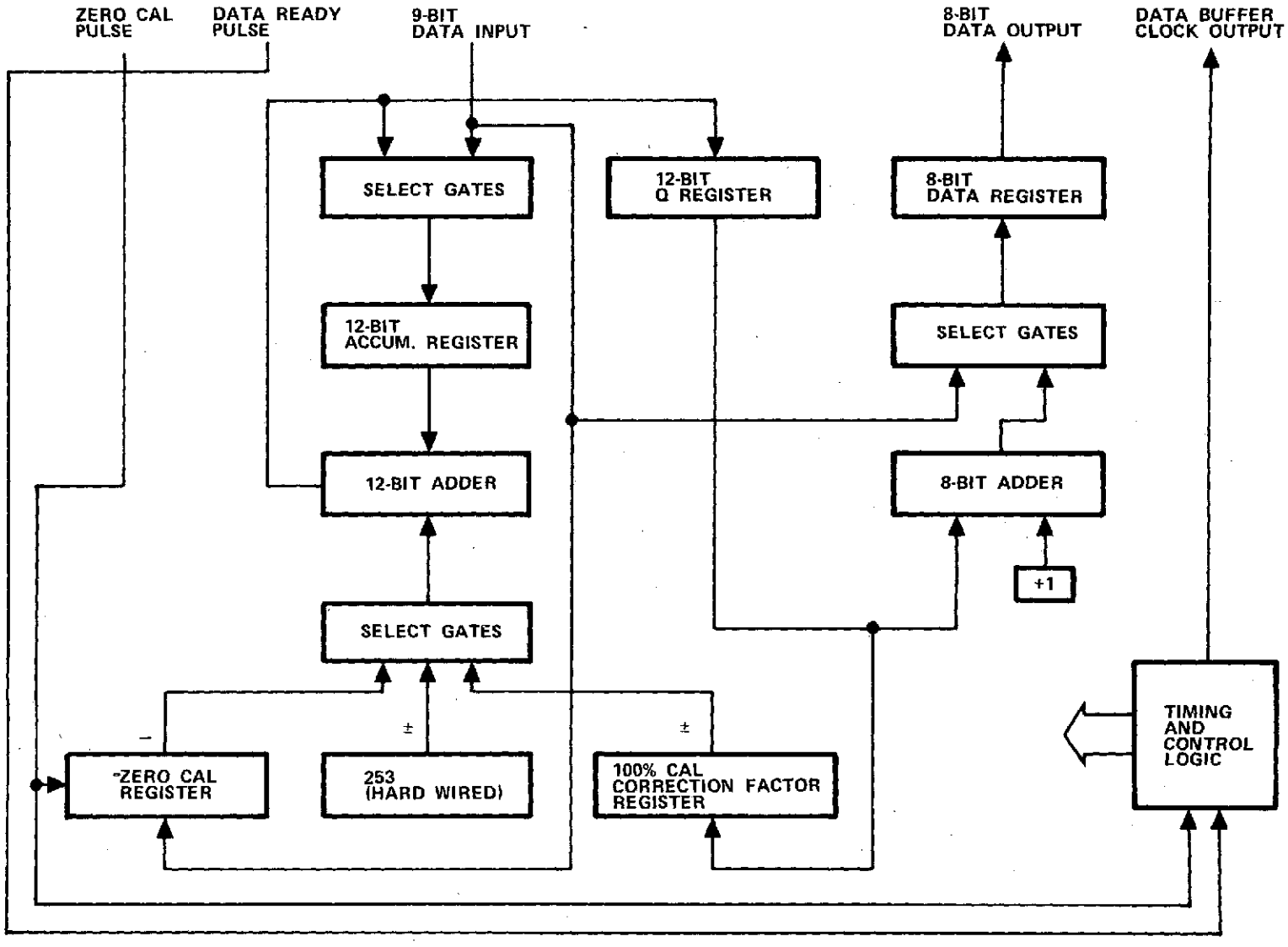


Figure 4-6. – Digital automatic scaler block diagram.

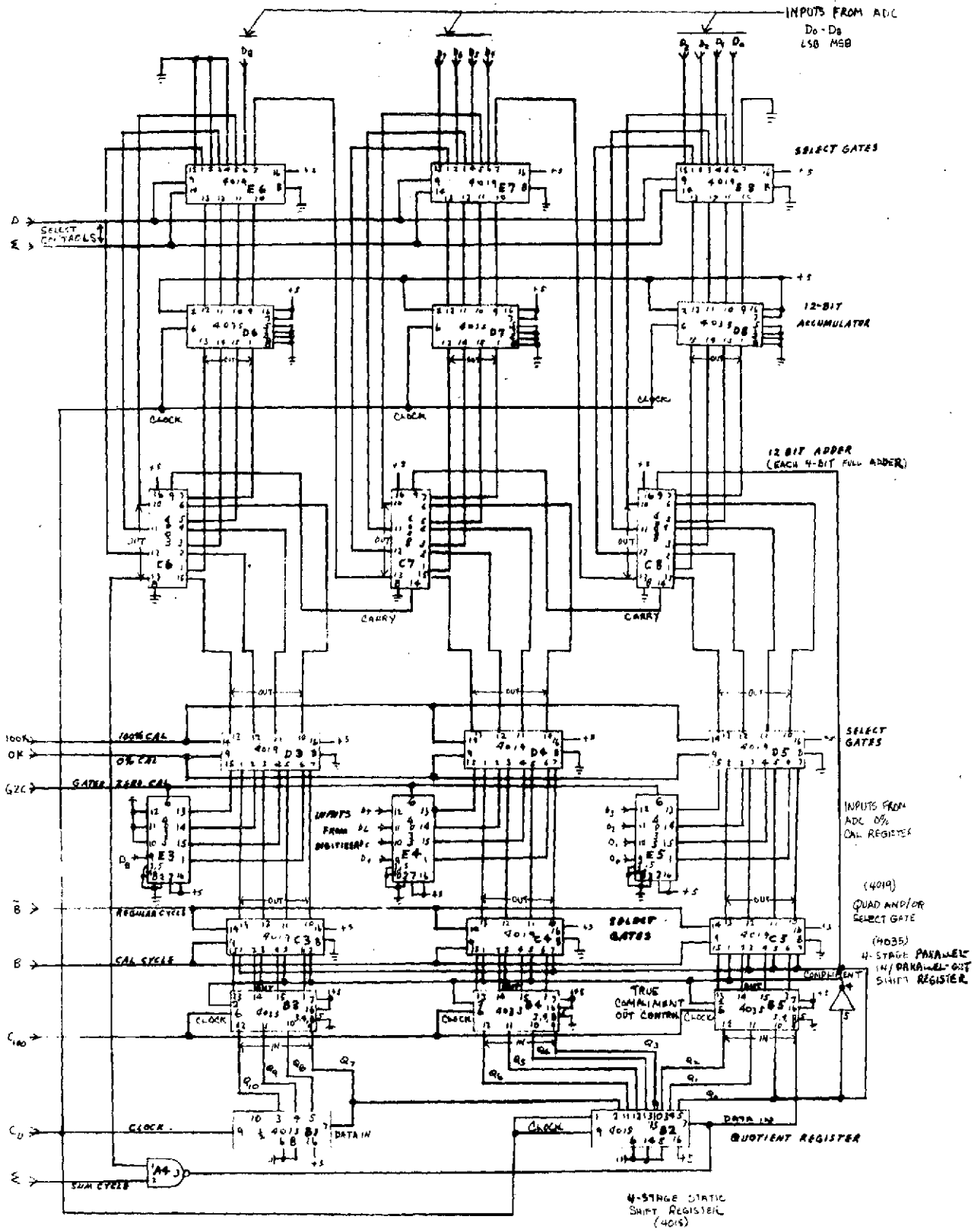


Figure 4-7. — Digital automatic scaler (section one) schematic.

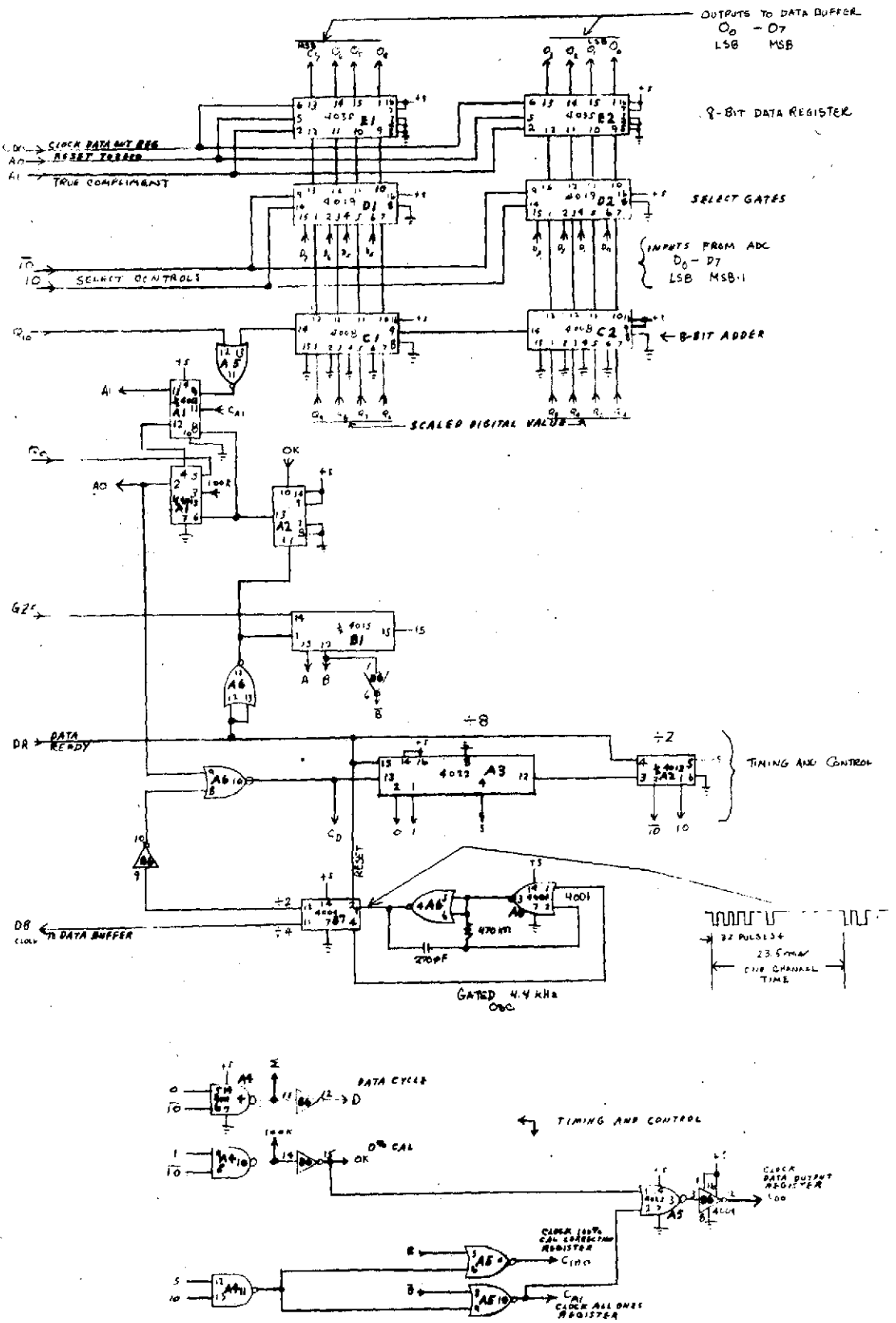


Figure 4-8. – Digital automatic scaler (section two) schematic.

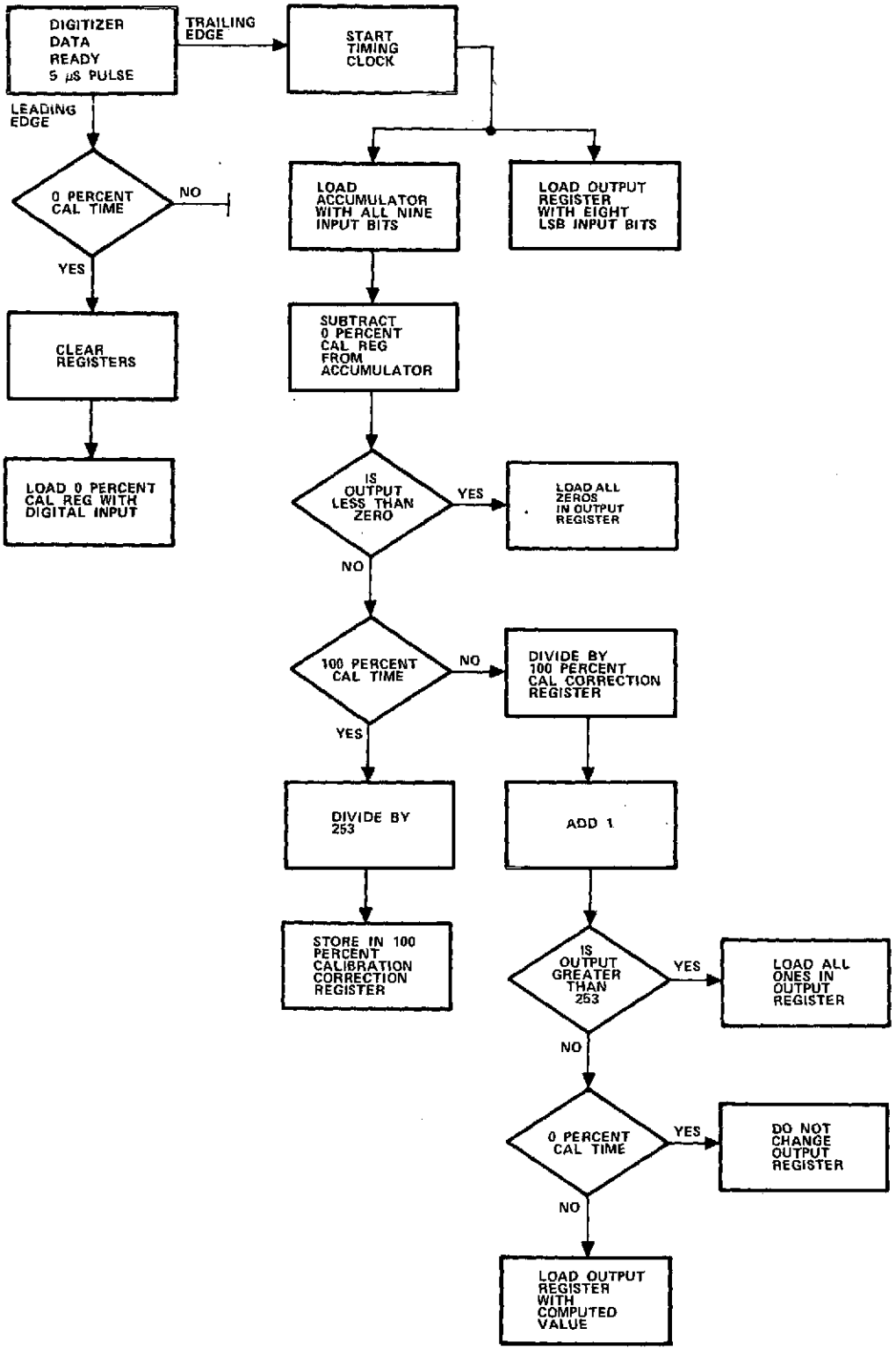


Figure 4-9. – Digital automatic scaler flowchart.

pulse to indicate that the input data is the 0 percent calibration information; the data ready pulse to indicate that the input data is stable and ready for processing; and the 9-bit data input from the digitizer section of the PAM decommutator. The signal outputs of the scaler are the 8-bit data output and a data buffer clock used by the data buffer.

The advantage of the digital scaler is its long-term stability and no set-up adjustments. At the beginning of each frame, the scale factors are recalculated and all data in that frame is scaled accordingly.

Basically, the scaler has three different processing operations: 0 percent calibration processing, 100 percent calibration, and data processing. These operations will be discussed individually, following a discussion of the digital output requirements.

The requirements on the scaler output data are:

1. The 9-bit 0 percent calibration and 100 percent calibration data will be put out in the 8-bit output unchanged, except that the most significant bit of the 9-bit number will be dropped.
2. Data which is less than the zero calibration value will be put out as 00000000_2.
3. Data which is equal to the zero calibration value will be put out as 00000001_2.
4. Data which is equal to the 100 percent calibration value will be put out as 11111110_2.

5. Data which is greater than the 100 percent calibration value will be put as 11111111_2.

6. Data which is greater than 0 percent calibration but less than 100 percent calibration will be put out as an 8-bit number whose magnitude reflects the percent relationship between the data and the 100 percent calibration, both referenced to 0 percent calibration, where 100 percent equals 11111110_2.

The first type operation of the scaler is during the 0 percent calibration time. The 0 percent calibration pulse is used to reset the system and load the 0 percent calibration number into the 0 percent calibration register. The falling edge of the data ready pulse starts the data clock which loads the output register with the eight least significant bits of the 0 percent value and the accumulator with the 0 percent data. To minimize gating requirements, the system then processes the 0 percent calibration data although the results of the processing are not used.

The second type operation is during the 100 percent calibration time. This operation is to generate a 100 percent calibration correction factor. The falling edge of the data ready pulse starts the data clock which loads the output register with the eight least significant bits of the 100 percent calibration data and loads the accumulator with the 100 percent calibration data. Then, after subtracting the 0 percent calibration, the 100 percent calibration value is divided by 253. The result of the division is stored in the 100 percent calibration correction factor register.

The third type operation occurs during the rest of the data times until the next 0 percent calibration pulse resets the system. This operation is to generate the processed, scaled data. The falling edge of the data ready pulse starts the data clock which loads the output register with the eight least significant bits of the input data and loads the accumulator with the input data. The reason the output register is loaded at this time is that the loading of the output register at the beginning of processing will be the same for all three types of operations, resulting in a decrease in the number of gates required for the scaler. Zero percent calibration is subtracted from the data, then the result is divided by the 100 percent calibration factor. One is added to the result of the division, and the sum is the final processed data which is loaded into the output register.

The equation for the processing of the data can be written as:

$$\text{Processed output data} = \frac{\text{data - 0 percent cal}}{\text{100 percent cal correction factor}} + 1$$

$$= \frac{\text{data - 0 percent cal}}{\frac{\text{100 percent cal - 0 percent cal}}{253}} + 1$$

$$= \frac{\text{data - 0 percent cal}}{\text{100 percent cal - 0 percent cal}} \times 253 + 1$$

The +1 is needed to meet requirements 3 and 4 on the output data. To meet requirements 2 and 5, circuitry is included to detect either of these conditions and force the output to the required number.

The arithmetics are performed using 12-bit two's complement type arithmetic (11 bits + sign bit). Nonrestoring type division is used. Fourteen clock pulses are required to process each 9-bit data word as follows:

Clock Pulse	Operation
1	Load input data into registers
2	Subtract 0 percent calibration from data
3-14	Divide data by 253 or 100 percent calibration correction factor
14	Load result into output register if data word or into 100 percent calibration correction factor register

If the input data is less than zero calibration, processing stops at clock pulse two. The clock is allowed to run to 16 because of requirements for data buffer clock. The clock is divided by two for the data buffer clock or a total of eight clock pulses. The scaler as shown in figures 4-7 and 4-8 uses 37 integrated circuits and two discrete components.

4.3 DATA BUFFER AND MDM INTERFACE

The data buffer and MDM interface circuits provide digital storage of a frame of PAM data which has been converted and scaled, as described in sections 4.1 and 4.2, and output the data to the MDM upon request. Timing circuits for the MDM interface detect readout commands from the MDM, format the data and shift this data as a block to the MDM at a 1-MHz bit rate.

4.3.1 Data Buffer and MDM Output

The block diagram of the data buffer and MDM output circuit is shown in figure 4-10. The schematics are shown in figures 4-11, 4-12, and 4-13. This circuit is typical of two required in the EVA signal processor. The buffer input is controlled by signals from the synchronizer section of the decom and a shift clock signal generated in the digital automatic scaling circuit. The select gates provide eight bits of data from the scaling circuit each PAM word time except one. The word that is not provided by the scaling circuit is the second channel of the frame sync pulse. Since the scaling circuit outputs data one word time after the digitizer, the zero calibration pulse provides the proper timing to select eight bits of status data to take the place of the second channel of the frame sync pulse. The zero calibration pulse gated by the data ready pulse is used to toggle the flip flop which controls the clock gates of the two 240-bit shift registers. Therefore, the status bits are the first eight bits in the stored data format followed by the zero calibration data.

The data ready pulse from the synchronizer loads the selected data into the 8-bit shift register and eight clock pulses generated in the scaling circuit shift the data into one of the 240-bit shift registers. During the time one frame is being shifted into one 240-bit shift register, the previous frame of data is available to be shifted out of the other 240-bit shift register when the MDM requests data. The signal message discrete, generated by the MDM, is present during a block transfer and inhibits the gated zero calibration pulse from toggling the shift control flip flop. This prevents the shift register switching during a block transfer.

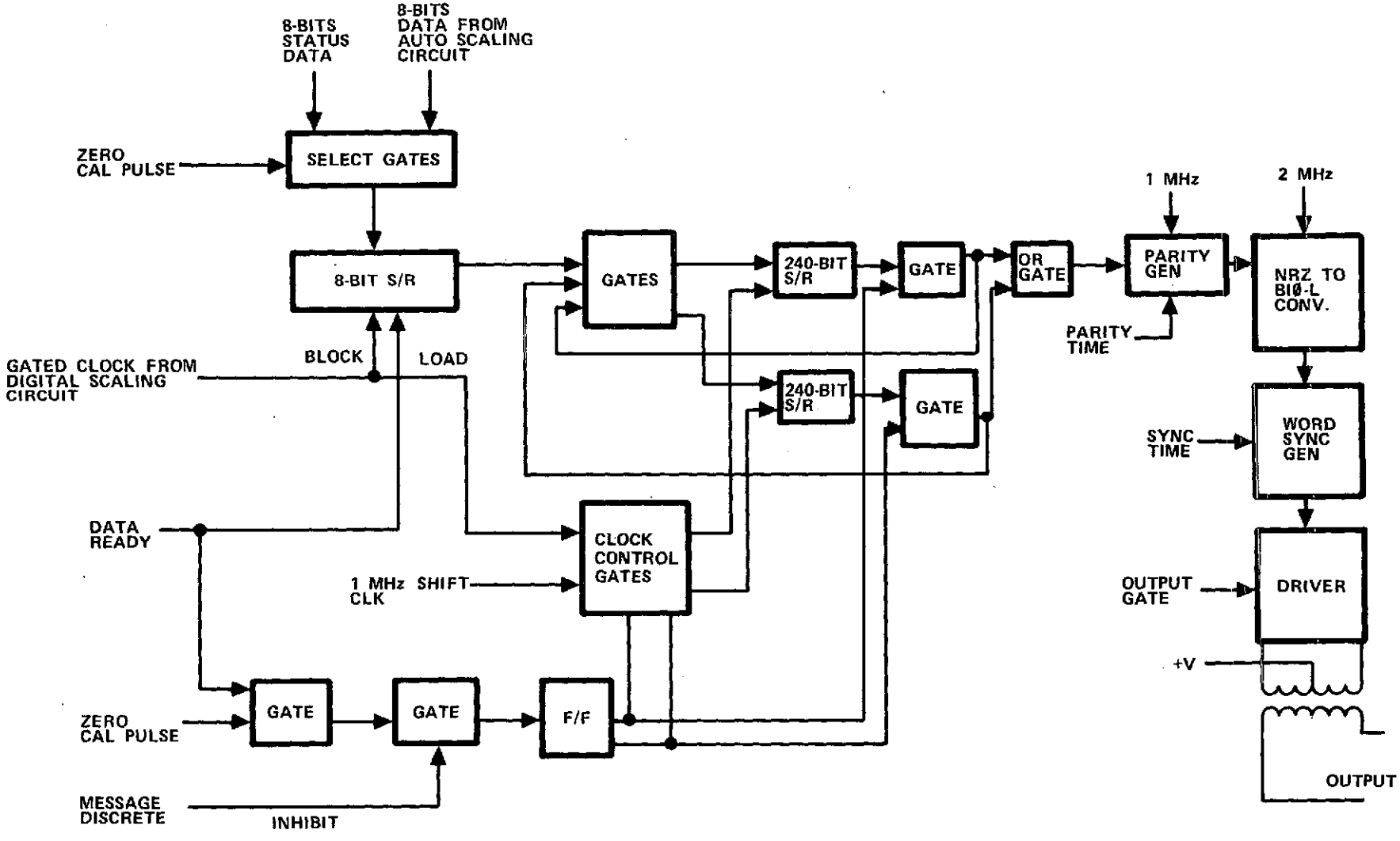


Figure 4-10. – Data buffer block diagram.

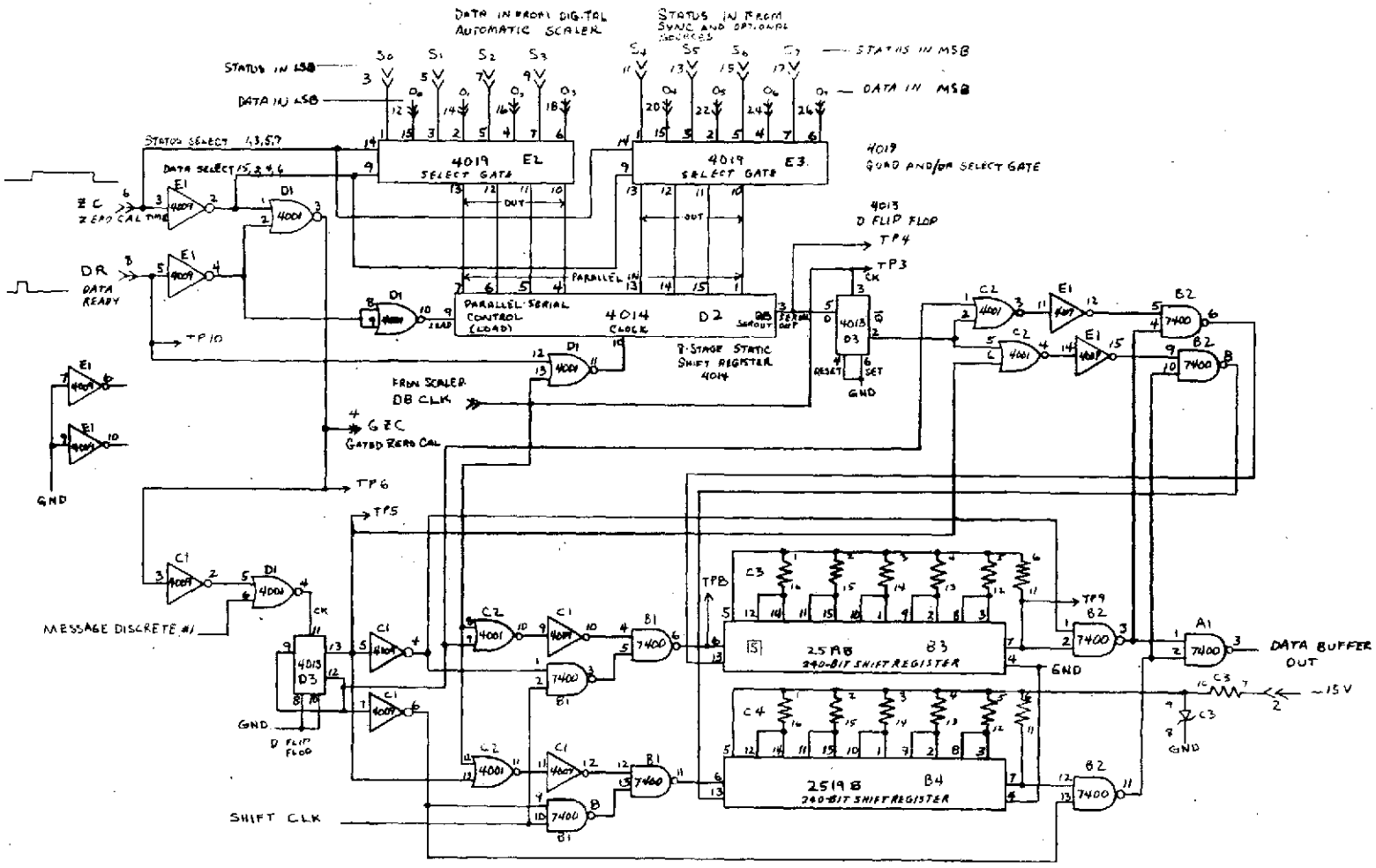


Figure 4-11. – Data buffer schematic.

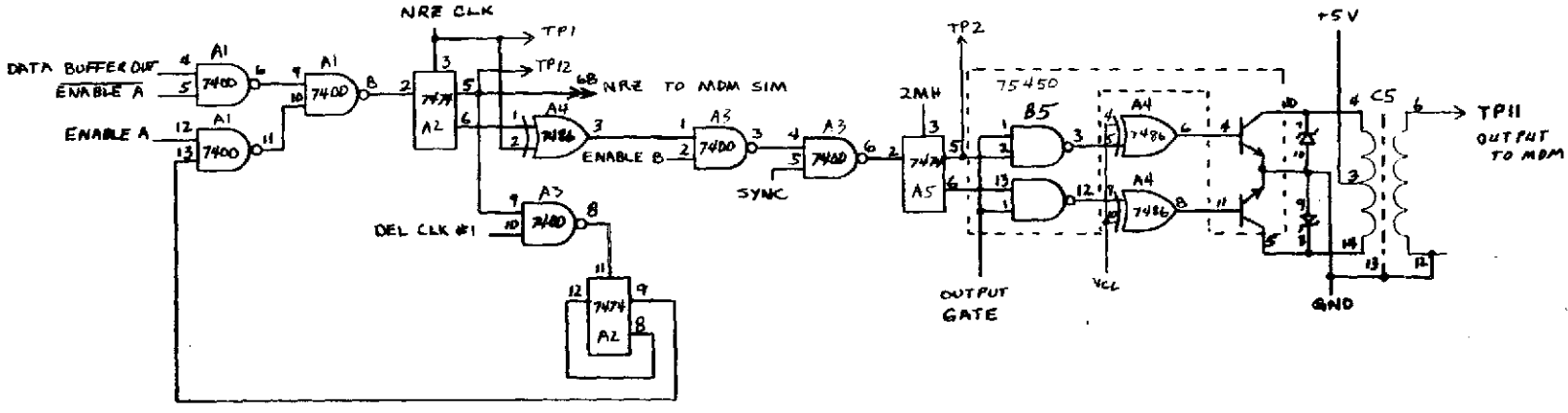


Figure 4-12. – Parity generator and data converter schematic.

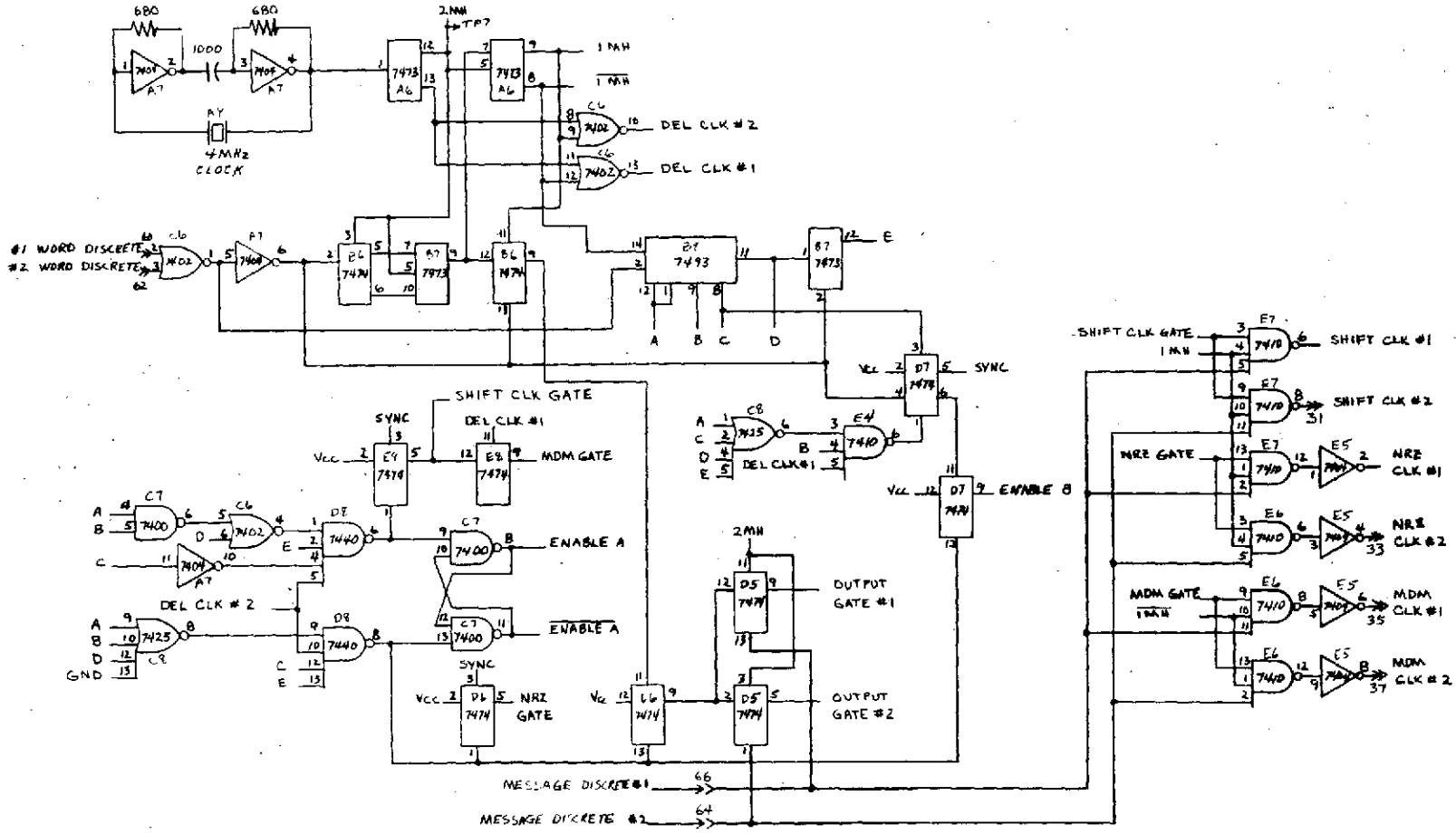


Figure 4-13. - Data buffer timing schematic.

When data is being shifted out to the MDM from one shift register, the data is also gated back into the same shift register to provide nondestructive readout. This feature allows the MDM to sample the data buffer at rates higher than the PAM frame rate.

The data from the 240-bit shift register is formatted as shown in figure 4-14. There are two 8-bit PAM words in each MDM word, and there are a total of 15 MDM words in one block transfer. The MDM interface timing provides 16 clock pulses each MDM word time to the clock control gates of the 240-bit shift registers. Other timing signals provide the word sync pulse width and timing to check and add parity as the seventeenth bit after word sync. The word sync details are shown in figure 4-15. The nonreturn-to-zero (NRZ) data is converted to biphase-level code and a gated driver couples the signal to a pulse transformer output. The biphase-level code is shown in figure 4-16.

4.3.2 MDM Interface Timing

The block diagram of figure 4-17 shows the timing circuits that are shared between the two PAM decommutators in the EVA signal processor. The schematics are shown in figures 4-18, 4-19, and 4-20. A 4-MHz crystal oscillator is used to provide the timing clock for the MDM interface. A divider provides 2 MHz which is used to detect a word discrete level change within 1/2 microsecond of the actual change. The word discrete and message discrete timing relationship is shown in figure 4-21. A digital delay circuit provides the proper response delay required by the MDM which is also shown in figure 4-21. The delay circuit also

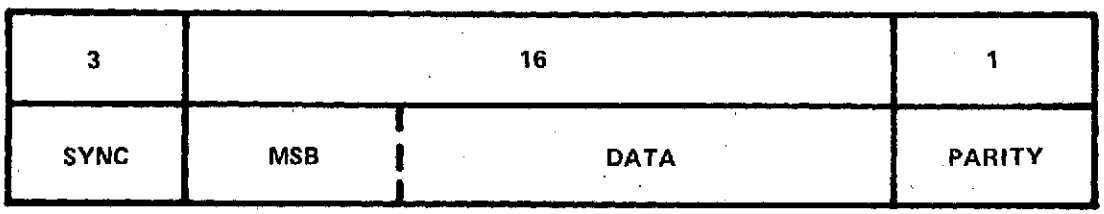


Figure 4-14. – Serial word format.

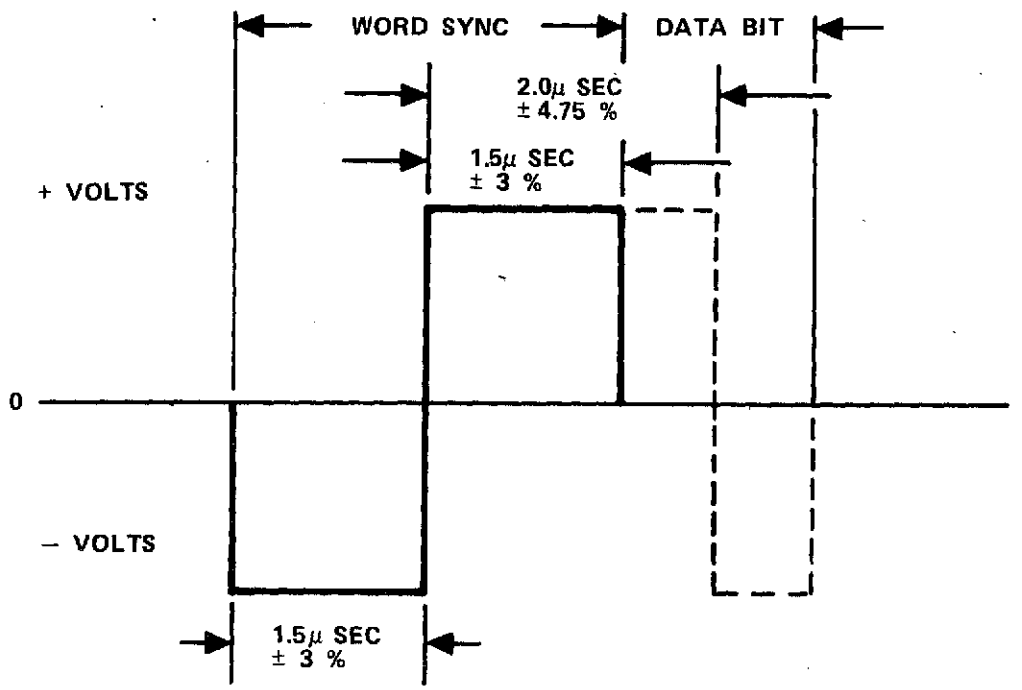
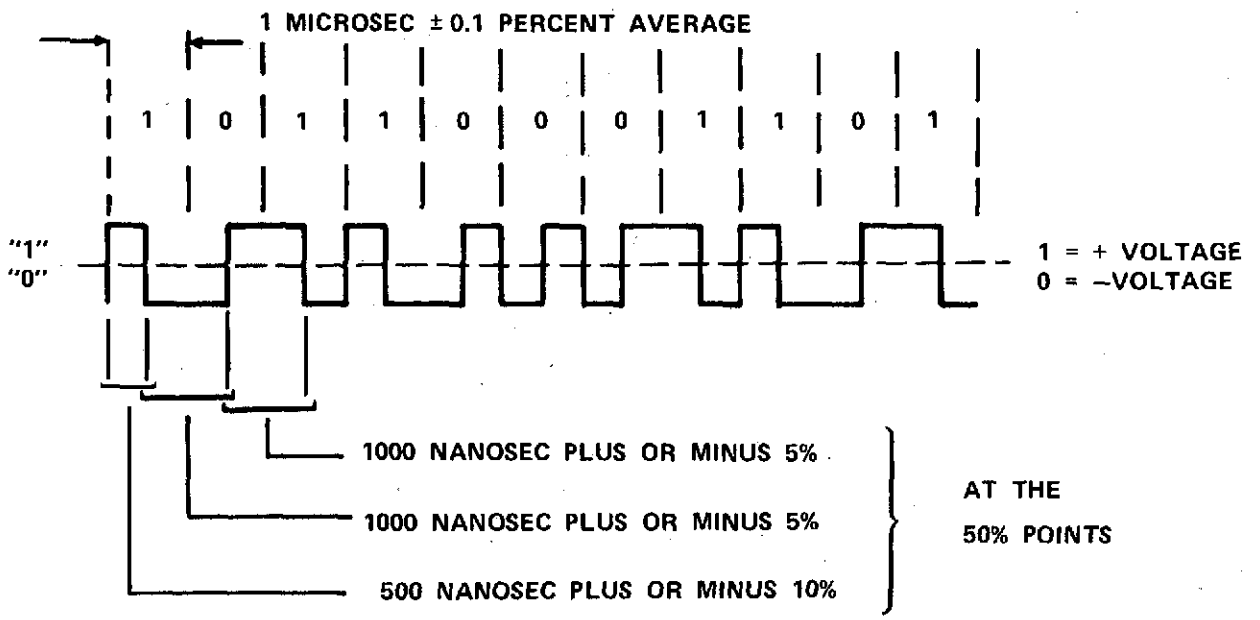


Figure 4-15. – Data word sync nonvalid Manchester code.



NOTE:

BI - PHASE LEVEL (MANCHESTER II)

"1" REPRESENTED BY 10
"0" REPRESENTED BY 01
} FOR DATA

"1" REPRESENTED BY 01
"0" REPRESENTED BY 10
} FOR $\overline{\text{DATA}}$

Figure 4-16. – Data code.

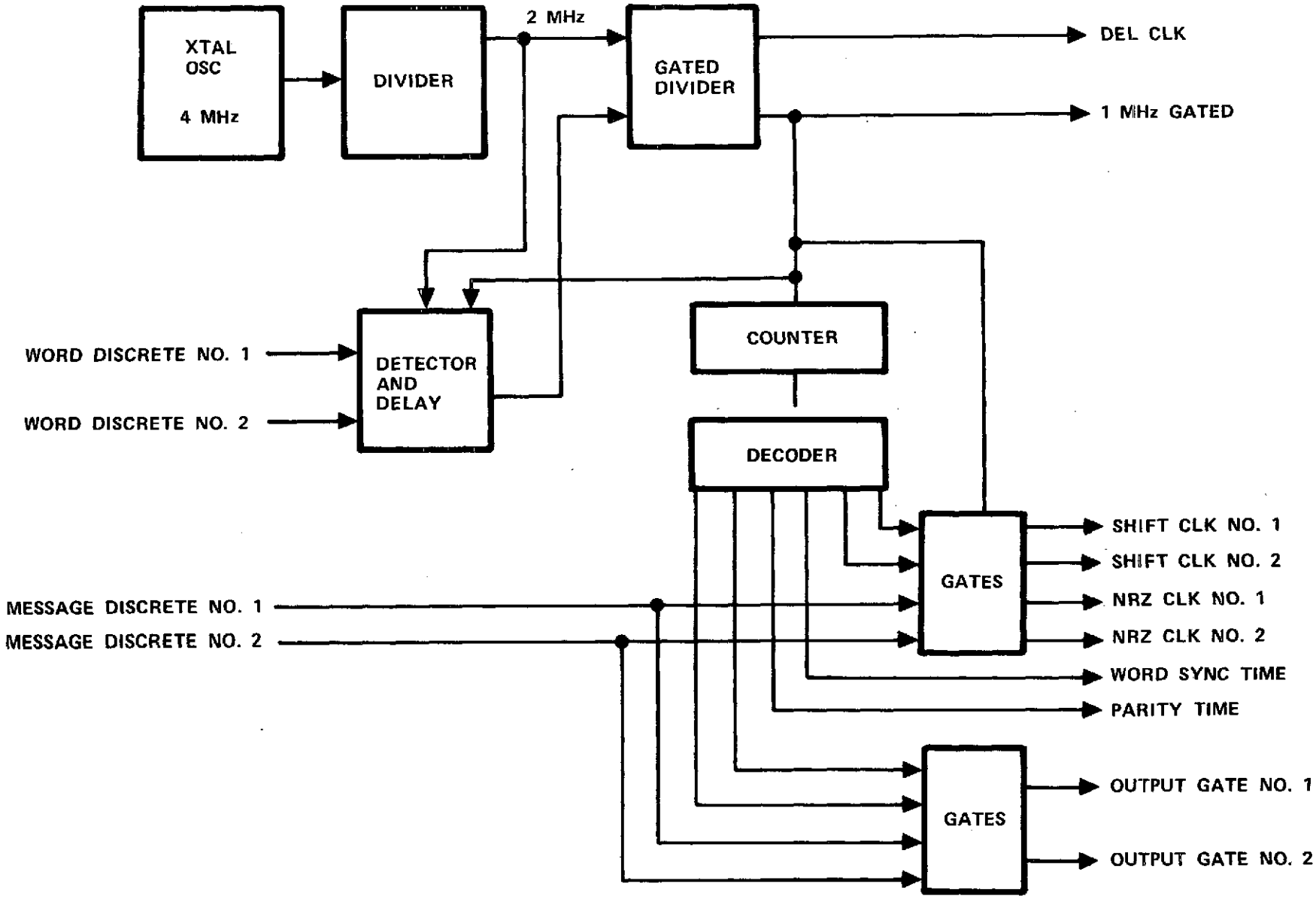


Figure 4-17. – MDM interface timing block diagram.

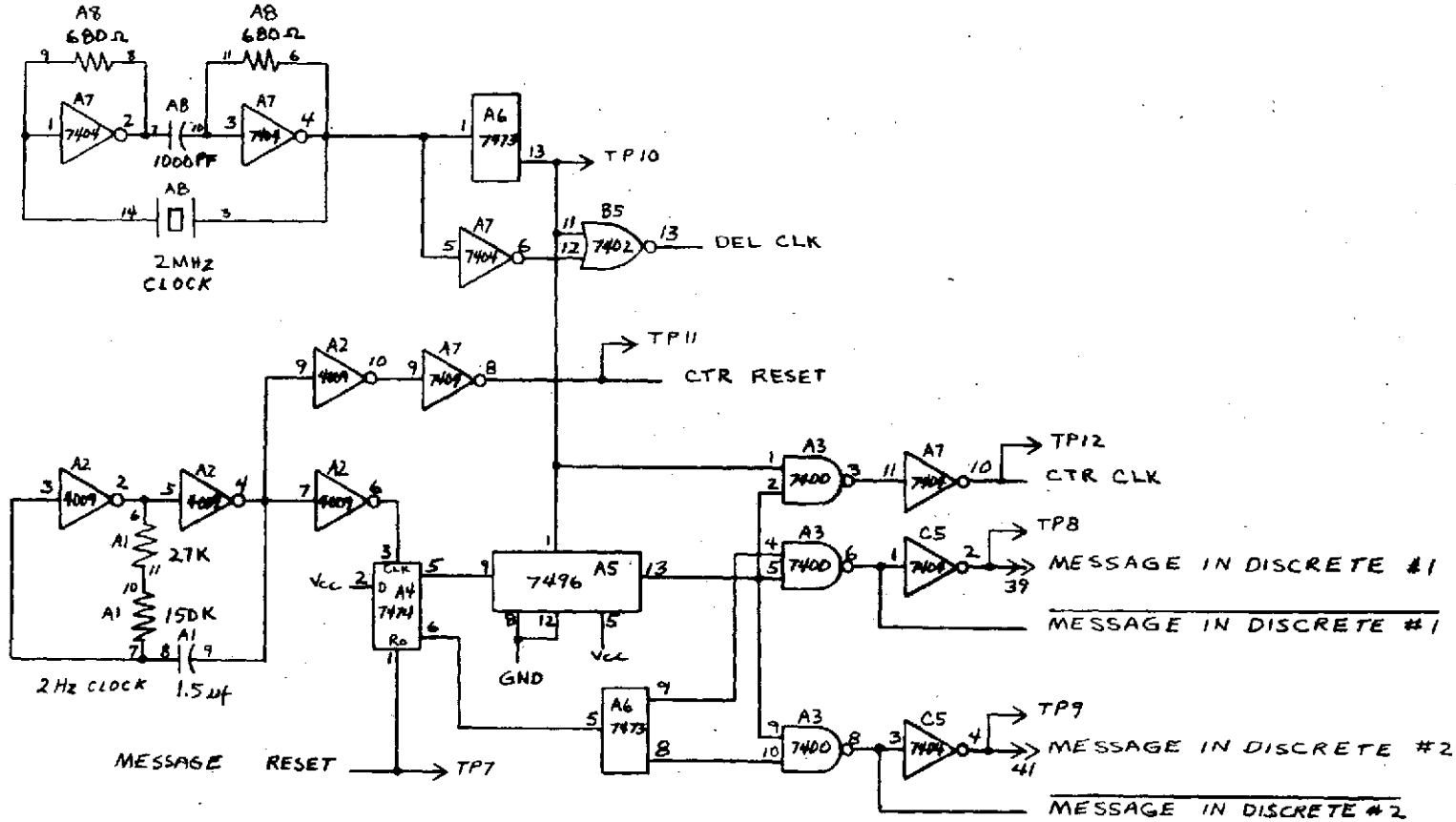


Figure 4-18. — MDM simulator clock schematic.

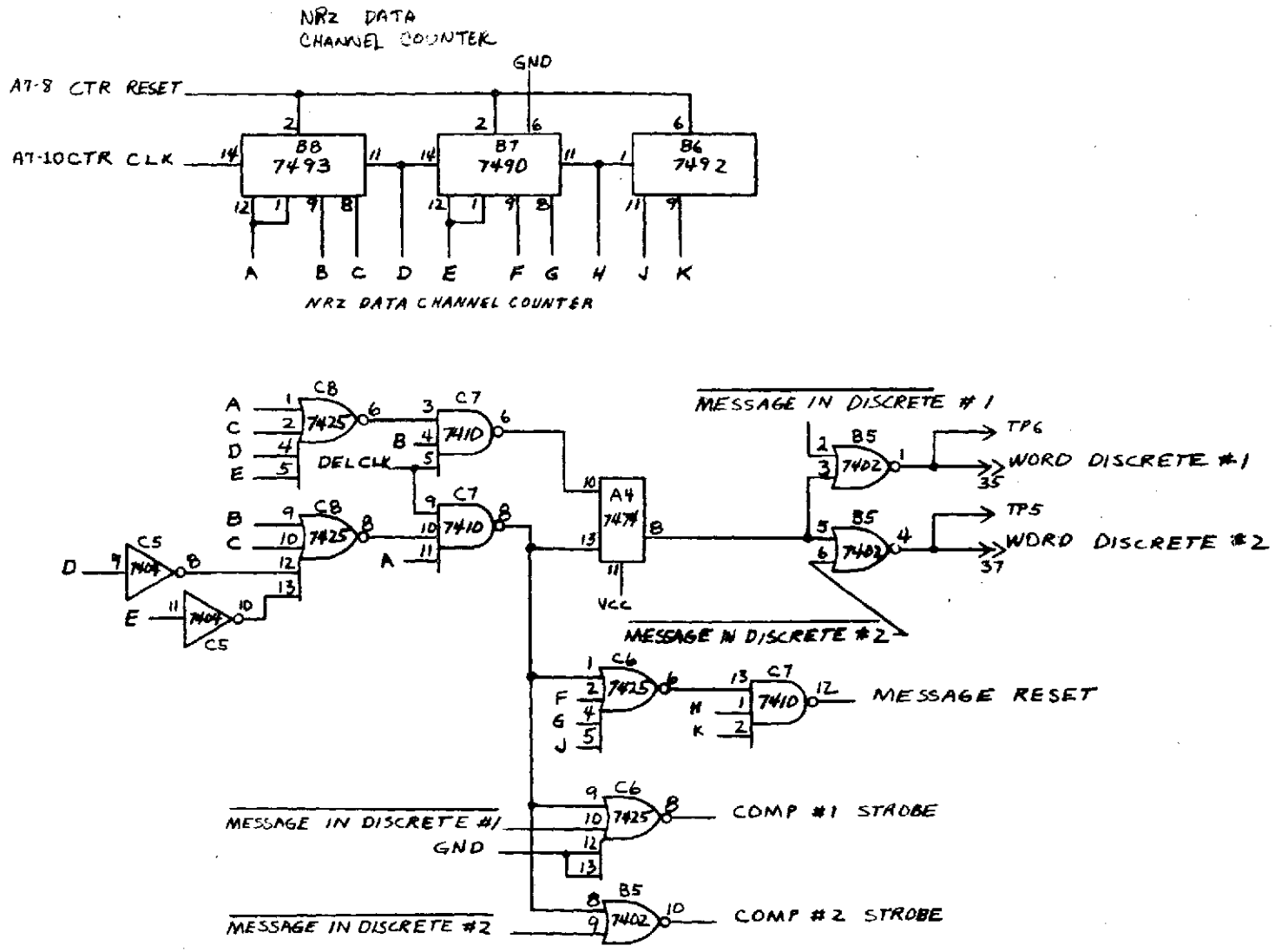


Figure 4-19. — MDM simulator control schematic.

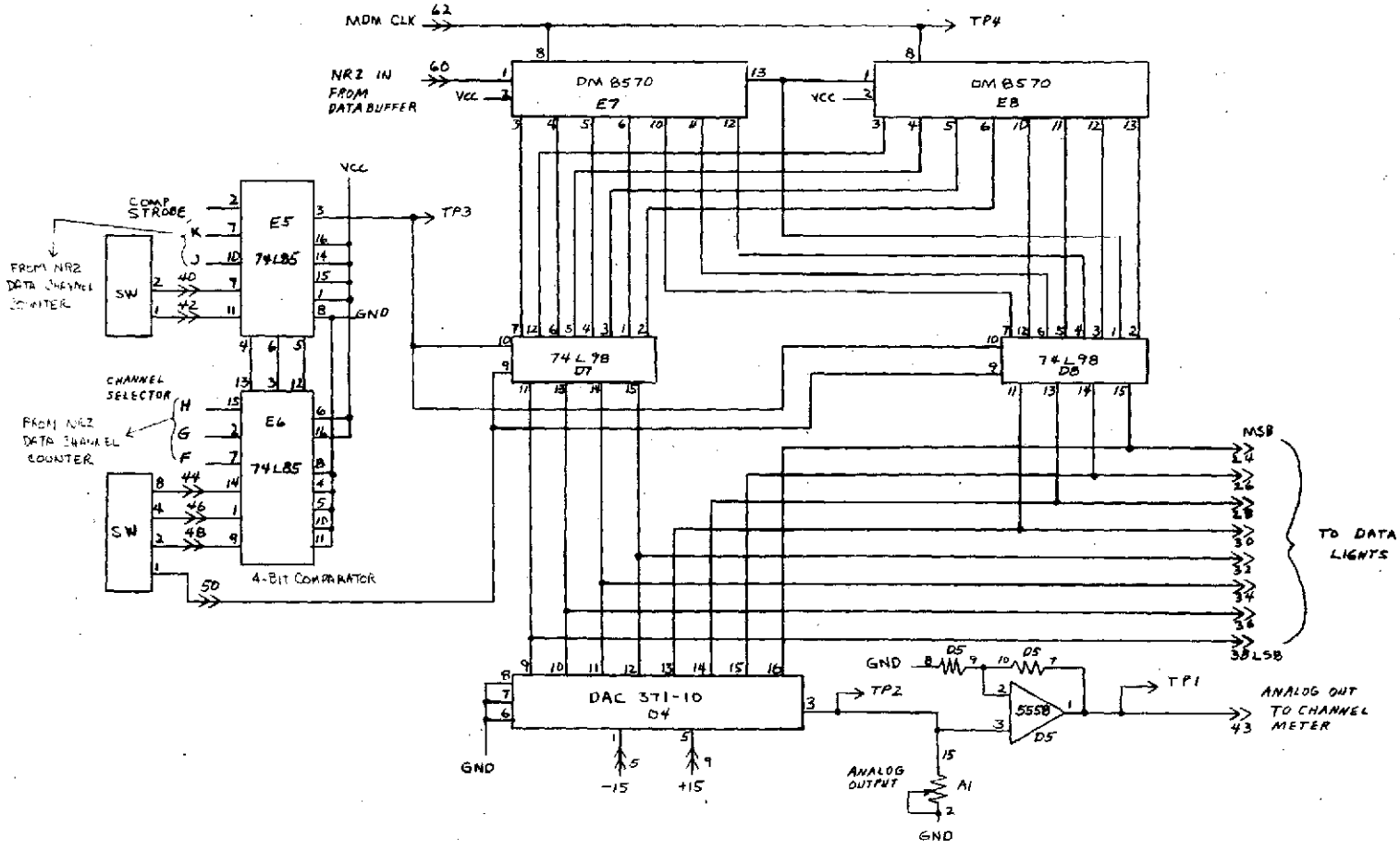


Figure 4-20. – MDM simulator data display schematic.

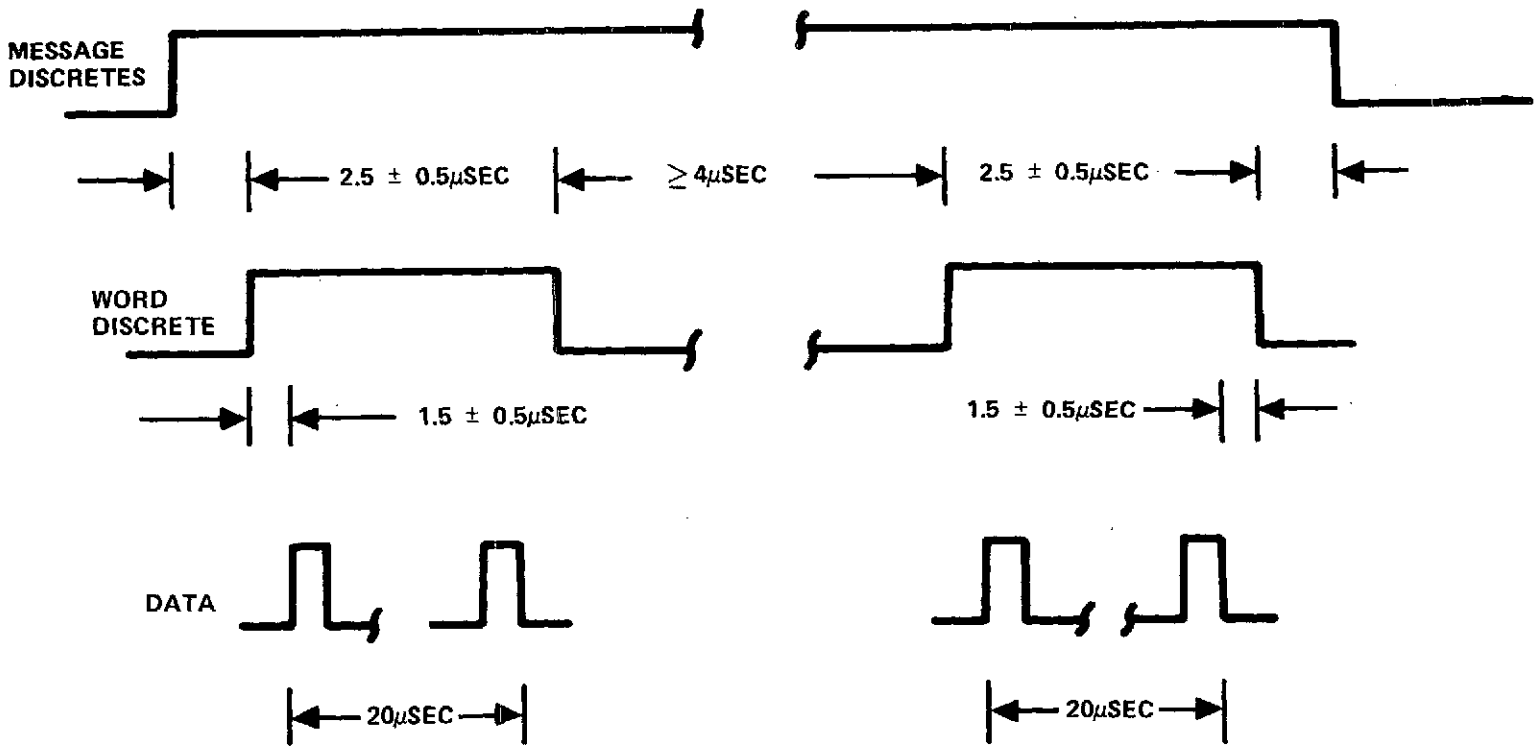


Figure 4-21. – Serial channel data transfer.

enables a gated divider to provide 1 MHz to a counter circuit. The counter states are decoded to provide the proper time sequence and duration for the word sync, data buffer output, shift clock, parity bit time, and the NRZ clock. The message discrete signals from the MDM provide the gate enable to the proper PAM decom data buffer and MDM interface.

5.0 PERFORMANCE

The laboratory version of the PAM decommutator portion of the Shuttle EVA signal processor meets or exceeds all specifications listed in table I.

The test configuration used to obtain data is shown in figure 5-1. A summary of the performance of the decom is portrayed in figure 5-2.

The system linearity is shown in figure 5-3. Figure 5-4 shows how noise affects accuracy of the channel outputs. In figure 5-5 it is shown that noise affects the high-frequency deviation channels first, when automatic scaling is not used.

Several synchronization schemes were used. The synchronization data obtained is shown plotted in figure 5-6. The characteristics of the channel rate phase locking circuits are shown in figure 5-7.

As can be seen from the graphs in figures 5-2 and 5-4, the ±0.5 percent accuracy of channel amplitude is not maintained with a discriminator output signal-to-noise ratio of less than 36 dB. Also, even though the decom remains partially locked below a discriminator output SNR of 10 dB, the data itself varies so much that it may be of little value.

The digital automatic scaling section compensates very well for errors in gain or level with a high signal-to-noise ratio signal.

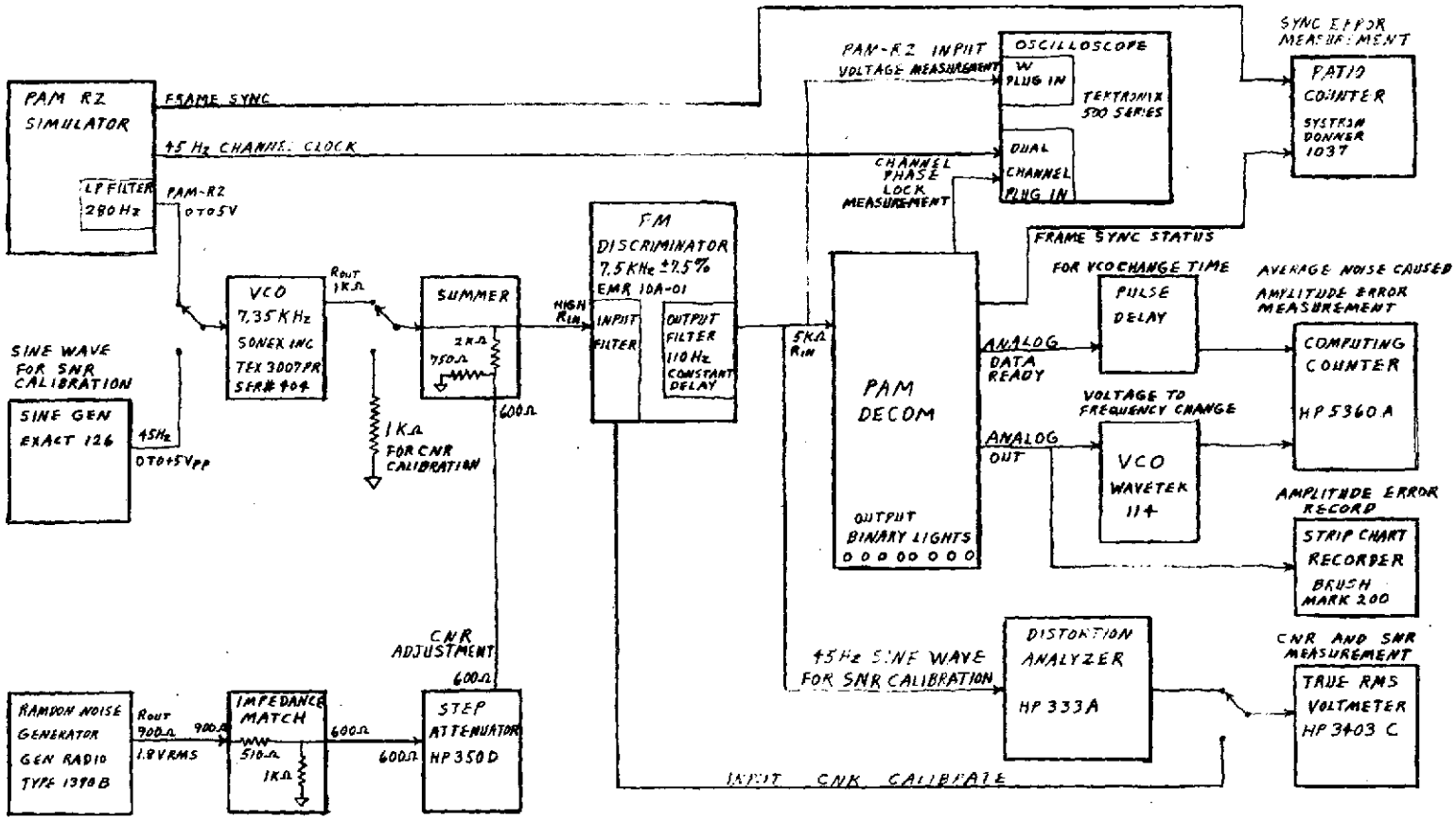


Figure 5-1. — PAM decommutator evaluation test configuration.

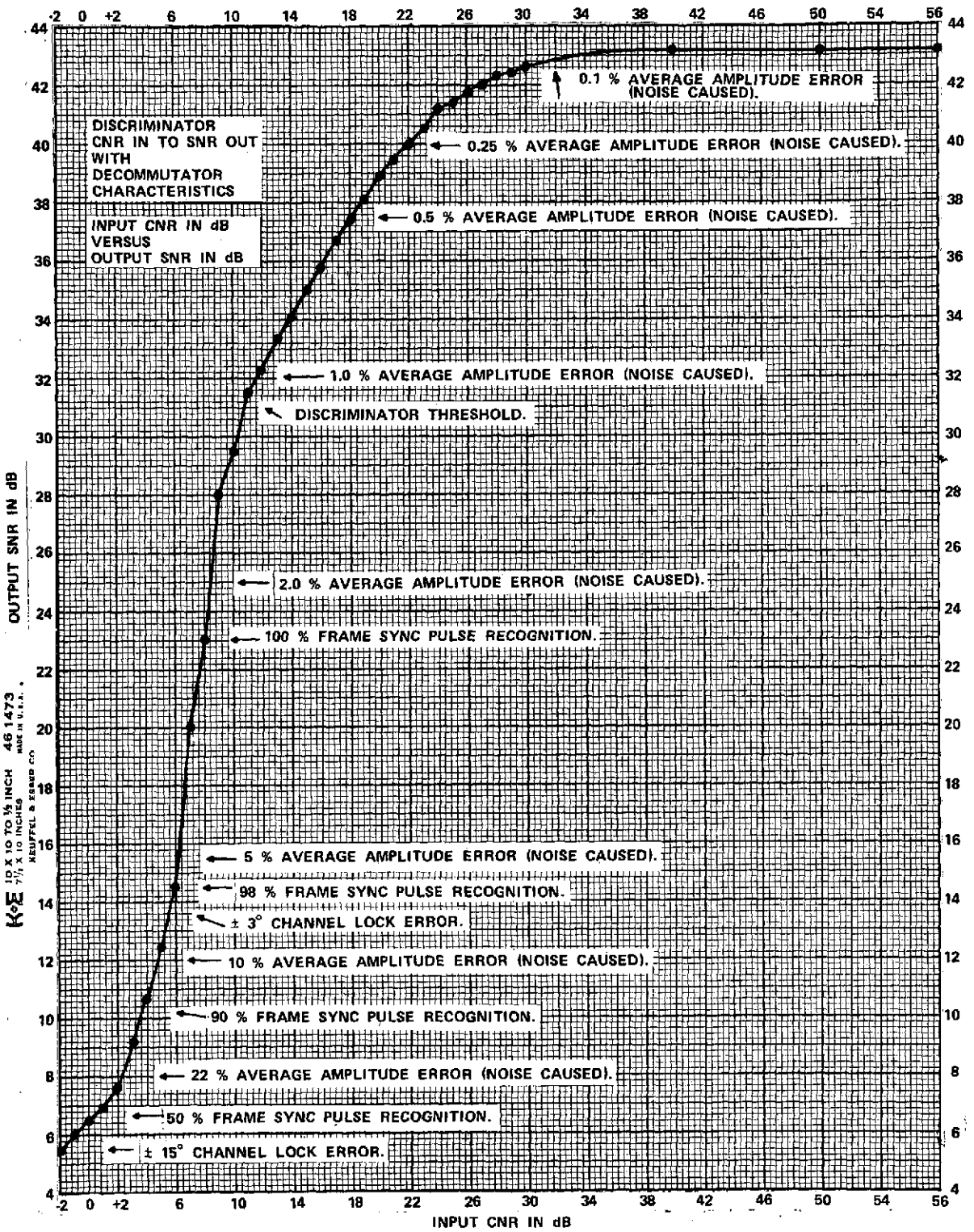


Figure 5-2. – Discriminator CNR "in" to SNR "out" with decommutator characteristic graph.

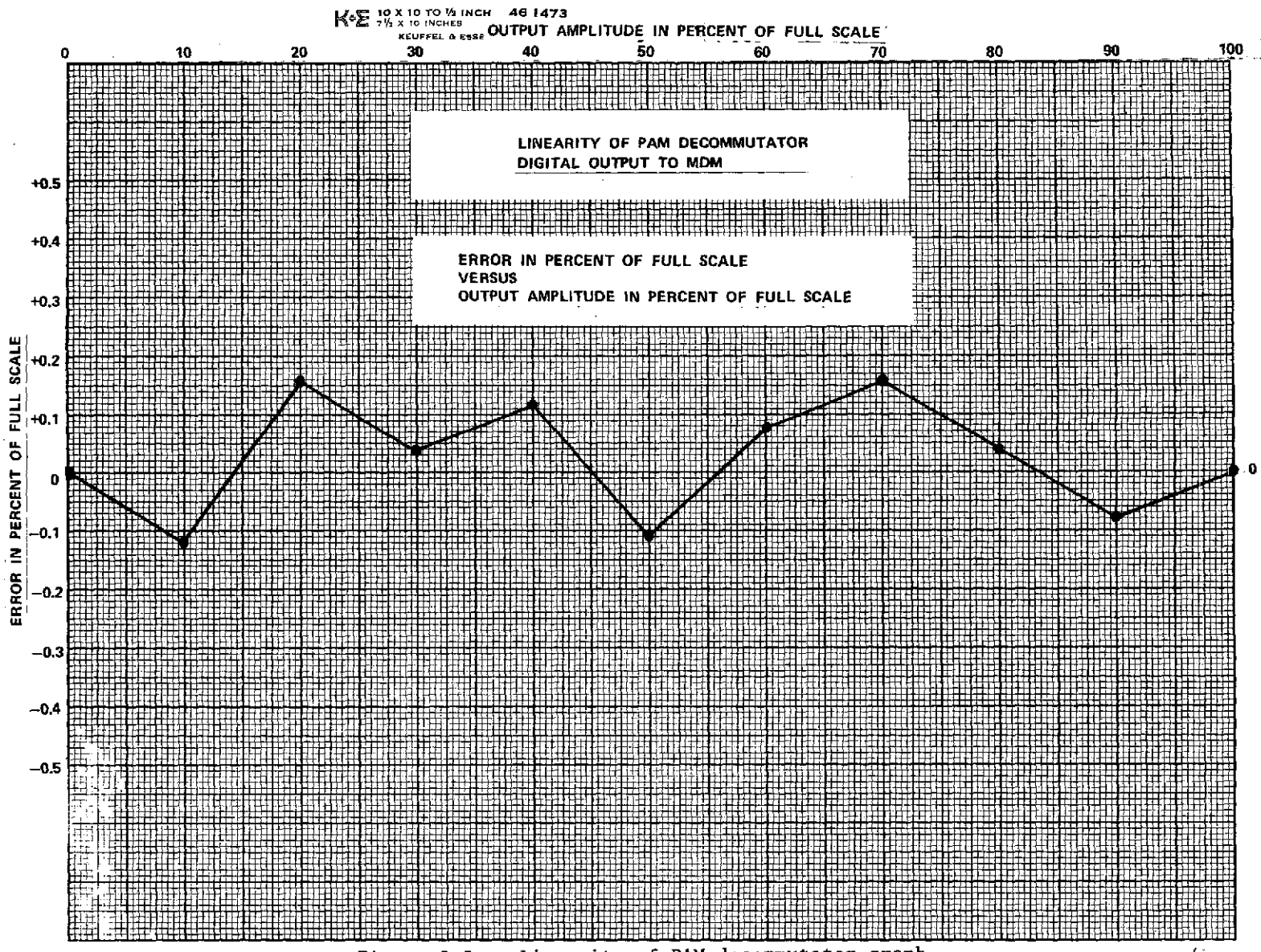


Figure 5-3. – Linearity of PAM decommutator graph.

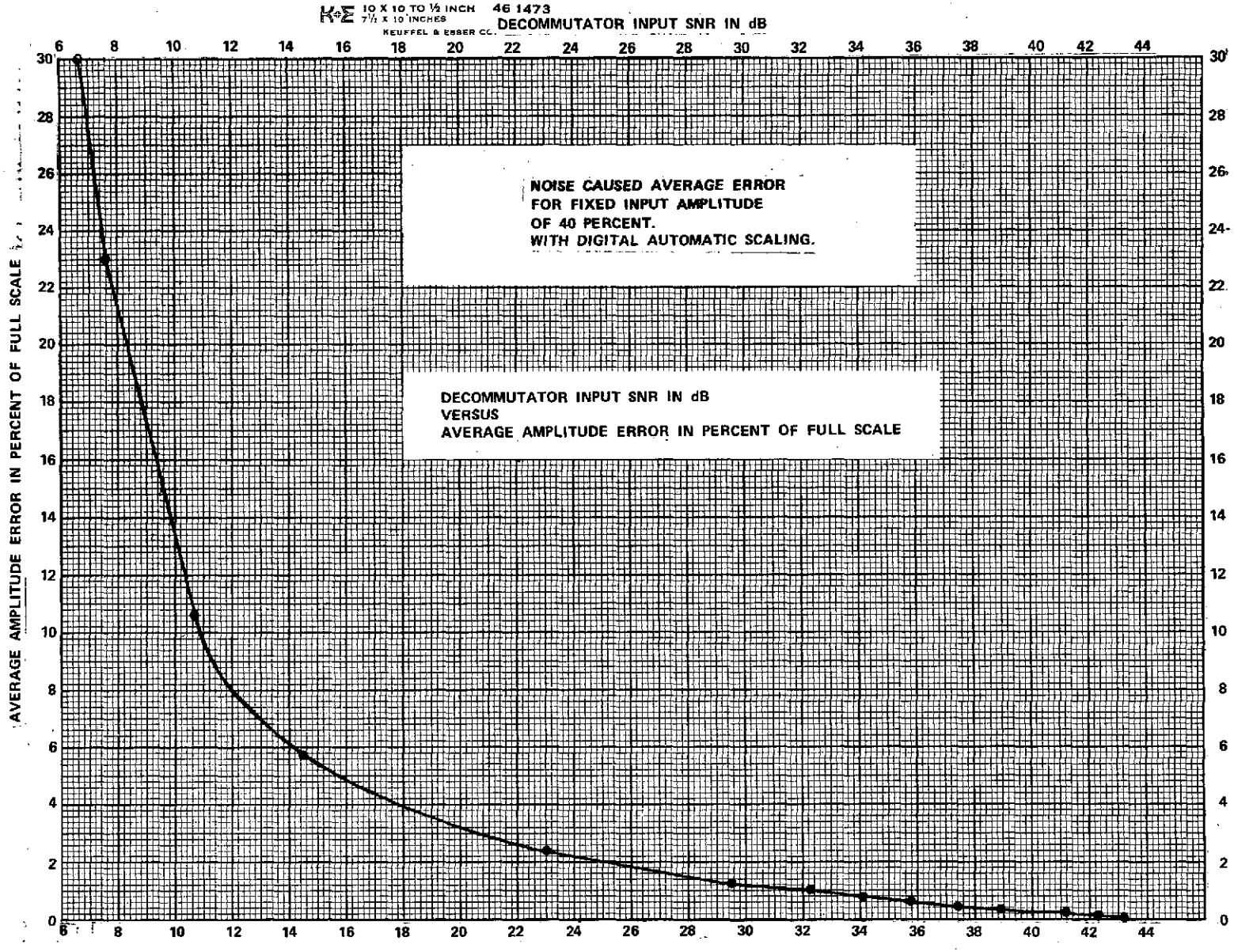


Figure 5-4. – Noise-caused average error graph.

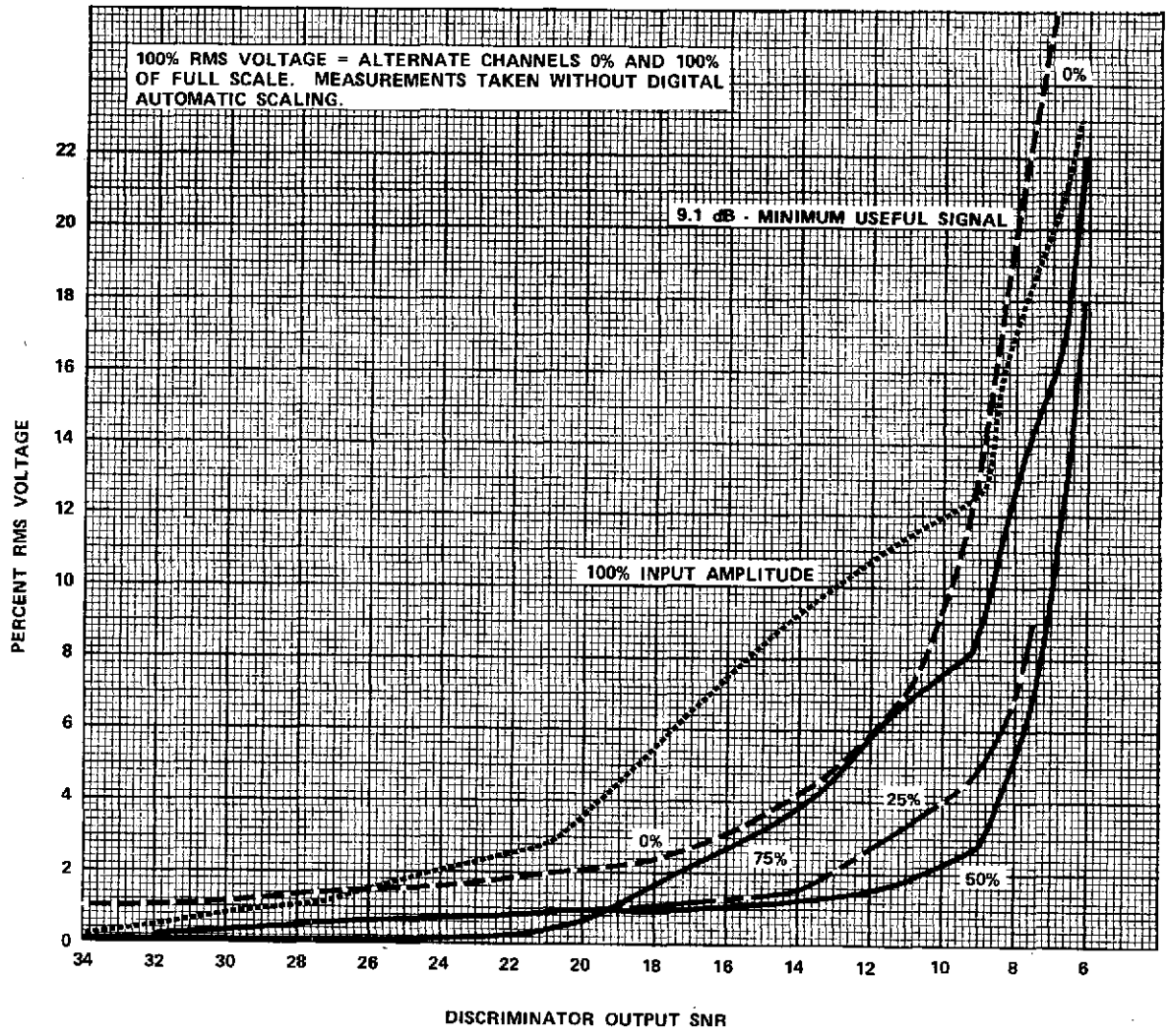


Figure 5-5. – Noise-caused rms voltage for fixed input amplitude channels.

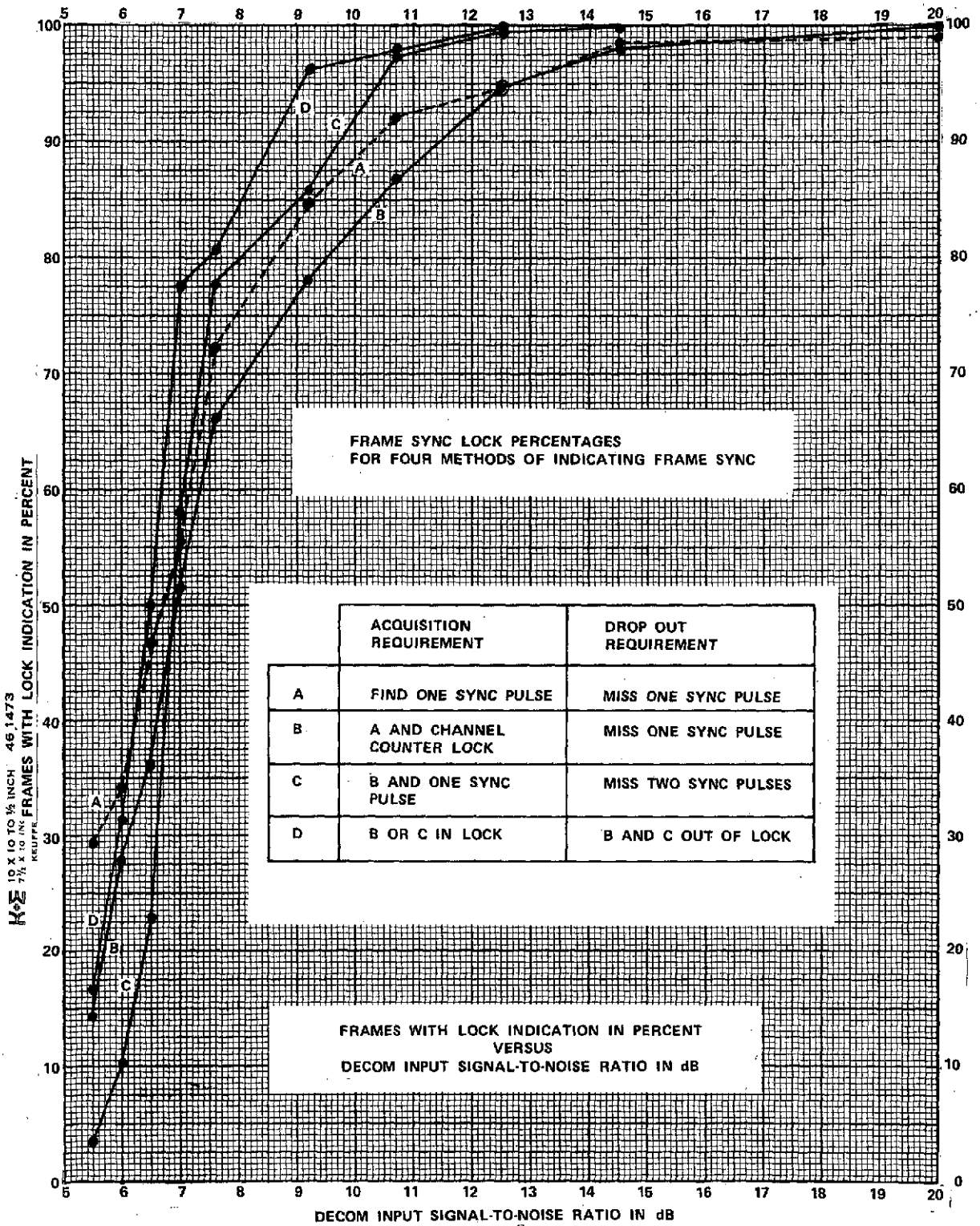


Figure 5-6. — Frame sync lock percentages graph.

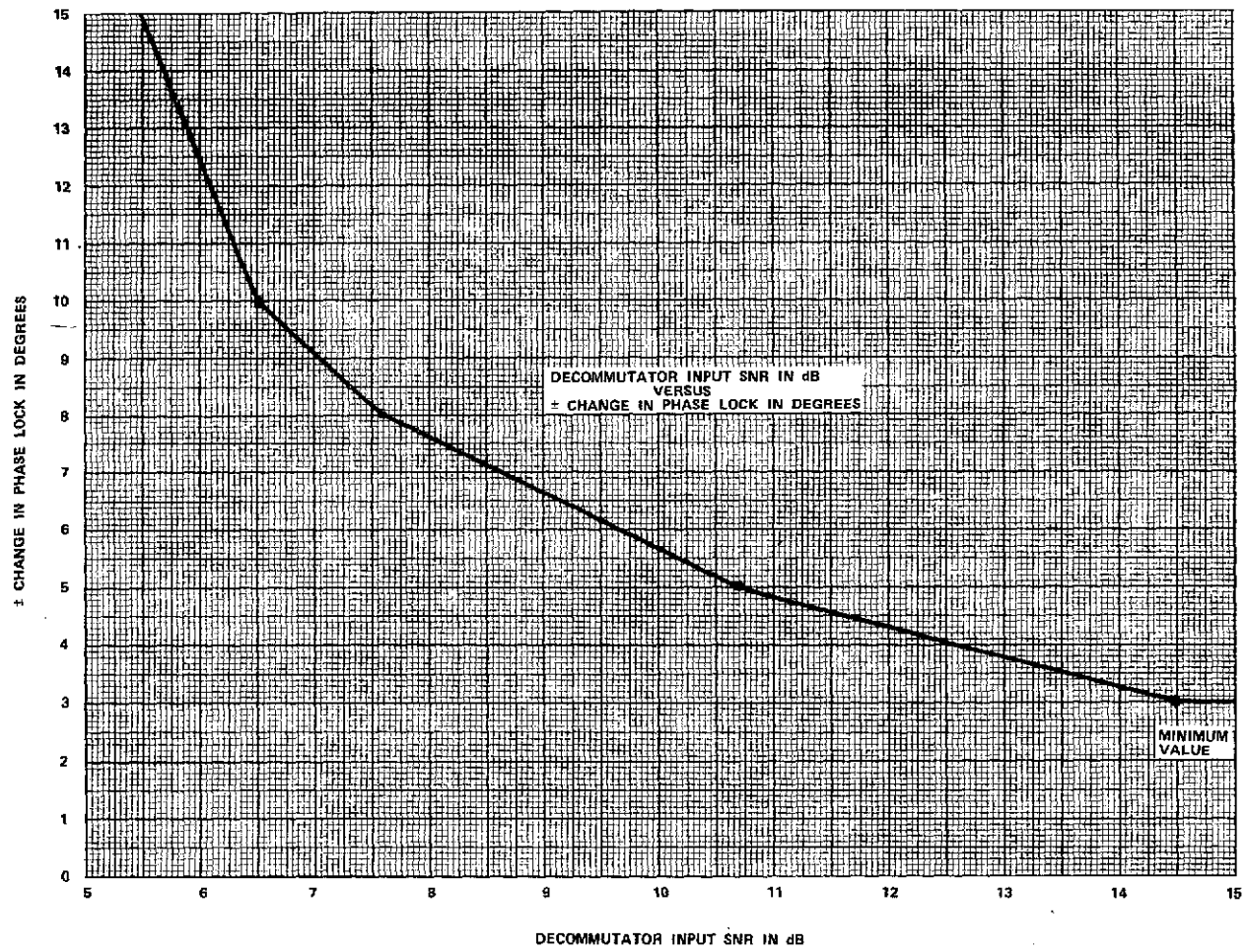


Figure 5-7. – Change in phase between incoming channel rate and channel locking oscillator graph.

When the signal-to-noise ratio at the decom input decreases below about 22 dB, the effect of the digital automatic scaling section is to decrease the accuracy of all amplitudes. This is because of the rapid deterioration of the high deviation calibration signals below FM threshold.

6.0 CONCLUSIONS

The PAM decommutator portion of the Shuttle EVA signal processor discussed in this report demonstrates one approach to the design and has served as a test model to provide performance data.

The data obtained shows accuracies obtained with various signal-to-noise ratios. Just how each principal function behaves with the signal-to-noise ratio is readily determined from the graphs.

APPENDIX

CONFIGURATION

BOARD LAYOUT AND TEST POINT FUNCTION

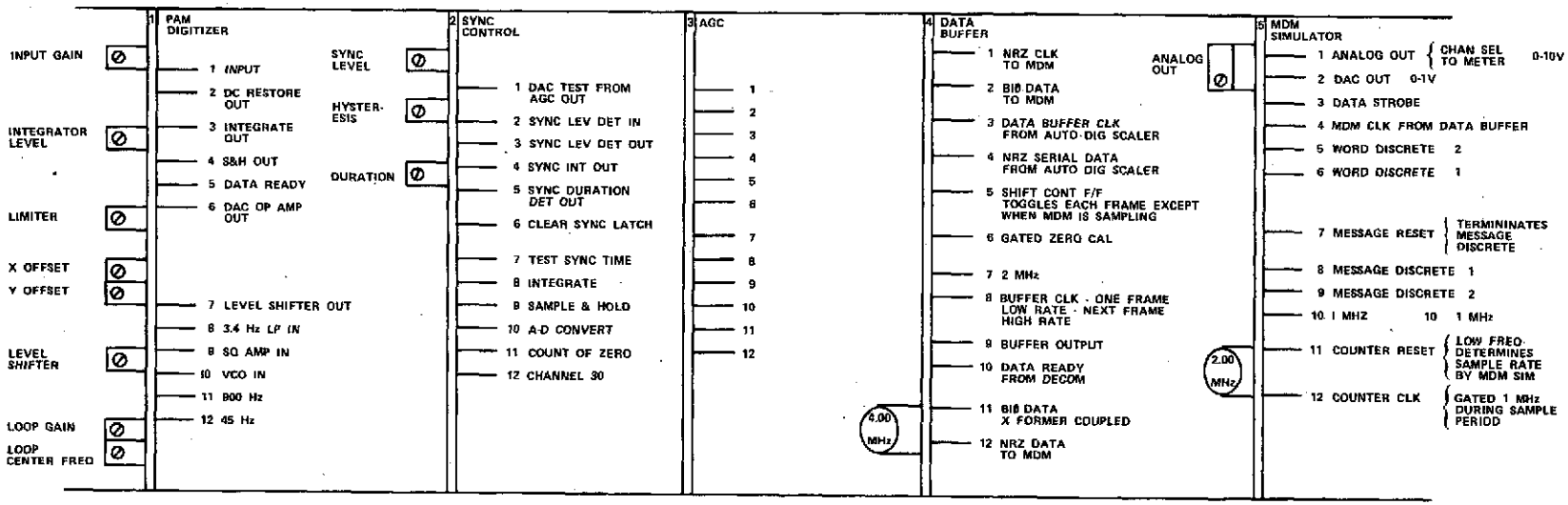


Figure A-1. — Board position and test point function.

NAME DIGITIZER & PLL **LOCATION** XA2 **BOARD** 1

BOARD TO BOARD CONNECTIONS

	FROM						FROM				
PIN	BOARD	PIN	IN	OUT	FUNCTION	PIN	BOARD	PIN	IN	OUT	FUNCTION
1	BUS		V		+5V Vcc	37					
2	BUS		V		+5V Vcc	38					
3	BUS		V		+5V Vcc	39					
4						40					
5	BUS		V		+15V	41					
6	BUS		V		+15V	42					
7						43	NC			V	TEST DAC #1 OUT
8	BUS		V		-15V	44					
9	BUS		V		-15V	45					
10	2	10		V	-5.6V	46					
11	2	11		V	+5.6V	47					
12	FRONT PANEL	IN	V		ANALOG PAM INPUT	48					
13	FRONT PANEL	GND	V		" SHIELD	49					
14						50					
15	2	15	V		LP FILTER OUT	51					
16	2	16	E21		A-D CONVERT TIME	52					
17	2	17	J41		SAMPLE AND HOLD TIME	53	3 4	53 8		V	DATA READY
18	2	18	H40		INTEGRATE TIME	54					
19						55	3	55		V	MSB BIT 1 DATA
20	2	20	J1		900 Hz DECODED	56					
21	2	21	J2		900 Hz DECODED	57	3	57		V	BIT 2 DATA
22	2	22	J3		900 Hz DECODED	58					
23	2	23	J4		900 Hz DECODED	59	3	59		V	BIT 3 DATA
24	2	24	J5		900 Hz DECODED	60					
25	2	25	J6		900 Hz DECODED	61	3	61		V	BIT 4 DATA
26	2	26	J7		900 Hz DECODED	62					
27	2	27	K8		900 Hz DECODED	63	3	63		V	BIT 5 DATA
28	2	28	K7		900 Hz DECODED	64					
29	2	29	V		$\overline{45Hz}$	65	3	65		V	BIT 6 DATA
30	2	30	V		45Hz	66					
31	2	31	V		900Hz	67	3	67		V	BIT 7 DATA
32						68	BUS		V		GND
33						69	3	69		V	BIT 8 DATA
34						70	BUS		V		GND
35						71	3	71			LSB BIT 9 DATA
36						72	BUS		V	V	GND

NAME SYNC CONTROL **LOCATION** XA4 **BOARD** 2

BOARD TO BOARD CONNECTIONS

	FROM						FROM				
PIN	BOARD	PIN	IN	OUT	FUNCTION	PIN	BOARD	PIN	IN	OUT	FUNCTION
1	BUS		V		+5V Vcc	37	3	9	V		BIT 4
2	BUS		V		+5V Vcc	38	3	11	V		BIT 5
3	BUS		V		+5V Vcc	39	3	13	V		BIT 6
4						40	3	15	V		BIT 7 ADS OUT TO
5	BUS		V		+15V	41	3	17	V		LSB BIT 8 TEST DAC
6	BUS		V		+15V	42					
7						43	NC			V	ADS TEST DAC OUT
8	BUS		V		-15V	44					
9	BUS		V		-15V	45					
10	1	10	V		-5.6V	46					
11	1	11			+5.6V	47					
12	4	6		V	0 percent CAL TIME	48					
13						49					
14						50					
15	1	15	V		LP FILTER OUT	51					
16	1	16	E7-15*		A-D CONVERT TIME	52					
17	1	17	E7-13*		SAMPLE AND HOLD TIME	53					
18	1	18	C6-4		INTEGRATE TIME	54	CONTROL PANEL	LT 1			SYNC STATUS A
19						55					
20	1	20	V		900Hz DECODED	56	CONT PANEL	LT 2			SYNC STATUS B
21	1	21	V		900Hz DECODED	57					
22	1	22	V		900Hz DECODED	58	CONT PANEL	LT 3			SYNC STATUS C
23	1	23	V		900Hz DECODED	59					
24	1	24	V		900Hz DECODED	60	CONT PANEL	LT 4			SYNC STATUS D
25	1	25	V		900Hz DECODED	61					
26	1	26	V		900Hz DECODED	62					
27	1	27	V		900Hz DECODED	63					
28	1	28	V		900Hz DECODED	64					
29	1	29	V		$\overline{45Hz}$	65					
30	1	30	V		45Hz	66					
31	1	31	V		900Hz	67					
32						68					
33						69	BUS		V		GND
34	3	3	V		MSB BIT 1 ADS OUT TO	70	BUS		V		GND
35	3	5	V		BIT 2 TEST DAC	71	BUS		V		GND
36	3	7	V		BIT 3 TEST DAC	72	BUS		V		GND

NAME DIGITAL AUTO SCALER **LOCATION** XA6 **BOARD** 3

BOARD TO BOARD CONNECTIONS

	FROM						FROM				
PIN	BOARD	PIN	IN	OUT	FUNCTION	PIN	BOARD	PIN	IN	OUT	FUNCTION
1	BUS		V		+5V Vcc	37					
2	BUS		V		+5V Vcc	38					
3	2/4	34/26		V	MSB BIT 1 SCALED DATA	39					
4						40					
5	2/4	35/24		V	BIT 2 SCALED DATA	41					
6						42					
7	2/4	36/22		V	BIT 3 SCALED DATA	43					
8						44					
9	2/4	37/20		V	BIT 4 SCALED DATA	45					
10						46					
11	2/4	38/18		V	BIT 5 SCALED DATA	47					
12						48					
13	2/4	39/16		V	BIT 6 SCALED DATA	49					
14						50					
15	2/4	40/14		V	BIT 7 SCALED DATA	51	4	4	V		GATED 0 percent CAL IN
16						52					
17	2/4	41/12		V	LSB BIT 8 SCALED DATA	53	1	53	V		DATA IN READY
18						54					
19	4	28		V	1.25 kHz CLOCK OUT	55	1	55	V		MSB BIT 1 RAW DATA
20						56					
21						57	1	57	V		BIT 2 RAW DATA
22						58					
23						59	1	59	V		BIT 3 RAW DATA
24						60					
25						61	1	61	V		BIT 4 RAW DATA
26						62					
27						63	1	63	V		BIT 5 RAW DATA
28						64					
29						65	1	65	V		BIT 6 RAW DATA
30						66					
31						67	1	67	V		BIT 7 RAW DATA
32						68					
33						69	1	69	V		BIT 8 RAW DATA
34						70					
35						71	1	71			LSB BIT 9 RAW DATA
36						72	BUS		V		GND

NAME DATA BUFFER **LOCATION** XA8 **BOARD** 4

BOARD TO BOARD CONNECTIONS

	FROM						FROM				
PIN	BOARD	PIN	IN	OUT	FUNCTION	PIN	BOARD	PIN	IN	OUT	FUNCTION
1	BUS		V		+5V Vcc	37					
2	BUS		V		-15V	38					
3	NC		V		LSB BIT 8 STATUS IN	39					
4	3	51		V	GATED 0 PERCENT CAL OUT	40					
5	NC		V		BIT 7 STATUS IN	41					
6	2	12	V		0 PERCENT CAL TIME IN	42					
7	NC		V		BIT 6 STATUS IN	43					
8	1	53	V		DATA READY IN	44					
9	NC		V		BIT 5 STATUS IN	45					
10						46					
11	NC		V		BIT 4 STATUS IN	47					
12	3	17	V		LSB BIT 8 SCALED DATA	48					
13	NC		V		BIT 3 STATUS IN	49					
14	3	15	V		BIT 7 SCALED DATA	50					
15	NC		V		BIT 2 STATUS IN	51					
16	3	13	V		BIT 6 SCALED DATA	52					
17	CONT PANEL	SYNC COM	V		MSB BIT 1 STATUS-SYNC	53					
18	3	11	V		BIT 5 SCALED DATA	54					
19						55					
20	3	9	V		BIT 4 SCALED DATA	56					
21						57					
22	3	7	V		BIT 3 SCALED DATA	58					
23						59					
24	3	5	V		BIT 2 SCALED DATA	60	5	35	V		WORD DISCRETE #1
25						61					
26	3	3	V		MSB BIT 1 SCALED DATA	62	5	37	V		WORD DISCRETE #2
27						63					
28	3	19	V		1.25 KHz CLOCK IN	64	5	41	V		MESSAGE DISCRETE #2
29						65					
30						66	5	39	V		MESSAGE DISCRETE #1
31						67					
32						68	5	60		V	NRZ OUT
33						69					
34						70					
35	5	62		V	1MHz CLOCK OUT	71	BUS		V		GND
36						72	BUS		V		GND

NAME MDM SIMULATOR **LOCATION** XA10 **BOARD** 5

BOARD TO BOARD CONNECTIONS

	FROM						FROM				
PIN	BOARD	PIN	IN	OUT	FUNCTION	PIN	BOARD	PIN	IN	OUT	FUNCTION
1	BUS		V		+5V Vcc	37	4	62		V	WORD DISCRETE #2
2	BUS		V		+5V Vcc	38	CONT PANEL	LT 8		V	LSB BIT 8 CHAN DISPLAY
3						39	4	66		V	MESSAGE DISCRETE #1
4						40	CONT PANEL	CHAN SEL		V	TENS BCD 2 CHAN SWITCH
5	BUS		V		-15V	41	4	41		V	MESSAGE DISCRETE #2
6						42	CONT PANEL	CHAN SEL	V		TENS BCD 1 CHAN SWITCH
7						43	CONT PANEL	ME-TER		V	ANALOG, SELECTED CHANNEL
8						44	CONT PANEL	CHAN SEL	V		UNITS BCD 8 CHAN SWITCH
9	BUS		V		+15V	45					
10						46	CONT PANEL	CHAN SEL	V		UNITS BCD 4 CHAN SWITCH
11						47					
12						48	CONT PANEL	CHAN SEL	V		UNITS BCD 2 CHAN SWITCH
13						49					
14						50	CONT PANEL	CHAN SEL	V		UNITS BCD 1 CHAN SWITCH
15						51					
16						52					
17						53					
18						54					
19						55					
20						56					
21						57					
22						58					
23						59					
24	CONT PANEL	LT 1		V	MSB BIT 1 CHAN DISPLAY	60	4	68	V		NRZ IN
25						61					
26	CONT PANEL	LT 2		V	BIT 2 CHAN DISPLAY	62	4	35	V		1 MHz CLOCK IN
27						63					
28	CONT PANEL	LT 3		V	BIT 3 CHAN DISPLAY	64					
29						65					
30	CONT PANEL	LT 4		V	BIT 4 CHAN DISPLAY	66					
31						67					
32	CONT PANEL	LT 5		V	BIT 5 CHAN DISPLAY	68					
33						69					
34	CONT PANEL	LT 6		V	BIT 6 CHAN DISPLAY	70					
35	4	60		V	WORD DISCRETE #1	71	BUS				GND
36	CONT PANEL	LT 7			BIT 7 CHAN DISPLAY	72	BUS				GND