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DIGITAL PHASE-LOCKED-LOOP SPEED SENSOR FOR ACCURACY IMPROVEMENT IN ANALOG SPEED CONTROLS

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16. Abstract

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SUMMARY

A digital speed control that can be combined with a proportional analog controller is described. The stability and transient response of the analog controller are retained and combined with the long-term accuracy of a crystal-controlled integral controller. A relatively simple circuit was developed by using phase-locked-loop techniques and total error storage. The integral digital controller will maintain speed control accuracy equal to that of the crystal reference oscillator.

INTRODUCTION

Analog feedback speed control systems have been used almost exclusively for precise speed control for many years. Electronic analog systems are capable of control accuracies of a fraction of a percent over long periods of time. In general, analog systems are simple and inexpensive and allow fast, smooth, and stable operation. But for accuracies of less than 1 percent, highly regulated power supplies, temperature-compensated components, and temperature-controlled ovens are required. Still, drifts of less than 0.001 percent per ^{o}C or 0.1 percent per year are nearly impossible to achieve. In a crystal reference digital system, speed control accuracy is not the major problem. Accuracies of less than 0.01 percent per year are easily obtained. However, expense and complexity are the most common reasons for not adopting digital systems. Also, their response tends to be slow, with step changes in the output that create transient response and stability problems.

The Lewis Research Center has been involved for many years in developing turbine-alternator power systems that require speed controls. These have generally been analog feedback systems (refs. 1 and 2), although digital systems have been considered (ref. 3). Precise speed control is desirable in a space power system both be-

cause of output frequency stability in alternating-current systems and because speed changes affect system efficiency. The speed control designed for the Mini-Brayton power conversion system (ref. 4) was a proportional, load-compensated, analog feedback system with short-term speed control accuracy of approximately 0.1 percent. Later in the development program the digital control described in this report was deveolped. The combination retains the short-term characteristics of analog control with the long-term stability of a digital system.

This design could be adapted to other systems and provides compromise between either fully digital or fully analog systems. This report describes the design of the digital system, its performance in the Mini-Brayton system, and information for its adaptation into other systems.

CONTROL TECHNIQUE SELECTION

In power system design, it is desirable to regulate the frequency accurately. Transient speed changes, as caused by load changes, must be corrected quickly and smoothly. Analog systems have been used satisfactorily in the Brayton power systems, but these control systems have been limited in accuracy. Therefore, a high-accuracy digital system was investigated for the Mini-Brayton system.

There are primarily two types of digital frequency sensors. One senses frequency difference and produces a voltage proportional to error. This is typically done by sensing input frequency or period and comparing it to a reference frequency or period. The difference is converted to a voltage. The sampling period is at least one-half cycle of the signal but typically several cycles. Since this is essentially a sampled data system, the output tends to change slowly and in discrete steps, causing voltage and/or frequency modulation and stability and transient response problems. Integral control could be obtained by digital integration. However, complex circuitry is required and the control typically has the above-mentioned serious drawbacks.

The second form of digital sensor uses a reference frequency and a phase detector. Phase-locked-loop (PLL) techniques have been used extensively in communication circuits but rarely in mechanical control systems. A PLL has a proportional control band of less than one cycle, and mechanical systems generally respond too slowly to stay in the error band. Also, a PLL is basically an integral controller with respect to frequency control. It will not result in a stable control loop on a turbine-alternator system, which is also an integrator, unless proportional control is added. However, the PLL concept has a smooth continuous real-time output and can be implemented with very little circuitry.

The PLL concept was used for this controller by overcoming the two problem areas,

limited control range and the need for an additional proportional control loop. PLL's are limited to a one-cycle control band. But, for example, if the input signal was divided by 10 and then applied to the PLL, the control band would be extended to 10 cycles of the input frequency. Alternatively, the total cycles of error could be counted, and a voltage proportional to this count added to the output of the PLL. This method was chosen. The original analog speed control loop for the Mini-Brayton system was a proportional controller. By retaining this controller and adding the PLL digital loop in parallel, the proportional control requirement was easily met.

A block diagram of the control loop is shown in figure 1. The Mini-Brayton engine operates with a constant turbine input power and a variable electrical power output as required by the user. The difference is dissipated in a parasitic load to achieve a power balance which controls the speed. The control concept presented in this report is not limited to this configuration and could just as easily control input power. The corresponding Bode plots of figure 2 indicate the characteristics obtained with and without the digital control and without proportional control. The loop would be stable without the digital control (i.e., less than 180° phase shift at a gain of 1) but unstable without the proportional control. However, the digital control adds to the loop gain, reducing the error.

SPEED CONTROL DESIGN

A digital controller was developed that incorporates the ideas presented in this report. A simplified block diagram showing the major components is presented in figure 3. A counter was used to measure the total number of error cycles from the phase detector. If the input frequency is too high, the counter total should be increased; if the input frequency is too low, the counter total should be decreased. Therefore, a countup or countdown (up/down) counter and an under/over frequency detector were used. A digital-to-analog converter (DAC) was used to convert the counter output to an analog voltage, which is added to the phase detector output to obtain a smooth continuous output. A pulse shaper was added to convert the phase detector output to a trigger pulse for the counter each time the phase detector goes through a 360° error. The counter has a limited capacity; therefore, during any sustained overspeed or underspeed, such as initial startup, the counter capacity would be exceeded. Overflow and underflow detectors were used to inhibit further counting by inhibiting the counter input pulses.

The complete schematic is shown in figure 4. Complementary metal-oxide semiconductor (CMOS) logic was used throughout because of its high noise immunity and low power consumption. A parts list is presented in table I. The components Q1, R1, and R2 convert the low-level magnetic pickup output to the CMOS logic level. This stage is

a self-biased, common-base amplifier converting a low-amplitude sine wave to a square wave. The crystal reference oscillator is a CMOS-compatible-output oscillator operating at the design control frequency (11.265 kHz for the Mini-Brayton, the magnetic speed pickup frequency at the 52 000-rpm design speed).

The components Z1A,B,C; Z2A,B,C; Z3A,B,C; and Z4A form the phase detector. The two outputs of this circuit can be combined to form a pulse-width-modulated output whose average value varies from 0 to 10 volts, proportional to a -360° to $+360^{\circ}$ phase error. The components R3, R4, and C1 perform the output averaging, available at C1.

The components Q2, Q3, Z5A, and Z5B and the associated resistors are the pulse shaper. Separate countup and countdown pulses are formed and then combined for a single clock pulse. The separate countup and countdown pulses are detected by Z1D and Z2D to control the up or down counting of the counter.

Two four-bit counters are combined to form an eight-bit binary (256 decimal) up/down counter. A R-2R DAC is driven directly from the counter and added to the phase detector output to form the output. The components Z6A and Z7A are the undercount and overcount detectors. These gates detect only the four most significant bits from the counter, which reduces the maximum counter range from 256 counts to 226 but reduces hardware by not requiring eight input gates for overcount and undercount detectors. An undercount signal blocks the generation of countdown pulses, and the overcount circuit will block countup pulses.

Since the design of this unit, a single CMOS PLL integrated circuit has been developed. This circuit could be used to replace the crystal reference oscillator and phase detector and also to simplify the clock-pulse-forming circuitry, effecting a significant parts count reduction.

PERFORMANCE

The circuit was tested with the breadboard Mini-Brayton electrical system and an alternator simulator. The transient response was governed almost completely by the analog system, which is reported in reference 4 and not repeated here. As the digital circuit was an integral controller, the steady-state error was zero, compared to the reference, and therefore equal to the crystal oscillator accuracy.

Power consumption of the CMOS logic was a few microwatts per gate. The major power consumer in this design was the crystal oscillator, followed by the clock pulse shaper, the DAC, and the input signal conditioning circuit. Total power consumption was about 100 milliwatts from a 10-volt dc supply.

Figure 5 shows various waveforms within the digital controller as the total system power level was increased, requiring the digital control to compensate. The phase de-

tector output, the up/down control, the clock pulse (inverted), and the digital sensor output are shown. At t_1, the input power was slowly increased for $4\frac{1}{2}$ seconds. The turbine-alternator speed increased, causing the phase detector output to increase. At $+360^{\circ}$ the phase detector output stepped back to zero, and a clock pulse (negative transition) was generated, stepping the counter one position. The up/down control had shifted to countup and would stay there until an underspeed was detected. The phase detector output was added into the DAC output, creating a ramped output (digital sensor output) instead of a stepping function. The parasitic power was proportional to the sensor output. In this case the phase detector component was too large, creating a small step at each count. This was not necessary but increased the smoothness of operation because of the hysteresis introduced. At t_2, the induced transient had settled out and steady-state operation had returned.

The phase detector output shown in figure 5 is the filtered pulse-width-modulated signal. The actual phase detector output is shown in figure 6 for a constant error of approximately 67°. The digital controller breadboard is shown in figure 7. The power supply, operating from a 90-volt dc bus, is also on this board.

CONCLUDING REMARKS

A simple inexpensive digital speed control design concept has been developed. The design is intended for use as an add-on to proportional analog controllers. The accuracy is limited only by the crystal reference oscillator, and there will be a negligible effect on the original system stability and transient response.

Lewis Research Center,
National Aeronautics and Space Administration,
Cleveland, Ohio, December 12, 1974,
506-23.

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TABLE I. - COMPONENTS OF

DIGITAL SPEED CONTROL

Designation	Component value
C1	0.01 μF
Q1	2N2060A
Q2	2N2906A
Q3	2N718A
R1, 6, 7	220 kΩ
R2, 5, 8	100 kΩ
R3, 4, 9	15 kΩ
R10, 11, 12	3.3 MΩ
R13	47 kΩ
Z1, 2, 5	4011
Z3	4023
Z4, 7	4012
Z6	4002
Z8, 9	4516
Z10	AD555

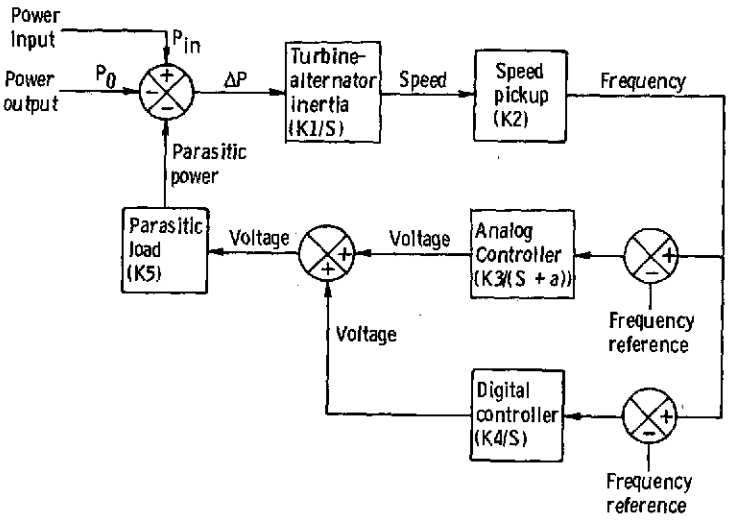

Figure 1. - Block diagram of speed control transfer function.

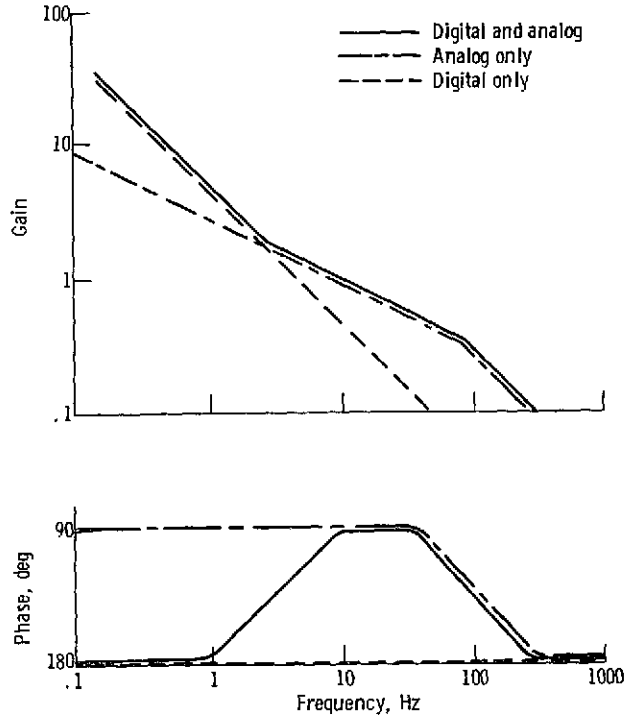

Figure 2. - Bode plots of speed control transfer function.

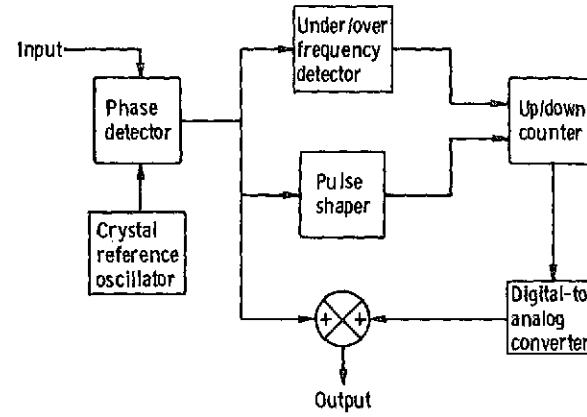

Figure 3. - Block diagram of digital speed sensor.

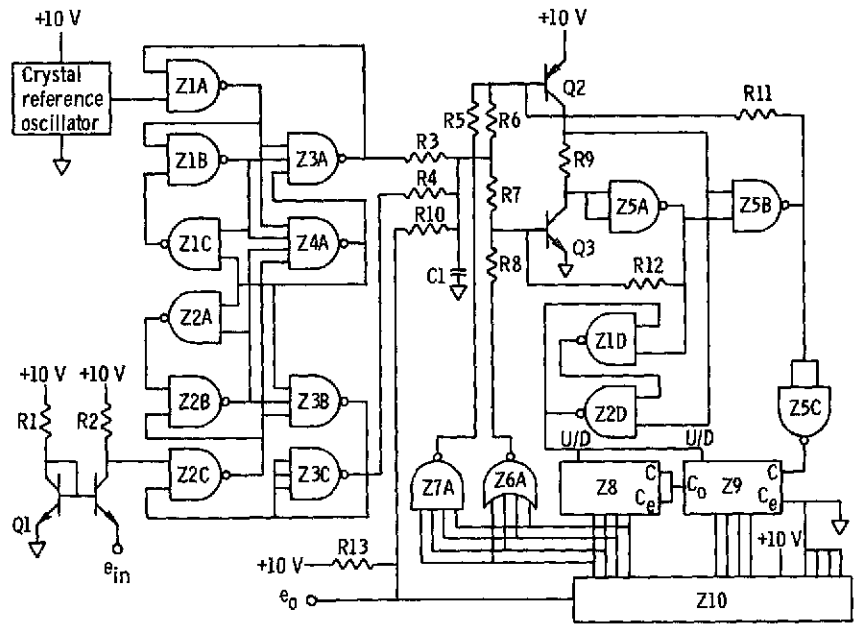

Figure 4. - Schematic of digital speed sensor.

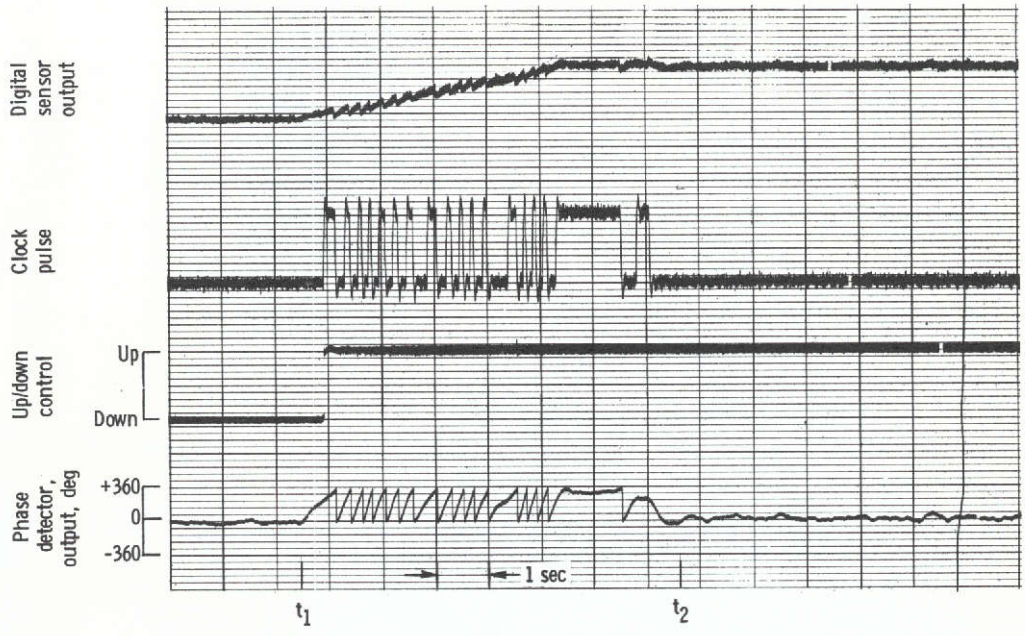

Figure 5. - Power transient response.

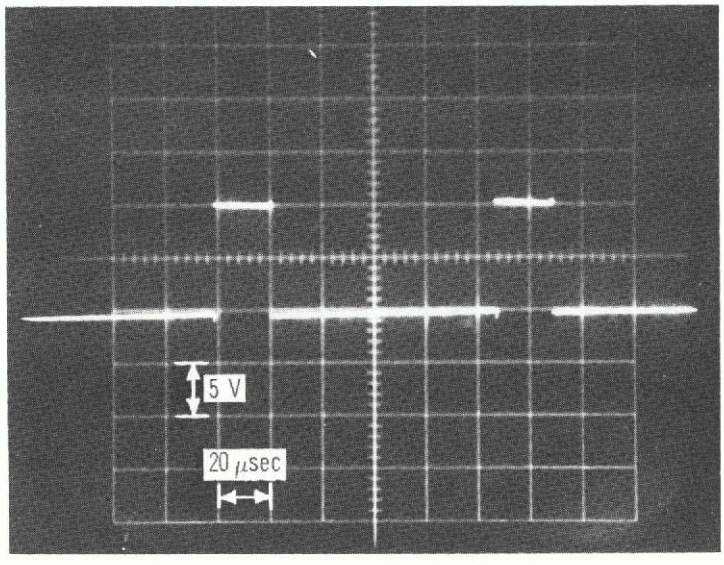

Figure 6. - Phase detector output.

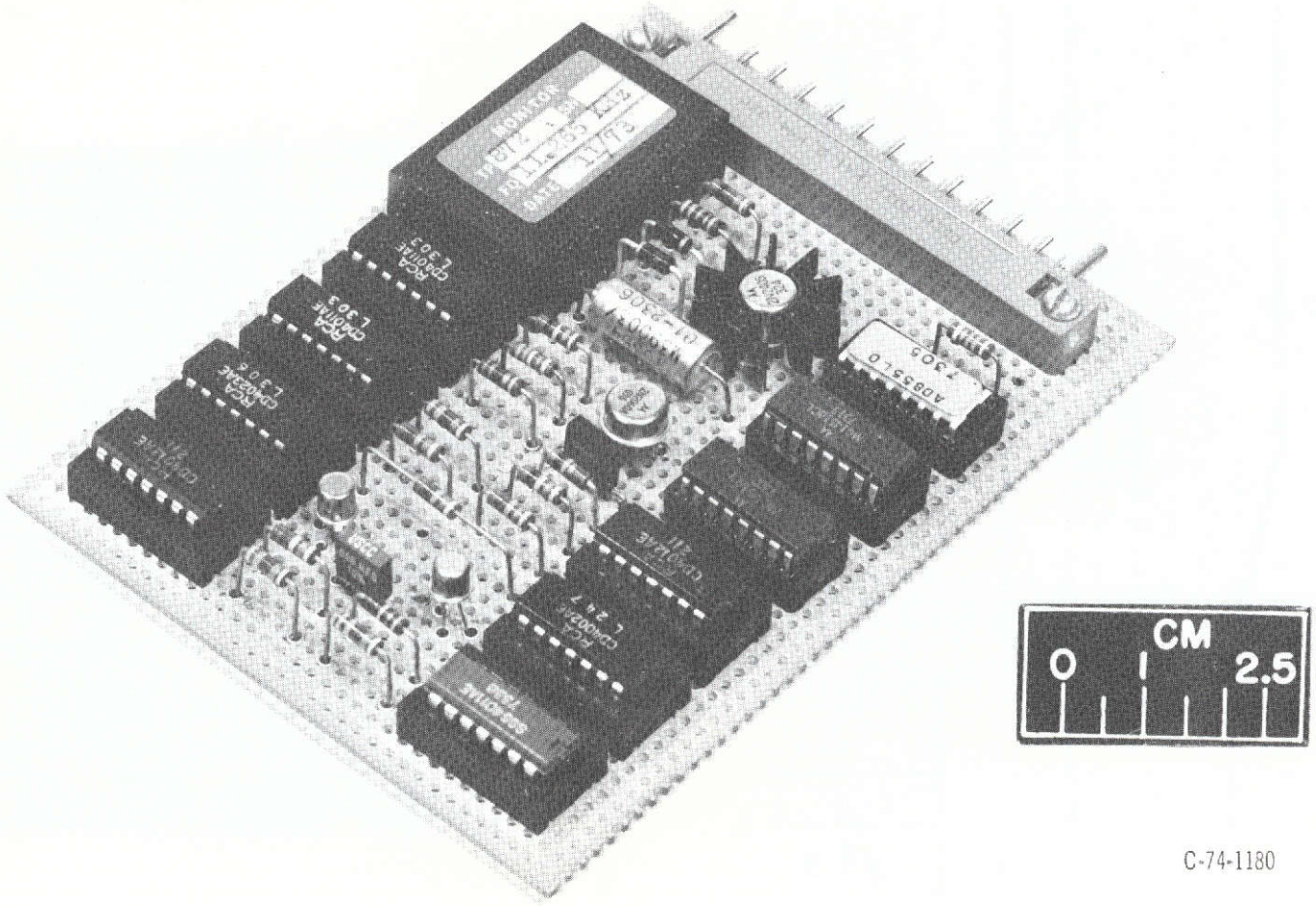

Figure 7. - Digital speed sensor breadboard.