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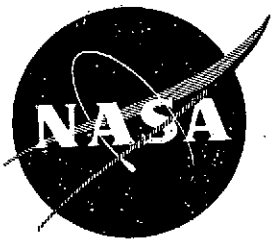

AEROSPACE TECHNOLOGY DEVELOPMENT OF THREE TYPES OF SOLID STATE REMOTE POWER CONTROLLERS FOR 120 VDC WITH CURRENT RATINGS OF FIVE AND THIRTY AMPERES, ONE TYPE HAVING CURRENT LIMITING

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16. Abstract

Three types of transistor remote power controllers (RPC) for 120VDC spacecraft distribution systems have been developed, built, and fully tested. Simple, efficient (99%), reliable and relatively low cost RPC designs are described with test results. Two generations of RPC's were developed. The first generation consists of a 5 ampere design (Type I) capable of limiting maximum overload current to 15 amperes for .1 second; a 5 ampere non current limiting design (Type II); and a 30 ampere non current limiting design (Type III). Each design provides overcurrent protection through an inverse I^2T trip out function with an automatic reset option. The non current limiting designs have selectable instant trip levels for high current overload protection. All designs have demonstrated step applied fault capability with a 4000 ampere surge, fast risetime (low inductance) power source. They have also been demonstrated to meet MIL - STD - 461A specification for Electromagnetic Interference. The second generation RPC's traded off specification compliance for reduction in cost and complexity for the Type I & II designs. These designs gave comparable performance in most areas and improved performance in other areas relative to the original designs with substantial improvements in cost and complexity. Improved areas of performance include; extended operating voltage range of 25 Volts dc to 132 Volts dc, no magnetic components are required, and superior partial load electrical efficiency was demonstrated. In both generations it was determined that the non current limiting type of RPC is not only feasible but is a more economical method of overload protection for certain load types.

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FOREWORD

The work described in this report was performed by the Control Systems Engineering Section at the Aerospace Electrical Division of Westinghouse Electric Corporation in Lima, Ohio. The work was done under contract number NAS 3-17771 with the National Aeronautics and Space Administration (NASA). The project was managed by Mr. Gale R. Sundberg of the Power Electronics Branch of the NASA Lewis Research Center in Cleveland, Ohio.

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D.A. Fox	-	Control Circuit and Trip Circuit Development
K.C. Shuey	-	Power Stage Development
D.E. Baker	-	Power Stage Development and Project Engineer

and many other Engineering Support Personnel

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1.0 Summary

The purpose of this report is to summarize the technology developed on contract NAS 3-17771. It is divided into 8 sections corresponding to each of the 8 tasks of the contract. These tasks are listed in the introduction along with the specification requirements.

1.1 Accomplishments

Two generations of circuit designs evolved from this work. The first generation of circuits met all of the functional requirements as listed in section 2.3 of this report. The second generation of circuits was the result of a contract modification which supported additional development effort for "simplified" circuit designs.

It became apparent, during the design phase of the project, that greatly simplified circuit designs could be realized if certain specifications could be relaxed slightly. Hence the contract was modified to add Task 7 and Task 8 to develop these simplified second generation circuits. Although these circuits do not meet all of the requirements established in section 2.3 of this report they do meet the intent of those requirements. For example, the voltage drop at rated load increased, but the power dissipation and efficiency of the RPC was essentially unchanged and the partial load efficiency is actually better.

1.2 Significant Accomplishments

Listed in the order of decending priority are the accomplishments on this project believed to be of significance to the RPC industry.

1. The technology of 120 VDC RPC's with ratings up to 30 amperes has been developed. The RPC can no longer be considered the roadblock to 120 VDC systems.

2. Electrical power efficiency of the RPC's is 98.5% to 99%.

3. Current limiting is by no means the only method of load and wiring protection. An instant trip design with an inverse I^2T trip time delay is compatible with many loads and is inherently lower cost and less complex than the current limiting type.

4. It was demonstrated that the RPC power stage has inherent ultimate current limiting for applied fault conditions without passive dI/dT limiting (power inductors). This performance was verified with a 4000 amp source with a cumulative power circuit inductance well below that which is anticipated for any practical power system.
(Reference paragraph 2.4 and 2.4.4)

5. The circuits are relatively simple and manufacturable. The 2nd generation circuits developed on the contract modification were yet simpler and consequently should be even more manufacturable.
(Reference paragraph 2.4 and 2.4.1)

6. The 2nd generation design has a steady state operating voltage range from 25 Vdc to 132 Vdc. The first generation circuits operate down to approx. 60 Vdc.
(Reference paragraphs 2.4 and 2.4.5)

7. The 2nd generation design has superior partial load efficiency performance over the original specification design. The full load efficiency of the 2nd generation design is essentially the same as the original design.

8. The 2nd generation design needs no magnetic components and therefore is amenable to multi chip hybrid packaging techniques.
(Reference paragraphs 2.4 and 2.4.3)

9. It has been demonstrated that Mil-Std-461A is a reasonable EMI specification for RPC's.

10. The digital control and status indication in the RPC is arranged such that interrogation for built in test is possible.

1.3 Problem Areas

All the problems encountered on this project were relatively minor in nature, however, there is one that is of interest. Being designers of RPC's it is not uncommon to need very fast power transistors and drive circuits which can respond quickly to applied short circuit faults. Consequently the benefits that reverse bias has on the switching speed of a power transistor are well known and would aid our efforts in inhibiting large

current flow upon instantaneous application of a zero impedance fault. However, the catastrophic effect it can have, i.e. reverse biased second breakdown (RBB), is also known and therefore is not usually applied to RPC designs. What was not known is that reverse bias (on the base emitter junction) of the power transistor is not a pre-requisite for RBB failures. This was discovered in the bread-board evaluation phase of the project and was verified by the power transistor manufacturer. It seems that RBB is possible if the impedance of base-emitter circuit is sufficiently low, on an instantaneous basis (such as a capacitor), and the base-emitter dV/dT is negative but V_{BE} need not necessarily be negative (reverse biased). Once this phenomenon was discovered and properly dealt with the problem dissolved.

All other problems were either device application problems or device capability problems and caused no serious reper-cussions.

1.4 Conclusions

The work performed on this project has demonstrated that 120 VDC RPC's with current ratings of 5 and 30 amperes are not only feasible but are relatively low cost, simple, efficient and reliable devices. RPC's can no longer be considered a road block to high voltage dc electrical systems.

The next logical step in the development of the solid state 120 VDC switchgear is the packaging of the circuits. It is recommended that further work be devoted to this end using hybrid multichip pakcaging techniques. Such techniques would reduce the RPC size to 2 or 3 cubic inches for the simplified circuit design. Work is being done in packaging relatively high power circuits, however, considerably more development is needed in this area before it is considered a ripe technology. In this respect such an undertaking would be furthering the development of solid state switchgear.

2.0 Introduction

High voltage dc electric power systems (above 100 V dc) are seriously being considered as candidate systems for future generation air and spacecraft. Recent NASA sponsored studies and investigations by the Navy have shown that high voltage dc transmission and distribution can provide significant weight reduction, greater design flexibility, higher reliability, and lower cost than conventional 28 V dc or 115 V ac systems. However, one of the principle factors delaying the application of high voltage dc to aircraft and space vehicle power systems is the lack of available, flight rated, control and protection equipment.

Currently available conventional electric switchgear suffers from limited reliability and from functional limitations. The limited reliability stems from inadequate quality control in the low cost mass production of electro-mechanical devices as well as their relatively high failure probability due to contact erosion. The functional limitations consist primarily of the inaccuracy of response and the relatively slow response time of circuit breakers. Currently available mechanical circuit breakers and switches for flight above 60,000 ft. are only suitable for voltages up to 50 V dc. Attempts to reduce transmission wire weight by adding remote operation to mechanical breakers in high voltage systems has resulted in excessively large, complicated devices.

Solid state electric switchgear offers great potential for high reliability, long life, fast response, and remote operation; however, it has, inherently, a high series voltage drop, a susceptibility to voltage transients, and requires a fuse for fail safe operation. Voltage and EMI isolation between power and control circuits present design obstacles.

The work effort is directed toward continuing the development and demonstrating technology of solid state switchgear in the form of remote power controllers and circuit breakers for high voltage dc power distribution in spacecraft and aircraft. Experimental studies varying critical parameters combined with fabrication and testing of engineering models of representative switchgear will serve to demonstrate this technology development.

2.1 Objectives

The objective of the contract is to develop three specific types of 120 Volt dc switchgear. The first type (Type I) has a current rating of five amperes and as a protection means it uses controlled current limiting in conjunction with an inverse time delay overcurrent trip characteristic. The second type (Type II) is also a five ampere rated unit but the protection means is a different inverse time delay overcurrent trip function

with an "instant" trip for currents exceeding a predefined level. The third type (Type III) is also an instant trip unit but has a steady state current rating of 30 amperes.

2.2 Tasks

To accomplish the technology development the project is divided into 8 tasks as follows: It should be noted that the last two tasks were added to the original contract when, in the course of development, it was discovered that relaxation of certain specification requirements would yield a simplified, lower cost unit.

Task 1	-	Preliminary Analysis
Task 2	-	Switchgear Breakboards; Design, Fabrication, and Evaluation
Task 3	-	Engineering Models, Design and Test Plan
Task 4	-	Fabrication of Engineering Models
Task 5	-	Testing of Engineering Models
Task 6	-	Delivery
Task 7	-	Simplified Circuit Analysis and Design
Task 8	-	Fabrication and Testing of Simplified Circuit Breadboards

2.3 Specifications

The specific operational requirements of the Solid State Switchgear are listed below.

2.3.1 Type I Remote Power Controller (RPC)

2.3.1.1 Steady state current rating of five amps at 120 $\pm$ 12 Vdc.

2.3.1.2 Voltage drop across the RPC at rated current is to be less than 1.0 volt.

2.3.1.3 Inverse trip time delay, T, must satisfy $(I^2 - 6^2)$ T = 20 amp^2 seconds $\pm$ 5% for I greater than 6 amperes.

2.3.1.4 The RPC is to limit the maximum load current to three times current (3x) up to 0.1 second before interruption. This 3x level is to be constant with respect to supply line (bus) voltage variations.

2.3.1.5 The RPC is to perform as defined in the presence of 50 micro-second bus transients from -65 volts to 200 volts peak instantaneous value.

2.3.1.6 The RPC is to be self powered from the bus and is to be controlled (on, off or reset) by a low power 15 Vdc $\pm$ 10% signal with a rate of rise greater than 1 volt/microsecond.

2.3.1.7 Output rise time and fall times are to be between 10 to 10,000 microseconds.

2.3.1.8 EMI generation and susceptability is to be minimized. Control and power circuits are to be dielectrically isolated.

2.3.1.9 The RPC is to provide optional automatic reset three times from the tripped state, with a delay between resets of 1 second.

2.3.1.10 Operating temperature: -55°C to 100°C, laboratory environment.

2.3.1.11 The RPC is to be trip free.

2.3.1.12 Power losses are to be minimized. Off state leakage current to be less than 5 milliamperes. The RPC is to provide remote status indication of the open or closed states.

2.3.1.13 Weight is to be minimized.

2.3.1.14 Failsafe I^2T is to be 625 Amp^2 - seconds for a current greater than 5x.

2.3.2 Type II RPC

2.3.2.1 The RPC is to have all characteristics the same as the type I RPC above except for item 1.3 and 1.4.

2.3.2.2 The RPC is to provide instantaneous trips for current levels of 15, 20 or 25 amperes (selectable).

2.3.2.3 Inverse trip time delay, T, is to satisfy $(I^2 - 6^2)\ T = 5$ amperes^2 seconds for I greater than 6 amperes.

2.3.3 Type III RPC

2.3.3.1 Steady state current rating of 30 amperes at 120 ± 12 Vdc.

2.3.3.2 Voltage drop across the RPC is to be less than 1.0 volt.

2.3.3.3 The RPC is to provide instantaneous trips for current levels of 60 or 90 amperes (selectable).

2.3.3.4 Inverse trip time delay, T, is to satisfy $(I^2 - 36^2)\ T = 100$ ampere^2 seconds, for I greater than 36 amperes.

2.3.3.5 The RPC is to be capable of series operation with either or both Type I and Type II RPC's.

2.3.3.6 The RPC must have the characteristics of the Type I RPC defined under 1.5 through 1.13 above.

2.3.3.7 Failsafe I^2T is to be 8000 ampere^2 seconds.

2.4 Additional Objectives

Westinghouse has been involved in the business of developing and manufacturing RPC's for several years and therefore has an interest in RPC's which goes beyond the specific NASA contractual requirements. It is for this reason that additional design objectives were established in an effort to influence the device toward less cost, better performance, and improved manufacturability. It is anticipated that the switchgear developed would ultimately be packaged using hybrid multi-chip packaging techniques. These additional unwritten design objectives are as follows:

2.4.1 Circuit simplicity is paramount. A simple circuit means lower cost and higher reliability.

2.4.2 Unless absolutely necessary no special or selected components shall be used. Again this means lower cost.

2.4.3 To facilitate the ultimate packaging task (not part of this contract) the use of magnetic components, especially high current magnetic components is to be minimized or preferrably eliminated.

2.4.4 The RPC should be compatible with very low impedance bus voltage sources.

2.4.5 It is desirable to have the RPC capable of operating continuously at supply voltages well below the 108 Vdc specified.

2.4.6 Electromagnetic interference (EMI) is to be within the limits of Mil-Std-461A.

3.0 Task 1 - Preliminary Analysis

The purpose of this task was to survey the semiconductor market for devices and develop basic circuit concepts which could meet the basic technical performance requirements established in section 2.3. Where necessary "soft" breadboards were to be constructed and evaluated in order to verify components and circuit concepts.

Primary emphasis was placed on the development of the power stages because they offered the biggest technical challenge. Although many circuit designs can perform the basic requirements, the specific requirements did require extensive engineering during Task I. The control, logic and trip circuits on the other hand are more straight forward and therefore required less effort.

3.1 Type I Power Transistor and Drive Circuit Selection

The Type I power switch is the 5 ampere current limiting power stage used in the Type I Remote Power Controller. The basic design requirements for this switch are given below.

a) Voltage drop $\leq$ 1 volt dc at rated load (5A).

b) Maximum sustaining off voltage 200 volts for 50 micro - sec and 120 volts $\pm$ 10% continuous.

c) Capable of limiting load current to 3X rated current regardless of load impedance for 0.1 second maximum.

d) Operating temperature range -55°C to 100°C.

e) Power loss for on and off states to be minimized.

These requirements stem from the NASA specification, Reference Paragraph 2.3 of this report. Component searches and circuit design concepts were generated for a technique to fulfill these basic requirements. The most demanding requirement is the ability of the device to dissipate the energy associated with the .1 second current limiting condition. That is, the transistor should be capable of safely dissipating 15 amps at 120 $\pm$ 10% volts or 1980 watts maximum for up to .1 second. This is the worst case condition of a shorted load and is applicable at maximum temperature. A survey of manufacturers with a

reputation for high power transistor capability was made in an effort to determine the highest S.O.A. (Safe Operating Area) devices available. The manufacturers surveyed included:

- Power Tech
- R C A
- Solitron
- Texas Instruments
- Westinghouse

Data sheets for the largest S.O.A. device manufactured by each company were obtained. Inspection of these data sheets revealed that no single device could meet our requirement of 15 amps at 132 volts for .1 second. Since these data sheets represent the largest available transistors it was concluded that no single device was available to do the job and that a circuit incorporating several components must be devised.

Further comparison of the data sheets revealed that the highest S.O.A. devices are Westinghouse types 164 or 2N2778. These are alloy transistors. Alloy units have long enjoyed the reputation of exceptionally high S.O.A. capability.

A direct comparison of the capability and cost of the various types of transistors is shown in Table 1. From this table and the S.O.A. data it is apparent that the best device to use for the Type I power switch development is the Westinghouse 2N2778 or Type 164 alloy transistor.

3.1.1 S.O.A. Improvement Technique for Type I Power Switch

Since the component search did not reveal any single device capable of withstanding the current limiting requirements of the 5 ampere RPC, it was necessary to develop a technique to share the dissipation with other devices. If this were impossible or impractical then we would have been forced to reduce the performance requirements of the RPC either in the area of operating voltage or the current limiting level.

Manufacturer	Type No.	Maximum Dissipation for .1 Second	I_C Max (Amps)	V_{CEO} (Volts)	Type	Cost ($) Single Unit	Comments
Power Tech	PT7503	3.5A, @ 75V @100°C 1.0A, @ 150V @ 100°C	70	150		95.00	V_{CEO} too low
Power Tech	2N5928	3.5A, @ 75V @ 100°C 1.0A, @ 150V @ 100°C	150	120		219.00	V_{CEO} too low
RCA	2N6259	7.5A @ 75V @ 25°C 1.2A @ 150V @ 25°C	30	150	Single Diffused	5.53	V_{CEO} too low. Must derate to 57% for 100°C Operation
Solitron	SDT5823	3..5A @ 75V @ 100°C 1.5A @ 150V @ 100°C	200	200	Planar	165.00	
Texas Instruments	TIXP549	.6A @ 75V @ 100°C -- @ 150V	100	120		240.00	V_{CEO} too low
Westinghouse	2N2778	6.0A @ 75V @ 75°C 2.0A @ 150V @ 75°C	30	200	Alloy	166.00	Must derate to 75% for 100°C operation
Westinghouse	164-20	6.0A @ 75V @ 75°C 2.0A @ 150V @ 75°C	20	200	Alloy	50.00	Must derate to 75% for 100°C operation

Table 1 - Performance Survey of High Voltage, High Power NPN Transistor

The solution to this problem turned out to be a circuit developed by Westinghouse for other current limiting dc switch applications. The circuit was originally developed to reduce the cost of a current limiting RPC by diverting part of the current from the power transistor to a lower cost power resistor. Sufficient current is maintained through the transistor to maintain current control (i.e., limit current to a fixed level regardless of overload impedance). This arrangement is shown by Figure 1.

Referring to Figure 1, when the power switch is off both Q1 and Q2 will be off and blocking load current. Note that Q1 and Q2 are shown as PNP transistors, this is for purposes of discussion only.

When the switch is on Q1 will be fully saturated and carrying all the load current, I_L, for normal load conditions. Also, during normal load conditions (i.e., $0 \leq I_L \leq 5$ amps), even if Q2 is fully saturated, it will carry an insignificant portion of the load current because of the relatively high series resistance, R1 and R2.

During current limiting conditions the current sensor output is compared to the reference by the current limit control circuit. Base current to Q1 and hence the load current will be controlled in a servo loop fashion. The level to which the load current is controlled (limited) is determined by the reference and will be constant and independent of the load impedance.

During current limiting V_S will be between 1 and 120 volts (200V transient) depending upon the overload resistance. As V_S increases (assuming Q2 is saturated) I_2 will increase and I_1 will decrease. Hence, part of the power dissipated during current limiting is diverted from Q1 to R1 and R2. Proper selection of R1 and R2 will keep Q1 within the S.O.A. over its entire voltage range.

I_2 must be limited to a value somewhat less than the current limiting level of 15 amps. This is so that Q1 will have sufficient current to maintain the maximum load current at 15 amperes. The purpose of zener Z1 is to force Q2 to limit I_2 to approximately 14 amps. The tolerance on this current level is not extremely critical since Q1 and the servo loop will automatically compensate for drifts and keep I_L at 15 amps. Diode CR1 is used for temperature compensation by cancelling the drift of Q2 base-emitter junction. The performance of this circuit is further illustrated by Figure 2. Equations defining the performance of the circuit are derived on the next page.

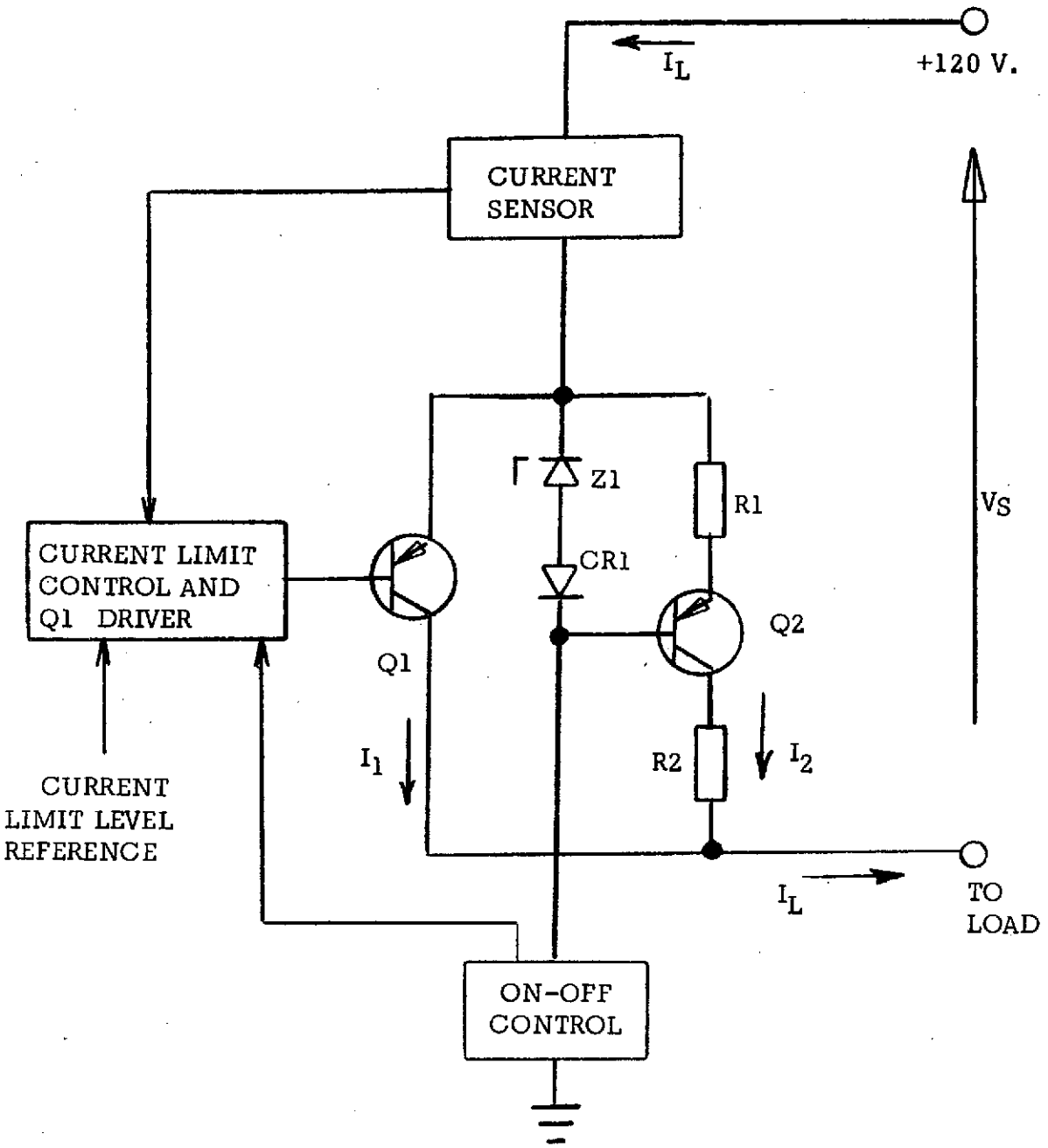

Figure 1 – Current Sharing Circuit to Boost S.O.A. Capability Beyond That of One Transistor

(A) Define V_{ϕ} (a constant) as value of V_S at which $V_{R1} = V_Z$ (or $V_{Q2} = 0+$) (A)

(B) Define I_{ϕ} (a constant) as value of I_2 at which $V_S = V_{\phi}$ then $I_{\phi} = V_{\phi} / (R1 + R2)$ (B)

Given:

(1) $I_1 + I_2 = I_L$ (1)

(2) $$\frac{V_S}{R1 + R2} = I_2 \leq \frac{V_Z}{R1}$$ (2)

(3) $$V_S \frac{R1}{R1 + R2} = V_{R1} \leq V_{Z1}$$ (3)

(4) $V_{Q1} = V_S$ (4)

(5) $0 \leq V_{Q2} = V_S - I_{\phi} (R1 + R2)$ (5)

$= V_S - V_{\phi}$ (from B)

then for: $V_S < V_{\phi}$	and for: $V_S \geq V_{\phi}$	
$V_{Q1} = V_S$	$V_{Q1} = V_S$	(6a, 6b)
$V_{Q2} = 0$	$V_{Q2} = V_S - V_{\phi}$	(7a, 7b)
$I_2 = \frac{V_S}{R1 + R2}$	$I_2 = \frac{V_Z}{R1} = I_{\phi}$	(8a, 8b)
$I_1 = I_L - \frac{V_S}{R1 + R2}$	$I_1 = I_L - I_{\phi}$	(9a, 9b)
$P_{Q1} = V_S \left[I_L - \frac{V_S}{R1 + R2} \right]$	$P_{Q1} = V_S (I_L - I_{\phi})$	(10a, 10b)
$P_{Q2} = 0$	$P_{Q2} = (V_S - V_{\phi}) I_{\phi}$	(11a, 11b)

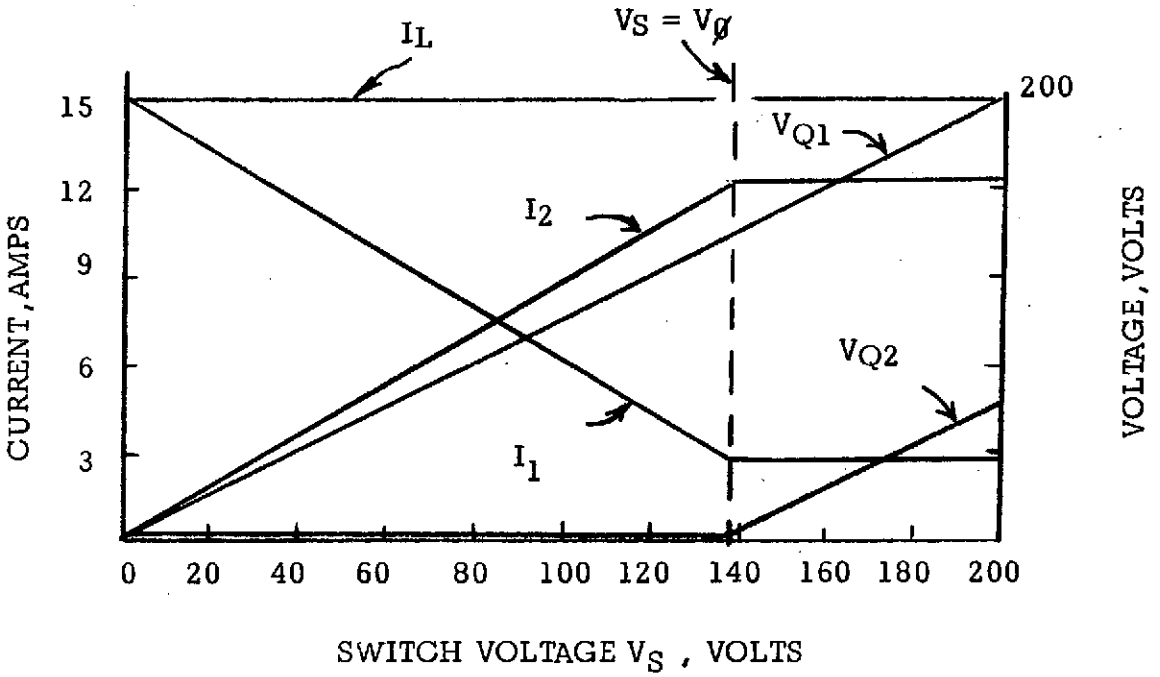

Figure 2 - Performance Characteristics of Circuit of Figure 1 , V_ϕ is a Design Parameter

The design problem then becomes the selection of V_{ϕ}, R1, R2 and V_Z such that Q1 and Q2 remain within their S.O.A. This can be done graphically by plotting the S.O.A. of the transistors and then fitting the circuit performance curves of Figure 2 around the S.O.A. curves.

The resulting graphical design is shown in Figure 3. It should be noted that bus voltages greater than 132 volts (120 + 10%) are transients of 50 microseconds in duration. It is assumed that only one such transient will occur within the 100 millisecond current limiting time. The Q1 curve from Figure 2 is fitted within the .1 second, 100°C S.O.A. curve which must extend up to 132 volts. To meet this requirement the Q1 curve can be tangent to the S.O.A. curve but must not cross over it. The resulting break point (V_{ϕ}) must be between 80 and 90 volts. This means that Q2 must sustain approximately 14 amps for up to 132-80 = 52 volts for .1 second. From the S.O.A. curves we see that a single device cannot handle that requirement. Therefore two devices are used which can withstand 7 amps at 52 volts for .1 second.

From this graphical analysis we can define the component values needed, from figure 3

$$R1 + R2 = 90/15 = 6 \text{ ohms}$$

If we assume the zener to be 5.6 volts (a fairly temperature stable zener) then from equation 8b:

$$R1 = 14/5.6 = .40 \text{ ohms}$$

and therefore

$$R2 = 6 - .4 = 5.6 \text{ ohms}$$

The S.O.A. booster circuit then becomes that shown by Figure 4. The entire 5 amp power stage including the Q1 driver and current limiting control is shown by Figure 5. This circuit is a slight modification of circuits used by Westinghouse for other RPC designs.

The helper circuit is energized only when the circuit is in a current limiting mode. The operational amplifier, Z1, is the current limiting control device. It controls Q1 in a class A mode to hold load current to 15 amps during current limiting. The 15 amp reference level is provided by the zero temperature coefficient (O.T.C.) zener CR4 and voltage divider R16 and R17. Resistor, R1, is a 50 mv. at 5 amp current sensing shunt.

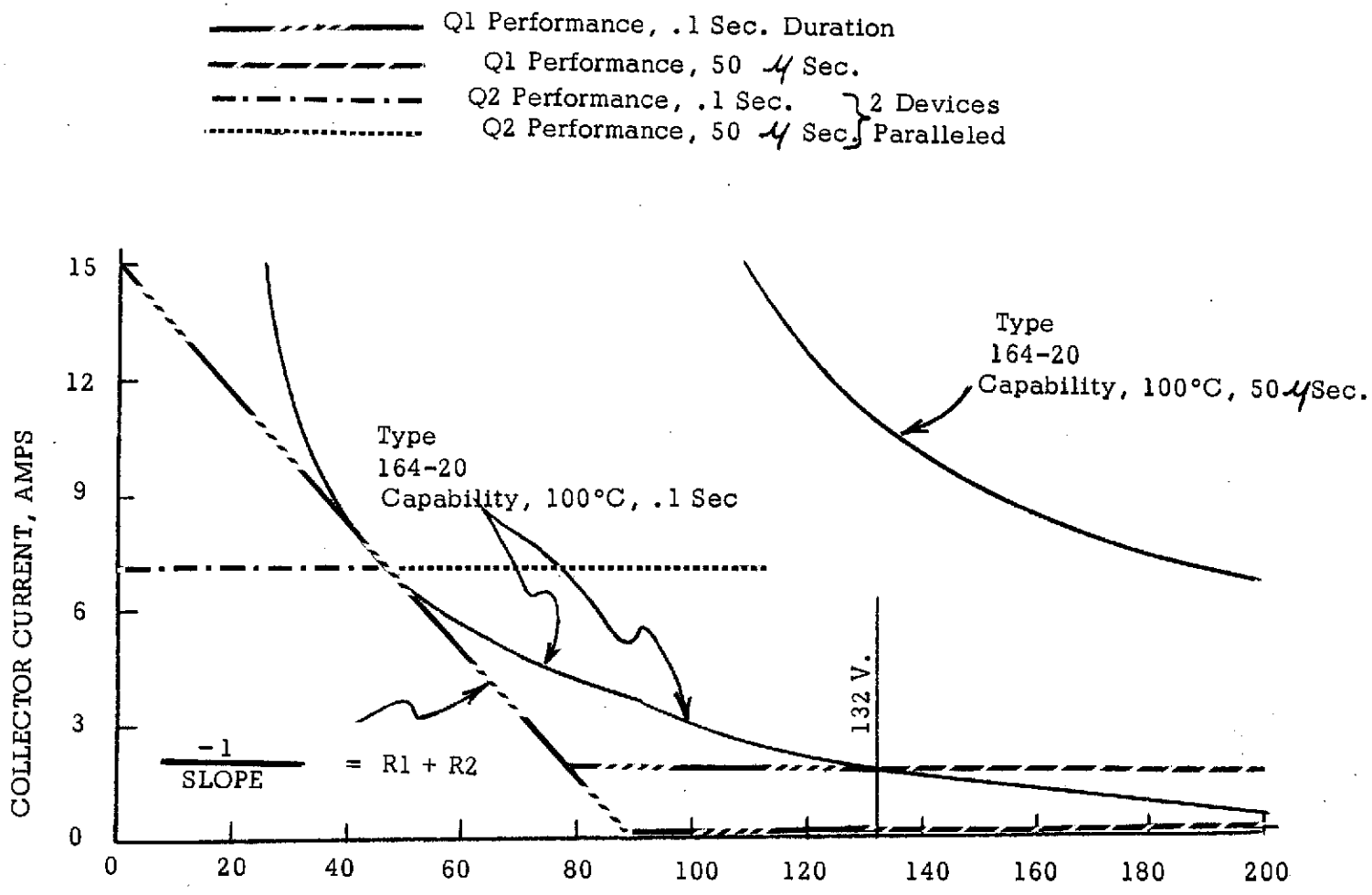

Figure 3 Graphical Design of Circuit Shown in Figure 1. Transistor Performance Levels Must be Within Capability Limits

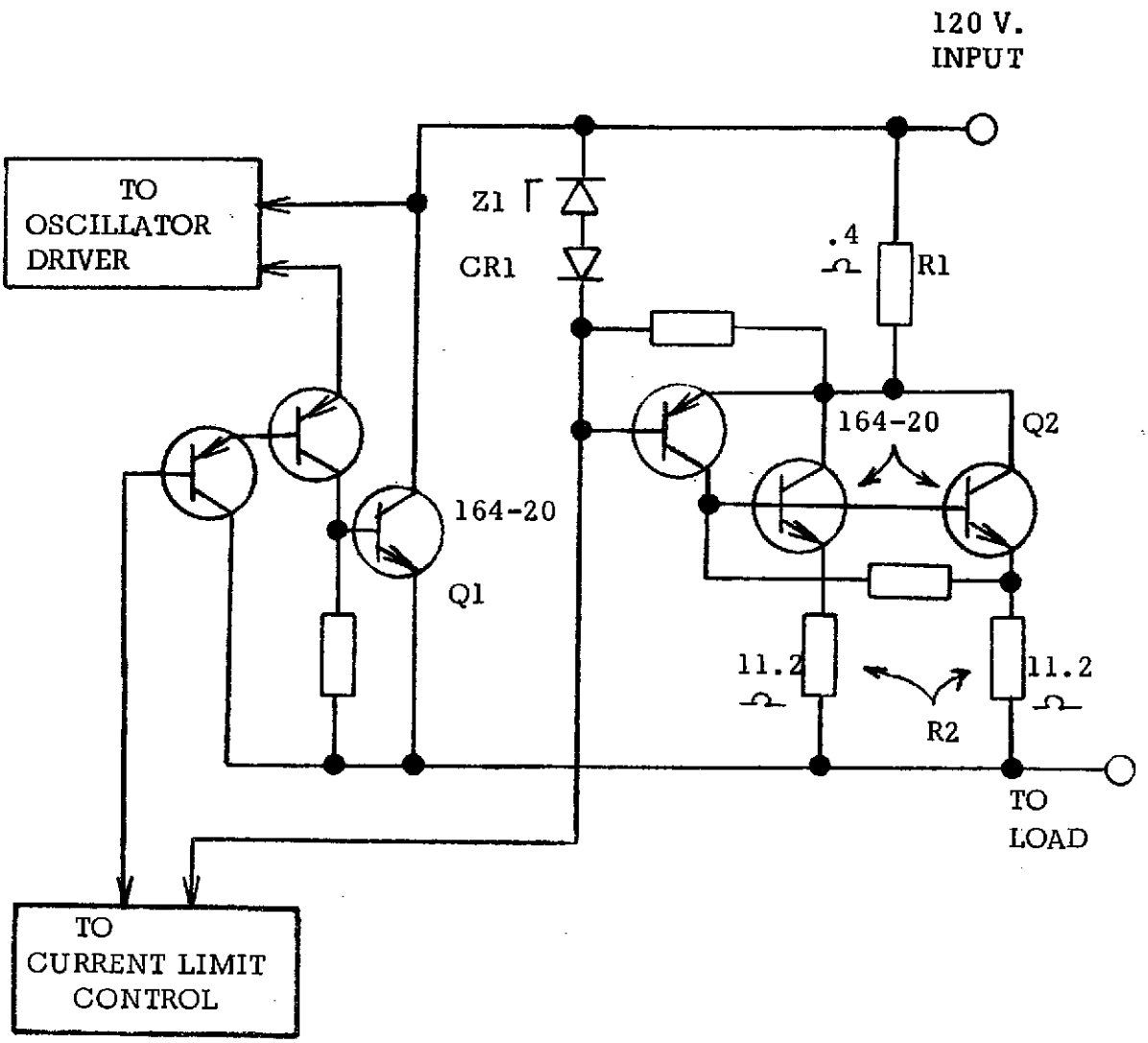

Figure 4 - Power Switch Design Exclusive of Q1 Driver Oscillator and Current Limit Control Circuit

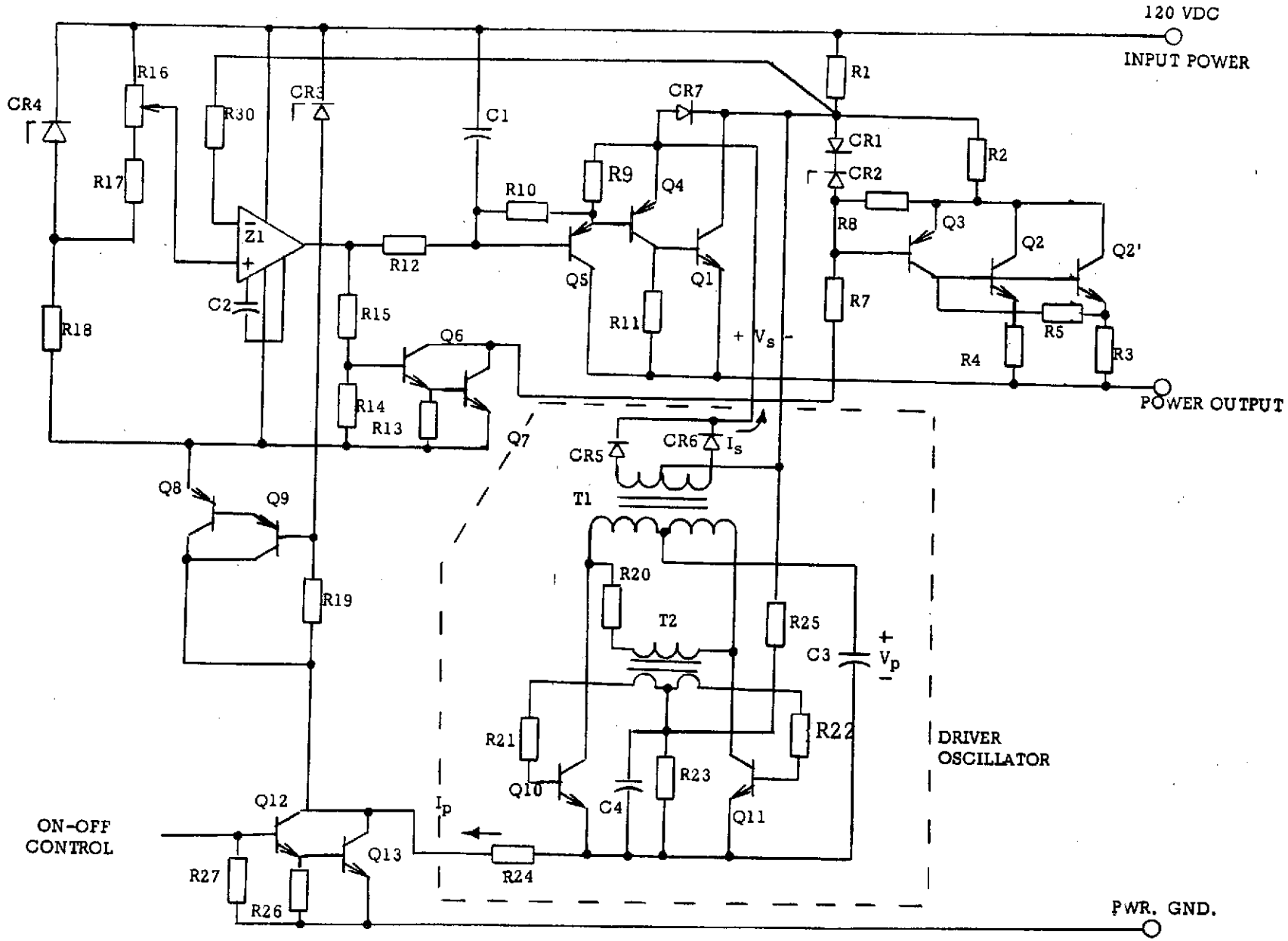

Figure 5 - Preliminary Type I Power Stage Design

3.1.2. Driver Oscillator Design

In order to minimize total power loss in the RPC it is essential that base drive current to the pass transistor be supplied with minimum current draw from the 120 volt supply line. Hence, an oscillator type driver is used so that a transformer can be used as a matching device. The approach to be used is shown in figure 5. It should be noted that maximum efficiency is not the only determinant for a transformer circuit. Since NPN transistors must be used for the power switch (due to lack of high power PNP transistors) there is no alternative to a transformer drive if 1.0 Vdc switch drop requirement is to be met.

The circuit of figure 5 is functionally represented by the circuit/block diagram of figure 1. The current limiting level of 3X is controlled by Z1. This basic circuit was developed by and has been used many times by Westinghouse and it is well defined. Z1 is an operational amplifier which can function properly with its inputs referenced to its own positive supply terminal.

The driver circuit for Q1 consists of Q4, 5, 10 and 11, T1 and associated resistors and capacitors. This particular circuit arrangement was selected above other techniques for the following reasons:

1. It uses a low voltage current sensing shunt (R1) which is simpler and more economical than magnetic type sensors. It is also very linear and has good temperature drift characteristics. The current sensor (and control amplifier Z1) is referenced to the power in line rather than the power out line thereby eliminating troublesome common mode rejection problems during current limiting.

2. Current limit control is controlled in a closed loop manner by Z1, Q5, Q4, Q1 and R1 but not through the transformer T1. This means that the switching transients from the transformer oscillator will not be coupled into the load circuit during current limiting and will therefore be nearly ripple free.

3. Overdrive to the pass transistor, Q1, for overload conditions is provided automatically without the sacrifice of added dissipation at rated load conditions. Therefore the oscillator circuit can be designed for rated load without regard for overload conditions.

4. Capacitor C1 serves the triple function of turn off fall time control, minor loop feedback for stability purposes and peak current limiting for applied fault conditions. The latter function is very important because this allows the power switch to begin current limiting action even before the operational amplifier Z1 can respond. Hence Z1 need not be a special, very high speed device.

The oscillator output will drive the power transistor with the maximum base current being limited by R24 in the primary circuit rather than the secondary circuit. This arrangement minimizes the voltages that the oscillator transistors must block.

The optimum turns ratio for T1 and the value of R24 were calculated and found to be 46.8:1 = Np : N_S and R24 = 2.4K. This calculation was based on the following assumptions:

1) The switch must be saturated (V_S < 1 volt) for a minimum steady state supply voltage of 100 volts.

2) Dissipation of base driver to be minimized for rated supply voltage of 120 volts.

3) Q1 to be driven with minimum forced gain of 10 for saturation.

4) The oscillator efficiency is 80%.

5) V_{BE} Sat = V_{CR5} = .75 volts.

These calculations also showed the oscillator current at 120 volt supply voltages to be

$$I_{OSC} = 20.6 \text{ ma}$$

for a theoretical base drive loss of

$$(120)\ (.0206) = 2.47 \text{ watts.}$$

Actual performance data was taken on a breadboard of the oscillator only. The data revealed that the design was somewhat optimistic. Subsequently, the turns ratio was altered to 38:1. The final data taken on the oscillator indicated an input current of 24.6 milliamperes at 120 VDC giving an actual dissipation of

(120) (24.6 ma) = 2.95 watts.

This basic oscillator design was used on all three types of switchgear developed on this contract.

A breadboard of the circuit (figure 5) was constructed to evaluate the circuit design and the capabilities of the power transistors. Some minor circuit changes were necessary but the performance did verify figures 2, 3 and 4. A summary of the static test data for the circuit (figure 6) is given in Table 2. The electrical efficiency of this design is calculated from the data to be 99%.

The minor circuit changes that were necessary to bring the performance up to desired levels are included in figure 6. The reasons for the changes are discussed below:

a) C7 and C8 were added to suppress output transients from Z1 during turn-on and thereby inhibit Q2 and Q3 during turn-on. Thus, turn-on is completely controlled by Q1 only.

b) R28 and R30 were added to reduce the gain and increase the bandwidth of Z1. This change enhances the stability of the current limit control.

c) R29, C6 and CR8 were added to improve the response of the current limiting circuit for step applied faults.

d) C4 and CR7 were added to better control the rate of charge of C1 during turn-on. This, in turn, improved the turn-on characteristics for rated load as well as overload conditions.

e) L1 was added to eliminate oscillator induced ripple currents in the load during current limiting.

f) C9 was added to slow the turn on rise time of the helper circuit and therefore reduce current limiting overshoot.

g) C10 was added to better reference the low side of the current sensor to the emitter of Q5 during current limiting.

Table 2 - Performance Data On Breadboard Of 5 Amp Current Limiting Power Stage As Shown By Figure 6

Temperature	+25°C				+100°C	
	ON State	OFF State	ON State	OFF State	ON State	OFF State
V_{Sw}	.228V	121.5V	.220V	120.9V	.30V	121.2V
I_{Gnd}	38 ma.	0 ma.	29 ma.	0 ma.	43 ma.	0 ma.
I_{Load}	5.0 a.	41 μa.	5.0 a.	21 μa.	5 a.	.6 ma.
V_{Bus}	120.8V	121.5V	120.5V	120.9V	120.6V	121.2V
$P_{Loss} = (V_{Sw})(I_{Load}) + (V_{Bus})(I_{Gnd})$	5.73W	5mW	4.59W	2.5mW	6.69W	70 ma
% eff $= \frac{P_{out}(100)}{P_{out} + P_{loss}}$	99.05	----	99.24	----	98.9	----

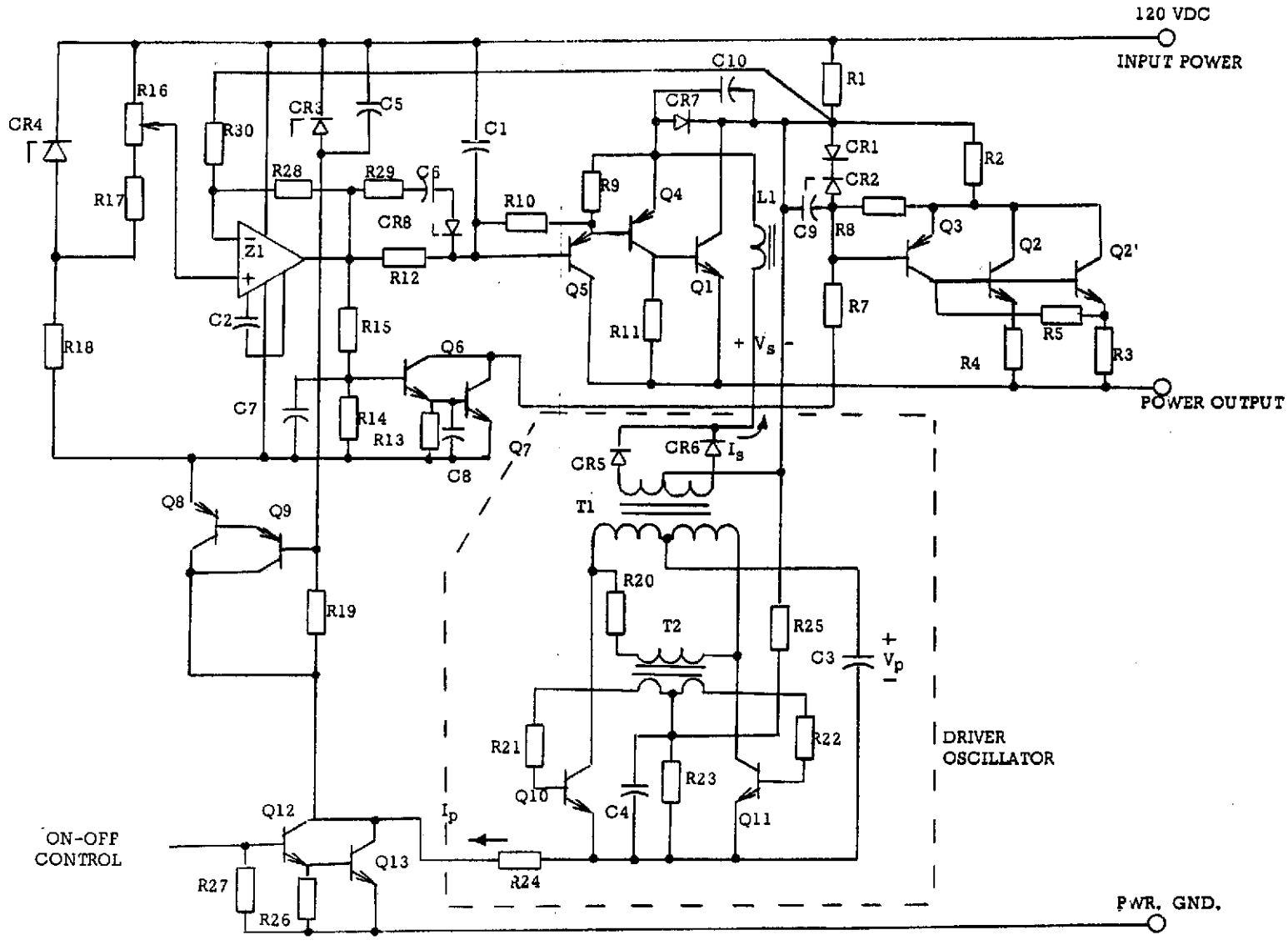

Figure 6 - Final Type I Power Stage Design

During the breadboard evaluation there was found to be more ripple than expected during current limiting. The magnitude of the ripple was about 10% of the current limit level and was the same frequency as the oscillator.

The ripple during current limiting was caused by the imperfect dc output voltage from the oscillator driver. The oscillator switching transients, although very fast, generate "holes" or transients in the rectified dc output of the oscillator. Hence "noise", in large amounts, is injected directly into the current limiting control loop. It is impossible to completely desensitize the circuit against this noise input and still maintain fast current limiting response time. Therefore the noise was filtered.

The output of the oscillator can be filtered either with a capacitor or inductor. However, for this particular situation, the inductor is smaller and less costly than a capacitor for equal performance improvements. The addition of the inductor was shown experimentally to virtually eliminate the ripple.

Although one of the design objectives is to minimize the quantity of magnetic devices, it is felt that the benefits of adding inductor L1 outweighed its disadvantages. The size of L1 is less than one-half the size of T1 and hence is not considered to be prohibitive.

The final circuit configuration for the Type I power stage is that shown by figure 6.

3.2 Type II Power Transistor and Drive Circuit Selection

The Type II and Type III power stages have essentially identical requirements except for current ratings. For this reason the smaller current rating (Type II - 5 amperes) was developed first with the intention of "scaling up" the design for the higher rating. The basic design requirements for the Type II RPC are given below:

a) Voltage drop < 1 volt dc at rated load (5A).

b) Maximum sustaining "off" voltage of 200 volts for 50 micro seconds and 120 volts $\pm$ 10% continuous.

c) Capable of passing 5X current (25A) for up to 8.5 milliseconds. Refer to paragraph 2.3.2.3.

d) Capable of withstanding an applied short circuit (at the output) when the switch is on without damage even though drive may not be relaxed (via the instant trip function) for several micro seconds.

e) Temperature range -55°C to +100°C.

f) Power loss for on and off states to be minimized.

These requirements stem from the NASA specification, reference paragraph 2.3 of this report.

The development effort for the Type II and Type III power stages involved the selection of power transistors and their drive circuits. The 5 ampere, Type II, design must pass 25 amperes for 8.5 milliseconds. Beyond that an instant trip is allowed. However, the finite time it will take to generate an instant trip signal in the control circuits will permit the current to overshoot 25 amperes. The amount of overshoot is the determining factor for transistor selection but is a function of both the circuit design and the transistor. The following options are possible for limiting the overshoot current. These options are for applied fault conditions which are the worst case conditions. The other, less severe condition, is when the RPC is turned on into a fault, in which case, the controlled rise time will keep dI/dT to manageable limits.

a) Limit di/dt to manageable levels with passive di/dt limiting (a line inductor).

b) Keep instant trip signal generation and propagation time to a minimum by using ultra high speed trip circuits.

c) Control peak current via the power switch design.

The first alternative would probably be the most effective approach, however, the weight of such an inductor could easily approach a half pound, a prohibitive level. Hence, the inductor was considered only as a last resort.

The second alternative is more desirable, but very high speed circuits have a tendency toward noise susceptability and high cost. The third alternative seems the best since the overshoot would depend upon the power stage design only and would be relatively independent of the trip circuit propagation time.

Similar to the Type I design it is essential that a transformer/oscillator circuit be used to furnish the base drive current. With this in mind several driver circuits were considered for the specific requirements of the Type II and Type III power switch.

The power transistor survey revealed that the 2N6249 series is probably best suited for this job when all parameters are considered, including cost. It is necessary to parallel sufficient quantity of transistors to handle the peak currents. Each transistor has a surge current rating of 30 amperes.

Several power stage circuits were designed, breadboarded, and evaluated. The best circuit configuration was found to be that of figure 7. This circuit is quite similar to the basic Type I power state (figure 6) except without precision current limiting. It was selected based on its merits listed below:

a) It used a low voltage current sensing shunt (R1) which is simpler and more economical than magnetic sensors. This shunt will also be used for the trip circuits.

b) Overdrive to the pass transistor, Q1, for overload conditions is provided automatically without the sacrifice of added dissipation at rated load conditions. Therefore the oscillator circuit can be designed for rated load without regard for overload conditions.

c) Capacitor C1 serves the dual function of turn off fall time control and peak current limiting for applied fault conditions. The latter function is very important because it removes drive from the power switch and therefore allows it to begin limiting current (for a few microseconds) while an instant trip signal is being processed in the control circuit. In effect the response time of the trip circuit is bypassed and is no longer a problem.

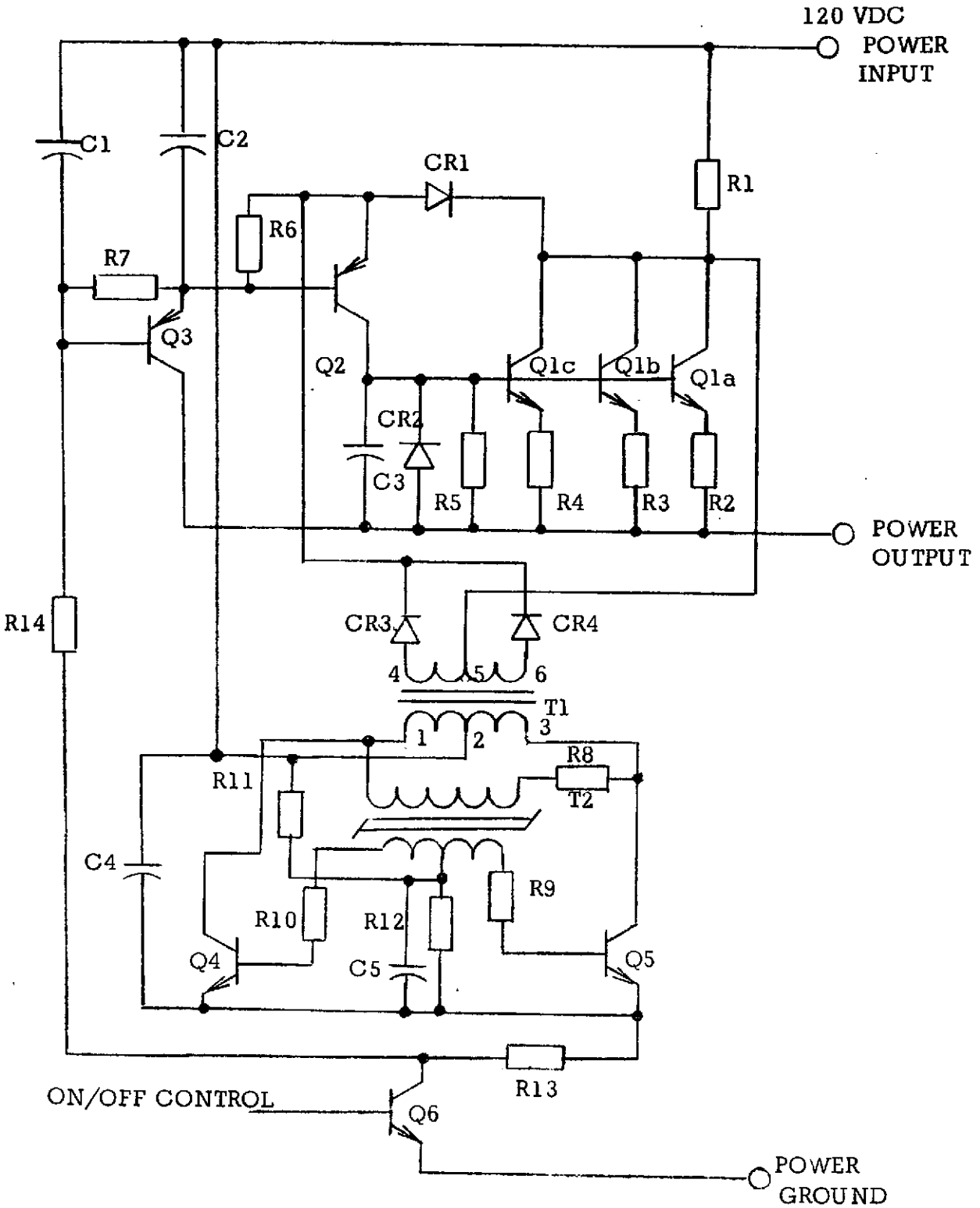

Figure 7 -Preliminary Type II Power Stage Circuit

d) Capacitors C2 and C3 serve to further reduce the peak current by coupling reverse voltage to the base of the respective transistors during applied faults.*

Preliminary test results on the breadboard were good. Electrical efficiency and static performance were virtually the same as the Type I data shown in Table 2. The room temperature data for the static performance is shown in Table 3.

The response of the switch to applied faults was extremely good. There was essentially no current overshoot for an applied fault which means that the response of the circuit was faster than the time constant of the external line inductance.

The line inductance as measured with an impedance bridge was found to be 10 microhenry. This represents the inductance of 25 feet (total current path) of #2 or larger welding cable with which the test set up was wired. In addition the 120VDC supply was a Harrison, Type 6475A, 0-120VDC, 0-100 Amp unit with a .1 farad (100,000 micro farad) output filter. This test set up was used in all of the RPC evaluation tests and is specified in the Test Plan developed in Task 3 of this project. The total surge capability of the set up was measured experimentally and found, for an applied fault, to be 4500 amps peak, at 1 millisecond giving an average dI/dT of 4.5 amps/microsecond and a total duration of 6 milliseconds. This response is shown by figure 8. It is believed that this test circuit represents a system with a surge capability and a dI/dT capability well above an actual aerospace electrical system. Therefore an RPC design compatible with this test set up was considered satisfactory.

After preliminary testing it was necessary to modify the circuit to bring the performance to desired levels. These changes are shown by the schematic diagram of figure 9 and are outlined below:

a) Inductor L1 was added to filter the oscillator output voltage. This modification was necessary in order to reduce switching transients across the relatively high speed power transistors Q1 (a, b, & c). Similar to the inductor added to the Type I power stage this inductor is relatively small and is, therefore, considered acceptable.

*These capacitors were later omitted. See text.

Table 3 - Performance Data On Breadboard Of 5 Ampere Non-Current Limiting Power Stage As Shown By Figure 7.

	ON	OFF
V_{sw}	.45 volts	120
I_{Gnd} (includes control & trip circuits)	.060 Amp	.018 Amp
I_{Load}	5 Amp	----
V_{Bus}	120 Volts	120 Volts
$P_{Loss} = (V_{sw})(I_{Load}) + (V_{Bus})(I_{Gnd})$	9.45 watts	2.16 watts
% Efficiency $= \frac{P_{out}}{P_{out} + P_{Loss}} 100$	98.45%	----

Vertical: I_{LOAD} = 1000 amp/cm.

Sweep: 2 millisecond/cm.

V_{BUS}: 120VDC

R_{LOAD}: 0 ohms applied with RPC by-passed. Current is limited only by impedance of the test set up wiring (i.e. 25 feet of #2 welding cable) and the power supply transient impedance

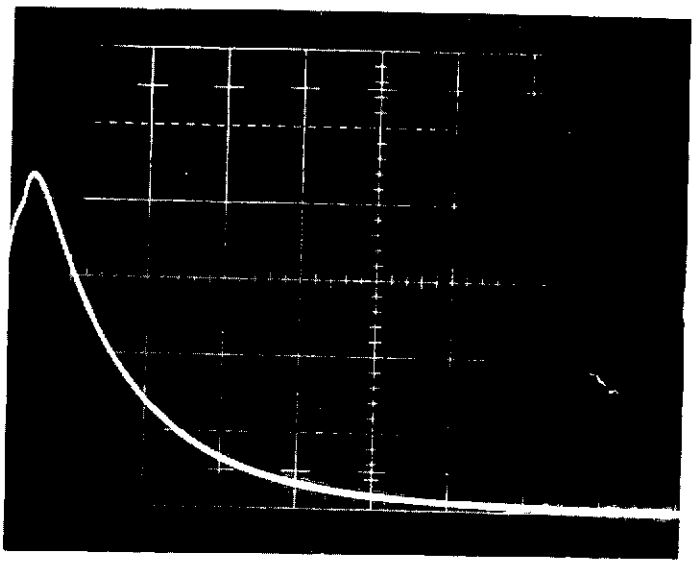

Figure 8 - Transient Surge Current Capability Of The RPC Test Circuit

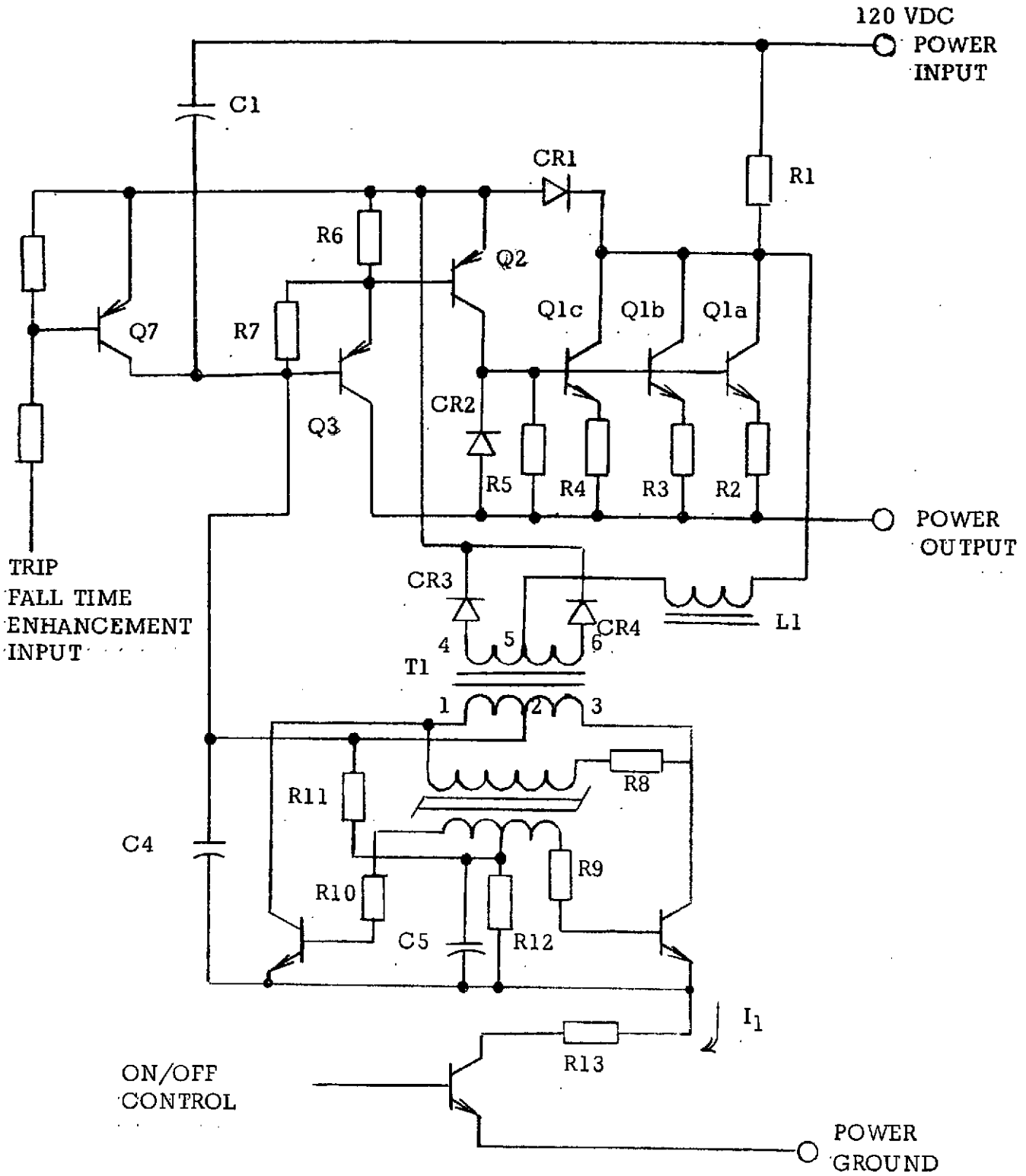

Figure 9 - Final Type II Power Stage Circuit

b) Transistor Q7 was added to quickly discharge capacitor C1 and thereby improve the fall-time of the power stage. This fall time enhancement circuit will be activated when the RPC trips off from an overload. This change was necessary to insure that the power transistors are not exposed to prolonged power dissipation during turn off from an overload trip.

c) A technique to reduce the power dissipation and thereby increase the performance of the circuits was incorporated into the Type II and Type III designs. Refer to the schematic diagrams figures 7 and 9. The change consisted in combining R13 and R14 into a single resistor R13 and hence combining the two current paths into one. The result is the elimination of the smaller of the two currents and its associated power dissipation thereby increasing the electrical efficiency of the circuit. This was done by moving terminal 2 of T1 from the 120 volt dc bus to the base of Q3 and deleting R14. The magnitude of the resultant current must be the larger of the two initial currents if similar oscillator currents and power switch saturation voltages are desired. The new value of R13 is therefore unchanged since this provides a resultant current essentially equal to the larger of the two initial currents. The calculated performance improvements are tabulated below along with the actual performance data:

Original Power Switch Dissipation	9.45 watts
Original Power Switch Efficiency	98.5%
Calculated reduction in Dissipation $= \frac{(120V)^2}{R14}$	2.88 watts
Calculated New Efficiency	98.9%
Actual Power Dissipation (B/B data)	6.34 watts
Actual Efficiency (B/B data)	98.95%

It was later discovered during breadboard tests, that the improved circuit could cause failure of the power transistors if, while the RPC was on, the bus voltage dropped to 60 Vdc for a sustained length of time (> 1 second).

Refer to the circuit as shown by figure 9 in this report. During normal operation V_{Bus} is 120 Vdc and oscillator current I_1 provides base current sufficient to saturate Q3. At sufficiently low V_{Bus} voltage levels the oscillator will stop running and I_1 will drop to a relatively low level as determined by the oscillator start resistor R11.

This level of I_1 is insufficient to completely saturate Q2 and Q3. Therefore, Q1 (a, b & c) will drop to a highly dissipative partial conduction state, which if sustained could cause thermal runaway and self-destruction.

The most obvious solutions to this problem is rather undesirable and "brute-force". That is a special circuit addition which would turn the switch full off if V_{Bus} ever dropped to the critical level. The theory of a less obvious and more elegant "fix" is described as follows:

For undervoltage conditions when the oscillator will not start I_1 is determined by R11. If the voltage across R12 is substantially higher than the voltage across R6 or R7, then the oscillator transistors will always be biased into conduction before Q105. This means that the oscillator will always start running before Q3 and the remaining power switch transistors are biased sufficiently to carry any load current. Hence if R6, R7 and R12 are properly selected we can insure that, if the bus voltage is below the oscillator start threshold, then no partial conduction or thermal runaway of the power switch can occur.

The critical ratio of $\frac{R6}{R11}$ and $\frac{R7}{R11}$ is one. A ratio greater than one will insure that partial conduction of the power switch can occur; whereas, a ratio less than one will insure that no partial conduction can occur. With a conservative ratio of .4, the Type II breadboard was checked and the switch output current was only a few microamps (normal leakage) with V_{Bus} just below the

oscillator start threshold. This threshold is at approximately 35 volts. Subsequent tests verified that the RPC is fully functional from that voltage to 132 volts steady state. Below 35 volts the RPC is off and fully protected against failure.

d) Further testing of the breadboards revealed unexplained failures of the power transistors Q1 (a, b and c) during short circuit tests. Since there was no current overshoot, the transistors (3 paralleled) were known to be operating well within their forward biased safe operating area and therefore that was eliminated as a cause for failure. Also with no current overshoot it can be shown that there can be no reverse base-emitter bias voltage applied to Q1 through the speed up capacitor C3 (refer to figure 2). Therefore reverse biased second breakdown was also eliminated as a possible cause of failure. Still having no explanation of the power transistor failures, the manufacturer of the 2N6249 transistor (Silicon Transistor Corp.) was contacted for assistance.

We reviewed the problem and our circuit techniques with Mr. J. Plaisted of STC (Silicon Transistor Corporation). His explanation of the cause of the failures is discussed below:

> The failure mode was believed to be reverse biased second breakdown (RBB). He advised that a reverse biased emitter junction is not necessary for RBB and that it can be caused by pulling reverse current out of the base while it is still forward biased. For our condition, the application of a fault generates a rapid increase in voltage across resistor R2, R3, and R4 (reference to figure 7) and this voltage is coupled by C3 to Q1 base. The base-emitter capacitance of Q1 is sufficient to allow reverse base current flow even though the base-emitter junction is still forward biased. Hence, the device is subjected to RBB conditions and failure is imminent.

The RBB failure mechanism was further substantiated by the shorted base-emitter junction of the failed transistors. According to Mr. Plaisted this characteristic is common to RBB failures.

The only acceptable solution to this problem was to eliminate capacitor C3. For similar reasons capacitor C2 was also eliminated. Due to the low current level in transistor Q3 it was found not necessary to remove capacitor C1.

The removal of these capacitors did change the response of the power stage. However, the transistors are now always in a forward biased state during a fault. Therefore, the forward biased safe operating area limits (SOA) determine the capability of the design. With the circuit of figure 9 and a test set up as described earlier the worst case applied faults were shown to fall with S.O.A. ratings of the 2N6249 transistors. Therefore, the conclusion was reached that the speed up capacitors were not necessary. The final circuit configuration for the Type II power stage, then, is shown by figure 9.

3.3 Type III Power Transistor and Drive Circuit Selection

The power stage for the Type III RPC is a scaled up version of the Type II. A schematic diagram of the circuit is shown by figure 10. Its performance features are the same as the Type II design discussed in section 3.2 of this report.

The specific performance requirements for this power stage are:

a) Voltage drop $<$ 1 volt dc at rated load (30A).

b) Maximum sustaining off voltage of 200 volts for 50 micro seconds and 120 volts $\pm$ 10% continuous.

c) Capable of passing 3X current (90 amps) for up to 15 milliseconds. Refer to paragraph 2.3.3.4.

d) Capable of withstanding an applied short circuit (at the output) when the switch is on without damage even though drive may not be relaxed (via the instant trip function) for several microseconds.

e) Temperature range -55°C to +100°C.

f) Power loss for on and off states is to be minimized.

These requirements stem from the NASA specification, reference paragraph 2.3 of this report. It was found necessary to parallel five 2N6249 power transistors in order to meet the surge current and applied fault requirements. The static data for the preliminary breadboard is shown by Table 4. The efficiency was slightly higher than expected at 99.28%.

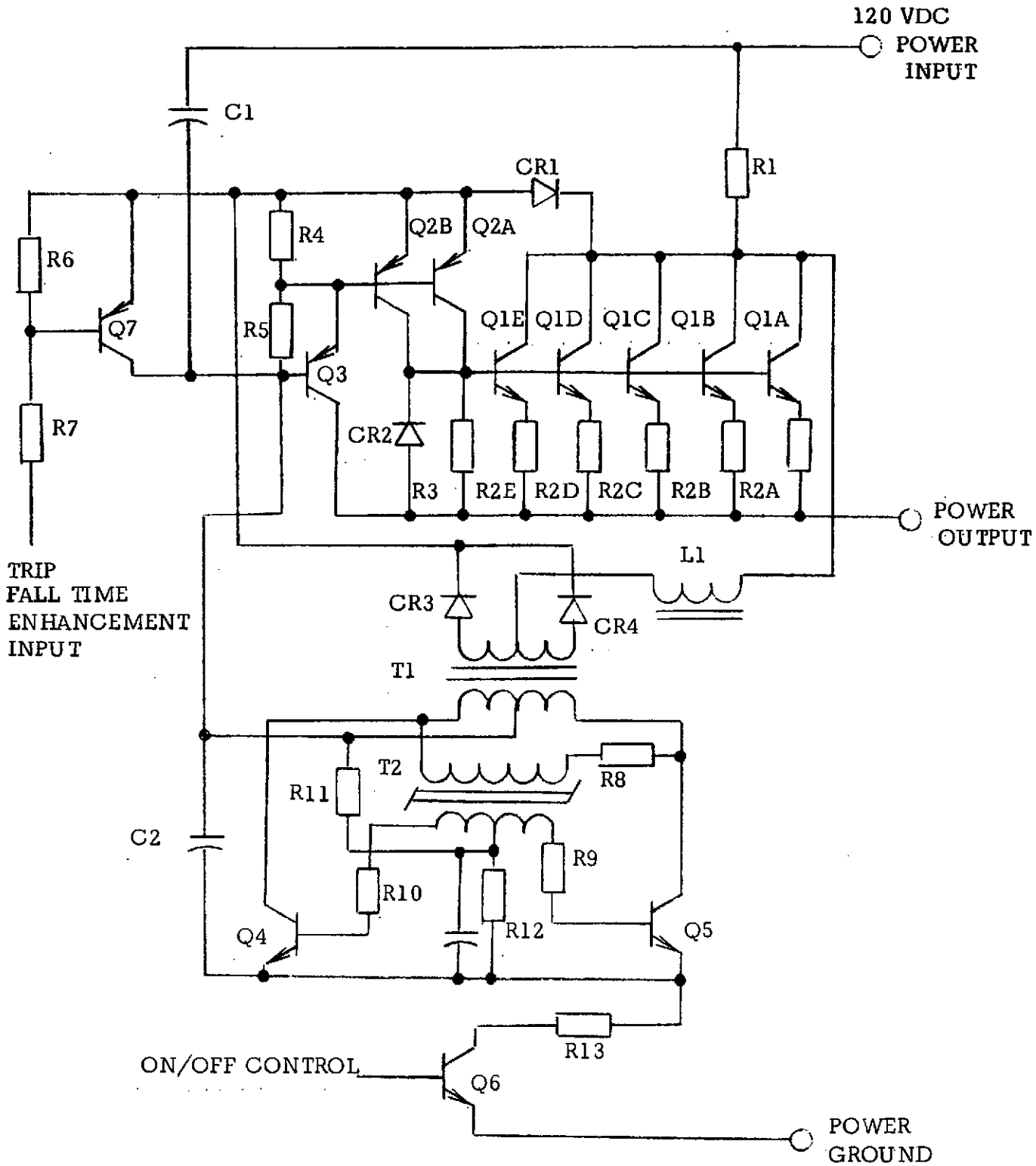

Figure 10 - Final Type III Power Stage Circuit

Table 4 - Performance Data on Breadboard of 30 Ampere Non-Current Limiting Power Switch as shown by Figure 10.

	ON	OFF
V_{Sw}	.44 Volts	120
I_{Gnd} (Includes Control & Trip Circuits)	108 ma	13 ma
I_{Load}	30 Amp	——
V_{Bus}	120 Volts	120 Volts
$P_{Loss} = (V_{Sw})(I_{Load}) + (V_{Bus})(I_{Gnd})$	26.16 Watts	——
% Efficiency $= \frac{P_{out}}{P_{out} + P_{Loss}}$ 100	99.28%	——

3.4 Trip Circuit Development

The function of the trip circuit is to monitor the load current and generate a trip signal to shut off the power stage when the load current exceeds specified levels. The time delay before trip is an inverse I^2T function established by the NASA specification, reference section 2.3. The specific requirements for each trip circuit are given below.

a.) Load current input signal is to be from a low voltage current sensing shunt. This shunt is part of power stage and it provides a linear signal of .05 $\pm$ 1% volts at RPC rated current.

b.) Output voltage is to be a digital signal which occurs at a time delay T_t, which meets the following equations:

Type I: $$T_t = \frac{20}{12 - 6^2}$$

Type II: $$T_t = \frac{5}{I^2 - 6^2}$$

Type III: $$T_t = \frac{100}{I^2 - 36^2}$$

where I is load current in amps and T_t is in seconds.

c.) Type II is to have selectable instant trip at 3X, 4X, and 5X rated current, i.e. 15 amps, 20 amps and 25 amps load current.

d.) Type III is to have selectable instant trip at 2X and 3X rated current, i.e. 60 amps and 90 amps load current.

These trip characteristics are plotted in figure 11. The desired trip equations are of the form

$$T = \frac{A}{X2 - X_0{}^2}$$

where X is the per unit current. This type of equation is particularly difficult to implement. It requires a multiplier to generate the term in the denominator. Analog multipliers are relatively costly and temperature sensitive. Therefore it was decided to adapt a trip circuit previously developed by

Westinghouse with a trip characteristic of the form

$$T = \frac{A\ (B - X)}{(X - C)}$$

For certain conditions this equation can be mathematically shown to be a good approximation of the desired trip equation. With the proper choice of constants the trip characteristics shown in figure 12 are produced. Comparison of figures 11 and 12 will illustrate the nearly exact duplication of the specified trip performance by the approximation circuit. These modified trip curves were submitted to NASA and were approved for the RPC design.

Figure 13 shows the circuit developed to generate the approximate trip characteristic. Current is sensed by shunt R1 which develops 50 mV at full load (X = 1.0). The shunt signal is amplified by Z1 with a gain set by the ratio of R7 to R6. In this case the gain in 100 so the output of Z1 is minus 5.0 volts referenced to the positive power supply at full load. Amplifier Z1 must be constructed such that its inputs will operate up to the positive power supply. The 101A operational amplifier was selected since it provides this capability.

Resistor R3 is adjusted for 6.0 volts across R4, so that the signal ground is 6.0 volts below the positive power supply. Thus, when the load current is 120% (X = 1.2) the output of Z1 will be exactly at signal ground. The difference is applied to Z2 so that the signal (X = 1.2) is integrated to form the basic time delay.

The output of the integrator, Z2, is compared to a reference set by R12 and R13. When the reference is exceeded, Q1 is turned on, and the trip signal is sent to the control logic.

Optional connections are provided for selection of instant trips at 2.0X, 3.0X, 4.0X, and 5.0X as shown on the trip curves, figure 12.

It should be noted that the instant trip propagation path is through amplifier Z1 and CR3, 4,5, or 6. The propagation delays of amplifiers Z2 and Z3 are bypassed therefore giving the best instant trip response time. Amplifier Z1 is externally compensated to give the best slew rate and still maintain stability and noise rejection.

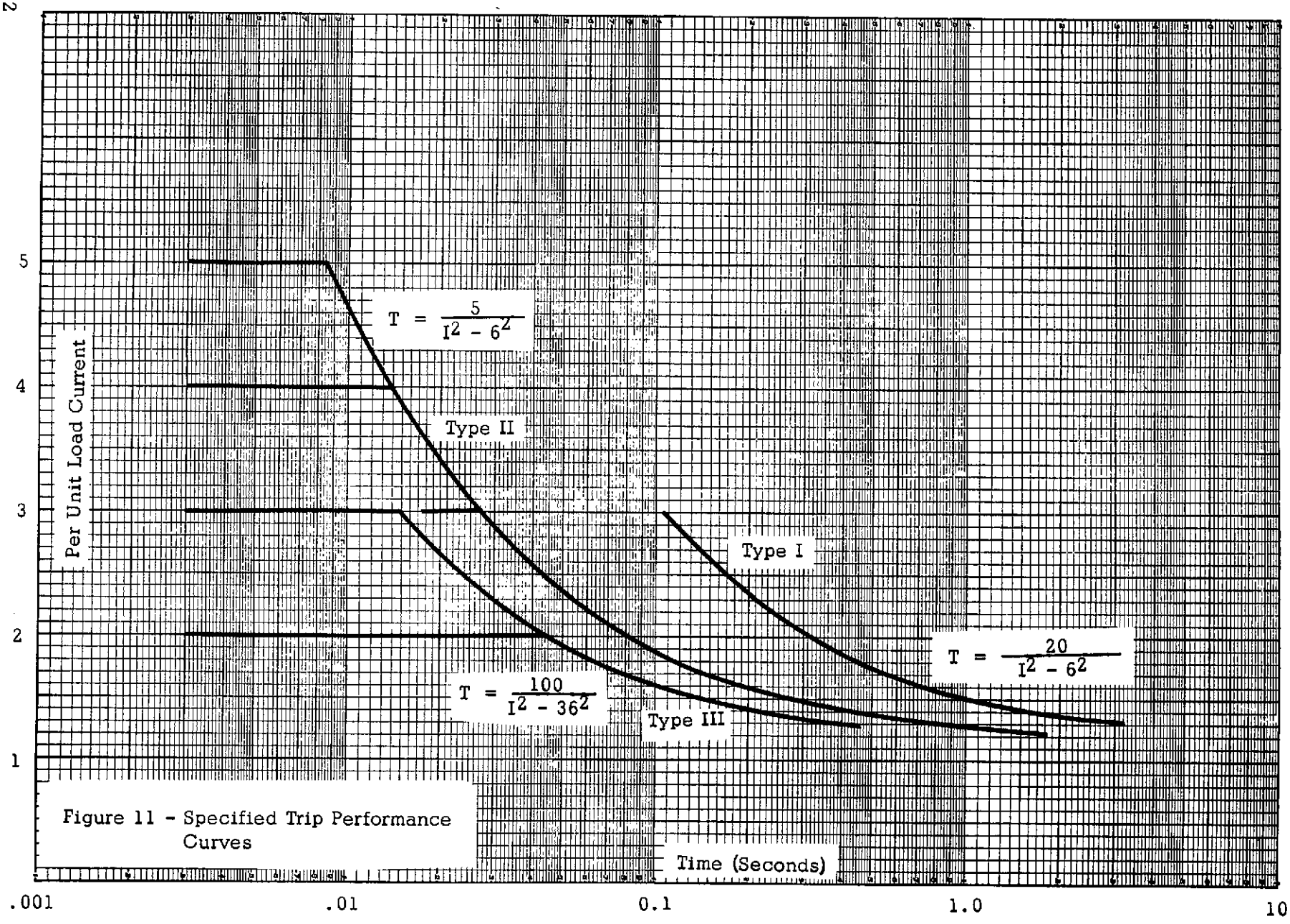

Figure 11 - Specified Trip Performance Curves

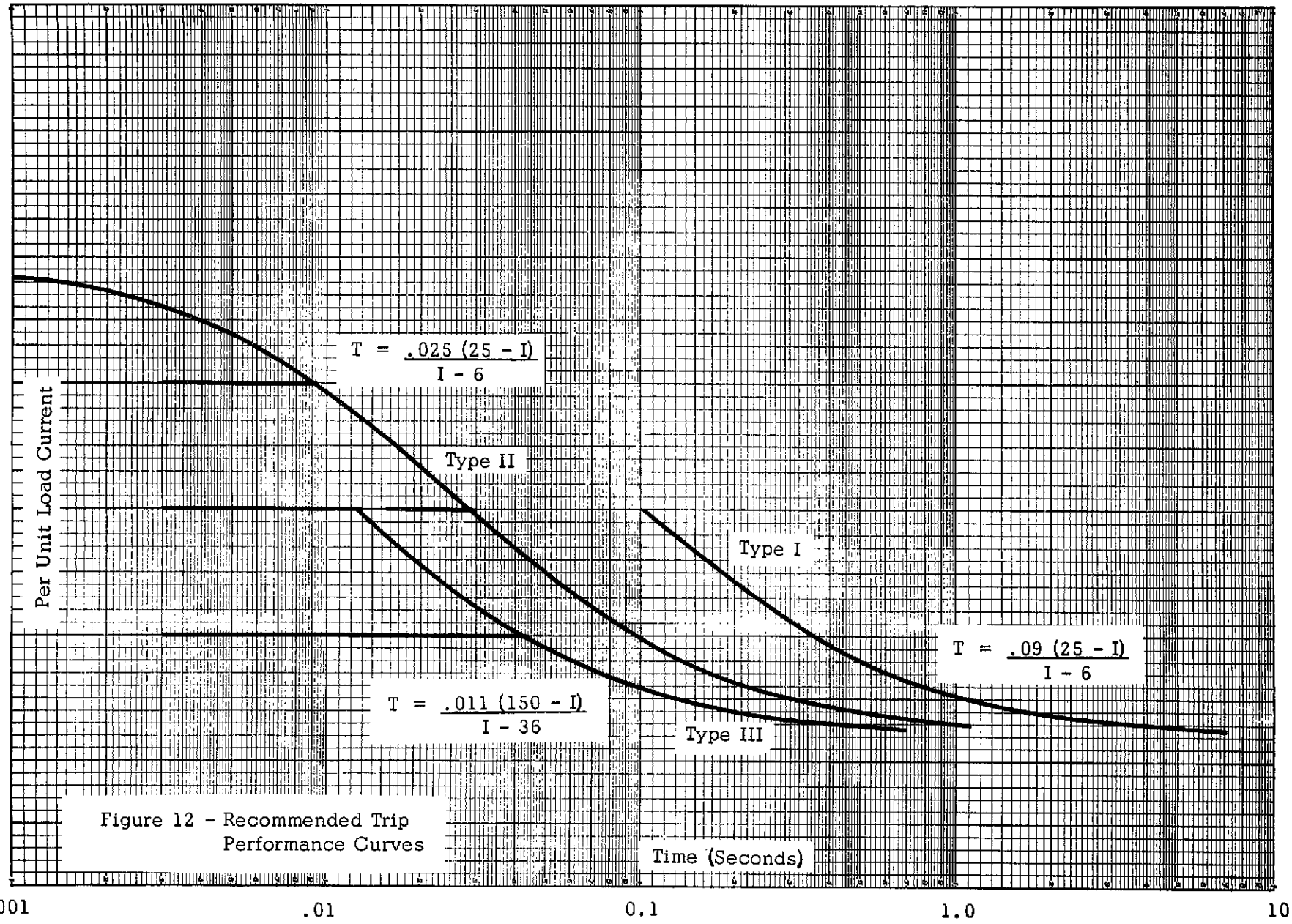

Figure 12 - Recommended Trip Performance Curves

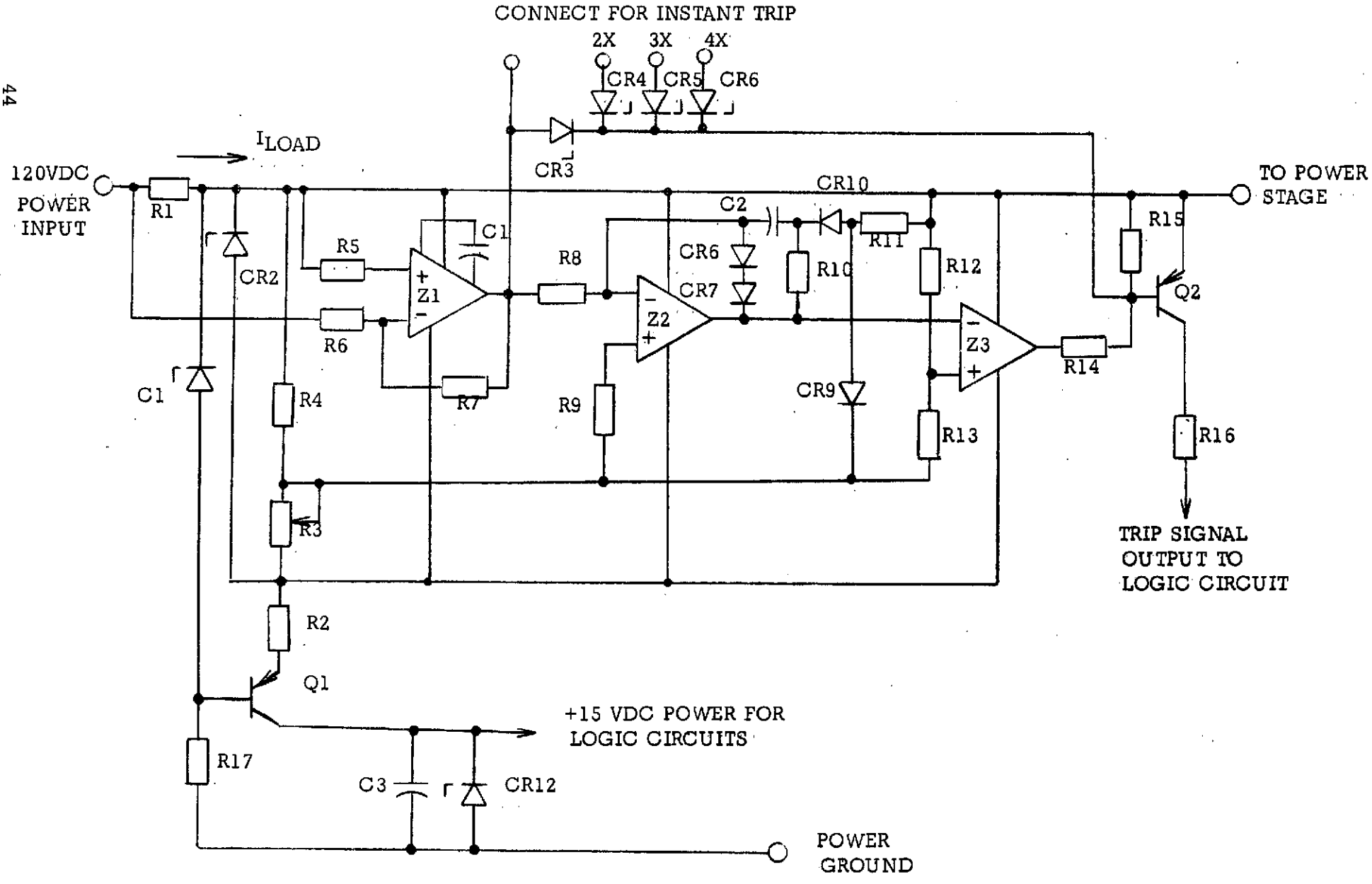

Figure 13 - Time Delay Trip Circuit

Test data of a preliminary "soft" breadboard is shown in figure 14. The performance was within the worst case calculated limits. The circuit as shown by figure 13 was then confirmed for the next contract task.

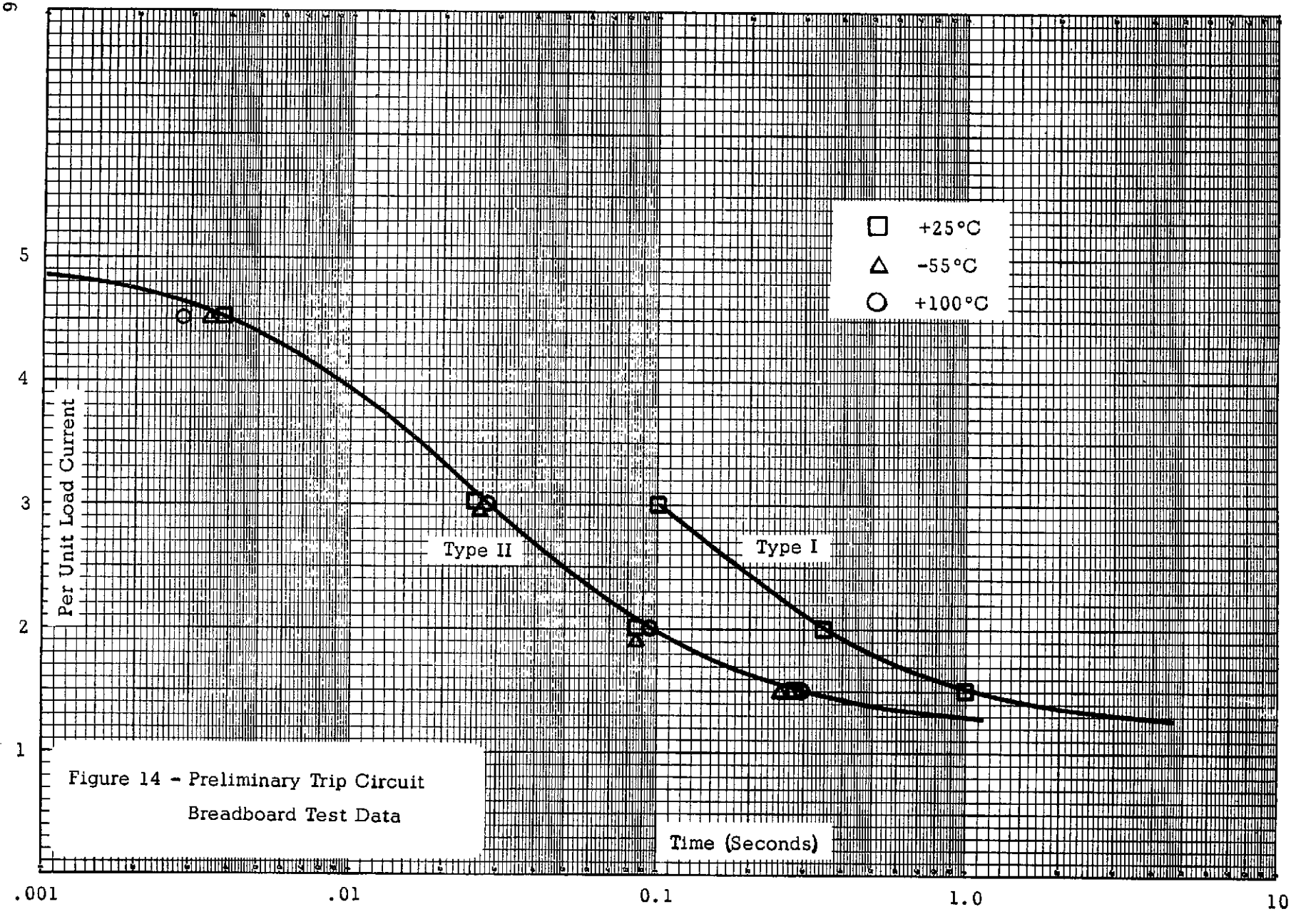

Figure 14 - Preliminary Trip Circuit Breadboard Test Data

3.5 Logic Circuit Development

The function of the logic circuit is to accept input signals from the control/isolation circuit and from the trip circuit and generate the proper output signals for status indication and power stage control. The specific design requirements are given below. These requirements stem from the NASA Specification, refer to section 2.3.

a) Application of a control signal shall generate a turn on signal for the power stage.

b) The turn on signal for the power switch will remain on until interrupted by either a relaxation of the control input or receipt of a trip signal.

c) The trip signal will be short duration and therefore the circuit must latch the power stage control off (tripped state) until reset by relaxing the input control signal.

d) Trip response and propagation time must be minimized.

e) The trip logic must be trip free, i.e., a trip and latch must occur even if the control signal remains.

f) Must have option to reset tripped state automatically three times with an approximate time delay of 1 second between resets.

g) Ambient temperature -55°C to +100°C.

h) Minimum power consumption.

The circuit of figure 15 was designed to meet these specific requirements with a minimum of complexity. It uses Complementary Metal Oxide Semiconductor (CMOS) logic to minimize power dissipation.

The D - flip flop, Z4, is the trip and latch function. The one shot, Z3, has a 1 second output pulse width and is used to effect the automatic reset. The number of automatic resets is counted by the tally counter constructed by D - flip flops: Z5, Z6, and Z7.

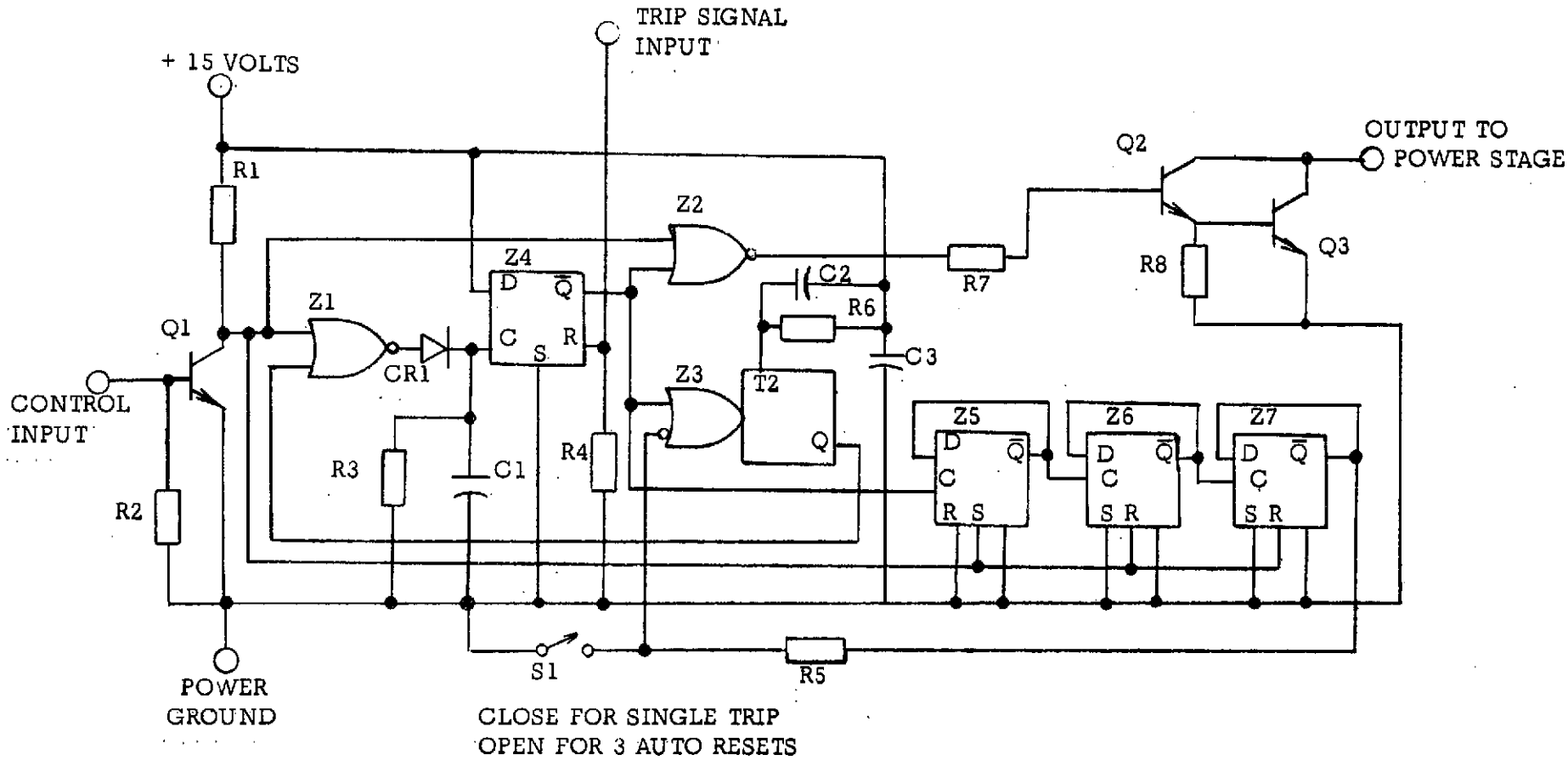

FIGURE 15- Logic Circuit For Type I, II, and II RPC Designs

When a control signal is applied to Q1 the power stage control transistors, Q2 and Q3, are saturated through Nor gate Z2 and the RPC will be turned on. If an overload current flows the trip signal will flip Z4 and turn off current flow through Z2 and Q2 and Q3. Simultaneously the one shot Z3 will be energized and begin a 1 second delay (assuming switch S1 is open). At the end of the one second delay Z4 will be reset through its clock input by the falling edge of Z3's Q output through Z1. The power stage will subsequently be re-energized through Z2, Q2, and Q3 and the process will repeat if there is another trip signal.

Each time the one shot is triggered its output will advance the tally counter one step through the clock input to Z5. After 4 trip outs (3 resets) the tally counter output, $\overline{Q}$ of Z7, will go low and inhibit further automatic resets by inhibiting triggering of the one shot. Relaxing the control signal will reset all D flip flops (trip and latch circuit and tally counter) to their original states.

For no automatic resets S1 is to be closed. This will inhibit automatic resets in the same manner that the tally counter does.

Capacitor, C1, diode, CR1, and resistor, R3, form a 10 to 20 millisecond noise immunity circuit which insures that the tripped state is not reset by control input noise. This is especially important on an instant trip RPC (Type II or III), which could be reset into a shorted load many times in a few milliseconds if the control signal was furnished by a mechanical switch with contact bounce or arcing.

Standby power consumption of this circuit is essentially zero for all states except for the dissipation in R7 when the RPC is on. Capacitor, C3, and diode, CR2, were needed to aid the one shot, Z3, in generating the relatively long, one second, reset delay time.

The trip signal propagation delay time is minimum. It has only to pass through Z4 and Z2 before it reaches the power stage control transistors.

3.6 Isolation Circuit Development

The purpose of the isolation circuit is to provide dielectric isolation between the control/indication signals and the power stage while preserving the necessary communications. Westinghouse experience in RPC design has resulted in several approaches to the control/status/isolation problem. The evaluation of these approaches has yielded five "rules-of-thumb" for control isolation which will result in reliable, manufacturable designs.

- Control circuits should be self-powered from control signal in order to keep circuits simple and reliable.
- Status indication or trip indication should be the grounding or sinking type, again to simplify circuits.
- Control voltage should be greater than 5 volts to keep cost down (NASA's requirement for 15 volts is good).
- Control current should be 10 ma minimum so that opto-couplers can be reliably used.
- Status indication saturation voltage should be 1.5 volts minimum to keep circuits simple and reliable.

The circuit shown by figure 16 was developed by Westinghouse for other applications. It is very straightforward and satisfies the NASA requirements (refer to section 2.3) and the rules of thumb mentioned above.

The optical couplers are preferred over magnetic devices because of cost, size, and weight. Up to 1500 VAC isolation can be achieved using standard, available opto-couplers.

Referring to figure 16, the control input to the RPC is sensed by the circuit consisting of R1, R2, CR2, and Q1. When the breakdown voltage of CR1 is exceeded, Q1 is turned on, turning off Q2, and allowing current to flow through the diode of optical isolator (OI). Resistor R3 provides a slight amount of positive feedback to ensure snap action of the sensor with no intermediate states. This sensing circuit has several advantages. First, it is relatively simple. Second, its input impedance is constant at approximately the value of R5, for a wide range of input voltages. Constant input impedance provides better noise immunity and allows several devices to be operated in parallel.

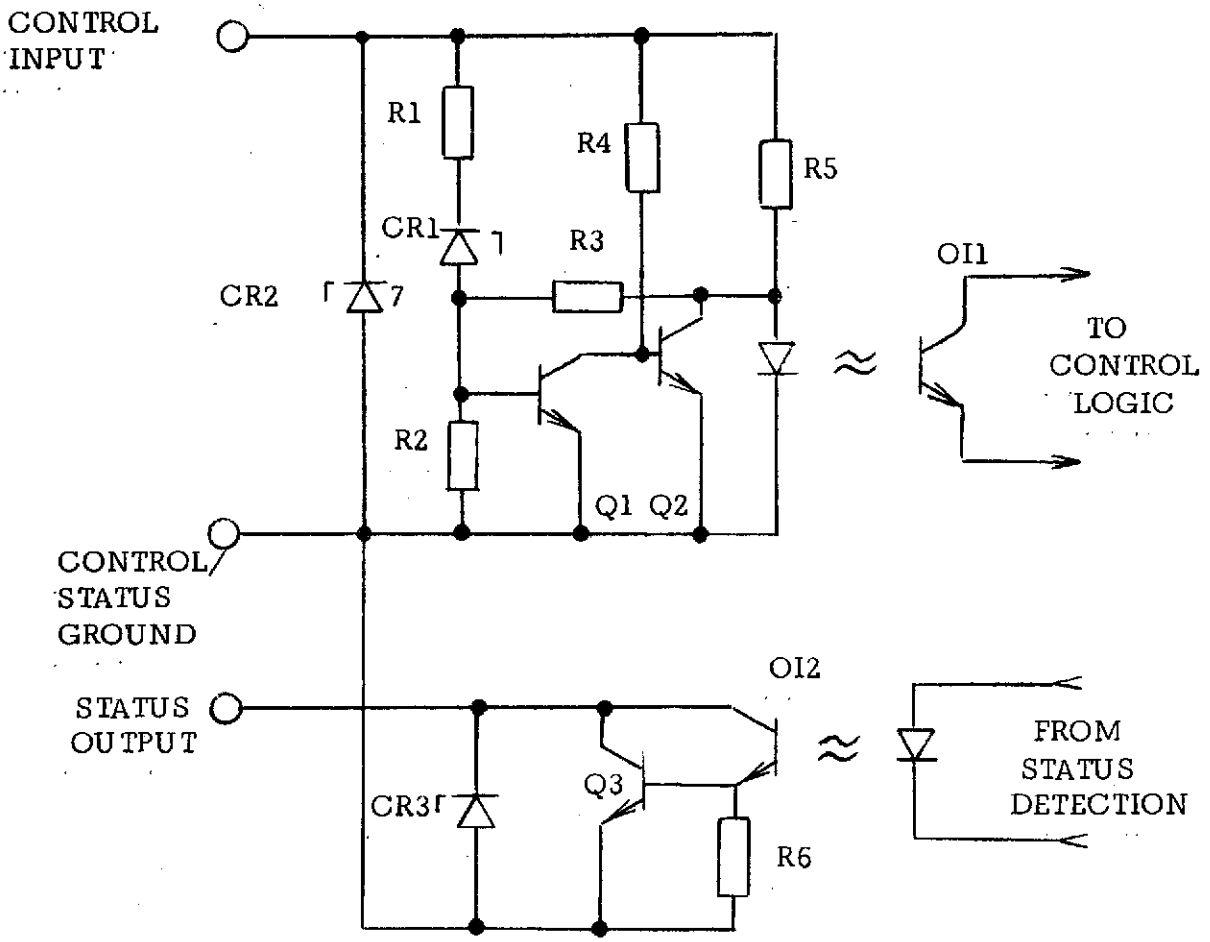

FIGURE 16 - Dielectric Isolation Circuit

3.7 Fail Safe Protection Development

The purpose of a fail safe mechanism in the RPC is to protect the system in case of failure of a faulted RPC. If the RPC is not able to clear the fault current (due to a shorted power transistor or other failure) the system power source may be overloaded, the bus voltage may drop, and system wiring may be damaged. The fail safe mechanism in the RPC is specified to open at some high I^2t value to protect against this type of failure.

The I^2t and steady state ratings of the fail safe mechanism must be above the normal overload trip circuit characteristic. The fail safe and overload I^2t specifications for the three RPC types are summarized below; referenced section 2.3.

	I^2t (amp^2 sec)	
	TRIP (UNFAILED)	FAIL SAFE
Type I	20	625
Type II	1 - 10	625
Type III	75 - 600	8000

One further requirement for a fail safe device is that is must withstand the 200V transient specified for the RPC. It was concluded that the best candidate for such a fail safe device as described above would be a fuse, if one could be found to meet the requirements.

If these RPC's are ever packaged using multi chip hybrid packaging techniques a discrete fuse will not be necessary. The chip interconnecting wires (bond wires) in such a design can be specified to provide the necessary I^2T failsafe ratings. Therefore, this fuse information is not necessary if and when hybrids are built.

Several types of fuses were considered, principally those of the Bussman Mfg. Co. The characteristic curves of the fuses were compared to the trip curves. A final selection of fuses was made on a basis of steady state rating and good fit between the trip curves and I^2t limit.

Figure 17 and figure 18 show the trip curves, I^2t limits, and fuse characteristic curves for the two types chosen.

Data on fuse temperature characteristics shows that melting characteristics, and physical dimensions, very substantially with temperature. Over the range of -55 to +100°C, the fuse melting current varies from 60% to 120%. This requires the steady state rating of the fuse to be above the minimum trip current of 6.0/60% = 10 Amps for the Type I and II RPC's and at least 36/60% = 60 Amps for the Type III RPC.

The "corner" of the I^2t specification provides an upper limit to the allowed fuse rating. So, for the type I and II RPC's the maximum one second rating for the fuse is 25/120% = 20.33 Amps and for the Type III RPC the .35 second rating is 150/120% = 125 Amps. These requirements allowed a fast search for possible candidates for the fail safe device.

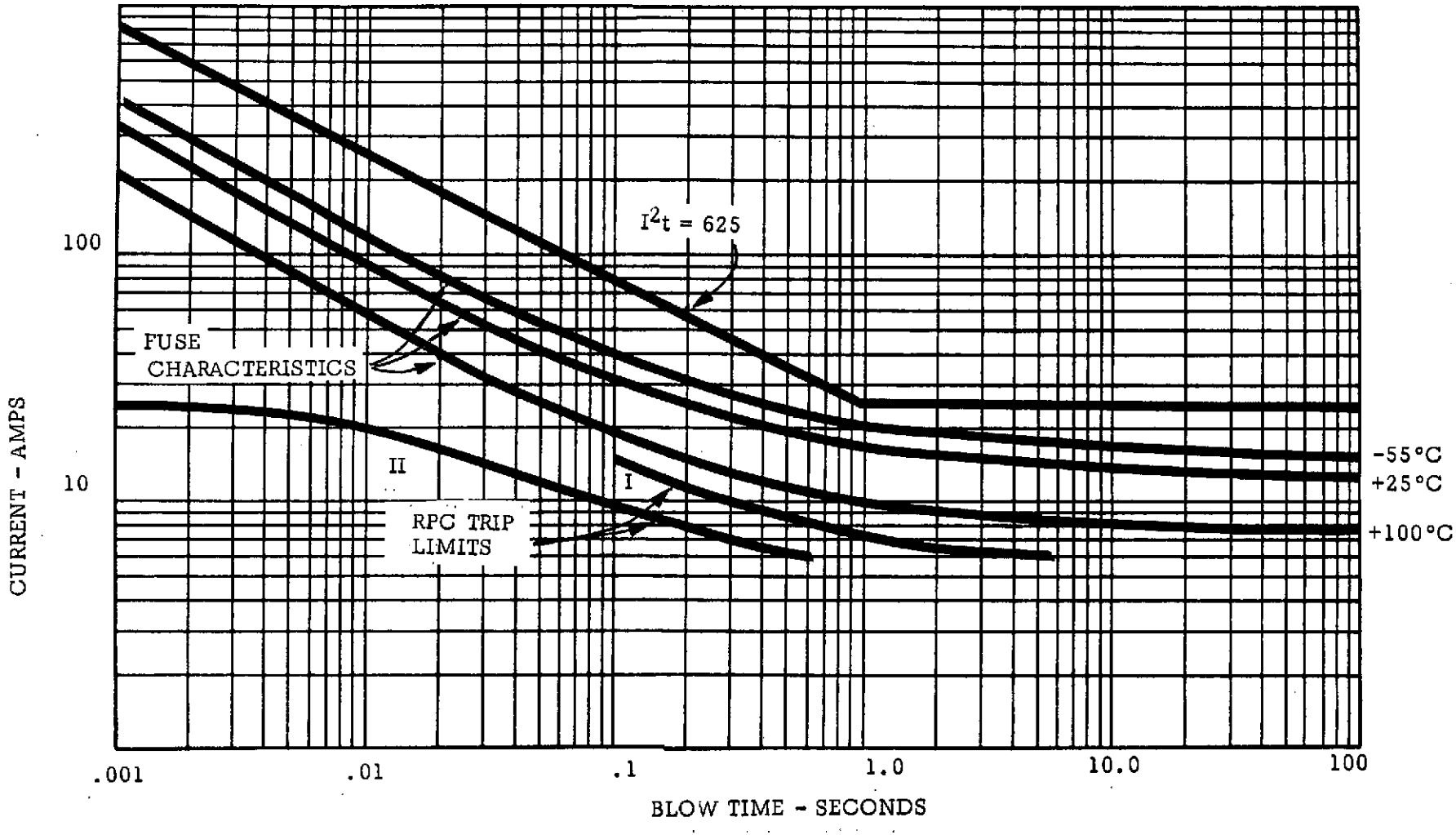

Figure 17-KAB-10 Fuse Characteristics

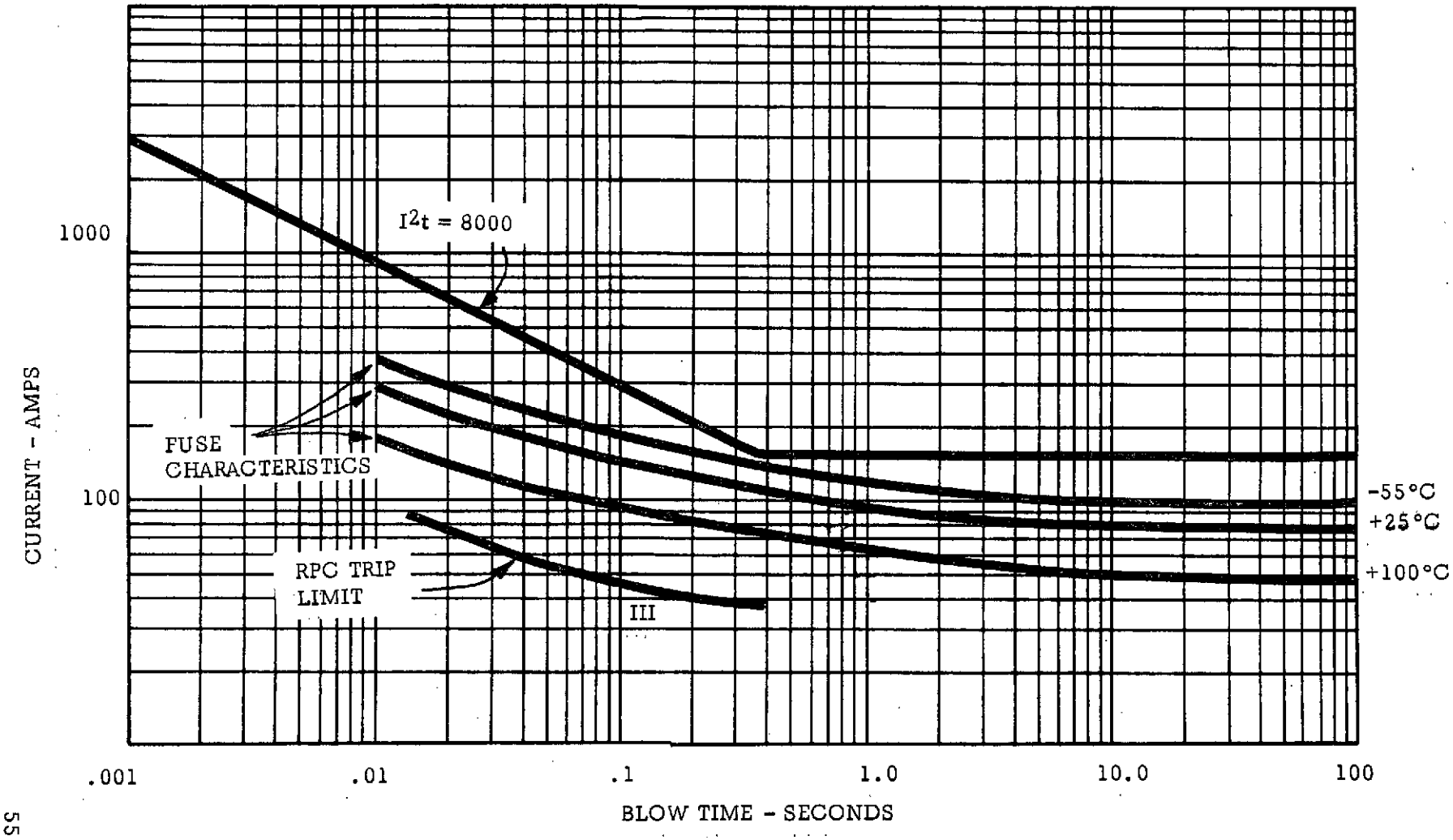

Figure 18 KAX-60 Fuse Characteristics

4.0 Task 2 - Switchgear Breadboards: Design, Fabrication & Evaluation

The objective of this task was to design, build, and evaluate a complete breadboard of each of the 3 types of RPC's. Each breadboard was tested in the laboratory over the entire temperature range to determine if the circuits and concepts could meet the performance requirements. The testing revealed areas of circuits deficiencies that were later corrected. However, the basic concepts were verified as capable of meeting the performance requirements. The details of the evaluation are discussed in this section.

4.1 Breadboard Circuits

The breadboards that were constructed for evaluation were an assemblage of the sub-circuits discussed in section 3.0 of this report. During preliminary testing it became apparent that some minor circuit modifications were necessary. The nature of the problems and the resulting circuit changes are discussed below. The final circuit, incorporating all the changes, are shown by figures 19, 20, and 21. These schematic diagrams represent the circuits which were built and evaluated during Task 4, Fabrication of Engineering Models and Task 5, Testing the Engineering Models.

Each of these schematics includes a series voltage regulator, which was not discussed in section 3.0 of this report. This regulator consists of transistor Q202, Zener CR207, and resistor R217. It furnishes power to the trip circuit and to the logic circuit via the same current path and, therefore, minimizes power dissipation. Voltage to the trip circuit is regulated to 30 volts by CR207 and Q202 and voltage to the logic circuit to 15 Volts by CR306.

The following circuit changes were made on all 3 circuit types. Referring to figures 19, 20, and 21:

A) Capacitors C203 and C307 were added to reduce noise susceptability of the trip logic circuit. The values of the capacitors were selected so as to provide adequate noise rejection with little effect on the trip circuit propagation time.

B) Zener diode CR212 was substituted for a resistor in order to improve the rise time of the trip signal at the collector of Q201. This in turn helped minimize the propagation time of the trip circuit.

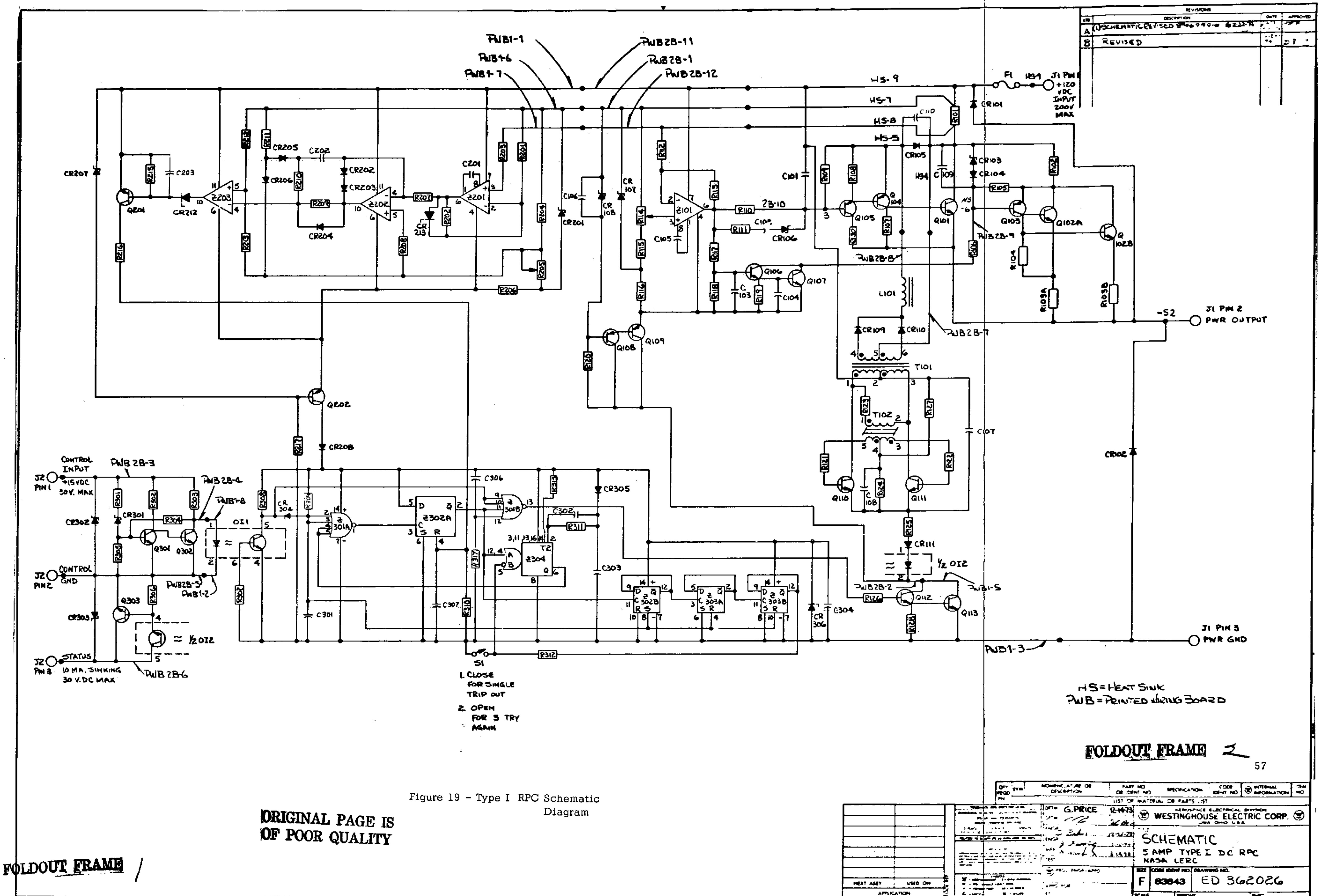

Figure 19 - Type I RPC Schematic Diagram

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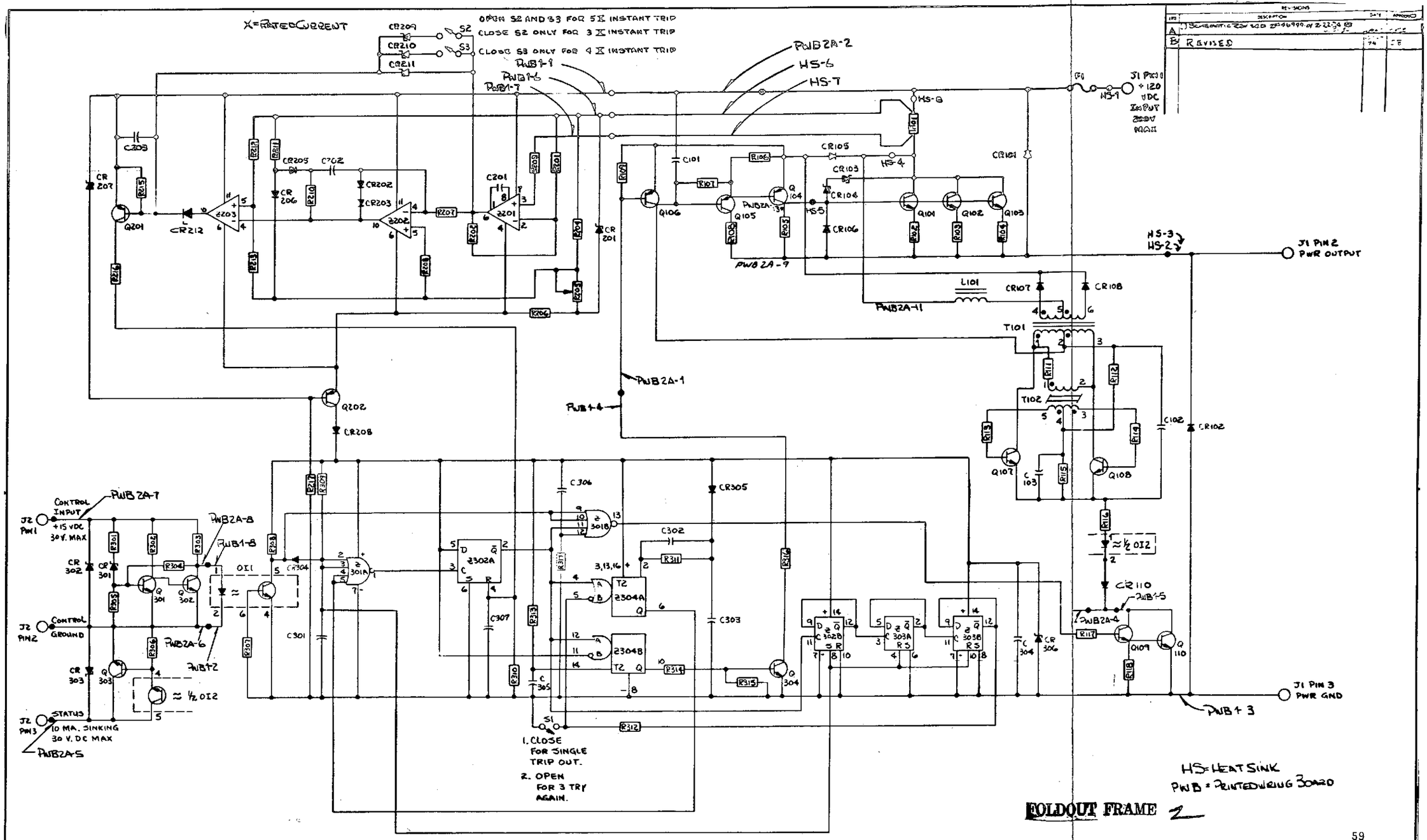
FOLDOUT FRAME 1



FOLDOUT FRAME 2

FOLDOUT FRAME 1

Figure 20 - Type II RPC Schematic Diagram

DRAWN	G. PRICE	2-18-73
ENGR		
ENGR		
MFG		
TEST		

WESTINGHOUSE ELECTRIC CORP.

TITLE: SCHEMATIC 5 AMP TYPE II DC RPC NASA LERC

SIZE F | FSCM NO 83843 | DRAWING NO ED 362029

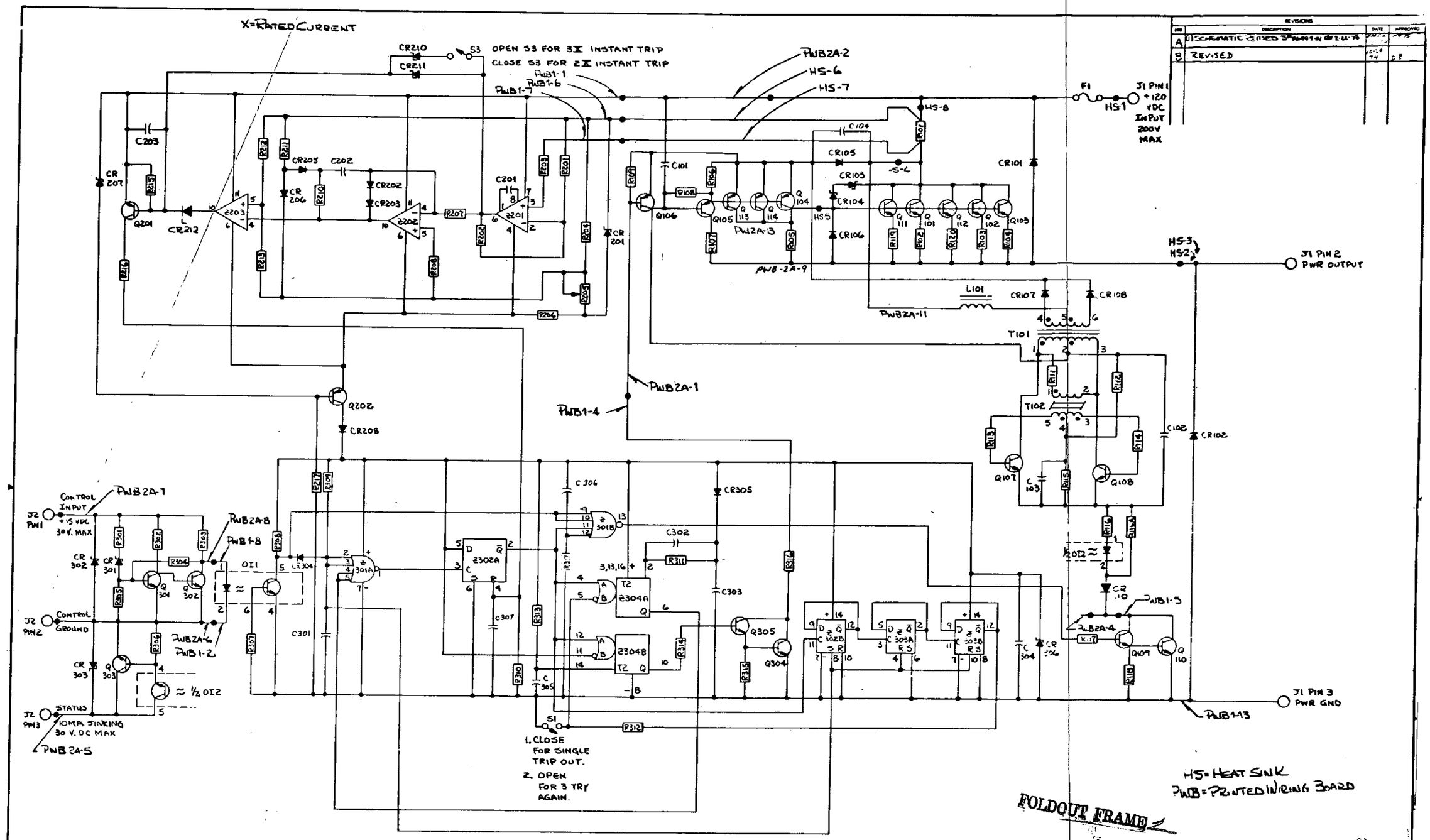


Figure 21 - Type III RPC Schematic Diagram

C) Capacitor, C301; diode, CR304, and resistor, R309, were added to provide a reset time delay. This time delay is set for 15 $\pm$ 5 milliseconds and is needed to insure that noise, such as switch contact bounce on the control input, does not reset the RPC from a tripped state. This is especially important for the instant trip Type II & III designs. For example, without the reset delay and with a shorted load the RPC could turn on, trip off and reset once for each contact bounce of the external control switch. Hence, the RPC could complete several high energy stress cycles within one or two milliseconds and result in damage to the power stage.

D) Capacitor C306 and resistor R317 were added to terminal 12 of Z301B. Upon energizing the RPC this circuit inhibits turn on of the power stage until after the trip and logic circuits are fully energized and properly initialized. Without this change the trip and logic circuits can "get lost" when the RPC is first energized and hence allow excessive current flow to a faulted load resulting in failure of the RPC.

E) Zener diode CR213 was added to the Type I RPC only. This diode prevents the transient current limiting overshoot from triggering an instant trip. Hence a full .1 second current limiting period is insured before trip off.

4.2 Breadboard Tests

Subsequent to the above modifications the breadboards were tested under conditions similar to those anticipated for the Engineering Models. These conditions included ambient temperatures of -55°C, +25°C, and +100°C. The tests were performed with a test set up designed to maximize surge current capability to insure stiff source compatibility. This was done by minimizing impedances in the power circuit loop. The test circuit which was used is defined by Figure 22 and Table 5. It is capable of delivering fault currents in excess of 4000 amperes as shown by figure 8.

Parameters evaluated during the breadboard tests were:

A. Static Performance at 60, 108, 120, and 132 Vdc.

1. Voltage drop at rated load resistance (on)
2. Power dissipation = $V_{switch} \times I_{load} + V_{bus} \times I$ gnd.
3. Efficiency at rated load resistance (on)
4. Leakage current (off)
5. Turn on and turn off voltage

B. Dynamic Performance

1. Turn on time and rise time
2. Turn off time and fall time
3. Automatic reset
4. Trip time delay conformance
5. Transient bus voltage
6. Current limiting (Type I)
7. Response to fault overloads
8. Incandescent lamp load (start capability)

4.3 Breadboard Test Results

The breadboard test data given in this report represents only a portion of all the data taken. The data that is of most significance is given herein. Should it be needed, the original data, in its entirety, is in Monthly Progress Report No. 7.

Table 5 - Breadboard Test Circuit Definition

The following is a component definition list for the test circuit schematic as defined by figure 22.

V_{Bus} Supply	Harrison Type 6475, 0-120 Volt, 0-100 Amp, Approx. 120,000 micro-farad output filter capacitor
V_{cont} Supply	0-30 Volt, 500 milliamp supply
R_{Load}	Variable Resistance, 0 to 50 ohms. 600 W at 24 ohms and 3.6KW at 4 ohms.
Power Circuit Impedance	#2 Copper stranded welding cable everywhere load current or fault current flows. 26 feet total length maximum.
Switch S2, S3	200 Amp knife switch
Fault Contactor	Hartman AR751FC, 200 Amp, 224 Volt dc, S.P.S.T. Contactor
V_1, V_2	Dana 4470 Digital Voltmeter
Oscilloscope	Tektronix 533, .022 micro-second rise time
Shunt	Non-inductive current metering shunt. T & M Research Products 1M-20, .01 ohm.

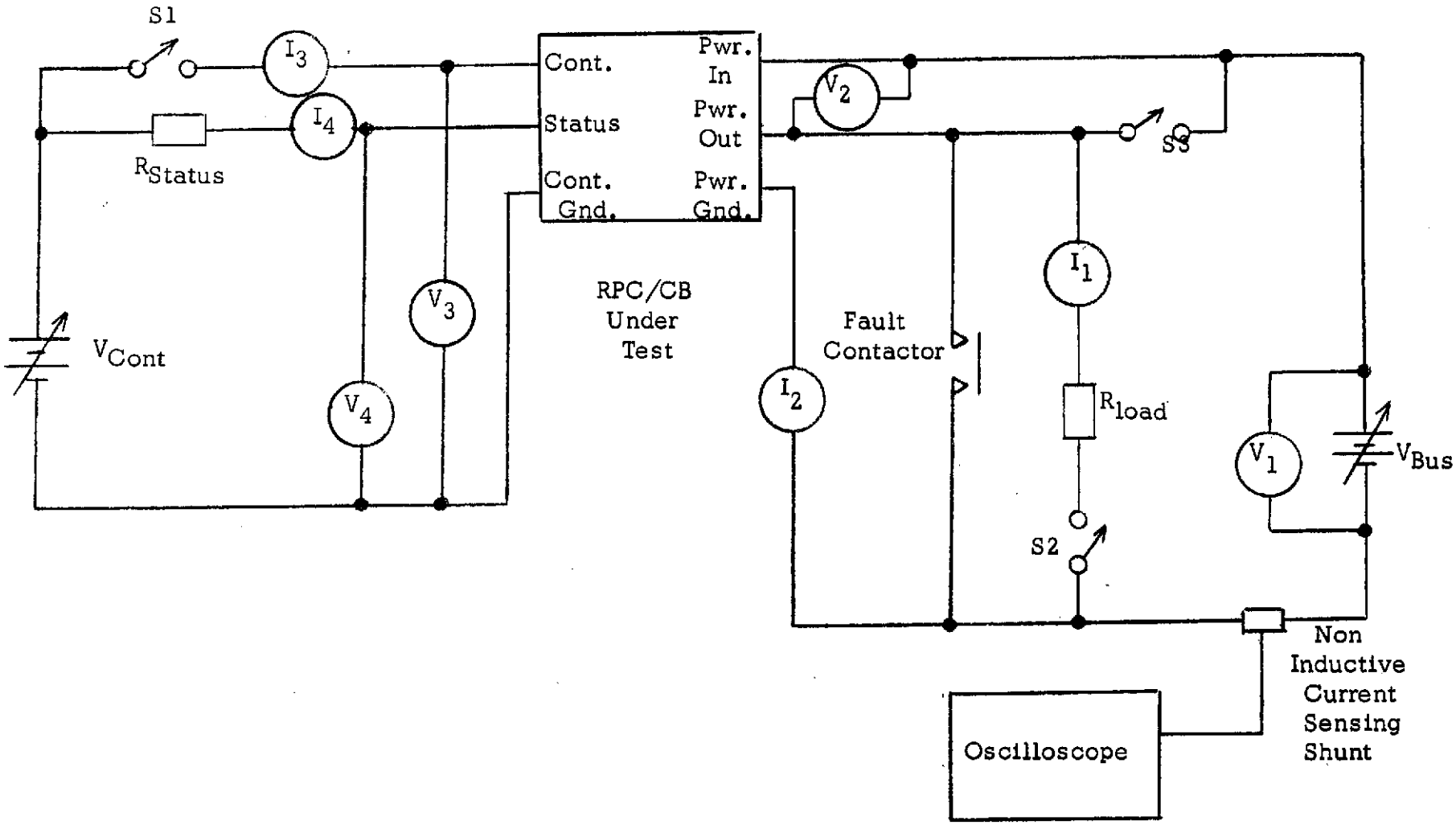


Figure 22-RPC Test Circuit

4.3.1 Type I

Key static and dynamic performance parameters of the breadboard as a function of bus voltage and temperature are plotted in figures 23 through 28. Figures 29 through 31 are photographs of actual performance which show the turn on and turn off characteristics and the response to applied short circuit faults. Applied faults are, as mentioned earlier, the worst case faults. Other pertinent test data is given in Table 6.

Table 6 - Test Data - Type I RPC Breadboard

Item	-55°C	+25°C	+100°C	Units
Turn On Voltage	7.9	8.0	7.9	Volts
Turn Off Voltage	7.8	7.9	7.8	Volts
Auto-Reset Delay Time	.8	.87	.85	Seconds
Incandescent Lamp Start Capability	600+	600+	600+	Watts
Current Limiting Ripple	.1	.25	.2	Amps P-P
Current Limiting Response Time	——	100	400	Micro-seconds
Current Limiting Peak Current	16	27	21	Amps
200 Volt Transient	OK	OK	OK	

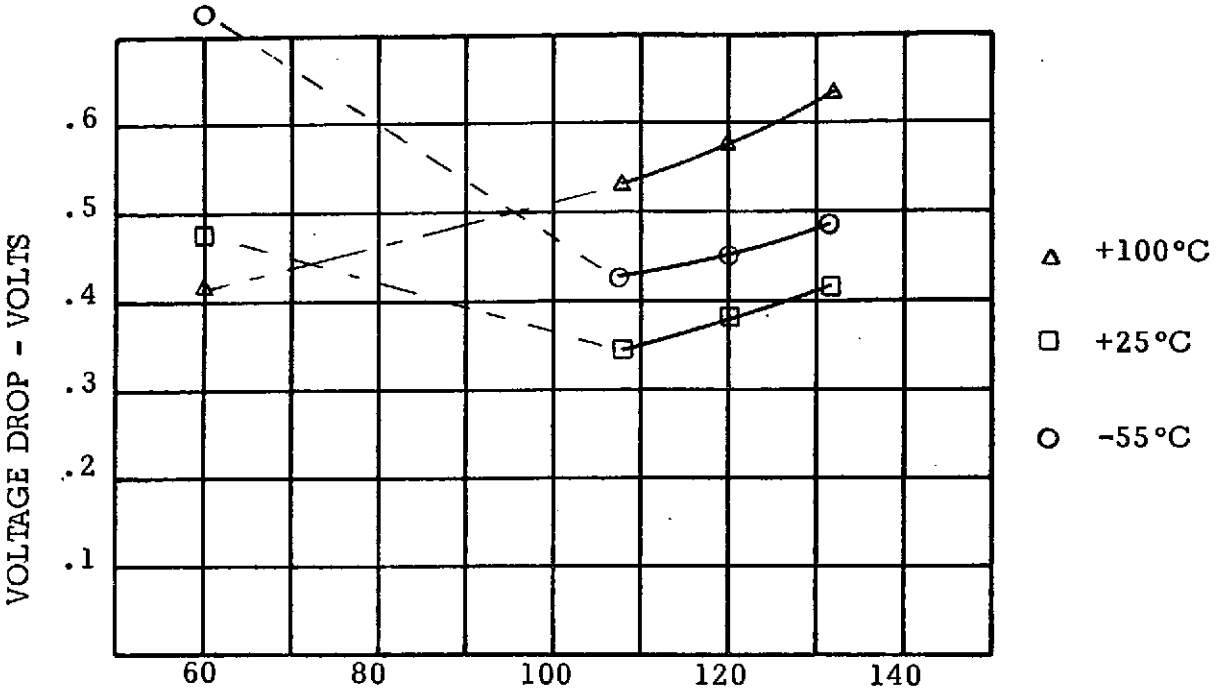
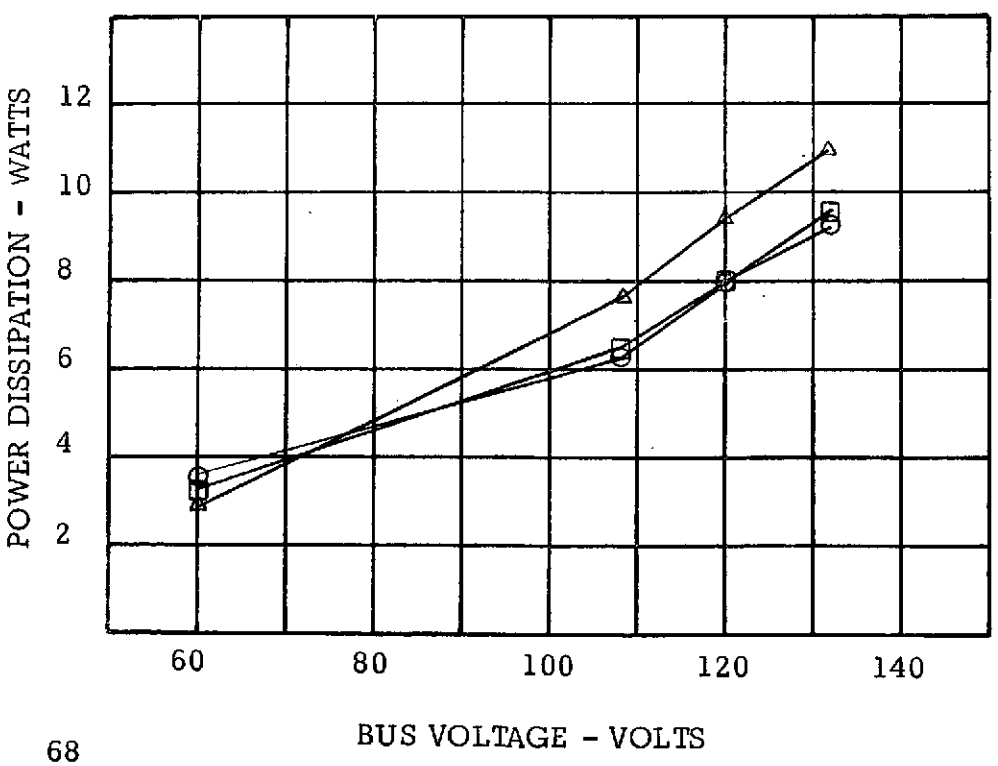


FIGURE 23 - TYPE I BREADBOARD VOLTAGE DROP DATA

FIGURE 24 - TYPE I BREADBOARD DISSIPATION DATA



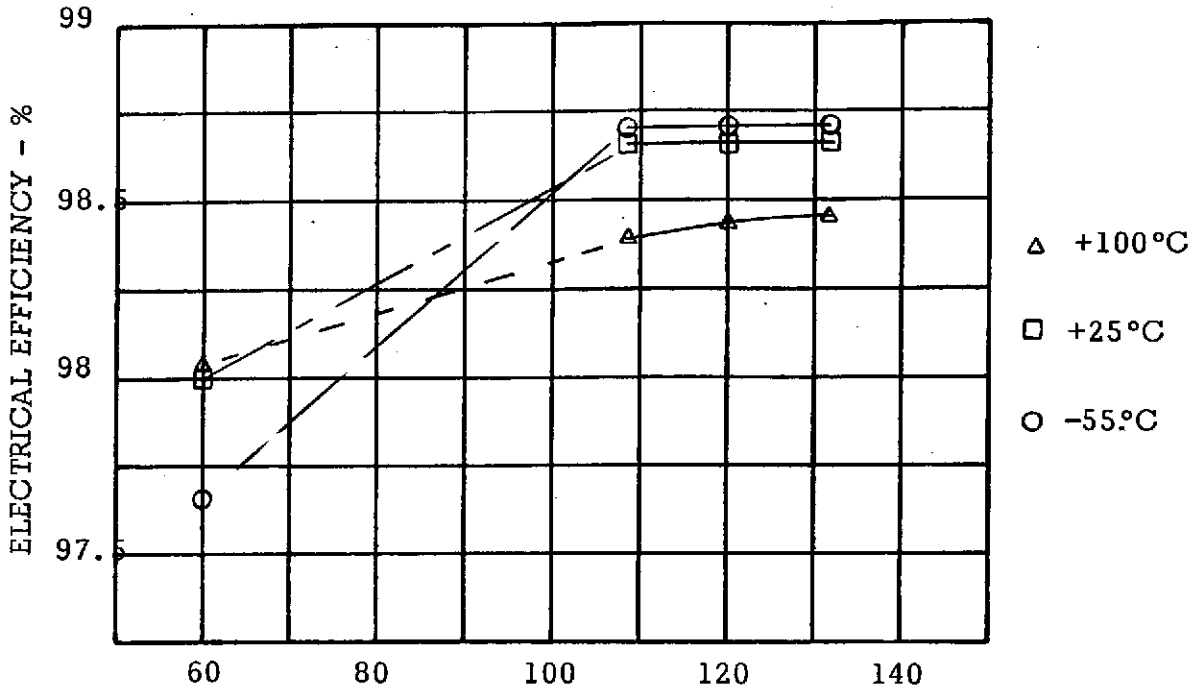
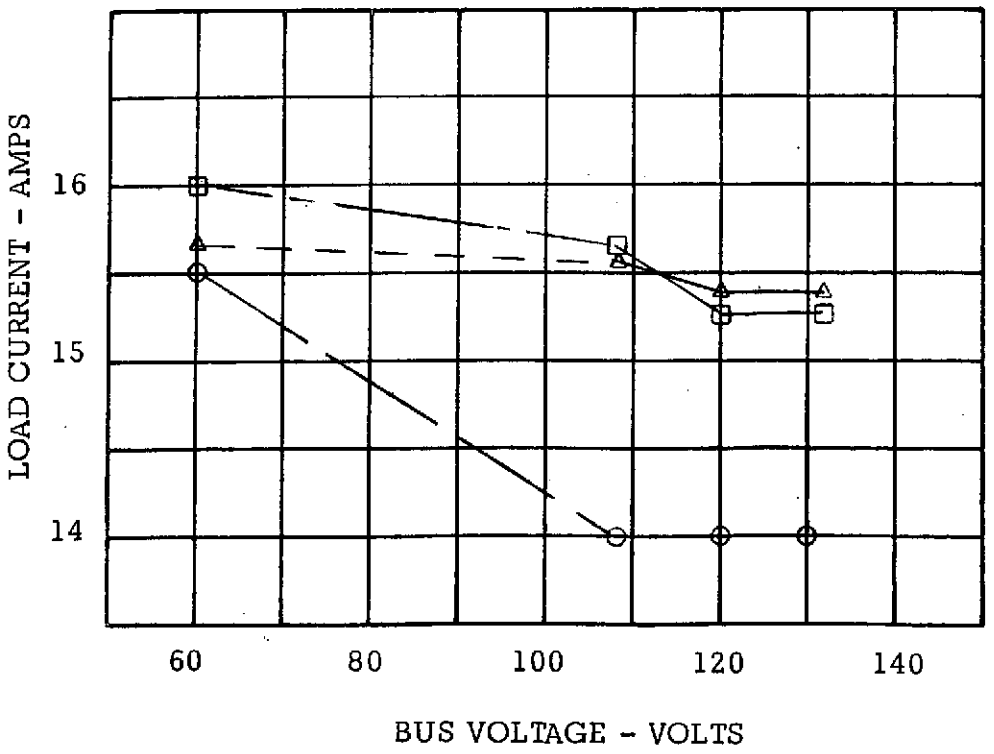


FIGURE 25-TYPE I BREADBOARD EFFICIENCY DATA

FIGURE 26- TYPE I BREADBOARD CURRENT LIMITING DATA WITH SHORT CIRCUIT LOAD.



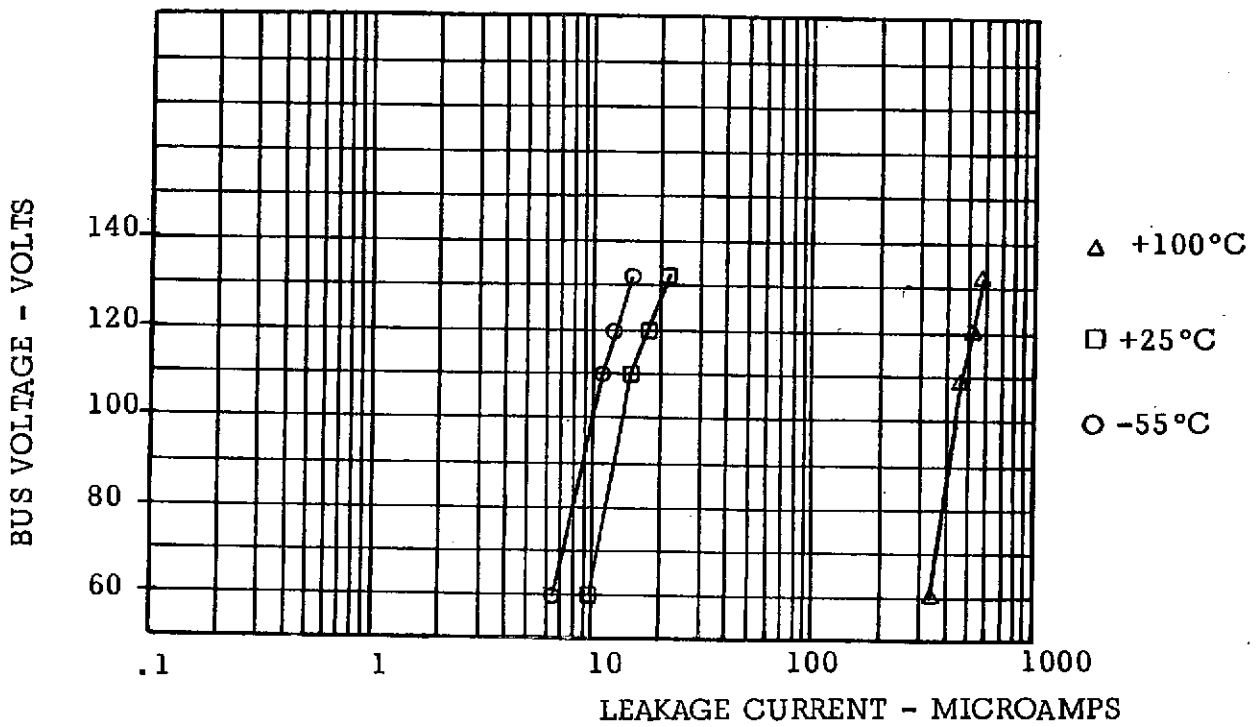
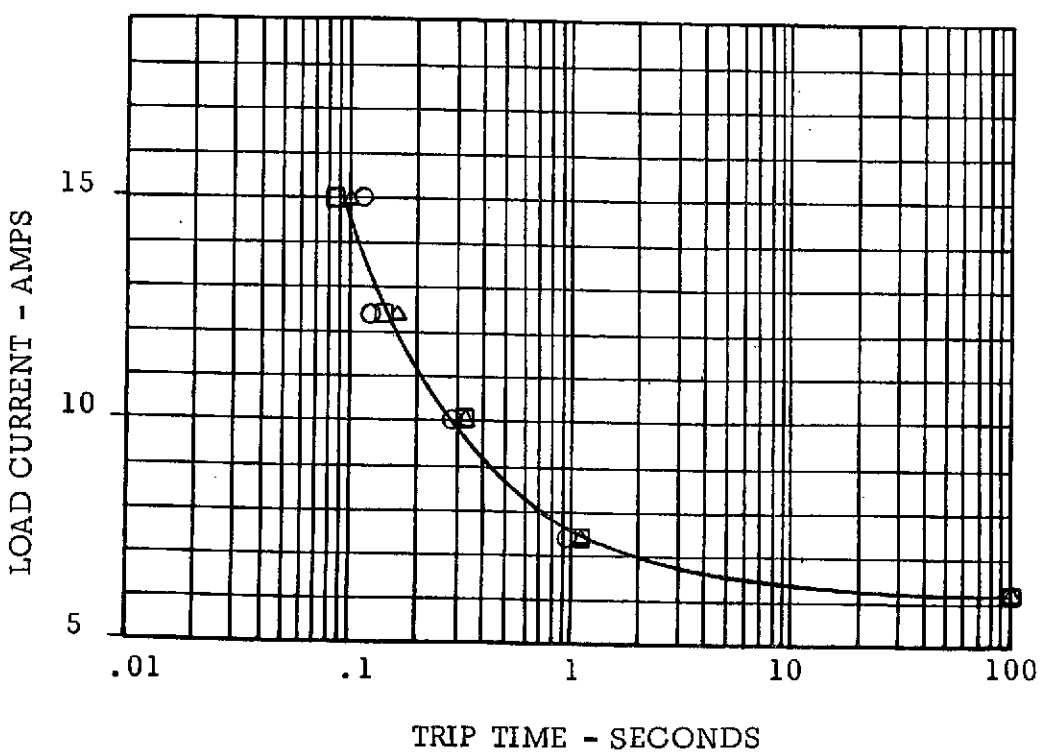


FIGURE 27 - TYPE I BREADBOARD LEAKAGE CURRENT DATA

FIGURE 28 - TYPE I BREADBOARD TRIP TIME DATA



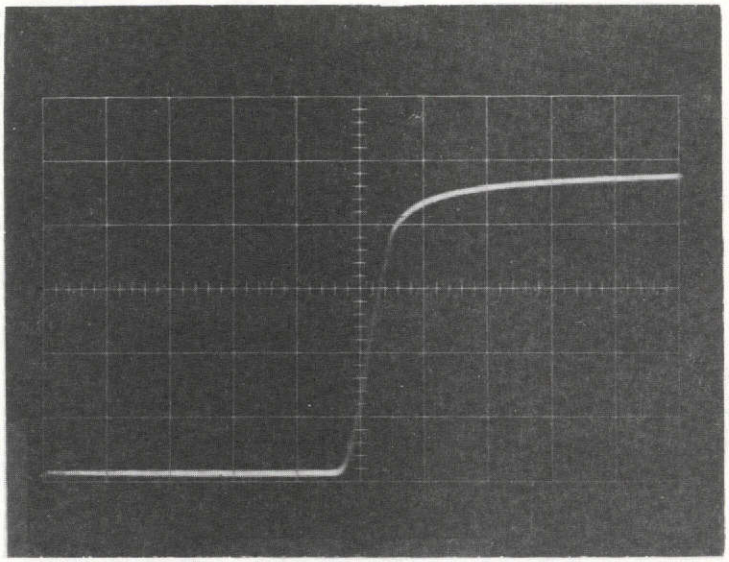


FIGURE 29 - TYPE I Turn On time

Vertical: Load Current, 1 amp/div.

Sweep: .1 millisecond/div.

V_{BUS} = 120 VDC, R_{LOAD} = 24 ohm

Temp. = 25°C

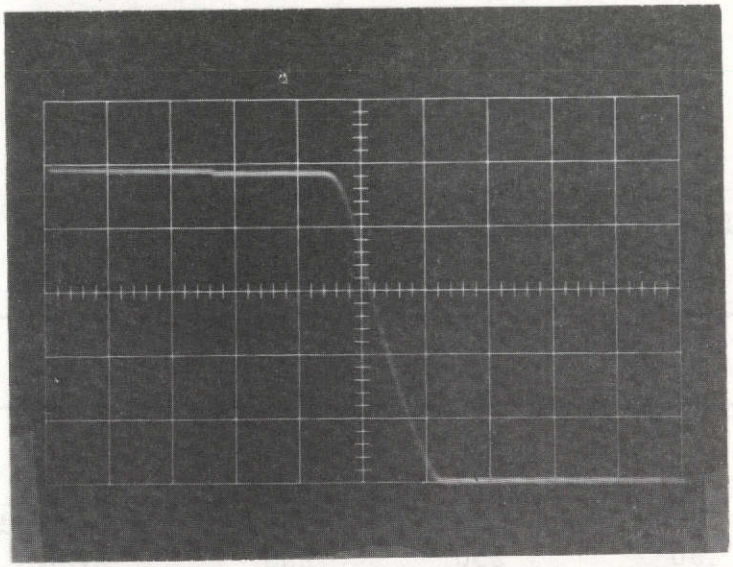


FIGURE 30-TYPE I Turn Off time

Vertical: Load Current, 1 amp/div.

Sweep: 50 microseconds/div.

V_{BUS} = 120 VDC, R_{LOAD} = 24 ohms

Temp. = 25°C

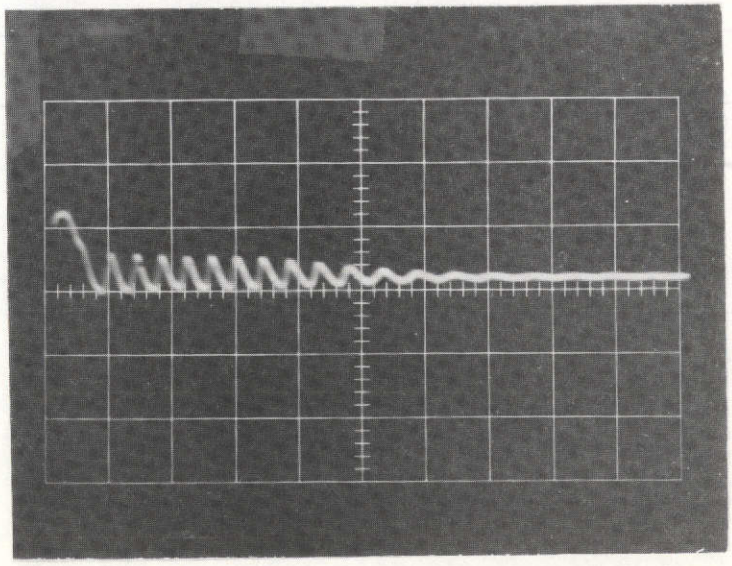


FIGURE 31-Current Limiting Response.

Applied Fault

Vertical: Load Current, 5 amp/div.

Sweep: .5 millisecond/div.

V_{BUS} = 120 VDC, Temp. = 100°C

R_{LOAD} (T = 0-) = 24 ohm

R_{LOAD} (T = 0+) = 0 ohm

4.3.2 Type II

Plots of the key static and dynamic performance data are shown by figures 32 through 36. Figures 37 through 39 are photographs of actual breadboard performance which show the turn on and turn off characteristics and the response to a worst case applied fault.

Other pertinent data is given in Table 7.

Table 7 - Test Data - Type II RPC Breadboard

Item	-55°C	+25°C	+100°C	Units
Turn On Voltage	7.6	7.6	7.5	Volts
Turn Off Voltage	7.5	7.4	7.4	Volts
Auto Reset Delay Time	.833	.833	.833	Seconds
Lamp Start Capability	250	250	250	Watts
Short Circuit Response Time (Applied)	0	3	3	Micro-seconds
Short Circuit Peak Current (Applied)	25	60	70	Amps
200 Volt Transient	OK	OK	OK	

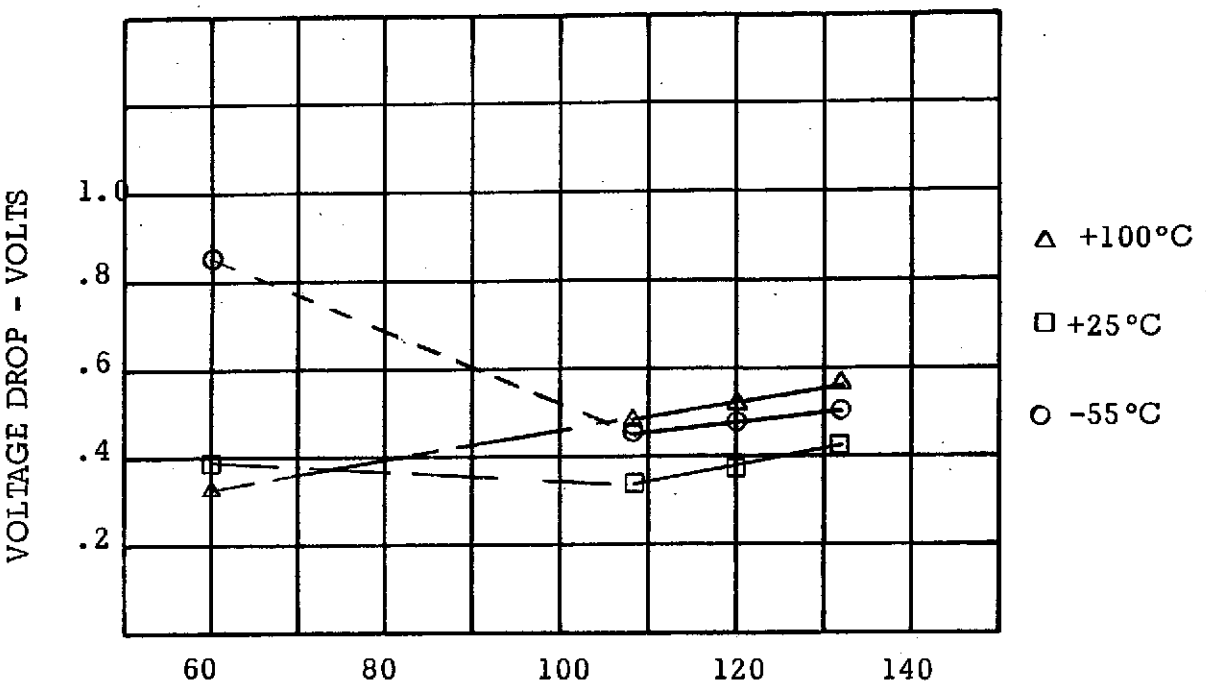
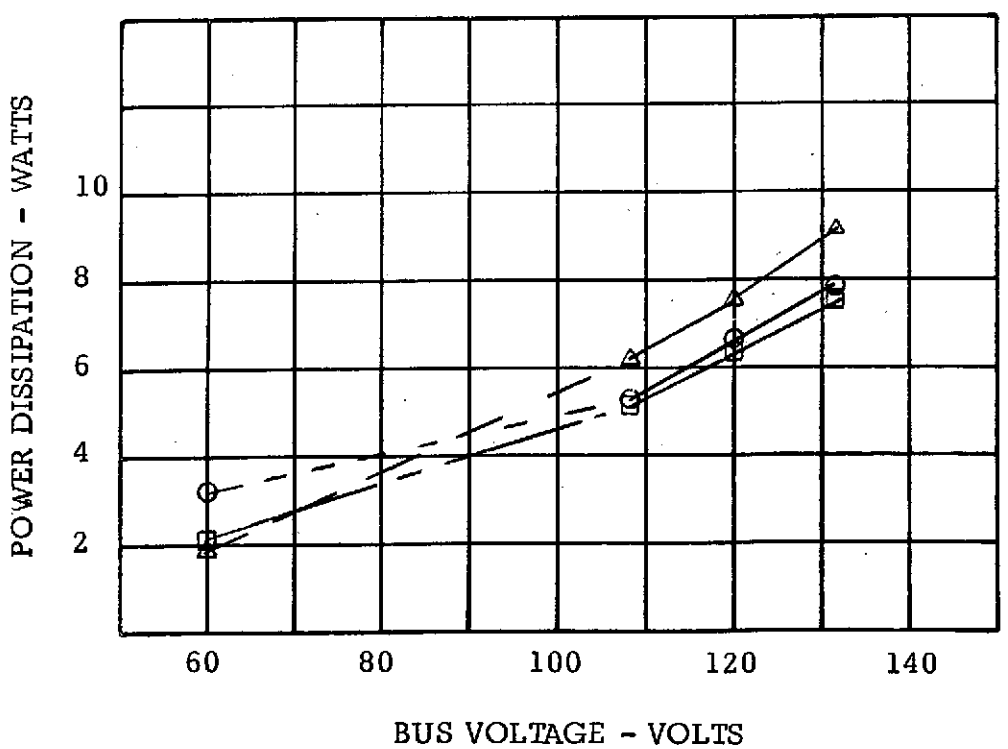


FIGURE 32 - TYPE II BREADBOARD VOLTAGE DROP DATA

FIGURE 33 - TYPE II BREADBOARD DISSIPATION DATA



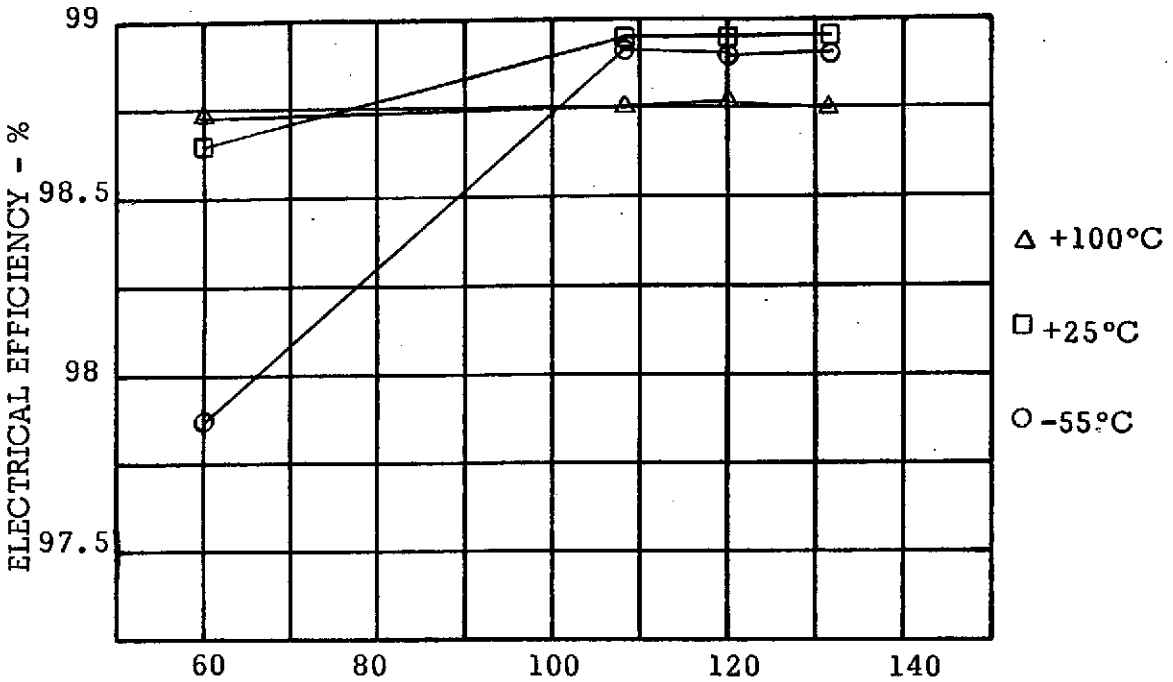


FIGURE 34 - TYPE II BREADBOARD EFFICIENCY DATA

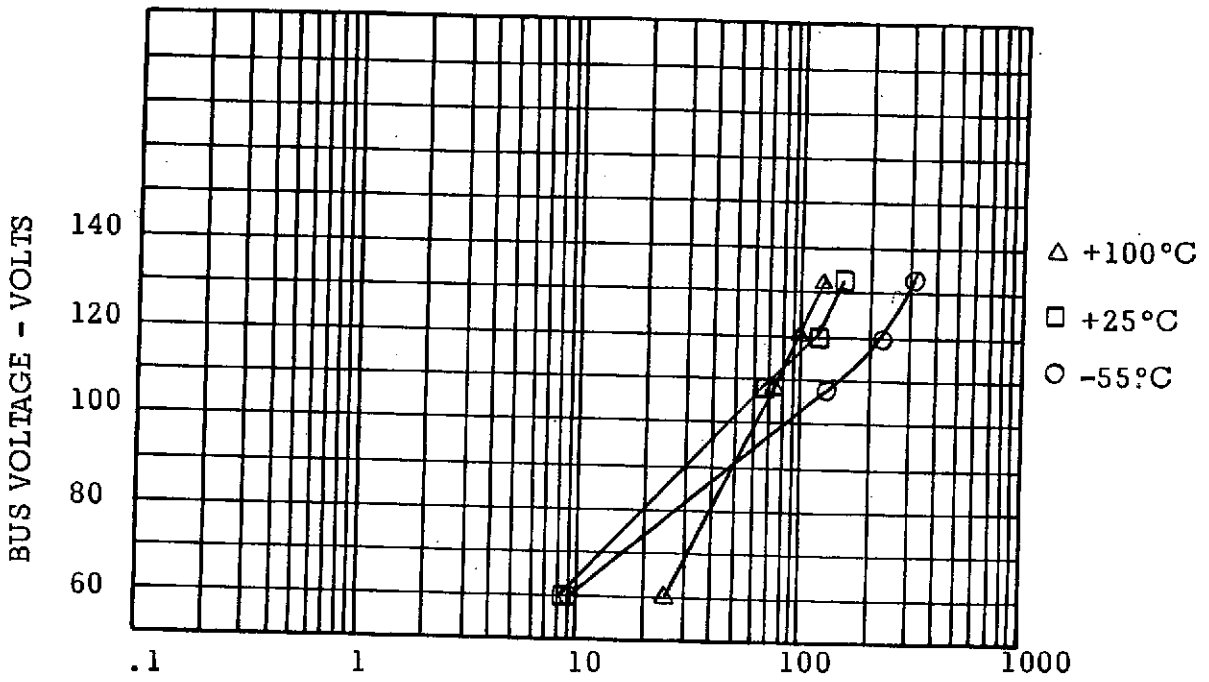
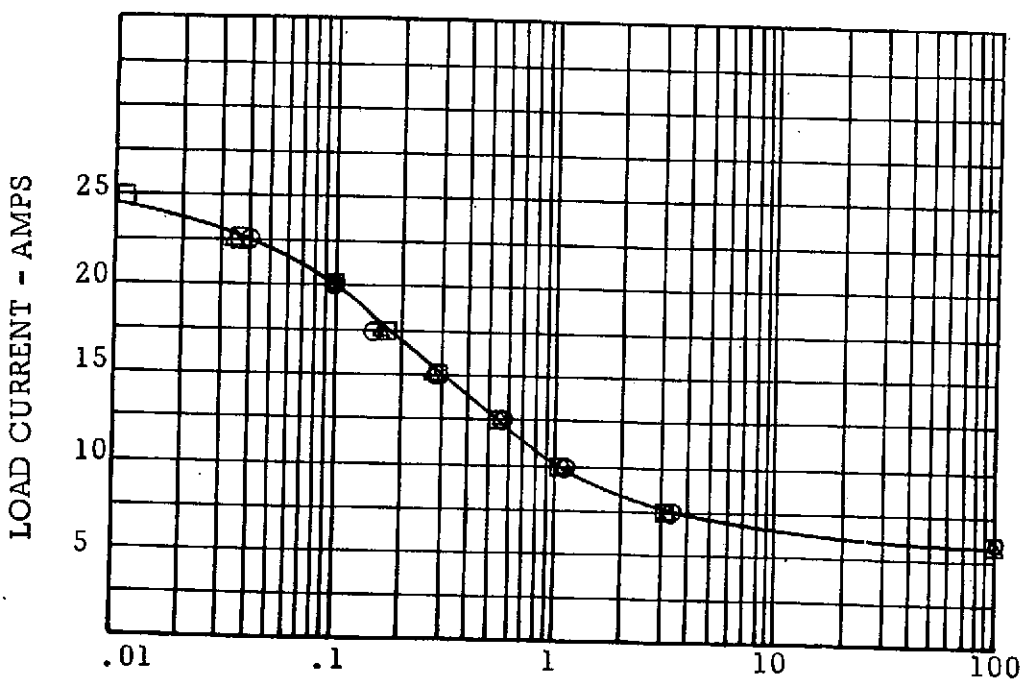


FIGURE 35 - TYPE II BREADBOARD LEAKAGE DATA

FIGURE 36 - TYPE II BREADBOARD TRIP TIME DATA



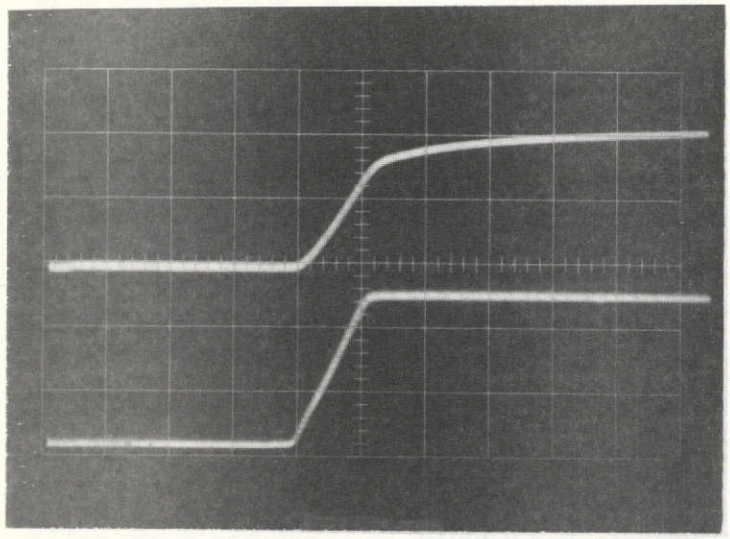


FIGURE 37 - TYPE II Turn On Time

Vertical: Top, Load Current, 2.5 Amp/div.
Bottom, Load Voltage, 50 volts/div.

Sweep: 20 micro seconds/div.

V_{BUS} = 120 VDC, R_{LOAD} = 24 ohms

Temp. = 25°C

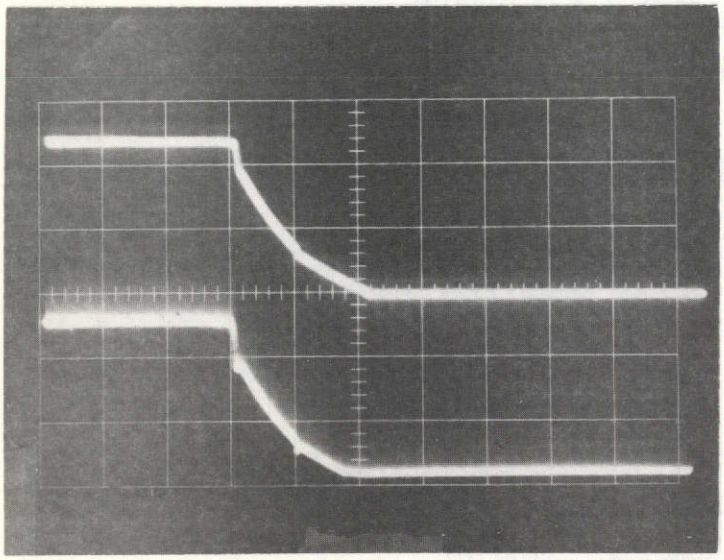


FIGURE 38 - TYPE II Turn Off Time

Vertical: Top, Load Current, 2.5 amp/div.
Bottom, Load Voltage, 50 volts/div.

Sweep: 100 micro seconds/div.

V_{BUS} = 120 VDC, R_{LOAD} = 24 ohms

Temp. = 25.C

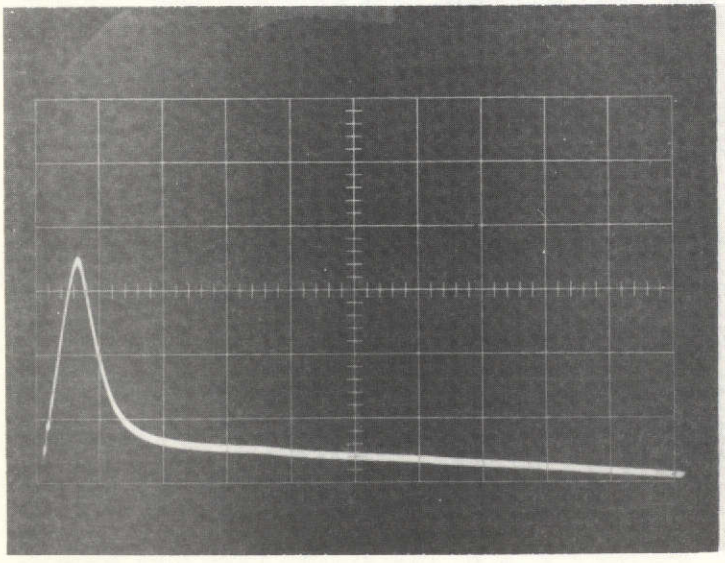


FIGURE 39 - TYPE II Instant Trip Response Time, Applied Fault

Vertical - Load current, 20 amps/div.

Sweep - 10 micro seconds/div.

V_{BUS} - 120 VDC, Temp = 100°C

R_{LOAD} (T = 0-) = 24 ohms

R_{LOAD} (T = 0+) = 0 ohms

4.3.3 Type III

Plots of the key static and dynamic performance are shown by figures 40 through 44. Figures 45 through 47 are photographs of actual breadboard performance which show the turn on and turn off characteristics and the response to a worst case applied fault.

Other pertinent data is given in Table 8.

Table 8 - Test Data - Type III RPC Breadboard

Item	-55°C	+25°C	+100°C	Units
Turn On Voltage	7.6	7.6	7.6	Volts
Turn Off Voltage	7.4	7.4	7.4	Volts
Auto Reset Time Delay	.83	.84	.9	Seconds
Incandescent Lamp Start Capability	1080	1080	1080	Watts
Short Circuit Response Time (Applied)	0	5	10	Micro-seconds
Short Circuit Peak Current (Applied)	100	110	135	Amps
200 Volt Transient	OK	OK	OK	

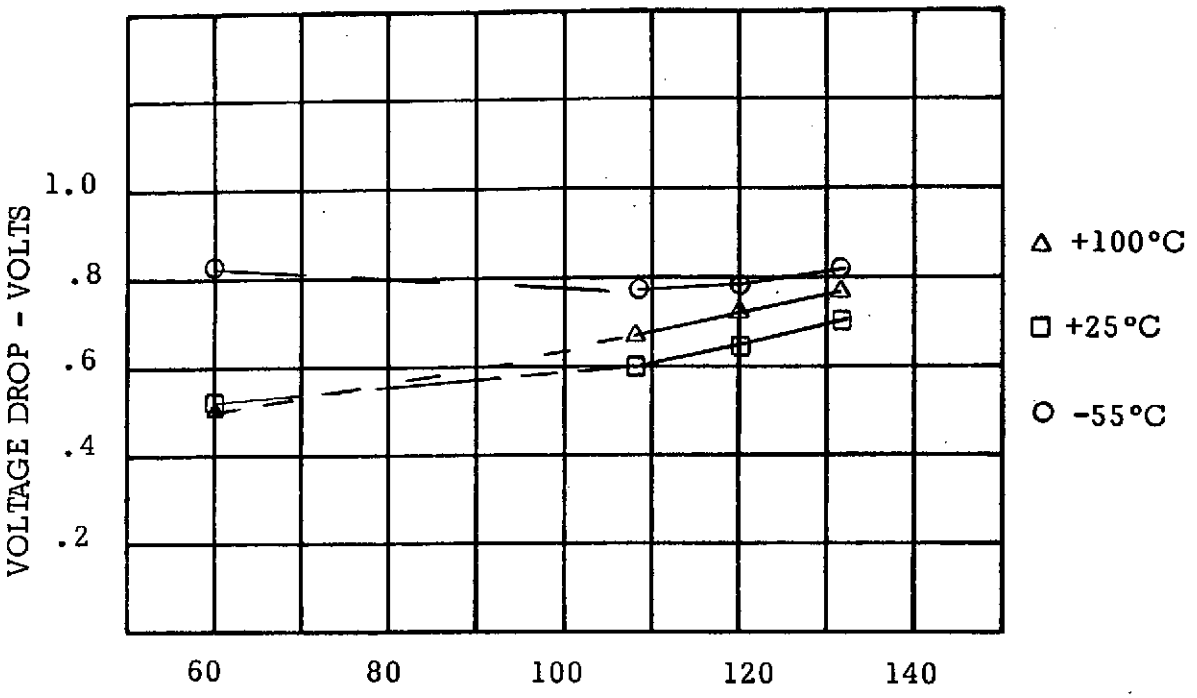
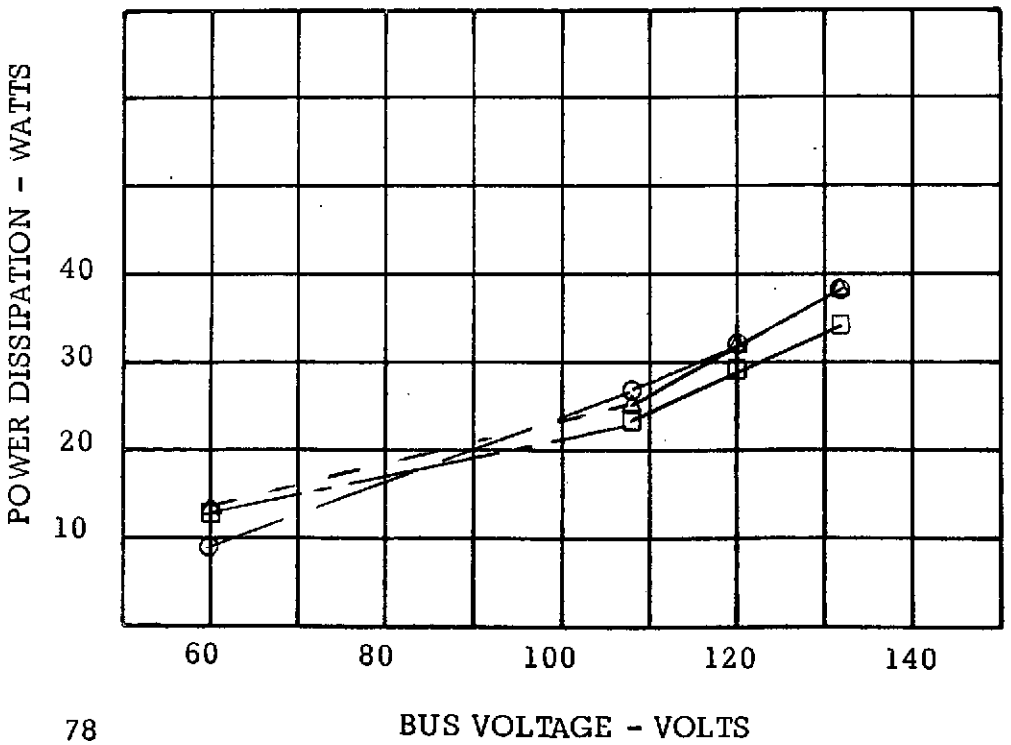
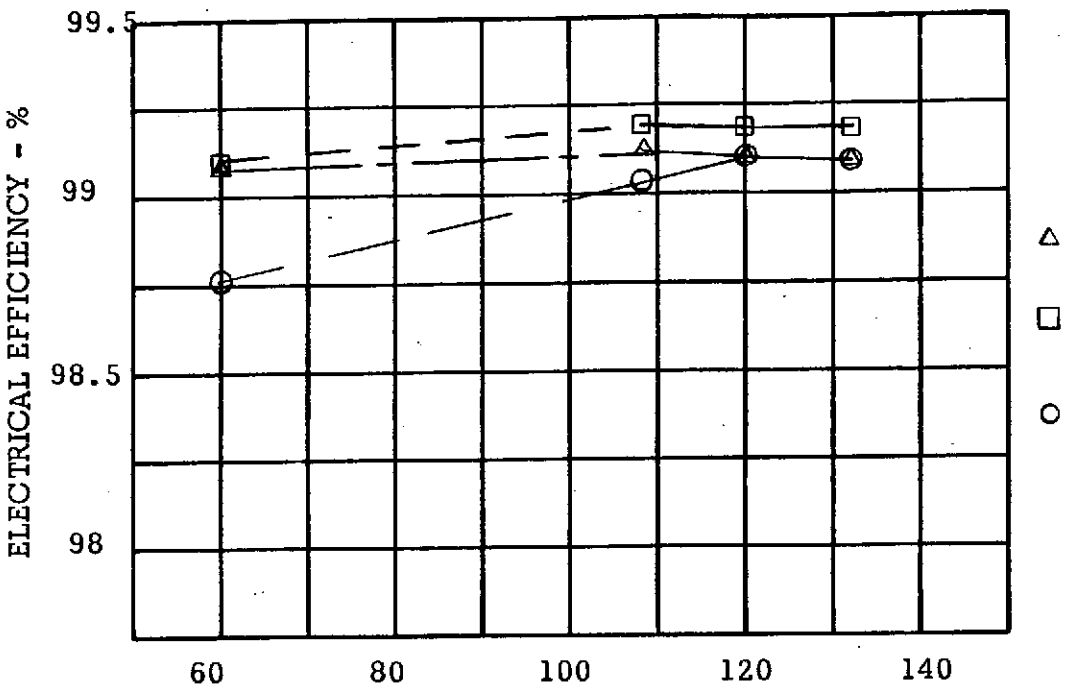


FIGURE 40 - TYPE III BREADBOARD VOLTAGE DROP DATA

FIGURE 41 - TYPE III BREADBOARD DISSIPATION DATA





BUS VOLTAGE - VOLTS

FIGURE 42 - TYPE III BREADBOARD EFFICIENCY DATA

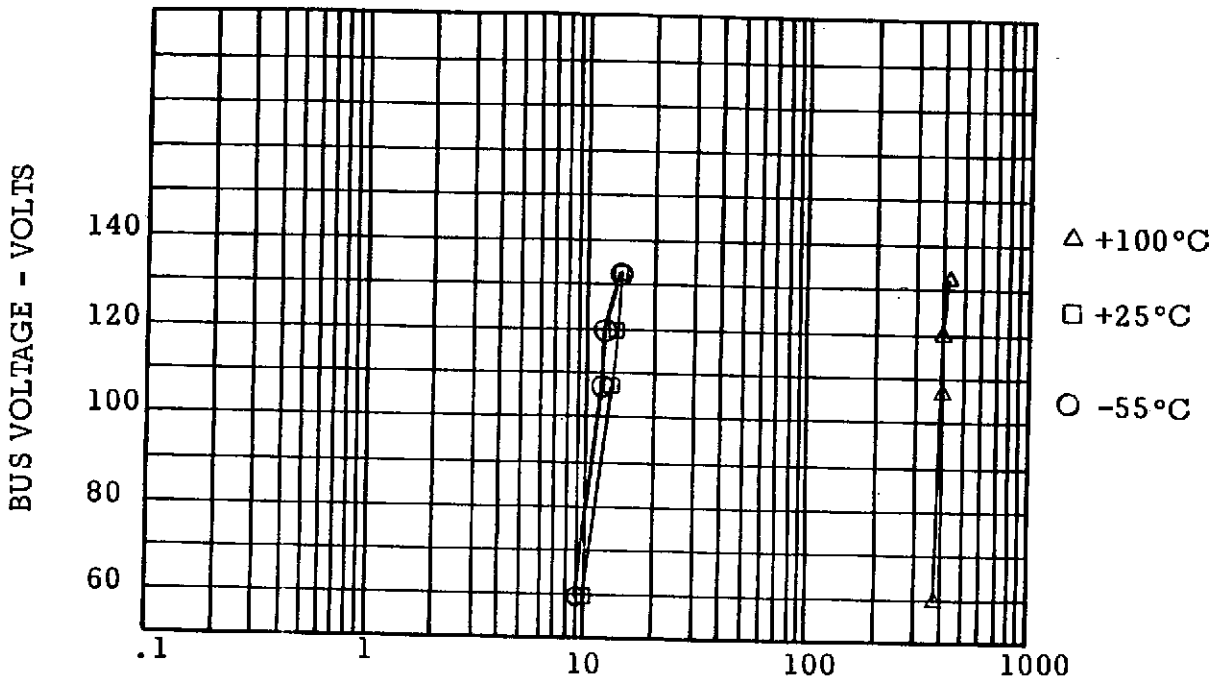
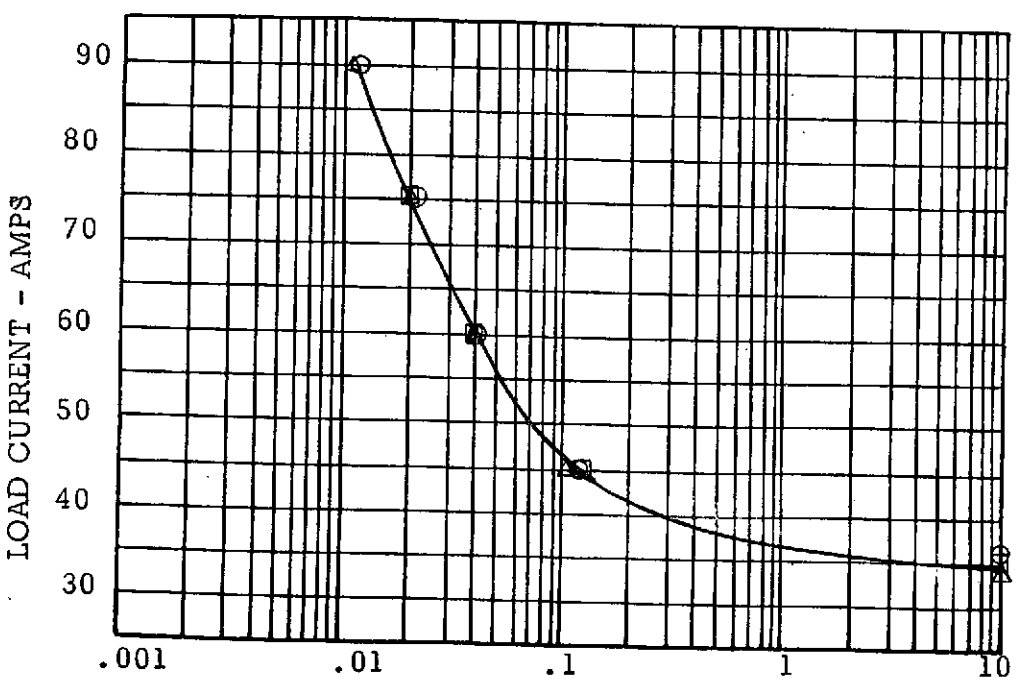


FIGURE 43 - TYPE III BREADBOARD LEAKAGE DATA

FIGURE 44 - TYPE III BREADBOARD TRIP TIME DATA



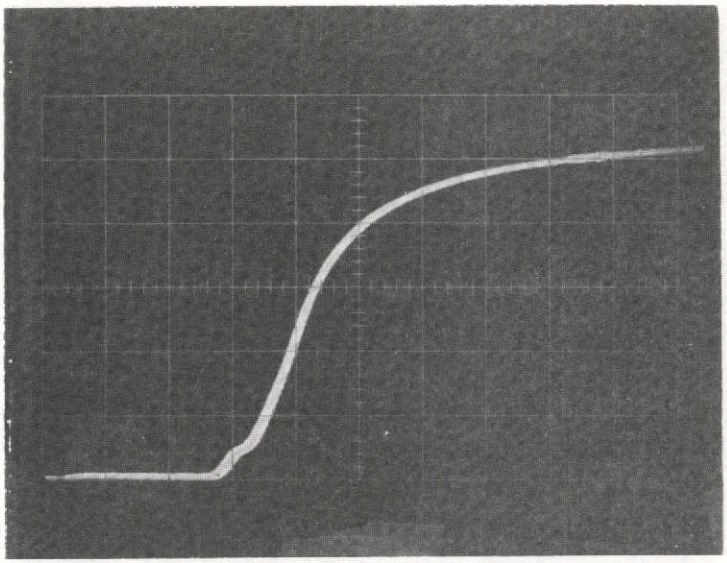


FIGURE 45 - TYPE III Turn On Time

Vertical: Load Current, 5 amp/div.

Sweep: 20 microseconds/div.

V_{BUS} = 120 VDC R_{LOAD} = 4 ohms.

Temp. = 25°C

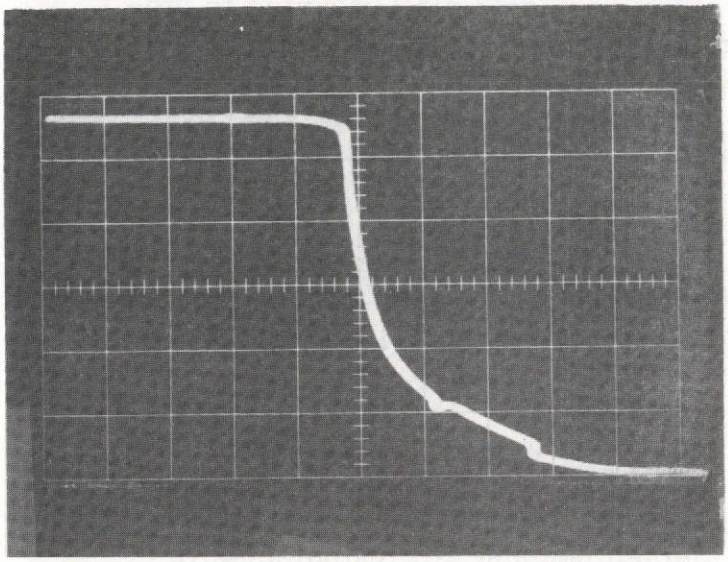


FIGURE 46 - TYPE III Turn Off Time

Vertical: Load Current, 5 amp/div.

Sweep: 50 microseconds/div.

V_{BUS} = 120 VDC, R_{LOAD} = 4 ohms

Temp. = 25°C

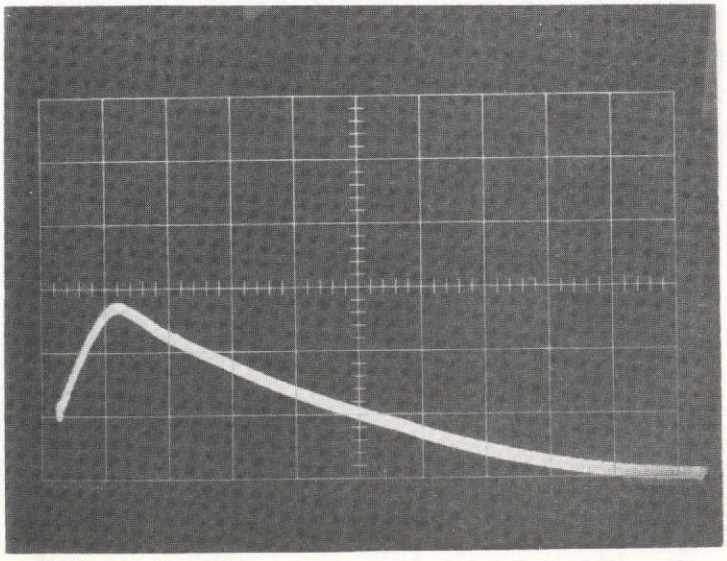


FIGURE 47 - TYPE III Instant Trip Response Time, Applied Fault

Vertical: Load Current, 50 amp/div.

Sweep: 10 microseconds/div.

V_{BUS} = 120 VDC, Temp. 100°C

R_{LOAD} (T = 0-) = 4 ohms

R_{LOAD} (T = 0+) = 0 ohms

5.0 Task 3-Engineering Models, Design, and Test Plan

During this task Engineering Models (E/M's) were designed using the circuits developed on Task 2. The structure of the E/M's was defined by NASA to be adequate for Laboratory environments and evaluations. It was further defined that it is not the purpose of this contract to develop elaborate subminature packaging techniques. Therefore, the package designs were standard printed circuit board and aluminum box configuration with terminal strips for external connections. The three types of RPC's were all packaged in the same basic box in order to standardize and keep costs down.

5.1 Mechanical Design and Outline Drawing

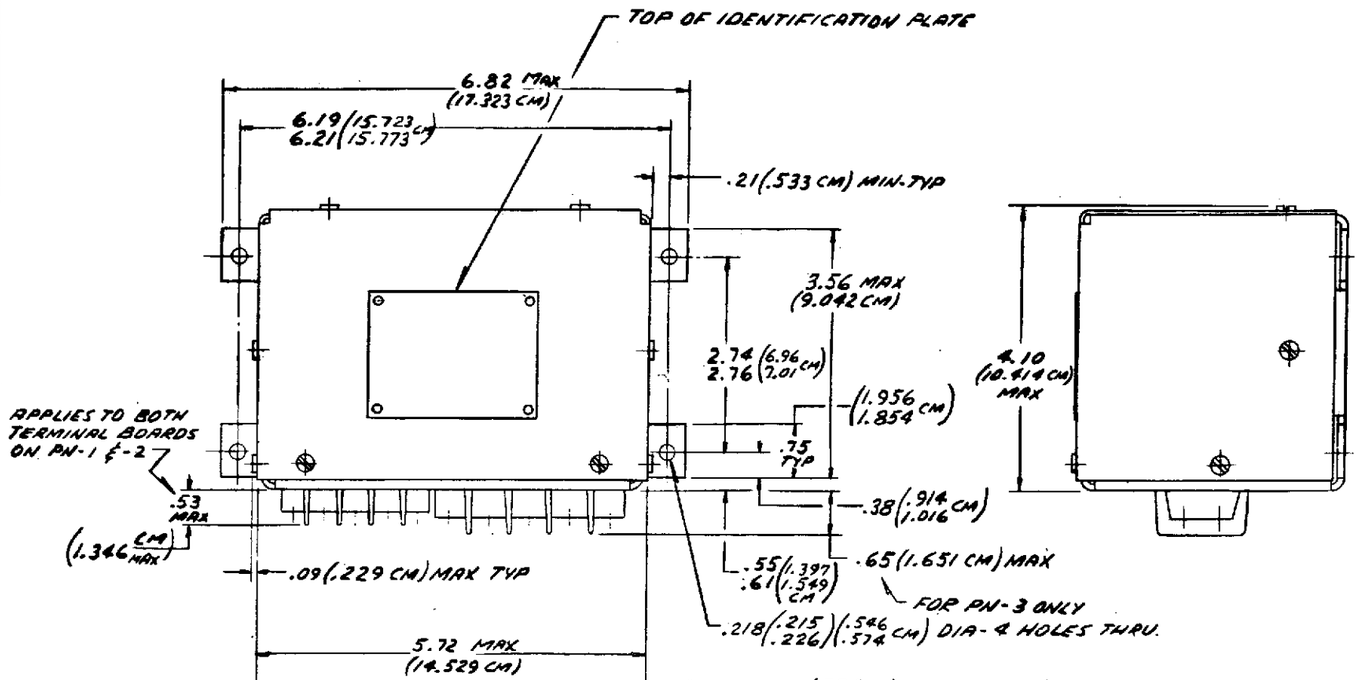
The approved design is shown by the Outline Drawing Y9006D40, on the following page. The units are cold plate mounted to provide cooling by conduction through the base to the mounting surface. The maximum cold plate mounting surface temperature must be limited to 100°C. Although it is not shown, the cover is perforated to permit additional cooling by convection for the Type 3, 30 ampere unit.

As defined by the NASA specification (Refer to section 1.3) the RPC's provide optional performance features. These functions include selectable instant trip levels for the Type II & III RPC's and optional automatic reset (3 times) for all types.

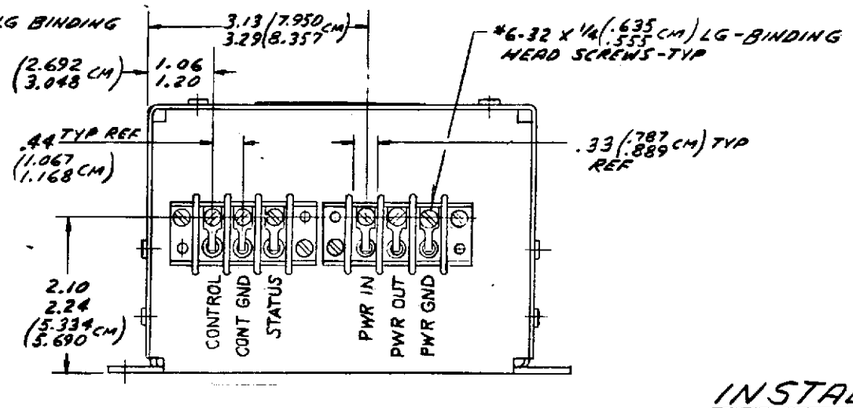
The required circuit interconnections to provide these functional options could be provided either through terminals brought outside or by selector switches mounted on printed circuit boards. The latter technique was selected because it eliminated extra wiring and noise pick up problems that would be associated with these high impedance circuits.

A special 4 pole DIP printed circuit switch is mounted on the top circuit board and can be easily programmed with the cover removed from the unit. An instruction label on the inside of the cover provides the necessary switch program information for each performance option.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



FRONT VIEW FOR PN-3 ONLY



FRONT VIEW FOR PN-1 & -2 ONLY

FOLDOUT FRAME 2

INSTALLATION DRAWING FOR PART NO. 946F999-1, -2 & -3

FOLDOUT FRAME 1

ORIGINAL PAGE IS OF POOR QUALITY

SPECIFICATION	GOVERNMENT SPECIFICATION	NAME OF PROCESS

83

QTY REQD PN #	SYM	NOMENCLATURE OR DESCRIPTION	PART NO. OR IDENT NO.	SPECIFICATION	CODE IDENT NO.	INTERNAL INFORMATION	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST					

946F999-3	
946F999-2	
946F999-1	
NEXT ASSY	USED ON
APPLICATION	

TOOL REF

TOLERANCE MFG. SPEC PER LA 101
DIMENSIONS IN INCHES. DO NOT SCALE DRAWING.
.510 DECIMAL TOLERANCES
UNLESS OTHERWISE SPECIFIED
2 PLACE ± .02 | 3 PLACE ± .005 | ANGLES ±1°
PROCESS TO BE APPLIED AS INDICATED ON DWG.
SPECIFICATIONS
WESTINGHOUSE SPECIFICATIONS TAKE PRECEDENCE IN MATERIAL ASSIGNED FOR WESTINGHOUSE GOVERNMENT OR OTHER SPECIFICATIONS APPLY ONLY WHEN NO WESTINGHOUSE SPECIFICATION IS INDICATED
SYMBOLS
W - WESTINGHOUSE SOURCE CONT DWG
W-SPEC-SOURCE CONT DWG
V - VENDOR PART
MFR AS REQ'D

DRTM	GEISER	3-6-74
DRTM		
ENGR		
ENGR		3-14-74
MFR		3-18-74
TEST		
PROJECT ENGR APPD		
APPD FOR		3-13-74
BY		

AEROSPACE ELECTRICAL DIVISION
WESTINGHOUSE ELECTRIC CORP.
LIMA, OHIO U.S.A.

TITLE
OUTLINE
REMOTE POWER CONTROLLER
NASA-LEWIS TYPES I, II & III

SIZE	CODE IDENT NO	DRAWING NO.
D	83843	Y9006D40

SCALE NTS | WEIGHT | SHEET

5.2 Test Plan

The test plan developed for evaluation of the Engineering Models is contained in Appendix I of this report. The plan includes the test circuit definition, tests which were performed, performance limits, and a test schedule for each Engineering Model Type.

An application guideline for the Engineering Models was also prepared and is contained in Appendix II of this report. The document includes among other items a performance specification summary for each RPC Type.

6.0 Task 4 - Fabrication of Engineering Models

During Task 4, two Engineering Models of each type were constructed to the design established in Task 3. A total of six units were constructed.

During this task a contract modification (MOD 1) was awarded to develop simplified 120 Vdc RPC circuits. The details of this modification are covered in section 9 of this report. A second contract modification (MOD 2) was requested by Westinghouse to extend the completion date. This was needed to accomodate a temporary manpower shift for the design of RPC circuits for NASA Space Shuttle.

The first modification extended the delivery data of the Engineering Models. This extension of time coincidently helped in solving problems incurred during Task 4. The problems were not technical in nature but related to the production scheduling and availability of components. These problems were finally resolved and the units were ultimately delivered on schedule.

7.0 Task 5 - Testing of Engineering Models

The Engineering Models were evaluated according to the Test Plan developed during Task 3, Reference Appendix I. The performance, in general, was as expected and was similar to the performance of the breadboards evaluated during Task 2. The detailed data filled approximately 75 pages for all 6 Engineering Models. This data is available, if needed, in Monthly Progress Report Number 14. The following is a brief summary of this data including problems and recommendations resulting from the testing.

Table 9 - Engineering Model Test Data Summary

Unit Type/ Serial No.	Switch drop at rated cond. (VOLTS)	Power Diss. (WATTS)	Efficiency (%)
I/1	.54	9.06	98.5
I/2	.39	8.18	98.6
II/1	.53	7.09	98.8
II/2	.46	6.16	98.9
III/1	.79	34.8	99.03
III/2	.90	38.3	98.9

Item		Comments About Performance
1.	Switch voltage drop. (on)	The 5 amp Type I and Type II RPC's exhibited voltage drops within limits and at levels which were expected. Although the 30 amp Type III met the limits, it was close, and was higher than expected. The 2N6249 power transistors (Unit #1) performed better than the 2N6251 devices (Unit #2) which supports the concept that higher voltage transistors have higher saturation voltages and/or lower gains. The problem can be remedied by using more transistors in the power switch.
2.	Electrical efficiency	The electrical efficiency of all units was as expected.
3.	Switch leakage	The leakage current was within limits and as expected.
4.	Turn on and Turn off times	Turn on and turn off times were within limits and as expected. However, it should be noted that for the instant trip RPC's (Type II & III), it is essential that the turn on and turn off times be minimized. This is necessary in order to keep the size and cost of the power switch transistors to a minimum and still be able to handle shorted load conditions.
5.	Automatic reset	Of the 6 units 2 were slightly out of limits. The problem is attributed to the poor quality mono-stable multivibrator (one shot) Z304A. This is a CMOS device (MC14528) and experience has shown that this device should be avoided especially for applications requiring pulses greater than a few milliseconds. A secondary problem is its inability to be powered up in the proper state. For this reason if the control signal is applied, then the power bus energized, it is impossible to guarantee that the RPC will start up in the on state. Of course, this problem can be remedied by a redesign to eliminate the 14528 device and should be done before the circuit is used in production.

6. Trip time delay (I^2T trip circuit)

The detailed data illustrates that this circuit functioned very good and exhibited excellent repeatability. The circuit approximates the desired I^2T function very closely without undue circuit complexity. The high propagation speed required for the instant trip did create some susceptability problems, however, these were resolved with by-pass capacitors.

7. Lamp Start Capability

The Type I current limiting RPC gives superior performance for high in-rush loads such as incandescent lamp loads. This is shown by this data below, however, it should be pointed out that the current limiting circuit is inherently more costly than the instant trip designs. This in-rush performance could be improved by moving the instant trip level to 10 or 15 times rated current (as opposed to 5x) but would be at the sacrifice of cost. However, the cost would be less than an equivalent current limit circuit because the power switch is always in saturation.

Table 10 - Lamp Start Capability

Unit	Max. Wattage	% of Rated Wattage
Type I	675-775	112-130%
Type II	250-300	42-50%
Type III	625	17%

8.	Short Circuit Response	Type I - Initial problems in the E/M's were traced to undersized power dumping resistors R103A & R103B. The problem was solved by increasing the rating from 10 watts to 25 watts. Except for this irregularity, the current limiting performance was very good. Settling times were typically less than 1 millisecond. Type II - No problems. The worst case fault is an applied fault (to an already closed RPC) which resulted in a typical 5 microsecond trip time with peak currents of 75 amperes. Type III - For reasons detailed in Section III of monthly report #14 the power switch for an instant trip RPC needs to have very fast rise and fall times. This will insure that the power switch will spend a minimum of time in a high dissipation state for shorted load conditions. It is recommended that turn on rise times be specified at 5 microseconds minimum for any future designs. Also in order to give the design a better safety margin it is recommended that a 90 amp instant trip unit use more than 5 2N 6249 transistors in parallel. The optimum number should be the subject of further development.
9.	Transient Voltage (200V.)	The units survived this test OK, however, occasionally a false trip occurred. The problem was traced to the Collector-Emitter capacitance of Q201. The problem was remedied by putting a 50Pf by-pass capacitor at the input terminal (Reset) of the trip flip-flop Z302A.
10.	Coordination-Series Operation	No problems, however, the secondary problem discussed in Section 5 of this summary applies to this requirement.

11.	EMI	No problem with EMI except that a small amount of filtering may be necessary to bring the Type III conducted broadband interference in limits.
12.	Mechanical	Temperature rise in the 30 amp, Type III RPC was higher than expected. The cover was subsequently perforated to improve convection cooling. It is necessary that this unit be operated with a fan blowing across it.

8.0 Task 6 - Delivery

All hardware - 3 RPC Breadboards, 6 Engineering Models, and 2 Simplified Circuit Breadboards were delivered as scheduled.

9.0 Task 7 - Simplified Circuit Analysis and Design

As a result of a contract modification Tasks 7 and 8 were added to develop simplified, low cost RPC circuits. Two types of simplified circuits were to be developed. The first type is a 5 ampere current limiting unit and is called the Type I Simplified RPC. The second type is a 5 ampere "instant trip" unit and is called the Type II Simplified RPC.

The purpose of Task 7 was to perform trade off studies between the original contract specifications (Reference section 2.3), circuit complexity and cost, and the intended application of the RPC's. Based on the results of these studies, designs for the simplified Type I and II RPC would be made. A further intent was to substantiate any variances in the specifications which were found necessary to accomodate the simplified designs.

The results of the trade off studies and analysis and the simplified designs were presented to, and approved by, NASA before any work was started on Task 8. The following paragraphs cover the simplified designs and trade off studies made.

9.1 Type I - Power Stage

The Type I power stage represents the largest potential area for cost reduction because the original circuit uses three, 50 dollar alloy transistors and three power resistors in an arrangement which can safely handle the 3x (15 amperes) current limiting condition. The short circuit condition forces full supply voltage, 132 volts steady state, across the RPC during the .1 second trip time. Additionally the power stage has a relatively expensive and complex oscillator circuit to provide efficient base drive current to the power transistor for less than 1 volt saturation voltage.

It was decided at the onset that the oscillator circuit would be eliminated entirely by using a Darlington configuration power switch. The reasons for this decision are discussed below.

The Darlington will reduce complexity, reduce cost, reduce radio noise generation, and increase reliability at the expense of a slight increase in voltage drop. The specification limits the maximum voltage drop to 1.0 volts whereas the Darlington will provide typically 1.2 volts with a maximum of 1.4 to 1.5 volts. This voltage drop can be achieved with substantially less base drive losses and therefore will maintain electrical efficiency comparable to the original design. An example is given below:

Referring to figure 48, assume each transistor has a gain of 10 (a conservative estimate) and the switch must carry up to 3 times rated current. Then I_B must be, to insure saturation:

$$I_B = \frac{I_L}{10^4} \times 3 = 3 \times 10^{-4} \; I_L$$

The total power stage losses at full load would be

$$P_{Loss} = (V_{Bus}) \; (I_B) + (1.2) \; (I_L)$$

or for our case

$$P_{Loss} = (120) \; (3 \times 10^{-4}) \; I_L + 1.2 \; I_L = 1.24 \; I_L$$

Power to the load is

$$P_L = V_L \; I_L = (120 - 1.2) \; I_L = 118.8 \; I_L$$

Electrical efficiency is by definition:

$$Eff = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{Loss}}$$

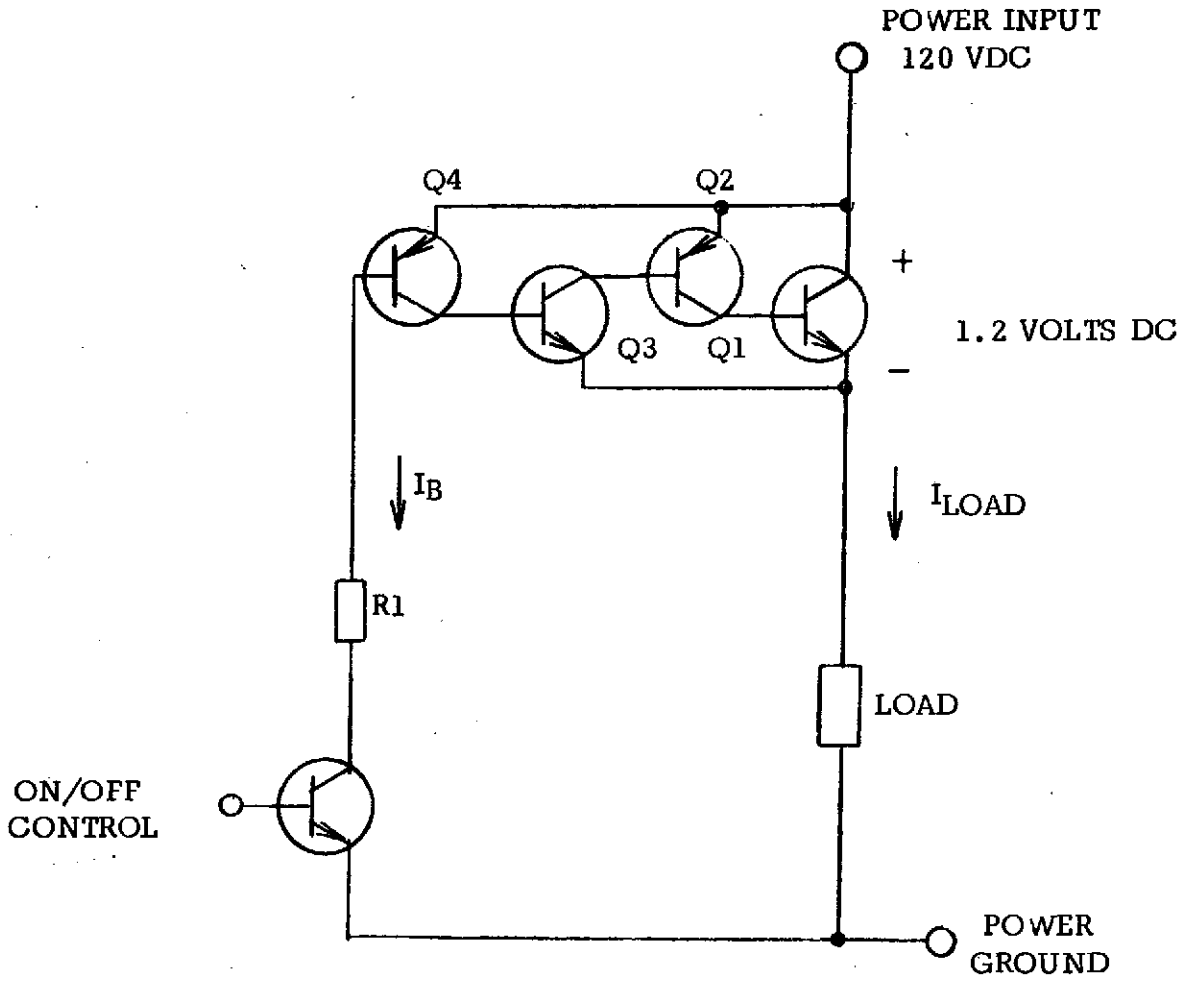


Figure 48 - Simplified Power Stage Concept

Hence for our case

$$\text{Eff} = \frac{118.8\ I_L}{118.5\ I_L + 1.24\ I_L} = 98.96\%$$

This efficiency is as good or better than the original transformer driven design. The efficiency, as expected, is independent of the RPC current rating.

An additional performance bonus of the Darlington is its partial load efficiency, which is superior to the transformer design. Figure 49 illustrates this comparison. These curves represent the total RPC dissipation which includes the time delay and logic circuits. The power stage dissipation alone at zero load current is less than one watt. Since RPC ratings are discrete, the average loading in any given system with many RPC's will never be 100%, therefore, the partial load dissipation is an important consideration.

The second area of investigation for the simplification of the Type I power stage is the current limiting function. As stated earlier the Type I RPC requires three 50 dollar alloy transistors and several resistors to withstand, safely, the dissipation during short circuit current limiting.

One cost reduction technique would be to eliminate the alloy transistors entirely. Such an arrangement is possible by putting all of the dissipation during current limiting into resistors (i.e. passive current limiting) and using lower cost transistors to switch in the proper amount of resistance. This type of design, however, gives poor current limiting quality, which can be improved only by increasing the number of resistors and switches, which in turn requires more complex sensing and control circuits. For reasons of complexity, the "passive" current limiting technique was considered only as a "last resort" solution to the problem.

A compromise solution to the problem was to reduce the number of alloy transistors and relax certain design requirements to accommodate this reduction. This arrangement resulted in a simple circuit design yet provided good current limiting characteristics. Figure 50 illustrates the circuit concepts.

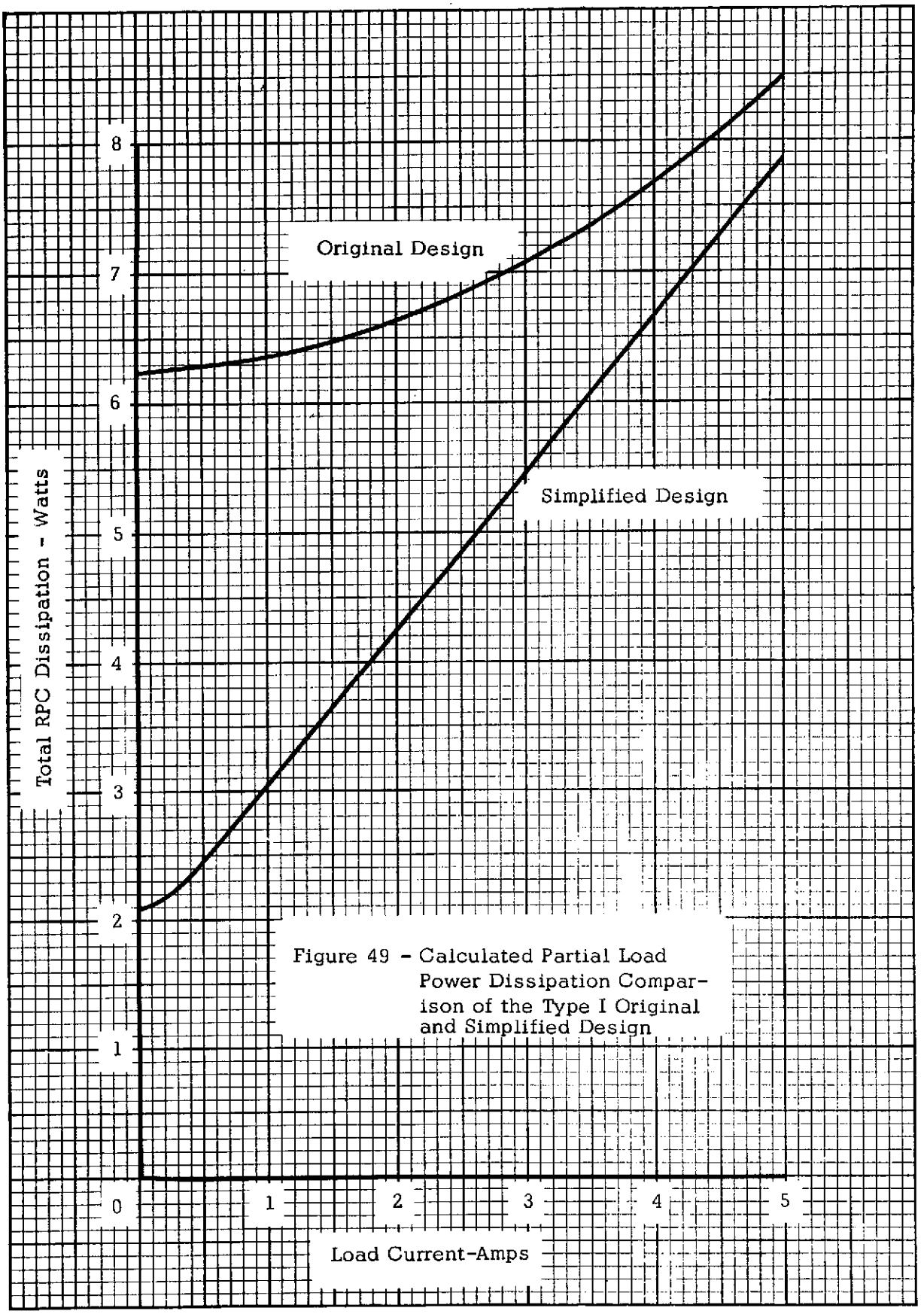


Figure 49 - Calculated Partial Load Power Dissipation Comparison of the Type I Original and Simplified Design

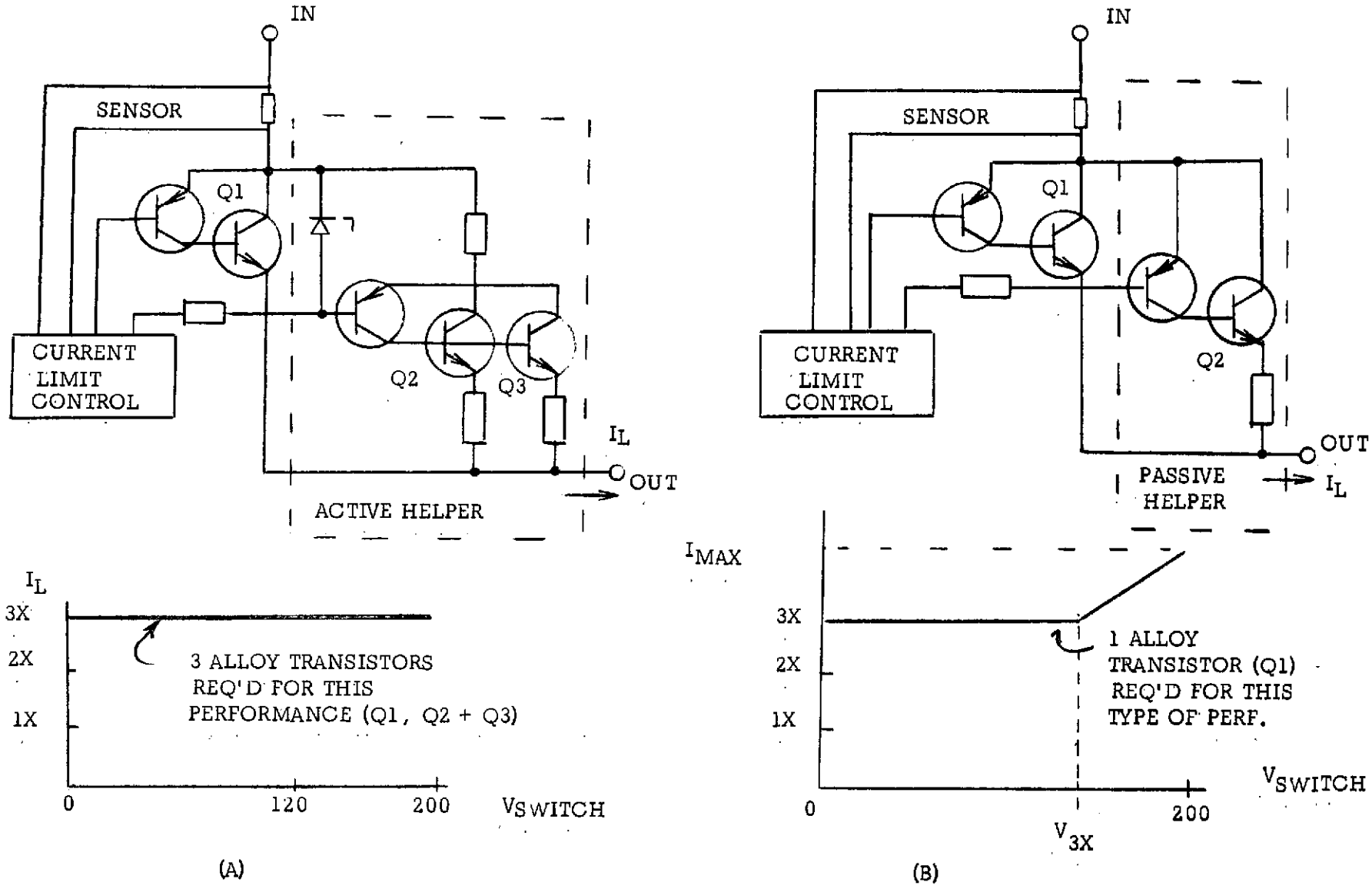


Figure 50 - Comparison of Circuit and Performance for Active and Passive Type Helpers

It uses a simple (passive) helper circuit rather than the original active helper circuit. Although the complexity is changed very little, the cost is improved 40 to 50 dollars for each alloy transistor (type 164) that is eliminated or replaced with a switching transistor.

The effect on the current limiting quality is also illustrated by Figure 50. The original design, Figure 50A, utilized the active helper and was capable of 3X current limiting at rated supply voltage (120 VDC) as well as during 200 volt, 50 microsecond transients with a shorted load. The proposed current limiting circuit performs essentially the same except that the helper remains in saturation and hence cannot limit load current to 3X for bus voltage levels above V_{3X} . V_{3X} is a design parameter dependent upon the capability of the 164 alloy transistor, the current limiting level, and the ambient temperature. The effects of V_{3X} on an actual application are as follows:

1. If V_{3X} is greater than or equal to nominal supply voltage, 120 VDC, then current limiting performance will not be sacrificed for nominal bus voltages. It will, however, exceed 3X for bus transient excursions above V_{3X} if the load impedance is very nearly zero.

2. If V_{3X} = 120 VDC then the maximum current can exceed 3X only if the load resistance is less than .22 of rated and V_{BUS} is 200 VDC.

A parametric study was made using graphic techniques similar to those in figure 2, to analyze the current limiting performance of the proposed circuit. The parameters considered in this study were cost (in terms of alloy transistors), ambient temperature and current limiting performance.

The trade off studies resulted in a variety of current limiting possibilities as a function of cost. These results were reviewed with NASA and the characteristic finally selected is shown by figure 51. The corresponding circuit uses 1 alloy transistor and can operate up to 100°C with a .1 second short circuit current limit time.

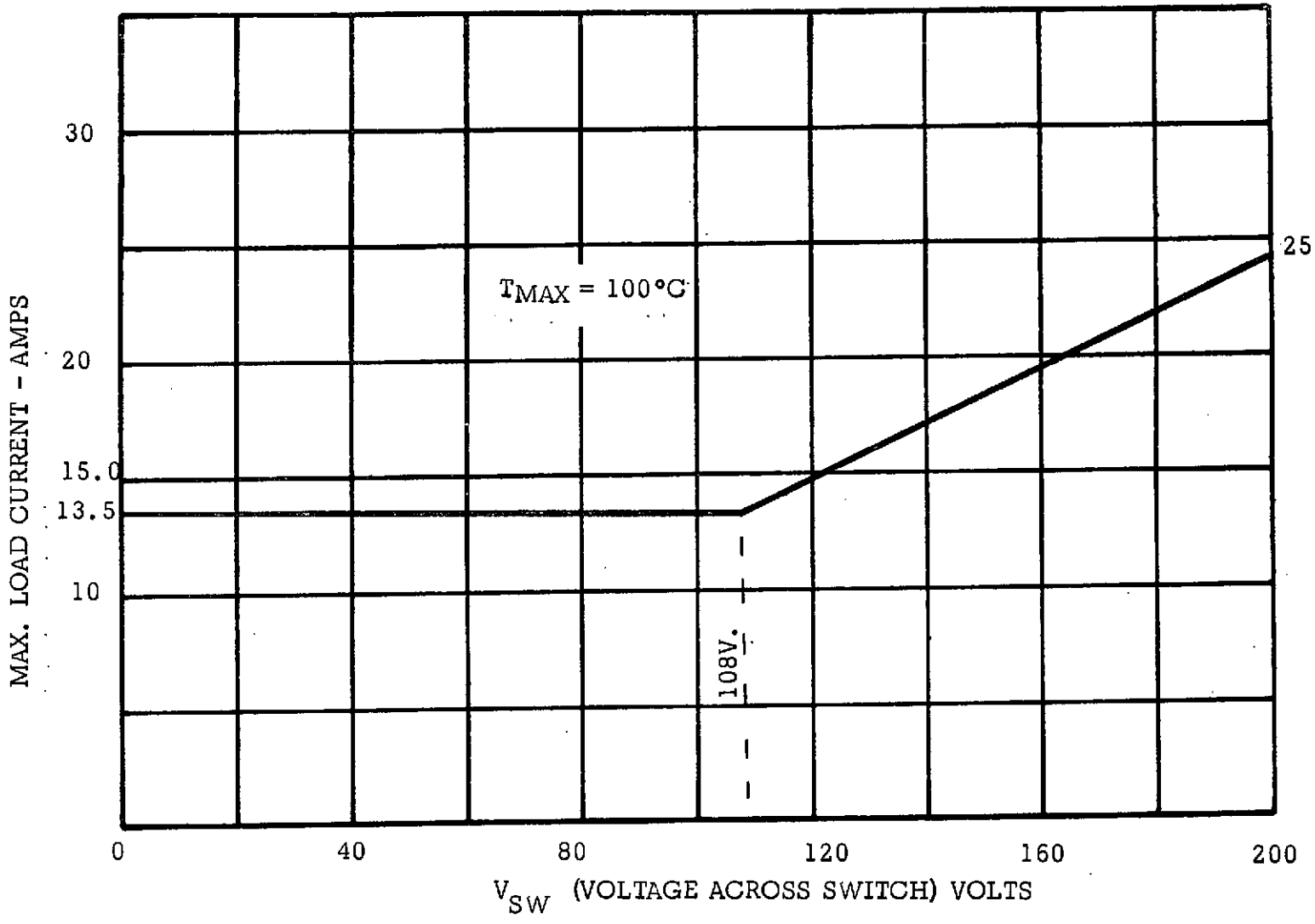


Figure 51 - Current Limiting Characteristic Using A Single Type 164 Transistor And A Simple (Passive) Sharing Circuit.

9.2 Type II - Power Stage

The Type II power switch was changed to a Darlington configuration for the same reasons the Type I was. The partial load dissipation of the Type II RPC is shown by figure 52. Unlike the Type I, the Type II Darlington has more dissipation at rated load than its transformer driven counterpart. However, the simplified Type I and Type II dissipations are essentially identical with power stage efficiencies of 98.96%. This efficiency is for the power stage only. The overall RPC efficiency including control and trip circuits was later shown to be 98.7%.

9.3 Trip Circuit

An obvious simplification of the time delay circuit was the elimination of the selectable instant trip levels for the Type II RPC. The effect of this deletion was first believed to have little real impact on the complexity of the circuit. However, after further development it was discovered that this deletion of function permitted a rather sizeable reduction in circuit complexity. The final circuit configuration, is shown by figure 53. This circuit provides essentially the same trip time characteristics as the original design with virtually no sacrifice in temperature sensitivity.

The function of 3 operational amplifiers has been combined into one thus eliminating two relatively costly items. Current is sensed by the same low voltage shunt (R_S) and is compared by Z1 to a stable reference ($V_{R'}$) set by CR2, R2, R3, and R4. This reference is set to 6 amps and no trip will result below that load current level. Above 6 amps Z1 will integrate through C1 and when the voltage at the base of Q1 goes below its emitter voltage (also a stable reference) a trip signal will result. Resistor R5 and zener CR1 eliminate the inaccuracies associated with the incomplete saturation of Z1 to its positive supply.

This circuit provides essentially the same equation for trip time delay as the original circuit design. That is, the equation is of the form,

$$T = \frac{A\,(B - X)}{X - C} \quad ,$$

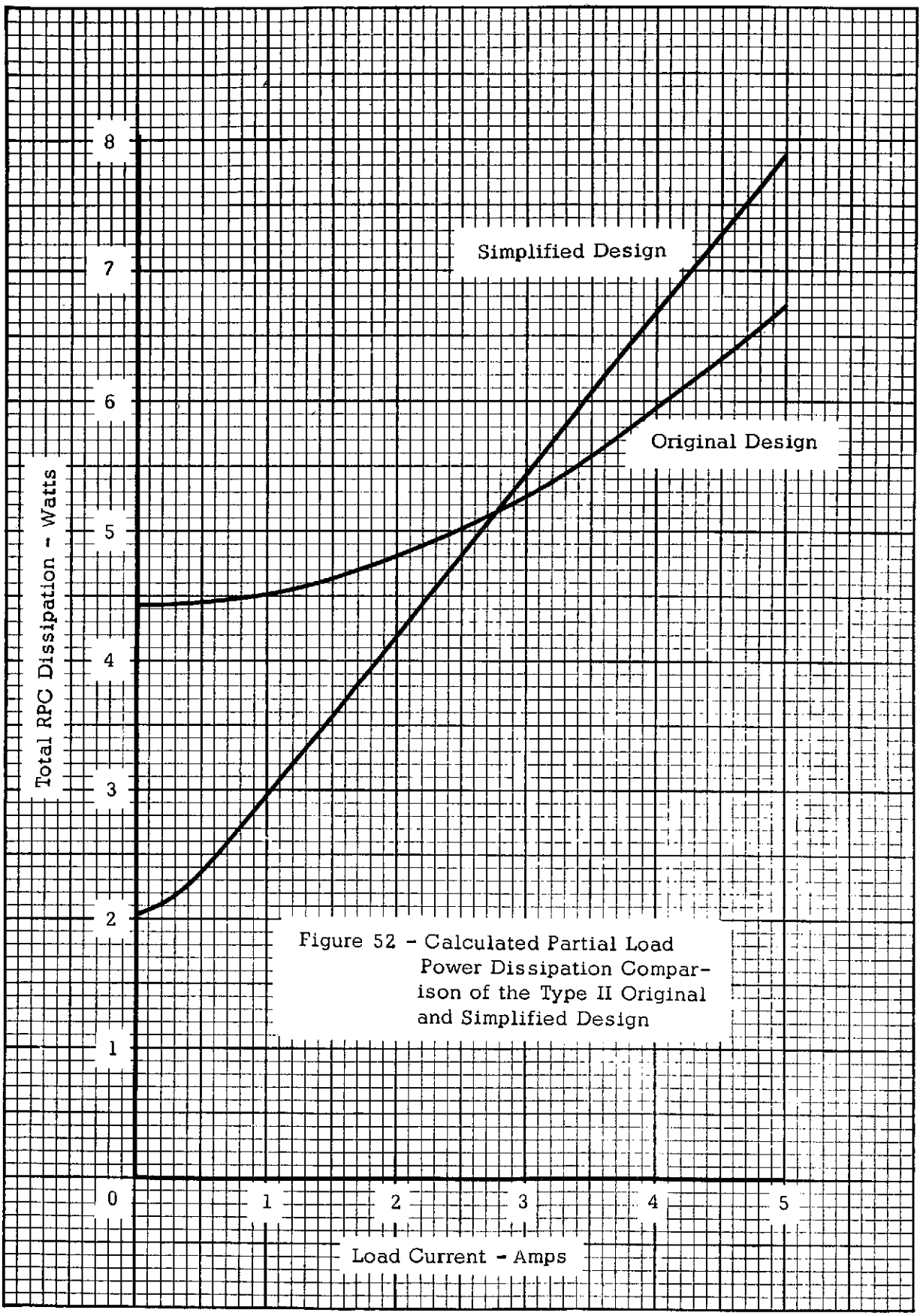
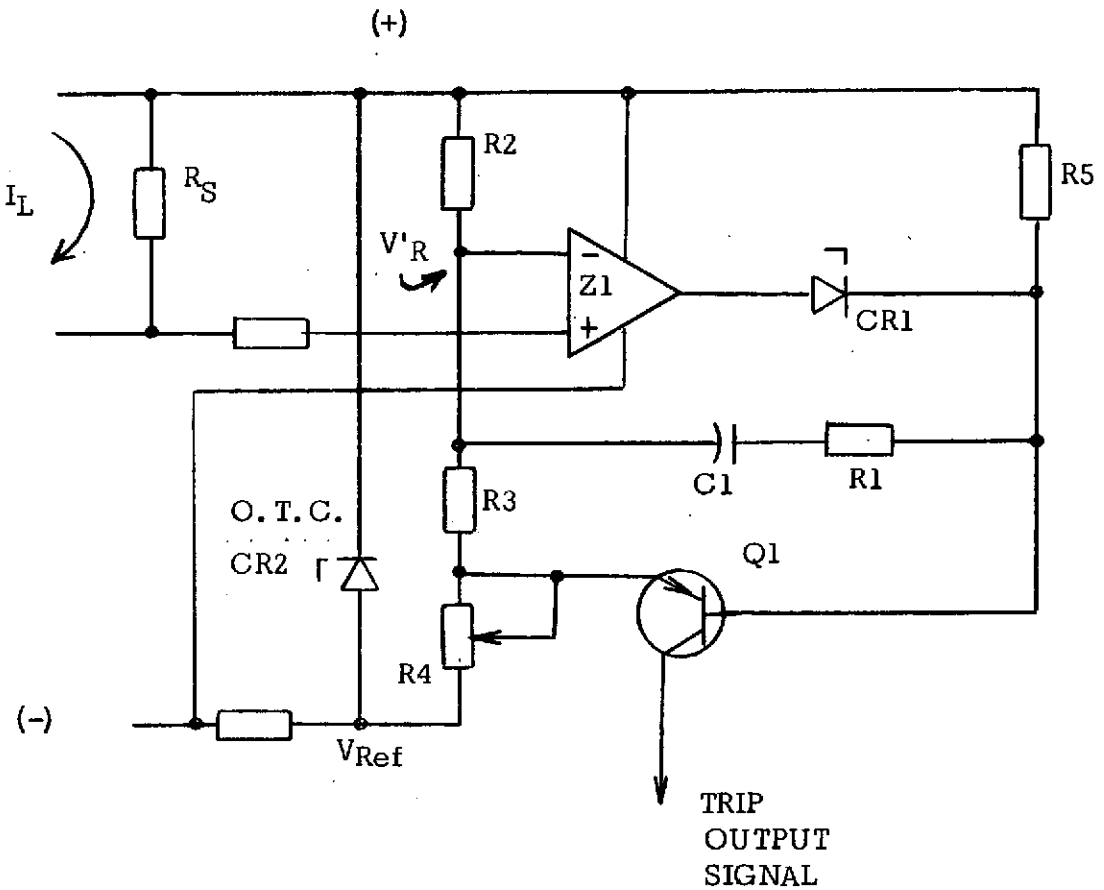


Figure 52 - Calculated Partial Load Power Dissipation Comparison of the Type II Original and Simplified Design



$$T = \left(\frac{\Delta V}{V_S - V_R'} - \frac{R1}{R_{in}} \right) R_{in}\ C$$

where:

$$R_{in} = \frac{R2\ R3}{R2 + R3}$$

$$V_S = R_S I_L$$

Figure 53 - Simplified Single Amplifier Trip Time Delay Circuit

which is also the equation of the performance of the original circuit design. The difference between the simplified circuits and original circuit lies in the worst case tolerance (or drift) due to manufacturing tolerances and ambient temperature. In order to judge the relative merits of the circuits a worst case analysis was made for both circuits. The results of this analysis for the Type I RPC are shown by the performance curves, figures 54 and 55. Assumptions that were made which affect the circuit performance are as follows:

a) All resistor tolerances are $\pm$ 1%.

b) Zener tolerance $\pm$ 5%.

c) Potentiometers can be adjusted to $\pm$ .2% of desired voltage.

d) Capacitor tolerance $\pm$ 10%.

e) Offset voltage on operational amplifiers is $\pm$ 2 millivolts maximum.

f) The operational amplifier can only saturate to within 0 to 1.5 volts from its positive bus supply.

g) Base-emitter voltage drift is $\pm$ .2 volts.

Comparison of the performance curves will show that the new circuit is essentially the same as for the original circuit. Therefore, this circuit was used in the simplified designs.

9.4 Logic Circuit

The logic circuit was simplified by eliminating the multiple automatic reset function. This modification had a significant impact on complexity, since it eliminated the tally counter and the automatic reset time delay circuit. The final circuit configuration is shown by figure 56. The troublesome mono-stable multivibrator MC 14528 has been eliminated entirely. The circuit provides the same performance as the original circuit except for the auto-reset function and, therefore, was used in the simplified designs. The design of this circuit is such that it always starts up in the proper state whether or not the control signal is present. Therefore, a momentary inhibit of the power stage during power up is not necessary.

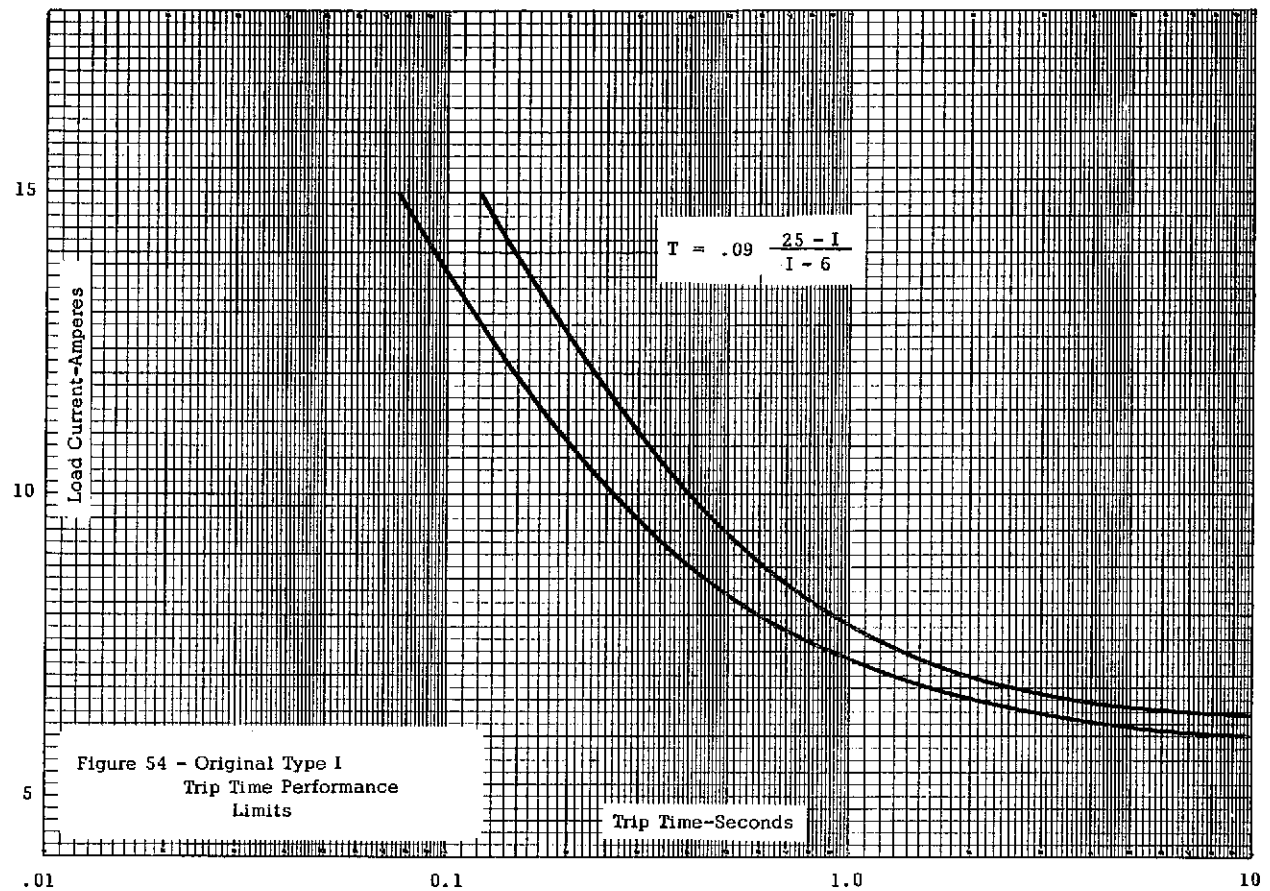


Figure 54 - Original Type I
Trip Time Performance
Limits

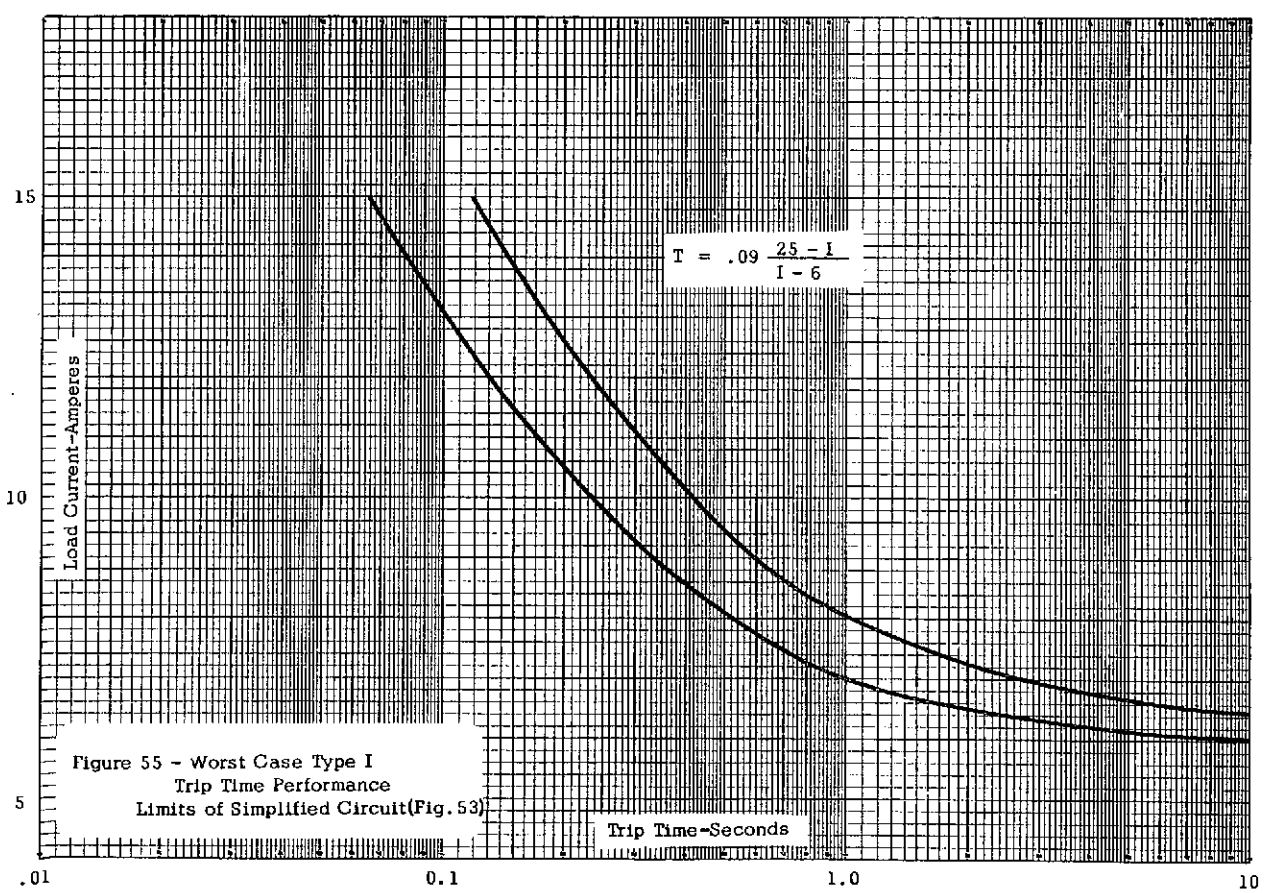


Figure 55 - Worst Case Type I
Trip Time Performance
Limits of Simplified Circuit(Fig. 53)

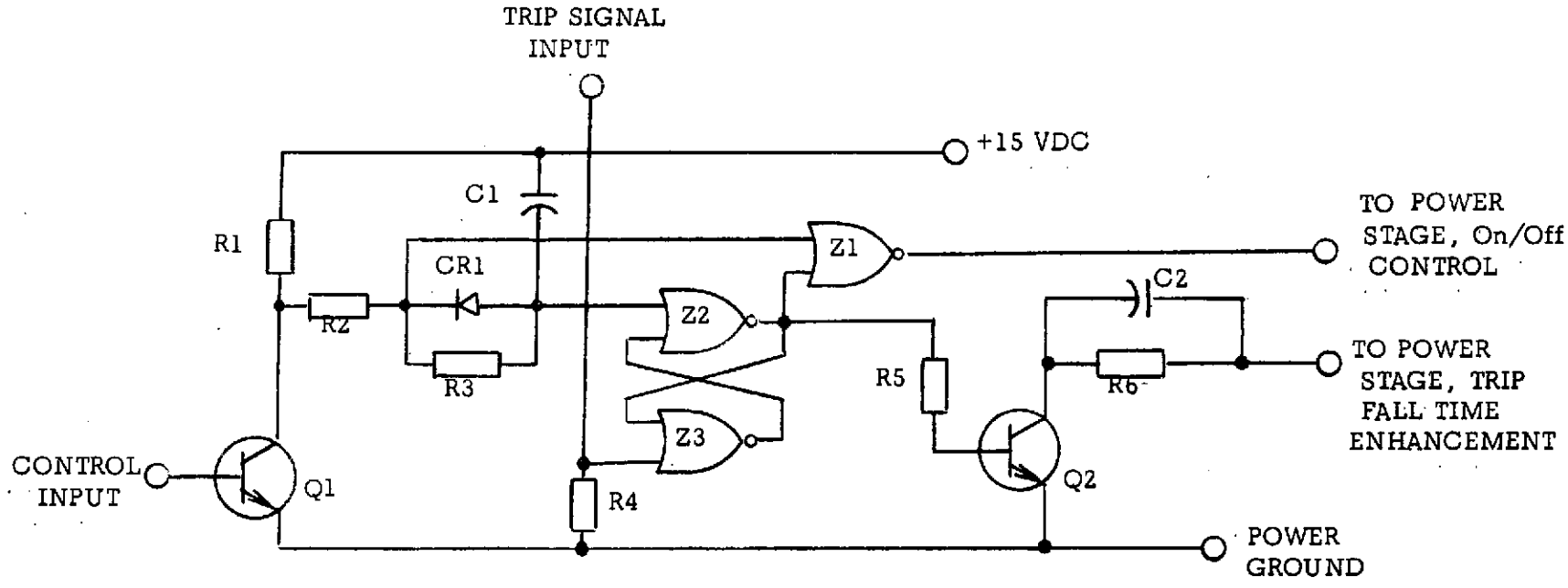


Figure 56 - Simplified Logic Circuit

9.5 Isolation Circuit

After several attempts it was concluded that no improvements could be made in the isolation circuits beyond that which was used in the original design. Other techniques were either more complex or more costly.

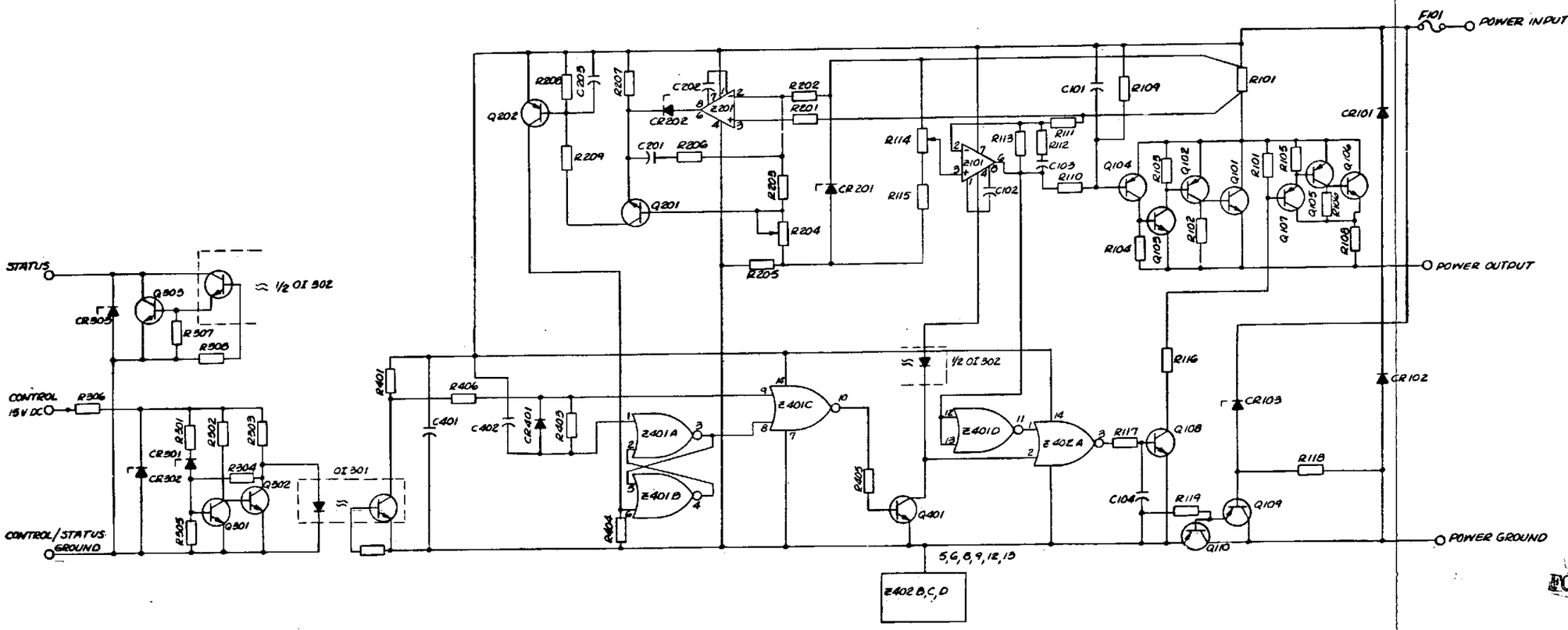
9.6 Simplified Design Schematics

The complete circuit for the simplified RPC circuit is an assemblage of the preceeding sub-circuits. They are shown by figure 57 for the Simplified Type I and by figure 58 for the Simplified Type II.

In both circuits the time delay and logic circuits are powered from a single 15 volt regulated supply referenced to the 120 volt input line. This is provided by Q109 & Q110 for the Type I and by Q106 & Q107 for the Type II. As a result the RPC is basically a 15 volt RPC series regulated from 120 volts. Therefore, it should function just as well at 20 volts as it does at 120 volts. This was later verified by evaluation of the breadboards, during Task 8.

Transistor Q202 was added and transistor Q201 was changed to an NPN in order to give a higher voltage trip signal. This was necessary in order to be compatible with the CMOS logic gates.

REVISIONS		
LTR	DESCRIPTION	DATE



FOLDOUT FRAME

Figure 57 - Simplified Type I Schematic Diagram

QTY REQD PN-1	SYM	NOMENCLATURE OR DESCRIPTION	PART NO. OR IDENT NO.	SPECIFICATION	CODE IDENT NO.	INTERNAL INFORMATION	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST					

NEXT ASSY	USED ON
APPLICATION	

DFTM RAB 10-31-74
DFTM J.F. Blair 11/6/74
ENGR [illegible] 11/7/74
ENGR
MFR
TEST
PROJ ENGR APPD
APPD FOR
BY

AEROSPACE ELECTRICAL DIVISION
WESTINGHOUSE ELECTRIC CORP.
LIMA, OHIO, U.S.A.

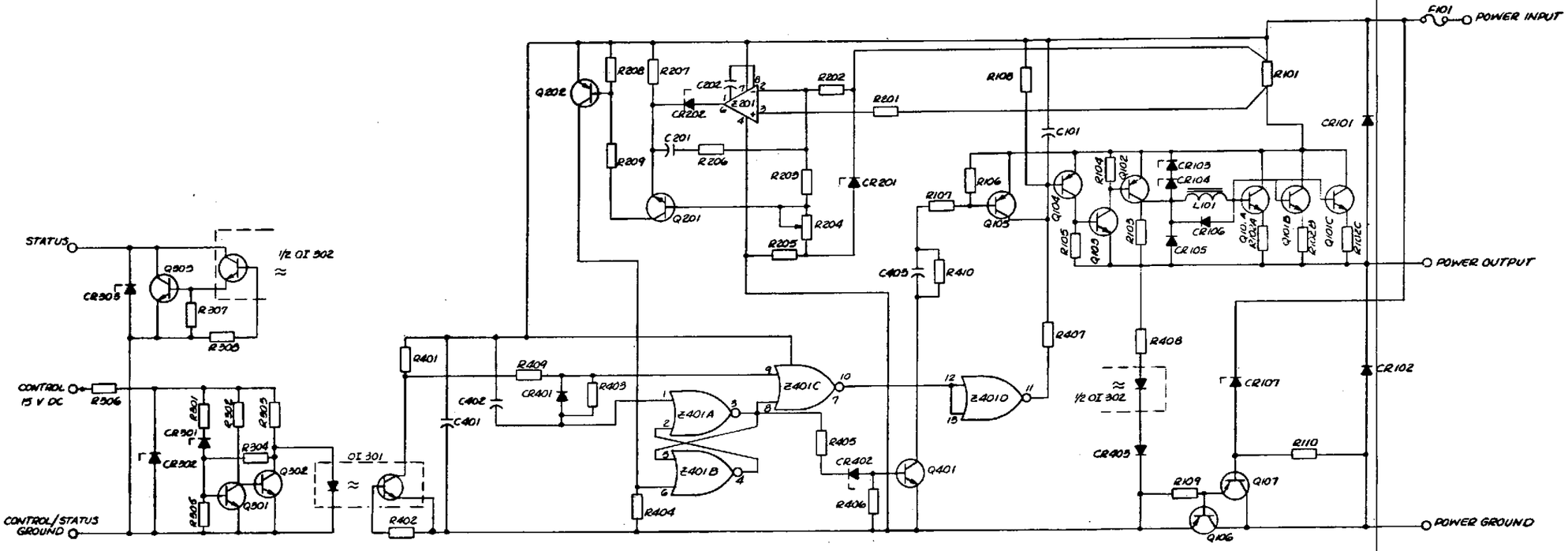
TITLE
SCHEMATIC DIAGRAM
SIMPLIFIED TYPE I - 120 VDC RPC

SIZE	CODE IDENT NO.	DRAWING NO.
D	83843	ED 362067

SCALE NONE | WEIGHT | SHEET

SPECIFICATION	GOVERNMENT SPECIFICATION	NAME OF PROCESS

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



FOLDOUT FRAME 1

FOLDOUT FRAME 2

109

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OF POOR QUALITY

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Figure 58 - Simplified Type II

Schematic Diagram

QTY REQD PN-1	SYM	NOMENCLATURE OR DESCRIPTION	PART NO. OR IDENT NO.	SPECIFICATION	CODE IDENT NO.	INTERNAL INFORMATION	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							

DFTM	KAB 10-31-74
DFTM	11/6/74
ENGR	11/7/74
ENGR	
MFG	
TEST	
PROJ ENGR APPD	
APPD FOR BY	

AEROSPACE ELECTRICAL DIVISION
WESTINGHOUSE ELECTRIC CORP.
LIMA, OHIO, U.S.A.

TITLE: SCHEMATIC DIAGRAM
SIMPLIFIED TYPE II - 120 VDC RPC

SIZE	CODE IDENT NO.	DRAWING NO.
D	83843	ED362068

SCALE NONE | WEIGHT | SHEET

NEXT ASSY	USED ON
APPLICATION	

TOOL REF

SPECIFICATION	GOVERNMENT SPECIFICATION	NAME OF PIECES

10.0 Task 8 - Fabrication and Testing of Simplified Circuit Breadboards

After approval of the simplified circuits developed on Task 7, one breadboard of both types was constructed. The circuits were then evaluated in accordance with the Test Plan developed on Task 3. After evaluation a detailed cost and performance comparison was made for the simplified versus the original designs.

10.1 Simplified Type I Breadboard Test Results

The test data given in this section represents only a portion of all the data taken. Should it be needed, the original data, in its entirety, is shown in Monthly Progress Report Number 16. Plots of key static and dynamic data are shown by figures 59 through 64. Figures 65 through 67 are actual performance photographs of turn on, turn off, and response to short circuit faults. Other pertinent data is shown in Table 11.

Table 11 - Test Data - Simplified Type I RPC Breadboard

ITEM	-55°C	+25°C	+100°C	UNITS
Turn On Voltage*	13.5	13.5	13.5	Volts
Turn Off Voltage*	12.5	12.6	12.2	Volts
Incandescent Lamp Start Capability	700	700	700	Watts
Current Limiting Ripple	0	0	0	Amps
Current Limiting Response Time	1.5	3	5.5	Micro-seconds
Current Limiting Peak Current	37	52	60	Amps
200 Volt Transient	OK	OK	OK	

*Breadboard set up for 28 volt control voltage. This breadboard has a selectable 15 volt or 28 volt control level.

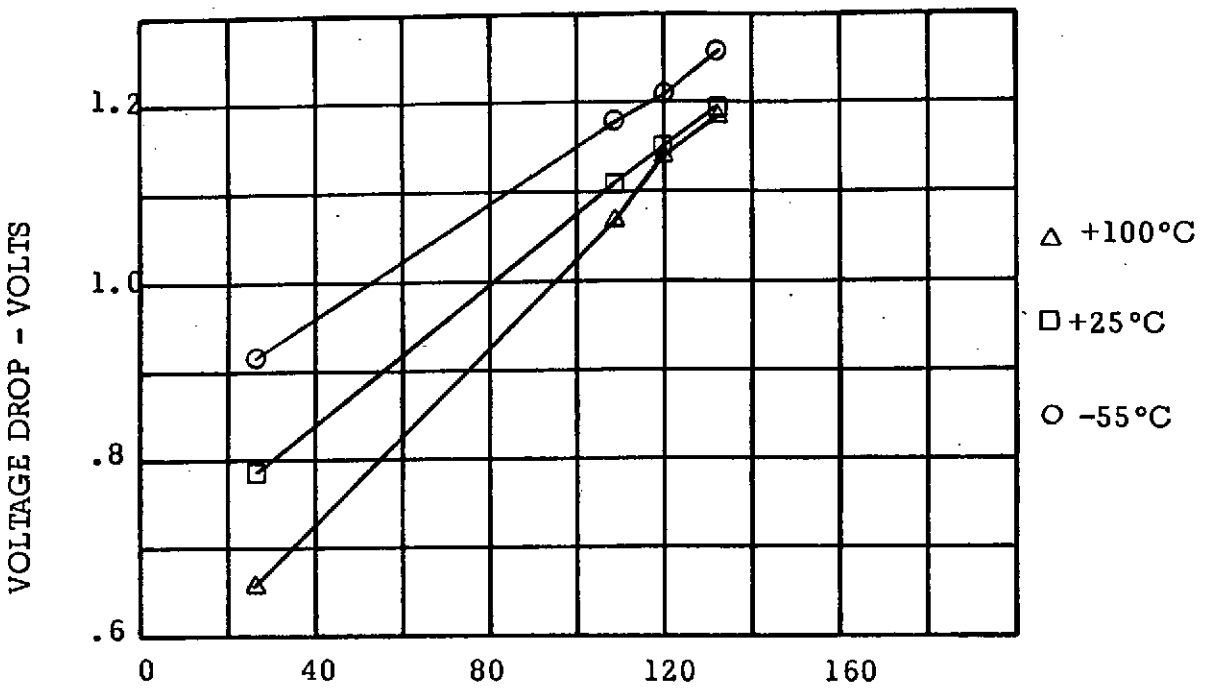
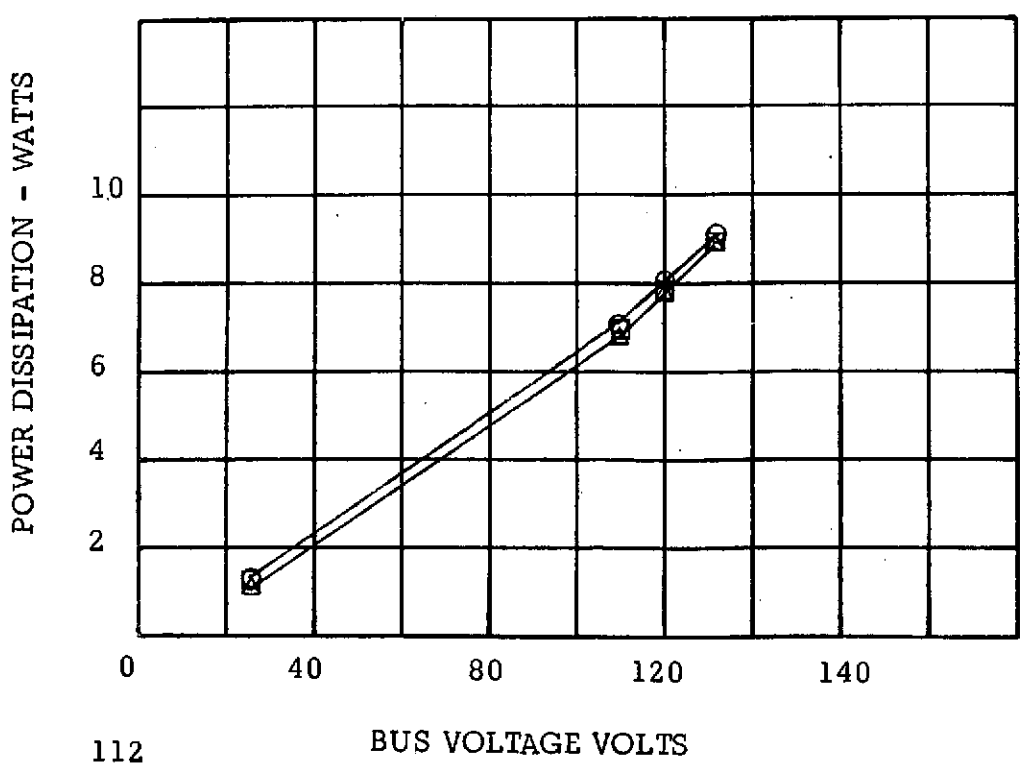


FIGURE 59 - SIMPLIFIED TYPE I BREADBOARD VOLTAGE DROP DATA

FIGURE 60 - SIMPLIFIED TYPE I BREADBOARD DISSIPATION DATA



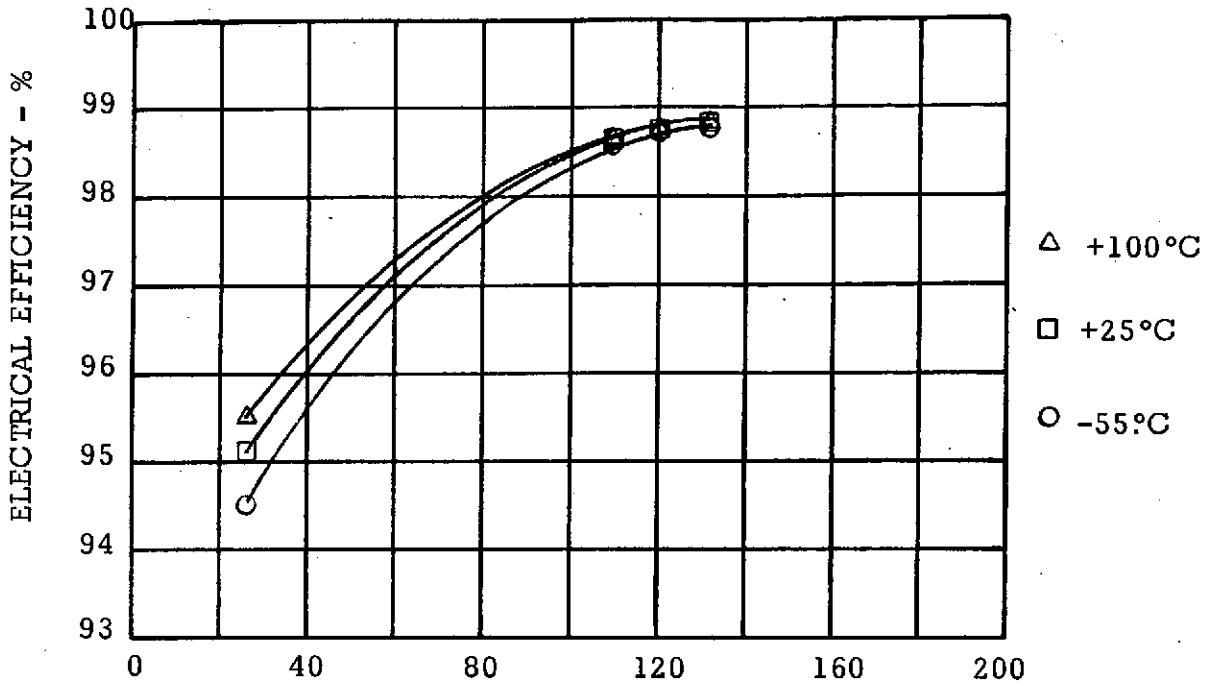
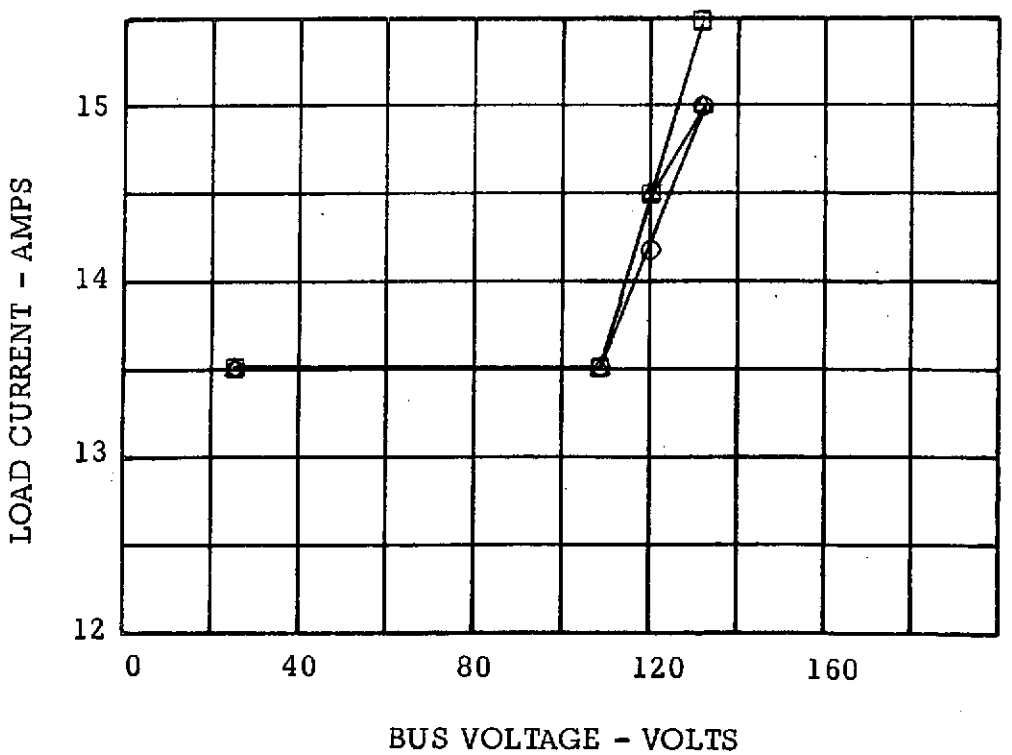


FIGURE 61 - TYPE I SIMPLIFIED BREADBOARD EFFICIENCY DATA

FIGURE 62 - TYPE I SIMPLIFIED BREADBOARD CURRENT LIMITING DATA WITH SHORT CIRCUIT LOAD



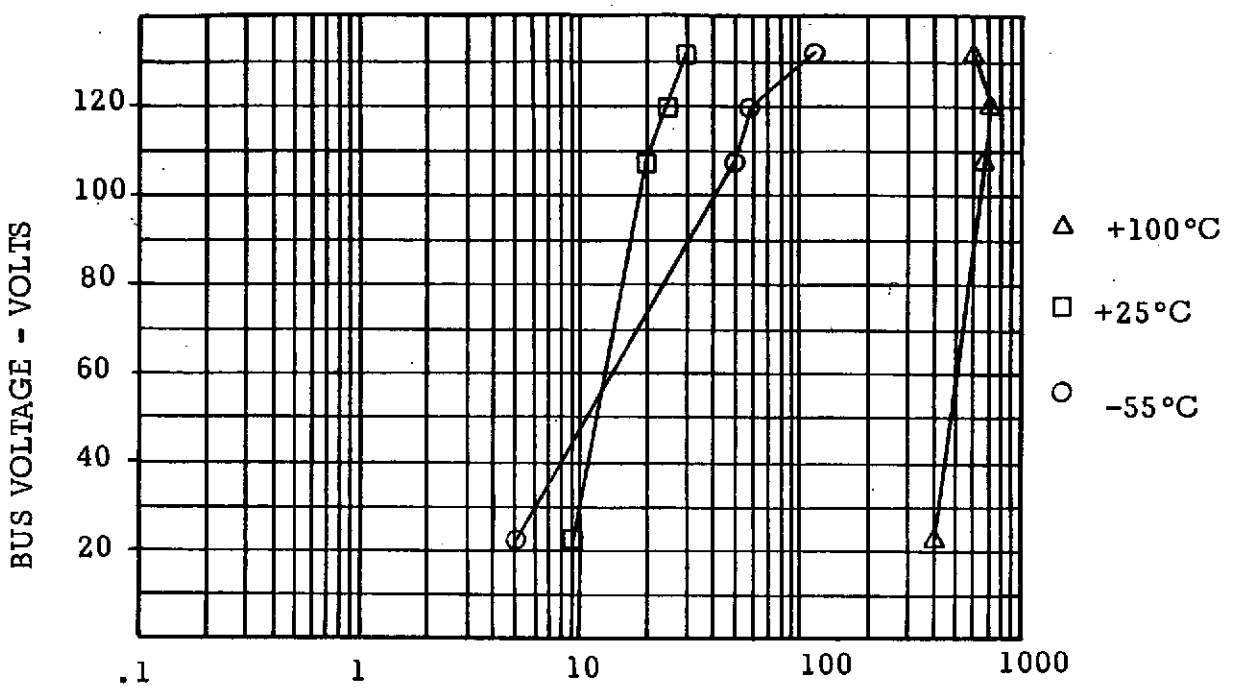
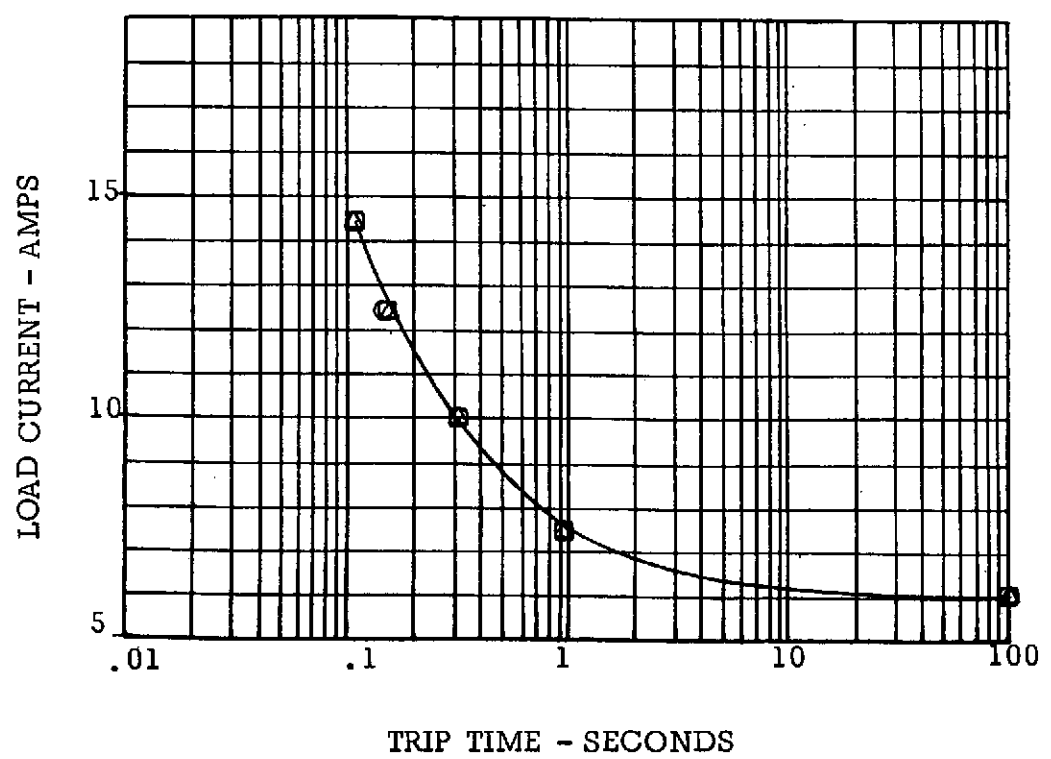


FIGURE 63 - SIMPLIFIED TYPE I BREADBOARD LEAKAGE CURRENT DATA

FIGURE 64 - SIMPLIFIED TYPE I BREADBOARD TRIP TIME DATA



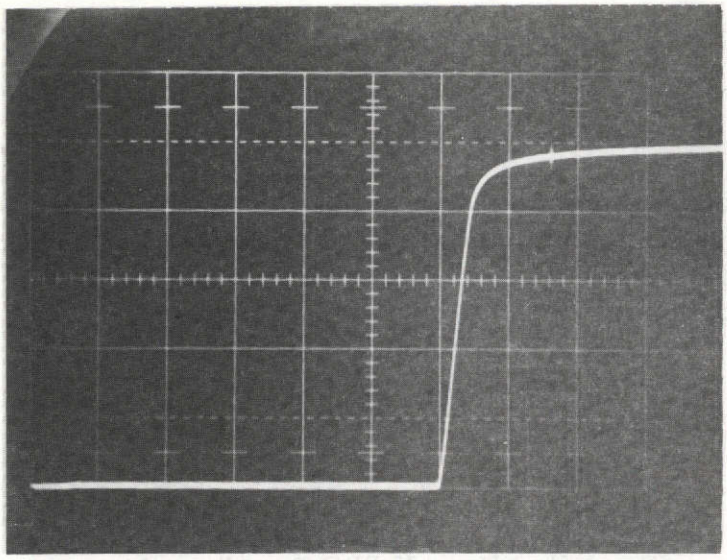


FIGURE 65 - Simplified Type I
Turn On Time

Vertical: Load Current, 1 amp/div.

Sweep: .1 millisecond/div.

V_{BUS} = 120VDC, R_{LOAD} = 24 ohms

Temp. = 25°C

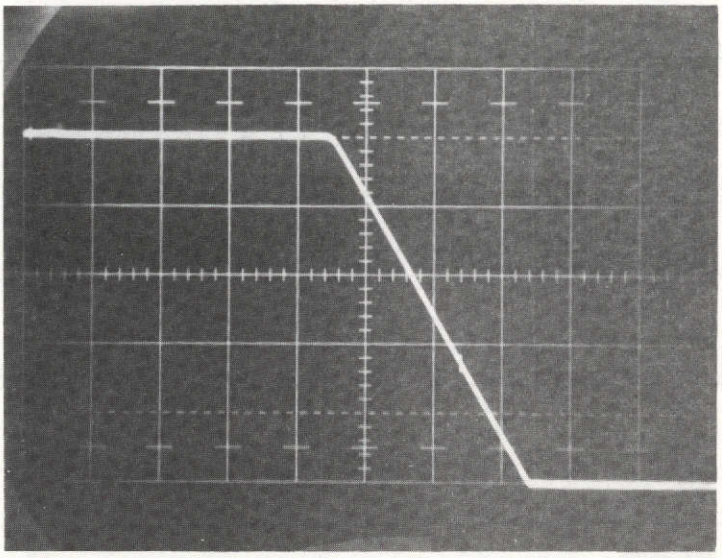


FIGURE 66 - Simplified Type II
Turn Off Time

Vertical: Load Current, 1 amp/div.

Sweep: .2 millisecond/div.

V_{BUS} = 120 VDC, R_{LOAD} = 24 ohms

Temp. = 25°C

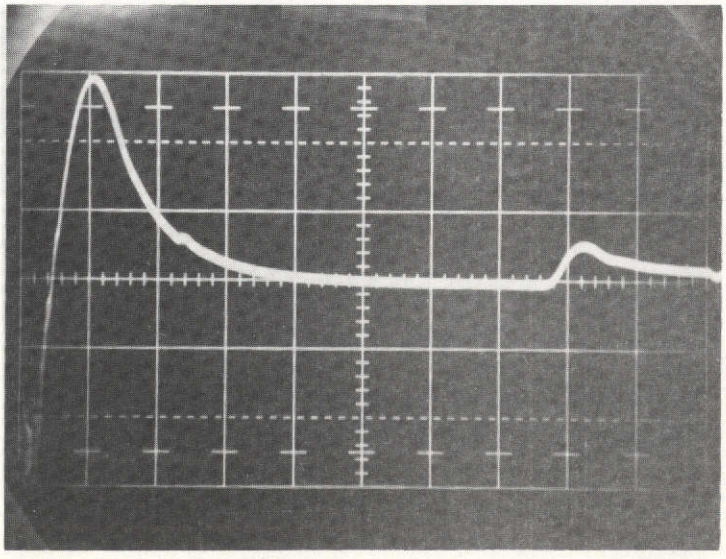


FIGURE 67 - Simplified Type I Response
To Applied Fault

Vertical: Load Current, 10 amp/div.

Sweep: 5 micro seconds/div.

V_{BUS} = 120 VDC, Temp. = 100°C

R_L (T = 0-) = 24 ohms

R_L (T = 0+) = 0 ohms

10.2 Simplified Type II Breadboard Test Results

The test data in this section represents only a portion of all the data taken. Should it be needed, the original data, in its entirety, is shown in Monthly Progress Report Number 16. Plots of key static and dynamics data are shown by figures 68 through 72. Figures 73 through 75 are actual performance photographs of turn on, turn off, and response to short circuit faults. Other pertinent data is shown in Table 12.

Table 12 - Test Data - Simplified Type II RPC Breadboard

ITEM	-55°C	+25°C	+100°C	UNITS
Turn On Voltage*	13.8	13.9	14.0	Volts
Turn Off Voltage*	12.9	12.9	13.2	Volts
Incandescent Lamp Start Capability	300	300	300	Watts
Short Circuit Response Time	2	3	6	Micro-seconds
Short Circuit Peak Current	30	60	70	Amps
200 Volt Transient	OK	OK	OK	

*Breadboard set up for 28 volt control. This breadboard has a selectable 15 volt or 28 volt control level.

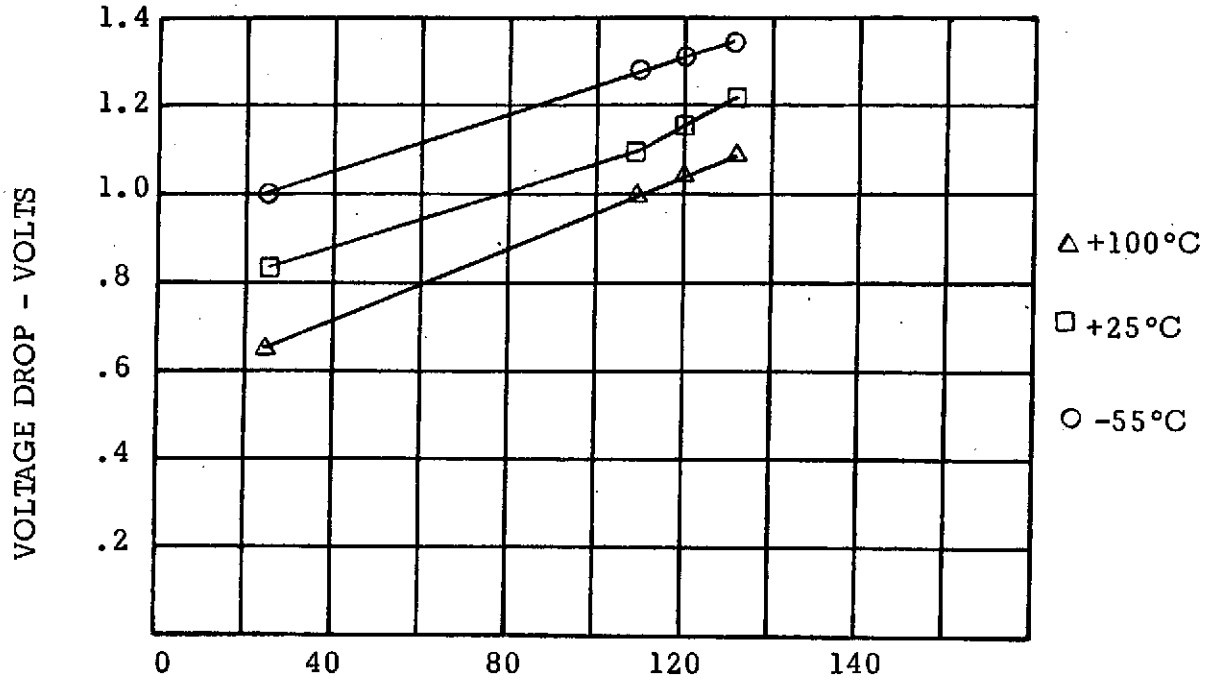
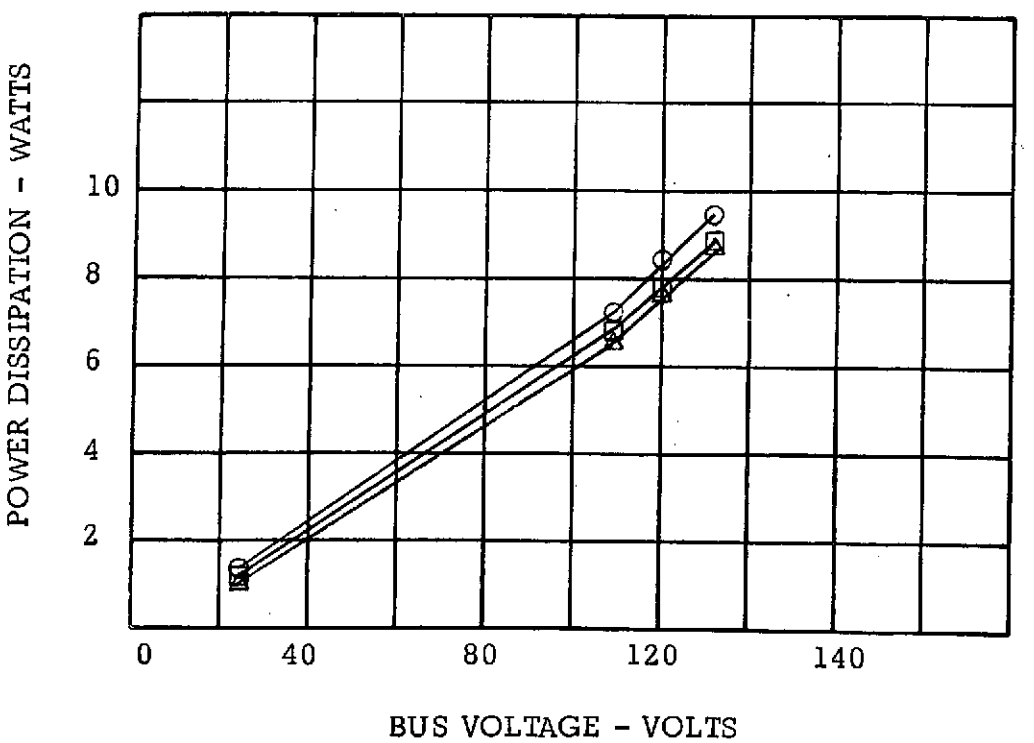


FIGURE 68 - SIMPLIFIED TYPE II BREADBOARD VOLTAGE DROP DATA

FIGURE 69 - SIMPLIFIED TYPE II BREADBOARD DISSIPATION DATA



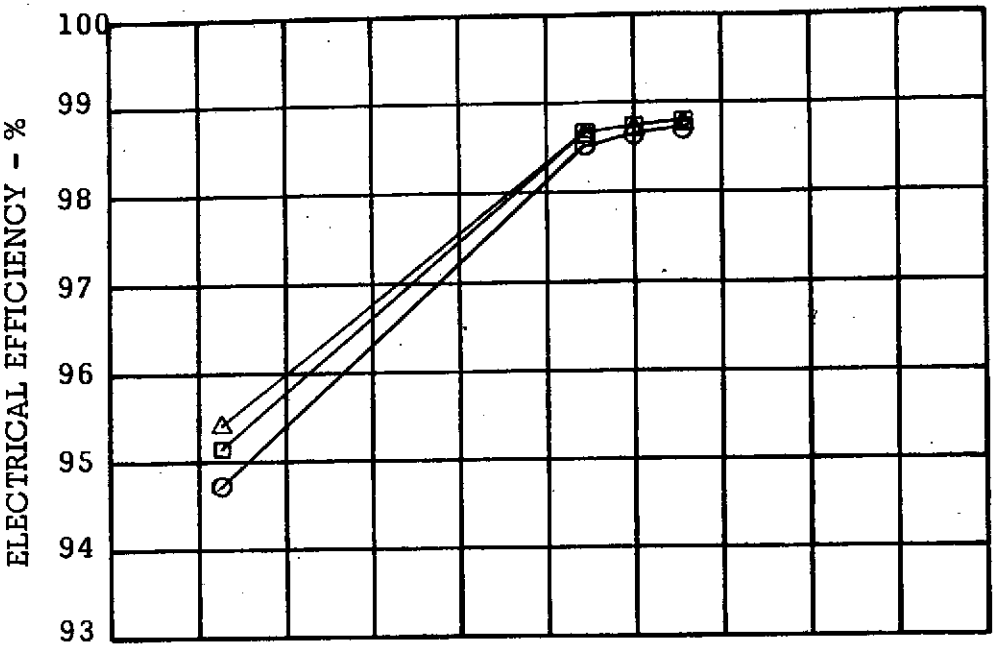


FIGURE 70 - SIMPLIFIED TYPE II BREADBOARD EFFICIENCY DATA

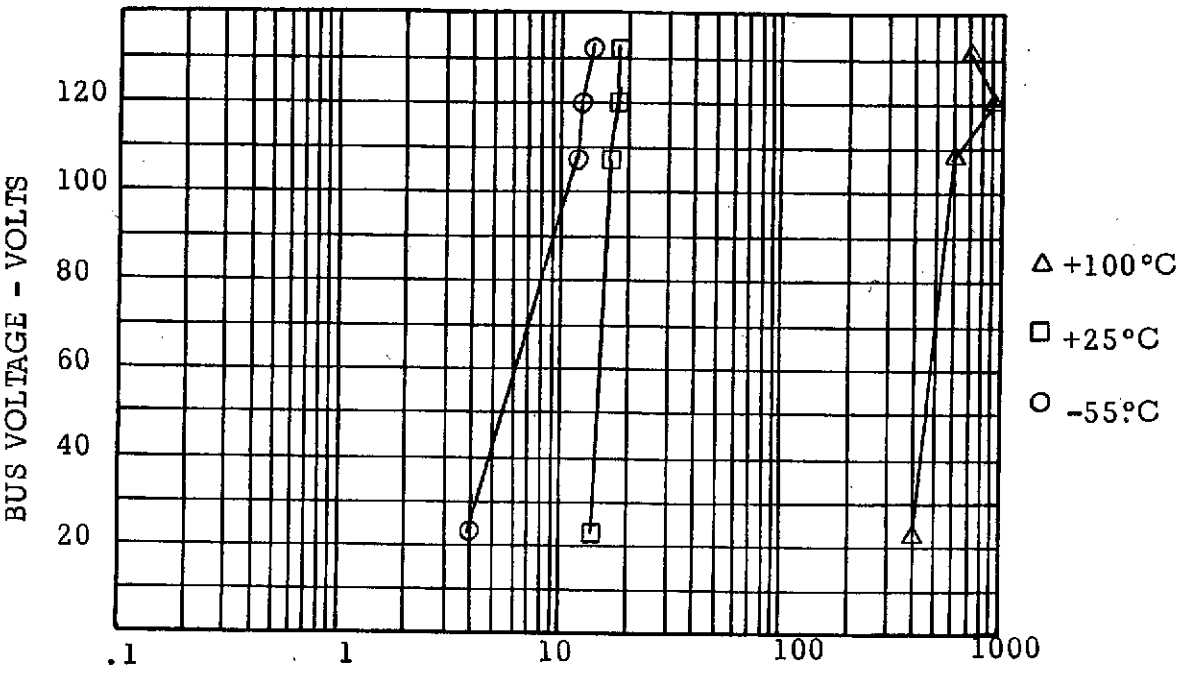
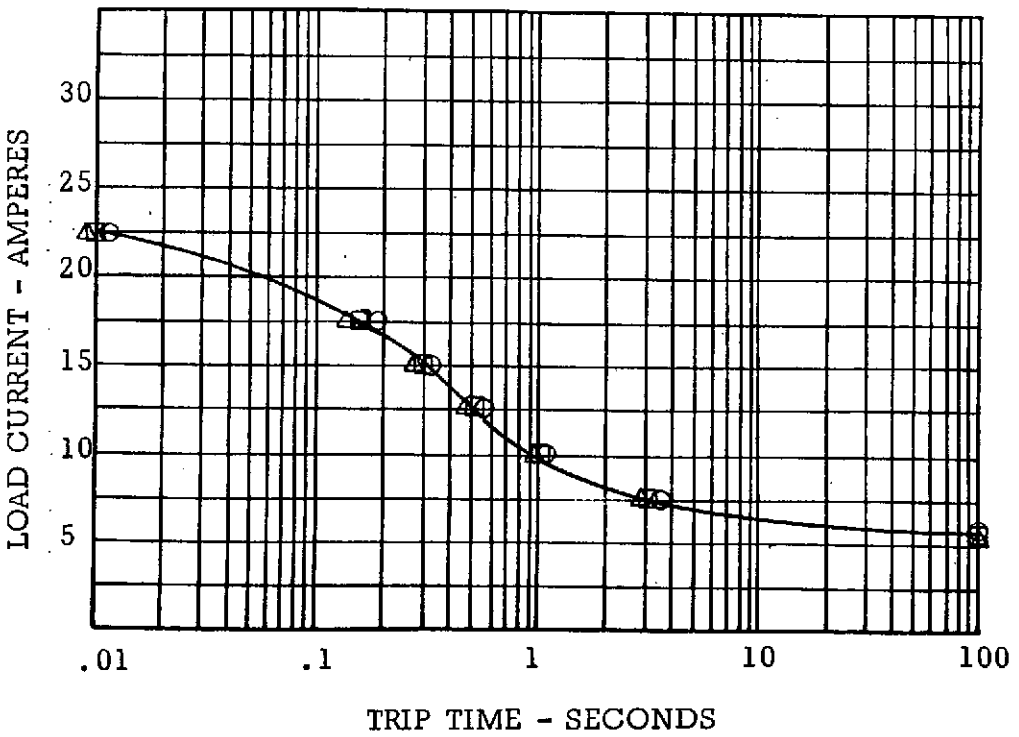


FIGURE 71 - SIMPLIFIED TYPE II BREADBOARD LEAKAGE DATA

FIGURE 72 - SIMPLIFIED TYPE II BREADBOARD TRIP TIME DATA



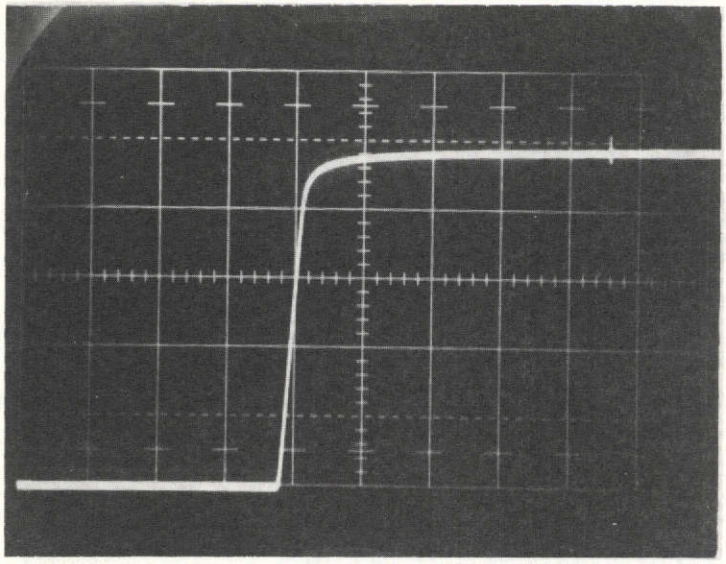


FIGURE 73 - Simplified Type II
Turn On Time

Vertical: Load Current, 1 amp/div.

Sweep: .2 millisecond/div.

V_{BUS} = 120 VDC, R_{LOAD} = 24 ohms

Temp. = 25°C

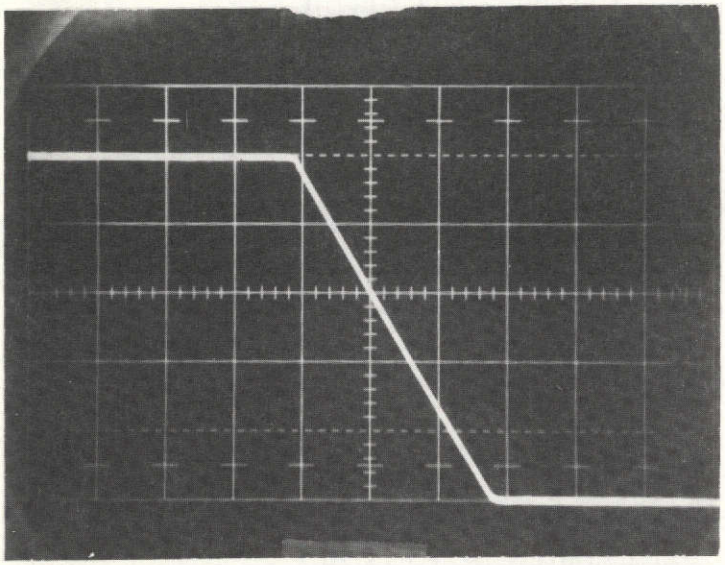


FIGURE 74 - Simplified Type II
Turn Off Time

Vertical: Load Current, 1 amp/div.

Sweep: .1 millisecond/div.

V_{BUS} = 120 VDC, R_{LOAD} = 24 ohms

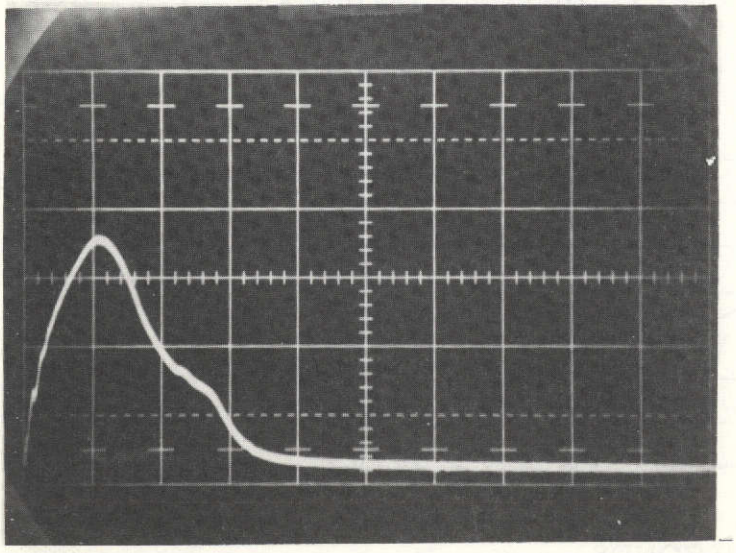


FIGURE 75 - Simplified Type II Response
To Applied Fault

Vertical: Load Current: 20 amp/div.

Sweep: 5 micro second/div.

V_{BUS} = 120 VDC, Temp. = 100°C

R_{LOAD} (T = 0-) = 24 ohms

R_{LOAD} (T = 0+) = 0 ohms

10.3 Performance Comparisons of Simplified and Original Circuit Designs

A complete performance comparison summary for the simplified and original circuit designs for the Type II and Type II RPC's is given in Appendix III. Also included in this Appendix is the recommended specification deviations for the simplified circuit designs.

APPENDIX I

TEST PLAN FOR ENGINEERING MODELS

DESCRIPTION

TEST PLAN FOR HIGH VOLTAGE SOLID STATE SWITCHGEAR FOR NASA LEWIS CONTRACT NO. NAS3-17771

APPROVAL	DATE
Engineer	
Design Sect. Mgr.	
Marketing Syst. Mgr.	
Qual. & Rel. Engrg.	
Supv. Standards	

REVISIONS	
A	Changed RS01 to CS06, Page 11 LDM 9/20/74

WESTINGHOUSE ELECTRIC CORP.
AEROSPACE ELECTRICAL DIV.
LIMA, OHIO, U. S. A.,

REV.	CODE IDENT NO.
	83843

DESIGN SPEC. NO. 774135

SHEET 1 OF 20

TEST PLAN FOR HIGH VOLTAGE SOLID STATE SWITCHGEAR FOR NASA LEWIS CONTRACT NO. NAS3-17771

1.0 SCOPE

This document covers the test plan which will be used to evaluate the Engineering Models (E/M's) built in Task IV of the referenced contract.

1.1 Units to be Evaluated

The switchgear to be evaluated consists of the following E/M's.

1.1.1 5 Ampere current limiting remote power controller per contract specification para. 5.1, hereinafter referred to as the Type I RPC.

1.1.2 5 Ampere non-current limiting remote power controller per contract specification para. 5.2, hereinafter referred to as the Type II RPC.

1.1.3 30 Ampere non-current limiting circuit breaker per contract specification para. 5.3, hereinafter referred to as the Type III RPC.

2.0 TEST SCHEDULE

The test schedule shall be as illustrated by Table I.

TABLE I
TEST SCHEDULE

Item No.	Tests	Para.	Temp. °C	Unit Serial Number		
				Type I	Type II	Type III
1.	Dielectric	4.1	25	1, 2	1, 2	1, 2
2.	Static Tests	4.2	25 -55 100	1, 2 1 1	1, 2 1 1	1, 2 1 1
3.	T_{on}, T_{off}, T_{rise}, T_{fall}	4.3	25 -55 100	1, 2 1 1	1, 2 1 1	1, 2 1 1
4.	Trip Characteristics	4.4	25 -55 100	1, 2 1 1	1, 2 1 1	1, 2 1 1
5.	Trip Free	4.5	25 -55 100	1, 2 1 1	1, 2 1 1	1, 2 1 1
6.	Automatic Reset	4.6	25 -55 100	1, 2 1 1	1, 2 1 1	1, 2 1 1
7.	Current Limit Level	4.7	25 -55 100	1, 2 1 1		
8.	Current Limit Ripple	4.8	25 -55 100	1, 2 1 1		
9.	Short Circuit Response	4.9	25 -55 100	1, 2 1 1		
10.	Instant Trip Set Level	4.10	25 -55 100		1, 2 1 1	1, 2 1 1
11.	Lamp Start Capability	4.11	25	1	1	1
12.	Coordination	4.12	25	1, 2	1, 2	1
13.	Transient Tests	4.13	25	1	1	1
14.	EMI Evaluation	4.14	25	2		2

3.0 TEST CIRCUIT CONFIGURATION

The test circuit shall be as shown by Figure 1 and it will be the basis of all tests performed on the E/M's.

3.1 Test Circuit Components

All instrumentation shall be calibrated in accordance with Westinghouse's standard quality assurance provisions. These provisions include meter calibration to MIL-C-45662A.

The remaining components in the test set up shall, as a minimum, be as specified below:

V_{Bus} Supply	Harrison Type 6475, 0-120 Volt, 0-100 Amp, Approx. 120,000 micro-farad output filter capacitor
V_{cont} Supply	0-30 Volt, 500 milliamp supply
R_{Load}	Variable Resistance, 0 to 50 ohms. 600 W at 24 ohms and 3.6 KW at 4 ohms.
Power Circuit Impedance. . .	#2 Copper stranded welding cable everywhere load current or fault current flows. 26 feet total length maximum.
Switch S2, S3.	200 Amp knife switch
Fault Contactor	Hartman AR751FC, 200 Amp, 224 Volt dc, S.P.S.T. Contactor
V_1, V_2.	Dana 4470 Digital Voltmeter
Oscilloscope	Tektronix 533, .022 microsecond rise time
Shunt	Non-inductive current metering shunt. T&M Research Products 1M-20, .01 ohm ohms

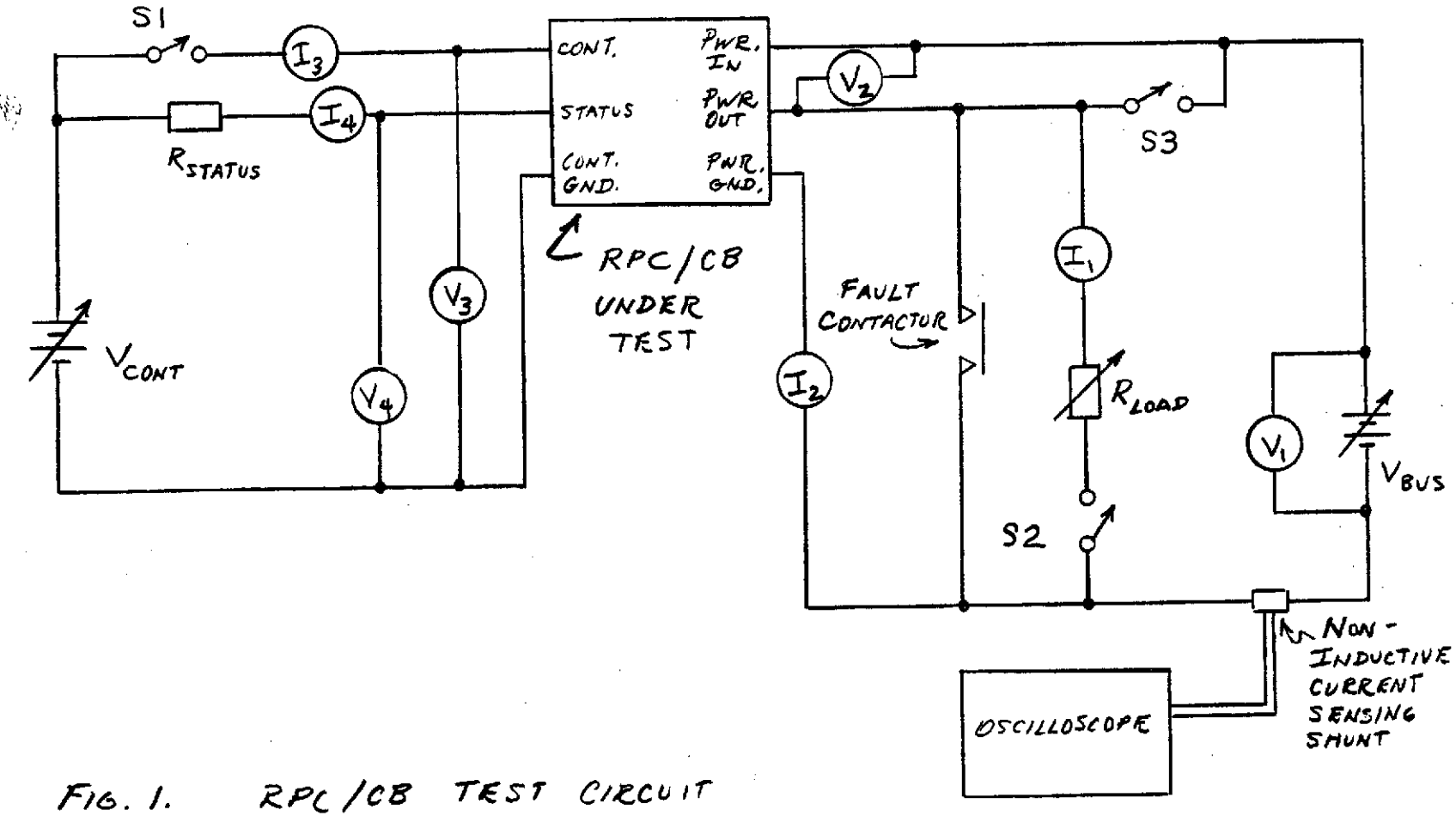


FIG. 1. RPC/CB TEST CIRCUIT

4.0 EVALUATION PROCEDURE

All test data shall be entered in the appropriate test data sheet shown in Appendix A. Tests at temperature extremes shall be performed on those units indicated by paragraph 2.0.

4.1 Dielectric

There shall be no leakage current in excess of five milliamperes nor evidence of arcing or flashover when 1000 VAC, 60 Hz is applied for one minute between all terminals and case. Repeat the above test except apply the test voltage between all power terminals and all control terminals.

NOTE: Unless otherwise specified all of the following tests will be at rated conditions; i.e., V_{Bus} = 120 VDC, I_{Load} = 5 amp (Types I & II), I_{Load} = 30 Amps (Type III), V_{cont} = 15 VDC (RPC On), V_{cont} = 0 VDC (RPC Off).

4.2 Static Tests

With the switchgear connected per para. 3.0 all meter readings shall be recorded with the switchgear in an "on state" and in an "off state". Test conditions shall be V_{Bus} = 80, 108, 120 and 132 volts dc, and ambient temperature shall be -55, +25, and +100°C. Control input voltage shall be 15 VDC or 0 depending upon the desired state of the switchgear except for $V_{3(on)}$ and $V_{3(off)}$ tests. Load shall be rated resistive load.

4.3 Turn-On and Turn-Off Characteristics

Turn-on and turn-off characteristics shall be monitored by an oscilloscope (Para. 3.0). Turn-on and turn-off times are defined as the time required for the load current to reach 90% of its final value after step application or removal of the control signal. Rise time and fall time are defined as the time required for the load current to go from 10% to 90% of its final value during turn-on or turn-off.

Test conditions shall be rated supply voltage and rated resistive load.

4.4 Trip Characteristics

Adjust load impedance to obtain an overload condition. Close the RPC by applying control voltage, monitor and record trip time. Supply voltage shall be at rated value. Overload current levels shall be as specified in the appropriate data sheet (see para. 4.0). The trip time is defined as the time between the current reaching 90% of the peak value at turn-on and falling to 10% of the same peak value at trip-off.

On Type II and Type III RPC's, program the appropriate instant trip level for each test point as defined by the data sheets, para. 4.0.

4.5 Trip Free

Verify during trip characteristics evaluation (para. 4.4) that the RPC is trip free, i.e., the RPC will trip even though the control signal remains at 15 VDC just prior to and after the trip-off occurs.

4.6 Automatic Reset

With the RPC programmed for no automatic resets, adjust the load for an overload, close the RPC and verify that only one overload trip occurs. With the RPC programmed for automatic reset again close the RPC and verify that three resets $\pm$ 0 occur. Record the average time between trip-off and automatic reset.

4.7 Current Limit Level

This paragraph applies to the Type I RPC only. Adjust the load impedance to zero ohms. Close the RPC, monitor and record the load current level. The load current will flow for .1 seconds before trip-off and therefore the measurement must be made quickly. Measurement of this current level is suggested by using the calibrated oscilloscope and current sensor. Adjust the oscilloscope time base to 10 milliseconds per division for this test. Repeat the above test for bus voltage settings of 132, 108 and 80 volts dc.

4.8 Current Limit Ripple

This paragraph applies to the Type I RPC only. Adjust the load impedance to zero ohms. Close the RPC by applying the control signal and record the peak to peak ripple current approximately 50 milliseconds after the load current begins to flow. The oscilloscope and current sensor must be used to make this measurement. Expand the oscilloscope time base and vertical gain as necessary to obtain accurate measurements. Repeat the test with the load impedance adjusted to 1.5, 3 and 6 ohm.

4.9 Short Circuit Current Limit Response Time

This paragraph applies to the Type I RPC only.

4.9.1 Close Into R_L = 0

With the RPC off close the fault contactor. Subsequently close the RPC, monitor the load current, and record the short circuit response time. This time is defined as the interval between the time the current initially reaches 100% of current limiting level and the time the current falls & stays within a band equal to ±10% of the current limiting level. Also record the peak current level.

4.9.2 Apply R_L = 0 to RPC

Repeat test 4.9.1 above except with the RPC closed and carrying no load current, close the fault contactor.

4.9.3 Apply R_L = 0 to RPC with Preload

Repeat test 4.9.2 above except adjust load resistance to demand 5 amps load current before the fault contactor is closed.

4.10 Instant Trip Set Level

This paragraph applies to the Type II and III RPC's only.

4.10.1 With the RPC off close the fault contactor. Subsequently close the RPC and monitor the load current and record the short circuit trip time. This time is defined as the interval between the current reaching the instant trip set point level then falling to 10% during trip off. Also record the peak current level. Repeat the test for each instant trip set point; i.e., I.T. = 2X, 3X, 4X, or 5X.

4.10.2 Repeat paragraph 4.10.1 above except with the RPC closed and carrying no load current, close the fault contactor.

4.10.3 Repeat test 4.10.2 above except adjust load resistance to draw 5 amps load current before the fault contactor is closed.

4.11 Lamp Start Capability

120 VAC incandescent lamps shall be used as a load for this test. Begin test with sufficient lamp load to insure that RPC always trips off during

lamp start. Decrease lamp load by 50 watt increments until the lamp load can be started without trip-off. During all testing allow 30 seconds between restart attempts to insure that filaments are cold. Do not leave lamps on more than 5 seconds at a time.

4.12 Coordination (Series Operation)

Test performed under this paragraph shall use the connection schematic shown by Figure 2. In addition load resistors R1, R2 and R3 shall be adjusted to provide the following load currents when the RPC's are on:

I_3	20 Amperes
I_2	5 Amperes
I_1	5 Amperes

Unless otherwise specified S4 and S5 are to be open.

4.12.1 With S2 and S3 open, close S1, then close S2 and S3 and observe that the Type I and Type II RPC's supply current to their respective loads.

4.12.2 Open S1, S2 and S3. Close S1 and observe that the Type I and Type II RPC's block current flow to their respective loads.

4.12.3 Close S1, then close S2 and S3. Close S4 and observe that the Type I limits I_1 to 15 amps for $.1 \pm .03$ seconds and then trips off. Neither the Type II nor the Type III RPC shall trip off. Repeat the test except Close S4 and then close S2. The results shall be the same.

4.12.4 Close S1, then close S2 and S3. Close S5 and observe that the Type II RPC trips off. Neither the Type I nor the Type III RPC shall trip off. Repeat the test except close S5 and then close S3. The results shall be the same.

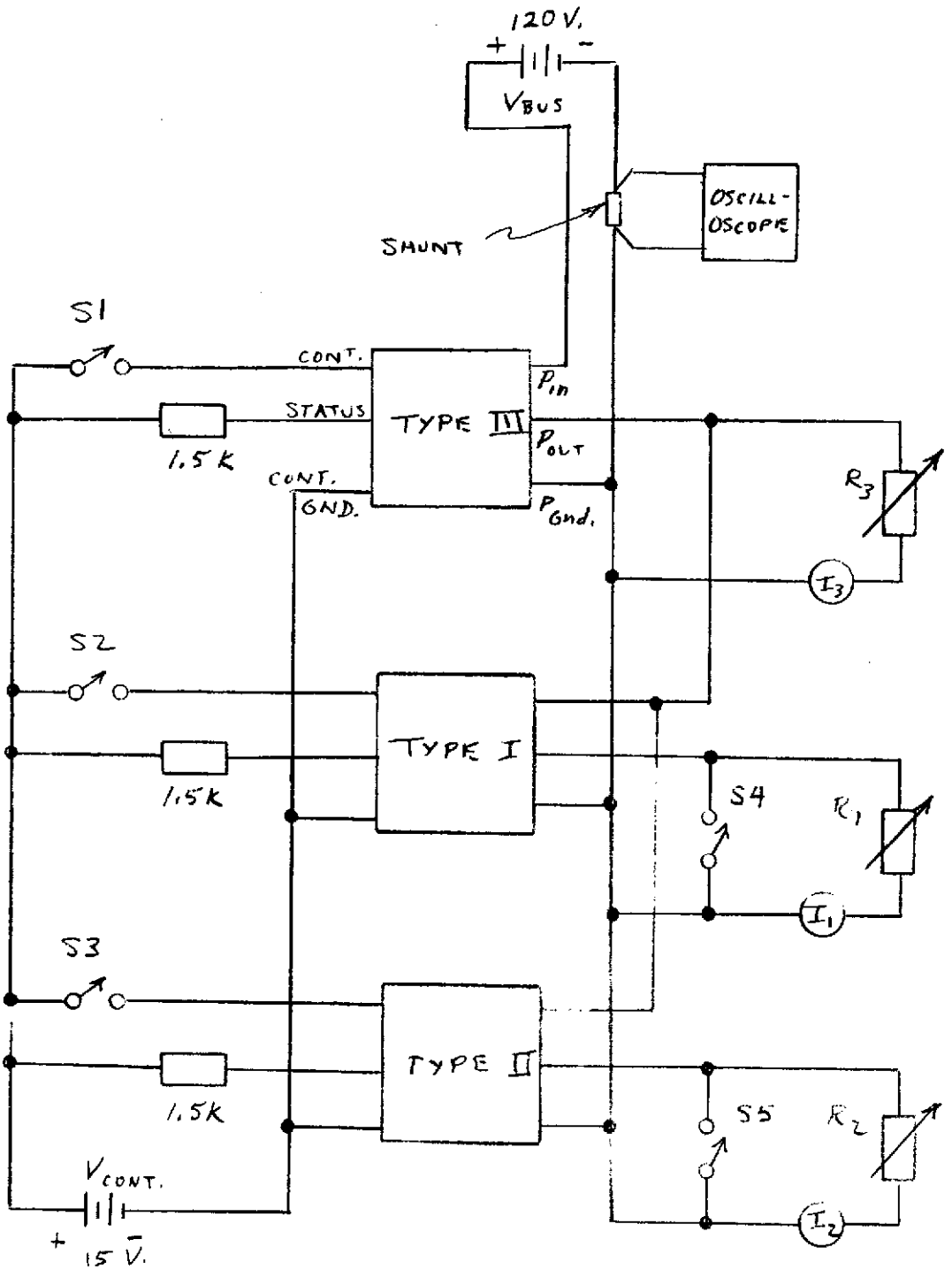


FIGURE 2 COORDINATION TEST CIRCUIT

4.13 Transient Test

4.13.1 200 Volt Transient Test

With rated load and supply voltage applied, close the RPC. To the 120 volt supply voltage add an 80 volt, 50 microsecond transient and verify that the RPC remains on by monitoring the RPC voltage drop. Repeat the test with the RPC off and verify that the RPC remains off by monitoring the load voltage. Use an oscilloscope as the voltage monitor.

4.13.2 -65 Volt Transient Test

With the RPC disconnected from the + supply terminal, apply a -65 volt, 50 microsecond transient to the RPC + supply terminals through a 10 ohm resistor. Verify that the RPC was not damaged.

4.14 EMI Evaluation

EMI generation and susceptibility tests shall be performed per MIL-STD-461A Class ID equipment. Specifically, the tests to be performed shall be:

CE 01
CE 02
CE 03
CE 04
CS 01
CS 02
RE 02
CS 06
RS 02
RS 03 (to 480 MHz max.)

These tests are for engineering evaluation only and therefore non-compliance with the specific test limits shall not constitute failure of the unit.

APPENDIX A

TEST DATA ENTRY SHEETS

Para. 4.2 Static Data
Device Tested _____
Serial No. _____
Test Conditions: V_{Bus} = 80V, 108V, 120V, 132V dc
R_{Load} = 24 ohms, 600 watts
V_{Cont} = 15 volt dc
Temp. = -55°C, +25°C, +100°C

Item	Units	State	V_{Bus} 80V Temp °C			108V Temp.°C			120V Temp.°C			132V Temp.°C			Limits
			-55	+25	+100	-55	+25	+100	-55	+25	+100	-55	+25	+100	
V_1 V_2 V_3 V_4	Volts ↓	On ↓													--- 1.0 max. --- 1.5 max.**
I_1 I_2 I_3 I_4	Amps Milliamps ↓														--- --- 10 ± 1 ---
*P_{Loss}	Watts	↓													I - 12 max.** II - 17 max.** III - 40 max.**
V_1 V_2 V_3 V_4	Volts ↓	Off ↓													--- --- --- ---
I_1 I_2 I_3 I_4	Microamp Milliamp ↓														5000 max. 15 max.** --- .1
*P_{Loss}	Watts	↓													2.5 max.**
V_3 (on) V_3 (off)	Volts Volts	Just On Just Off													7.5±.75** 7.5±.75**

*Calculated from $(V_1)(I_2) + (V2)(I_1)$
**These limits were established from calculated worst case performance.

DIELECTRIC OK_____
Para. 4.1

DYNAMIC TEST DATA FOR 5 AMP CURRENT LIMITING TYPE I RPC

SERIAL NO. OF UNIT TESTED: _____

TEST CONDITIONS: V_{Bus} = 120 VDC
V_{Cont} = 15 Volts
Temp. = -55°C, +25°C, +100°C

Para.	Item	Special Conditions Other than Rated	Units	Temp °C			Limits
				-55	+25	+100	
4.3	Turn on Time, T_{on}**	Rated load, R_L = 24 ohm	microsec				10-10,000
4.3	Rise Time, T_R		microsec				10-10,000
4.3	Turn Off Time, T_{off}**		microsec				10-10,000
4.3	Fall time, T_F		microsec				10-10,000
4.6	Auto Reset Delay Time	R_L = 0	seconds				1 ± .2
4.4	Ultimate Trip Current	Vary R_{Load} and monitor Z202 output	Amps				6 ± .3*
4.4	7.5 amp trip time	R_L = 16 ohm	second				1.05 ± .20*
4.4	10 amp trip time	R_L = 12 ohm					.34 ± .07*
4.4	12.5 amp trip time	R_L = 9.6 ohm					.17 ± .035*
4.4	20 amp trip time	R_L = 6 ohm					.1 ± .03*
4.4	S.C. trip time	R_L = 0					.1 ± .03*
4.9	Short Circuit Current Limit Response Time	a) Close into R_L = 0**	millisec				
		b) Apply R_L = 0 to RPC**	millisec				
		c) Apply R_L = 0 to RPC**	millisec				
4.7	Current Limit Level	a) R_L = 0, V_{Bus} = 120	Amps				
		b) R_L = 0, V_{Bus} = 132					
		c) R_L = 0, V_{Bus} = 108					
		d) R_L = 0, V_{Bus} = 80					
4.11	Lamp Load Compatibility Test	Cold Filament	Watts Max.				
4.13.1	+200V Transient (Record V_{Load} Peak)	a) Rated Load, On	Volts				
		b) Rated Load, OFF	Volts				
4.13.2	-65V Transient						

*These limits established from calculated worst case performance data.
**Record results (I_{Load}) of these tests with oscilloscope photograph.

DYNAMIC TEST DATA FOR 5 AMP CURRENT LIMITING TYPE I RPC (Cont'd)

SERIAL NO. OF UNIT TESTED: _____

TEST CONDITIONS: V_{Bus} = 120 VDC
VCont = 15 Volts
Temp. = -55°C, +25°C, +100°C

Para.	Item	Special Conditions Other than Rated	Units	Temp °C			Limits
				-55	+25	+100	
4.8	Current Limit Ripple	a) R_L = 6 ohm b) R_L = 3 ohm c) R_L = 1.5 ohm d) R_L = 0 ohm**	Amps P-P				
4.5	Trip Free		Indicate if OK				
4.9	Short Circuit Current Limit Peak Current	a) Close into R_L = 0 b) Apply R_L = 0 to RPC c) Apply R_L = 0 to RPC with 5 amp preload	Amps				

*These limits established from calculated worst case performance data.
**Record results (I_{Load}) of these tests with oscilloscope photograph.

DYNAMIC TEST DATA FOR 5 AMP INSTANT TRIP TYPE II RPC

SERIAL NO. OF UNIT TESTED: _____

TEST CONDITIONS: V_{Bus} = 120 VDC
V_{Cont} = 15 VDC
Temp. = -55°C, +25°C, +100°C

Para.	Item	Special Conditions Other than Rated	Units	Temp °C			Limits
				-55	+25	+100	
4.3	Turn on Time, T_{on}	Rated Load, RL = 24*	microsec				10-10,000
4.3	Rise Time, T_R	Rated Load, R_L = 24	microsec				10-10,000
4.3	Turn off Time, T_{off}	Rated Load, R_L = 24*	microsec				10-10,000
4.3	Fall time, T_F	Rated Load, R_L = 24	microsec				10-10,000
4.6	Auto Reset Delay Time	R_L = 0, I.T. = 25**	seconds				1 ± .2
4.4	Ultimate Trip Current Level	Vary R_{Load} and monitor Z202 output	Amp				6 ± .3
4.4	7.5 amp trip time	R_L = 16 ohms	second				.29 ± .075
4.4	10 amp trip time	R_L = 12 ohms					.094 ± .018
4.4	12.5 amp trip time	R_L = 9.6 ohms					.048 ± .009
4.4	15 amp trip time	R_L I.T.**					
		a) 8 15					0-.034
		b) 8 20					.028±.006
		c) 8 25					.028 ± .006
4.4	17.5 amp trip time	a) 6.86 15					0 - .02
		b) 6.86 20					.016 ± .004
		c) 6.86 25					.016 ± .004
4.4	20 amp trip time	a) 6 15					10^{-4} max.
		b) 6 20					0 - .012
		c) 6 25					.009 ± .003
4.4	25 amp trip time	a) 4.8 15					10^{-4} max.
		b) 4.8 20					10^{-4} max.
		c) 4.8 25					0 - .0015

*Record results (I_{Load}) of these tests with oscilloscope photograph.
**I. T. = Instant Trip current set point in amps.
NOTE: All trip time limits established from calculated worst case performance.

DYNAMIC TEST DATA FOR 5 AMP INSTANT TRIP TYPE II RPC (Cont'd)

SERIAL NO. OF UNIT TESTED: _____

TEST CONDITIONS: V_{Bus} = 120 VDC
V_{Cont} = 15 VDC
Temp. = -55°C, +25°C, +100°C

Para.	Item	Special Conditions Other than Rated	Units	Temp °C			Limits
				-55	+25	+100	
4.4	40 amp trip time	a) 3 15 b) 3 20 c) 3 25					10^{-4} max. 10^{-4} max.
4.10.1	S.C. Trip Time (close RPC into fault)	a) 0 15 b) 0 20 c) 0 25*					
4.10.3	S.C. Trip Time (applied fault with 5 amp preload)	a) 0 15 b) 0 20 c) 0 25*					
4.10.2	S.C. Trip Time (applied fault)	a) 0 15 b) 0 20 c) 0 25*					
4.10.1	S.C. Peak Current (close RPC into fault)	a) 0 15 b) 0 20 c) 0 25	Amps				
4.10.2	S.C. Peak Current (applied fault)	a) 0 15 b) 0 20 c) 0 25					
4.10.3	S.C. Peak Current (applied fault with 5 amp preload)	a) 0 15 b) 0 20 c) 0 25					
4.11	Lamp Load Compatibility Test	Cold Filament	Watts Max				

*Record results (I_{Load}) of these tests with oscilloscope photograph.

DYNAMIC TEST DATA FOR 5 AMP INSTANT TRIP TYPE II RPC (Cont'd)

SERIAL NO. OF UNIT TESTED: _____

TEST CONDITIONS: V_{Bus} = 120 VDC
V_{Cont} = 15 VDC
Temp. = -55°C, +25°C, +100°C

Para.	Item	Special Conditions Other than Rated	Units	Temp °C			Limits
				-55	+25	+100	
4.13.1	+200V Transient (Record V_{Load} Peak)	a) Rated Load, On b) Rated Load, Off	Volts Volts				
4.13.2	-65V Transient						
4.5	Trip Free		Indicate if OK				

DYNAMIC TEST DATA FOR 30 AMP INSTANT TRIP TYPE III RPC

SERIAL NO. OF UNIT TESTED: _____

TEST CONDITIONS: V_{Bus} = 120 VDC
V_{Cont} = 15 VDC
Temp. = -55°C, +25°C, +100°C

Para.	Item	Special Conditions Other than Rated		Units	Temp °C			Limits
					-55	+25	+100	
4.3	Turn on Time, T_{on}	Rated Load, R_L = 4ohms*		microsec				10-10,000
4.3	Rise Time, T_R							
4.3	Turn Off Time, T_{off}	*						
4.3	Fall Time, T_F							
4.6	Auto Reset Delay Time	R_L = 0, I.T. = 90 **		seconds				1 ± .2
4.4	Ultimate Trip Current Level	Vary R_L and monitor Z202 output		Amps				36 ± 1.8
4.4	45 Amp Trip Time	R_L = 2.67 ohms						.128 ± .03
		R_L	I.T.**					
4.4	60 Amp Trip Time	a) 2	60	Seconds				.0 - .049
		b) 2	90					.041 ± .008
4.4	75 Amp Trip Time	a) 1.6	60					10^{-4} max.
		b) 1.6	90					.02 ± .004
4.4	90 Amp Trip Time	a) 1.33	60					10^{-4} max.
		b) 1.33	90					0 - .015
4.4	200 Amp Trip Time	a) .60	60					10^{-4} max.
		b) .60	90					10^{-4} max.
4.10.1	S.C. Trip Time (close RPC into fault)	a) 0	60					
		b) 0	90*					
4.10.2	S.C. Trip Time (applied fault)	a) 0	60					
		b) 0	90*					

*Record results (I_{Load}) of these tests with oscilloscope photograph.

**I.T. = Instant Trip Current set point in amps.

NOTE: All trip time limits established from worst case performance calculations.

DYNAMIC TEST DATA FOR 30 AMP INSTANT TRIP TYPE III RPC (Contd)

SERIAL NO. OF UNIT TESTED:_____

TEST CONDITIONS: V_{Bus} = 120 VDC
V_{Cont} = 15 VDC
Temp. = -55°C, +25°C, +100°C

Para.	Item	Special Conditions Other than Rated	Units	Temp °C			Limits
				-55	+25	+100	
4.10.3	S.C. trip time (applied fault with 30 amp preload)	a) 0 60 b) 0 90*	Seconds				
4.10.1	S.C. Peak Current (close RPC into fault)	a) 0 60 b) 0 90	Amps				
4.10.2	S.C. Peak Current (applied fault)	a) 0 60 b) 0 90					
4.10.3	S.C. Peak Current (applied fault with 30 amp preload)	a) 0 60 b) 0 90					
4.11	Lamp Load Compatibility Test	Cold Filament	Max. Watts				
4.13.1	+200V Transient (Record V_{Load}) Peak	a) Rated Load, On b) Rated Load, Off	Volts Volts				
4.13.2	-65V Transient (Record V_{Load})						
4.5	Trip Free		Indicate if OK				

*Record results (I_{Load}) of these tests with oscilloscope photo.

APPENDIX II

APPLICATION GUIDELINES FOR THE ENGINEERING MODELS

APPLICATION GUIDELINES FOR THE 120VDC SWITCHGEAR ENGINEERING MODELS

CONTRACT: SOLID STATE SWITCHGEAR TECHNOLOGY DEVELOPMENT

NUMBER: NAS-3-17771

Prepared By:

CONTROL SYSTEMS ENGINEERING
WESTINGHOUSE ELECTRIC CORPORATION
AEROSPACE ELECTRICAL DIVISION

AUTHOR: D.E. Baker

DATE: September 24, 1974

Prepared For:

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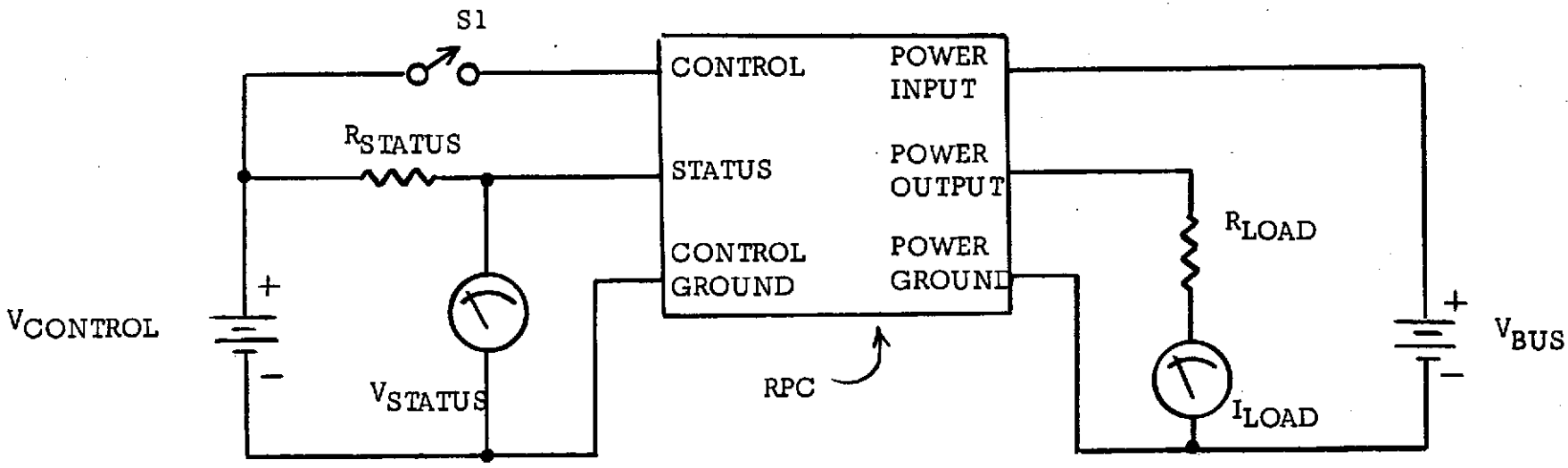


FIGURE 1 - CONNECTION DIAGRAM FOR TYPE 1, 2, & 3 RPC.

I. CONNECTIONS

The RPC or Circuit Breaker should be connected as shown by figure 1. The control side of the unit should be wired with conductors sufficient to carry 10 milliamps steady state. The power side of the unit should be wired with conductors sufficient to carry current equal to the rating of the unit.

II. RATINGS

A. Control

Nominal Control input voltage----------15VDC
Max " " " ----------30VDC
Nominal Control input current----------10 milliamp.
Status sink current----------10 milliamp.

Turn on Control Voltage----------7.5 $\pm$ .75 VDC
Turn off Control Voltage----------7.5 $\pm$ .75 VDC

Status voltage (sinking)----------1.2 volts max at 10 milliamps.
Status voltage (open)----------15 VDC.

B. Power

1. Type I

Nominal Bus Voltage----------120 $\pm$ 12 VDC
Max. Bus Voltage----------200 VDC for 50 microseconds
Load Current----------5 amps Nominal
Ultimate Trip Level----------6 $\pm$ .3 amps.
Current Limit Level----------15 $\pm$ 1 amps.
Trip time equation----------$T = .09\left(\frac{25 - I}{I - 6}\right)$

2. Type II

Nominal Bus Voltage----------120 ± 12VDC
Max Bus Voltage----------200 VDC for 50 microseconds
Load Current----------5 amps Nominal
Ultimate Trip Level----------6 ± .3 amps.
Instant trip level----------Selectable at 15,20 or 25 amps.
Trip Time equation----------$T = .025 \left(\frac{25 - I}{I - 6}\right)$

3. Type III

Nominal Bus Voltage----------120 ± 12 VDC
Max. Bus Voltage----------200 VDC for 50 microseconds
Load Current----------30 amps. Nominal
Ultimate Trip Level----------36 ± 1.8 amps.
Instant Trip Level----------Selectable at 60 or 90 amps.
Trip Time Equation----------$T = .011 \left(\frac{150 - I}{I - 36}\right)$

III. OPERATION

With the RPC or circuit breaker connected per figure 1 the RPC will inhibit load current when S1 is open. With S1 closed the RPC will energize the load. Voltage drop from the power input terminal to the power output terminal will be 1 VDC or less if the load current is equal to or less than the rating of the unit. Overload currents in excess of the ultimate trip level will cause the RPC to trip off. The trip time is defined by the trip time equation as defined in section II.

For severe overloads the Type I RPC will limit max. current to 15 amps for .1 $\pm$ 03 seconds. For severe overloads the Type II and III RPC's will trip off instantly (approx. 10 microseconds) when the load current crosses the instant trip level specified in section II. The tripped state is reset by momentarily relaxing the control signal for 20 milliseconds minimum.

The status indication logic is as shown below:

State	Normal		V_{BUS} Dead		$V_{CONT.}$ Dead	
	Cont.	Status	Cont.	Status	Cont.	Status
On	1	0	1	1	θ	θ
Off	0	1	0	1	0	0
Tripped	1	1	θ	θ	θ	θ

1 = high, 0 = Low, θ = impossible condition

IV. PRECAUTIONS

1. Always be sure that the power ground terminal is connected to the negative side of the bus supply. If this line is metered (for current) it is advisable to by-pass the ammeter with a switch which is depressed only when a reading is taken. This will prevent the possibility of an inductive load commutation spike (at turn off) from blowing a meter fuse and hence disconnecting the power ground terminal.

2. To insure proper start up, power up the bus power supply before the RPC is turned on.

3. The bus power supply must be capable of delivering 200 amps short duration (1-10 milliseconds) with a voltage drop to 80 VDC minimum when using the Type II or III RPC's.

4. Fan cool the Type III unit.

APPENDIX III

PERFORMANCE AND COST COMPARISON

OF THE ORIGINAL AND THE SIMPLIFIED CIRCUIT DESIGNS

PART I

TYPE I, 5 AMPERE, 120 VOLT DC

CURRENT LIMITING RPC

TABLE I
PERFORMANCE COMPARISON OF THE TYPE I ORIGINAL DESIGN AND THE FINAL SIMPLIFIED DESIGN

Item	Original Design	New Simplified Design	Comments
1. Voltage Drop at rated conditions	.4 to .55 volts dc	1.15 volts, dc	Should be acceptable for a 120 volt system
2. Max. Voltage Drop	.67 volts (+100°C, 110% load)	1.26 volts (-55°C, 110% load)	
3. Power Dissipation at rated conditions	8.2 to 9.1 watts	7.87 watts	New design dissipates less power
4. Efficiency at rated conditions	98.5%	98.7%	More efficient than old design
5. Max. Dissipation	11.75 watts (100°C, 110% load)	9.11 watts (-55°C, 110% load)	New design exhibits a more desirable negative temperature coefficient.
6. Operating voltage range (power bus)	80 V. to 132 Vdc continuous	20 V, to 132 Vdc continuous	New design is completely functional at 20VDC, and is capable of limited operation to 10VDC.
7. Efficiency at 25 Vdc bus voltage	N.A.	95% at rated load current	Old design is not functional below approx. 45 volts.
8. Trip Characteristics	Meets $T_T = .09 \frac{(25 - I)}{(I - 6)}$	Same as original design	See figures 4 and 8

TABLE I (Cont'd)

Item	Original Design	New Simplified Design	Comments
9. Current Limiting Performance	3x rated current from 80 V, to 200V.	2.7x rated current from 25V, to 108V., 5x max. at 200V.	See figures 1 and 2. Compatible with 4500 amp source.
10. Current Limiting Settling time	1.0 milliseconds	15 micro seconds	
11. Automatic Reset	Selectable 0 or 3 times	None	
12. Lamp Start Capability	775 watts	700 watts	Incandescent Type
13. EMI generation and susceptability	Good, meets MIL-STD-461A	Should be much better than original design.	No EMI tests were run on new design.
14. No. of electrical components	138	81	Reduced by 41%
15. Cost of electrical components	$225	$79	Reduced by 65%

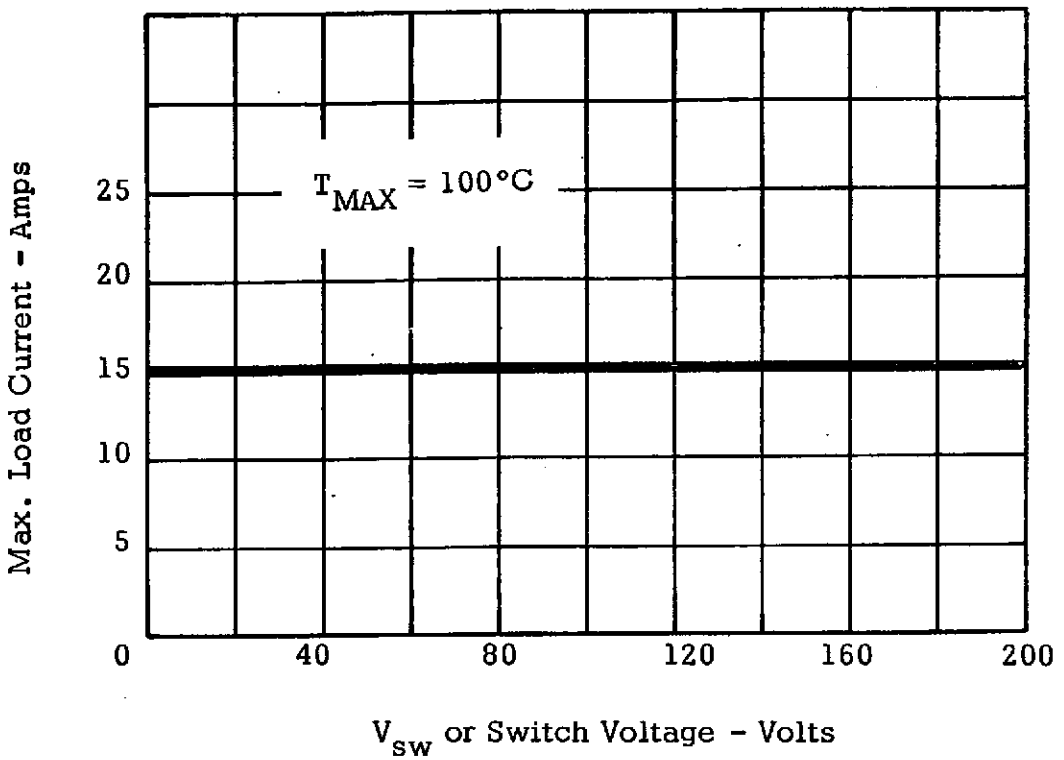
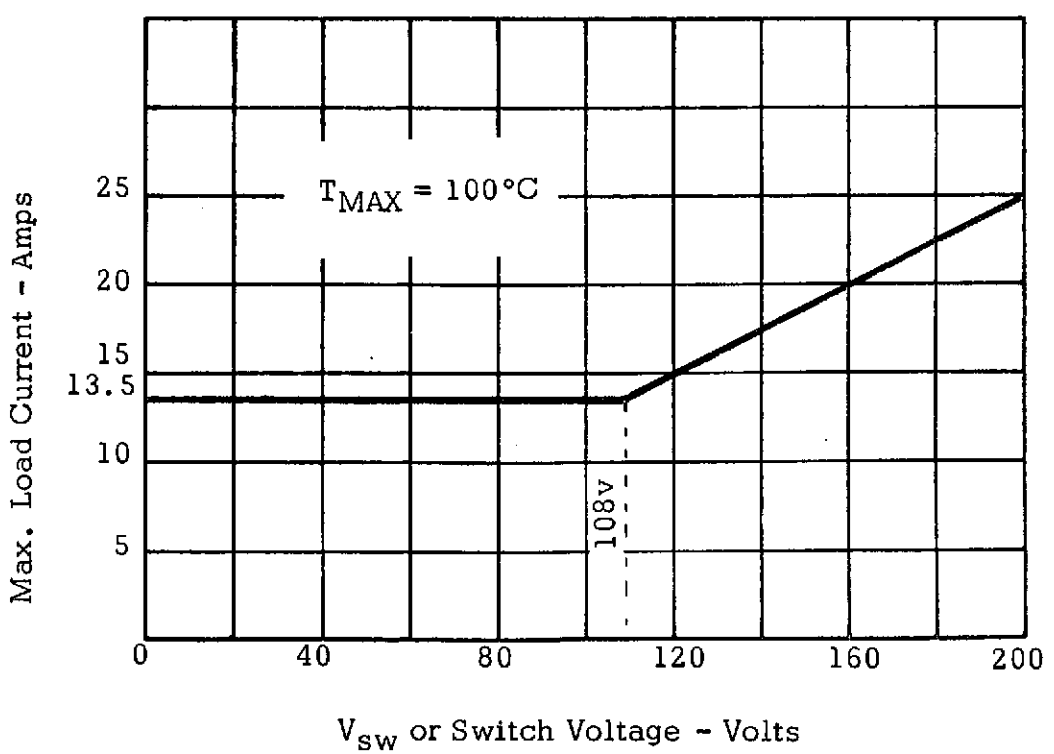


Figure 1 - Original Type I Current Limiting Performance Using an Active Helper - 3 Alloy Transistors

Figure 2 - Current Limiting Performance of Simplified Type I RPC with Passive Helper - 1 Alloy Transistor



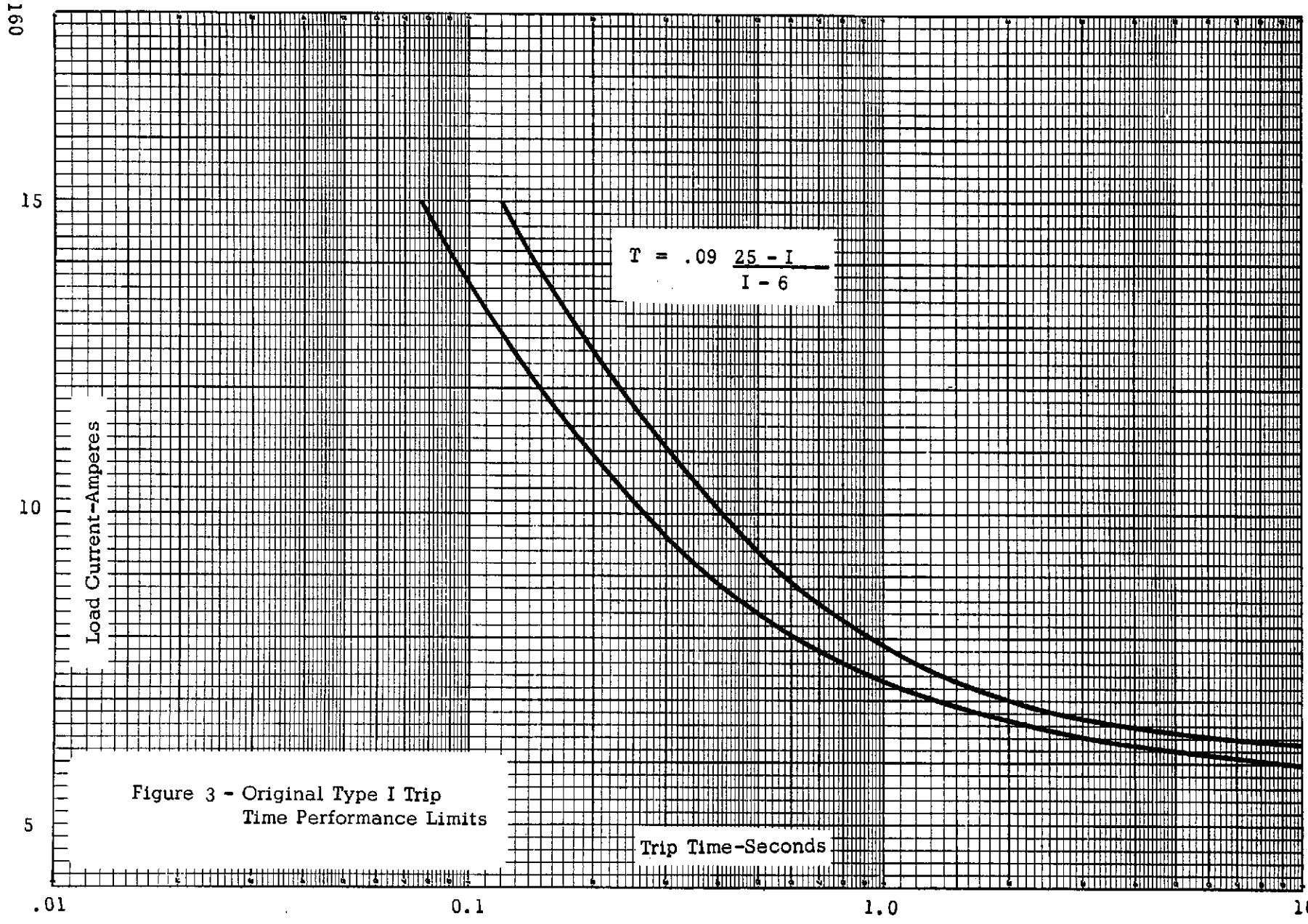


Figure 3 - Original Type I Trip Time Performance Limits

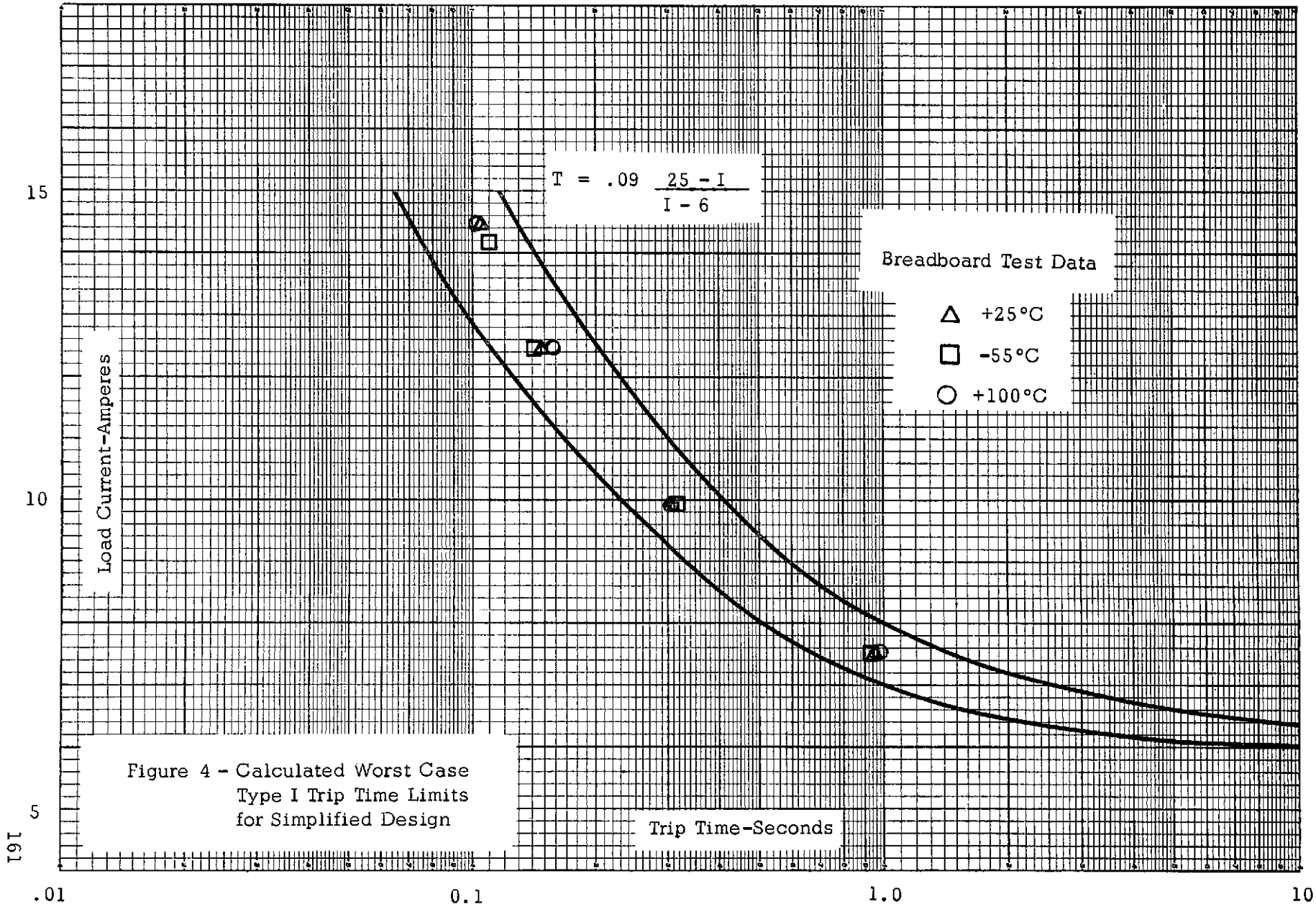


Figure 4 - Calculated Worst Case Type I Trip Time Limits for Simplified Design

PART II

TYPE II, 5 AMPERE, 120 VOLT DC

INSTANT TRIP RPC

TABLE III
PERFORMANCE COMPARISON OF THE TYPE II ORIGINAL DESIGN AND THE FINAL SIMPLIFIED DESIGN

Item	Original Design	New Simplified Design	Comments
1. Voltage drop at rated conditions	.46 to .53 volts dc	1.16 volts dc	Should be acceptable for a 120 volt system.
2. Max voltage drop	.62 volts (+ 100°C, 110% load)	1.35 volts (-55.C, 110% load)	
3. Power dissipation at rated conditions	6.2 to 7.1 watts	7.84 watts	New design dissipates slightly more power.
4. Efficiency at rated conditions.	98.8 to 98.9%	98.7%	Increased dissipation reflects a lower efficiency, however, the sacrifice is small.
5. Max. dissipation	9.22 watts (+ 100°C, 110% load)	9.37 watts (-55°C, 110% load)	New design exhibits a more desirable negative temperature coefficient.
6. Operating voltage range (power bus)	80 V. to 132 V. continuous	20 V. to 132 V. continuous	New design is completely functioned at 20VDC, and is capable of limited operation to 10VDC.
7. Efficiency at 25 VDC bus voltage	N.A.	94.7% at rated current	Old design not functional below approx. 60V.

TABLE III (Cont'd)

Item	Original Design	New Simplified Design	Comments
8. Trip Characteristics	Meets $T_T = .025 \frac{(25 - I)}{(I - 6)}$	Same as original design	See figures 5 and 9. The new design has a fixed 5x instant trip level. The original design has selectable 3x, 4x, & 5x instant trip levels.
9. Short circuit capability	Compatible with 4500 amp source.	Compatible with 4500 amp source.	
10. Automatic Reset	Selectable 0 or 3 times	None	
11. Lamp Start Capability	300 watts	300 watts	Incandescent Type
12. EMI generation and susceptability	Good, meets MIL - STD-461A	Should be much better than original design.	No EMI Tests were run on new design
13. No. of electrical components	117	78	Reduced by 39 %
14. Cost of electrical components	$103	$57	Reduced by 45 %

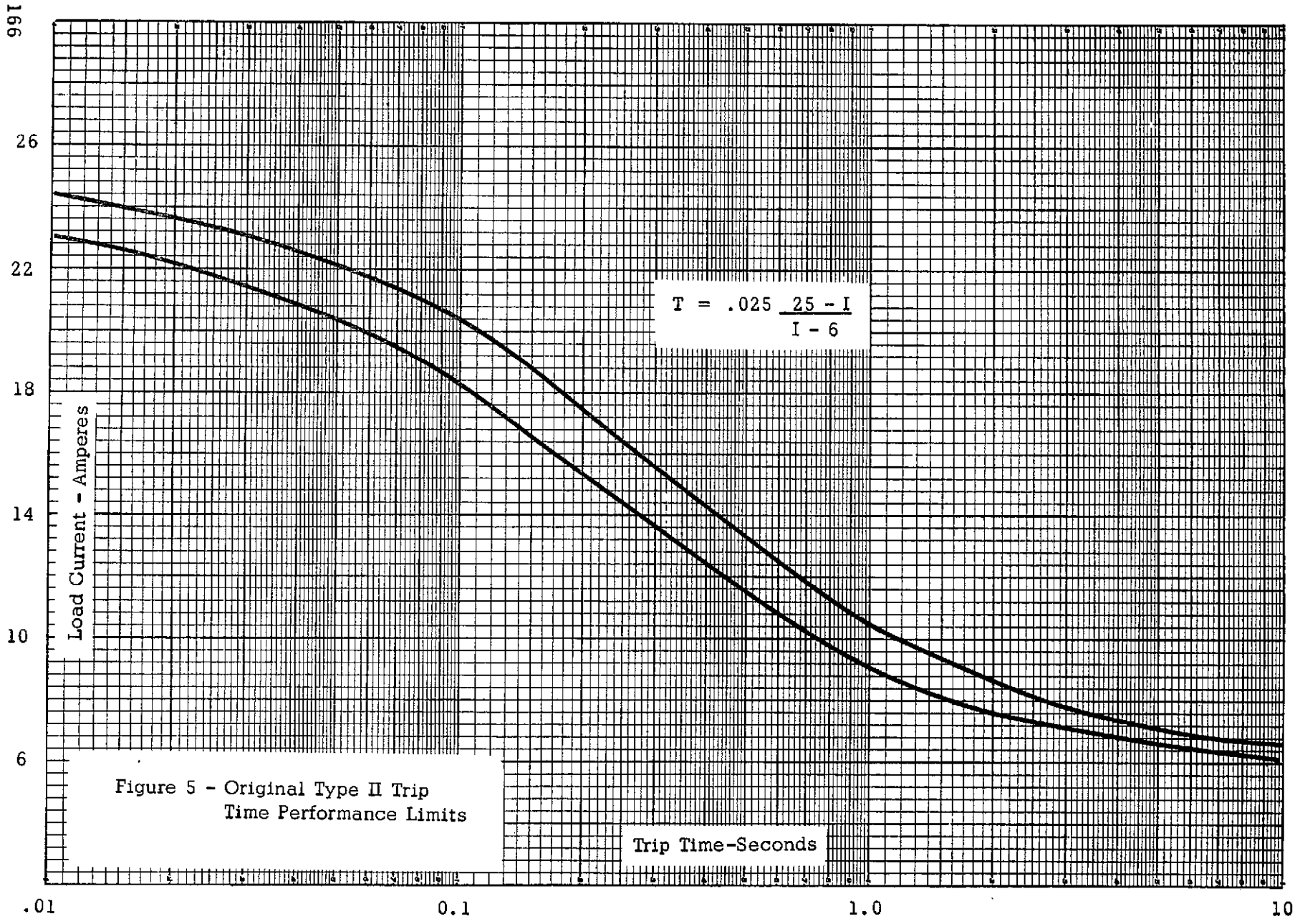


Figure 5 - Original Type II Trip Time Performance Limits

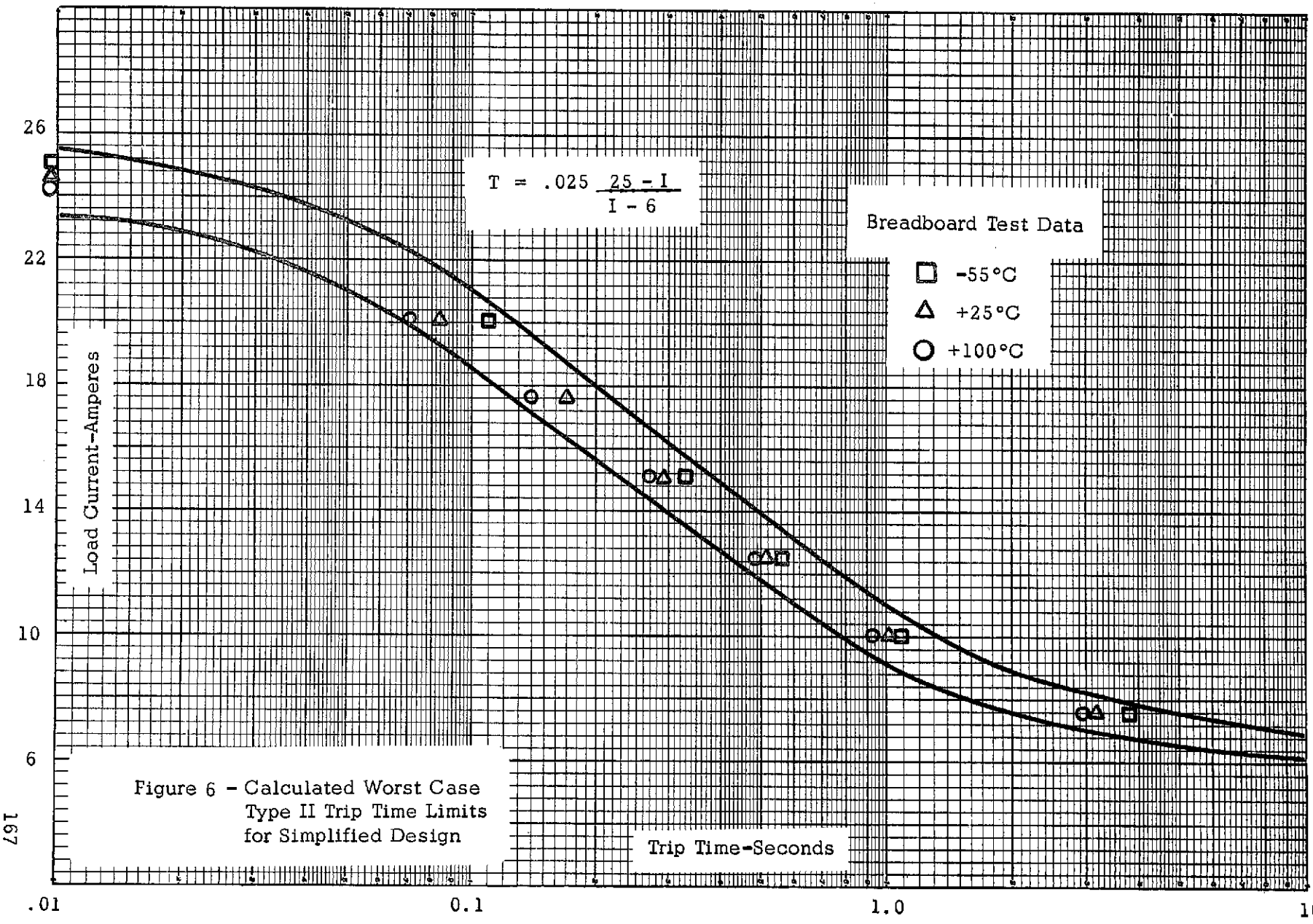


Figure 6 - Calculated Worst Case Type II Trip Time Limits for Simplified Design

PART III

RECOMMENDED SPECIFICATION DEVIATIONS

TO

ACCOMODATE THE SIMPLIFIED DESIGN

SPECIFIC SPECIFICATION DEVIATIONS REQUIRED
FOR THE SIMPLIFIED CIRCUIT DESIGN

NASA SPECIFICATION PARA. NO.	SPECIFICATION DEVIATION/COMMENT
5.1.1	No change.
5.1.2	Change To: The voltage drop across the RPC at rated current and rated supply voltage must be less than 1.5 volts.
5.1.3	No change.
5.1.4	Change To: For all overload currents, $I_L \geq 13.5$ amps, the RPC shall limit the current to 13.5 amps. For overloads which cause the switch voltage drop (V_S) to exceed 108 volts, the RPC shall limit the current to $I_L = .125\ V_S$. The current limit must continue for .1 seconds before interruption.
5.1.5	No change.
5.1.6	No change.
5.1.7	No change.
5.1.8	No change.
5.1.9	Delete entire paragraph.
5.1.10	No change.
5.1.11	No change.
5.1.12	No change.
5.1.13	No change.
5.1.14	No change.
5.2.1	No change.

NASA SPECIFICATION PARA. NO.	SPECIFICATION DEVIATION/COMMENT
5.2.2	Change first sentence to: Shall provide instantaneous ultimate current trips at 25 amperes.
5.2.3	No change.

PART IV

ORIGINAL CONTRACT SPECIFICATIONS

5.0 Specifications for Solid State Switchgear

5.1 An electric remote power controller (RPC) with the following characteristics:

5.1.1 Capable of carrying continuously a dc current, I_o, up to I_o=5A in a load supply line at 120±12 V dc.

5.1.2 The voltage drop across the RPC at rated current must be less than 1.0 volt.

5.1.3 Shall interrupt a current I≥6A within a time interval, t, that corresponds to $(I^2-6^2)t=20$ Amp^2 seconds within ±5%.

5.1.4 For overload currents I≥15A., the RPC shall limit the current to $3.0I_o$ for a time, t, up to 0.1 second before interruption. The current limit value must be constant with respect to all variations of the supply line voltage.

5.1.5 Must be capable of performing all defined protective functions in the presence of voltage transients 50% above (peak value: +200 V dc) and -150% below (peak value: -65 V dc) rated supply voltage for durations up to 50 μsec.

5.1.6 The RPC must be self powered from supply line and capable of manual remote operation, close and open, from low power level signals of magnitude 15 V dc ± 10% and rate of rise greater than 1 Volt/microsecond.

5.1.7 The RPC shall incorporate controlled rate turn on/turn off with output voltage rise and fall times within the range of 10 microseconds to 10 milliseconds determined to minimize EMI.

5.1.8 The RPC shall provide transient and EMI isolation between source and load. All control and power circuits shall be electrically isolated.

5.1.9 The RPC shall provide the option to automatically reset three times with a delay time interval of 1 second between turn off and turn on.

5.1.10 The RPC shall perform all functions within a temperature range of -55°C to 100°C in laboratory air.

5.1.11 The RPC must operate trip free, i.e., automatic circuit interrupt command has priority over close command when power circuit is carrying an overload current.

5.1.12 Power losses shall be minimized both with circuit "open" and "closed." With breaker "open" leakage current shall not exceed 5 mA. The RPC shall provide remote status indications of the "open" and "closed" conditions with minimum power dissipation.

5.1.13 Total weight of RPC shall be minimized.

5.1.14 The RPC shall incorporate fail safe protection. In the event of a failure of the RPC in a shorted condition, the RPC shall fail open within one second when a current $I > 5I_o$ is applied. Fail safe $I^2t = 625$ Amp^2 second.

5.2 An electric remote power controller (RPC) with the following characteristics:

5.2.1 To be capable of performing all the functions and having all the characteristics of the RPC defined under 5.1 above, except 5.1.3 and 5.1.4.

5.2.2 Shall provide instantaneous ultimate current trips at current levels of 15, 20 and 25 A. (Instantaneous in this case is defined as the time interval, $\tau < 1.0$ microsecond, between the time at which the overload current reaches the ultimate trip level and the time at which circuit interruption is initiated.)

5.2.3 Shall interrupt transient overload currents, $I \geq 6$A, but less than the ultimate trip level when the energy proportional to I^2t is within the limits $1 < I^2t < 10$ A^2 sec. Permissable, overload response may approximate the equation $(I^2 - 6^2)\ t = 5$ A^2 sec.