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NR+D

hi-shear CORPORATION / ORDNANCE DIVISION

TORRANCE · CALIFORNIA

FINAL REPORT

ON

THE DESIGN AND DEVELOPMENT

OF A HIGH VOLTAGE POWER SUPPLY

CONTRACT: NAS8-29858

PREPARED FOR

GEORGE C. MARSHALL SPACE FLIGHT CENTER

ALABAMA, 35812

2 DECEMBER 1974

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Approved by: G B Little

G. B. Little, Chief Project Engineer

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SUMMARY OF MONTHLY PROGRESS

AUGUST 1973

The originally proposed circuit designed to meet specification 40M39515B, has been redesigned and upgraded to meet specification 40M3960. Redesign also eliminated some potential problem area in the original design. Component values have been calculated, and most breadboard components have been procured.

SEPTEMBER 1973

The circuit design has been breadboarded and tested. The circuit design and parts list were submitted to NASA at the PDR meeting held at HSC on 27 September 1973. Only one change was made at the PDR, and that was to decrease the sensitivity of the trigger enable input. Since the PDR, the parts list has been revised to meet specification 85MO3936, "EEE Parts Selection Application Guidelines for the Space Shuttle External Tanks and Solid Rocket Booster."

OCTOBER 1974

EBW Firing Unit Circuit Design

Hi-Shear Corporation's design approach is described using as an aid the schematic diagram SK1731. The arm signal is applied to a voltage/current regulator which regulates the voltage and limits the charging current to the DC to DC converter. The DC to DC converter increases the 20 VDC from the regulator to 2300 VDC and charges the energy storage capacitor. Two-three electrode spark gaps are used to switch the energy stored in the capacitor to the EBW load. A monitor circuit, which is a precision voltage divider, monitors the voltage on the capacitor. The three electrode spark gaps are triggered by the trigger circuit when the proper firing signal is

applied to the trigger circuit inputs. The firing signal also turns off the arm input regulator, preventing recharging of the energy storage capacitor after firing.

Regulator - The voltage regulator is a series pass transistor type of regulator. The arm voltage and current is regulated by series transistor Q1. Transistor Q4 amplifies the difference between the regulated output and the temperature compensated reference source VR2. The combination of Q4 and Q2 controls the series pass transistor Q1 in the feedback loop. Current regulation is obtained by VR1 which starts to turn off the series pass transistor Q1 when more than 700 MA is drawn through R2. The regulated output voltage is approximately 20 VDC. The regulator is turned off by trigger signal through CR3 and R6. Transistors Q1 and Q2 have VCEO ratings of 80 volts in order to regulate the voltage transients on the arm signal that can be as high as 50 volts. The regulator and DC to DC converter have been tested over the input voltage and temperature ranges with the total output voltage variations being only 3.6%. This variation easily meets the specification which allows for a total charge voltage variation of 8.7%. The regulator control is taken from the input to the converter rather than the output, which allows for better isolation between input and output circuits.

DC to DC Converter - The DC to DC converter utilizes the conventional push-pull, common emitter, single saturable transformer configuration. This configuration was selected over various single ended half wave converters because it is easier to filter, and it can easily be used with a voltage

doubler circuit. A half wave voltage doubler is used on the output of the converter to reduce the required secondary voltage, and improve overall converter efficiency. Also, since the energy storage capacitor is required for peak holding, the monitor output will be less than 3 volts with the storage capacitor out of the circuit.

Output Circuit - The output circuit uses two three-electrode gaps connected in series with resistor R27 to keep SG1 on until SG2 turns on. Resistors R27 and R28 provide "keep alive" current for the triggered gaps SG1 and SG2 until the safety gap in the EBW Ordnance turns on.

Trigger Circuit - Two trigger storage capacitors (C5 and C6) are used to insure sufficient primary current in each trigger transformer. Transistor Q9 and zener diode VR4 comprise a current regulator which charges the trigger capacitors at a linear rate.

Zener diode VR3 and SCR Q7 form a threshold detection circuit which triggers Q8 when the trigger capacitors reach 18 volts. Q8 dumps the trigger capacitors into the trigger transformers primaries. Diodes CR9 and CR10 comprise a hold off circuit, unless trigger enable is present. After triggering, Q7 holds off current regulator Q9 to keep the trigger current low.

Additional environmental tests have been performed on the firing unit bread-board, and the unit performs correctly. EMI tests have been performed on the firing unit, and the data indicates that filtering will be required on all pins of input connector J1. The line that requires the most filtering is the

power return followed by the power input, the trigger lines, and the monitor line. A filter is now being designed to provide the required attenuation. The high voltage subassembly is now being packaged. It will be encapsulated in epoxy, and it will contain all high voltage components, except for the energy storage capacitor. High voltage terminals on the subassembly are designed to be sealed after wires are soldered to them. A preliminary PW board layout has been made, and it will be finalized after the high voltage subassembly design is completed. The preliminary case design will be finalized after the filter design is complete.

NOVEMBER AND DECEMBER 1973

The circuit has been changed to incorporate ceramic and film capacitors to replace all tantalum capacitors. Tantalum capacitors are not allowed on Space Shuttle in applications where the ambient temperature can be above 70°C. The film capacitors are many times larger than the tantalum capacitors, and this necessitates repackaging the firing unit.

JANUARY 1974

The circuit has been repackaged to incorporate the large film capacitors. The new packaging requires two circuit boards, one for the arm circuit, and one for the trigger circuit. The high voltage subassembly is connected to and placed between the two boards. Further breadboard tests have shown that the film trigger capacitors exhibit superior electrical characteristics to the tantalum capacitors.

FEBRUARY, MARCH, AND APRIL 1974

The drawing package is finished and has been sent to NASA. Joe Burson from MSFC visited Hi-Shear Corporation on February 4, 1974 and reviewed

the drawings. He made several suggestions as to changes that would improve the unit, and HSC will incorporate these changes.

JUNE 1974

The output connector is completely designed and parts procured. The connector consists of 3 parts (body, insulator and pins). The parts will be nickel plated, and then the connector parts and cover will be brazed together at one time. The cable has been designed and fabricated. The electrical parameters of the cable will be calculated and then determined by test. The components for the boards have been procured.

JULY 1974

The cable drawing has been sent to NASA. A shield termination ring was designed and fabricated to terminate the shield of the cable to the RB10-48612-3S connector. (Drawing enclosed). Our first brazing operation on the connector was fair. After inspecting the connector, more silver was needed. More silver was added in the second connector which produced a good brazed surface. In addition, a brazing ring was also designed for the input connector. This will give rigidity to the mounting surface. The power boards have been completed. One set of boards is under test.

AUGUST, SEPTEMBER, AND OCTOBER 1974

All EMI filters have been received. The breadboard converter transformer was tested within the H.V. subassembly. The results indicated that a more efficient transformer was needed because the idle current of the complete power supply at hot temperature (93^{o}C) exceeded the specification of 250 ma. After careful consideration, a ferite core transformer was selected. This ferite transformer performed very well under test. The arm current was

well within specifications. Further problems did occur at cold temperature (-54°C). High frequency oscillations and slow charge time occurred at cold. After a complete analysis on the charging circuit, the following solutions were selected to solve the above problems.

a. Decrease surge resistor R2

b. Increase base emitter resistors R13 and 14

c. Decrease R1 and R2 in the H.V. assembly

The above solutions were tested and proven good at both cold and hot temperatures. A revised schematic and parts list will be sent to NASA as soon as the drawings are changed. The H.V. subassemblies have been tested. They are now being potted.

NOVEMBER 1974

Units S/N 101 and 102 were assembled and tested per NASA specification 40M39640. The test data is recorded in Appendix A. The cable was tested with a HSC .01027Ω load. The test data is recoreded in Appendix B.

APPENDIX A

SPECIFICATION PARAGRAPH	INPUT PARAMETERS	-54°C	AMB.	+93°C
3.4.4.1 DC-DC Converter Characteristics - The systems shall operate within requirements on 24 to 32 Vdc delivered through an internal resistance of less than 1 ohm. It shall be referred to as 28 Vdc throughout this specification. The converter or any part of the firing system shall not be damaged by the application of an input signal of any amplitude between 0 and 36 volts or application of a 50-volt, 10 microsecond input pulse.	24V	OK	OK	OK
	32V	OK	OK	OK
	0 - 36	OK	OK	OK
	50V at 10 MSEC	OK	OK	OK
3.4.4.2 DC-DC Converter Output Voltage - The DC-DC converter output voltage supplied to the storage unit shall be 2300 ± 100 Vdc with a peak-to-peak ripple of not greater than 200 volts.		$V_{MONITOR}$	$V_{MONITOR}$	$V_{MONITOR}$
	24V	4.585	4.750	4.790
	36V	4.888	4.758	4.828
3.4.4.2.1 Charging Current - The charging current over the 24 to 36 Vdc input range shall not exceed (TBD) amperes peak and shall decay to a maximum average "idle" current of 0.25 ampere within 1.0 seconds.		I_{ss}	I_{ss}	I_{ss}
	36V	149 ma	170 ma	230 ma

S/N 101

SPECIFICATION PARAGRAPH	INPUT PARAMETERS	-54°C	AMB	+93°C
3.4.4.3 Storage Capacitor - The storage capacitor shall be capable of charging 2200 volts in not more than 1.0 seconds after input power is applied to the DC-DC converter.	24V	.8 sec	.6 sec	.4 sec
3.4.4.3.1 Bleed Circuit - A bleed circuit shall be provided that will allow the stored voltage to decay to 300 volts and monitor voltage to 0.6 volts within 15 seconds after removal of input power. The bleed circuit shall provide redundant bleed paths so that a single failure will not cause complete loss of the bleed circuit. Either bleed circuit shall allow the stored voltage to decay to 300 volts within 90 seconds after removal of input power.	36V	11 sec	12 sec	12.5sec
3.4.4.4.1 Trigger Circuit Initiate - No storage elements in the trigger circuit shall be activated until application of a 28 ± 4 Vdc trigger signal. Input impedance shall be less than 10 K ohms and shall provide protection against negative transients of -50 Vdc with 10 microsecond durations. Positive transients of 50 Vdc and 10 microsecond durations shall not damage or trigger the system. Firing of the system shall occur within 4 ± 1 milliseconds after application of the trigger signal.	24V	4.0MS	4.2MS	4.5MS
	32V	3.5MS	3.7MS	4.0MS
	50V at 10 MSEC	OK	OK	OK

S/N 101

SPECIFICATION PARAGRAPH	INPUT PARAMETERS	-54°C	AMB	+93°C
3.4.4.4.2 Trigger Circuit Enable - A 28 ± 4 Vdc trigger enable signal shall be required prior to the trigger initiate signal to fire the unit unless pins J1B and J1C are externally connected, in which case, a single 28 ± 4 Vdc signal applied to either J1B or J1C will fire the system.	24	OK	OK	OK
	32	OK	OK	OK
3.4.4.4.3 Trigger Circuit Sensitivity - The trigger circuit shall require a peak input current of not less than 110 ma and not more than 250 ma to operate. Steady sate average trigger circuit input current after operation shall not exceed 75 ma. The trigger circuit shall not operate when subjected to an 8 Vdc input signal or an input transient pulse of 50 volts amplitude and 10 microsecond duration. Note: This applies to the trigger circuit initiate and trigger circuit enable.		I_{peak}	I_{peak}	I_{peak}
	32V (Enable)	140 ma	150 ma	160 ma
	32V (Initiate)	150 ma	150 ma	160 ma
		I_{ss}	I_{ss}	I_{ss}
	32(Enable)	19.6 ma	20 ma	20ma
	32(Initiate)	21ma	21ma	21ma

SPECIFICATION PARAGRAPH	INPUT PARAMETERS	-54°C	AMB.	+93°C
3.4.4.4.5 DC-DC Converter Cut-off - Application of the trigger signals shall activate a DC-DC converter turn-off circuit which prevents recharging of the storage unit. Input current to the converter shall not exceed 50 milliamperes after cut-off.	32V($I_{converter}$)	24ma	24ma	25ma
3.4.4.6 Firing unit status monitoring - The firing unit shall be provided with a monitoring circuit which will indicate the voltage to which the storage unit is charged. The monitor circuit impedance shall be 10K ohms ± 1.0%. The monitor voltage shall be 4.6 ± 0.3 volts under normal operating conditions. Monitor voltage rise time to 4.3 volts shall be less than 1.0 seconds. Maximum peak-to-peak monitor voltage variation shall not exceed 0.41V. The monitor shall be capable of determining that the storage unit discharged through the switching device. Nominal sensitivity shall be 500 volts per volt under open circuit conditions.	24(V_{mon})	4.585v	4.750V	4.790V
	36(V_{mon})	4.588v	4.758V	4.828V
	24 (Time)	.8sec	.6sec	.4sec
	36 (Ripple)	.05V_{pp}	.06V_{pp}	.06Vpp

SPECIFICATION PARAGRAPH	INPUT PARAMETERS	-54°C	AMB.	+93°C
3.4.4.1 DC-DC Converter Characteristics - The systems shall operate within requirements on 24 to 32 Vdc delivered through an internal resistance of less than 1 ohm. It shall be referred to as 28 Vdc throughout this specification. The converter or any part of the firing system shall not be damaged by the application of an input signal of any amplitude between 0 and 36 volts or application of a 50-volt, 10 microsecond input pulse.	24V	OK	OK	OK
	32V	OK	OK	OK
	0 - 36	OK	OK	OK
	50V at 10 MSEC	OK	OK	OK
3.4.4.2 DC-DC Converter Output Voltage - The DC-DC converter output voltage supplied to the storage unit shall be 2300 ± 100 Vdc with a peak-to-peak ripple of not greater than 200 volts.		$V_{MONITOR}$	$V_{MONITOR}$	$V_{MONITOR}$
	24V	4.516	4.709	4.729
	36V	4.522	4.716	4.750
3.4.4.2.1 Charging Current - The charging current over the 24 to 36 Vdc input range shall not exceed (TBD) amperes peak and shall decay to a maximum average "idle" current of 0.25 ampere within 1.0 seconds.		I_{ss}	I_{ss}	I_{ss}
	36V	140 ma	168 ma	237 ma

SPECIFICATION PARAGRAPH	INPUT PARAMETERS	-54°C	AMB	+93°C
3.4.4.3 Storage Capacitor - The storage capacitor shall be capable of charging 2200 volts in not more than 1.0 seconds after input power is applied to the DC-DC converter.	24V	.9 sec	.6 sec	.35 sec
3.4.4.3.1 Bleed Circuit - A bleed circuit shall be provided that will allow the stored voltage to decay to 300 volts and monitor voltage to 0.6 volts within 15 seconds after removal of input power. The bleed circuit shall provide redundant bleed paths so that a single failure will not cause complete loss of the bleed circuit. Either bleed circuit shall allow the stored voltage to decay to 300 volts within 90 seconds after removal of input power.	36V	10 sec	11 sec	12 sec
3.4.4.4.1 Trigger Circuit Initiate - No storage elements in the trigger circuit shall be activated until application of a 28 ± 4 Vdc trigger signal. Input impedance shall be less than 10 K ohms and shall provide protection against negative transients of -50 Vdc with 10 microsecond durations. Positive transients of 50 Vdc and 10 microsecond durations shall not damage or trigger the system. Firing of the system shall occur within 4 ± 1 milliseconds after application of the trigger signal.	24V	4.3 MS	4.4MS	4.5 MS
	32V	3.5 MS	3.6 MS	3.7MS
	50V at 10 MSEC	OK	OK	OK

SPECIFICATION PARAGRAPH	INPUT PARAMETERS	-54°C	AMB	+93°C
3.4.4.4.2 Trigger Circuit Enable - A 28 ± 4 Vdc trigger enable signal shall be required prior to the trigger initiate signal to fire the unit unless pins J1B and J1C are externally connected, in which case, a single 28 ± 4 Vdc signal applied to either J1B or J1C will fire the system.	24	OK	OK	OK
	32	OK	OK	OK
3.4.4.4.3 Trigger Circuit Sensitivity - The trigger circuit shall require a peak input current of not less than 110 ma and not more than 250 ma to operate. Steady sate average trigger circuit input current after operation shall not exceed 75 ma. The trigger circuit shall not operate when subjected to an 8 Vdc input signal or an input transient pulse of 50 volts amplitude and 10 microsecond duration. Note: This applies to the trigger circuit initiate and trigger circuit enable.		I_{Peak}	I_{Peak}	I_{Peak}
	32V(Enable)	160 ma	175 ma	180 ma
	32V(Initiate)	150 ma	157 ma	160 ma
		I_{ss}	I_{ss}	I_{ss}
	32(Enable)	20.5 ma	21 ma	21 ma
	32(Initiate)	21 ma	21 ma	21 ma

SPECIFICATION PARAGRAPH	INPUT PARAMETERS	-54°C	AMB.	+93°C
3.4.4.4.5 DC-DC Converter Cut-off - Application of the trigger signals shall activate a DC-DC converter turn-off circuit which prevents recharging of the storage unit. Input current to the converter shall not exceed 50 milliamperes after cut-off.	32V ($I_{Converter}$)	25ma	25ma	25ma
3.4.4.6 Firing unit status monitoring - The firing unit shall be provided with a monitoring circuit which will indicate the voltage to which the storage unit is charged. The monitor circuit impedance shall be 10K ohms ± 1.0%. The monitor voltage shall be 4.6 ± 0.3 volts under normal operating conditions. Monitor voltage rise time to 4.3 volts shall be less than 1.0 seconds. Maximum peak-to-peak monitor voltage variation shall not exceed 0.41V. The monitor shall be capable of determining that the storage unit discharged through the switching device. Nominal sensitivity shall be 500 volts per volt under open circuit conditions.	24 (V_{Mon})	4.516V	4.709V	4.729V
	36 (V_{Mon})	4.522V	4.716V	4.750V
	24 (Time)	.9sec	.6sec	.35sec
	36 (Ripple)	.02V_{pp}	.02V_{pp}	.025V_{pp}

APPENDIX B

SHORT CABLE

Using the HSC .01027 OHM load the time to peak and peak current is .904 microsecond and 3017 amperes.

COMPUTER ANALYSIS

```
RUN
VALUE OF T1,T2,I1,I2,C

?2.1E-6,4.1E-6,29,18,1E-6

RESISTANCE      INDUCTANCE      FREQUENCY
 0.188935800     3.96155E-07     250000.0000




SCRATCH
LOAD0
RUN
VALUE OF R,V,L,C

?.1889358,2356,3.96155E-7,1E-6
TIME TO PEAK    PEAK CURRENT
 9.04087E-07     3017.261583
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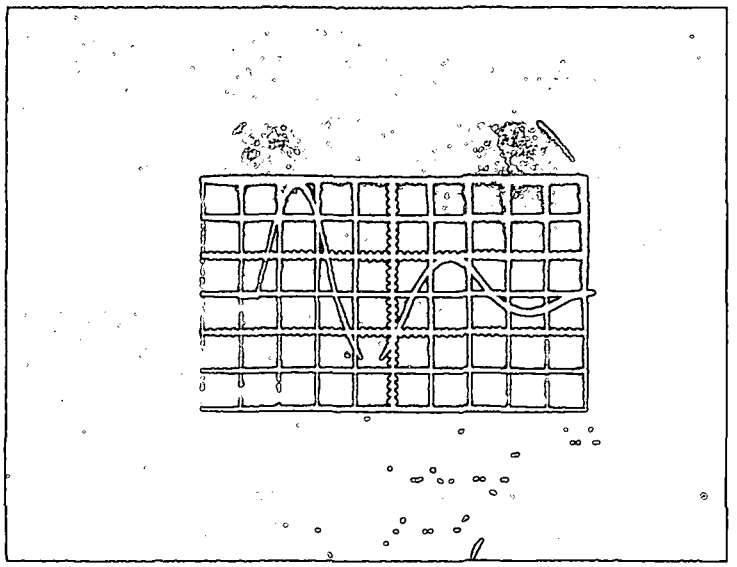
PHOTO

10V/DIV

1 MICROSEC/DIV

V = 2356



SHORT CABLE

Using the HSC .01027 OHM load the time to peak and peak current is .904 microsecond and 3017 amperes.

COMPUTER ANALYSIS

```
RUN
VALUE OF T1,T2,I1,I2,C

?2.1E-6,4.1E-6,29,18,1E-6

RESISTANCE      INDUCTANCE      FREQUENCY
 0.188935800     3.96155E-07     250000.0000
```

```
SCRATCH
LOAD0
RUN
VALUE OF R,V,L,C

?.1889358,2356,3.96155E-7,1E-6
TIME TO PEAK    PEAK CURRENT
 9.04087E-07     3017.261583
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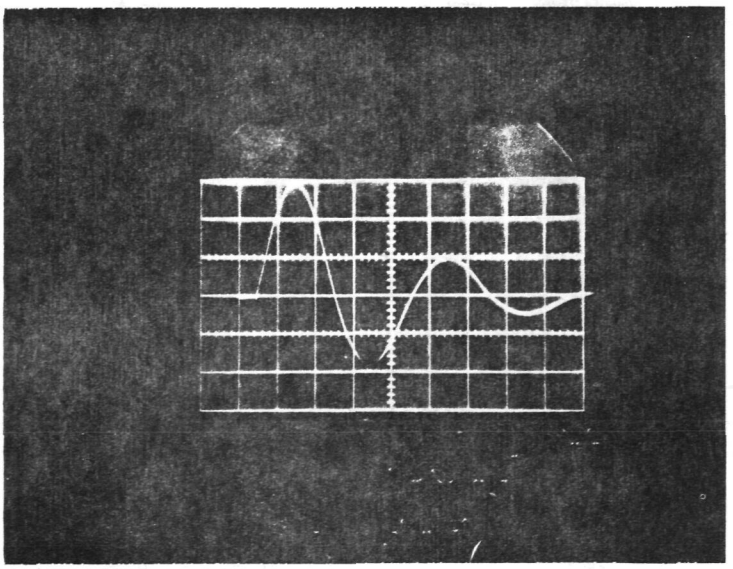
PHOTO

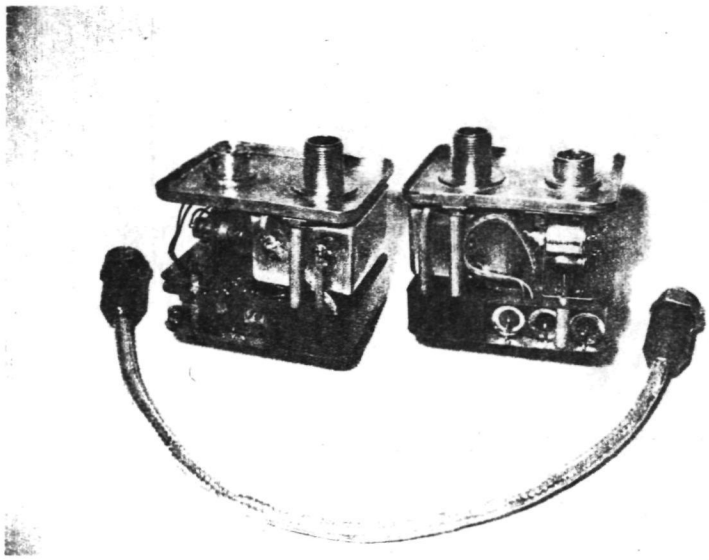
10V/DIV

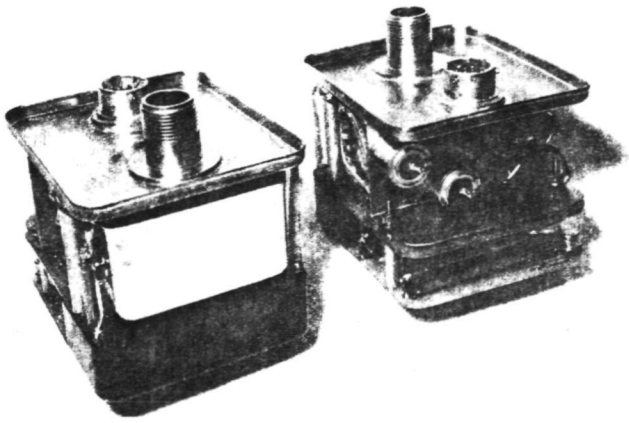
1 MICROSEC/DIV

V = 2356



APPENDIX C





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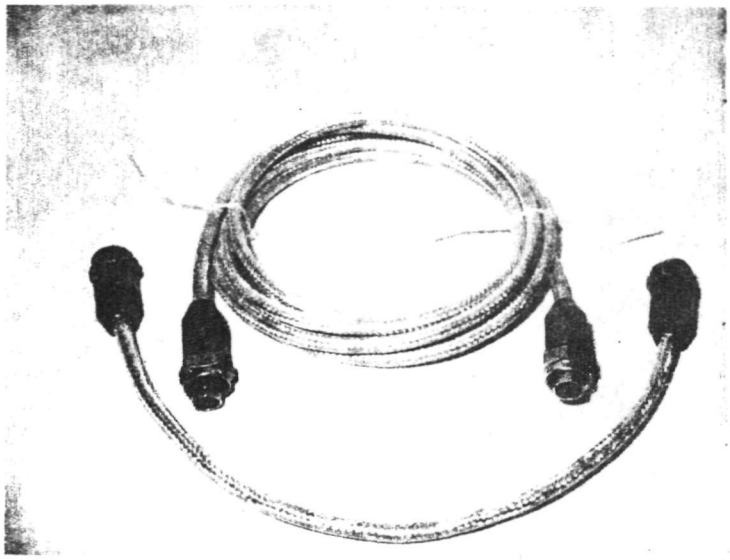

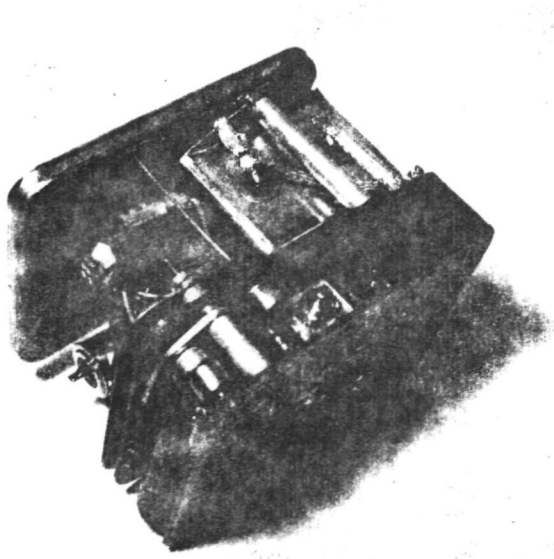

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