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SEQUENTIAL COLOR VIDEO TO PARALLEL COLOR VIDEO CONVERTER

Final Report

Contract Number NAS-9-13781

Prepared for:

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Lyndon B. Johnson Space Center
Houston, Texas 77058

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Contract Number   NAS-9-13781
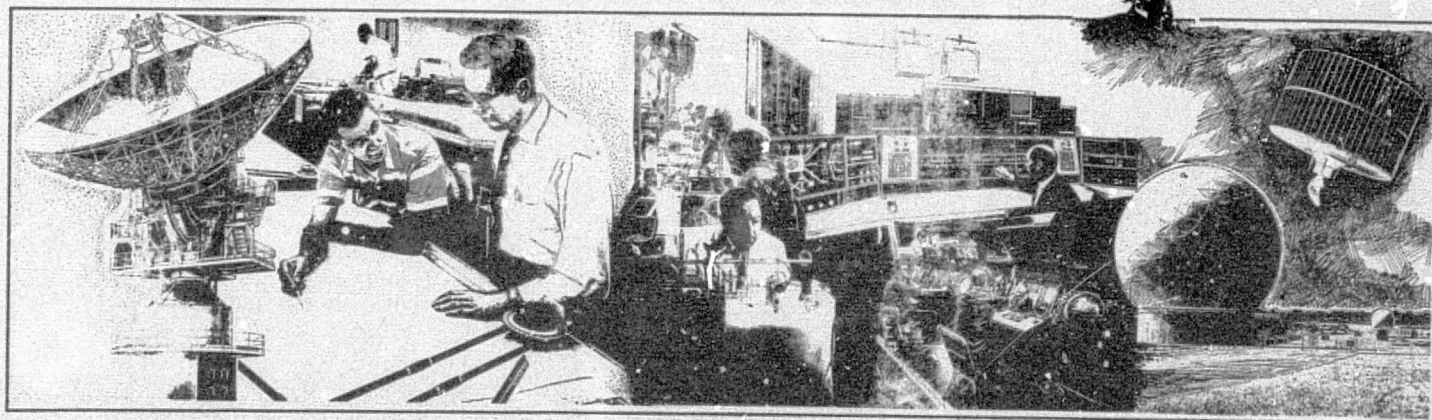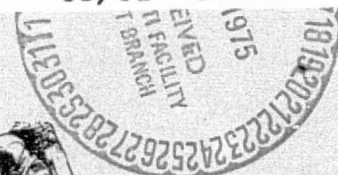
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TABLE OF CONTENTS

1.0   INTRODUCTION

This document is the final report on the serial to parallel converter contract. The object of this report is to summarize the results of the entire contract effort and to present recommendations and conclusions based on the experience and results obtained. The object of the project was to perform the engineering design, development, breadboard fabrication, test and delivery of a breadboard field sequential color video to parallel color video converter.

The background of the project is of interest and is excerpted from the project request for proposal."

"At this time, the optimum color TV camera to use onboard a manned space vehicle in terms of operational stability and ease of operation, weight, power, volume, etc., is the field-sequential color system. The present type of field-sequential color TV system (FSCTV) utilizes standard scanning rates (60 fields/second. This rate has been chosen in order to be as compatible as possible with the United States commercial networks. It also allows extensive use of commercially available television equipment for video processing and display. This low color update rate, however, results in a TV display that flickers when viewed on a monitor. This flickering picture is undesirable because of the eye strain and psychological fatigue it causes the observer. To eliminate this flicker, the field-sequential color signal must be converted to a parallel format. That is, each individual primary color must be segregated from the field-sequential signal and its update rate increased enough to eliminate the flicker. The Apollo/Skylab color TV systems eliminates the flicker on the ground by using a conversion system which utilizes a heavy and bulky disk recorder. This ground system is impractical to package for flight and, therefore, the development of a flight type color converter is required for a closed-circuit TV system to be used in a spacecraft. The Figure A block diagram describes an overall functional approach. The contractor is encouraged to minimize the amount of field storage over that shown. Because the device may be used on spacecrafts, the contractors are encouraged to minimize the power, weight, and volume of the device."

The Western Development Laboratories of Aeronutronic-Ford achieved the objectives of the project and delivered a complete converter breadboard that met or exceeded all of the specifications.

Figure 1-1 is a simplified block diagram of the STP converter. Field sequential color is generated by a monochrome video camera with a spinning 3 color wheel that filters the input scene luminance with a different color each TV field. The camera also generates a composite sync segnal and a signal identifying the phase of the color wheel (green field). The camera signal enters the STP Color Converter where they are converted into a NTSC compatible color signal such as would be generated by a conventional 3 tube NTSC color camera. The NTSC video signal from the converter is used by a conventional NTSC color monitor to display a flicker free color image of the input scanner.

Figure 1-2 is a block diagram of the STP converter that was developed and delivered during the project. The A/D converter is a 3-bit delta modulator which will be discussed in detail during this report. The compatible D/A converters are 3-bit delta demodulators. The video storage delays were implemented using PMOS shift registers as will also be discussed in this report. The timing on sync circuitry generates NTSC compatible synchronization which is combined with the output parallel video signals and provide timing and control signals to permit the data selector to gate the signals from the A/D converter or one of the two field memories into the proper D/A converter. The outputs of the 3 D/A converters consist of parallel NTSC video with composite sync and blanking inserted.

This report consists of a specification summary followed by a discussion of a number of system tradeoffs that led to selection of the delivered system configuration. After the system tradeoff, a

3 COLOR WHEEL

```
                VIDEO                        STP                      NTSC
VIDEO    ──────────────▷              NTSC    COLOR
CAMERA          SYNC     ──────────▷  COLOR   VIDEO  ──────────▷      COLOR
                GREEN                 CONVERTOR                       MONITOR
                FIELD    ──────────▷
```
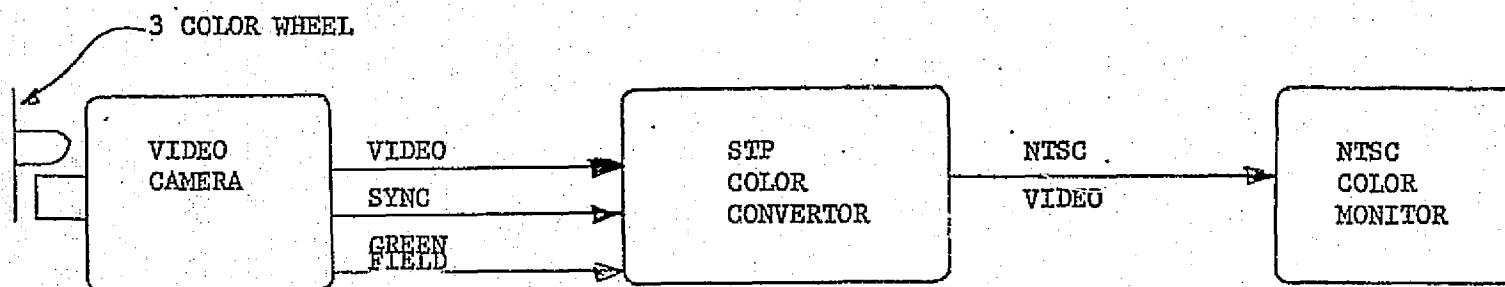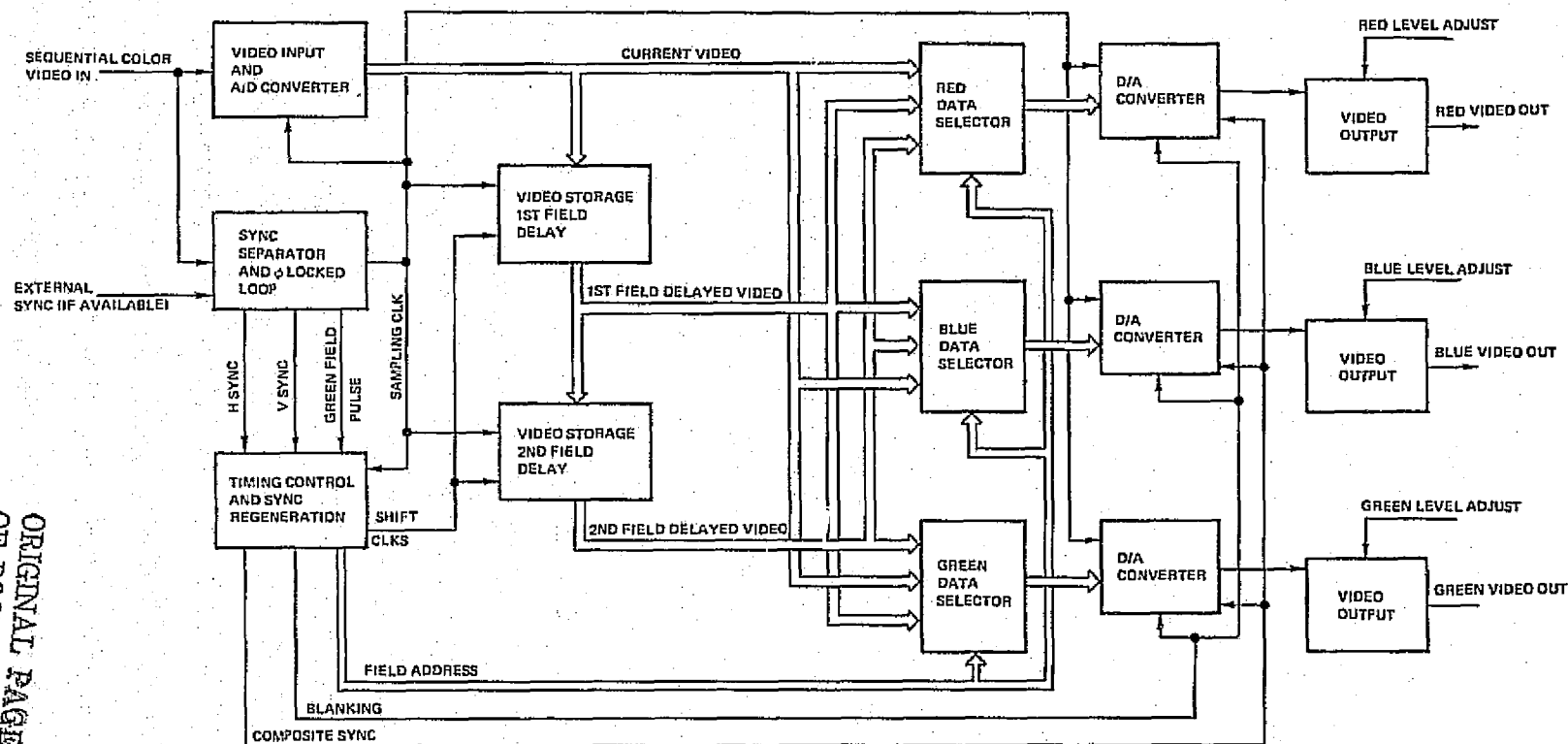
FIGURE 1-1

FIGURE 1-2

Sequential-to-Parallel Color Video Converter Block Diagram

description and discussion of the delta modulator/demodulator, the memory, and the format control and synchronization follows. Following the hardware discussions, a summary of the reliability analyses and packaging study related to a spacecraft packaged version of the STP converter is presented.

Finally, performance results measured with breadboard STP converter are presented followed by recommendations and conclusions based upon the results of the contract effort.

Table 2-1 is a summary of the key specification of the
STP Converter. Several of the key specifications such as
field to field gain stability, channel to channel gain and
response represent areas of major performance difficulty
in conventional analog designs (particularly those utilizing
moving part memories). The selected digital approach with
a non-moving solid state memory inherently eliminates these
problems due to its basic system architecture. The use of
digital memories and precision stable D/A Converters reduces
the field to field and channel to channel gain stabilities
to less than $\pm$ 1/2 of a least significant bit of the D/A
Converters which results in virtual elimination of flicker
and color fidelity problems associated with conventional
analog designs. Moving part memories (discs and drums) have
inherent line to line pixel alignment and filter problems
which cause a response reduction caused by channel to channel
registration. The use of a solid state digital memories
and crystal oscillator controlled timing reduces this source
of error to the limit of the short term stability of the crystal
timing clock. This error which can be a significant problem
in rotating part memories for the STP Converter becomes many
orders of magnitude less than an acceptable limit.

TABLE 2-1

S T P   C O N V E R T E R

SPECIFICATION SUMMARY

KEY SPECIFICATIONS

o	FIELD TO FIELD GAIN STABILITY	~ 5%
o	LUMINANCE RESOLUTION	~ 10 SHADES OF GRAY
o	CHANNEL TO CHANNEL GAIN	~ 0.5 IRE UNITS
o	RESOLUTION	~ 440 TV LINES
o	RESPONSE	~ 440 LINES MTF IS 50% OF 220 LINE MTF
o	BANDWIDTH	~ 4.2 MHz
o	NOISE	~ $\frac{\text{PP VIDEO}}{\text{RMS NOISE}}$ 45 db (equivalent to 6 Bit PCM)

2.0   SPECIFICATION SUMMARY (continued)

Table 2-1 list the principal specification. Several additional specifications are of interest and are required to permit functional interface of the STP Converter with its associated equipments. The following paragraphs contain the detailed specifications imposed on the converter.

2.1   Design Specifications

2.1.1   Conversion Design Requirements

In performing the conversion process, the converter first separates the individual primary colors (see Figures A and B) from the field-sequential color signal. The color field in each separated signal is then delayed (or stored) for one field period and then reinserted into the individual video signal. The same field is then delayed (or stored) for a second field period and then again inserted into the individual video signal. The three parallel video output signals thus contain video data in every output field. With proper matching of the output fields, flicker is eliminated and output distortion is kept minimum. If a solid state analog (using a mosiac type device) technique is utilized for storage of the video fields, the A/D and D/A converters shown on the diagram (Figure A) may not be required.

2.1.2   Video Storage Device

The STP color converter shall use a solid state storage device or devices including digital type components or solid state image sensors which can retain an image for the stated purpose. The converter shall not use any type of electron tube or mechanical delay line (such as glass or quartz) for storage of the video signal.

2.1.3   Power Supply

The STP converter shall be capable of operating from a 110 V power supply.

COMPOSITE FIELD - SEQUENTIAL
COLOR VIDEO SIGNAL

ORIGINAL PAGE IS
OF POOR QUALITY
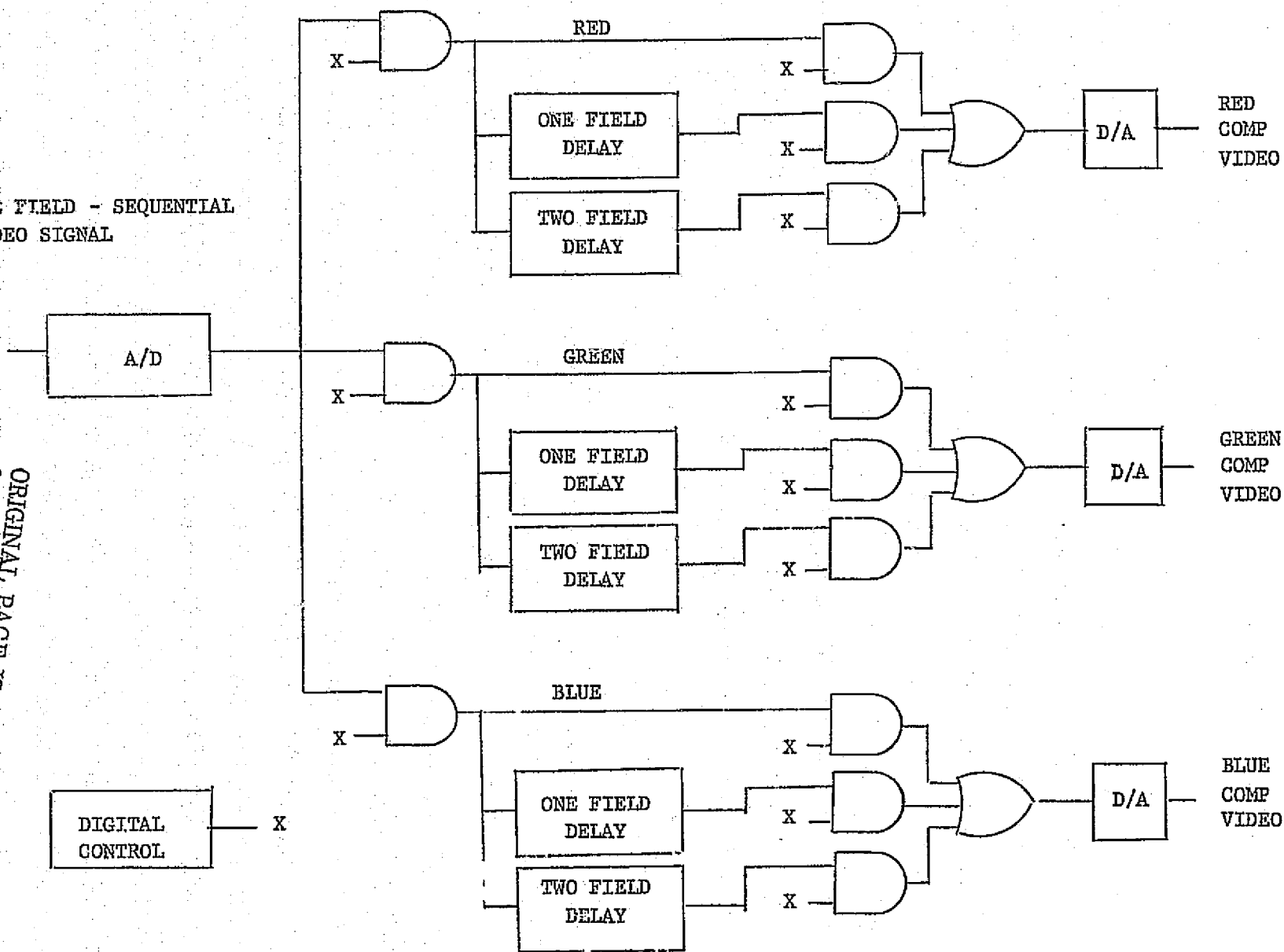
FIGURE A

STP FUNCTIONAL DIAGRAM
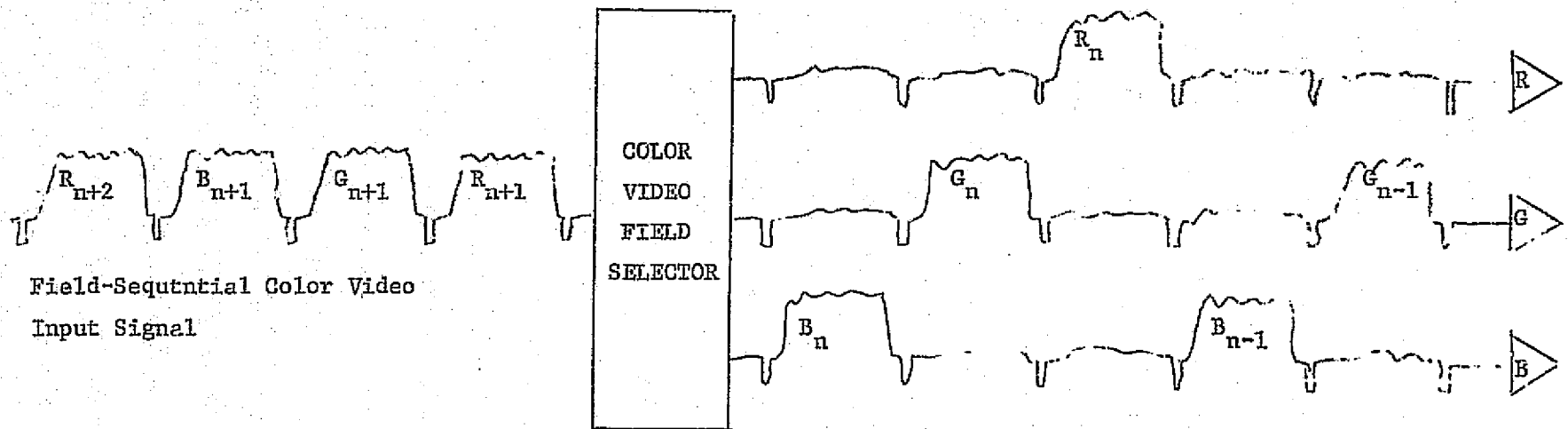
Field-Sequntial Color Video
Input Signal

COLOR VIDEO FIELD SELECTOR

R_{n+2} B_{n+1} G_{n+1} R_{n+1}

R_n R
G_n G_{n-1} G
B_n B_{n-1} B

DELAY (STORAGE) AND RESAMPLE

R_{n-1}
G_{n-2}
B_{n-2}

R_{n-2} R''_{n-3} R'_{n-3} R_{n-3} R''_{n-4} R'_{n-4}

G''_{n-3} G'_{n-3} G_{n-3} G''_{n-4} G'_{n-4} G_{n-4}

B'_{n-3} B_{n-3} B''_{n-4} B'_{n-4} B_{n-4} B''_{n-5}
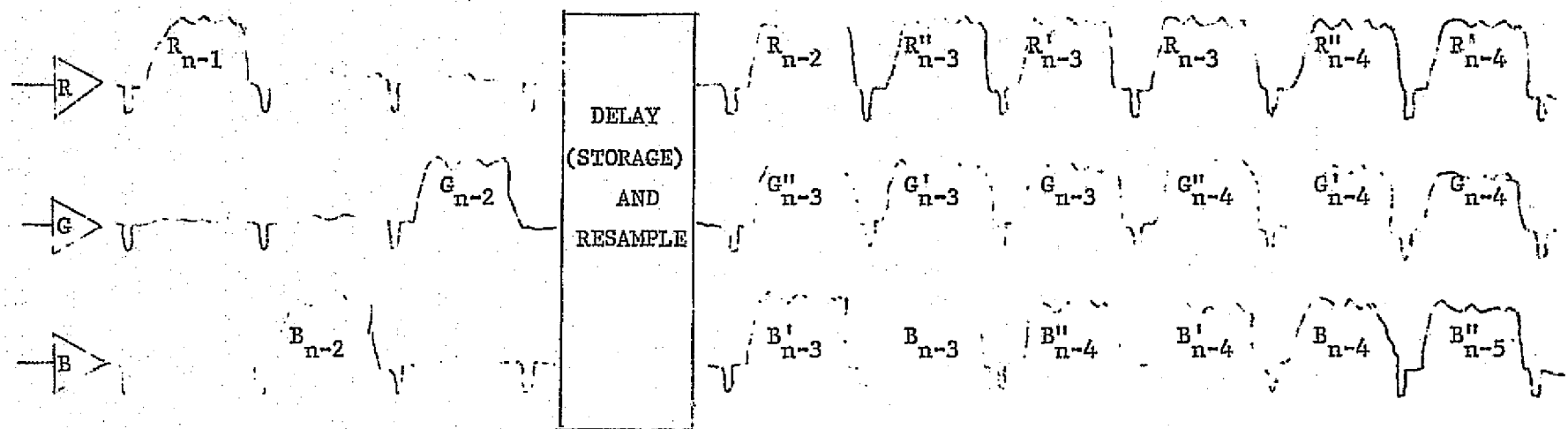
NOTE: R'_n indicates red field R_n delayed for one field period.
       R''_n indicates red field R_n delayed for two field periods.

2.1.4   Video Input Signal

The composite video input signal (field-sequential color
video) to the STP converter shall conform to NTSC color tele-
vision standards as currently utilized by the commercial net-
works in the United States with respect to vertical and hori-
zontal scanning rates, synchronizing pulses, interlace ratio,
lines per frame, fields per second, and aspect ratio.

The voltage of the composite video signal shall be nominally
1.0 volt (0.714 volts from blanking to reference white and
0.286 volts from blanking to sync pulse amplitude) when termin-
ated in 75 ohms.

2.1.5   Video Input Impedance

The video input impedance shall have a value of 75 ohms
($\pm$5%).

2.1.6   Video Output Signal

The red, green, and blue composite video output signals from
the STP converter shall conform to NTSC color television standards
as currently utilized by the commercial networks in the United
States with respect to vertical and horizontal scanning rates,
synchronization pulses, interlace ratio, lines per frame, fields
per second, and aspect ratio.

The voltage of the composite video signals shall be nominally
1.0 volt (0.714 volts from blanking to reference white and 0.286
volts from blanking to sync pulse amplitude) when terminated in
75 ohms.

2.1.7   Field-To-Field Gain Stability

For the total range of required resolution, the amplitude of
each element of each output field as measured at the analog output
of the converter shall be matched to within 5% of the respective
element of the input field as measured at the analog input (field-
sequential signal) of the converter. The object of this require-
ment is to insure that no discernable flicker occurs in the video
output.

2.1.8 Luminance Resolution (Gray Shades)

Each channel of the converter shall be capable of resolving a minimum of 10 luminance levels (gray shades) equally spaced from the black level to the peak white level.

2.1.9 Channel-To-Channel Gain

For the total range of luminance resolution (gray shades) and using a monochrome gray shade input signal, each channel shall be adjustable so that output levels are within 3.5 mv (0.5 IRE units) of each other. Once adjusted (and without changing the input signal) the converter shall maintain this output level tolerance for a minimum period of 10 hours without readjustment (see Figure C).

2.1.10 Channel-To-Channel Registration

The object of this requirement is to insure that the uncertainty of matching elements (fields) from channel-to-channel will not cause a degradation of the resolution of an input signal having a low S/N. The time variation (including jetter) of an element in each output signal field (a field from each channel) shall be such that 440 TV lines can be resolved with a response not less than 50% of the response of 200 TV lines. Conformance with this requirement shall be demonstrated using a monochrome input. Resolution shall be determined from a monitor display and response shall be measured from a waveform monitor presentation (see Figure D).

2.1.11 Resolution

The converter shall be capable of converting a video signal having a vertical resolution of 330 TV lines/raster height and a horizontal resolution of 440 TV lines/raster width. The converter shall not cause any degradation of this resolution. Each active line of video shall be processed.

CHANNEL-TO-CHANNEL GAIN & LUMINANCE RESOLUTION (GRAY SHADES)

Each channel shall be capable of resolving
a minimum of 10 luminance levels (gray
shades) equally spaced from black level
to peak white.

PEAK WHITE

Each channel must be adjustable so
that output levels are within 3.5
(0.5 IRE units) of each other.

BLACK

RED CHANNEL   GREEN CHANNEL   BLUE CHANNEL
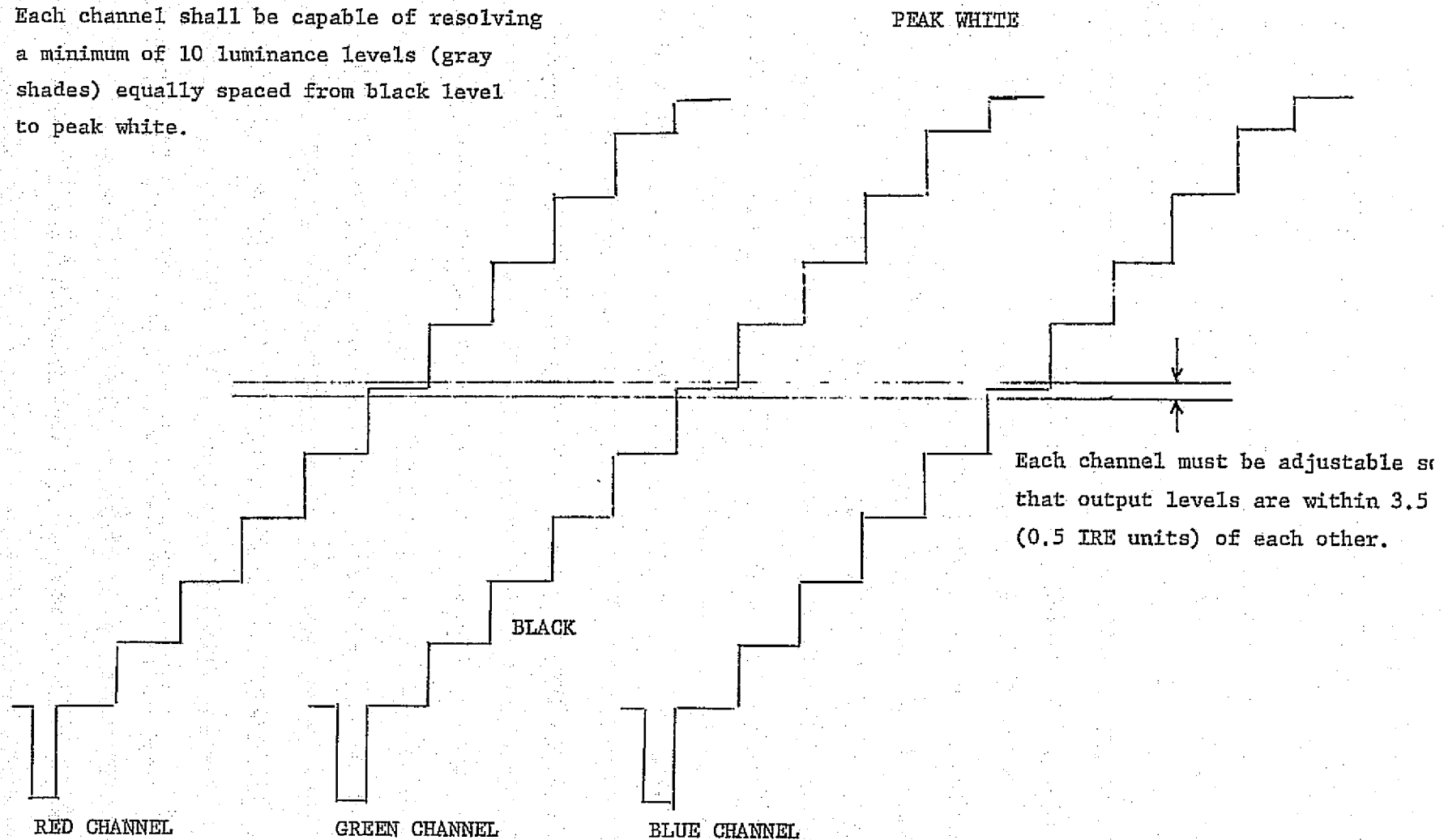
FIGURE C

CHANNEL-TO-CHANNEL REGISTRATION

Red Channel Output

(Field R_n Line xxx)

Green Channel Output

(Field G_n Line xxx)

Blue Channel Output

(Field B_{n-1} Line xxx)
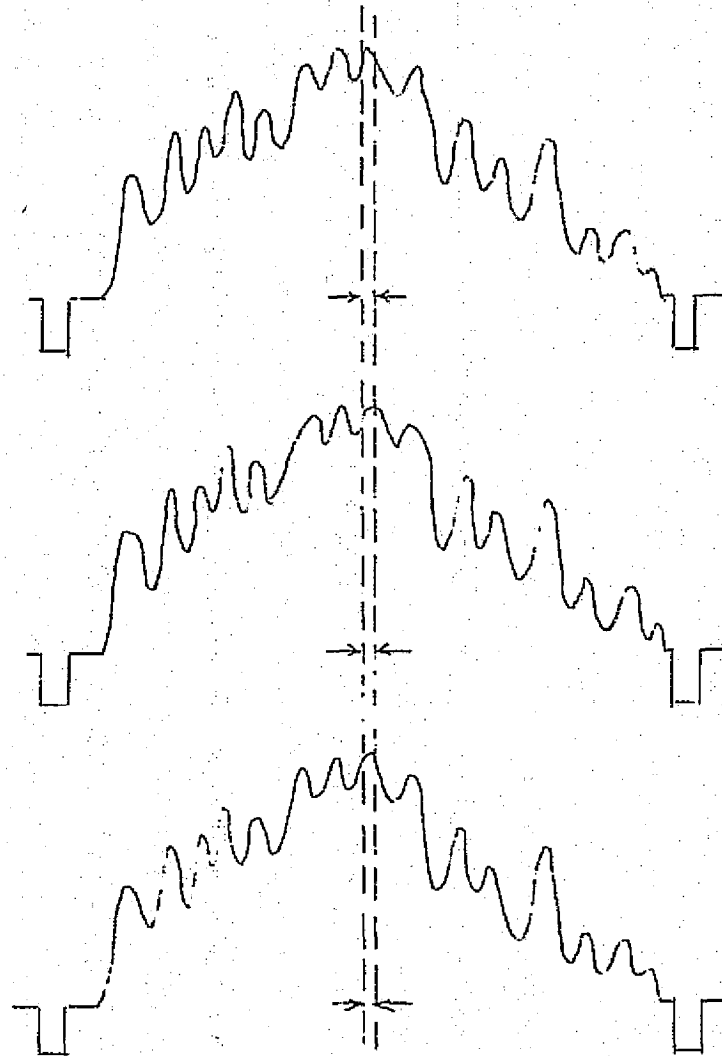
The time variation (including jitter) of an element in each output signal field (a field from each channel) shall be such that 440 TV lines can be resolved with a response not less than 50% of the response of 200 TV Lines.

FIGURE D

2.1.12   Signal-To-Noise Ratio

Assuming an input signal of +60 db, the final analog output signal shall have an S/N not less than +45 db with the S/N defined as follows:

$$S/N = 20 \log_{10} \frac{\text{peak video signal (0.714 volts)}}{\text{rms noise voltage}}$$

where rms noise voltage may be defined as peak-to-peak noise voltage divided by six.

In no case shall any coherent noise be evident in the video output signal.

2.1.13   Test Signal Requirements For Government Acceptance

The converter (or portion thereof) shall be tested to determine conformance with design specifications and requirements by using standard test signals supplied by commercially available television test equipment.

2.1.14   Minimization Of Color Storage

The resolution specified shall apply to the composite color/luminance picture and shall not necessarily imply that each color video signal must meet the stated resolution. Hence, the contractor is encouraged to investigate techniques of minimizing the storage requirements for the individual primary colors based upon the capability of the human eye to discriminate each color. Additional storage reduction may be achieved by utilizing one of the digital redundancy removal techniques such as predictors, interpolators, statistical encoders, delta modulators, etc. in conjunction with the above minimization of color storage.

3.0 SYSTEM TRADEOFF

A number of system tradeoffs were made during the STP Converter Program. The purpose of these tradeoffs was to select system techniques and architecture that allowed achievement of the specified performance with a minimal cost in hardware complexity, weight, power and failure rate consistent with spare hardware design. The system tradeoffs considered; analog to digital conversion techniques, two field vs. a four field memory, implementation techniques for the selected analog to digital conversion techniques, and a tradeoffs of memory technologies. Table 3.1 is a listing of the A/D Conversion Techniques considered for use in the STP Converter Program. Six Bit PCM was used or the benchmark to compare the various alternatives against. The parameters of concern are; the compression ratio over 6 Bit PCM (a 2:1 compression ratio requires 3 bits per pixel compared to the 6 bits per pixel required for 6 Bit PCM), the distortion, hardware complexity (implied reliability), internal speed required (related to technical difficulty or complexity) and the required power. In addition, the requirement for an elastic buffer is also listed since the differential PCM techniques which offering a data compression advantage, require the considereable additional system complexity addition of a large size elastic buffer. The system hardware cost of this elastic buffer (which is not considered part of the A/D Converter) is so substantial for a device the size of the STP Converter, that A/D Conversion techniques requiring such a buffer are eliminated from further consideration.

One bit delta modulation offers a data compression advantage and hardware complexity advantage over 6 Bit PCM but suffers in a system comparison due to the distortion which although listed as moderate (for most application) is inadequate to meet the STP Converter requirements unless the data compression advantage is lost.

Multi-Bit Delta Modulation offers a 2 to 3 to 1 data com-
pression over PCM and if properly designed can have very low
distortion and can meet the STP Converter specification. Its
hardware complexity may be greater than PCM but for an applica-
tion like the STP Converter, the resultant data compression
and the consequent reduction in memory make Multi-Bit Delta
Modulation a most attractive alternative. The required power
is about double that the PCM but again a comparable saving is
made in memory power. Differential PCM offers comparable data
compression (actually a little less due to extra coding over-
head) to Multi-Bit Delta Modulation and offers the advantage
of no distortion compared to PCM. Unfortunately elastic buffers
are required which adds a system penalty far in excess of the
somewhat improved distortion.

Two Dimensional Multi-Bit Delta Modulation offers a 3 - 4:1
compression over six 6-Bit PCM and has acceptably low distor-
tion. The increased hardware complexity and power consumption,
however, are excessive in overall system cost when compared to
the reduction in memory required. In addition, the higher in-
ternal speed required results in the hardware operating near
its technology limit or an even greater increase in complexity
for parallel processing.

Transform coding compression (such as Harry Slant, and Cosine
Transforms) is listed for completness since these techniques are
currently receiving a great deal of attention and offer very
attractive data compression ratios with low distortion. The
amount of hardware required for a real time, 2 dimensional trans-
form data compression is many many times more costly then any
saving in memory gained by the improved data compression ratio.

A weighing of the alternatives discussed above resulted in
Multi-Bit (one dimensional) Delta Modulation being selected as
the A/D Conversion Technique. The selected conversion technique
is 3 Bit Delta Modulation with an infinite time constant single
integrator. The details of the implementation will be discussed
in Section 4.0.

A/D CONVERSION TECHNIQUES TRADEOFFS

TECHNIQUE	COMPRESSION RATIO OVER 6 BIT PCM (Affects Memory Required)	DISTORTION OVER PCM	HARDWARE COMPLEXITY OVER PCM	INTERNAL SPEED REQUIRED	POWER CONSUMPTION REQUIRED (W)	ELASTIC BUFFER REQUIRED
6 Bit PCM	1:1	None	1	1	8-10	No
1 Bit Delta Modulation	1-2:1	Moderate	0.6	2	5	No
Multi-Bit Delta Modulation	2-3:1	Low	1-3	2	15-25	No
Differential PCM	2-3:1	None	2-3	3-4	25	Yes
2 Dimensional Differential PCM	3-3.5:1	None	3-4	6-8	50-60	Yes
2 Dimensional Multi-Bit Delta Modulator	3-4:1	Low	3-4	6-8	40-50	No
Transform Coding-Compression	8-10:1	Low	30-50	100-200	300-500	No

Multi-Bit Delta Modulation (3-Bit) Selected For STP Converter

TABLE 3-1

Table 3.2 presents a summary of the tradeoffs of a 2 field
delay vs. a 4 field delay for the quantity of memory. The 4
field delay is twice as complex and costless, 1/2 as reliable
and consumes twice as much power. In addition, the color trail-
ing of moving objects is twice as large as that for a 2 field
system. The system performance advantage for a 4 field system
is that if no vertical matrix is present, the vertical modulation
transfer function (MTF) at 490 TV line is 1.0 as compared to a
parallel color system while the 2 field delay system reduces
the vertical MTF to 0.33 at 490 TV lines. This reduction is
caused by the interlace scan system with odd and even fields.
In a 2 field memory system, the composite parallel output always
has 2 field currently aligned and one field misregistered ver-
tically by the pitch of one scan line. This misregistration
does not occur in a 4 field memory system and the loss of verti-
cal MTF does not occur. The loss of vertical MTF at 490 TV lines
however, does not present a STP converter from meeting its spec-
ification of having a vertical resolution of 330 TV lines. The
basic scanning process with the resultant Kell factor limits the
vertical resolution to about 330 TV lines long before the effect
of 1/3 field misregistration would limit the resolution. The
considerations discussed above resulted in the selection of a
2 field delay memory due to its major hardware and reliability
advantage together with the fact that its use does not prevent
the resolution specification from being met. Tests on the final
equipment have verified that this was a valid choice.

Table 3.3 lists the hardware implementation tradeoff on the
design of the Delta Modulator/Demodulator. The all analog
approach is the most attractive in terms of complexity and power
consumption. This approach has been used successfully on many
programs which do not have the stringent stability and noise spec-
ifications required for the STP Converter. It is doubtful that
on all analog 3 Bit Delta Modulator could be built meeting the
STP specification with the long term stability required for a
space mission.

TABLE 3-2

2 FIELD DELAY vs. 4 FIELD DELAY

MEMORY TRADEOFFS

	RELIABILITY	POWER CONSUMPTION	VERT MTF AT 490 TV LINES	COLOR TRAILING	COST
2 Field Delay	1	20 Watts	.33	1/30th second	1
4 Field Delay	1/2	40 Watts	1.0 (Only if no Vert. Motion)	1/15th second	2

2 Field Delay selected for STP Converter.

The all digital approach offers outstanding stability and
requires no alignment. Unfortunately, components which would
have permitted fabrication of an all digital approach with
adequate timing margin were not available when the design
decision was made in early 1974.

A Hybrid Analog/Digital Delta Modulator and an all digital
Delta Demodulator was selected as the final design for the
STP Converter contract. This approach is capable of meeting
the specification and could be built in 1974 with available
components.

The major hardware implementation tradeoff was in the choice
of memory technology. Table 3.4 lists the memory technologies
considered and this system tradeoffs of interest for the STP
Converter. Program schedule required the selection of memory
elements which were available in February of 1974. As illustrated
in Table 3.4 the schedule constraint limited the choice to P MOS
shift registers, cores or C MOS RAM's (Drum, Discs and Delay
lines were properly excluded from use in the contract).

Core Memories are well developed and feature good reliability
and low cost, unfortunately they have a severe weight and power
penalty compared to P MOS Shift Registers. C MOS RAMs have a
power advantage over P MOS Shift Registers and more graceful
failure mode advantage, but suffer a severe size and we ght dis-
advantage. In addition, the cost per bit was much higher and the
technology was not as well developed as P or N MOS.

Consideration of all of tradeoffs related to the memories
resulted in the selection of P MOS Shift Register. If the choice
were to be remade today the choice would be between N MOS RAMs
or Charge Storage Device even though the P MOS Shift Registers
were and are adequate for the application.

TABLE 3-3
DELTA MODULATION/DEMODULATION HARDWARE TRADEOFFS

	COMPLEXITY	DELTA MOD. POWER CONSUMPTION WATTS	PRECISION STABILITY	ALIGNMENT	LOOP TIMING MARGIN
All Analog	Lowest	5	Can Not Meet Long Term Drift Requirements	Very Critical	Adequate
All Digital	Highest	28	Outstanding	Non-Required	Adequate when new ECL ROM's are available mid 1975
Hybrid Analog/ Digital Delta Mod. & Digital Delta Demod.	Moderate To High	23	Non-Critical	Simple Non-Critical	Adequate to Marginal (D/A Converter Improvement Recommended)

TABLE 3-4

MEMORY TECHNOLOGY TRADEOFFS

TECHNOLOGY	AVAILABLE FEB. 1974	AVAILABLE FEB. 1975	SIZE & WEIGHT	POWER CONSUMPTION WATTS	PERFIRALS REQUIRED	COMMERCIAL COST ¢ PER BIT	REMARKS
Bubble	No	No	0.1	5	Moderate	0.05	Reliability uncertain, may have severe temp. range limitation.
N MOS RAM's (4K)	No	Yes	1	20	Minimum	0.2	Good packaging density and reliability plus excellent failure degradation.
P MOS Shift Registors (2K)	Yes	Yes	1	20	Moderate	0.4	Good packaging density and reliability.
Charge Storage Devices (16K)	No	Yes	.3	10	Minimum To Moderate	0.4	Excelent packaging & Power Uncertain reliability plus fair failure degradation.
Cores	Yes	Yes	3	80	Severe	0.3	Severe power & weight penalt good reliability.
C MOS RAM's (.5K)	Yes	Yes	8	8	Minimum To Moderate	10	Severe size & cost penality technology not as well developed as P and N-MOS.
Drums, Discs, Delay Lines	Yes	Yes	Large	Large			Bulkey, High Power, heavy excluded from use in contrac

4.0   DELTA MODULATOR/DEMODULATOR

Basic operation and testing of the Delta Modulator is outlined below along with necessary block diagrams and tables.

4.1   General Description of Delta Modulator

The general operation of the Delta Modulator is broken down into three major areas, Analog Input Circuits, Quantizer and Code Converter, and Digital Integrator. The following diagrams are used in the operation description: Figures 4.1, 2, 3, 4, 5, 6).

4.1.1   Video Input Analog Circuits

Figure 4.1 is a block diagram of the Delta Modulator showing the various functional blocks which make up the subsystem. Figure 4.2 is a block diagram of the Analog Input Circuits. The video input signal from the camera is buffered by an input amplifier. Input impedance is 75 ohms. A 5 m.c. 5 pole filter is used as the pre-sampling filter for the video input data. The output of the filter is buffered with an (A.C.) coupled non-inverting amplifier. The amplifier has an offset adjustment to center the video signal about ground. Reference Drawing (007).

The video signal is split at the output of the A.C. coupled amplifier. One signal is buffered and sent to the memory sync circuits. This signal is used to generate the vertical and horizontal timing for the memory and Delta Modem.

The other video signal is sent to the blanking amplifier (reference Drawings (003), (001). The blanking amplifier inserts a reference ground level into the signal to be quantized. The signal to be quantized is then symmetrical about ground with a peak-to-peak video signal of about .85 volts. It is necessary to do this so as to use the full dynamic range of the delta modem. Offset adjustments are provided to adjust the reference blanking level to .00 volts.

BLOCK DIAGRAM DELTA MODULATOR   Fig 4.1
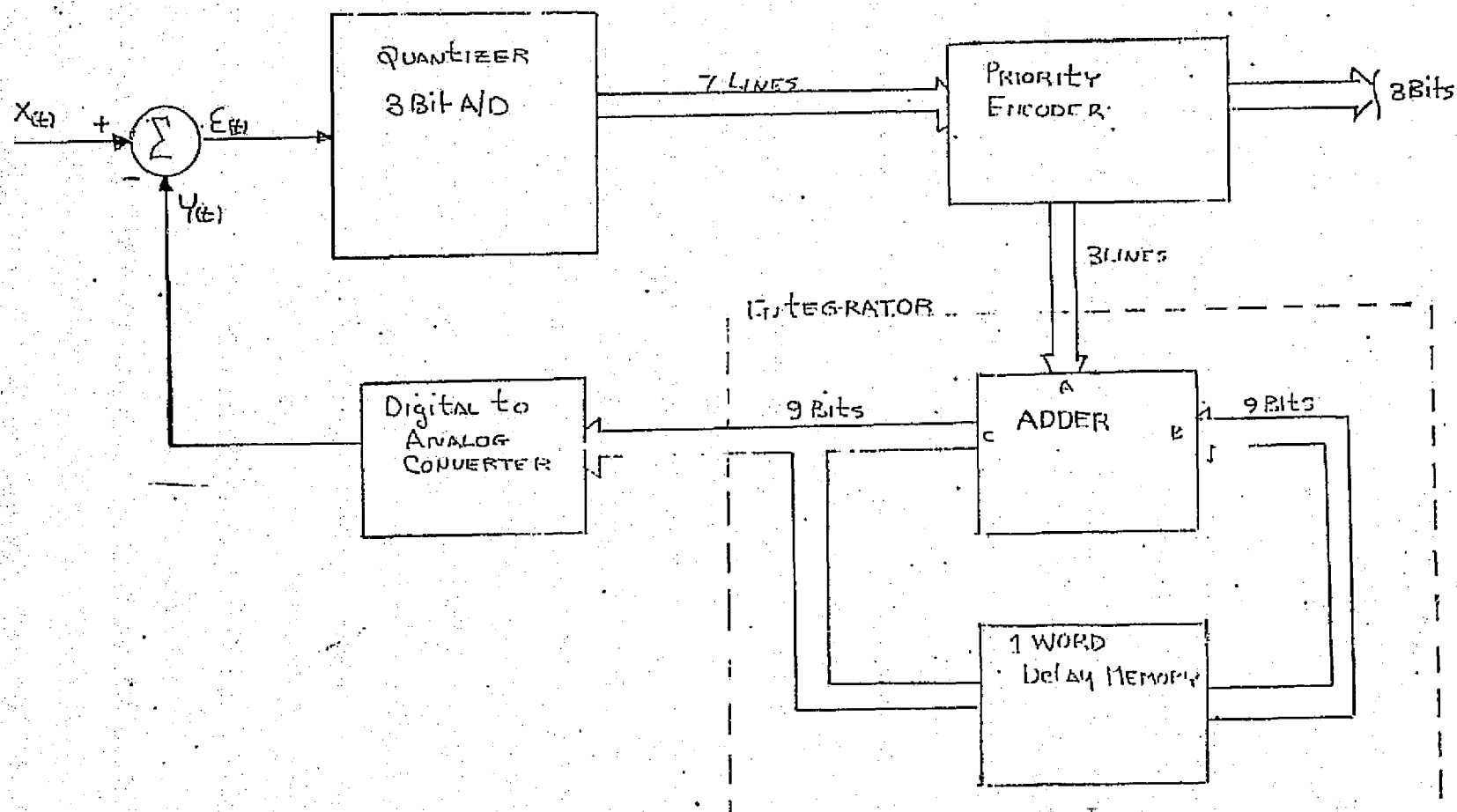
FIGURE 4.2

BLOCK DIAGRAM ANALOG INPUT ELECTRONICS

(F.P.)

BLANKING INPUT

VIDEO
INPUT   J7

$f_c = 5$ MHz

BUFFER

5 POLE FILTER
BUTTERWORTH

BUFFER
AMPLIFIER

BLANKING
AMPLIFIER

VIDEO
DRIVER AMP

TO VIDEO OUT Σ

OFF SET BIAS

OFF SET ADJUST.

BUFFER
AMPLIFIER

VIDEO OUTPUT TO SYNC SEPARATOR

(F.P.) Front Panel
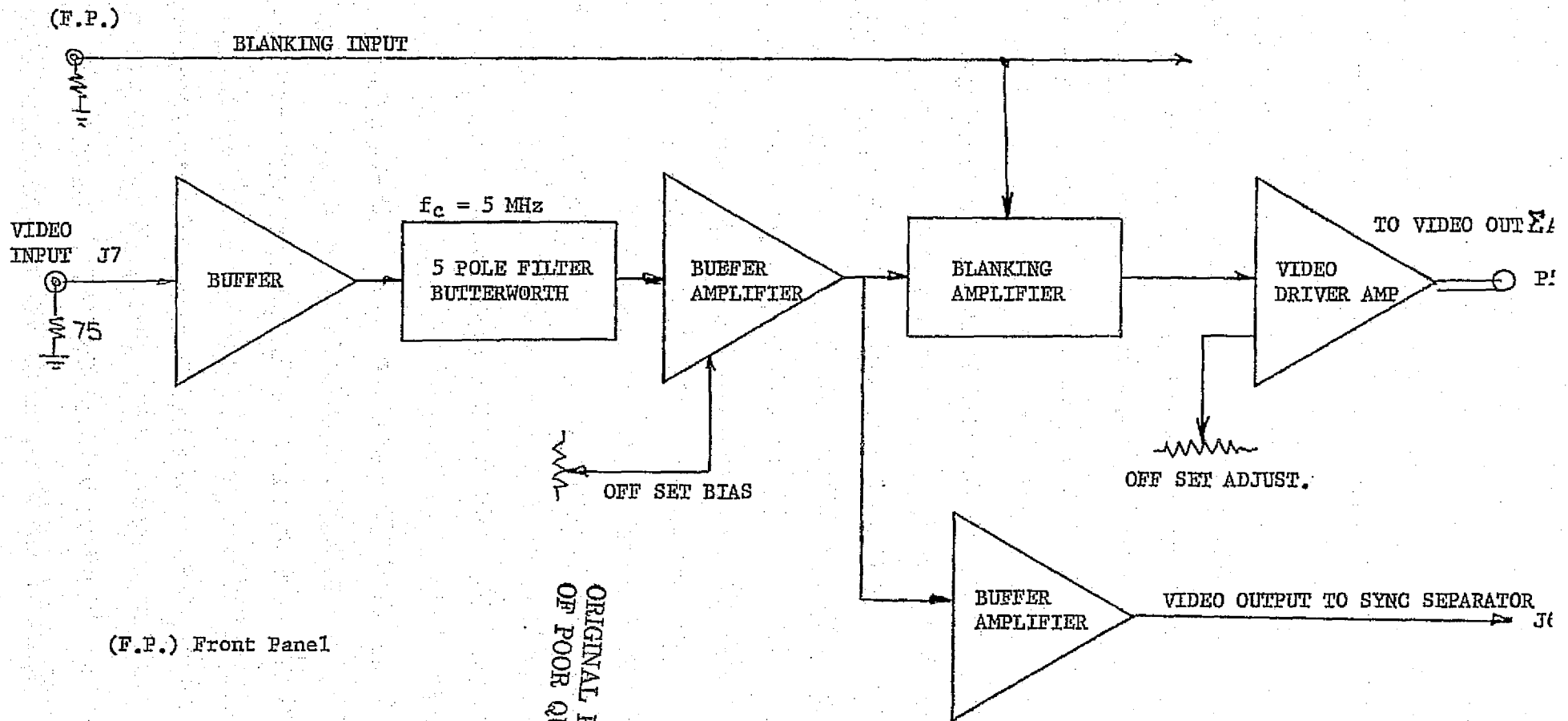
FIGURE 4.3 - BLOCK DIAGRAM QUANTIZER AND CODE CONVERTER ELECTRONICS
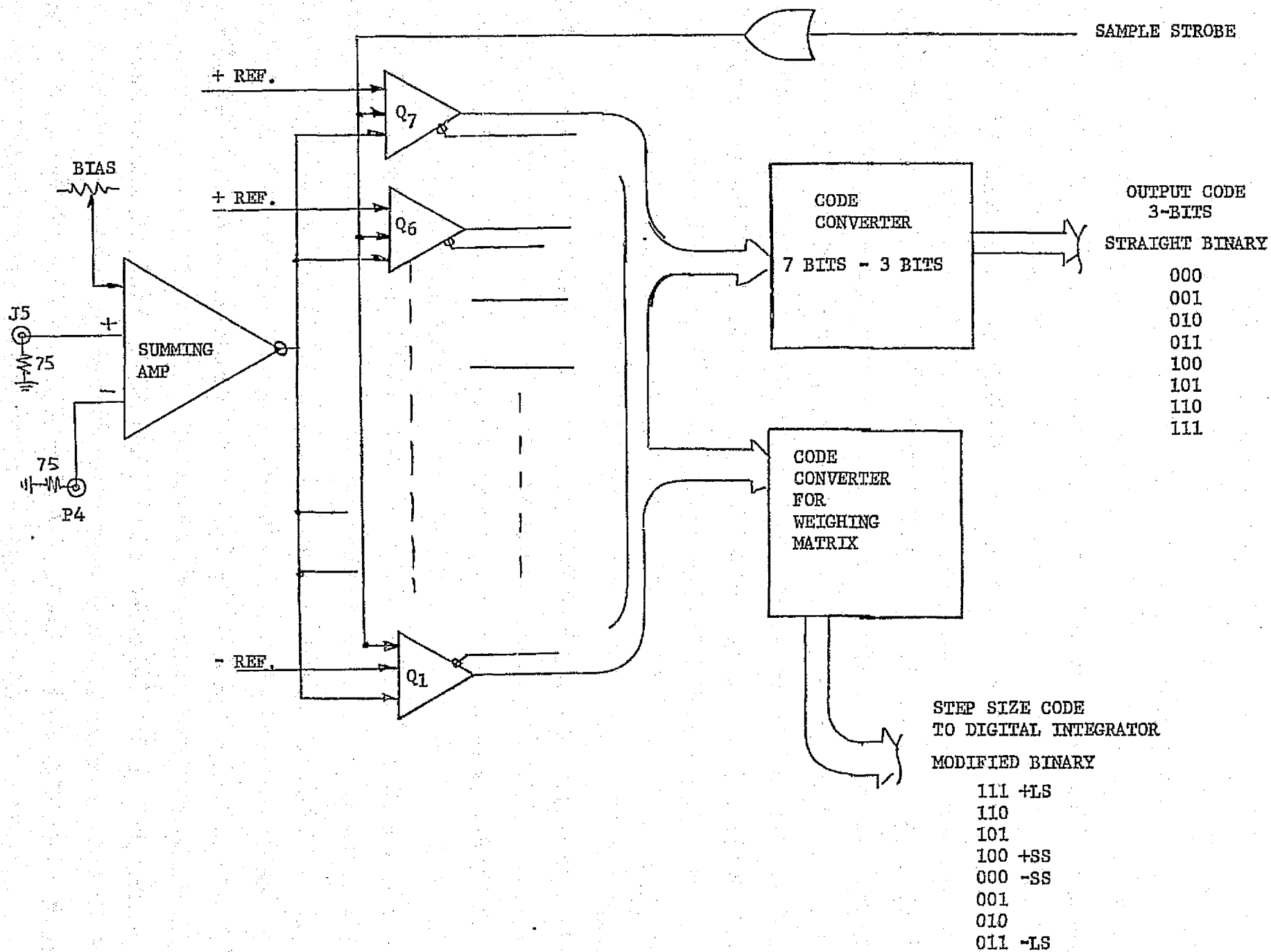
4.1.1   <u>Video Input Analog Circuits</u> (Continued)

Another requirement for having a blanking reference level is that the
digital delta mod-demod has to start from a reference level. The delta
demod is blanked to this reference level during retrace (horizontal and
vertical sync time). The first sample out of the Delta Modulator is
referenced to this blanking level; hence the delta mod-demod will have
amplitude tracking in the digital integrators. The memory unit blanks
the data during retrace; hence any data output during retrace is false
information and would start the delta demod in error if allowed to
integrate during retrace; hence we blank both mod and demod digital
integrators to the reference ground level.

Because we blank both the input video and integrator signal to a
reference blanking level, the largest error signal which can occur at
the digital integrators of either the mod or demod is one small size
step at the beginning of any scan line.

4.1.2   <u>Summer Quantizer</u>

Figure 4.3 is a block diagram of the Summer Quantizer electronics,
reference Drawing (010).

The summing amplifier is an inverting operational amplifier, reference
Drawing (001). It has a closed loop band width of about 80 mc with a
signal propagation delay of about 8 ns. The summing amplifier sums the
output of the digital integrator and the blanked video input. The output
of the summer drives the seven quantizer amplifiers used to quantize the
loop error signal.

The quantizers used are (AM 685). They have a nominal 7 ns propagation
delay and also has an internal strobe. This strobe is used to sample
the quantized data, and is the reference timing point for the closed
loop system, reference Figure 4.2.3.

FIGURE 6.3 — BLOCK DIAGRAM QUANTIZER AND CODE CONVERTER ELECTRONICS

SAMPLE STROBE

+ REF.

Q_7

BIAS

+ REF.

Q_6

J5

75

SUMMING
AMP

75

P4

Q_1

− REF.

CODE
CONVERTER

7 BITS − 3 BITS

CODE
CONVERTER
FOR
WEIGHING
MATRIX

OUTPUT CODE
3-BITS

STRAIGHT BINARY

000
001
010
011
100
101
110
111

STEP SIZE CODE
TO DIGITAL INTEGRATOR

MODIFIED BINARY

111 +LS
110
101
100 +SS
000 −SS
001
010
011 −LS
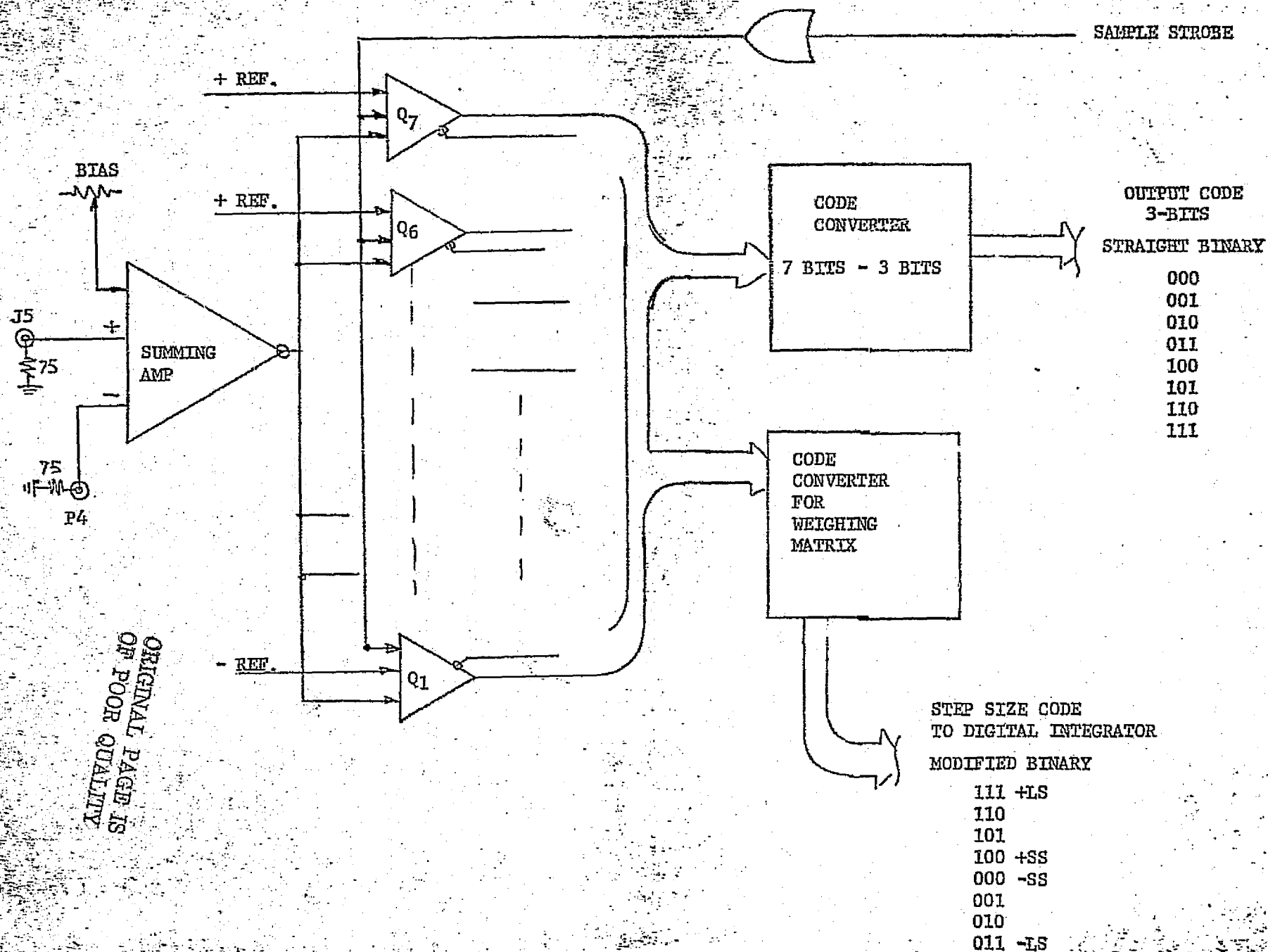
4.1.2   Summer Quantizer (Continued)

The quantized sampled data is then used to drive the digital loop
integrator, and this data is also converted to a 3-bit binary code,
which is the outputted data of the delta mod.

The output 3 bit code is generated in a 7 line to 3 line MECL 10K
priority encoder. This encoder is sampled by word clock (WS), and
the 3 bit data code is outputted to the digital memory for reformatting.

The quantized data to the integrator is a modified binary code, and it
is coded to represent the quantized step size (111 equals largest
Positive Step, and (011) equals largest Negative Step size).

The step size code pertains to a particular weight which is added or
subtracted from the digital integrator.

4.1.3   Digital Integrator

A block diagram of the digital integrator is shown in Figure 4.4, also
reference Drawing (012).

The digital integrator accumulates successive samples of the quantized
error forming the reconstructed video signal. This reconstructed
signal is fed back to the summing amplifier and differenced with
incoming video to form the error signal.

The integrator consists of an input signal complementer, arithmetic
unit, memory storage, and a digital to analog converter. The integrator
is implemented as an infinite time constant integrator, as contrasted
with an analog version which would have a finite time constant (leaky
integrator).

A weighting matrix is used to determine the corresponding error step
size added to the integrator. This weighting matrix was intended to
select a variety of large and small step sizes for evaluation of
dynamic response and noise performance, reference Drawing (011).

FIGURE 4.4 - BLOCK DIAGRAM OF DIGITAL INTEGRATOR
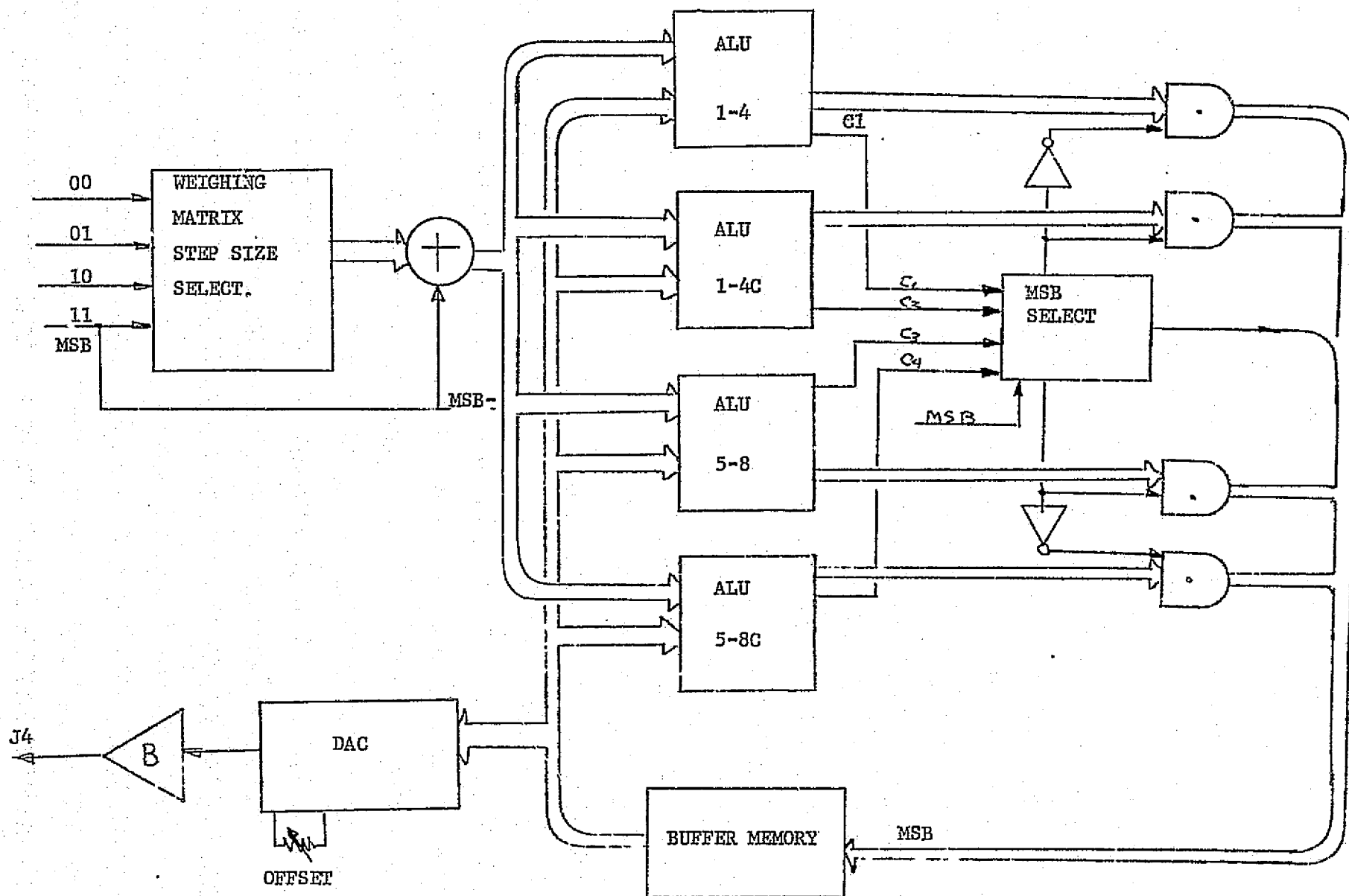
Because of the limited amount of time available to close the delta mode loop at 12.25 m.s.s. rate (80 nano-second), it was necessary to wire across the delta mod weighting matrix, and fix the step size input to the (ALU)arithmetic logic unit. This was necessary because of poor settling time of the D.A. converter (25-30 ns).

In order to decrease the full add cycle time of the MECL ALU, the design features a multiplexed 9 Bit Full Adder. The total full add time can be cut in half (44 ns to 24 ns) by selecting the correct sum based on conditions of carriers in the ALU, reference Figure 4.5.

Figure 4.5 gives the conditions for selection of the proper ALU sum to be multiplexed. The ALU's are arranged with and without carry in add one. For example, if we wish to add two Binary Numbers together (both numbers positive), we first select ALU (1 - 4) A. We next examine carriers C_1, C_2, C_3 and C_4 to determine which succeeding ALU will be selected. In this manner it is possible to select the proper sum in less than 14 ns. Multiplexing of the outputs takes about 6 to 7 ns with a total full add-subtract taking less than 24 ns.

A full ripple through full add subtract with look ahead carry would take about 43 ns. This would be an excessive loop delay and it would not be possible to close the digital delta mod loop in less than the prescribed 80 ns time.

The output of the add-subtract logic is stored in the one bit buffer memory, which completes the integrator logic. Successive samples are added and stored reconstructing the sampled input video data.

The digital word which exists on the buffer memory is inputted to a high speed digital to analog converter. This signal is transformed to an analog voltage   This voltage is used to form the error signal when summed with the input video.

FIGURE 4.5
ALU SELECTION

C_{IN} (Only in Subtract (B) used)

```
┌──────────┐          ┌──────────┐
│ A        │          │ B        │
│ Bits     │          │ Bits     │
│ 1-4      │          │ 1-4      │
│          │          │          │
│          │          │          │
└────┬─────┘ C1       └────┬─────┘ C2
     ▼                     ▼
┌──────────┐          ┌──────────┐
│ C        │          │ D        │
│ Bits     │          │ Bits     │
│ 5-8      │          │ 5-8      │
│          │          │          │
│          │          │          │
└────┬─────┘ C3       └────┬─────┘ C4
     ▼                     ▼
┌──────────┐          ┌──────────┐
│ E        │          │ F        │
│ Bit 9    │          │ Bit 9    │
│          │          │          │
└────┬─────┘ C5       └────┬─────┘ C6
     ▼                     ▼
```
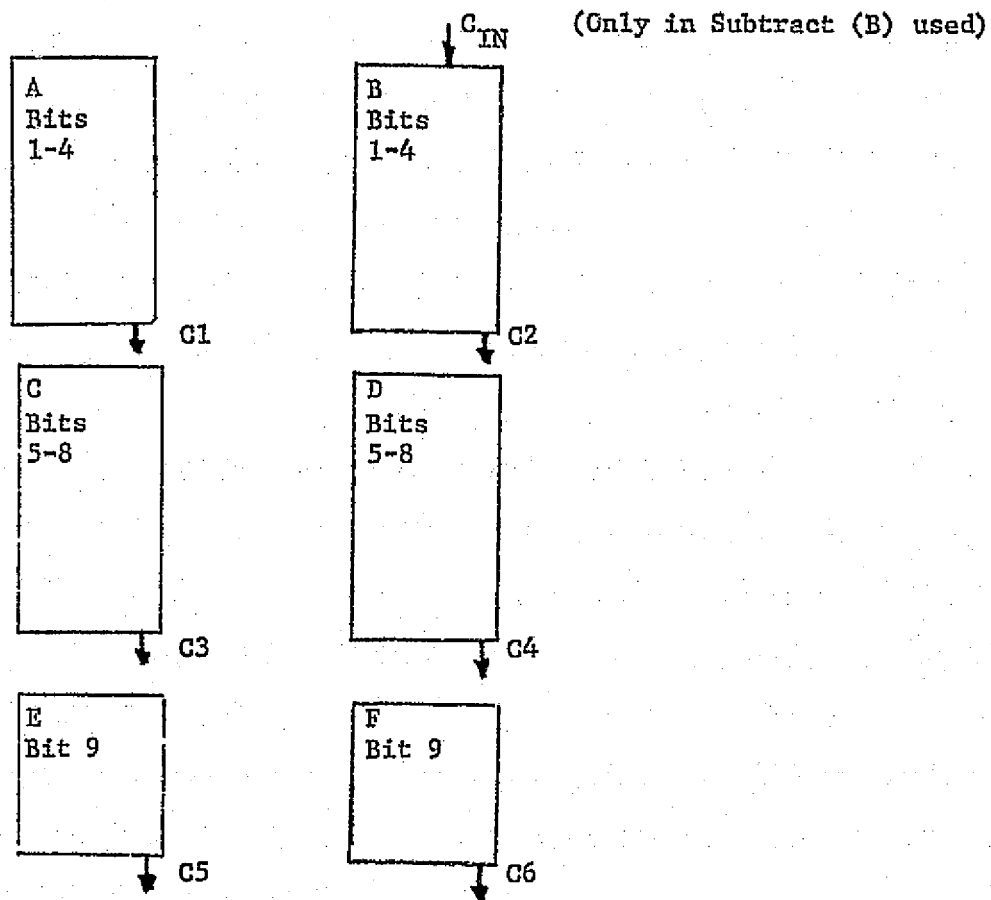
CONDITION:

If Adding:

Valid Combinations   ABE + ABF + ADE + ADF

If Subtracting:

$$BCE + BCF + BDE + BDF$$

The Conditions of the carriers determine selection of C, D, E, F

The Condition of ADD or SUBTRACT determined by (MSB)

4.1.3 Digital Integrator (Continued)

The above described components when interconnected as shown in Figure 4.1 and Drawing (012) form the digital delta modulator. Propagation delay of the loop is 80 ns, which is sufficient to assure operation of the loop.

4.2 General Operation of the Delta Demodulator

The following outlines the general operation and testing of the digital delta demodulators. Reference will be made to the following figures, 4.6, 4.7, 4.8, and 4.9.

4.2.1 General Operation

A block diagram of a digital Delta Demodulator is shown in Figure 4.6. This block diagram shows a single channel demodulator. The actual delta demodulator has three identical channels for the Red, Blue and Green fields.

There are two basic sections of the demodulator; the digital code converter and integrator, and the analog output circuitry.

The binary input code is first converted to a bipolar code (standard binary notation for plus or minus weighing). The input code is then weighed depending on the particular system response desired. Weighing is done by the step size converter.

Step sizes are selected by a front panel control switch which adjusts the four coded steps. It should be noted that this step size control was bypassed in the modulator unit. The modulator step size was set to correspond to a code (3434), reference Drawing (011). The code is read largest step first, smallest step last, and from left to right on the front panel. The code can be changed in the modulator if desired by rewiring the code weights. The demodulator is still connected to the code selector switches and hence must always be set to 3434 as long as the modulator is wired for this code.

FIGURE 4.6 - BLOCK DIAGRAM DELTA MODULATOR
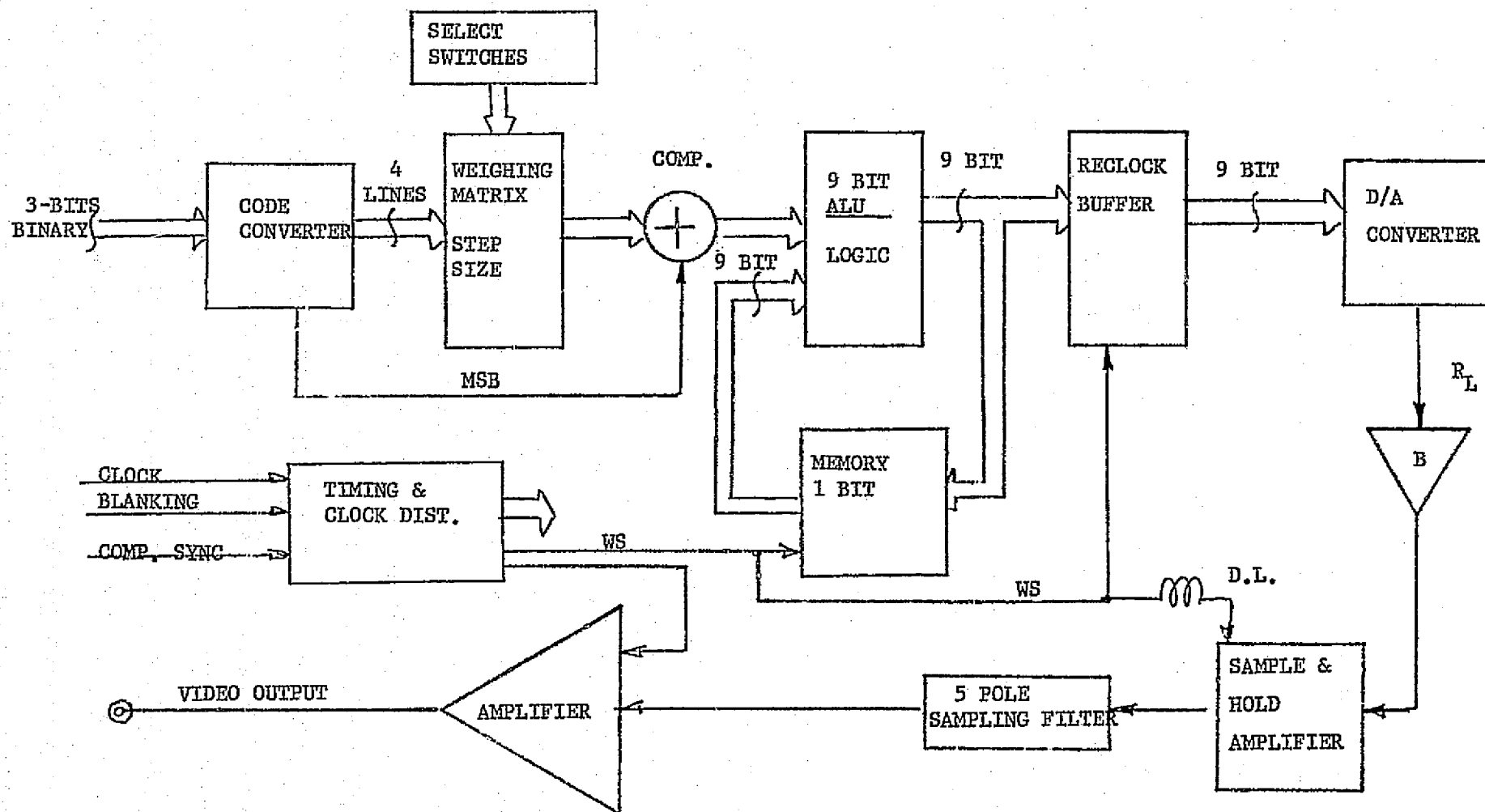
4.2.1 General Operation (Continued)

The weighed code is inputted to the digital integrator and summed with
the feed back memory signal. The integrated (reconstructed signal) is
then outputted to the digital to analog converter, and analog processing
electronics.

4.2.2 Description of Arithmetic Unit In Demodulator

The Arithmetic Unit in the Demodulator consists of two ALU's, a full
adder, 8 modulators, 2 complementing gates, and a 1-bit delay memory.
This unit performs a nine bit add-subtract with the input data from the
weighing matrix and the one clock period delayed sums from the memory
(Figure 4.7).

Input data from the weighing matrix consists of 9 bits in standard sign
magnitude form. The most significant bit contains the sign information,
a one representing a negative number and a zero a positive number. The 8
least significant bits contain the magnitude information.

<div align="center">

SIGN BIT

Y X X X X X X X

MAGNITUDE

</div>

When the sign bit is high the complementing circuit is activated,
inserting the complemented magnitude bits into the ALU's instead of
the normal sum. If the sign bit does not indicate a negative number
the weighing matrix word passes directly into the adder's. The output
of the complementers is summed directly with the one clock delayed sums
from the memory. There is no recomplementing necessary at the output
of the adders when the weighing matrix input is a negative quantity.
This is possible because the D.A.C. is operated in the unipolar mode
(see Table 1). The adders operate in a straightforward manner except
when the weighing matrix vector is negative When this occurs an end
around carry is generated out of the full adders. This carry must then
be added back into the sum in the adder.
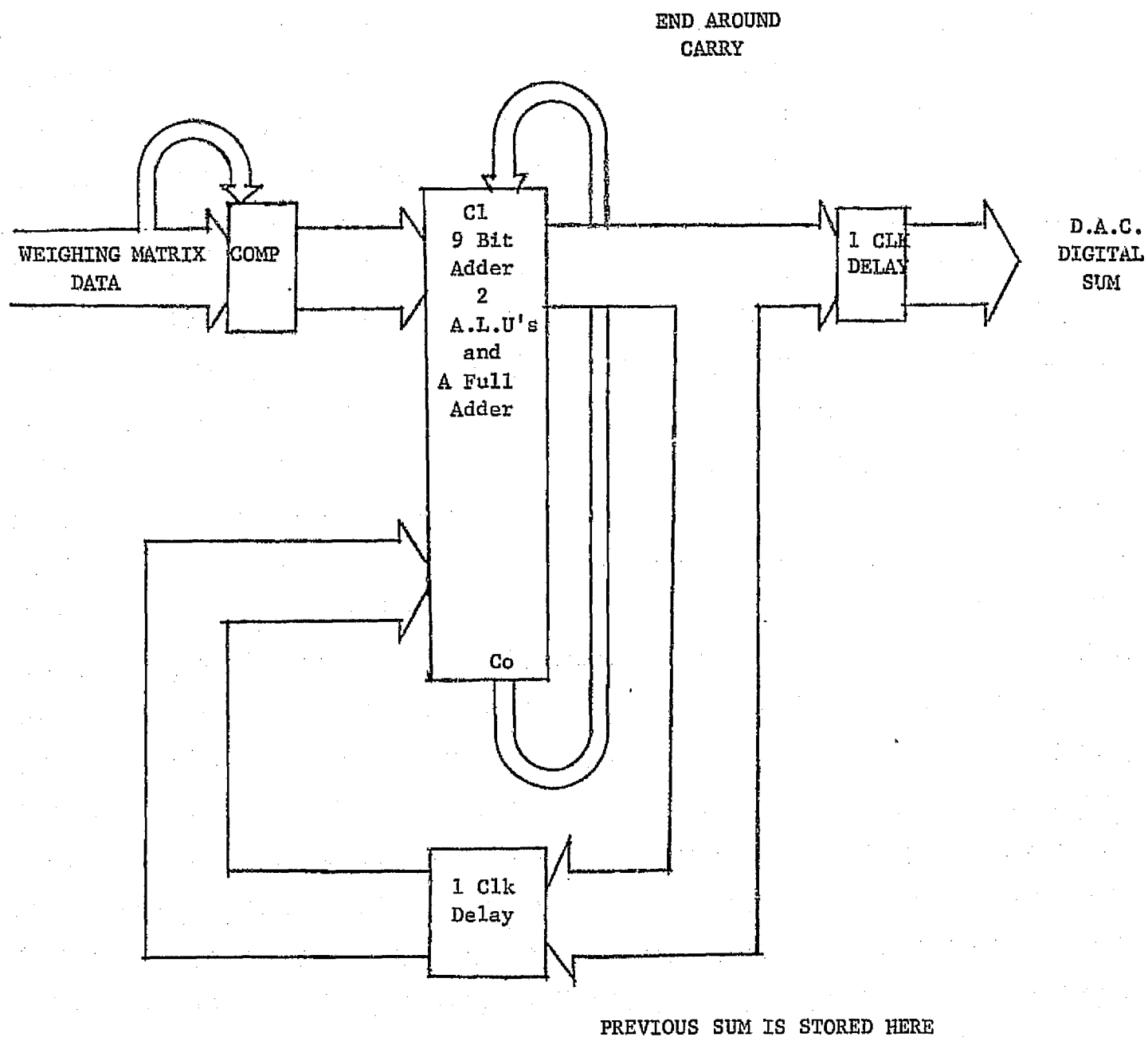
FIGURE 4.7   BLOCK DIAGRAM OF ARITHMETIC UNIT IN DEMOD

Because the D.A.C. is operated in the unipolar mode there is no
characteristic problem of a positive and a negative zero normally
associated with one's complement arithmetic.

TABLE 1

1111	7	
1110	6	
1101	5	
1100	4	
1011	3	
1010	2	Four Bit Sample Array of numbers
1001	1	which are clocked directly into
1000	0	the D.A.C. and which are also
0111	-1	delayed one clock period and
0110	-2	summed with the sign magnitude
0101	-3	data from the weighing matrix.
0100	-4	
0011	-5	
0010	-6	
0001	-7	

The operation of this circuit can also be explained by several 4-bit
examples.

The addition of a negative number from the weighing matrix to a positive
number from the memory is shown as:

-4	1 1 0 0	Data from weighing matrix
	1 1 0 1 1	Complemented data
+2	1 0 1 0	1 Clock delayed sum from memory.
	0 1 0 1	
	<u>0 0 0 1</u>	End around carry added in
-2	0 1 1 0	Final Sum

4.2.2   Description of Arithmetic Unit In Demodulator (Continued)

Words appear from the weighing matrix in sign magnitude form.   The
magnitude is then complemented before being inserted in the adders.
The coding of the delayed memory sum can be checked with Table 1;
notice that since the weighing matrix sum is negative that an end
around carry is generated out of the most significant bit and must be
added into the final sum.   The coding of the final sum also may be
checked on Table 1.   Additional examples of arithmetic operations are
shown below.   They demonstrated the addition of two negative numbers,
two positive numbers, and a negative number and a positive number which
add up to zero.

```
      -4              1 1 0 0              -4      1 1 0 0
 End around           1 1 0 1 1                    1 0 1 1
 carry
      -2              0 1 1 0              +4      1 1 0 0
                      0 0 0 1
                      0 0 0 1
      -6              0 0 1 0
```

FIGURE 4

```
       4              0 1 0 0
       2              1 0 1 0
       6              1 1 1 0
```

FIGURE 5

```
      -4              1 1 0 0
 End around           1 1 0 1 1
 carry
      +4              1 1 0 0
                      0 1 1 1
                      0 0 0 1
       0              1 0 0 0
```

FIGURE 6

All of the initial delayed sums and final sum can be checked on Table 1.

4.2.3 Delta Demod Analog Circuits

Figure 4.8 shows the analog circuits used to process the digital output signals. Reference should also be made to Drawing (008).

The output of the digital integrator is converted to an analog signal by the D/A converter. It should be mentioned that the digital word appearing at the integrator of the delta mod is identical to that appearing at the digital demod integrator. The D-A converters are current dacs and are initially matched with one percent resistors. Gains are matched on the final voltage output amplifiers.

Because the output signal of the DAC can have a switching glitch, a sample and hold amplifier is used to remove this spike. The sampler is phased with a delay line so as to sample the analog output during the middle of a sample period, reference Figure 4.9a.

A five pole filter is used to smooth the output of the sampler and to remove the clock sampling edges from the video.

The video is summed with composite blanking and composite sync.

Composite Sync and blanking are obtained by combining the delta demodulator blanking furnished by the memory sync separator with a composite sync signal generated also by the memory. These signals are combined in a current switched amplifier. The levels of the blanking and sync can be adjusted independently. This is necessary because the video reconstructed from the digital integrator was modified to use the maximum dynamic range of the delta modulator, reference Figure 4.9b.

The signal gains of each output amplifier are adjusted to track each other within ± .5% and the output level of the fifth step of a 10 step gray scale is adjusted to within 5 mv of each other.

The output video amplifier is designed to drive a 75 ohm terminated load.

FIGURE 4.8 - BLOCK DIAGRAM ANALOG (RGB) OUTPUTS
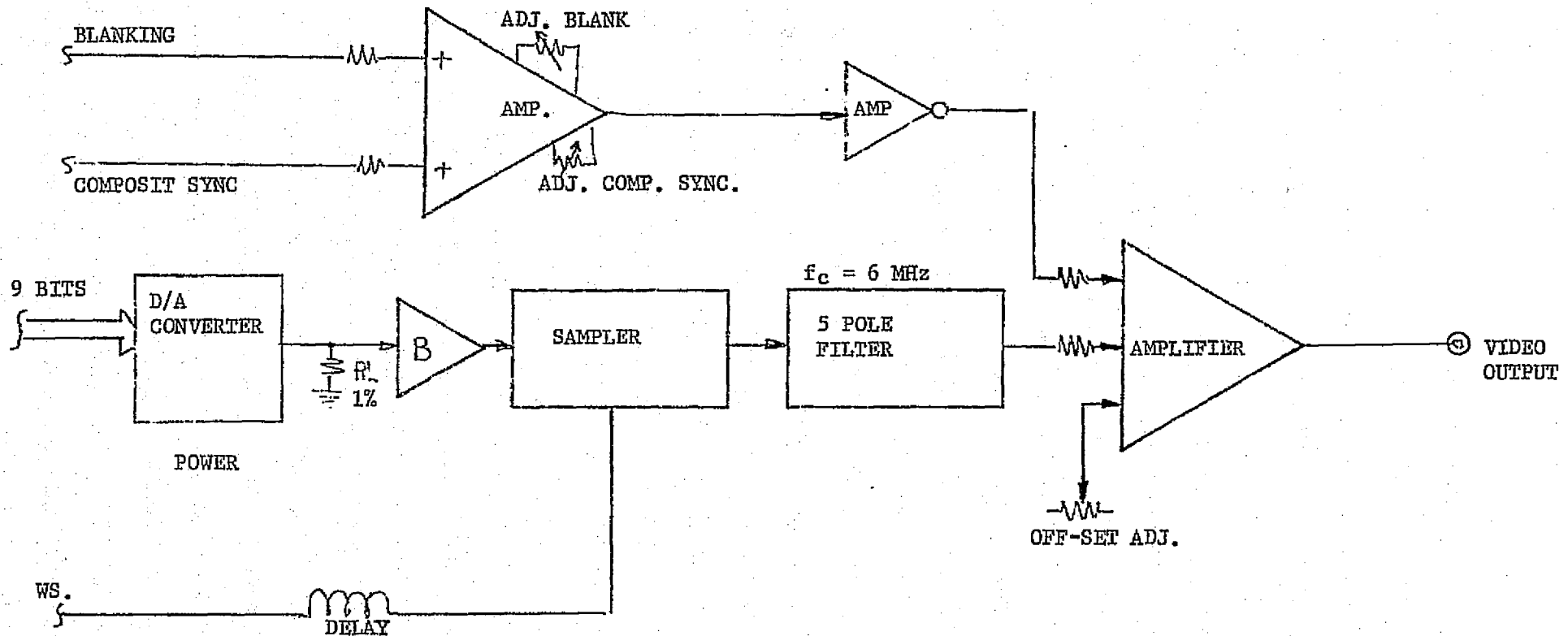
FIGURE 4.9a - SAMPLE AND HOLD SAMPLING TIMES

W.S.
CLOCK

GLITCH

VIDEO

SAMPLER
CLOCK DELAYED

SAMPLED
VIDEO OUT

GLITCH REMOVED
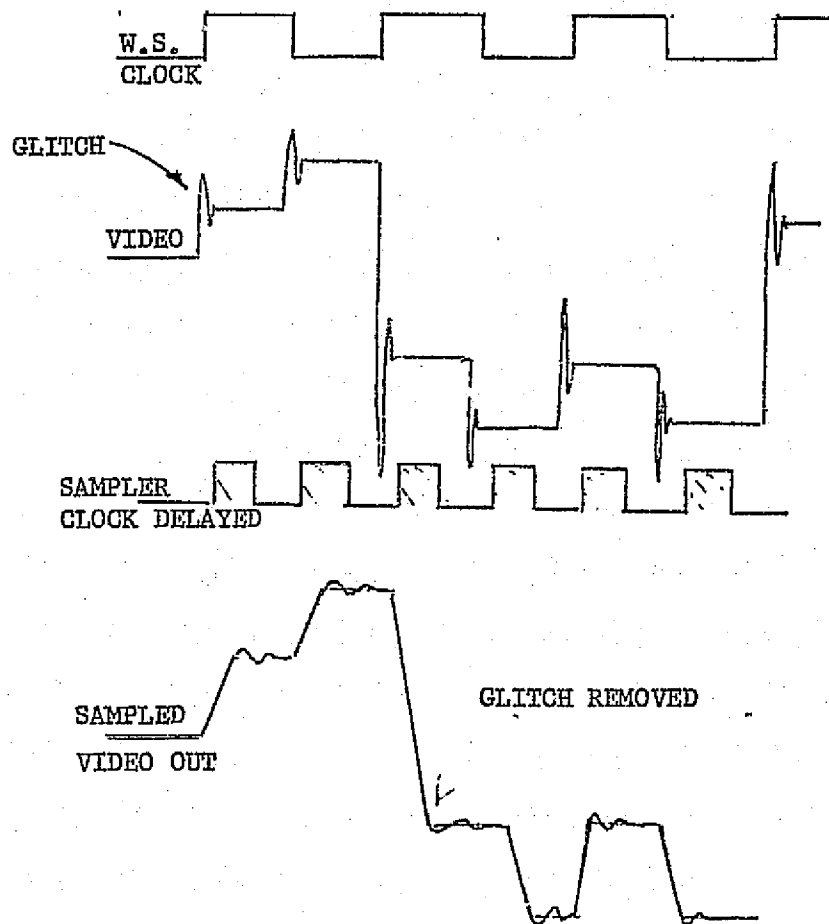
FIGURE 7.4 b - COMPOSITE SYNC & BLANKING INSERTION

COMPOSITE SYNC

VIDEO OUTPUT
OF FILTER

COMPOSITE VIDEO
OUT
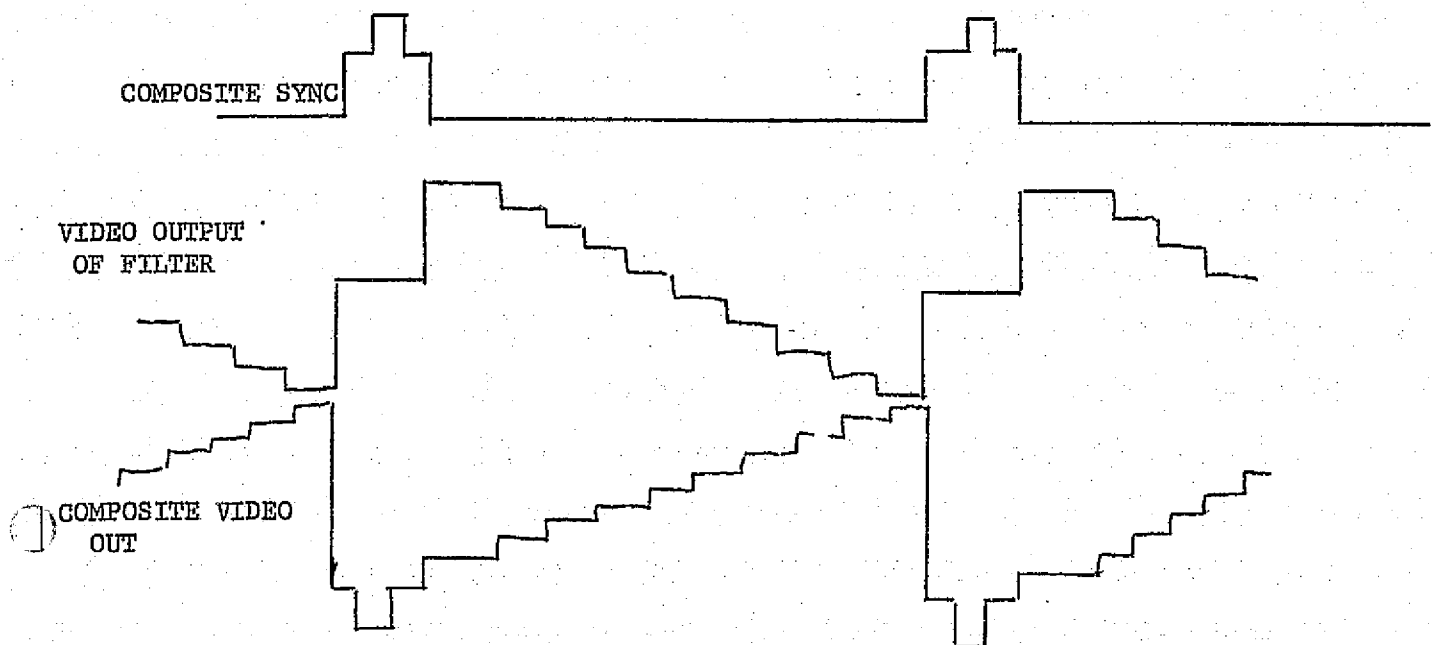
4.3   Design Trade-off Analog vs Digital Integrator

As described above the design approach was to use an all digital loop
integrator. The initial design was to incorporate an all analog
integrator. This design approach had to be changed due in part to the
required accuracy of the analog current switches. This accuracy was
approximately .01% of full scale for a full 620 sample scan line. This
accuracy was required because any offset current would be integrated
(plus or minus) during the scan line time and hence the absolute value
of the integrator at the end of a scan line could be in error by as much
as 5% under worst case conditions. Because of the difficulty in main-
taining this accuracy it was felt that an all digital integrator had to
be implemented. It should be pointed out that the limiting constraint
placed on the delta mod was that it had to operate with an almost
infinite time constant. This constraint was placed on the system by
the requirement that all three output channels (Red, Blue, Green) had
to track within 2.5 mv of each other with a one volt peak-to-peak output
signal.

In order to achieve this requirement it was necessary to use an all
digital delta demod implementation. By doing this we could use a
digital to analog converter as the analog output device for each delta
demod. This would allow us to normalize the analog out from all three
channels during blanking (all channels start from same reference point).
This also compensated for any offset in the delta modem due to bias
error because all three data outputs use the same analog to digital
converter. The most important consideration is that the D-A converter
is driven by a digital word, hence there is no accumulative error due
to temperature drift on the circuits.

4.3.1   Hybrid Delta Modem

Based on the above constraints and limitations a hybrid delta modulator
was developed. The modulator was discussed in section 4.1.1.

4.3.1 Hybrid Delta Modem (Continued)

The features of this approach employed use of an analog summer and quantizer coupled with a digital integrator and digital to analog converter. This approach was not optimum because of constraints on the D-A converters available for use (settling times were excessive for eight bit conversions, 10-15 ns). This excessive settling time, coupled with the conversion glitch, required the delta mod loop to operate in a marginal condition. The marginal condition was excessive loop time in converting a sample and feeding this sample back for comparison with incoming video. Closed loop times of about 75 ns to 80 ns were experienced, which left almost no margin for temperature variation of components in the loop (closed loop time for 12.2 ms is 82 ns).

4.3.2 All Digital Delta Modulator

An all digital delta mod-demod is proposed for any follow-on effort. An all digital unit would improve loop time and eliminate the D-A converter in the loop. Both mod and demod would be all digital and would require almost no alignment or adjustment with the exception of the input and output analog processing circuits.

Figure 4.10 is a block diagram of an all digital delta mod. The difference between the hybrid design and the all digital design is the replacing of the analog circuits in the closed loop with digital circuits. Specifically these would be the analog summer amplifier replaced with an 8 bit ALU; the quantizer replaced with a digital look up comparator (Random Access Memory, RAM); and the digital analog converter. We would not need to convert the stored integrator word to an analog signal, hence we eliminate the need for a D-A converter in the loop. We must add an A-D converter to the input of the loop. This is necessary to convert the analog video to digital samples. The loop conversion time of the digital loop is in the order of 60 ns. This would support a real time sample rate of about 16.5 megasamples per second and would provide adequate margin for the loop.

4.3.2   All Digital Delta Modulator (Continued)

As pointed out in following sections, with a sample rate of 12.5 mss
we were able to resolve 550 line horizontal with no noticeable
contouring of the video image when quantized with 3 bit.

It should also be pointed out that using the all digital approach, we
can easily change the quantizing from one, two or three bits to support
available data bandwidths.

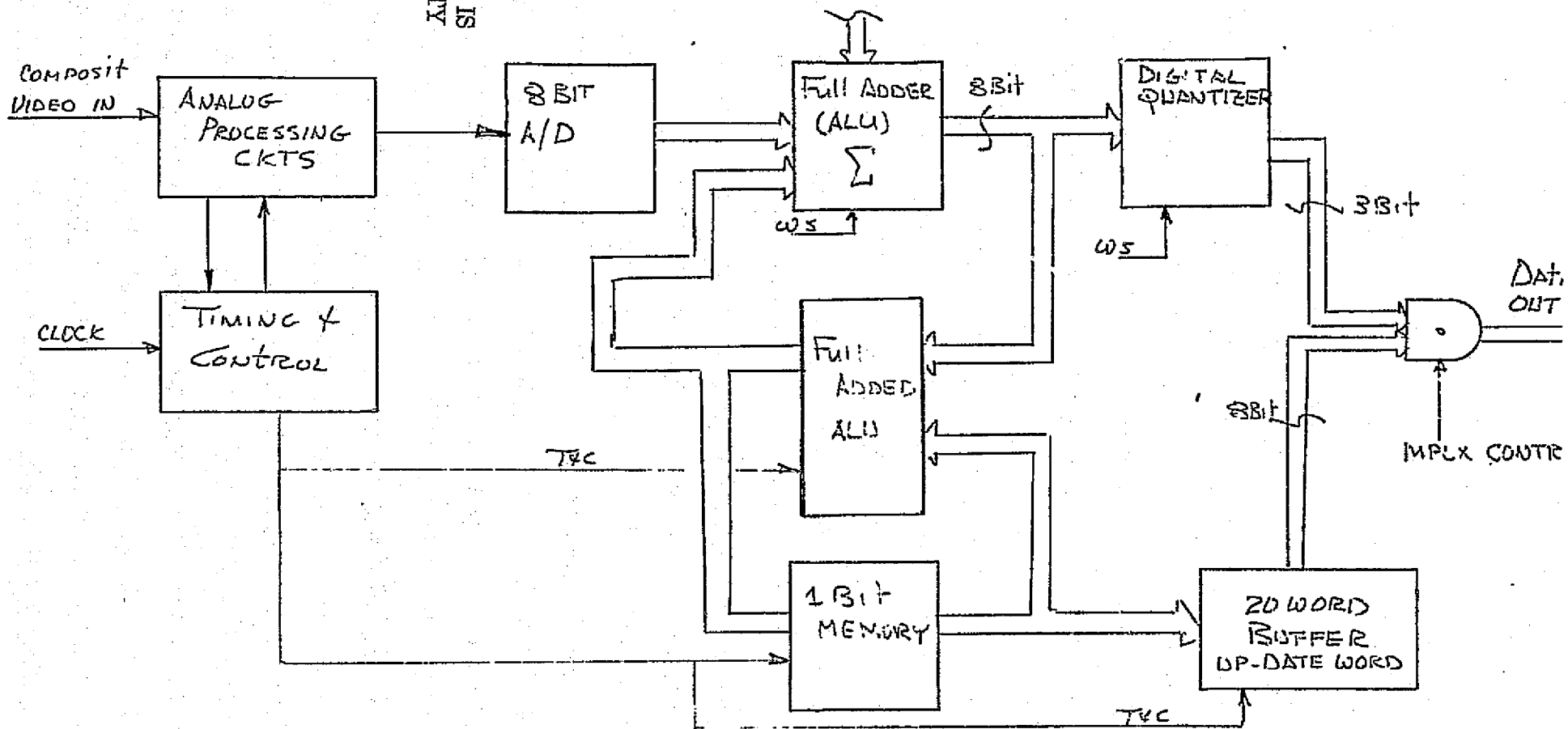4.3.3   Uplink and Downlink Transmission of Digital Delta Mod Data

For possible transmission of video data over radio links a delta
modulator performs quite well. It affords good data compression with
a minimum of equipment. (Two bit delta mod equivalent to 6 bit PCM
for black and white, 3 bit delta mod equivalent to 6 bit PCM for color
and 8 bit PCM for black and white.) The digital data can be easily
modulated PSK, or QPSK. The information quality versus link error rate
is quite good. Excellent performance at error rates of 10^{-3} can be
achieved using integrator update words which can be transmitted during
retrace. These update words are the exact values of the digital
integrator at specific times during a scan line. These values can be
buffered, stored and transmitted to the demod during retrace blanking
time. The words can be used to reset the demod integrator in the advent
of link errors in the received digital data.

This process is not necessary when an analog modulator-demodulator is
used. The reason being that the integrator is made to leak with a
specific time constant. In this way the delta mod-demod is D.C.
restoring and hence link errors introduced tend to integrate out. Delta
modulators of this type have been utilized at sample speeds in excess
of 100 megasamples per second.

For the digital delta mode the same pseudo error masking can be accomplished
by reinserting the exact value of the integrator at specific times. The
amount of stored data required is equivalent to about 3% of the line scan
data. It is also necessary to buffer one line of received data. This is
necessary to reinsert the update data in the respective scan line.
Figures 4.10 and 4.11 show in block diagram form this process.

COMPOSIT VIDEO IN

ANALOG PROCESSING CKTS

CLOCK

TIMING & CONTROL

8 BIT A/D

Full Adder (ALU) Σ

8Bit

DIGITAL QUANTIZER

WS

WS

3Bit

Full Added ALU

T&C

Dat OUT

8Bit

IMPLX CONTR

1 Bit MEMORY

20 WORD BUFFER UP-DATE WORD

T&C

ALL DIGITAL DELTA-MODULATOR FIG 4.10
WITH UP DATE WORD FOR DATA TRANSMISSION
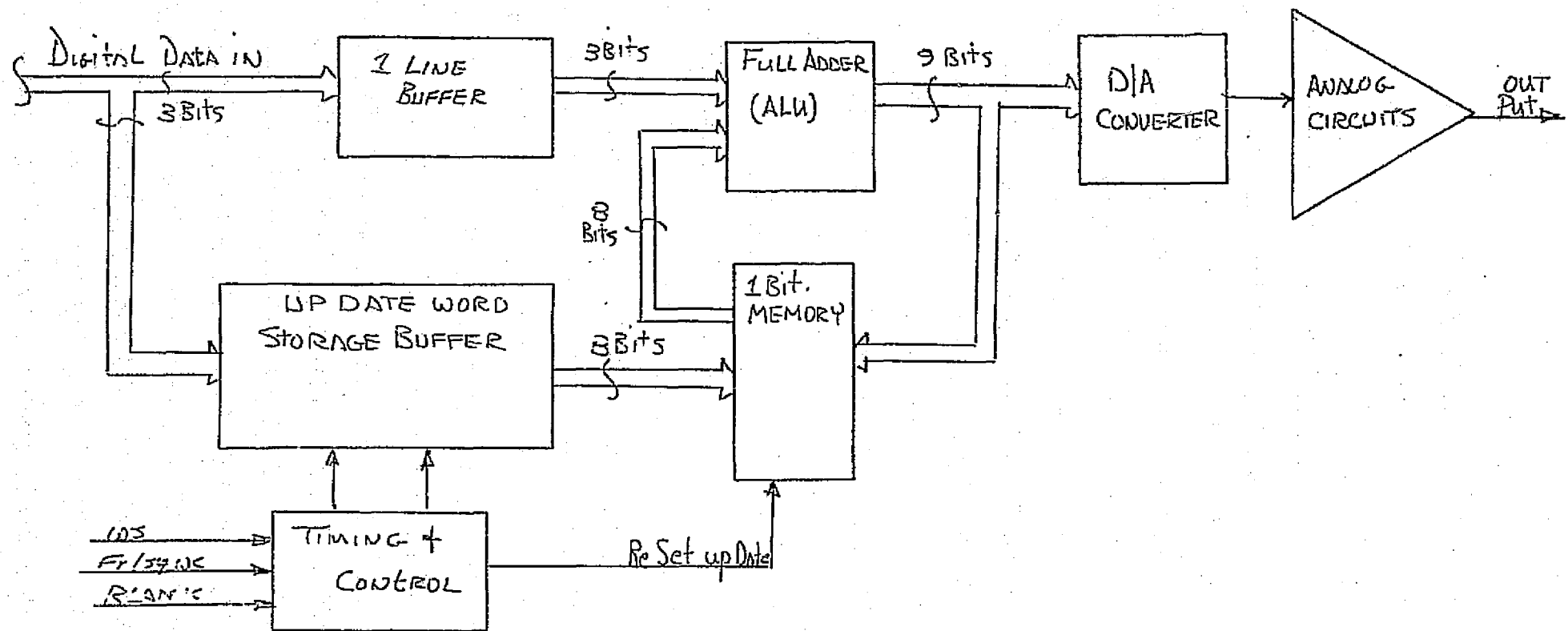
FIG 4.11   Delta Demod For UP-LINK · DownLink Data

5.0   MEMORY DESIGN DESCRIPTION

5.1   Block Diagram Description Of The Final Design

The two memories are packaged on six wire-wrap cards. The associated data selectors and interfaces are packaged on the remaining two cards.

One memory provides dynamic storage of the three-bit coded video data for a delay of one vertical field. The second memory is cascaded from the first for a two-field delay. The current video data, the one-field delayed and the two-field delayed data provide simultaneous access to three sequential color fields.

The coded three-bit video data is converted into three 16-bit words by serial-to-parallel shift-registers to reduce the access time required by the MOS memories. The actual shift rate of each MOS device is further reduced by multiplexing the data 5:1. This action reduces the power consumption in the memory to acceptable levels. Each memory is implemented with 2048-bit MOS dynamic shift registers in an 16 X 5 array per input bit. The shift rate during active lines is 76.8 kHz (See Figure 5-1).

Three data selectors sort the current video data and the memory data into red, blue and green color data. The data selectors are controlled by the field address from the timing and sync card. Due to the cascading process in the two memories, the input sequential color reappears with a one-field and then with a two-field delay. The data selectors provide simultaneous output for each color, by routing the data from the memories as it reappears. The data from the data selectors is converted to three-bit video data by serial to parallel converters.

5.2   Timing Description

The two field delay memories store digitized video data sequentially for one television field each. The data selectors generate parallel color data from the current video data and the data from the two memories. Thus, the three outputs from the data selectors contain information from both the even and odd fields of the television frame. In order for parallel color video to be registered

properly the output of the memories has to be aligned such that
the odd and even field video overlay exactly. This alignment
is accomplished by clocking the memory in such a manner that the
first digitized video sample of the first full horizontal line
appears at the outputs of the memories at the same time regard-
less whether the digitized video originated from an odd or even
field. (See Figure 5-2)

The incoming video is digitized at 640 samples per horizontal
line. Each field consists of 245 active lines plus vertical re-
trace of 17.5 lines. The required memory cells to store one field
of video is 245 X 640 = 156800 cells per bit of encoded data.

The memory is organized with 2048 bit shift-registers in an
16 X 5 array for 2048 X 16 X 5 = 163840 memory cells.

Each bit of the digitized date from the Delta Modulator is
converted to 16 bit parallel words. Each list of the 16 bit words
is sequentially stored in one of five 2048 bit shift-registers.
To store this data for one field 156800 ÷ 16 = 9800 shift-pulses
have to be supplies to the memory. The storage cells in excess
of the required number are 163840 - 156800 = 7040. These cells
are shifted during vertical retrace by 7040 ÷ 16 = 440 shift-pulses
to provide dynamic refresh and position the data for the start of
the next field.

The input video data is encoded with standard Sync for 525
line television. This sync produces a 2:1 interlaced raster with
the start of the even field delayed by one half line with respect
to the start of the odd field. The output data selectors use odd
and even field data simultaneously to generate the parallel color
video. Thus, the data applied to the data selectors from the memories
has to be aligned such that each field starts at the same time re-
gardless whether the input originated in the odd or even field.
This alignment is accomplished by delaying the start of vertical
sync for the even field by one-half line. The modified raster
parameters, as far as the memory is concerned, are now as follows:

5.2   <u>Timing Description   (continued)</u>

                Odd Field (18 lines retrace +245 lines video) plus

                Even Field (17 lines retrace +245 lines video)

                For a Total of 525 Lines (see Figure   ).

The 9800 active video shift clocks are used identically for both the odd and even fields. However, the 440 dynamic refresh shift clocks are distributed as follows:

      Odd Field: 14 lines X 20 clocks plus 4 lines X 40 clocks =
                    440 Clocks

      Even Field: 12 lines X 20 Clocks plus 5 lines X 40 Clocks =
                    440 Clocks

This method of storing and shifting the video data through the field delay memories assures that the output parallel video data is registered properly.
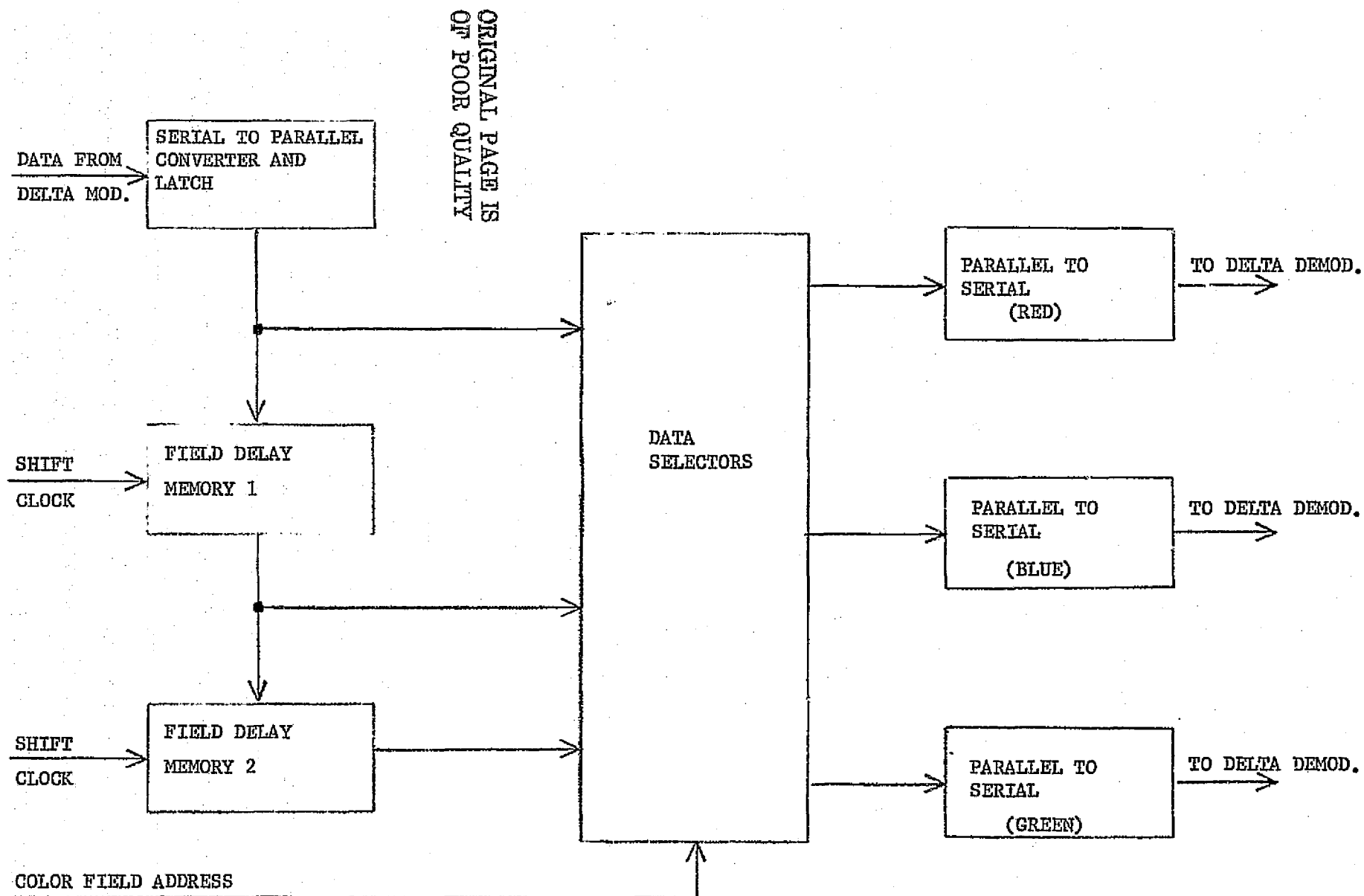
FIGURE 5-1
DELAY MEMORIES, BLOCK DIAGRAM

ONE FRAME

VERTICAL
RETRACE

ODD   FIELD

VERTICAL
RETRACE

EVEN
        FIELD

18 LINES
440 SHIFT CLOCKS

245 LINES
9800 SHIFT CLOCKS

17 LINES
440 SHIFT CLOCKS

245 LINES
9800 SHIFT CLOCKS
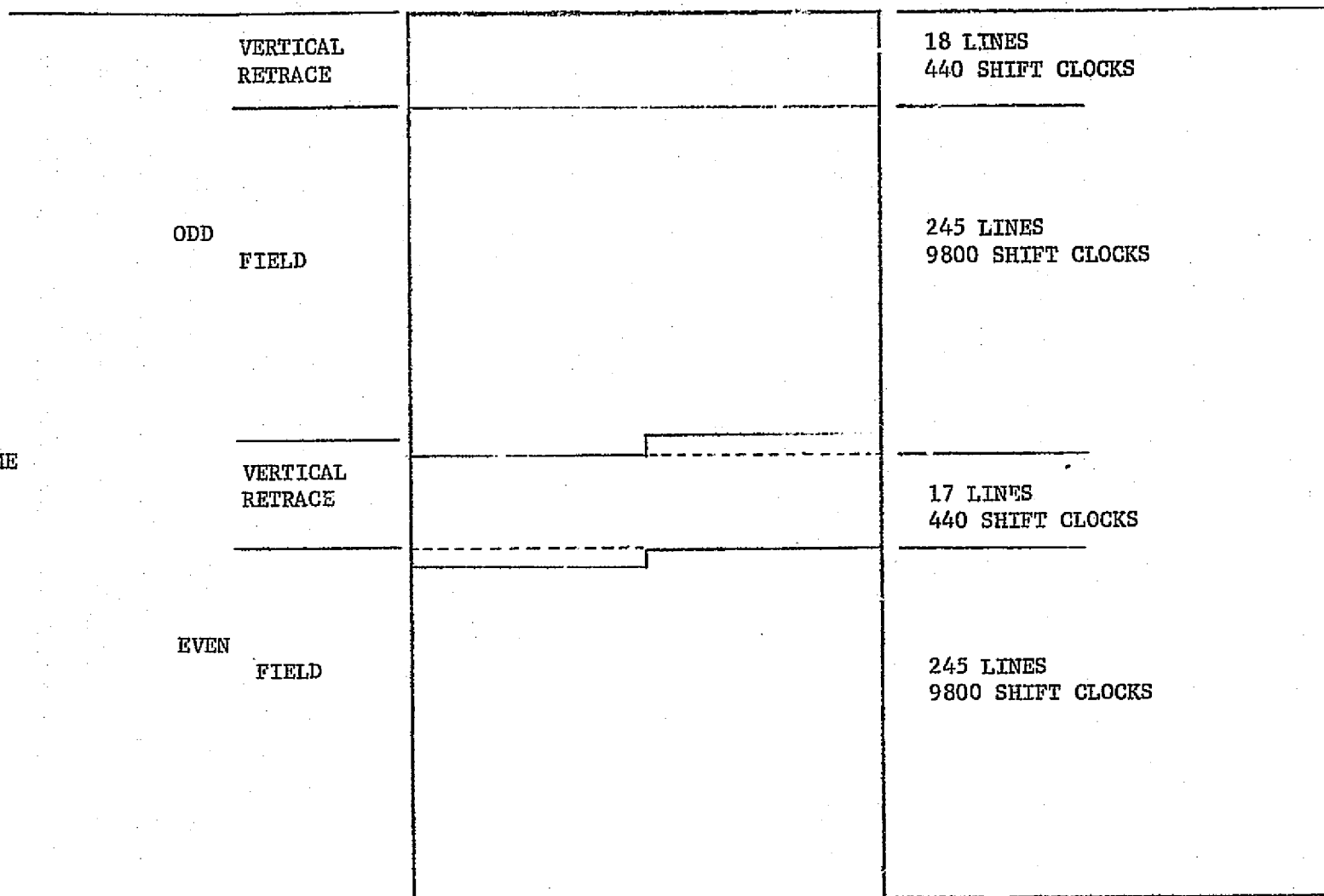
FIGURE 5-2

MEMORY SHIFT CLOCK DISTRIBUTION FOR ONE FRAME

6.0   TIMING AND SYNC

6.1   Block Diagram Description

        The Timing and Sync functions include the sync separator, sync
regeneration, video data, sampling timing and the memory shift
clocks. (See Figure 6-1)

        All the timing signals derive from a 24.5454 MHz crystal oscil-
lator. The clock distribution network generates the 12.27 MHz
sampling clocks for the Delta Modulator, Demodulators, the sync
counters and the memory serial to parallel and parallel to serial
registers.

        The active video counter counts 640 sampling clocks for every
horizontal line. The output of this counter is decoded by the
memory timing generator to provide the memory shift-register clocks
and the parallel to serial and serial to parallel converters. At
the end of the active video the horizontal retrace counter is en-
abled. This counter counts 132 Sampling Clocks and is synchronized
to the horizontal sync pulse detected by the sync separator from the
composite video. The output of both horizontal counters are decoded
and output blanking pulses to the Delta Modulator/Demodulators. These
pulses synchronize the start of conversion in the Delta Modulator/
Demodulators with the Field Delay Memory. The horizontal counters
also output two equally spaced pulses for every horizontal line to
the vertical counter. The vertical counter counts 525 half lines
or 262.5 horizontal lines for every field which is necessary to gen-
erate the vertical sync for a 2:1 interlaced raster. The vertical
counter is synchronized to the vertical sync pulse from the sync
separator.

        The sync regeneration circuits decode the horizontal and verti-
cal counters and assemble the composite sync and blanking. The out-
put sync is delayed 1.96 uSec. from the input sync to compensate for
the processing delays through the memory.

A modulo 3 counter is the color field address generator. This counter tracks the color fields of the input sequential video and controls the data selectors in the memory for the output synthesis. The field address counter is advanced during vertical retrace and is reset when the color sync during line 18 of the green field is detected.

6.2   Timing Description

Table 6-1 shows the measured pulse widths of the output composite sync and blanking. All parameters meet EIA specification RS170 for 525 line composite sync.

Figure 6-2 is a timing diagram of the synchronization between the Delta Modulator, the Field Delay Memory and the Delta Demodulators. Point A on the timing diagram is the start of the active video on a horizontal line. For the first four sampling clocks (A to B) the Delta Modulator outputs zero reference level data. The serial to parallel shift-register in the memory converts every 16 inputs from the Delta Modulator, starting at A, to 16 bit parallel word. This 16 bit word is stored in a register and then written into the first memory at the trailing edge (G) of the memory one shift clock. The 16 bit word which has been stored for one field, is read out of the first memory at F and written into the second memory at J. The current video data, stored in a register at C, the one field delayed data, read out of memory one at F, and the two field delayed data, read out of memory two at H, are routed through the data selectors and loaded into the parallel to serial shift-registers at D. Data output from the memory to the Delta Demodulators starts at D. The first four bits of the output data (D to E) are the zero reference for the Delta Demodulators. The interval between A and D is the processing delay through the memory.
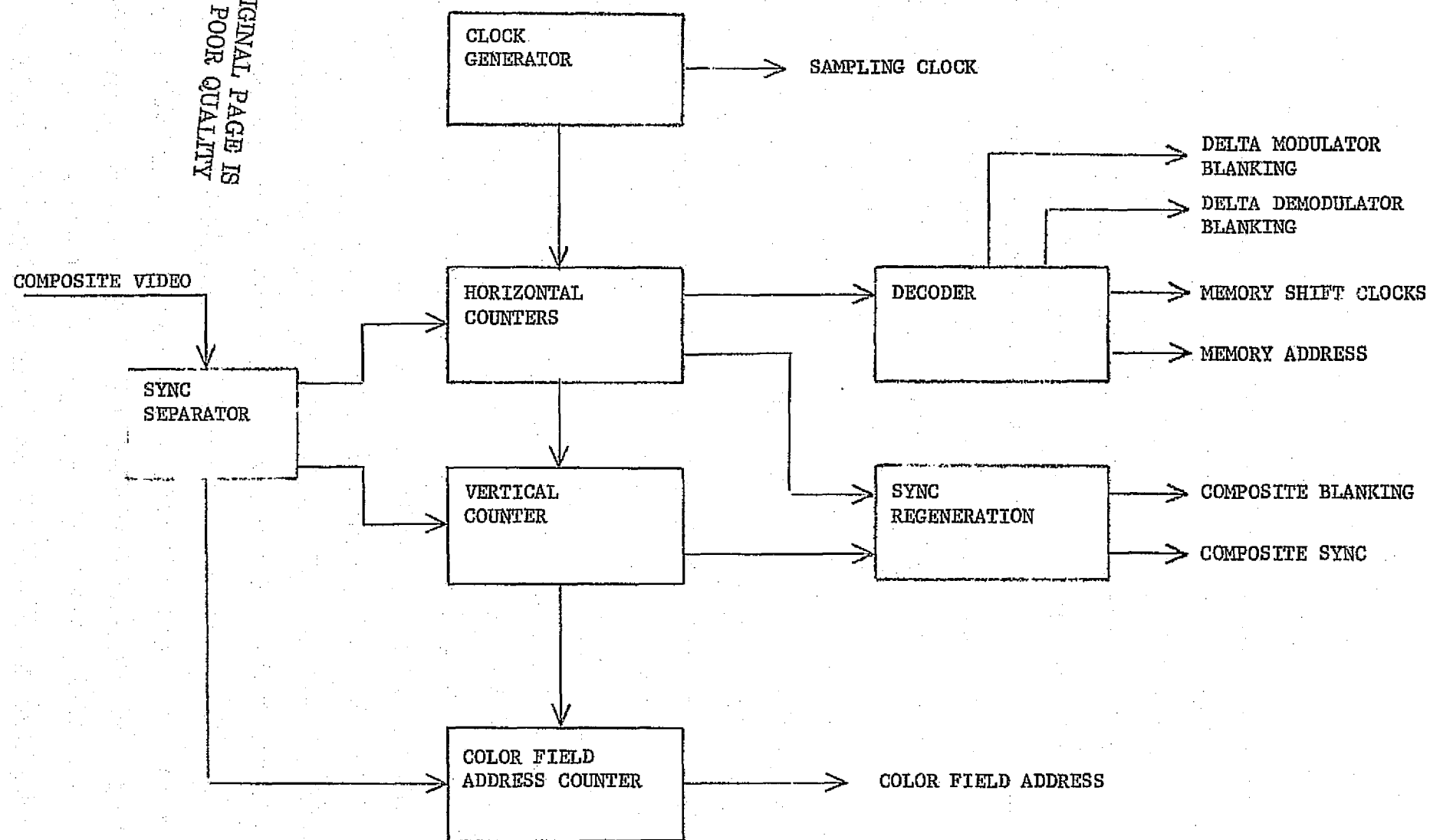
FIGURE 6-1

TIMING AND SYNC BLOCK DIAGRAM

TABLE 6-1

STP HORIZONTAL SYNC PARAMETERS

	EIA RS 120 SPECIFICATION	STP
Horizontal Interval	H	62.9 µsec.
Blanking	.178 H max. = 11.2 µsec.	10.76 µsec.
Horizontal Sync	.075 H $\pm$ .005 H = 4.718 µsec. $\pm$ .315 µsec.	4.89 µsec.
Front Porch	.02 H min. = 1.26 µsec.	1.47 µsec.
Back Porch	.065 H min. = 4.09 µsec.	4.73 µsec.
Equalization Pulses	.45 H Sync to .5 H sync = 2.2 µsec. to 2.45 µsec.	2.45 µsec.
Vertical Sync Pulses	.5 H - (.07 H $\pm$ .01 H) = 27.67 µsec. to 36.48 µsec.	35.53 µsec.

SAMPLING CLOCK

HORIZONTAL ACTIVE VIDEO
ENABLE

DELTA MODULATOR
UNBLANKING

SERIAL TO PARALLEL REGISTER
LOAD PULSE

PARALLEL TO SERIAL REGISTER
LOAD PULSE

DELTA DEMODULATOR
UNBLANKING

MEMORY 1 SHIFT CLOCK

MEMORY 2 SHIFT CLOCK
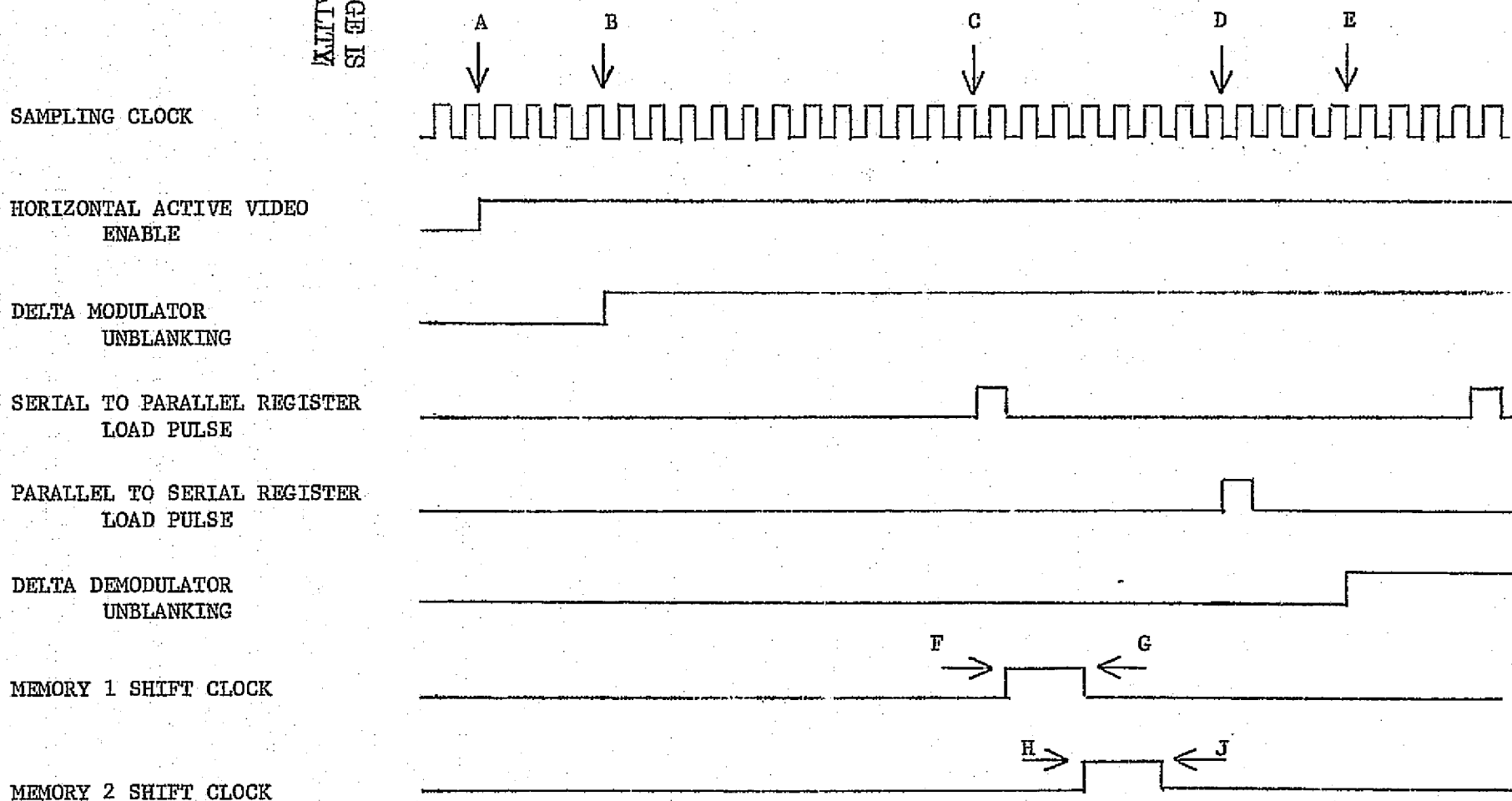
FIGURE 6-2

STP SYNCHRONIZATION TIMING DIAGRAM

7.0 RELIABILITY ANALYSIS

It is important to asses the reliability of a spacecraft packaged version of the STP Converter. The breadboard design that was completed and delivered was used as a baseline to compute the estimated reliability performance of the STP Converter.

It is assumed that a different reliability philosphy is appropriate for equipment planned for the Space Shuttle program than for conventional long life unmanned space equipment. The assumed philosphy is that the typical mission life is short (168 hours) and that repairability even limited on orbit repairs are not excluded. To this end the basic single thread probability of survival (no redundancy or degraded modes of operation permited) for a 168 hour mission is of interest.
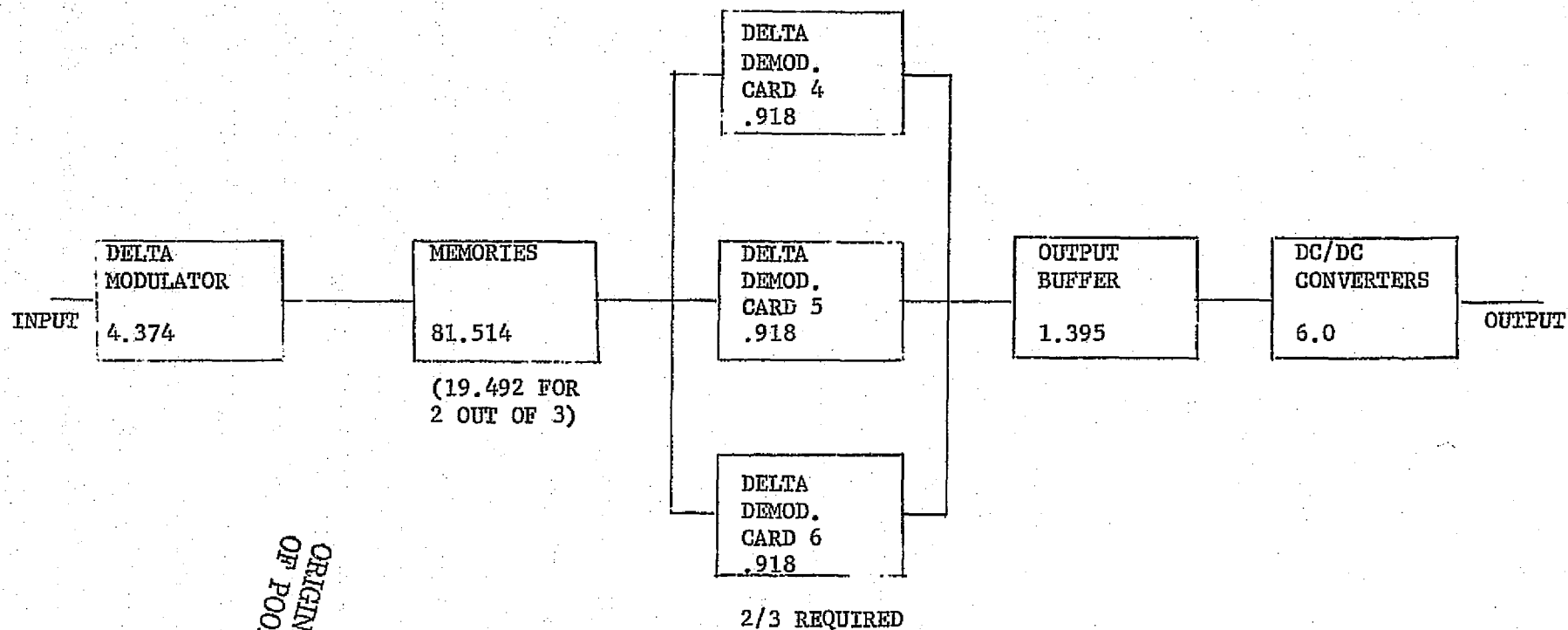
Figure 7-1 is the Reliability Configuration block diagram used for the reliability analysis of the STP Converter. The failure rate in failure per 10^6 hours for each block are included in each block. Table 7-1 is the back-up data containing the total part counts and failure rate for each block shown in Figure 7-1.

Inspection of Figure 7-1 indicates that the single thread failure rate of the memories at 81.514 failure per million hours dominates the total single thread failure rate of 96.037 failures/10^6 hours.

Using the single thread failure rate of 96.037 F/10^6 hours results in a reliability of 0.984 for a 168 hour mission. This number may not be sufficiently large. A number of approaches may be used to improve this number. The most obvious first approach would be to include a single redundant memory card or to allow the system to degrade to a 2 Bit rather than a 3 Bit Delta Modulator system in the event of a memory or a single Delta Demodulator failure. In either case, the reliability by this single cost effective measure is improved to 0.995 for a 168 hour mission. This may be adequate, if not additional redundancy may be applied to improve the reliability even further.

```
                              ┌──────────────┐
                              │ DELTA        │
                              │ DEMOD.       │
                              │ CARD 4       │
                              │ .918         │
                              └──────────────┘

┌──────────────┐  ┌──────────────┐  ┌──────────────┐  ┌──────────────┐  ┌──────────────┐
│ DELTA        │  │ MEMORIES     │  │ DELTA        │  │ OUTPUT       │  │ DC/DC        │
│ MODULATOR    │  │              │  │ DEMOD.       │  │ BUFFER       │  │ CONVERTERS   │
INPUT │        │  │              │  │ CARD 5       │  │              │  │              │  OUTPUT
│ 4.374        │  │ 81.514       │  │ .918         │  │ 1.395        │  │ 6.0          │
└──────────────┘  └──────────────┘  └──────────────┘  └──────────────┘  └──────────────┘
                   (19.492 FOR
                   2 OUT OF 3)

                              ┌──────────────┐
                              │ DELTA        │
                              │ DEMOD.       │
                              │ CARD 6       │
                              │ .918         │
                              └──────────────┘
```

2/3 REQUIRED

TOTAL F/R 96.037 / 10^6 HOURS

FUNCTIONAL F/R 30.858 / 10^6 HOURS (2/3 REQUIRED)

RELIABILITY FOR 168 HOUR MISSION:

R_2 = .984

R_2 = .995 (1 REDUNDANT MEMORY CARD)

FIGURE 7-1

RELIABILITY CONFIGURATION BLOCK DIAGRAM

Part Stress and Failure Rate

Ckt Ref	Component-Description	QTY.	Stress Ratio	Failure Rate – F/10^6 Hours		
				k	λ	Total
	SA1					
	Transistors, G.P.	4			.008	.032
	Transistors, FET	1			.035	.035
	Resistors, Film or Comp.	19			.002	.038
	Capacitors, Ceramic	13			.002	.026
	Capacitors, Tant.	2			.001	.002
	Coils	2			.005	.010
	Diode Array	1			.010	.010
	SUBTOTAL					.153
	A1					
	Transistors, G.P.	12			.008	.096
	Resistors, Film or Comp.	28			.002	.056
	Capacitors, Ceramic	12			.002	.024
	Capacitors, Tant.	2			.001	.002
	A1 SUBTOTAL					.178
	Resistor, Film or Comp.	3			.002	.006
	Connectors, BNC	2			.040	.080
	SUBTOTAL FOR ABOVE					.417
	Above Circuit	3				1.251
	Above Circuit	2 Out of 3				0
	COMMON PARTS					
	Transistors, G.P.	3			.008	.024
	Resistors, Film or Comp.	7			.002	.014
	Capacitors	3			.002	.006
	Connectors, BNC	2			.040	.080
	Connector, Card	1			.020	.020
	SUBTOTAL COMMON					.144
	2 Out Of 3					.144
	3 Out Of 3					1.395
	Memory Cards	6			10.337	62.022
	Timing & Sync Card	1			4.330	4.330
	Interface Card (Type C)	1			5.335	5.335
	Interface Card (Type D)	1			3.002	3.002
	Connectors, BNC	20			.040	.800
	Terminal Block	1			.010	.010
	Rectifiers, 1N2519	3			.005	.015
	DC/DC Converters	3			2.000	6.000
	TOTAL					81.514

If memory cards are 2/3 for success
then functional common is 19.492 for
balance of memory group.

Assembly Name		Amb. Temp.	k Factor	
STP FIELD DELAY MEMORIES SUBSYSTEM				**PHILCO** Ford
		Date		Philco-Ford Corporation Western Development Laboratories Division 3939 Fabian Way Palo Alto, California 94303
		2-13-75		

Assembly P/N			
	WDL-ST-A20400	Page	of

WDL—2940 B
11-72

Part Stress and Failure Rate

Ckt Ref	Component-Description	QTY.	Stress Ratio	Failure Rate – F/10^6 Hours		
				k	λ	Total
	Integrated Circuits, Digital	22			.050	1.100
	MOS IC's	90			.100	9.000
	DIP Resistors – 16 PIN	3			.008	.024
	DIP Capacitors – 16 PIN	5			.008	.040
	Resistors, Film or Comp.	25			.002	.040
	Diodes, 1N4001	20			.002	.040
	Capacitors, CK05	30			.002	.060
	Capacitors, M39003	3			.001	.003
	Connector, Card	1			.020	.020
	TOTAL					10.337

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Assembly Name	Amb. Temp.	k Factor	**PHILCO** Ⓕ
STP			Philco-Ford Corporation
MEMORY CARD	Date 2-13-75		Western Development Laboratories Division 3939 Fabian Way Palo Alto, California 94303

Assembly P/N		
	WDL-ST-A20400	Page of

Part Stress and Failure Rate

Ckt Ref	Component-Description	QTY.	Stress Ratio	Failure Rate – F/10⁶ Hours		
				k	λ	Total
	Integrated Circuits, Digital	79			.050	3.950
	Integrated Circuits, Linear	2			.050	.100
	DIP Resistors	5			.008	.040
	Oscillator	1			.020	.020
	Resistors, Film or Comp.	40			.002	.080
	Capacitors, CK05	35			.002	.070
	Capacitors, M39003	4			.001	.004
	Diodes, Si, L. Power	7			.002	.014
	Transistors, NPN, 3 W	2			.008	.016
	Transistors, PNP, 3 W	2			.008	.016
	Connector, Card	1			.020	.020
	TOTAL					4.330

Assembly Name		Amb. Temp.	k Factor	**PHILCO** *Ford*
STP				Philco-Ford Corporation
TIMING & SYNC CARD		Date 2-13-75		Western Development Laboratories Division 3939 Fabian Way Palo Alto, California 94303

Assembly P/N			
	WDL-ST-A20400	Page of	

Part Stress and Failure Rate

Ckt Ref	Component-Description	QTY.	Stress Ratio	Failure Rate – F/10⁶ Hours		
				k	λ	Total
	Integrated Circuits, Digital	103			.050	5.150
	DIP Resistors	14			.008	.112
	Capacitors, CK05	25			.002	.050
	Capacitors, M39003	3			.001	.003
	Connector, Card	1			.020	.020
	TOTAL					5.335

Assembly Name		Amb. Temp.	k Factor	PHILCO Ford
STP INTERFACE CARD (TYPE C)		Date 2-13-75		Philco-Ford Corporation Western Development Laboratories Division 3939 Fabian Way Palo Alto, California 94303
Assembly P/N	WDL-ST-A20400		Page of	

WDL—2940 B
11-72

Part Stress and Failure Rate

Ckt Ref	Component Description	QTY.	Stress Ratio	Failure Rate – F/10^6 Hours		
				k	λ	Total
	Integrated Circuits, Digital	57			.050	2.850
	DIP Resistors	10			.008	.080
	Capacitors, CK05 Type	25			.002	.050
	Capacitors, M39003 Type	2			.001	.002
	Connector, Card	1			.020	.020
	TOTAL					3.002

Assembly Name		Amb. Temp.	k Factor	PHILCO 〈Ford〉
STP INTERFACE CARD (TYPE D)		Date 2-13-75		Philco-Ford Corporation Western Development Laboratories Division 3939 Fabian Way Palo Alto, California 94303
Assembly P/N	WDL-ST-A20400		Page of	

WDL—2940 B
11-72

Part Stress and Failure Rate

Ckt Ref	Component-Description	QTY.	Stress Ratio	Failure Rate – F/10⁶ Hours		
				k	λ	Total
	FILTER & BUFFER					
	Transistors, G.P.	7			.008	.056
	Diodes, Zener	1			.010	.010
	Resistors, Film or Comp.	21			.002	.042
	Capacitors, Ceramic	8			.002	.016
	Capacitors, Tantalum	3			.001	.003
	Coils	2			.005	.010
	SUBTOTAL					.137
	AC					
	Transistors, G.P.	2			.008	.016
	Integrated Circuit	1			.050	.050
	Diodes	5			.002	.010
	Diode Array	1			.010	.010
	Resistors, Film or Comp.	10			.002	.020
	Capacitors, Ceramic	5			.002	.010
	SUBTOTAL					.116
	A1	1			.178	.178
	SY1	1			.176	.176
	OTHER					
	Integrated Circuit	1			.050	.050
	Transistor	1			.008	.008
	Diode, Zener	1			.010	.010
	Resistors	8			.002	.016
	Capacitors, Ceramic	3			.002	.006
	Capacitors, Tantalum	3			.001	.003
	Connectors, BNC	2			.040	.080
	Connectors, Card	1			.020	.020
	SUBTOTAL					.193
	TOTAL					.800

Assembly Name	Amb. Temp.	k Factor	**PHILCO** 🅕
STP CARD 2	Date 2-13-75		Philco-Ford Corporation Western Development Laboratories Division 3939 Fabian Way Palo Alto, California 94303
Assembly P/N WDL-ST-A20400		Page of	

Part Stress and Failure Rate

Ckt Ref	Component-Description	QTY.	Stress Ratio	Failure Rate – F/10^6 Hours		
				k	λ	Total
	DAC					
	Connector	2			.020	.040
	Connector, BNC	1			.040	.040
	Integrated Circuit	1			.050	.050
	Resistors	3			.002	.006
	Capacitors, Ceramic	2			.002	.004
	Capacitors, Tantalum	2			.001	.002
	SUBTOTAL					.142
	B1 BUFFER AMP.					
	Transistors	2			.008	.016
	Resistors, Film or Comp.	8			.002	.016
	Capacitors, Ceramic	4			.002	.008
	Capacitors, Tantalum	2			.001	.002
	SUBTOTAL					.042
	PIGGYBACK BOARD					
	Integrated Circuits	17			.050	.850
	Resistors, Film or Comp.	55			.002	.110
	SUBTOTAL					.960
	TOTAL					1.144

Assembly Name	Amb. Temp.	k Factor	**PHILCO** (Ford)
STP			Philco-Ford Corporation
CARD 3B	Date		Western Development Laboratories Division
	2-14-75		3939 Fabian Way Palo Alto, California 94303

Assembly P/N		
	WDL-ST-A20400	Page of

Part Stress and Failure Rate

Ckt Ref	Component-Description	QTY.	Stress Ratio	Failure Rate – F/10^6 Hours		
				k	λ	Total
	Integrated Circuits	13			.050	.650
	Resistors, Film or Comp.	108			.002	.216
	D/A Converter	1			.184	.184
	TOTAL					1.050

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Assembly Name	Amb. Temp.	k Factor	**PHILCO** Ⓕ
STP			Philco-Ford Corporation
CARD 3C	Date 2-14-75		Western Development Laboratories Division 3939 Fabian Way Palo Alto, California 94303

Assembly P/N	WDL-ST-A20400	Page of

WDL—2940 B
11-72

Part Stress and Failure Rate

Ckt Ref	Component-Description	QTY.	Stress Ratio	Failure Rate – F/10⁶ Hours		
				k	λ	Total
	DAC & BUFFER AMPLIFIER	1			.184	.184
	Integrated Circuits	13			.050	.650
	Resistors, Film or Comp.	32			.002	.064
	Connector, Card	1			.020	.020
	TOTAL					.918

Assembly Name		Amb. Temp.	k Factor	**PHILCO** (Ford)
STP				Philco-Ford Corporation
DEMODULATOR		Date		Western Development Laboratories Division 3939 Fabian Way
CARDS 4 OR 5 OR 6		2-14-75		Palo Alto, California 94303
Assembly P/N	WDL-ST-A20400			Page of

8.0 PACKAGING RECOMMENDATIONS

The STP Converter electronics, as presently configured, could be packaged as shown in Fig. #1. This concept is compatible with the mechanical design requirements of North American Rockwell International Specifications for electronic equipment aboard the Space Shuttle.

The weight and volume estimates as shown on the face of the drawing represent gross estimates that are constrained by the power being dissipated. In the absence of definitive environmental criteria, further refinement of weight and volume cannot at this time be made.

To achieve these volumes, a packaging approach was selected that designs the electronics on standard multi-layer ceramic interconnect boards of approximately 3.0 inches high by 5 3/4 inches wide. These cards could then be plugged into predetermined slots in the housing for mechanical support and required heat transfer. The interconnection of these cards would be made by a harness or a multi-layer board at the bottom of the housing. Access to this housing or multi-layer board would be through a removable bottom cover.

The electronics come in basically three forms: standard I.C. flat packs; standard DIP packages; and discrete transistors, diodes, capacitors and resistors. The standard I.C. flat packs would be soldered directly to the 3 x 5.75 ceramic interconnect boards with the qualified DIP packages being handled the same. For the discrete parts, a standard 1 x 1 inch hybridized package could be used to minimize the packaging weight and volume. These 1 x 1 inch packages would then be soldered to the standard cards.

This will then result in a mechanical design that would minimize weight and volume while retaining maintainability and producibility features.
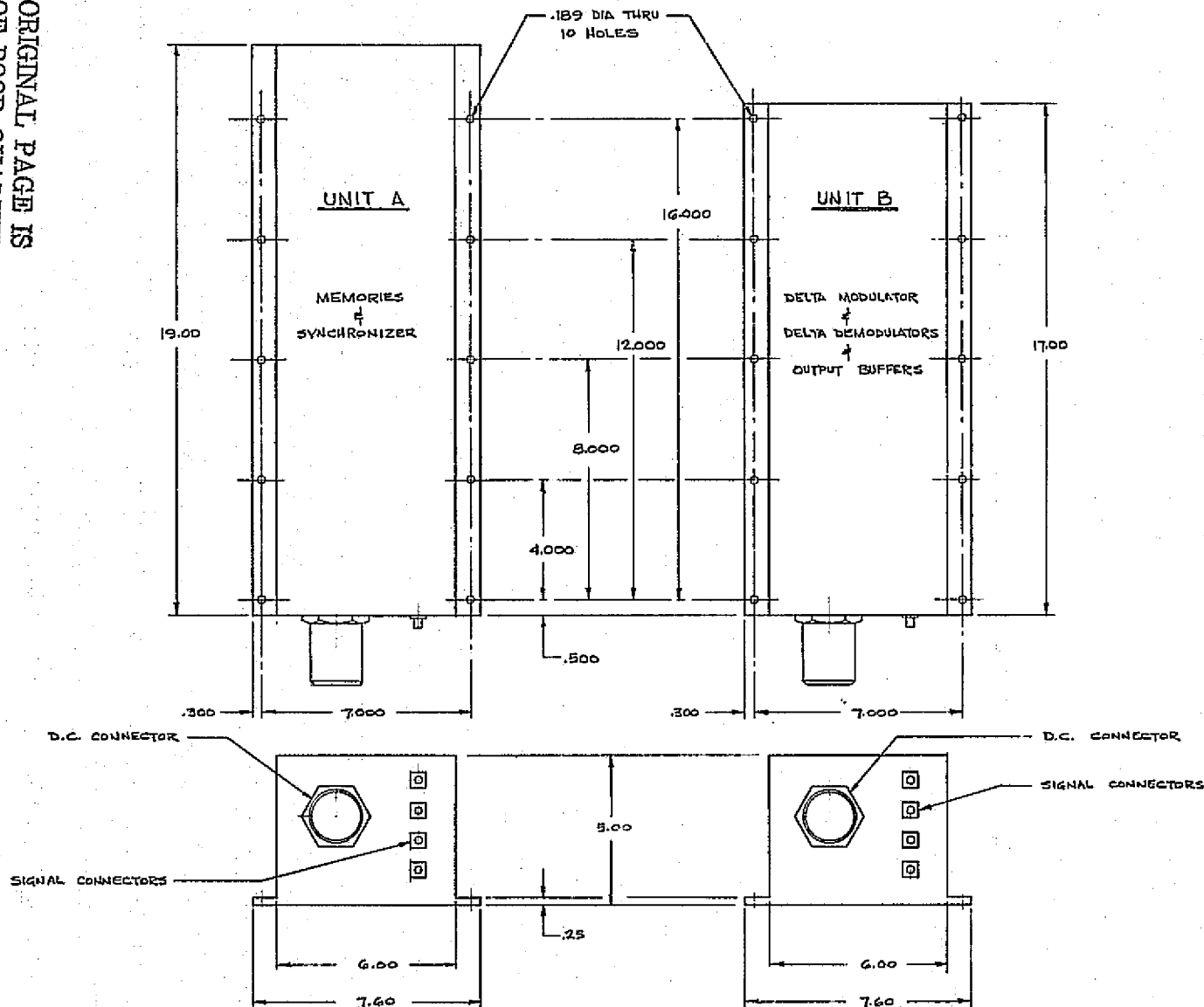
.189 DIA THRU
10 HOLES

UNIT A

MEMORIES
&
SYNCHRONIZER

UNIT B

DELTA MODULATOR
&
DELTA DEMODULATORS
&
OUTPUT BUFFERS

19.00

17.00

16.000

12.000

8.000

4.000

.500

.300   7.000   .300   7.000

D.C. CONNECTOR   D.C. CONNECTOR

SIGNAL CONNECTORS

5.00

.25

SIGNAL CONNECTORS

6.00   6.00

7.60   7.60

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. SPECIFICATIONS	UNIT A	UNIT B
BASE AREA	144 IN²	129 IN²
UNIT WEIGHT	15 LBS	13.4 LBS
UNIT VOLUME	577 IN³	516 IN³
POWER DISS.	20 W	62 W

FIGURE 8-1

DC/DC CONVERTERS

Power Supplies

Design Approach

The DC/DC converter requirements are effectively met by a design originally developed for the SMS program. This design is presently in production for the NATO III and GOES programs and is in orbital operation on the SMS spacecraft.

The design utilizes an inverter working from a preregulated bus. Feedback from the output transformer provides an error signal to the pulsewidth - modulated preregulator to maintain constant output voltage. Each converter is packaged in a T-frame module utilizing thickfilm techniques. Figure 1 illustrates this configuration.

The basis for this choice is:

a. Converter requirements are satisfactorily met by this design approach.

b. This choice has the advantage of being a proven flight tested design.

c. The thick-film packaging technique has produced demonstrated weight savings, assembly and test-time savings, and unit-to-unit uniformity.

d. Development time and schedule risk are both reduced.

Detailed Requirements

The converters must meet the following requirements:

a. Convert the primary bus voltage to the voltages required by the memory.

b. Provide regulation for line, load, and temperature variations.

c. Provide turnon current surge limiting, output overload current limiting, and overvoltage protection.

d. Isolate the using equipment from the input bus.

e. Filter the input bus voltages and reduce conducted interference fed to the bus.

f. Provide protection for the vehicle by preventing disablement of the input bus by a single component failure in a converter or in its load circuitry.

g. Maintain systems compatibility by careful consideration of EMC requirements.

Converter Operational Description

The converter is an inverter working from a preregulated bus with feedback to maintain regulation. Its various functional sections shown in Figure 2 are described in the following paragraphs.

Inverter

The inverter section consists of an astable multivibrator oscillator gating circuitry for the transformer drive transistors. Careful control of rise and fall times allows a maximum of efficiency.
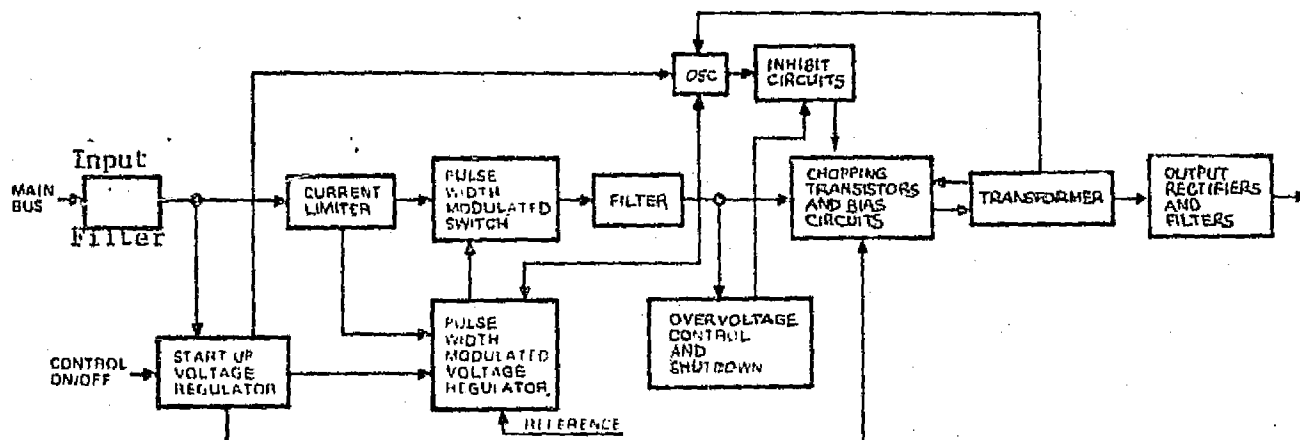
FIGURE 2
CONVERTER BLOCK DIAGRAM

PWM Regulator

The pulsewidth modulated (PWM) voltage regulator varies its pulsewidth with input voltage to maintain a constant output voltage. The regulator takes its feedback from an output of the transformer to stabilize the output voltages with variations in inverter, transistor, transformer, and load characteristics. The PWM regulator runs at twice the inverter frequency. The inverter is set to approximately 55 kHz. This allows effective output filtering with minimum component size.

Current Limiter

The current limiter circuit is located in the positive power line and is a peak detection type. The circuit senses the current in the power switch of the preregulator; this eliminates the possibility of shorts causing an unsensed overcurrent condition. The overcurrent circuit is a foldback type that provides lower current levels inside the converter during overload. Upon removal of the overcurrent condition, normal operation is automatically restored.

Overvoltage

The overvoltage control and shutdown circuit limits voltage overshoot conditions that might occur on the preregulated bus and all outputs to 120% of normal operating voltage. If the overvoltage was caused by a circuit malfunction or a component failure causing a loss of the control loop, the circuit will inhibit the inverter causing all output voltages to go to zero. In the event that the overvoltage condition is temporary, the circuitry automatically resets to normal operation.

Startup Regulator

The startup voltage regulator, which powers the control circuitry when the output voltages are low, is a linear regulator. The circuit is active only when the supply is turning on or when it is in current limit.

Output Filter

The output waveform is a full wave rectified square wave requiring a minimum of filtering. The requirement is easily handled by a single pi-section.

PREREGULATOR   INVERTER   FILTER

L1   T1   L2   Q1   T2   FILTER

COVER   R1 S.A.T.   Q2   Q3

FOAM

L1   L2   T2   FILTER

INPUT PINS   Q1   FRAME   OUTPUT PINS
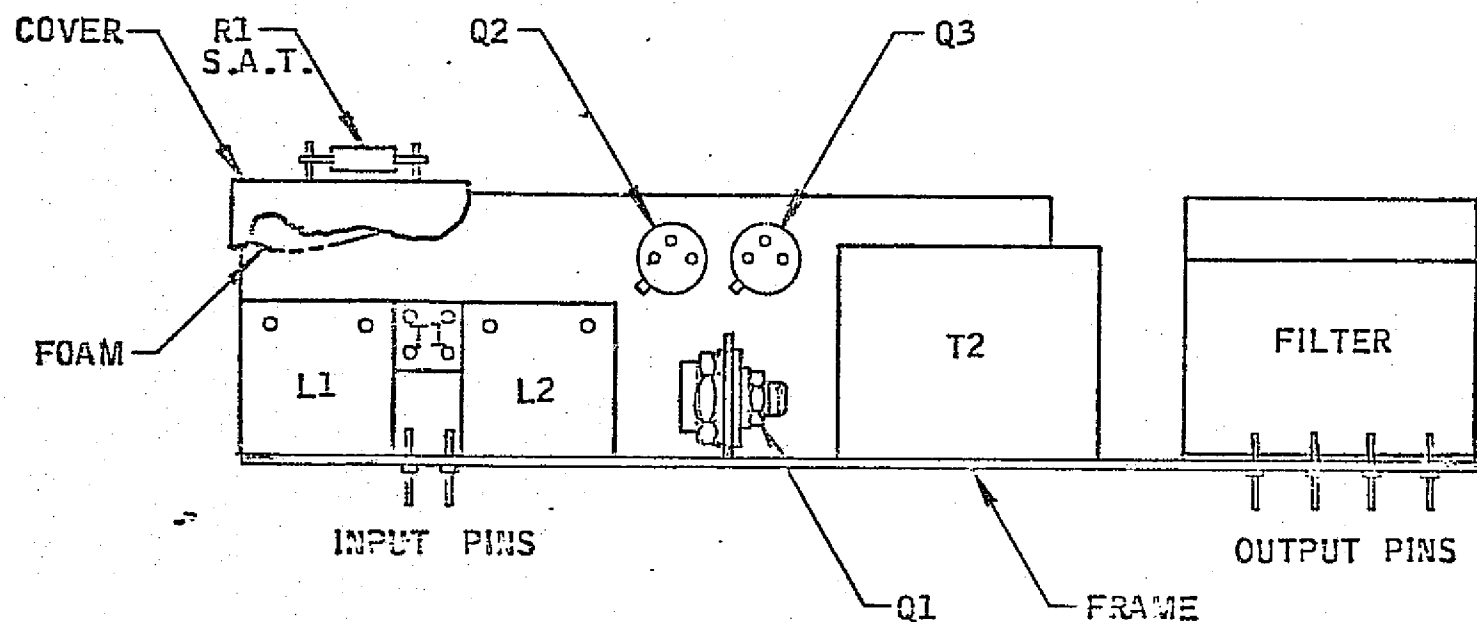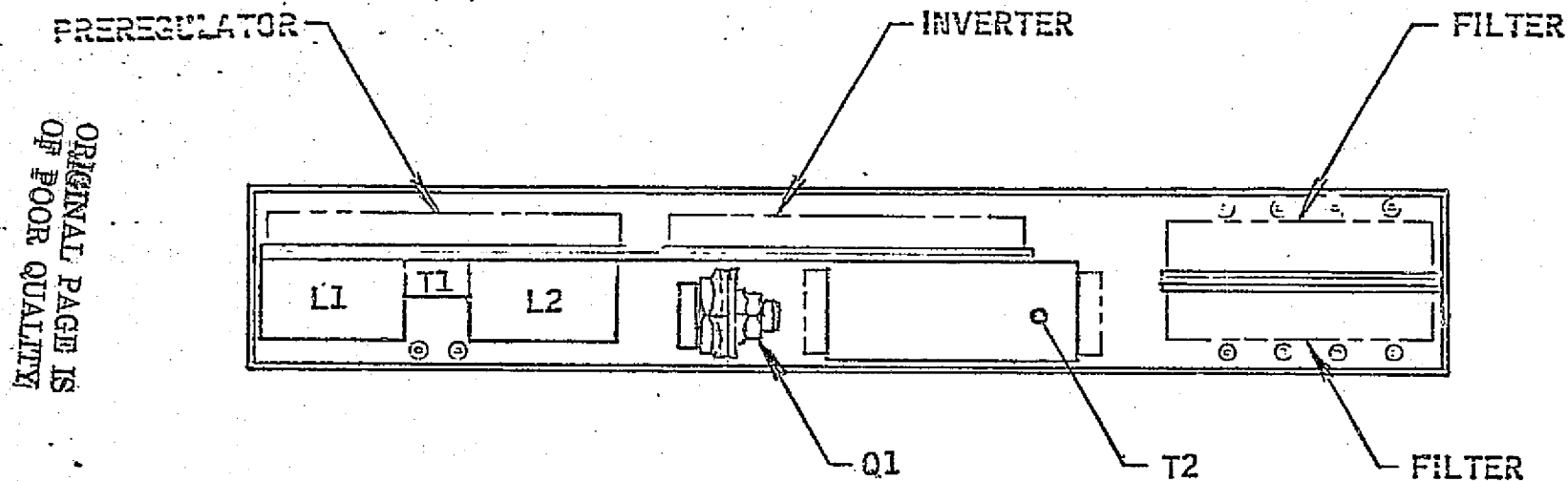
APPROXIMATE SIZE AND WEIGHT

.97" Wide x 1.4" High x 10" Long

0.7 Lbs.

DC/DC CONVERTER
"T" FRAME TYPE

FIGURE 1
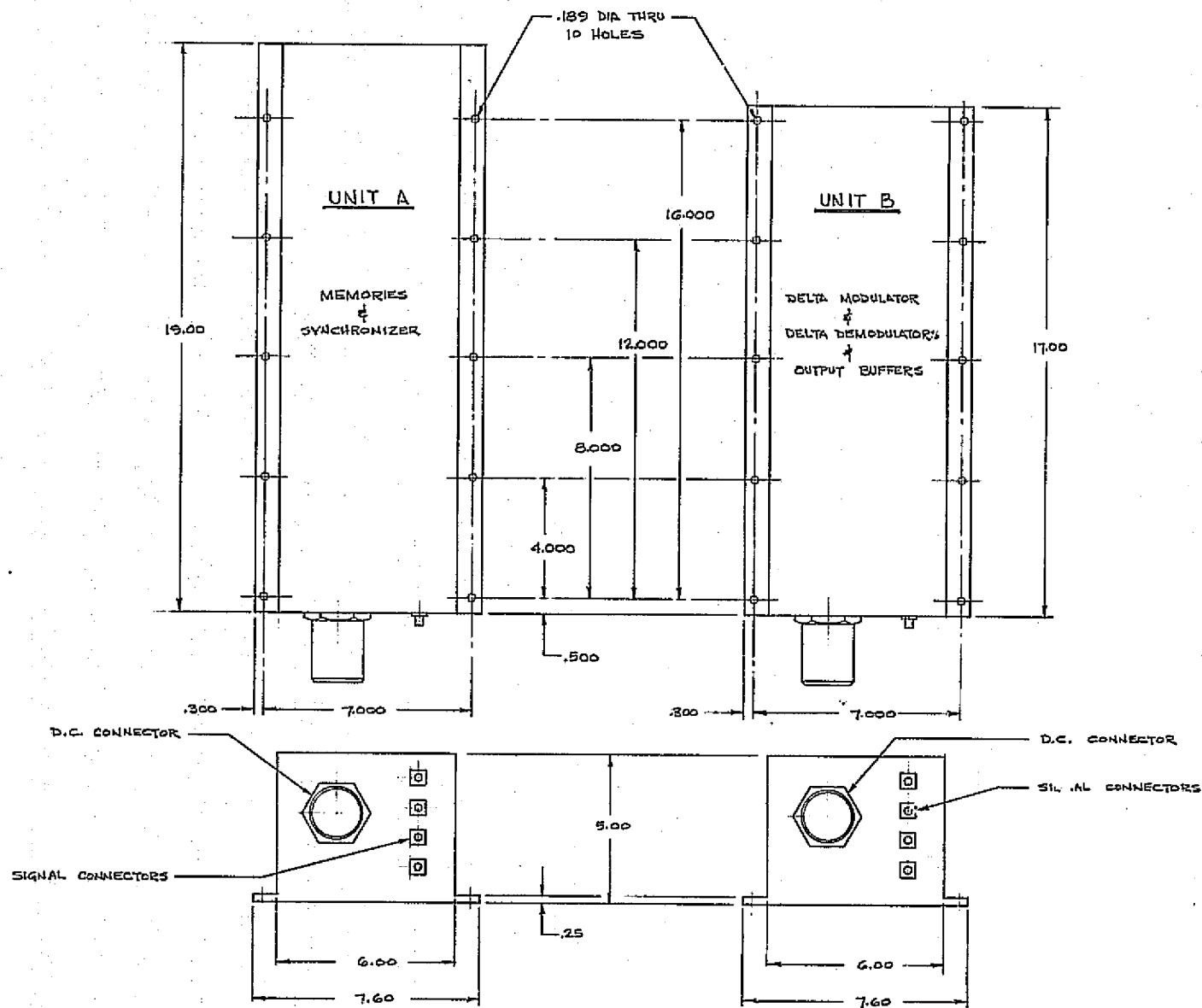
.189 DIA THRU
10 HOLES

UNIT A

MEMORIES
&
SYNCHRONIZER

UNIT B

DELTA MODULATOR
&
DELTA DEMODULATORS
&
OUTPUT BUFFERS

16.000

12.000

8.000

4.000

19.00

17.00

.500

.300   7.000

.300   7.000

D.C. CONNECTOR

D.C. CONNECTOR

SIGNAL CONNECTORS

SIGNAL CONNECTORS

5.00

.25

6.00

7.60

6.00

7.60

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. SPECIFICATIONS

	UNIT A	UNIT B
BASE AREA	144 IN²	129 IN²
UNIT WEIGHT	15 LBS	13.4 LBS
UNIT VOLUME	577 IN³	516 IN³
POWER DISS.	20 W	62 W

9.0   MEASURED PERFORMANCE

This section presents the measured results obtained using the STP converter breadboard that was delivered.

9.1   Test Results

Photos of Images Transmitted Through System. Photo 9-1 is of a 1956 Retma target that was transmitted through the STP converter. The camera and monitor were high resolution monochrome equipments capable of producing 800 TV lines resolution back to back. Focus of the monitor, however, was not constant across the field and maximum resolution can only be obtained at selected portions of the output image. In the case of photo 9-1, the monitor was focused to give maximum resolution for the horizontal resolution test widges at the lower half of the target. Observe that the horizontal resolution is almost 550 TV lines in contrast to the specification of 440 TV lines. The lack of maise and the excellent gray scale fidelity are also noteworthy.

Photo 9-2 is a similar image processed through the STP converter again by combining all three output channels. The image material consists of artist's concepts of the Space Shuttle which were selected to give a subjective evaluation of imagy processed by the STP converter.

9.2   Specification Comparison

Specifications compared to performance Table 9-1 is a chart comparing the specification of the STP converter to measured laboratory results using the breadboard converter. Note that all specifications are met or exceeded.

9.3   Delta Mod-Demod Signal Waveforms

Typical signal waveforms are shown in the following figures 9.1, 9.2. These signals were taken with a standard 10-step gray scale generator and are intended to show typical information wave forms.
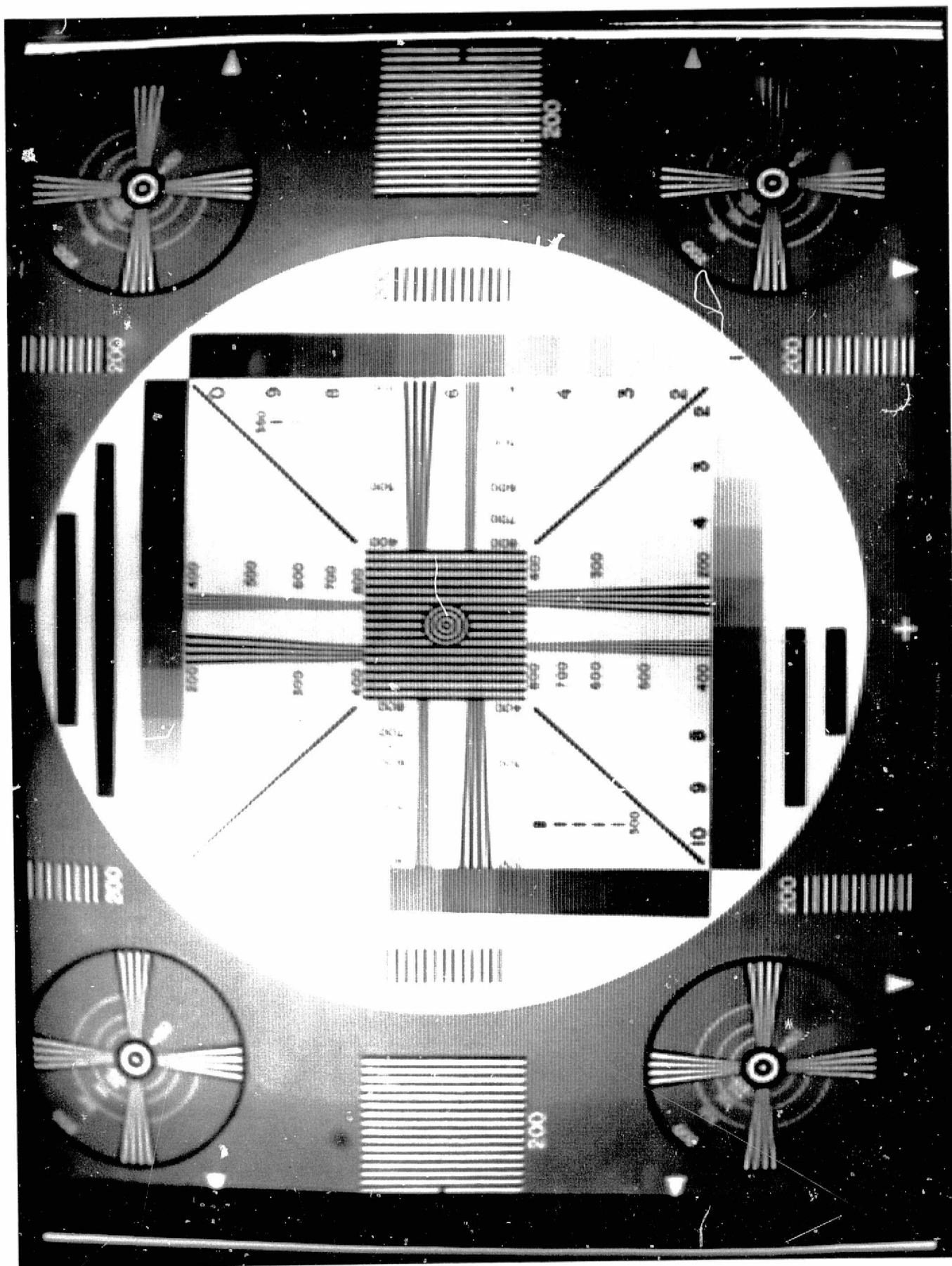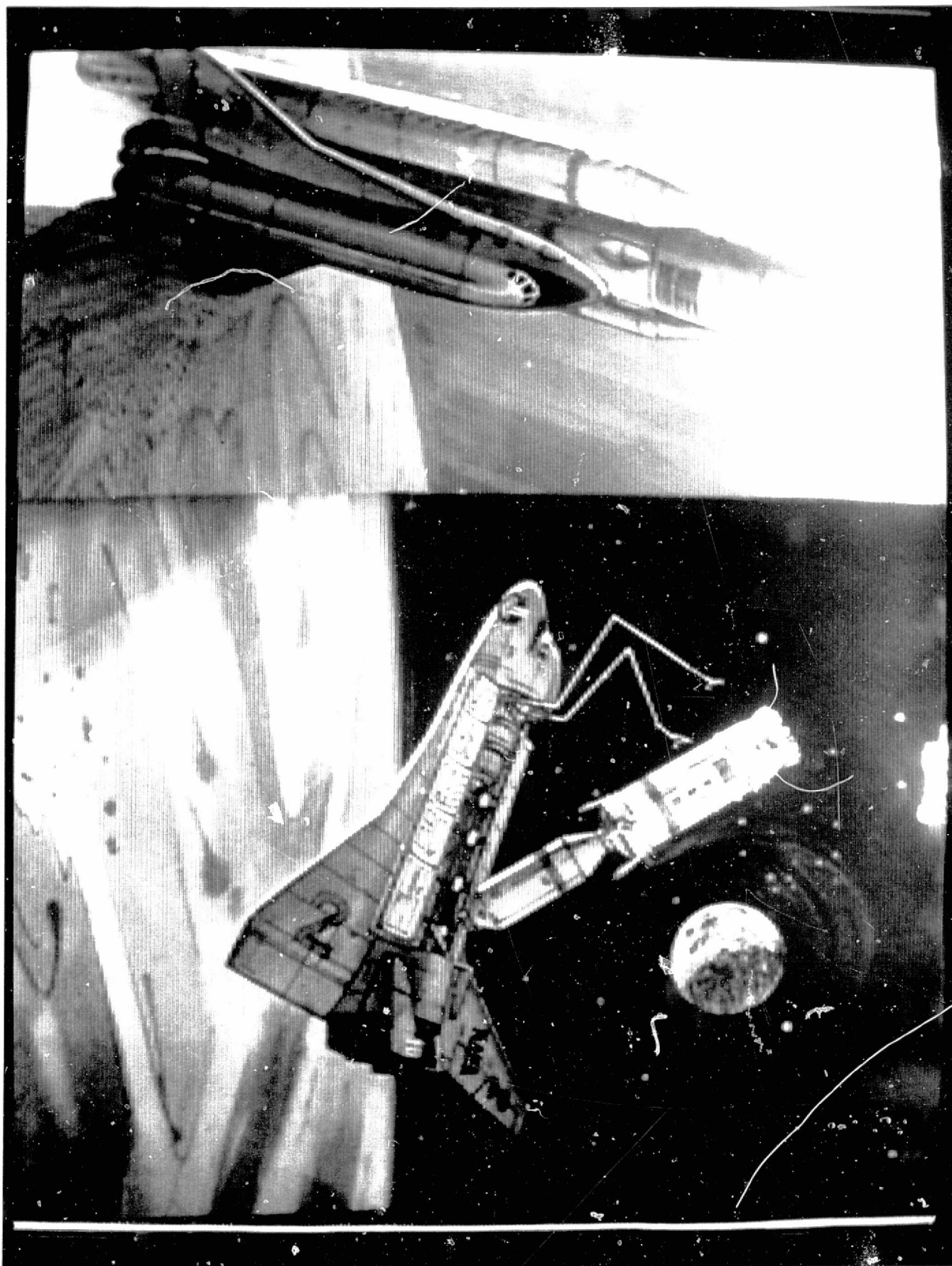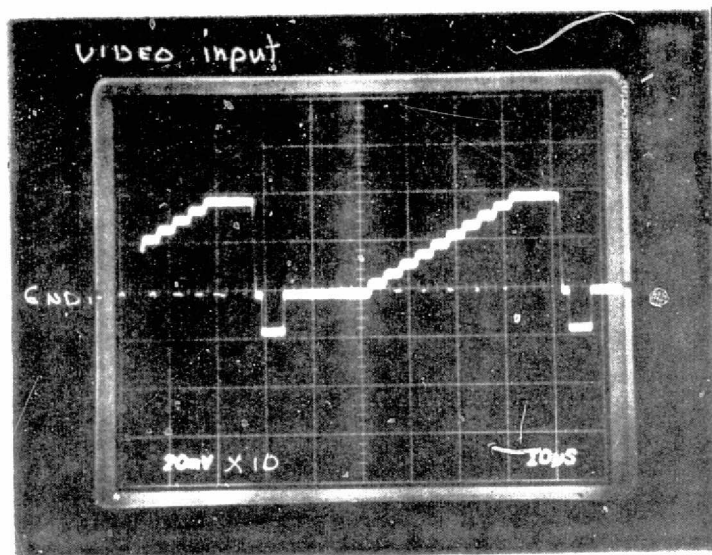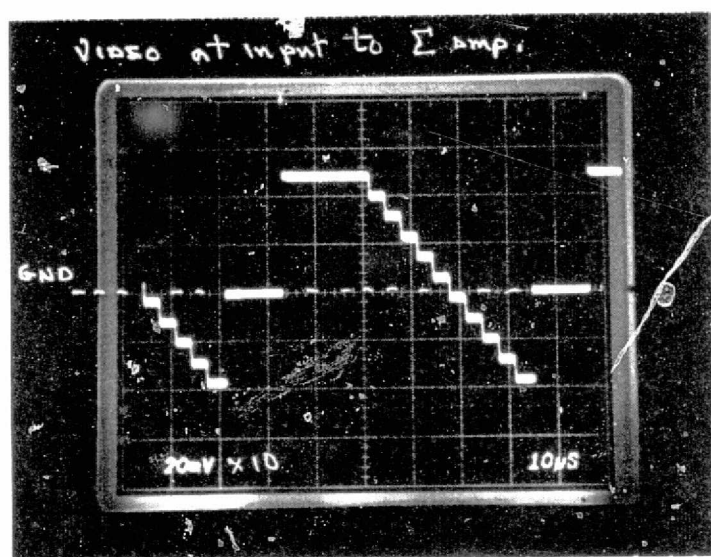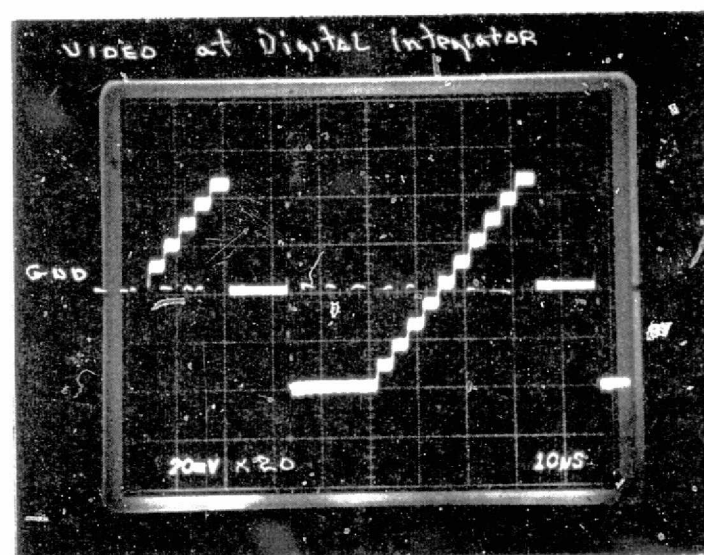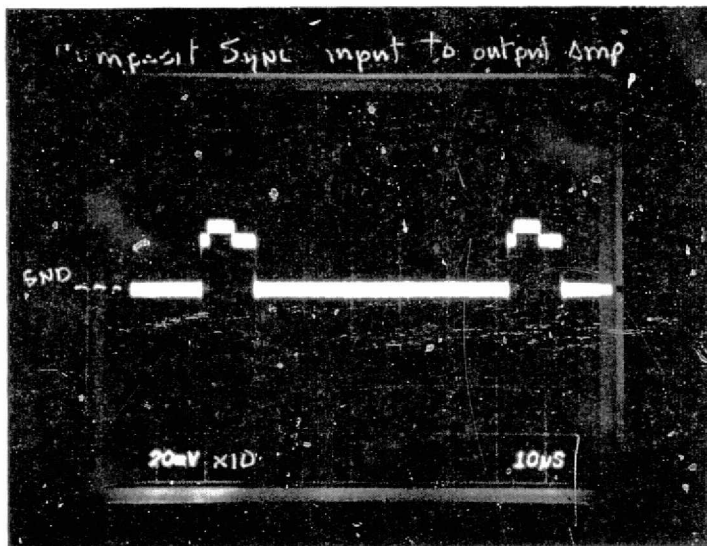
(A)   VIDEO INPUT TO DELTA MOD
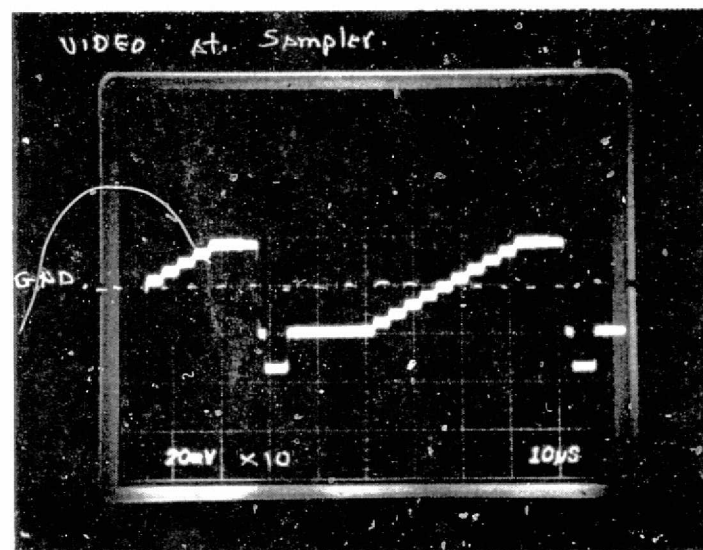
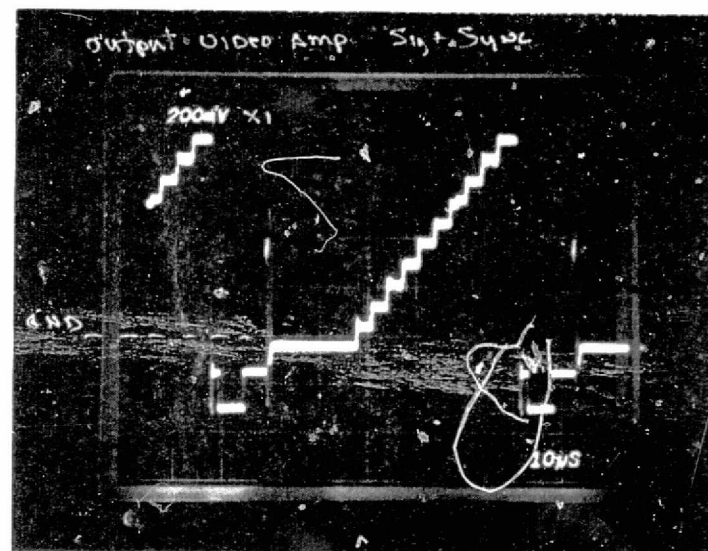(B)   VIDEO INPUT TO DELTA MOD BLANKING AMP.

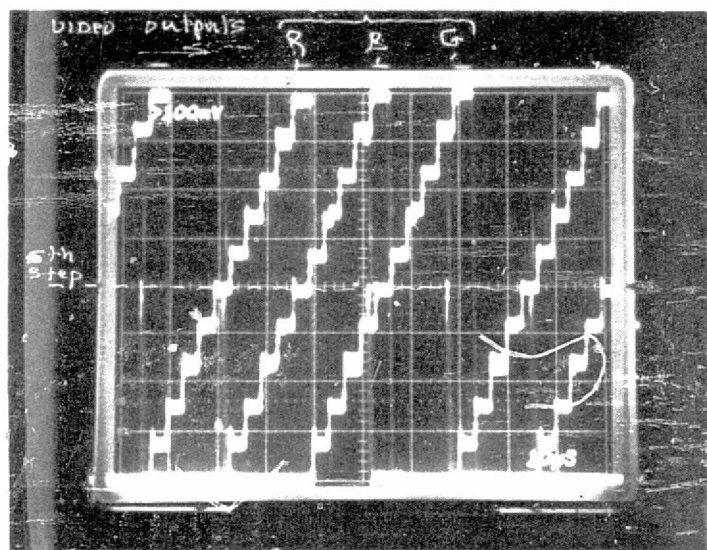(C)   VIDEO AT INPUT TO DELTA MOD SUMMING AMP.

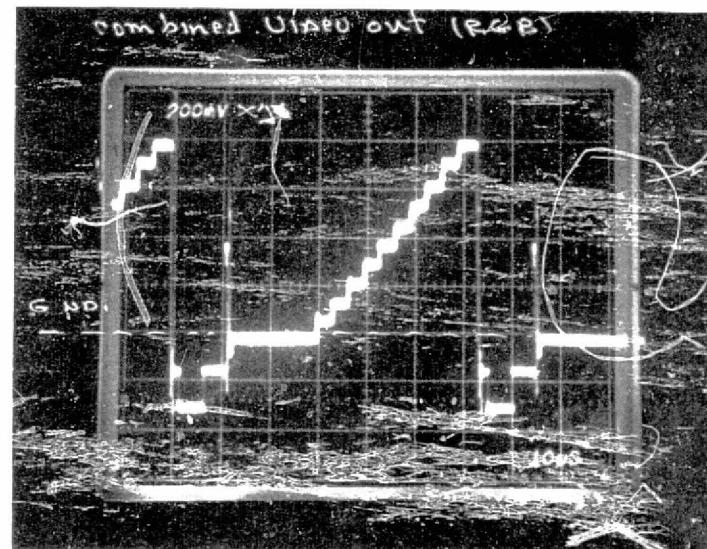(D)   VIDEO AT DIGITAL INTEGRATOR D/A CONV.

FIG. 9-1

(A) COMPOSITE SYNC INPUT TO OUTPUT
VIDEO AMP.

(B) SYNC PLUS VIDEO - OUTPUT OF VIDEO AMP.

(C) THREE CHANNELS (RGB) SUPERIMPOSED OUTPUTS

(D) COMBINED (RGB) OUTPUT FOR DISPLAY ON BLACK
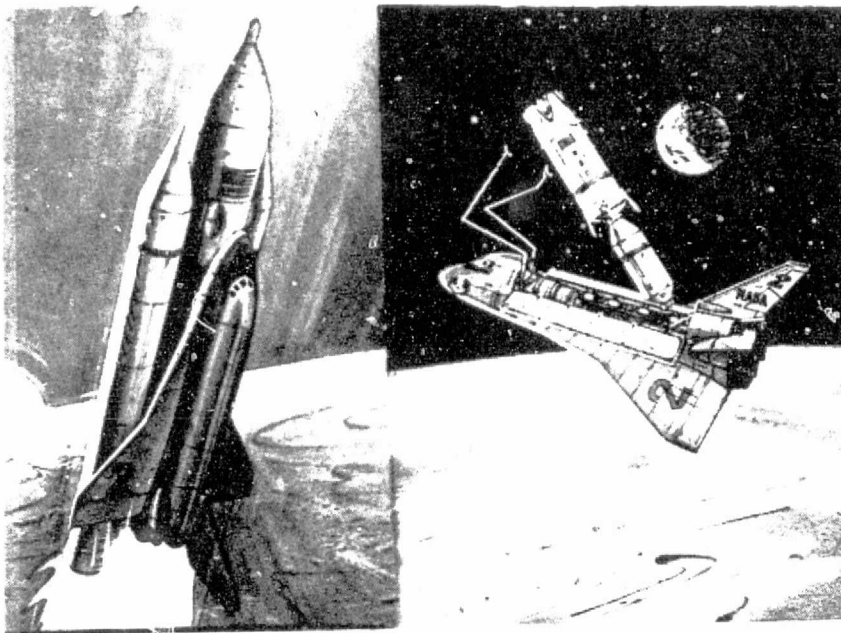AND WHITE MONITOR.
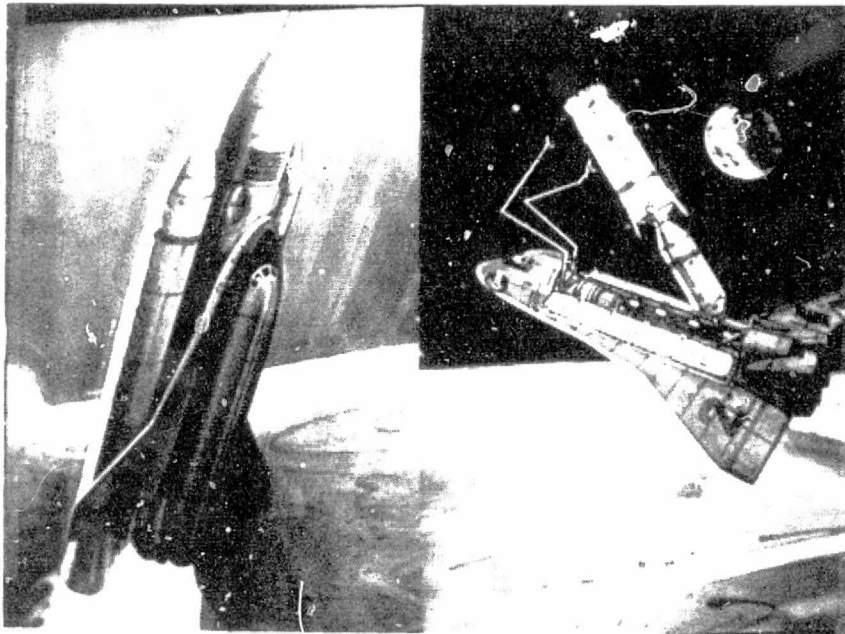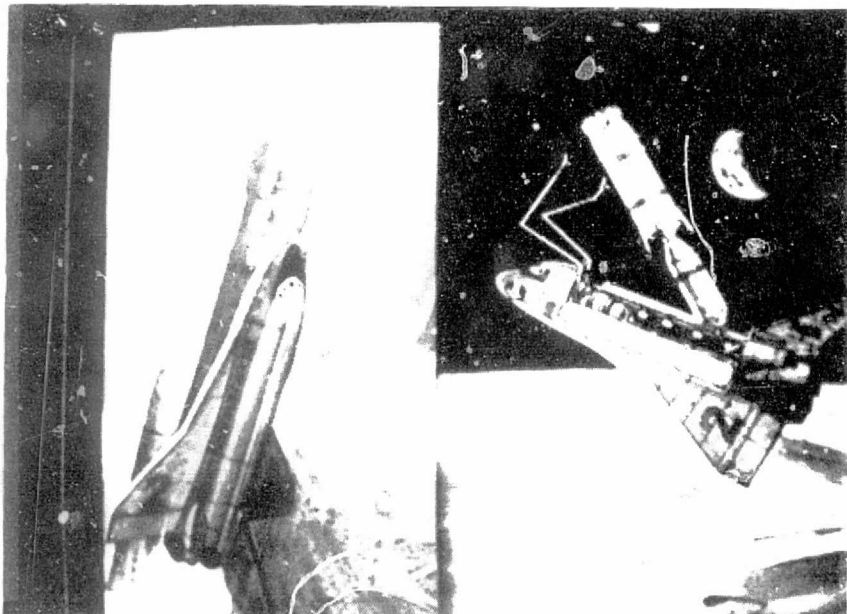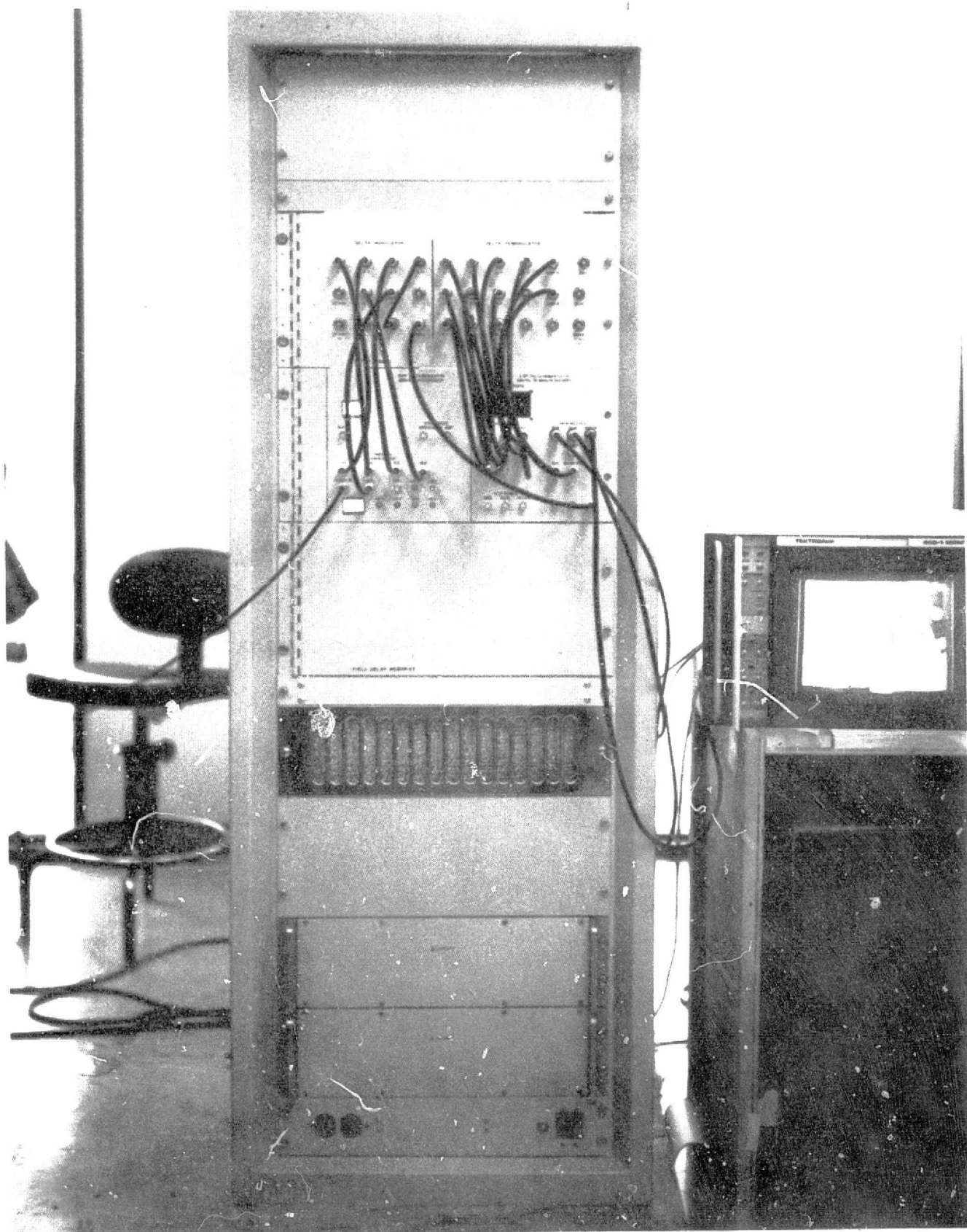
FIG. 9-2

PHOTO (A)

ORIGINAL PHOTO

PHOTO (B)

PHOTO OF BACK TO BACK
OPERATION OF CAMERA &
T.V. MONITOR

PHOTO (C)

PHOTO OF OPERATION
THREE DIGITAL DELTA
MODULATOR AND MEMORY

FIG. 9-3

Figure 9.1A shows the input video signal to the delta modem. This signal is standard NTSC video (.75 volts video .250 volts composit sync.) Figure 9.1 B, C, show the centering of the video about ground reference and the blanking of the composit sync signals. Figure 9.1 D. is the reconstructed video at the output of the digital integrator in the delta mod loop. It should be noted that the polarity of 9.1 (c) and (d) are reversed. These two wave forms are summered to form the error signal which is quantized to three (3) bits. The video waveform of Figure 9.1.D is the exact same signal which appears at the output of the Delta Demod digital integrator, this wave form represents the reconstructed video information.

Figure 9.2 are typical wave forms in the digital demod. Figure 9.2.A,B show composit sync. Figure 9.2.C shows the output of the red, blue, green channels, with the same gray scale input at the delta mod. Figure 9.2.D is a combined video signal of the red, blue, green channels added to gether to form one video signal. Note the channel registration showing the ability of the digital delta mod to preserve linearity of the gray scale. Also, note that the peak to peak noise is much less than one grey scale step of the 10 step video waveform.

Figure 9.3 A, B, C are photos taken from a bl ck and white monitor using polaroid film. They show the original photo, a picture run back to back with the camera and monitor, and the picture run thru the complete Delta mod-memory-Demod system.

TABLE 9-1

SPECIFICATIONS vs. STP CONVERTER PERFORMANCE

Video Input Impedance	75 Ohms $\pm$ 5%	75 ohms $\pm$ 3%
Field-To-Field Gain Stability	5%	0.1%
Luminance Resolution	10 Gray Shades	>15 Gray Shades
Channel-To-Channel Gain	3.5 mv	3.5 mv
Channel-To-Channel Registration	440 Line Response at least 50% of 220 Line Response	440 Line Response >60% of 220 Line Response
Vertical Resolution	330 TV Line of raster height	330 TV Line of raster height
Horizontal Resolution	440 TV Line of Raster Width	>500 Line of Raster Height
Signal-To-Noise Ratio	Not Less Than 45 dB	48 dB

RECOMMENDATIONS AND CONCLUSIONS

The test results obtained with the breadboard STP Converter together with the subjective quality of the converted image observed on a color monitor are excellent and verify the validity of the design approach.

The digital approach indeed does not exhibit the classical pictorial stability problems associated with analog STP converters. In addition, the noise performance of the 3 Bit Delta Modulator is excellent and produces no observable noise increase over analog TV with the camera back to back with the monitor. One surprise was the excellent horizontal resolution obtained with the design A/D Converter and horizontal sampling rate. The sampling rate was selected by assuming a equivalent horizontal "Kell" factor of 0.7. The resultant assumption should have limited the horizontal resolution to the specified value of 440 TV line. The observed horizontal resolution however, is much better than this and is closer to 550 TV lines. This observation provides a basis for questioning such a conservative value of horizontal "Kell" factor in the future and also suggests that the quantity of memory might be reduced for an operational STP Converter and still permit obtainment of the required resolution.

The principal recommendations resulting from the experience of the project are to redesign the 3 Bit Delta Modulator using an all digital approach, and to substitute N MOS RAM or Digital CCD memories for the P MOS Shift Register memories incorporated in the present design.

Both of these recommendations would take advantage of improved technology components that were not available at the time of the project design commitment. An all digital Delta Modulator is now possible using high speed ECL - RAMs or a look up table and would increase the Delta Modulator timing loop margins as well as eliminating the need for analog alignment. The use of 4096 X 1 MOS - RAMs memories offer a performance and cost advantage while the digital CCD memories offer a weight and power advantage. The principal performance advantage of the N MOS RAMs is more graceful performance degradation where a typical memory failure

10.0   RECOMMENDATIONS AND CONCLUSIONS   (continued)

(a single bit) would cause a limited streak problem in any
one TV line instead of multiple streaks in the case of a
shift register memory failure.