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INVESTIGATION OF SYSTEM INTEGRATION METHODS FOR BUBBLE DOMAIN FLIGHT RECORDERS

By T. T. Chen, O. D. Bohning et. al.

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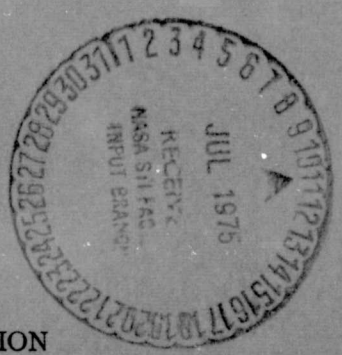

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16. Abstract

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A small 60 k bit engineering model was built and tested to demonstrate the feasibility of the bubble recorder. It consists of six 10 k bit, 24 μm period bubble memory chips assembled in three individual packages forming three recorder tracks. Recorder operating modes include erase, sequential write, chip align, byte read and search. The intrinsic operating speed is 150 kHz but it can read and write asynchronously at any lower speed. Using power strobing and dc restore, a detection error rate between 10^{-6} to 10^{-8} is achieved with a 300 μV detection signal and the hard error rate is better than 10^{-12}. The recorder also has been successfully tested for an extended temperature range between 0 to 50°C for operating test and -25°C to 85°C for non-operating data retention test.

Based on the various studies performed, a projection is made on a 5×10^7 bit prototype recorder. Using a 10^5 bit, 16 μm period, serial memory chip with 16 chips assembled is one coil set, it is estimated that the recorder will occupy 190 in.^{3}, weigh 12 lb and consume 12 w power when all of its four tracks are operated in parallel at 150 kHz data rate.

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SUMMARY

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1. INTRODUCTION

The objective of this program was threefold, first, to investigate the system integration methods for bubble domain flight recorders, second to construct a small engineering model to demonstrate the feasibility of fabricating a flight recorder by using current bubble memory technology, and third to make an estimate on the suitability of bubble technology in a simple satellite data recorder. The intent of this program was to make maximum use of the existing materials and devices. No work to extend or modify the present ferrimagnetic film or bubble device technology was performed.

More specifically, the work performed in this contract can be summarized as several tasks as listed below.

Task 1 - Perform package design including chip bonding, electrical connections and associated thermal and mechanical effects.

Task 2 - Electronic design to give appearance of serial first-in-first-out recorder track.

Task 3 - Rotating field network design.

Task 4 - Design of the bias field structure.

Task 5 - Investigate interaction between bias field, rotating field and packaged device performance.

Task 6 - Construction of a small engineering model.

Task 7 - Estimate level of effort to advance bubble recorder technology to a simple satellite data recorder.

Because of the time involved in the design and construction of some of the hardware, such as the memory chip and its ceramic package for the engineering model application, the construction of the model actually started at the very beginning of this program. Thus, the model performance does not necessarily correlate to the studies performed in the other tasks. Instead, the conclusions derived in the studies are implemented in the task above of designing a simple satellite recorder.

During the construction of the engineering model, it was found that the memory chips can be operated at 150 kHz which is the prototype design goal. Thus, the engineering model performance was modified to 150 kHz operation for all the studies.

In June 1974, a six-month extension was granted in this program and three additional tasks were added to the study.

Task 8 - Perform operational tests on the engineering model over the temperature range of $0^{o}C$ to $50^{o}C$ and data rates up to 150 kHz including the memory chip operation margin, detector error rate and system reliability.

Task 9 - Fabricate eight 10^4 bit memory elements tested for operation at data rates up to 150 kHz.

Task 10 - Fabricate an exerciser to test and evaluate the engineering model.

This report is organized in accordance to the individual study tasks. Section 2 gives an overview on the recorder system and discusses some of its potential applications. Section 3 discusses the package; Section 4, electronic design; Section 5, rotating field network; Section 6, bias field structure; and Section 7, tolerance in the field network design. The design detail on the engineering model is presented in Section 8 and a projected prototype recorder design is discussed in Section 9. The detail study on the present memory chip and the feasibility model is documented in Section 10.

This report was prepared by the Electronics Research Division, Autonetics Group, Electronics Operations of Rockwell International, Anaheim, California, under NASA Contract Number NAS1-12435. It summarizes the work performed during the period from July 1973 to November 1974.

This contract was administered by the Microelectronics Group, Flight Instrumentation Division, Langely Research Center, NASA, Langely Virginia. The contract monitor was Dr. R. L. Stermer, Jr.

The contract work was performed in the Applied Magnetics Department, Physical Science Laboratory, under the planning and direction of J. L. Archer, Department Manager. The responsibility was divided as following: The device packaging study (Section 3) was performed by C. L. Zachry of the Magnetic Circuits group under the guidance of R. F. Bailey, Group Supervisor. The electronic system study (Sections 2, 4, 8, 9 and 10) and recorder and exerciser electronics design were contributed by O. D. Bohning of the Magnetic System group under the supervision of J. E. Ypma, Group Supervisor. The magnetic system study (Sections 5, 6, 7, 8, 9 and 10) and the magnetic module were performed by T. T. Chen of the Magnetic Circuits group under the direction of L. R. Tocci, Group Supervisor. The principal investigator was T. T. Chen and the program managers were L. R. Tocci and J. L. Archer. Acknowledgement is given to A. G. Campbell, D. F. Welch, and G. N. Meldrum for testing and construction of the recorder hardware; T. R. Oeffinger and P. K. George, for some of the device evaluation; P. E. Elkins, C. D. Sallee, E. F. Grubb, A. B. Jones, N. L. Lind, E. Walker for device fabrication, and R. G. Wolfshagen, J. L. Williams, T. Kobayashi and other members of the Applied Magnetics Department for their discussions and suggestions.

2. GENERAL DESCRIPTION OF A BUBBLE RECORDER

2.1 Magnetic Bubble Recorder

A bubble domain recorder system which will operate as a flight recorder is shown in Figure 1. It is organized into several independent tracks similar to a tape recorder. Each track consists of a number of large capacity single loop bubble memory chips with individual bubble generator, annihilator and detector circuits. These chips are electrically connected in series to act as a FIFO type memory. Using small field coils and a permanent magnet bias the operating power is comparable to a tape recorder and the standby power is zero. Using a moderate bubble propagation rate of 150 kHz the bubble recorder data rate is comparable to that of most flight recorders.

Bubble recorders, however, have two additional attributes that add dimensions of flexibility and reliability not found in the present tape recorder. As the bubble memory can be easily turned on or off within one data cycle, the bubble recorder can be read or written into asynchronously at any frequency up to the intrinsic rotating field frequency. With this unique property it can be used for incremental recording or recording and playback at lower frequencies.

The second attribute is derived from the bubble recorder organization. In this organization each chip can be considered an an independent block of information. Thus, in addition to reading out these blocks serially, random block access can be used. This chip-to-chip independence also allows implementation of schemes whereby malfunctioning chips can be bypassed such that the reliability is increased and the recorder lifetime is not dependent on the malfunction of a single component.

Other attributes of a bubble recorder inherent in the technology include non-volatility of stored data and the nondestructive readout of data. The long term retention of information is ensured in a bubble memory by using permanent magnets to provide the required bias field but the retention of the location of the beginning bit of a record is not ensured without other provisions. A computer will begin processing at a fixed memory location which leads to a sequence of program dependent addresses which is a satisfactory arrangement for a random access memory connected to a central processor. But, the bubble memory may be a stand-alone component subjected to power outages and power shutdowns which lead to considerations of other schemes for the nonvolatile retention of the location of the last bit written, several of which will be described in the Electronic Design Philosophy section. Readout of the bubble recorder is nondestructive being accomplished by detection of the influence of the bubble on a magneto resistance detector.

2.2 Recorder Applications

In present satellite and deep space systems, tape recorders play an important role in information collection, storage and transmission. Those recorders have a wide range of storage capacity and operating frequency to meet different mission requirements. The space applications require zero standby power and nondestructive readout so that data retrieval is safeguarded indefinitely and so that it can be reread in case of transmission failure. Because of the high percentage of failures associated

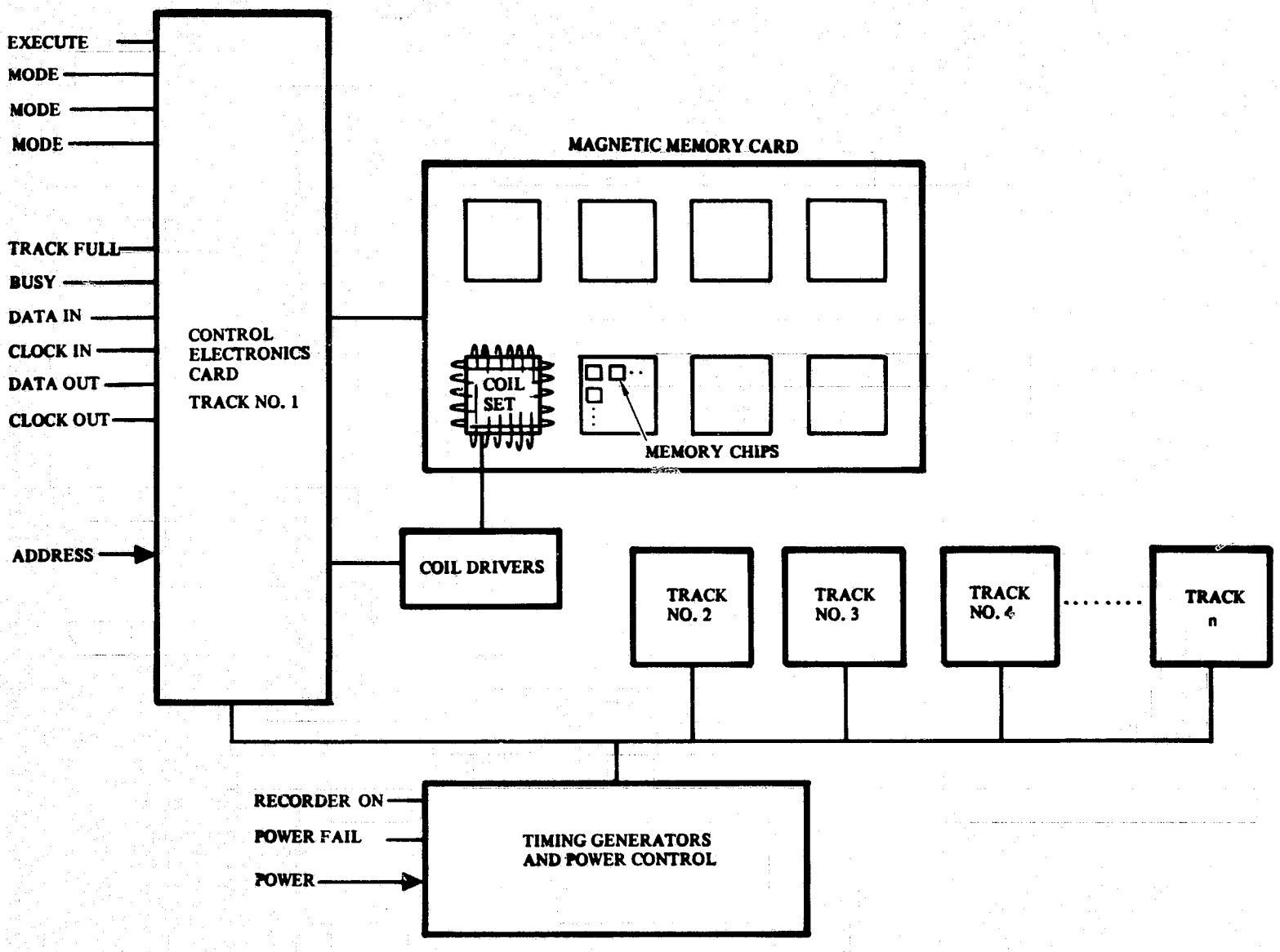


Figure 1. Bubble Domain Recorder Organization

with mechanical tape handlers, it was deemed desirable to develop a totally solid stable bubble recorder which would have the desirable attributes of tape but without the tape's inherent mechanical inertia or failure history. During the definition phase of the bubble recorder, consideration was given to all potential recorder applications so that the completed flight model would exhibit a flexible interface and so that the operational modes would be versatile enough to preclude redevelopment of a new recorder for every specialized space program. Two broad categories of applications are described below.

2.2.1 Blocked data formatting. - A major task in some telemetry systems (acquisition, data reduction, etc.) is the requirement for the fast formatting, processing, or conversion of computer or analog data. Searching through a long data track for a specific block of data is time consuming and fortunately is not necessary in a bubble recorder so long as the whereabouts of the data is known. A scheme to select blocks of data using chips having optimized capacity (100,000 bits) is easily implemented without increasing complexity. A block diagram of a memory system which uses the basic recorder as a subsystem is given in Figure 2. To use the system, data are first loaded into the RAM buffer along with its identifying address. Whenever convenient, the data along with parity codes are loaded into a particular chip of the bubble recorder. The short term data transfer rate can be as fast as the buffer will allow. To retrieve data, the desired address is matched with the proper chip location and that chip is interrogated until that address is found. The data which follow the address are then stripped of its control characters and fed out with a clock. Other subsystems can be added to provide more specialized features such as a bubble memory module having 10^4 bit chips which could provide faster access for a limited number of data blocks.

Important to the basic recorder design, as far as this class of applications is concerned, is the attribute of individual chip addressing and the synchronization of the data between all chips. Requirements like erasing or aligning the track before use are incumberances in these applications. Desirable are features such as being able to read in the same cycle as writing (but before writing) which will permit a read-modify-write mode of operation on a bit-by-bit basis.

2.2.2 Asynchronous data logger. - The other major category of application for a bubble recorder is the asynchronous accumulation of data from many inputs (along with appropriate identifiers) which are stored until such time as a data readout is desired. Figure 3 shows the type of system organization required using the basic recorder. The control consists of a device which samples the experiments' status and gates the results along with a clock to the recorder. This controller is much simpler than that required for the block organizing application.

Important to recorder design in this class of operation is sequential selection, power switching, synchronous data transfer, and nonvolatile storage of both data and data location. A feature such as track align permits readout of data starting with data which were entered first is desired.

2.3 Recorder Modes of Operation

Providing for the many potential applications such as the two described above requires a flexible command repertoire. The set of seven operational modes given below provide the capability of either blocked data formatting or asynchronous data logging

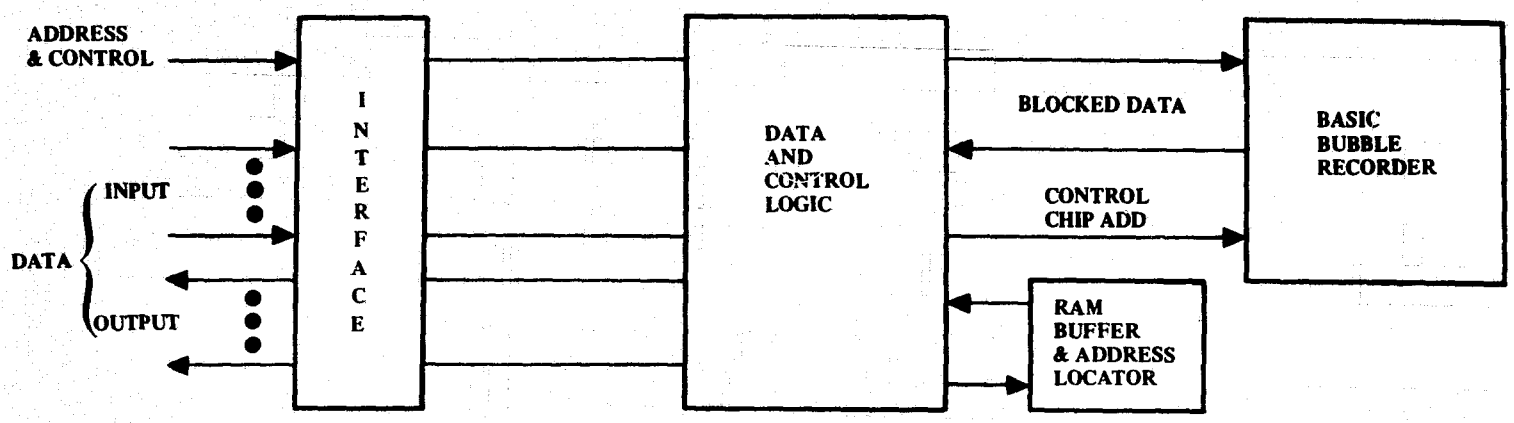


Figure 2. Mass Storage Bubble Memory System

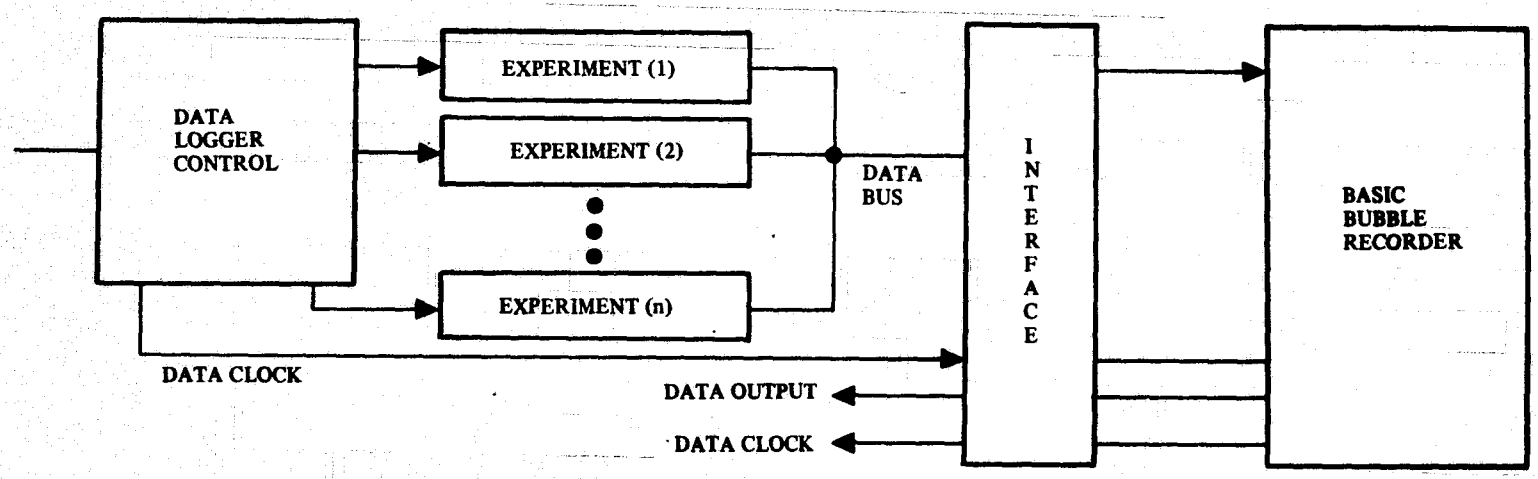


Figure 3. Data Logger Bubble Memory

and are suggested for incorporation into a sattelite bubble recorder. All but the chip addressing commands (4 and 5) were used in the feasibility model.

1. Erase - All bits are erased from all chips in a track.

2. Sequential Write - Data are accepted a bit at a time at whatever rate is desired up to the 150 kHz recorder rate. An indicator is provided when the track is filled.

3. Chip Align - All chips are aligned to their initialized position to provide proper record position in case a readout is desired.

4. Addressable Single Chip Write - A single chip can be written with data without disturbing the chip counter. An indicator is provided when the chip is filled.

5. Addressable Single Chip Read - This is a block read completed in a single chip rotation.

6. Byte Read - A Byte of data (7, 8, or 9-bits) is read for every request made.

7. Search - A sequential read is started and continues until either the track is completely read or until the operation is halted.

Figure 1 shows a set of control lines which is capable of performing the desired commands. Three mode lines are suggested which when properly decoded provide eight possible operations. The data-in and clock-in provide for asynchronous loading of data at the user's discretion, and the address lines provide for individual chip selection. Consideration for the selection of signal levels depend on such things as the standby state of the controller logic. These considerations will be covered in detail in Section 4 on design philosophy. Timing for the recorder track is expected to be generally like that shown in Figure 4.

2.4 Major Design Considerations

The order of priorities given below for the performance of a sattelite recorder form the basis of the decisions made in the design of the recorder. The list heavily favors long term remote location applications such as in space where maintainability is least required while reliability and functional performance are the most desired characteristics.

1. Functional Performance
2. Reliability
3. Power
4. Cost
5. Weight and Volume
6. Radiation Hardness
7. Maintainability

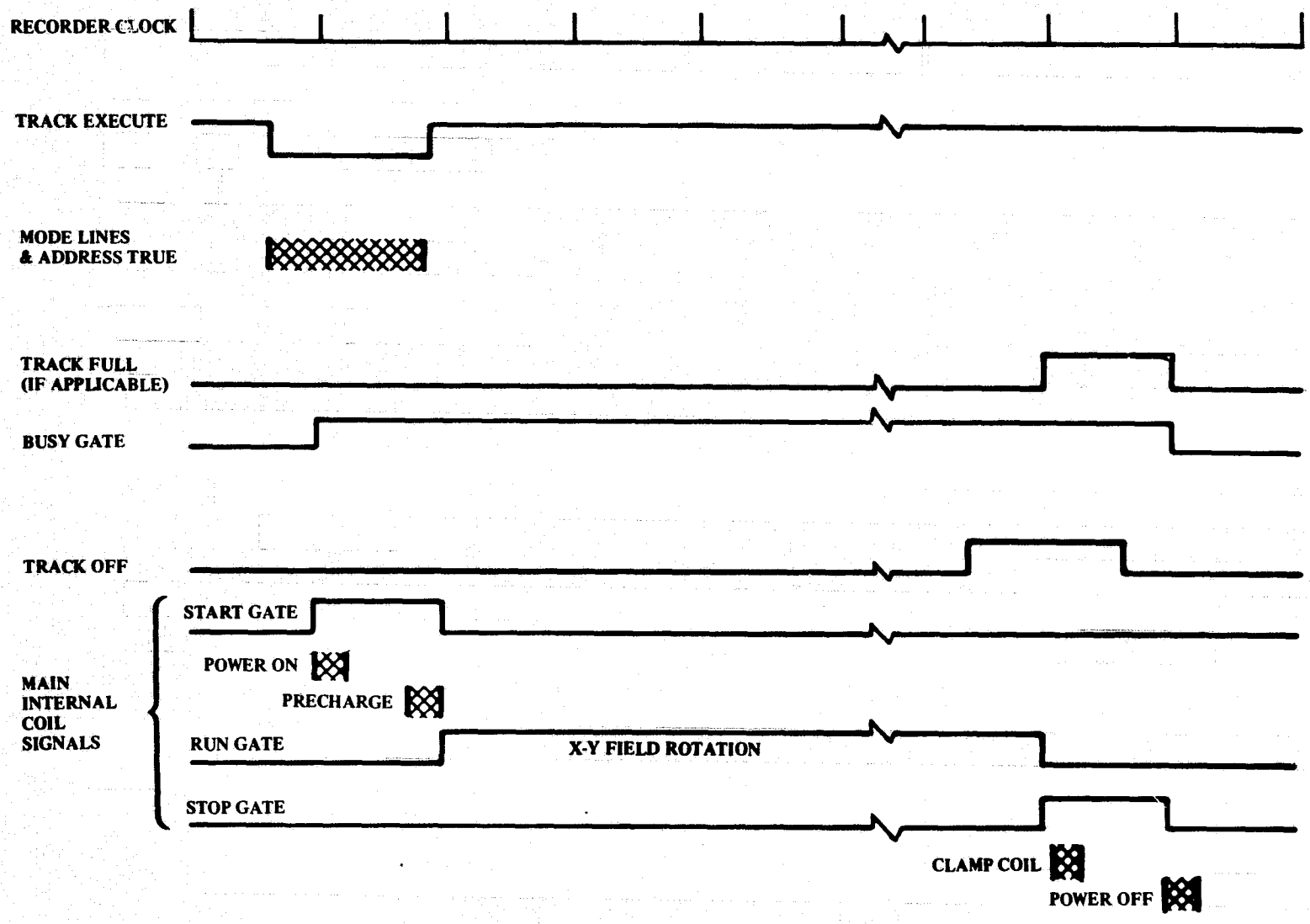


Figure 4. Recorder Interface Timing

A common denominator in achieving most of the factors listed above is the component count of the system. This property of systems should become an important consideration in the design of a recorder. Component reducing techniques, such as matrixing of chip functions, busing preamplifiers together, and consolidation of common functions, (like timing) were evaluated in the feasibility model and are being suggested for implementation in sattelite recorder designs.

Various steps can be taken to achieve a reliable system among which are techniques of soldering or installation of a screened grade of parts. Poor technique will preclude a reliable system regardless of the grade of parts. Techniques such as two layer PCB (vs multilayer), no connectors, minimization of interface connections (as with beam leads) will produce a system design which can be upgraded by more reliable parts. In this way the range of application for the recorder can be extended from low-cost to high reliability.

Hardening a system is similar to making it reliable in that a level of hardness can be achieved by various low-cost techniques short of selection of a hardened grade of parts. For example, shunting photo currents past a transistor's base to emitter junction with a resistor is inexpensive and is beneficial for reasons other than hardening. Also, using a derated value of Beta in the design is good practice for reliability considerations as well as for radiation. Unfortunately, most hardened TTL integrated circuits do not have grade-for-grade, pin-for-pin compatibility with low power TTL.

Cost of electronics are minimized by designing with parts that are commonly available which have years of usage. The "Dual In Line" package for integrated circuits is less expensive and more frequently used than the flatpack leading to a situation where volume is in conflict with cost.

These examples suggest that design priority should be established early in the development of a sattelite recorder so that system tradeoffs made in the early phases of design can lead to choices which can be retained in production models. For example the use of interboard connectors would have been acceptable in the feasibility model but to force evaluation of a more reliable approach, taped cables were used.

3. PACKAGING, BONDING AND HANDLING

Many assembly techniques and package materials used for standard integrated circuits can be used for packaging bubble memory devices. For example, standard handling methods and materials such as mounting epoxies and wafer and dice containers are applicable to bubble devices. However, bubble devices do have different packaging restrictions compared with semiconductor devices. These devices operate on the bulk properties of the magnetic material, and are relatively insensitive to environmental contamination with the exception that the permalloy film is vulnerable to halogen ions (Ref 1). With proper passivation on the permalloy overlay, hermetic seals should not be a requirement for bubble devices. On the other hand, the permalloy film is sensitive to prolonged high temperature (150°C) treatment (Ref 2) and thus the allowable temperature range in the packaging process is more restrictive than for conventional semiconductor devices. In general, the packaging technology for bubble memories presents its own unique set of criteria compared to conventional electron device packaging. The principal differences lie in the necessity for alignment of the device, bonds, and package structure with respect to the X, Y and Z magnetic fields required for device operation. Thus unique packaging considerations, which include mechanical and electromagnetic alignments are required when looking for a material and technique for device assembly. These considerations must also include the usual criteria of weight, volume, power restrictions, and physical stress (e.g., vibration, thermal and mechanical shock). Both ceramic and polymer (flexicircuit) packaging materials were evaluated and recommendations are made according to our present knowledge. Dicing techniques, bonding configurations and methods, and dice mounting are also discussed.

3.1 Packaging

Ceramic Packaging. - Alumina and beryllia ceramic materials are available substrate materials. However, beryllia was quickly eliminated from consideration because the technology for cofiring a conductor pattern on the package does not exist for beryllia as it does for alumina. Some of the attributes of the alumina ceramic tape multilayer technology are:

1. High thermal conductivity of 99.5 percent that of pure alumina,
2. Multilayer circuit capability,
3. Compatibility with known die mounting adhesives and eutectic bonding techniques,
4. Compatibility with many package sealing methods (e.g., solder, soft glass, epoxy),
5. The package may be used also as a coil form for the X-Y drivefield.

The multilayer ceramic technology possesses disadvantages, such as:

1. High resistance circuitry where the circuit line cannot be plated because of being buried between layers of ceramic material,

2. High abrasive contacts which abrade the connector coating (gold) on spring type connectors, producing unreliable contacts,

3. Marginal adhesion of the electrolessly plated gold to the tungsten metal circuit material,

4. Sharp edges and corners which cause damage to mating parts viz, wire coil wound directly on the package, PC boards, connectors,

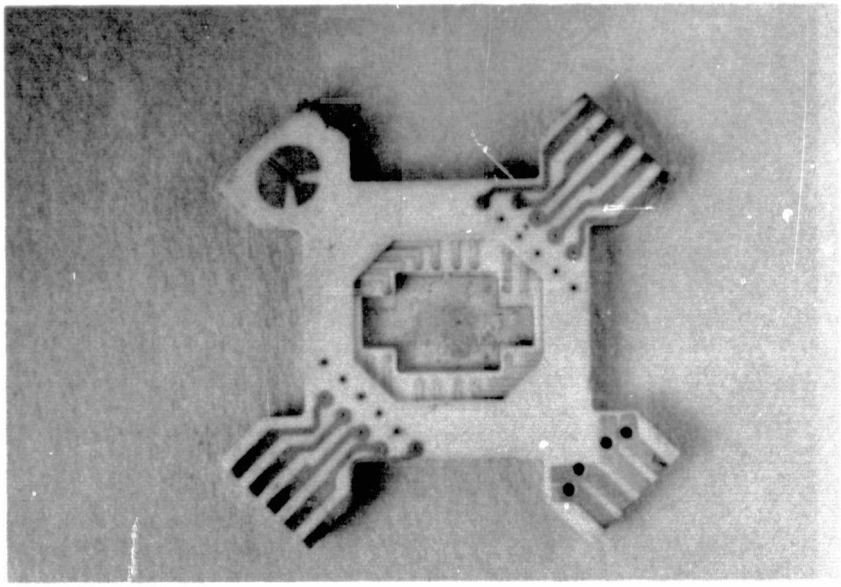
5. Excessive package thickness compared to some other materials,

6. Dimensional tolerance control from one process run to the next is questionable.

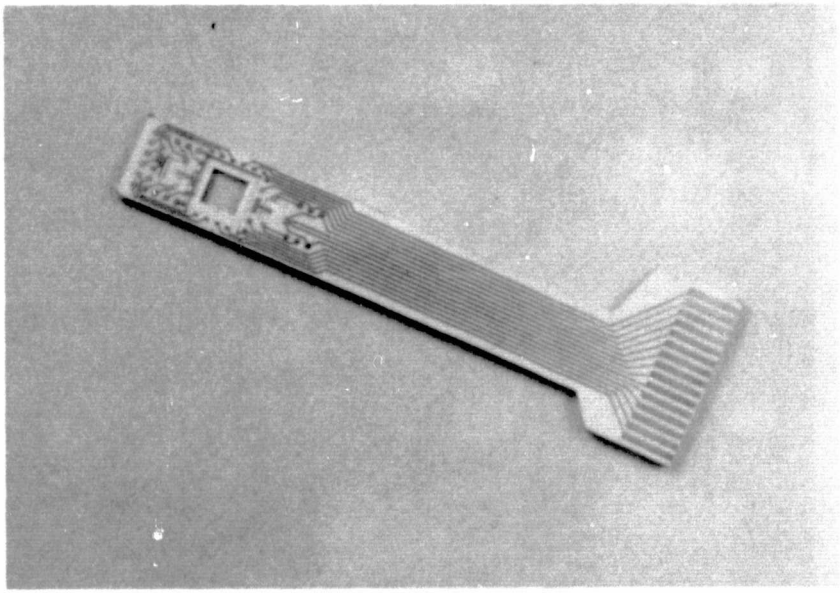
Two examples of the multilayer alumina tape process packages are shown in Figures 5a and 5b*. Figure 5a (package A) is a six layer package designed to accept two bubble memory devices and their sense amplifiers and detector bridge circuits. Conductor lines are continaed on four levels of the package. Metallized via holes connect the different levels where needed. A metallized layer on the bottom of the device well provides a common electrical connection for the sense amplifiers and a good base for either epoxy or eutectic die mounting. The package exterior shape was designed such that a set of rotational field coils could be wound directly on the package. This arrangement provides close coupling of the fields and the active element plane of the device(s). Figure 5b (package B) is a test board designed to be inserted into a coil fixture for functional die testing prior to actual packaging. The dimensional stability and repeatability of the process used to fabricate these packages proved erratic when attempting to fire the long thin structure. The design goal was dimensional tolerances of ± 0.005 in. and < 0.004 in./in. planarity. The yield on package A was on the order of 50 to 60 percent and the yield of package B dropped to less than 20 percent because of the inability to keep the above mentioned tolerances. Electroless gold plating was used to decrease the resistance of the conductor lines and to provide a bondable material. The adhesion of this plating to the cofired tungsten conductor lines exhibited a high failure rate when subjected to mechanical, thermal and vibration shock test. This package fabrication process would provide a versatile, planar, medium dense package provided that the aforementioned problems can be design compensated or eliminated.

Polymer packaging (flexcircuit). - An example of a flexible circuit/cable is shown in Figure 6. The base material is polyimide. A copper sheet of one ounce weight per square foot (1.4 mils thick) is laminated to the polyimide base and pattern plated with gold to $\sim 2\mu$m thick. The next step is to etch away the exposed copper, leaving the pattern shown. The pictured circuit includes a unique feature - beam circuitry. This circuitry feature is second only to beam lead devices, in configurations available to decrease $d\phi/dt$ pickup. Some of the other attributes are:

*These packages were developed under in-house programs but the studies to be reported on package A were performed under Task 1 of this contract.

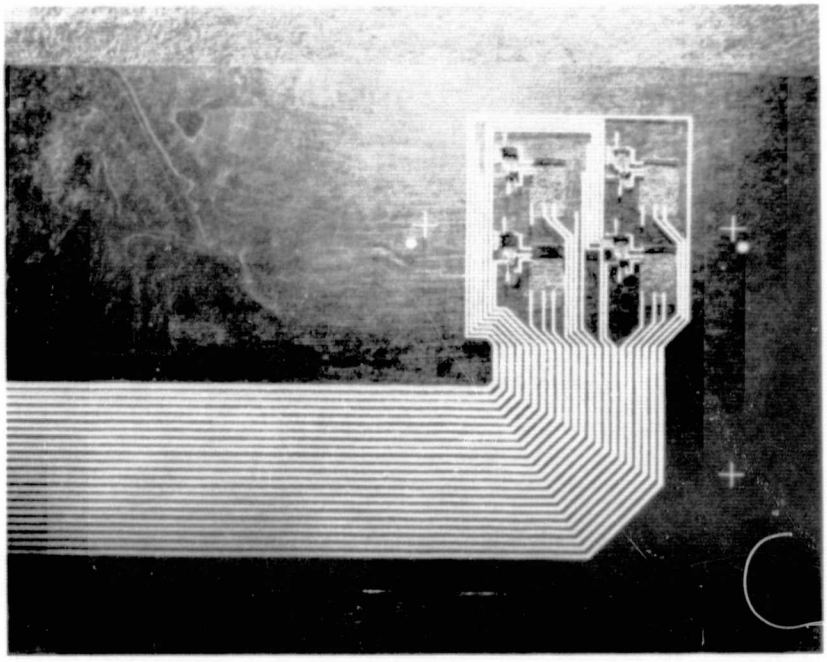


(a)

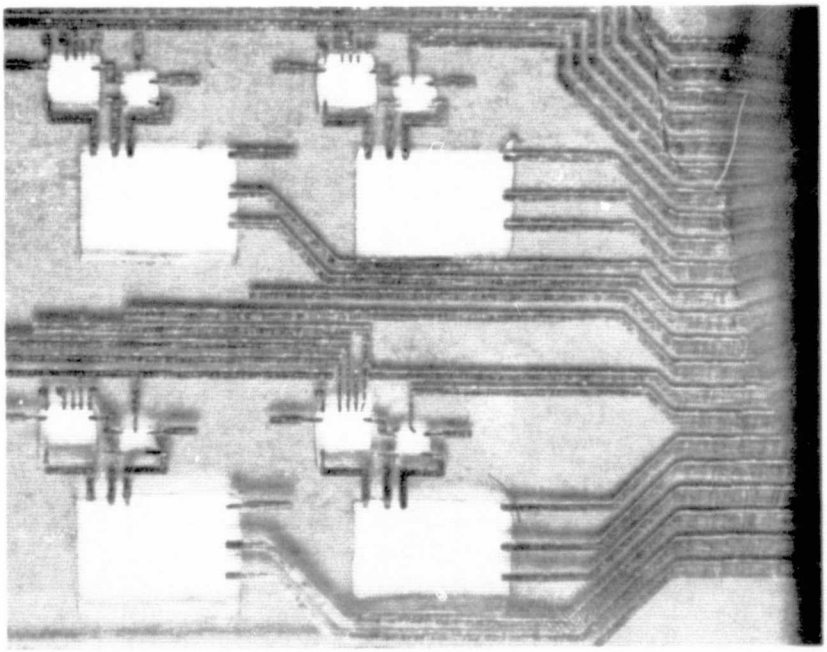


(b)

Figure 5. Multiple Layer Aluminum Package



(a) Polyimide Base Circuit/Cable



(b) Close up of the Device Area of the Polyimide Base Circuit

Figure 6. Polymer Package Circuit Concepts

1. Polyimide can be laminated to

   a. Itself
   b. Glass
   c. Ceramic
   d. Epoxy glass PC board material
   e. Metal
   f. Cermet

   (All of these can be used as stiffeners for coil forms and/or device mounting bases and heat sinks.)

2. The number of bonds can be reduced by one-half because the circuit and flexcable intraconnector are one and continuous in construction.

3. Line definition in the beam circuit area is sufficient to allow for IC's, diodes, etc. (i.e., 3.5 mil wide beams on 7 mil centers).

4. Via construction as pictured in Figure 7 is a feasible method of keeping the via transfer hole area to a minimum. Thus, multilayer construction, and high density conductor circuit lines are possible.

5. The flexible cable portion can be folded out of the package area and connected directly to the next level of the system, e.g., PC board (Figure 8).

6. A low profile multilayer circuit and/or device package may be achieved because of the thin circuit material (available in 1 mil through 3 mil standard thicknesses).

7. The circuit can be produced in multiples per panel and material costs are low (Ref 3).

Figure 8 is a cross section of a polyimide based package for a bubble memory. It consists of beam lead devices and single layer polymer based circuitry, plus two stiffener/device mounts. The beam lead portion may be replaced by strap bonded ribbon or beam circuitry for economy or ease of process. The single layer circuitry may be expanded to double-side or multilayer circuitry as necessary. The stiffeners may be made from ceramic or epoxy glass whichever is adequate for thermal distribution. The devices can be mounted in a face-to-face arrangement to increase the die density of the package also to minimize the package height. (A comparison of different chip arrangements are shown in Section 9.3).

The package is inserted into a field coil which is in turn inserted into an orthogonal field coil. The cable portion of the circuit/cable is folded out of the package between the coils and directly interconnected to the next layer of the system. Additional development is required to raise the thermal tolerance of the polymer system. The epoxy sheet laminate used as an adhesive at present is rated at 100°C. Another polymer composite which uses no added adhesive layer between the conductor and itself is Polyimide-Amide. The thermal tolerance is approximately 250°C. This

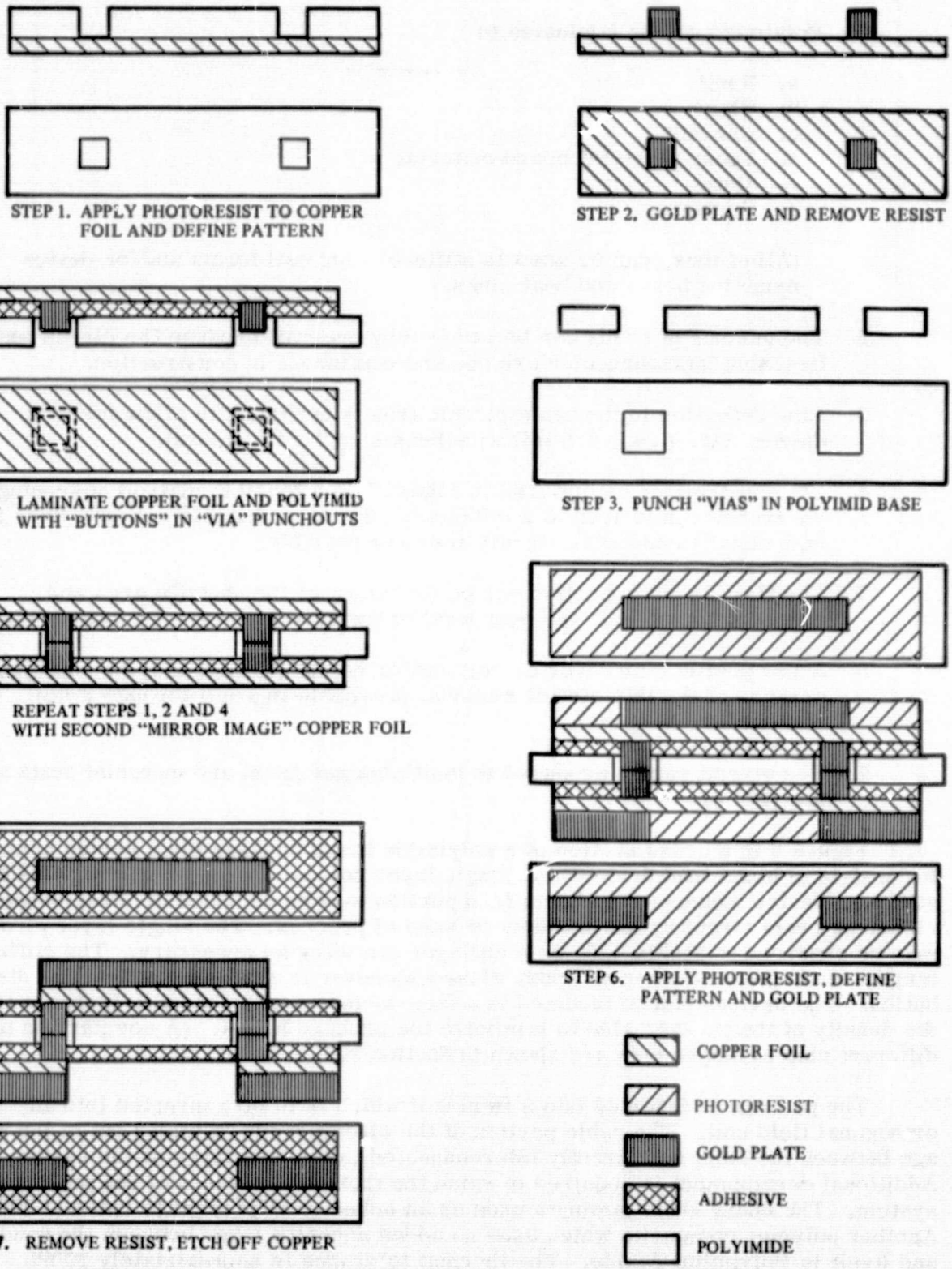


Figure 7. Proposed Construction for Flexible Circuits

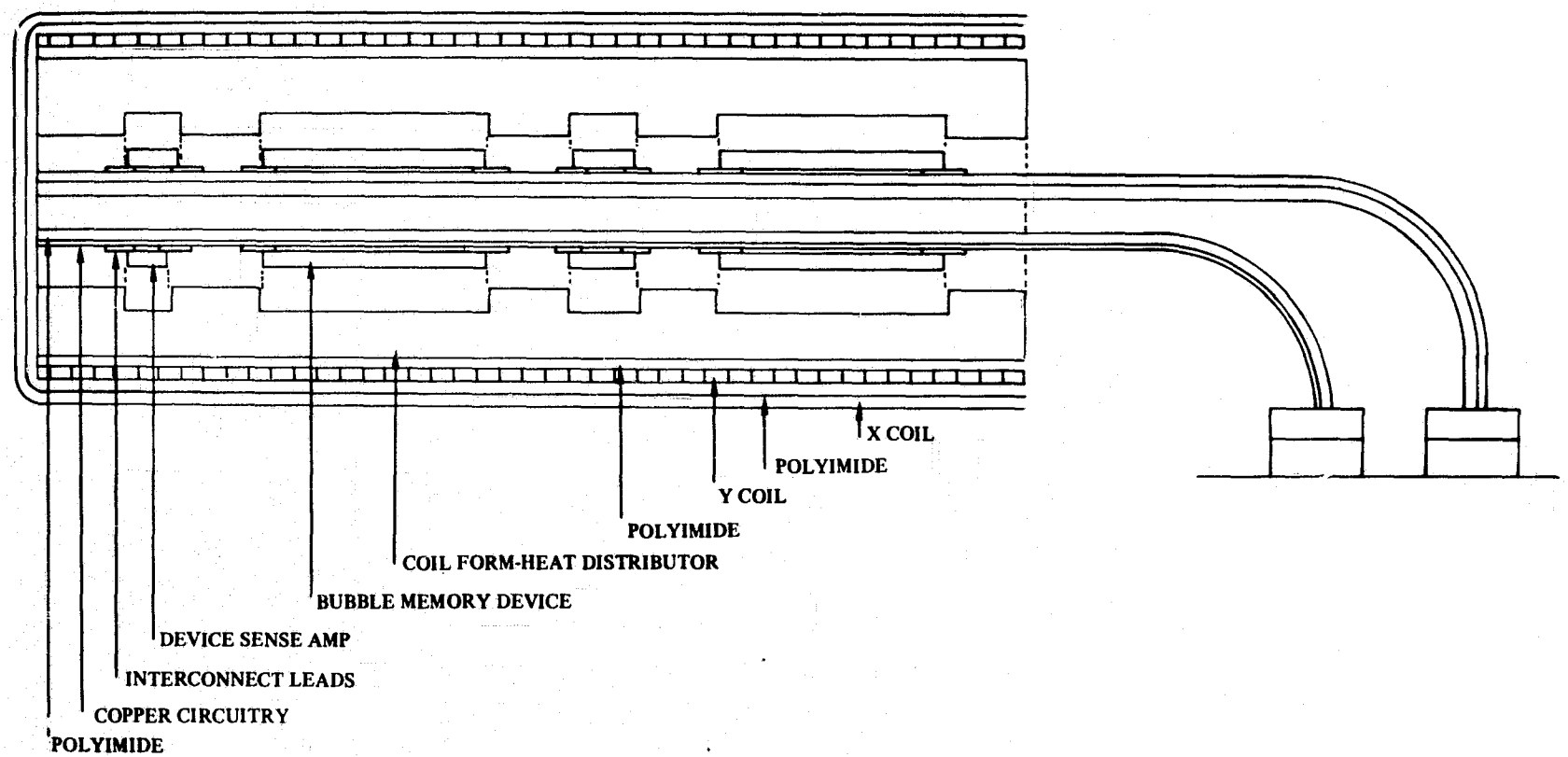


Figure 8. Polyimide Based Bubble Memory Package

material is similar in other properties and capabilities to the Polyimide flexible circuit base material. It would be prudent to consider materials like this for future bubble packaging efforts.

Polymer-ceramic combination. - The polymer material is versatile where intra level connection is of prime importance and has the advantage of keeping the total package to a low profile. However, the package must also serve as a planar reference and for device mounting. Ceramic can be used where thermal conductance and uniformity is important. Since the circuitry is not deposited on the ceramic the shape can be machined as necessary to ensure a smooth, flat base. The polymer materials mentioned previously are compatible with ceramic material uses of this type. The polymer would contain a circuit overlay bonded to the devices which are mounted on the ceramic. It should also be noted that where heat is not a problem, a less expensive package system may be constructed using epoxy-fiberglass (PC board) in place of ceramic.

3.2 Dicing

Four methods, (1) diamond scribe and break, (2) diamond impregnated wire sawing, (3) diamond impregnated high speed wheel sawing, (4) laser dicing, have been experimentally tested for the present program and other in-house projects, and a different degree of acceptability has been achieved with each.

Diamond scribe and break. - The diamond scribe method is the least desired because the garnet has no preferred cleavage plane. The scribed surface line may or may not follow through the rest of the thickness of the wafer. Hence breaking the wafer can lead to random and erratic sizes and shapes of dice that do not conform to the device pattern on the wafer. The scribe and break yield improves considerably for wafer thicknesses ≤ 0.3 mm.

Wire saw. - Good edge configurations are achieved by sawing with a diamond impregnated wire. The speed of cutting is second to a scribe/break method. Dice density on the wafer is reduced because of the wide kerf (min 0.008 in.) (Figure 9). Damage to the bubble material outside the immediate ($\sim$0.001 in.) area of the cut is inconsequential. The method would not be acceptable in a high production, low process cost situation where device density per wafer and process step time are major considerations.

Diamond wheel saw. - Indexing accuracy and narrow kerf (≤ 1.4 mils) are the principal attributes of the high speed (18,000 RPM) diamond impregnated saw (Model 602 Tempress). However, because of the hardness and the present thickness ($\sim$0.5 mm) of the garnet, cutting through the wafer on 10 to 14 streets takes about nine hours. The traverse speed is normally 5 cm/sec and penetration/pass is $\sim$0.005 mm. The blade may fail due to wear at any time during the cutting cycle, causing damage to the wafer surface, and the device patterns. Over such an extreme length of time of exposure to a process the probability of a damage is very high.

Laser scribe and break. - The CO_2 10.6 μm wavelength laser has been used to scribe several garnet wafers (Figure 10). The results are:

1. Acceptable edge configuration, slightly serrated,

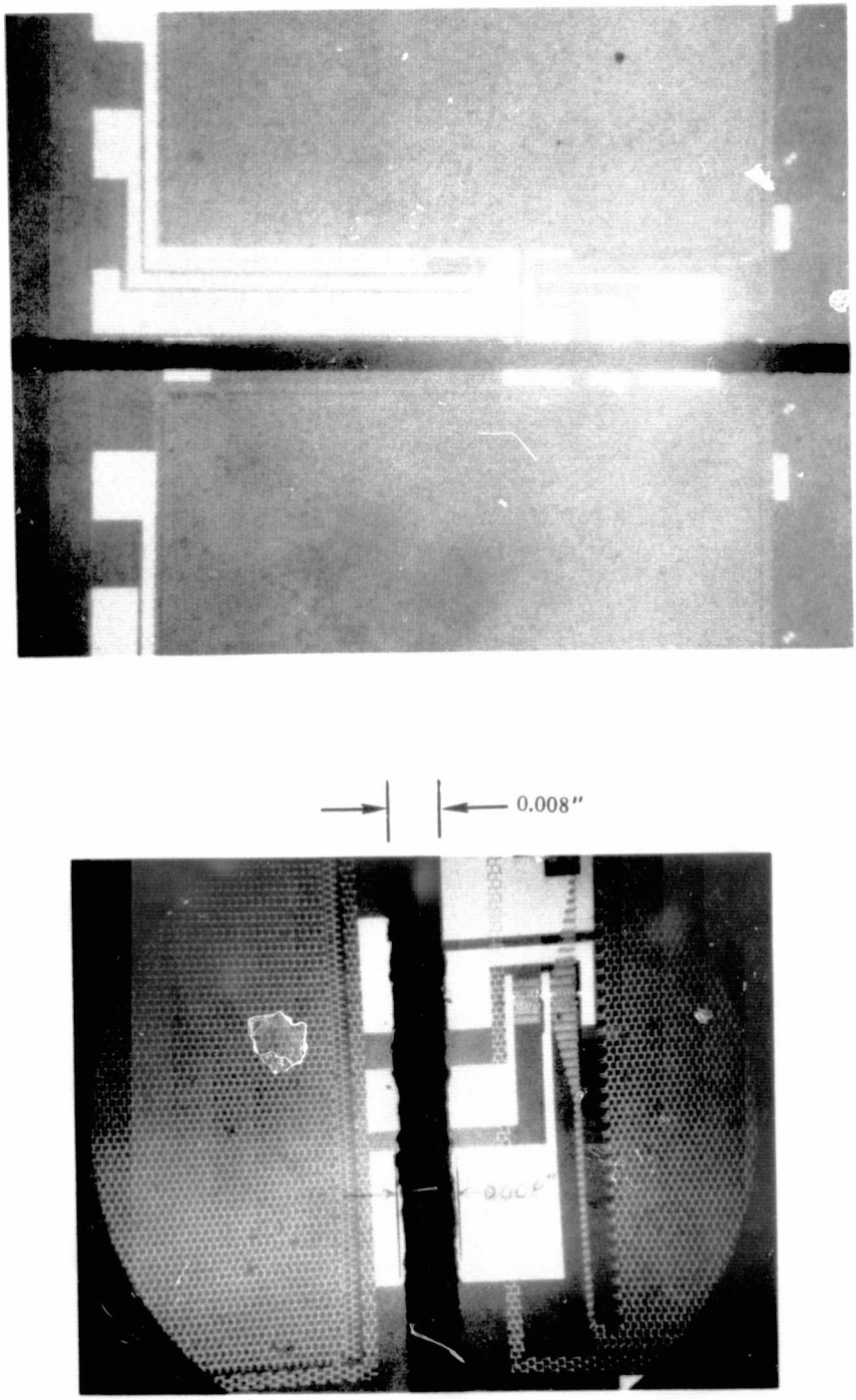
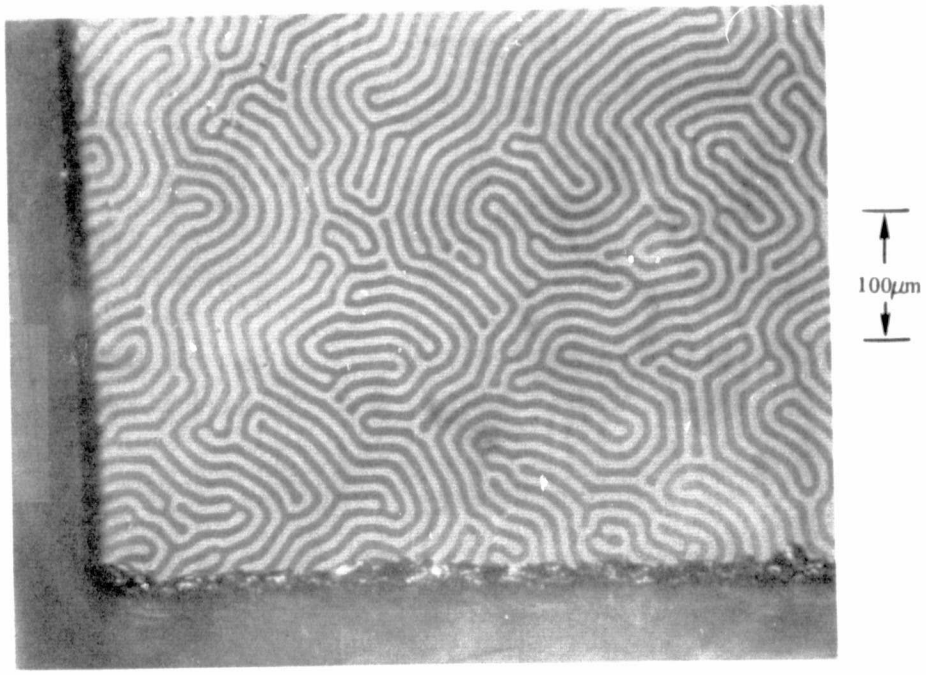
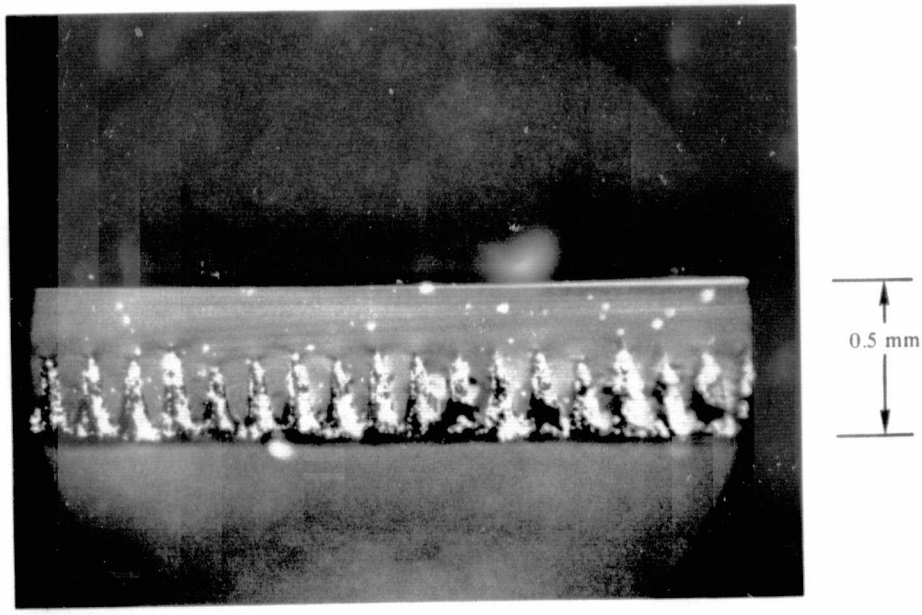


Figure 9. Diamond Impregnated Wire Sawn Garnet Wafer
(10^4 Die Pattern)



(a) Top view of the garnet wafer under polarized microscope. The laser scribed edge shows very little damage to the magnetic domains (Strip width 0.5 μm).



(b) Cross section view of the garnet wafer. Laser pulses penetrated from the bottom side.

Figure 10. Garnet Wafer Scribed by a CO_2 10.6 μm Wavelength Laser

2. High scribe speed, ~5 min/wafer,

3. Accuracy of cutting (with proper visual aid),

4. Negligible damage to the magnetic garnet film through heat effect.

A 50 watt machine (Coherent Radiation, Model 42) was peaked at 37 to 40 watts in the continuous mode, then used in the pulse mode to scribe the wafer from the back side. The pulses penetrated the wafer to ~40 percent of its thickness (0.2 mm in a 0.05 mm thick wafer). The traverse of the sample chuck table is arranged to produce 500 μs length pulses every 0.1 mm. The wafer was then placed against a silicone rubber sheet to prevent damage to the devices and allow flexure of the wafer during breaking. A little practice and care produces good wafer yield of accurate sized dice.

3.3 Bonding

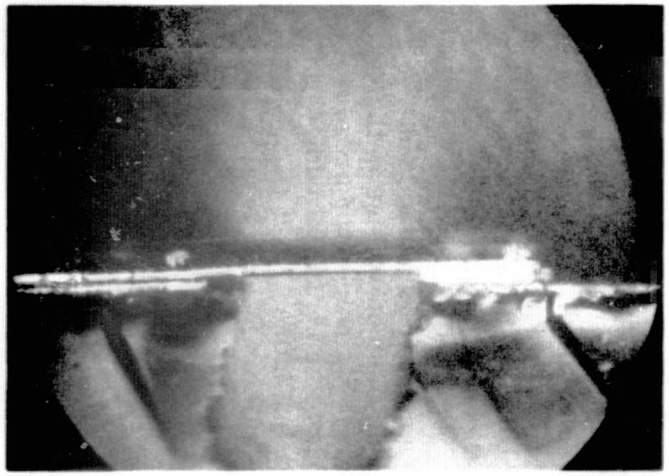
Since bubble memory devices are deposited on SiO_2 spacing layers, the basic bonding techniques for semiconductor devices can be adopted without any difficulty. In the present devices, Aℓ-Cu and CrAu interconnection pads are used. Both the thermal compression bonding and ultrasonic bonding have been tested and were found to be adequate. For future single level devices, bonds might have to be made on NiFe pads. For this case thermal compression bonding has been found suitable.

The bubble memory device is operated in a rotating magnetic field and a $d\phi/dt$ type voltage will be induced in any closed conductor loop. This induced voltage in the detector circuit will contribute systematic noise. To minimize this noise, the area enclosed by the bonding wire between the chip and package has to be kept minimum. Three bonded lead configurations have been studied as shown in Figure 11. It is apparent that the strap bond using ribbon conductor gives the minimum loop area, therefore the least $d\phi/dt$ pickup.

3.4 Device Mounting

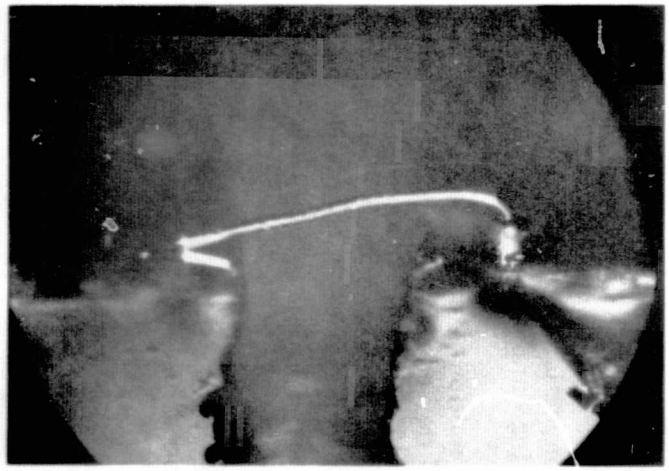
There are two unique requirements on the mounting of bubble devices as compared with conventional semiconductor devices: the device orientation and the temperature cycling during mounting.

The bubble motion is controlled by the in-plane rotating field, hence it is important that all devices have the same orientation with respect to the in-plane field so that there will be minimum phase variation on the device functions (such as generation, detection, annihilation, etc.). Bubble devices must also be parallel to the rotating field plane so that the in-plane field will not produce any perpendicular component to the device plane which reduces the operating margin. (These requirements will be discussed in detail in Section 7.) These conditions require that the device be mounted with much better accuracy than the corresponding semiconductor chips. Machines with device alignment control (such as an epoxy bonder) will be used in bubble chips mounting.



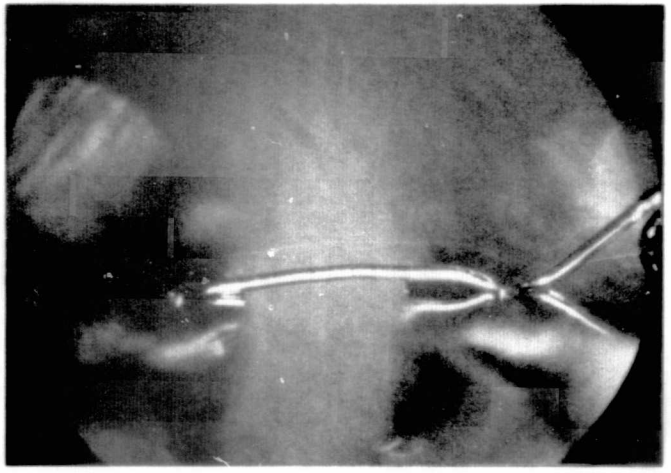
STRAP BOND
(WEDGE-WEDGE RIBBON)

AREA = 6.6 □MIL
$\frac{d\phi}{dt}$ PICKUP = 13.24 μV



BALL-WEDGE
BOND

AREA = 104.4 □MIL
$\frac{d\phi}{dt}$ PICKUP = 208.84 μV



LAP-LAP WIRE
BOND (STITCH)

AREA = 33 □MIL
$\frac{d\phi}{dt}$ PICKUP = 66 μV

Figure 11. Different Bonding Configurations and their Induced Voltage in a 30 Oe In-Plane Rotating Field

A common epoxy adhesive (Ablebond 606-4) used for hybrid semiconductor systems has been used for the present program. This epoxy can be cured at 125°C in one hour. This adhesive is screened on the substrate to ensure even thickness. Good thermal conductivity is not required for the present configuration since the memory organization is relatively simple and does not dissipate excessive power (less than 10 mw) in the device area.

Eutecting mounting is another possibility for bubble memory die mounting. Tests have been made for several bonding materials including gold-silicon, gold-germanium and regular lead-tin (63-37) solder. The test die were 10 K bit memory devices with 50 Å Cr and 5000 Å Au deposited on the backside and the packages used were commercial grade ceramic IC packages with gold plated metalization in the device mounting floor. Standard bonding procedures were used. All materials provided good bonds and attempts to pry the devices from the floor of the packages resulted in shearing of the bubble dice instead of breaking the bond.

Eutectic mounting is fast, simple and provides good thermal transfer between memory chip and package but it requires relative high mounting temperature (~500°C for Au-Si and Au-Ge ~190°C for 63-37 Pb-Sn). These process step temperatures not only impose more stringent requirements on the bubble device passivation but also exclude the possibility of using any low temperature packaging materials such as polyimide or epoxy packages.

At present, the allowable temperature cycling on the bubble memory devices is still not clear. It has been shown (Ref 2) that non-passivated permalloy films experience degradation (increased Hc and reduced $4\pi M$) when exposed to temperature greater than 150°C under nitrogen atmosphere for long times (~20 hr). But it also has been reported (Ref 4) that with proper passivation, thin permalloy film magnetoresistance detector can withstand heating of 250°C for more than 1000 hr. Before a detailed study has been made on the temperature-time effect on the bubble memory devices, it is recommended that low temperature die mounting techniques be used for bubble device mounting.

3.5 Wafer and Dice Handling

The permalloy propagation pattern is vulnerable to mechanical and chemical as well as thermal damage. Damage due to scratches or abrasion will prevent proper device operation. Elevated die temperatures can permanently change the magnetic properties of the permalloy. The chlorine ion is particularly damaging to permalloy in the presence of H_2O vapor (Ref 1). As little as 10^{-3} chlorine ion concentration in contact with permalloy at room temperature will eventually catalyze a reaction which transforms the pattern elements into a jelly-like substance which is hydroxides of Ni and Fe. To control these factors during handling of the completed wafer and dice, a coating of semiconductor grade polyvinyl co-polymer is spun onto the surface of the wafer/dice which can be easily removed by solvent when necessary. This process is considered only intermediate and temporary at this time and will be eliminated when a proper passivation technique has been established.

4. ELECTRONIC DESIGN PHILOSOPHY

This section covers (1) a discussion of circuit design concepts suitable for a satellite recorder and (2) describes specific circuits designed for and used in the feasibility model to evaluate the concepts. During the construction and evaluation of the feasibility model several new ideas and some short comings in design were discovered which are also discussed.

The most promising concepts in meeting the priorities of a satellite recorder are recommended for incorporation in a prototype design discussed in Section 9. More development is suggested for some circuits.

As far as circuit integration for future systems, the two specific circuits suggested for development are a multichannel preamplifier and a consolidation of some of the control electronics, with the preamplifier development offering the most payoff in terms of organization simplicity.

4.1 Feasibility Model Organization

Circuit topology for the feasibility model was organized along functional lines as shown in Figure 12. Each block of the diagram corresponds to a section following this one. Requirements for the design of the circuits in each block stem from the properties of the bubble chip. The required rotating field is provided for by the coil driver block, while the generation, annihilation, and sensing of the bubbles is accomplished by those blocks. All necessary timing for the functions which interface directly to the memory chip is provided by the timing section while the control section converts the input commands into specific action on the part of other blocks. To reduce power dissipation only the sections of the electronics required for operation are turned on - and this function is provided for by the power switching and distribution section.

4.2 Control Electronics

Functions such as byte control, bit counting, asynchronous-to-synchronous conversion, and turn-on/turn-off control all come together under the heading of control electronics. This section is categorized further according to specific circuits in the following paragraphs. The basic philosophy used in controlling the recorder is one where gated timing is produced by timing pulses which are continuous and in synchronization with each other (see the Timing Section) and "anded" with signals from the control section. Figure 13 illustrates the scheme in block form. The input signals are converted into gates by using counters of various bit durations and then are "anded" with a selected timing pulse (annihilation for example). Phasing is established by designating an edge of one of the timing pulses as 0 deg. In the case of the feasibility model, the reference (0 deg) occurs when maximum current flows out of the "x" coil which corresponds with the recorder clock (RCLS) signal. It is recommended that this control philosophy be continued into prototype design especially since several manufacturers produce MOS and bipolar programmable logic arrays (Ref 5) which can be substituted in place of the block on the right of Figure 13 whenever the control design becomes thoroughly proven and accepted.

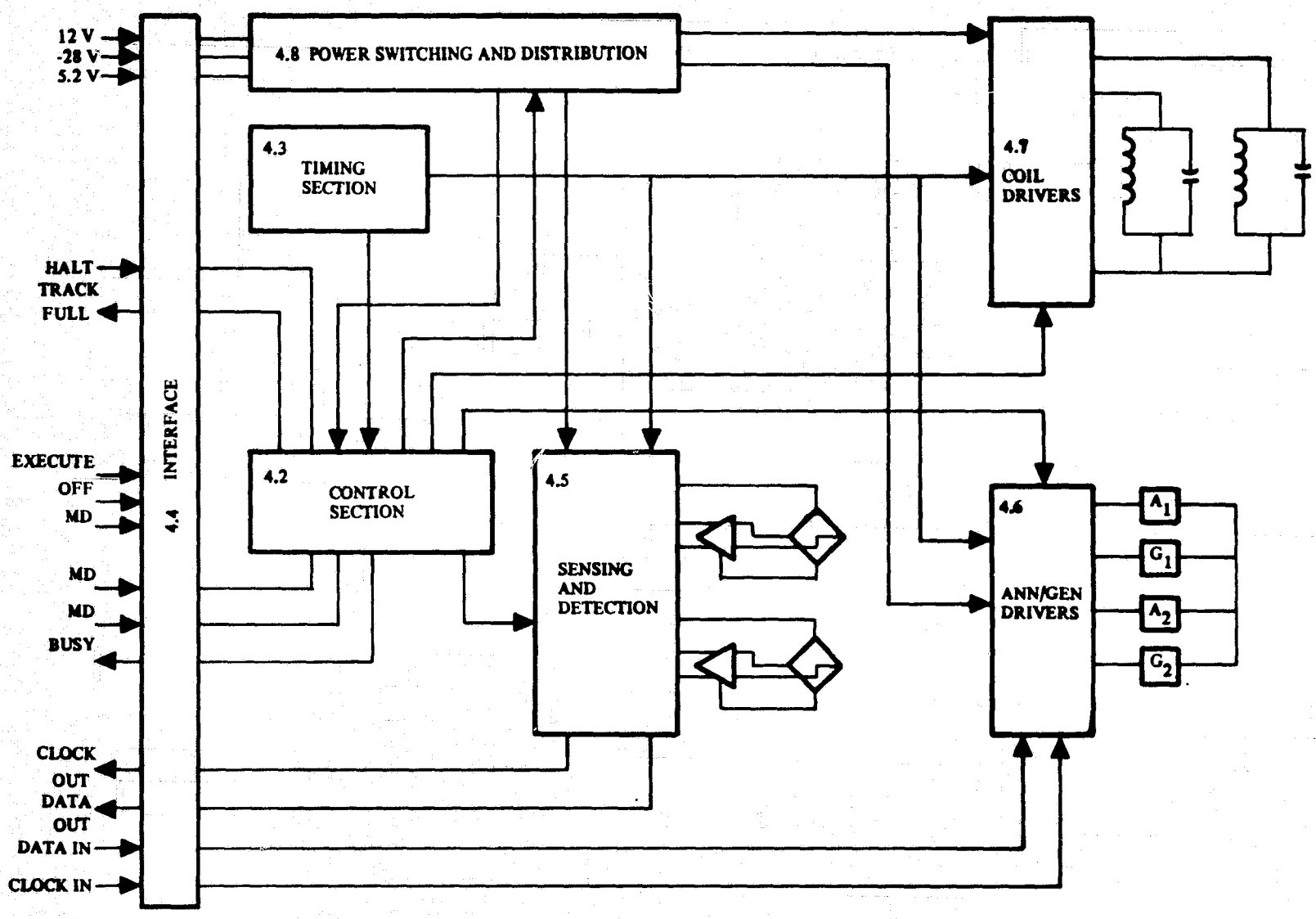


Figure 12. Functional Organization of a Single Track

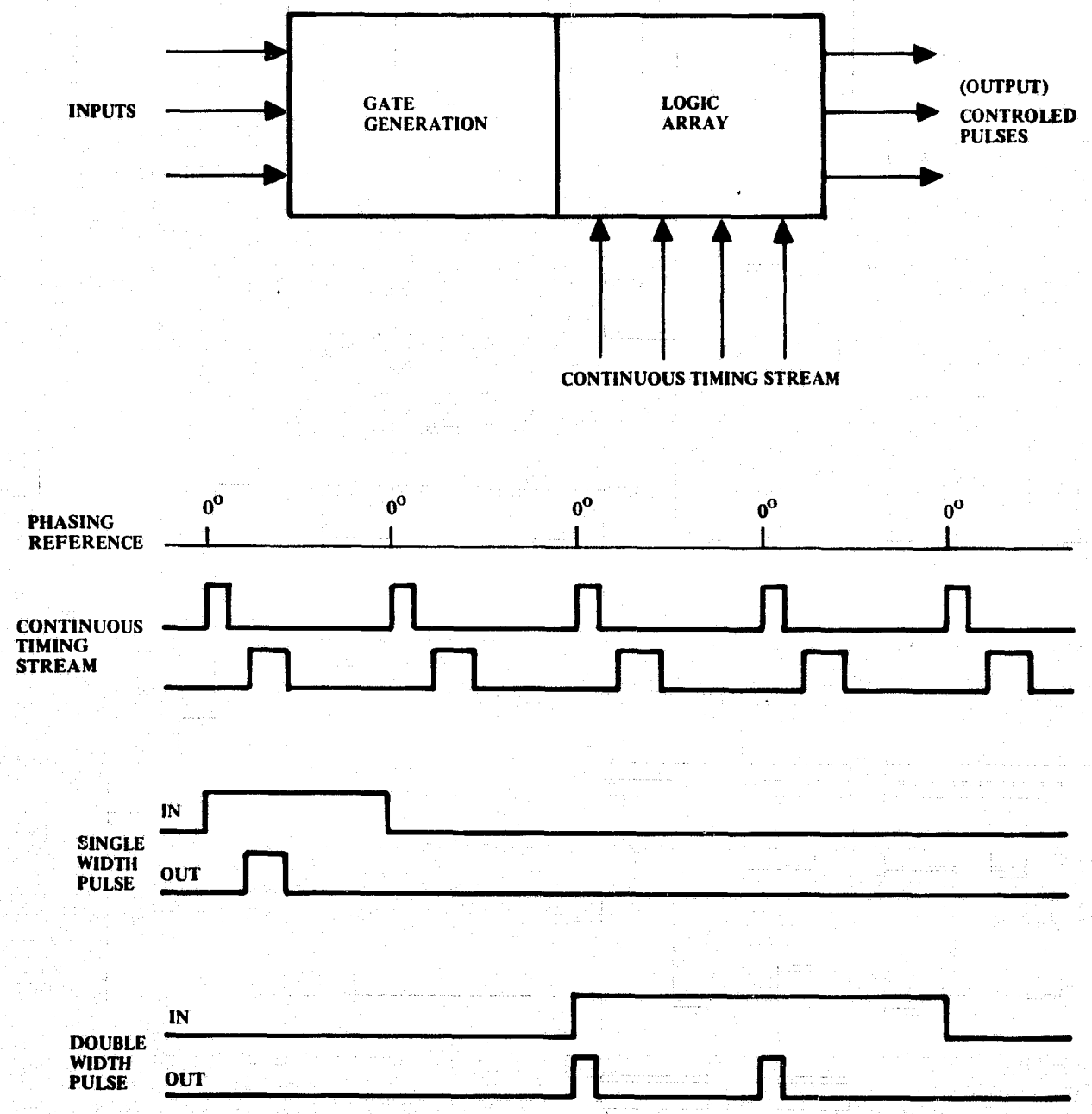


Figure 13. Examples of Gated Timing

Run Control. - When turning on the feasibility model it is necessary to start a sequence of starting, running, and stopping various functions including the coil. Two flip-flops and a logic state decoder provide the controlled action as shown in Figure 14. The sequence is as follows:

1. A start gate which enables all functions associated with starting coils and turning on power to key sections. This gate lasts one clock period.

2. A run gate which enables all functions associated with running the coils, the generator, the annihilator, and the sensing electronics as specified by the mode. When the run time requirements are satisfied, whether 8 cycles or 10,000, a command will discontinue the action and go to the next step.

3. A stop gate which enables the coil shutdown operation and which turns off power associated with the operating section. The circuit shown in Figure 14 uses as its basic principle the fact that a JK flip-flop holds a state for zero/zero inputs. Two flip-flops produce four states, three of which control the sequence described above and the fourth which is an off condition. The memory is busy for all of the three steps in the sequence. "Busy" is decoded for use by the interfacing unit as well as internal to the memory. The circuit of Figure 14 constitutes part of the gate generation block of Figure 13.

Async-sync converter. – The block diagram of Figure 15 covers the essential features of the converter. Data are clocked into the shift register with the data clock supplied by the user until the counter has reached a count corresponding to a full register at which time the rotating field is turned on by the full register flag. Data in the register are gated to the generator circuit starting from the first bit in and proceeding sequentially to the last in until no more data are available at which time the rotating field is shut off by using the data available indicator. If new data arrives between adjacent generator timing pulses, the down count is blocked so that the multiplexer doesn't miss the shifted data. If input data rate is equal to the rotating field rate, the rotating field will remain on continuously, but if the input data rate is lower, the rotating field will shut down periodically to allow the input data to catch up.

Mode control decoder. - Operation of the recorder (Section 2.3) is controlled by logic levels of three binary input lines which are decoded and used throughout the memory for specific control. (see Figure 16.) Mode control is a constituent of gate generation as illustrated in Figure 14. Low power latches are used to maintain the mode for long operations without requiring interface to be maintained. The truth table gives the conversion from the input lines to the desired signal lines.

Track counter. - When an erase or a search mode is initiated, the rotating field is turned on until the two chips in the track are completely erased or interrogated. The most significant bit of the counter gives the chip count which is a separate flip-flop with set-reset logic for nonvolatility consideration. At the end of a search operation the counter will have counted 10,223 field rotations so that the next rotation is a shutdown cycle leaving the mark bubble 15 bit rotations behind.

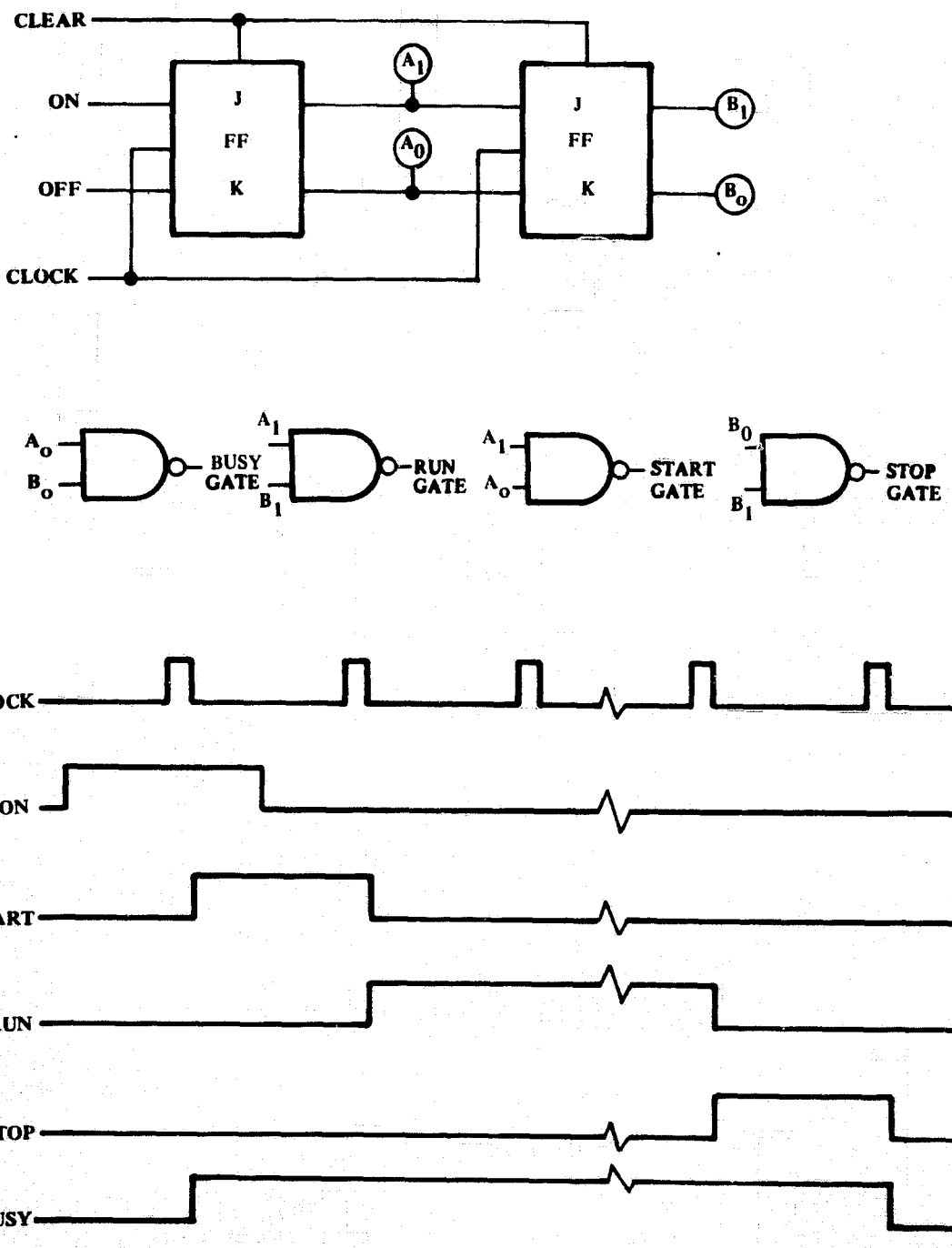


Figure 14. Run Control Circuit

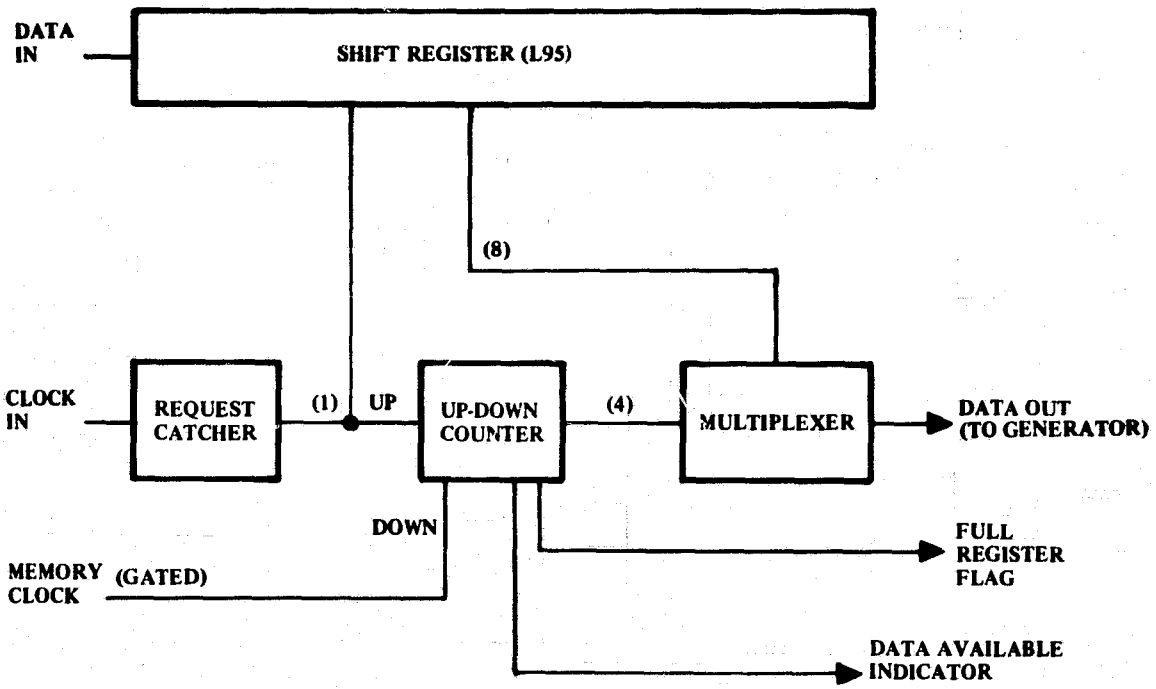


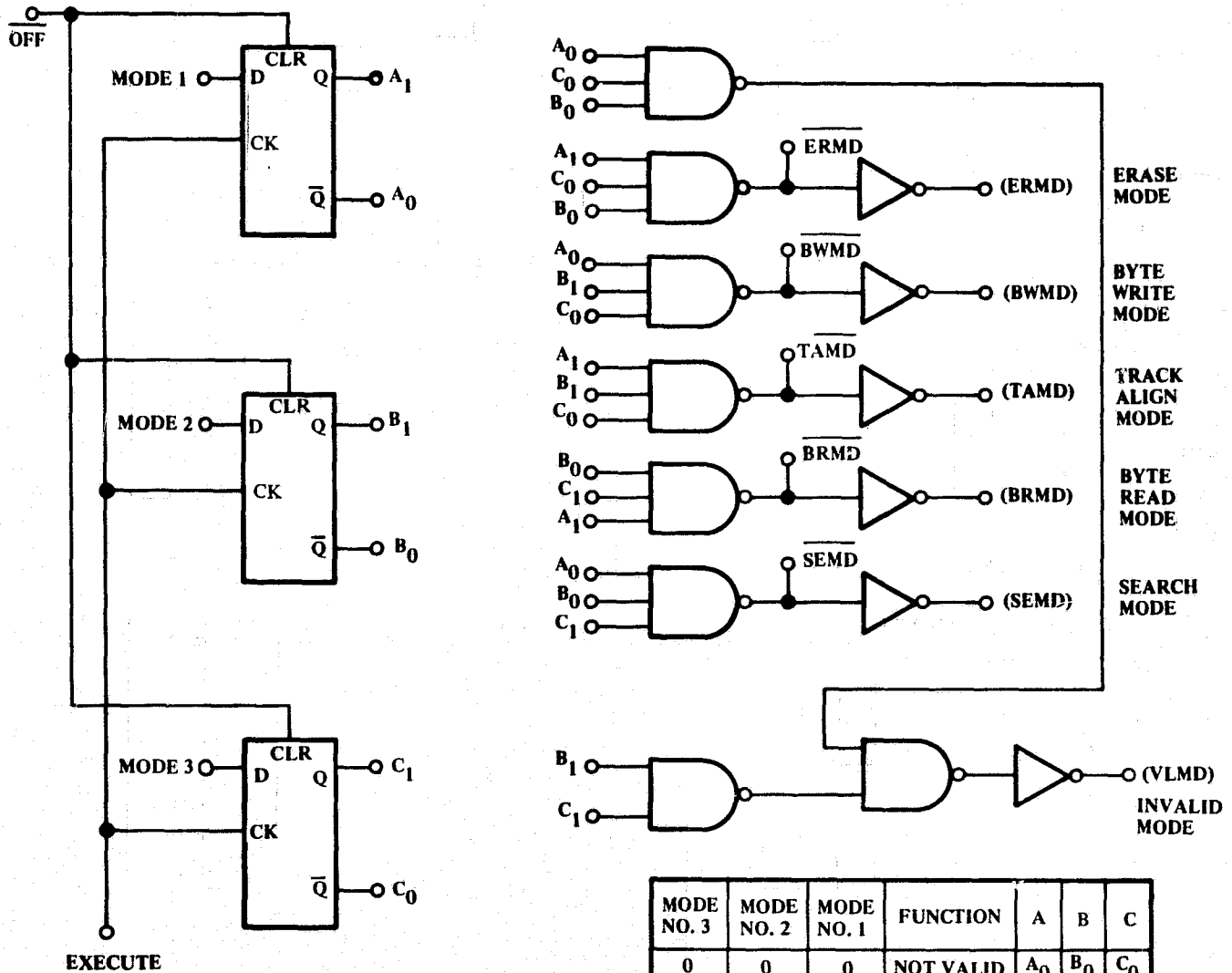
Figure 15. Async-Sync Converter

The track counter was designed using low power CMOS in such a way that the energy in the decoupling capacitors on the track board would maintain the count for several minutes when a power source or regulator without a bleeder shuts off. Implementation of the counter logic is inefficient in that two approaches were used to detect the end of count. Redesign is recommended before use in a prototype design.

4.3 Timing Section

Phasing and pulsewidth control for the recorder functions: driving, sensing, generation, and annihilation are accomplished by a timing section which is common to all tracks. Timing precision (hundreds of nanoseconds) is easily provided for by low-power TTL logic which has delay times of 20 nsec typically. The rotating field period is 6.67 μsec which is slow compared to the TTL flip-flop toggle rates. This makes possible use of a high frequency clock followed by a frequency divider. During evaluation of the feasibility model this timing circuitry was found to be power switchable, precise, nongliching and trouble free. Therefore it is recommended for a prototype.

Crystal controlled clock. - In order to preclude time displacement error (flutter error) and to provide accurate timing between recorded events, a crystal controlled clock was chosen to be the basis of timing for the complete recorder (Figure 17). The TTL level output signal from the oscillator is gated so that during turn-on of the recorder, and during the transition of the oscillator, the signal may be prevented from affecting any other function. Release of the gate is synchronized with the next clock pulse after the ON command goes high. The feasibility model has



MODE NO. 3	MODE NO. 2	MODE NO. 1	FUNCTION	A	B	C
0	0	0	NOT VALID	A_0	B_0	C_0
0	0	1	ERMD	A_1	B_0	C_0
0	1	0	BWMD	A_0	B_1	C_0
0	1	1	TAMD	A_1	B_1	C_0
1	0	0	SEMD	A_0	B_0	C_1
1	0	1	BRMD	A_1	B_0	C_1
1	1	0	NOT VALID	A_0	B_1	C_1
1	1	1	NOT VALID	A_1	B_1	C_1

Figure 16. Mode Control Decoder

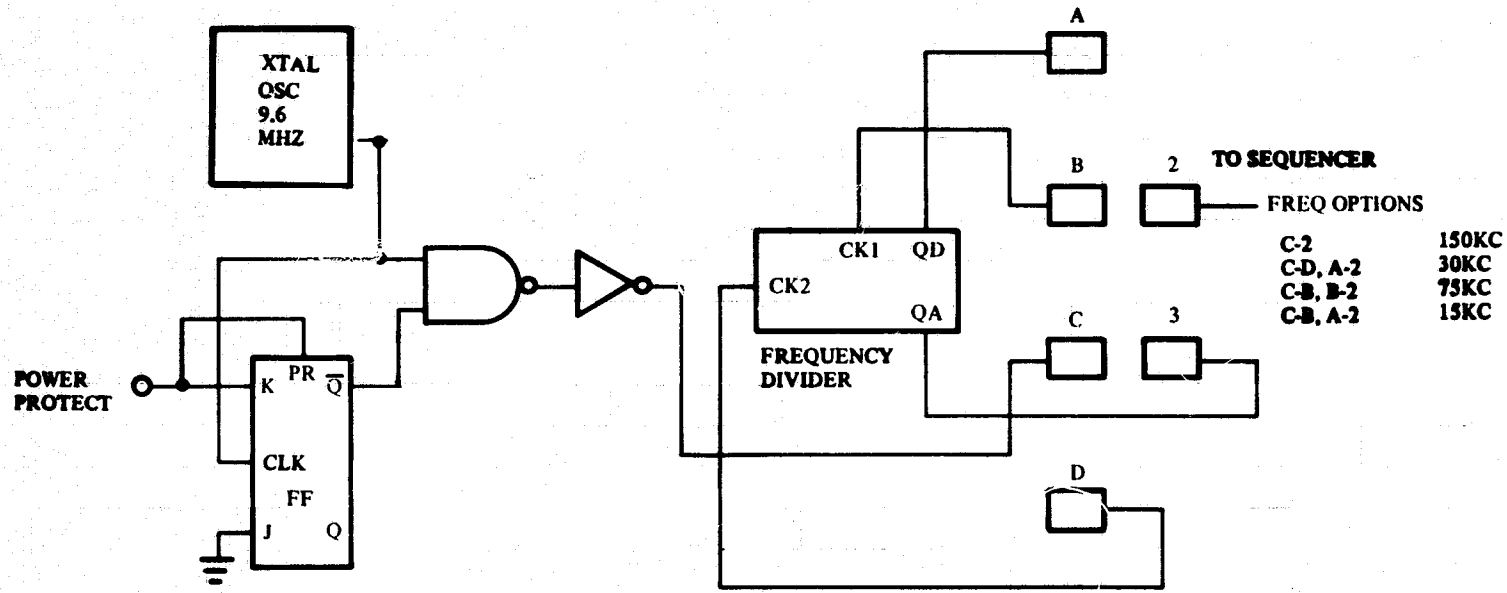


Figure 17. Oscillator and Clock Control

a frequency divider to provide optional rotating field rates. A problem encountered in the feasibility model was that when the oscillator was repetitively turned ON and OFF it could not be restarted for a very long time after the third turnoff. This restart problem was bypassed for the remainder of the feasibility model testing by connecting the oscillator directly to 5.2 volts. This is a potential problem which must be addressed during the design of a ptototype.

Sequencer timing. - The sequencer uses a series of lower frequency waveforms (which do not have coincident edges) to eliminate gliching and race conditions. Each stage of the three tier divider is a four-state counter circuit (Figure 18) where only one of the two flip-flops change state at each clock edge. By using one of the four states to clock the second stage, which in turn has one state as a clock for the third stage, a single field rotation can be resolved into 64 steps of approximately 100 nsec apiece. By selecting appropriate overlapping waveforms any pulsewidth at any phasing, within the 100 nsec resolution, can be generated. The circuit of Figure 19 has two stages per tier providing eight steps per tier for the second and third stage which gives more resolution without resorting to the first tier. The two stages are synchronized together directly through the J/K terminals and indirectly through the reset terminals. This precludes the possibility of the two becoming phased incorrectly and continuing incorrectly phased. If during operation of the divider the timing is purposely jammed by temporarily shorting any Q terminal, the timing will correctly phase itself by the automatic reset circuits when the jam is removed.

Timing Generation. - Timing for the sequencer is given in Figure 20. A sample of one of the approximately 15 timing signals is shown below the diagram (RCLS). For most of the signals only a two input gate is required and in no case was the first tier resorted to. The actual timing generated for the feasibility model is quite specific to that model and is appropriately given in the feasibility model section.

4.4 Interface

Normally in aerospace programs interface is rigidly specified by the users of memory to accommodate telemetry or processors. In the development of a stand-alone bubble memory the task is to choose a flexible enough interface so that most of these user needs can be met.

Signal levels. - When communications between boxes within a large system is interrupted by a power shutdown, the various boxes can be protected by the "buss high" concept where action can only be initiated by a logic low or current sinking level. To turn the feasibility model on requires a low on the "on" terminal for approximately 1.5 microsecond but only if the "OFF" terminal is low. Only an active device with current sinking capability can operate the recorder. To turn a track on requires a low "track on" for approximately 15 microseconds but only if "track off" is low.

Specifying operational modes. - Section 2 has a description of the seven modes of operation envisioned for a general purpose bubble recorder. To simplify interface and to eliminate the possibility of requesting two modes at the same time the mode control has a decoder so that the three input lines will specify only one of potentially

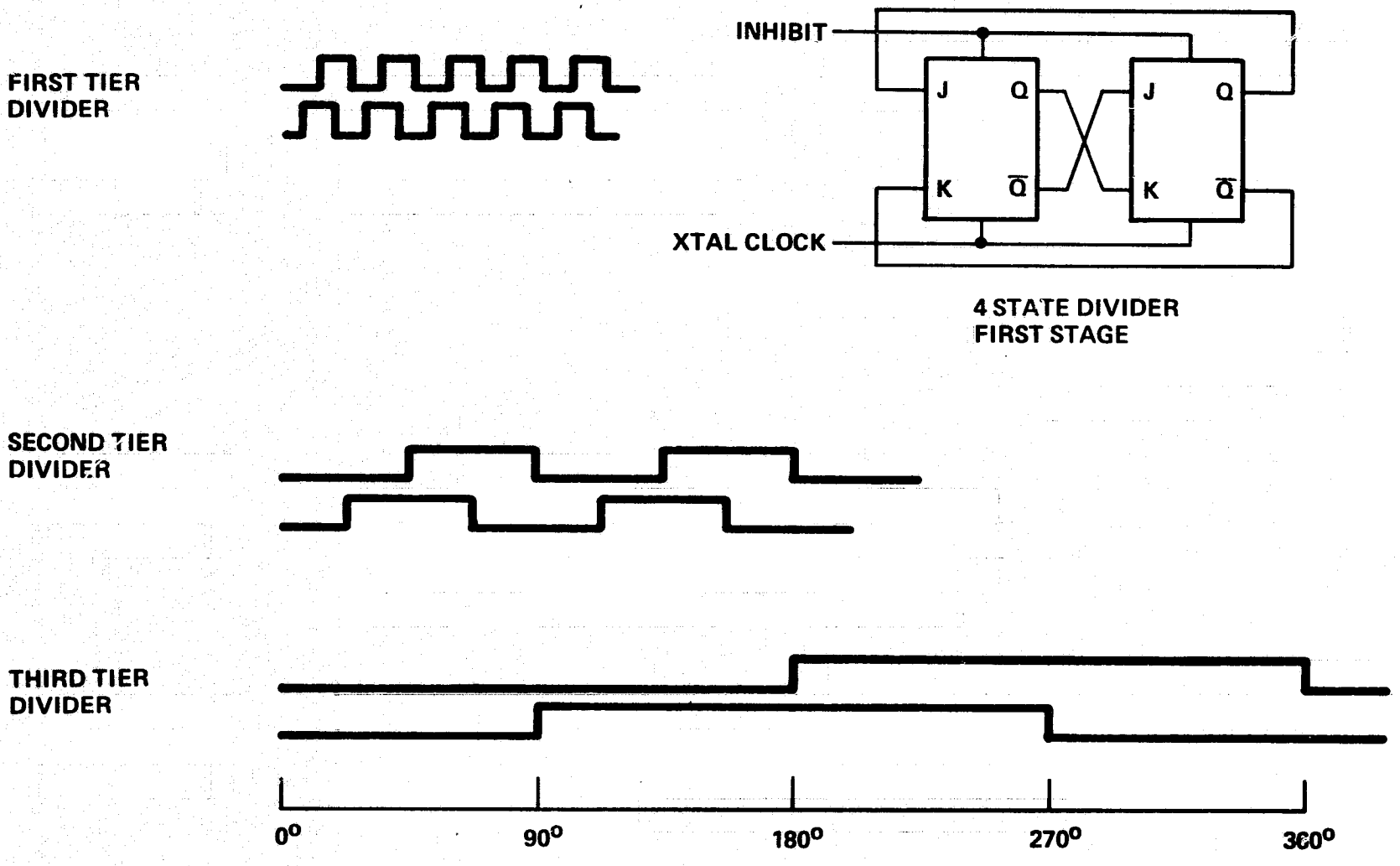


Figure 18. Timing Schematic and Diagram

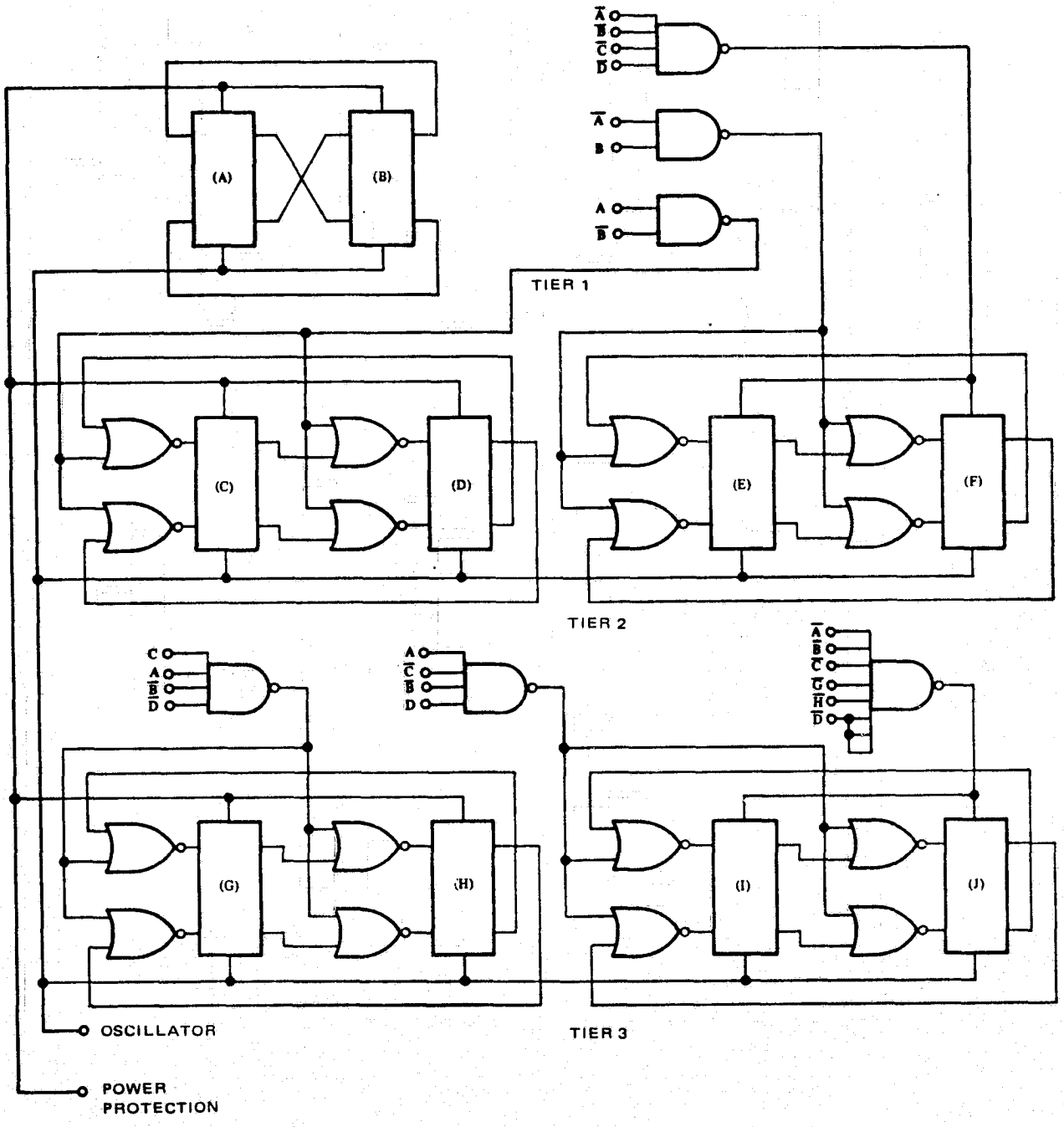


Figure 19. Sequence Timing Circuit

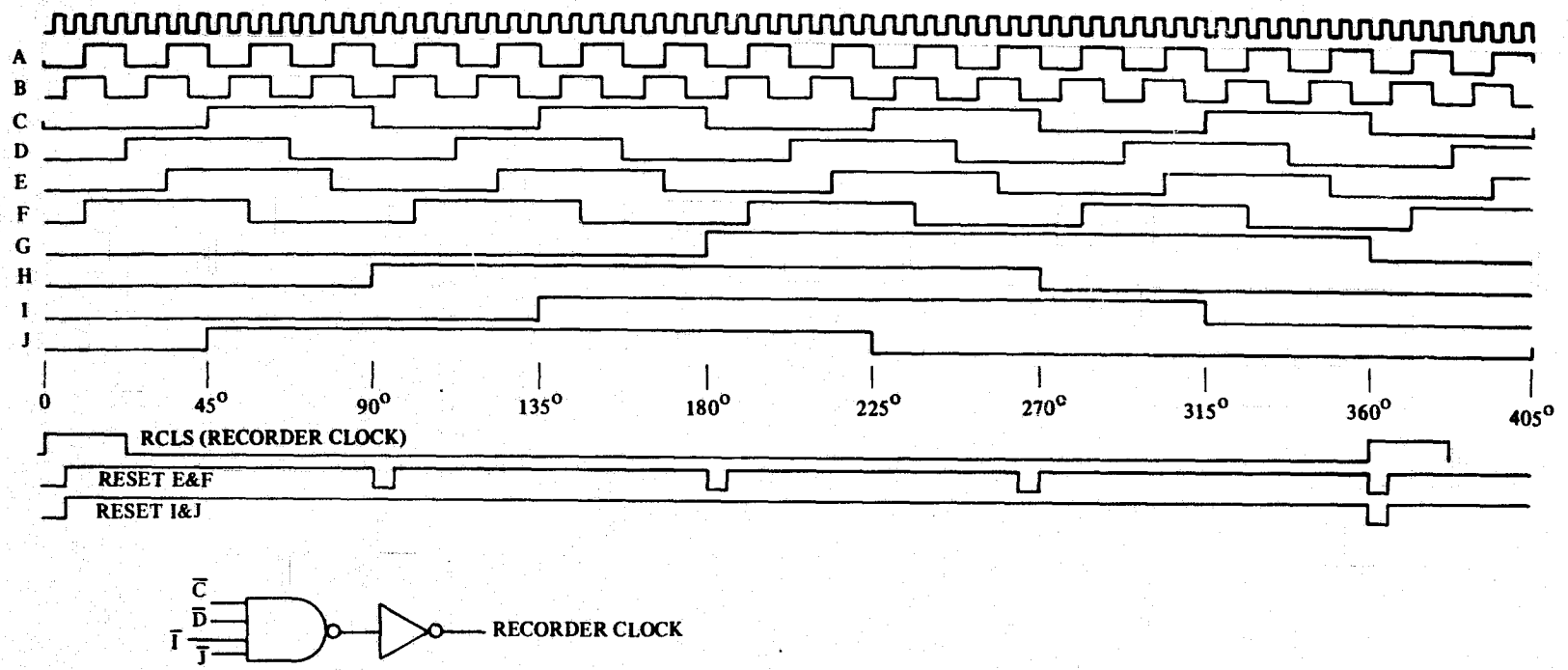


Figure 20. Sequence Timing

eight modes. Since the recorder may be operating for long periods of time in any particular mode these input signals are latched within the first 10 microseconds of the execute pulse which frees the controller for other tasks. When operating in this environment the controller will need to know the recorder's status.

Status indicators. - Status indicators are desirable from the user's viewpoint in some applications. For example a track full indicator provides the user with information as to which tracks of a multitrack system are filled; an alignment flag which occurs with a specific counter count allows the user to know when a block of chip size is filled; and a busy flag can be used to refrain from erroneously starting a new operation. The Busy flag and the track full flag were provided in the feasibility model.

Track turn on/turn off. - A contingency which affects interfacing to the feasibility model was a condition where there is data on the input register which must be put into the bubble track before the track is allowed to be shut down or before a new mode is engaged. The track must then be turned on first to run the data out before an off command will be acknowledged. Another situation was with the recorder on/track on control where the requirement is that a user must turn on the recorder which turns on some power to provide the clock; then to use the recorder he must execute an operation which turns on necessary sections within a track. Simplifying these user conditions (including commands for unscheduled power interruption) is a task that should be considered carefully at the beginning of a new design.

4.5 Sensing and Detection

A sense channel was designed for the NASA bubble recorder application so that the bridges and preamps could be selectively power strobed (Figure 21). In the serial track organization of the bubble recorder only one amplifier and one bridge need be turned on only for a duration sufficient to latch the signal. Major functions of the channel include the following:

1. A bridge and preamplifier which is located on the substrate in proximity to the memory chips.
2. A level shifter which provides termination for preamplifiers.
3. A capacitor voltage restore circuit.
4. A threshold detecting sense amplifier.
5. A strobed data latch.

Other considerations in the design include the reliable detection of submillivolt signals in the presence of noise and the amplifier and bridge voltage offsets. These considerations lead to the use of capacitive coupling between stages which unfortunately is susceptable to waveform averaging and is not amenable to power strobing unless the capacitors are discharged after channel turn on but before signal arrival. Typical detection circuit waveforms are shown in Figure 21. The upper photo shows the preamplifier being turned on in time for the bubble output portion of the signal envelope while the photo at the lower right shows the signal envelope at logic level and as it is latched into the data holding register. The detector signal after amplification by the preamplifier but without power strobing is at the lower left.

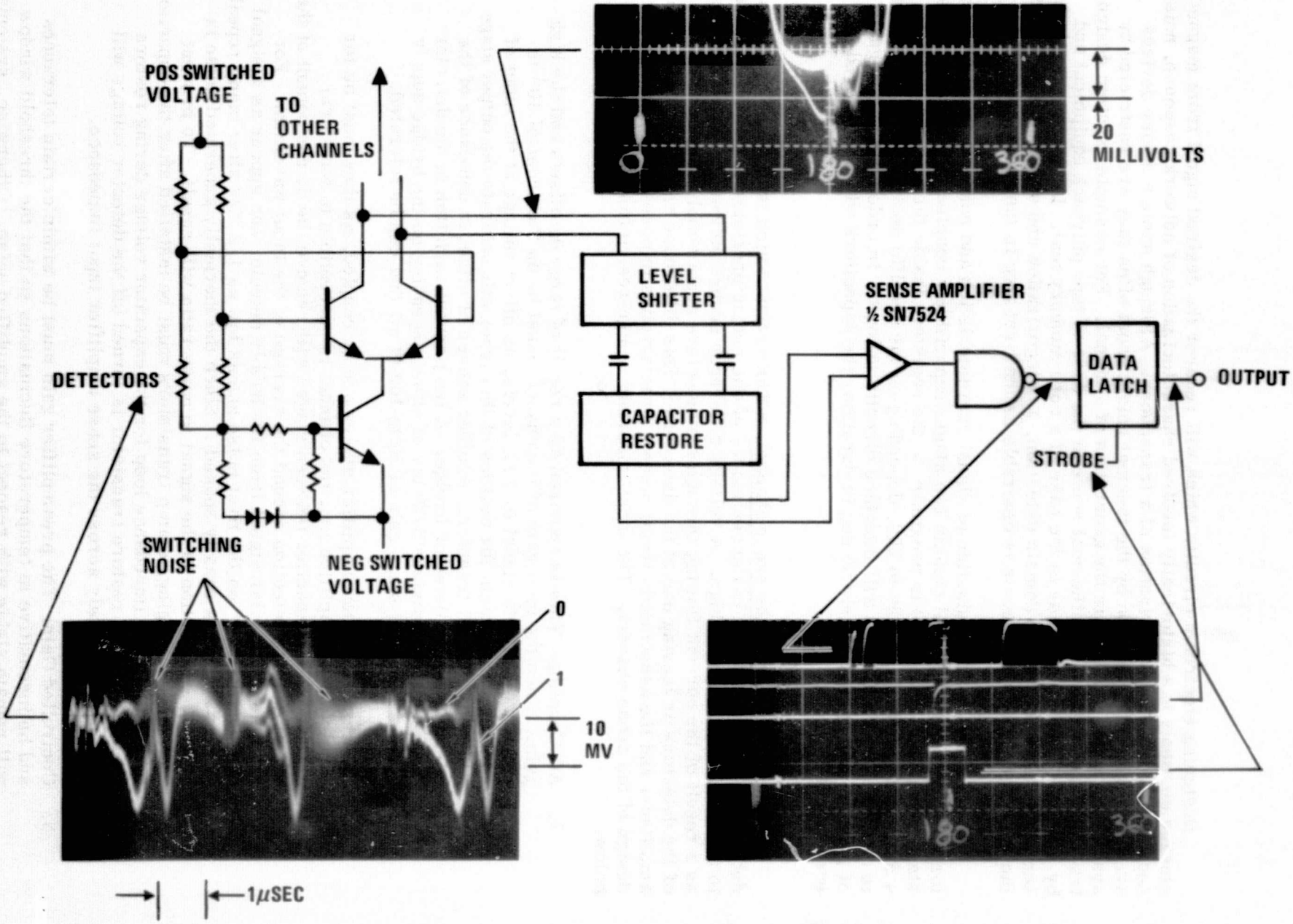


Figure 21. Detector Circuit and Signal Waveform

Designing electronic circuits which will recover the desired signal from magnetic storage elements has historically involved characterization of network response, noise sources, and the characterization of a transducer. Although some memory devices are restricted in application by the thermal noise, most often they are restricted by systematic noise produced in the generation of a signal. For example, system design tradeoffs are restricted by thermal noise in the case of tape playback equipment and by systematic selection noise in the case of a core memory mat. In pursuing a reliable sensing scheme for bubble domain detection, a categorization and a characterization of the observed signal components is desirable as the first step in the design.

As a result of the evaluation of signal characteristics and noise, a sense channel for submillivolt signals will contain two stages capacitively coupled together. The first stage (preamplifier) will be in proximity to the registers inside the coil and will have a differential gain of from 50 to 200, depending on the specific design. The next stage is a threshold detector and will interface directly to logic. In order to detect signals of greater than approximately 90 deg in duration, the capacitors will be restored in every cycle.

Characterization of the sense channel. – The variant which is detected in a bubble detector is due to a change in the resistance of one magnetoresistor element referenced to another in a common bridge. A voltage difference occurs between the two detectors as a result of the current flowing through the detectors and a bubble approaching one of the detectors or leaving one of the detectors. This difference signal (waveshape and amplitude) and the associated circuit noise characteristics impose restrictions on the design of the sense channel. The most important design restrictions are enumerated below:

1. AC Coupling: This is required as a result of large dc offsets and the high gain. Since the total gain of the channel must be on the order of 10^4 to amplify the bubble signal to TTL levels, an offset voltage at the input of 1 or 2 mv (minimum for devices of this type) will saturate the output stage preventing signal transfer. Another source of offset is unbalance of the resistors in the detector bridge. A ten percent variation in the detector resistance can produce 5-20 mv of offset depending on the bridge supply current. A first stage gain of 50 to 100 is all that can be tolerated.

2. DC Restore: When amplifier stages are ac coupled, as they must be for bubble signal amplification, the channel is susceptible to waveform averaging. A capacitor between stages will remove the dc component of the signal causing detection around the average of the input waveform. For example, a unipolar signal from the bubble detector can appear as a signal of magnitude "V" on the first pulse and as low as 1/2 "V" after many repeats (10^4 or so pulses equally spaced). Since the thermally generated noise is bipolar, a reduction in the signal to noise ratio will result. To prevent waveform averaging, clamp transistors must be installed after the capacitors to provide a low impedance loop for the capacitor voltage during restore time. When the restore transistor is turned off the detector voltage will drop predominately across the sense amplifier input impedance.

3. Controlled Gain: The preamplifier gain must be within certain tolerances and be insensitive to temperature fluctuations so that the threshold window will remain stable with respect to the amplified noise. Otherwise, systematic noise amplitude will be uncertain with respect to the threshold setting.

4. Threshold Detection: Threshold detection with a controlled reference will be used with or in the sense amplifier. For 2-phase detection, bubble signals can be either polarity depending on which detector has a bubble. Bipolar threshold detection is therefore desired.

Categorization of the signal components. - A categorization of noise sources expected in a bubble memory sense channel is an important consideration in the overall design and is, in addition, a prelude to an analysis of the bit error rate. A tabulation (and a discussion) of the various expected noise sources is given below, followed by an estimate of the bit error for a typical sense channel.

Signal components/Faraday pickup ($d\phi/dt$ noise) – This noise is a voltage which is induced in a loop of conductor whose cross section is exposed to the rotating field. The loop area, the frequency and the magnitude of the field, and the orientation of the field with respect to the loop all influence the magnitude of the noise.

To deal with $d\phi/dt$ noise in a multichip system, it will be necessary to design a controlled lead structure from the memory chip to the sense amplifier external to the coil package. Otherwise individual compensating networks must be provided per chip and they must be individually adjusted. The latter approach is undesirable in a system using a large number of chips.

In the feasibility model a cancellation circuit was used initially because of the $d\phi/dt$ pickup in the ceramic package. Establishing a d-c level by restoring the inter-amplifier capacitors has the effect of reducing the severity of the $d\phi/dt$ pickup since the rate of change is better than twice for the signal as it is for the maximum slope of the $d\phi/dt$ noise. The detector used for the feasibility model chip has a fast fall time edge which was found judicially placed for restore and strobing and which eliminated the requirement for cancellation despite the poor lead placement of the butterfly package. By using the strobing feature of the sense channel considerable relief from $d\phi/dt$ noise is expected but conversely by reducing the $d\phi/dt$ noise component in the sense signal budget considerable improvement in error rate is expected. ($d\phi/dt$ noise control is still necessary.) For the feasbility model a reasonable value for this noise component is approximately 50 mv peak at strobe time.

Signal components/cross-coupled noise. — Whenever large currents at high frequency flow in proximity to a sense line, or whenever a large voltage exists between the sense line and other conductors, the possibility exists for systematic noise coupled into the sense channel. This type of noise can be discerned in the lower left photo of Figure 21 as the repetitive portion of the waveform in synchronization with the trace. At strobe time (upper photo) the trace is relatively clear even when generating or annihilating a bubble. In setting up the sense channel the only region which should be kept free of this kind of systematic noise is the time after restore release and before strobe.

Signal components/detectors switching noise. — As the magnetization in the two detectors of the bridge is rotated, non-linear switching transistions occur which give a random output signal. The lower left photo in Figure 21 suggests that the randomness occurs within a narrow time duration mostly outside of the restore to strobe window. This behavior is similar to that reported in thin permalloy film detector. (Ref 6)

Signal components/bubble-bubble interaction. - Depending on the pattern design for the detector and the associated track design, the field which a magnetoresistance detector is sensitive to is a superposition of bubble fields from several bit positions away. In determining the minimum "one" signal for an estimate of detector error rate, consideration must be given to this effect.

Signal components/thermal noise. - The usual technique employed in the determination of total noise and the bandwidth limiting effect as the noise passes through a sense channel is that sources have a specifiable value of noise power per infinitesimal unit of frequency or a noise spectral density. By integrating the noise spectral density for the various sources over frequency the noise power is obtained. Figure 22 shows results (thermal noise only) for a 733 amplifier, a detector resistance of 100 Ω, and a bandwidth equal to the center frequency. For the flight recorder sense channel using a CA3005 preamplifier limited to about 670 kHz in bandwidth the thermal noise is expected to be about 5 μv rms at the output of the preamplifier.

Detection error rate. — In the assembly of large bubble memories containing many chips within a coil and many coils, it is inconceivable that chips be connected to individual cancellation voltages or that they be tweaked individually. Therefore, to analyze the bit error rate a composite of all chips' signals must be considered. Figure 23 indicates how this composite of signals and the systematic noise is to be treated. Consider what happens when the threshold of the second stage of amplifier is adjusted from 0 volts to a voltage which exceeds the maximum amplitude of the bubble signal. At zero volts the systematic noise is detected in addition to the bubble signal. As the threshold is increased fewer and fewer no-bubble errors are detected and when the voltage reaches the threshold of the systematic noise, the probability of correct determination of the absence of a bubble is 50 percent as a result of the random noise. Increasing the threshold will reduce the error rate further until a minimum is reached. Above this minimum the bubble read errors begin to increase until right at the signal minimum minus the systematic noise maximum, 50 percent of the bubble will be missed.

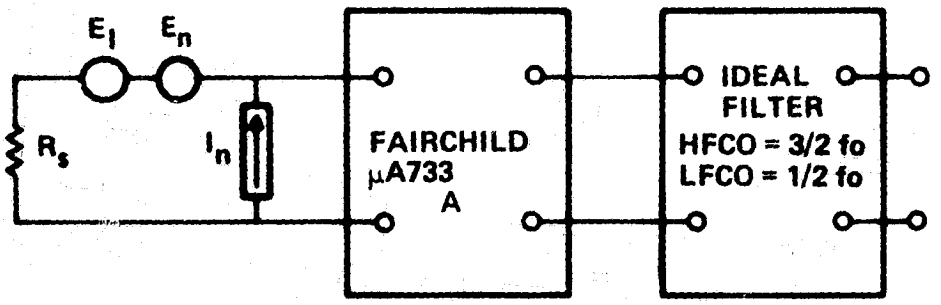
So far the results of the feasibility model testing indicate the principle contributor to the error rate is magnetic switching noise. An error rate of less than 10^{-10} errors per detection for individual chips was measured for the feasibility model at 150 kHz rotating field rate. The failures include about 50 percent false ones and 50 percent false zeros indicating that the threshold setting was in the valley of the detection curve (see Figure 23). After 10^{+9} field rotations (2 hr at 150 kHz) no hard errors (moved, missing or extra bubbles) were found.

Evaluation of signal waveforms show typical output to be 400 μv, systematic noise of 100 μv peak, and nonsystematic noise of 18 μv rms. The switching noise (15 μv rms) is assumed to be random within the channel bandwidth. For these conditions the calculated rate is approximately 10^{-8} errors per bit

$$[(E_o - 2V_{sys})/2V_n \text{rms} = 5.5\sigma \text{ or } \simeq 10^{-8} \text{ errors.}].$$

It should be emphasized that these results are for only a single chip. Results for the testing of composite signals (which will be covered in Section 10) show more total systematic noise for many chips in the same package.

SENSE CHANNEL THERMAL NOISE



THE SENSE CHANNEL NOISE MODEL

$$\left(\frac{V_{OUT}}{A}\right)_{RMS} = \sqrt{\int_0^{\infty} \left[E_I^2 + E_n^2 + I_n^2 R_s^2\right] \left[T_R(f)\right]^2 \, df}$$

THE EQUATION FOR UNCORRELATED SOURCES

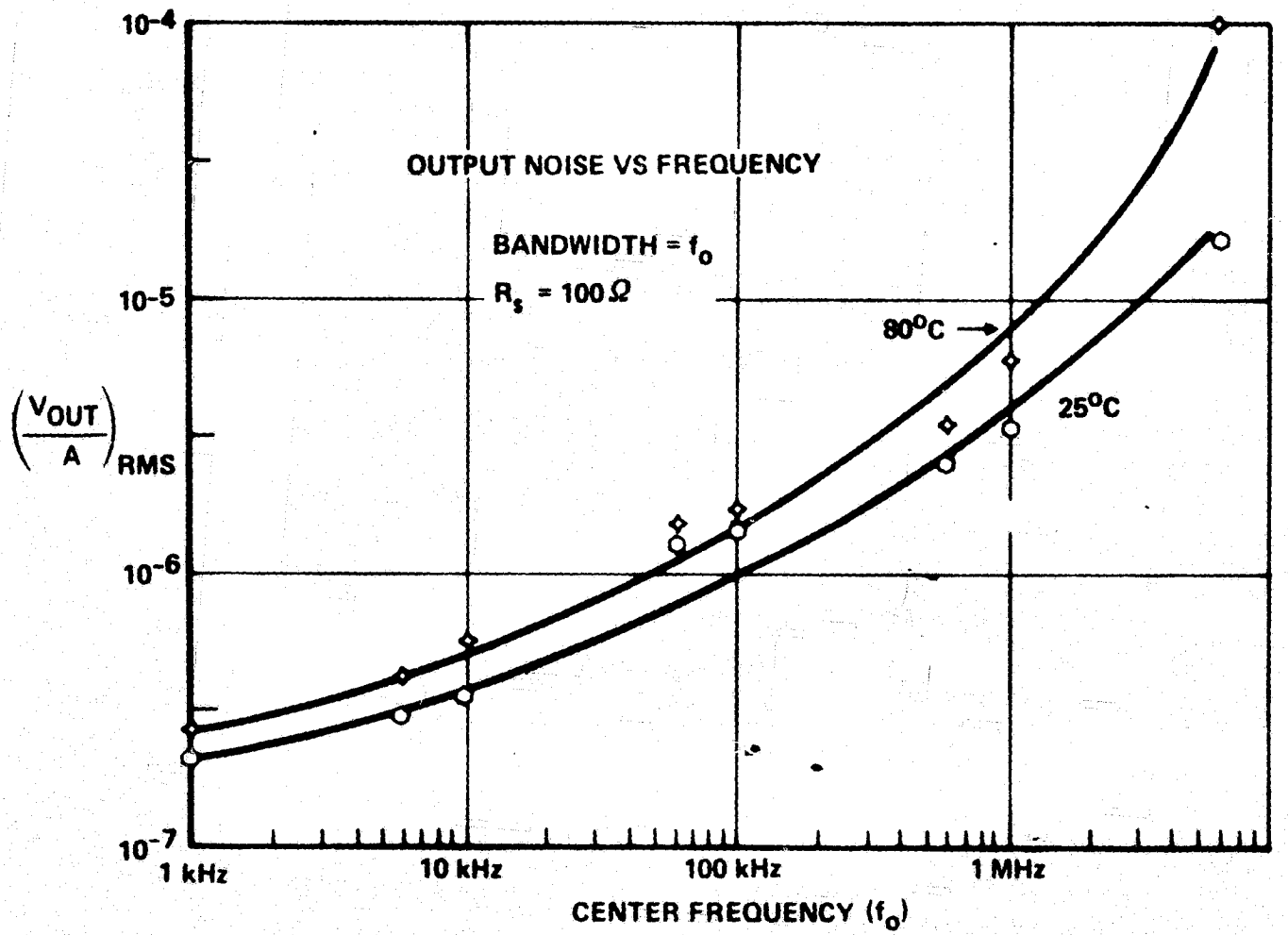


Figure 22. Thermal Noise Model

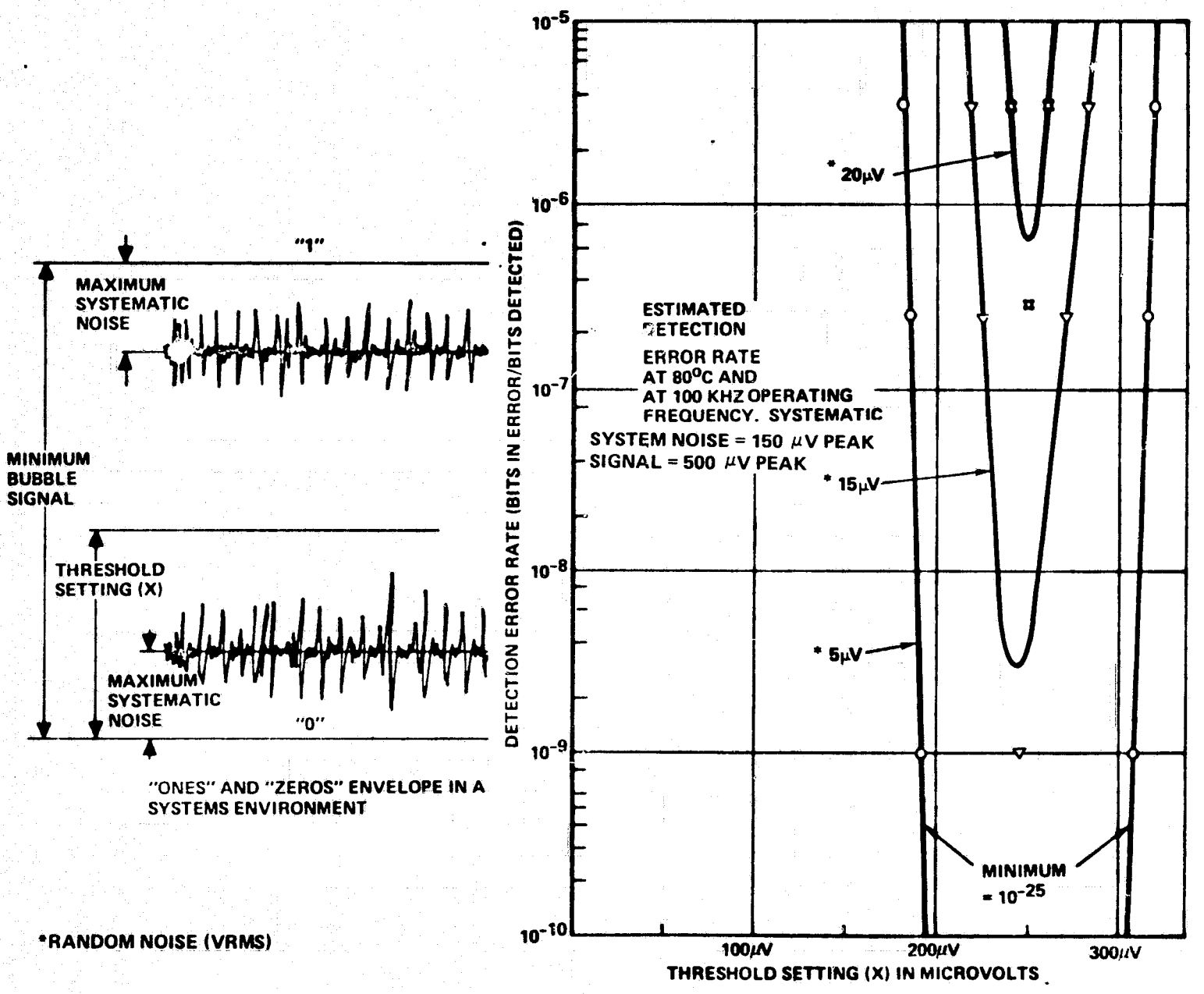


Figure 23. Detection Error Rate as a Function of Detection Threshold

Worst case sense channel calculations. - The factors which presently are known to affect (or which have affected) sense channel margin are listed in Table I. Subtracting the systematic noise from the minimum composite signal gives the minimum sense amplifier input "1" signal while the total systematic noise is the maximum "0" signal. Halfway between, allowing for threshold variation, will be the best threshold setting. Notice that the setting will be compromised for thermal effects as well as for composite signal effects. Nonsystematic noise power is totalled over the bandwidth giving the deviation of the probability distribution and the bit error rate.

The detection scheme used for the feasibility model is given in Figure 24. Gain for the feasibility is nominally 68 ± 4 for a ±25°C temperature variation and bridge current is nominally 3 ma in each detector.

Sense channel response. - A complete sense channel with preamplifier, restore, and sense amplifier was set up to evaluate the channel's frequency response as a prelude to the actual implementation in the feasibility model. Figure 25 shows the results for the conditions of injected sine wave on the bridge, first without DC Restore, and next with the DC Restore. Notice that the applied signal at a higher frequency will transfer through to the sense amplifiers (lower right) even if the restore is on 100 percent of the time. When a shunt capacitor is added across the sense amplifier input, the higher frequency components are attenuated as shown by the dotted line. Putting 16 preamplifiers in parallel had the same effect. The voltage follower attenuates the signal slightly as expected. The feasibility model has PNP's as level shifters and followers instead of the NPN's used in the breadboard.

Preamplifier power dissipation. - Dissipation in the preamp and bridge is (for 150 kHz) below 7-8 milliwatts because of the bridge current and preamp current sharing technique, the low duty cycle, and the inherently low power of the simple differential pair.

4.6 Annihilation and Generation

Bubble annihilation and generation is controlled by the signal levels from the control section and timing signals from the sequence board.

Except for logic, the circuits used to produce the current pulses are all similar to the one shown in Figure 26 for Gen. 2. The driver is connected as a current source to eliminate the loops' resistance variation from the current regulation equation. A medium power gate with high voltage capability is required to sink the expected control current of the PNP transistor. The "gliching condition" which occurs on turn-on or turn-off is prevented by the RUNG (RUN GATE) which is logic low and sinking current during power transition. The "or" gate was chosen to force the timing signal to sinking current (inverted signal) when a generator current is desired. An open or "dead" interface will not produce current.

Although this circuit is satisfactory for the feasibility model, several objections can be raised on its use in a prototype system. The first is that the collector current is dependent on a dividing network which is supply voltage dependent and base current limited. The second is that the current is linearly dependent on supply voltage variations which could impose undue margin requirements on the memory element operation. A better method is shown in Figure 27. The driver is a NPN transistor whose base voltage is controlled with respect to the negative supply by a common reference. This

TABLE I

HYPOTHETICAL[1] WORST CASE SENSE MARGIN

	25°C -ΔT		25°C		25°C +ΔT		Units
Detector output (Min)	450		500		550		μv
Timing jitter degradation (Max)	50		10		50		μv
X/Y field signal degradation (Max)	20		10		70		μv
Bit-bit interaction (Max)	20		5		50		μv
Cross coupled noise (Max)	10		10		10		μv
dϕ/dt noise (Max)	20		20		20		μv
	Max	Min	Max	Min	Max	Min	
	0	1	0	1	0	1	
Preamplifier input voltage	50	330	35	445	90	350	μv
Preamplifier output voltage	2.5	17.5	1.7	22.2	3.3	16.5	mv
Sense amplifier input (After Attenuation)	2.3	15.7	1.5	20	3.0	15	mv
Sense Amp input adjusted for threshold uncertainty	4.3	14.7	3.5	19	5	14	mv
Best setting for threshold[2]	9.5		11.2		9.5		millivolts
Thermal noise power/√~ (detector)	1.2×10^{-18}		1.6×10^{-18}		2.1×10^{-18}		$(volts)^2$
Thermal noise power/√~ (I_n for Amp)	10^{-22}		10^{-22}		10^{-22}		$(volts)^2$
Thermal noise power/√~ (V_n for Amp)	10^{-18}		10^{-18}		10^{-18}		$(volts)^2$
Nonsystematic switching noise/√~	5×10^{-16}		5×10^{-16}		5×10^{-16}		$(volts)^2$
Total nonsystematic noise (RMS) at sense amp input	1.0		1.2		1.4		mv
Bit error rate failures/bit	10^{-7}	10^{-7}	10^{-8}	10^{-8}	10^{-4}	10^{-4}	

[1] The numbers used are hypothetical. The table is for the purpose of identifying factors in a worst case analysis.

[2] for this case 9.5 is the best overall compromise.

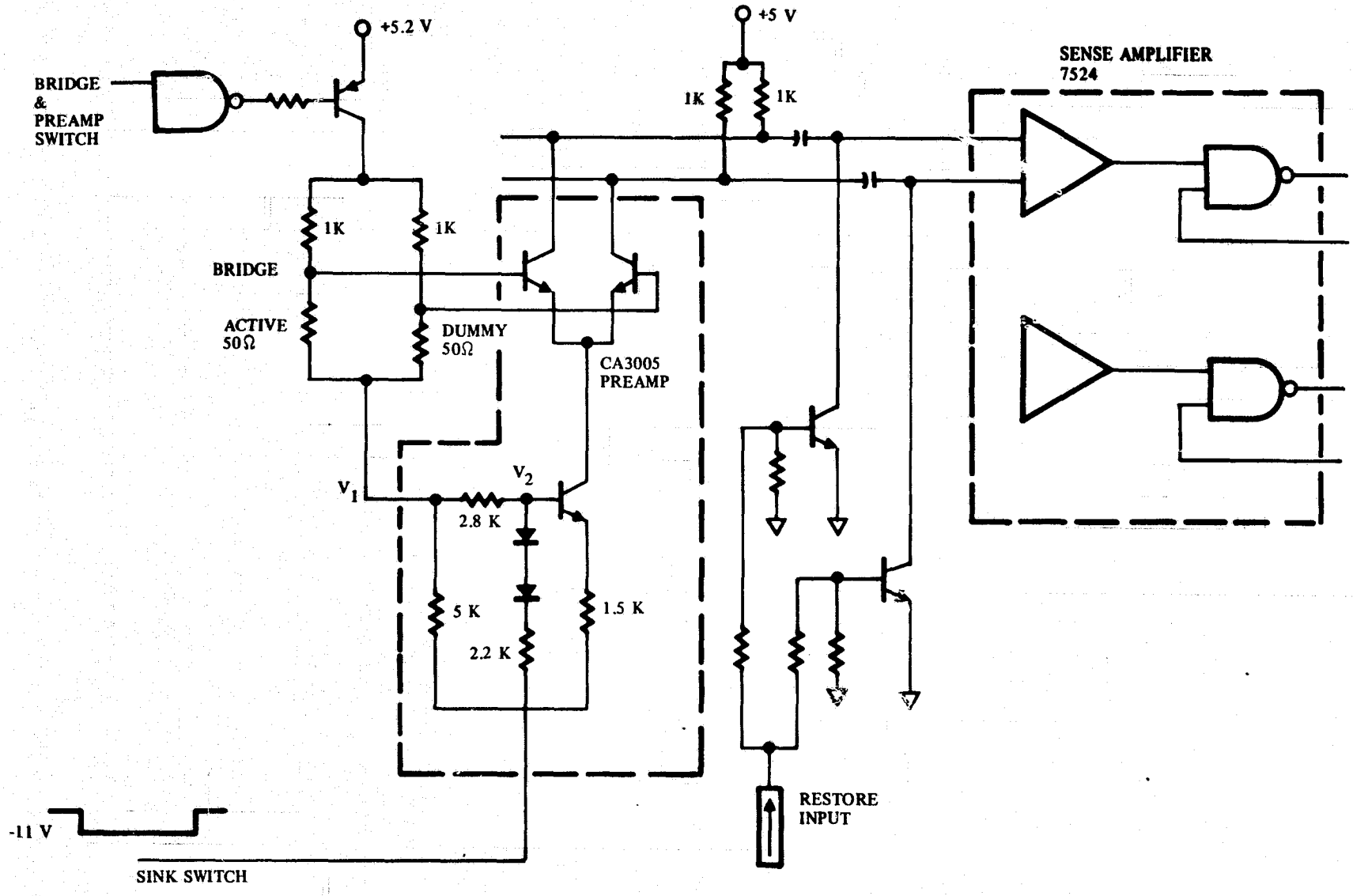


Figure 24. Detection Scheme

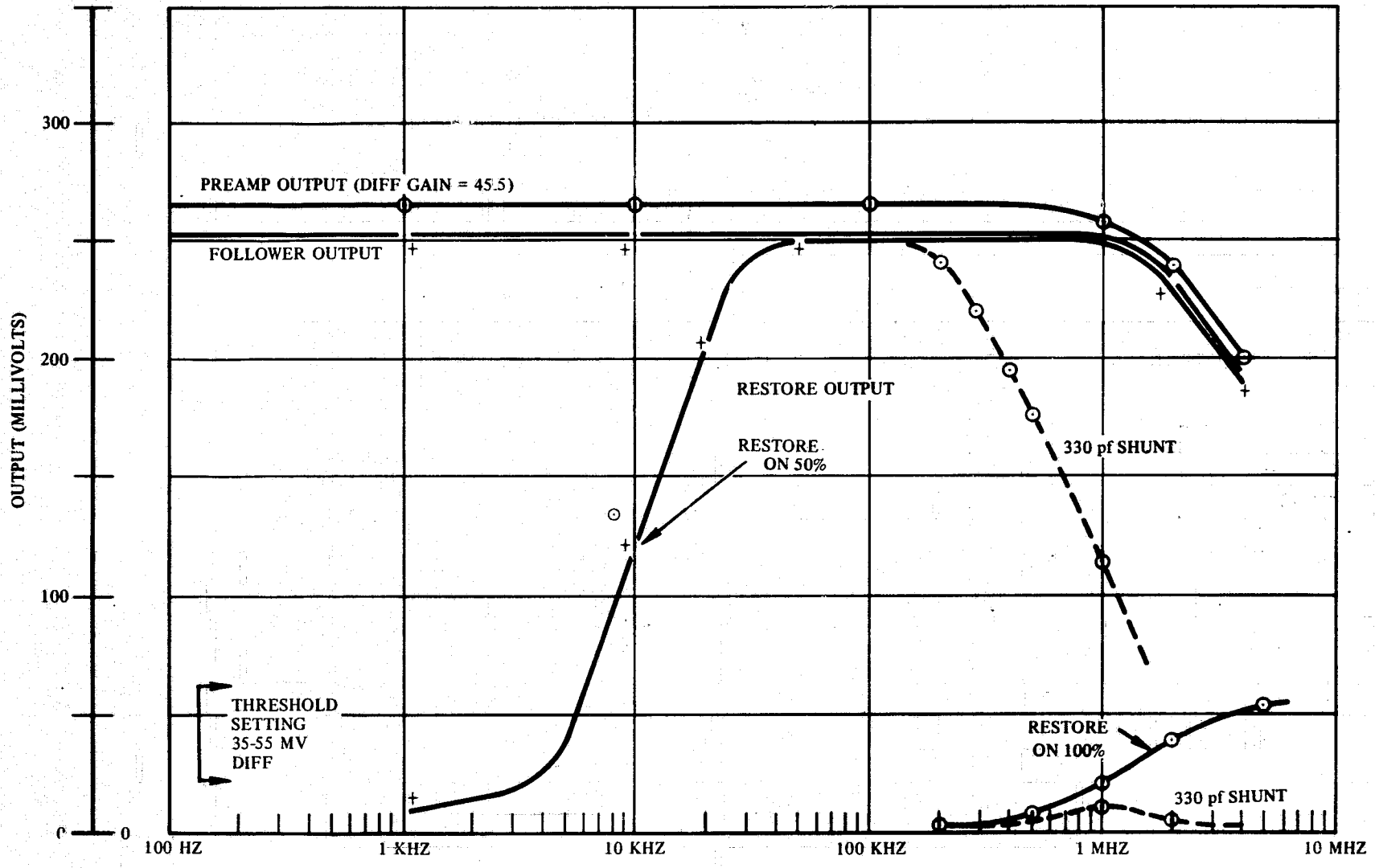


Figure 25. Sense Channel Response

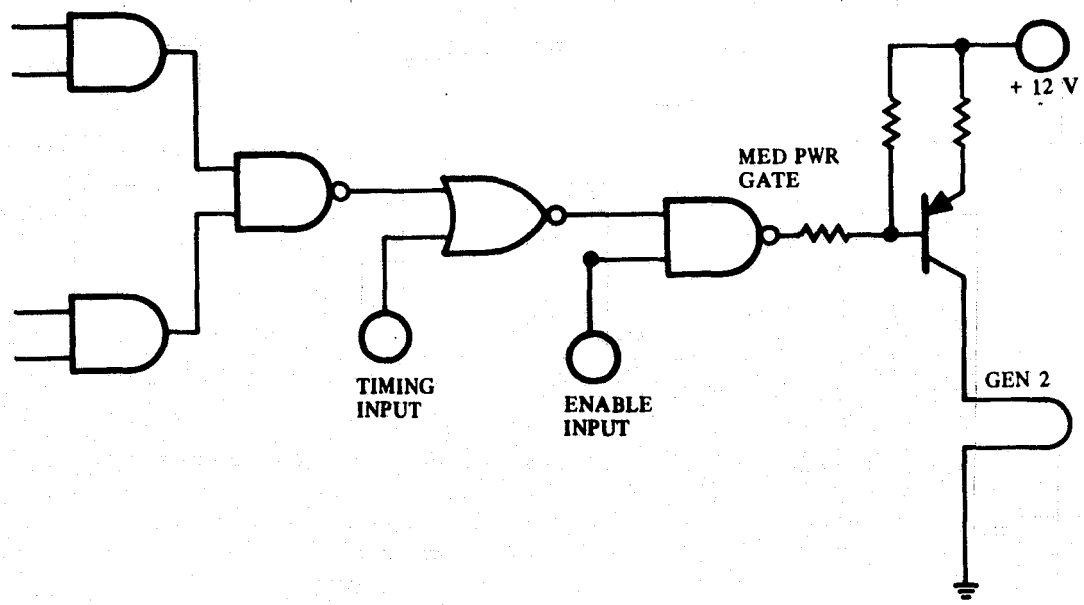


Figure 26. Circuit Topology used for Annihilator/Generator

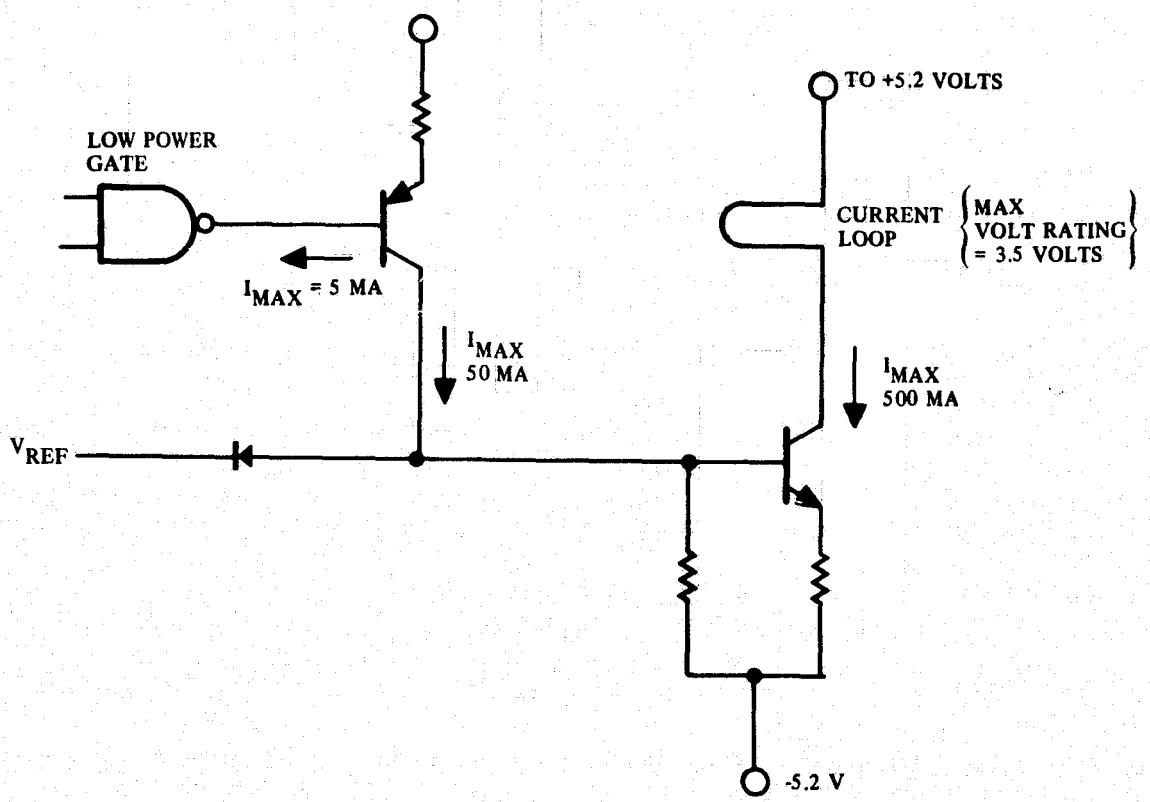


Figure 27. An Improved Current Loop Driver

will be derived from a zener diode connected to the negative voltage and turned on only during use. A low power low voltage gate is all that is required for pulse generation, a benefit of installing an extra transistor in the circuit. This arrangement is especially useful in connection with the matrix concept for the chip associated electronics discussed in the prototype recorder design (Section 9).

4.7 Coil Driver

Before describing individual circuits, the principles involved in the feasibility model driver and tank circuit will be explored. The coil and the capacitor are paralled in this design so that, for a high Q circuit, the impedance of the tank circuit ($|Z_{IN}|$ of Figure 28) will be high compared to typical semiconductor switch impedances in the driver circuitry and in the power supply.

In an ideal series circuit all pass elements, including leads, must be capable of carrying maximum coil current. Their drops, plus the sum of the semiconductor junction volt drops (0.6 volts x the number of junctions), times the current is the instantaneous power dissipation. Because of semiconductor junction characteristics, the power dissipation will not drop linearly as a function of increasing coil Q. Practical mechanical considerations dictate a reasonable length of cable (6 inches) from the coil to the driver which is another potential source of dissipation.

On the other hand a parallel circuit of high Q requires very low current from the driver making possible lower dissipation in the pass elements as Q is increased. The tendency is as Q increases the lower the current and the lower the dissipation in the driver, pass elements, and power supply. For low power application where a high Q coil is used, the parallel tank circuit appears the most satisfactory. It is not just the dissipation of the coil that is important but the dissipation of the whole function of X/Y field generation which includes the drive circuitry.

To exploit the advantages of a parallel tank circuit it is preferable to place the tuning capacitors close to the coil on the same board, so that no large instantaneous currents flow in the cabling during field rotation.

One concept that was evaluated in the feasibility model is the idea that energy lost in the coil need only be replenished periodically. This allows use of single polarity saturated switches as drivers (see Figure 29) instead of the cumbersome bi-polar linear type. This switch is turned on for only 180 deg which leads to the simplified circuit of Figure 29 having the following characteristics:

1. Two supplies are required: -V and +5 volts.
2. One drive transistor and 1 predrive transistor are required.
3. Storage time variation is still possible. A high speed transistor is required with provision for base charge removal.
4. It can be started in one polarity.
5. Idle power is zero except in the gate which is in its low power state.
6. The predriver power is reduced by using a dual level current source. The first level supplies a large amount of charge to turn on the drive transistor quickly.

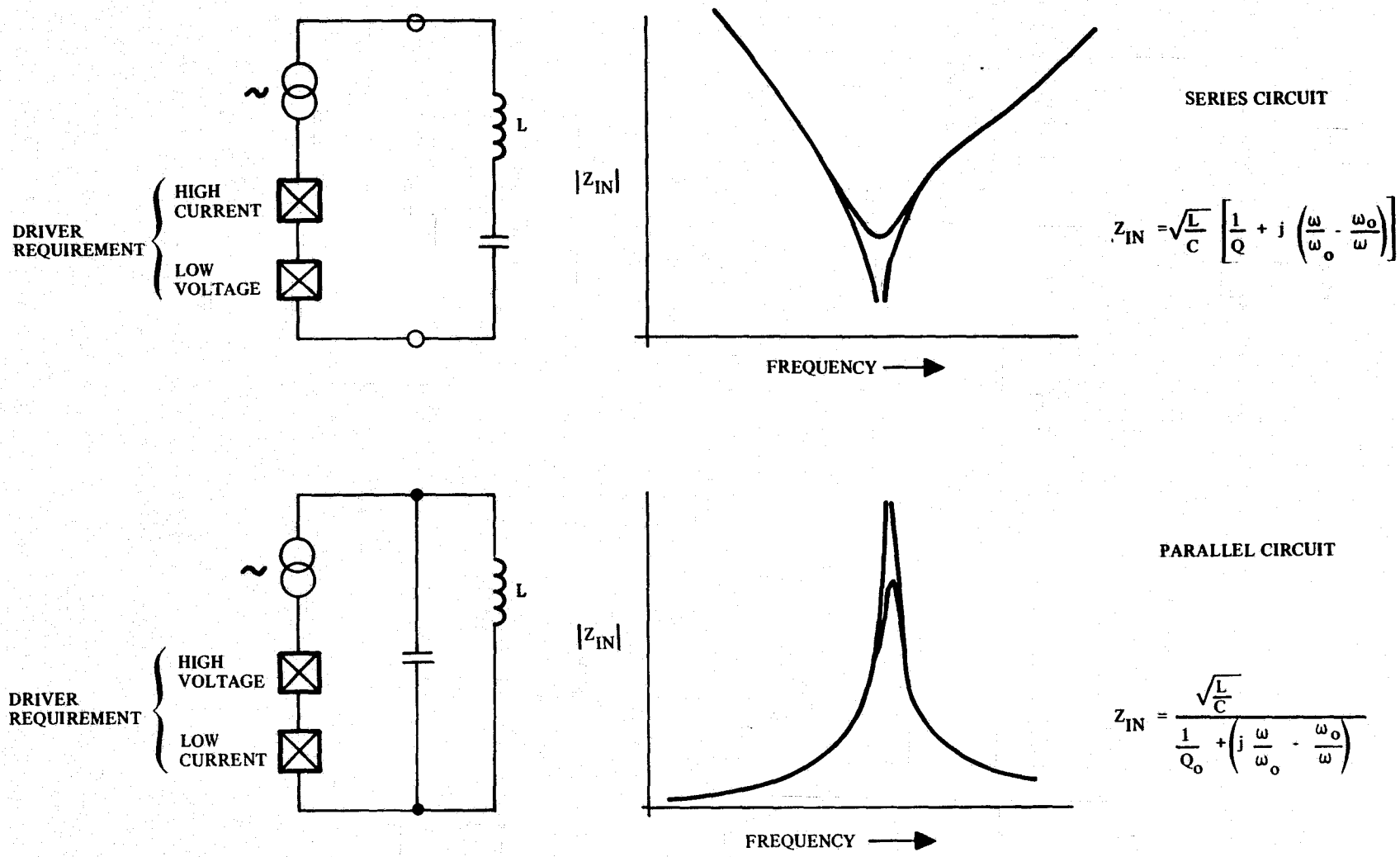


Figure 28. Series and Parallel Resonance for Coils

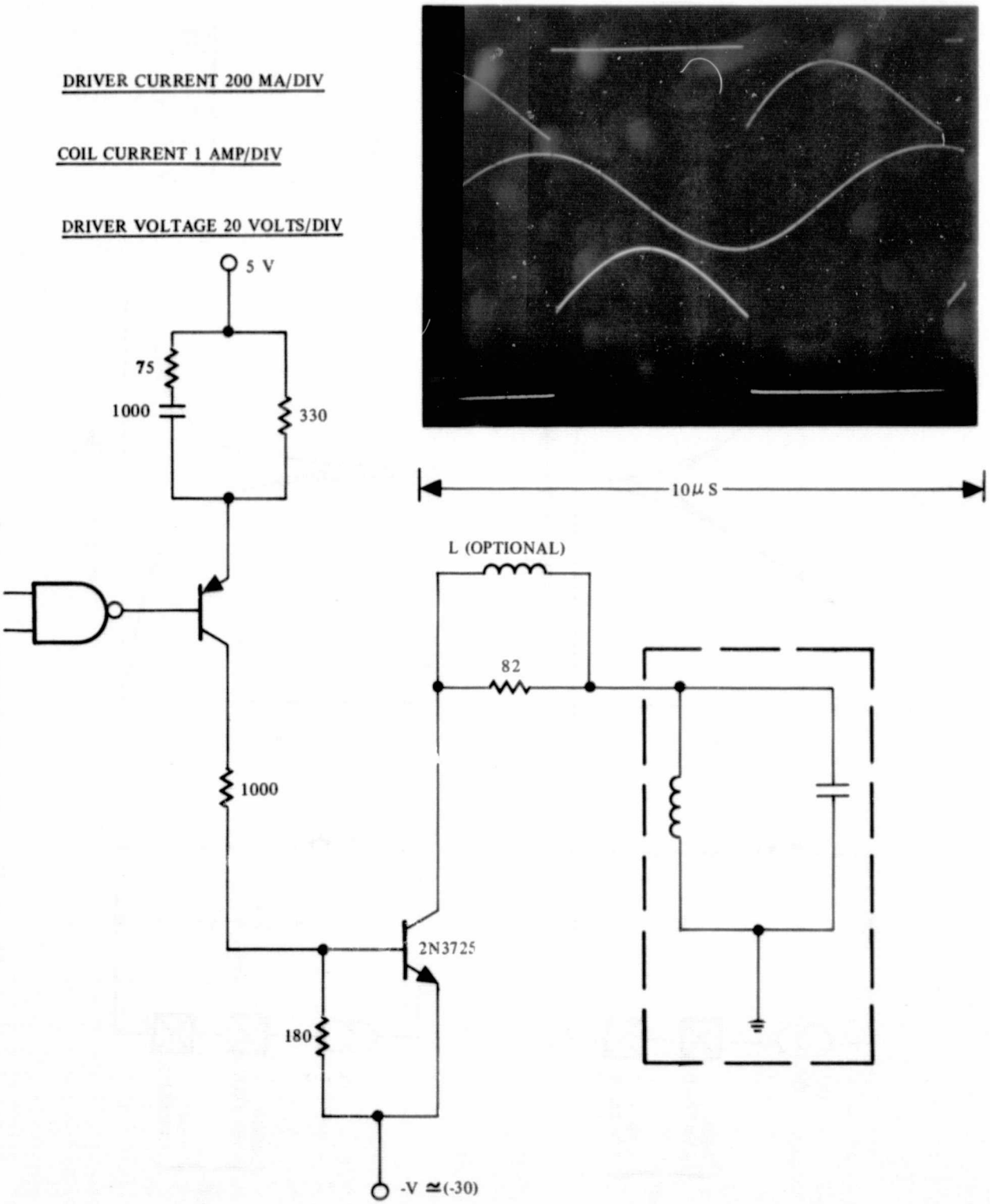


Figure 29. Coil Driver Circuit

Other effects were considered in the design, such as the effect of coil Q on frequency stability. If the Q is high, a small excitation will cause the coil and capacitor to oscillate at their characteristic frequency but not necessarily at the driver's frequency, resulting in a long time before equilibrium is reached between the two. Another effect is that if Q is low, an effective DC current flows in the coil as a result of the unipolar driver. Neither of these effects were thoroughly evaluated in the feasibility model study except as provided for in operational tests over temperature. The feasibility model coil has an approximate inductance of 14 μH and a Q of 8 to 10.

Drive electronics. - The essential features of the drive electronics is given in Figure 30. A current source is used to initially start the coil by charging the capacitor according to the rate ($dv/dt = I/C$). Charging the capacitor with current source is preferred for speed over precharging the coil with a voltage source which is supply voltage limited.

The run circuit is a saturated switch with a current limiting network in the collector and which, in the feasibility model, is turned on for 180 deg. Without the limit network, the current waveform would be excessively distorted. The stop circuit is a resistor paralled with the tank and switched on during shutdown. The clamp circuit is more extensive than shown, requiring a provision for effectively removing the saturation drops.

Selective testing of the circuit was done at room temperature using a breadboard and the feasibility model. A good opportunity was missed by not exploring the possibility of minimizing the driver pulsewidth so that the collector network could be eliminated. Figure 31 gives the timing relationships between coil waveforms, driver waveforms, and a polar representation of the rotating current vector.

A consideration which must be made in the design is the availability of capacitors with desirable characteristics for use in the tank circuit. The range of application is limited on one side by bulky, unstable capacitors and, on the other side, by the coil's own distributed capacitance. Polycarbonate capacitors were chosen for the feasibility model primarily for their specifications on value stability over temperature and, secondarily, for their small size and low loss.

Another consideration is for the breakdown voltage, speed, dissipation, and current capability of applicable and readily available components. A breakdown of 60 volts, power dissipation of 600 mw, current of 0.5 amps, and F_t of 300 MHz characterize the common, low cost electronic components (diodes transistors, capacitors and resistors). Parts can be found within this range that are NASA approved, small, and that are widely used. When component performance disgresses much from the baseline characteristics, cost, reliability, power dissipation, or size become impacted. An example of this idea is shown in Figure 32. This is a summary of the $F_t \times V_{ce}$ product vs cost for switching transistors. The higher the product, the better the performance overall in terms of power dissipation and voltage handling capability. Notice that small improvements in performance are costly and notice also that the very commonly used 2369 transistor is the highest performance of the lowest cost end of the range.

Start circuit. - The start circuit is a current source capable of delivering 1.5 amp for 1 μsec. In the feasibility model 2 discrete transistors (2N3725's in TO-5 cans) were used to provide experimental flexibility but in the prototype restricted to a number of cycles between starts, a single transistor of a package will suffice.

Run circuit. - The run circuit is a saturated switch designed for low power dissipation. Unlike the start/stop circuits which are duty cycle limited, the run circuit must be used in every cycle. This requires a circuit such as in Figure 33 which has a low power predrive as well as a low power saturated driver.

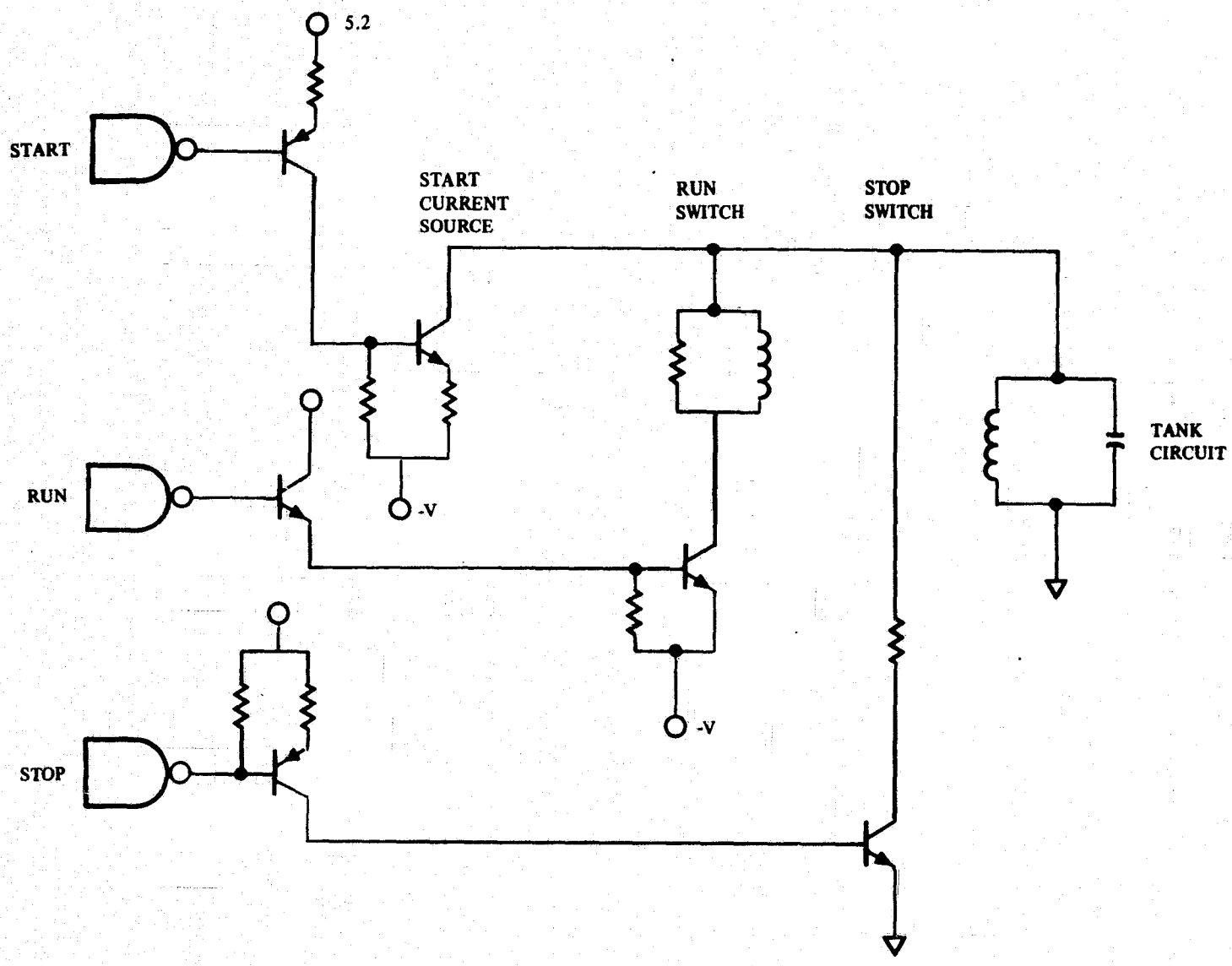


Figure 30. Drive Electronics (X Driver)

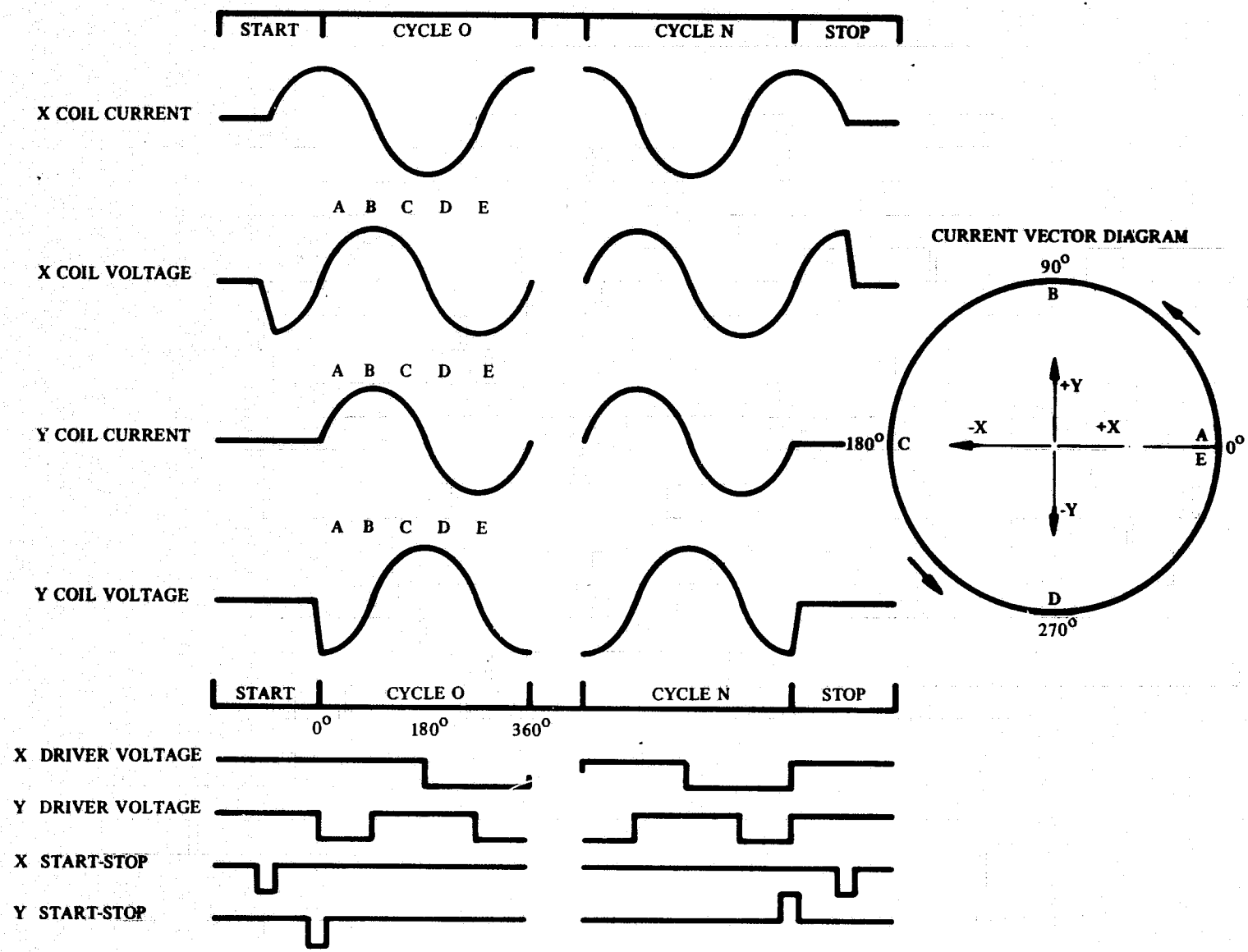


Figure 31. Timing Relationships between the Driver and the Coil

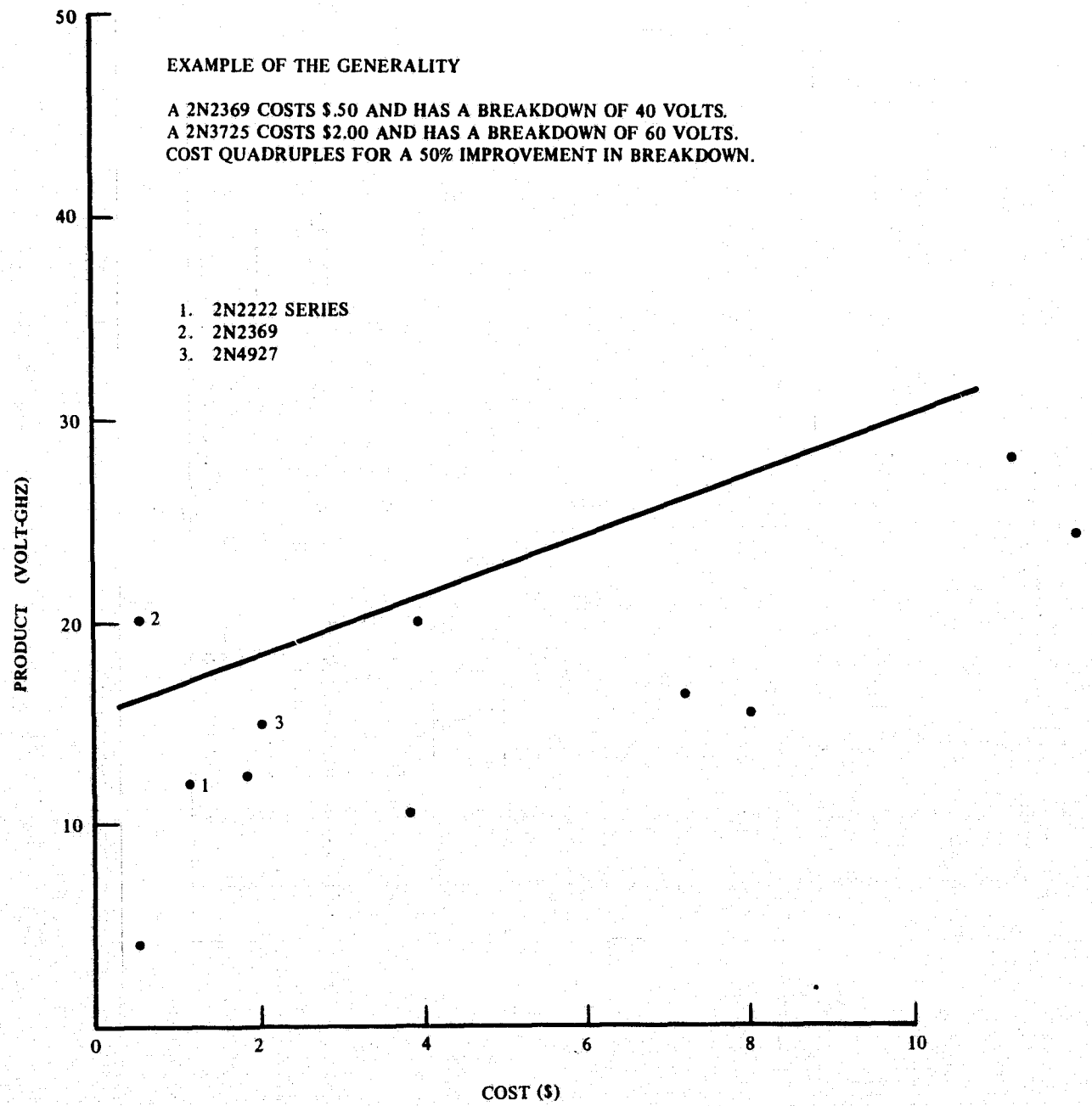


Figure 32. Transistor Rating and Cost

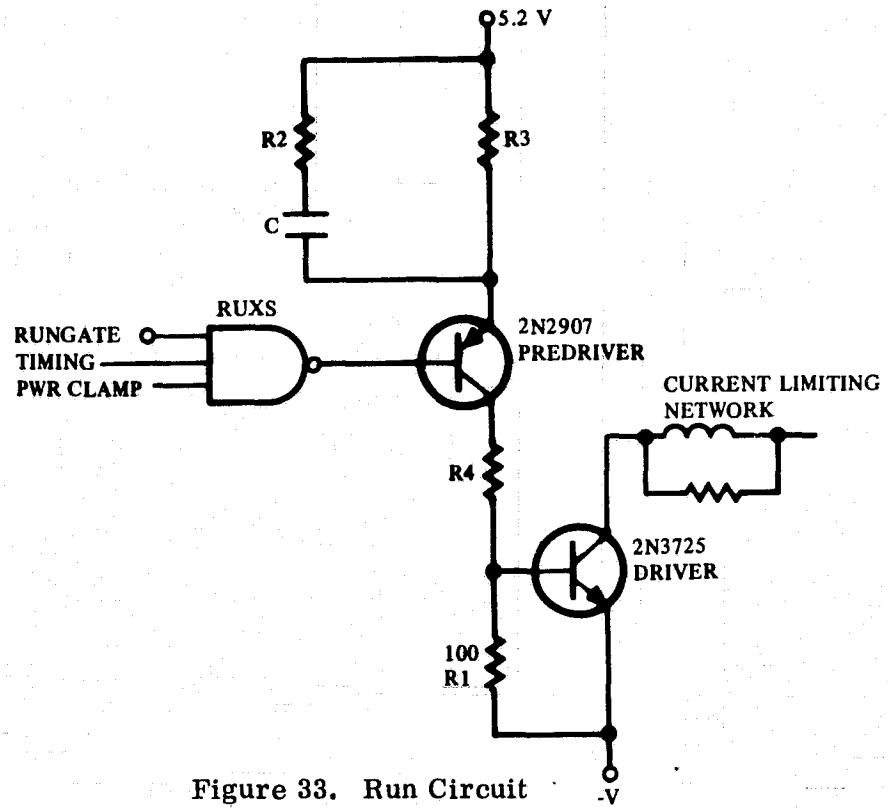


Figure 33. Run Circuit

To ensure saturation and fast turn-on of the driver transistor a collector current of 0.4 amp requires a base current of 50 mA. To maintain saturation with a collector current of 0.4 amp requires a lower base current (≈16 mA for a Beta of 25). A fast turn-off and a low B-E voltage during positive excursions of the collector voltage require a low base-to-emitter resistance. A minimum V_{BE} of 0.5 v will require 5 mA for a resistance of 100 ohms. A maximum current of 8.5 mA will flow in addition to the 16 mA required in the base. The PNP predriver current source is capable of 60 mA during the turn-on and 25 mA during the rest of the cycle.

The dissipation in the 2N3725 Driver is as follows:

using $\begin{cases} V_{CE} < 0.7 \text{ volts} \\ V_{BE} < 0.9 \text{ volts} \end{cases}$

$[(0.7)\ (0.2) + (0.9)\ (0.02)]\ 50\% \approx 40$ mw + Switching Transistors

$\approx (20v)\ (0.2)\ 5\% \approx 200$ mw

Total power = 250 mw.

The drive transistor can be combined with others in a DIL package, but in the feasibility model a discrete transistor was used to provide flexibility. Regardless of assumptions, except possibly breakdown, driver and predriver transistors can be a part of a quad package for a prototype. Breakdown voltage is specified with a lower value in a quad pack.

The current limiting network (see Figure 33) is a power reduction technique. During the capacitance recharge time of the tank circuit, current must be limited. One way to do it is to use an inductor/resistor in parallel so that the initial surge is through the resistor and so that current builds up slowly in the inductor. As the voltage across the inductor drops, less current will flow in total but more will proportionally flow through the inductor reducing power dissipation over all. Recovery of the inductance current will occur in the next 1/2 cycle according to the L/R of the parallel network ($\approx$1 μsec which is more than satisfactory). This inductor/resistor network was tested in the breadboard and found to be useful in reducing power dissipation so the provision was also provided in the feasibility model. Because of the secondary importance of the concept the inductance wasn't installed. In the interests of circuit economy and power dissipation it is advisable in the prototype breadboarding to first explore the idea that the driver need only be on for the peak minimum voltage of the coil.

Logic inputs for the driver circuits are the previously discussed gated waveform from the control section, timing signal from the sequence board, and power clamp.

Timing to the driver during run in relationship to the start time was found to have implications as far as the sense signal phasing during start-up is concerned. If the start circuits are idealized current impulses at 0 deg, the first cycles are identical to the following cycles. However, in the practical circuit, current actually flows in the inductor before the capacitor is fully charged resulting in a phase difference between the X current and the Y current which is different than in cycles which follows. The result is that the bubble signal may miss the strobe on the first bit unless the shift in current flow is compensated for by shifting the timing. Once this was done in the feasibility model full start/stop sensing became possible.

Stop circuit. – The most difficult part of the driver design for the feasibility model was the stop circuit because of these three factors.

1. The X coil and the Y coil voltages are at opposite polarity when they are shut down. Ramifications include a requirement for two different circuits and a difficulty in matrixing with other coils drivers.

2. Timing is more critical than for starting because in the case of stopping the timing must match with the resonnant frequency of the coil which has a variability (thermal etc.).

3. Because of the retention of magnetization in the permalloy, overshoot of the X current will cause a weakening of the poles in the permalloy pattern resulting in scrambled data.

During breadboard evaluation, a concept was tried where energy would be removed quickly from the capacitor when the coil current reached zero. When this approach was evaluated in the feasibility model it was discovered that precise timing referenced to the rotating field was required. The discrete timing of the sequencer (oscillator referenced) could not provide the resolution of one shot timing as used in the breadboard.

The principle of critical damping which was finally used in the feasibility model is that for an oscillator network there exists a value of damping resistance that will remove

energy within a fraction of a cycle. However, it is still not as fast as removing energy from the capacitor when the coil current equals zero. For the parallel network with a lossy coil (Figure 34) the impedance looking into the terminals is

$$Z_{in} = \frac{S\,LR_2 + R_1R_2}{S^2\,LCR_2 + S\,(L + R_1R_2C) + R_1 + R_2} \tag{1}$$

the 2 poles will be:

$$S_{pole} = \frac{L + R_1R_2C}{2L\,C\,R_2} \pm \sqrt{\frac{L + R_1R_2C}{2L\,C\,R_2} - \frac{R_1 + R_2}{LCR_2}} \tag{2}$$

and the value of R_2 for critical damping is:

$$R_2 = -\frac{LCR_1}{4\,LC - R_1C^2} + \sqrt{\left(\frac{LCR_1}{4\,LC - R_1C^2}\right)^2 + \frac{L^2}{4\,LC - R_1C^2}} \tag{3}$$

the zero of the impedance for small (by comparison) R_1 will be on the order of tens of μsec which means that the energy decay will depend on the attenuation factor $((L + R_1R_2C)/2\,LCR_2)$.

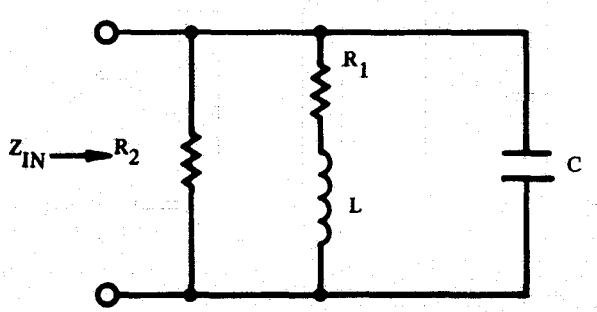


Figure 34. Lossy Coil and Critical Damping

For the values of R_1, L and C for the butterfly coil of 0.4 ohm, 14 μH, and 0.07 μf, R_2 will be 14 ohm and the damping time constant will be 2 μsec which is satisfactory for the 6.67 μsec cycle period.

The trouble with applying the critical damping principle in many circuits is that the control semiconductors are nonlinear as the potential across them approaches the junction potential. The change that was made to the driver stop circuit was the installation of back-to-back diodes driven by a current source as shown in Figure 35. Essentially the impedance of Point A to ground, looking into the clamp, is low and constant as the energy of the tank circuit is depleted because the two junction potentials cancel and because the difference between R_{D1} and R_{D2} is small. Results such as those given in Figure 36 show that any desired degree of damping may be achieved (overdamped or underdamped) by selection of an appropriate damping resistor. By contrast a transistor and diode clamp to ground only effectively a clamp to 1 v and thereafter is an undamped circuit. Notice that the polarity of the X and Y clamps must differ since the voltage is opposite at shutoff. Field effect devices have characteristics which would be ideal for this application except that the damping resistance of approximately 10Ω will be affected by channel resistance and its variation. Although this circuit performed well when adjusted, some difficulty was experienced during setup in keeping the overshoot below 10 percent of the peak current.

Driver matrixing. – During breadboard evaluation a driver matrixing scheme was tried which was installed in the feasibility model but later dropped because of the start/stop problem. The effort in designing and implementing a driver matrix is secondary to a chip function matrix and accordingly was put off for future development.

4.8 Power Distribution and Switching

The philosophy used to obtain a low power design for the feasibility model is given in the following paragraphs. Because of the requirement of zero standby power a circuit was designed so that power to the entire recorder including the sequencer electronics could be shut down. The chief advantage of a power switch internal to the recorder is that the recorder can be shut down without having to discharge the decoupling capacitors and having to recharge them on turn on, thereby reducing line surges. Key to the circuit's zero standby operation is a PNP transistor which is turned on when an input low is supplied and which is substantially latched by a flip-flop.

Low power TTL vs CMOS choice. - So much of the memory electronics in a large bubble recorder will have an association with the actual driving of coils, driving of annihilators and generators, or the sensing of a bubble that the decision as to which type of logic is best must be made on the basis of fan out to the bubble and coil functions. A proportionately large amount of power is dissipated in the coil which makes insignificant the potential power savings of MOS over low power TTL in the timing section. Considering also the fast power up capability of low power TTL and the fact that power switching will be used it is unclear how much savings in power for MOS or CMOS logic lines really produce. In addition low power TTL is qualified for space applications, e.g., (Viking program) and if properly derated can tolerate near planet radiation (total dose) whereas presently available CMOS cannot.

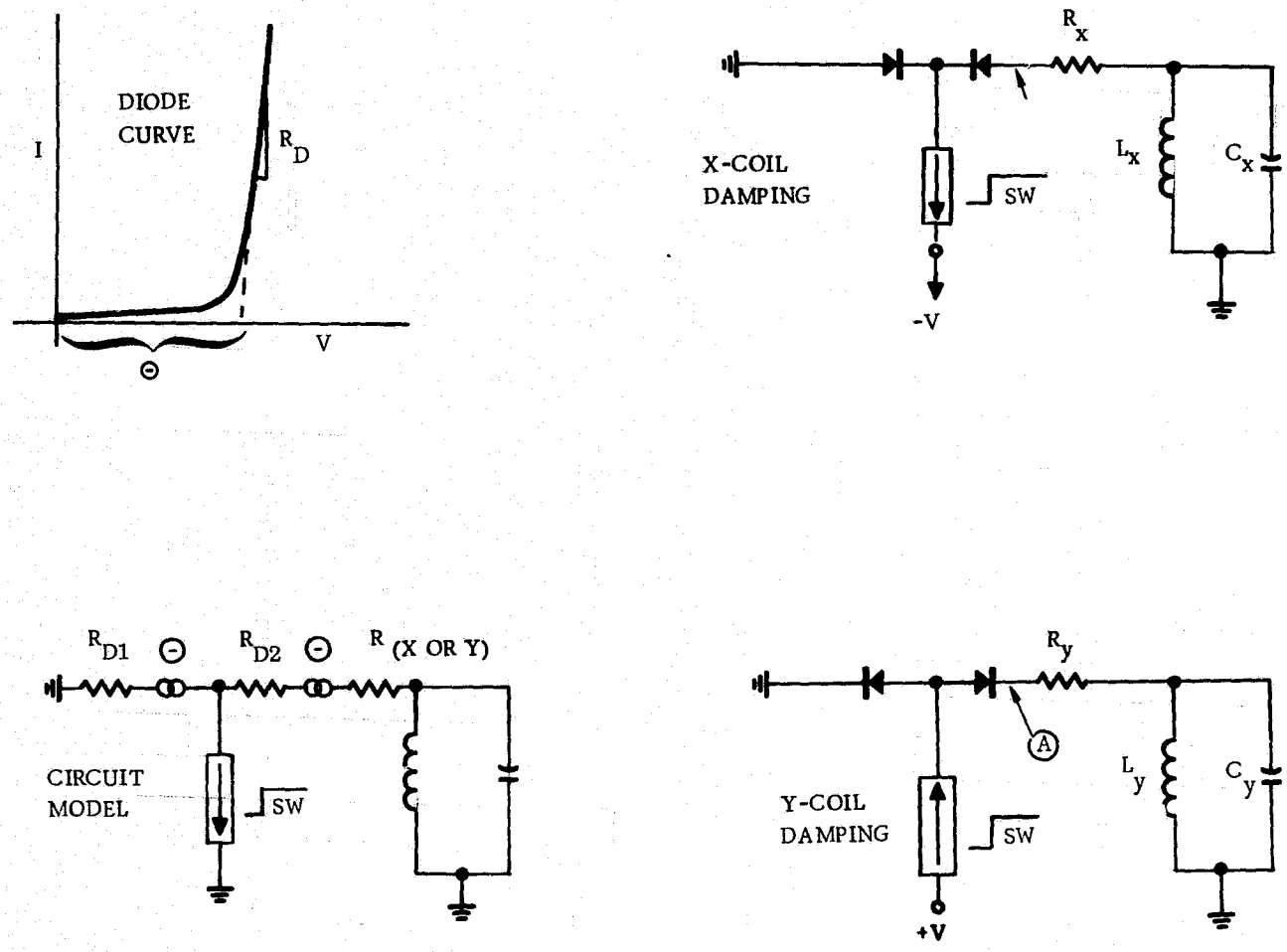
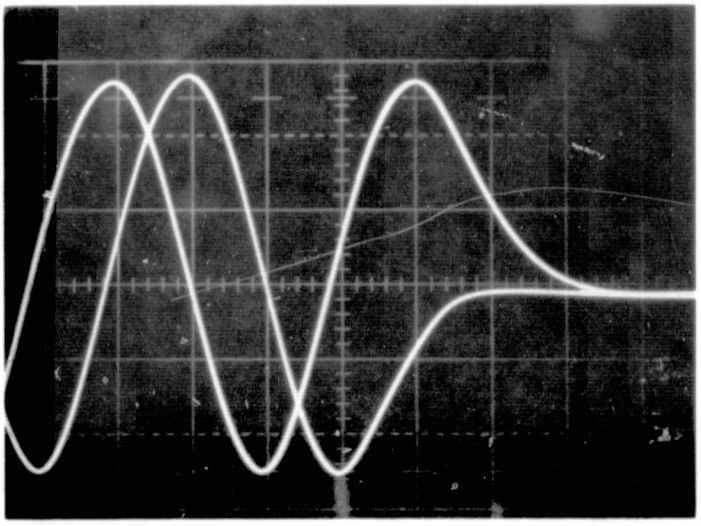
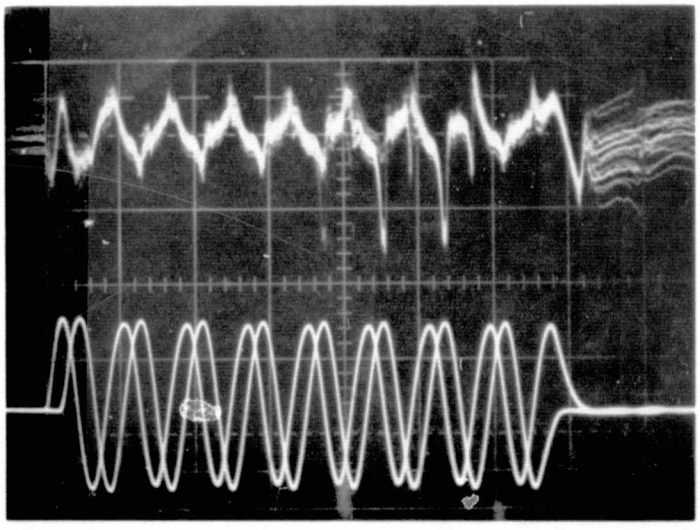


Figure 35. Damping Circuits for Driver



(a)

X CURRENT LEADING } 400 ma/DIV
Y CURRENT LAGGING } ≃1.6 μS/DIV



UPPER RIGHT SIGNAL OUTPUT FOR A BURST OF 8 ROTATIONS 20 mV/DIV } 8 μS/DIV

LOWER RIGHT COIL CURRENT FOR A BURST OF 8 ROTATIONS 1 AMP/DIV

Figure 36. Coil Associated Waveforms

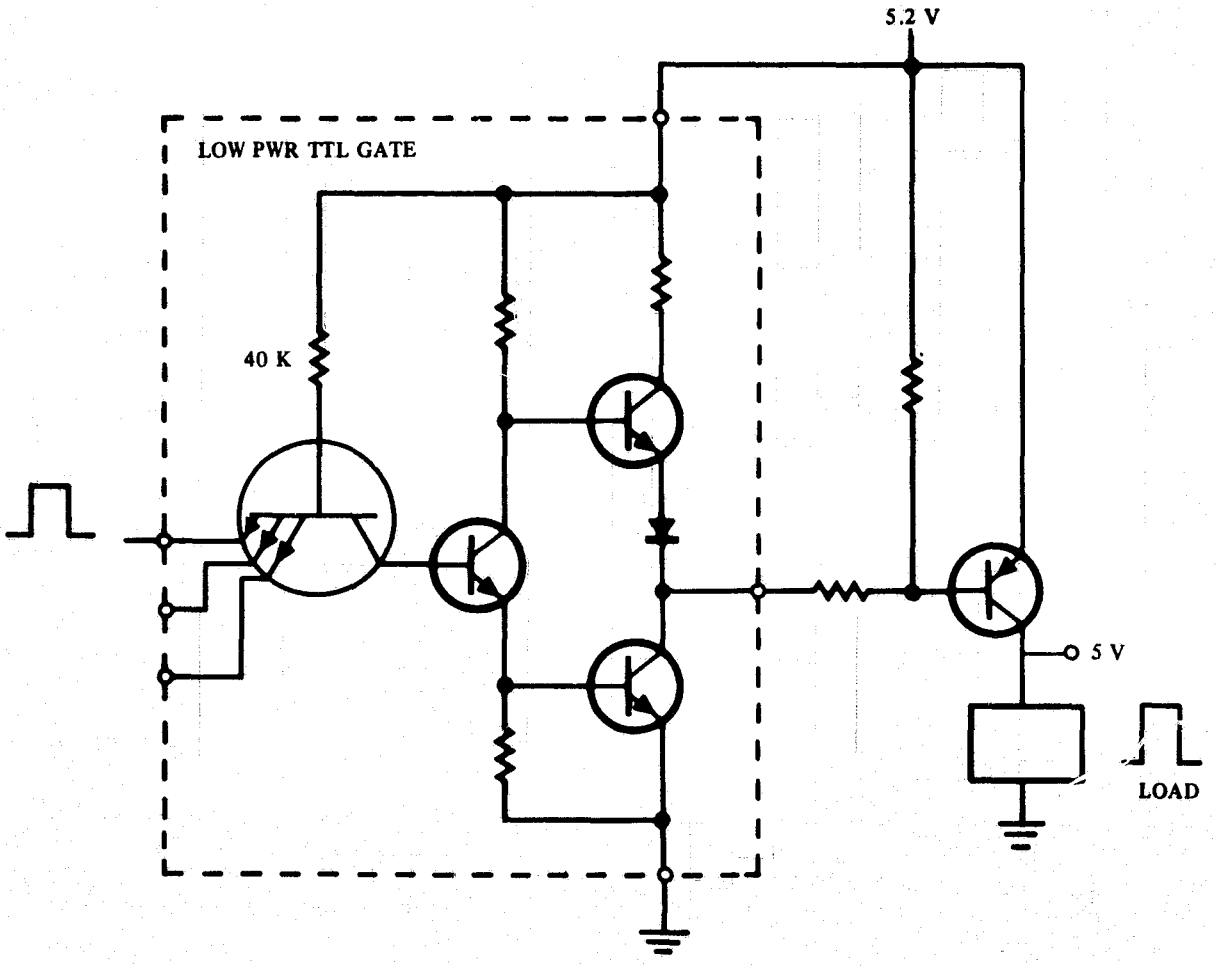


Figure 37. Low Power Switch

Zero standby circuits. - Switches and current sources used in the feasibility model dissipate no power unless the circuit is supplying current to the coil or bubble function. Power is not used to hold a circuit off which saves power and transistors are used in the linear mode (current source) wherever applicable which saves power by eliminating storage time. Figure 37 is an example of a voltage switch configured using a low power TTL gate as the base driver. When the circuit is off it dissipates only 1/2 of a milliwatt including the Gate. Most of the power is dissipated in the load when the circuit is on. In some situations a current which flows to a negative voltage is desired as in level shifting and in this configuration dissipation occurs in the transistor and in the emitter-to-supply control resistor. In the saturated case, the top transistor of the TTL output facilitates turnoff for certain values of base limiting resistance.

Power switching. – A few sections such as the sensing section or the annihilator/generator section need only be turned on for a few modes of operation. For example sensing is required only during the read modes and just as well be off at other times. Actually the sense amplifier in the feasibility model is turned on for only a quarter of a cycle which conserves more power. Figure 38 shows the power switches used in the feasibility model. During turn on of a switch a power on clamp (a guaranteed zero) is required on the input to ensure that under all conditions the output will not glitch and will not be able to sink the base current of the transistor as the supply voltage rises. These type of switches can be nested (as they are in the feasibility model) so long as all the emitters go to a common voltage. Another feature of the concept is that logic done within a section can sometimes be done as part of the power switch thereby improving logic utilization. Going from one section of logic to another can be a logic problem as it was in a few cases in the feasibility model unless the unpowered state is considered.

Decoupling. – By using power switches within the memory to disengage the active circuitry, zero standby power is achieved without having to disengage the decoupling capacitors. In this way the power supplies, regulators, and distribution busses can be considered as one complete subsystem which has distributed energy storage. When using the system each submodule can be quickly turned on and used without having to charge capacitors and wait until ringing stops.

Within the recorder a grid of decoupling capacitors exists such that energy is available very close to the power switches or to the drivers which constitute the pulse sources and to the circuit returns which must sustain the current without injecting Ldi/dt voltage into another circuit. For fast rise time pulses a number of low ESR ceramics are used to improve the energy replenishment until the higher ESR tantalums can deliver sufficient current. For high reliability programs a resistor in series with the tandalums is desirable which makes the ceramics more important for longer recoveries leading to a still greater use of ceramics.

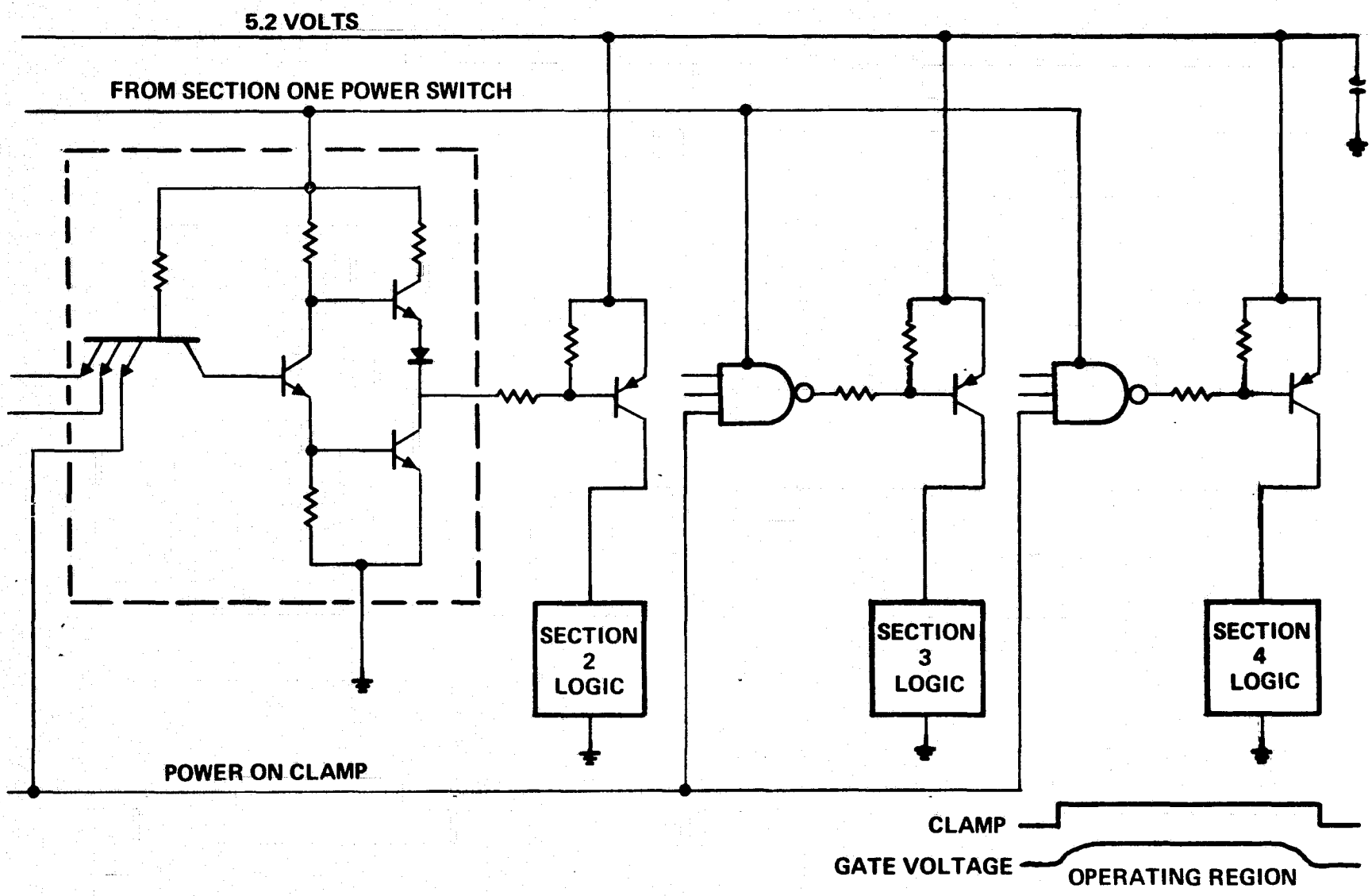


Figure 38. Power Distribution

4.9 Data Protection and Nonvolatility

When the recorder is powered down, orientation of initial data reference must be maintained in nonvolatile storage to ensure sequential readout of previously stored data. In the feasibility model the technique which was used was the record precursor which is a bubble leading the record in an otherwise erased track, a two core and flip-flop circuit and a CMOS address counter. Using the precursor, the procedure is to first erase the track completely and then allow data to enter aperiodically and asynchronously until the chip is filled. The precursor bubble which leads the record is the first to be detected causing commutation to the next chip and so on until the track is full. To maintain knowledge of which of the two chips is full, a ferrite core was used which loads a flip-flop on turn-on and which is written by the flip-flop on turn-off. If during readout the power is interrupted, the CMOS counter will hold the chip bit count on residual power for 15 minutes. To gain an appreciation of this concept look at Figure 39 which shows the device orientation on the chip and the assembly of a record on the chips using the feasibility model chip. Notice that as the chips are filled going from Chip 1 to Chip 4, a gap is introduced on each chip as a result of the generator to detector spacing. Backing up to read the record head is no problem since the selection can depend on sensing the mark bubble until the desired chip is reached. To count down toward the first chip filled requires a jog of 16 bits per chip but to count up toward the last chip filled requires rotation of each chip for its full count. This organization clearly has some drawbacks to consider when chip oriented selection is mixed with the FIFO selection. The Feasibility model is limited in flexibility in this regard.

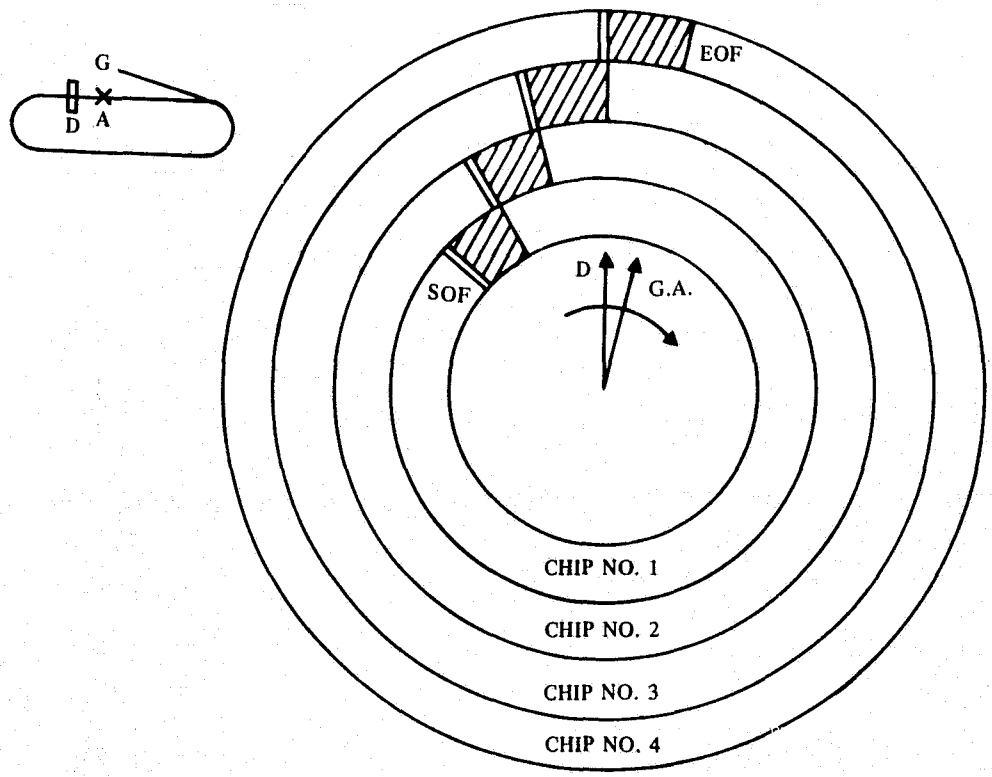


Figure 39. Four Chip Track with Slewed Record

Figure 40 shows a better method of assembly using a chip design where the generator and the detector would be aligned. Notice that filling does not produce a gap so that chip selection can be completely random. Whenever the bit counter is at its initialized position, the selection to any other chip can be made. This is suggested for a prototype design.

Although the fewest electronics parts are required for the precursor technique the approach is not flexible enough to allow the type of applications envisioned for bubble recorders such as block accessing. For a prototype design the potential for each of these three techniques (precursor, core store, and CMOS counter) was explored relative to the larger size memory. Factors like precursor bubble reliability and power dissipation have led to the consideration for the prototype design of the use of a core storage technique for complete counter status maintenance.

Basic to the core storage technique is a four element square loop core wound as a single core with enough turns to achieve an output voltage sufficient to preload a counter directly (Figure 41). On track turn on the core string for the chosen track would be interrogated which presets the serial register. As the track is loaded the address count of the track register is incremented by adding and shifting. On turn-off the cores are written sequentially as the address is fed into the driver; thereby storing the record status permanently in non-volatile storage. This serially incremented counter technique was chosen over LSI counters because available counters either dissipate excessive power (like 600 mw) or require too many components (for MOS-TTL transistor interface).

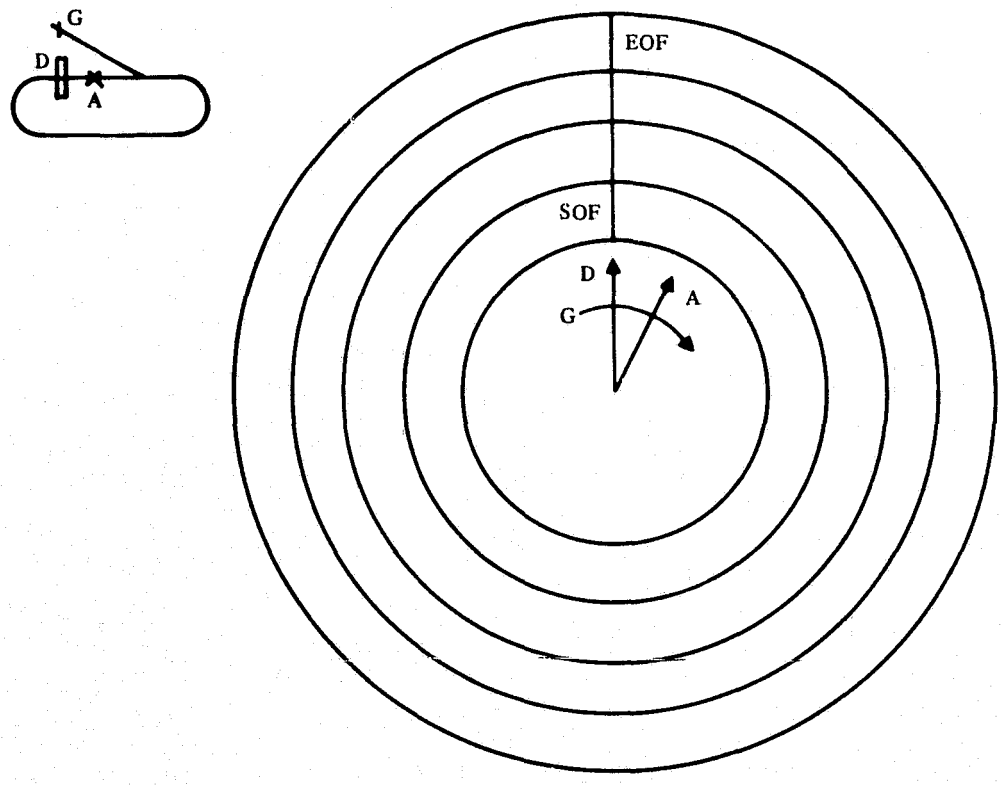


Figure 40. Four Chip Track with Synchronized Record

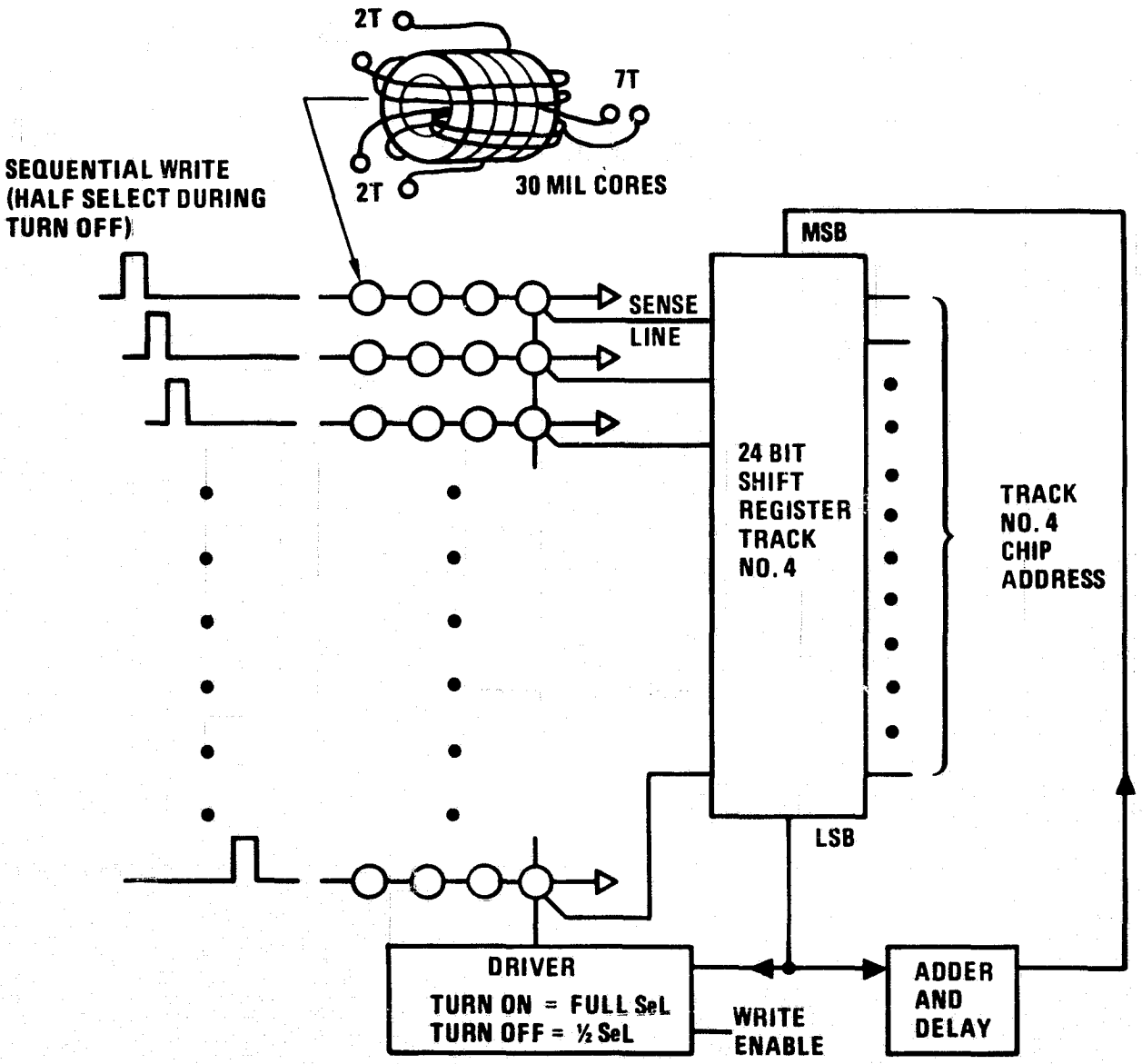


Figure 41. Address Counter Storage

Figures 42 and 43 show the circuitry required for the purpose of count detection and chip addressing. Count detection would be simple being a comparison of two serial patterns rather than a parallel comparison. The serial word to which the current address is to be compared is generated once by the sequencer for use by all tracks. The chip addressing either uses the counter word or by the addressable word as required by the type of command and this requires selection latches as shown. The advantage of this approach is that a sequential fill of the track can be interrupted for a random chip read or chip write (provided the chips are in their initialized position) after which the sequential filling can resume at the last chip filled.

In summary, changing the chip element alignment slightly can simplify the bookkeeping and allow random access of chips. The proposed circuit using cores and low power shift registers illustrates the potential for simple low cost and reliable power disruption protection. Furthermore the cores and core circuitry are adjunct to the storage and control circuitry so that if a particular user does not require address nonvolatility it can be left off the board. This is not true of the precursor concept. Therefore, this approach is recommended for use in a prototype design.

4.10 Packaging Pertaining to Electrical Design

The philosophy of developing a recorder to fit a wide range of applications from low cost to high rel should be considered in the mechanical design of the electronics boards. Although multilayer PCB construction (5-20 layers) using flat packs is unquestionably more dense than any technique using double sided board and DIL packages, it is not amendable to a low cost program. Low cost techniques such as wave soldering or pin for pin substitution of low cost parts are not possible. On the other hand if 2 layer board with DIL's is used, the best high rel grade or the commercial grade of parts may be inserted in the board depending on the end users need. Besides double sided board is inherently more reliable and requires less quality control effort than multilayer board.

One approach to improving the density of the double sided board construction but without impacting cost or reliability significantly (shown in Figure 44) is by interdigitating 2 boards so that the space between dual in lines (necessary for conductor placement) is filled by another board's dual in lines.

The only thermal consideration which must be made is for the coil drivers where the problem is dispersing heat to reduce a potentially high junction temperature. This will be handled in the few cases where it may occur by using a heat strip under the dual in line to conduct the heat to the card mounting rail and by paralleling drivers where necessary.

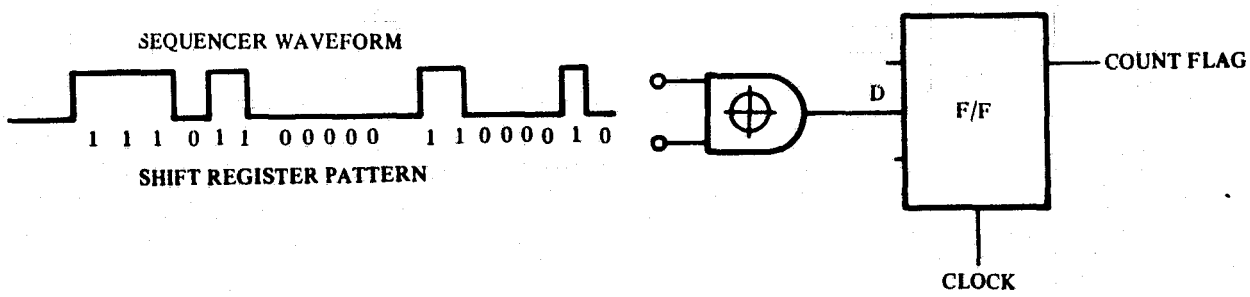


Figure 42. Count Detection Circuit

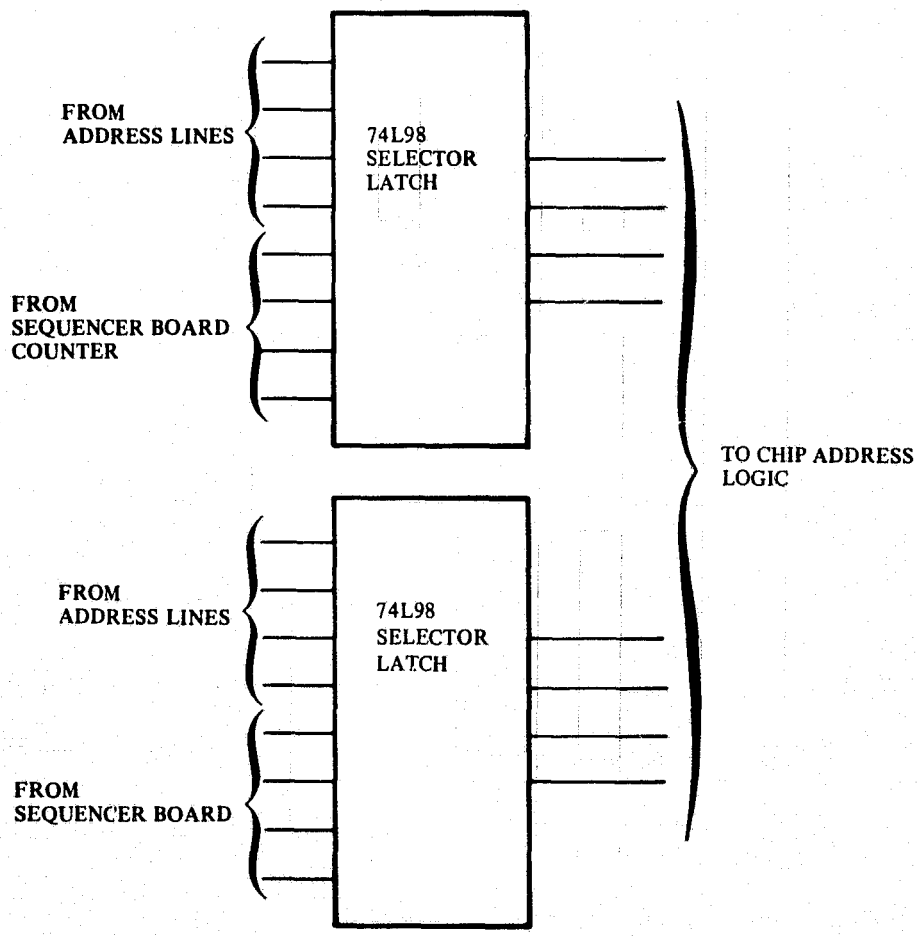


Figure 43. Chip Address Logic

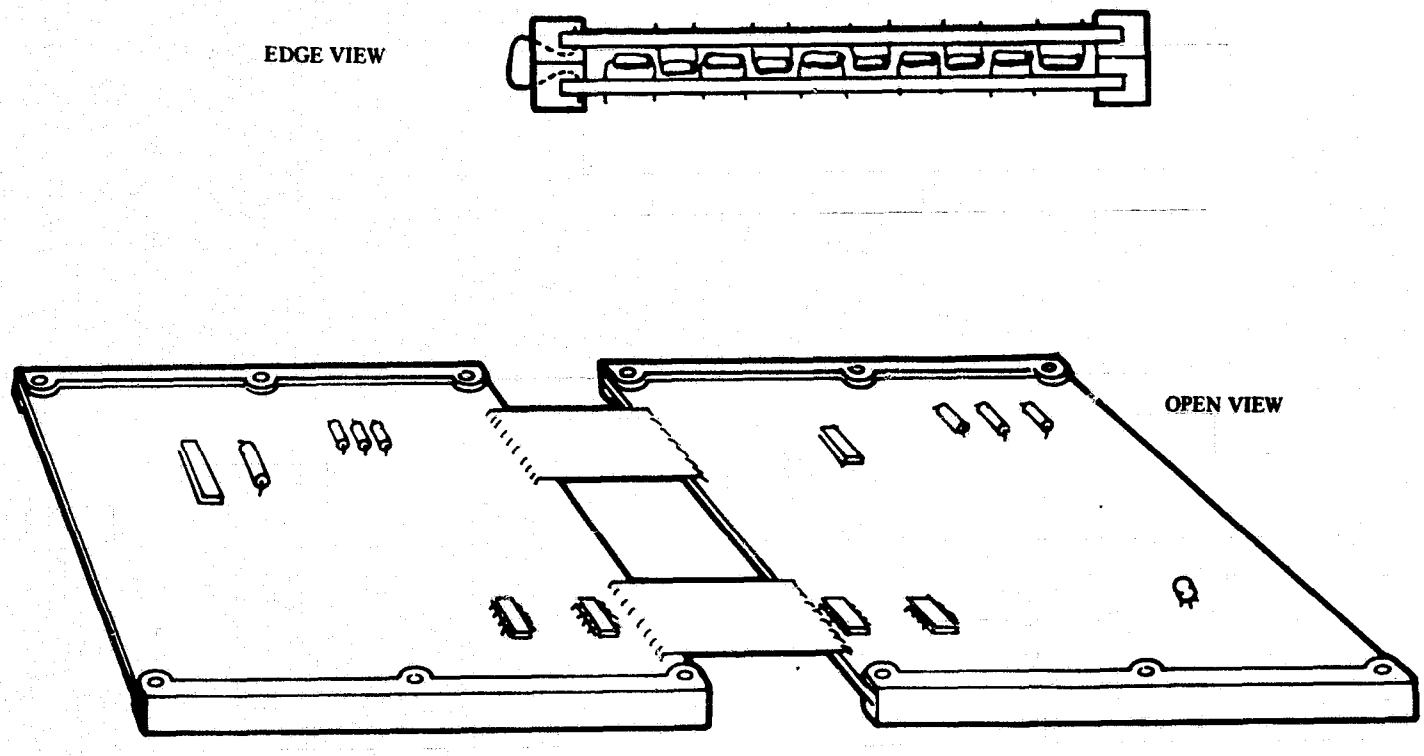


Figure 44. Interdigitating PCB

5. ROTATING FIELD NETWORK

In the field access type bubble memory system, a rotating field is essential for the device operation. The mechanism of this field generation will impact the design device package, magnetic module, and electronic system organization. The design goals of this field generation network are as follows: (1) it can generate a magnetic field with maximum uniformity in the device area, (2) this field can be uniformly rotated at a maximum frequency (desired data rate of the memory device), (3) it can be driven by a simple electronic circuit and will not disturb the device thermal environment, and (4) it is small in size, light weight, easy to construct, and compatible with the device packaging.

Two basically different concepts have been studied and reviewed in this program: the close coil structure and the open coil structure. Figure 45 shows the basic concept of the close coil structure. The rotating field is generated by two orthogonal air core solenoid windings. Memory devices are placed inside the windings and accessed from the corners or the edges of the windings. This structure is simple, light and compact. However, the devices are difficult to access and the heat generated from the coil will heat up the devices. In the open coil structure, as illustrated in Figure 46, the devices are placed outside of the coil winding so that they are easily accessible and can be packaged separately with the coils. In addition, since the devices are not enclosed in a winding there is less of a heating problem than with the close coil structure for the same coil power. However, under present design, this open coil structure is larger, heavier and requires more power than the close coil approach. Extensive development work has to be done before open coils will supersede the basic close coil structure.

5.1 Close Coil Structure

It is well understood that a uniform magnetic field can be generated between two infinite size parallel conductor planes carrying opposite electrical current. In order to approach this ideal situation inside a solenoid winding, it is obvious that the solenoid has to be formed by two large size conductor planes placed as close together as possible. This arrangement is called a flat-coil, as illustrated in Figure 47. To achieve a uniform field, the windings have to be straight and parallel. The simplest approach in this type of coil winding is to place conductor wires sequentially on the surface of the coil form, forming a layer of wires with uniform height. The conductors for the next layer can be placed directly on top of the first layer and parallel to the conductors in the first layer. To vary the number of turns in this coil, these layers can be connected in series or in parallel by properly connecting the terminals of the winding.

5.1.1 Simple analysis. – Using the dimensions and the symbols shown in Figure 47, and assuming the conductors are circular and closely spaced the coil parameters can be given by the following equations:

$$H_o = KJ = KN_\ell N_t I/c \tag{4}$$

$$R_{d-c} = \rho N_\ell N_t (2a + 2b)/s \tag{5}$$

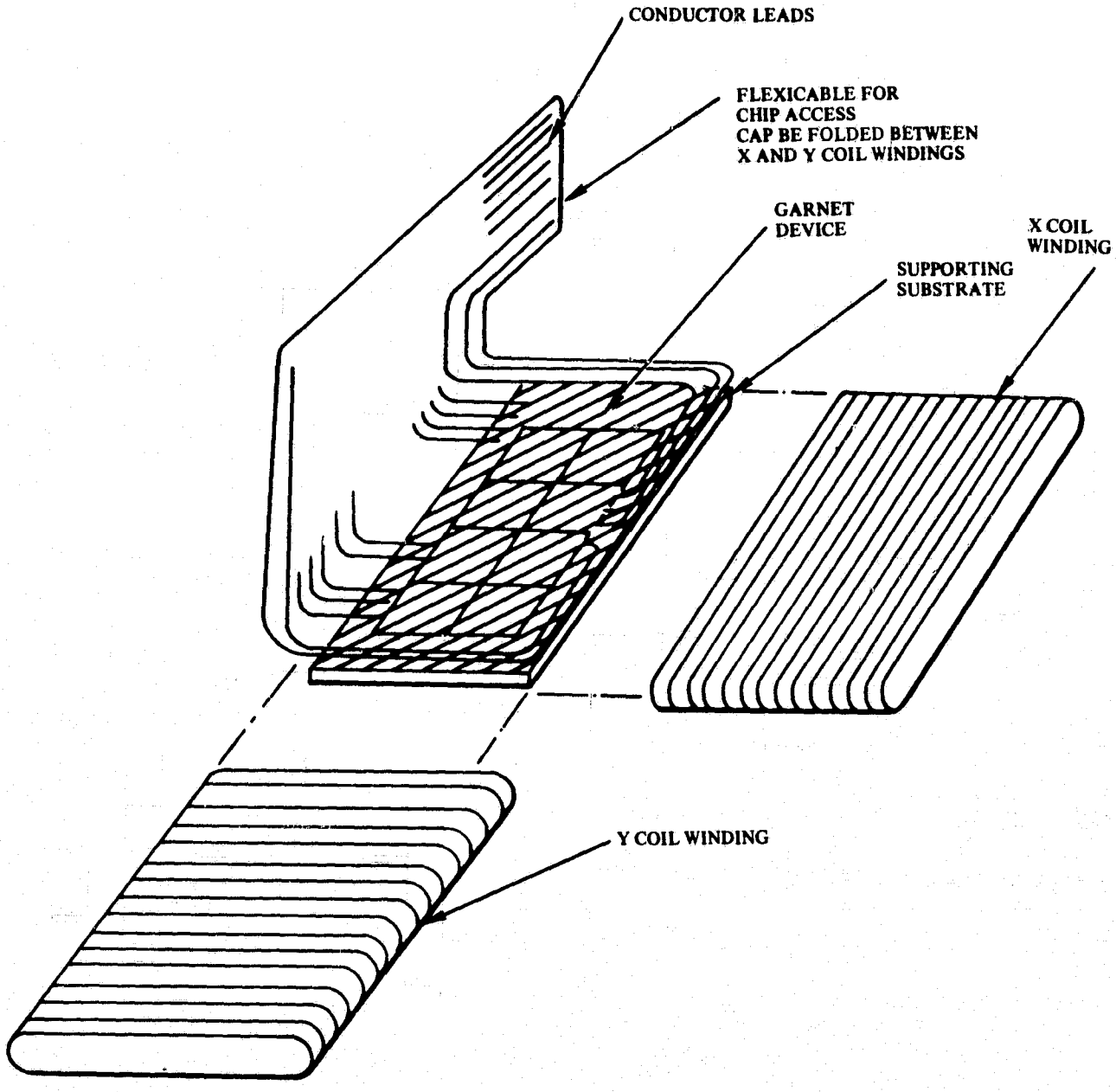


Figure 45. Closed Coil Structure for Bubble Memory Packaging

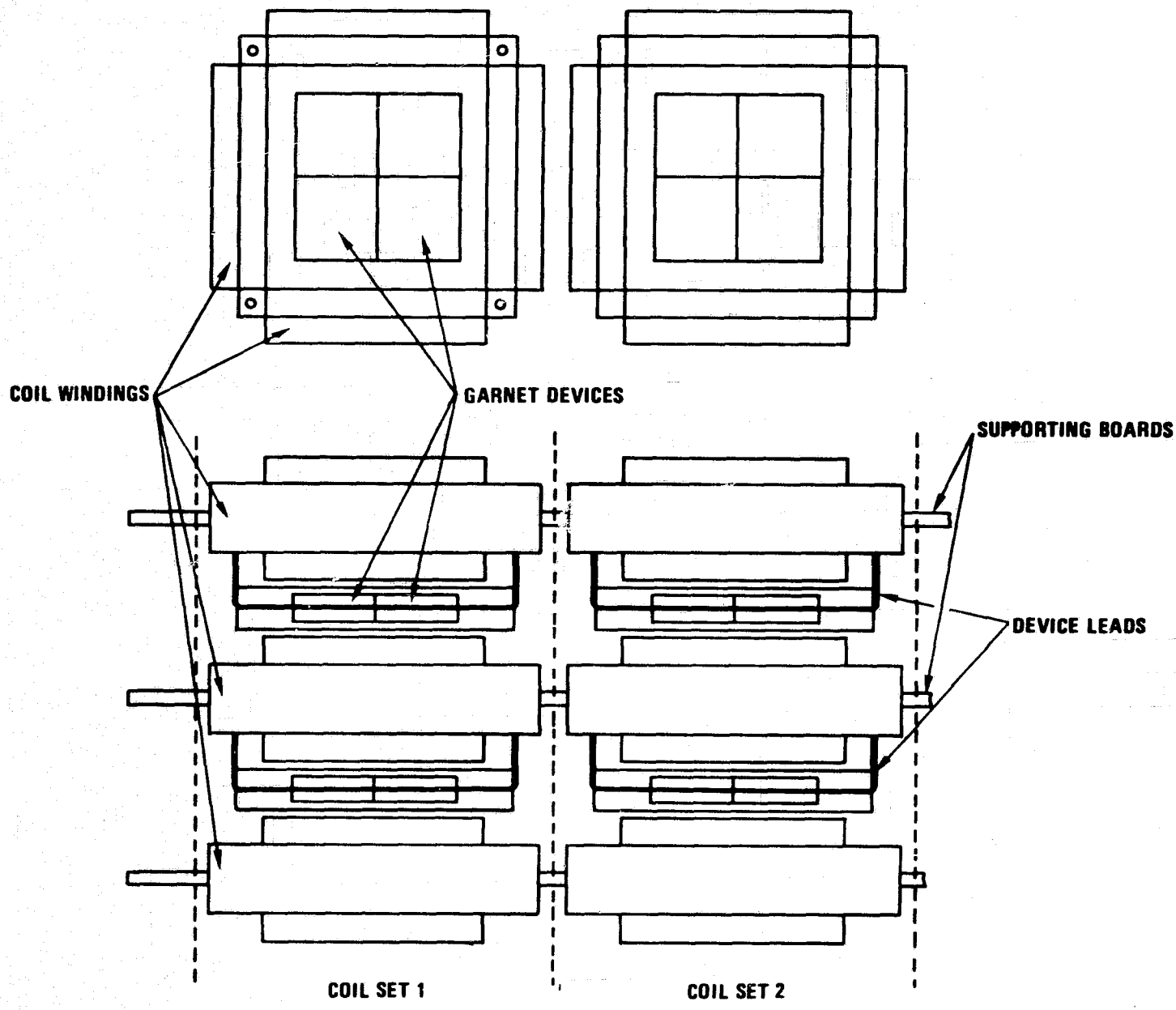


Figure 46. Open Coil Structure

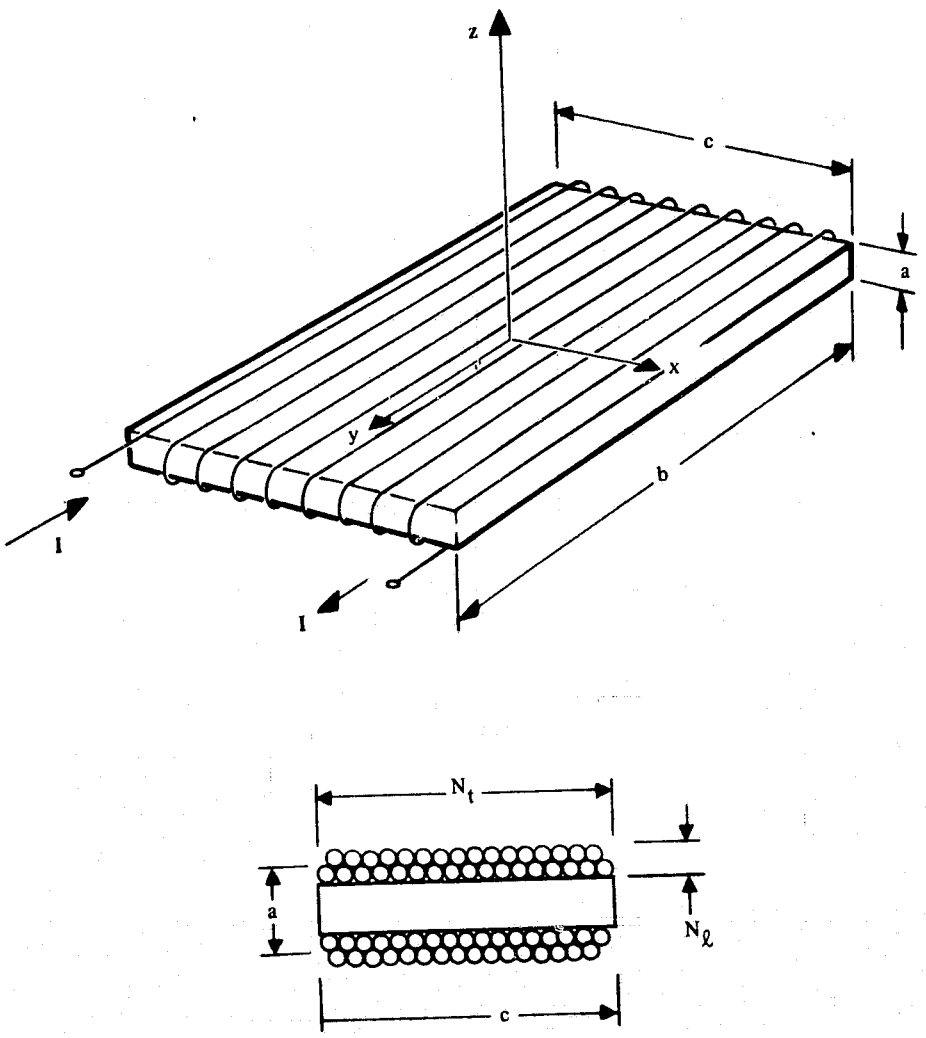


Figure 47. Flat Coil Structure

$$P_{d-c} = 1/2\, I^2 R = \frac{H_o^2}{K^2} \rho \frac{(a+b)c^2}{N_\ell N_t s}$$

$$\approx \frac{H_o^2}{K^2} \frac{4}{\pi} \frac{\rho(a+b)c}{N_\ell d} \qquad (6)$$

$$L = N\phi/I \sim \mu_o H_o bc / I N_t N_\ell \qquad (7a)$$

$$= \mu_o K \frac{ab}{c} N_\ell^2 N_t^2 \qquad (7b)$$

$$V_c = 2\pi f LI \sim 2\pi f \mu_o ab N_\ell N_t H_o \qquad (8)$$

where H_o is the magnetic field at the coil center. K is a shape factor which depends on the coil geometry. J is the current density along the coil axis. R_{d-c} and P_{d-c} are the d-c resistance and d-c power dissipation in the coil winding respectively, ρ, s and d are the resistivity, crossectional area and diameter of the conductor wire respectively. a, b, c and N_ℓ, N_t are the coil dimensions and number of layers and turns in the layer as shown in Figure 47. L and V_c are the coil inductance and voltage across the coil when operated at frequency f. I is the current in the winding.

It can be seen from (Eq 4) that the coil sensitivity (field strength per unit current) is directly proportional to the number of turns in the coil. When the coil is approaching to two infinitely long current strips (i.e. $b/a \to \infty$ in Figure 47) the value of the shape factor K is given by

$$K = \frac{2}{\pi} \tan^{-1} c/a \qquad (9)$$

(Eq 6) shows that the power dissipation is proportional to the area of the coil (if $a \ll b$) but inversely proportional to the wire size and the total number of turns in the coil. In the later case which means the more the conductors in the coil winding, the less the power dissipation.

Equations (4) and(8) indicate the current and voltage requirements on the coil are directly related to the number of turns in the winding.

5.1.2 Field uniformity. — The magnetic field generated from the electrical current can be simply calculated from the Biot-Savart law. Unfortunately, since the integration over a two dimensional plane does not give an explicit solution, a computer program is used to calculate the field numerically. The basic assumptions on the calculation are the following: (1) the coil is in a flat rectangular shape consisting of a finite number of windings with each winding composed of four straight sections of conductors and (2) the conductor current is a line current located at the center of the conductor. Thus, the magnetic field at any point inside the coil can be calculated by summing the field contribution from each conductor segments of the winding. The calculation results are summarized in a series of graphs. The dimensions are scaled to the length of the coil and the field strengths are scaled to the maximum field at the coil center.

Uniformity in the coil plane. — The inplane field (H_x) variation along the coil axis for coils with different thicknesses is shown in Figure 48. The field peaks at the coil center and drops monotonically toward the coil edge. To achieve a larger uniform area, it is desirable to use a thinner coil because it approaches the parallel planes arrangement. The field variation, perpendicular to the coil axis (H_x v.s. y), is relatively uniform. As shown in Figure 49, the field increases when close to the edge. This effect is due to the contribution from the side windings. This variation can be minimized by reducing the length of the side winding, that is, limiting the coil height. Moving along the axis perpendicular to the coil plane, the field variation is quite uniform, except when it is very close to the windings. In the arrangement shown in Figure 45, the coil width has to be greater than the coil length, and, the devices are located under the area covered by both coil windings. If the coil height is not too big (e.g., $a/c < 0.4$), the uniform area in this structure then is primarily limited by the field distribution along the coil axis. This area can be represented by the effective length of the coil (c^*) over which the field variation is within a preselected value. Figure 50 shows the effective length of a coil as a function of the coil height. The flatter the coil, the longer the effective length, and the larger the uniform area.

Uniformity perpendicular to the coil plane. — From the packaging point of view, it is desirable to use a large coil height so that several device planes can be stacked in one coil structure. In this arrangement devices can no longer be placed at the symmetry plane of the coil, giving rise to vertical field components which can modulate the bias field applied to the device.

Figure 51 shows the vertical component along the coil axis in a plane 0.02 unit distance ($c = 1$) above the centerplane. The thin coil has less vertical component inside the coil but it increases very rapidly when moving close to the coil opening. The variation perpendicular to the coil axis (H_z v.s. y) is relatively smooth and drops off when close to the coil edge. This is because the side windings do not contribute to the vertical field component.

Figure 52 shows H_z v.s. z along two vertical lines at $x = 0$, $y = 0$, and $x = 0.3$, $y = 0.55$. The vertical component increases almost linearly with the vertical distance z and it's slope increases with the coil height. The effect of this variation can be represented by an effective height a^* which is defined as the maximum thickness over which the vertical field component is less than a preselected value. Figure 53 shows a set of plots of a^*/a as a function of a/c for the area with $|x|/c < 0.3$. In this plot, the effective height actually decreases with the increase of coil thickness at small a/c values. If the area of concern is extended to $|x|/c < 0.4$, this phenonenon is no longer true, because, in this case, the vertical component increases very rapidly near the coil edge.

Angular distortion. — The two side windings of the flat coil also contribute to the magnetic field. These windings introduce horizontal components (H_y) in the area away from the symmetry plane ($y = 0$ plane). The effect of this component causes a skew in the field distribution and introduces a velocity fluctuation in the rotating field. The angular deviation along y direction is plotted in Figure 54 for several coil thicknesses. As expected, the thin coil has less angular distortion than the thick coil.

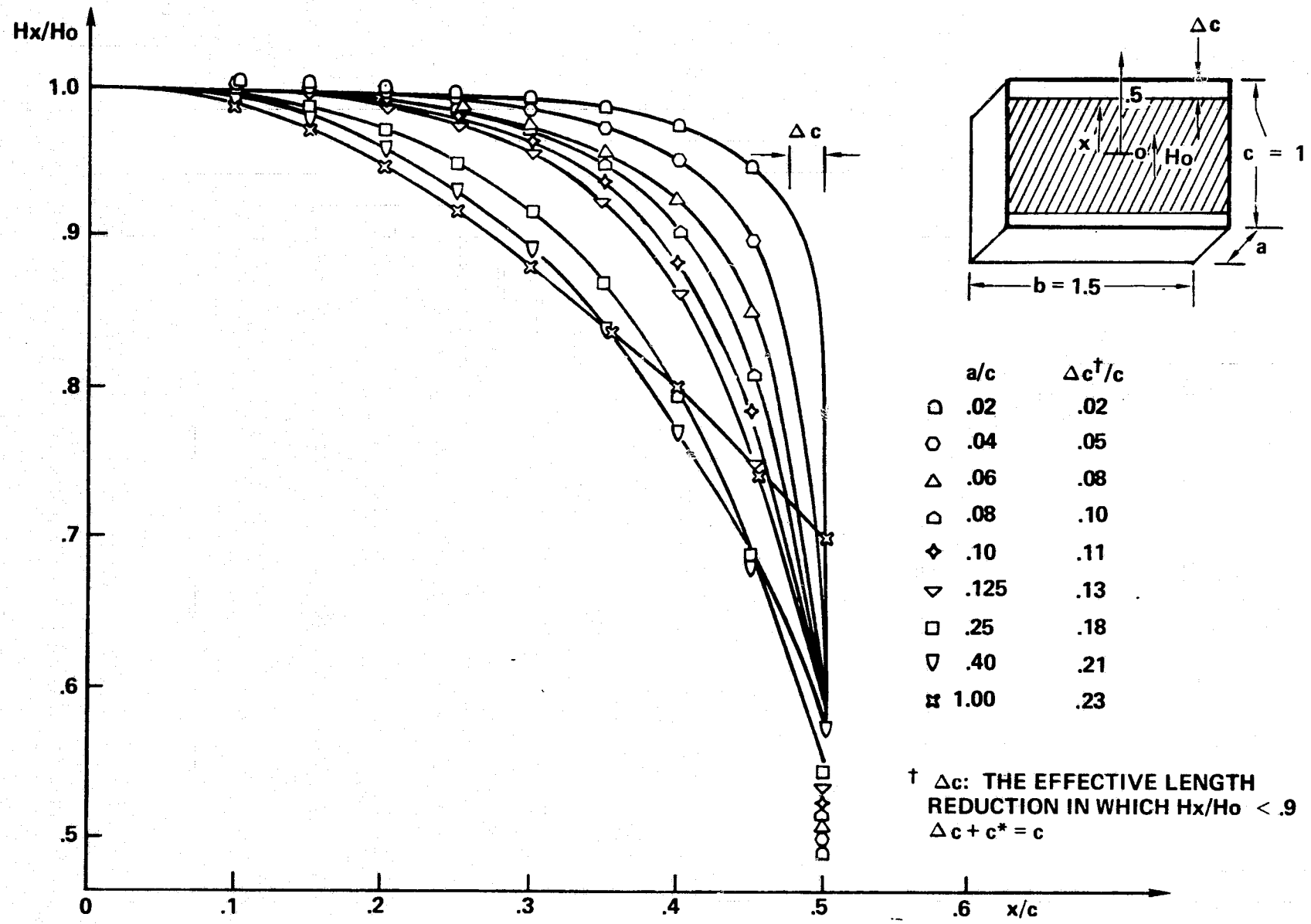


Figure 48. The Effect of Coil Height on the Axial Field Variation in a Flat Coil

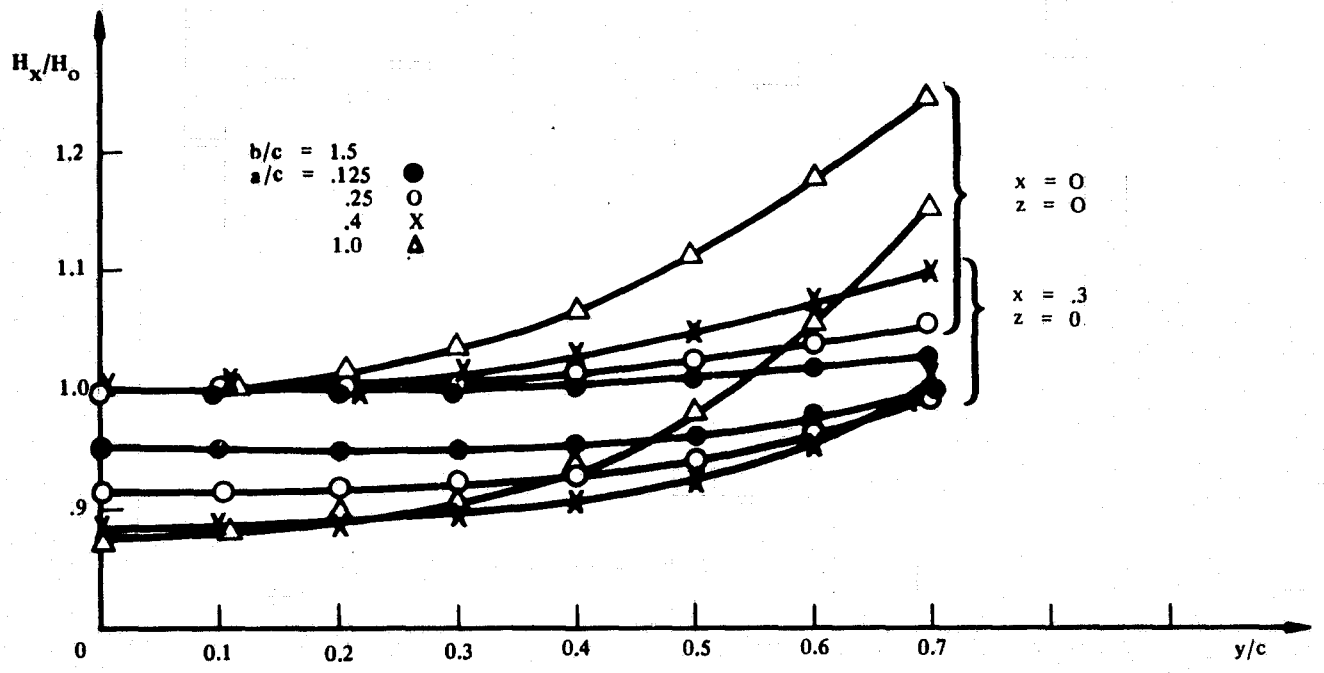


Figure 49. H_x vs y in a Flat Coil

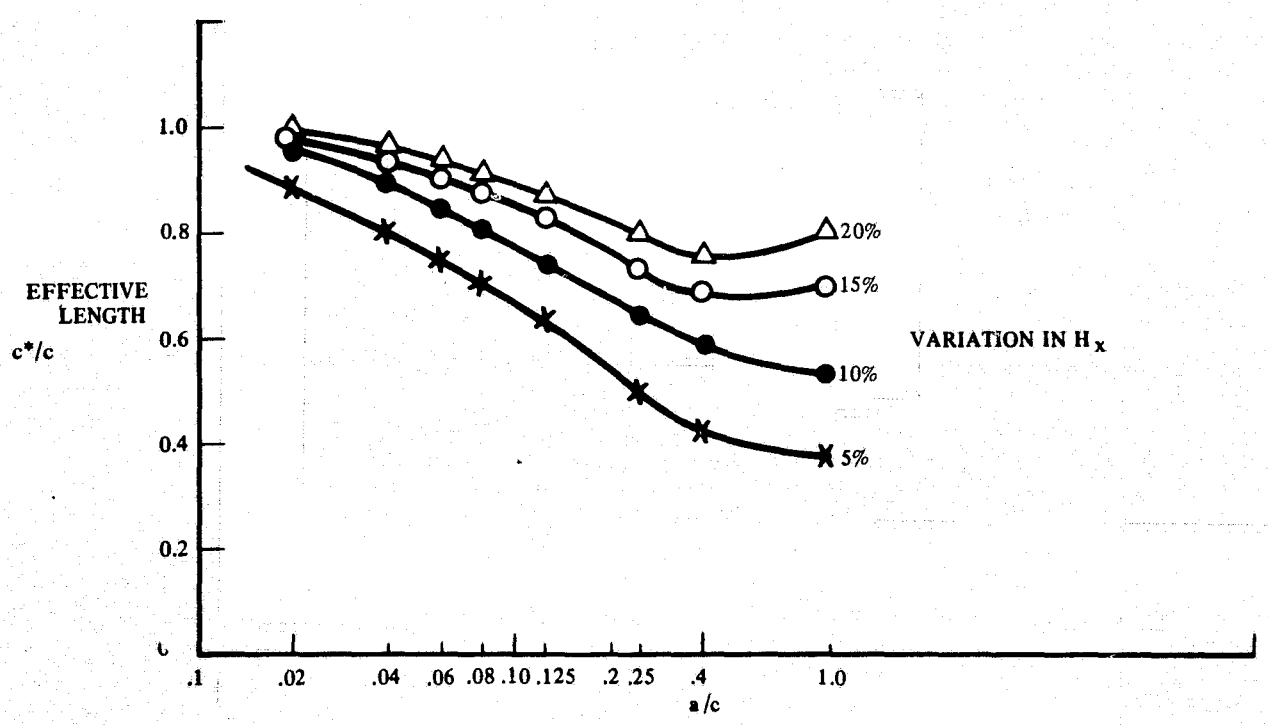


Figure 50. Effective Coil Length as a Function of Coil Height

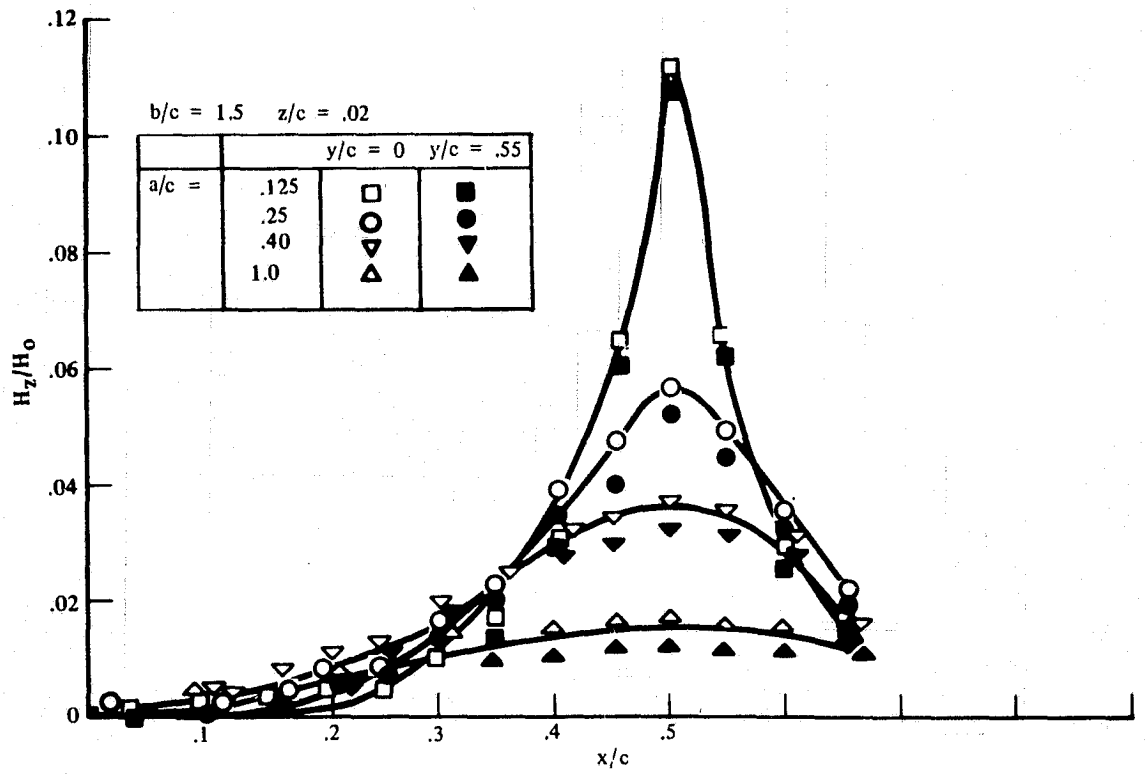


Figure 51. Hz vs x in a Plane 0.02 Unit above the Symmetry Plane

Effect of wire spacing. — In a large coil structure where power dissipation is high, it is desirable to have the wire loosely wound so that air circulation in spacing can reduce the heating effect in the system. However, if the wires are widely separated, additional fluctuations in the field distribution will occur. Calculations show that the effect is greater on the vertical component than in the in-plane component. For distances greater than a wire spacing away from the winding the field fluctuations due to the wire spacing smooth out and can be ignored.

Coil sensitivity. — The coil sensitivity is also a function of the coil geometry. This can be represented by the factor K in Eq 5. In a very flat coil ($b >> a$) this value approaches the value for an infinite current sheet and increases when the winding approaches a circular solenoid, as shown in Figure 55. This increase is due to additional contribution by the side windings in the coil.

Field uniformity improvement. — As shown in Figure 48 the effective area in the flat coil structure is primarily limited by the field of both ends of the coil. This is due to the reduction of averaged current density over a large distance at coil ends. The simplest approach to improve the field distribution is by adding turns at both ends to compensate the current decrease. An example is shown in Figure 56 where 10 percent increase in the winding at ends can improve the 90 percent uniform field area by 20 percent. In a solid coil winding adding turns at coil ends makes the coil thickness nonuniform which increases the total volume of the coil assembly. If the windings are loosely spaced, these additional turns can be added in between windings by using thinner wire. This arrangement will not change the coil dimension but will make the winding more complicated.

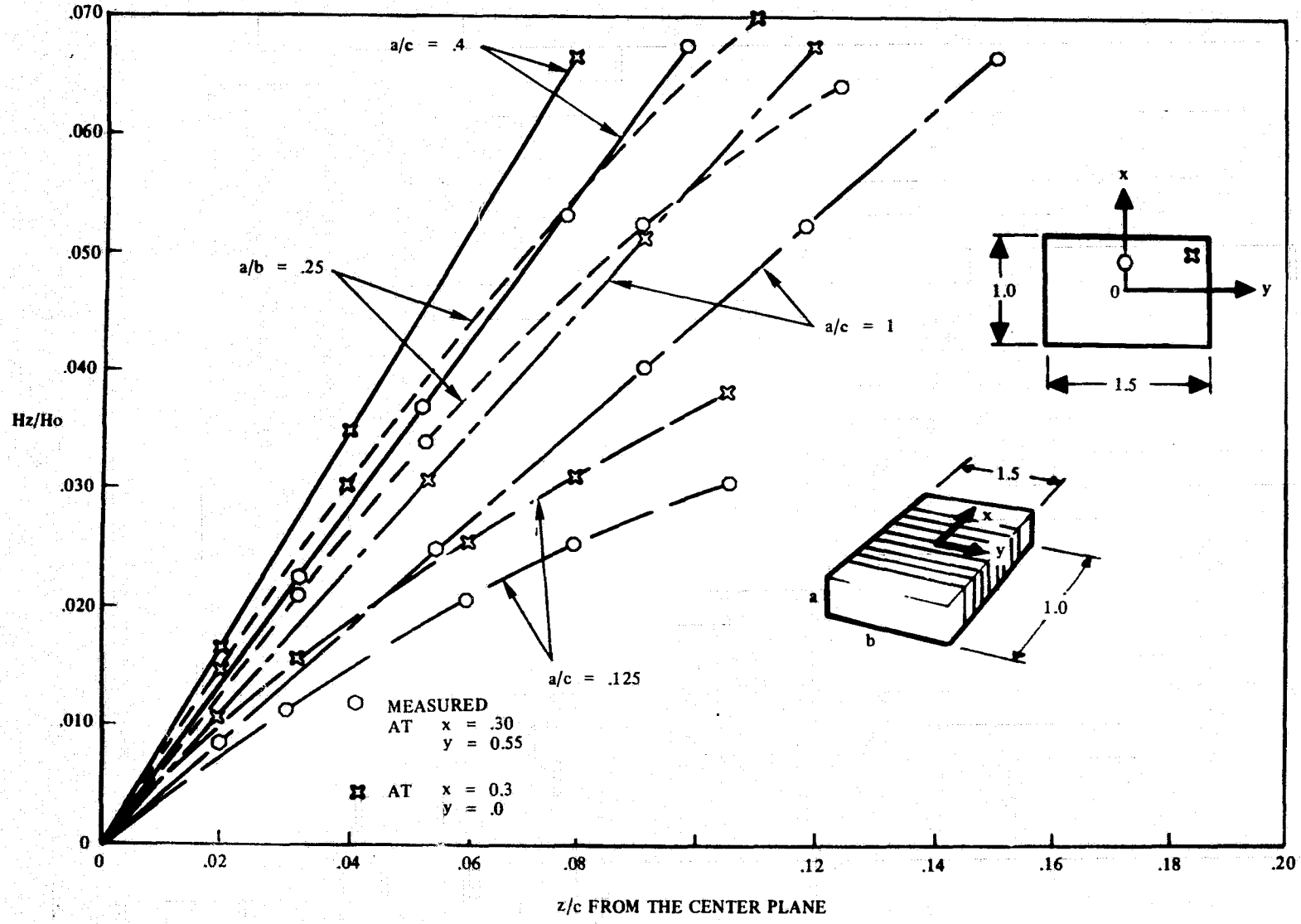


Figure 52. Hz vs z in a Flat Coil

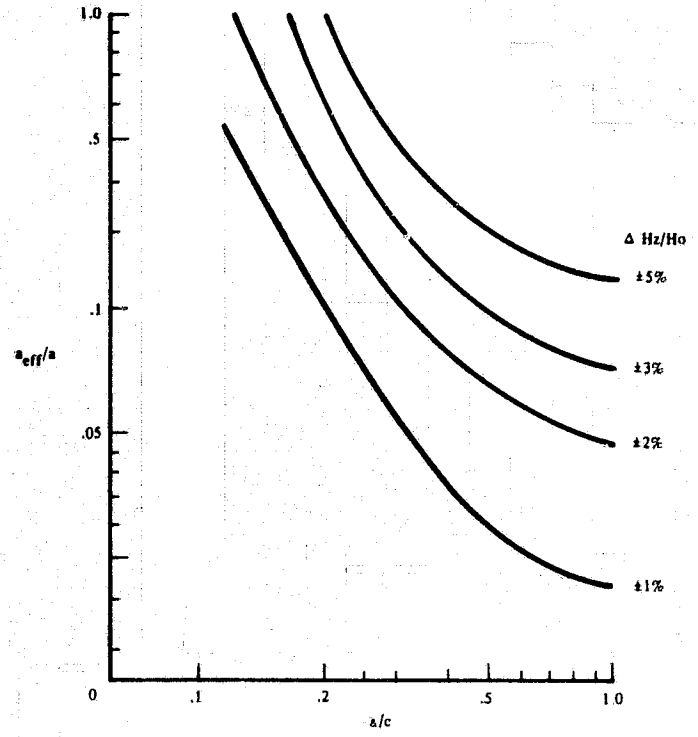


Figure 53. Effective Coil Height as a Function of Coil Height-to-Length Ratio in the Area with $|x|/c < 0.3$

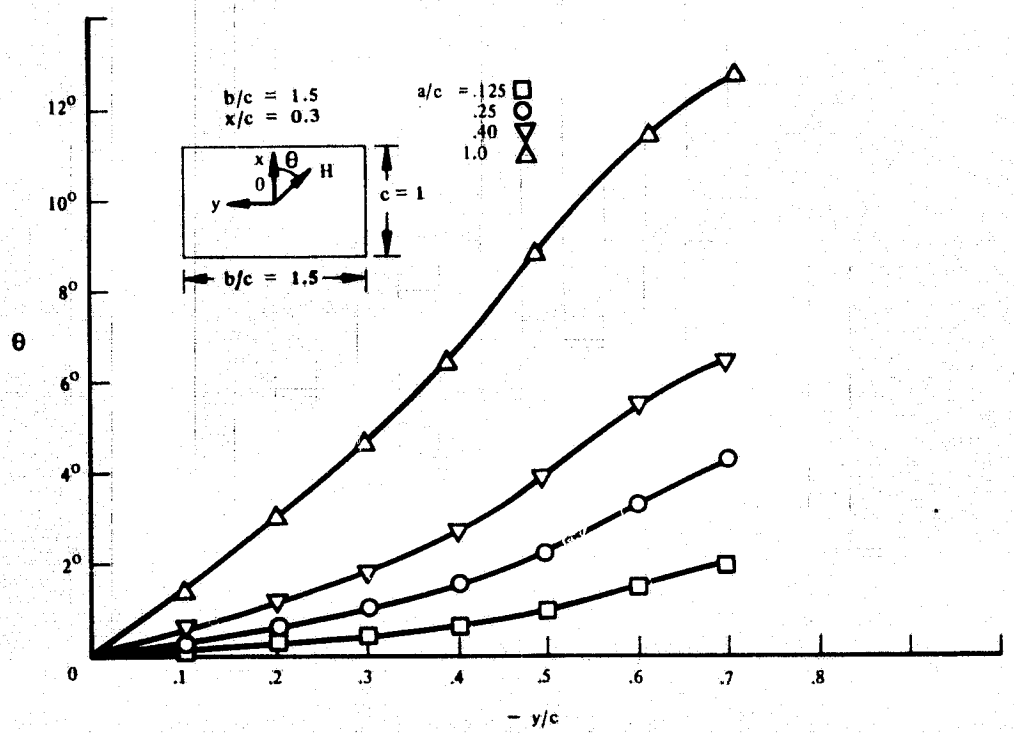


Figure 54. Angular Deviation of the In-Plane Field as a Function of Position

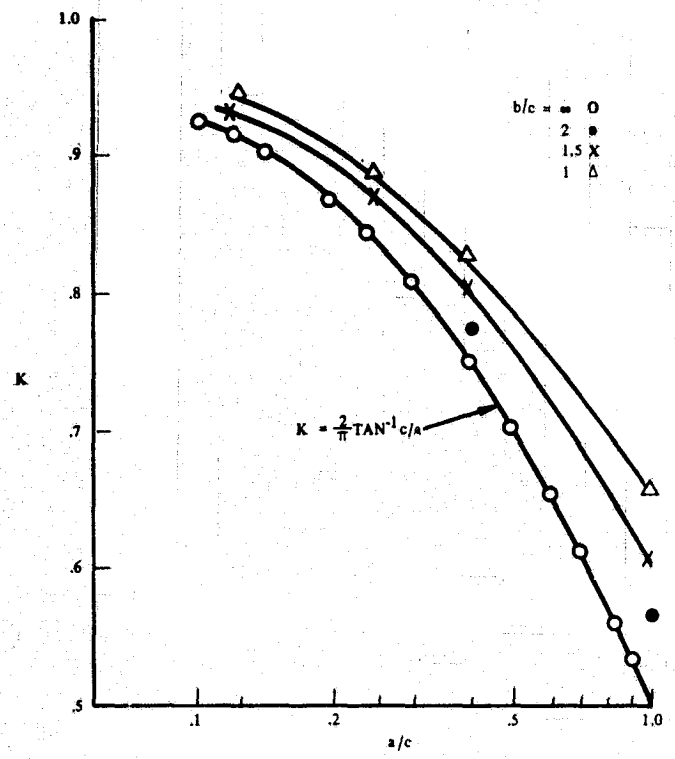


Figure 55. Coil Sensitivity as a Function of Geometry

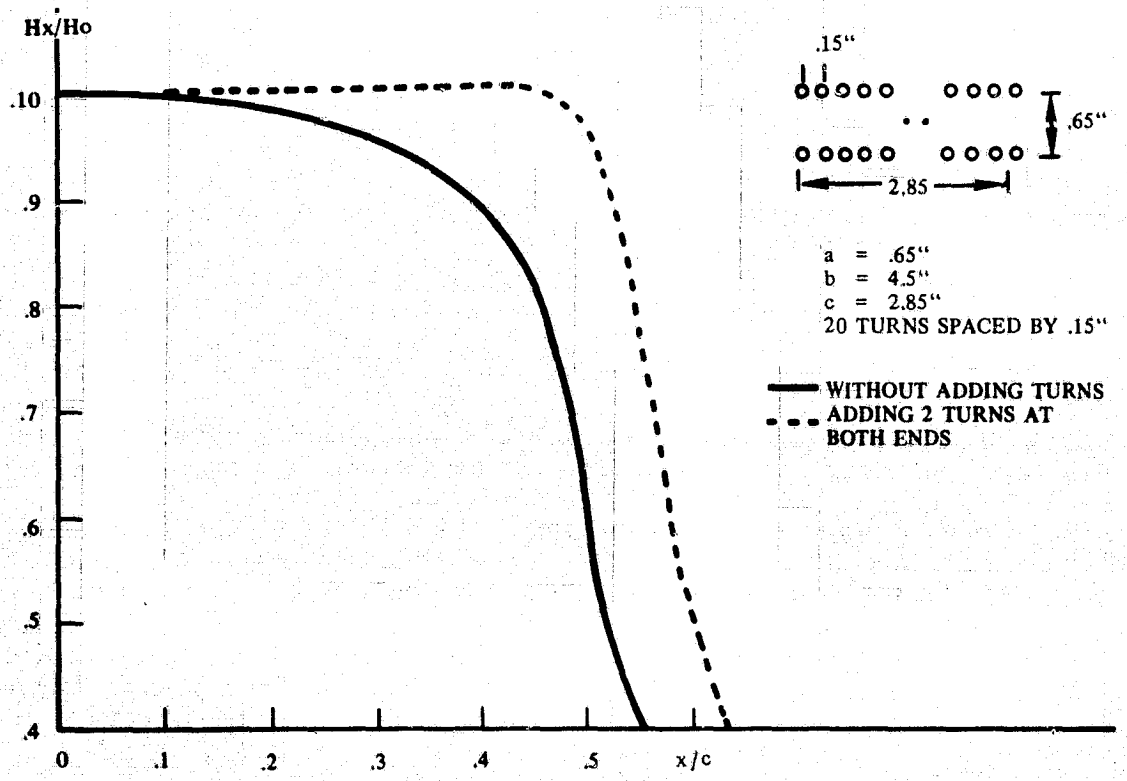


Figure 56. Axial Field Distribution in a Flat Coil With and Without Compensating Turns

Leakage field. — As can be seen from Figures 48 and 56, the magnetic field outside the coil depends on the height of the coil but they all drop off rapidly at a distance of several coil heights away. In the coil package arrangement shown in Figure 45, there is a definite spacing between devices mounted in different coils for device control leads and coil windings. For a flat-coil design, this spacing is sufficient to decouple the leakage field generated from one coil assembly to effect the bubble domain stored in a nearby coil assembly.

5.1.3 Coil loss. — In the field coil design it is important to keep the coil dissipation low, not only for a minimal system power requirement but also for a better device thermal stability. The later is due to the fact that when memory devices are mounted close to the field coil, excessive heating in the coil will raise the device operating temperature causing mismatch between the device bias margin and the permanent magnet bias field supply.

The bubble memory chips and their package consists mostly of nonmagnetic and high resistivity material whose magnetic and eddy current loss in a rotating magnetic field is very small. The power loss in the drive field coil then is primarily due to the joule heating in the coil itself.

Equation 6 shows that d-c power loss in a flat coil is inversely proportional to the wire diameter and the number of turns in the winding. When operated at high frequency, additional a-c loss is introduced by the eddy current effect (skin effect and proximity effect) and stray capacitance effect. When the coil operating frequency is less than its self resonant frequency, the stray capacitance of the coil can be treated as an equivalent capacitor connected in parallel with the coil. The apparant resistance Req in this circuit then is given by (Ref 7).

$$Req = R/(1-\gamma^2)2$$

where R is the true coil resistance and γ is the ratio of the operating frequency to the coil lowest self resonant frequency. Empirical formula have been developed to calculate the a-c loss in solenoids due to skin effect and proximity effect. (Ref 8) Unfortunately, when using an equivalent sized circular solenoid to represent the flat coil, the calculated a-c resistance show less frequency dependence than the measured value. An attempt was made to calculate the a-c loss in a flat coil system on a wire-by-wire basis. However, the work has not progressed too far because of the complexity of the problem. The problem was also attacked experimentally by measuring the loss in different windings. Some of the results are summarized in the following graphs.

The coil loss is determined by measuring the field sensitivity of the coil and the resonance resistance of the coil when it is connected in series with a low loss capacitance. (G.R. Type 1419-B Polystyrene Capacitor Box.) The field sensitivity is measured by inserting a small sensing coil in the coil to be tested and measuring the $d\phi/dt$ voltage. In all the measurements the induced voltage is linearly proportional to the frequency so that the a-c field sensitivity can be simply represented by the d-c field sensitivity measured by Hall probe. (This assumption is only valid when the operating frequency is lower than the coil self resonant frequency).

Loss in simple windings. — Figure 57 shows some resonance resistance measurements on different windings wound around a 1 in. x 1.5 in. x 0.06 in. coil form. A thicker wire has lower d-c resistance but the loss increases faster at high frequency as compared with a thinner wire winding. When the power dissipation for fixed rotating field is plotted as a function of frequency for this particular coil size, as shown in Figure 58, above 500 kHz, the winding using AWG 32 wire dissipates the least power.

Using double layer windings can improve the power loss as indicated in Eq (6) but it also introduces additional high frequency loss as can be seen in Figure 57. Part of this additional loss results because the magnetic field in the winding area is not uniform, and the field changes polarity when moving across the winding. Thus, the eddy current induced in the winding are different between layers. At high frequency this effect will cause a nonuniform current distribution between layers (larger current density at outer layer) and result a higher a-c resistance in the coil.

This nonequal field distribution effect can be compensated for by using a Litz wire type winding (Ref 9). This type of conductor consists of a large number of strands of fine wire that are insulated from each other except at the ends where various wires are connected in parallel. The strands are woven in such a way that each strand occupies all possible positions in the cable to approximately the same extent. This results in an equalizing of the flux linkage on each strand and causes the current to divide uniformly between strands. Two measurements on Litz wire winding are also shown in Figure 57. The improvement is not very significant. Although the Litz wire winding is expected to have a flat frequency response in the low radio frequency range, the present data does not show any definite advantage over the single strand wire at higher frequencies. Besides, the wire is bulky, difficult to handle, and expensive.

Loss in split windings. — Other than Litz wire winding, another technique can be used to avoid the nonequal current distribution between different layers in simple windings. That is by using several parallel wires for each layer but put all layers in series. This arrangement is equivalent to use a ribbon type conductor with thin but wide cross section and put all turns in series. The optimum thickness for the conductor should be equal to twice of the skin depth at the operating frequency. An example is illustrated in Figure 59.

For a large size coil, the a-c loss in the winding also increases as a result of higher coil inductance and stray capacitance. An example is shown in Figure 59. To circumvent this effect the inductance of the coil has to be kept low by reducing the effective number of turns in the coil. This can be done by either parallelling a large number of conductors in the layer (or use wider ribbon) or by splitting the coil winding into smaller sections and driving these sections in parallel by one driver or driving them separately by several drivers. Figure 59 also shows the effect of this split winding in reducing the coil inductance and improving the frequency response.

Loss in spaced windings. — In a large size coil, the coupling between wires can be reduced effectively by increasing the spacing between conductors. (Ref 10). An example is shown in Figure 61 where a loosely wound see through coil is compared with

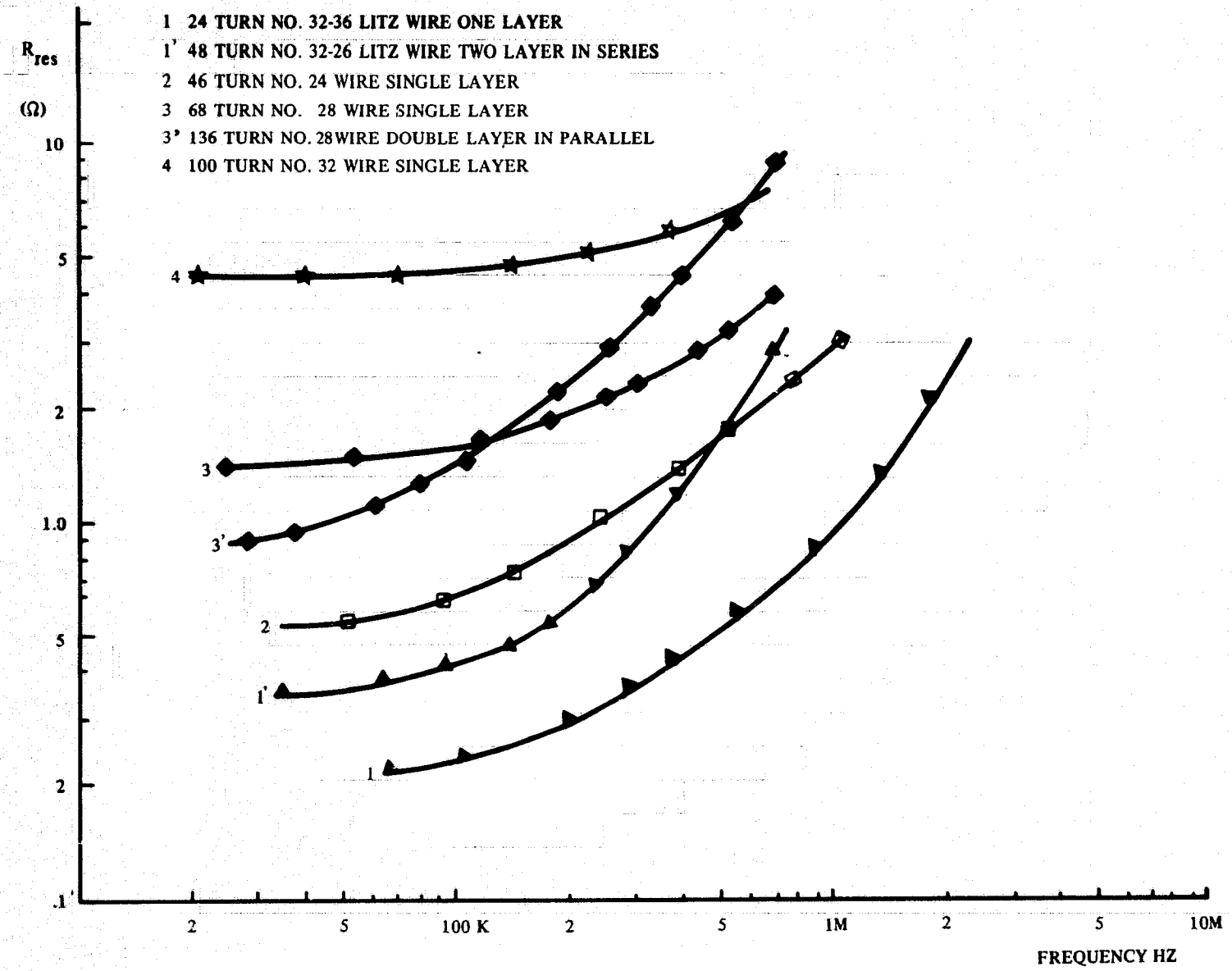


Figure 57. Resonance Resistance Measurements on Different Windings

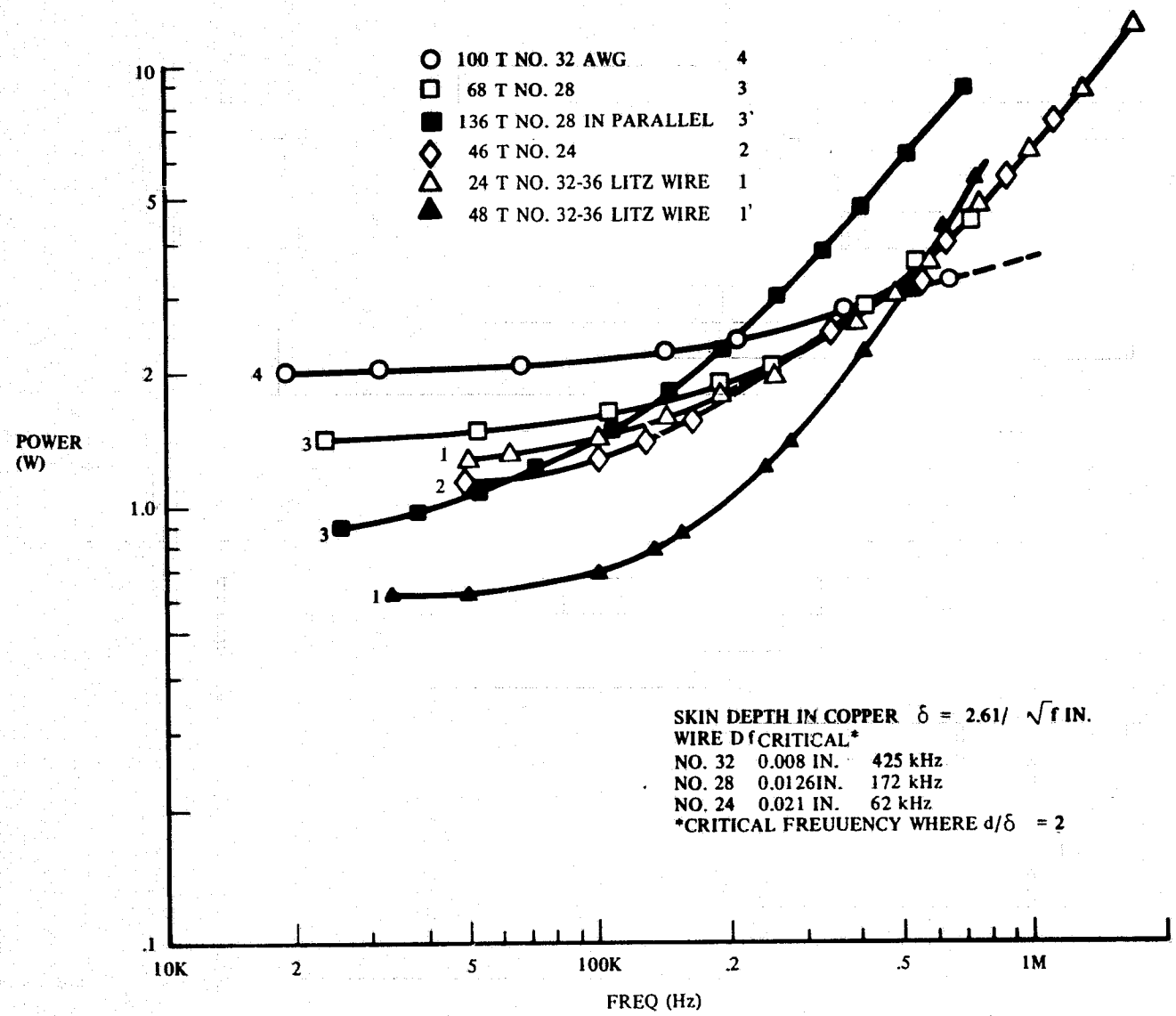


Figure 58. Power Dissipation for 30 Oe Peak Field in Different Windings Shown in Figure 57

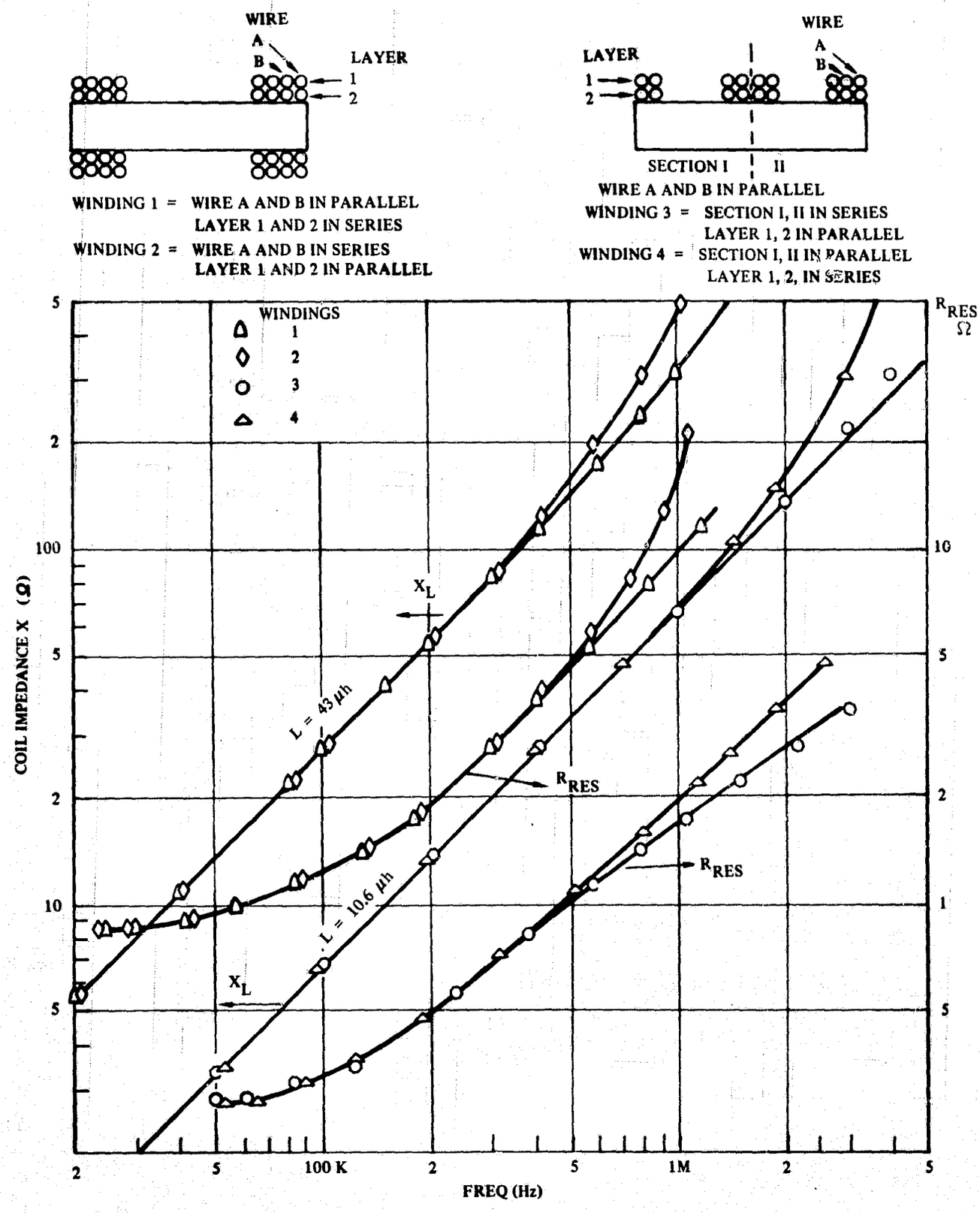


Figure 59. Loss in Split Winding Coils

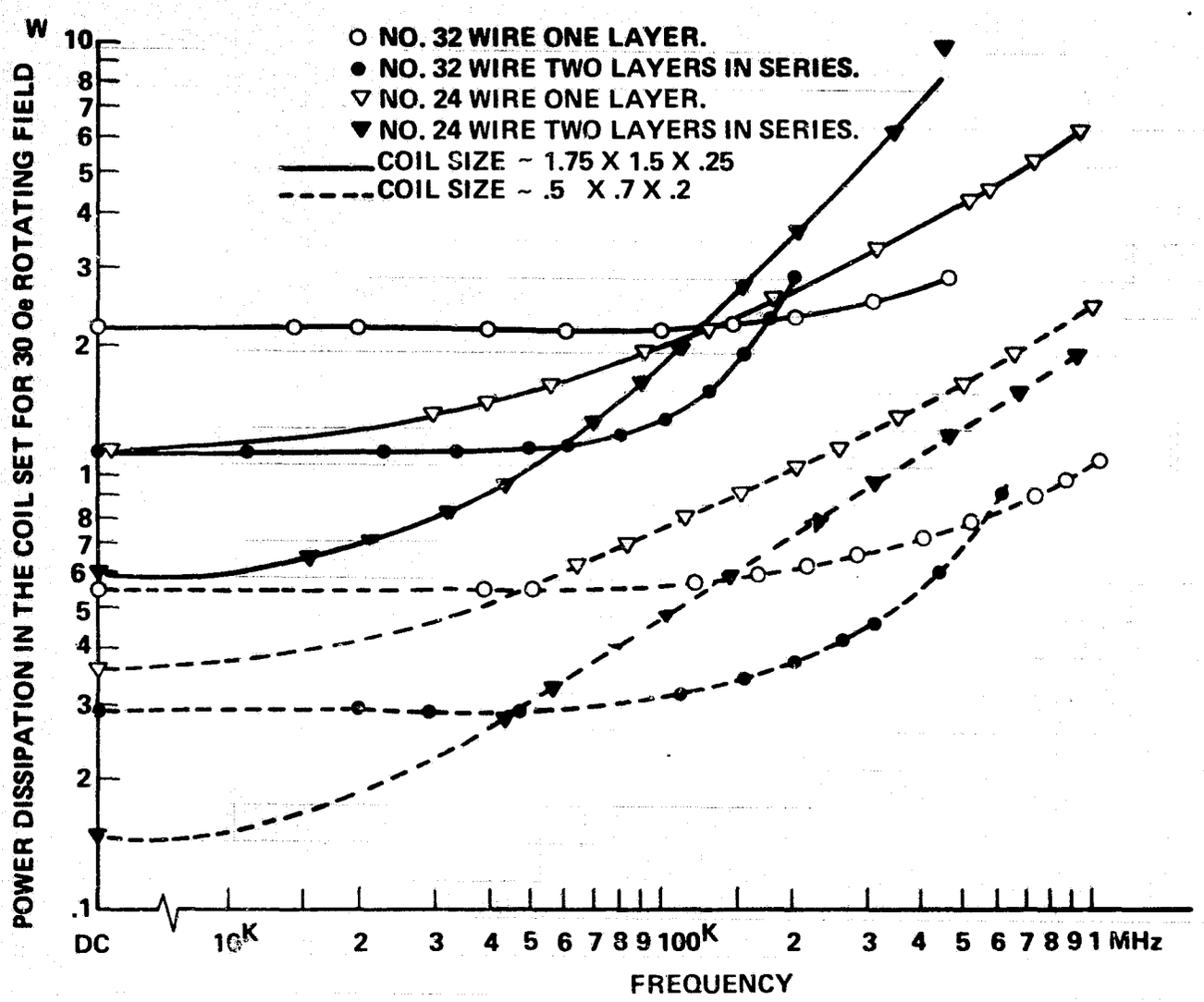


Figure 60. Power Dissipation vs Frequency for Coils with Different Windings and Sizes

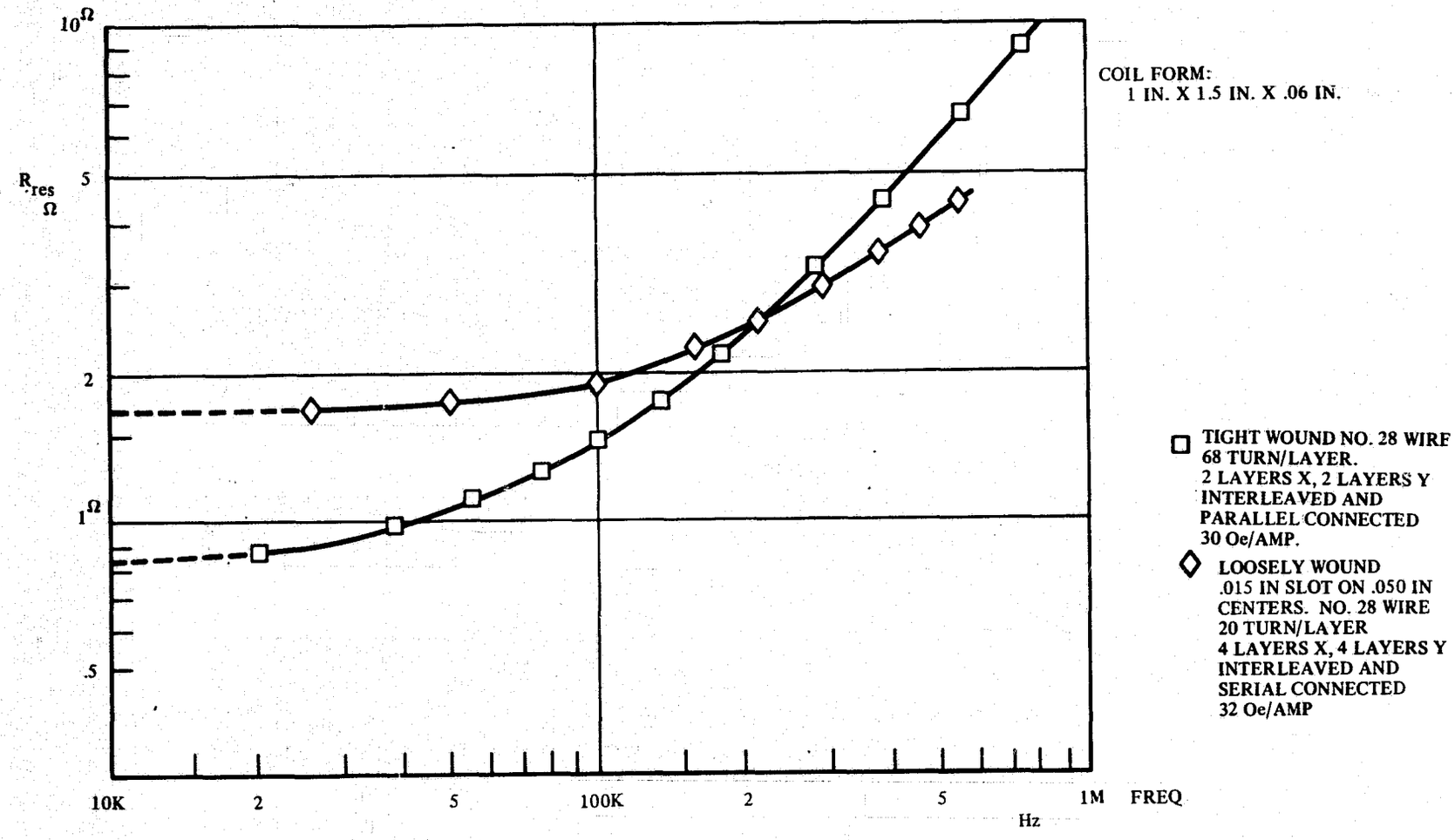


Figure 61. Coils with Spaced Winding and Solid Winding

a same size solid coil. The coil sensitivities are very close so that the same graph also compares the power loss in the windings. At low frequency the solid winding consumes about half of the power of the spaced winding because the former has more conductor area in the winding. As frequency goes up, the power dissipation in the see-through coil increases slower than the solid coil because of the spacing between the conductors. Above 200 kHz, the see through coil actually performs better than solid coil.

This spaced winding is difficult to fabricate, need proper wire guide to control the spacing between wires, it is bulkier thus poorer field uniformity than the corresponding solid coil. But it can accommodate some field compensating turns as discussed in subsection field uniformity and has better heat dissipation because the cooling air can flow through the winding.

Summary. — Based on the above experimental results the following conclusions can be made on how to improve the frequency response of a high frequency field coil. The best winding for the coil would be a ribbon type single conductor, with a thickness equal to twice the skin depth and wound in series between layers. The inductance of the coil has to be kept as low as possible to minimize the stray capacitance loss. This inductance adjustment can be by increasing the ribbon conductor width or by subdividing the winding into smaller sections in the case of large coil. A properly controlled spacing between windings is favorable from the standpoint of reducing the high frequency loss, although it increases the d-c loss by reducing the available amount of conductor in the winding. But, all these techniques can only reduce some of the coupling loss. In the development of a high frequency field access type bubble memory the field coil design will be a major obstacle.

Coupling loss. — When the magnetic module is assembled, the coupling between orthogonal windings and between the coils and the bias structure will result in additional power loss. The eddy current loss due to the metalization in the substrate packages is negligible as compared with the other two coupling losses.

To generate a rotating field, two orthogonal coils are placed against each other which causes coupling between them. First, there is additional stray capacitance which lowers the self resonance frequency and introducing additional loss. Reducing the coil inductance will minimize the effect. Secondly there is eddy current loss in the other winding. If small wires are used this loss can be very small.

The principle loss results from the coupling between in-plane field coil and the bias plates. Since the bias plates are made of thick permalloy they will introduce large a-c loss to the coil if the coil is close to the plate. A simple way to decouple the rotating field from the bias plate is by inserting a thin copper foil between them. The eddy current generated in the copper foil can prevent the high frequency field from penetrating into the bias plate. The copper foil approach is inexpensive and simple and the nonmagnetic foil will not disturb the bias field. However, the eddy current loss in the foil can be larger than the bias plate coupling loss if the foil is too thick.

Another decoupling approach is to use a low loss magnetic shunt which will sink all the external flux from the coil and have very little high frequency loss in itself. One such shunt material is a low-loss ferrite plate. Figure 62 compares the coupling loss between no shield, copper foil shield and ferrite plate shields. The results indicate that the ferrite plate shield is very effective up to very high frequencies. However, as the ferrite plate is magnetic the ferrite plate has to be flat, (provide a constant gap in the device area) in order to maintain the uniformity of the bias field. In addition it must be uniform in composition and thick enough to ensure low magnetic loss in itself. For a large size coil a flat ferrite plate approach can be very expensive.

5.1.4 Stripline coil. — In a large capacity recorder, a large number of small rotating field coils have to be employed because of the power dissipation and packaging complexity limitations. Thus, the reproducibility of the coils has to be controlled. This section proposes a stripline coil structure which can be batch fabricated while providing better manufacturing control than the regular wire wound coil.

The basic arrangement of the stripline coil is illustrated in Figure 63. A parallel conductor pattern is photolithographically etched on a strip of conductor foil supported by an insulating film (such as polyimide film). This strip is then wrapped around a coil form and shaped to the required dimension. The starting edge of the strip can be folded out and placed over the end edge of the strip. By shifting the conductor lines by one conductor spacing and connecting all the matched conductors on both edges, the conductors will be connected in series to form a single coil winding. Since there is only one strip to be wound the coil geometry and inductance are much easier to control than the multiple turn wire wound coils.

Besides being simpler in construction, the stripline coil actually offers the optimum configuration for reducing the high frequency loss. Since photolithographic techniques are used, the conductor width and the spacing between conductors can easily be adjusted for optimum coil inductance and a-c loss. The conductor strip itself is equivalent to a flat conductor ribbon which should offer better high frequency response. In addition for the multiple layer structures, the conductors are series in each turn first before being connected to the next turn, which is equivalent to the bank winding technique (Ref 10) for reducing the stray capacitance in the wire wound coil. Therefore, the stripline coil has some intrinsic advantages over the wire wound coil in terms of the high frequency coil loss.

The concept of improving field uniformity by increasing the current density at both ends of the coil can also be easily implemented in the structure. Since the conductors all have the same thickness and are connected in series, the current density in each conductor is inversely proportional to the conductor width. Thus, a perfect field compensation can be achieved by simply designing a conductor pattern with narrower width conductors at the edges of the coil.

Several stripline coils have been tested on this program. The field profile for a coil with an evenly distributed conductor pattern (which is similar to that of the wire wound coil) is shown in Figure 64. The effect of variable width conductor pattern is simulated by shorting the inner turns of this coil. Definite improvement in the field uniformity can be observed in the figure.

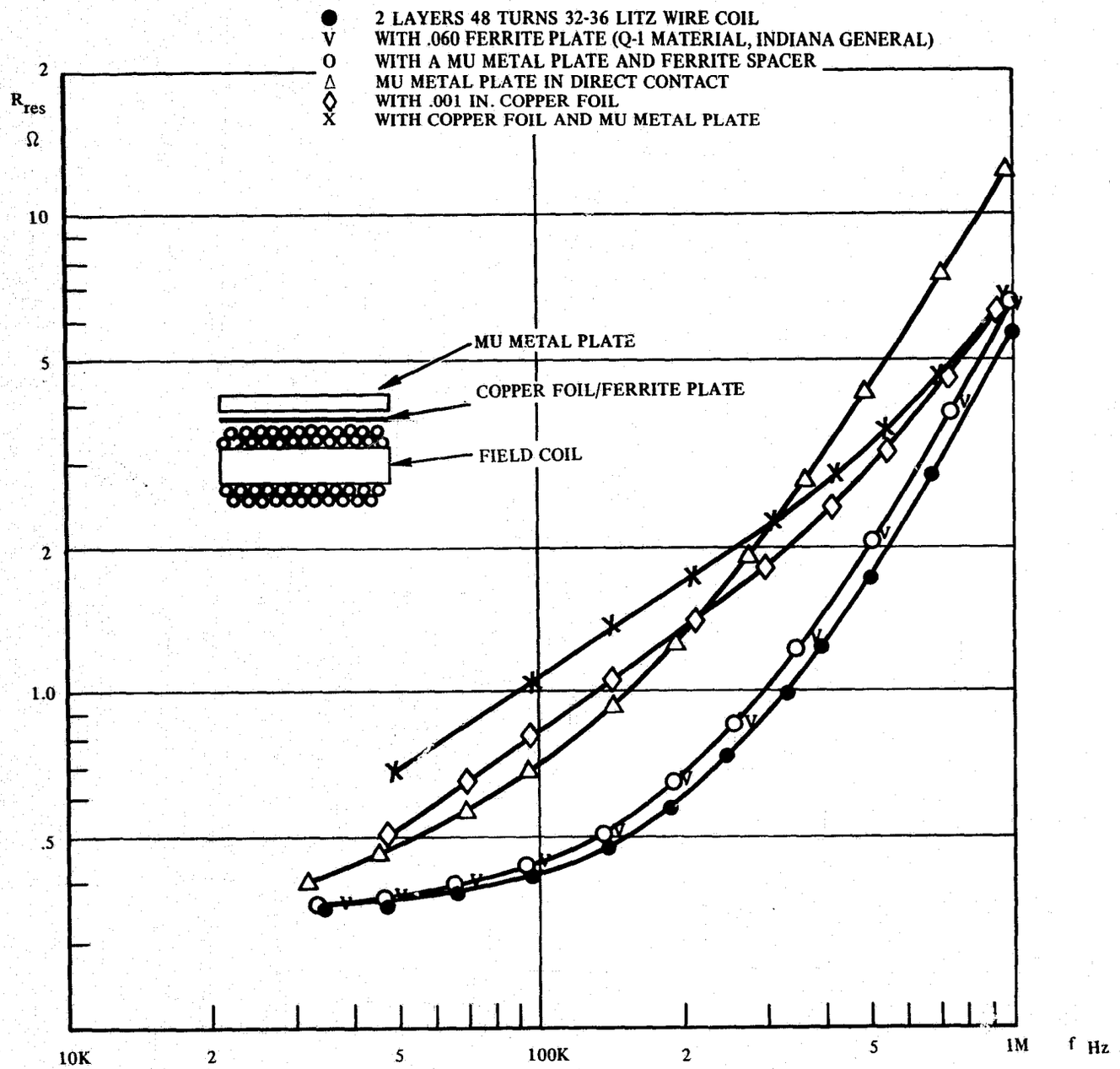
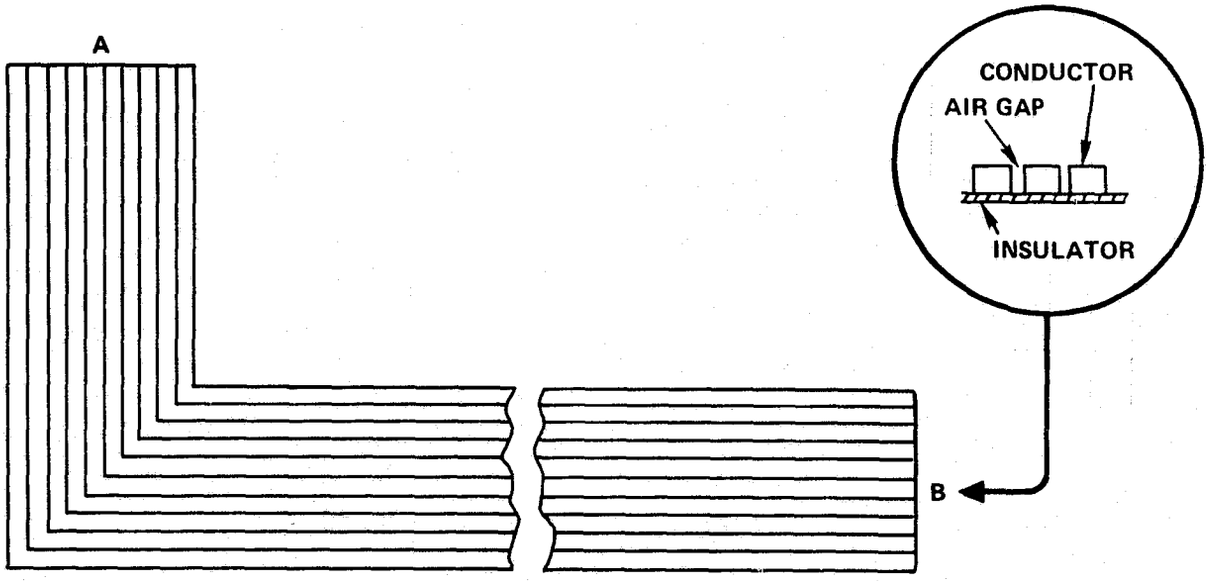
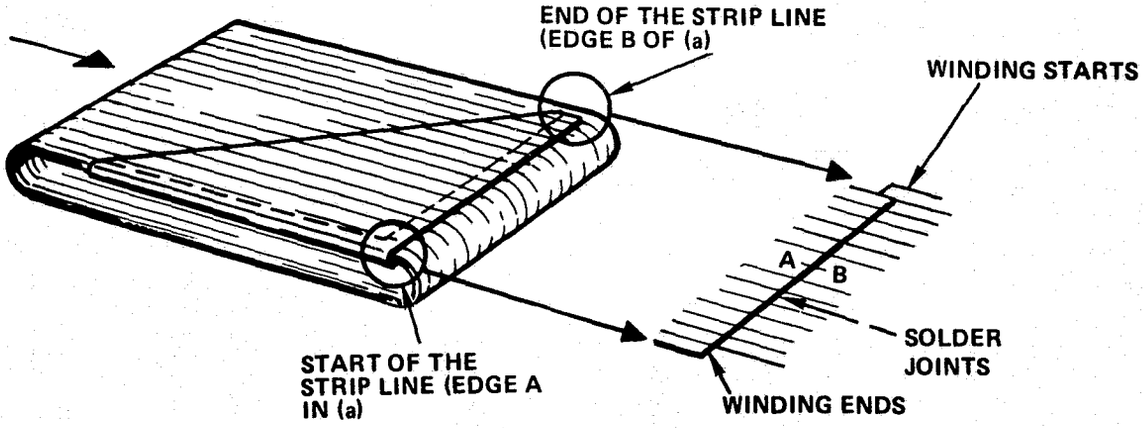


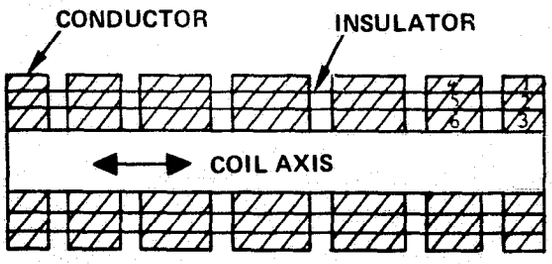
Figure 62. Coupling Loss Between In-plane Coil and Bias Plate with Ferrite and Copper Foil Shield



(a) Etched Strip Line Pattern



(b) Strip Line Coil Winding



(c) A Variable Width Strip Line Coil

Figure 63. A Stripline Coil Configuration

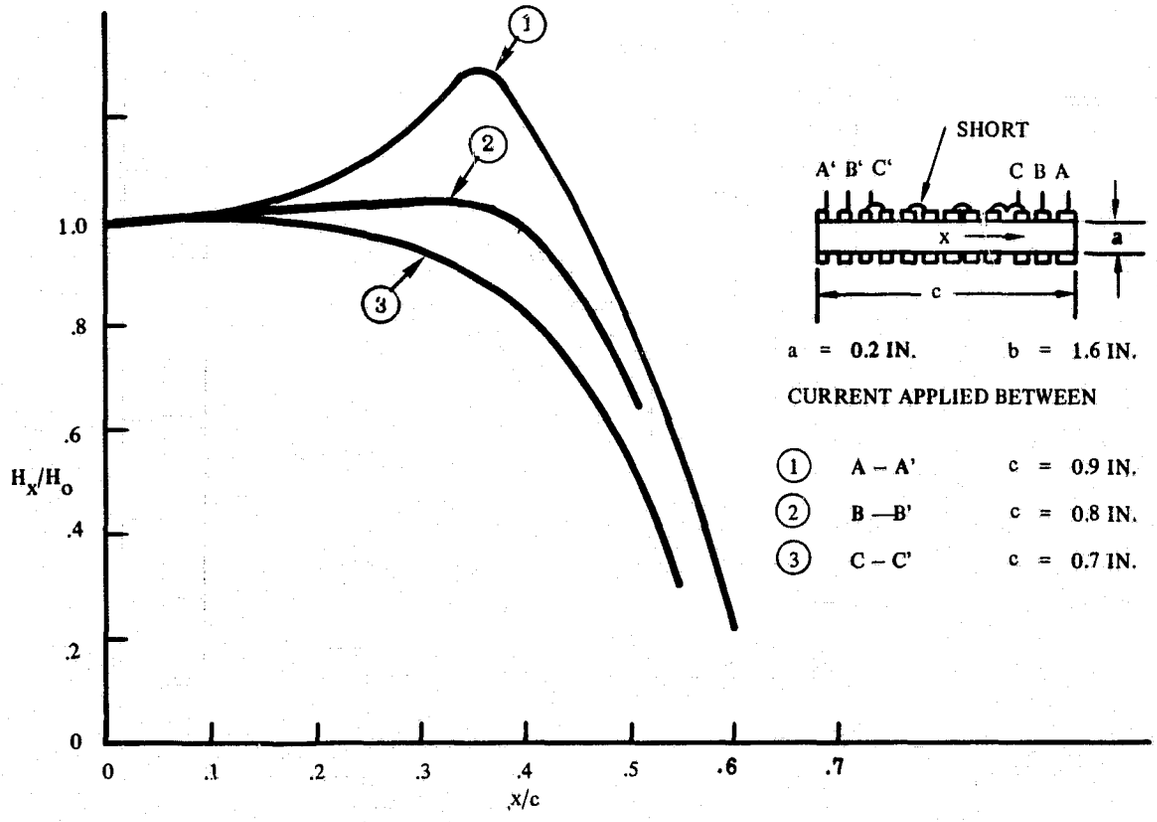


Figure 64. Axial Field Distribution in a Stripline Coil

Figure 65 shows the coil loss as a function of frequency for three stripline coils with different number of layers. The frequency response is smoother than the wire wound coil but the slope does increase with the number of layers. One drawback of present stripline coils is that the power dissipation is higher than the corresponding wire wound coil of the same dimension. This result is due to the polyimide film used which has only 0.002 in. thick copper on a 0.002 in. thick insulator. This arrangement is rather inefficient because of the low ratio between conductor area and the winding cross section area. In addition the conductor of stripline is plated copper which has higher resistivity than the solid copper wire.

For an optimum use of the stripline conductor, the conductor thickness has to be twice its skin depth ($\delta = 2.61/\sqrt{f}$ in. for copper). For moderate frequency operation the conductor may have to be very thick (0.007 in. for 500 kHz). A thick conductor polyimide film is difficult to make as the copper tends to crack during the coil wrapping operation. Also a thick conductor pattern is difficult to define in the chemical etching process. A possible solution to this problem is to use a polyimide film that has both sides plated with conductor films. In this arrangement, the film thickness can be half of that required for single sided film and the etching and stress problems are not amplified. The conductors on both side of the insulating films can be connected in parallel during coil wrapping to form an equivalent thick film as illustrated in Figure 66.

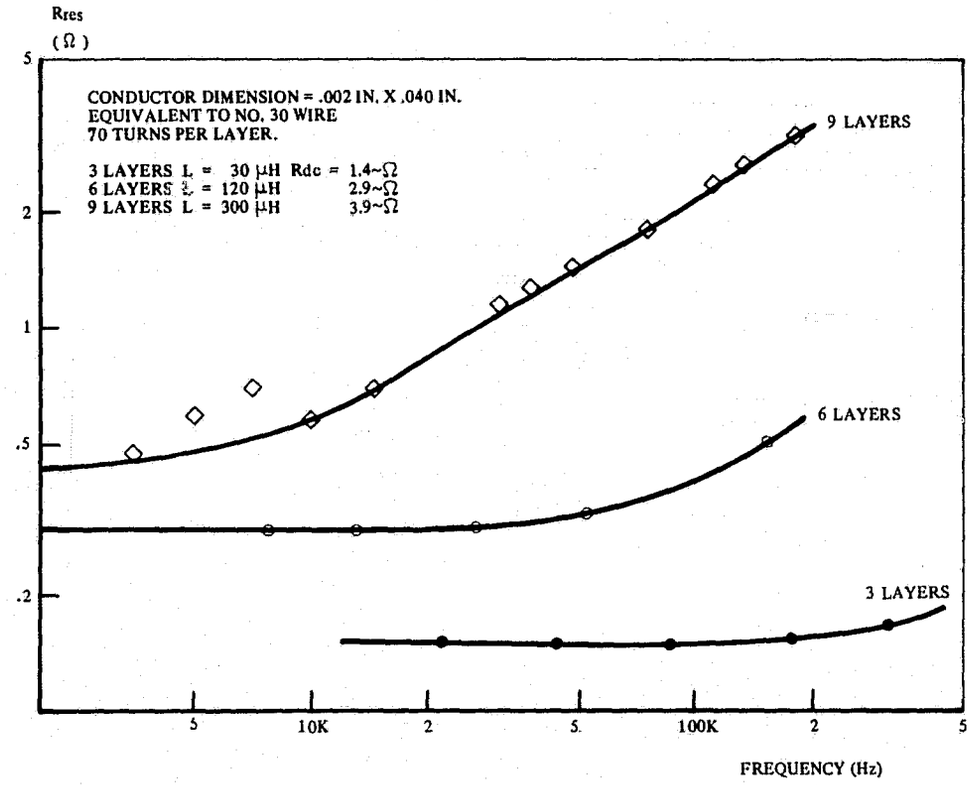


Figure 65. Resonance Resistance vs Frequency in Three Stripline Coils

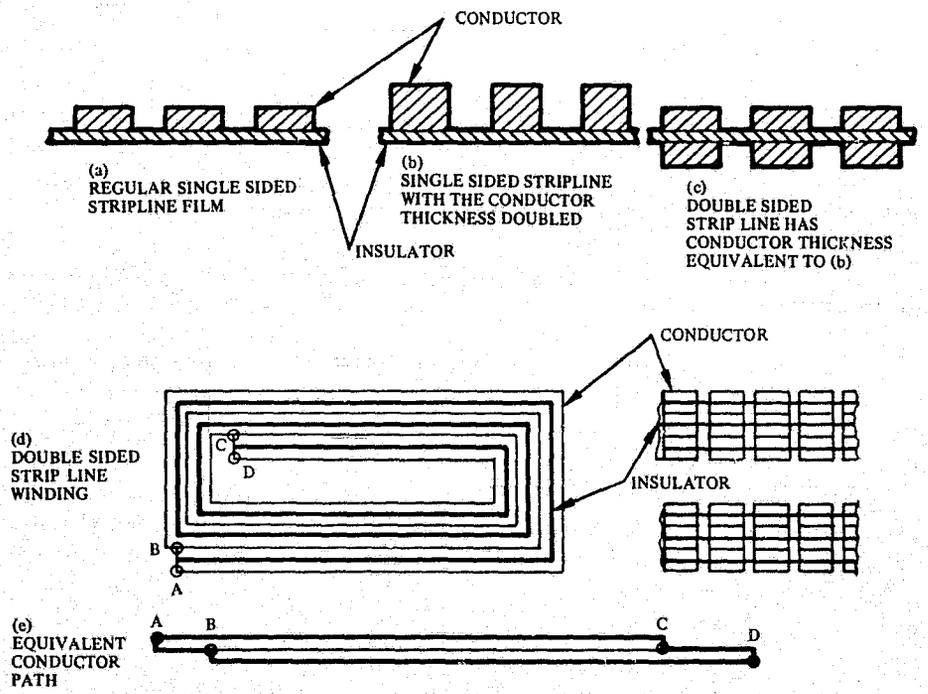


Figure 66. Doubled Sided Stripline Coil

5.2 Open Coil Structure

The concept of using an open coil structure is to utilize the magnetic flux outside of the solenoid so that the device access will not be limited by the coil structure. Three different concepts will be reviewed in this section, two of them are disclosed in the literature and the third one is developed in this program.

5.2.1 Ferrite pole structure (Ref 11) - The basic concept of this approach is derived from the early Helmholtz type coil arrangement where bubble devices are placed between two coils. Since a uniform field is only required in a very thin plane (~0.4μm) where the permalloy elements are located, the height of the Helmholtz coil can be compressed down to a flat coil shape to reduce the volume of the space over which the field is generated. To further minimize the magnetic reluctance in the flux return path, ferrite core can be inserted into the coil and circled by a ferrite ring as shown in Figure 67.

The field uniformity between two flat coils can be calculated in the same way as for the field inside the coil. The uniform area is found to be rather small as compared to the overall area occupied by the two coil pairs. Although the use of ferrite pole pieces can improve the field uniformity it also may introduce distortions as a result of the coupling between x and y pole pieces. Figure 68 shows a field mapping on a pole piece model made of mu metal. For the present structure, the 20 percent field uniform area only occupies about 13 percent of the air gap area and is less than 1 percent of the total pole piece area. Shaping the pole face can improve the field uniformity but the total usable area is still small.

The sensitivity of this arrangement is also low. This is due to the large leakage path between pole pieces and also the large demagnetization factor of the pole piece itself. The demagnetization factor can be reduced either by increasing the length or by decreasing the thickness of the pole piece. In the first approach the overall coil area has to be expanded while in the latter approach the leakage field will be further increased and the alignment of the device to the coil plane becomes much more critical.

The overall efficiency of this network can be improved by matrixing these coils, as shown in Figure 67, so that the field from both ends of the pole piece can be utilized. This results in a large field network which requires large amounts of power to drive them simultaneously.

In summary, the ferrite pole structure is able to achieve an open structure but has the following disadvantages.

1. The active area is quite small as compared to the overall field network area.

2. All the coils in one plane have to be energized simultaneously which requires large driving power.

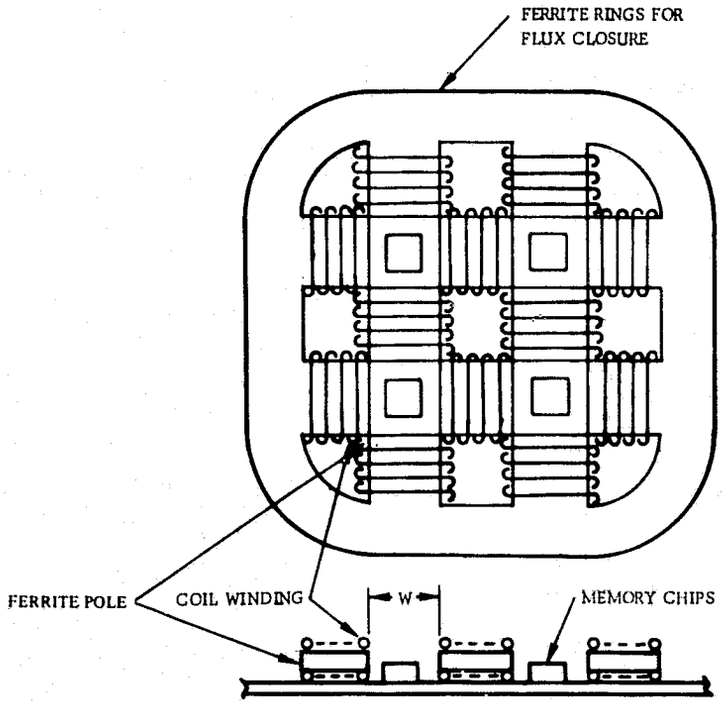


Figure 67. Ferrite Pole Structure

3. All the devices and coils have to be aligned in one plane which introduces packaging problems.

4. Ferrite poles will reduce the efficiency of the bias structure and also interfere with the rotating field in other device planes placed above or below them.

5.2.2 Flat-faced coil. (Ref 12) – The basic arrangement of flat-faced coil is illustrated in Figure 69. Instead of using a closed winding, the return path of the conductor current is spread into a plane forming a flat spiral coil. Two sides of this coil are straight with parallel wires. When two of the coils are placed face-to-face the magnetic field in the area between the straight sections of the coils is identical to that inside a flat solenoid coil. By placing two sets of these spiral coils perpendicular to each other, as shown in Figure 69, a rotating field can be achieved under the cross area of the straight sections. The detail of this coil design is discussed in the original paper and a prototype module using this coil has been successfully demonstrated at 100 kHz.

The flat-faced coil is simple in structure, easy to fabricate and can be mounted separately with the devices, but it also has the following restrictions.

1. The coil area can not be fully used because of the circular part of the spiral winding and the center open space required to minimize the interference between opposite current path.

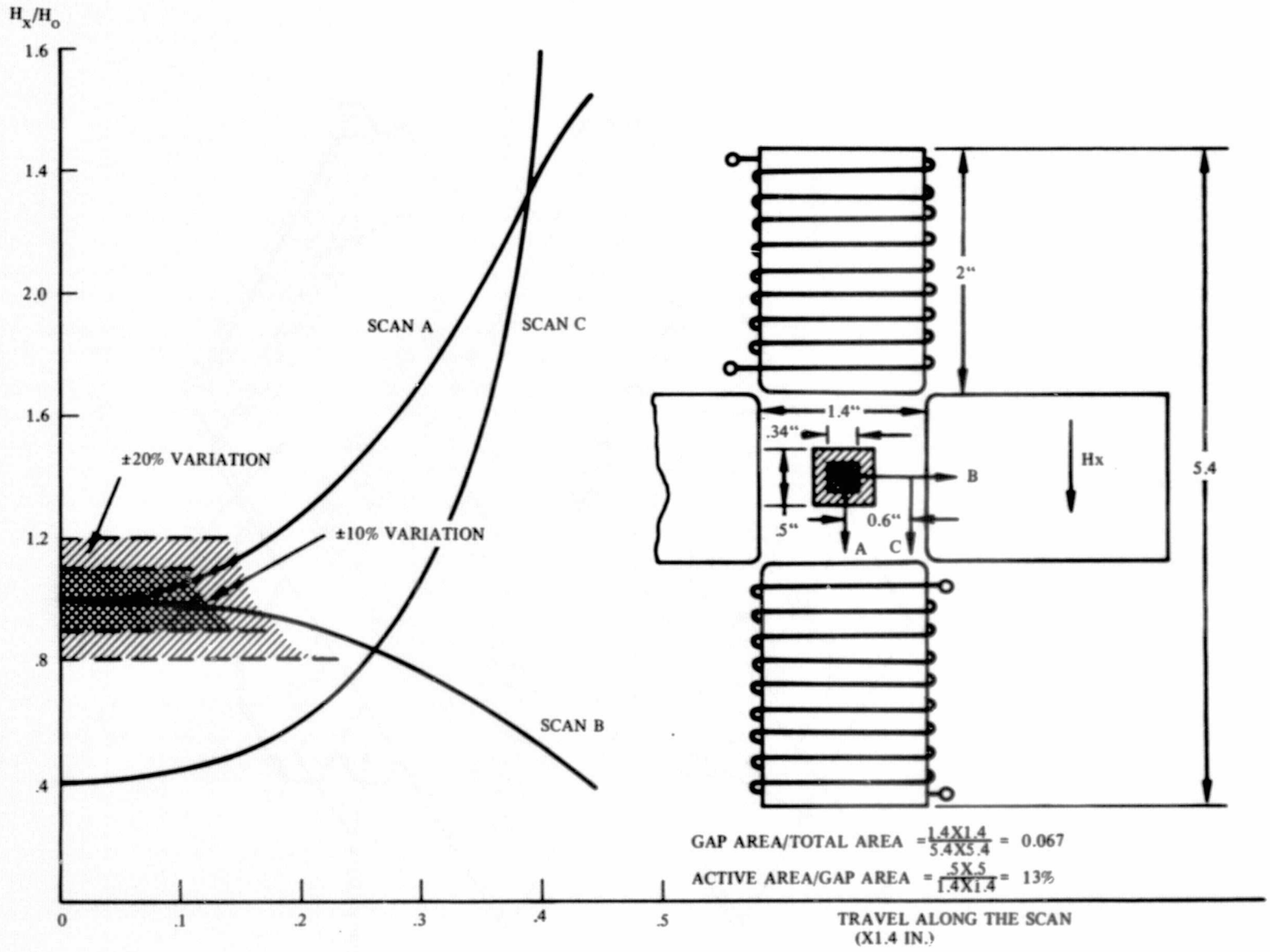


Figure 68. Field Mapping on Two Rectangular Pole Piece Pairs

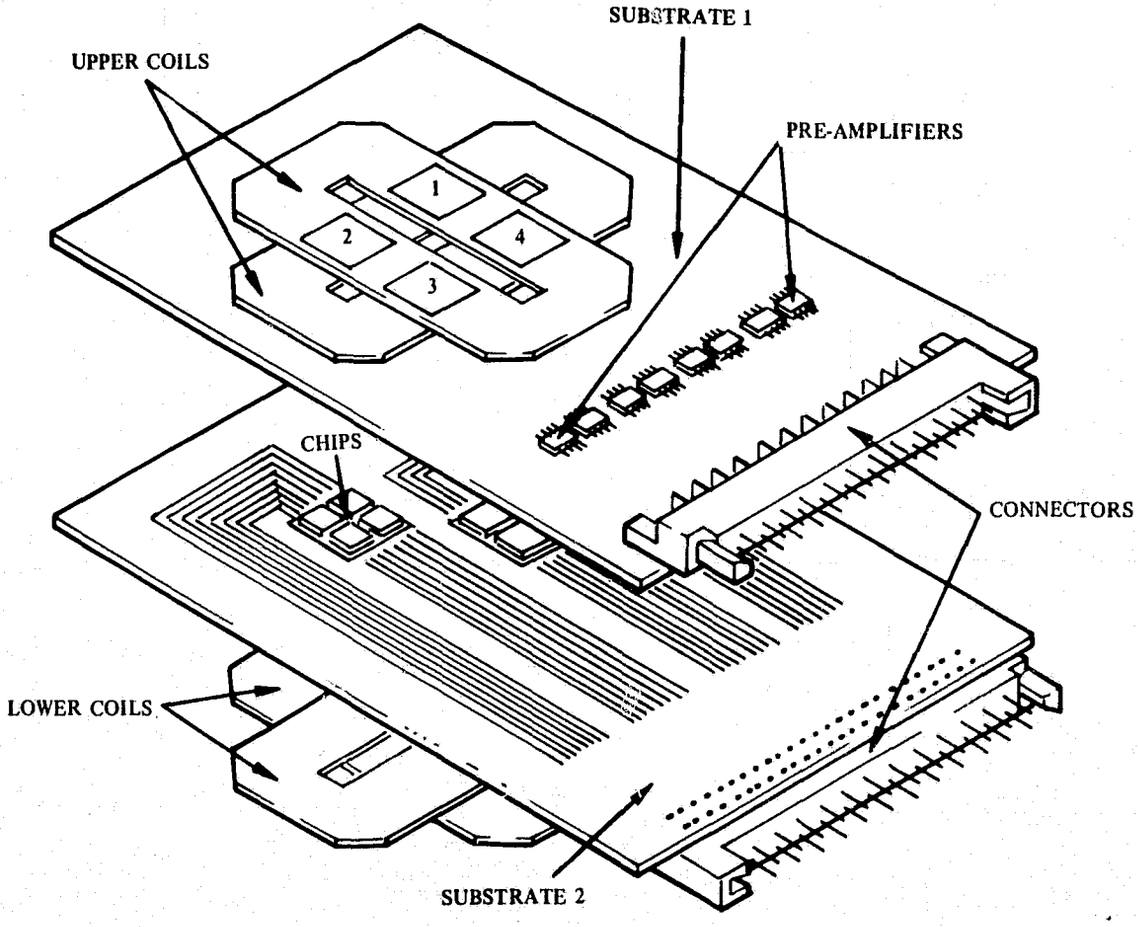


Figure 69. Flat Faced Coil for Bubble Package

2. The four usable spaces have different rotating field phasing and direction. A pair of memory chips with two different sense of rotations (clockwise and counterclockwise) has to be used.

3. Can not be stack packaged without additional decoupling provided by ferrite plates between coil planes.

5.2.3 Ferrite coil structure. — The H_x vs z plot in a flat air core coil indicates that the in-plane field drops off sharply when moving from the inside of the coil to the outside of the coil. This is because the magnetic field generated from the two current sheets in the coil winding cancel each other in the region outside of the coil. Inserting a magnetic shield between the coil windings will isolate the magnetic field from each current sheet, insuring that the magnetic field above each coil winding is equivalent to that generated by a single current sheet. The region between two face-to-face ferrite shielded coils is equivalent to an air core coil. This is the basic concept of the ferrite coil structure illustrated in Figure 70.

Several ferrite coils (No. 28 wire wrapped around 1 x 1 x 0.05 in. ferrite plates) have been made to test the feasibility of this concept. Figure 71 shows the in-plane field mapping inside a ferrite coil pair. The field distribution in the center part of the coil is similar to that in an equivalent size air core flat foil. However, near the edge of the ferrite plate, the in-plane field decreases quite rapidly and reverses polarity outside the ferrite plate area. The leakage field from the ferrite coil pair is much greater than the regular air core coil. This is expected because in the ferrite pole approach this leakage field is used to drive the devices.

To generate a rotating field, a second winding can be wrapped around the same ferrite plate in a direction perpendicular to the first winding so that two orthogonal fields can be generated with the same ferrite pair. A test coil set has been made using two ferrite coils for the in-plane rotating field and two pancake coils for the bias field supply. This coil structure is shown in Figure 72. The field distribution is similar to that in Figure 71. Devices mounted in ceramic packages have been tested successfully up to 50 kHz. Higher frequency operation is limited by the high coil loss due to ferrite plate loss and the capacitive loss caused by the high inductance in the ferrite coil. In the present test structure, the coil size is 1 x 1 x 0.1 in. with two parallel layers of 58 turns AWG 28 wire. The inductance is 260 μH and the self resonance frequency is around 300 kHz. The a-c resistance increases from 2 Ω at 10 kHz to 5 Ω at 50 kHz and 10 Ω at 100 kHz. This loss can be improved by using low loss ferrite plate and by rearranging the coil winding to lower the coil inductance.

In the ferrite coil pair, two coils are required to generate one rotating field. In order to utilize the field from the return path of the winding, several ferrite coils can be stacked so that bubble devices can be placed at both sides of the ferrite coil as shown in Figure 73.

Since the ferrite coils are completely separated from the memory devices they can be separately packaged as shown in Figure 74. Unlike the ferrite pole case, the coils are coupled between planes but not in the same plane, so that a large matrix plane can be built to share a single bias structure.

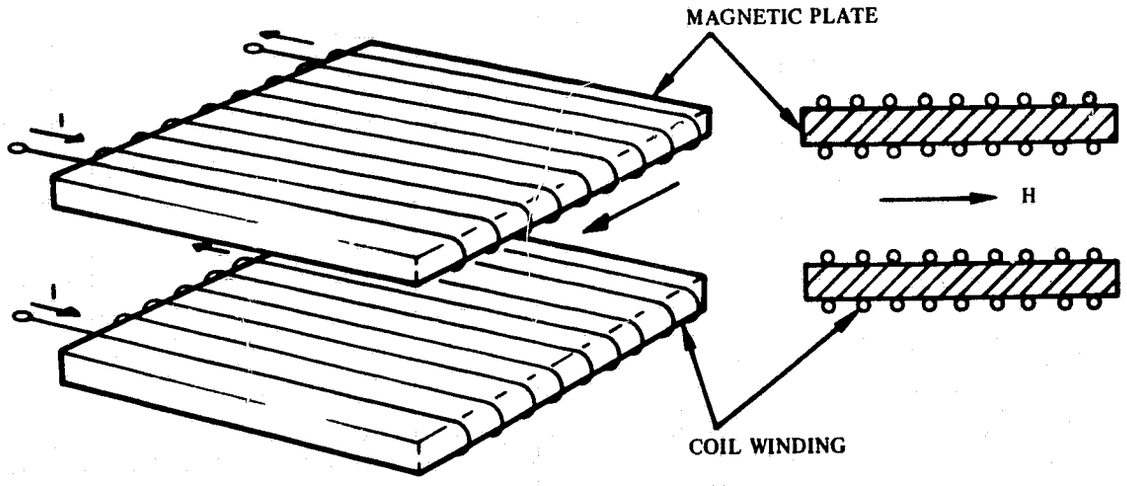


Figure 70. Magnetic Plate Core Coil

Compared to the other two approaches, this structure is more compact, can be stack packaged and has no phase difference in each available rotating field region. However, there are many potential problems which have to be investigated further. These include the high frequency coil loss, the high inductance associated with the coil, the coupling between coil pairs in the matrix, the coupling between two orthogonal windings in the same ferrite plate, the bias structure design for the stacking coils and the effect of ferrite material nonuniformity on the high frequency field distribution, etc.

5.3 Conclusion

At the present time, the coil power dissipation is the main concern in the design of the rotating field network for the bubble memory recorder. In both the open coil and close coil approach, the rotating fields are all generated from the same coil winding, and thus they have the same high frequency loss problem. If a thick conductor polyimide film can be made, the stripline coil structure should be the optimum design for a high frequency low loss coil. Intrinsically, the closed flat coil approach should give lower power dissipation than any of the open coil structures.

Both the flat face coil and the ferrite coil packages offer the attractive features of being open structures so that device packaging is simpler and the thermal stability is better than the close coil arrangement. However, because of the power dissipation, size and weight limit, they are not suitable for bubble recorder application at this time.

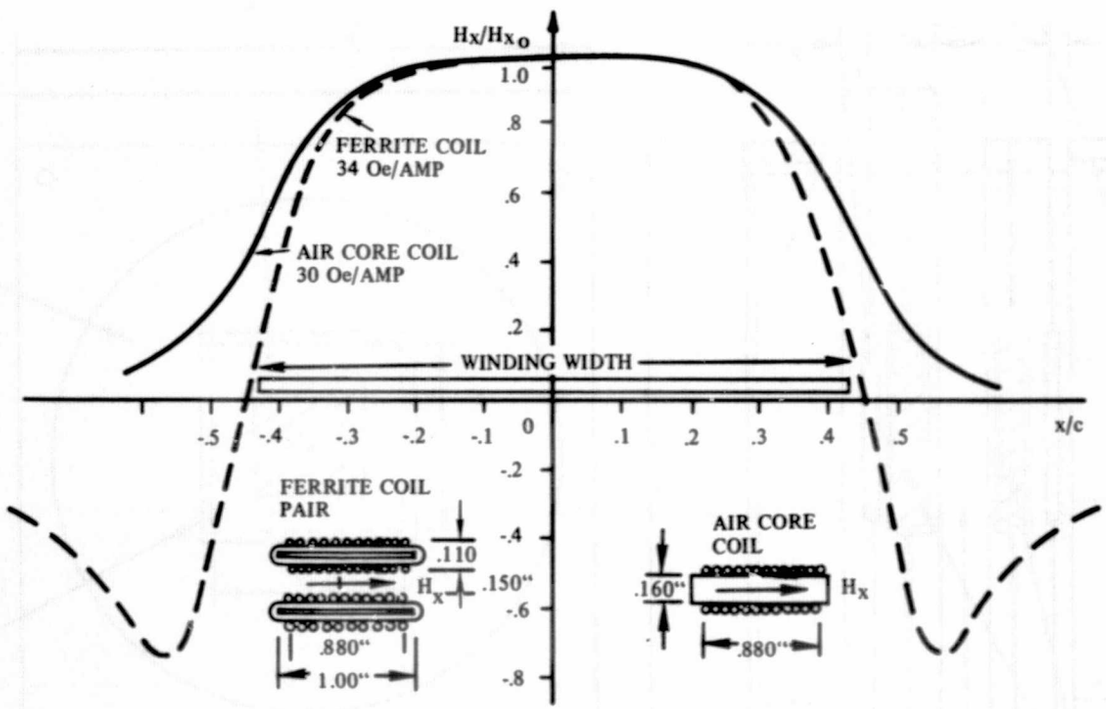


Figure 71. Axial Field Distribution in an Air Core Coil and a Ferrite Coil Pair (Mapped Under d-c Current)

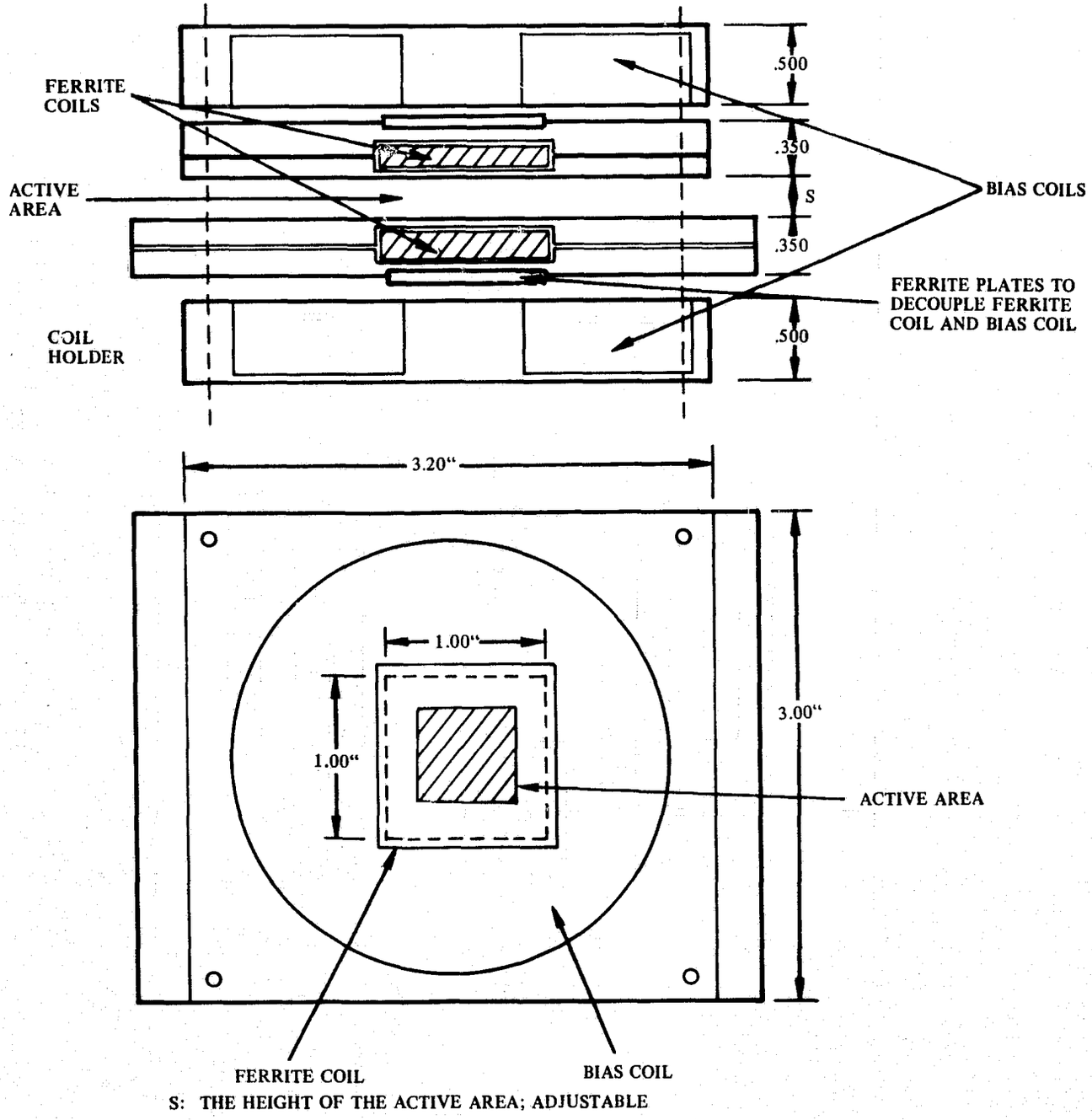


Figure 72. A Ferrite Coil Structure

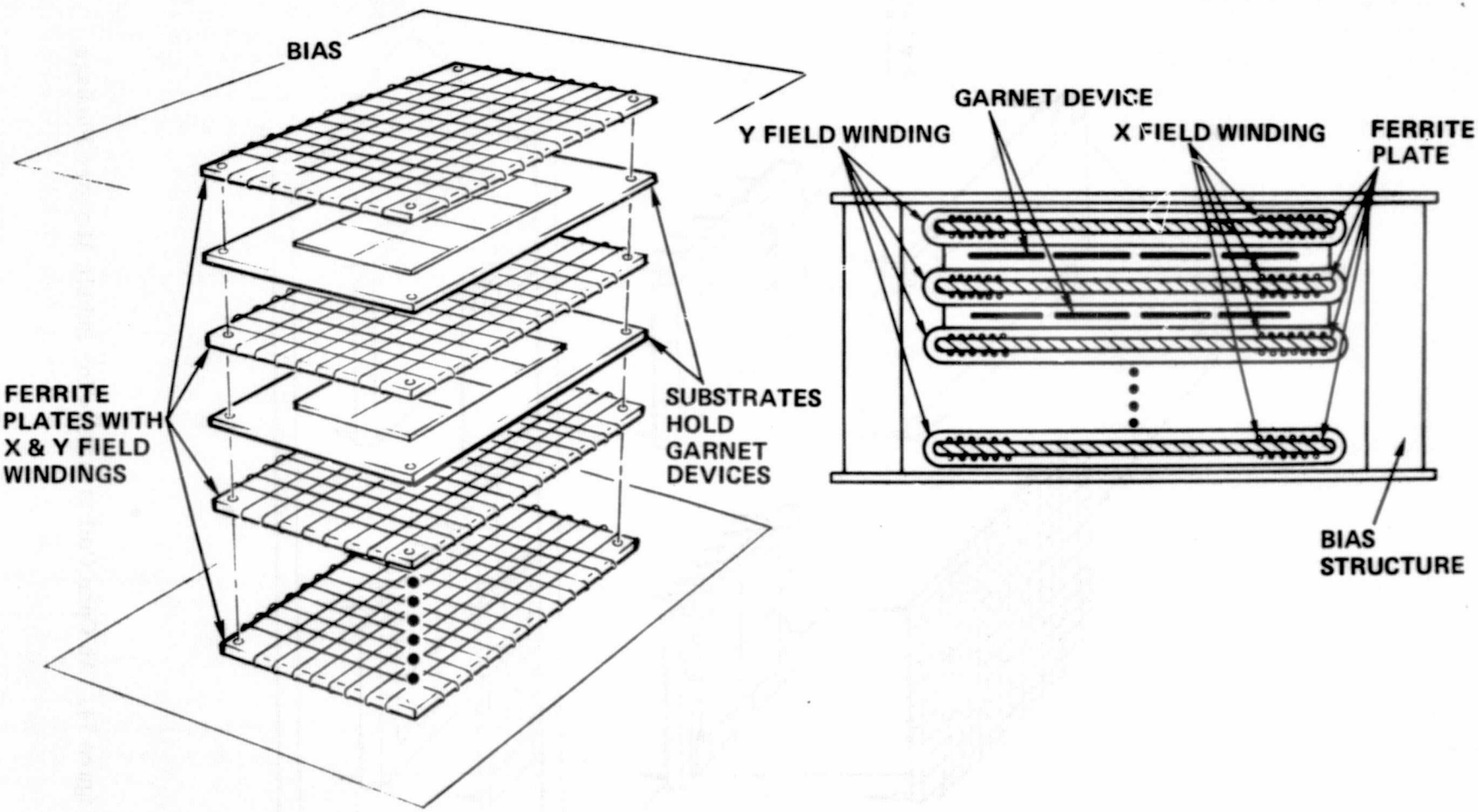


Figure 73. Ferrite Core Coil Stack

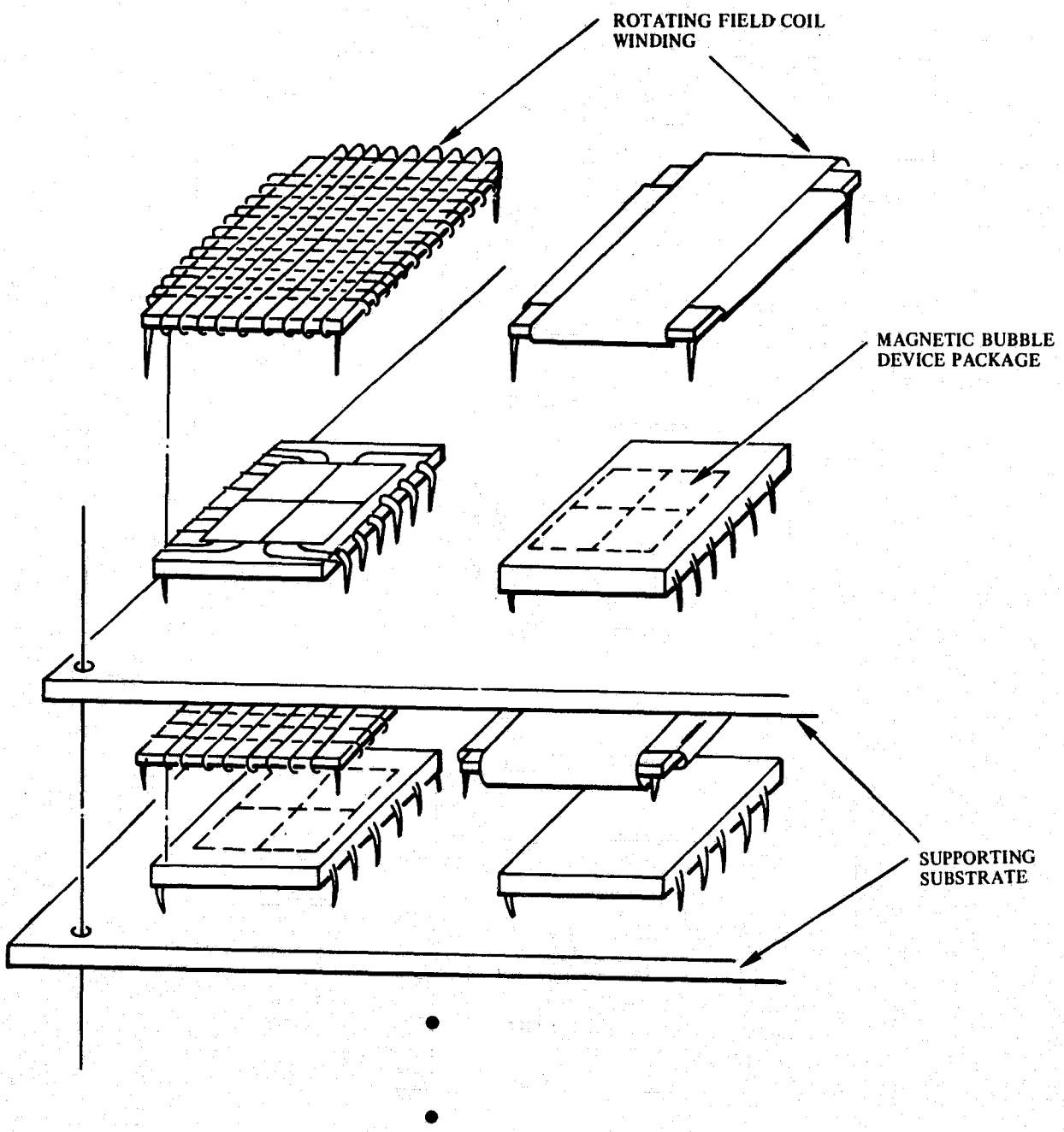


Figure 74. An Open Coil Structure for Bubble Memory Package

6. BIAS STRUCTURE DESIGN

The permanent magnet bias structure is essential for bubble memory recorder nonvolatility. This structure has to be able to supply a uniform field that matches the bias requirement of the memory device over the whole operating temperature range, and must be magnetically shielded to protect the memory device either from external field interference or from polluting the other instruments placed close to the recorder. In addition, this structure has to be light in weight, small in size and stable in the space environment.

The best configuration for providing a uniform magnetic field over a large area is permanent magnets placed between two parallel plates with high permeability, or a Watson magnet structure. (Ref 13) To accomplish the magnetic shield, one of the plates can be extended and turned around to enclose the other plate thus forming a close structure as shown in Figure 75. This structure is used as a basis in the following discussion.

6.1 Simple Analysis

Assuming the magnetic field in both the air gap and magnet itself are uniformly distributed and the bias plates have very small reluctance and are thus close to an equipotential surface, the following simple relationships can be established between magnetic field in the air gap and inside the magnet:

$$H_m \ell_m = f H_g \ell_g \tag{11}$$

and

$$B_m A_m = F B_g A_g \tag{12}$$

where H_m, B_m, ℓ_m, A_m, and H_g, B_g, ℓ_g, A_g are the field intensity, flux density, length and area of the magnet and air gap respecitvely. The factor f accounts for the relative mmf drop in the magnetic circuit other than the air gap of interest. In the present case where a large air gap region is present in the structure, f is close to unity. The other factor F represent the leakage factor in the system. Its value can be calculated by estimating the permeance of all the possible magnetic flux path in the system. (Ref 14)

The load line for the permanent magnet then is given by

$$B_m/H_m = \mu_o F/f A_g \ell_m/A_m \ell_g \tag{13}$$

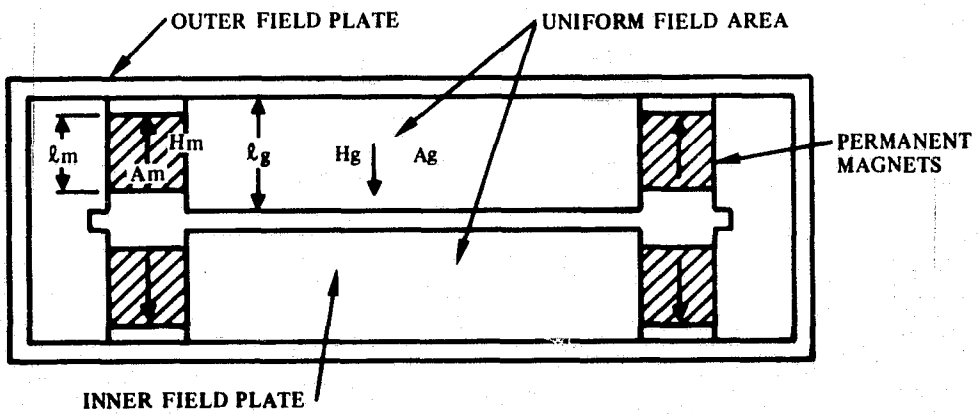


Figure 75. Parallel Plate Bias Structure

The operating point of the magnet is determined by the simultaneous solution of this equation and the demagnetization curve of the magnet as shown in Figure 76. The magnet is operated most efficiently if this operating point is located at the maximum energy $((B_m H_m)max)$ area.

In a structure where several identical magnets are used, the magnet system can be treated as a single magnet with an equivalent magnet area equal to the sum of individual area. If these magnets are different, then each magnet has to be treated separately. The effect of coupling between magnets can be represented by shifting the load line to the left by an amount equal to the resulting field from other magnets (Figure 76). The total flux in the air gap is the sum of the flux from each magnet.

6.2 Field Adjusting

Since the above calculation can only give a rough estimation for the expected magnetic field and also the commercial graded magnets do not have good reproducibility, a field adjustment mechanism must be employed in the bias structure. A coarse adjustment of the field can be accomplished by inserting soft magnetic shunt. A shunt with cross section area A_s and saturation flux density B_s inserted between bias plates will subtract additional flux from the magnet and increase the slope of the load line. Equation (12) is modified to

$$A_m B_m = A_s B_s + F A_g B_g \qquad (14)$$

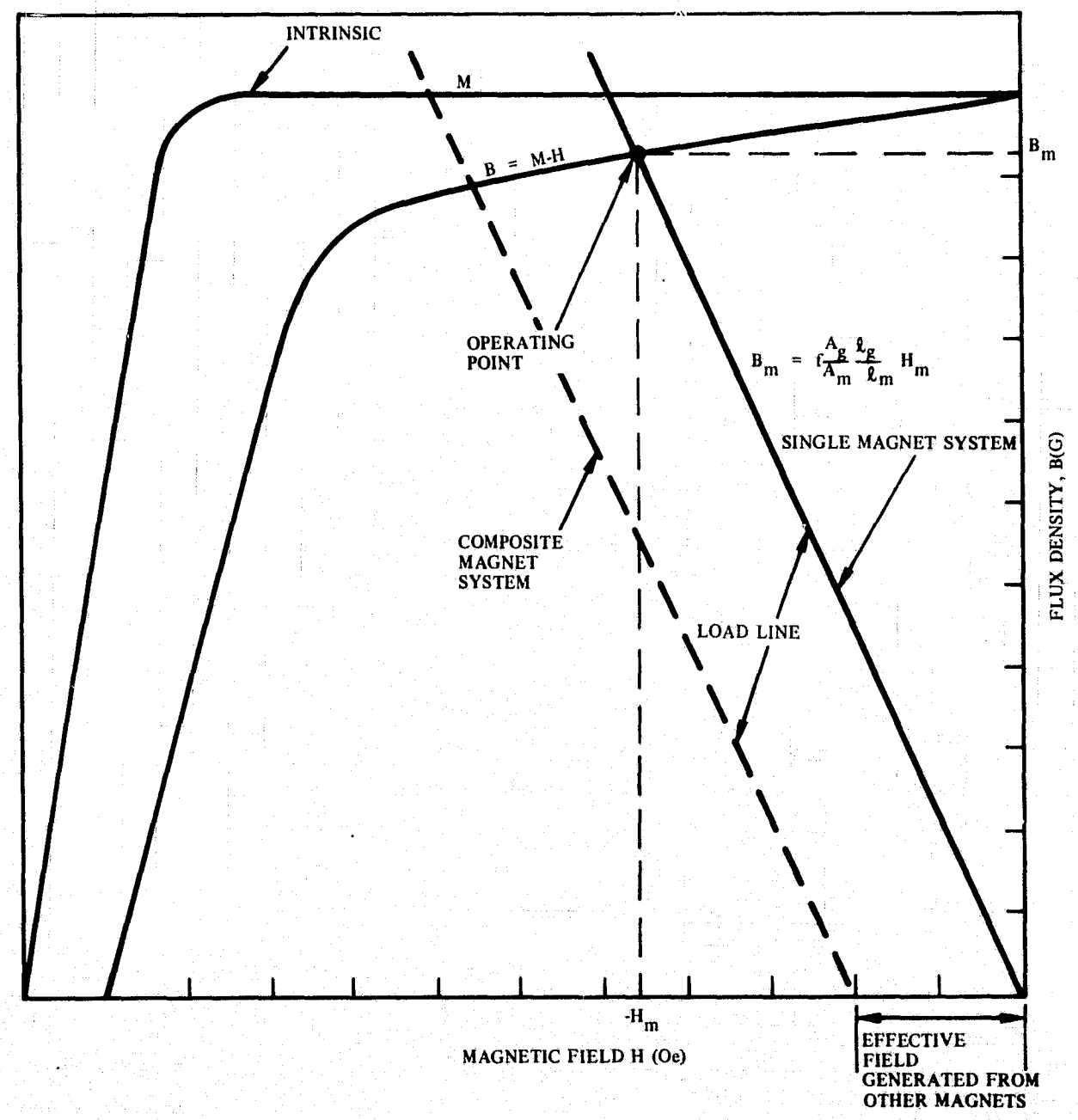


Figure 76. Typical Permanent Magnet Demagnetization Curve and the Load Line of the Structure

and

$$B_m/H_m = \frac{A_s \ \ell_m \ B_s}{A_m \ \ell_g \ H_g} + F\frac{A_g \ \ell_m \ B_g}{A_m \ \ell_g \ H_g} \qquad (15)$$

Therefore the operating point of the magnet shift upward.

If the magnet is operated in a linear minor loop region, the change in magnetic field is directly proportional to the change in the shunted flux.

$$\Delta H \simeq \frac{1}{F}\frac{\ell_m}{\ell_g}\Delta H_m$$

$$= \frac{1}{F}\frac{\ell_m \ \ell_s}{\ell_g \ \ell_g} B_s \qquad (16)$$

The effect of the shunt then is directly proportional to its cross sectional area and flux density.

For fine tuning of the bias field, a continuous field adjustment structure is used. Figure 77 shows two possible arrangements that can be employed. One is a rotatable shaft with a bar magnet inserted at center (Ref 15). The amount of flux coupled to the air gap can be controlled by rotating the angle of the shaft. An alternative approach is to replace the magnet by a soft magnetic bar that acts as a shunt. In this case, the field can only be adjusted in one direction (i. e. lowering the field). A simpler arrangement is shown in Figure 77(b) where a soft magnetic screw is used as a shunt. The gap distance can be adjusted by lowering (or raising) the screw which changes the permeance of the flux path and reduces (or increases) the bias field. In both arrangements the field variation is not linear with respect of the rotating angle of the shaft or the travel distance of the screw.

6.3 Field Uniformity

Under the assumption of the infinitive permeability of the bias plates, the magnetic field inside the bias structure is a function of the gap length such that

$$H_g(x)\,\ell_g(x) = \text{constant.} \qquad (17)$$

where $H_g(x)$ and $\ell_g(x)$ are the magnetic field and gap length at position x respectively.

It is obvious that in order to hold a uniform field distribution inside a bias structure, the tolerance in the gap variation has to be better than the allowable variation in the field distribution.

In reality, the permeability of the bias plate is not infinite, so that the plate is not an equal potential surface. Nonuniformity in the field distribution is then introduced due to the magnetic potential drop across the plates. This problem has been

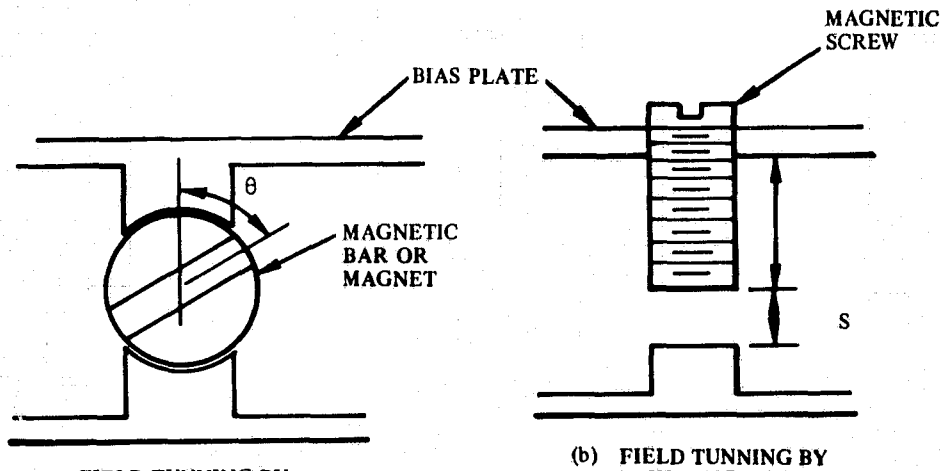


Figure 77. Field Adjusting Arrangements

solved for a highly simplified case (Ref 16) where the plates are assumed to be infinitive in one direction so that the end effect of the bias plate can be ignored. The problem is thus simplified to a one-dimensional problem which can be treated as a distributed magnetic circuit. The field uniformity is found to be a function of a characteristic distance λ which is given by

$$\lambda = \sqrt{\mu_r \ell_g T/2} \tag{18}$$

where μ_r is the relative permeability of the bias plate and T is the plate thickness. The relative field uniformity in the center of the bias plate is a function of λ only. For example, the length of the uniform area around the plate center with field variation less than 1 percent is equal to $\pm 0.14\lambda$. Therefore in a structure where the plate size is large enough to overcome the fringe field effect at the boundary, the uniform field area is a direct function of λ.

Around the boundary, the field intensity drops because of the finite plate size. This effect can be understood from the electric field calculation between two electrically charged conductor plates. For magnetic plates, the magnetic field distribution is actually better than the electric field distribution in the equivalent electrically charged sheets. This is due to the fact that the magnetic flux density near the plate edge is greater than that in the plate center.

In the rod shaped or block shaped permanent magnets, the magnetization distribution is not uniform because the demagnetization field inside the magnet is not constant and also the magnetic particles in magnet are not exactly aligned. Thus, leakage flux exists on the magnet side walls, which cause a nonuniform field distribution in the area close to the magnet. This nonuniform demagnetization effect can be avoided if the magnets are magnetized after they are assembled between the bias plates. However, if the orientation of the magnet components are not uniform, the particle reorientation may occur as the magnet ages. To minimize the effect of this leakage flux a thin soft magnetic shim can be placed around the magnets and act as a shield for the magnet.

The field uniformity inside the bias structure is very difficult to calculate, and it also depends on the quality of the magnetic component used which can not be well controlled. Therefore, magnetic bias design has to be evaluated experimentally.

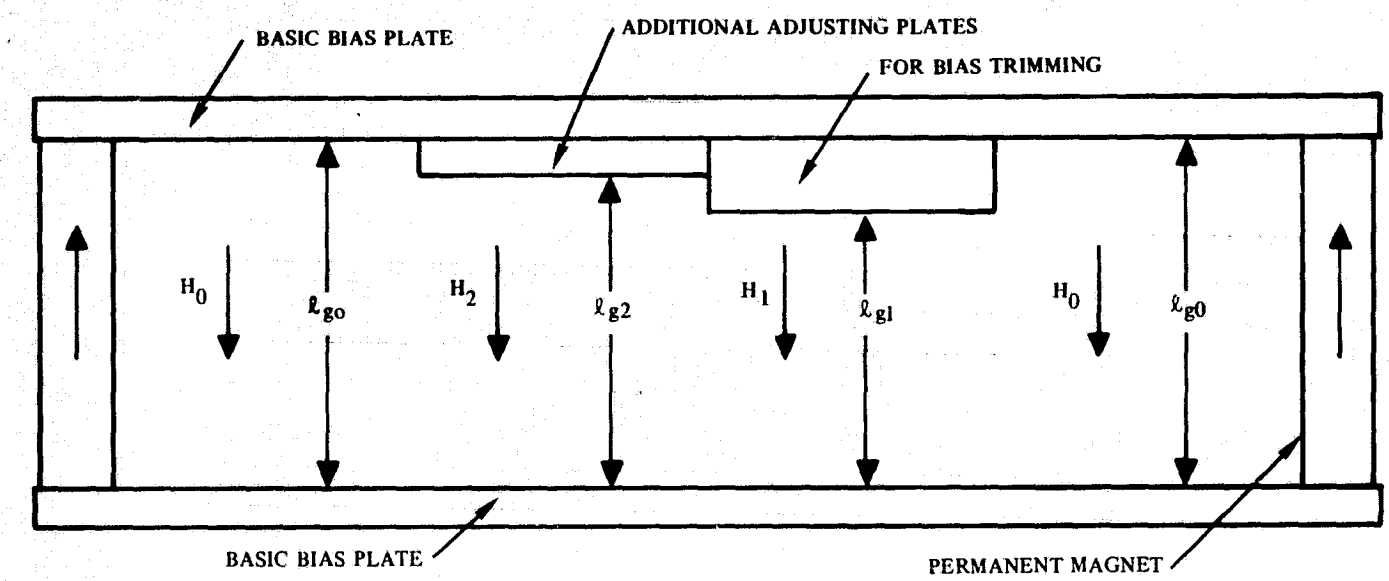
6.4 A Multiple Gap Bias Field Structure

In the bias field design it is desirable to use a single large bias structure to accommodate all the memory chips so that the waste area around the boundaries can be minimized. In the constant gap bias structure design, a single bias structure has two major problems. First, a uniform field is difficult to achieve because of the finite permeability of the bias plates. Second, under the present material and device processing technology, a large inventory of chips is required to provide the matched chips necessary for a single gap structure. An alternative approach to counter the problems is to design a bias structure with different local bias field values which can match several groups of devices with different bias requirements.

Figure 78 shows a design concept for this multiple gap bias field structure. A staircase type bias plate is used instead of a flat plate. If the reluctance of the bias plate can be ignored, the field distribution inside the structure is inversely proportional to the local gap length. These air gap steps can be achieved by epoxing small soft magnetic plates (e.g. ferrite or mu metal plates) to the base plate according to the bias requirement of the bubble chips grouped in the magnet structure. In this type arrangement, the uniform field area can be limited to several small areas, thus the nonuniformity caused by the finite permeability of the plates is not as serious as in the case of a single bias value structure.

Figure 79 shows some field mapping of a magnet structure with stepped air gaps. Introducing steps in the bias plate does disturb the field uniformity near the step boundary, but it smooths out away from the step. In the present example, with a gap distance of 0.250 in. and step height of 0.030 in. the transition length is about 0.2 in. The bias field variation between memory devices is expected to be not more than a few oersteds, so that a smaller step height can be used to reduce the non-uniform transition region.

This bias plate step only changes the relative field value inside the structure. The bias adjusting technique discussed for parallel plate structure can also be applied to this structure. The local bias distribution will be changed proportionally.



$$H_0 \ell_{g0} = H_1 \ell_{g1} = H_2 \ell_{g2} \cdots$$

$$H_0 = H_{g1} : H_{g2} : \cdots = \frac{1}{\ell_{g0}} = \frac{1}{\ell_{g1}} : \frac{1}{\ell_{g2}} \cdots$$

$$\Delta H_1/H_0 = (H_1 - H_0)/H_0 = (\ell_{g0} - \ell_{g1})/\ell_{g1} = \Delta\ell_1/\ell_{g1}$$

Figure 78. A Multiple Gap Bias Structure for Magnetic Module with Different Biased Memory Chips

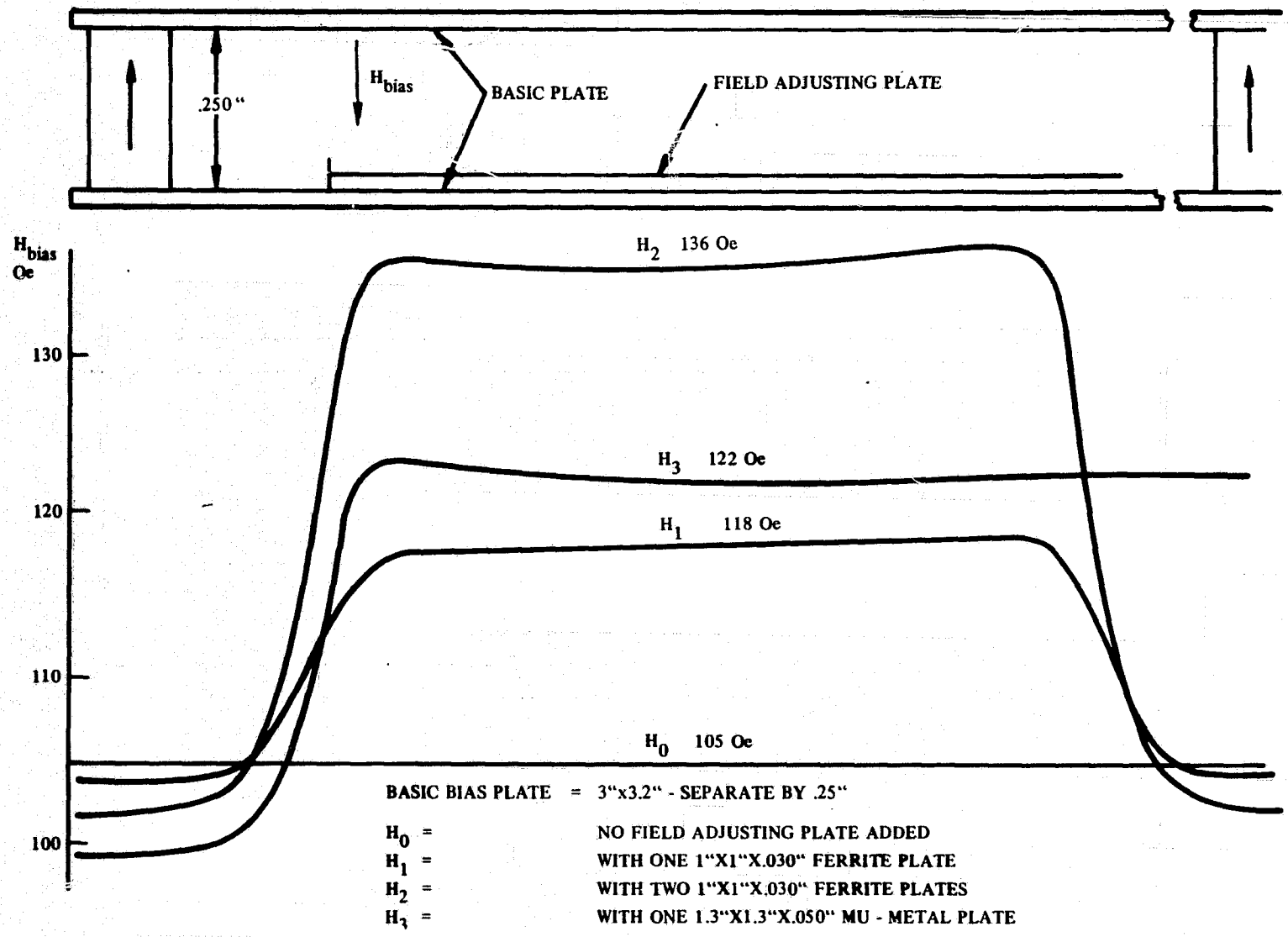


Figure 79. Field Mapping Between Two Parallel Plates with Additional Field Adjusting Plates Added

6.5 Temperature Compensation

To operate the memory device over a specified temperature range, the temperature coefficient of the bias structure has to be matched to that of the memory device such that the bias value always falls in the device bias margin. In a magnetic structure with field adjusting shunt, the magnetic field in the field gap can be derived from Eq (14).

$$H_g = \frac{1}{F A_g \mu_o} (A_m B_m - A_s B_s) \tag{19}$$

The temperature variation in both magnet and shunt will all affect the bias field in the gap such that

$$\Delta H_g / H_g = \left(\frac{1}{1 - \frac{A_s B_s}{A_m B_m}} \right) \frac{\Delta B_m}{B_m} - \left(\frac{1}{\frac{A_m B_m}{A_s B_s} - 1} \right) \frac{\Delta B_s}{B_s} \tag{20}$$

The temperature coefficient of H_g then can be adjusted by properly choosing the temperature coefficient of the magnet $(\Delta B_m / B_m)$ or shunt $(\Delta B_s / B_s)$.

Usually all magnet and shunt materials have negative temperature coefficients. To match a garnet material with positive temperature coefficient a large temperature sensitive shunt (such as Carpenter 32) has to be used. For a negative coefficient garnet, the temperature tracking can be achieved by properly selected magnets.

The choice of temperature coefficient is restricted by the available magnet material. To achieve a wider variation in the bias temperature coefficient, a composite magnet structure technique can be used. In this structure, the bias field is supplied by several types of magnets with different temperature coefficients. The temperature coefficient of the structure then is the averaged value of each individual components. For example, if Alnico 5 ($\Delta Br/Br\,\Delta T \sim -0.013\%/C^o$) and ferrite ($\Delta Br/Br\,\Delta T \sim -0.2\%/C^o$) magnets are used in a composite structure, a bias field temperature coefficient ranging from -0.013 percent to -0.2 percent per degree can be achieved by properly adjusting the flux contribution from each magnet component.

Considerations on bubble material temperature characteristics and the details on temperature compensation techniques have been investigated in a separate program. (Ref 1)

6.6 Shielding and Leakage

In the space craft application, the magnetic bubble recorder has to be closely packed with a number of other instruments. Thus, it is important that the magnetic fields generated in the recorder be confined in the structure so as not to cause any

interference with other instrumentation. Two types of magnetic field sources have to be considered, the d-c permanent magnet bias field and the a-c rotating field.

The bias structure design shown in Figure 75 is a self enclosed structure covered with magnetic plates. These plates not only act as a pole face for the bias field but also serve as a magnetic shield. Assuming these plates are tightly joined, the leakage field from this structure can be estimated by the following formula (Ref 17)

$$H_o/H_s = 0.22\,\mu\,[1 - (1 - t/r_o)^3] \qquad (21)$$

H_o is the Magnetic field in the absence of shield and H_s is that with the shield. μ and t are the initial permeability and the thickness of the shield (in the present case, the bias plate). r_o is the radius of sphere enclosing the same volume as the outer surface of the structure.

For a 0.1 in. thick plate and a structure with a volume of 70 in.^{3} (2 x 5 x 7 in.) the shielding efficiency was calculated from the above equation is $0.025\,\mu$. The field inside the structure is on the order of 100 Oe. If the bias plate has a permeability of 10,000, the leakage field will be in the order of 0.5 Oe. The above values are estimated under the ideal condition. In reality, there are openings in the bias structure for device board connection, pin holes for field adjustment and air gaps between cover plates which will further increase the leakage field.

The effect of a small opening in the structure can be estimated by replacing this hole with an equivalent sized magnetic dipole, and calculating the field from this dipole. The magnitude of the dipole moment can approximate by the product of the field in the hole and the volume of the hole. The leakage field calculated from this dipole is inversely proportional to the third power of the distance from the dipole.

Increasing the bias plate thickness is not very effective in improving the shielding effect according to Eq (21), also it is not practical in a flight recorder application because of its size and weight limitations. Thus, a multiple layer magnetic shielding technique has to be used which is a common practice in the magnetic industry. (Ref 17)

The analysis of a-c rotating field leakage can be treated in the same manner as the d-c leakage. In addition as the rotating field is a high frequency field the eddy currents induced in the bias plates can further inhibit the field from penetrating. A copper shield in conjunction with the magnetic shield could appreciably increase the effectiveness of the a-c shielding.

6.7 Conclusion

Because of the distributed nature of the magnetic flux path and the nonlinear behavior of the magnetic components the magnetic properties of a bias structure are very difficult to estimate accurately. The actual structure design depends on experimental field mapping data.

To optimize the bias structure, the following techniques can be used:

1. Use a thin and long permanent magnet structure so that the magnetic flux is evenly distributed in the bias structure with minimum flux density variation, and also minimize the nonuniform field area due to end effect.

2. The magnets should be magnetized within the bias structure and shielded with magnetic shims to minimize the field nonuniformity near the magnet region.

3. Use thick, flat and properly annealed bias plates placed parallel to each other so that the field variation in between the plates can be kept minimum.

Besides, the operating point of the magnet has to be close to the maximum energy region to achieve a maximum efficiency of the magnet. After the magnet structure is assembled it should go through a temperature treatment to stabilize the magnet. All these techniques are well established in the magnet industry which can be directly applied in the magnetic module design for bubble recorder.

7. TOLERANCE IN MAGNETIC FIELD NETWORK

In a large capacity bubble recorder, a numer of device packages, coil assemblies and bias structures will be used. It is obvious that all these structures cannot be made exactly identical and as a result variations in the field network characteristics are inevitable. This section will discuss the effects of these variations on the bubble memory device operations based on a study using the present chip design.

7.1 In-Plane Rotating Field Variation

As discussed in Section 5, the inplane field network, the nonuniformity in the in-plane rotating field coil includes variation in the in-plane field magnitude, angular skew in the distribution, or field components perpendicular to the device plane. In the assembly of the in-plane field network, additional variation may be introduced such as the nonorthogonality between x and y coils, the misalignment between the device plane and the coil plane or the misalignment between device orientation and the coil axis. When the coil is connected to the driver circuit, mismatching of the resonance capacitor, instability in the coil driver may also induce further distortion. All these variations can be summarized in the following categories. Variation in the magnitude of the field, fluctuation in the rotating field angular velocity, the deviation between the rotating field phasing and the device orientation, the existence of field components perpendicular to the device plane and the distortion of the in-plane field coil driver turn off waveform. When these variations are small, their effect on the device operation can be discussed separately.

Field magnitude variation. - Field magnitude fluctuation can be caused by any distortion in the rotating field network; such as the nonuniform field distribution in the coil, nonorthogonality between two drive coils, misalignment between device and coils, instability in the coil driver, or mismatching between the coil and the resonance capacitor. The effect of these variations can be understood from the device operating margin plot. Figure 80 shows a typical device operating margin plot. For prictical device operation under the consideration of minimum coil power dissipation, the driving field value is usually chosen at a minimum value such that the device has a reasonable bias margin and reliability. If any fluctuations in the driving field magnitude occur, the device driving field must be increased to ensure the entire device area is always exposed to a rotating field greater than that minimum value. This type of variation usually will not effect the bias margin but, will increase the power consumption in the coil set.

Angular velocity fluctuation. - An angular skew in the field distribution or the nonorthogonality between x and y coils or a phase variation between the x and y coil driver currents all result in field magnitude variation and fluctuations in the rotating field angular velocity. When the deviation is small, its effect can be represented by a change in the average velocity.

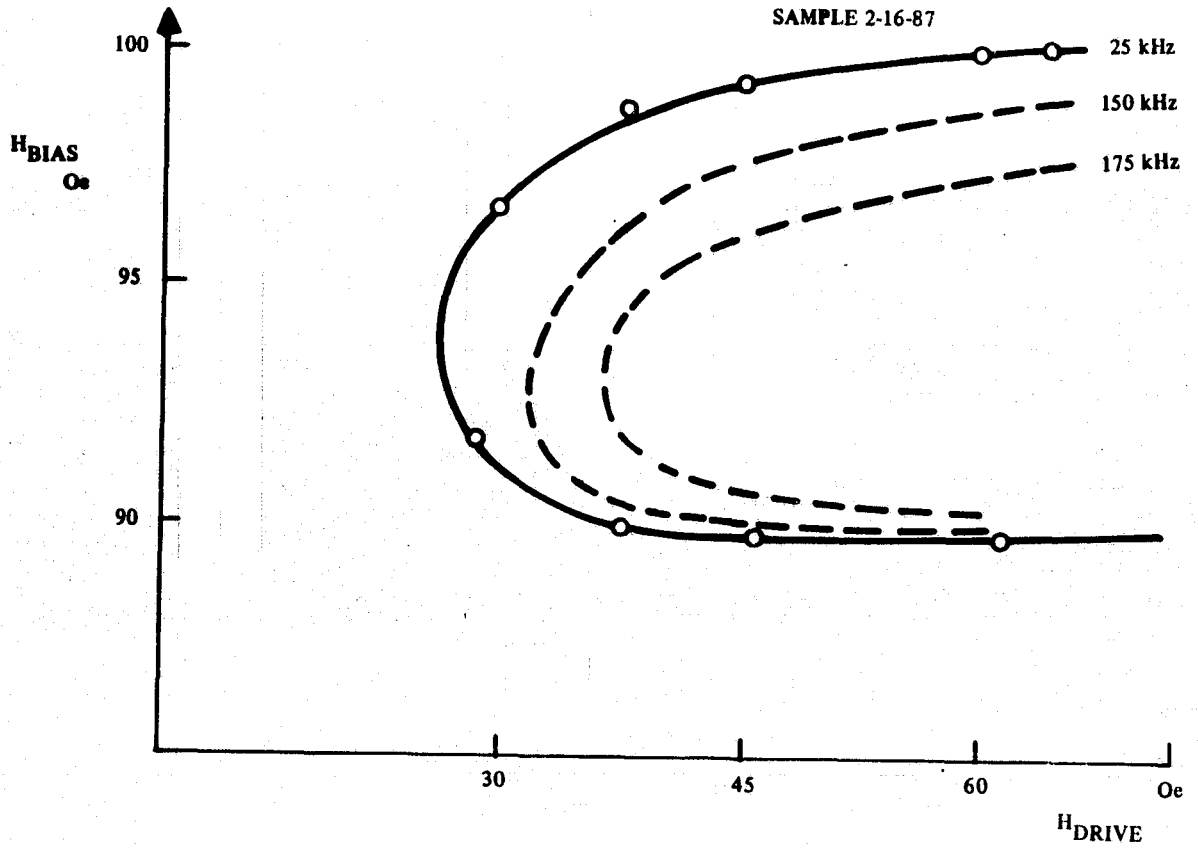
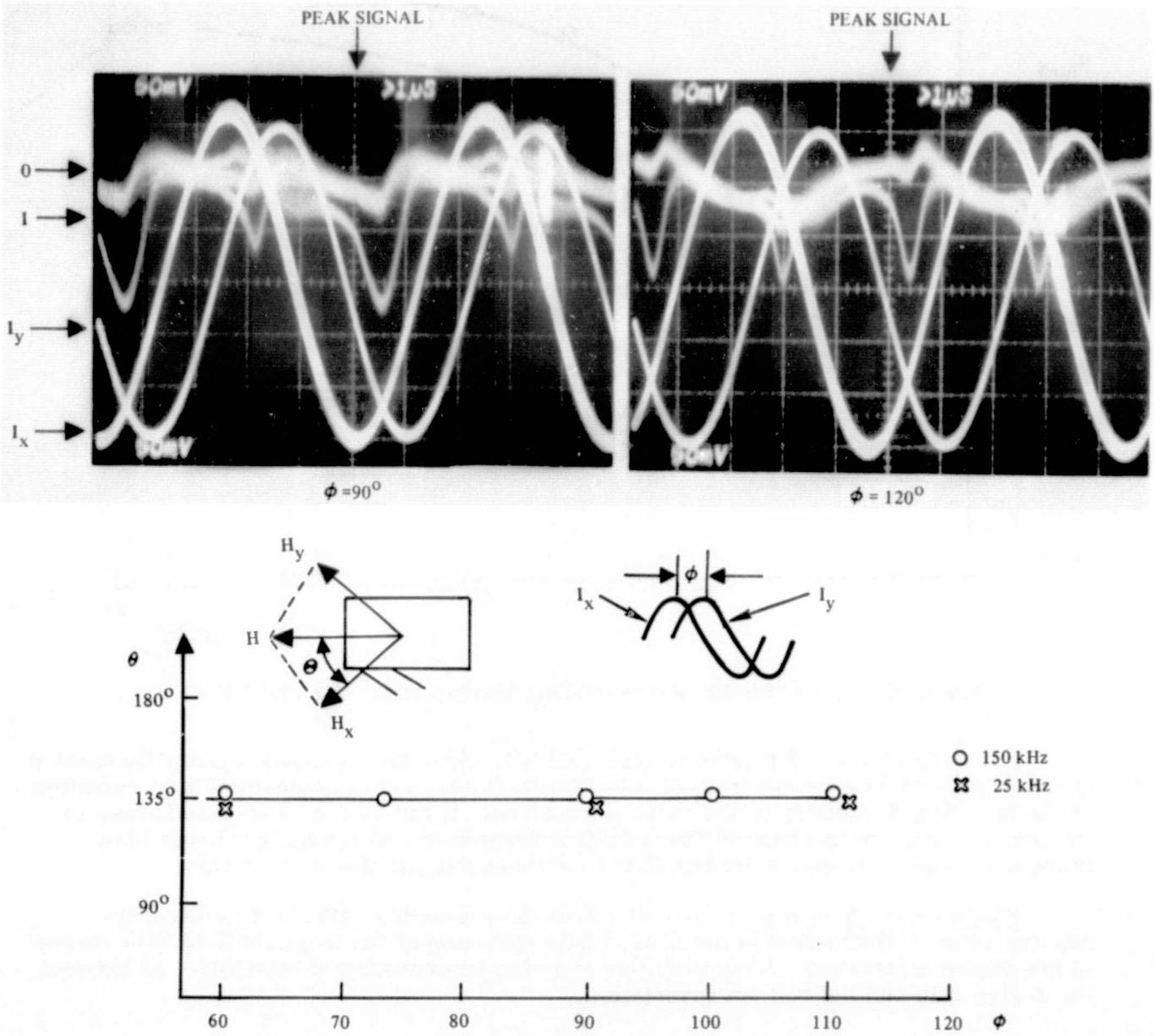


Figure 80. A 10k Bit Device Operating Margin at 25 kHz and 150 kHz

For example, a δ deg skew in each coil will cause an averaged velocity fluctuation of $\pm 4\delta/\pi$ percent in each quadrant of the rotating field. This is equivalent to a variation of the operating frequency by the same percentage. If the device is operated close to its velocity limit an increase in the operating frequency will result in a lower bias margin or require a higher driving field to compensate for this distortion.

Phase angle variation. - Another effect in conjunction with the rotating field angular velocity fluctuation is the phase angle variation of the in-plane field with respect to the device orientation. This variation can also be caused by a misalignment between the device chip and the coil set orientation.

Under the continuous operation, the bubble position only depends on the orientation of the in-plane magnetic field. Therefore, a small phase distortion in the rotating field will not affect the device operation margin but will change the phasing on the control functions such as generation, annihilation and detection. The fixed relation between the bubble position and the in-plane field can be proved by measuring the detector signal phasing at different rotating field phase angle. The data are shown in Figure 81 where no significant variation has been found for device operated either at 25 kHz or 150 kHz.



θ = ORIENTATION OF THE IN-PLANE FIELD WITH RESPECT TO THE DEVICE ORIENTATION

ϕ = PHASE ANGLE DIFFERENCE BETWEEN X COIL AND CURRENT AND Y COIL CURRENT

Figure 81. Effect of Rotating Field Phase Distortion on the Detector Output Signal

The effect of the driving field phase angle variation on the device control phasing can be directly extrapolated from their phasing margins. For the present loop generator and annihilator designs, their phase margins are quite wide (close to 180 deg) so that they will not be affected by the phase distortion unless they are positioned very close to the margin limit. The detector strobe phasing on the other hand, is quite narrow such that variations in the driving field phase will result in a higher soft error rate. The tolerance in the phase shift primarily depends on the width of the detector signal.

When the field is turned off the bubble resting positions depend on the in-plane field turn off angle. If the angular variation is too big, the bubble resting position may shift from a favorable position (having a deeper potential well) to a less favorable position (having a shallower potential well). This shift can cause reduction in the gated operation margin. In a properly designed pattern the safety shut off angle is quite wide (can be greater than ±45 deg). Thus this angular variation effect should not be a concern.

Vertical field components. - Any vertical field component induced by the in-plane rotating field will modulate the bias field at the same frequency as the operating frequency. The net effect is a reduction in the operating bias margin by an amount equal to the peak to peak amplitude of this fluctuation. However, the actual device is operated in a gated mode with rotating field turned on and off repeatedly. The high bias field end of the margin for the gated operation is usually substantially lower than that of the continuous operation. (The difference for the lower bias field end is generally less.) Depending on the device design and the arrangement of the chip in the field structure (esp the bias field alignment), the device gated margin can be anywhere from zero to approximately the continuous margin value. Because of this difference, the misalignment of the in-plane field will not severly effect the gated margin unless the induced bias fluctuation exceeds the margin difference between gated and continuous modes. If this difference is 2 Oe under 30 Oe during field, the misalignment of the in-plane field could probably be as great as 4 deg before it effects the gated margin.

Distortion in the rotating field turnoff waveform. - When the device is operated in a gated mode, the bias margin further depends on the way the field is turned off. Any overshoot in the shut off of the coil current will reverse the magnetization of the permalloy elements causing the bubbles to drift away from their resting positions or even collapse. In the voltage precharge type driver circuit as discussed in Section 4. Electronic Design Philosophy, this overshoot is mainly contributed by the x coil current. However, a large distortion in y current shut off may alter the rotating field shut off direction and cause data instability. In the present device a 2 or 3 Oe in-plane field is sufficient to cause bubble shifting away from its resting position. For a 40 Oe driving field, the turnoff overshoot has to be controlled less than 10 percent.

7.2 Bias Field Variation

Two posssible problems can be associated with the bias structure: the bias field magnitude variation and the in-plane component of the bias field. The later one can be caused by improper bias structure design or simply due to the misalignment of the device package in the bias structure. When using matched devices the variation of the bias magnitude within the structure should be less then ±1 percent so minimum loss of margins will occur.

The field component in the device plane can be more critical to the device operation. This in-plane component acts as a dc field superimposed on the ac rotating field. Ideally it should only affect the operating margin in the same manner as the non-uniformity in the in-plane field magnitude. However for some component configurations the operating margin may be sensitive to this dc component. An example is shown in Figure 82 where a 10k bit device is operated continuously at 25 kHz. The operating margin shows a cut away portion where the device will not work at high driving field end. When the device is observed at a visual speed, it is found that the cut away portion is due to the T-bar to chevron transition region where bubbles collapse at the end of the diagonal bar.

When operated under gated mode, this dc field component will also effect the turn-off of the rotating field. If the dc field is directly opposite to the field turn-off direction the net effect will be the same as the case where there is an overshoot in the rotating field turn-off current waveforms. If the dc field is in the other direction, then it acts as a holding field which will greatly stabilize the bubble propagation. This effect is illustrated in Figure 83 where the device bias margin under fixed rotating field is plotted as a function of the bias tilting with respect to the device. The amount of reverse tilt can be tolerated by the device depends on the device design and its processing parameters.

By using a proper tilt in the bias field, the effect of rotating overshoot can be compensated. An example is also shown in Figure 83. The dc component in a direction perpendicular to the rotating field turn off direction is not very critical to the device operation. In the cases when the turnoff direction is so chosen that the bubble is not resting on a favorable potential well position, a slight off axis tilt can introduce a d-c field which can move the bubble to a nearby position with stronger coupling between permalloy and bubble (deeper potential well). In this manner, the device gated propagation margin can actually be improved by a properly controlled misorientation in the bias field. Start - stop device operation and the techniques to improve its operation are currently being investigated on another military program. (Ref 18).

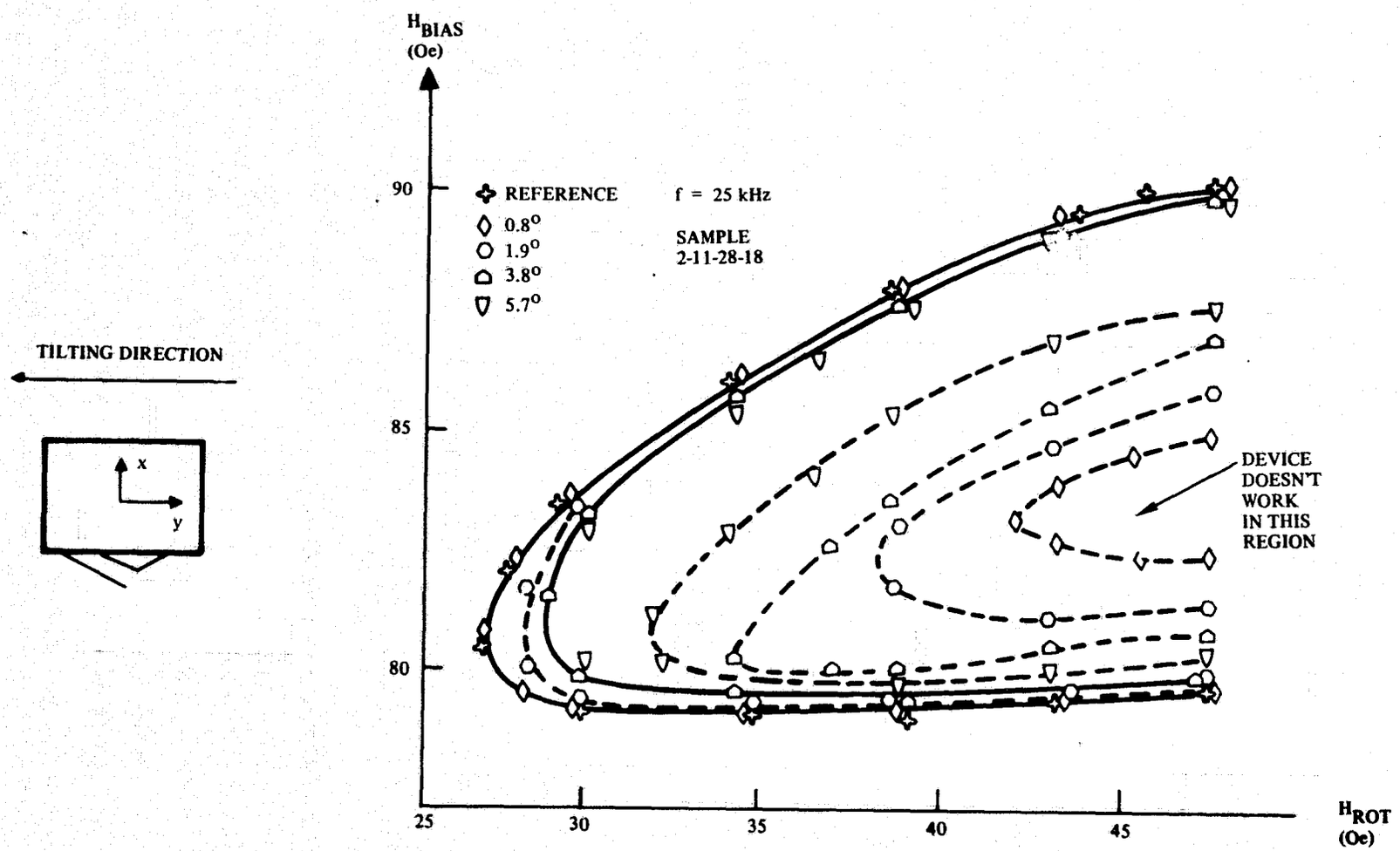
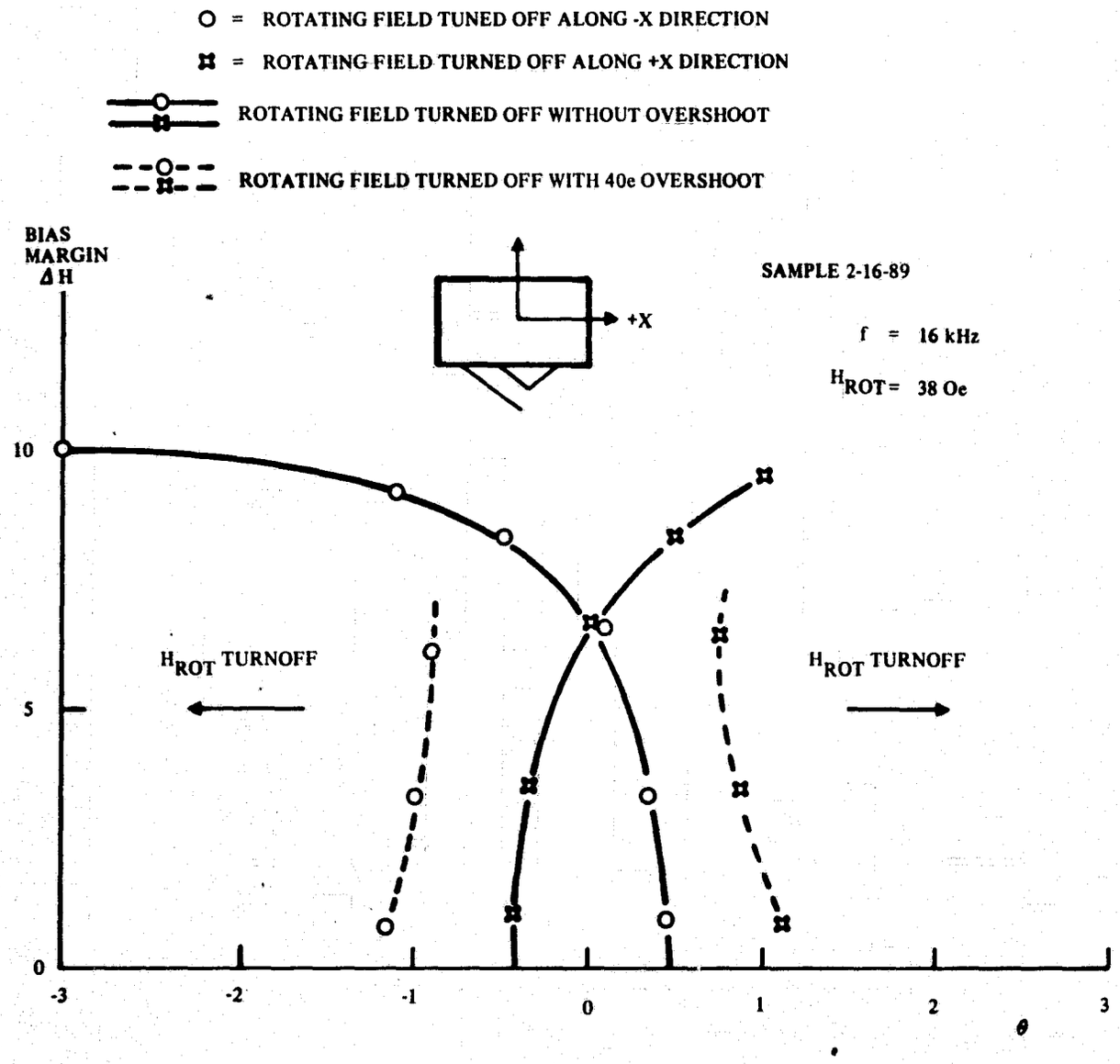


Figure 82. Effect of Bias Tilting on Device Continuous Operating Margin



θ = BIAS FIELD TILT ANGLE

θ = 0 PERFECTLY ALIGNED

θ < 0 BIAS FIELD HAS AN IN PLANE COMPONENT ALONG -X DIRECTION

θ > 0 BIAS FIELD HAS AN IN PLANE COMPONENT ALONG +X DIRECTION

ΔH = DEVICE BIAS MARGIN AT H_{ROT} = 38 Oe

LOWER MARGIN ALMOST CONSTANT = 89 Oe

Figure 83. Effect of Bias Field Tilting on Device Gated Operating Margin

8. ENGINEERING MODEL DESIGN

To demonstrate the feasibility of bubble memory recorder, a 60k bit engineering model has been constructed. The design goals of this model are listed in Table II. As the model design was started in parallel with the other study tasks, many of the results of the study tasks are not implemented in the Engineering Model. Although the recorder operating frequency was specified as 25 kHz maximum, the design goal of the electronic portion of the model was aimed toward the ptototype recorder frequency (150 kHz).

TABLE II.

ENGINEERING MODEL DESIGN GOALS

Number of track	3
Number of chip:	6
Capacity per track:	20,000 bits
Total capacity:	60,000 bits
Density:	10,000 bits/chip
Record speed per track: on chip	2,500 bits/sec
Playback per track: on chip	25,000 bits/sec
Error rate:	10^{-4} error/bit
Operating Power: Standby	0 watts
Record	3 watts
Playback	5 watts
Size:	200 in^3
Temperature ambient	$25^{o}C = 5^{o}C$

8.1 Memory Chip Description

The basic storage chip was designed under an in-house program but modified for the recorder application. As shown in Figure 84 it is a 10240 bit single loop shift register with T-bar storage and chevron composing branch and surrounded by a T-element guard rail (Figure 84 (b), (c)). The overall chip size is approximately 0.1 x 0.2 in. but the active device area excluding the guardrail is about 0.085 x 0.130 in.

The main storage region is composed of T-bar (or more precisely I-bar) propagation elements. The basic period is 24 μm so that the storage density in this area is 1.7×10^9 bit/m^2 or 1.12×10^6 bit/in^2. The line width and the gap width in this pattern are around 3 μm and 2 μm respectively.

A 28 μm period chevron propagation branch is used for bubble generation (write), annihilation (erase), and detection (read) functions. The generator and annihilator circuits are conductor loops located in the gap between chevron columns. (Figure 84 (d)) Passing a current pulse in these loops generates a local field under the loop area. If this field is opposite to the bias field, it can reverse the magnetization in the garnet and nucleate a new bubble. If the field is in the same direction as the bias field then it will collapse any bubble which is located under the loop. These circuit components are fully compatible with the propagation circuit in terms of speed and operating margin.

The detector is a conductor shorted thick film chevron stretcher detector (Ref 19 Figure 84(e)). The chevron column is expanded from three elements to 12 elements to increase the bubble size thus produce more magnetic flux from the bubble. At the longest stretch position the chevron elements in the column are connected in series by conductor films which overlap the ends of chevrons. The magnetic flux from the bubble induces a resistance variation in these permalloy elements (planar magnetoresistance effect) which can be sensed by passing a current through the detector elements and measuring the voltage variation across it. To eliminate the background variation induced by the in-plane rotating field, a reference detector element is placed next to the active one. They then are connected to the amplifier circuit in a bridge configuration employing two additional fixed resistors (1k Ω).

A guard rail surrounds the entire device. It is comprised of T-type propagation elements which are arranged so that propagation is always away from the device area. Thus, spurious bubbles outside the device area (possibly generated by edge defects) cannot cause errors in the stored data by migrating into the device area. (Ref 20).

The devices are fabricated on $YEuTM._{65}GaIG$ bubble material which as a $4\pi M_s$ around 200 gauss, strip width of 6.5 μm, thickness of 6 μm and wall mobility of 330 cm/sec Oe. The device processing procedures are as follows: A 1000 Å thick SiO_2 sputter deposited directly on top of the garnet, followed by an evaporated layer of 5000 Å thick 80-20 AℓCu film. The SiO_2 spacer is used to relieve stress in the garnet material caused by the AℓCu film. The generator and annihilator patterns are chemically etched in the AℓCu film. Another layer of sputtered SiO_2 approximately 1 μm thick is deposited followed by layer of 4000 Å thick sputtered 80-20 NiFe film. The propagation elements are photolithographically defined and etched by ion milling. The purpose of the SiO_2 spacer layer is to properly couple the bubble domain and the

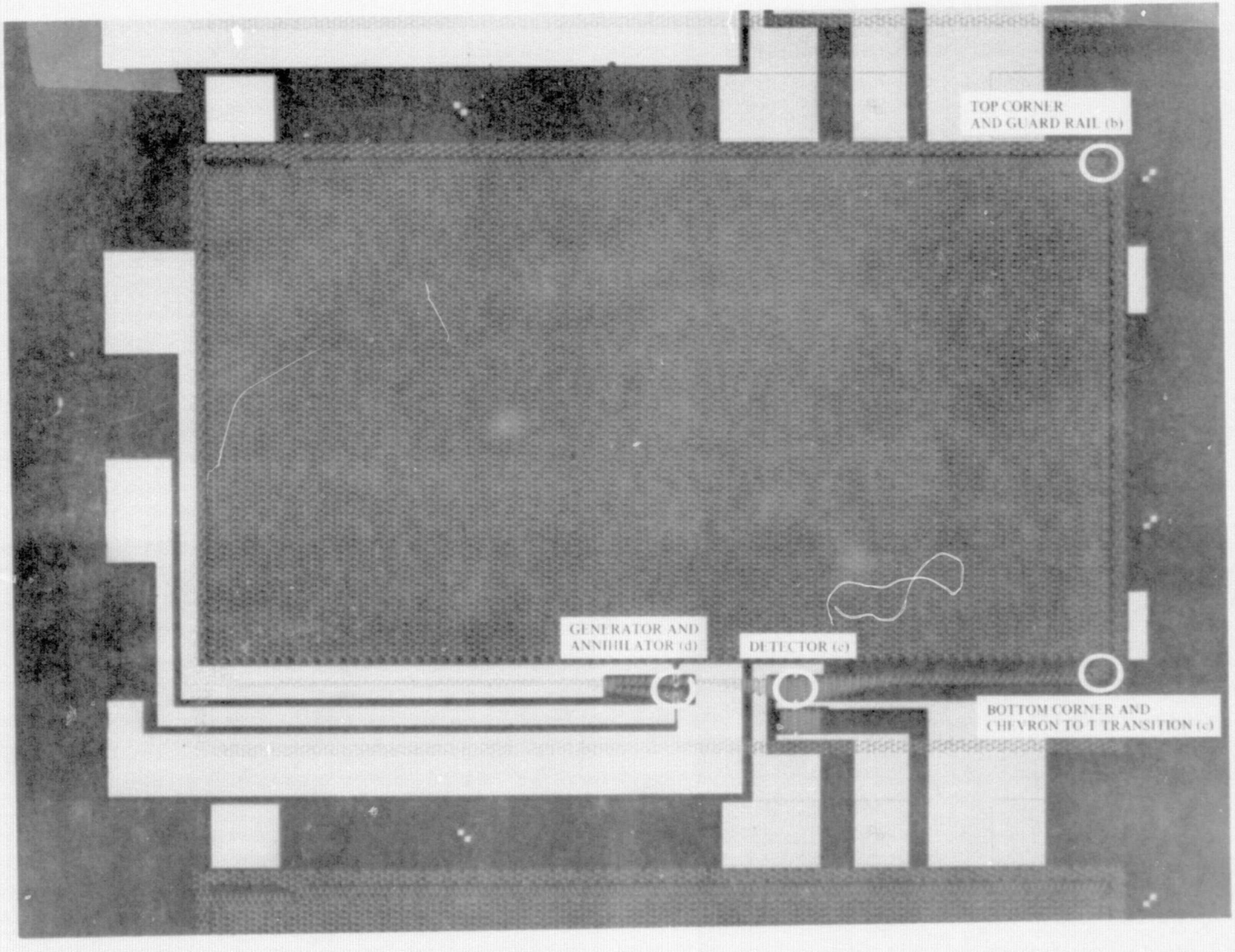
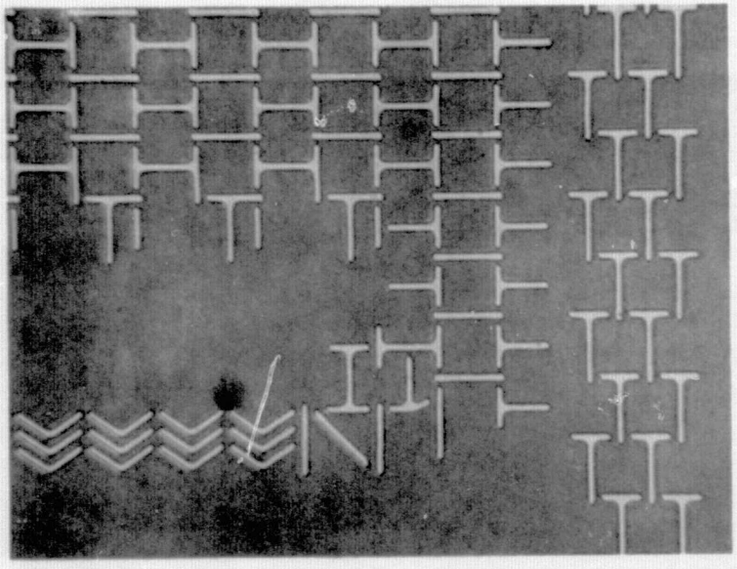
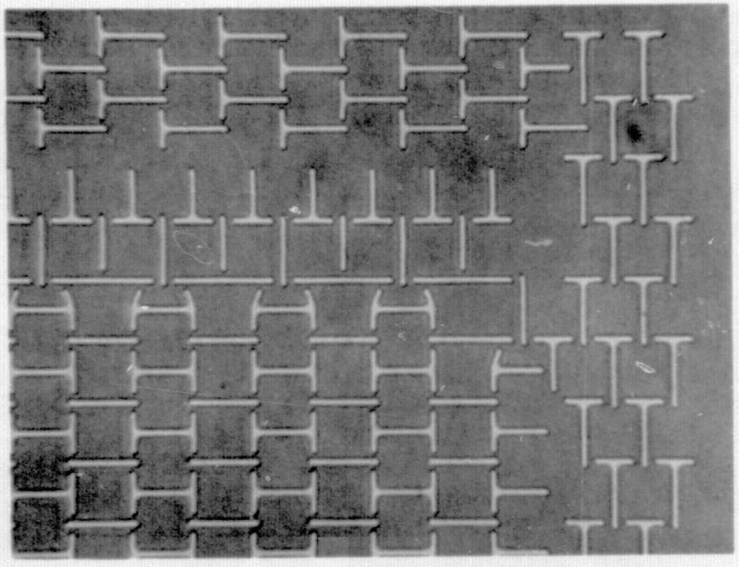


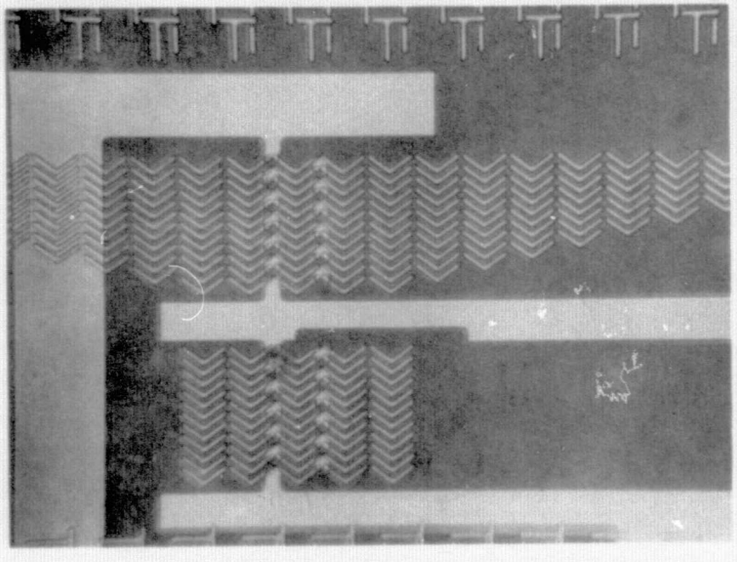
Figure 84. 10240-Bit Bubble Memory Chip



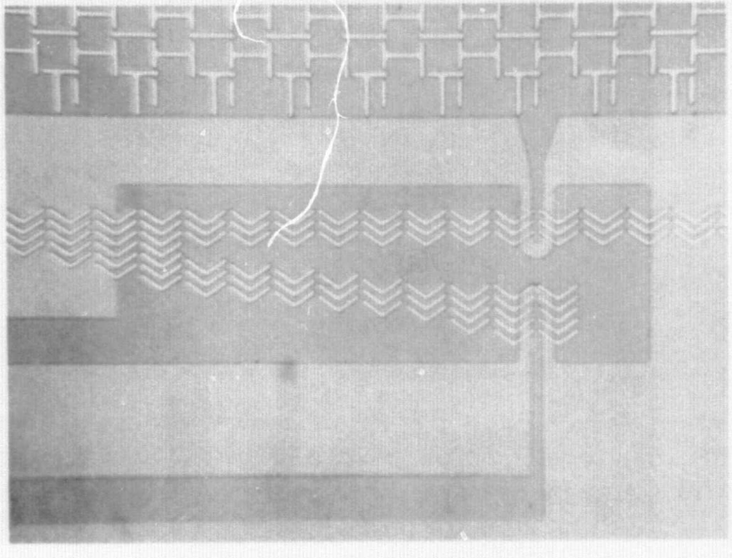
(c) BOTTOM CORNER AND T-BAR CHEVRON TRANSITION



(b) TOP CORNER AND GUARD RAIL



(e) DETECTOR



(d) GENERATOR AND ANNIHILATOR

Figure 84. (Cont)

permalloy in order to achieve an optimum device operation. A final layer of 5000 Å CrAu film is deposited on top of NiFe pattern to form the connection to the detector elements. The generator and annihilator are placed between the garnet and permalloy pattern to be close to the garnet and to prevent shielding by the permalloy.

A typical device operating margin is shown in Figure 85. Although the original goal was only 25 kHz the device can be operated reliabily at 150 kHz with a 6 to 8 Oe bias margin at 40 Oe rotating field. The generator and annihilator currents are nominally 300 ma - 1 μsec and 150 ma - 1 μsec respectively. The detector output signal waveform is shown in Figure 86. The signal sensitivity is between 100 μv/ma to 150 μv/ma. A detail discussion on the performance on this memory chip will be given in the Section 10 on feasibility model evaluation.

8.2 Device Package

The package used in the feasibility model is shown in Figure 5. It was developed by in-house programs in connection with other bubble memory packaging. It is a three layer buried metalization alumina structure made using an aluminum tape process. There are 20 conductor leads brought out on two "ears." These conductors are gold plating on fired tungsten. In the center area of the package there is a 0.210 x 0.210 in. cavity for two 10k bit bubble devices and two 0.1 x 0.1 in. cavities on both sides of the large cavity for resistor and preamplifier chips used in the detector bridge circuit. An alumina plate (fourth layer) can be placed over the cavity area to seal the package. The total thickness of the package without the cover plate is 0.06 in. The thickness of the cover plate is 0.04 in. Two driving coils can be wound around the package guided by the "ears." The dimension of the winding area is 0.560 x 0.560 in. the overall size of the package including ears is 0.9 x 0.9 in.

The package was originally designed so that two memory chips would be placed back to back, each chip pad section being close to their preamplifier circuit. After testing it was found that by using a proper sensing circuit the induced voltage due to long detector leads was not as serious as first expected. A modification was made so that both chips were aligned in the same direction as shown in Figure 87 with one chip having detector connections flying over the active device area. In this arrangement, both chips have the same timing control for read, write and erase, which greatly simplifies the electronic control circuits.

The bubble memory chips are cemented to the ceramic package. As the chips fit tightly in the cavity the orientation of the chips are determined by the dicing tolerances which can be controlled to within a few degrees. All the interconnections between chips and packages are accomplished by thermal compression bonds using 0.001 in. gold wire. After bonding is completed, the devices are coated with a layer of polyvinyl copolymer for protection. After the cover is sealed on, the package is wrapped with in-plane field coil windings.

The package is mounted in a plastic holder. In an earlier design spring connectors were molded in the plastic holder for contact connection between ceramic package and external leads. Because of improper alignment between the connecting pads in the package and its holder and also an insufficient pressure to break through the oxidation layer on the conductor surfaces, this approach was not successful. Instead, a miniature plug (Cannon NTG1-9ST80) is directly soldered on the package "ear" to ensure a reliable electrical connection as shown in Figure 88.

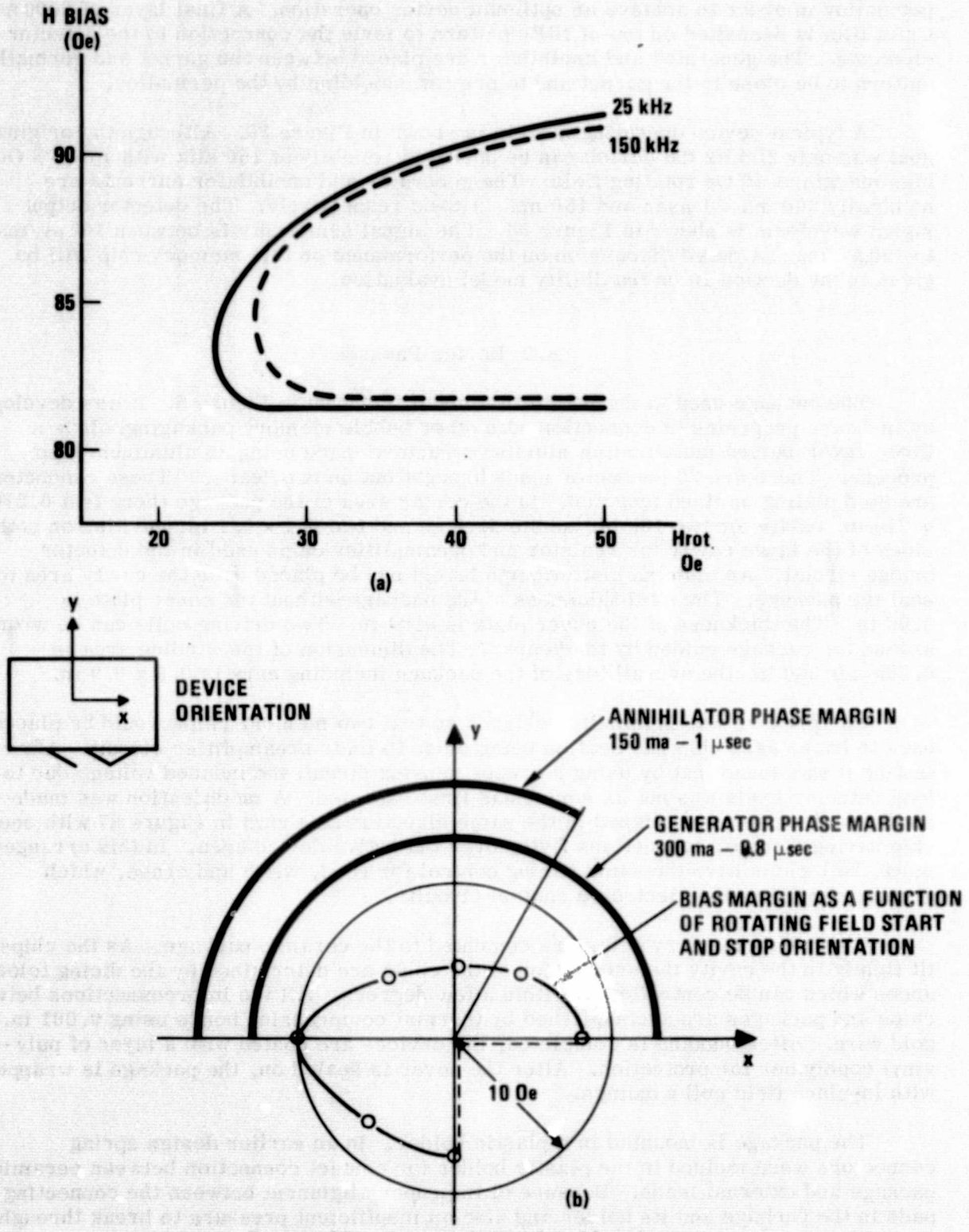
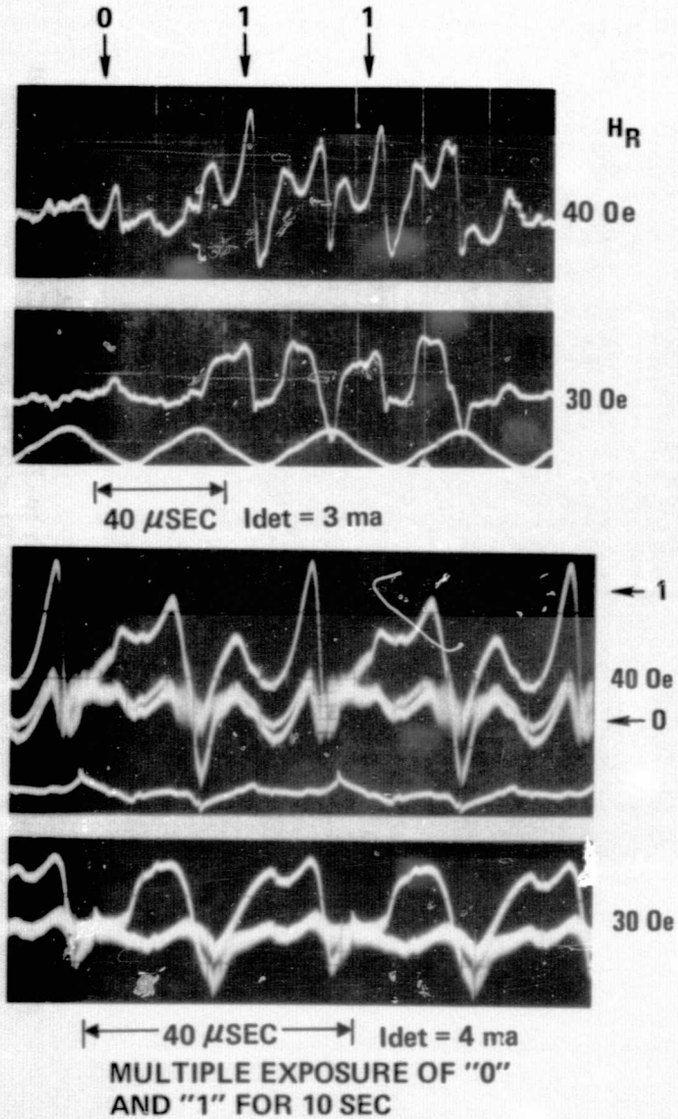


Figure 85. Device Operating Margin



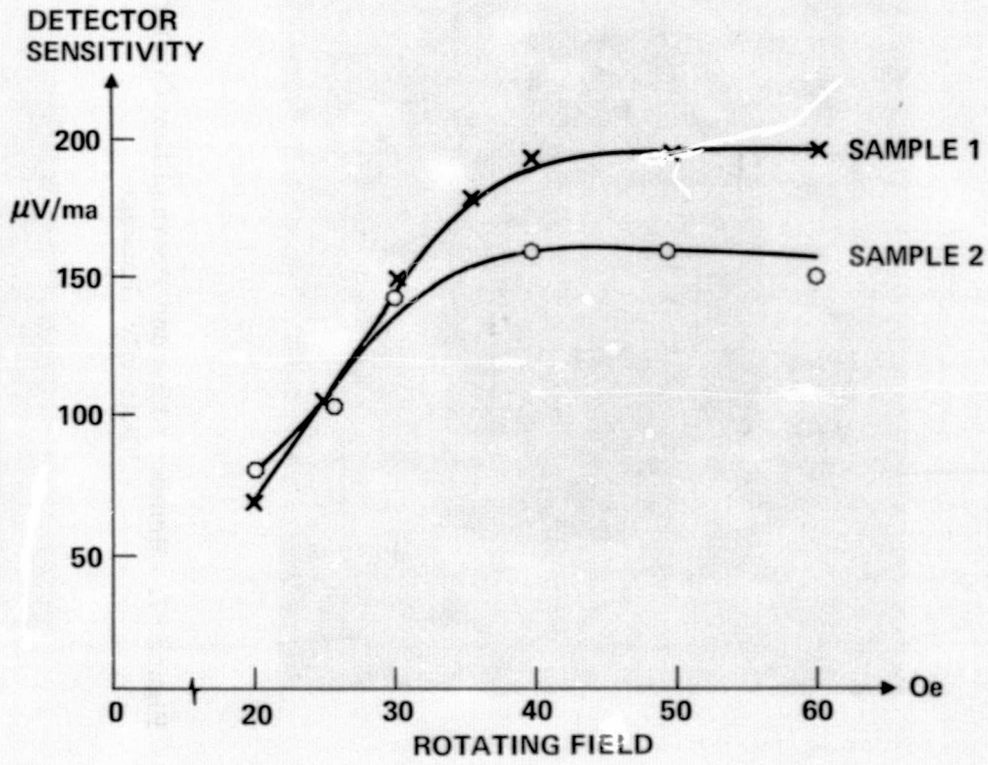


Figure 86. Detector Output

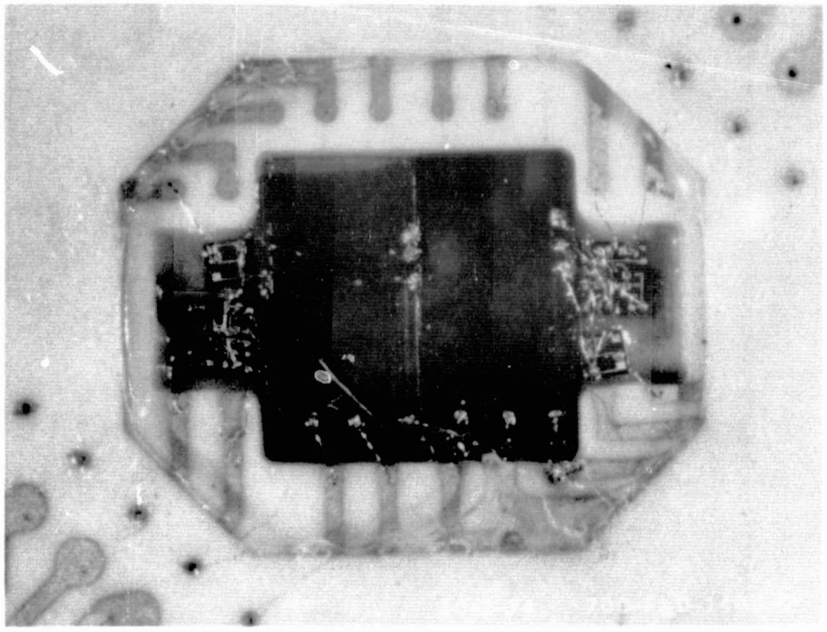


Figure 87. Memory Chips and Preamplifier Circuitries in "Butterfly" Package

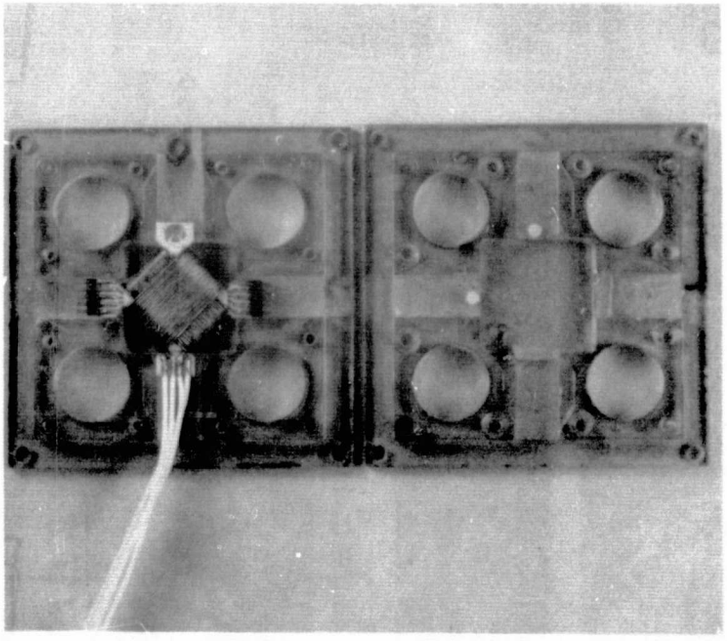


Figure 88. Butterfly Package with In-Plane Field Coil Winding and Connectors in Plastic Holder

When the package is sandwiched in the plastic holder four pieces of rubber padding are placed above or below each ear so that when the plastic holders are clamped together the package level can be adjusted by two plastic screws placed in the top holder directly above two "ears" of the package. In this manner the package plane can be properly oriented in the bias structure as discussed in Section 7.2 Bias Field Variation.

8.3 In-Plane Field Winding

The in-plane rotating field coils are wound directly on the ceramic package as shown in Figure 88. Each coil has two layers of winding interwoven with each other. Each layer has 26 turns of AWG 28 wire and are connected in series. The average dimensions of the coils are 0.36 x 0.60 x 0.14 in. for x and 0.36 x 0.60 x 0.16 in. for y. The calculated field uniformity in the device area is within 10 percent and the angular skew in the field distribution is less than ±5 deg. The peak field efficiency at the coil center is 55 Oe/amp (K = 0.78).

The coil inductance is about 12 μh and the d-c resistance is about 0.46Ω. The a-c loss in the coil as function of frequency is shown in Figure 89. At 150 kHz, using a minimum rotating field of 40 Oe the coil drive current is 0.8 amp which results in a 0.77 w dissipation in the package under continuous operation. This power consumption will cause a temperature rise about 25°C from the room temperature operation. The memory however, is not intended to operate continuously except under test conditions. When operated with full write rate of 10kHz the coil is only turned on for 7 percent duty cycle. Even at 150kHz read rate, the whole package can be read within 0.2 sec. Under this low duty cycle operation condition the heating effect due to the coil winding does not cause serious effect. Thus, no effort was made to lower the a-c loss in the coil.

8.4 Bias Structure and Magnetic Module

The basic design of the bias structure is based on the same concept as discussed in Bias Structure Design, Section 6, except that two separate inner pole pieces are used so that there are two independent sets of cavities. In addition, cylindrical magnet structures are used instead of bar type structure as in Watson magnet arrangement because of the desire to make a smaller structure. Figure 90 shows a basic bias structure for one single track. The magnetic field is generated by four 0.25 x 0.25 x 0.125 in. rare earth cobalt (Rarenet) magnet epoxyed in a 0.5 in. diameter 0.55 in. long cylindrical magnet structure. These magnet structures are epoxyed to the inner bias plate (1.65 x 1.65 x 0.050 in.). The coarse field adjusting shunt (0.060 in. diameter soft iron pins) and fine tuning screws (0.25 in. diameter mu-metal screws with 40 thread/in thread) are all integrated in the magnet structure as shown in Figure 90. The memory package in its plastic holder is placed directly above the inner bias plate with magnet structures positioned in the four holes of the plastic holder. The top bias plate is placed on top of this assembly and held securing to the magnet structures by means of metal screws.

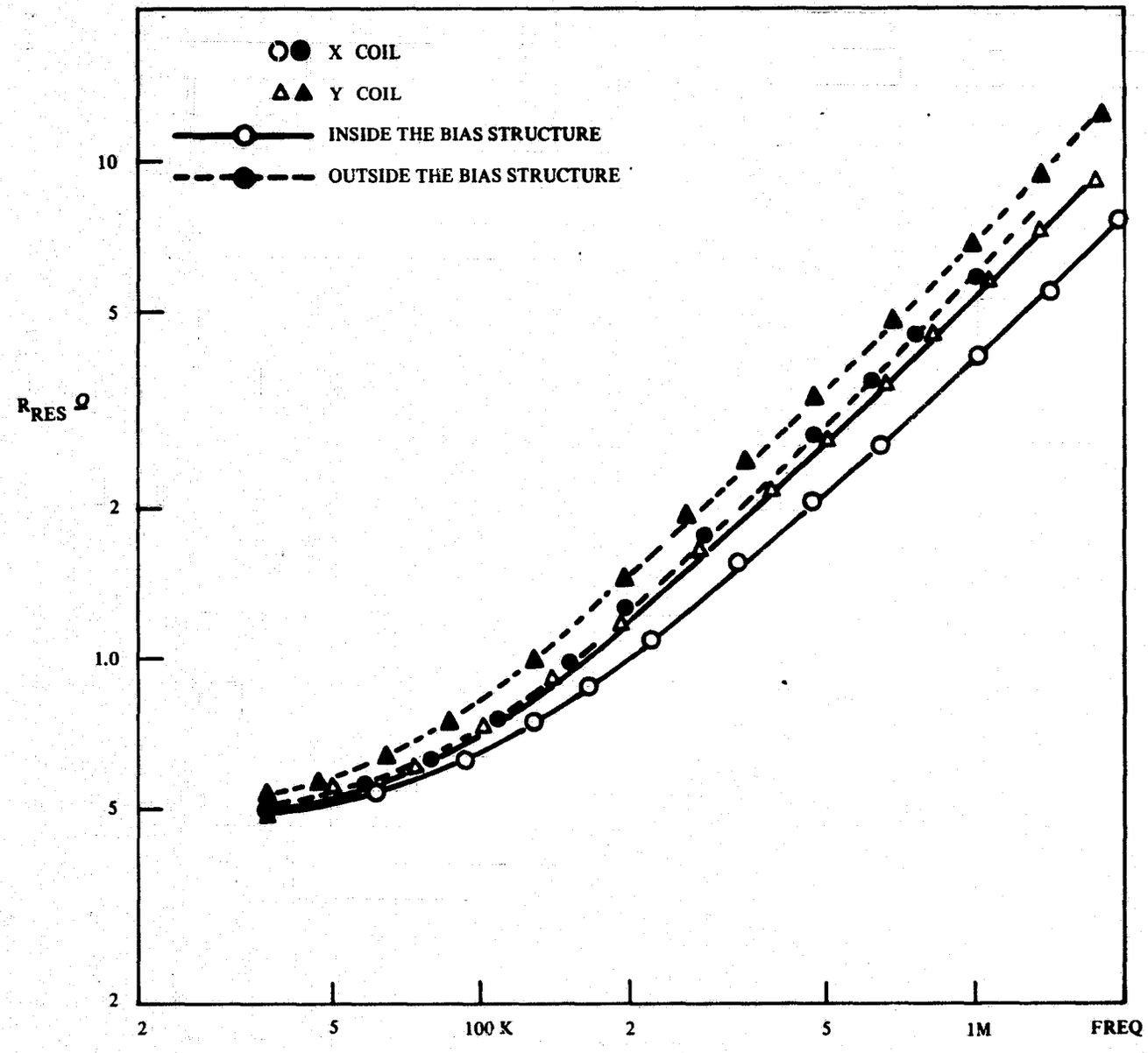


Figure 89. Coil Resistance as a Function of Frequency

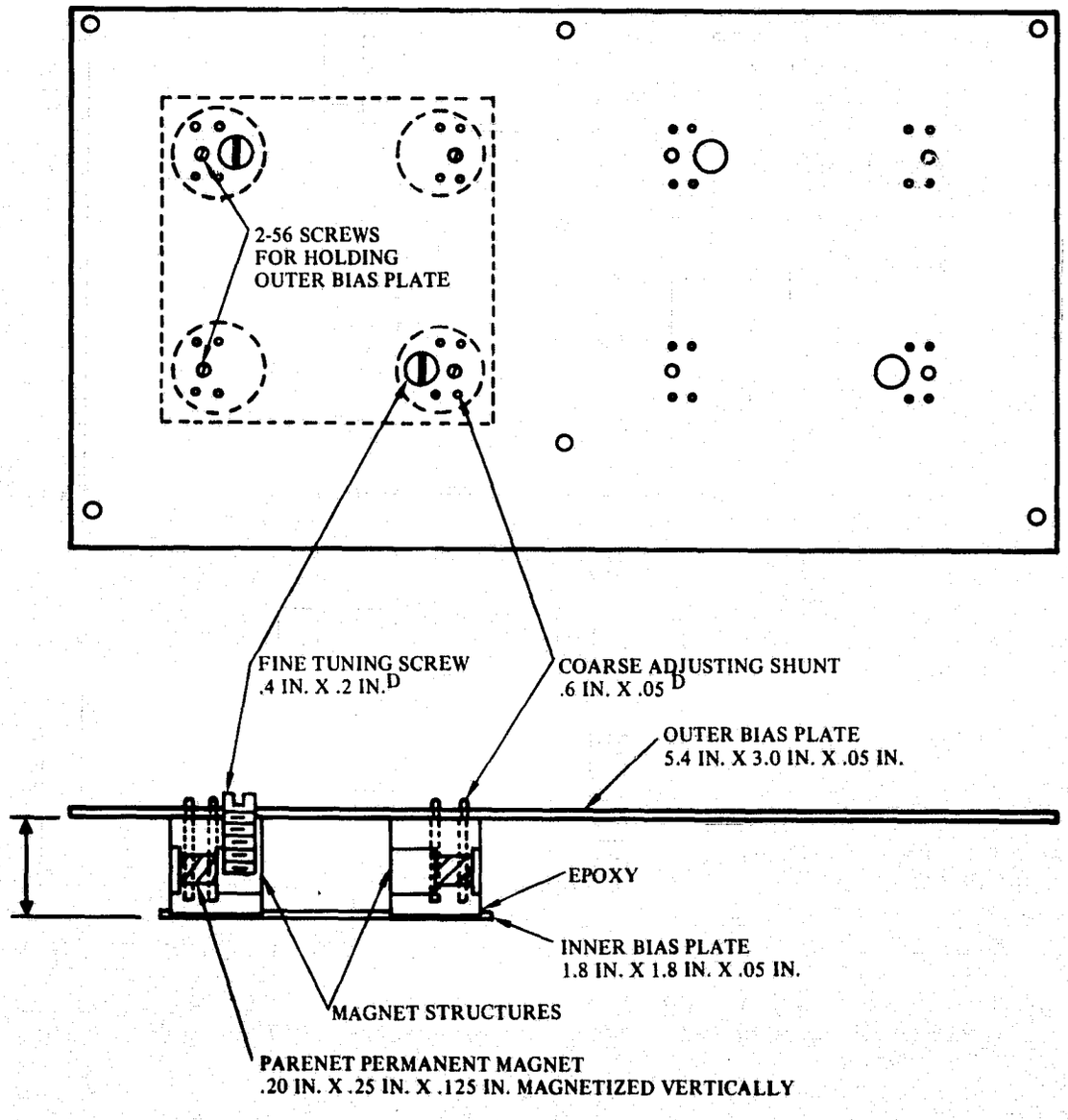


Figure 90. Basic Bias Structure for One Track

Two of these basic assemblies are attached to one outer bias plate but they have separate inner bias plates so that their bias fields at this point are still independent. The third assembly is attached to another outer bias plate but on the other half of this plate there is a dummy assembly with two magnet structures. These two outer bias plates are placed on an aluminum frame as shown in Figure 91. The four sides of the frame are covered with mu-metal plates to form a closed structure. Assembled innerplates of the bias cavities contact each other and are now closely coupled through the side plates so that the magnetic fields are not independent.

The magnetic field distribution inside the structure is shown in Figure 92. The field distribution varies according to the shunt pins distribution which indicates that the reluctance in the bias plate is not low enough to ensure an equal potential surface. However, the variation in the active device area is less than 0.3 Oe which is sufficient for the present application. The coarse field adjustment is proportional to the number of shunts in the cavities as shown in Figure 93(a). The magnetic field in each cavity can be approximated by the following relations with an accuracy of ± 2 Oe

$$H_1 = 125 - 2.4\ P_1 - 1.75\ P_2 \text{ Oe}$$

$$H_2 = 122 - 1.8\ P_1 - 2.3\ P_2 \text{ Oe}$$

$$H_3 = 117 - 2.45\ P_3 \text{ Oe}$$

where, H_1, H_2 and H_3 are the field in cavities 1, 2, and 3 as designated in Figure 91 and P_1, P_2, and P_3 are the number of shunt pins in each cavity. The fine tuning screws are turned to maximum air gap in the above measurements.

The effect of the fine tuning shunts are shown in Figure 93. As expected the field variation is not a linear function with respect to the travel of the screw. This makes the field inside each cavity difficult to estimate from the shunt combinations.

The memory devices in the package are accessed through two miniature connectors soldered to the two ears of the ceramic package. These connectors are wired to a large connector (Amphenol 57 - 40360) mounted on the front side of the bias structure. In-plan field coil leads are soldered directly on one of the ceramic package ear and the leads from all three tracks are brought out from one slot in a side wall without crossing the chip access leads. In this arrangement, two openings have to be made on the magnetic cover plates of the module which will cause some field leakage. The leakage measurement will be discussed in Section 10 on the Feasibility Model Evaluation.

The overall dimension of this magnetic module is 6 x 3 x 1.2 in. and it weighs 1.75 lb, including all the devices, packages and connectors. Figure 94 shows the picture of the assembled module.

8.5 Engineering Model Electronics

This section is a discussion of the electronics used in the feasibility model. Applicable discussions on individual circuitry are covered in Section 4 leaving this section mainly as a performance critique and a discussion of the setup problems. Schematics, wiring lists, label lists, etc. are too bulky to include here, being appropriately included as a travel document with the Engineering Model. Detailed circuit design is being retained in laboratory notebook 11321.

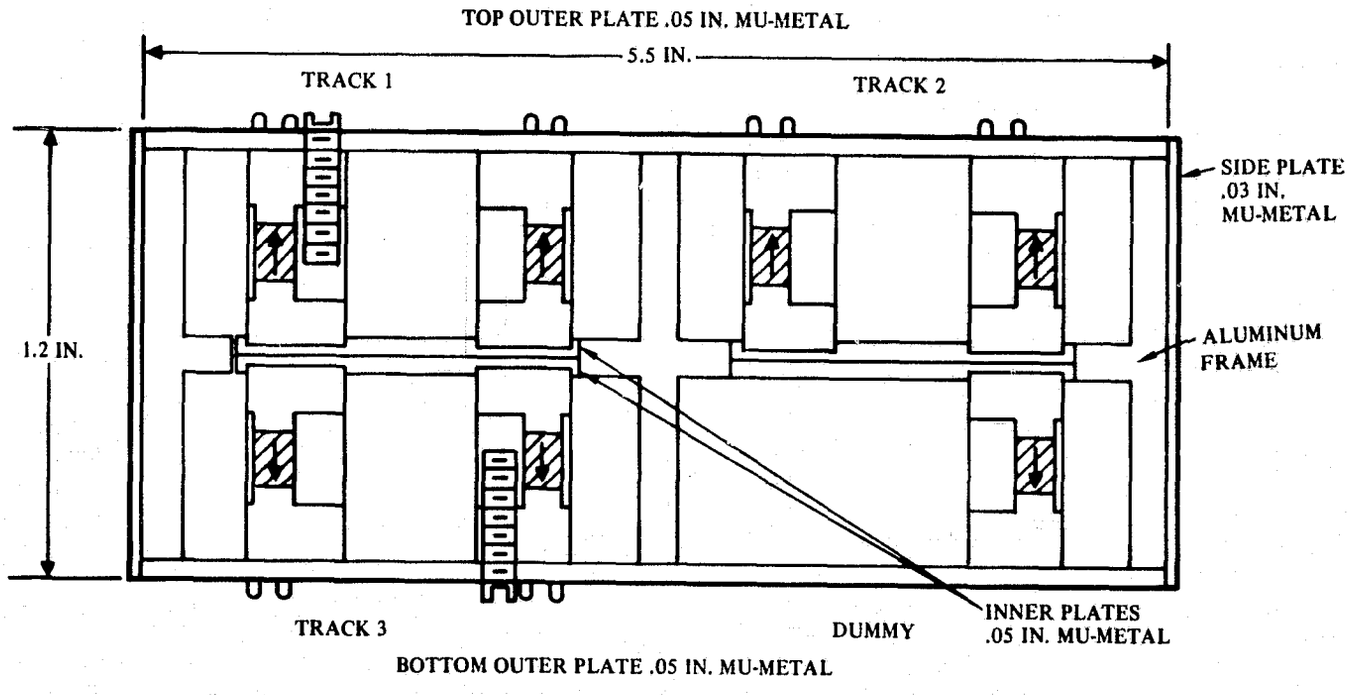


Figure 91. Magnetic Bias Structure

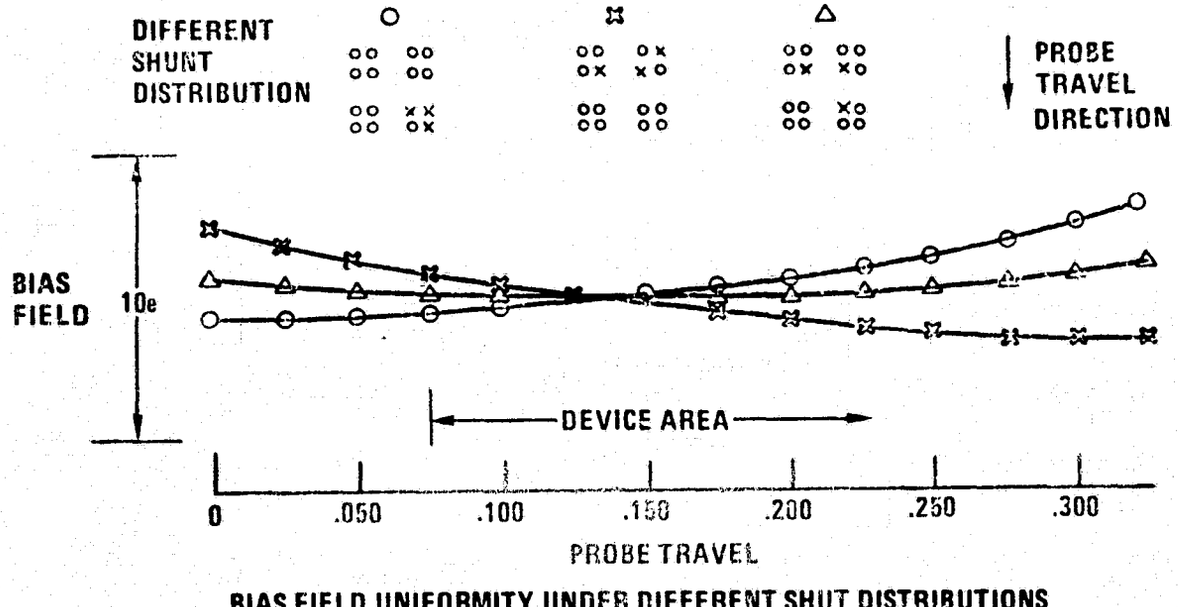
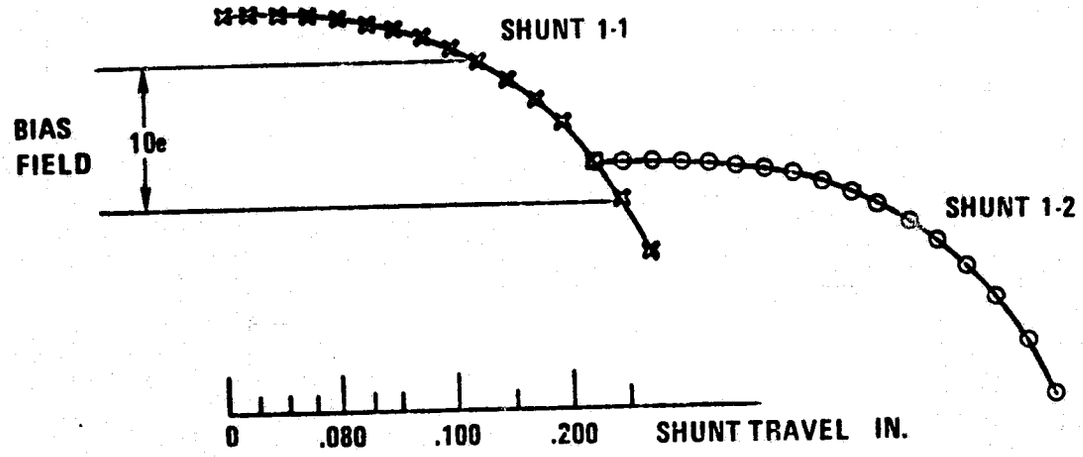


Figure 92. Bias Field Uniformity under Different Distributions



EFFECT OF THE FINE TUNING SHUNTS

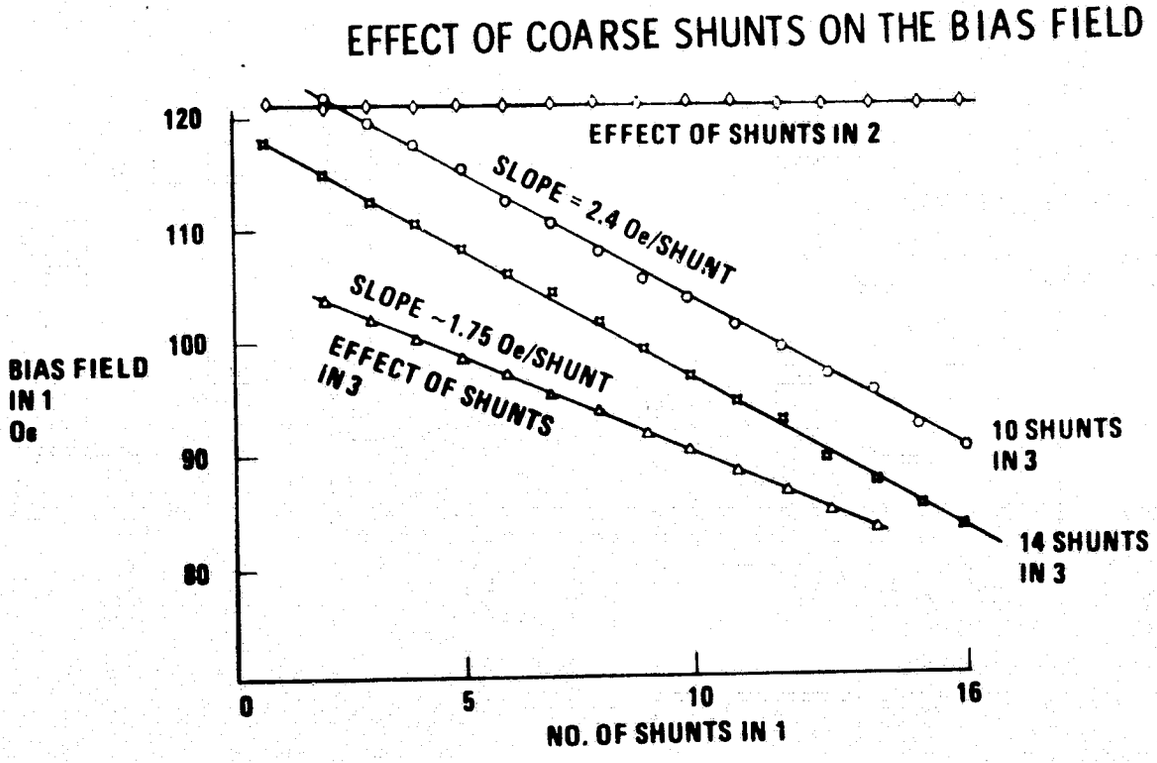


Figure 93. Bias Field Adjustment

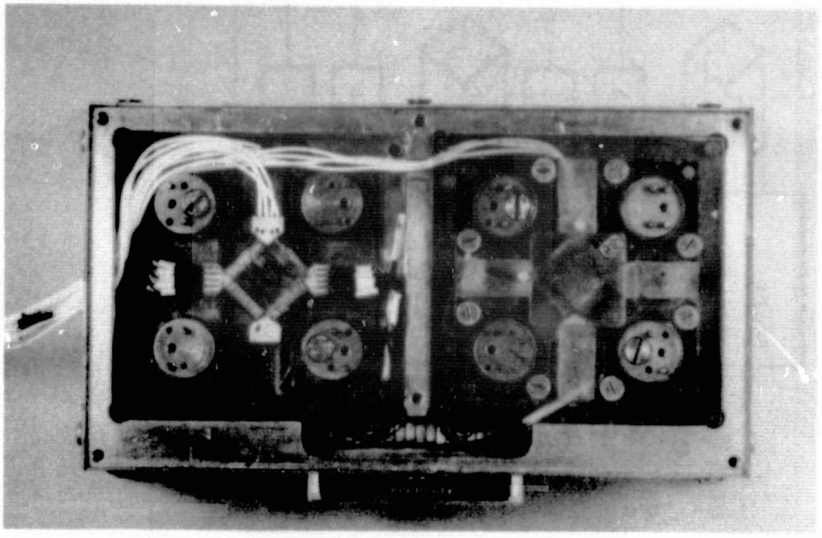


Figure 94. Magnetic Module with Top Bias Plate and Plastic Cover Removed

Description of the engineering model electronics. – The Engineering Model was designed so that circuit concepts applicable to large recorders could be evaluated. Accordingly, techniques such as chip-to-chip switching and coil turn-on/turnoff were explored. Figure 95 is the block diagram of the Engineering Model showing 3 tracks of 2 chips apiece and a timing board. Functionally, the circuits can be organized according to Figure 96. Discussion of each of these blocks and the circuits within them were covered in Section 4. Layout of the electronics boards involved conventional commercial parts as shown in Figure 97 and 98. Layout was primarily a matter of convenience with extra board space allocated and with the parts laid out according to function. For example, drivers are toward the bottom of Figure 97, sensing is in the middle and logic is toward the top. Connections between boards is done with flexible circuits to demonstrate the ease of debugging and testing of boards in a "nonconnector" assembly.

Major problem areas discovered during the testing are as follows:

1. Sensing and detection. On turnon the x/y field phasing may be different from the long term "equilibrated" phasing which will cause a misplaced output relative to the strobe. The start phasing was corrected.

2. X coil turnoff overshoot is critical as discussed in Section 7. Reducing overshoot to less than 10 percent of peak amplitude corrected the problem.

3. Use of the precursor bubble (which identifies a record head) complicated checkout because it is in effect within a feedback loop where an extraneous bubble signal or the precursor can cause an indication of a full chip. This problem was aggrevated by the high error rate of some of the chips.

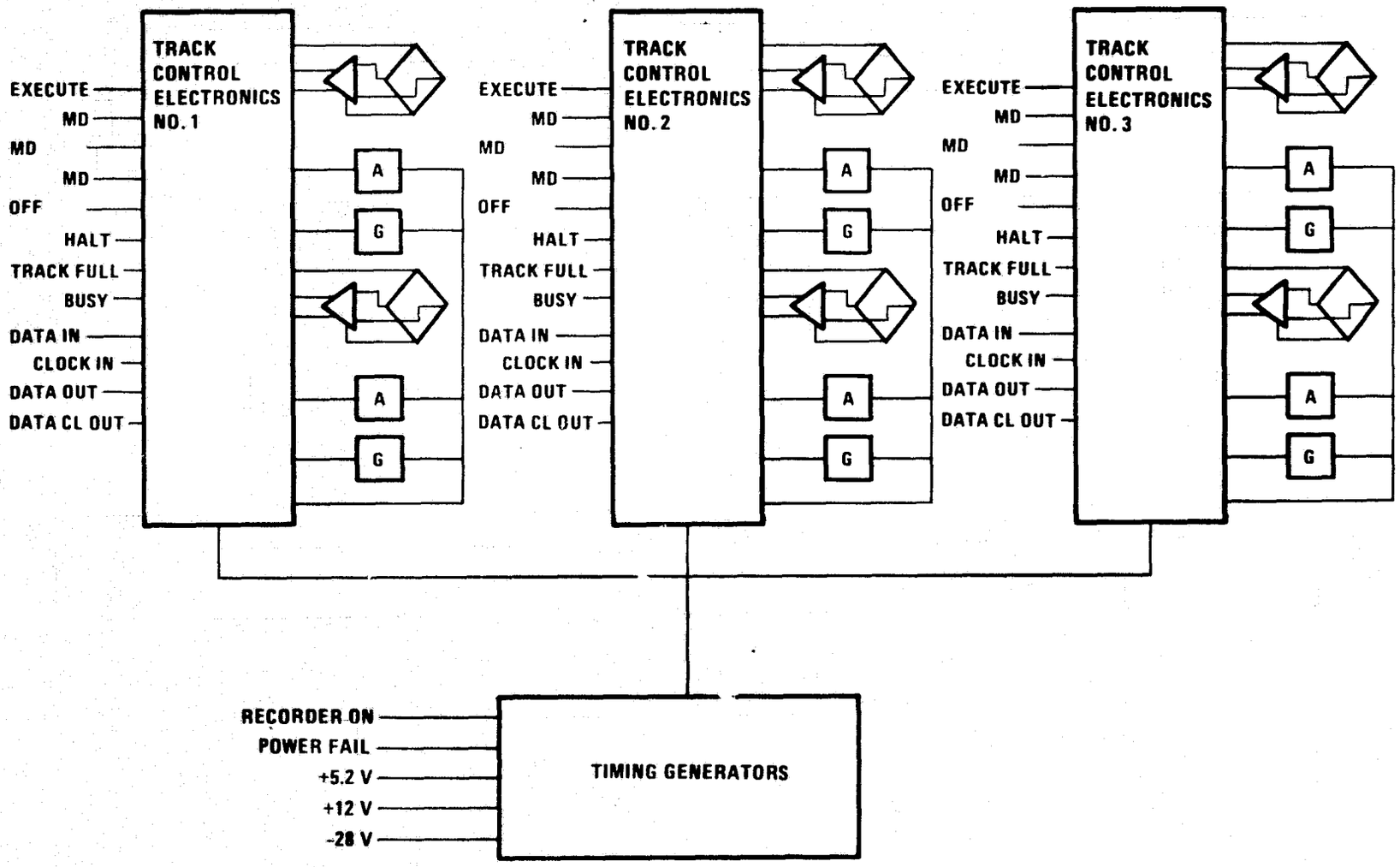


Figure 95. Engineering Model Block Diagram

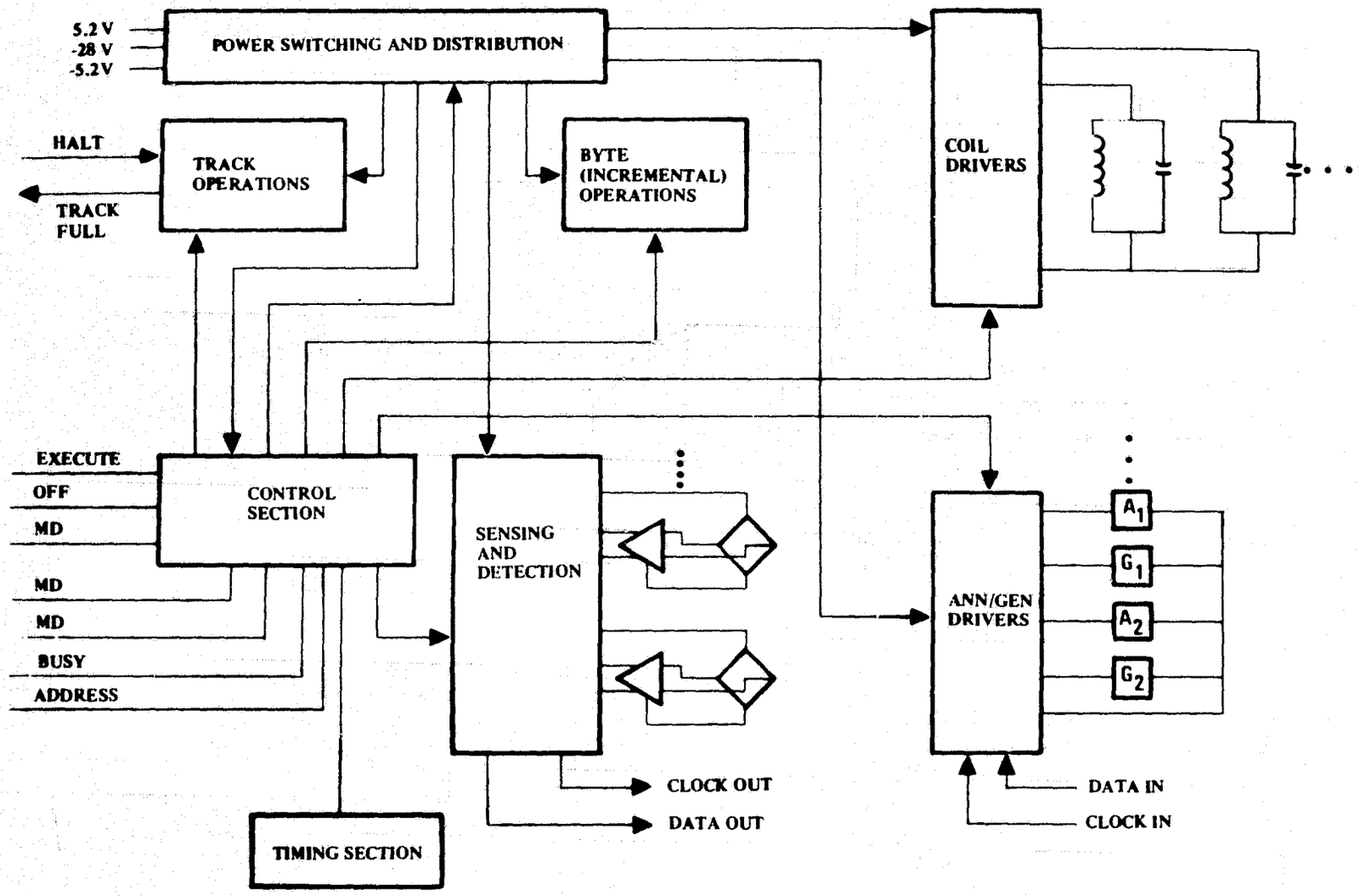


Figure 96. Track Board Block Diagram

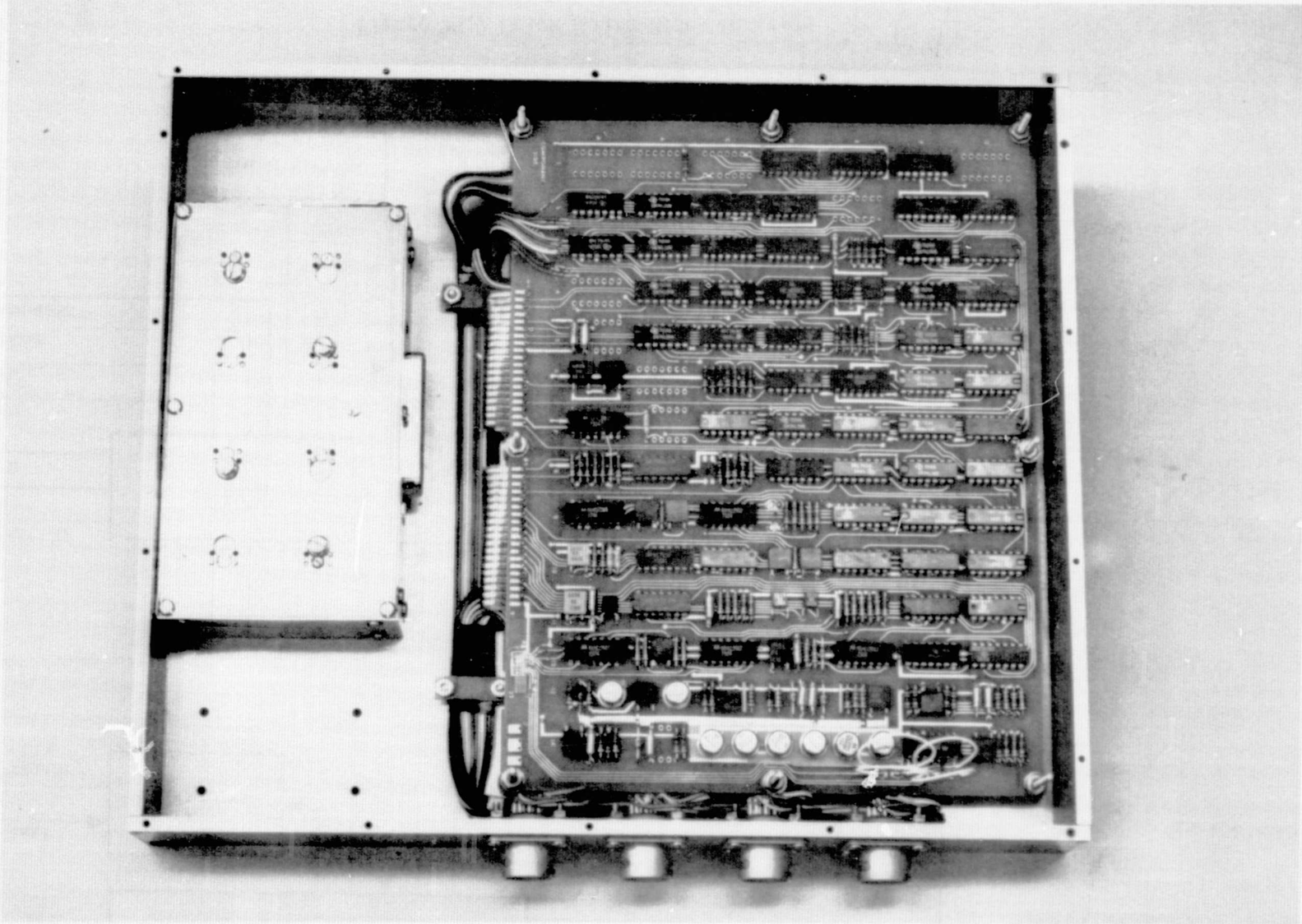


Figure 97. Top View of the Engineering Model Showing Track Board

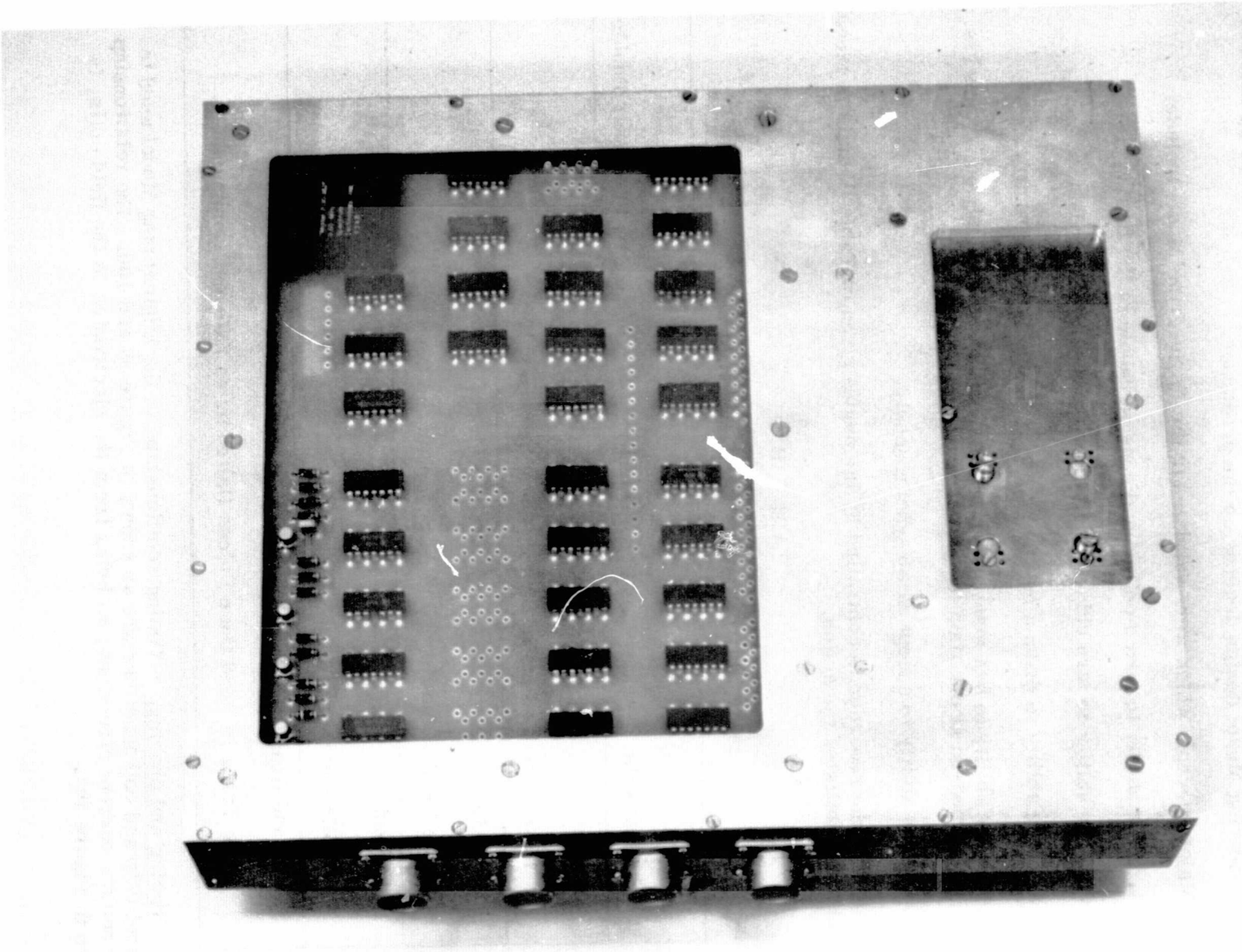


Figure 98. Bottom View of the Engineering Model Showing Timing Boa .d

Solutions to the first two were easily implemented in the Engineering Model but for the third the only solution is to continue to improve error rate since so much of the Engineering Model design depends on the precursor.

Major concepts which were validated in the Engineering Model include:

1. The ability to turn a coil on and sense a bubble in the first cycle.
2. The ability to turn chips on and off without scrambling data.
3. The ability to drive a coil using low cost, low power circuitry.
4. The ability to bus many preamplifier together so that only one channel is turned-on at one time for a short duration when needed.
5. The ability to accept data asynchronously.

Operation of the recorder is controlled by the modes given in Table III and the execute signal which initiates the action.

TABLE III.

ENGINEERING MODEL OPERATION MODES

Erase Clears the Track of Bubbles and Writes a Single Record Precursor Bubble
Write Asynchronous Data is Written Onto the Track
Track Align The Head of the Record is Aligned with the Detector
Byte Read 8 Bits are Read
Search and Read The Track is Read Once Unless Halted by an External Command

Timing and phasing. – Timing relationships in the Engineering Model used to control chip and coil functions are as shown in Figure 99 and 100. The relationship between the current directions, as being from the electronics to the field coils, is given in Figure 101.

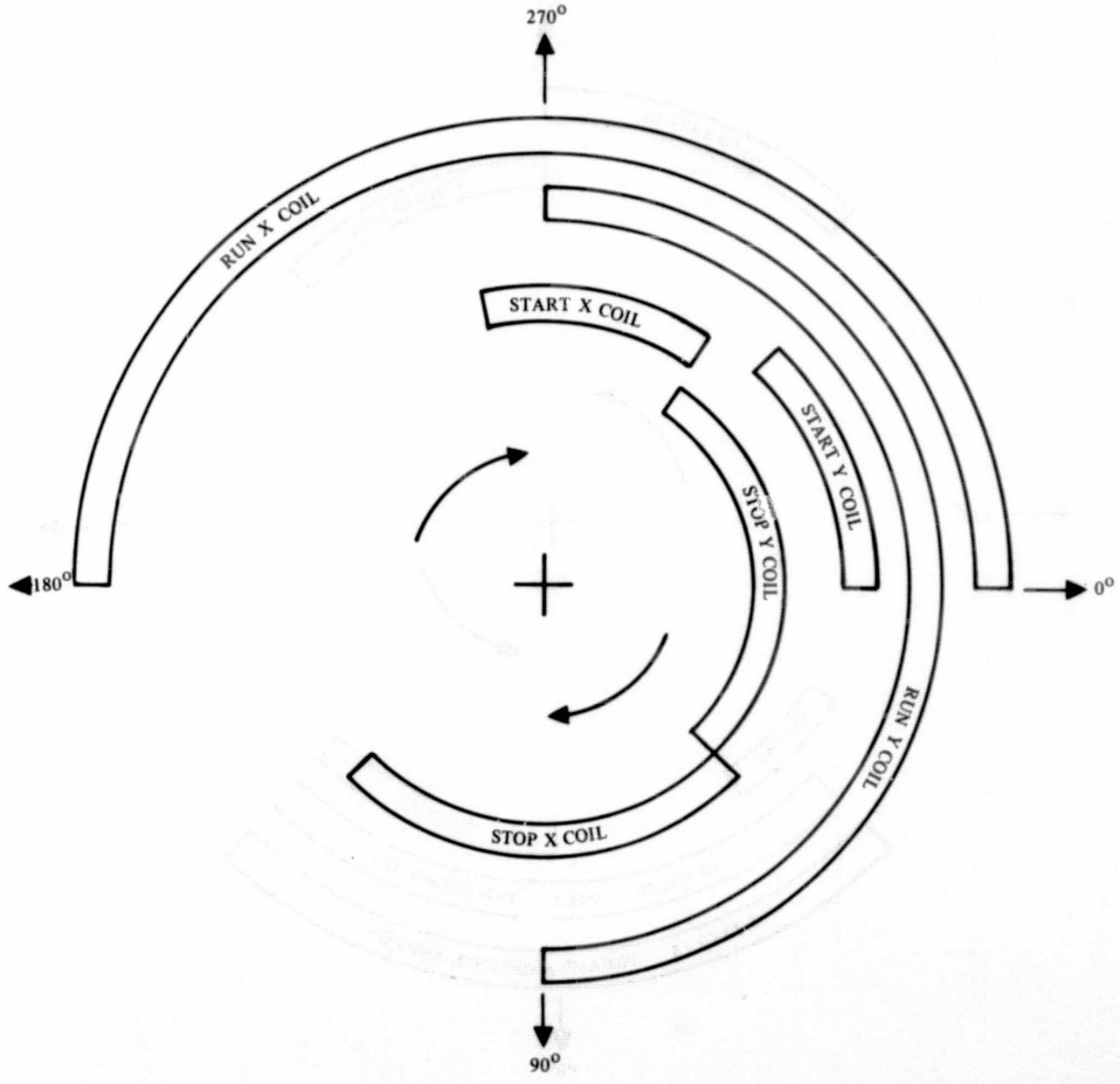


Figure 99. Coil Driver

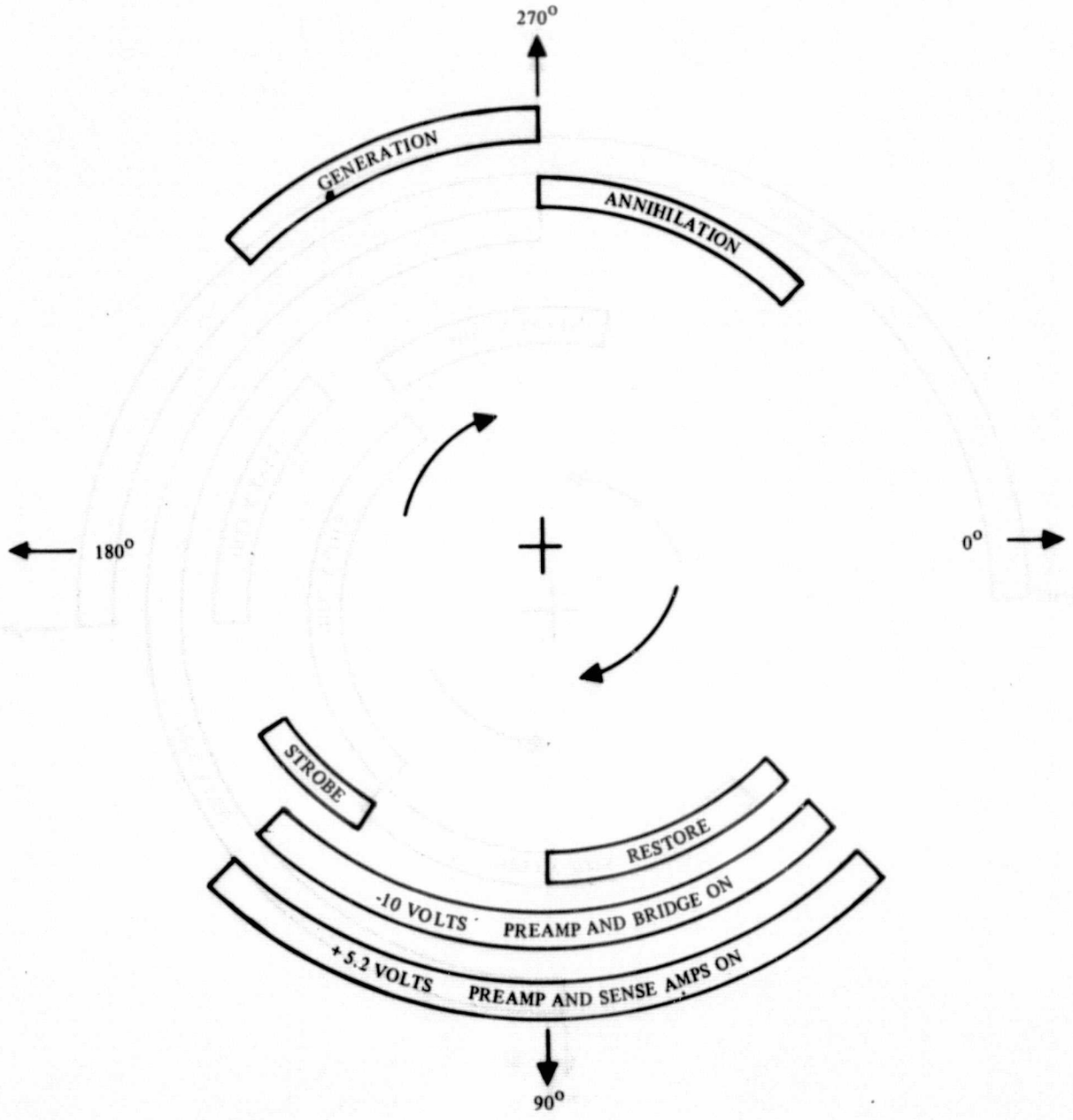


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Figure 100. Chip Driver and Sensing Timing

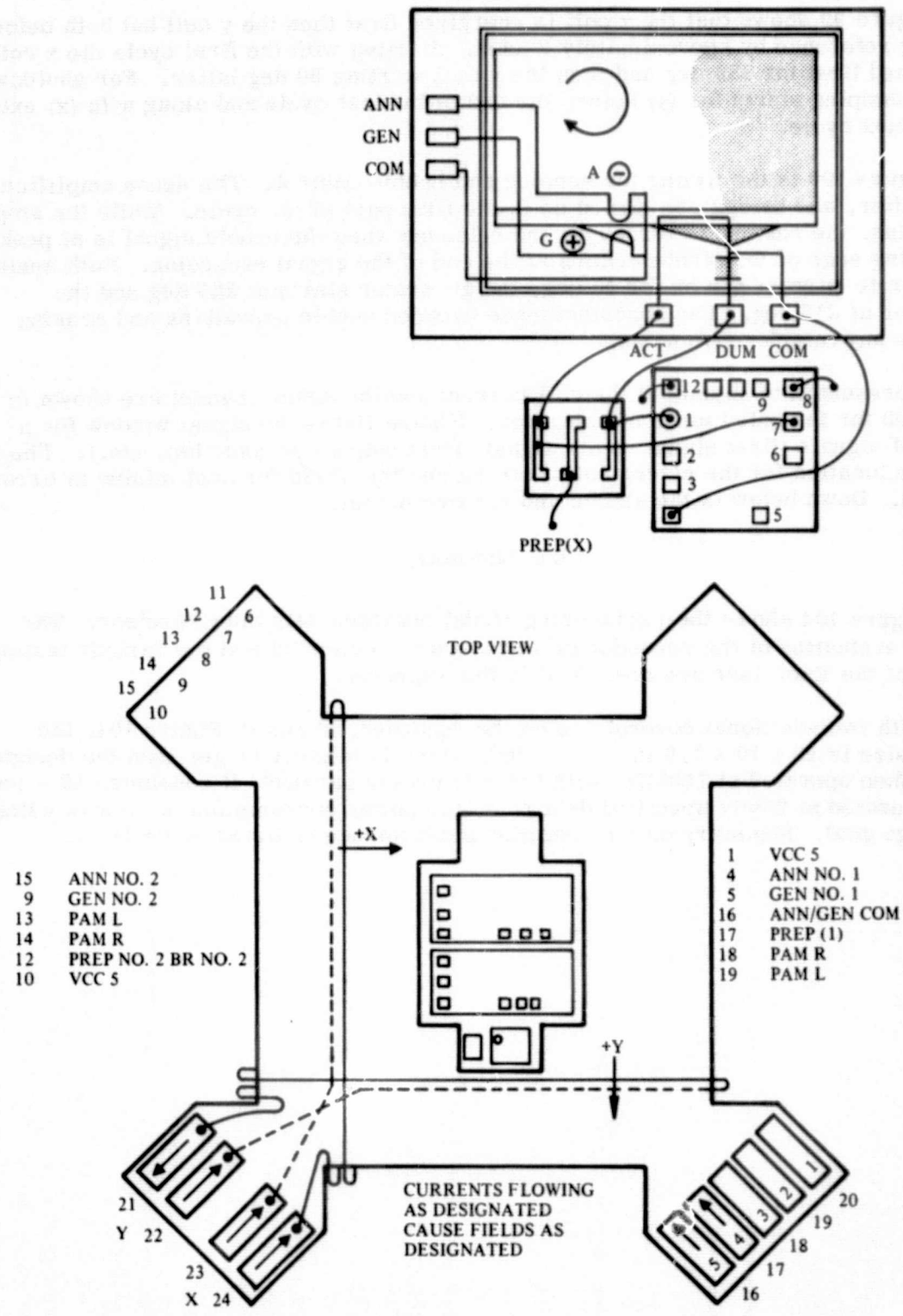


Figure 101. Current and Field Orientation in the Package

Figure 99 shows that the x coil is energized first then the y coil but both before the 0 deg reference by approximately 2 μsec. Starting with the first cycle the x coil is replenished first for 180 deg and then the y coil starting 90 deg latter. For shutdown, critical damping starts for (y) before the end of the last cycle and along with (x) extends into the next cycle.

Figure 100 is the timing for sensing and bubble control. The sense amplifier, preamplifier, and bridge are turned on in the first part of the cycle. While the amplifiers are settling, the restore is turned on and released when the bubble signal is at peak. The leading edge of the strobe occurs at the end of the signal excursion. Both annihilate and generate current are on for 45 deg, the generator starts at 225 deg and the annihilator at 315 deg. The noncoincidence between bubble operations and sensing precludes any interference noise.

Representative signals of the coil current and the sense channel are shown in Figure 102 for the gated mode of operation. Figure 103 is the signal window for a number of signals (first signal vs nth signal, first chip vs second chip, etc.). The (↓) shows the location for the placement of strobe and threshold for best minimum error operation. Down below is the strobe and restore pulses.

8.6 Summary

Figure 104 shows the Engineering Model operated with the Exerciser. The detailed evaluation of the recorder is discussed in Section 10 and the various testing options of the Exerciser are described in the Appendix.

With two additional coverplates on the recorder, shown in Figure 104, the overall size is 12 x 10 x 1.8 in. or 216 in^3, which is slightly larger than the design goal. When operated at 150kHz with three tracks in parallel, it consumes 15 w power but if operated at 25kHz specified data rate, the power consumption of 3 w is within the design goal. Summary on the recorder performance is listed in Table IV.

VERT = 1A/DIV; HORIZ = 6.67 μS/DIV
TOP = Y CURRENT, BOT = X CURRENT
TIMING MARKS = RCLS
CURRENT INTO CAPS = UP
-V = 16 VOLTS

VERT = 1A/DIV; HORIZ = 833 NS/DIV
TOP = Y CURRENT BOT = X CURRENT
TIMING = RCLS
CURRENT INTO CAPS = UP
SHOWING A SINGLE CYCLE

TOP = SENSE AMP INPUT
10101010 PATTERN
10 MILLIVOLTS/DIV; 6.67 μS/DIV
MIDDLE TTL OUTPUT DURING
WRITING CYCLE
BOTTOM = TIMING MARKS (RCLS)

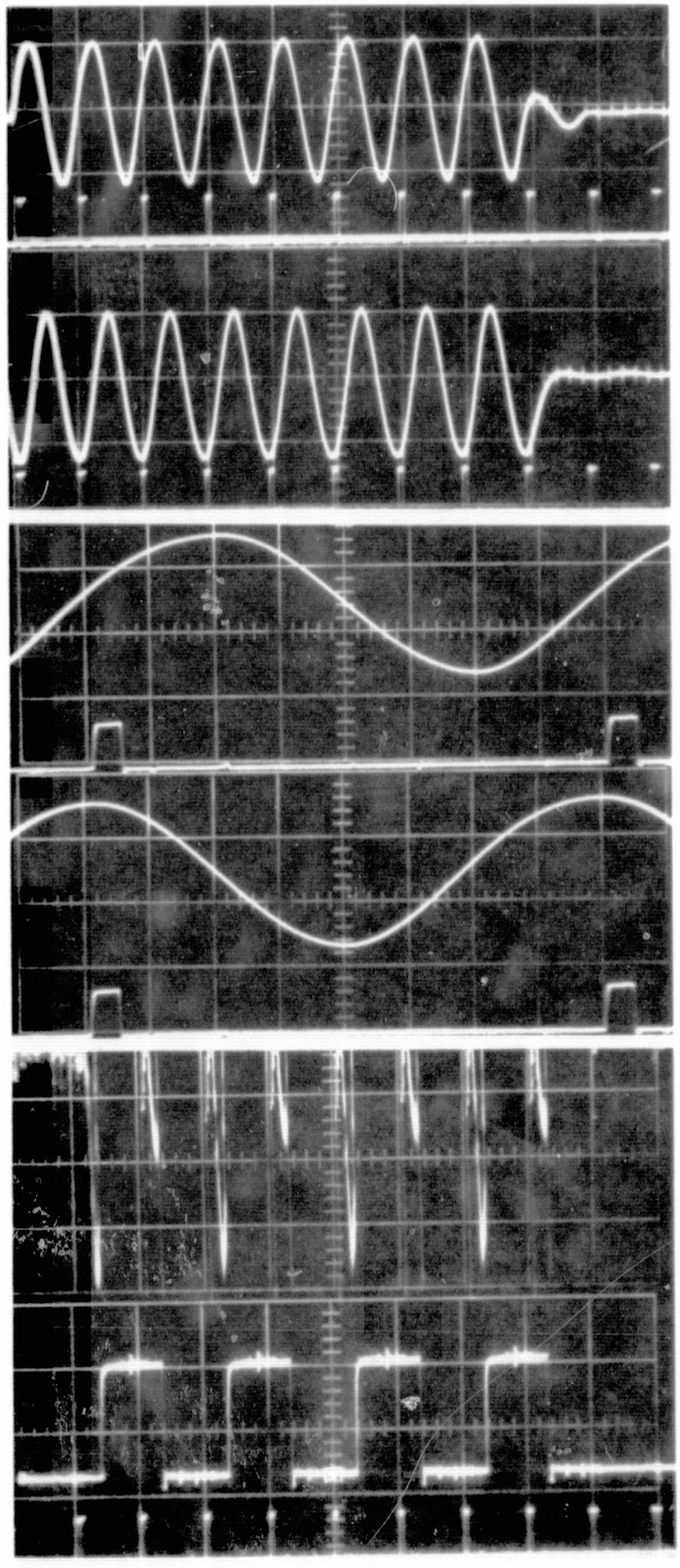
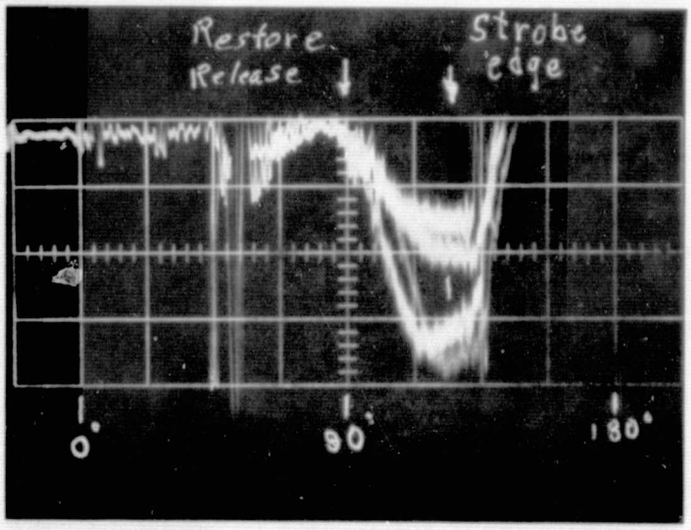
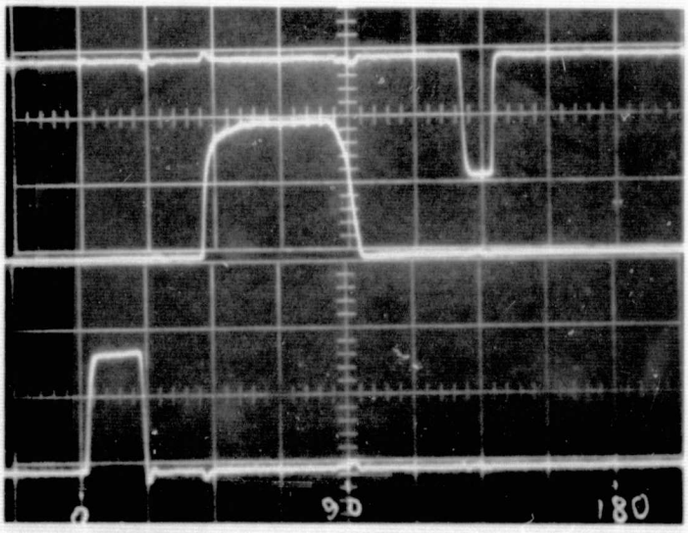


Figure 102. Current Waveforms and Sense Signals



SIGNAL COMPOSITE
SENSE AMP INPUT
FIRST 3 BITS
10 MILLIVOLTS/DIV; 416 NS/DIV

CONDITIONS
-V = 14.5 VOLTS



SENSE CHANNEL TIMING
TOP STROBE (STRS)
MIDDLE RESTORE (RESS)
BOTTOM CLOCK (RCLS)
2 VOLTS/DIV; 416 NS/DIV

Figure 103. Sense Channel Signals (Composite)

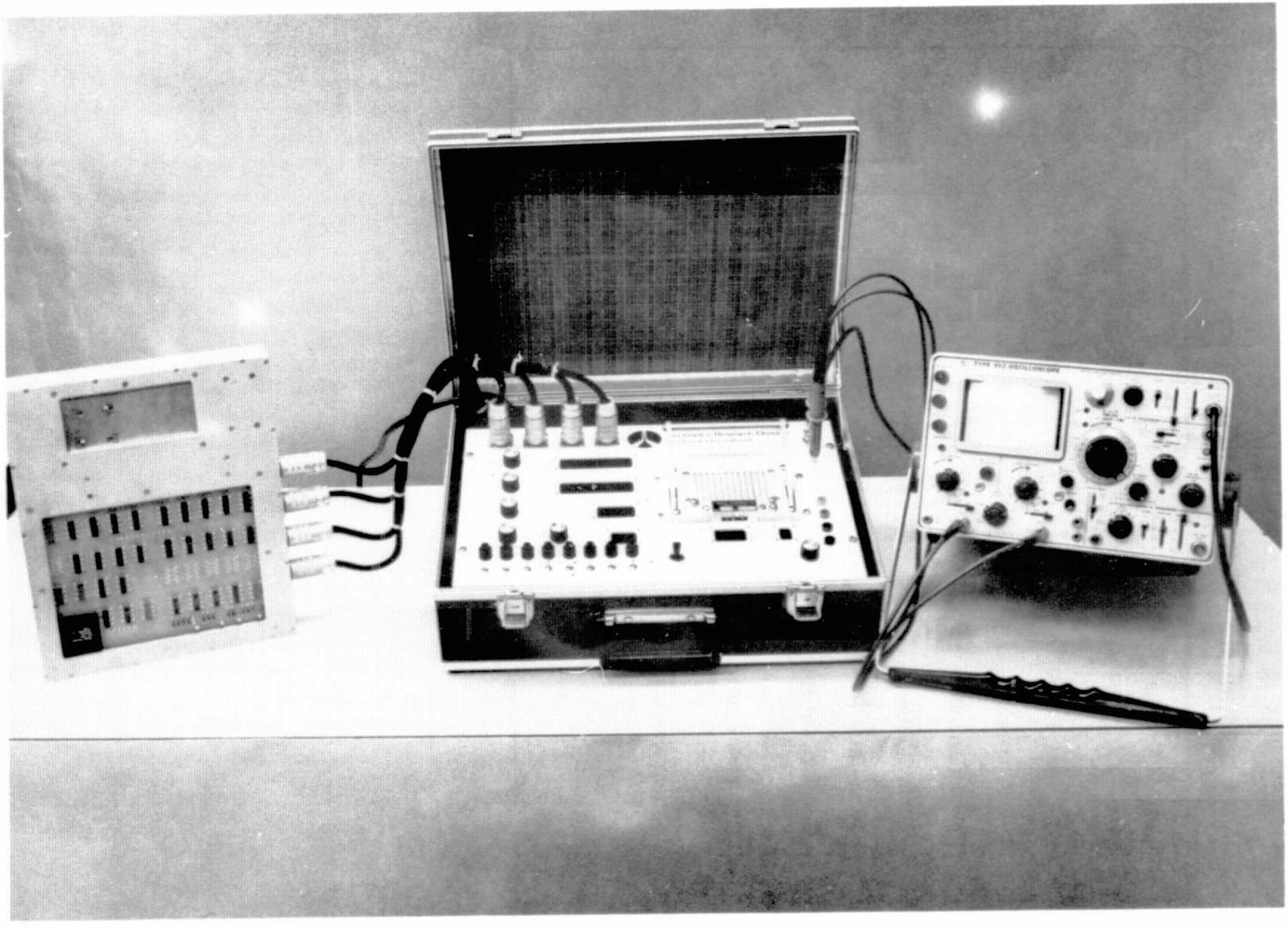


Figure 104. The Feasibility Model with Exercisor

TABLE IV.

ENGINEERING MODEL PERFORMANCE SUMMARY

Number of Tracks	3
Number of Chips	6
Capacity per Track	20,000 bits
Total Capacity	60,000 bits
Rework Speed	up to 1.5×10^5 bits/sec
Playback Speed	up to 1.5×10^5 bits/sec
Error Rate	10^{-4} to 10^{-8} error/bit
Operating Power Standby	0 watt
Operating Continuous at 150kHz	~ 5 w/track 15 w total
Asynchronous at 25kHz	~1 w/track 3 w total
Size	$12 \times 10 \times 1.8$ in. = 216 $in.^3$
Weight	9.25 lb

9. PROTOTYPE RECORDER DESIGN

In this chapter, a conceptual design of a 5×10^7 bit bubble recorder prototype is presented. The design parameters are listed in the original work statement as shown in Table V. Different design considerations are discussed separately based on the study results discussed in the previous sections. All the design concepts have been demonstrated to be feasible either in this program or in the literature, but some of them require further development before they can be used in a prototype recorder.

The discussions are concentrated on the major elements of the Bubble recorder. These include the storage chip organization, the device package, the rotating field coil, the bias structure and the control electronics. This section is concluded with a summary of the projected performance and a mock-up drawing on the prototype appearance.

TABLE V.

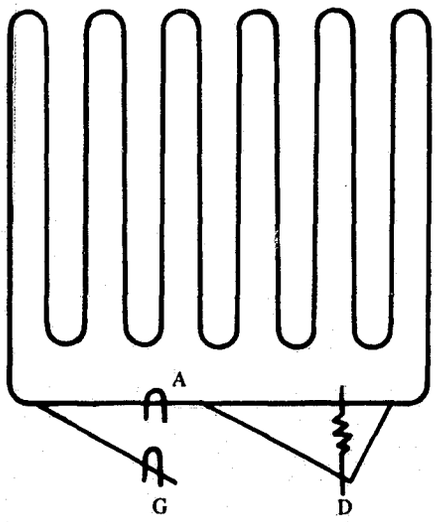
PROTOTYPE RECORDER DESIGN GOALS

Number of tracks:	4
Total capacity:	4.6×10^7
Recored speed per track:	6.4×10^3 bits/sec
Playback speed per track	1.5×10^5 bits/sec
Power:	
Playback	6 watts
Record	4 watts
Size:	6 x 7 x 5 in.
Weight:	8 lb
Record time:	120 min
Playback time:	5 min
Temperature Environment:	0°C to 50°C

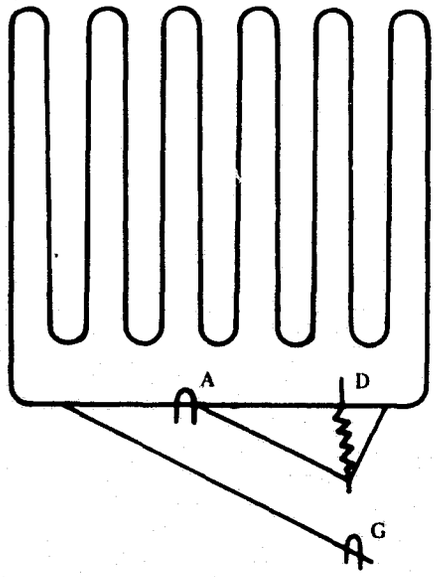
9.1 Chip Organization

For FIFO recorder application, a single loop serial register is still the best chip organization. It is obvious that the larger the chip capacity the fewer the associated components required and the better the system reliability. At present photolithography limits of 1μm resolution dictate that a 16 μm period bubble circuit is the highest density (2.5×10^6 bit/in.^{2}) circuit that can be achieved. The optical resolution also limits the device area to approximately 0.25 x 0.25 in. limiting a simple loop device to 10^5 bits or less. A yield analysis indicates (Ref 21) that single loop arrangement without redundance loop in the device can have a reasonable yield under present processing conditions. Thus, a 100k bit chip is assumed for the present phototype design.

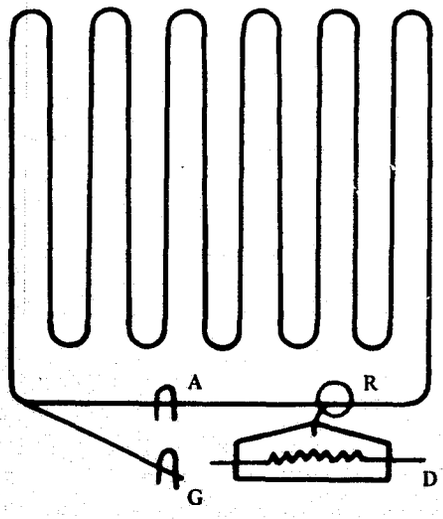
In the present single loop organization, there are three control functions on a chip, i.e., generation, annihilation and detection. With the detection circuit in the loop there is a finite separation between the detector and annihilator positions. The



(A) GENERATOR ALIGNED WITH ANNIHILATOR



(B) GENERATOR ALIGNED WITH DETECTOR



(C) GENERATOR,ANNIHILATOR AND DETECTOR ALL ALIGNED

G = GENERATOR
A = ANNIHILATOR
D = DETECTOR
R = REPLICATOR

Figure 105. Three Possible Organizations for Single Loop Storage

generator is located in a separate branch and can be positioned at the same position as the annihilator, which causes a gap in the memory loop and requires a chip align mode in the recorder function. In the prototype design, it is suggested that the generator be aligned with the detector to eliminate the gap in the memory track so that the recorder can be accessed on single chip basis. This arrangement however, introduces a delay between generation and annihilation function which has to be remembered by the control electronics. This problem can be avoided by using an off track detector such as guard rail detector (Ref 22) where the stored information is replicated toward the detector by either an active (Ref 23) or a passive (Ref 24) replicator. In this arrangement all the generation annihilation and detection functions can be aligned to one single bit position, no phase delay is then involved. However, it requires one additional control function. All three organization concepts are illustrated in Figure 105.

For the component design the basic T-bar propagation and storage elements and the chevron composition branch can still be used in the 100k bit chip design but the inner 180 deg corner in the T-bar structure and the chevron and T-bar transition designs have to be modified to improve the bias margin and lower the driving field. The loop generator and annihilator design can still be applied to the 16 μm period circuit. Single level design (Ref 23) can be considered to simplify the processing and improve yields.

The present two level detector design has to be simplified on the basis of alignment difficulty between chevron elements and gold contact and also the additional processing procedure required for the contract level. A single level thick film detector of the zig-zag type (Ref 22) can be used. To achieve a signal level better than 1 mv (in order to be able to drive some existing amplifier circuit (Ref 25) it is estimated that the detector has to be more than 80 chevrons long and operated with 3 or 4 ma. The detector resistance will be around 400 Ω.

An alternative approach in the detector design is to use an off track detector as discussed before. Using two passive replicator and annihilator combination an alternative bit detection can be achieved in two parallel guard rail detectors. By putting these two detectors in the same detector bridge circuit a full data rate detection can be regained. The circuit arrangement is shown in Figure 106. In this arrangement, the length of the detector stretch will not effect the basic storage loop layout so that higher detector output can be expected. Since two paralled detectors are used, bubbles only propagate alternatively in the detector, less bubble interaction is expected in this circuit therefore the whole chip can be operated with a less in-plane driving field.

The success of this design depends on the passive replicator which has not been fully evaluated in this laboratory yet. An active replicator which requires additional improvement can also accomplish the same function but it requires bi-polar driving current which will complicate the matrixing circuit when assembled in the system.

To reduce noise problems in the sense circuit, two additional factors have to be considered in the detector design. First, the detector resistance has to be kept low (preferably less than 300Ω). A large detector resistance will not only require a large decoupling resistance in the detector network (thus higher detector supply voltage) but also increases the coupling noise in the sensing circuit. Secondly, the $d\phi/dt$ voltage must be reduced by minizing the loop area closed by the detector leads or by adding additional lead in the detector circuit (as shown in Figure 106) so that the $d\phi/dt$ voltage

induced in the active and dummy detector elements can cancel each other (Ref 26). When an alternative bit detector circuit is used, the $d\phi/dt$ effect can further be avoided by extending the sense circuit restore and strobing separation to one field cycle (Ref 27).

9.2 Package and Rotating Field Coil Design

To minimize the recorder size and complexity it is preferable to put as many device chips in one coil set as possible. On the other hand, the coil power and the package complexity increases with the number of chips in the coil set. In the present system projection, the device chip itself is relatively simple and thus the package cost per chip should be almost independent with the size of the package. (The larger the package, the less the total number of packages required but the higher the cost of each package.) Thus, the package size is primarily limited by the field coil and its driver which are dependent on the voltage and current capabilities of the available power supply.

For the convenience of the control electronics it is preferable to have the number of chips per coil be a multiple of four. Under present power and size limitations it is felt that a 16 chips per coil arrangment, as shown in Figure 107 is the optimum design for the prototype recorder. To achieve a 1.2×10^7 bit per track capacity it would require eight coils for each track and 32 coils for the 4.6×10^7 bit four track recorder.

The chips can be arranged in a 2 x 4 array in two levels for easy access of individual chip. Either of the three package concepts discussed in Section 3 on device packaging can be applied in the present package. Figure 107 shows a package arrangement using the polymer package approach. Assuming the overall chip size is 0.3 x 0.3 x 0.02 in., two levels of 16 chips can fit into a 1 x 1.8 x 0.07 in. package. These two levels of chips can be placed in a face-to-face arrangement as shown in Figure 107 (b) or can be stacked in the same direction as shown in Figure 107(c). In the first case the bubble circuits are very close to the center plane of the coil so that the in-plane field distortion can be kept minimum. However, the bubbles in different levels sense opposite rotating fields so that two different sets of devices which are mirror image of each other are required. This also requires opposite timing controls. The arrangement shown in Figure 107(c) is simpler but it needs an additional spacer so that the device planes can be symmetrical to the coil plane. Since the devices are not placed at the center plane of the coil bias modulation may be induced by in-plane field and thus some small loss of device operating margin may result.

For the chip organization shown in Figure 106 there will be 43 leads from each layer when all the chips are directly accessed out of the package. If additional preamplifier chips and matrixing diodes are mounted within the package the total number of leads in each level can be reduced to 17 (8 chip selections, 4 function selections, 2 sense output 2 power supply and 1 ground). In either case, the conductor lead density is relatively low and can be achieved easily with present technology.

For assembly convenience, the in-plane field coils are wound separately and slid over the device package. Coil winding can be either strip line or ribbon conductors. At 150 kHz the skin depth of copper is 0.0067 in. so that the optimum conductor thickness is 0.013 in. Using a double sided strip line coil a 0.0067 in. thick copper foil would be required.

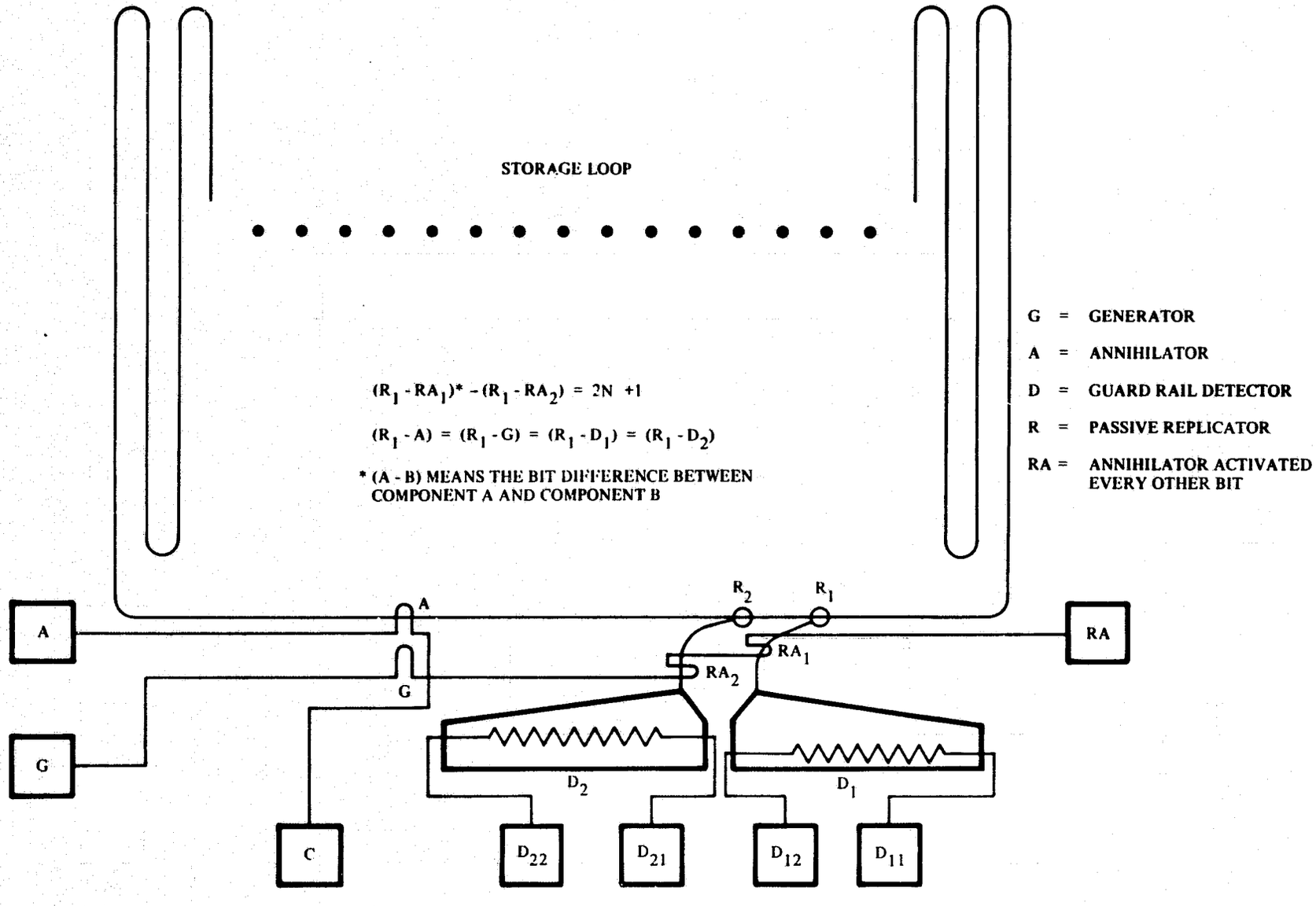


Figure 106. A Memory Chip Organization with Passive Replicator, Annihilator Combination and Guardrail Detector

Assuming a simple coil structure and using the dimensions shown in Figure 107, the coil parameters calculated for both packaging arrangements are shown in Table VI. With 2 amp peak drive current, a 30 Oe in-plane rotating field can be generated with a power dissipation less than 1.28 w for the coil shown in Figure 107(b) and 1.32 w for the coil shown in Figure 107(c). The bias modulation in the later case is less than 1 percent of the peak in-plane field so that if the device bias margin is wide enough, the face-to-face configuration is not really necessary. If a variable width strip line coil is used, the coil dimension, coil-inductance and power dissipation can be further reduced.

9.3 Magnetic Module and Bias Field Supply

The major consideration on the bias structure design is the size of the structure. Using a large structure can minimize the size and weight of the bias module but it requires that all the chips used in the track have to be properly matched in the bias margin. A smaller structure can offer more flexibility in device selection but it will increase the recorder weight. A structure incorporating both attributes is the multiple gap bias structure discussed in Section 6.

Assuming a single bias structure all the coils in each track can be mounted on one track board. As shown in Figure 108 a 4.6 x 6.10 x 0.05 in. PC board would be sufficient for a 2 x 4 array of coil assemblies. The coils must be properly spaced and aligned in the structure to ensure that the leakage field from one coil would not effect the stability of the bubble domain stored in the neighboring coils.

The connection between the track board and external electronics are accomplished by flexicable. For each track board, after properly matrixing the control functions and sensing circuits, a total of 92 leads are needed which would require a two level flexicable circuit.

A bias structure design following the guide lines discussed in Section 6, is shown in Figure 109. The four track boards with 32 coil assemblies will fit in a 7.2 x 5.8 x 1.7 in. magnetic module. Using 0.05 in. thick bias plate with initial permeability of 20,000, the characteristic length of the structure is 19 in. (Eq 20) which is sufficient to cover the whole device area with less than 1 percent variation in the bias field. Using an aluminum frame for supporting the track board and covering the whole structure with 0.05 in. permalloy plates the structure will weigh about 5.5 lb.

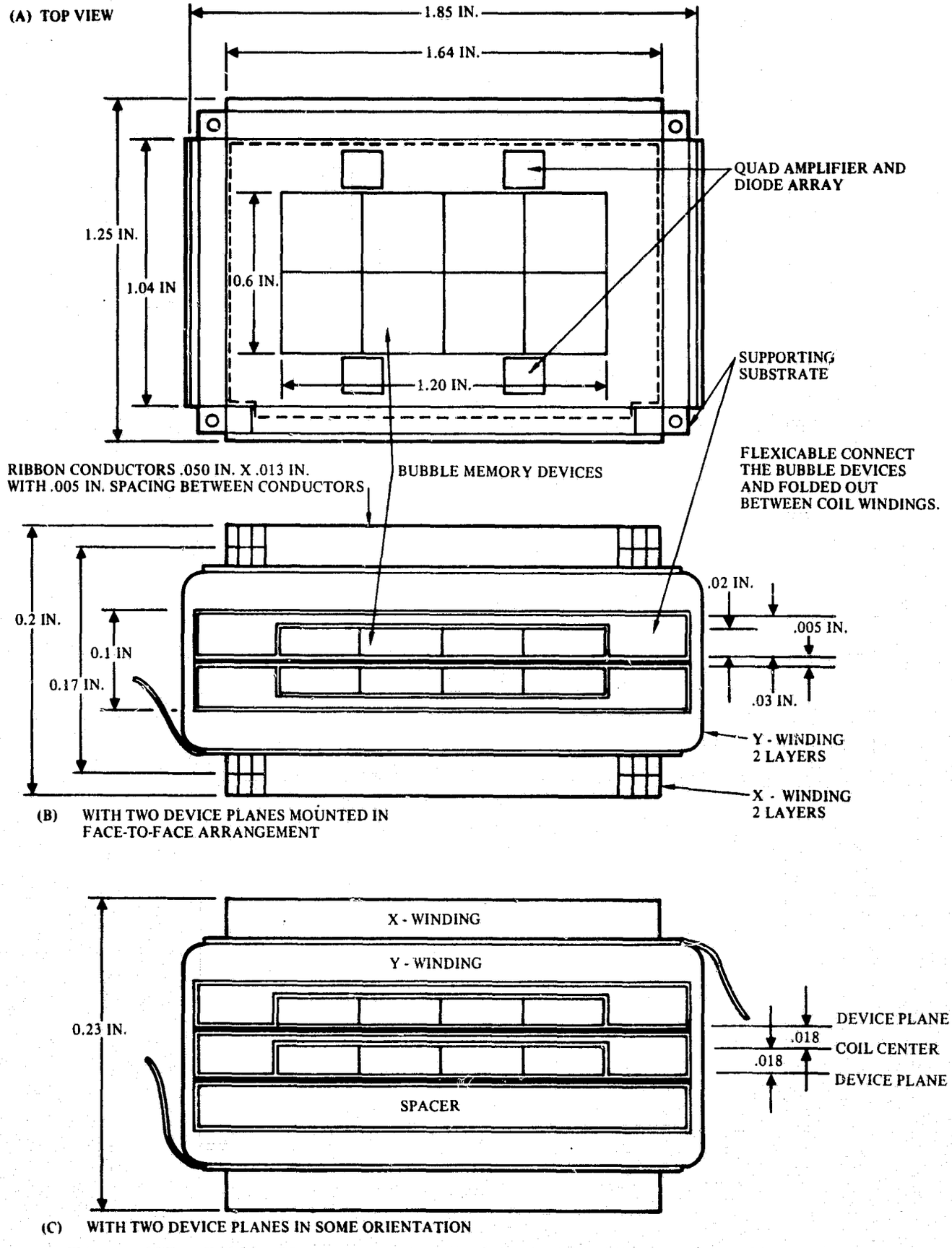


Figure 107. Bubble Memory Device Package and In-Plane Field Coil Set

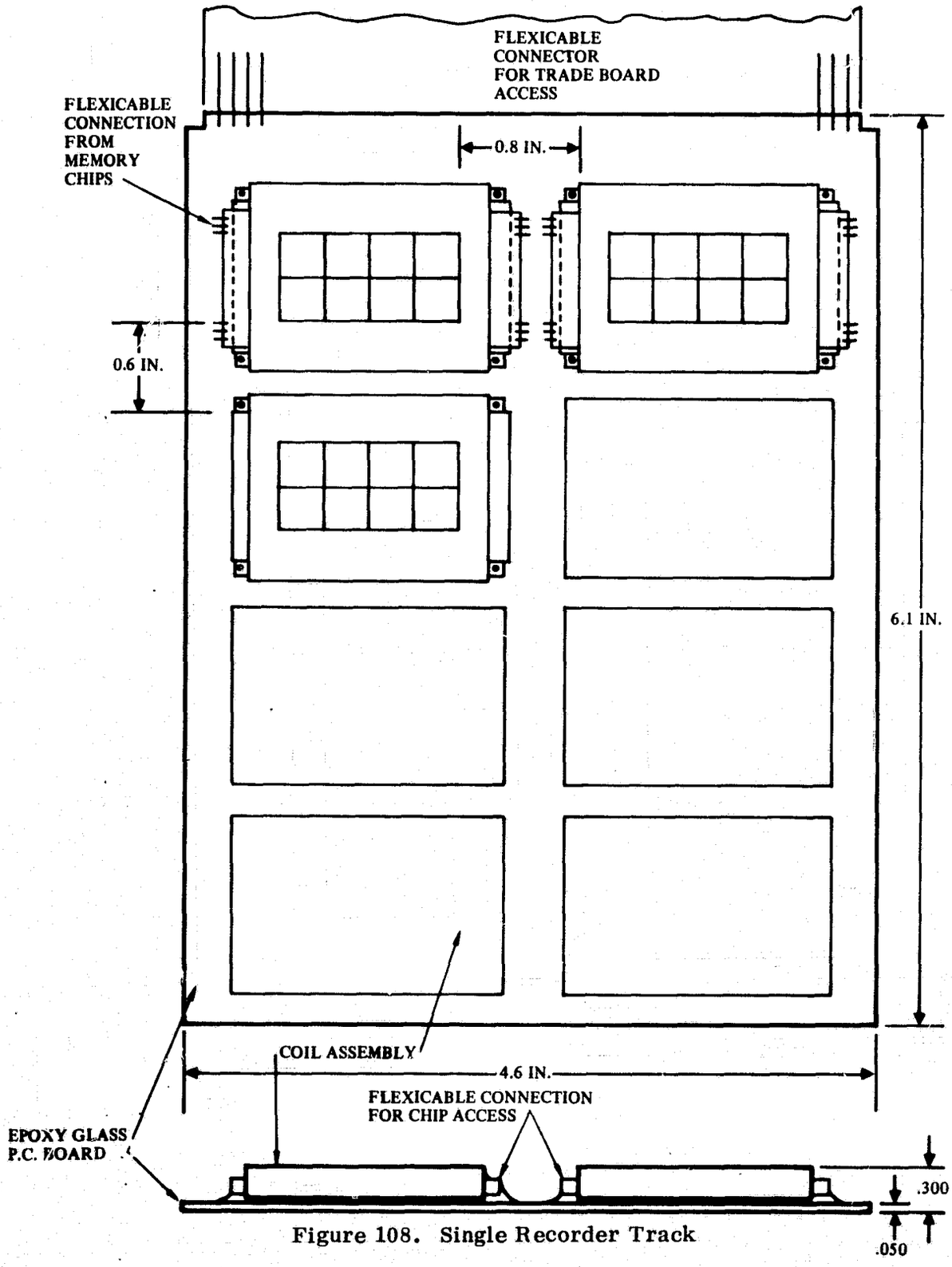


Figure 108. Single Recorder Track

TABLE VI.

IN-PLANE FIELD COIL PARAMETERS FOR PROTOTYPE RECORDER

Coil	Size[i]	$N\ell \cdot N_t$	L[ii]	Rd.c[iii]	K[iv]	Ho	C*/C[v]	$\Delta Hz/Ho$[vi]	P[vii]	Vc[viii]
For the package design shown in Figure 107(b)										
X	0.17 x 1.25 x 1.64 $in.^3$ (0.1 = 0.76 = 1)	2 x 30	14 μh	0.17 Ω	0.95	17 Oe/Amp	0.78	~	0.68 W	26
Y	0.10 x 1.85 x 1.04 $in.^3$ (0.1 = 1.78 = 1)	2 x 19	8 μh	0.15 Ω	0.95	17 Oe/Amp	0.78	~	0.6 W	15
For the package design shown in Figure 107(c)										
X	0.20 x 1.25 x 1.64 $in.^3$ (0.12 = 0.76 = 1)	2 x 30	16 μh	0.175 Ω	0.94	16.8 Oe/Amp	0.75	$<\pm 0.5\%$	0.7 W	30
Y	0.13 x 1.85 x 1.04 $in.^3$ (0.125 = 1.78 = 1)	2 x 19	10 μh	0.155 Ω	0.94	16.8 Oe/Amp	0.74	$<\pm 1\%$	0.62 W	19

(i) Represented as a = b = c according to Figure 47.
(ii) Estimated from Equation (7b)
(iii) Assume $\rho = 1.7 \times 10^{-8}\ \Omega - m$
(iv) Refer to Figure 55
(v) Refer to Figure 50. Assume H/Ho < 10%
(vi) Refer to Figure 52
(vii) Assume 2 amp peak current and Rac/Rdc = 2
(viii) Peak voltage across the coil at 150 kHz

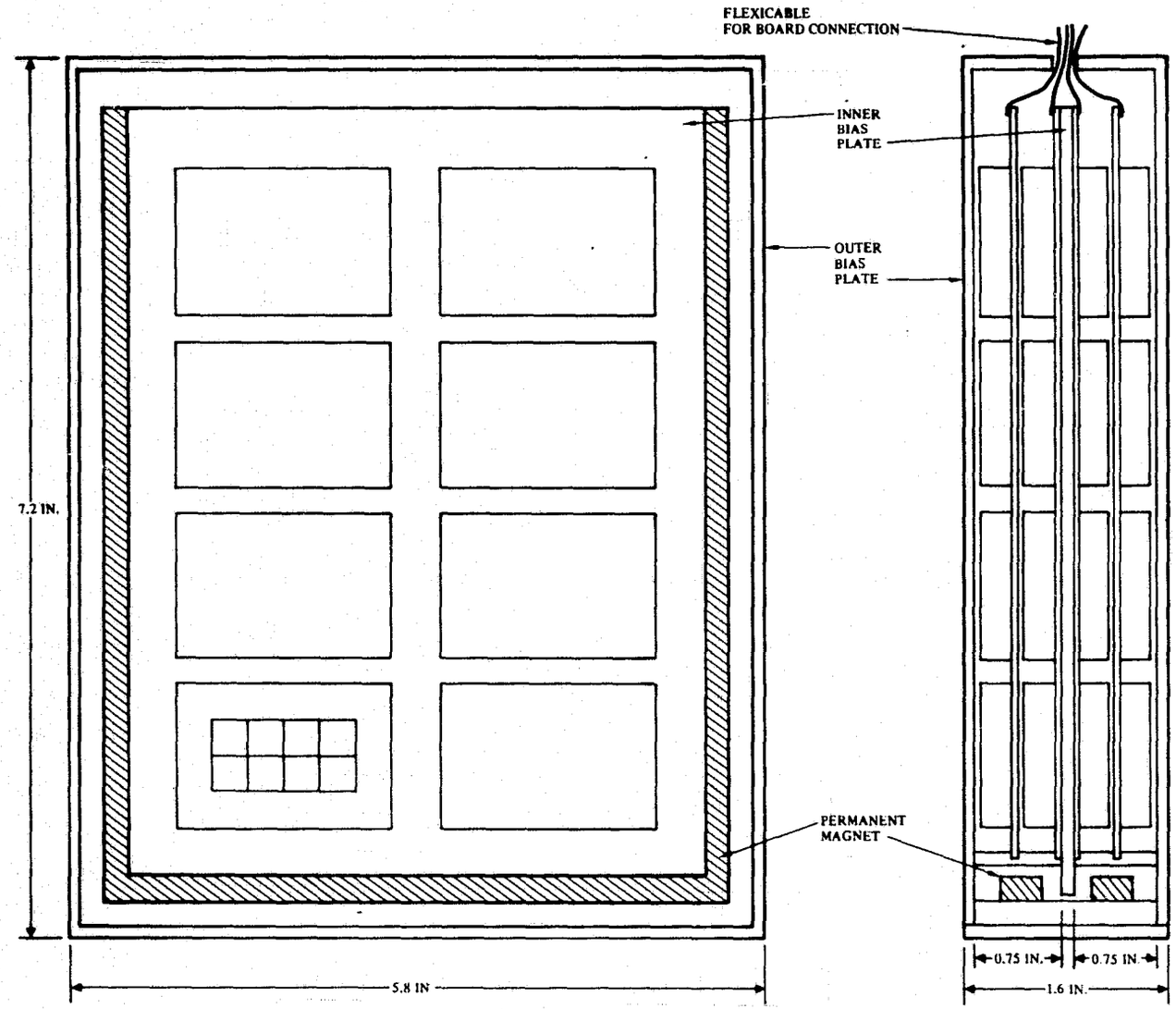


Figure 109. Magnetic Module for Prototype Recorder

9.4 Electronics Estimate

Based on individual circuits designed and tested as part of the Engineering Model study, an accurate cost, power, and reliability model can be organized for a prototype flight recorder. Figure 110 is a block diagram of all four tracks showing interface to each module and to I/O. For the purposes of the electronics estimate the functions are organized according to whether they are associated with the chip, the coil, or the control and timing as shown in Table VII. Factors which control the electronics cost, power, and MTBF are directly affected by design decisions and choices made at the memory element level. For example, the introduction of a new chip function adds a whole new section of electronics for selection, driving, and control.

Sections associated with each function will be summarized as far as parts count, number, interface, and space occupied based upon the electronics design illustrated in the representative schematics. The general attributes of power, MTBF, and price for each section will be summarized for the electrical design from these section by section subtotals.

The following discussion and tables give the study guidelines and the assumptions used to arrive at the recorder's attributes. General guidelines for the proposed concept are taken from the requirements list given in the Statement of Work. Table VIII gives the chip characteristics which are assumed for the baseline estimate. Results of the baseline performance (cost, power, etc) will be covered first followed by a discussion of guidelines and then by the circuit-by-circuit estimate.

The purpose of this estimate is in directing attention to critical design areas, for making relative comparisons between functional sections, in providing a baseline for capacity extrapolations, and in providing an "order of magnitude" estimate of cost for the electronics parts and parts assembly. ABSOLUTE RESULTS ARE ONLY ROUGHLY ACCURATE SINCE THEY DEPEND ON EXTENUATING CONDITIONS SUCH AS PURCHASING DEPARTMENT'S QUANTITY BUY, ON INFLATION, OR ON THE EXACT SPECIFICATIONS TO WHICH THE MEMORY IS BUILT.

9.4.1 Results of the prototype recorder's electrical estimate. — Prototype characteristics (power dissipation, size, etc.) are obtained by assembling the surveys for all the individual circuits (see Table IX). A total of 89 IC's and 361 axially leaded devices which can be sized six to an IC will take approximately 100 sq in. of area when allocating 2/3 in^2 per integrated circuit. Two and one half boards each 6 x 6.5 in. will suffice. The mock-up drawing (Figure 118) shows Dual-in-lines being nested on alternate boards so that the profile is minimized for the total 4 track stack-up of 10 boards. Read and write power will be approximately 1.3 and 1.5 w respectively per track for the electronics. As discussed in Section 4 most of the dissipation is associated with chip and coil drivers. With the recorder on but without rotating field, the idle power will be approximately 500 mw. Standby of course would be zero.

The failure rate for the Hi-rel system is 6.6 failures per 10^6 hr or an MTBF of 150,000 hr and for the low cost system is 1600 failure per 10^6 hr or an MTBF of 600 hr for severe environment operations. These are per track failures so that if any individual track means failure of a mission the MTBF is divided by 4 but if four tracks are operated redundantly the MTBF of the recorder is multiplied by ≈2 (assuming active parallel redundancy).

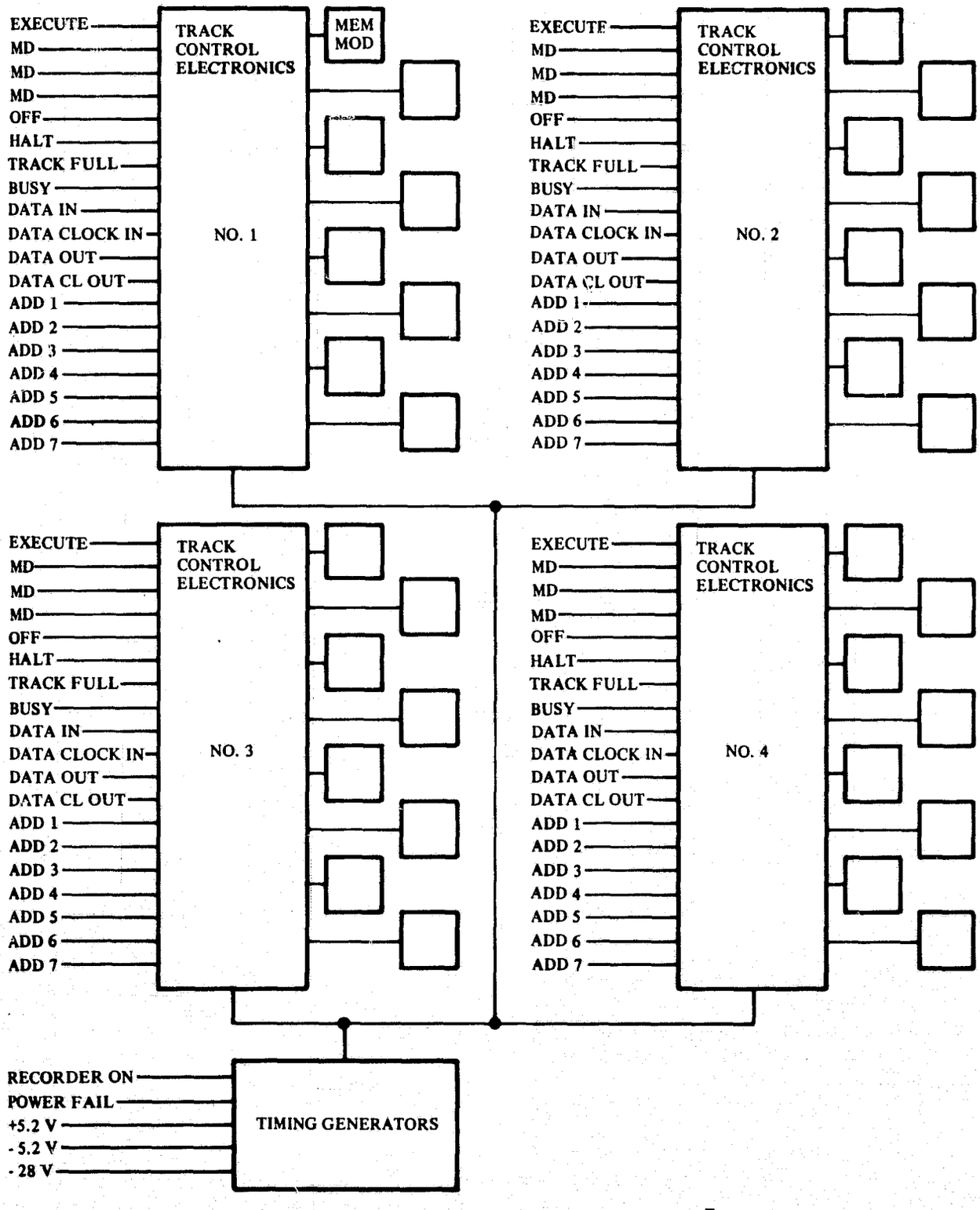


Figure 110. Recorder Block Diagram for a 5 x 10^7 Bit Prototype

TABLE VII.

CONTROLLING FACTORS IN THE ESTIMATE

Memory Element Considerations which Affect Electrical Design	Electrical Design Divisions	Prototype Estimate Results
Detector Output		Power Dissipation Standby, Idle, Read, Write
Number of Functions	Chip Associated Parts	
Functional Current Required		MTBF - Hard Electronics Failures
	Coil Associated Parts	
Functional Timing		
Functional Margins	Control Associated Parts	
Data Rate		Price - Parts Cost, Assembly Cost, Testing Costs
Element Size		

Cost of the electronics including the assembly cost is given in the last two columns and is 5 millicents and 17 millicents per bit for the low cost and Hi-rel versions respectively. Several exercises can now be done to ascertain what specific technique or component use will impact cost and reliability. For example, in Table XV that the estimated labor for winding and testing square loop cores dominates the cost of the control electronics for the low cost approach. Perhaps in non-critical applications, where power is non-interruptable, these cores could be left off the board for economy. Another useful property illustrated by the summary is that the electronics associated with controlling the chip dominates as far as cost or MTBF over control and/or coil associated electronics.

9.4.2 Impact of the Chip Organization

Memory chip capacity. – A question often asked is "how many bits must be included on a chip before the recorder system can be considered economical for a specific application?" To provide a basis for decision, the electronic parts can be assessed vs chip capacity for a constant capacity memory. The approach is to explore the effects of deviating from the baseline 10^5 bit chip estimate by using scaling factors for each circuit (given on the right column of each survey sheet). For example three selection diodes are required per chip so that the number of diodes required for a system varies linearly with chip capacity. Plots for reliability (failure rate per track) and costs are given in Figures 111 and 112.

TABLE VIII.

BASELINE CHIP CHARACTERISTICS

Detector Output	>500 μv
Number of bits	$>10^5$
Number of Control Functions	3
Number of Interface Lines	7
Functional Current Requirements	
Detector	8 ma (total)
Generator	350 ma
Annihilator	150 ma
Functional Impedance	
Detector	200Ω
Generator	<5Ω
Annihilator	<10Ω
Functional Timing	
Detector	25% Duty Cycle
Generator	10% Duty Cycle
Annihilator	20% Duty Cycle
Functional Margin	
Detector	7 ma ± 10%
Generator	380 ma ± 10%
Annihilator	170 ma ± 10%
Data Rate	6.67 μs/Bit
Element Size	0.3 x 0.3 in.

TABLE IX.

SUMMARY OF ESTIMATION RESULTS *
SINGLE TRACK (12 M BITS)

	Quantity	Read (Milli W) Power	Write (Milli W) Power	Idle (Milli W) Power	Connections	Failures Hi-Rel (Per 10^6 Hr)	Failures Commercial (Per 10^6 Hr)	Hi-Rel Cost (Dollars)	OEM Cost (Dollars)
Chip Associated Electronics	329	317	547	154	2008	3.0	880	1451	357
Coil Associated Electronics	150	660	660	100	444	.84	295	252	72
Control Associated Electronics	139	315	315	315	1008	2.8	403	364	164
Totals	618	1292	1522	569	3560	6.6	1578	2067	593
Total No. IC's	89								
Total No. Resistors and Capacitors	361								

*See Electronics Estimate Page 161 for Conditions

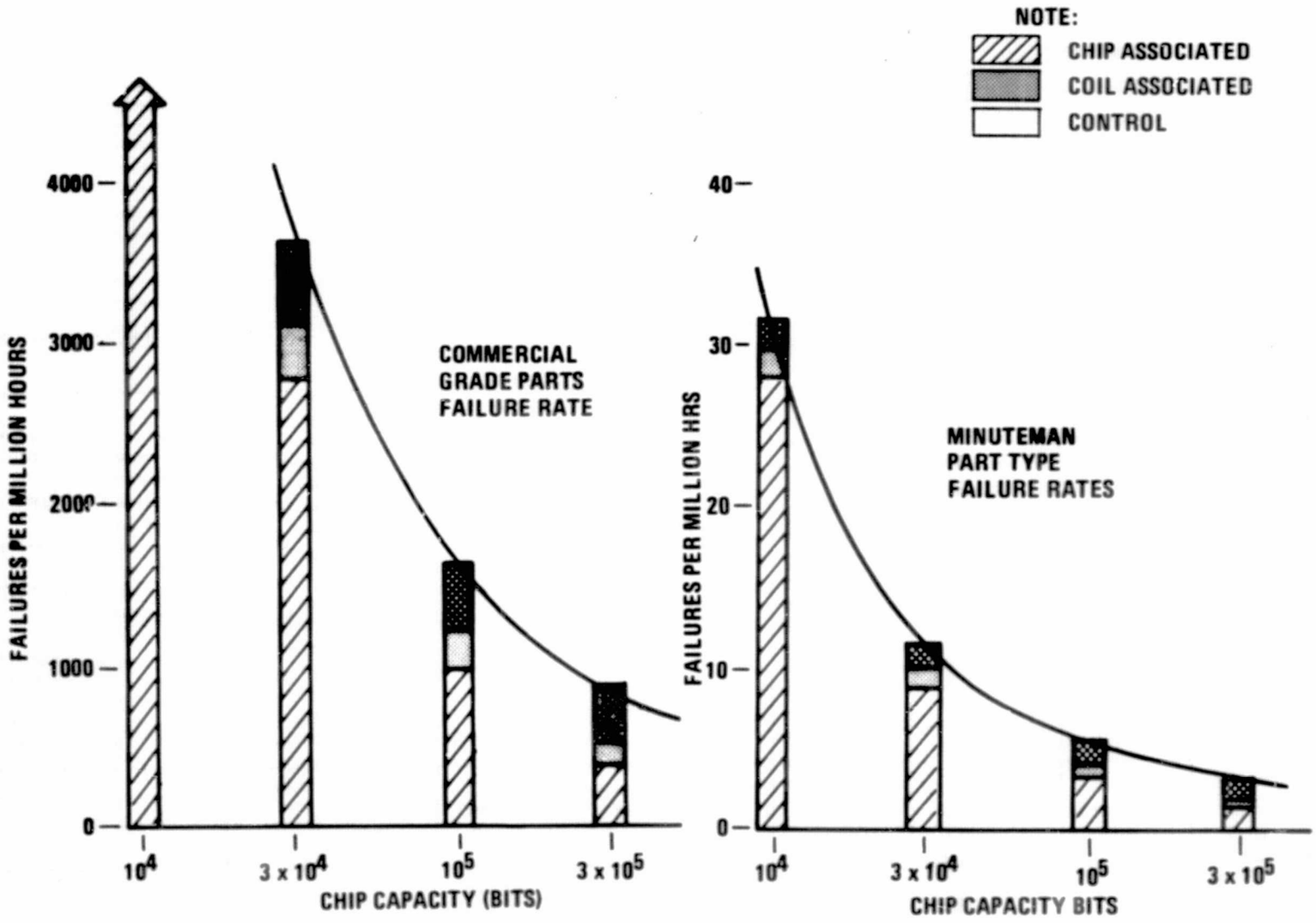


Figure 111. Track Failure Rate vs Chip Capacity
(See Electronics Estimate P-160 for Conditions)

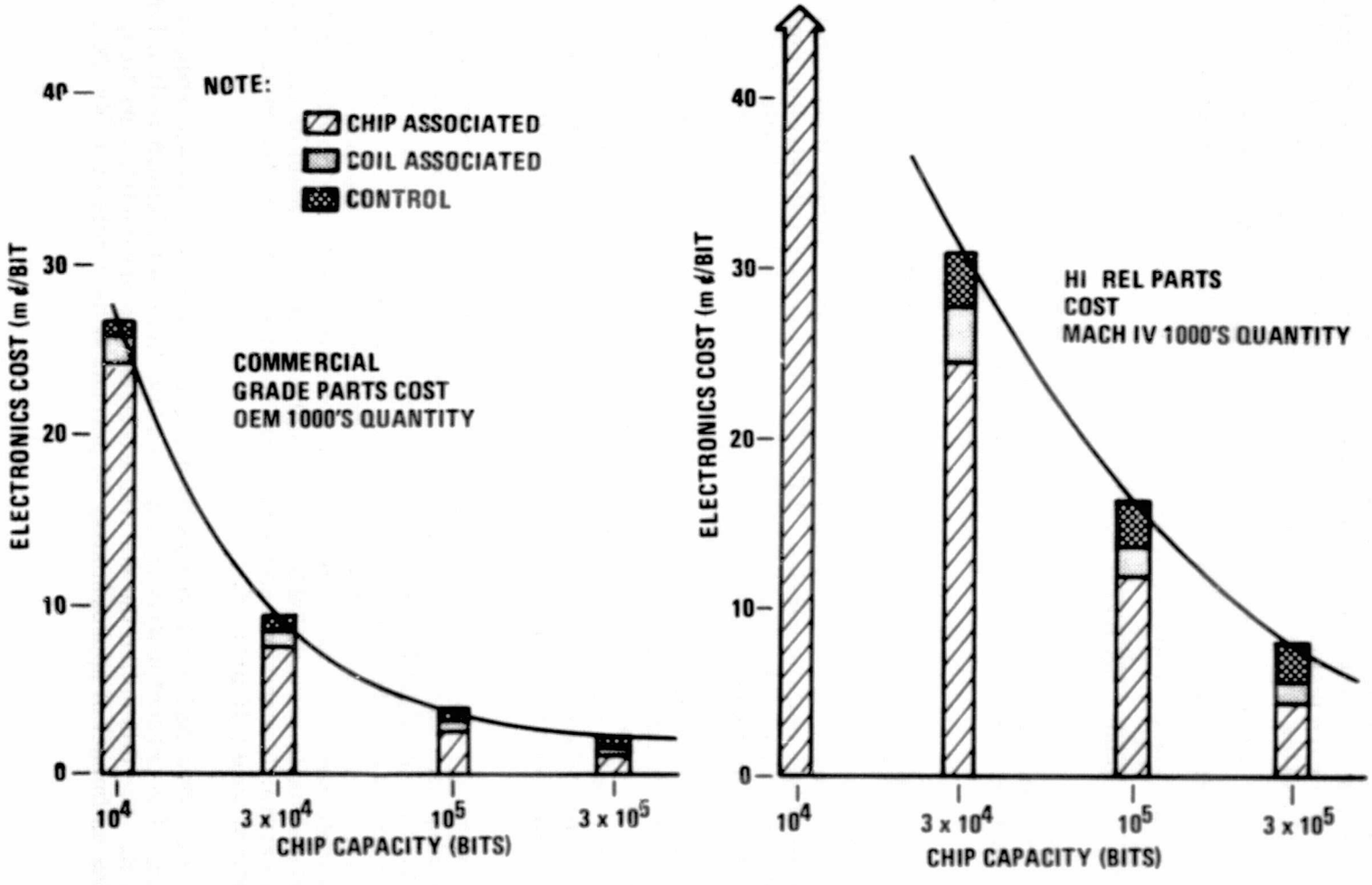


Figure 112. Per Bit Electronics Cost vs Chip Capacity

Core electronics/bubble electronics comparison. — A way to initiuitively understand why chip capacity and chip configuration is important in the recorder design is to compare a core mat of 1024-bits with a bubble memory of 10^6 bits. In the core mat (Figure 113(a)) the amount of electronics for a perfectly squared matrix is 128 selection switches (SS) and one sense amplifier (SA) or $\frac{SS}{128} + \frac{SA}{1024}$ parts/bit. For the 10^6 bubble memory (Figure 113(b)) using 10^3 bit chips the amount of electronics is 4 (32) selection switches (or drivers), 1000 sense amplifiers and about 100 coil drivers $\left(\frac{128\ SS}{10^6} + \frac{SA}{1000} + \frac{CD}{10,000}\right)$ parts/bit).

Notice how the sensing circuit dominates the bubble memory electronics parts count. Depending on relative component costs and for a small 1 K capacity bubble chip, conditions can exist where a core memory will be less expensive than a bubble memory.

Alternate choice of sense amplifier. — The survey of recorder characteristics (size, power, etc.) show that the effect of memory chip capacity and functional choice on electronic circuitry is quite important. For the 10^5 bit chip, the chip associated electronics dominates the coil associated electronics because there are 128 chips per track but only 8 coils to service. Likewise the sensing and detection dominate over annihilate and generator electronics because the circuit complexity of the latter is made up of simple switches. Choice made about the way the bubble signal is detected greatly affect the recorder design outcome. Table X gives a comparison between four choices of amplifier configuration. Besides cost and power, the chief consideration is the ability for moving the threshold to the most optimum voltage for minimum error rate. The fixed threshold of the MC1544 and the open bandwidth appear at present to be a problem. As far as removing all semi-conductors including preamps from the coil (of 16 chips), the number of lines coming out of the package would increase to 86 and space would have to be allocated on the PC board for $\simeq$ 96 in.^{2} for preamps or amplifier.

Alternate chip designs. — Other chip designs are being considered on other programs, such as the one of Figure 106, where the annihilator, generator, and detector are all aligned by using a guardrail detector and passive replicators. Another annihilator is required per chip to annihilate every other bit before they enter the detector. A way to assess the impact of this proposal on the estimate is to consider the new element as an additional annihilator connected to the matrix. In the chip associated parts survey (Table IX) the increase in parts would be approximated, 10 diode arrays, 30 resistors and 4 quad transistors. Cost of electronics would increase by approximately 10 percent.

An active replicator (presently using a bipolar current) will require a separate matrix. The present matrix concept is a one diode per element matrix for unipolar current. For this option the matrix, excluding the preamplifier portion, is doubled causing an impact of approximately 30 percent to the totals of Table IX .

TABLE X.

SENSING OPTIONS

	AC Coupled Motorola MC1544 Amplifier	Individual CA3005 Preamps	CA3005 Diced into Quads from Purchased Wafers	Developed 4 Channel Preamps
Unit Cost 1000's OEM	3.50/Channel	2.00	1.50	10-20
Delta Cost/Bit Over Estimated	3 m¢/Bit	1.5 m¢/Bit	1.0 m¢/Bit	20 m¢/Bit
Interface Lines Out of Coil	33	23	23	23
Recorder Volume Impact	(0) Chips are in Now Linear Field Region	(0)	(0)	(0)
Sensing Chips within Coil	4	16	4	4
Unit Power + Bridge Power	64 Milliwatts	7 Milliwatts	7 Milliwatts	7 Milliwatts
Chief Disadvantages	1 Cannot adjust bandpass of amplifier 2 Difficult to adjust threshold to accommodate signal. Restricts detector design. Cannot accommodate systematic noise riding on baseline. 3 Must select units for threshold.	1 Extra connections required inside of the package to buss preamplifiers together.	1 Same as individual preamps.	1 Too costly to develop especially on initial small quantity programs.
Chief Attributes	1 Approved for NASA Space Applications (Vikins)	1 Designed especially for bubble signals. 2 Can accomodate future detector signal designs. 3 Can evolve with improvements of detector. Connection to bridge reduces connections.	1 This is an interim between individual chips and monolithic version. 2 This will accomodate changes in detector design. 3 This is a step in an evolutionary development process.	1 Interface is simple. Also other functions such as the selection diodes could be part of the chip. Ideally what would be useful is a memory service semiconductor chip.

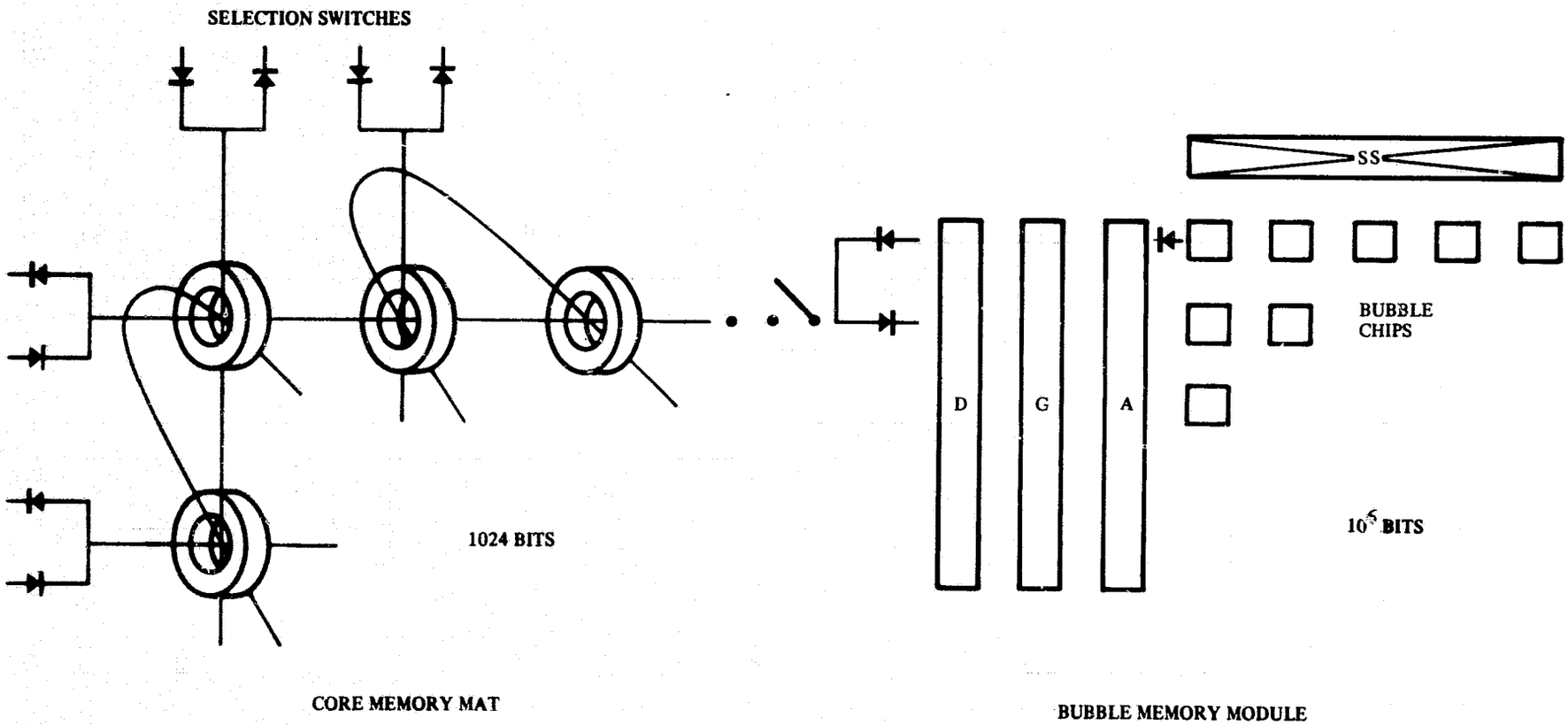


Figure 113. Core Memory Mat Compared with a Bubble Memory Module

9.4.3 Estimation Guidelines

Estimating Procedure. – The basis of the electrical design estimate is first the identification of circuitry similar to prototype circuitry and second the partitioning of the electrical design into small circuits that can be individually analyzed. By analyzing small divisions the estimation errors become small and randomized between optimistic and pessimistic. Each circuit's parts are surveyed according to parts quantity, power dissipation, failure rates, and cost. This survey is given in Tables XI and XII. Connection failure rate and assembly cost are added separately but appear in the final tally. A scale factor was determined for the parts of each circuit which is a factor by which the difference in chip capacity affects parts quantity. For example, if the chip capacity is 10^6 then the quantity of selection diodes drops by 10 for a constant capacity memory.

Failure rates. – Two sets of failure rates will be used so that the cost of reliability can be relatively assessed. One kind of application is assumed to be a commercial like secondary system which is required for a short period of time in a severe environment but in a situation where failure won't jeopardize human life of a mission. Remote monitoring such as in a sesimograph or telemetry backup in a secondary rocket are examples of this kind. Components are commercial grade operated continuously at 50°C with a missile application factor applied for the continuency of vibration and shock. The other set of rates is for applications where failure would be catastrophic to a mission such as for a computer program store or for missile guidance. Components are military Hi-rel grade (TI's Mark II or MIL-STD-883) with Minuteman rates applied with a 20 percent average stress, 40°C temperature, and for field use. Table XI gives the rates (mostly from Mil Handbook 217A) used throughout the study. A failure is defined as an open, short, or parameter change greater than the specified tolerance.

The primary reasons for looking at these two widely divergent sets of failure rates are these. In the first instance the application is a low cost one where the unit could be repaired, if it fails and the question is "how long before repair is required for severe use?" In the second instance the unit is too remote for repair or is critical to a mission so that the user of the recorder is forced to provide less stringent environment and is forced to use Hi-rel parts. As discussed in the section of Electronic Design, the goal of the design is to configure the recorder so that reliability can be upgraded without fundamental design changes so as to be able to fit a wide range of applications.

Power dissipation. – Power dissipation is estimated for the three conditions of read, write, and idle where idle is the condition where the recorder is on with the sequence logic operating but without rotating field on. Read power or write power is the maximum power dissipated in performing a required function assuming continuous operation. Power dissipated in integrated circuits is the maximum specification value modified by the duty cycle if the device is being switched. In the case of diodes, resistors, or transistors, the maximum voltage and maximum current is assumed but situations where semiconductors are in series with resistors occur which have to be treated so that the series network power is maximized. Judgement is in some cases necessitated by the work required to identify precise timing, currents and voltages.

TABLE XI.

FAILURE RATES (PER 10^6 HR)

Circuit Element	Maximum 0 - 0.8 Stress 50°C Missile Application (K)	Minimum 0.2 Stress 40°C Field Use
Microcircuit (existing with history)	4	. 01
Microcircuit (exceptional, developed, or hybrid)	8	. 02
NPN Quad Transistors Non op/op	2.5/10	. 028
PNP Quad Transistors Non op/op	5.0/30	. 028
Individual Diodes (Including zeners)	4	. 002
MIL-R-22684 Resistors	1.6	-
MIL-R-55182 Level P Resistors	-	. 003
Ceramic Capacitors MIL-C-11015	.6	. 003
Solid Tandulam Capacitors MIL-C-39003 (Level M)	3	-
Solid Tandulam Capacitors MIL-C-39003 (Level S)	-	. 003
Connections[2]	. 003	.0003
Passive Core CKT (estimated)[3]	2	. 02

(1) From Mil Hdbk 217A

(2) From RADC data

(3) High-Rel Pulse Transformers = .02 from RADC

TABLE XII.

ASSEMBLY AND PARTS COSTS (1000 QUANTITY)

	Minimum Class C OEM Price	Maximum Minuteman Grade Mark IV TI Catalog Price
Simple Gates and Flip Flops	.50	2.50
Medium Scale Integrated Ckts	2.00	10.00
Developed Microcircuit	5.00	25.00
Quad Transistors	3.00/png	15.00
Resistors	.15	.50
Ceramic Caps	.15	.50
Tandalum Caps	1.00	2.00
Preamp Chips	2.00	10.00
Diode Arrays (ea)	3.00	15.00
Sense Amplifiers	1.50	7.50
Flexible Cables	10.00	30.00
Electronic Assembly and Inspection (5 sec/bond at $10/hr)	3 ¢/bond	3 ¢/bond

Assembly and parts cost. — Prices of components used in this estimate are from 1973/74 manufacturers price lists for 1000 quantity (OEM for the commercial grade, MARK IV for Military Hi-rel IC's) and from catalog prices (Cramer) according to the Military part number. The reason for using these prices is two-fold. First they identify the costly areas of the design for the electronics and secondarily they roughly establish how big the chip must be before the electronics costs becomes insignificant. In most cases the price is available but in a few cases an estimate was required. The basis for assembly cost is the labor required to install each pin of the components and is assumed to be 5 sec/pin at $10.00/hr.

9.4.4 Circuit-by-circuit estimate. — This section is a survey of circuit performance in terms of power dissipation, cost, etc. The electronics is divided into 3 functional catagories and these catagories are further divided into individual circuits which are evaluated.

Chip associated parts. — Chip functions such as annihilation, generation, and amplification require more piece parts by far than either the coil drive section or the control section and as such contribute disportionately to MTBF and cost. The concept assumed is one which will use the 100,000 bit single register chips connected by a power selection matrix for all three functions as shown in Figure 114. Since 128 chips are required per track, organized 16 per coil assembly, an 8 x 16 line diode matrix is conveniently used for function and chip selection. The function of the top switches will be to apply voltage to individual chips within each coil while the function of the bottom switch is to perform a function on only the chips in one coil package. Only 16 top switches are needed and 24 function switches are needed one for each function. The important feature of this baseline concept is the matrix given in Figure 114 where the three functions of annihilator, generator, and detector share the same selection switches. Diodes and preamplifiers are located within the coil so that advantage may be taken of busing the outputs together to reduce interface lines to the electronics board.

Furthermore by using these components in chip form instead of in packaged form, the volume requirement is greatly reduced. Within the coil there exists an area around the edge where the field is non-uniform so that semiconductor chips can easily be placed there without impacting coil design considerations. The diode selection is typical of selection schemes found in plated wire and core systems and the differential amplifier arrangement was one of the first linear IC's made but concern exists over the cost of special preamplifier chip development if required for immediate programs.

Figure 115 is a preamplifier chip design that would simplify interface and reduce component count inside the coil package. It is four CA3005's on a chip with the selection diodes and bridge completion resistors. Figure 116 is a block diagram of the circuitry between the preamplifiers and the output data latch. A summary of circuit characteristics (parts count etc.) is given in Table XIII for the circuits described above.

Coil associated parts. — The basis for this part of the estimate is the Engineering Model Driver circuit with a separate selection switch for each coil set (see Figure 117). The components used are representative of the quantities and types required of a prototype design. The driver was tested in the Engineering Model but the whole coil matrix and the selection switch was not. Actually a FET Selection Switch (with low R_{on}) or a MOS monolithic analog switch would be more efficient for selection except that the technical ramifications of such a design haven't been explored. Table XIV is the count, power, and failures per 10^6 hr for these circuits.

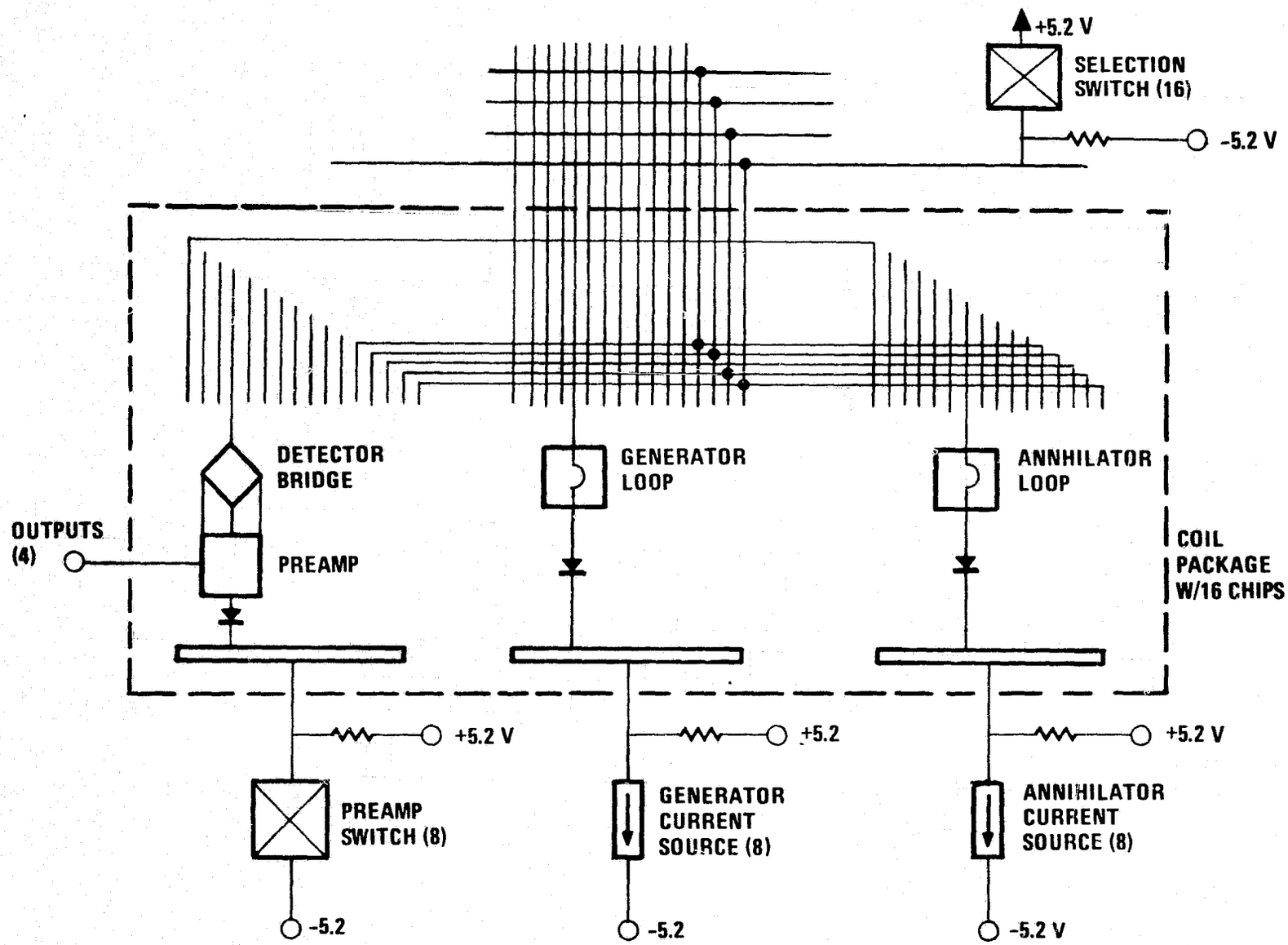


Figure 114. Selection Matrix for Chip Associated Electronics

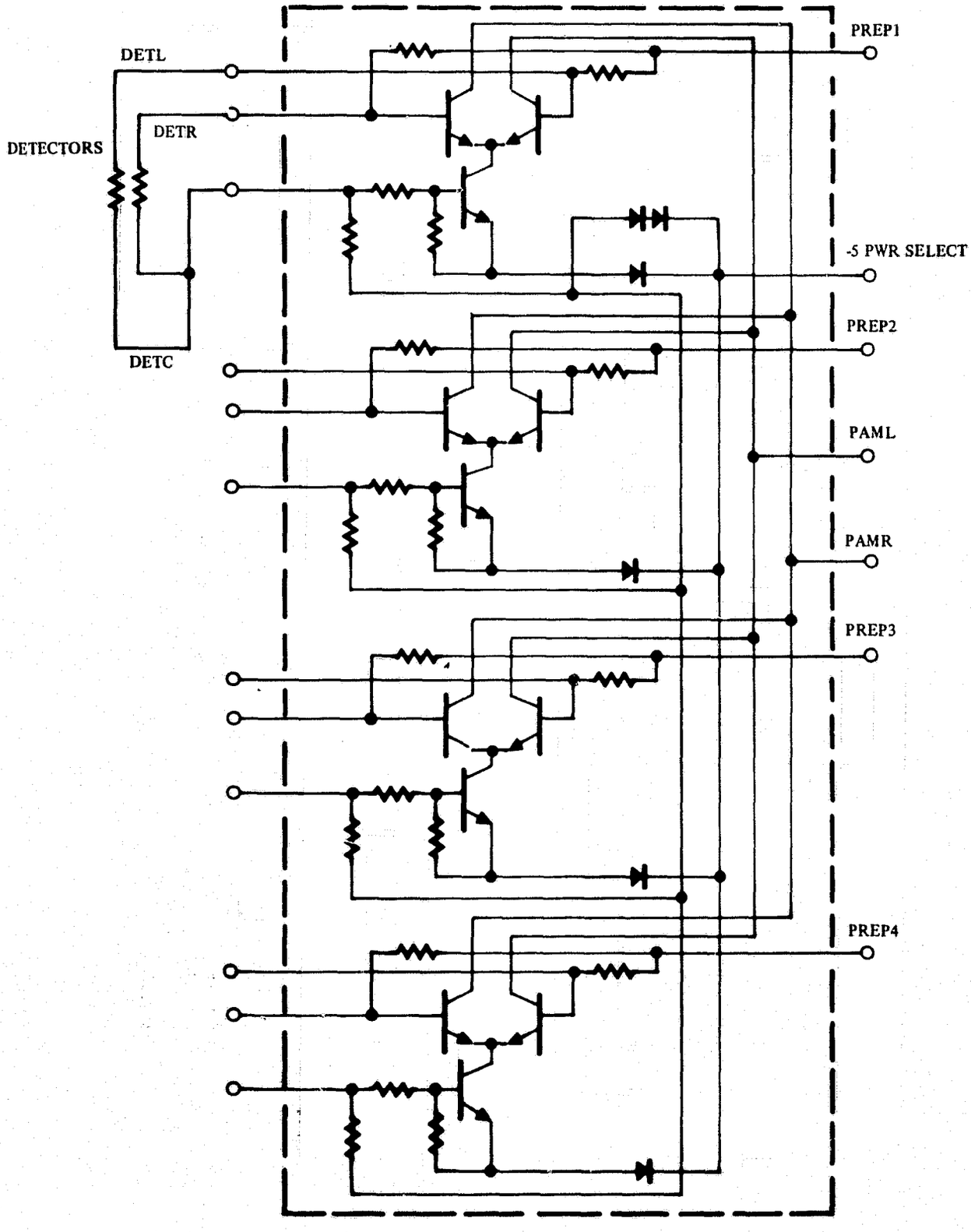


Figure 115. Four-Preamplifier Chip (4 CA3005 Amplifiers on a Chip)

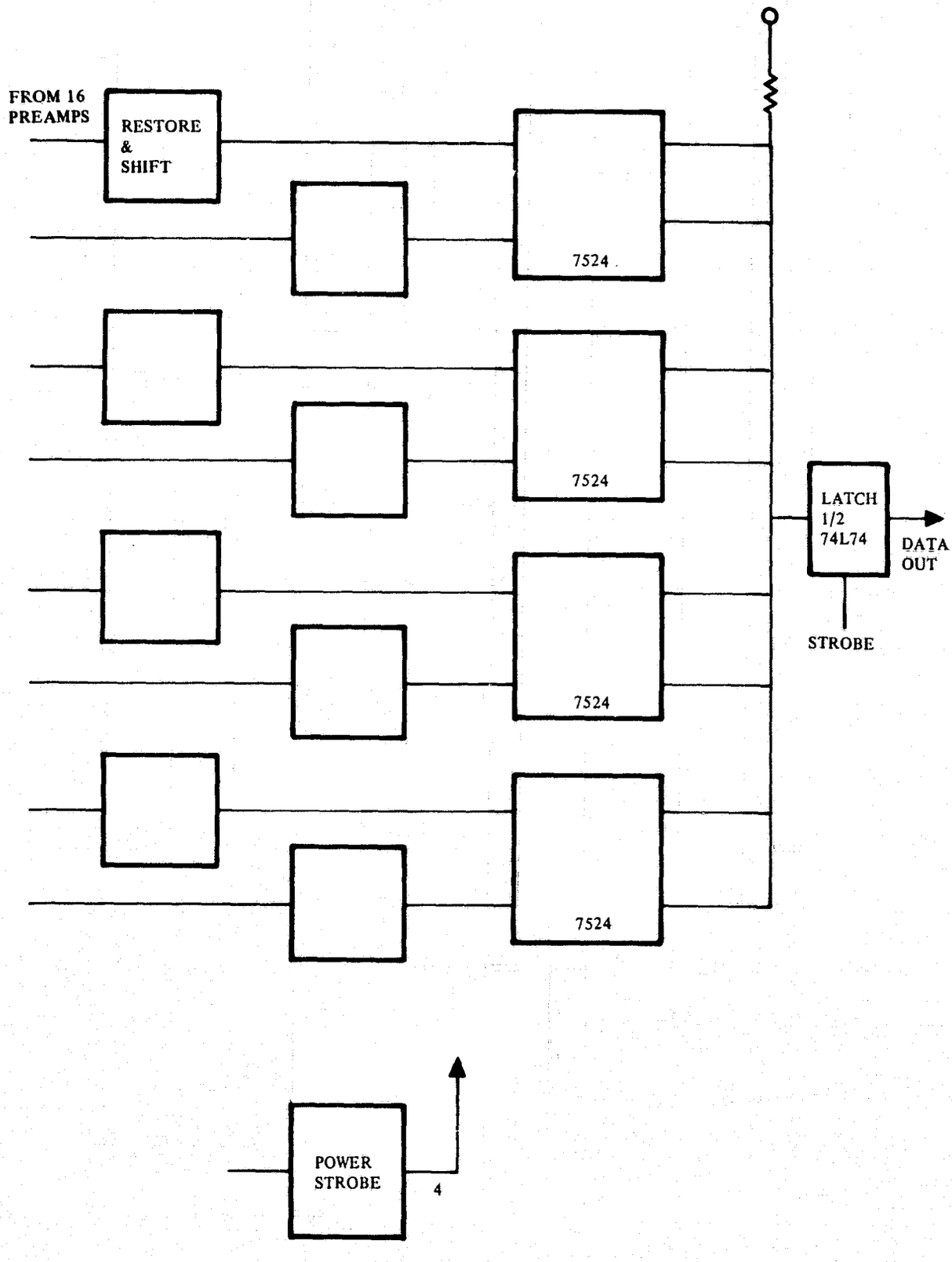


Figure 116. Signal Detection Block Diagram (Single Channel)

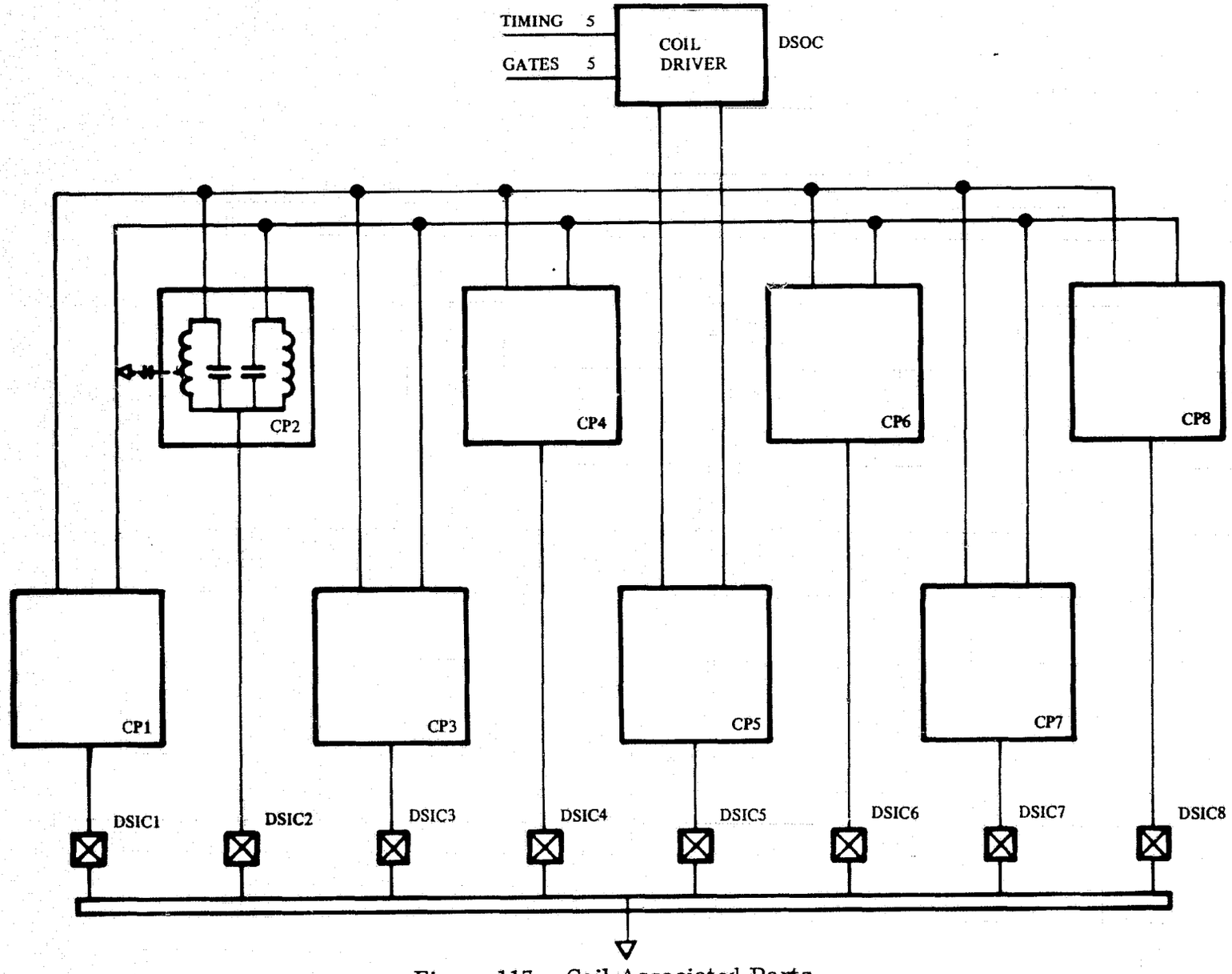


Figure 117. Coil Associated Parts

TABLE XIII.

CHIP ASSOCIATED PARTS (PER TRACK)

Description	Part Number	Quantity	Mill W Read Power	Mill W Write Power	Milli W Idle Power	Connection and Type	X10^6 Hr Failures (MM)	X10^6 Hr Failures Class C	Assembly and Test Cost $	Hi Rel Cost $	OEM Cost $	Scale Factor
8 Diode Array	FSA1410 or TID 2X	32	1	50	-	288 (TC)	.32	128	8.64	480	96	
Resistors	22684 or 55182	1/4	80	150	-	388 (Solder)	5 x 8	310	11.64	97	29	$\frac{\eta}{2}+\sqrt{\frac{\eta}{2}}$
Preamps	Developed	32	10	-	-	608 (TC)	.64	256	18.24	320	64	
Decoders	MC14515	3	110	110	110	52 (S)	.03	12	1.56	30	6	
PNP Quads	2907	12	33	33	-	168 (S)	.34	60	5.04	180	36	
NPN Quads	2222	12	4	150	-	168 (S)	.34	30	5.04	180	36	
Flex Circuits	Developed	8	-	-	-	184 (S)	-	-	5.52	32	16	
Gates (SSI)	7400	1	50	50	40	14 (S)	.01	4	.42	2.50	0.50	
Sense Amps	7524	4	25	-	-	64 (S)	.04	16	1.92		6.00	
Data Latch	74L74	1	4	4	4	14 (S)	.01	4	.42	2.50	.5	1
Ceramic Capacitors	MIL-C-11015	15				30 (S)	.04	9	.90	7.50	2.25	1
Tantalum Capacitors	MIL-C-3900	15				30 (S)	.04	45	.90	30	15	1
Subtotals		329	317	547	154	2008	.6	6	60.	60.	60.	
Totals		33 ICs 194 resistors 30 caps					3.0	880		1451	357	

TABLE XIV.

COIL ASSOCIATED PARTS (PER TRACK)

Description	Part Number	Quantity	Milli W Read Power	Milli W Write Power	Milli W Idle Power	Connection and Type	x 10^6 Hrs Failures (MM)	x 10^6 Hrs Failures Class C	Assembly and Test Cost $	HI Rel Cost $	OEM Cost $	Scale Factor
Medium Power Gates	7420	3	160	160	100	42 (Solder)	.03	12	1.30	7.50	1.50	$\sqrt{N}$
PNP Quads	2907	4	200	200	-	56 (Solder)	.11	22	1.70	60	12	$\sqrt{N}$
NPN Quads	3725	6	100	100	-	72 (Solder)	.17	18	2.20	90	18	$\sqrt{N}$
Resistors	22684 or 55182	121	200	200	-	242 (5)	.36	194	7.26	61	18	$\sqrt{N}$
Ceramic Capacitors	MIL-C-11015	8				16	.02	24	.5	4.00	1.20	1
Tantalum Capacitors	MIL-C-39000	8 8				16	.02	24	.5	16	8	1
Subtotals		150	660	660	100	444	.133	1.33	13.5	13.5	13.5	
Totals							.84	295		252	72.2	
		13 IC's 121 Resistors										

Control Electronics. – A variety of control is required for the drivers and amplifiers in order to produce the several modes of operation such as read or write. Gating and decoding provides the gate signals which control when timing is provided to the current sources from the timing board. Power switching supplies power to only the section in need. Track operations keep count of the elapsed field rotations; Byte operation provides acceptance of asynchronized input data; and the data control section provides the threshold detection and clocking out of the data. The circuits used in this estimate are the Engineering Model circuits with adjustments to quantity where applicable for the prototype. Table XV is the summary of parts count, power, and reliability.

9.5 Prototype Description

The summarized data from previous sections lead to the concept design for a 5×10^7 bit 4 track recorder as illustrated in Figure 118. A cold plate in the middle provides mechanical support for the magnetic module on one side and the 10 electronics boards on the other side connected together in a zig-zag configuration to allow assembly and testing. Table XVI gives the characteristics of this prototype design.

As compared with the design goals shown in Table V the recorder size is within the design goal but the weight is 50 percent higher. This is primarily due to the magnetic module (5.5 lb) where heavy bias plates are used (3 lb). The weight due to the copper conductor in the coil winding is also significant (2.2 lb). Therefore, the bubble memory package alone will exceed the 8 lb goal. Some improvement can be made by increasing the coil capacity thus reducing the module size. This will further increase the power dissipation which is not very desirable.

The power dissipation is twice the design goal when four tracks are operated in parallel. The main power dissipation is from the coil driver and the coil (about 2 w per track) which can be minimized by reducing coil size. But this will be a direct conflict with the weight and size requirement. Another alternative is to share four tracks with a single coil set which can lower the power dissipation to 5 w for four tracks. In this arrangement the four tracks cannot be operated independently any more. In order to achieve the expected design goal shown in Table V further research and development efforts have to be made in bubble memory technology, such as smaller bubble size to reduce the overall package size and wieght, faster bubble speed so that the device can be operated at lower duty cycle, or using self biased material (Ref 28) to eliminate the bias structure, etc.

TABLE XV.

CONTROL ASSOCIATED PARTS (PLUS 1/4 OF SEQUENCER ELECTRONICS)

Description	Part Number	Quantity	Milli W Read Power	Milli W Write Power	Milli W Idle Power	Connection and Type	x 10^6 Hr Failures (MM)	x 10^6 Hr Failures Class C	Assembly and Test Cost $	Hi Rel Cost $	OEM Cost $	Scale Factor
Lower Power Gates	74L00 etc	20	75	75	75	75 (S)	.2	80	8.4	50	10	$\sqrt{N}$
Med Power Gates	7400 etc	2	16	16	16	28 (S)	.02	8	.84	5	1	$\sqrt{N}$
Med Scale Int Ckts	L192 L95 etc	11	200	200	200	176 (S)	.22	88	5.3	110	22	1
Simple Flip Flops	74L74 etc	6	24	24	24	84	.06	24	2.5	15	3	1
PNP Quads	2907	3	-	-	Pwr Down	42	.08	7.5	1.26	45	9	1
NPN Quads	2222	1	-	-	Pwr Down	14	.03	5	.42	15	3	1
Square Loop Cores	Special	96	-	-	Pwr Down	384	1.9	192	96	9.6	.96	
Subtotals		139	315	315	315	1008	.3	3	115	115	115	
Totals							2.8	403		364	164	

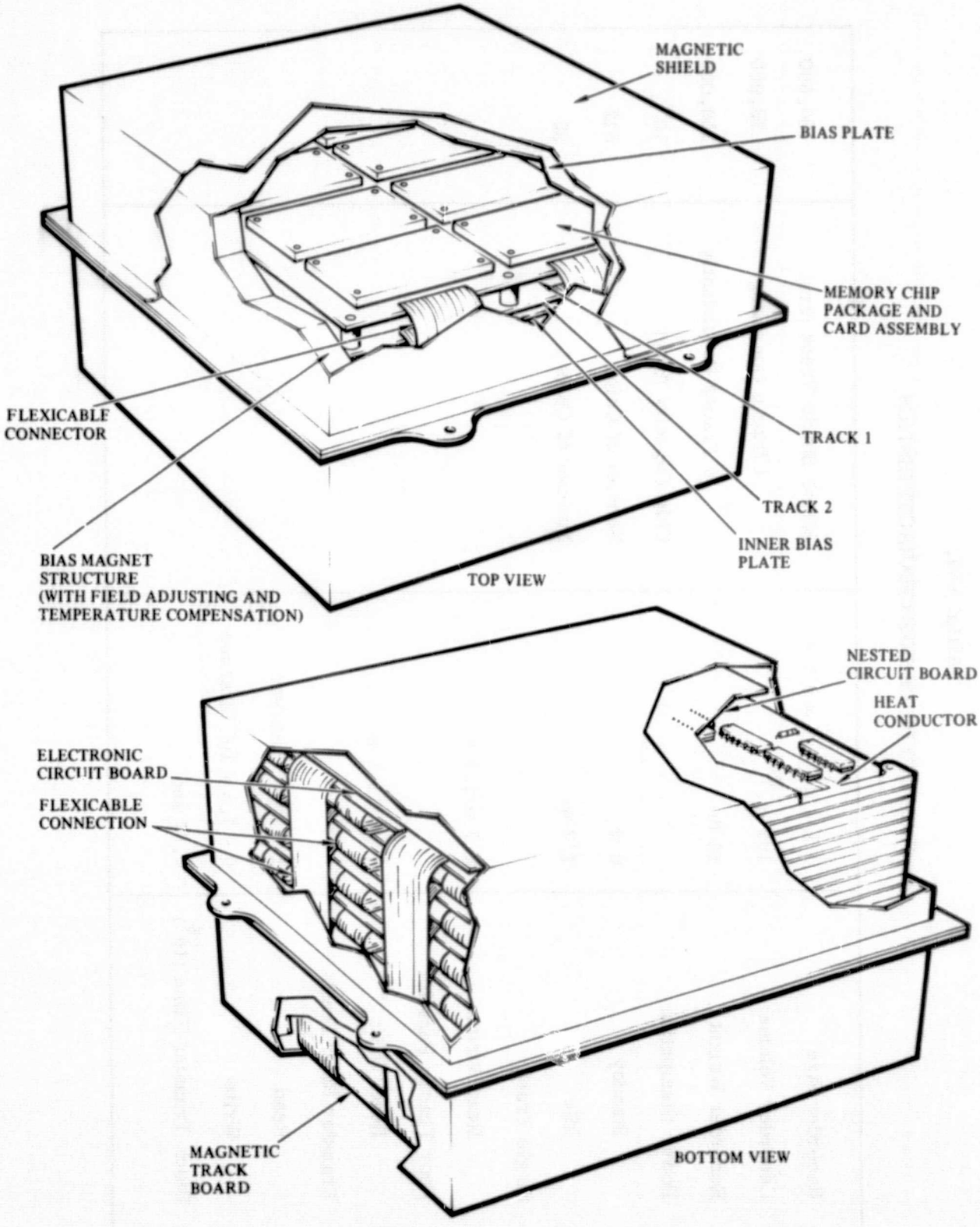


Figure 118. Prototype Bubble Recorder

TABLE XVI.

PROTOTYPE DESIGN CHARACTERISTICS

Recorder Size	4 1/4 x 7 1/4 x 6 1/4	MTBF Single Track (hrs)	150,000
Recorder Volume	192 $in.^3$	4 Tracks Operating	33,000
Recorder Weight	12 lb	4 Tracks Redundantly	350,000
Power Dissipation		Chip Capacity (bits)	10^5
Standby	0 w	Number of Chips	512
Idle	1/2 w	Number of Coils	32
Single Track			
Read/Write	2.7 w/2.8 w		
Four Tracks Parallel			
Read/Write	11 w/11.5 w		
Transfer Rate/Track			
Read	1.5×10^5 bits/sec		
Write	$0 - 1.5 \times 10^5$ bits/sec		
Block Transfer Time (10^5)	0.67 sec		

10. ENGINEERING MODEL EVALUATION

This section summarizes the test results on the Engineering Model. These results are divided into three categories: the memory chip performance, the magnetic module characteristics, and the recorder system operation as a unit. Emphasis for the chip level tests was on operational characteristics including propagation, generation and annihilation margins, and detector signal waveforms and their variation among different chips. The testing temperature was between 0 and 50°C. The magnetic module evaluation emphasised the leakage magnetic field and temperature characteristics between 0 and 50°C. The overall performance of the recorder is summarized in Para 10.3. Error rate measurements were performed between 0 and 50°C and a nonoperating data retention test was extended between -25 and 85°C. The basic operating frequency was 150 kHz but the device was operated in a gated mode with an effective data rate between 1 kHz to 40 kHz. The long term reliability problem of the bubble memory chips are being studied under an in-house program. Some of the results on present memory chips will be discussed in Appendix C for the completeness of the device evaluation.

10.1 Memory Element Evaluation

10.1.1 Memory chip operating margins. - Eight 10K bit memory chips were mounted in four separate ceramic ("butterfly") packages for the engineering model. Three of them were assembled in the magnetic module and the last one was used as a spare. Two types of garnet bubble materials $(YEuTm)_3(GaFe)_5O_{12}$ and $(SmY)_3(GaFe)_5O_{12}$ were used for chip fabrication. The material characteristics are shown in Table XVII. The processing procedures for these chips are identical to those discussed in Para 8.1.

Propagation Margin. - The propagation margins of these devices are shown in Figure 119. Both the continuous operating margin at 25 kHz and the gated operating margin (eight steps at a time) at 150 kHz are plotted for comparison. The margins were taken with a laboratory model bubble domain memory exerciser (Ref 29). With the chips mounted in the ceramic packages and with the rotating field generated either from an open coil structure (see Para 5.2.3, Figure 72) for 25 kHz operation or from the windings on the package for 150 kHz operation. Measurements were taken by varying the bias field value under several fixed rotating field values. Margin boundaries were determined by visually observing a few word patterns (out of 1280 words in the register) for several memory cycles. The MSBF (see Appendix C) so determined is about 10^{-5}.

All of the chips tested had a bias margin of about 10 Oe for a 50 Oe driving field. However, this margin narrows down substantially at 150 kHz gated operation. The minimum driving field also increases from 35 Oe to about 45 Oe. This margin degrading is believed to be caused by the nonuniformity in the permalloy propagation pattern. Weak poles in the propagation path, due to wide gaps or skinny bars, will not stop the bubble propagation or cause catastropic failure but will increase the failure probability and degrade the reliability of the circuit (Ref 30). This effect can be partly compensated by introducing a holding field (through device tilting in the bias field) in the device plane which enhances the pole strength (Ref 18). In cases, such as butterfly 13, the gated operating margin is very narrow thus the tilting of the device plane in the bias structure is very critical in order to achieve a reasonable reliability.

C-3

TABLE XVII.

MATERIAL PARAMETERS OF THE DEVICES USED IN THE ENGINEERING MODEL

Track No.	Package No.	Wafer	Composition	h(μm)	w(μm)	4πMs(gauss)	ℓ(μm)	σ_w(ergs/cm^2)	H_{coll}(Oe)
1	15	2-16-87	$Y_{1.57}Eu_{0.78}Tm_{0.65}$	5.66	6.21	209	0.712	0.261	103
3	13		$Ga_{1.05}Fe_{3.95}O_{12}$						
2	7	2-16-89	$Y_{1.57}Eu_{0.78}Tm_{0.65}$	5.11	6.14	215	0.754	0.262	93.2
			$Ga_{1.05}Fe_{3.95}O_{12}$						
Spare	17	2-18-28	$Y_{2.62}Sm_{0.38}Ga_{1.05}$	6.47	6.42	180	0.714	0.184	91.3
			$Fe_{3.85}O_{12}$						

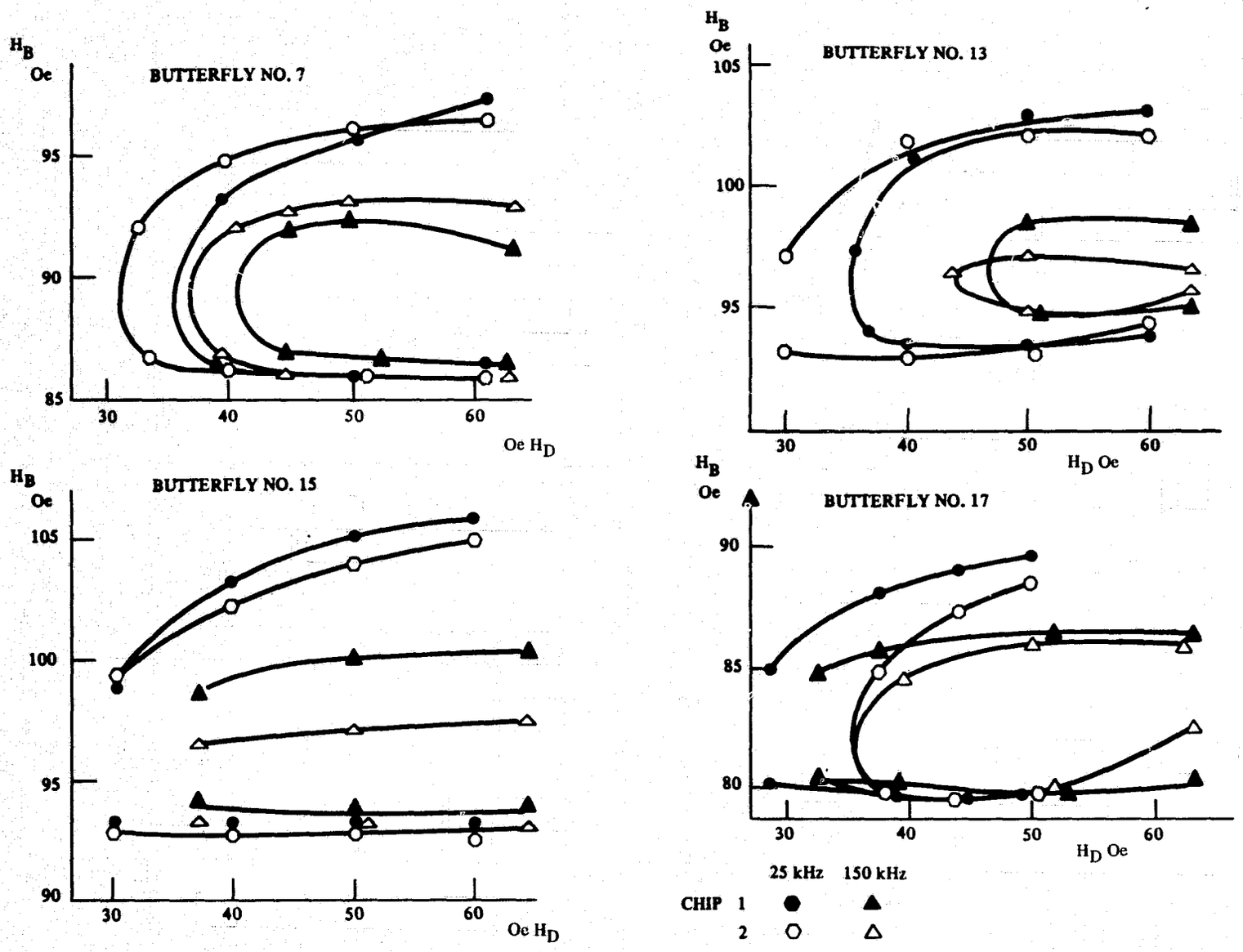


Figure 119. Device Propagation Margins (Room Temperature)

Generation and annihilation. - Unlike the device propagation margins, the generator and annihilator characteristics are quite consistent between various chips. The minimum generating current is primarily determined by the wall energy of the material. For the present design and process, the minimum generating current for (YEmTm) GaIG (σ_W = 0.26 ergs/cm^2) is about 300 ma at room temperature; while for (SmY) GaIG (σ_W = 0.18 ergs/cm^2) the generating current can be reduced down to 200 ma. Varying the generating current pulsewidth will not effect the minimum current significantly. However larger pulsewidth can increase the joule heating produced in the conductor loop which may raise the garnet temperature and thus reduce the wall energy and the generating current. A typical set of phase margin plots are shown in Figure 120(a). The generating phase margin is normally greater than 90 deg.

The annihilator characteristic is more sensitive to the current pulse conditions. A typical set of the annihilator phase margins is illustrated in Figure 120(b). For low current levels (less than 100 ma in this case), the phase margin is very narrow (about 20 deg). It can be extended close to 180 deg by employing a higher current level. However, large annihilator currents will introduce unstable annihilation which limits the phase margin. In addition, when the current level is too high, the annihilator may convert to a generator because basically the annihilator loop is very similar to the generator loop.

The above margins were taken with the device operated by an optimum operating condition, (50 Oe driving field and bias field setting at the center of the bias margin). When the operating condition is moved toward the boundary of the operating margin the generator and annihilator may not work reliably. That is, the generator may generate extra "one's" when the word is almost empty and insufficient "one's" when the word is almost full and the annihilator may not annihilate all the bubbles that pass by. An example is shown in Figure 121 where a test sample was operated at 150 kHz continuously. The generator and annihilator show a reliable operating margin that is narrower than the device propagation margin thus further limiting the whole device operating margin. The exact nature of this unreliability is not quite clear. But from the visual observation of the generation and annihilation functions it is expected that a modification in the generator loop design can improve the generator reliability. For example, the area between conductor loop and permalloy poles can be minimized thus reducing the possible sites for domain nucleation. In addition, optimizing the control current pulses could also improve the generation and annihilation reliability.

Detector signal. - The detector signal characteristics of the engineering model devices are identical to those shown in Figures 21, 81 and 86 except that the detector sensitivity is less than that shown in Figure 86 (between 80 μv/ma to 120 μv/ma). Because of the relatively short stretch (15 elements) and high driving field the detector signal is not very sensitive to bias variations in the operating range.

As shown in Figure 86 the basic detector signal waveform varies with the driving field. This effect can be explained by observing the magnetoresistance variation on a single detector element (without a dummy detector) in a rotating field. Figure 122(a) shows the ΔV variation across the detector element under bubble and no bubble states as a function of rotating field magnitude. At low driving fields the bubble field enhances the in-plane field in magnetizing the permalloy elements thus producing a wide signal with two large bumps (Figure 122(b)). At a higher in-plane field the magnetoresistance variation saturates and the bubble signal is primarily induced by the

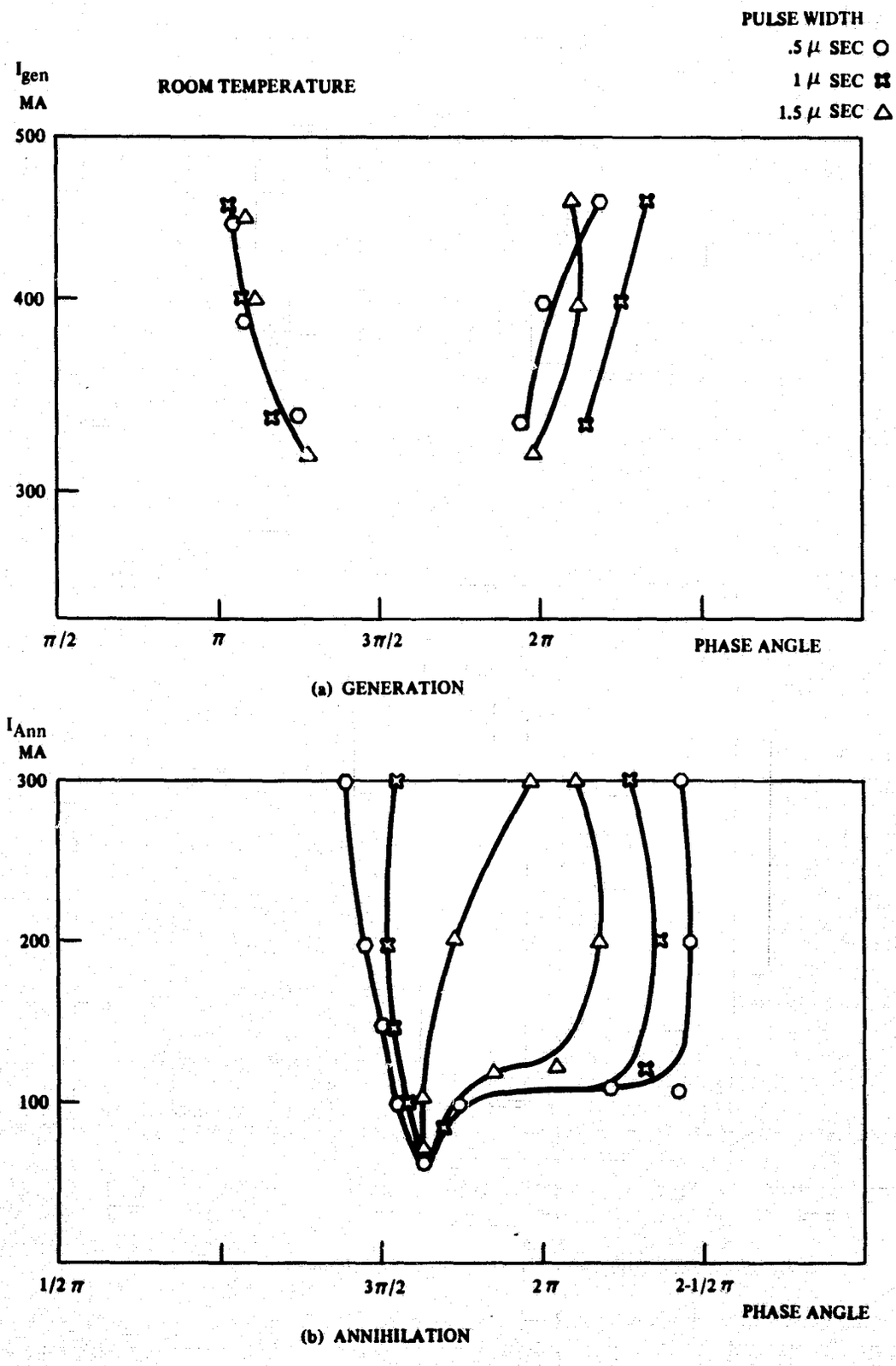


Figure 120. Generator and Annihilator Phase Margin
Sample 2-16-51 $(YEu\,Tm)_3(GaFe)_5O_{12}$

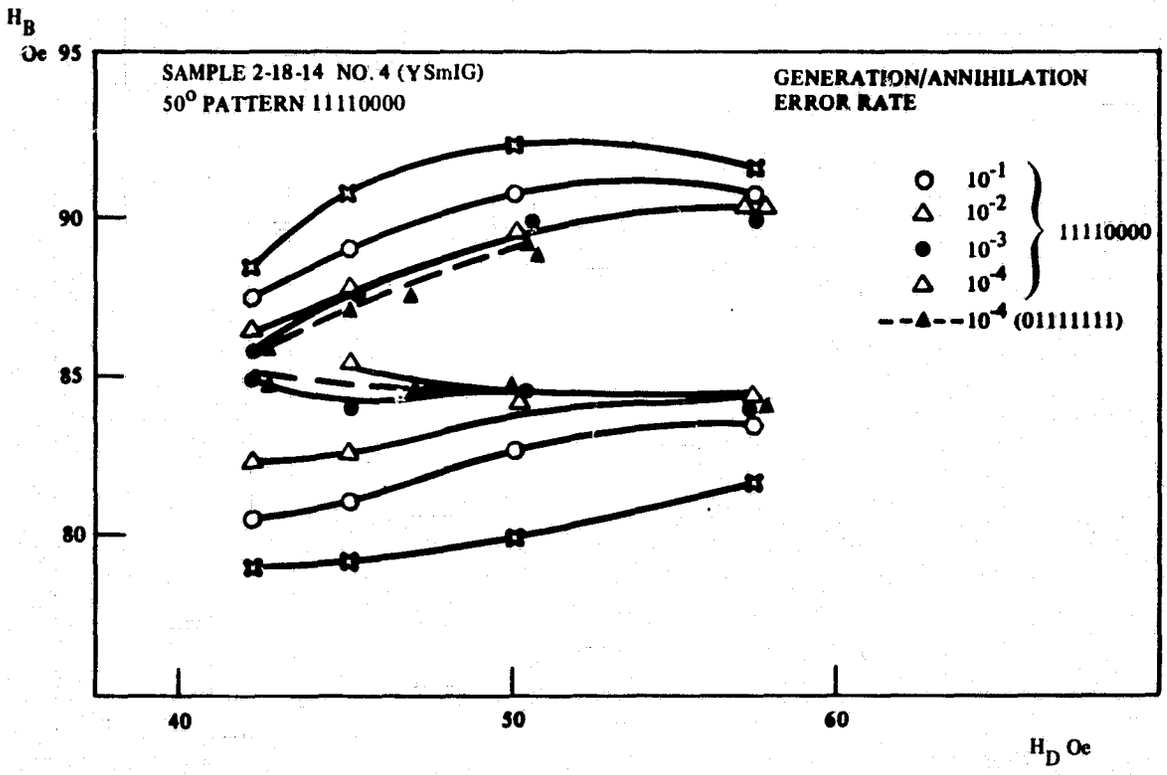
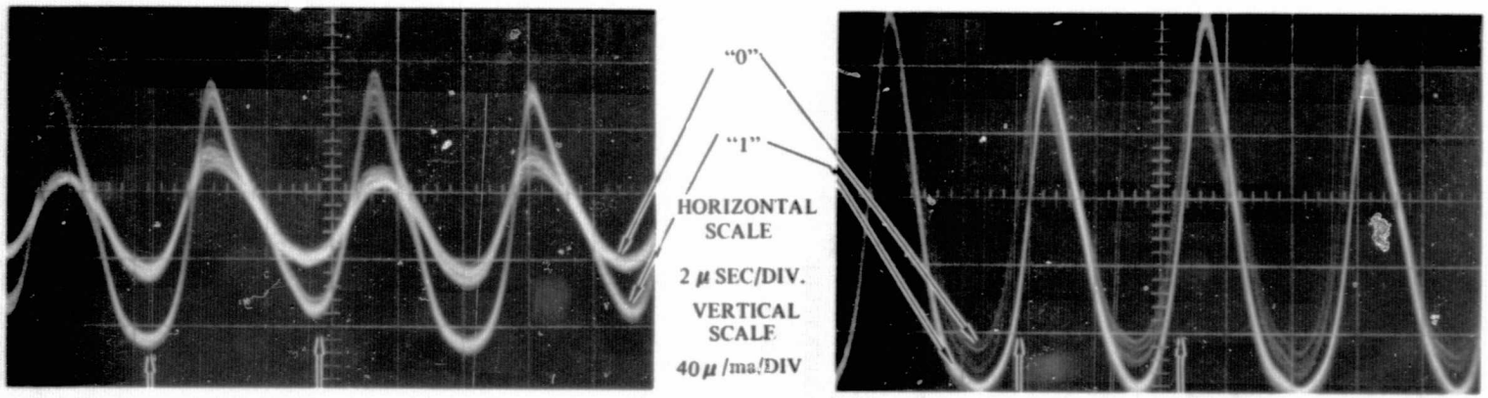


Figure 121. Generator and Annihilator Error Rate as a Function of Operating Condition

phase shift in the permalloy magnetization caused by superimposing the bubble field on the in-plane field. This effect is illustrated in Figure 122(c) which shows a superposition of "0" and "1" states under this operating mode. The signal generated is much narrower in width and the detector window is also shifted by 45 deg as compared to the low driving field case. The transition between these two operation modes is determined by the demagnetization factor of the detector elements. When the devices are processed under similar permalloy composition and thickness, the detector signal waveforms and phase angles are fairly consistent between chips.

10.1.2 Temperature characteristics. - The individual chips used in the engineering model have not been characterized in the specified temperature range outside the magnetic module. Instead, a similar chip with identical properties was measured and the results are summarized in Figure 123. The device operates quite satisfactorily between 0 and 50°C. As compared with the data at 50°C the bias field, minimum driving field and generator current all increases at 0°C because of the negative temperature coefficient of $4\pi M_S$, coercivity, wall energy and the mobility. All these variations require higher driving power for the bubble memory device. At the high temperature end the detector sensitivity is substantially lower because of the combined effect of the reduction in both the magnetoresistance anisotropy effect in permalloy film and the magnetization in bubble material.

The effect of the temperature on the detector signal can be best illustrated in Figure 124 where the detector output is plotted as a function of detector current at different temperature environments. The detector signal does not increase linearity with the detector current because of the joule heating effect in the detector element which

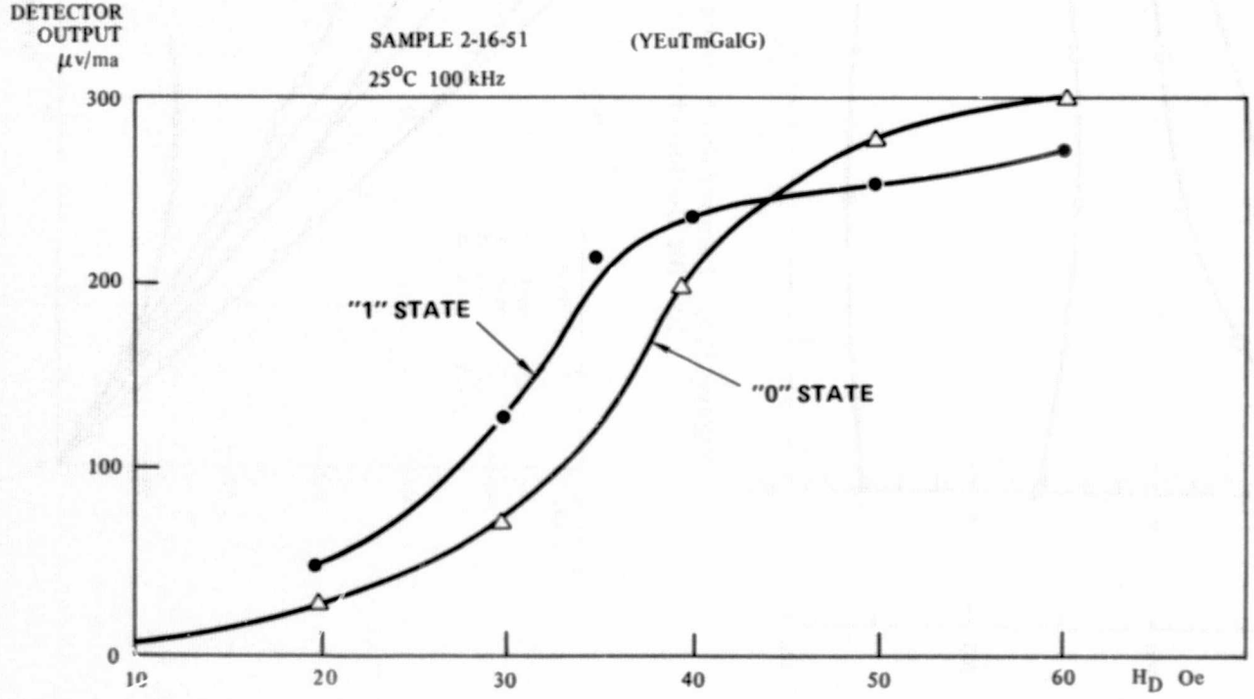


DETECTING POSITIONS

(b) DETECTOR ELEMENT OUTPUT AT H_D = 30 Oe

DETECTING POSITIONS

(c) DETECTOR ELEMENT OUTPUT AT H_D = 40 Oe



(a) DETECTOR ELEMENT M.R. VARIATION (PEAK TO PEAK VALUE) AS A FUNCTION OF DRIVING FIELD MAGNITUDE

Figure 122. Magnetoresistance Variation Across the Detector Element

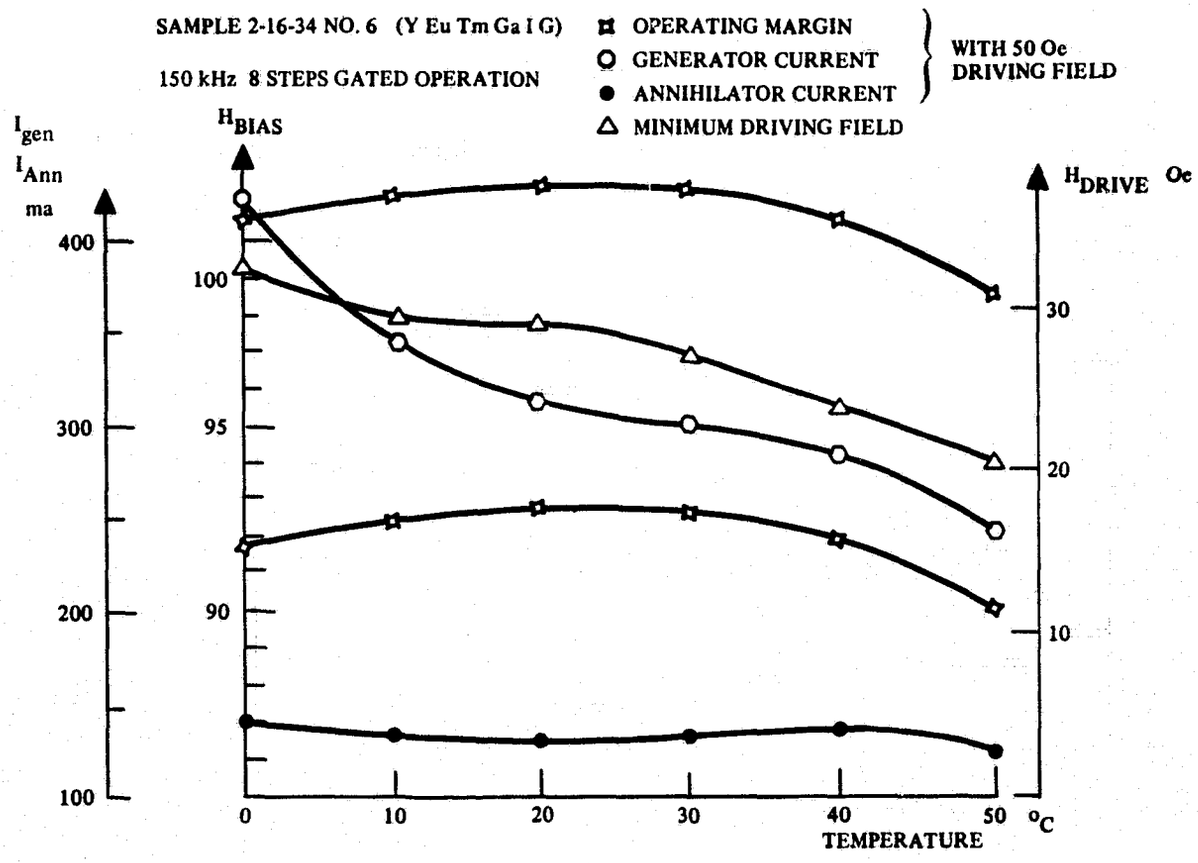
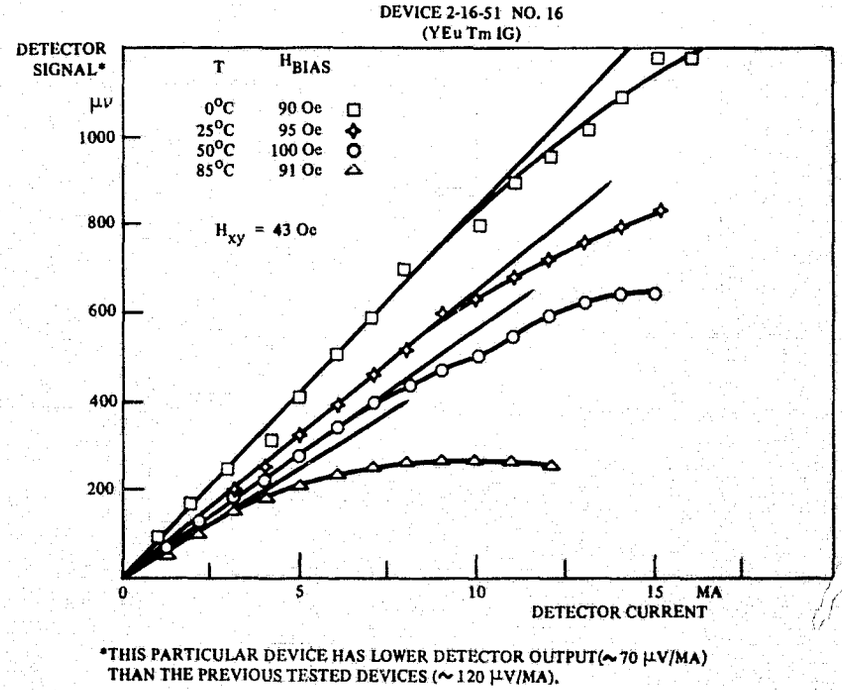


Figure 123. Temperature Characteristics of a 10^4 Bit Device on YEuTmIG



*THIS PARTICULAR DEVICE HAS LOWER DETECTOR OUTPUT(~70 μV/MA) THAN THE PREVIOUS TESTED DEVICES (~120 μV/MA).

Figure 124. Detector Output Signal as a Function of Detector Current at Different Temperatures

effectively raises the temperature in the detector area. An increase in the device operating temperature will not only reduce the detector sensitivity for low current level but also limit the maximum current level that can be supplied to the detector which will further lower the detector output. However, in the engineering model the detector current was only turned on for about one-quarter cycle, thus the detector self heating effect is not as serious as shown in Figure 124.

10.2 Magnetic Module Evaluation

Operating temperature in the ceramic package. - In the engineering model the effective data rate for continuous operation is limited to below 80 kHz. This limit is due to the joule heating in the driving field coil. As can be seen from Figure 94, the device packages are supported by plastic holders which have very poor thermal conductivity. Heat generated from the coil will accumulate in the package and raise the device temperature environment.

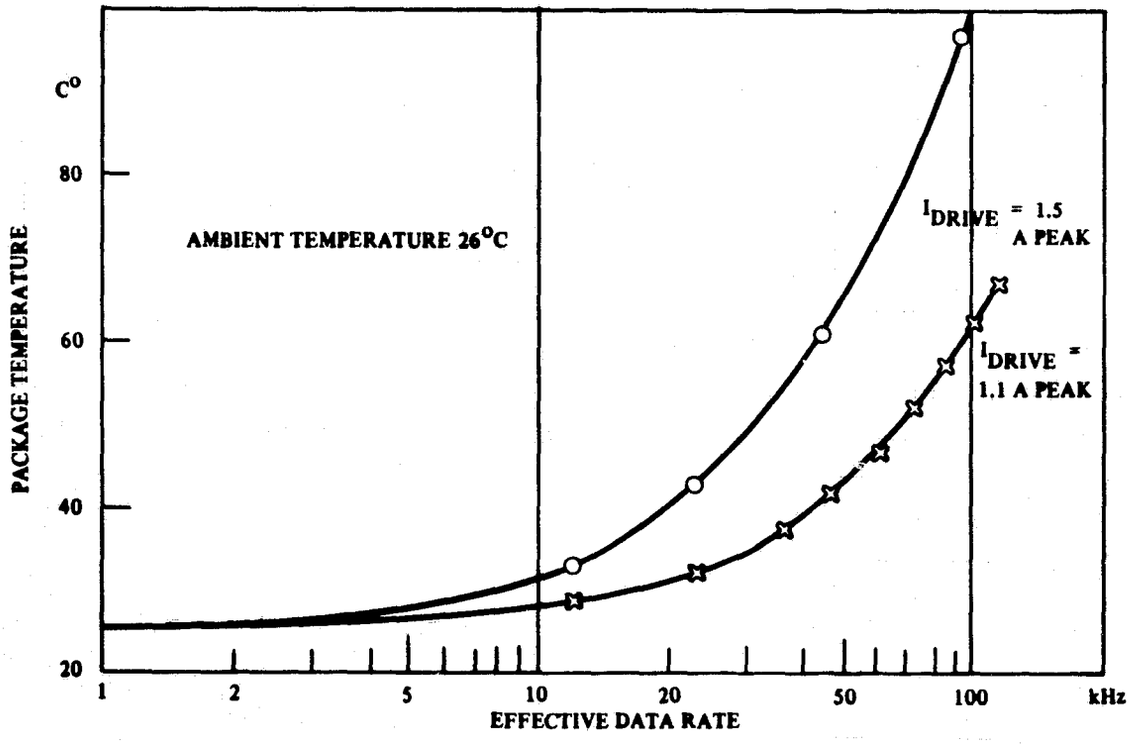
This heating effect was measured by bonding a thermistor chip (Carborundum Type A) in the package and monitoring the resistance variation at different operating conditions. Room temperature data are shown in Figure 125. At 80 kHz effective data rate, the temperature rise is about 55°C. The time constant for the temperature rise is in the order of few minutes. In the recorder application, each package will only be turned on for a very short period. At 150 kHz data rate the time required for accessing two chips is less than 0.14 sec with 1.5 amp drive, the temperature raised in this period is less than 1°C which should not present any heating problem on the device performance.

Temperature coefficient of the bias structure. - The temperature coefficient of the bias structure was measured by using a conventional Hall probe (Bell STB4-0404 probe and 640 incremental gaussmeter) and environment chamber (Statham IFF70/TR). The measured data are shown in Figure 126 where the temperature coefficient varies between 0.05 percent/C° at 0°C and 0.15 percent/°C at 50°C. Compared to the temperature coefficient of the device operating margin, any device with more than 3 Oe bias margin should be able to operate between 0 and 50°C.

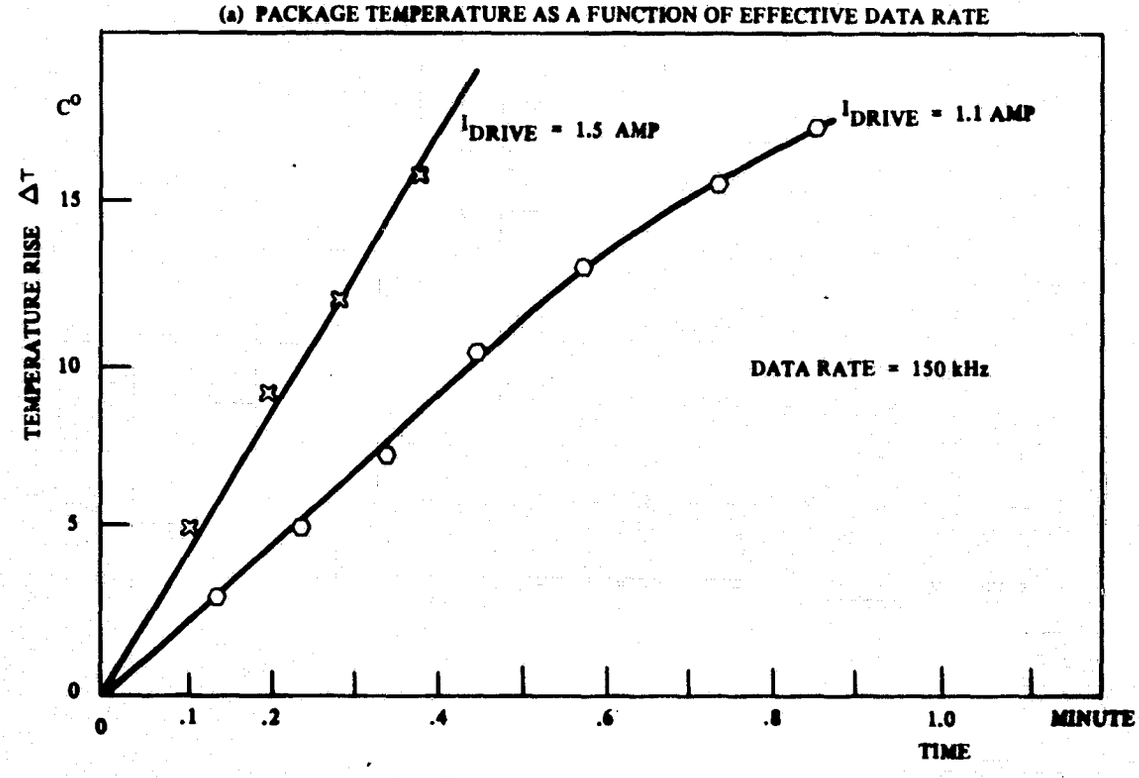
Leakage field from the magnetic module. -The magnetic leakage field around the magnetic module have been mapped with a Hall probe for dc fields and a small searching coil for ac fields (150 kHz). As expected, the maximum leakage field occurs around the edges and corners of the magnetic module. An example of the field distribution map is shown in Figure 127. When using 0.03 in. thick mu metal cover plates the maximum leakage field is less than 10 Oe dc and 0.5 Oe ac. When the plate thickness is increased to 0.05 in. the maximum leakage fields reduce to 6.0 Oe dc and 0.4 Oe ac. This field drops off very fast when the probe is moving away from the magnetic module. At a separation of one inch the leakage field is less than 10 percent of that measured at the module surface.

10.3 Recorder System Evaluation

10.3.1 Description of system tests. - Before obtaining error rate data, the Z-bias of the module was adjusted for best operation of all chips for a given X-Y drive field by either turning the fine tuning shunts or by adding, removing or shifting coarse shunts.



(a) PACKAGE TEMPERATURE AS A FUNCTION OF EFFECTIVE DATA RATE



(b) TEMPERATURE RISE IN THE PACKAGE AT 150 kHz DATA RATE

Figure 125. Temperature Variation in the "Butterfly" Package

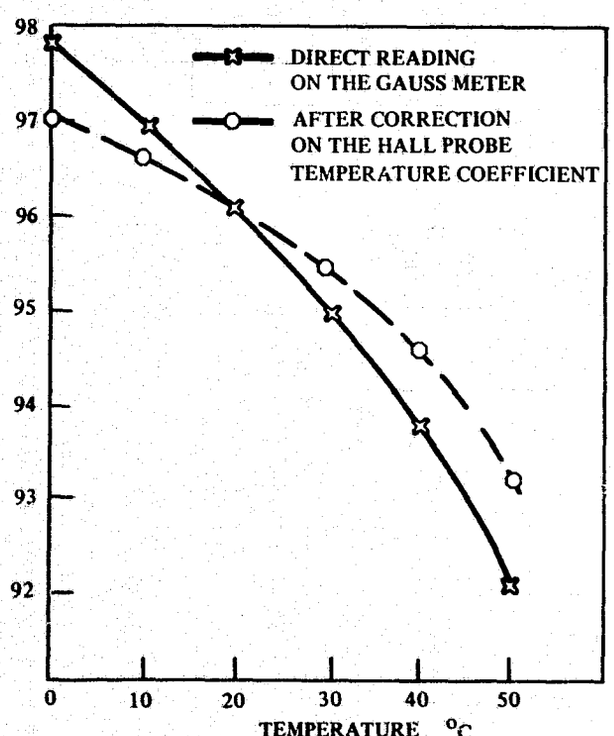


Figure 126. Temperature Variation of the Bias Field in the Magnetic Module (Cavity No. 1)

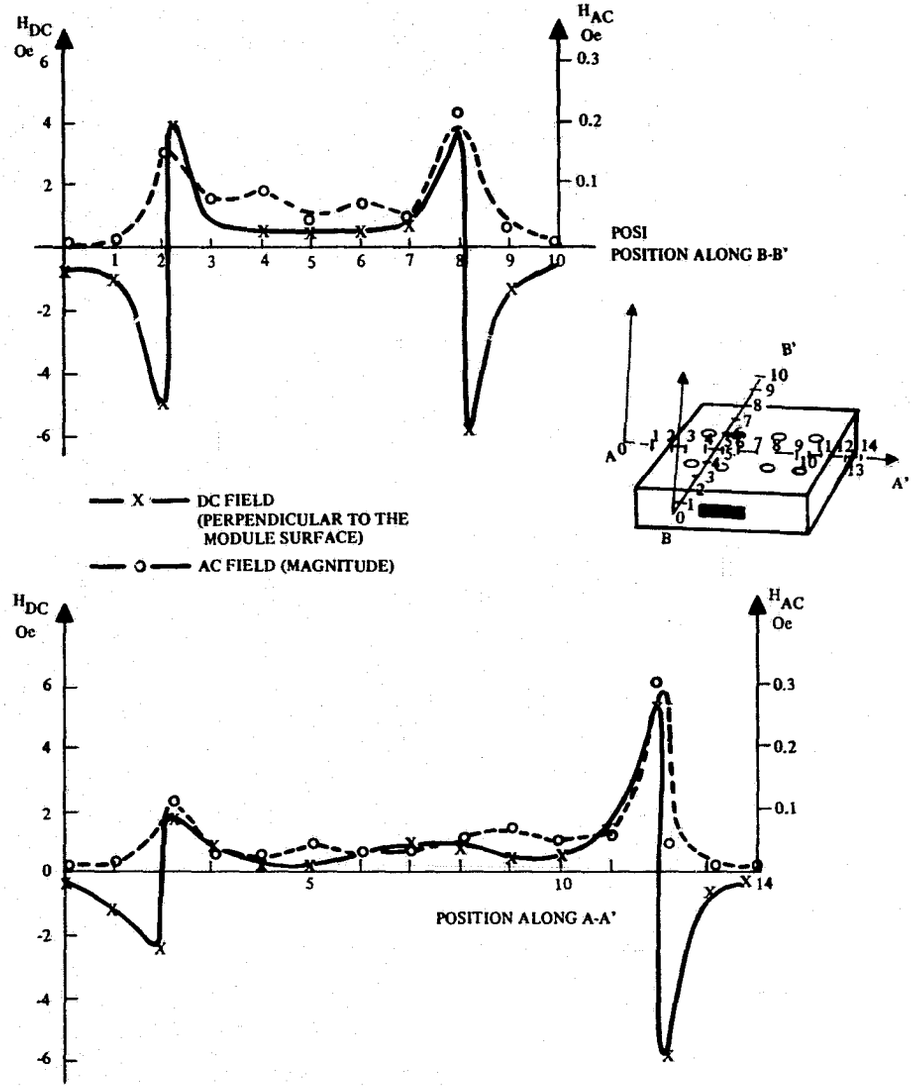


Figure 127. Leakage Field Mapping on the Magnetic Module

The criteria for acceptable adjustment was that three patterns (all ones, a single zero in seven ones, and a single one in seven zeros) must propagate without hard error for 5×10^5 eight-bit patterns around the 10K register (about two minutes). In order to systemize the optimization, a record of changes was made on the chip for a set of initial conditions, voltages, currents, etc. These data, along with subsequent test data on the error rate measurements, will be kept as collateral material in Laboratory Notebook No. N9532.

After the setting up of conditions such as bias, drive voltages, etc, a complete characterization of soft error rate vs threshold setting was done at room temperature for many different data patterns. Data rate was set at 40 kHz (gated operation at 150 kHz propagation rate) to reduce the effect of self-heating of the coil on the chip and the temperature was set at 25°C. Probable accuracy is ±2°C.

A few patterns were chosen to be repeated at the temperature of 50°C and 0°C in order to obtain the thermal coefficients. The sheer volume of data points precluded measuring error rate for all patterns, for all temperatures and for all data rates. In most cases, an average of 90 failures was used to obtain each error rate data point but for the lower rates such as 10^{-8} errors per test (which takes hours) the test criteria dropped to nine errors in order to reduce the test time.

A series of photographs was taken of the actual output waveforms of the sense channel observed at the sense amplifier input so that a different and collaborating set of data could be available on signal shape and thermal coefficients.

Finally a series of tests were done to determine the effect of extended temperature (-25 to 85°C) on the nonoperating data retention. Data were written at room temperature and then the module's temperature raised or lowered to the test temperature, stabilized for 30 min (nonoperating), then returned to 25°C for a data check. Only the module was inserted in the temperature chamber throughout the test series.

A mechanical failure in one of the butterflies (track 3) occurred during testing which resulted in the loss of some data. After the above described tests, the failure was critiqued and corrected (a poor bond).

Once this test series was completed, the recorder was assembled (with selected resistors for threshold determination) and a series of long term validation tests were run. These consisted of selecting a pattern and operating the recorder until a hard error occurred or until something like 10^{14} bubble shifts occurred.

10.3.2 Presentation of system test results. - Figure 128 gives the values of current and voltage determined to be the best for operation at room temperature and are the baseline conditions for the following tests. The Z-bias of Chip No. 2 of Track No. 3 couldn't be adjusted to eliminate the propensity toward collapse when more than five bits were put into the eight-bit pattern.

Soft error rate and pattern sensitivity. - Figure 129 gives some of the results on the detector soft error rate vs threshold setting for several different word patterns. The soft error rate for each data point is calculated on the basis of the number of errors made in attempting to detect the expected outcome. For example, if four ones are put in a pattern and if 10^6 patterns are run before 40 extra zeros are observed, the soft error rate is 10^{-5} errors per detection trial.

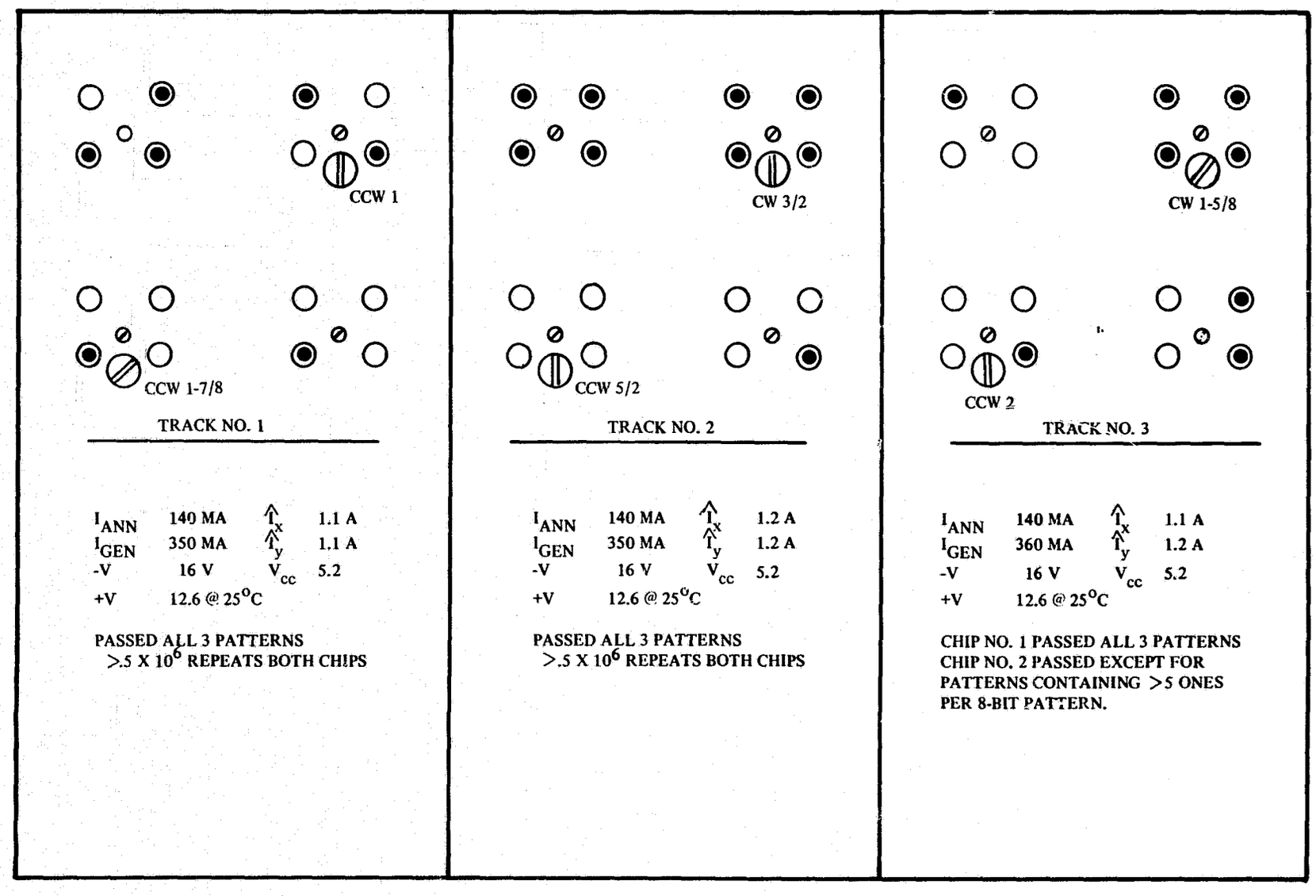


Figure 128. Configuration of Module During Test

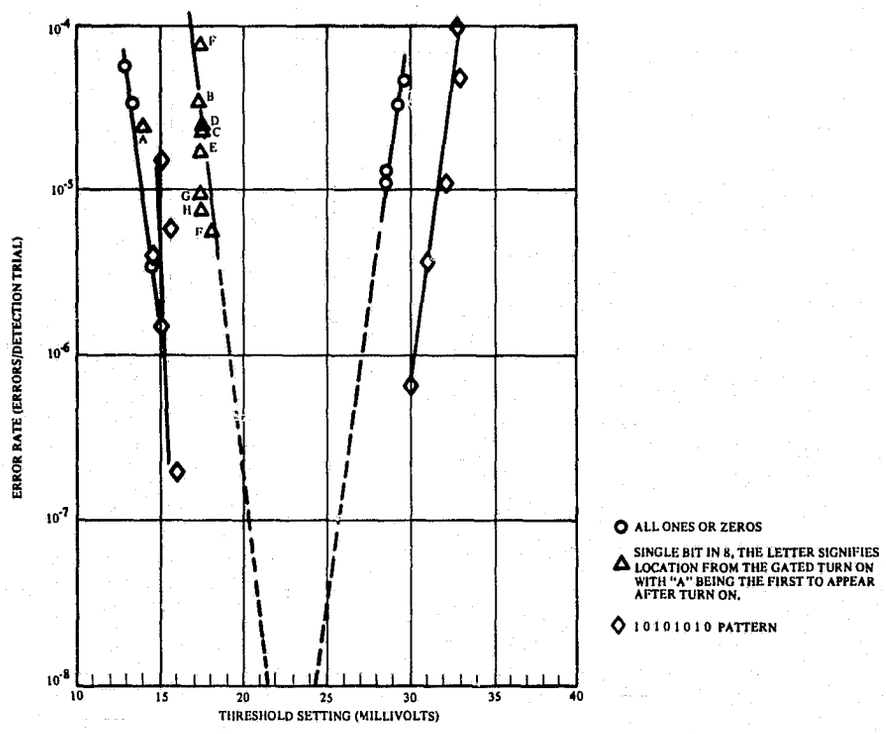


Figure 129. Error Rate vs Threshold for Various Patterns (for Track No. 1 Chip No. 1) at 25°C

The all "ones" and all "zeros" patterns give the basic error rate curve for the detector. Adding "zeros" or "ones" to the pattern tends to shift the error rate curve toward the right as a result of bit-bit interaction between adjacent bubble signals. When a "one" state is next to a "zero" state the bubble stripe has an additive influence on its neighboring zero signal, therefore it moves the low end of threshold setting upward. On the other hand, a "one" state has a subtractive influence on the neighboring "one" state, therefore the patterns with "zeros" may have a higher threshold setting than all "ones" patterns. In the error rate vs threshold curve shown in Figure 129 the low end limit of threshold curve is set by one "one" and seven "zeros" pattern and the high end limit is set by all "ones" pattern. If the "subtractive" and "additive" effect between adjacent bits can be assumed to be equal, then the worst case word pattern would be seven "ones" and one "zero" in an eight-bit word.

Since the device was operated in a gated mode, it was suspected that the turn-on and turn-off of the rotating field may introduce a positional sensitivity on the error rate. This effect was tested by writing a single one in the eight-bit gated pattern where the "one" was moved to each of the eight positions in the pattern. The result is also shown in Figure 129. Notice that this composite curve is fairly straight and shifted to the right (from all zeros case) except for the case of the first bit which shows a higher signal level. A careful study on the signal waveform suggests that this difference is not a result of a larger bubble signal at first bit position but simply due to transient effect in the detection circuit itself. With proper design this transient could be removed and the bubble signal would not have a positional dependence.

Hard Error Rate and Pattern Sensitivity. - The pattern sensitivity on the hard error rate is more difficult to define. As discussed in Para 10.1 the memory chip gated margin is sensitive to permalloy pattern definition and uniformity. Weak positions may effect those bit patterns where bubbles have to rest at those positions. But these effects may also be compensated to a certain degree by adjusting the bias field value, rotating field phase angle and the tilting of the device plane. Therefore, if the chip is not properly designed and processed the pattern sensitivity of the hard error rate depends on the individual chip condition and operating environment. For instance, the two chips in Track No. 1 (butterfly No. 15) show no hard error up to 10^{13} bubble cycles but Chip No. 2 of Track No. 3 (butterfly No. 13) cannot pass more than five "one's" in an eight-bit pattern. On Chip No. 2 of Track No. 2 (butterfly No. 7) bit No. 3 of the 8-bit pattern had a tendency to collapse earlier when first mounted but this sensitivity was removed by increasing the tilting of the package in the magnetic module. As discussed in Appendix C, if the permalloy pattern is uniform, the hard error rate will be directly proportional to the distribution of bubbles in the pattern. At high bias field end where bubbles fail by collapsing, an all "ones" pattern is the worst case; but at the low bias field end where hard errors occur due to bubble shifting, then alternating "one's" is a worst case pattern.

10.3.3 Temperature effect. - The photos of the waveforms (Figures 130 and 131) show the effect of temperature on signal output. Also, they illustrate signal variations from chip-to-chip mostly as a result of variations of $d\phi/dt$ brought about by variations in lead height and length. The signal shape is fairly constant over temperature at least in the limited duration sensed.

Notice that an undamped high frequency (20 MHz) parasitic loop is present in the sensing electronics which is manifested by the synchronized low amplitude ringing on some of the waveforms at sensing time. By identification of the parasitic components involved, these ringing circuits can usually be damped in large systems. For reference, Figure 21 and the accompanying text describe the operation of the sense channel.

The last pair of waveforms at the bottom of Figure 131 show the eight-bit pattern containing alternate ones and zeros for Track No. 3. Notice that the first bit after turn-on is essentially the same as following bits. Phasing must be reasonably constant after turn-on to provide uniform detection.

Another way used to obtain the temperature coefficient of the signal was by measuring the error rate curve for different temperatures as is shown in Figure 132 for Chip No. 1 of Track No. 1.

A summary of signal temperature coefficients as obtained from the various empirical data is given in Table XVIII. For these limited data points, considerable scatter is apparent which averages about -0.8 percent change/^{o}C. This variation is attributed by the temperature dependence of both the detector signal (about -1 percent/^{o}C according to Figure 124) and the preamplifier gain (calculated to be -0.2 percent/^{o}C). The CA3005 pre-amp has flexibility in regard to temperature compensation (see Figure 21) which can be exploited to some advantage in a new design.

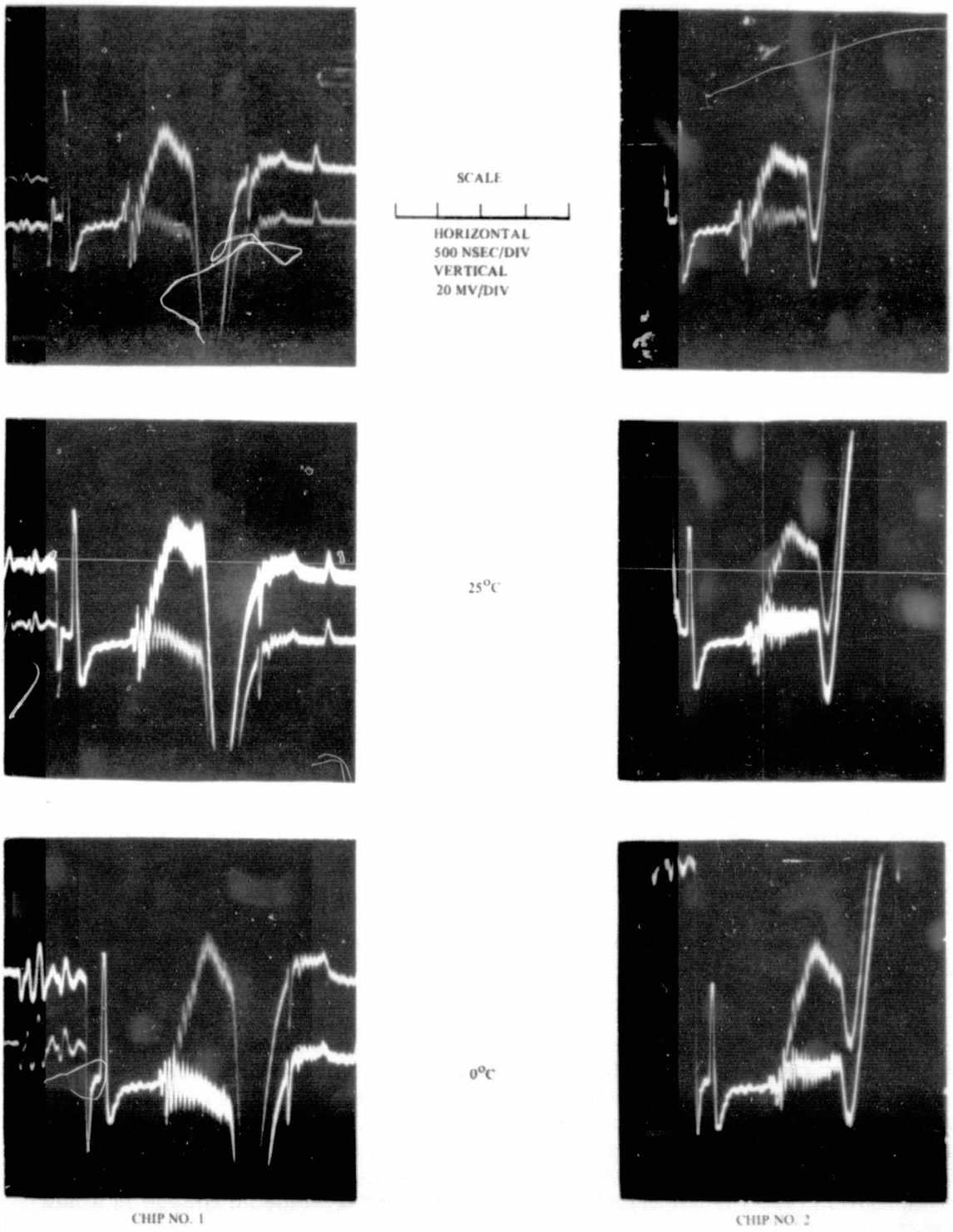


Figure 130. Sense Amplifier Inputs for Track No. 1

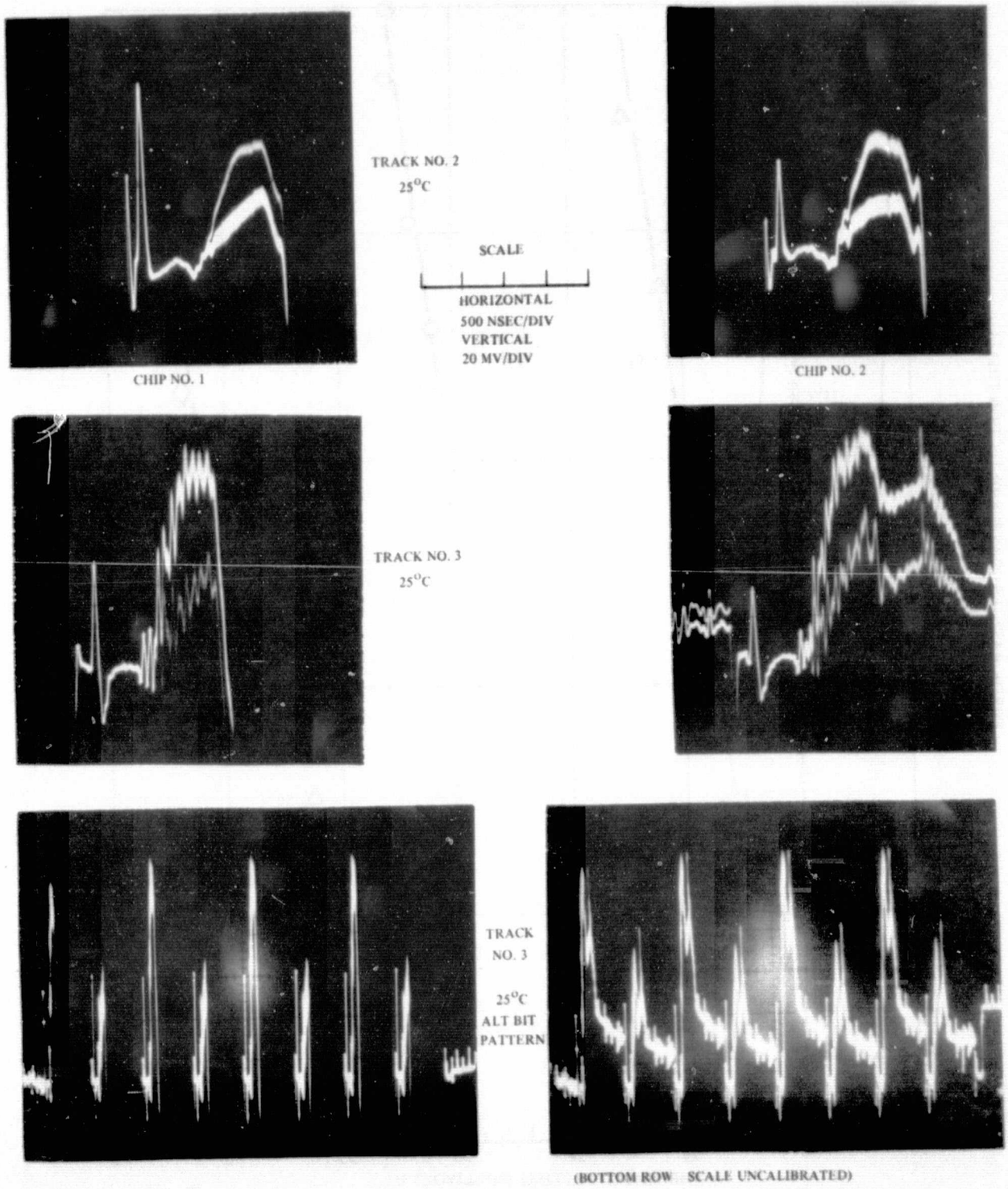


Figure 131. Sense Amplifier Inputs for Track No. 2 and No. 3

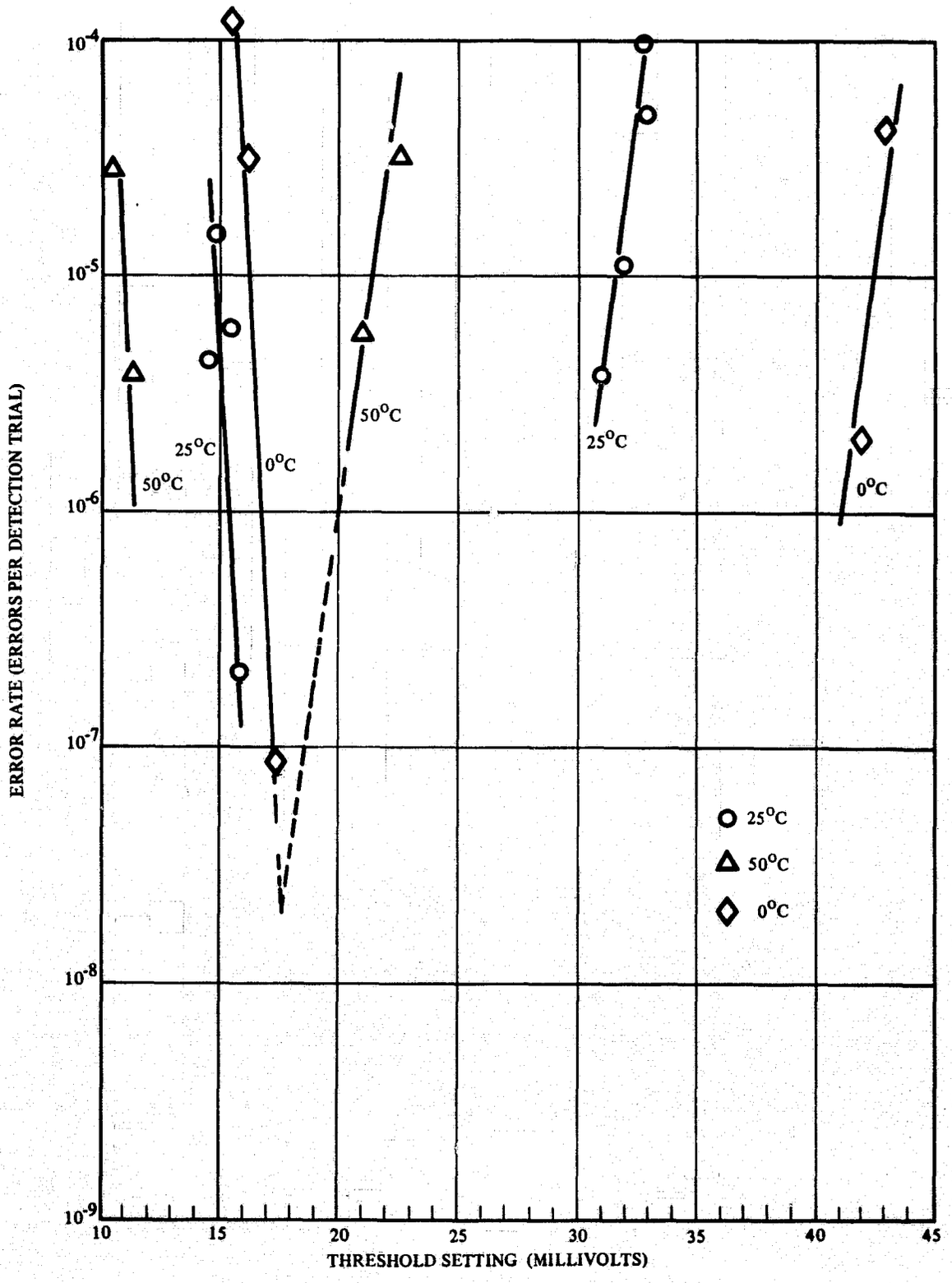


Figure 132. Error Rate vs Threshold for Three Temperatures
Track No. 1 Chip No. 1 for 10101010 Pattern

TABLE XVIII.

TEMPERATURE COEFFICIENT OF THE SENSE SIGNAL, PERCENT PER ^{o}C
(Range From 0 to 50°C)

Identification	Error Rate Thermal Coefficient		Waveform Thermal Coefficient	
	0's	1's	0's	1's
Track No. 1 Chip No. 1	-0.7/°C	-1.38/°C	≈-1	-0.79/°C
Track No. 1 Chip No. 2	-0.6	-1.4	0%	-1/°C
Track No. 2 Chip No. 1	-0.2	-0.67	N.A.	N.A.
Track No. 2 Chip No. 2	-0.5	-0.6	N.A.	N.A.
Track No. 3 Chip No. 1	0	-0.5	N.A.	N.A.
Track No. 3 Chip No. 2	N.A.	N.A.	N.A.	N.A.

Figure 133 gives the error rate for a composite of chips in the module. Part of the chip-chip variation is due to $d\phi/dt$ noise. The worst match is for Track No. 3 and is almost totally due to noise difference between the two chips. Even though the gate time of the amplifier is short, the $d\phi/dt$ is so severe because of the uncontrolled lead structure that the factor must be acknowledged as a significant proportion of the sense error budget where many chips are used. In setting up the tracks a $d\phi/dt$ cancellation coil had to be used to balance the difference between two chips on Track No. 1 and Track No. 3.

To evaluate performance over temperature, two tests were used; the first is a dynamic test, the results of which are given in Table XIX; and the second, a static or nonoperating test, the results of which are given in Table XX. One track can be described without qualification as having an operating range greater than from 0 to 50°C and a nonvolatile range greater than -25 to 85°C.

The evaluation described above was done primarily to elicit the characteristics of the module by putting only the module in the environmental chamber, by holding supply voltages constant, and by using a slow data rate (≈40 kHz) since the bubble memory module is the primary experimental device.

The generator unreliability discussed in Para 10.1 also has been observed in the system test. Occasionally, and with certain patterns at room temperature, the generator will not write a full chip correctly. Apparently the present generator pulse is not optimized and the writing reliability can be further improved by adjusting the pulse-width and amplitude. Another observation is about the threshold stability. Apparently as data rate increases and temperature of track board components increases, the bridge supply voltage actually observed at the reference voltage divider drops causing a tendency toward extra ones. A more stable design is suggested in this area for prototype work.

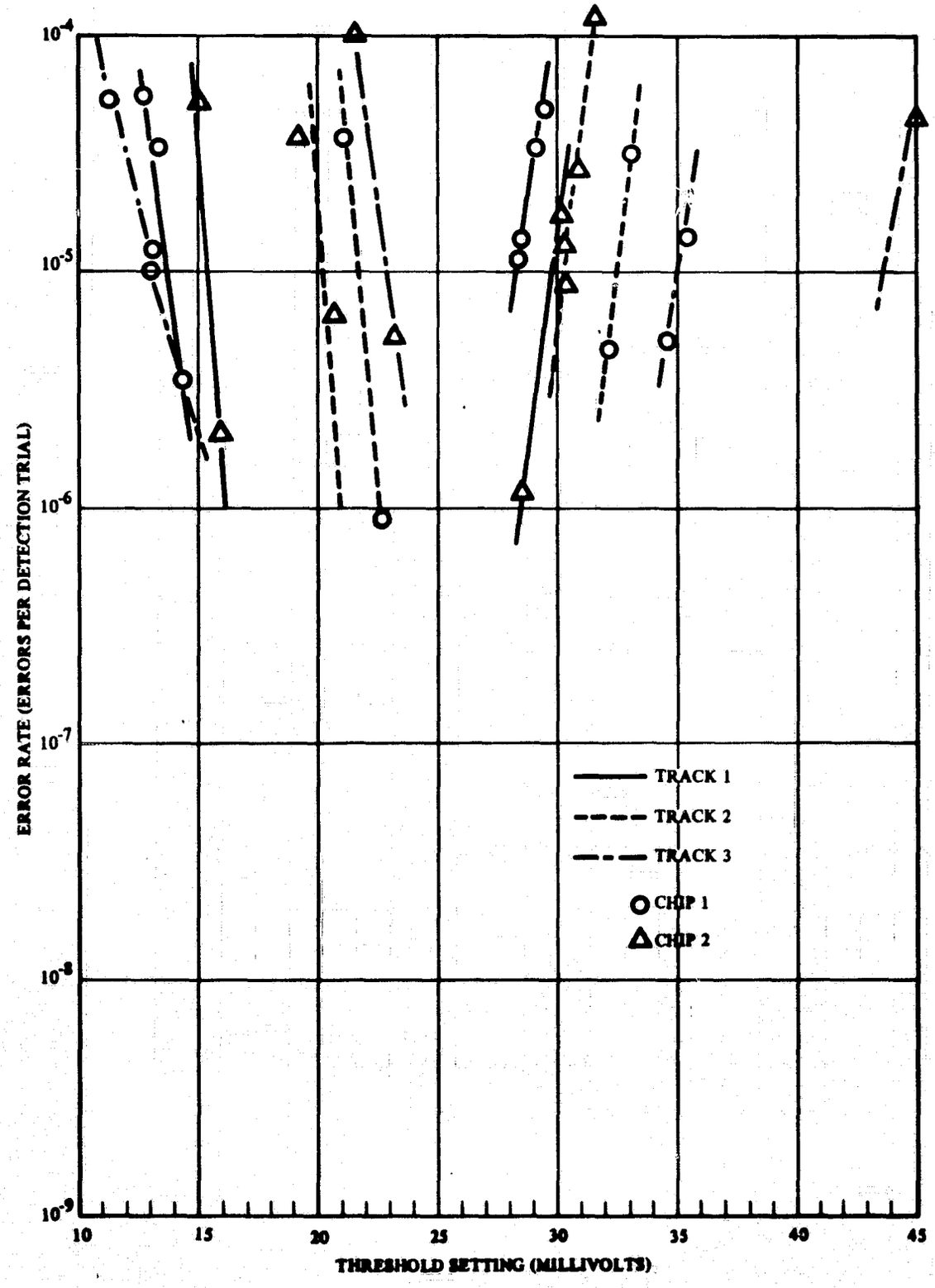


Figure 133. Error Rate vs Threshold for Three Tracks All Ones and All Zeros at 25°C (Two Chip Composite)

TABLE XIX

RESULTS OF THE OPERATIONAL* TESTS FROM 0 to 50°C

		0°C	25°C	50°C
Track No. 1	Chip No. 1	Passed	Passed	Passed
	Chip No. 2	Passed	Passed	Passed
Track No. 2	Chip No. 1	Passed	Passed	Passed
	Chip No. 2	All ones fail: Bit No. 3 & No. 7 Bit 3 more than Bit 7	Passed	Passed
Track No. 3	Chip No. 1	No data collected because of bond problem.	Passed	Passed
	Chip No. 2	All ones - general collapse not associated with specific bit.	Very touchy - usually works with a few bits in the pattern; but with more than five will not pass the criteria.	All ones - bomb 01010101 okay 10101010 bomb
General		Had to boost the +v supply for generator/ann to 15v to obtain an effective write for all patterns.		Had to reduce +v supply to 10v to reduce collapsing of bubbles during write. Writing was still difficult.

*Operation is defined as propagating without hard error, using three patterns (all ones, seven ones with a zero, and seven zeros with a one) for 5×10^5 eight-bit patterns detected. A 30-minute soak at the test temperature was done before testing began. Operation pertains only to propagation. A generation/annihilation test was not done.

TABLE XX

RESULTS OF STATIC DATA STORAGE* TEST

	-25°C	+85°C
Track No. 1 Chip No. 1	No Errors 11110000	No Errors 11110000
Chip No. 2	No Errors 10101010	No Errors 10101010
Track No. 2 Chip No. 1	No Errors 11011111	Shutdown invalidated this test
Chip No. 2	No Errors 10101010	Visual check okay 10101010 but scrambled data with improper shutdown before error check
Track No. 3 Chip No. 1	No data available	No data available
Chip No. 2	00000100 Errors Ext. ones	Errors 00000100 Ext. ones

*The criteria is the retention of a pattern without error written at 25°C and retested at 25°C after a 30-minute soak at the test temperature and a 30-minute resoak at 25°C before testing.

10.4 Summary

The present test data indicate that the bubble domain recorder has the capability of fulfilling the design requirements of a simple prototype flight recorder for satellite application. The engineering model can be operated at 150 kHz data rate with 10^{-8} soft error rate and 10^{-13} hard error rate which is better than conventional tape recorders. Two of the three tracks demonstrate a successful operating range between 0 and 50°C but the third track has some limitation on one of the chips. However, the chip level test on the spare track indicates both chips have wide gated operating margins at 150 kHz which can replace the present Track No. 3.

The bias adjustment in the magnetic module is quite critical due to the reduced operating margin of the chip at the high frequency. The reliable operating margin can be expanded by chosing better material, optimizing the pattern design and improving the processing uniformity.

11. CONCLUSION

The performance evaluation on the engineering model (summarized in Section 10) successfully demonstrated the feasibility of fabricating a flight recorder under the current bubble memory technology. This model has been operated at 150 kHz intrinsic data rate with a soft error rate better than 10^{-6} and a hard error rate approaching 10^{-13}. This performance greatly exceeds the conventional tape recorder system. With the power shutdown protection circuitry for nonvolatility, this bubble memory can be used as a direct replacement for a present mechanical tape recorder system. In addition, the memory can be easily organized as a block oriented memory for other applications. Utilizing the asynchronous capability of bubble devices the memory can be operated to a very low frequency. These capabilities add dimensions of flexibility and reliability not found in present tape recorder systems.

The projection to a 50M bit simple satellite data recorder (summarized in Section 9) uses 100K bit capacity, 16 μm period bubble memory chip. The proposed prototype satellite data recorder can be made with a size less than 200 in.^{3}, a weight of 12 lb and power consumption of 12 watts power when all of its four tracks are operated in parallel. The data rate can vary from very low up to 150 kHz with an error rate at least equal to or better than that achieved in the engineering model. The power dissipation and recorder weight however, will exceed the design goals by a factor of 2 and 1.5, respectively. Some tradeoffs can be made (such as operating all tracks synchronously) to better approach the design goals. To reduce both the size and weight while still maintaining independent track operation capability would require further research and development efforts. These efforts include using a smaller bubble size, a faster bubble speed, a lower driving field and a lower bias field.

APPENDIX A.
A PLANAR MAGNETO RESISTANCE (PMR) PROBE FOR FIELD MEASUREMENT

In the bubble memory system, the alignment of bias field with respect to the device plane is important to the device operation (see Section 7). The conventional semiconductor Hall probe can only measure the magnetic field perpendicular to the probe device plane, therefore, it is not sensitive enough to check whether a magnetic field is perpendicular to a device plane or not. Besides, the Hall probe is bulky, expensive, needs sophisticated supporting electronics and can not be easily attached in the bubble memory system. In this section, an alternative probe using Planar Magneto Resistance effect in a ferromagnetic film (PMR probe) is proposed. Unlike the semiconductor probe, it measures the field in the plane of the magnetic film which is the real value interested in the field access type bubble devices.

A-1 Planar Magneto Resistance Effect

The basic structure of the proposed probe is shown in Figure A-1 where A is a vacuum deposited and photolithographically defined magnetic film pattern. It is electrically connected by two metallic film connectors B and C. A constant current source is connected to A so that any resistance variation in A can be sensed by measuring the voltage drop across B and C. The dimension of A is so chosen that the demagnetization field of A is much greater than its coercivity and anistropy field. When no external magnetic field is applied, A is demagnetized in a multiple domain state.

When a uniform magnetic field H is applied in the plane of A, the domains in A will start to align along the direction of H (i.e. the film is being magnetized) causing a magnetoresistance variation in A.(Ref 19) This variation is sensed as a voltage change, ΔV, across A, and is a function of H as illustrated in Figure A-2. When H is sufficiently greater than the demagnetization field H_d along the direction of the applied field H, ΔV will reach a saturation value, $\Delta V_S(\theta)$, according to the relation (Ref 31).

$$R_S(\theta) = I\Delta R \cos 2\theta \qquad \text{(A-1)}$$

where

I is the current in A

ΔR is the magnetoresistance anisotropy in A

θ is the angle between I and H

This is called the planar magnetoresistance effect in the ferromagnetic films. The present magnetoresistance probe for bubble detection is based on the same phenomenon.

A-2 Use of the PMR Probe for In-Plane Field Calibration

When the demagnetization field in the permalloy film is uniform the magnetization of the film is a linear function of the applied field (if the film coercivity H_c and anisotropy H_k are much smaller than demagnetization field H_d) and saturates at an external field H equal to H_d. This saturation effect can be seen from the magnetoresistance variation as a function applied in plane field. The demagnetization field in a circular permalloy disk is given by

$$H_d = 0.043\ \tau/\delta \text{ Oe} \qquad \text{(A-2)}$$

where τ is the film thickness in Å and δ is the disk diameter in mils (0.001 in.). The value of the magnetization in permalloy film is relatively stable at room temperature, and thus the value of H_d is determined by the disk geometry only and can be used as a reference value for field calibration.

Figure A-3 (a) shows a test pattern with nine permalloy disks. The diameter of the disk is 0.010 in. and film thickness is 4000Å which gives H_d = 17.6 Oe. The probe resistance is about 2.6 Ω. With 100 ma probe current a magnetoresistance variation around 1 mv can be obtained. Figure A-3 (b) shows the ΔV output from the probe under a slowly varying field. This field sensitivity can be calibrated from the point where the magnetoresistance variation begins to saturate. The accuracy can be better than ±5 percent in this example.

A-3 PMR Probe for Bias Field Alignment

If the applied magnetic field H on the PMR probe is an alternating field, the variation in V will then oscillate at a frequency twice that of the alternating frequency of H. This effect is illustrated in Figure A-4 (a). If H is symmetrical in shape then the oscillations in ΔV will have equal peaks. If an additional field differing in frequency is superimposed on H causing an asymmetrical total field, it will induce variations in the amplitude of ΔV waveform as illustrated in Figure A-4 (b). Using this property, the alighment of a magnetic field perpendicular to A can be achieved by monitoring the variation induced by an in-plane oscillating field. Misalignment in vertical field will introduce a component in the plane of A and cause asymmetry in ΔV waveform.

In order to increase the sensitivity of this probe the shape of A can be elongated to a long bar and several bar elements can be connected in series. This arrangement also averages out any nonuniform magnetization effect in each individual bar. Because of the large shape anisotropy in the bar elements it is only sensitive to field components along the bar direction. Thus two sets of bars perpendicular to each other are required in order to sense any randomly oriented in-plane field component.

The signal from each set of bars can be displayed simultaneously simply by connecting these bars in series and using an in-plane rotating field instead of an oscillating field. The output from each set of bars are shifted 90 deg in phase and can be separately identified. An example of this design is shown in Figure A-5(a) where two sets of magnetic film elements (typical dimensions are 10μm x 50μm x 0.5μm using 80-20 NiFe film) are connected by conductor films, (such as CrAu or AlCu). A typical output from this design is shown in Figure A-5 (b). The resistance of this probe is about 60 Ω. Using a 5 ma probe current a 1 mv voltabe variation can be measured under 5 Oe rotating field. A 100 μv asymmetry can be easily identified in this waveform which corresponds to about

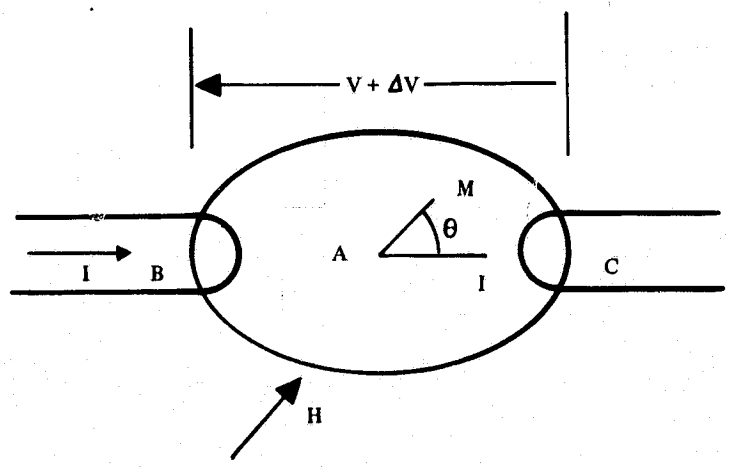


Figure A-1. A Basic PMR Probe

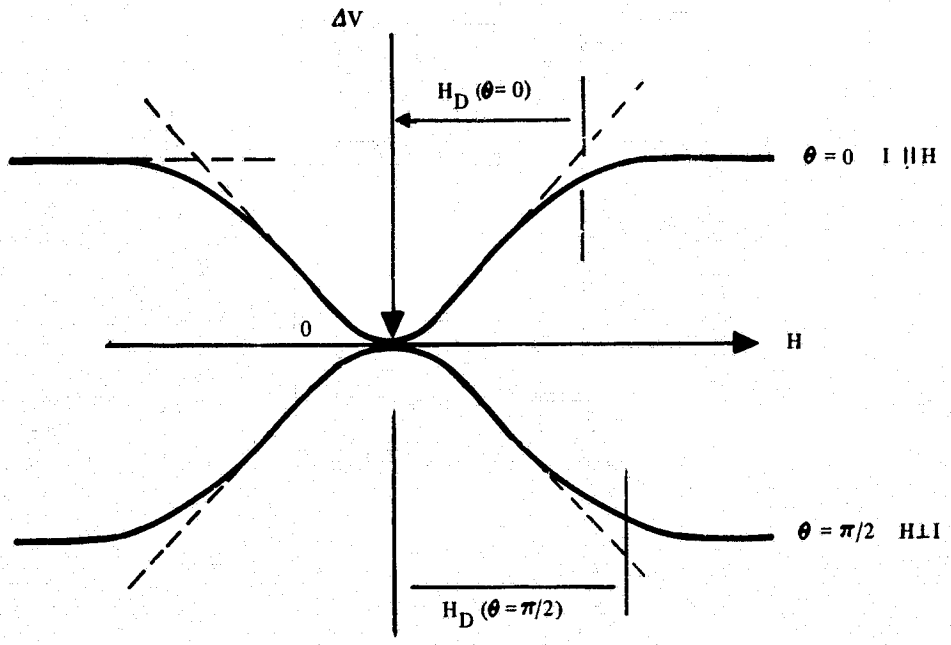
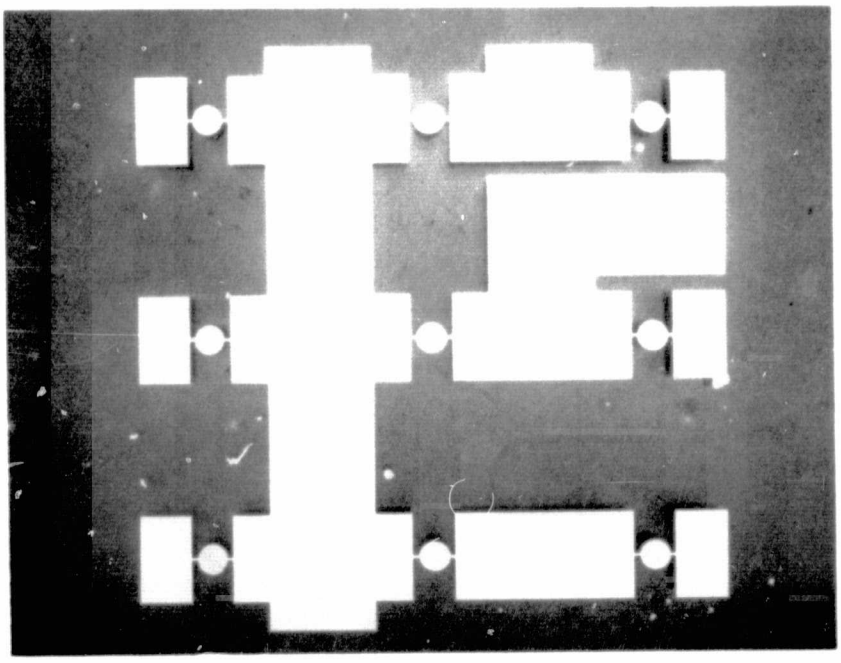
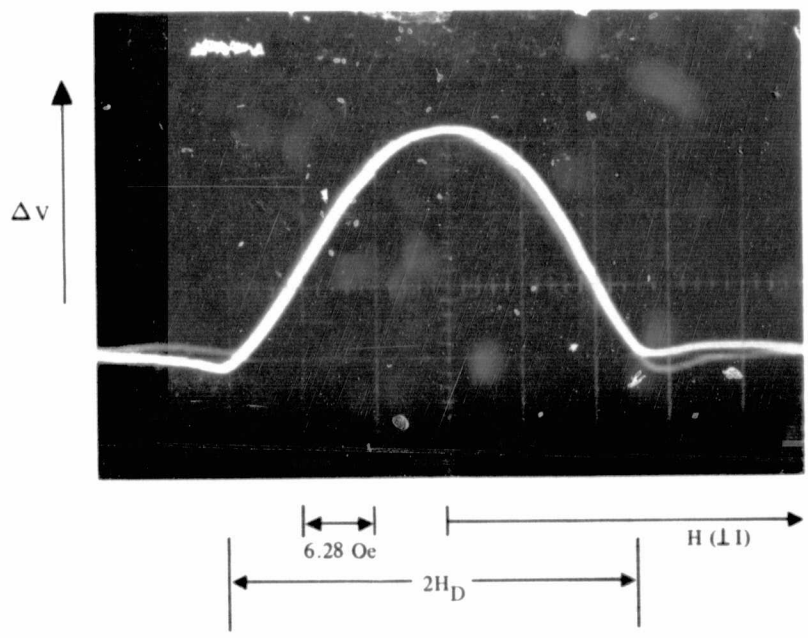


Figure A-2. Voltage Variation Due to Magneto Resistance in Permalloy Film

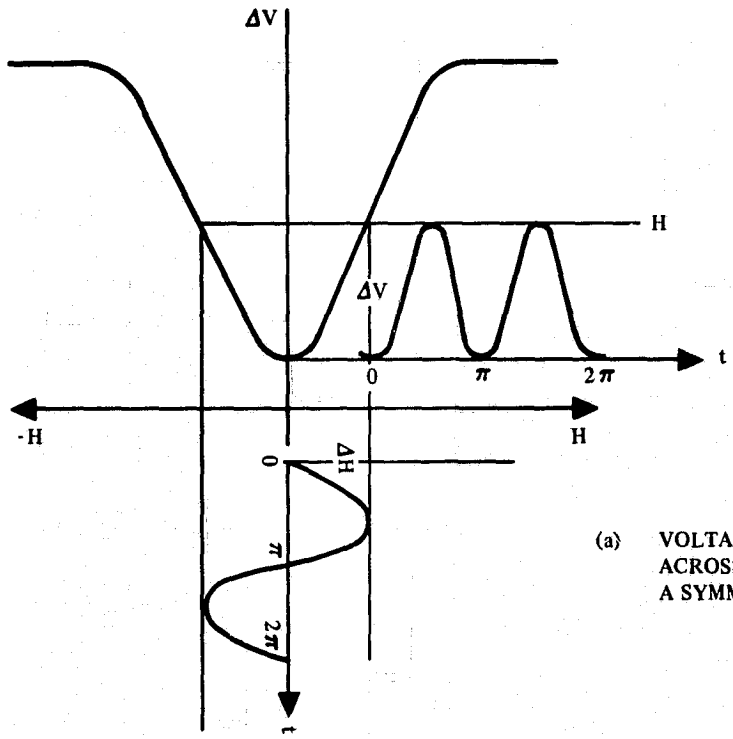


(a) CIRCULAR DOTS ARE PERMALLOY FILM 10 MIL DIAMETER

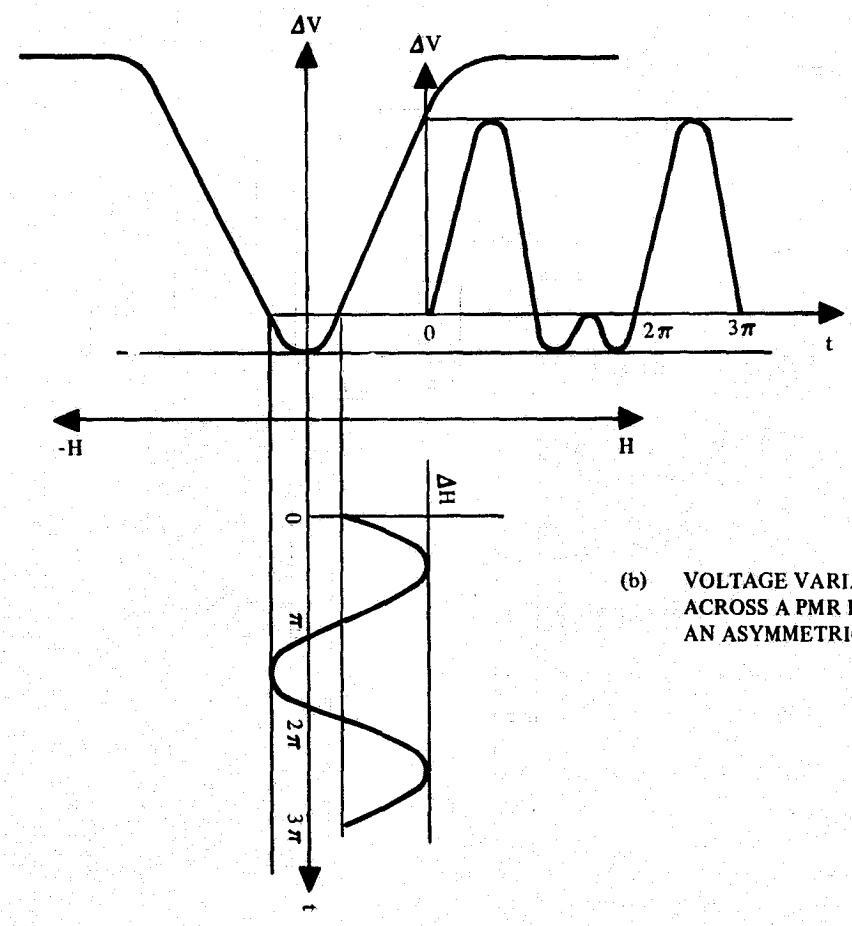


(b) ΔV VS H MEASURED ACROSS ONE PERMALLOY DOT (4000Å THICK $H_D \sim 17$ Oe)

Figure A-3. A Permalloy Field Probe Design

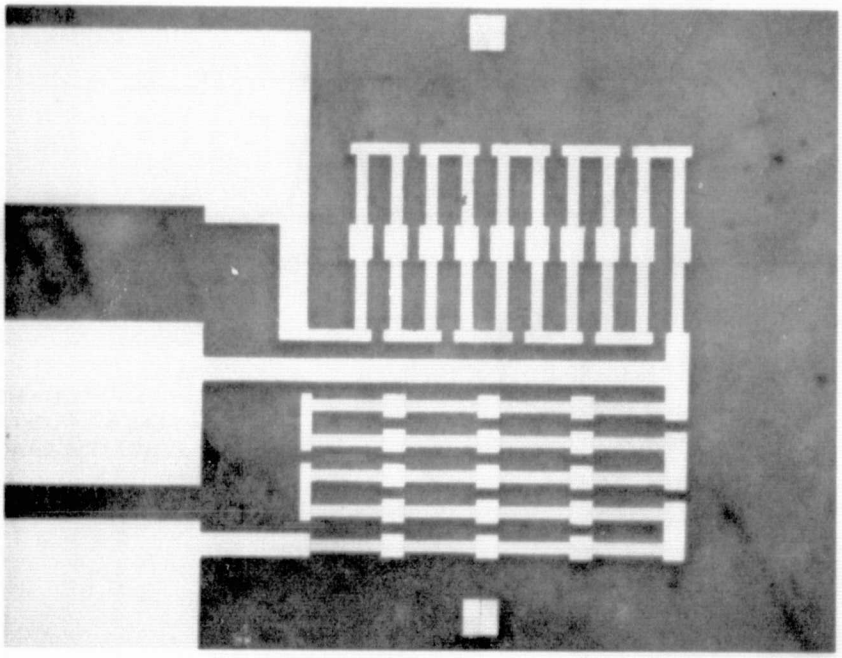


(a) VOLTAGE VARIATION ACROSS A PMR PROBE IN A SYMMETRICAL AC FIELD

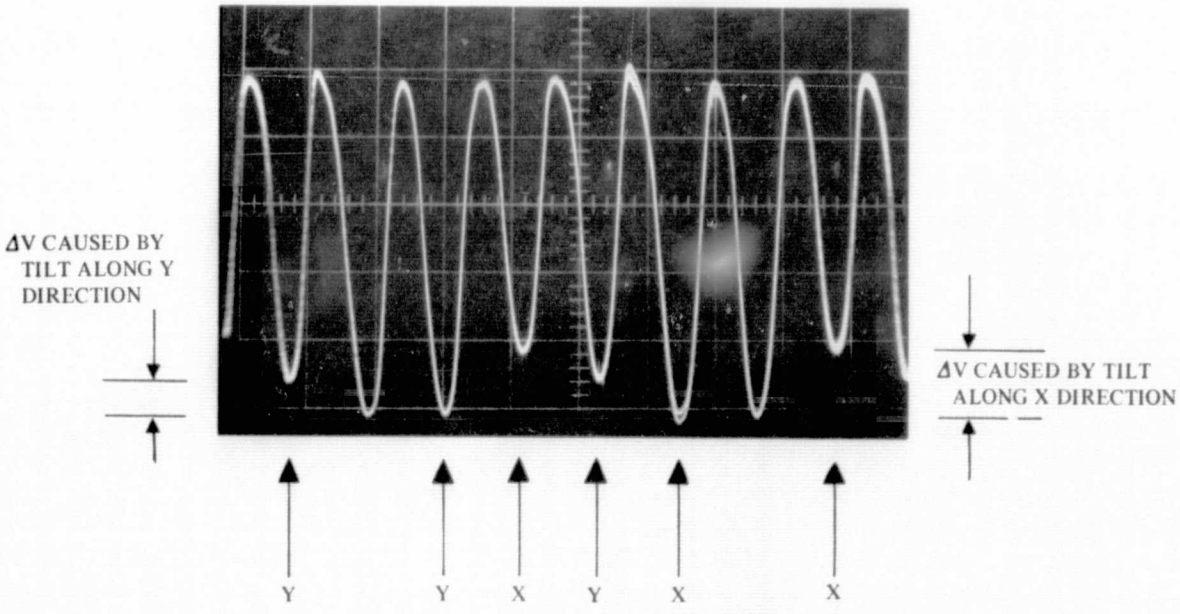


(b) VOLTAGE VARIATION ACROSS A PMR PROBE IN AN ASYMMETRIC AC FIELD

Figure A-4. Bias Field Alignment



(a) A PMR PROBE FOR FIELD ALIGNMENT



(b) PROBE OUTPUT UNDER TILTED BIAS FIELD

Figure A-5. A PMR Probe for Bias Field Alignment

0.3 Oe in-plane component on the probe. If the bias field is 100 Oe, this corresponds to ±0.17 deg accuracy in bias field alignment on the bubble memory device plane. Higher accuracy can be obtained by simply increasing the probe current, probe resistance (i.e., number of permalloy elements) or vertical field strength.

This probe can be integrated with the bubble memory circuit. An example is shown in Figure A-6 where the chevron elements in the guardrails are connected as probe elements. It has been shown that the magnetoresistance variation in a chevron structure is very similar to that in a bar element (Ref 19) thus, the probe function should also be similar.

A-4 Discussion

The previous examples demonstrate the feasibility of this PMR probe. Its reliability of course, depends on the permalloy quality of which both the coercivity and anisotropy fields have to be kept minimum. The single disk type probe shown in Figure A-3 is not very stable because of the induced anisotropy in the permalloy film. The probe shown in Figure A-5 uses a number of small bar elements which offers much better stability in the output signal than the single element probe.

In summary, as compared with Hall probe, this PMR probe is much simpler in structure, smaller in size, offers very good resolution in vertical field alignment, and can be integrated with the bubble memory device.

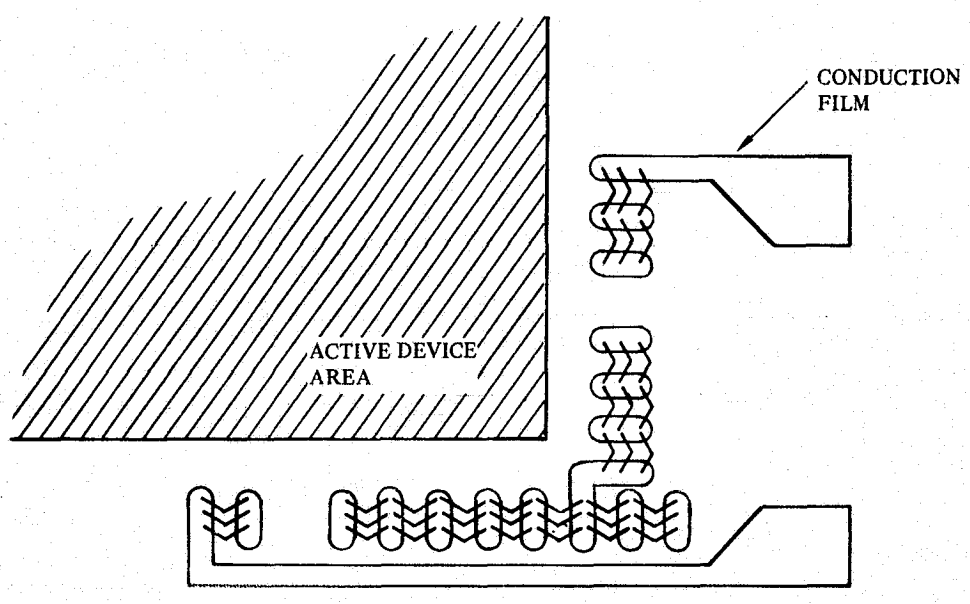


Figure A-6. PMR Probe for Field Alignment
Integrated into the Chevron Guardrail of a Bubble Device

APPENDIX B.
FEASIBILITY MODEL EXERCISER

B. 1 General Description

The exerciser used to test the feasibility model is a sequential machine (not unlike an appliance timer) which steps through a sequence of programmed functions such as error counting or recorder on/off. Any number of the functions can be executed in any one of 10 time steps. Any step can be held by one of two counters which are set on the front panel. Any subset of time steps can be looped up to 1000 times. Test programs of duration greater than 24 hrs can be run on the exerciser. A cyclical 8-bit pattern generator and an error analysis section are used for evaluating recorder performance.

The heart of the exerciser (Figure B-1) is a single IBM card reader which has 220 switches (corresponding to card locations) wired as a 10 x 22 matrix and 20 switches wired independently. Program control is provided by the lower 240 locations of the IBM card. The step generator changes to a new step on every clock unless inhibited by one of the inhibit inputs. A preload input allows return to a previously used step, which permits looping of a number of steps in the program. The two counters (A and B) can inhibit a new step transfer until they reach the end of their count. The recorder is also able to inhibit step transfer until some recorder function like track read is finished.

The pattern register holds an 8-bit pattern which is loaded in parallel from switches. On a write command the 8-bit pattern is serially loaded into the recorder as a cyclical pattern. When unloaded, the recorder data is fed into the data register so that it may be compared with the 8-bit pattern in the pattern register on a bit-by-bit basis.

By examining two bits of the data at a time a determination of bubble shift is made as well as whether the failure is due to a missing bubble or to an extra bubble. These various possibilities are decoded and counted in the Error Counter and display section.

An IBM card is used to control the test program through holes punched in the last 240 card locations (columns 61-80, rows 0-12) according to a program listing a sample of which is given in Figure B-2. The test program is executed sequentially, starting from columns 61 and 62 as the first step and proceeding to columns 79 and 80 as the tenth or last step. By using two columns per step, the total number of allowable functions is 24, but only 22 are used dynamically (selectable during a time step); the rest being available for static instructions the way individual front panel switches would be used.

Any step selected may be repeated (step RPTA or step RPTB) up to 10^7 times. Any group of steps can be repeated or looped up to 10^4 times (begin loop, end loop).

Besides the exerciser control functions listed above, there are synchronization instructions, error control instructions, and various instructions necessary for the control of all recorder operations. The dynamic instructions are given in Table B-1.

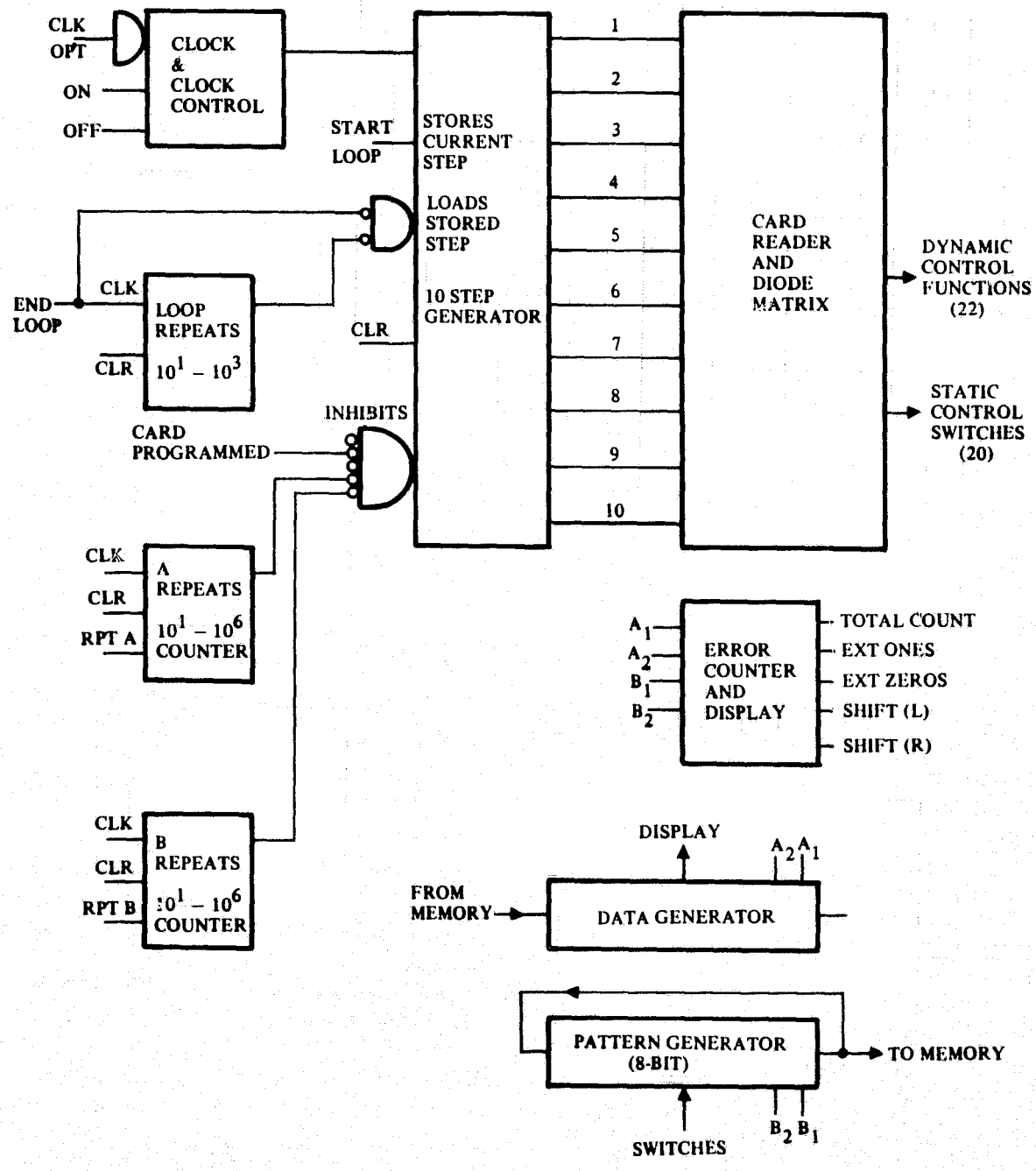


Figure B-1. Exerciser Block Diagram

CARD NUMBER: 54 PURPOSE: BYTE WRITE/BYTE READ

STEP	COL.	PUNCHES	FUNCTION
0	61	0	RECORDER ON CLEAR A AND B, SYNC
	62	3, 4, 0	
1	63	8, 2	TRACK ON (BYTE WRITE)
	64		
2	65	7	WRITE DATA, RPTB
	66	5	
3	67		WRITE DATA
	68	5,	
4	69	9	TRACK OFF, RPTA (DELAY)
	70	-, 8	
5	71	0	RECORDER ON
	72		
6	73	5, 9	BEGIN LOOP CLR A
	74	4, 9	
7	75	5, 1, 3, 8	TRACK ON (BRMD), SLOW CLOCK, RPTA
	76	-, 9	
8	77	4	END LOOP
	78	9	
9	79		TRACK OFF
	80	8, 9	

Figure B-2. Sample of Test Program

TABLE B-1.
EXERCISER DYNAMIC INSTRUCTIONS

	Odd Column Punch		Even Column Punch
Execute Recorder Operation	&	Hold Step Until Recorder is not Busy	&
RECORDER OFF	-	Hold Step for A Count	-
RECORDER ON	0	Scope Sync	0
Recorder Mode	1	Stop Test	1
Recorder Mode	2	Spare	2
Recorder Mode	3	Clear Registers (Except A)	3
END LOOP	4	Clear A Register	4
BEGIN LOOP	5	Write Data	5
TEST FOR ERROR	6	Stop on Errors	6
Hold Step for B Count	7	Hold Step Until Track is Full	7
CLOCK OPTION	8	Turn Track OFF	8

Punch 9 is for Static Instructions.

B.2 Program Example

To illustrate recorder testing using the exerciser the program given in Figure B-2 will be described. This program is used to examine the data flow into the recorder and the output data of the recorder. Since this test is a functional test of electronics and memory chip the program doesn't specify error analysis. During step zero the recorder is turned on, exerciser counters are cleared, and the oscilloscope is sent a synchronization pulse. Step one is for turning the track on in the write mode which makes the track receptive to data and the data's clock. During step two data is fed into the recorder in decade increments minus a single bit so to fill the track with a precise number of 8-bit patterns,an extra single write is done in step three. Step 4 is a recorder shut-off which clears and shuts down the recorder and Step 5 is another turn-on. A loop is created between Steps 6, 7, and 8. During Step 8 a request is made from the recorder for 8-bits of data. A slower clock is used since the request shouldn't be made more often than every 8-bits. The total number of repeats possible in this loop is 10^{11}requests for 8-bits but normally only 10,000 is specified for functional testing. Finally, Step 9 is for turning the track off. Dynamic punches for program control are given in Table B-1 but the static instructions specified by "9" in the punch column are not. These instructions are functions such as the card number display.

The main purpose for an exerciser of this type was to provide flexibility during the program by allowing construction when neither the tests nor the functions were firmly defined. A photo of the exerciser is shown in Figure 104. As the feasibility model program developed, the exerciser was used first to evaluate itself, then to perform a series of functional tests on recorder functions such as sensing, and finally was used to evaluate recorder performance in terms of error rates under simulated environmental conditions.

B.3 Prototype Exerciser

A sequential machine such as the feasibility model exerciser, but with expanded capability, is recommended for the testing of a prototype recorder. Features the exerciser should have include the following:

1. Function Control - On the order of 30 to 40 commands will be required to exercise the recorder through power up/down cycles, chip addressing, voltage margining, scope synchronization, multiple track operation, etc.

2. Computer Compatibility - A RAM is suggested as an adjunct to the reader so that communication with a computer or to I/O devices such as a terminal is possible. The computer will be freed from real-time control by the exerciser control so that it would be available for data analysis (schmooing plotting etc.).

3. Production Compatibility - An exerciser can be useful in both production and engineering provided a fixed set of certifiable function parameters is available to production and a variable set including computer control is available for engineering tests. A number of static control bits can be provided for this capability.

4. Submodule Test Capability - By putting a section of characterized and certified system electronics under dynamic function control it becomes possible to extend the capability of the system exerciser to include the evaluation of a submodule such as a memory coil package.

APPENDIX C.
THE LONG TERM RELIABILITY OF THE BUBBLE MEMORY CHIP*

It has been reported (Ref 30) that when magnetic bubble domains are propagated in the permalloy circuit, it has a certain probability of failure which is proportional to the number of steps it operated in the device. In this section, some measurements on the reliability of the memory chip will be discussed. The test chip was a 10k bit memory chip fabricated on YSmGaIG which is identical to those to be delivered under Task 9 of this program. The basic model on the long term reliability problem will be first discussed followed by a description of the measuring procedure and finally some measurement results will be presented and discussed.

C.1 Basic Assumption

The devices studied here are propagated under sufficient driving field so that the errors occur by bubble collapse at the high bias margin end or by splitting in two at the low bias margin end. The occurrence of errors is assumed to be random and can be represented by a probability function P. The value of P is a function of the bias field and independent of the number of steps the bubble propagates. This probability function varies with the device parameters (such as critical velocity of the material, velocity fluctuation in the device design etc.) and operating conditions (driving field, temperature etc.).

Under this assumption the number of errors, E, occurring after a number of propagation steps, S, can be represented as:

$$\Delta E/_{\Delta S} = PN \tag{C-1}$$

where N is the total number of bubbles in the device at Step S. For S=0 the total number of bubbles is N_0 and

$$N_0 = N + E \tag{C-2}$$

If P is independent of N, Eq (C-1) can be solved as

$$E/_{N_0} = 1 - e^{-PS} \tag{C-3}$$

A mean step between failure (MSBT) then can be defined as:

$$MSBT = \frac{1}{P}$$

This value can be measured from the initial slope of E vs S plot and can be used as a comparison parameter for device long term reliability study.

*This part of work was performed under an in-house program.

A similar relation can be derived for the low bias field end of the margin where bubbles tend to split rather then to collapse. In this case it is assumed that for each error the bubble only splits.

C.2 Experimental Procedure

A 10^4 bit 24 μm period serial device (No. 9 on wafer 2-18-45 $Y_{2.62}Sm_{0.38}Ga_{1.15}Fe_{3.85}O_{12}$) was used for this study. The device was propagated continuously in a high reliability exerciser. The chip was populated with repetitive 8-bit words and monitored through the detector circuit. An error counter was used to count the number of errors in 10^4 memory cycles, at a rate about 1 Hz and another counter was used to register the total operating steps. At the beginning of each measurement a controlled word pattern was written into the register, either with the bias field set at the desirable value or at a lower value where the bubble pattern can be correctly written and then adjusted to the desirable value. As soon as the pattern was correctly written and the bias field was adjusted, the step counter started to count the propagation steps and the number of errors in the register was recorded along with the number of propagation steps. The Error vs Step curve was then plotted on log-log graph, and the value of $1/_P$ was determined by extrapolating the linear part of the curve to $E/_{No} = 1$. Long term reliability plots were obtained at different bias settings by repeating the above procedure. The reproducibility of these curves is generally good (less than 20 percent) if the bias field and temperature are controlled correctly.

C.3 Measurement Results

A typical error vs step plot for device operated at high bias field end is shown in Figure C-1. When the error rate is high, the curve fits closely with the model (Eq (C-3)). At lower bias field setting, the error rate curve deviates from the model which could be attributed by the temperature drift in this relatively long measureing period. (The temperature may have dropped a few degrees during the measurement which is sufficient to cause an effective bias variation of a few tenth Oersted.) However, the MSBT value may still be able determined from the initial stop of these plots.

Figure C-2 shows a bias vs MSBF plot for 150 kHz, 250 kHz, and 350 kHz. The slope generally is less than 0.3 Oe per decade. A detail comparison between slopes is difficult because of the experimental accuracy (the bias field can only be read to 0.1 Oe and temperature cannot be well controlled). As can be seen in Figure C-1 there is no significant difference in the margin shrinkage curve between 150 kHz and 350 kHz at the high bias field end. But at the low bias field end both the 250 kHz and 350 kHz curves show an upward slop of about 0.3 Oe/decade. At 150 kHz the bubble tends to stripe out at the low end which causes a catastrophic failure (slope then is defined as zero).

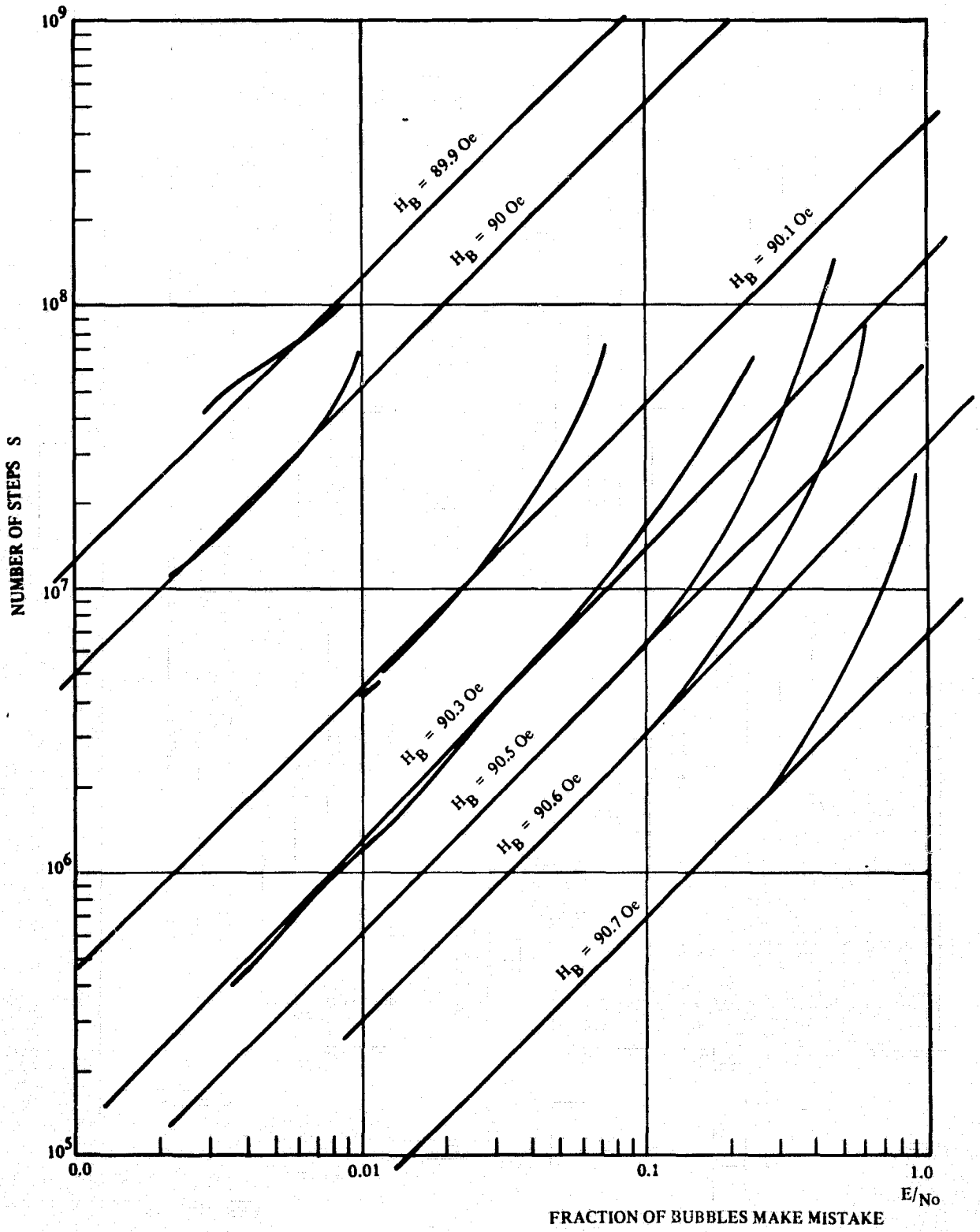


Figure C-1. Error Rate Measurement for a 1024-Bit Register. Operated at 250 kHz Under 50 Oe Driving Field

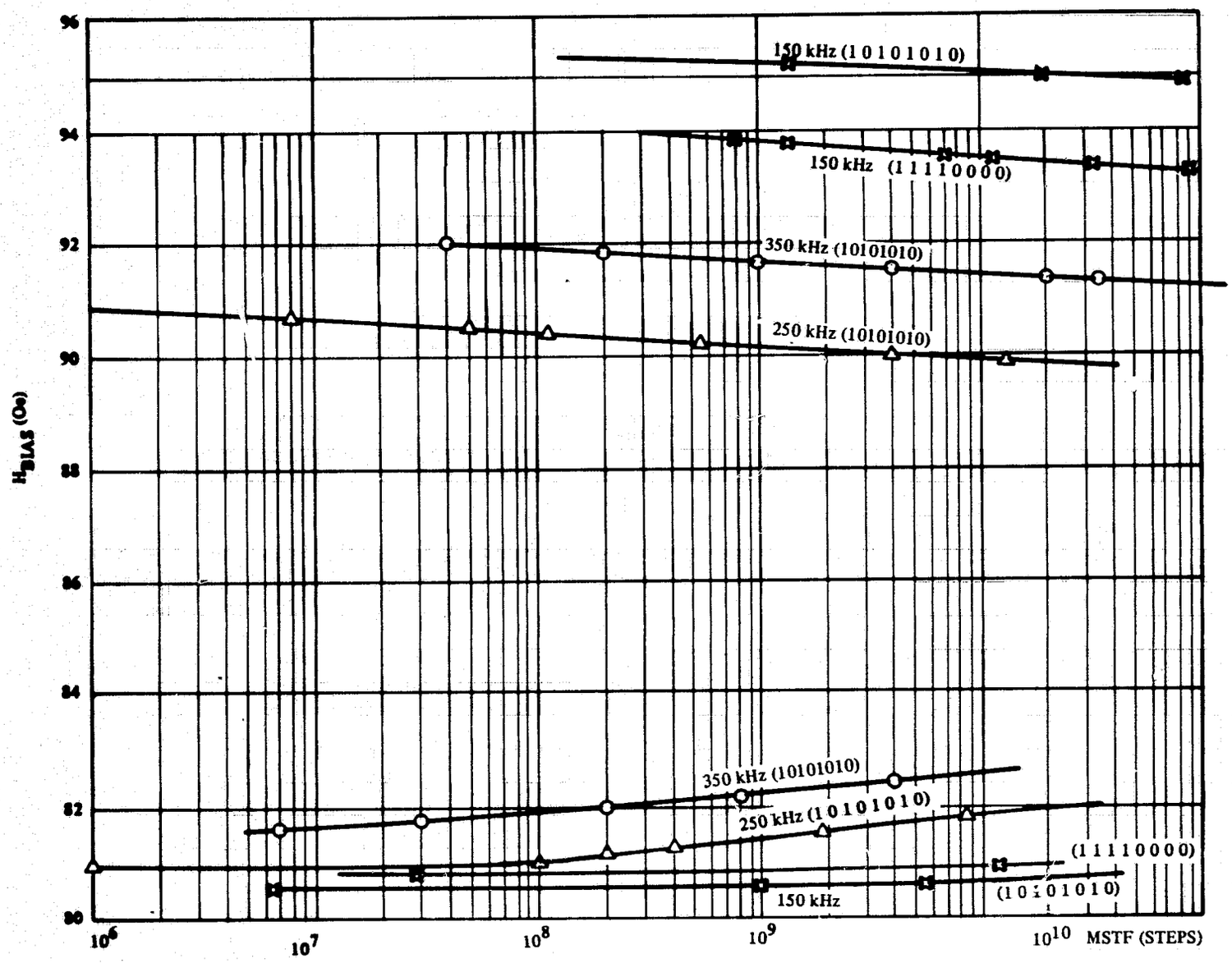


Figure C-2. MSBF as a Function of Bias Field for the 10^4 Bit Device Operated at 150 kHz, 250 kHz, and 350 kHz (At 350 kHz, a phase shift was introduced to the rotating field to optimize the propagation margin)

C.4 Discussion

Although the value of MSBF is directly related to the probability for bubbles making errors, this number does not really represent the hard error rate one can expect for the device or system. This is because all bubbles are being manipulated regardless whether they are read or not. In the recorder application the chips are grouped in individual coils. If the chip capacity is N_B and there are N_C chips in a coil to read the stored information in the coil once will manipulate each bubble stored in the chip by N_C N_B steps. If a hard error rate of P is expected from the recorder than the MSBF for the device should be better than $\frac{1}{P} N_B N_C$. In the prototype design $N_B = 10^5$, $N_C = 8$ if the specified error rate is 10^{-8} than the MSBF for the memory chip should be 10^{14}. The data shown in Figure C-1 indicates a margin reduction slope less than 0.3 Oe/decade at 150 kHz. For the type of margin measurement discussed in Para 10.1 with an error rate about 10^{-4}, an additional 3 Oe has to be deducted from the available bias margin. In view of the fact that present devices have a bias margin more than 12 Oe this 3 Oe reduction would not seriously limit the device operation.

This long term margin measurement proves the reliability of the material and the basic device design. This margin shrinkage effect depends on the device bias field only. When operated in a gated mode, turn-on and turn-off of the rotating field will introduce additional margin limitation due to the bubble stop conditions, but it should not vary the basic nature of the margin shrinkage effect from the continuous operating condition. With proper device fabrication and a dc holding field applied to the device the gated operation should not be a serious problem.

NEW TECHNOLOGY APPENDIX

A major accomplishment of this program is the demonstration of the feasibility of the bubble domain recorder with operating characteristics exceeding the original design goals. Other significant achievements on the program are listed in the following.

1. A polymer packaging concept and a via construction technique are proposed which can significantly reduce the package size, complexity and improve the package reliability (Para 3.1, polymer package. P. F. 74E10, "Substrate for Chip." O. D. Bohning and C. L. Zachry, Jan. 1974*, also P. F. 74E185, "Printed Circuit System," C. L. Zachry and A. J. Niezwiecke, Sept 1974.)

2. A bridge amplifier circuit is developed for bubble detection which can be integrated with the diode selecting matrix thus simplifying the electronic system. (Para 4.5, Sensing and Detection, P. F. 74E40, "Bridge/ Amplifier" O. D. Bohning, Feb. 1974)

3. A strip line coil structure is proposed for rotating field generation. This coil is simple, easy to control, has low a-c loss and can be shaped to have maximum field unformity. (Para 5.1.4, Strip Line Coil, P.F. 74E67, "A Strip Line Coil Design for Magnetic Field Generation in Bubble Memory Devices," T. T. Chen and J. E. Ypma, April 1974 and P. F. 74E114, "A Low Loss Strip Line Coil for Magnetic Memory Devices," T. T. Chen and C. L. Zachry, June 1974.)

4. An open coil structure concept is suggested using ferrite plate cores for rotating field generation. The bubble memory devices can be packaged separately with the coil structure thus simplifing the package and increasing the packaging reliability. This coil structure can also be adopted for wafer inspection and package testing which simplifies the testing procedure. (Para 5.2.3, Ferrite Coil Structure, P.F. 74E66, "An Open Coil Structure for Bubble Memory Device Packaging," T. T. Chen, J. E. Ypma, April 1974, and P.F. 74E82, "Bubble Domain Circuit Evaluation Coil Set," T. T. Chen, J. L. Williams, April 1974)

5. For bias structure design, a multiple gap structure is proposed which enables bubble chips with different bias margin requirements to share one single bias structure. (Para 6.4, A Multiple Gap Bias Field Structure, P. F. 74E175, "A Variable Gap Bias Structure for Magnetic Bubble Memory Package," T. T. Chen, Sept. 1974)

6. An improved chip organization for recorder application using a passive replicator and annihilator combination so that all chip control functions can be aligned to the same bit position. This arrangement simplifies the electronic control system and also adds flexibility in the detector circuit. (Para 9.1, Chip Organization Prototype Recorder.)

*Some of the achievements were filed in the form of patent disclosures, the information listed here are the file number, title, authors and filing date.

7. The instability problem in the bubble memory device under gated operation mode has been identified and a bias tilting arrangement has been adopted to enhance the bubble stability and also compensates the overshoot in the rotating field turnoff waveform. (Para 7.2, Tolerance in Magnetic Field Network).

8. A magnetoresistance probe is proposed for bias field alignment on the memory device package. The structure is simple and the sensitivity has been demonstrated to be better than 0.2 deg. (Appendix A. A PMR Probe for Field Measurement, P. F. 74E165, "A Planar Magnetoresistance Thin Film Probe for Magnetic Field Alignment," T. T. Chen, Aug. 1974. First reported under contract F19628-72-C-0342.)

REFERENCES

1. L. R. Tocci, et al, "Magnetic Bubble Memory," Technical Report Air Force Avionics Lab., Wright Patterson Air Force Base, Ohio, AFAL-TR-74-171, 1974.

2. R. F. Bailey, J. L. Williams, "Temperature Step Anneal Effects on the Physical and Magnetic Properties of Permalloy Films," Paper 220, Elec. Chem. Soc. Meetings, Chicago, Ill., May 1973.

3. J. Shaheen, et al, "Beamleaded Interconnection for Bubble Memory Devices," Materials and Process Report, TR74-241-047-MLB/PCB-13, Rockwell International, 1974.

4. A. Gangulee, C. H. Bajorek, F. M. d'Heurle and A. F. Magadas, "Long Term Stability of Magnetoresistive Bubble Detectors," IEEE Trans. Mag. MAG-10, 1974 p 848.

5. A. D. Sypherd and Q. C. Cassen, "System Design Concepts Using SOS Programmable Logic Arrays," Paper 28-3 IEEE INTERCON, New York, N. Y., Mar. 1974.

6. G. S. Almasi, and G. E. Keefe, "High Speed Sensing of Small Bubble Domains," AIP Conf. Proc. No. 10, 97, p 251.

7. F. E. Terman, Radio Engineers' Handbook, McGraw Hill, N.Y. 1943, p 85.

8. Ibid, p 74

9. Ibid, p 37

10. Ibid, p 84

11. R. F. Plachy, "A Solid State Replacement for Satellite Tape Recorder," Technical Memorandum, John Hopkins Univ., T. G. 1194, July 1972.

12. H. Maegawa, J. Matsuda, and M. Takasu, "Flat Packaging of Magnetic Bubble Devices," IEEE Trans. Mag. MAG 10, 1974, p 753.

13. L. J. Richmond and D. W. Parker, "An Economical Method of Magnet Construction giving a Large Volume of High Homogenity Field," Int. Conf. Magnet Tech. 1867, Rutherford Laboratory Publication, 1967, p 129.

14. H. C. Roters, Electromagnetic Devices. John Wiley and Sons, N.Y. 1942 p 126.

15. R. G. Wolfshagen, Private Communication.

16. D. S. Bartran and L. G. Chow, "Analysis of Magnetic Fields Encountered Between Two Permeable Sheets," IEEE Trans. Mag. MAG 10, 1974, p 379.

17. F. E. Terman, Radio Engineers' Handbook, McGraw Hill, N.Y. 1943, p 128.

18. L. R. Tocci, et al, "Magnetic Bubble Memory," Final Report, Contract F33615-73-G1105, Air Force Avionics Lab., Wright Patterson Air Force Base, Ohio. To be published. Also I. S. Gergis, T. T. Chen, and L. R. Tocci, "The Effect of D. C. Inplane Field on the Operation of Field Access Bubble Memory Device," to be published.

19. T. T. Chen, P. K. George, L. R. Tocci and J. L. Archer, "A Study on the Chevron Thick Film Detector," AIP Conf. Proc. 18, p 115, 1973.

20. P. I. Bonyhard, J. E. Geusic, A. H. Bobeck, Y. S. Chen, P. C. Michaelis and J. L. Smith, "Magnetic Bubble Memory Chip Design," IEEE Trans. MAG 9, 1973, p 433.

21. R. F. Bailey and J. P. Reekstin, "Yield Analysis of Large Capacity Magnetic Bubble Circuits with Redundance Design, "IEEE Trans. Mag. MAG 10, 1974 p 856.

22. A. H. Bobeck, et al, "Evolution of Bubble Circuits Processed by a Single Mask Level, "IEEE Trans. Magnetics MAG 9, p 470, 1973.

23. T. J. Nelson, "Progress in All-Permalloy Bubble Control Functions," AIP Conf. Proc. No. 18, p 95, 1974.

24. T. J. Nelson, "Passive Replicator for Magnetic Bubbles, 20th 3M Conf. San Francisco, Dec. 1974.

25. R. B. Stermer, private communication.

26. P. C. Michaelis, "Magnetic Bubble Mass Memory, "INTERMAG Conf. Paper 22.1, Toronto, 1974.

27. R. A. Baugh, R. B. Clover, L. S. Cutler, R. L. Lacey, and R. F. Waites, "Some Aspects of Bubble Memory Module Design," INTERMAG Conf. Paper 22.2, Toronto, 1974.

28. H. Uchishiba, H. Tominaga, T. Obokata and T. Namikata, "Growth and Properties of Stable Self-Biasing Double Layer Epitaxial Garnet Films," IEEE Trans. MAG 10. 1974, p A80.

29. P. J. Besser and T. N. Hamilton, "Investigation of Chemical Vapor Deposition of Garnet Films for Bubble Domain Memories," Contract Report NASA CR-132325, Section 7. October, 1973.

30. P. W. Shumate, P. C. Michaelis and R. J. Pierce, "Long-Term Propagation Studies in Magnetic-Bubble Devices, AIP Conf. Proc. No. 18, 1974, p 140.

31. T. T. Chen and V. A. Marsocci, "Planar Magnetoresistivity and Planar Hall Effect in Nickel Single Crystal Films," Physica 59, 1972, p H98