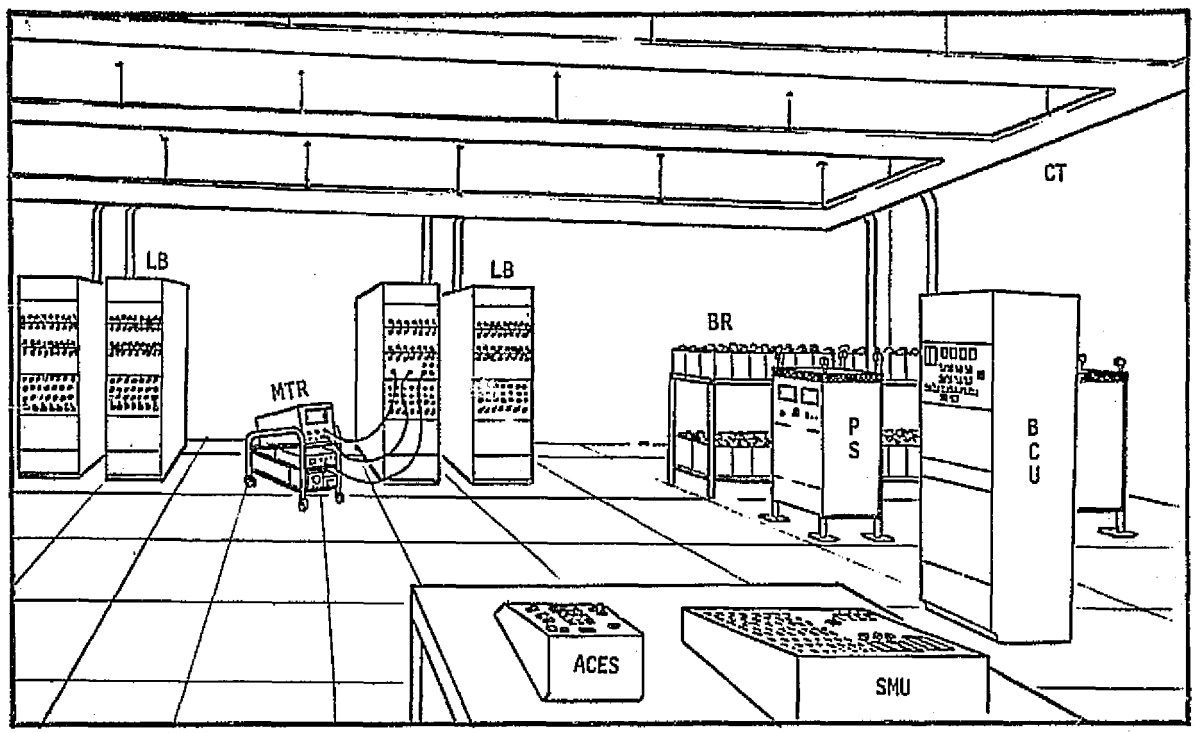
# RESEARCH STUDY ON MULTI-KW DC DISTRIBUTION SYSTEM






MAY 1975

FINAL REPORT

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Prepared for

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# ACRONYMS

| | |
|---|---|
| ACES | Automatically Controlled Electrical Systems |
| BCU | Bus Control Unit |
| BIT | Built in Test (ACES) |
| DCC | Distribution Control Center (ACES) |
| DED | Data Entry and Display (ACES) |
| HVDC | High Voltage DC |
| ICAP | Interactive Circuit Analysis Program |
| PWM | Pulse Width Modulator |
| RIO | Remote Input Output Unit (ACES) |
| RPC | Remote Power Controller |
| SMU | Supervision and Monitor Unit |
| SSRPC | Solid State Remote Power Controller |
| TB | Terminal Board |

# 1.0 INTRODUCTION

## 1.1 BACKGROUND

This report summarizes the results of work performed in the second phase of a study program to demonstrate technology readiness for advanced power distribution system design concepts.

This program was planned on the basis of recommendations resulting from a comprehensive "Space Vehicle Electrical Power Processing Distribution and Control Study", (NAS8-26270) performed by TRW Systems as part of the NASA space vehicle technology development program. The objectives of the first year of this program "Multi-KW DC Distribution System Study" (NAS8-28726) were:

- Provide detailed definition of the program and test objectives
- Make recommendation for selection and sizing of the test facility
- Evaluate high voltage dc power distribution system state-of-art and availability of test hardware

This study was completed successfully April 1974. The objective of the second phase of effort which is the subject of this report was to provide sufficiently detailed definitions of test facility subsystems to enable planning and installation of the test facility by Marshall Space Flight Center personnel. The subsequent phases of this program will provide support for procurement and installation of the test facility, system test planning and evaluation.

## 1.2 SCOPE OF WORK

The second phase of the Power Processing, Distribution and Control Development Program is a continuation of the TRW and MSFC in-house effort. It consists of:

- Completion of the detailed design, fabrication and installation of the technology breadboard.
- Selection of electromechanical and solid state relays, circuit breakers, remote power controllers and associated control and display equipment.

- Design of filtering and isolation circuits which are to be evaluated in the technology breadboard.

TRW Systems efforts are limited to design analysis and tradeoff studies. All procurement, fabrication and installation of equipment for the technology breadboard will be performed by NASA/MSFC.

# 2.0 SUMMARY AND CONCLUSION

## 2.1 PROGRAM OBJECTIVES

The primary objective of this second phase of the Multi-KW DC Distribution System Study is to provide a detailed definition of the HVDC Test Facility and the equipment required to implement the test program. The basic elements of the Test Facility are illustrated in Figure 2.1-1 and consist of the power source, conventional and digital supervision and control equipment, power distribution harness and simulated loads. The regulated DC power supplies provide steady-state power up to 36 KW at 120 VDC. Power for simulated line faults will be obtained from two banks of 90 ampere-hour lead-acid batteries. The relative merits of conventional and multiplexed power control will be demonstrated by the Supervision and Monitor Unit (SMU) and the Automatically Controlled Electrical Systems (ACES) hardware. The distribution harness is supported by a metal duct which is bonded to all component structures and functions as the system ground plane. The Load Banks contain passive resistance and reactance loads, solid state power controllers and active pulse width modulated loads. The HVDC Test Facility is designed to simulate a power distribution system for large aerospace vehicles. System cost has been minimized by selection of industrial quality components and extensive use of model shop approaches.

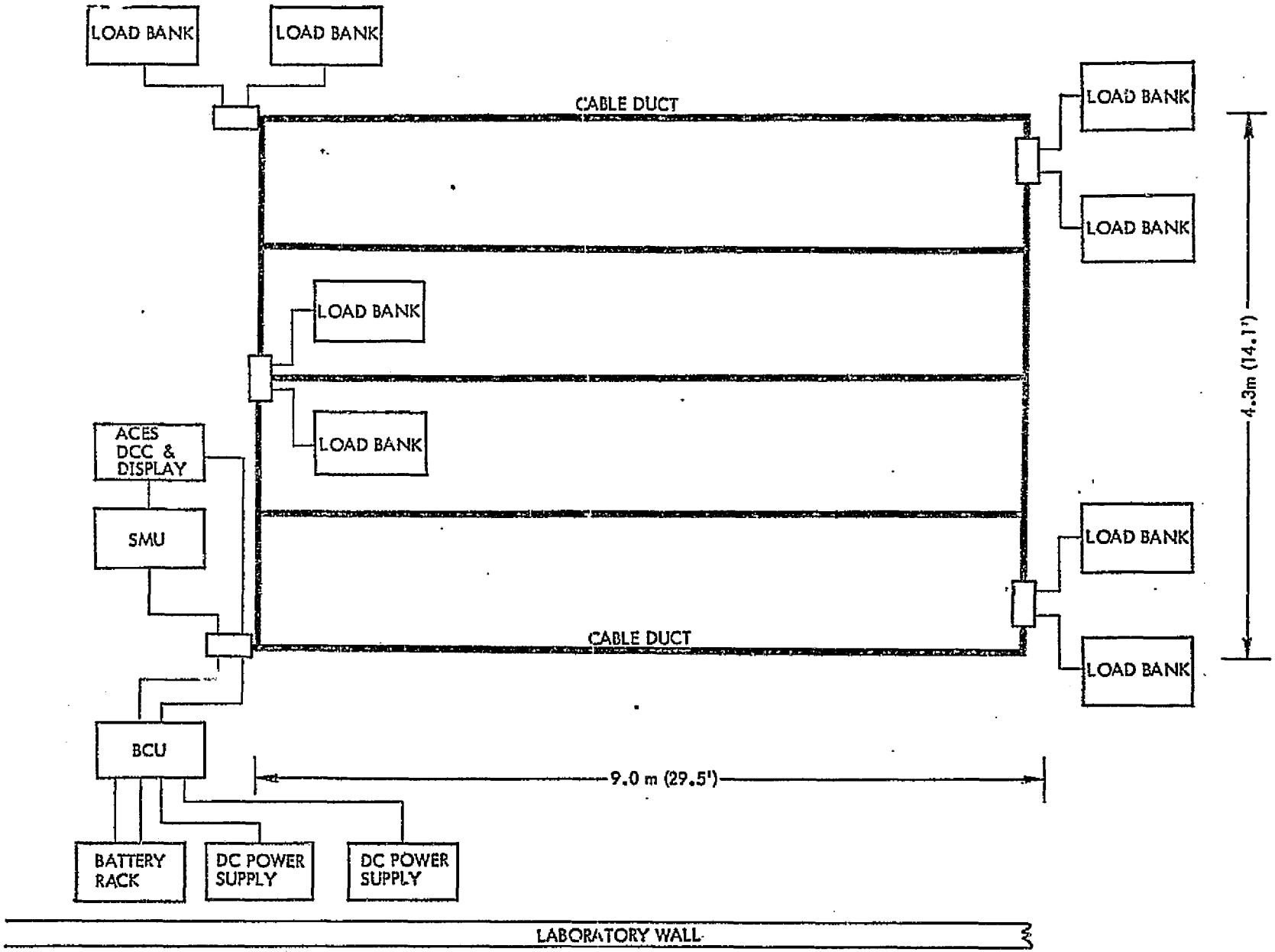



Figure 2.1-1. Test Facility Elements

## 2.2 TEST FACILITY

Relocation of the laboratory has required minor modification of the Test Facility configuration defined in Phase 1. Batteries and high dissipation components have been moved into the laboratory area since an outside platform is no longer available. Forced ventilation required for these elements has been included in the design. Further study of the test site will be performed by MSFC engineers to evaluate the benefits of relocating the high dissipation elements to the roof of the building.

The second phase of the advanced power distribution, supervision and control methods study at TRW includes the detailed design of the load banks, supervision and monitor unit, power source, cable mock-up, filter and isolation circuits. These tasks have been completed and are described in detail in Section 3.1 of this report. Procurement, assembly, installation and test of HVDC equipment is to be performed at MSFC. In addition to the minimum requirements of the contract tasks, analysis of Test Facility circuit designs and distribution cable parameters have been performed to improve system effectiveness and provide basic criteria for component and subsystem tests.

### 2.2.1 Load Bank Design

Engineering drawings have been completed for all load bank panels and electronic circuits. Interconnecting wiring between load bank components and between the load bank and other system elements has been defined. The initial design of the Pulse Width Modulator (PWM) provides a 500 watt dynamic load and an expected 1.5 KW ultimate load. The PWM design provides frequency control from 5 KHz to 15 KHz and duty cycle control from 5% to 95%. Pulse width modulated converters and regulators will be simulated with this design. The control and monitor interface has been designed to be compatible with the ACES Remote Input/Output (RIO) hardware. These interfaces are connected at all times and conventional or multiplexed data-bus control can be selected from the control panels. Both monitoring systems can be operated simultaneously to display data on each panel. Solid state switches have reached an advanced state of development and have been included in the Load Bank design. These devices offer a solution to several potential high voltage problems as well as existing noise problems at standard bus voltage levels.

### 2.2.2 Cable Mockup Design

Definition of the main bus cable and all conductors in the harness has been completed and is defined in detail in Section 3.3. The main bus utilizes #8 nickel coated stranded wire and will be assembled at MSFC. The conductors defined for control and supervision may be purchased as a completed cable or obtained from MSFC storage. The cable duct design has been modified from the continuous folded configuration defined in Phase 1 to a five element grid to allow more flexibility in the selection of cable run lengths. Testing will consist of continuity and insulation verification tests which may be performed in the Test Facility area.

### 2.2.3 Source Simulator Design

The source simulator design permits series and parallel connections of the power supplies and batteries. Power is normally supplied to the Bus Control Unit (BCU) from the power sources on an individual basis. Parallel configuration and battery charging modes are controlled at the BCU. Series configurations are implemented by manual controls at the Power Source switch panel. Each of the two battery packs consist of ten 90 ampere hour lead-acid batteries. The regulated power supplies provide up to 150 amperes at 2 -135 volts and are regulated to 0.1%. These components are designed to simulate a fuel cell power source for a large space vehicle. Details of the design may be found in Section 3.4 of this report.

### 2.2.4 Supervision and Control

The supervision and control systems for the Test Facility consist of the Supervision and Monitor Unit (SMU) and the Automatically Controlled Electrical Systems (ACES) hardware. The SMU utilizes hardwire connections, bi-level controls, bi-level and analog displays. The ACES power management system makes use of a multiplexed data bus for bi-level control and display functions. The features of this digital system include triple redundancy, programmed load management, automated load shedding and built-in-test (BIT). All interfaces between the two systems are at the locations of the control and monitor functions. The design permits display of monitored functions on both panels simultaneously. Control "ON" conditions may be implemented from either system on a logical "OR" basis.

Details of the design and schematic drawings are presented in Section 3.5 of this report.

### 2.2.5 Filters and Isolation Circuits

Steady-state and transient interference limits were defined for this system based on extrapolation of MIL-STD-461A and MIL-STD-704 requirements. Allowable voltage noise generation limits were set 6db below the susceptibility limits defined in these standards. Conducted interference was calculated on the basis of source impedance presented at the load terminals of the distribution cable. Impedance for the nickel coated #8 wire was calculated for a range of frequencies by a computer program developed during this contractual period. Analysis of equivalent systems demonstrated a 17db noise advantage for 120 VDC systems compared to 28 VDC systems at higher frequencies. Filter designs for 500 watt regulated converters for a range of frequencies from 1KHz to 20KHz were calculated on the basis of the generated EMI limits. Electrical and physical filter parameters and details of the EMI analysis are presented in Appendix B and Section 3.6 respectively of this report.

### 2.2.6 Conclusions

This phase of the Multi-KW DC Distribution Study has provided a detail design of the Test Facility Subsystems. Facility configurations, electrical and electronic design were verified by analysis and computer simulation. Schematic drawings have been completed, major procurement items and piece parts have been identified and vendors recommended where appropriate. Further verification of Test Facility subsystems performance and validation of the detail design will be obtained by MSFC test of procured components and breadboard models.

# 3.0 DETAILED TECHNICAL DESCRIPTION

## 3.1 INTRODUCTION

The basic purpose of the Multi-KW Distribution System Study and associated NASA/MSFC in-house effort is to demonstrate technology readiness and performance advantage of high voltage dc (HVDC) distribution and control systems for large manned aerospace vehicles. This demonstration is to be accomplished through operation and test of a technology breadboard which simulates an advanced design power system and includes power source, distribution, loads, supervision and control functions. The continued development of solid state power controllers provides additional impetus to the interest in high voltage distribution systems. These devices are currently gaining acceptance for space applications and can provide a solution to high voltage power switching problems. It is planned to include several solid state remote power controllers in the technology breadboard to demonstrate their performance and compatibility with the power distribution system. Conventional bi-level/analog control and display systems are placing increased penalties on system cost, weight size, complexity, and reliability. Several power management systems have been defined which utilize a digital multiplexed data bus and a small special design programmable computer. It is anticipated that near term state-of-art power systems will employ this control and display approach. The HVDC Test Facility interfaces have been designed to be compatible with both the conventional and a digital computer controlled power management system. The conventional control and display console was designed under this contract and approximates the SKYLAB approach. The Automatically Controlled Electrical System (ACES) digital control and display hardware were developed by Westinghouse and will be available for use in the completed Test Facility at MSFC.

### 3.1.1 Functional Description

The basic configuration of the HVDC Test Facility is illustrated in Figure 3.1.1-1. The technology breadboard is comprised of two sets of battery packs and regulated power supplies, Bus Control Unit (BCU), distribution cable, Load Banks and supervision and control equipment. The last consists of the Supervision and Monitor Unit (SMU) and ACES.

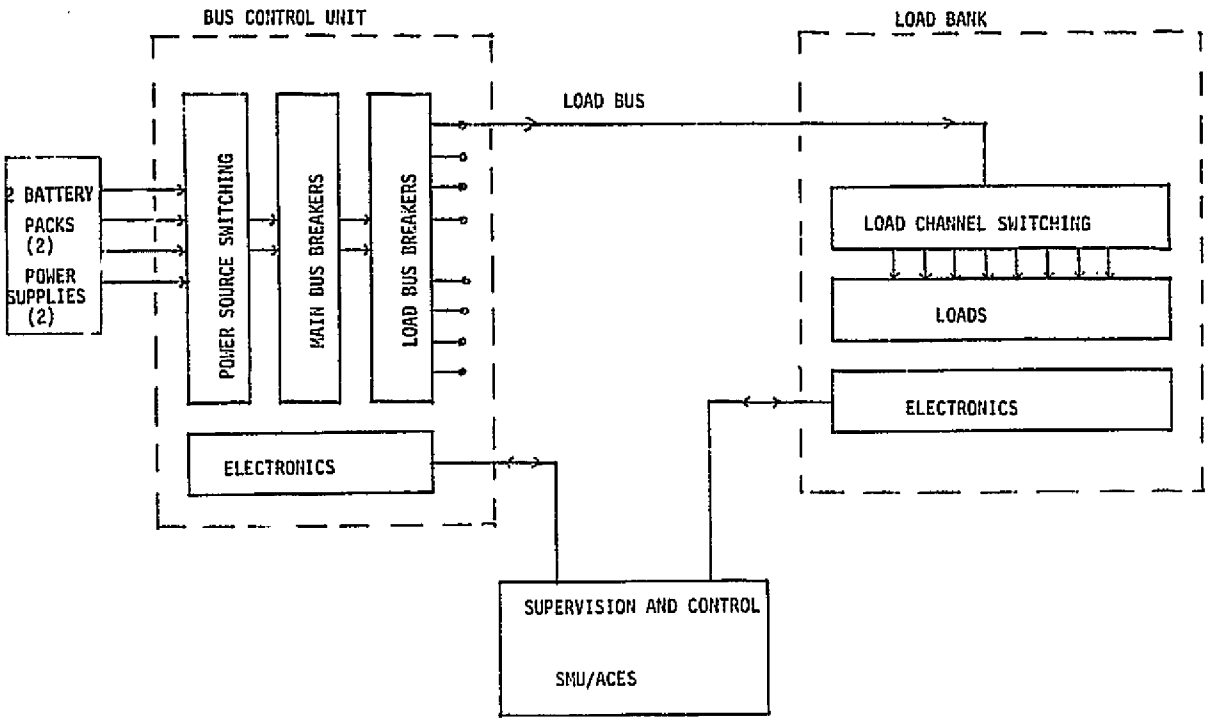



Figure 3.1.1-1. Functional Block Diagram ∿ Test Facility

The battery and voltage regulator power source can be reconfigured to provide voltage from 28 to 240 VDC and may supply up to 36 KW at 120 VDC. The BCU serves as a aerospace bus control panel and performs bus control, major fault protection and battery charge control functions. Power from the batteries and regulated power supplies is applied to two main buses in the BCU, which may then supply the power to as many as eight separate Load Banks via the power distribution harness. This design models the main bus/redundant bus configuration standard in aerospace applications. Each load bank simulates passive and dynamic load interfaces with eight individually controlled load channels. The load design includes filter designs which ensure that distribution cable noise does not exceed the limits of MIL-STD-461A. The supervision and control equipment (SMU and ACES) interfaces with remote power controller and status monitor circuitry in the BCU and the Load Banks. All wiring and cabling which runs between the supervision and control equipment, the Load Banks and the BCU is carried in a duct which simulates the space vehicle structural ground plane.

## 3.2 LOAD BANK DESIGN

The load banks provide the power utilization equipment characteristics necessary to demonstrate the steady state and dynamic performance of the power distribution system for line voltages from 28 to 300 Vdc. The load banks also serve as a test bed for state-of-art RPCs (Remote Power Controllers) and ACES (Automatically Controlled Electrical System). The design of the load banks will provide simulation of the characteristics of spacecraft equipment which is in current use or proposed for future applications. Surplus or industrial quality components are to be used for loads where available since the direct purchase of space qualified hardware is not consistent with planned program funding. The electrical power interface between the load banks and the Test Facility elements is illustrated in Figure 3.2-1.

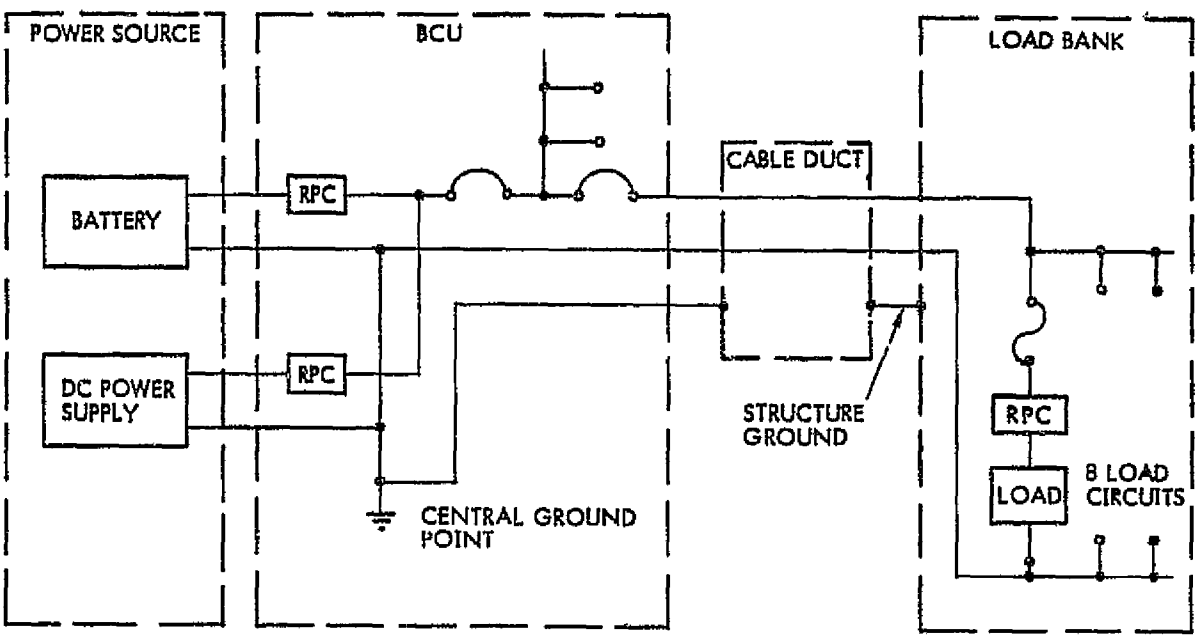



Figure 3.2-1. Power Distribution Circuit Elements

Power from the regulated supply and/or the battery is switched to the load bank bus at the BCU. The load bank provides eight parallel load paths consisting of R, L and C networks, a solid state RPC with resistive load and a Pulse Width Modulator (PWM) which simulates solid state regulator/converter operation. Loads may be modified by patch cords which provide a means for flexible reconfiguration.

### 3.2.1 Load Bank Functions

The load banks provide capability for space vehicle load simultion and observation of steady state and transient currents and voltages. The functions associated with one load channel are illustrated in Figure 3.2.1-1.

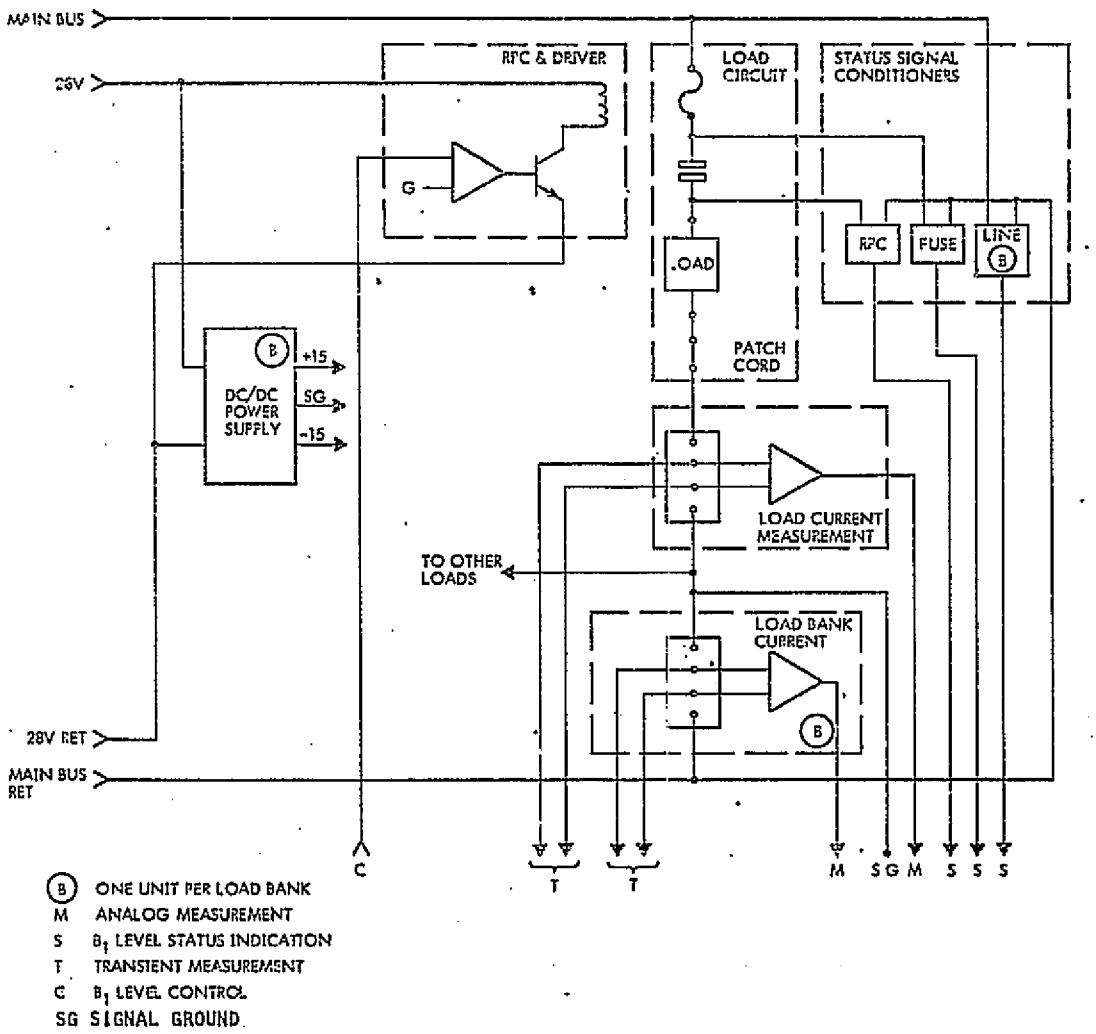
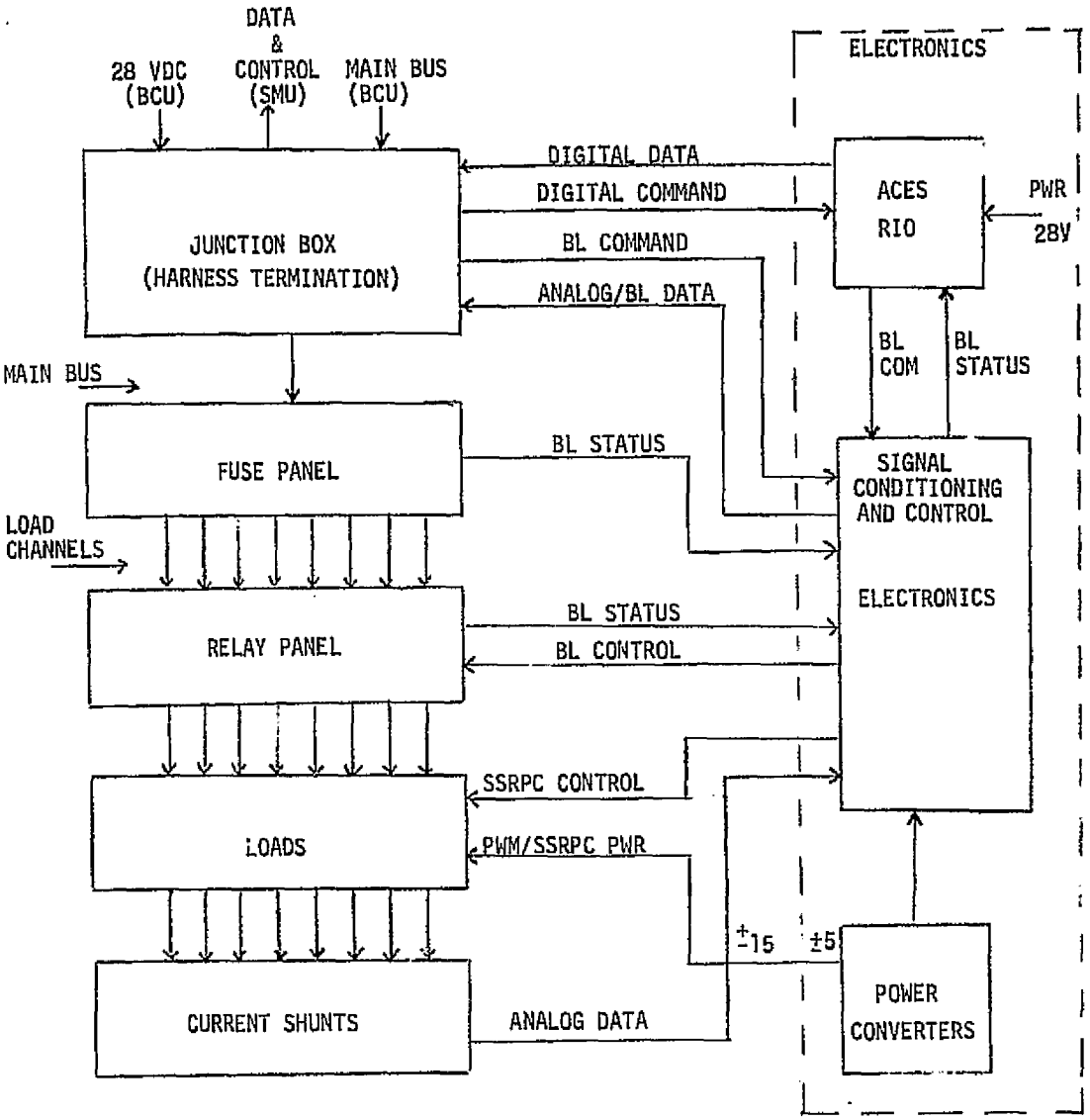



Figure 3.2.1-1. Functional Schematic for One Load Circuit

Each load circuit contains a fuse, contactor, simulated load and current shunt for measuring individual load current. Total load bank current is monitored by a current shunt in the common return. Operational states at fuses and contactors are sensed by the electronics to provide bi-level status signals to local and remote panel indicators. Analog signal transducers condition current shunt voltages to 0 - 5VDC for metering. Status signals and jacks for transient current measurements are provided on the front of the load bank panels. Steady-state current and voltage measurements and status signals are displayed on the SMU panel. Status signals are also monitored by ACES and displayed on the DED. Load channel contactors are operated by local switches on the front of the load bank panel or remotely by the SMU or ACES on an "or" logic basis. Each load bank contains secondary power converters to provide required voltages and ground isolation for solid state signal conditioning circuits.

### 3.2.2 Load Bank Configuration

A load bank will be assembled on one or more standard equipment racks. Load bank components consist of a set of panel mounted assemblies for harness termination, fuses, relays, loads, current shunts, control electronics and power converters. These components and their electrical interfaces are illustrated in Figure 3.2.2-1. The harness termination panel serves as an electrical distribution box for control and supervision signals. With the exception of the main bus all harness conductors interface with Load Bank circuits through terminal strips on this panel. The use of terminal strips on all panels is consistent with the model shop approach and simplifies assembly and reconfiguration. The main bus goes directly to the fuse panel where it is divided into eight load channels. These channels then flow progressively through the fuse panel, relay panel, load panel and current shunt panel. The electronics provide load bank status monitoring, relay control drive and analog signal conditioning. ACES is a digital data bus control feature of the Test Facility. Details of this component are discussed in the succeeding paragraphs.




BL - Bi LEVEL
SSRPC - SOLID STATE REMOTE POWER CONTROLLER
PWM - PULSE WIDTH MODULATOR
ACES - AUTOMATICALLY CONTROLLED ELECTRICAL SYSTEM (WESTINGHOUSE DIGITAL CONTROL)
RIO - REMOTE INPUT/OUTPUT UNIT (ACES)

Figure 3.2.2-1. Load Bank Component Interfaces

### 3.2.2.1 Fuse and Relay Panels

The circuitry for the fuse and relay panels is shown in Figure 3.2.2.1-1. The main bus conductors terminate on TB1 and TB2. A twisted pair couples the voltage at this point directly to a test jack on the front of the Load Bank Test Panel for observation of bus voltage transients.

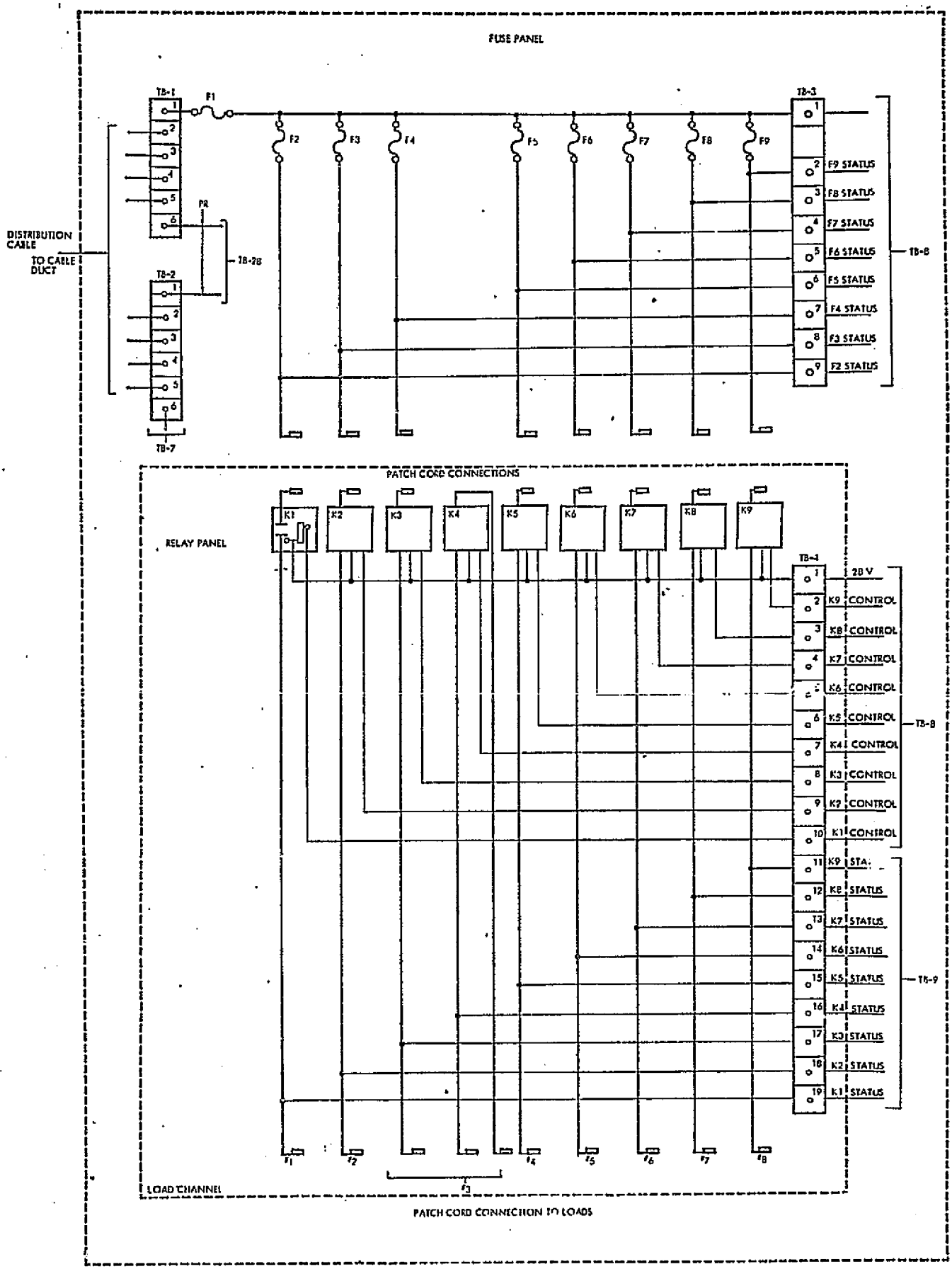



Figure 3.2.2.1-1. Fuse and Relay Panels

There are no protective impedances in this pair in accord with the need for measurement fidelity. The load bank and load channels are protected by fuse 1 (100 a) and fuses 2 through 9 (20 a) respectively. The ratings are nominal since appropriate fuses will be selected during operation for each test. Load channel current flows through fuses and patchcords (not shown) to the switchgear contacts on the relay panel. Relay 4 is in addition to the relays required for channel power control and will be used to simulate multiple switching transients. Open and close status is sensed by the electronics through connections to the load side of the fuses and relay contacts. Relays are operated by grounds applied to one side of the relay coils by the electronics control interface.

3.2.2.2 Load Panel

The load panel (Figure 3.2.2.2-1) provides steady-state, transient, passive and dynamic loads. Details of the panel mounted resistors, inductors and capacitors which simulate switching transients and fixed loads are defined in the Phase 1 report.

An auxiliary floor mounted resistive load is defined for loads which exceed the heat dissipation capability of a panel. Two high power load designs are required to provide resistive paths for 10, 20, 40, and 80 amperes at 28 and 120 VDC. Forced air ventilation will be required for these loads if they are operated in the laboratory due to the maximum thermal dissipation of 36 KW. The cost and effort involved with forced ventilation may be avoided if the high power loads are mounted on the roof of the building. Each load will require approximately four square feet of mounting area with a height of one and on/half feet. Sufficient space or protection for surrounding structure and roof should be provided due to radiated and convected heat. Temperature of effluent air is approximately 200°F; the temperature of the dissipative elements is not available at this time.

Panel mounted resistive loads are provided for the Solid State Remote Power Controller (SSRPC) and the Pulse Width Modulator (PWM). The design

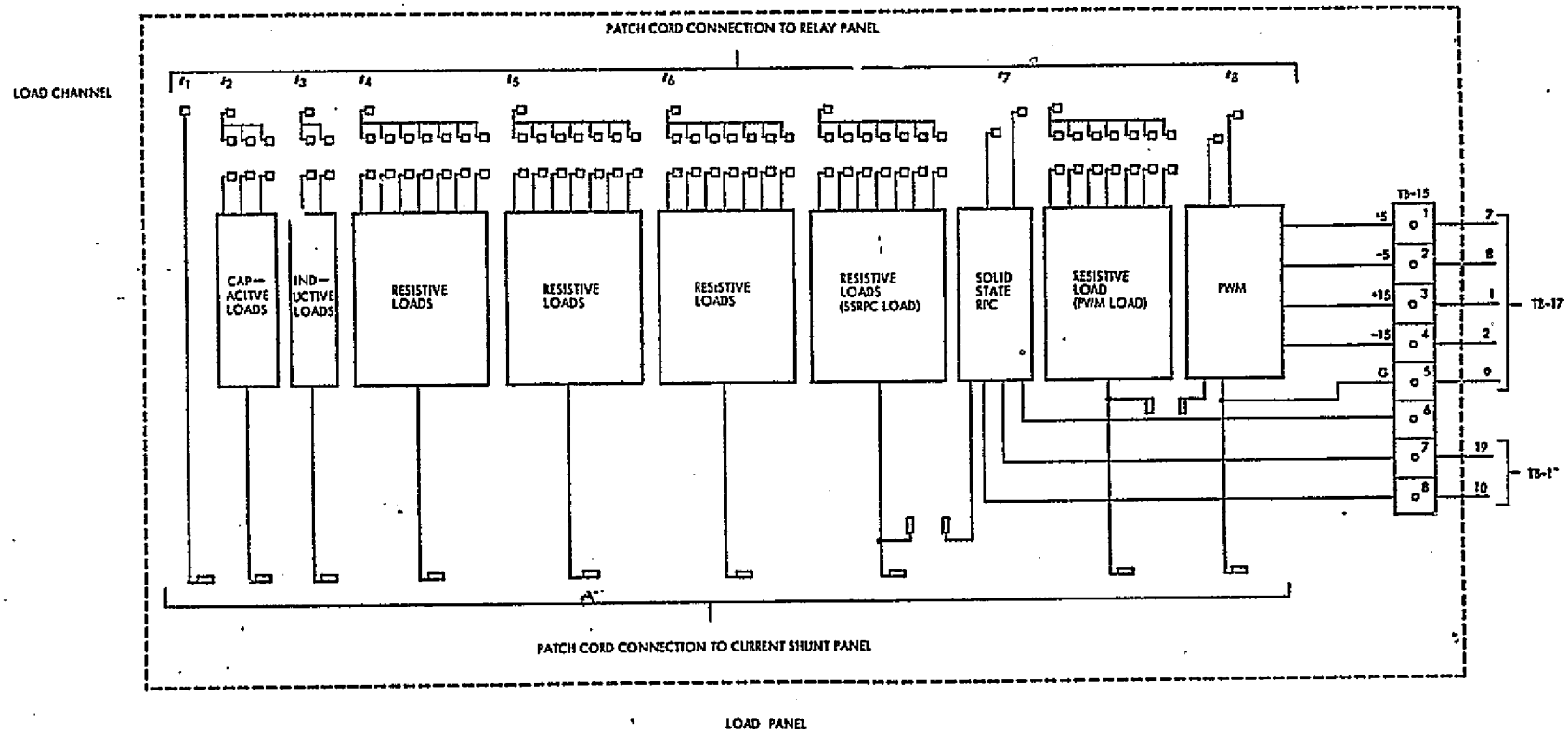



Figure 3.2.2.2-1. Load Bank Load Panel

of solid state switches circuit protection, limiting, etc. has advanced in recent years, and they are available for test at line voltages up to 120 VDC. These switches are expected to provide significant advantages with respect to speed of operation, descreased transient noise, fault current limiting, circuit protection, and remote controllability. The PWM will simulate pulse width modulated loads and converters. Frequency and pulsewidth are controlled manually in the present design but may be easily modified for remote control if necessary. Input filter designs are provided for a range of input voltages and currents in Appendix B. Recent developments and design of the SSRPC and the PWM are presented in subsequent sections on Load Bank Electronics. The SSRPC may interface with the electronics or ACES for status monitoring and control functions. The PWM requires ±15 and ±5 VDC power for operation from the Load Bank Secondary converters.

3.2.2.3 Current Shunt Panel

The current shunt panel illustrated in Figure 3.2.2.3-1 contains the transducer for measuring steady state and transient currents. Two twisted pairs are connected to each shunt. One pair provides an input to the electronics for analog signal conditioning, the other connects to jacks on the front of the load bank panel for transient measurements. Access to each shunt will be provided to permit direct measurement of current transients. The main bus ground (TB-2) is returned to the main bus termination on the fuse panel. The main bus ground is also connected to the electronics as signal ground for analog measurements. This signal ground configuration is necessary to avoid excessive stress on the signal conditioners during severe main bus transients.

3.2.3 Load Bank Electronics Design

The electronic components include ACES Remote Input Output (RIO) units, secondary power converters, Solid State Remote Power Controller (SSRPC), Pulse Width Modulator (PWM) and signal conditioning and control circuitry. The SSRPC will be obtained by MSFC from ongoing NASA development programs.

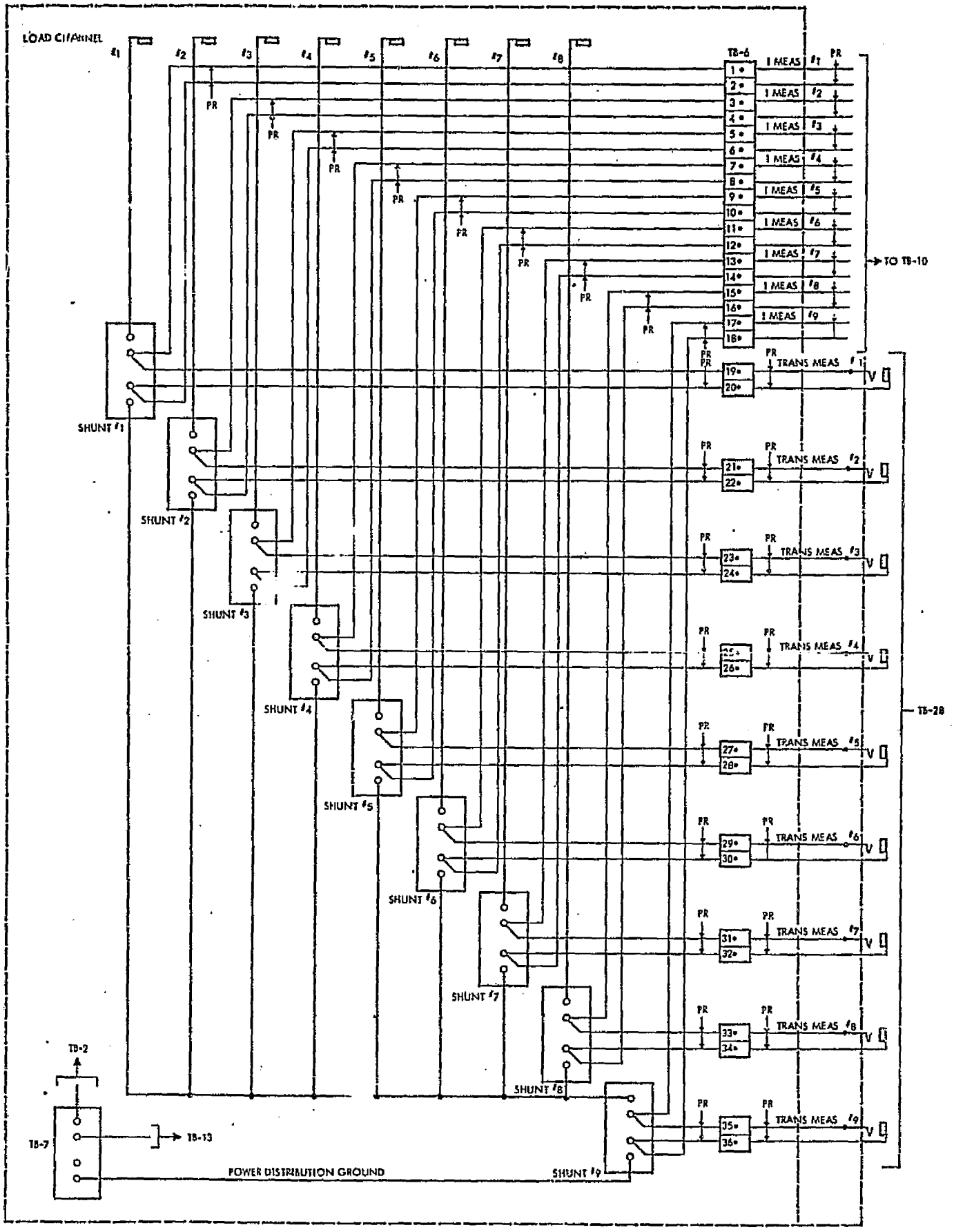



Figure 3.2.2.3-1. Current Shunt Panel

A limited supply of ACES components developed by Westinghouse are currently available at MSFC. Secondary power converters (28/±15, 28/±5) may be purchased economically from a vendor. The PWM, signal conditioning and control circuits are new designs which have been derived analytically and will require breadboard testing at MSFC.

3.2.3.1 Solid State Remote Power Controllers

SSRPC's have been designed for voltages from 28VDC to 120VDC in development programs sponsored by NASA LeRC and MSFC. Informal data indicate current features include capability to 30 amperes, automatic fault sensing, breaker functions, reset logic and bi-level status outputs. These developments are significant with respect to space vehicle design. Current power switchgear designs utilize relays with fuses as the most reliable method of fault protection for high currents. Quality control of relays and fuses is expensive and vendors oppose imposition of aerospace source controls; contact bounce and arcing generate conducted and radiated EMI. At higher currents and voltages, arcing becomes more severe and constitutes a safety hazard in a manned vehicle. Solid stage switchgear should provide a solution for these functional problems. Demonstration of performance under simulated flight condition is necessary to establish confidence in reliability and quality control. A portion of the analytic studies in later phases of this study will be directed at evaluation of system noise generation and transient stress on solid state switchgear. Additional discussion of state-of-art configuration and performance of solid state switchgear may be found in Section 3.2.3.4 of the Phase 1 report.

3.2.3.2 Pulse Width Modulator

The Pulse Width Modulator (Figure 3.2.3.2-1) is designed to simulate a solid state regulator or converter. The major elements of this component are the input filter, semiconductor switch and the drive electronics. Filter designs are obtained from a computer program developed in Phase 1. A range of filter designs which include physical and electrical parameters are provided in Appendix B; additional designs for any selection of line voltage and power will be provided to MSFC, as required by the test program. Filter designs meet the conducted interference requirements defined in

Section 3.6 of this report. A Solitron SDT 5853 transistor was selected for the solid state switch on the basis of response time, current and voltage capability. The performance of semiconductors in the current and voltage range of interest is poorly documented and the full power capability of the RWM will be defined in laboratory test; the initial design will have a 500 watt capability. It is anticipated that this capability can be increased to a value in excess of 1.5 KW.

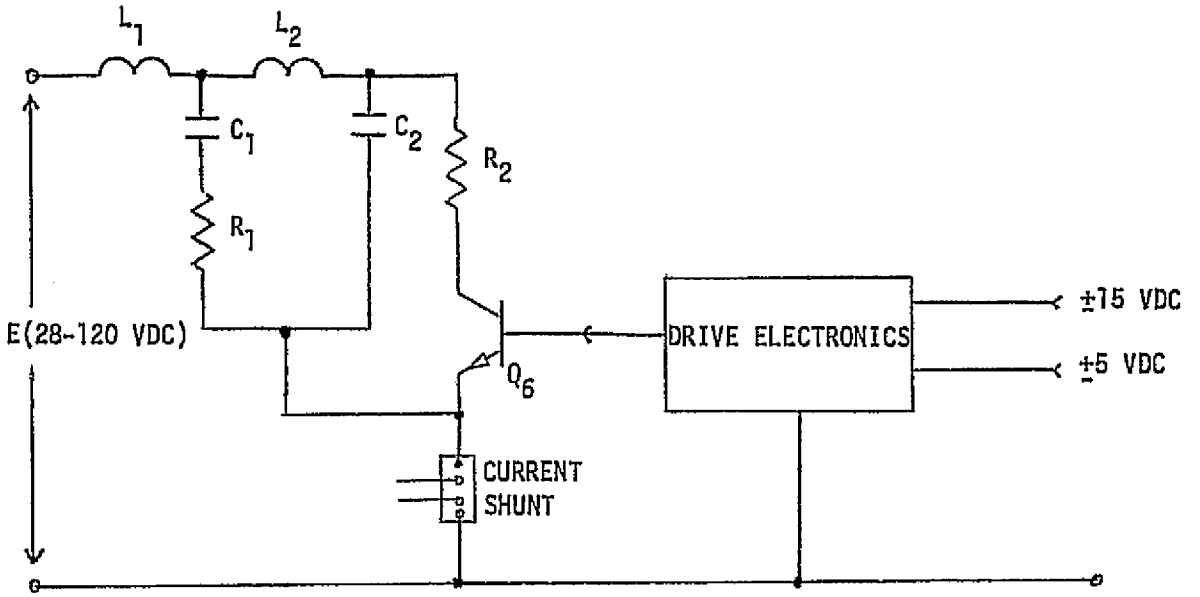



Figure 3.2.3.2-1. PWM Functional Block Diagram

The drive electronics circuitry illustrated in Figure 3.2.3.2-2 is designed to provide manual frequency control from 5.0 KHz to 15.0 KHz and 5% to 95% duty cycle. A sawtooth waveform is developed by IC-1 and IC-2 to provide pulse width control. Adjustment to R8 changes the trigger level for IC-3 which functions as a threshold detector to develop the variable duty cycle waveform. Diode network CR-5 through CR-8 maintain fixed signal amplitude limits on the input to the following stage. Transistors Q1 through Q5 constitute a feedback amplifier to drive switch Q6. This amplifier is designed to provide a fast initial transient with overshoot as shown in Figure 3.2.3.2-3. Subsequent to the initial transient, the drive on Q6 is maintained at a level selected to minimize storage delay

| SCHEMATIC |
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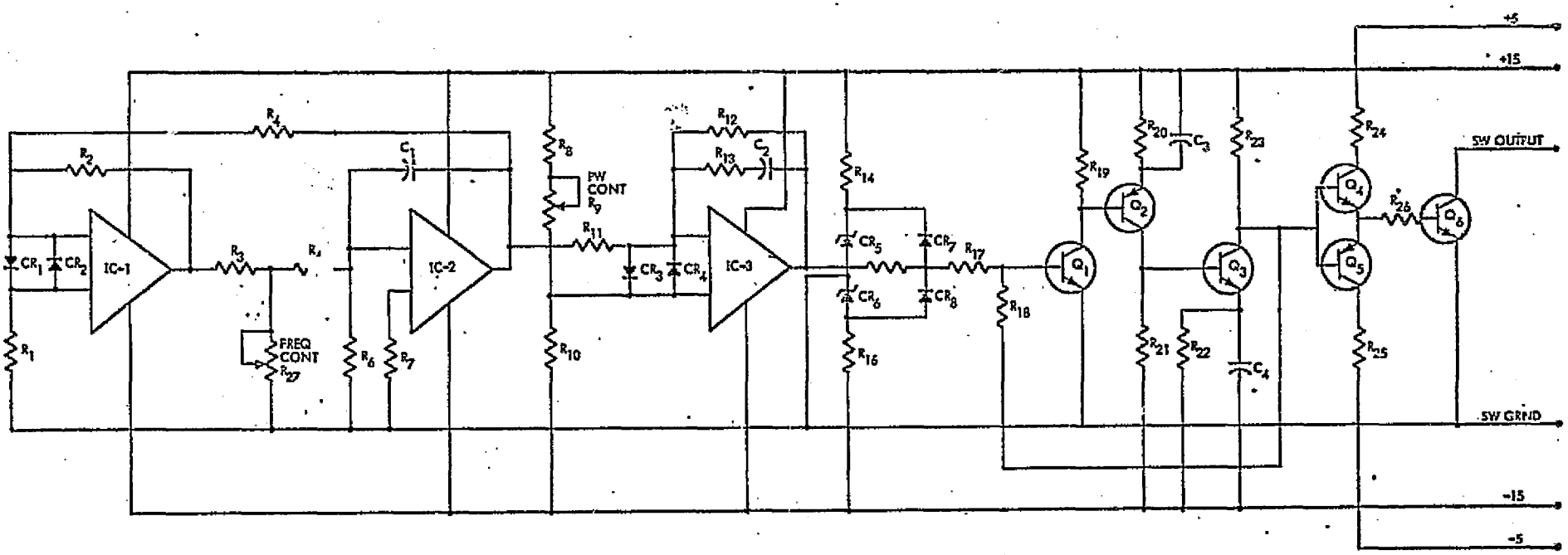


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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| $R_1$ | 100K | $R_8$ | 3.3K | $R_{15}$ | 3K | $R_{22}$ | 120Ω 5W | CR1-4 1N3613 | $Q_1$ 2N2222 |
| $R_2$ | 300K | $R_9$ | 100K (WIREWOUND POT) | $R_{16}$ | 5.1K | $R_{23}$ | 120Ω 5W | CR5-6 CR7-8 1N3613 | $Q_2$ 2N2907A |
| $R_3$ | 3K | $R_{10}$ | 20K | $R_{17}$ | 60K | $R_{24}$ | 4Ω10W | $C_1$ 500 pf | $Q_3$ 2N5154 |
| $R_4$ | 200K | $R_{11}$ | 5.1K | $R_{18}$ | 40K | $R_{25}$ | 4Ω10W | $C_2$ 300 pf | $Q_4$ 2N5154 |
| $R_5$ | 20K | $R_{12}$ | 300K | $R_{19}$ | 6K ¼W | $R_{26}$ | 6Ω5W | $C_3$ 0.1 µf | $Q_5$ 2N5005 |
| $R_6$ | 100K | $R_{13}$ | 15K | $R_{20}$ | 4K ¼W | $R_{27}$ | 30K (WIREWOUND POT) | $C_4$ 3 µf | $Q_6$ SDT 5853 |
| $R_7$ | 20K | $R_{14}$ | 5.1K | $R_{21}$ | 4K ¼W | | | | |

| | |
| --- | --- |
| $IC_1$ | LM101 |
| $IC_2$ | LM101 |
| $IC_3$ | LM106 |

NOTE: ALL RESISTORS 1/8 WATT, CARBON COMPOSITION UNLESS OTHERWISE NOTED.

Figure 3.2.3.2-2. PWM Drive Electronics Schematic

and second breakdown. Phase/gain characteristics are illustrated in Figure 3.2.3.2-4. Although this circuit has been simulated with ICAP, nonlinear characteristics and complex response to high electrical stress evidenced by real devices leaves areas of design to be resolved in breadboard test. It is expected that this configuration will perform satisfactorily with a 500 watt load and 120VDC line, but further development coordinated with breadboard tests will be required for increased load power.

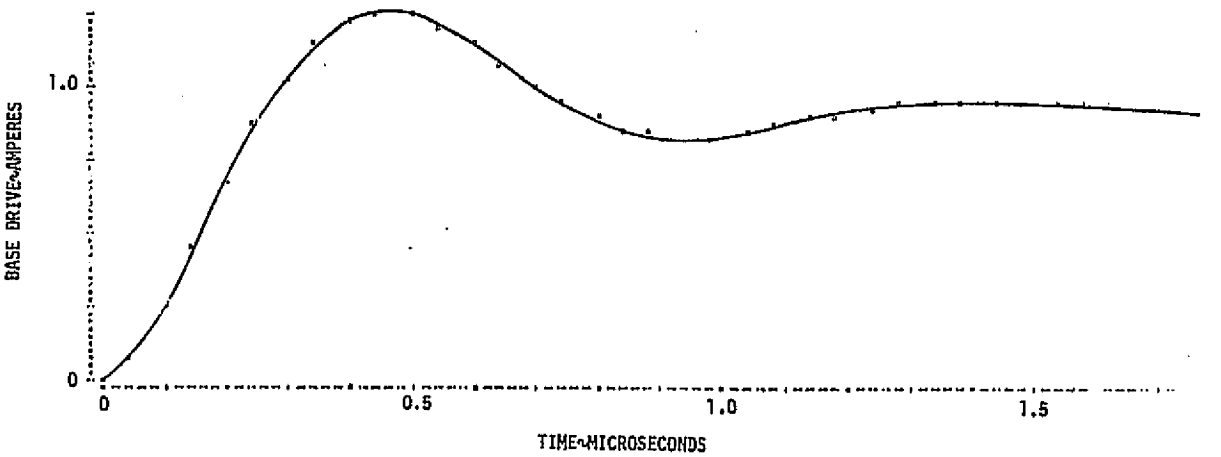



Figure 3.2.3.2-3. Drive Amplifier Transient Response

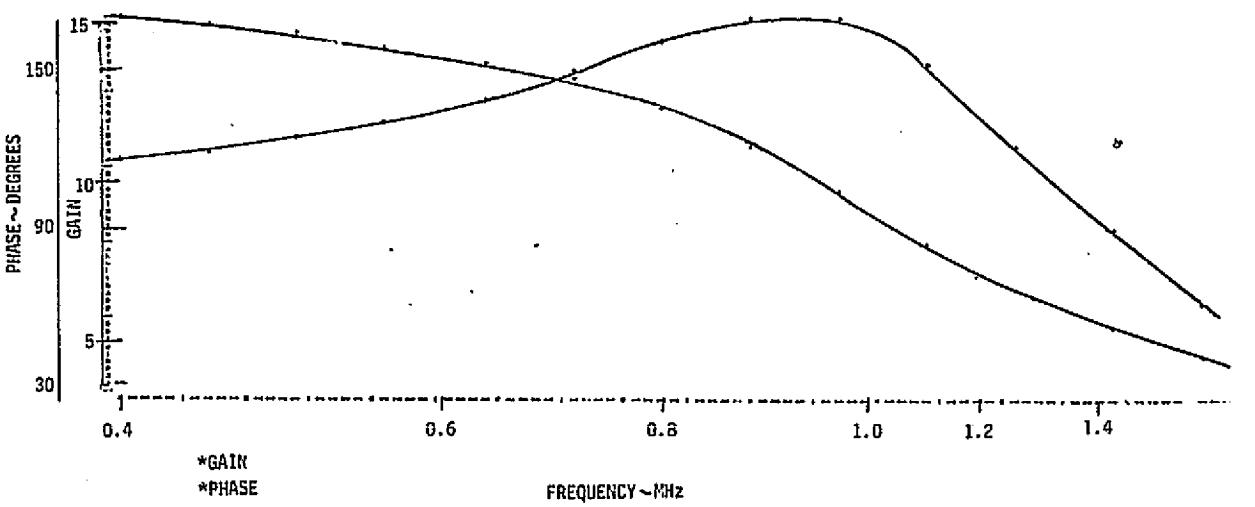



Figure 3.2.3.2-4. Drive Amplifier Frequency Response

### 3.2.4 Signal Conditioning and Control Electronics

The signal conditioning and control electronics Figure 3.2.4-1 consist of circuits designed to drive relays and display indicators and condition current shunt signals for meter displays. These circuits were designed to operate with both local (Load Bank) and remote (SMU, ACES) control and display panels without interface circuit modifications.

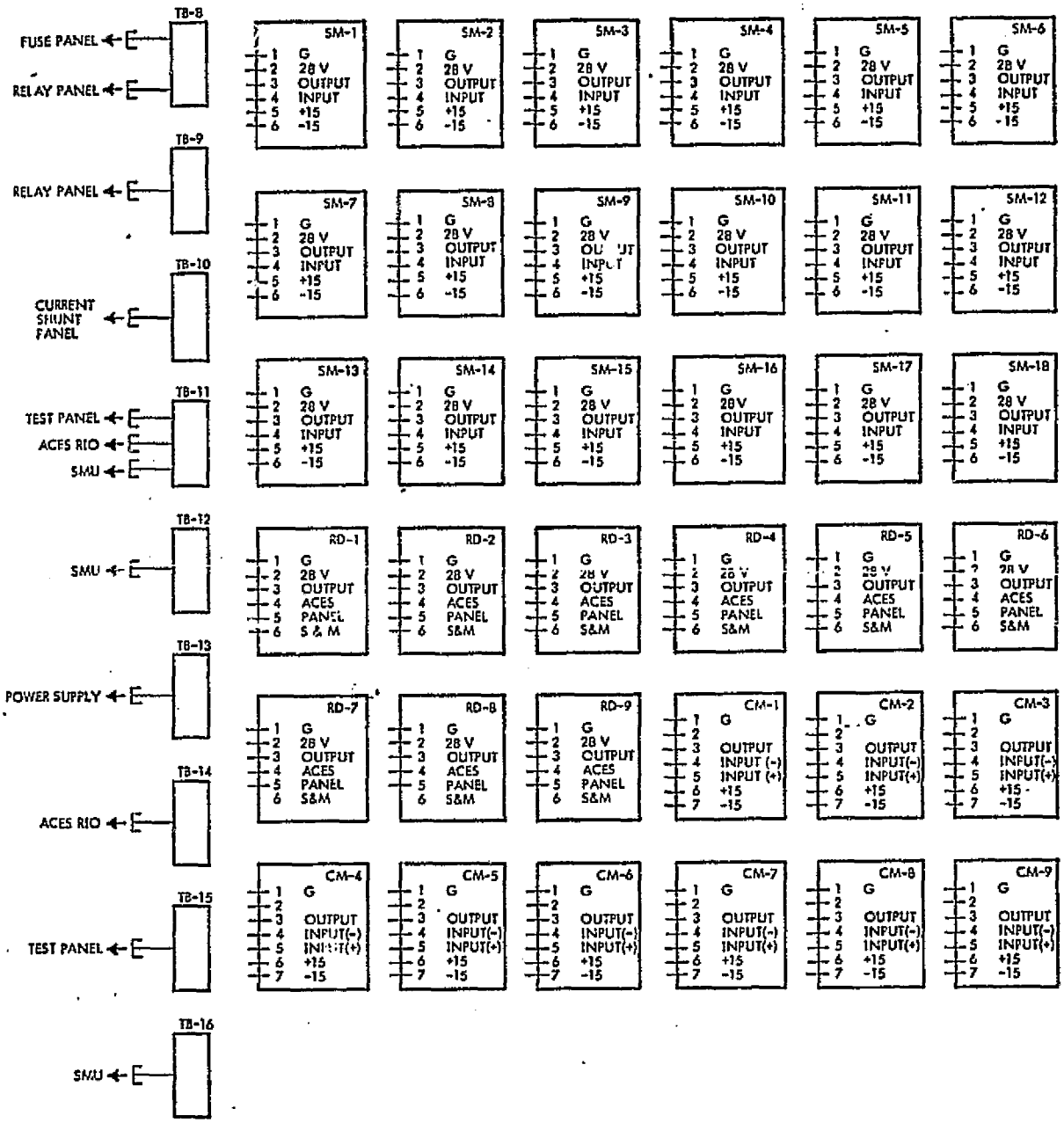
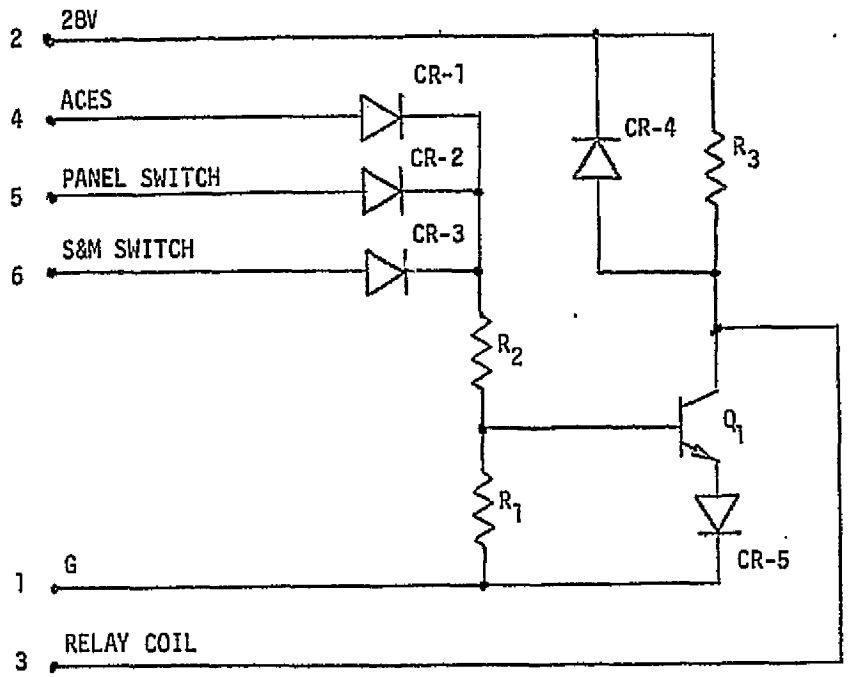



Figure 3.2.4-1. Load Bank Electronics

### 3.2.4.1 Relay Driver

The relay drivers (RD- on Figure 3.2.4-1) consist of a straightforward semiconductor switch as illustrated in Figure 3.2.4-2. Bi-level control signals are input at terminals 4, 5 and 6. The relay coils are connected between the 28V bus and the switch Q5. The ACES control system provide 28VDC in the "ON" condition and essentially zero in the off condition. ACES characteristics are given in Table 3.2.4-1.




| | |
|---|---|
| $R_1$ | 3K 1/8 Watt |
| $R_2$ | 5.1K 1/2 Watt |
| $R_3$ | 10K 1/4 Watt |
| $Q_1$ | 2N2222 |
| CR1-CR5 | 1N3613 |

Figure 3.2.4-2. Relay Drive Circuit

Table 3.2.4-1. ACES Control Interface

| CONDITION | |
|---|---|
| "ON" | Source Voltage 28VDC ± 10%<br>Source Impedance 100Ω<br>Maximum Current <0.04 Amperes |
| "OFF" | Maximum Current <40 Microamperes |

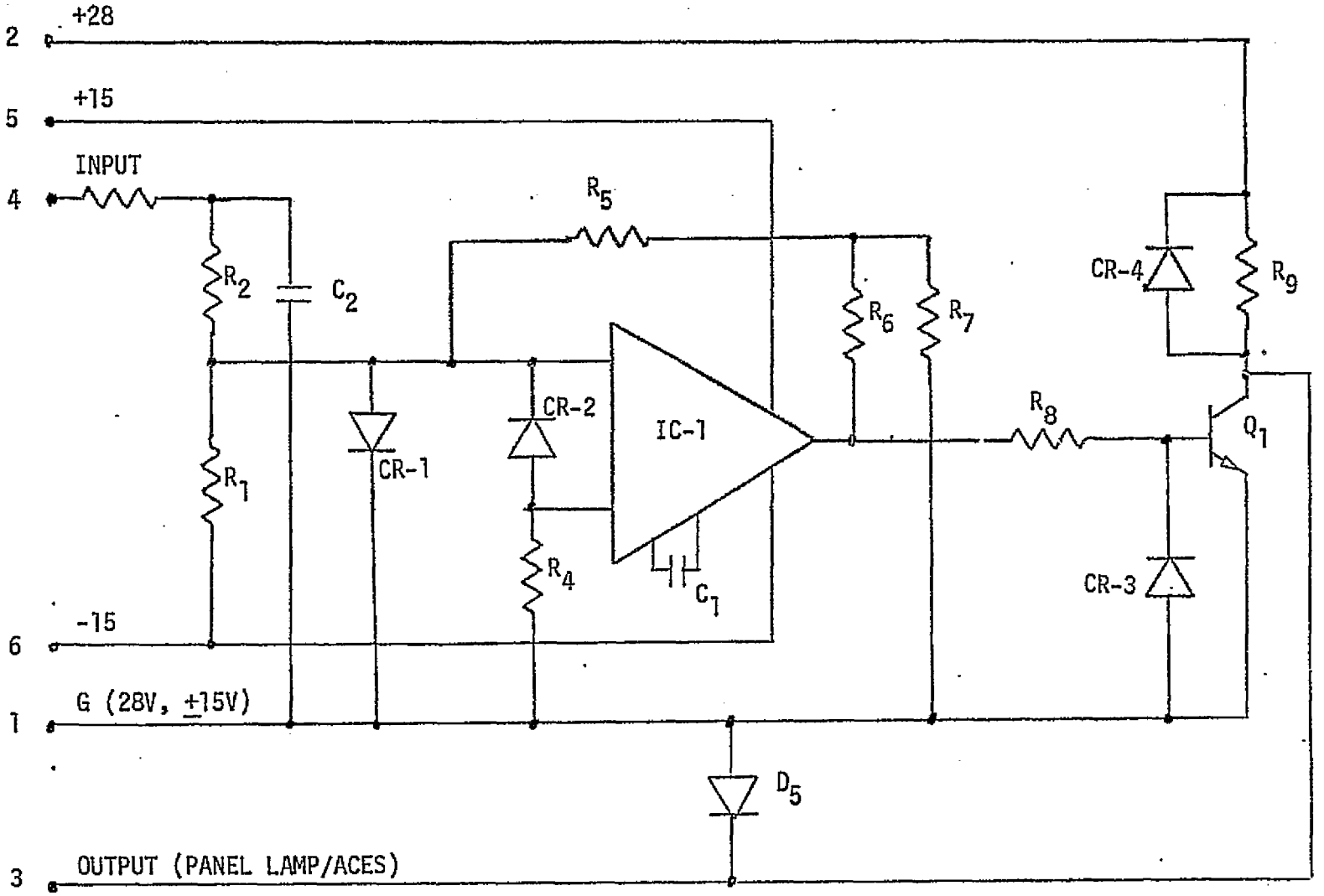
The panel switches on the Load Bank and SMU panel provide 28VDC from secondary power bus in the "ON" condition and open circuit in the "OFF" condition. With these input conditions it appears unnecessary to define more elaborate circuitry for this function. Specific information on the current required for relay drive was not available, however, the limited data that could be obtained indicate that the requirement is less than 100 ma. The use of the 2N2222 allows sufficient margin for later requirement variations. Diode CR1 through CR3 provide isolation between inputs. The relay driver responds to any of the three inputs on a logical "OR" basis for the "ON" condition and a logical "AND" basis for the "OFF" condition. Consequently, supervision panels which are not functioning should have all control switches in the "OFF" position. The design assumes a worst case Beta of 30 for the 2N2222 which is adequate for laboratory operation.

3.2.4.2 Status Monitors

The status monitors (indicated by SM- on Figure 3.2.4-1) are designed to indicate presence or absence of voltage and provide drive for two panel lamps. The circuit design for this function is shown in Figure 3.2.4-3. The maximum current through the 2N2222 for two panel lamps (40 ma per lamp) and the ACES logic input (2.7 ma ± 20%) is 83.2 ma. The integrated circuit IC-1 supplies 2.8 ma minimum base drive to Q1 to supply this load. IC-1 is a biased bi-stable circuit designed to operate "ON" with +20 volts at the input (terminal 4) and "OFF" with 14 volts at that terminal. This circuit was evaluated for worst case response with the ICAP program; parameters used in this analysis are given below.

Table 3.2.4-2. Worst Case Parameters

| | |
|---|---|
| LM101 | |
| Input Offset Voltage | ±5 mv |
| Input Offset Current | 200 ± 10% nA |
| Input Bias Current | 400 ± 10% nA |
| Input Resistance | 300, 800 K ohms |
| Voltage Gain | 25, 160 V/mV |
| All Resistors | ± 1% |
| All Voltages | ± 5% |




| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $R_1$ | 1.0M | $R_5$ | 0.412M | $R_9$ | 20K | $C_1$ | 30pf | Note: Resistors 1/8W unless otherwise noted. |
| $R_2$ | 0.562M | $R_6$ | 1.0M | CR1-5 | 1N3613 | $C_2$ | 0.01μf | |
| $R_3$ | 0.25M | $R_7$ | 100K | $Q_1$ | 2N2222 | | | |
| $R_4$ | 0.511M | $R_8$ | 4.7K | IC-1 | LM101 | | | |

Figure 3.2.4-3. Status Sense Circuit

The sensitivity of the input trigger levels was determined by adding a dummy high gain negative feedback loop between the output of IC-1 and terminal 4 of the input. Resistor R4 was lifted from the output of IC-1 and connected to ±15 volts to simulate the two stable states of the circuit. The input is then driven to the voltage which results in the transition state (zero volts) at the output of IC-1. This evaluation resulted in the following data.

Table 3.2.4-3. Status Monitor Worst Case

| Condition | Required Input Voltage |
|---|---|
| ON | 17.69 < E < 21.06 VDC |
| OFF | 14.89 > E > 11.65 |

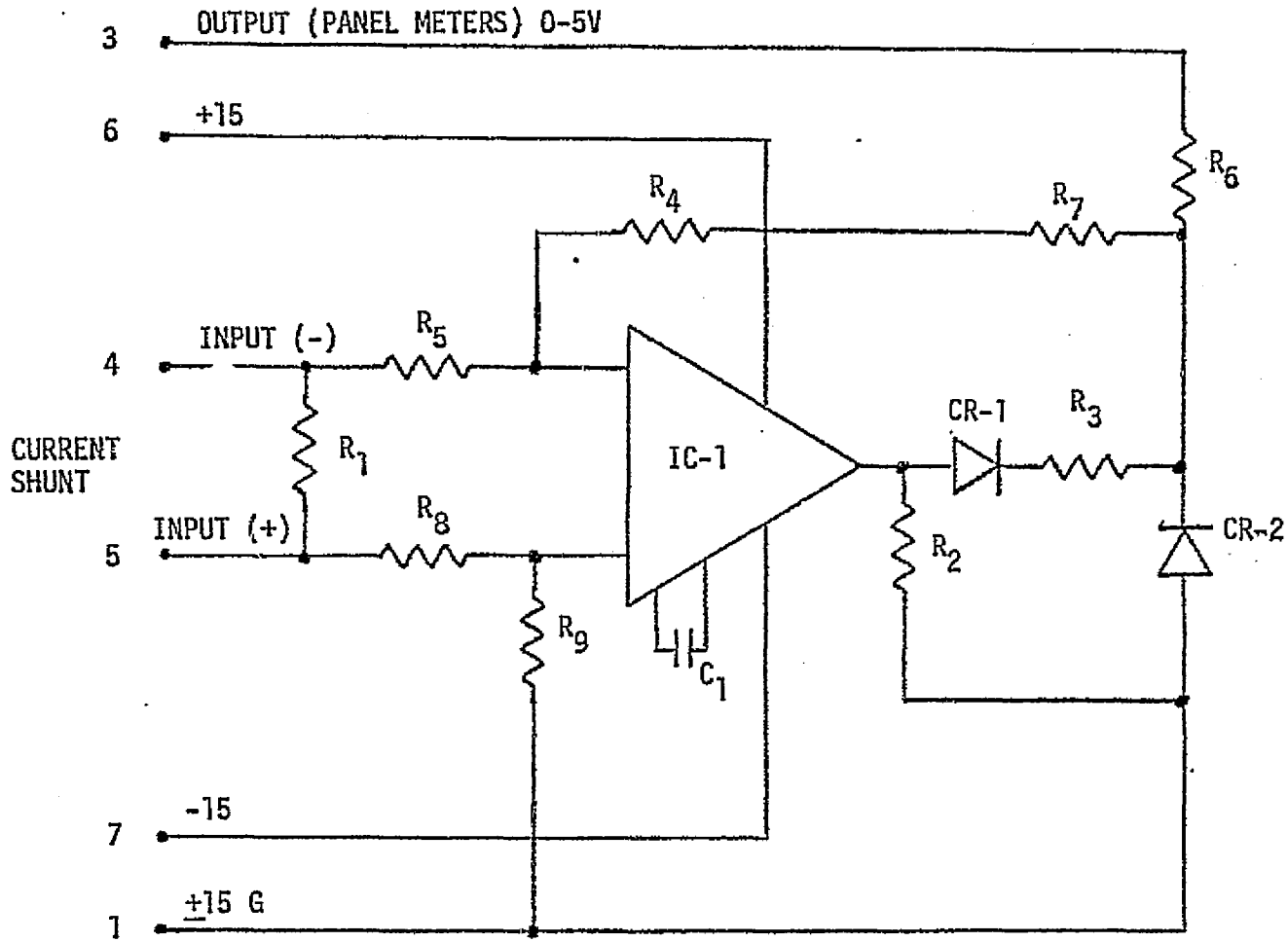
The significant values, minimum "ON" voltage and maximum "OFF" voltage indicate range of operation under worst case conditions. In an actual design the two trigger levels would tend to track and margins between levels will be approximately 6 volts.

### 3.2.4.3 Current Monitor

The current monitor designs (indicated by CM- in Figure 3.2.4-1) are illustrated in Figure 3.2.4-4. This amplifier conditions the voltage developed across the load channels and load bank current shunt (0- 0.2VDC) to standard meter display drive voltage (0- 5.0VDC). Although the meters have not been selected for this program and will probably be obtained from MSFC storage, the current design may be easily modified to any standard meter characteristic. Worst case operation of this amplifier was evaluated with parameter variation similar to those for the status monitor. Output voltage stability was evaluated for minimum and maximum input conditions and yielded the results below.

Table 3.2.4-3. Current Monitor - Worst Case

| Input Voltage | Output Voltage | | |
|---|---|---|---|
| | MIN. | NOMINAL | MAX. |
| 0 | -0.149 | -0.001 | +0.143 |
| 0.2 | 4.829 | 5.072 | 5.323 |




| | |
|---|---|
| $R_1$ | 1.0K |
| $R_2$ | 100K |
| $R_3$ | 24.3K |
| $R_4$ | 24.3K |
| $R_5$ | 1.0K ± 1% |
| $R_6$ | 1.0K |
| $R_7$ | 1.0K ± 1% |
| $R_8$ | 1.0K ± 1% |
| $R_9$ | 24.3K ± 1% |
| $C_1$ | 30pf |
| CR1-2 | 1N3613 |
| IC-1 | LM101 |

NOTE: All resistors 1/8 watt unless otherwise noted.

Figure 3.2.4-4. Load Current Monitor

These values indicate ±2.5% and ±5% (of full scale) possible error at the remote meter display without part selection. This is considered adequate for this design since the remote display is used for information only. Accurate measurements will always be performed with local instruments at the load bank test panel.

These signal conditioners require balanced inputs since the current shunt terminals will be at a small but significant voltage off ground. The ±15 volt secondary converter and signal ground for the current monitor are connected to main bus ground. This configuration eliminates excessive electrical stress across the semiconductors during severe main bus transients such as major fault simulation. The signal conditioner is also protected from transients coupled through the leads between the load bank and the SMU by diodes CR1 and CR2. The stability of the feedback amplifier was evaluated on ICAP with a simulated 50 meter signal lead attached to the output. Gain and phase margin are approximately 12db and 50° under these conditions. While it is preferred that these margins be larger for a signal conditioner, simple compensation techniques and uncertainties in the frequency characteristics of the actual harness make further design study undesirable prior to breadboard tests.

### 3.2.5 Load Bank Interface Wiring

The signal conditioning and control electronics interface with all load bank components, load bank test panel (Figure 3.2.5-1) and the SMU panel switches, panel light and meter displays. The interconnections between these circuits are defined in Table 3.2.5-1. Secondary power converter and R10 connections are shown in Figure 3.2.5-2. A summary of load bank harness runs is illustrated in Figure 3.2.5-3.

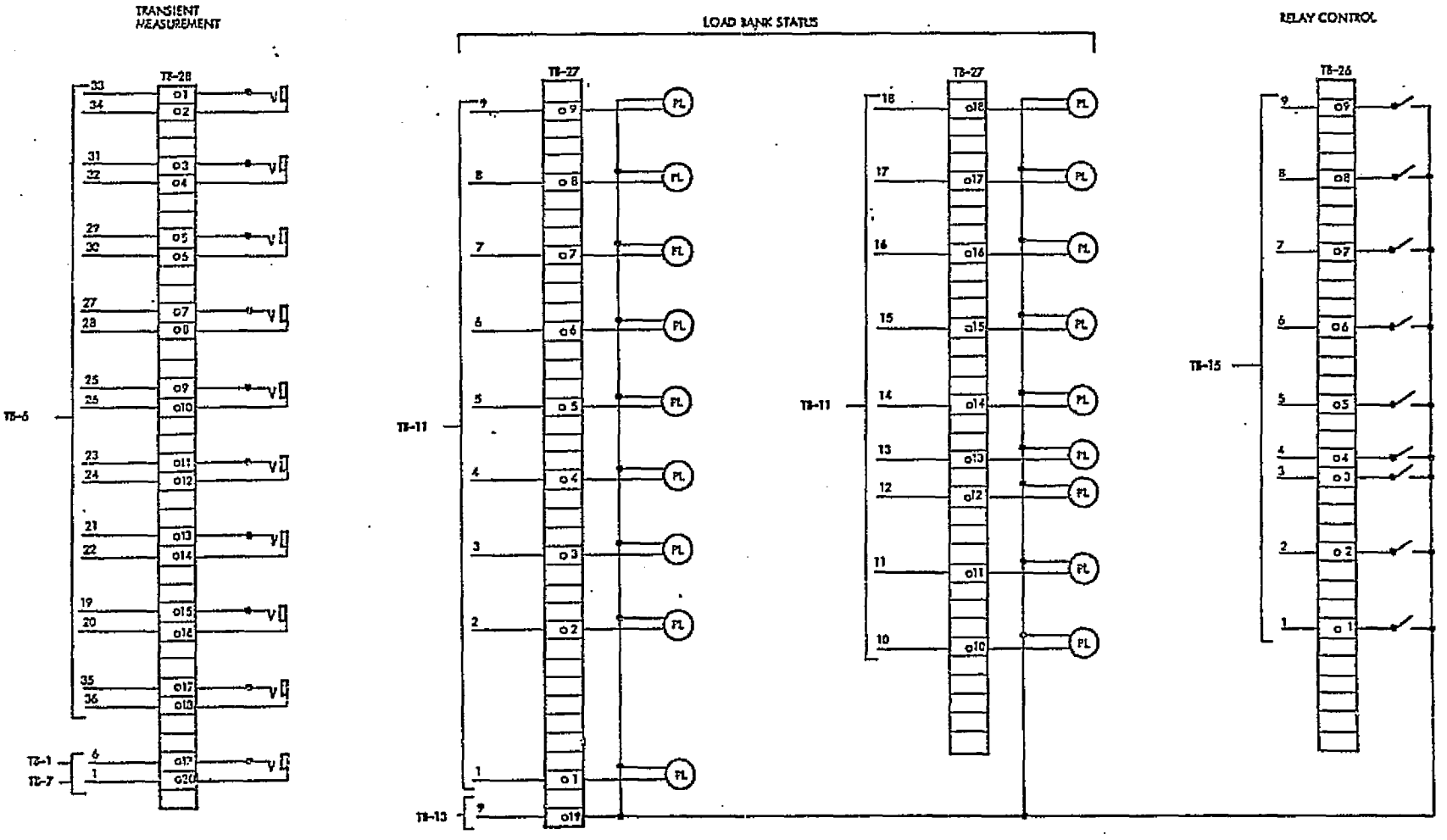



Figure 3.2.5-1. Load Bank Test Panel

Table 3.2.5-1. Load Bank Signal Conditioning Electronics Interface

| | INTERFACE | | ELECTRONICS | | |
|---|---|---|---|---|---|
| SIGNAL | TERMINAL BOARD | TERMINAL | TERMINAL BOARD | TERMINAL | ELECTRONICS TERMINAL |
| F1 Status in | 3 | 1 | 8 | 1 | SM-1-4 |
| F2 Status in | 3 | 2 | 8 | 2 | SM-2-4 |
| F3 Status in | 3 | 3 | 8 | 3 | SM-3-4 |
| F4 Status in | 3 | 4 | 8 | 4 | SM-4-4 |
| F5 Status in | 3 | 5 | 8 | 5 | SM-5-4 |
| F6 Status in | 3 | 6 | 8 | 6 | SM-6-4 |
| F7 Status in | 3 | 7 | 8 | 7 | SM-7-6 |
| F8 Status in | 3 | 8 | 8 | 8 | SM-8-6 |
| F9 Status in | 3 | 9 | 8 | 9 | SM-9-6 |
| K1 Status in | 4 | 11 | 8 | 10 | SM-10-4 |
| K2 Status in | 4 | 12 | 8 | 11 | SM-11-4 |
| K3 Status in | 4 | 13 | 8 | 12 | SM-12-4 |
| K4 Status in | 4 | 14 | 8 | 13 | SM-13-4 |
| K5 Status in | 4 | 15 | 8 | 14 | SM-14-4 |
| K6 Status in | 4 | 16 | 8 | 15 | SM-15-4 |
| K7 Status in | 4 | 17 | 8 | 16 | SM-16-4 |
| K8 Status in | 4 | 18 | 8 | 17 | SM-17-4 |
| K9 Status in | 4 | 19 | | | |
| K1 Control out | 4 | 1 | 9 | 1 | RD-1-3 |
| K2 Control out | 4 | 2 | 9 | 2 | RD-2-3 |
| K3 Control out | 4 | 3 | 9 | 3 | RD-3-3 |
| K4 Control out | 4 | 4 | 9 | 4 | RD-4-3 |
| K5 Control out | 4 | 5 | 9 | 5 | RD-5-3 |
| K6 Control out | 4 | 6 | 9 | 6 | RD-6-3 |
| K7 Control out | 4 | 7 | 9 | 7 | RD-7-3 |
| K8 Control out | 4 | 8 | 9 | 8 | RD-8-3 |
| K9 Control out | 4 | 9 | 9 | 9 | RD-9-3 |
| I Meas #1 (+) in | 6 | 1 | 10 | 1 | CM-1-5 |
| I Meas #1 (-) in | 6 | 2 | 10 | 2 | CM-1-4 |
| I Meas #2 (+) in | 6 | 3 | 10 | 3 | CM-2-5 |
| I Meas #2 (-) in | 6 | 4 | 10 | 4 | CM-2-4 |
| I Meas #3 (+) in | 6 | 5 | 10 | 5 | CM-3-5 |
| I Meas #3 (-) in | 6 | 6 | 10 | 6 | CM-3-4 |
| I Meas #4 (+) in | 6 | 7 | 10 | 7 | CM-4-5 |
| I Meas #4 (-) in | 6 | 8 | 10 | 8 | CM-4-4 |
| I Meas #5 (+) in | 6 | 9 | 10 | 9 | CM-5-5 |
| I Meas #5 (-) in | 6 | 10 | 10 | 10 | CM-5-4 |
| I Meas #6 (+) in | 6 | 11 | 10 | 11 | CM-6-5 |
| I Meas #6 (-) in | 6 | 12 | 10 | 12 | CM-6-4 |
| I Meas #7 (+) in | 6 | 13 | 10 | 13 | CM-7-5 |
| I Meas #7 (-) in | 6 | 14 | 10 | 14 | CM-7-4 |
| I Meas #8 (+) in | 6 | 15 | 10 | 15 | CM-8-5 |
| I Meas #8 (-) in | 6 | 16 | 10 | 16 | CM-8-4 |
| I Meas #9 (+) in | 6 | 17 | 10 | 17 | CM-9-5 |
| I Meas #9 (-) in | 6 | 18 | 10 | 18 | CM-9-4 |
| K1 Control in | 20 | 1 | 14 | 1 | RD-1-4 |
| K2 Control in | 20 | 2 | 14 | 2 | RD-2-4 |
| K3 Control in | 20 | 3 | 14 | 3 | RD-3-4 |
| K4 Control in | 20 | 4 | 14 | 4 | RD-4-4 |
| K5 Control in | 20 | 5 | 14 | 5 | RD-5-4 |
| K6 Control in | 20 | 6 | 14 | 6 | RD-6-4 |
| K7 Control in | 20 | 7 | 14 | 7 | RD-7-4 |
| K8 Control in | 20 | 8 | 14 | 8 | RD-8-4 |
| K9 Control in | 20 | 9 | 14 | 9 | RD-9-4 |
| K1 Control in | 24 | 1 | 16 | 1 | RD-1-6 |
| K2 Control in | 24 | 2 | 16 | 2 | RD-2-6 |
| K3 Control in | 24 | 3 | 16 | 3 | RD-3-6 |
| K4 Control in | 24 | 4 | 16 | 4 | RD-4-6 |
| K5 Control in | 24 | 5 | 16 | 5 | RD-5-6 |
| K6 Control in | 24 | 6 | 16 | 6 | RD-6-6 |
| K7 Control in | 24 | 7 | 16 | 7 | RD-7-6 |
| K8 Control in | 24 | 8 | 16 | 8 | RD-8-6 |
| K9 Control in | 24 | 9 | 16 | 9 | RD-9-6 |

Table 3.2.5-1. Load Bank Signal Conditioning Electronics Interface (Continued)

| | INTERFACE | | ELECTRONICS | | |
|---|---|---|---|---|---|
| SIGNAL | TERMINAL BOARD | TERMINAL | TERMINAL BOARD | TERMINAL | ELECTRONICS TERMINAL |
| K1 Control in | 26 | 1 | 15 | 1 | RD-1-5 |
| K2 Control in | 26 | 2 | 15 | 2 | RD-2-5 |
| K3 Control in | 26 | 3 | 15 | 3 | RD-3-5 |
| K4 Control in | 26 | 4 | 15 | 4 | RD-4-5 |
| K5 Control in | 26 | 5 | 15 | 5 | RD-5-5 |
| K6 Control in | 26 | 6 | 15 | 6 | RD-6-5 |
| K7 Control in | 26 | 7 | 15 | 7 | RD-7-6 |
| K8 Control in | 26 | 8 | 15 | 8 | RD-8-6 |
| K9 Control in | 26 | 9 | 15 | 9 | RD-9-6 |
| F1 Status out | 19,23,27 | 1 | 11 | 1 | SM-1-3 |
| F2 Status out | | 2 | | 2 | SM-2-3 |
| F3 Status out | | 3 | | 3 | SM-3-3 |
| F4 Status out | | 4 | | 4 | SM-4-3 |
| F5 Status out | | 5 | | 5 | SM-5-3 |
| F6 Status out | | 6 | | 6 | SM-6-3 |
| F7 Status out | | 7 | | 7 | SM-7-3 |
| F8 Status out | | 8 | | 8 | SM-8-3 |
| F9 Status out | | 9 | | 9 | SM-9-3 |
| K1 Status out | | 10 | | 10 | SM-10-3 |
| K2 Status out | | 11 | | 11 | SM-11-3 |
| K3 Status out | | 12 | | 12 | SM-12-3 |
| K4 Status out | | 13 | | 13 | SM-13-3 |
| K5 Status out | | 14 | | 14 | SM-14-3 |
| K6 Status out | | 15 | | 15 | SM-15-3 |
| K7 Status out | | 16 | | 16 | SM-16-3 |
| K8 Status out | | 17 | | 17 | SM-17-3 |
| K9 Status out | 19,23,27 | 18 | 11 | 18 | SM-18-3 |
| Signal Ground | 24 | 1 | 12 | 1 | TB-13-10 |
| I Meas #1 out | | 2 | | 2 | CM-1-3 |
| I Meas #2 out | | 3 | | 3 | CM-2-3 |
| I Meas #3 out | | 4 | | 4 | CM-3-3 |
| I Meas #4 out | | 5 | | 5 | CM-4-3 |
| I Meas #5 out | | 6 | | 6 | CM-5-3 |
| I Meas #6 out | | 7 | | 7 | CM-6-3 |
| I Meas #7 out | | 8 | | 8 | CM-7-3 |
| I Meas #8 out | | 9 | | 9 | CM-8-3 |
| I Meas #9 out | 24 | 10 | 12 | 10 | CM-9-3 |
| +15 volts | 22 | 1 | 13 | 1 | 6,CM-1 through CM-9 |
| -15 volts | | 2 | | 2 | 7,CM-1 through CM-9 |
| Gnd | | 3 | | 3 | 1,CM-1 through CM-9; TB-13-10 |
| +15 | | 7 | | 4 | 5,SM-1 through SM-18 |
| -15 | | 8 | | 5 | 6,SM-1 through SM-18 |
| Gnd | 22 | 9 | | 6 | 1,RD-1 through RD-9; 1,SM-1 through SM-18; TB-13-6 |
| +28 | 18 | 7 | | 7 | 2,RD-1 through RD-9; 2,SM-1 through SM-18; TB-13-9 |
| 28V G | 18 | 15 | | 8 | TB-13-6 |
| 28V | 27 | 19 | | 9 | TB-13-7 |
| 120V G | 2 | 2 | 13 | 10 | TB-13-3; TB-12-1 |

F Fuse
K Relay
I Meas. - Load bank bus or load channel current measurement

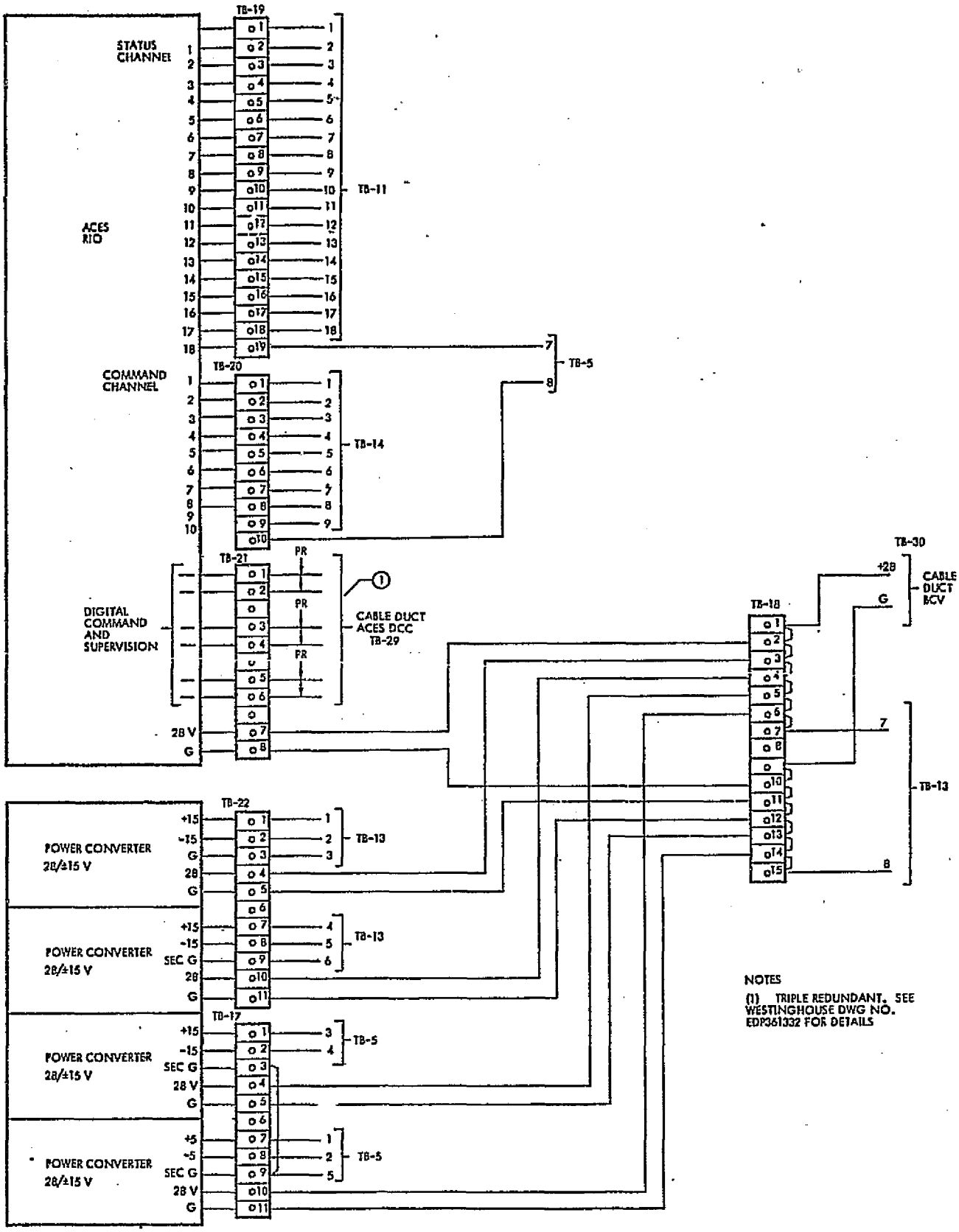
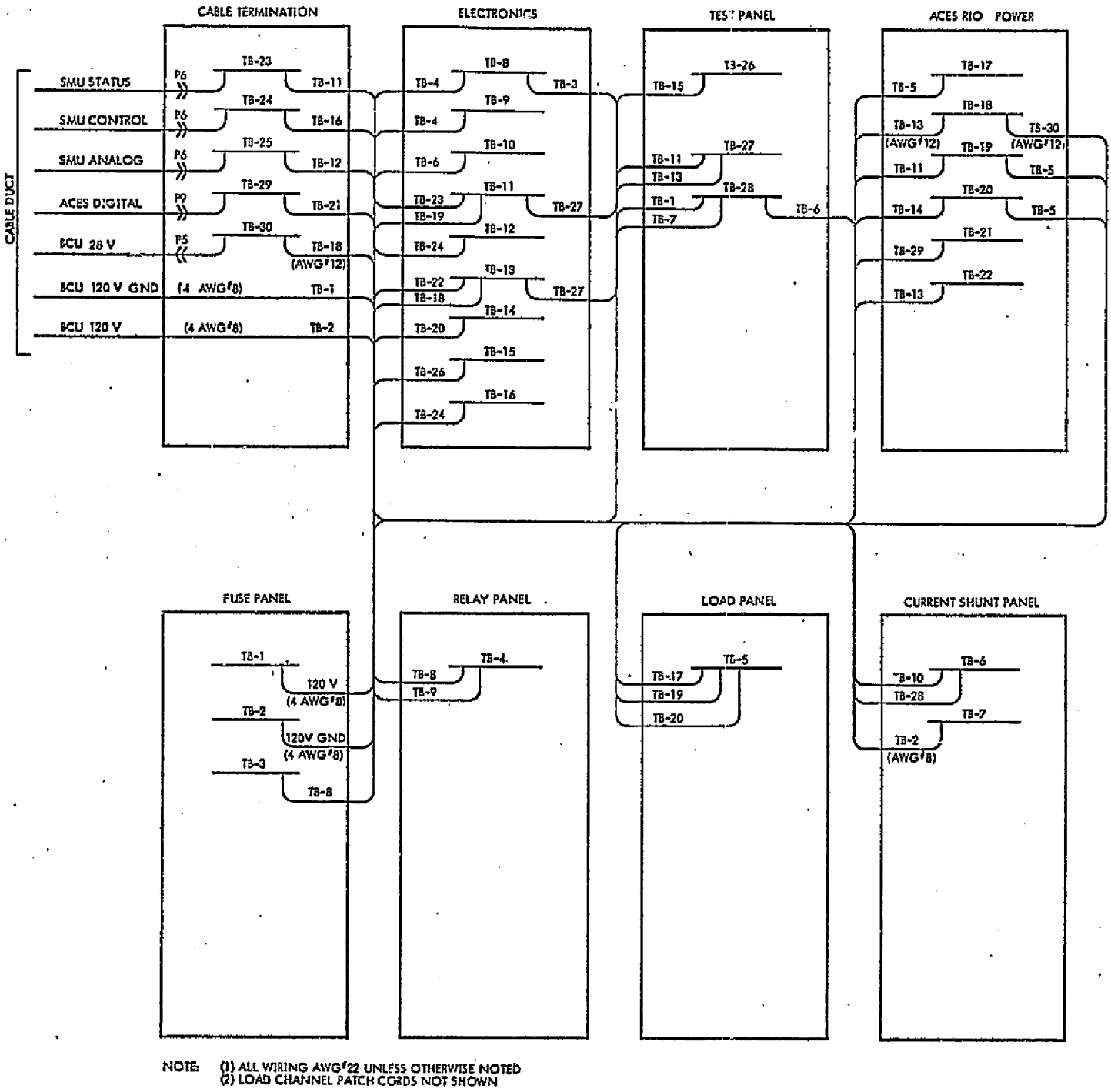



Figure 3.2.5-2. Panel-ACES RIO and Power Converters




NOTE: (1) ALL WIRING AWG#22 UNLESS OTHERWISE NOTED
(2) LOAD CHANNEL PATCH CORDS NOT SHOWN

Figure 3.2.5-3. Load Bank Interconnection

## 3.3 Cable Mockup Design and Test

The distribution harness is a major study element in this program. It is usually adequate to treat the electrical interconnections between subsystems as lumped R, L and C circuits for small spacecraft where harness runs are less than five (5) meters. However, transmission parameters are required to establish a valid analytical model for high frequencies or large spacecraft. Some limited investigative studies have been made on aircraft harnesses although there has been no significant characterization of large spacecraft distribution system parameters. Furthermore, the environment of space vehicle development and production normally precludes tests or use of instrumentation not directly related to the mission plan. The High Voltage Test Facility is designed to electrically simulate an aerospace vehicle electrical distribution system. Tests will be performed under steady-state and transient conditions to fully characterize the electrical performance of the harness and to establish a data base for analysis of power and signal transmission parameters.

The harness runs between Test Facility elements are illustrated in Figure 3.3-1. A cable duct will support the cable, simulate vehicle structure and provide personnel safety. Electrical bonding will be maintained between the cable duct and the BCU, SMU and the load banks. Frame ground connections will also be provided between the power source components and the BCU. The electrical system design is consistent with single point ground philosophy. The design approach is illustrated in Figure 3.3-2.

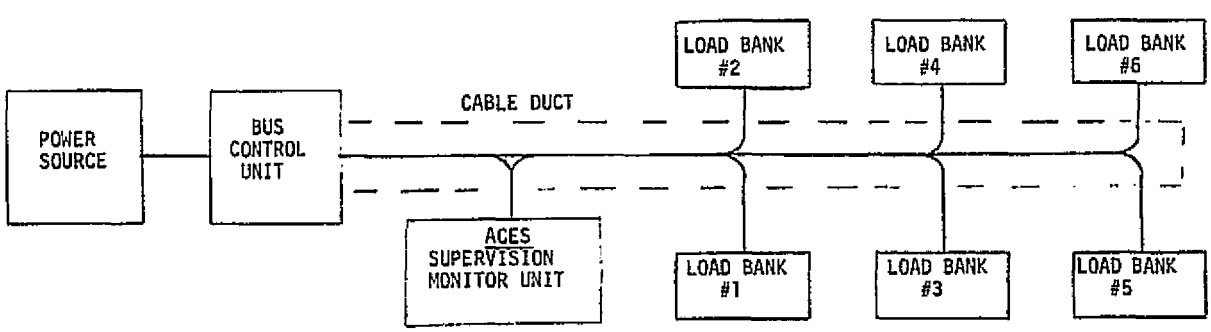



Figure 3.3-1. Test Facility Cable Runs

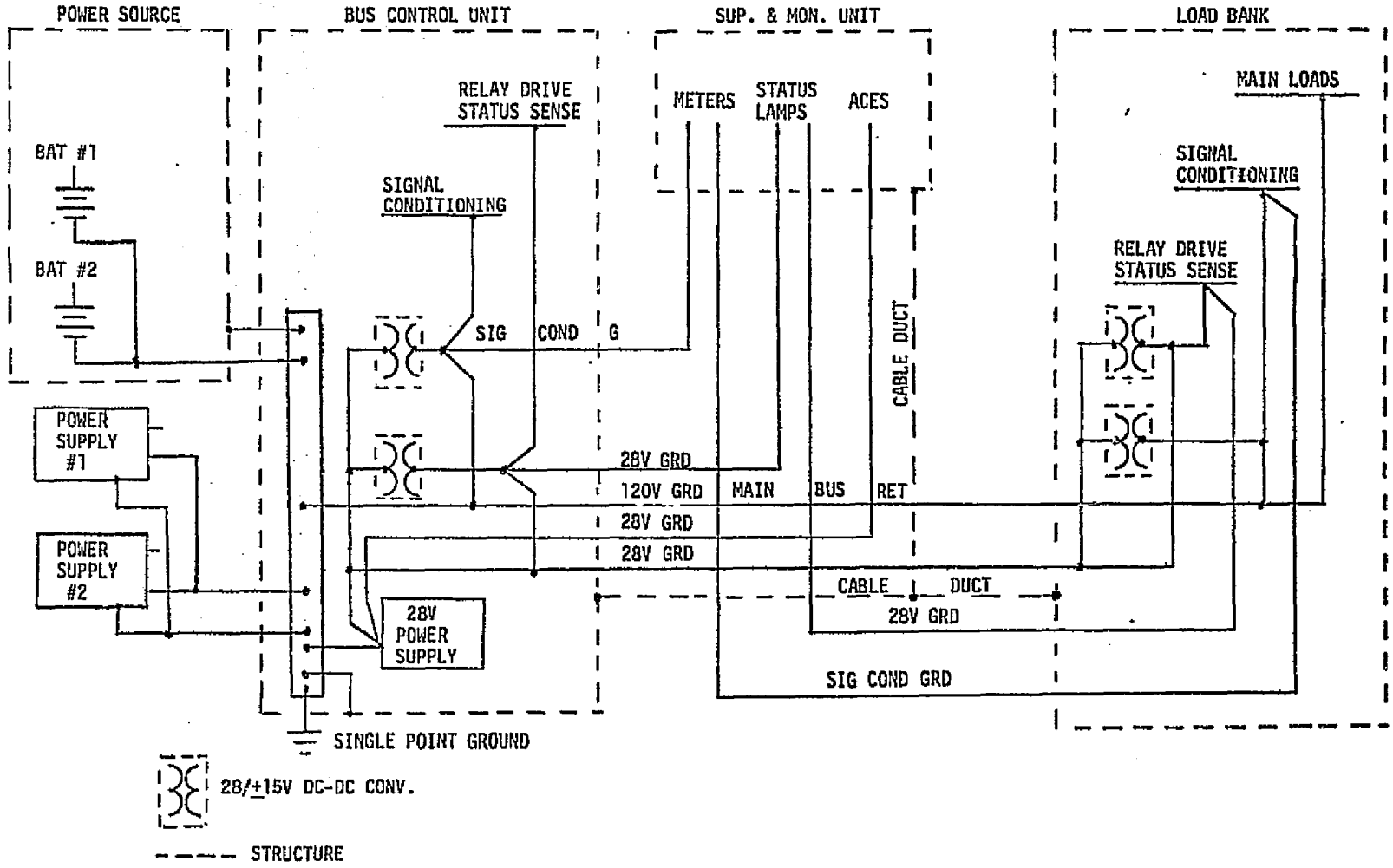



Figure 3.3-2. HVDC Test Facility - Grounding Configuration

### 3.3.1 Harness Design

The Test Facility cables will be routed between the BCU, Load Banks and SMU via metal trays suspended from the laboratory ceiling. The harness will consist of the main power bus, secondary power bus, signal and control cables. Initially these will be separate but physically adjoining harnesses. During later tests, all wiring will be laced together to obtain data on coupled EMI.

System cables and connectors are identified in Figure 3.3-3. It should be noted that ACES cable runs are shown for illustration only. The data bus consists of nine (9) twisted shielded pairs forming a triple redundant system. Details on cables, connectors and wiring are provided in the Westinghouse ACES manual Dwg. No. 361332. The SMU cables are 50 AWG #22 conductors which provide approximately ten spare conductors. Cable WP1-( ) is the main power bus which will carry a maximum of 300A in steady-state to the designated ( ) load bank. This cable is of major interest in this study and the design requirements are given below.

Classification - Type IV - Open Bundle

(a) This classification is for the general use outside the crew compartment area. The electrical characteristics of this cable will be similar to those of a crew compartment area cable and the economical open construction provides better access for test and the inspection than the enclosed designs.

(b) Style - Style B
Spot ties were selected for reasons of economy and ease of fabrication.

(c) Lay of Wire - Configuration T - Twisted.
This is a preferred configuration which minimizes radiated and coupled EMI. Random lay would provide better access and ease of fabrication but does not have the desired characteristics for simulation and test of a flight harness.

(d) Wire
The wire shall be standard wire nickel plated copper or copper alloy.

(e) Insulation - TFE or FEP (Teflon)

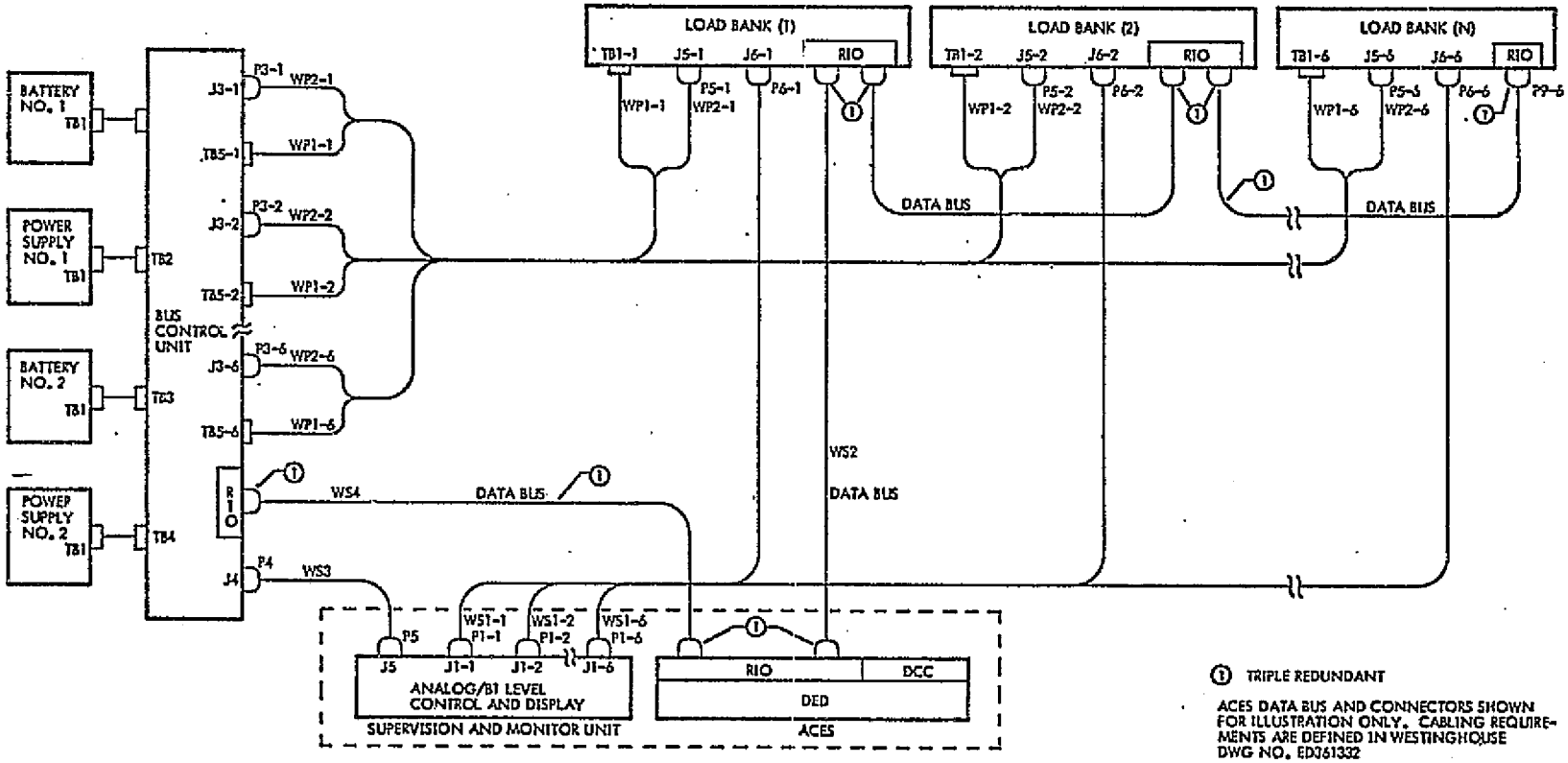



Figure 3.3-3. Test Facility Cabling

Since the cost of design and assembly is based on model shop techniques, it is expected that the harness will be assembled in the test laboratory. It may not be feasible to twist the longest cable (50 meters) to be used in the program in this environment. The standard alternative configuration is random lay. However, it is preferable that the orientation between conductors remain constant throughout the cable due to the requirement to measure transmission parameters. The parameters affected by conductor orientation are distributed capacitance and inductance. Capacitance is influenced primarily by the proximity of the supporting cable trays and would be more equally distributed between conductors with random lay as opposed to the fixed orientation. However, random lay reduces the value of the measurements results due to the lack of design control. Inductance is a function of the spatial distribution and polarity of current flow through the cable cross-section. It is necessary to control the conductor orientation in order to evaluate the effect of current polarity distributions. Informal measurements in multiconductor cable have indicated major shifts in cable inductance for different selections of positive and negative current paths. Consequently, the maintenance of fixed conductor orientation in the main bus distribution cable is necessary to effective performance of the test program.

The conductors in the main bus power cable are #8 (MSFC # similar to AWG) nickel coated stranded wires. The physical characteristics as required by MSFC Specification 40M39513 are summarized below.

| | |
|---|---|
| Conductor size | #8 (MSFC) |
| Nominal Conductor Area | 16,983 circular mils |
| Number of strands | 133 |
| Strand size | #29 (MFSC) |
| Plating | 0.2 mil nickel |
| Resistance | 0.688 ohms/1000 feet |
| Insulation | FEP or TFE |
| Insulation Thickness | 20 mils (minimum) |

It should be noted that MSFC wire size differs slightly (≈3%) from standard AWG cross-sections. Automated analysis and measurements have been performed for this conductor and are discussed in detail in

Appendix A. Both approaches indicate that a single pair of these conductors become quarter wave resonant at about 15 MHz. From this data it is estimated that a 5 pair (#8) 50 meter cable will become resonant at approximately 3 MHz. Resonant conditions are a factor in the generation and coupling of radiated and conducted EMI.

The parameters of other harness cables are not considered critical and may be procured from vendors or from MSFC stock. Identification and wiring lists for all cables are provided in Tables 3.3-1 to 3.3-11.

Table 3.3-1. Cable Identification

Converter Copy

Cable Harness and Wiring

| Cable | Description |
|---|---|
| WP1-( ) | Main bus power distribution, BCU to Load Banks ( ) |
| WP2-( ) | Secondary power (28 VDC) distribution, BCU to Load Banks ( ) |
| WP3 | Source power distribution, Battery I to BCU |
| WP4 | Source power distribution, power supply I to BCU |
| WP5 | Source power distribution, Battery II to BCU |
| WP6 | Source power distribution, power supply II to BCU |
| WS1-( ) | Control and monitor signals, SMU to Load Bank ( ) |
| WS2-( ) | Control and monitor signals, ACES to Load Banks |
| WS3 | Control and monitor signals, SMU to BCU |
| WS4 | Control and monitor signals, ACES to BCU |

Table 3.3-2. Wire List

| BCU | COMPONENT - CABLE # WP1-( ) | | | | | LOAD BANK |
|---|---|---|---|---|---|---|
| Connector Terminal Lugs TB5-( ) Terminal | AWG Guage | Current Amps | Voltage Volts | Signal | Function | Connector Terminal Lugs TB1-( ) Terminal |
| 1 | 8 | 20 | 300 | DC | Main Bus-Power | 1 |
| 2 | | | | | | 2 |
| 3 | | | | | | 3 |
| 4 | | | | | | 4 |
| 5 | | | 300 | | Main Bus-Power | 5 |
| 6 | | | - | | Main Bus-Power | 6 |
| 7 | | | - | | | 7 |
| 8 | | | - | | | 8 |
| 9 | | | - | | | 9 |
| 10 | 8 | 20 | - | DC | Main Bus-Power | 10 |

Table 3.3-3. Wire List

| BCU | COMPONENT - CABLE # WP2-( ) | | | | | LOAD BANK |
|---|---|---|---|---|---|---|
| Connector Terminal Lugs P3-( ) Terminal | AWG Guage | Current Amps | Voltage Volts | Signal | Function | Connector Terminal Lugs P5-( ) Terminal |
| 1 | 12 | 4 | 28 | DC | 28 VDC Power | 1 |
| 2 | 12 | 4 | - | DC | 28 VDC Ret | 2 |
| 3 | 12 | - | - | Spare | - | 3 |
| 4 | 12 | - | - | Spare | - | 4 |

Table 3.3-4. Wire List

| BAT I | COMPONENT CABLE # WP3 | | | | | BCU |
|---|---|---|---|---|---|---|
| Connector Terminal Lugs TB1 Terminal | AWG Guage | Current Amps | Voltage Volts | Signal | Function | Connector Terminal Lugs TB1 Terminal |
| 1 | 00 | 150 | 120 | DC | 120 VDC Power | 1 |
| 2 | 00 | 150 | 120 | DC | 120 VDC Return | 2 |

Table 3.3-5. Wire List

| POWER SUPPLY I | COMPONENT CABLE # WP4 | | | | | BCU |
|---|---|---|---|---|---|---|
| Connector Terminal Lugs TB1 Terminal | AWG Guage | Current Amps | Voltage Volts | Signal | Function | Connector Terminal Lugs TB2 Terminal |
| 1 | 00 | 150 | 120 | DC | 120 VDC Power | 1 |
| 2 | 00 | 150 | 120 | DC | 120 VDC Return | 2 |

Table 3.3-6. Wire List

| BAT II | COMPONENT CABLE # WP5 | | | | | BCU |
|---|---|---|---|---|---|---|
| Connector Terminal Lugs TB1 Terminal | AWG Guage | Current Amps | Voltage Volts | Signal | Function | Connector Terminal Lugs TB3 Terminal |
| 1 | 00 | 150 | 120 | DC | 120 VDC Power | 1 |
| 2 | 00 | 150 | 120 | 1 | 120 VDC Return | 2 |

Table 3.3-7. Wire List

| POWER SUPPLY II | COMPONENT CABLE # WP6 | | | | | BCU |
|---|---|---|---|---|---|---|
| Connector Terminal Lugs TB1 Terminal | AWG Guage | Current Amps | Voltage Volts | Signal | Function | Connector Terminal Lugs TB4 Terminal |
| 1 | 00 | 150 | 120 | DC | 120 VDC Power | 1 |
| 2 | 00 | 150 | 120 | DC | 120 VDC Return | 2 |

Table 3.3-8. Wire List

| SMU | COMPONENT - CABLE # WS1-( ) | | | | | LOAD BANK |
|---|---|---|---|---|---|---|
| Connector P1-( ) Terminal | AWG Gauge | Current Amps | Voltage Volts | Signal | Function | Connector P6-( ) Terminal |
| 1 | 22 | 0.04 | 28 | Bi-level | Fuse #1 Status | 1 |
| 2 | \| | \| | \| | \| | #2 | 2 |
| 3 | \| | \| | \| | \| | #3 | 3 |
| 4 | \| | \| | \| | \| | #4 | 4 |
| 5 | \| | \| | \| | \| | #5 | 5 |
| 6 | \| | \| | \| | \| | #6 | 6 |
| 7 | \| | \| | \| | \| | #7 | 7 |
| 8 | \| | \| | \| | \| | #8 | 8 |
| 9 | \| | \| | \| | \| | Fuse #9 Status | 9 |
| 10 | \| | \| | \| | \| | Relay #1 Status | 10 |
| 11 | \| | \| | \| | \| | #2 | 11 |
| 12 | \| | \| | \| | \| | #3 | 12 |
| 13 | \| | \| | \| | \| | #4 | 13 |
| 14 | \| | \| | \| | \| | #5 | 14 |
| 15 | \| | \| | \| | \| | #6 | 15 |
| 16 | \| | \| | \| | \| | #7 | 16 |
| 17 | \| | \| | \| | \| | #8 | 17 |
| 18 | 22 | 0.04 | 28 | Bi-level | Relay #9 Status | 18 |
| 19 | 22 | <0.01 | 28 | Bi-level | Relay #1 Control | 19 |
| 20 | \| | \| | \| | \| | #2 | 20 |
| 21 | \| | \| | \| | \| | #3 | 21 |
| 22 | \| | \| | \| | \| | #4 | 22 |
| 23 | \| | \| | \| | \| | #5 | 23 |
| 24 | \| | \| | \| | \| | #6 | 24 |
| 25 | \| | \| | \| | \| | #7 | 25 |
| 26 | \| | \| | \| | \| | #8 | 26 |
| 27 | 22 | <0.01 | 28 | Bi-level | Realy #9 | 27 |
| 28 | 22 | <0.01 | 15 | Analog | Meas #1 Current | 28 |
| 29 | \| | \| | \| | \| | #2 | 29 |
| 30 | \| | \| | \| | \| | #3 | 30 |
| 31 | \| | \| | \| | \| | #4 | 31 |
| 32 | \| | \| | \| | \| | #5 | 32 |
| 33 | \| | \| | \| | \| | #6 | 33 |
| 34 | \| | \| | \| | \| | #7 | 34 |
| 35 | \| | \| | \| | \| | #8 | 35 |
| 36 | 22 | <0.01 | 15 | Analog | Meas #9 Current | 36 |
| 37 | 22 | 0.8 | 28 | DC | 28 V Power | 37 |
| 38 | 22 | 0.1 | 300 | DC | Meas Line Volts | 38 |
| 39 | 22 | 0.1 | - | DC | 120 V (Signal) Gnd | 39 |
| 40 | 22 | - | - | - | Spare | 40 |
| 41 | \| | \| | \| | \| | \| | 41 |
| 42 | \| | \| | \| | \| | \| | 42 |
| 43 | \| | \| | \| | \| | \| | 43 |
| 44 | \| | \| | \| | \| | \| | 44 |
| 45 | \| | \| | \| | \| | \| | 45 |
| 46 | \| | \| | \| | \| | \| | 46 |
| 47 | \| | \| | \| | \| | \| | 47 |
| 48 | \| | \| | \| | \| | \| | 48 |
| 49 | \| | \| | \| | \| | \| | 49 |
| 50 | \| | \| | \| | \| | Spare | 50 |

## Table 3.3-9. Wire List

| ACES | COMPONENT - CABLE # WS2-( ) | LOAD BANK |
|---|---|---|
| Connector Terminal | | Connector Terminal |
| Cable and connector design specified in ACES Manual - see Westinghouse Dwg. No. 361332 | | |

## Table 3.3-10. Wire List

| BCU | COMPONENT - CABLE IDENT # WS3 | | | | | SMU |
|---|---|---|---|---|---|---|
| Connector P4 Terminal | AWG Gauge | Current Amps | Voltage Volts | Signal Type | Function | Connector P2 Terminal |
| 1 | 22 | 0.04 | 28 | Bi-level | Status PS-1 | 1 |
| 2 | \| | \| | \| | \| | \| BAT-1 | 2 |
| 3 | \| | \| | \| | \| | \| PS-2 | 3 |
| 4 | \| | \| | \| | \| | \| BAT-2 | 4 |
| 5 | \| | \| | \| | \| | \| Main Bus 1 | 5 |
| 6 | \| | \| | \| | \| | \| Main Bus 2 | 6 |
| 7 | \| | \| | \| | \| | \| Load Bus 1 | 7 |
| 8 | \| | \| | \| | \| | \| Load Bus 2 | 8 |
| 9 | \| | \| | \| | \| | \| Load Bus 3 | 9 |
| 10 | \| | \| | \| | \| | \| Load Bus 4 | 10 |
| 11 | \| | \| | \| | \| | \| Load Bus 5 | 11 |
| 12 | \| | \| | \| | \| | \| Load Bus 6 | 12 |
| 13 | \| | \| | \| | \| | \| Load Bus 7 | 13 |
| 14 | \| | \| | \| | \| | \| Load Bus 8 | 14 |
| 15 | \| | \| | \| | \| | \| Parallel Alert | 15 |
| 16 | 22 | 0.04 | 28 | Bi-level | Status Parallel Active | 16 |
| 17 | 22 | <0.01 | 28 | Analog | Meas Current PS-1 | 17 |
| 18 | \| | \| | \| | \| | \| Current BAT-1 | 18 |
| 19 | \| | \| | \| | \| | \| Current PS-2 | 19 |
| 20 | \| | \| | \| | \| | \| Current BAT-2 | 20 |
| 21 | \| | \| | \| | \| | \| Current Main Bus 1 | 21 |
| 22 | \| | \| | \| | \| | \| Current Main Bus 2 | 22 |
| 23 | \| | \| | \| | \| | \| Voltage PS-1 | 23 |
| 24 | \| | \| | \| | \| | \| Voltage BAT-1 | 24 |
| 25 | \| | \| | \| | \| | \| Voltage PS-2 | 25 |
| 26 | 22 | <0.01 | 28 | Analog | Meas Voltage BAT-2 | 26 |
| 27 | 22 | <0.01 | 28 | Bi-level | Command BAT-1 Main Bus 1 | 27 |
| 28 | \| | \| | \| | \| | \| PS-1/Main Bus 1 | 28 |
| 29 | \| | \| | \| | \| | \| BAT-2/Main Bus 1 | 29 |
| 30 | \| | \| | \| | \| | \| PS-1/Main Bus 1 | 30 |
| 31 | \| | \| | \| | \| | \| BAT-1/Main Bus 2 | 31 |
| 32 | \| | \| | \| | \| | \| PS-1/Main Bus 2 | 32 |
| 33 | \| | \| | \| | \| | \| BAT-2/Main Bus 2 | 33 |
| 34 | 22 | <0.01 | 28 | Bi-level | Command PS-2/Main Bus 2 | 34 |
| 35 | 22 | 0.04 | 28 | Bi-level | Command Parallel Source | 35 |
| 36 | 22 | 2.0 | 28 | DC | 28 V Power | 36 |
| 37 | 22 | 2.0 | - | DC | 120 V Grnd | 37 |
| 38 | 22 | - | - | - | Signal Grnd | 38 |
| 39 | 22 | - | - | - | Spare | 39 |
| 40 | \| | \| | \| | \| | \| | 40 |
| 41 | \| | \| | \| | \| | \| | 41 |
| 42 | \| | \| | \| | \| | \| | 42 |
| 43 | \| | \| | \| | \| | \| | 43 |
| 44 | \| | \| | \| | \| | \| | 44 |
| 45 | \| | \| | \| | \| | \| | 45 |
| 46 | \| | \| | \| | \| | \| | 46 |
| 47 | \| | \| | \| | \| | \| | 47 |
| 48 | \| | \| | \| | \| | \| | 48 |
| 49 | \| | \| | \| | \| | \| | 49 |
| 50 | 22 | \| | \| | \| | Spare | 50 |

Table 3.3-11. Wire List

| ACES | COMPONENT - CABLE # WS4 | LOAD BANK |
|---|---|---|
| Connector Terminal | | Connector Terminal |
| Cable and Connector design specified in ACES manual - see Westinghouse Dwg. No. ED361332 | | |

## 3.3.2 Connectors

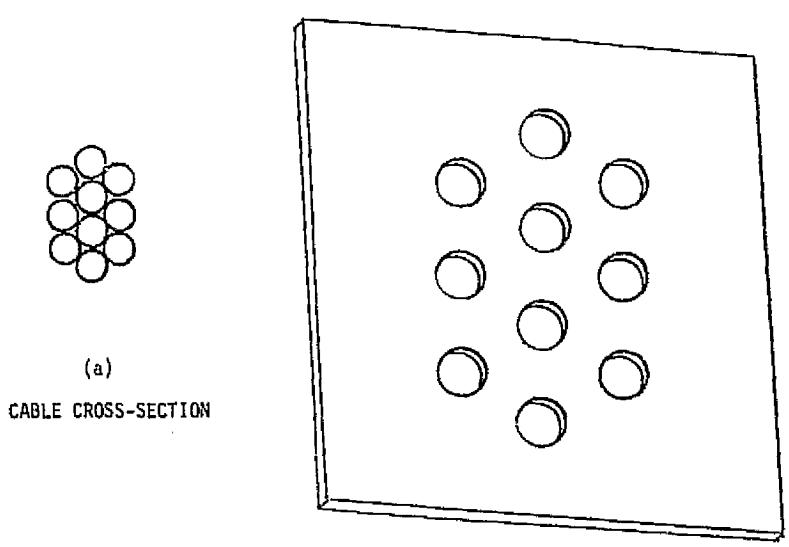
Connectors may be of any manufacture of good commercial quality. MFSC part numbers for applicable connectors are provided in Table 3.3-12.

Table 3.3-12. Facility Connectors

| | |
|---|---|
| P1-( ) | NB6E22-55SNC |
| J1-( ) | NB7E22-55PNC |
| P2 | NB6E22-55SNC |
| J2 | NB7E22-55PNC |
| P3 | NB6E14-4PNC |
| J3 | NB7E14-4SNC |
| P4 | NB6E22-55PNC |
| J4 | NB7E22-55SNC |
| P5-( ) | NB6E14-4SNC |
| J5-( ) | NB7E14-4PNC |
| P6-( ) | NB6E22-55PNC |
| J6-( ) | NB7E22-55SNC |
| ACES CONNECTORS | Per Westinghouse Dwg. No. EDP 361332 |

### 3.3.3 Harness Assembly

There are a number of possible cross-section configurations for the main bus power cable which result in desired minimum spacing between conductors. However, unless potting or a non-standard harness tie is used, the cable will assume an approximation of the configuration shown in Figure 3.3-4a due to the radial force of the harness ties and the low friction of the teflon insulation. Consequently, the selected conductor orientation will conform to this configuration. Control of conductor orientation during assembly may be maintained by the use of a simple pattern, Figure 3.3-4b, which may be easily fabricated. The ends of the conductors are passed through the pattern and fastened with harness ties. The pattern is moved along the conductors maintaining the cross-section configuration of the cable as harness ties are added. The cable may be assembled in this way in any convenient area or in the cable duct. The relative disadvantages of threading a long heavy cable through the duct supports and working on scaffolding will need to be evaluated at the time of assembly. The decision with regard to twisting the main bus is considered an important factor in this design. Resolution of this issue must await discussion with MSFC engineers and evaluation of assembly resources.



(a)
CABLE CROSS-SECTION

(b)
CABLE ASSEMBLY PATTERN

Figure 3.3-4. Cable Configuration Control

The prefabricated cables for the remainder of the harness will be placed in the cable tray individually and secured to the trays and to each other. Cable entry and exit from the duct may be over the sides of the tray or through access ports if available. A constant physical configuration is necessary to maintain test control during an extended study program. Sections of cable which run between the duct and test facility components should be supported and secured to metal struts to maintain cable configuration and also protect personnel from damaged conductors. The metal struts should be bonded to the component and cable duct to maintain frame ground continuity.

### 3.3.4 Cable Trays

The cable tray or duct provides support for the cable, simulates vehicle structure and provides protection from arcing for the operating personnel. The cross-section of the duct should provide 9.7 $cm^2$ for each (100A) load bank served; cable weight is approximately 1.0 kg/m for each (100A) load bank served. Although the present steady state capability of the power supplies is three hundred amperes (300A), it is assumed that six load banks with one hundred ampere capability each may be used in the facility. On this basis, the requirements for the cable duct are:

| | |
|---|---|
| Conductor Carrying Cross-Section | 58 $cm^2$ (minimum) |
| Support Weight | 6.25 kg/m (minimum) |

The configuration of the cable tray as shown in Figure 3.3-5 permits more flexibility in selection of cable routing than the previous approach which featured a single continuous path. Junction boxes have also been discarded as an unnecessary complication. The cable trays may be fabricated out of any material although non ferrous metal is preferred. The trays must be electrically bonded together and to the structures of the HVDC Test Facility for personnel safety and correct conditions. Notices must be posted to display hazardous voltages and current warnings.

### 3.3.5 Functional Test

The number of wires and level of complexity of the test facility cable do not justify use of specialized harness verification and test equipment frequently utilized for this purpose. However, if such equipment

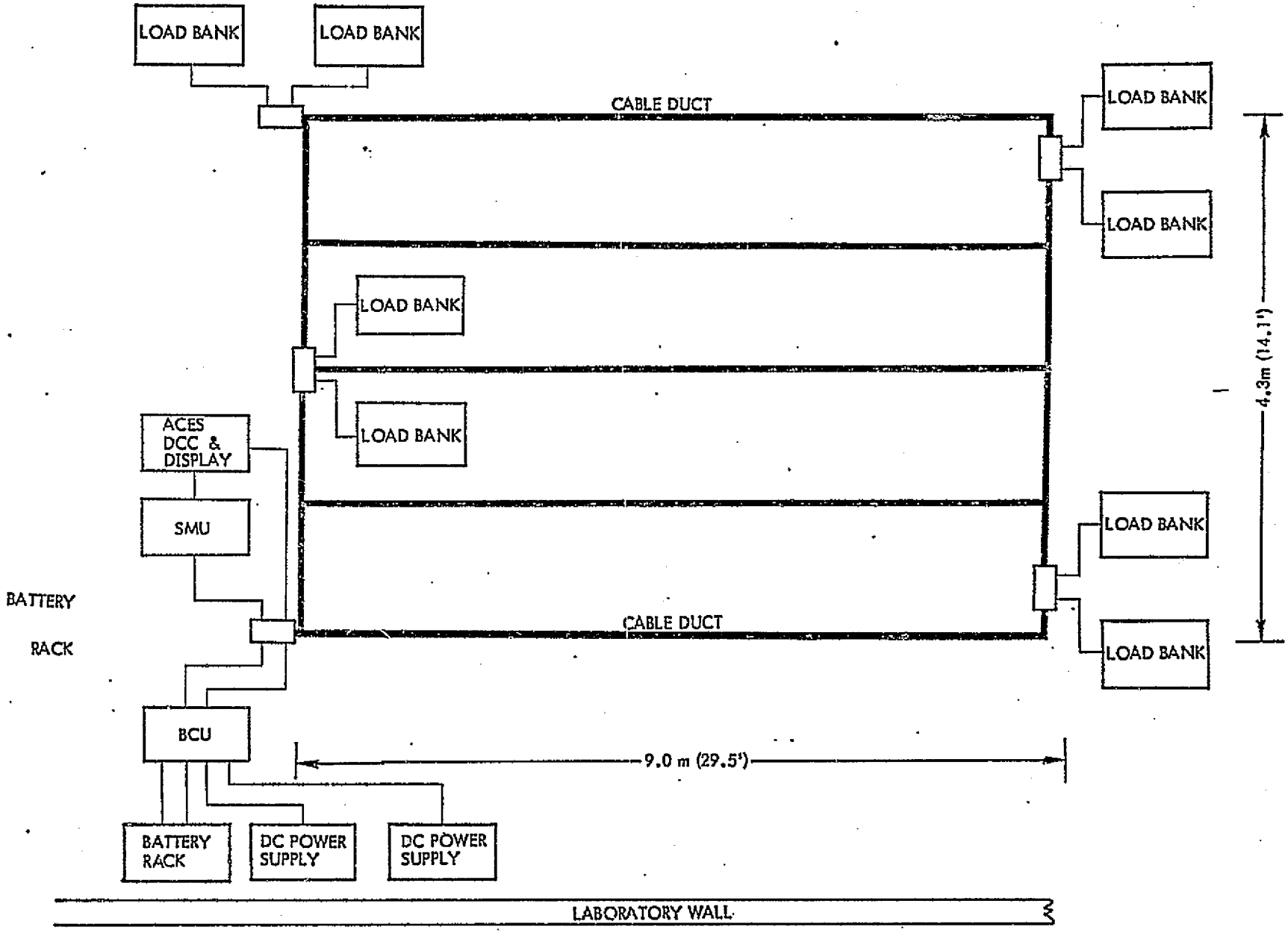



Figure 3.3-5. Cable Tray

is readily available, time and effort may be conserved. Tests on cables shall meet the following criteria.

- Continuity Test — $R <$ The greater of 1.1 $R_o$, 0.2 ohms
  $R_o$ = Calculated conductor resistance

- Connectors main bus terminal lugs shall provide less than 0.1 volts drop between wire and terminal strip while conducting ten (10) amperes.

- Leakage Test

| | |
|---|---|
| Leakage Voltage | 1500 VDC $\pm$ 10% |
| Leakage Resistance | > 100 Megohms |
| Leakage Dwell | 1/2 Second Minimum |

- Inspection - Verify that power source cabling polarity is maintained correctly.

  Verify that individual conductors in the main bus are connected to their designated terminals.

It must be noted that despite simple test requirements, the Test Facility will contain hazardous voltage and current. Assembly errors are a source of danger to personnel as well as a potential cause of equipment damage.

## 3.4 SOURCE SIMULATOR DESIGN

The power source for the Multi-KW HVDC Test Facility consists of two 120V battery packs and two 2-130 Vdc power supplies. The functional schematic diagram of Figure 3.4-1 defines the electrical interface between the power source and the test facility elements. Power source configuration is controlled by the battery and power source switch panels; system power control is provided by switchgear in the BCU. The power source design provides simulation of a large fuel cell with steady-state power of 36 KW at 120 and 240 Vdc.

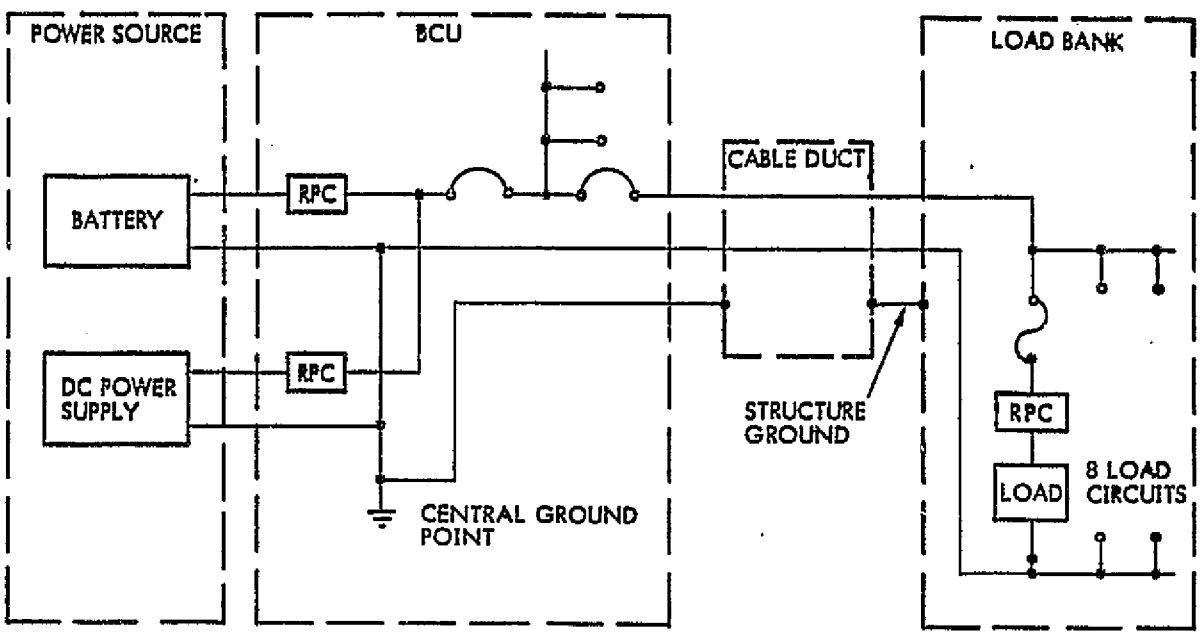



Figure 3.4-1. Power Distribution Circuit Elements

### 3.4.1 Power Source Requirements

The power source is required to provide simulation of large spacecraft power source under steady-state and major fault transients to enable the study of power distribution characteristics, power switchgear performance, and fault removal techniques. The required characteristics were based on expected performance of fuel cell power sources and were defined in Phase I report (Multi-KW DC Power Distribution System Study Program, Contract NAS8-28726, April 1974).

Power Source Characteristics (Fuel Cell)

| | |
|---|---|
| Voltage | 28-120 Volts |
| Current | 0-150 Amperes |
| Response | 10 msec |
| Dynamic Impedance | 15 mohms |
| Static Impedance | 30 mohms |

Effective simulation of flight hardware electrical performance is required. Physical, thermal, and life requirements are to be consistent with laboratory applications and constraints. Maximum use of cost effective commercial/industrial quality equipment where appropriate is a preferred approach.

### 3.4.2 Power Source Hardware

The configuration of the Test Facility power source is illustrated in Figure 3.4-2. Batteries and power supplies were selected during the previous phase of this study.

The electrical and physical characteristics of the system elements are as follows:

Power Supply (Christie Electric 2C0135-150E4S)

| | |
|---|---|
| Voltage | 2-135 Volts dc |
| Current | 0-150 Amperes |
| Output KW | 20KW Max |
| Regulation (Static) | 0.1% or 50MV |
| Regulation (Dynamic) | 10 Volts (No Load - Full Load) |
| Ripple | 100 mv |
| Response Time | 50 msec (No Load - Full Load)<br>125 msec (Full Load - No Load) |
| Input Power | |
| Voltage | 220/440/480 3Ø AC 57-63 Hz |
| Current | 46 Amperes/Phase (440 Vac) |
| Weight | 650 lbs |
| Size | 18"(W) x 22 1/8"(D) x 30 7/8"(H) |
| Number Required | 2 |

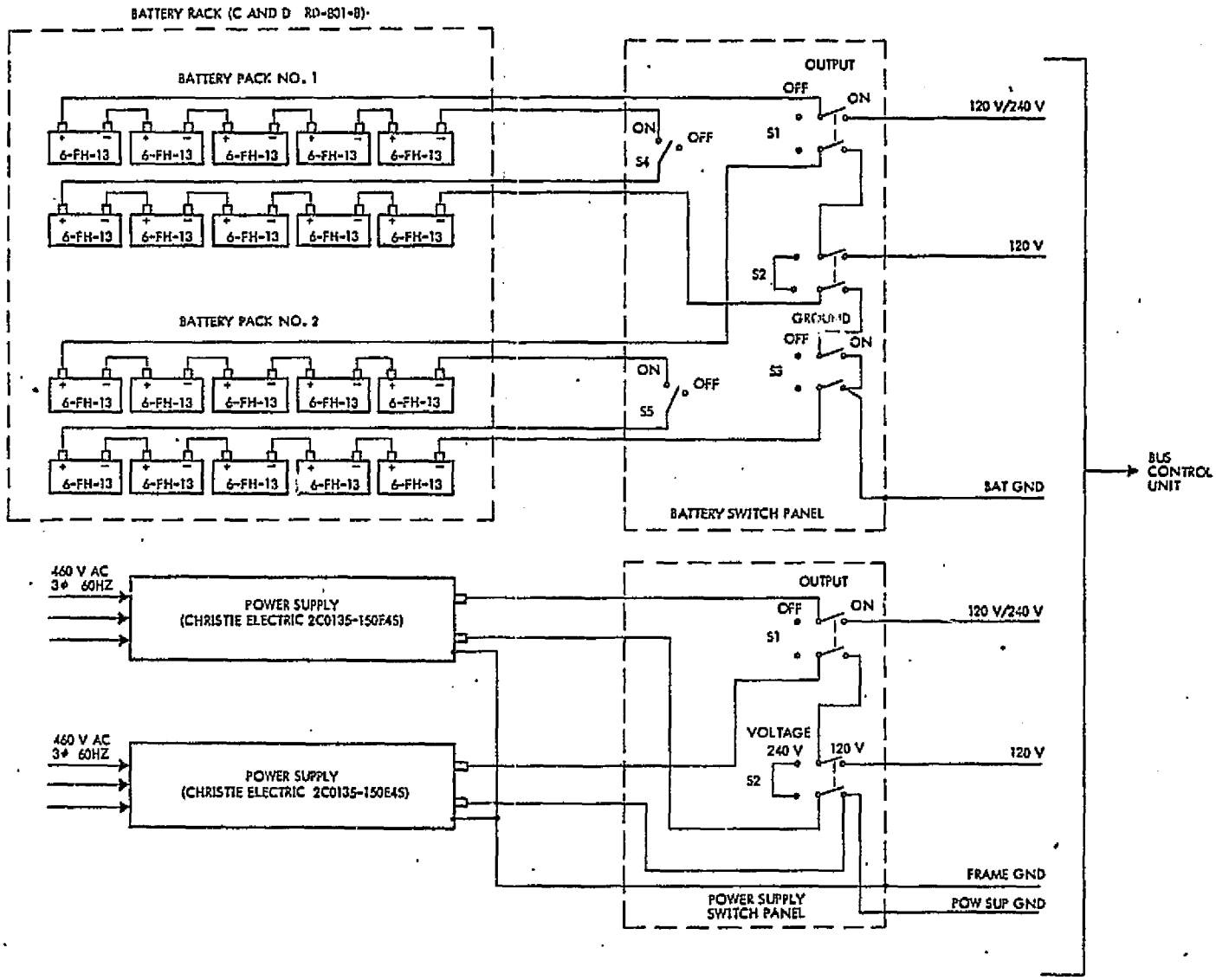



Figure 3.4-2. Power Source

Batteries (Exide 6-FH-13)

| | |
|---|---|
| Type Cell | Lead Acid |
| Capacity | 90 Ampere-Hours (5 hour rate)<br>32 Ampere-Hours (5 minute rate) |
| Voltage | 12 Volts |
| Plates/Cell | 13 |
| Size | 14 1/4"(L) x 7 5/16"(W) x 10 13/16"(H) |
| Weight | 78 lbs (Filled) |
| Number Required | 30 (Includes 10 Spares) |

Battery Rack (C&D Batteries RD-80i-8)

| | |
|---|---|
| Type | Two Tier |
| Size | 96"(L) x 16"(W) x 35 11/16"(H) |
| Weight | 132 lbs |

The function of the switch panels is to enable implementation of 120V and 240V configurations. Switches are also provided to open ground, output, and intermediate terminals. This reduces the possibility of contacting hazardous voltage during assembly and maintenance.

### 3.4.3 Performance

The quality of performance of the power source is determined by the degree to which an effective simulation of a fuel cell is achieved. The analysis of fuel cell performance was performed in the previous report; the equivalent circuit is shown in Figure 3.4-3.

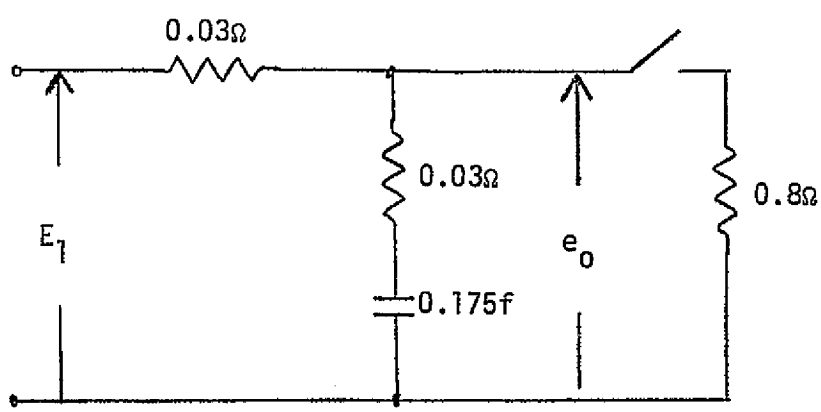



Figure 3.4-3. Fuel Cell Equivalent Circuit

The expected response to a 150 ampere step load from a 120 volt source is,

$$e_o = 0.965(120)(1 + 0.0187e^{-98.2t}) \qquad \text{Eq. 3.4-1}$$

A preliminary analysis of the Christie power supply based on output transient measurements was also performed and the equivalent circuit is illustrated in Figure 3.4-4. The output response of this circuit to a 150 ampere step load indicated in Equation 3.4-2.

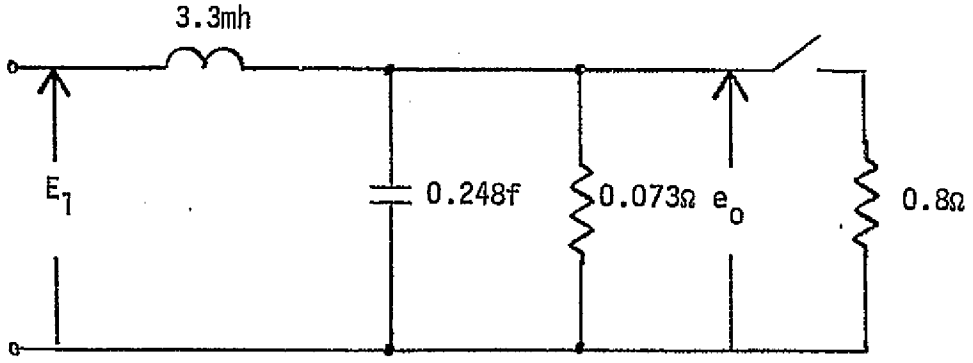



Figure 3.4-4. Power Supply Equivalent Circuit

$$e_o = 120(1 - 0.289e^{-30.2t} \text{ Sin } 17.5t) \qquad \text{Eq. 3.4-2}$$

During simulation of a fuel cell source, it is planned to parallel two 120V battery packs and one Christie power supply. Analysis in the previous report has shown that the equivalent source impedance of the batteries will be approximately 0.037 ohms. The equivalent circuit is illustrated in Figure 3.4-5.

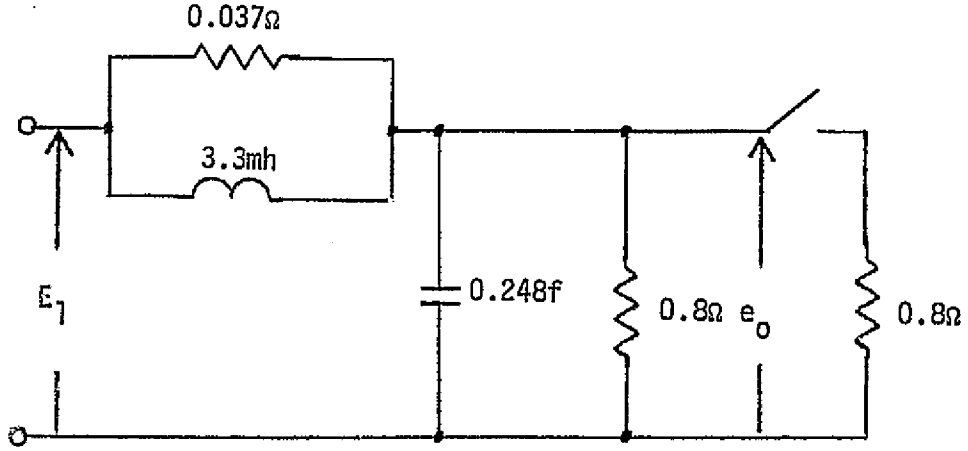



Figure 3.4-5. Combined Battery and Power Supply

Response to the 150 ampere step load is,

$$e_o = 120(1 - 0.026e^{-84.7t} \text{ Sinh } 77.1t)$$

$$= 120(1 + 0.026e^{-161.8t} - 0.026e^{-7.6t}) \qquad \text{Eq. 3.4-3}$$

The addition of resistance in series with the power supply completes the simulation configuration as illustrated in Figure 3.4-6.

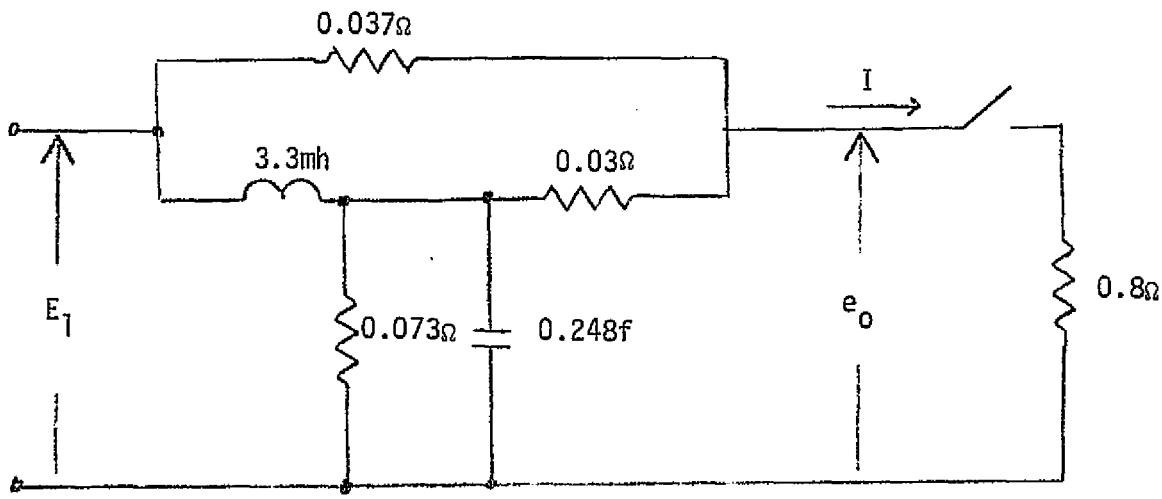



Figure 3.4-6. Fuel Cell Simulation (I<300a)

The output response to the 150 ampere step load is then,

$$e_o = 0.979(1 + 0.032e^{-105.5t} + 0.032e^{-11.7t}) \qquad \text{Eq. 3.4-4}$$

Comparison with Equation 3.4-1 indicates that this response is a reasonable approximation of the Fuel Cell Source.

Use of the batteries and combinations of small resistances and large capacitors would provide a more accurate simulation. However, the major function of the battery is to supply high fault pulse current. The power supply provides steady-state loads and maintains the batteries in the necessary fully charged state prior to fault testing. When a major fault condition is simulated, the maximum output of the power supply may be exceeded if fault removal techniques are not in effect. At that point (approximately 300 amperes), the power supply performs an automated shut-down and the batteries provide the total load current. The source

impedance then consists of the series 0.037 ohms of the battery and a shunt element comprised by the 0.03 ohm resistance added to the power supply and the power supply output capacitance of 120,000 μf. This network (Figure 3.4-7) continues to provide good simulation of the fuel cell source.

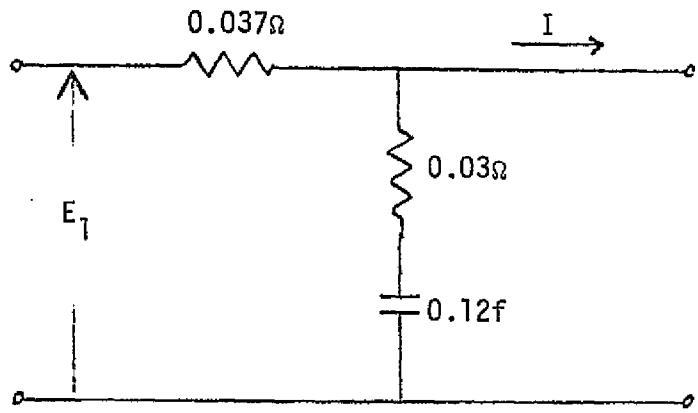



Figure 3.4-7. Fuel Cell Simulator (I>300a)

### 3.4.4 Battery Charging

The batteries may be floated on the power bus during normal operation to maintain full charge and to control the power source impedance parameters. If the batteries are not to be used for extended periods, life will be extended by complete discharge. Subsequent to such periods, recharging is necessary and will be performed by manual control. The recharge operation may be implemented conveniently through the Bus Control Unit as illustrated in Figure 3.4-8. Battery supplier instructions should be followed; however, there are no critical factors involved. Charging may be performed at high rates without damage or hazardous electrical and thermal conditions. Care must be exercised to insure venting of effluent gases to outside air. The following simple procedure should be sufficient to perform the battery charging operation.

1. Open main breakers (BCU).
2. Adjust power supply(s) to two (2) volts less than the battery voltage.
3. Close the contactors which establish the desired charge path.
4. Raise the power supply voltage until the required charge rate is established.
5. Periodic adjustments will be required until the desired float potential is achieved.

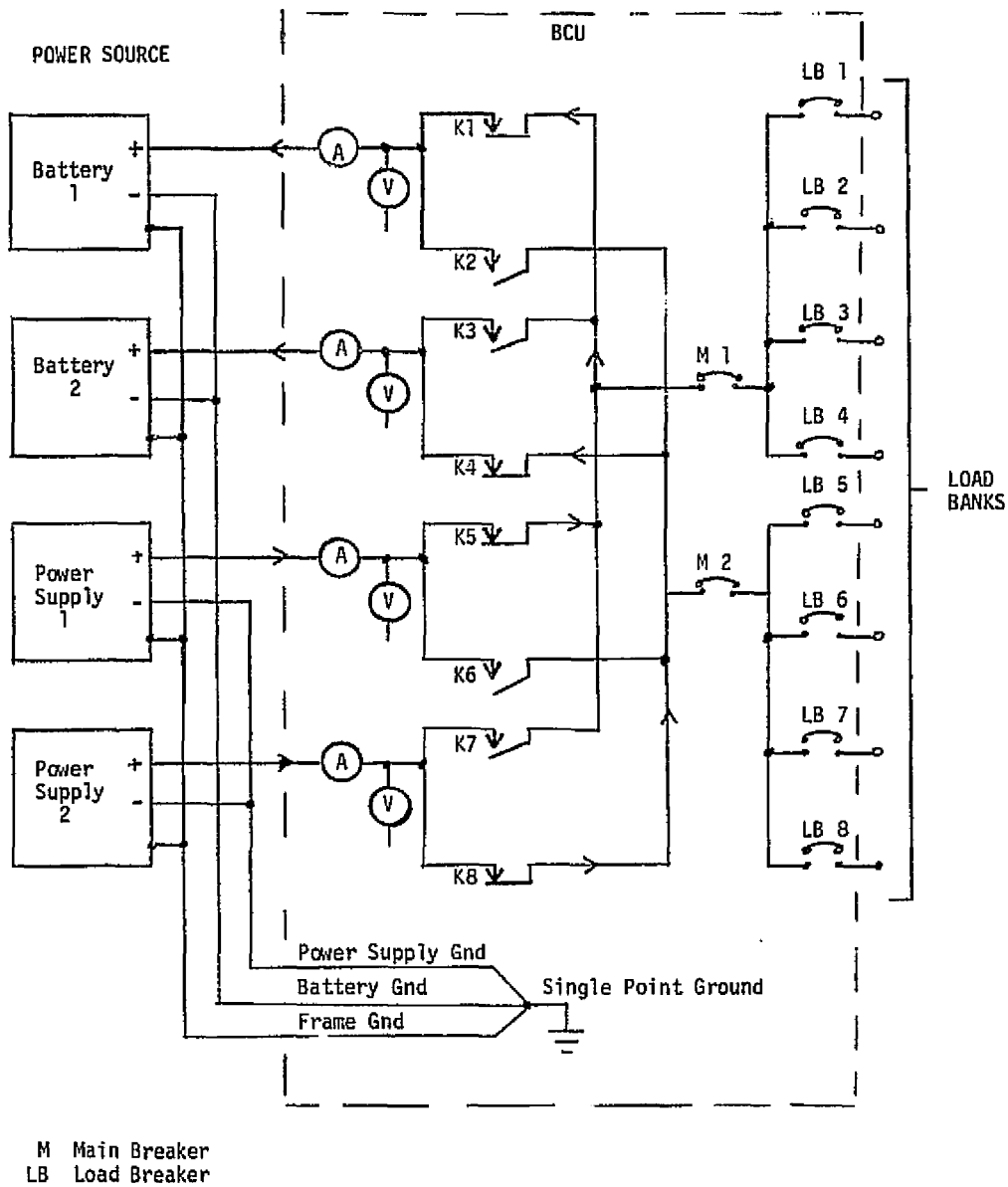



Figure 3.4-8. Battery Charging Paths

It should be noted that the power source involves hazardous voltages and currents. Adequate switching capability is provided to reduce the necessity of working on active circuits; however, batteries cannot be turned off. During assembly and modifications of the battery pack, it will be necessary to operate with essential live circuits. While shock hazard is small, the inherent high current capability can produce arcing and heat hazards.

## 3.5 SUPERVISION AND CONTROL

The HVDC Test Facility provides a means for comparison of conventional (analog, bi-level) and digital supervision and control approaches. The conventional design has been defined in the current study; the digital system is a Westinghouse development and the components for a limited installation are available at MSFC. These supervision and control systems simulate a "cockpit" control panel and will also serve as a test control station during facility test operations. Both systems are connected at all times and facility subsystem functions may be operated to the "ON" condition from either panel on a logical "OR" basis. During normal operation simulation one of the systems will have all control functions set to the "OFF" condition to prevent functional interference. Data may be displayed on both consoles at all times. In addition to these supervision and control systems, manual controls and test jacks are provided on the Load Banks for local control and measurements. All local controls will be set in the "OFF" condition during normal facility operation. Precise measurements, EMI evaluation and transient performance will be implemented with one or more mobile test racks which may be moved conveniently to the test location. Semi-permanent test sets are preferred to maintain control measurement parameters particularly when several interconnected pieces of equipment are required for a test program. These test sets were defined in Phase 1 of this study program and will be summarized in subsequent paragraphs.

### 3.5.1 Digital Control

The ACES system developed by Westinghouse utilizes a digital command and data acquisition approach to control remote power switching devices and monitor binary data which describe the state of a power distribution system. Drawing and descriptions at the ACES equipment were taken from the Automatically Controlled Electrical Systems (ACES), System and Operational Description Manual, October 1972.

Signals are transmitted on a redundant data bus which provides weight and reliability advantages over the classic separately wired approach. Control of the system is maintained with a small general purpose computer using time multiplexed signals. In addition it may be programmed for self checkout, automatic fault sensing and control and power sequencing. The

functional elements of the system are the general purpose computer which is designated Distribution Control Center (DCC), and local interface equipment designated Remote Input/Output unit (RIO) and the operators panel designated Data Entry and Display (DED). The system is designed with the intent to interface with solid state RPCs but is compatible with electronic/electromagnetic power switchgear. The general configuration of the system is illustrated in Figure 3.5.1-1. The RIO provides all interfaces between the DCC, the power distribution system and the DED. The major components of the system are connected in a triply redundant configuration as illustrated in Figure 3.5.1-2. The internal circuits in each RIO are also triple redundant.

The following is a brief description of the elements of the system. Complete details may be found in System and Operational Description Manual provided by Westinghouse at MSFC.

### 3.5.2 Distribution Control Center (DCC)

The DCC is a small general purpose military type computer of modular design and uses standard transistor-transistor-logic (TTL) integrated circuit devices of medium scale integration (MSI) complexity to maximum advantage. It is composed of control, arithmetic, memory and input/output units.

The control unit operates with 16 single-address instructions, all indexable and capable of using any one of eight general purpose registers. A computing speed of over 300,000 instructions per second is obtained with magnetic core memory.

The arithmetic unit features parallel arithmetic logic on the 16 bit words. It uses fixed point, fractional two's complement notation. It contains eight general purpose registers.

The magnetic memory is in 4096 word modules and is expandable to 16 modules; cycle time is 1.0 microsecond. The approximate memory requirement for this system is 1K words per RIO; this includes all software functions.

The DCC input/output unit contains a serial data transmission capability for multiplexed communication with the RIOs, a real time clock, and

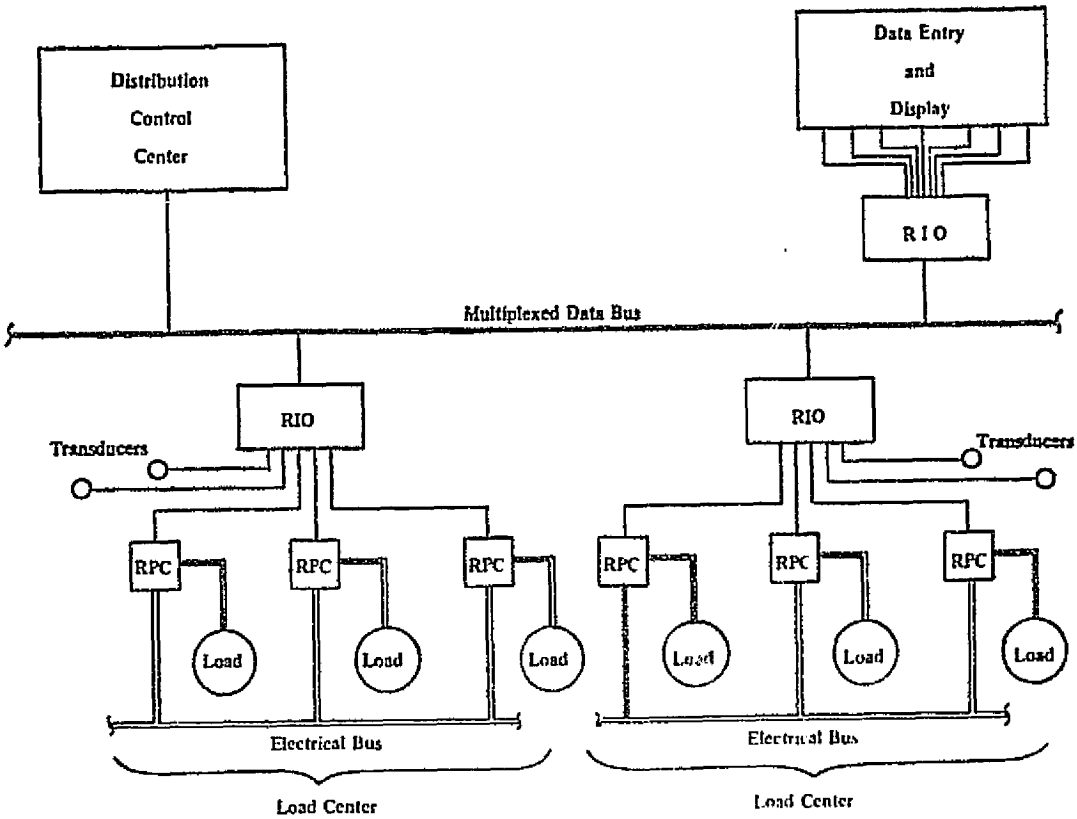



Figure 3.5.1-1. System Schematic

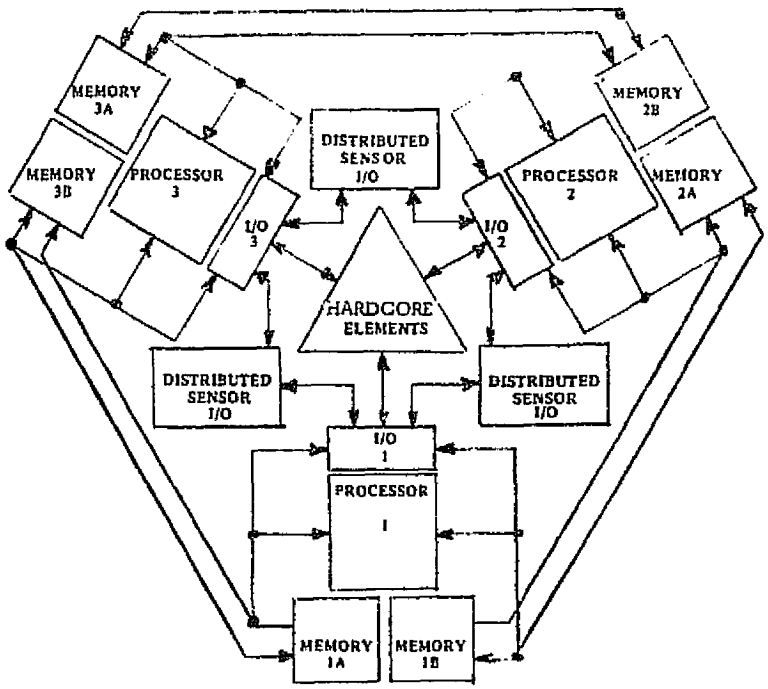



Figure 3.5.1-2. Triple Redundant System - ACES

additional input/output mode control. The buses which interconnect the DCC with the RIOs are in triplet, with provision in the DCC for built-in test to verify the integrity of each bus individually. The unit can withstand a data bus short circuit to ground on any one bus, or a short between DATA I and DATA II without damage.

### 3.5.3 Data Entry and Display Panel (DED)

The DED contains a 10 digit keyboard, a numerical display and several switches and indicating lamps. An operator can open or close an RPC by keying in the appropriate three digit RPC address and pressing the "open" or "close" switch. The DCC is programmed to permit keyboard control of only selected RPCs. If an incorrect address or an address of an RPC not subject to keyboard control is keyed in, the "invalid address" lamp will light.

If an RPC trips, the "RPCs tripped" lamp lights. The addresses of the tripped RPCs can be displayed by switching to the "RPCs trip" mode and pressing the "clear/update" switch.

If the system goes into an automatic load shedding mode, the "loads shed" lamp will light. The addresses of the RPCs controlling the shed loads can be displayed in a manner similar to that for tripped RPCs by switching to the "loads shed" mode.

### 3.5.4 Remote Input/Output Units (RIOs)

Each RIO will accommodate up to 64 transistors, status lamps, RPCs or any combination thereof. Each has 64 command output and 64 status inputs. The control outputs provide signals which activate an RPC or the panel indicator. The status inputs accept signals form transducers, limit switches, and the status indicator output of an RPC.

The RIOs are assigned an address via a permanently wired mating connector, so each RIO in the system has a unique address code. Random access to the RIOs in the system is thus provided with only one part number RIO.

Each RIO is constructed in triplet in such a manner that it is essentially three input/output units, each one driven by a separate data bus.

Each unit is completely self-contained with its own power supply, each power supply provided with three sources of power. Thus a failure in one unit will not propagate into another unit. The outputs of the units are joined at a buffer which drives the RPCs. Each RPC has its own buffer unit. A failure in any portion of the individual units has no effect on system performance. A failure in the buffer affects only one RPC. Each buffer can be current limited so that the output may be short circuited without disturbing the rest of the control system.

### 3.5.5 ACES Interface

Interfaces exist between ACES, the Test Facility and the conventional Supervision and Monitor Unit (SMU) at the control input to the relay drivers and the output from the status sensors. These circuits are discussed in sufficient detail in Section 3.2 Load Bank Design. Control and status sense interface circuits are shown in Figure 3.5.5-1a and 3.5.5-1b. The ACES interface parameters are given in Table 3.5.5-1. This data was obtained informally from Westinghouse personnel and engineering sketches.

Table 3.5.5-1. Interface Definition

| ACES | TEST FACILITY |
|---|---|
| Control | Relay Driver |
| "ON" | |
| Open Circuit Voltage (L) <28V* | Maximum Input Voltage (P) > 40V |
| Maximum Load Current (P) <0.04A | Maximum Input Current (L) @ 30V <0.006A |
| "OFF" | |
| Maximum Output Current (L) <40μa | Maximum Input Current (P) <200μa |
| Status Sense | Status Output |
| Sense "ON" | |
| Output Current (L) 2.7±20 milliamps | Min. Sink Current (R) >100 ma |
| Sense "OFF" | |
| Maximum Sink Current (P) <40μa | Max Sink Current (L) <0 |
| Open Circuit Voltage <15V (L) | |
| L = Circuit Limited | * Power Source Voltage |
| P = Permissible Limit | |
| R - Required Value | |

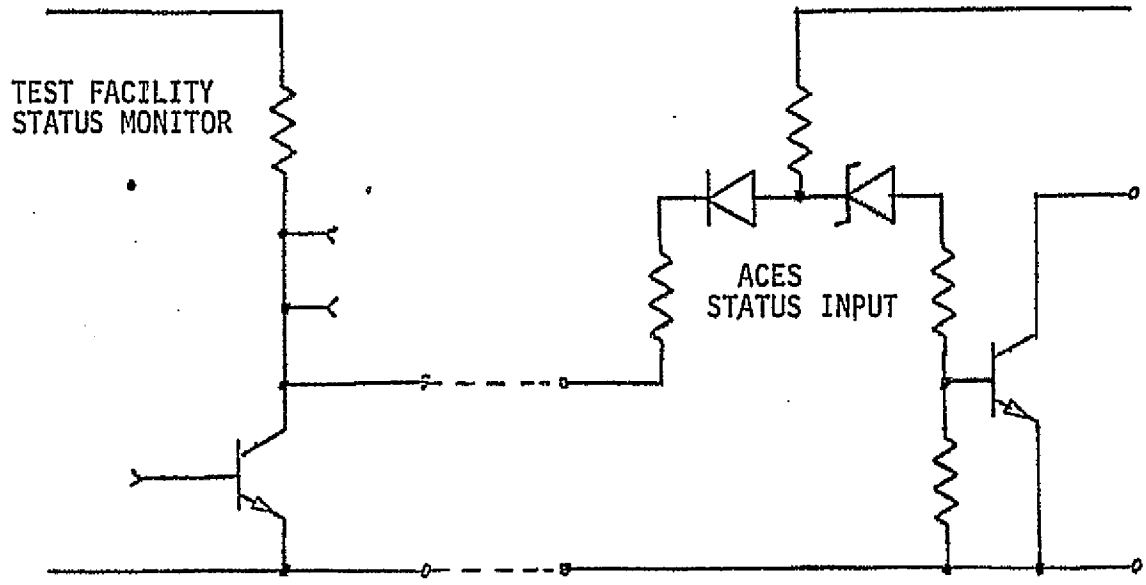



Figure 3.5.5-1a. Status Monitor Interface - ACES

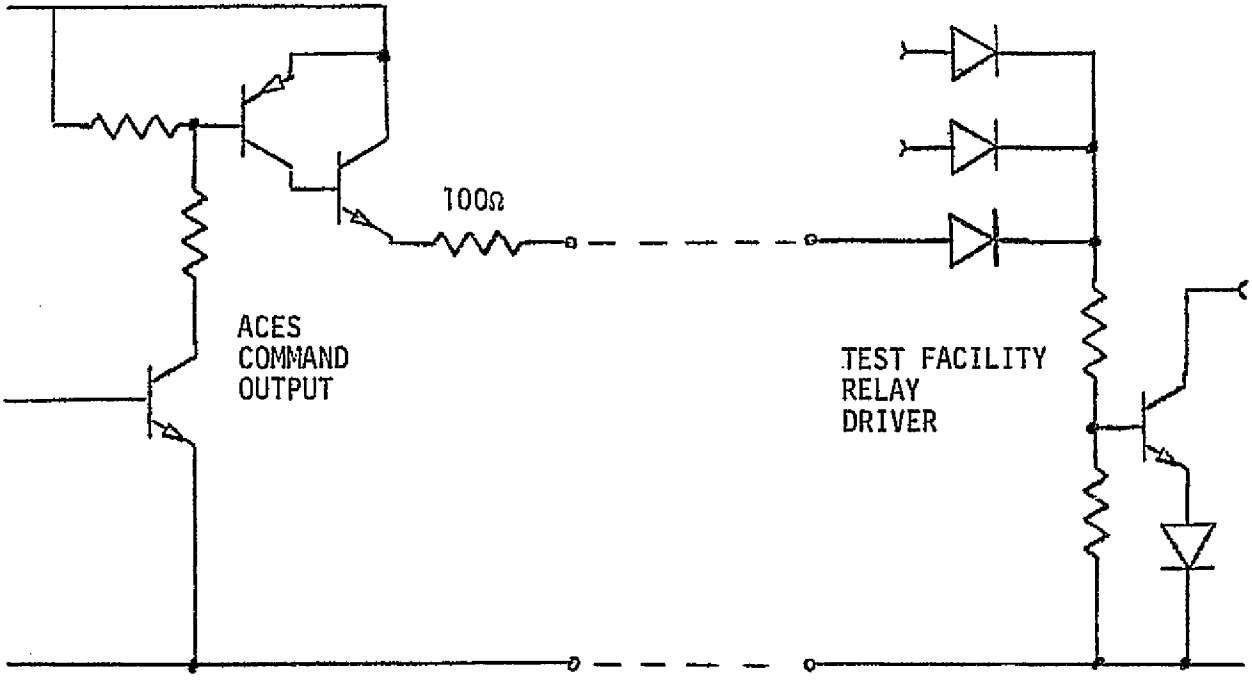



Figure 3.5.5-1b. Command Interface - ACES

### 3.5.6 Supervision and Monitor Unit

The Supervision and Monitor Unit (SMU) provides displays and controls of BCU and Load functions. The BCU functions are located on the left side of the panel (Figure 3.5.6-1) and provide individual controls to connect any one of the four power sources to either main bus. Paralleling power

supplies is inhibited by logic in the BCU; attempts to connect two power sources to one main bus will result in a Parallel Source C/W alert. Parallel source operation can be enabled by moving the Parallel Source C/W switch to "ON". Status lamps indicate presence of voltage from a power source at the input to the BCU, main bus voltage and load bank bus voltage. Voltage and current for any one power source may be selected and displayed on a dual face vertical scale meter. Load bank bus current and voltage and individual load channel current are also displayed as selected by the rotary switches. The status of all load bank fuses and relays are displayed on the right side of the panel along with the relay control panel switches. This is somewhat more elaborate than would be expected in a conventional "cockpit" control panel, however the displays are considered consistent with the experimental nature of the Test Facility.

### 3.5.6.1 SMU Circuit Design

The SMU functions are implemented with simple switching network and passive components. The Load Banks and the BCU provide required supply voltages and grounds on an individual basis to prevent ground loops. The SMU interfaces with the BCU through receptacle J2. Associated control and display circuits are illustrated in Figure 3.5.6-2. Panel lights have been added to provide quick look source control status consistent with the Load Bank displays. Load Bank voltage and current control and display circuits are shown in Figure 3.5.6-3. Interface connections for eight Load Banks are provided through receptacles J1-1 through J1-8. Load Channels are selected by rotary switch S12; Load Banks are selected by rotary switch S13. Panel lamp and load channel switching circuitry is shown in Figure 3.5.6-4. Signals to each switch contact and panel lamp are indicated by the listing for the J1 receptacle on Figure 3.5.6-3 and 3.5.6-4.

It has been assumed that the panel lamps will require at least 40 ma at 28VDC. Signal conditioner design for the meter displays has assumed input resistance greater than 100KΩ for the meters. Specific hardware has not been defined for the SMU since it is expected that MSFC stores will supply available parts. Deviations from the circuit design assumptions are not expected to require redesign. However, it such redesign is indicated, only minor modifications would be required.

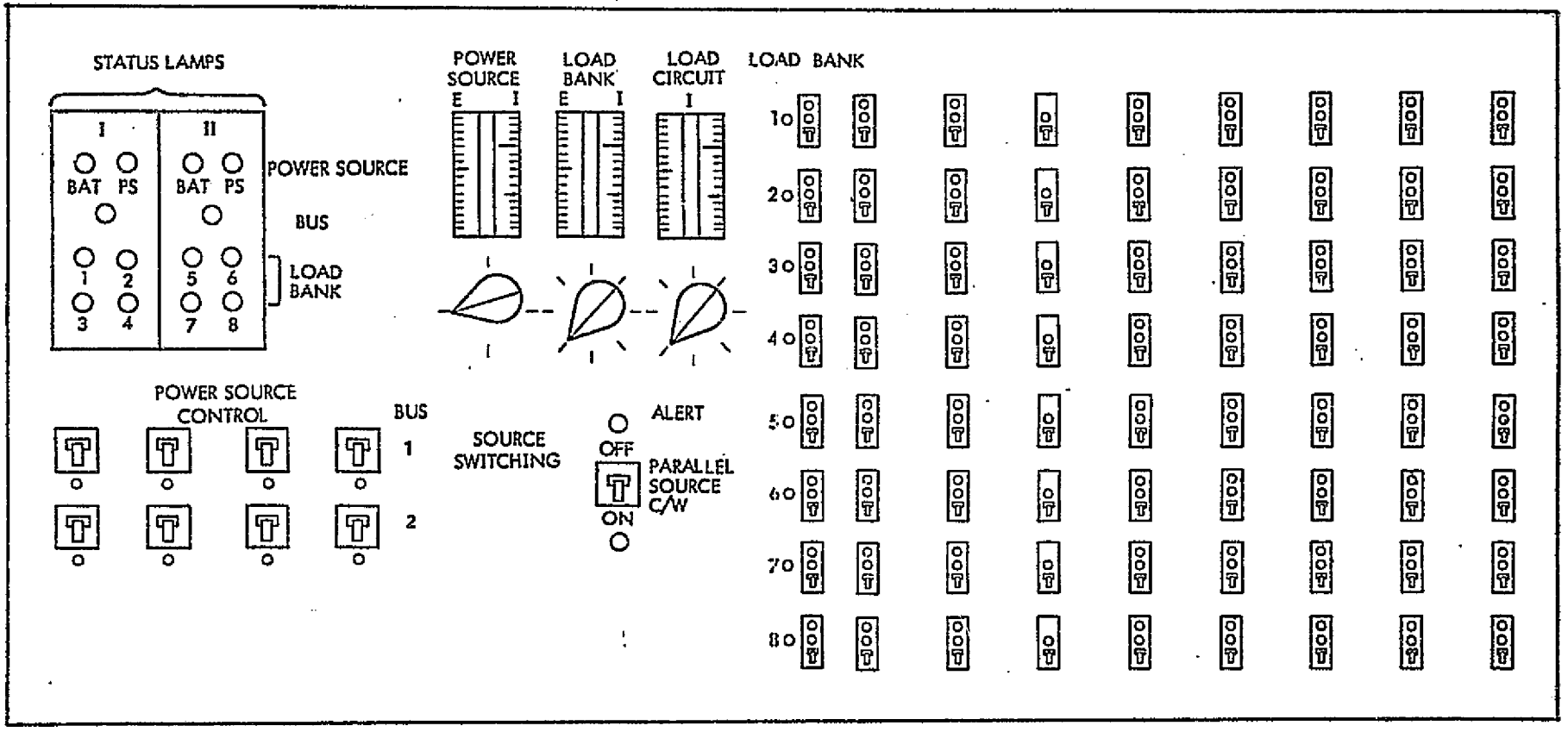



Figure 3.5.6-1. Supervision and Monitor Control and Display Panel

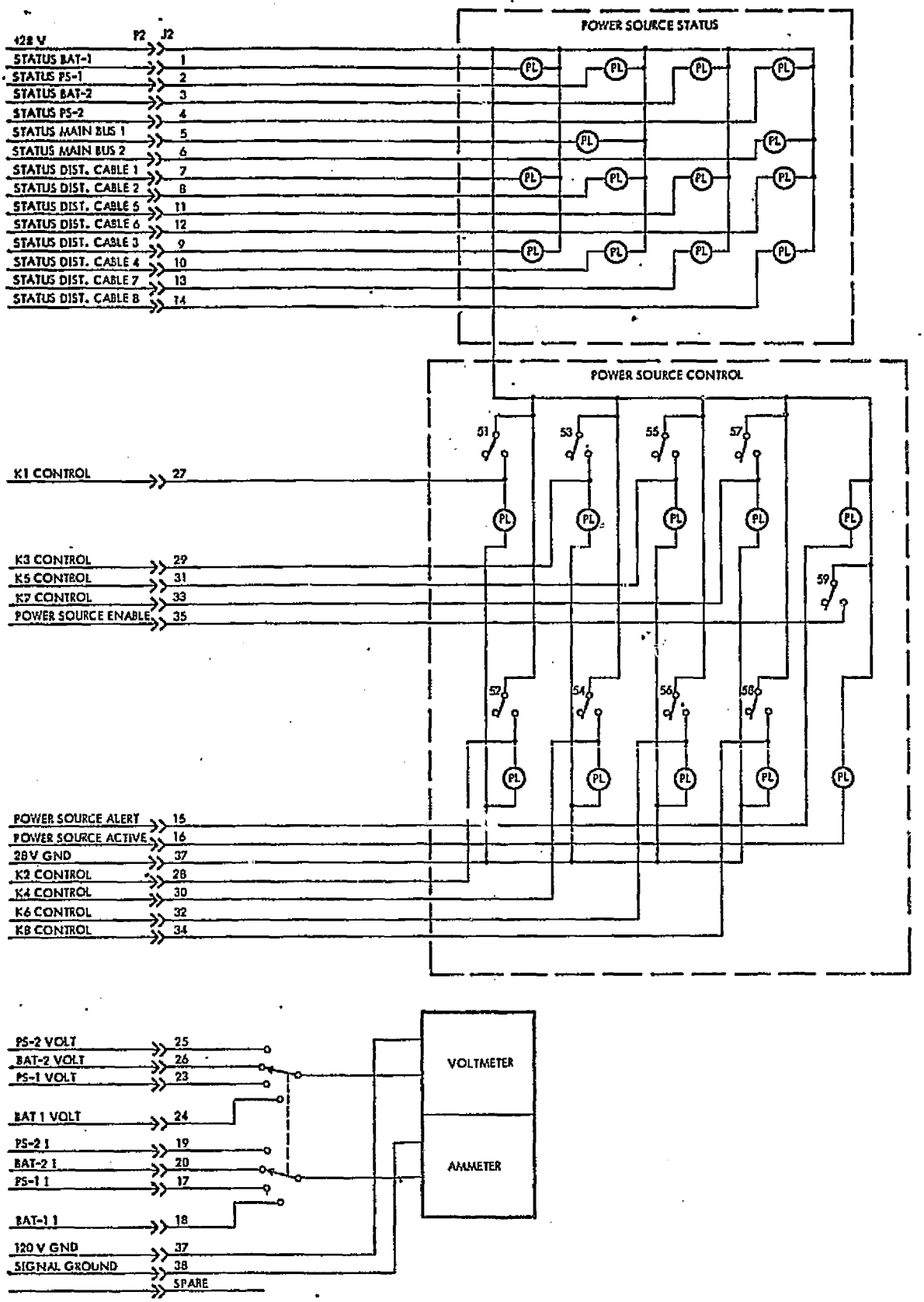



Figure 3.5.6-2. Supervision Monitor Unit Power Source Display and Control

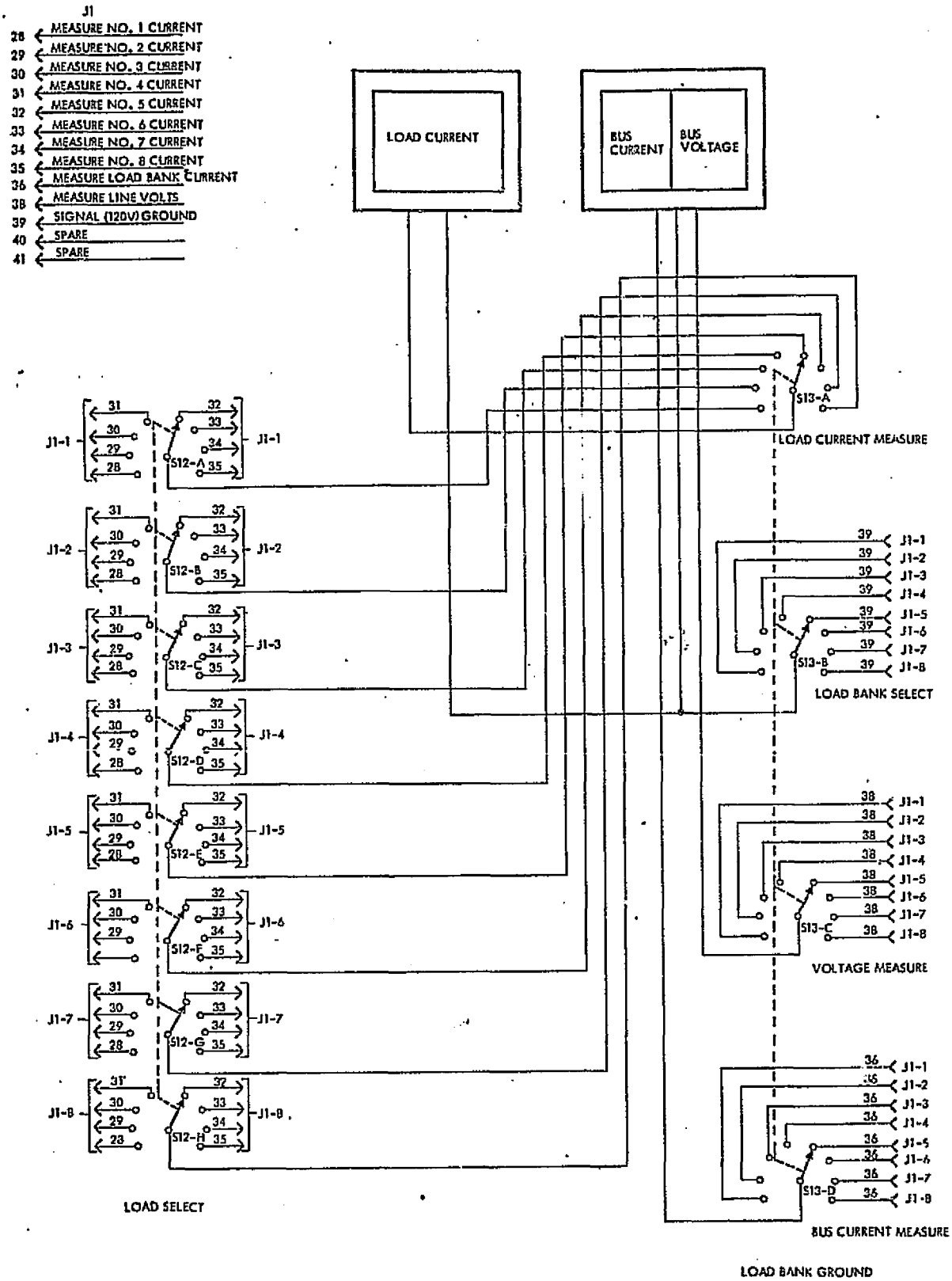



Figure 3.5.6-3. Supervision Monitor Unit Load Bank Analog Measurement Display

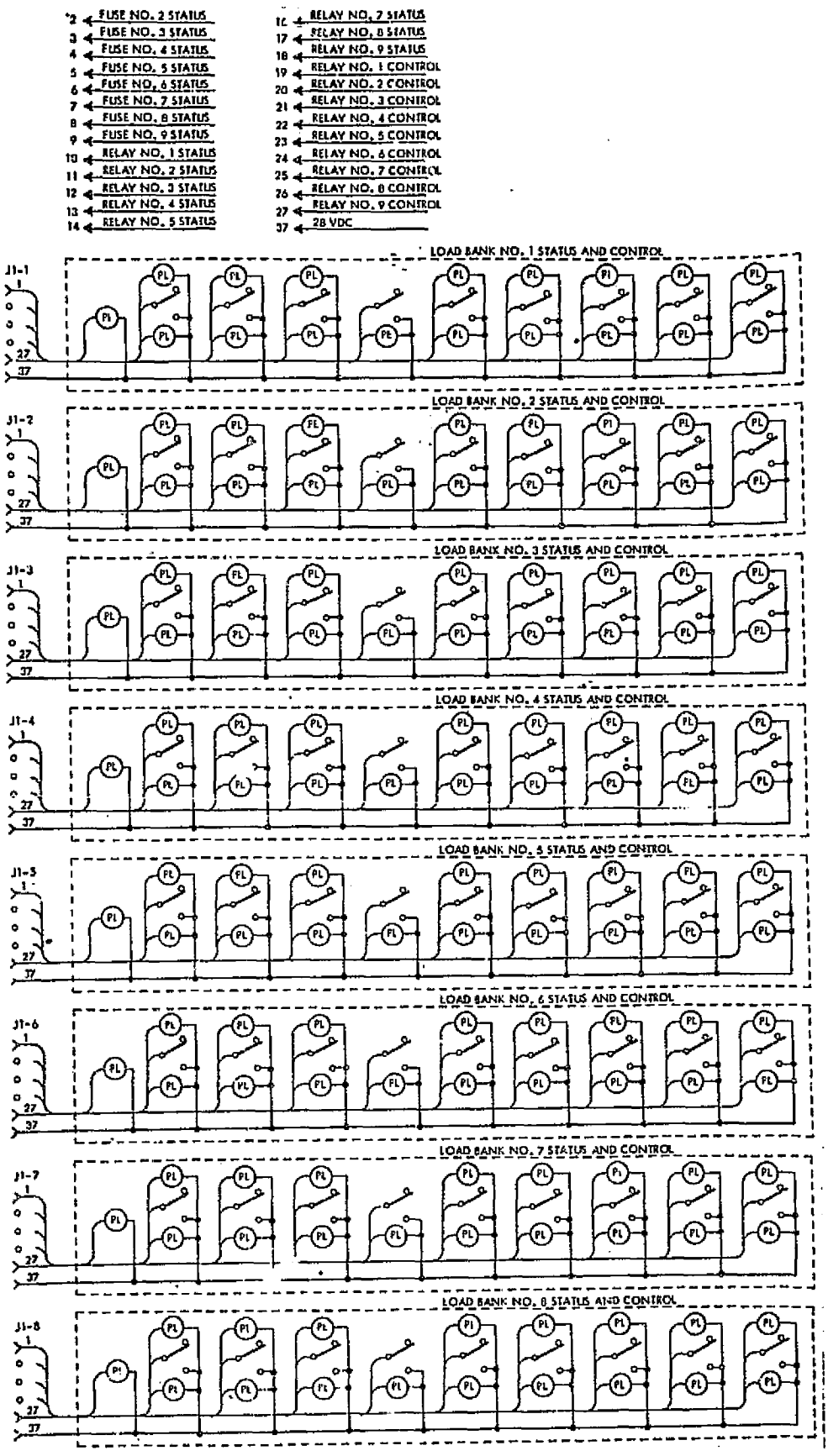



Figure 3.5.6-4. Supervision Monitor Unit Status and Control

### 3.5.6 Mobile Test Set

A number of tests requiring precise measurements were defined in Section 3.3 of the Phase 1 report. In order to obtain valid correlations between measurements obtained at different points in the Test Facility over a period of time, it is necessary to maintain rigorous control over test equipment parameters. A formal test control program involving frequent recalibration and measurement of all test equipment response against standards is not economically feasible for this study. Consequently, the recommended approach is to define test equipment configuration for each type of measurement and perform required calibrations on the assembled test set-up. Deviations of measurement parameters are avoided by mounting test components on a mobile equipment rack which may be moved to each test location without disturbing test equipment interfaces. These test set-ups should be maintained intact during a test series. Records of interconnecting test leads should identify connectors, test probes, test lead type and length. Records should include a unique serial number for each element of a test equipment assembly in the event that it is necessary to rerun measurements. Simple test equipment calibration approaches may be utilized and maintained in the Test Facility area if they are restricted to calibrations pertinent to the requirements of each test plan. For example an oil filled capacitor, a length of coaxial line and a current shunt can serve as a standard for all voltage and current transient measurements. All equipment will be initially calibrated by standard procedures and photographic records of response to the test facility standard will be maintained. The physical configuration and electrical parameters of any such test standard should be maintained invariant by rigid mountings, secured harnessing and electrostatic shielding. Selection of test equipment, standards and specific testing procedures must be deferred until the availability of equipment and personnel at MSFC can be established. Recommendations for test equipment configurations were defined in the Phase 1 report and are restated in the subsequent paragraphs.

### 3.5.7 Test Instrumentation

A tentative list of equipment to implement the tests described in the preceding sections is shown in Table 3.5.7-1.

Table 3.5.7-1. Test Instrumentation

| Quantity | Instrument | Comments |
|---|---|---|
| 1 | Impedance Bridge | HP4260A |
| 2 | Low Freq. Wave Analyzer | Fairchild EMC-10 |
| 2 | High Freq. Wave Analyzer | Fairchild EMC-25 |
| 3 | Oscilloscope | Tektronix 547 |
| 3 | Scope Camera | HP196A |
| 2 | Visicorders | Honeywell 1508 |
| 2 | Galvanometer Amplifiers | Honeywell T6A |
| 2 | Memory Voltmeters | Micro Instruments 5208, 5201C |
| 2 | DC Mullivoltmeter | Digital |
| 2 | AC Millivoltmeter | Digital |
| 1 | AF Signal Generator | As Available |
| 1 | RF Signal Generator | As available |
| 4 | Multimeters | As available |

In addition all normal accessories such as EMI antennas, current probes, oscilloscope plug-in amplifiers, and calibrated test leads used with the above will be required.

The test equipment listed above have been selected as representative models of the instruments required based on measurement needs and general availability. The quantities listed are considered minimum for maintaining the quality of the data base. This is not intended to restrict the use of other instruments which perform equally well. Since availability of equipment at MSFC will influence the final selection of test equipment, it is pertinent at this time to discuss the measurement requirements and instrument capabilities.

1. Impedance Bridge. The principle requirement is the capability of measuring reactances down to the values expected in the distribution cable. These values are not specified but are expected to fall in the vicinity of 0.3 microhenries and 10 picofarads per foot. The capability of the Hewlett Packard Model 4260 Universal Bridge is given in Table 3.5.7-2. Measurements are normally

performed with an internal 1 KHz oscillator but may be implemented with an external oscillator functioning between 20Hz and 20 KHz. It is desirable to perform the measurements over a wider range of frequencies since the above range is not sufficient to provide significant added value to the measurements at 1 KHz. If an instrument can be obtained at MSFC which can perform the impedance measurement at frequencies up to 50 MHz, the definition of the distributed parameters of the power distribution harness will be considerably improved.

Table 3.5.7-2. Specifications - Model 4260 HP Universal Bridge

**CAPACITANCE**

Range: 1 pF to 1000 μF, in 7 ranges.

Accuracy:

±(1% + 1 Digit), from 1 nF to 100 μF.

±(2% + 1 Digit), from 1 pF to 1 nF and 100 μF to 1000 μF.

Residual capacitance = 2 pF.

**INDUCTANCE**

Range: 1 H to 1000 H, in 7 ranges.

**ACCURACY**

±(1% + 1 Digit), from 1 mH to 100 H.

±(2% + 1 Digit), from 1 μH to 1 mH and 100 H to 1000 H.

Residual inductance ≤ 1 μH.

**DISSPATION FACTOR**

Range: Low D (series C): 0.001 to 0.12.
High D (parallel C): 0.05 to 50.

Accuracy (C greater than 100 pF):

Low D: ±(5% + 0.002) or one dial division, whichever is greater.

High D: ±(5% + 0.05) or one dial division, whichever is greater.

**QUALITY FACTOR**

Range: Low Q (series L): 0.02 to 20.
High Q (parallel L): 8 to 1000.

Accuracy (L greater than 100 μH):

Low Q: ±(5% + 0.05) or one dial division, whichever is greater.

High Q: ±(5% + 0.002) or one dial division, whichever is greater.

2. Wave Analyzers. The Fairchild EMC-10 and EMC-25 provide coverage from 20 Hz to 1.0 GHz, and are standard EMI measuring instruments. Any instruments capable of measurements to current specifications such as MIL-STD-461/462 are adequate for this function.

3. Memory Voltmeters and Visicorders. These instruments represent a practical method for monitoring of steady state and transient noise. Depending on the model, most visicorders are able to accommodate from 12 to 36 galvanometers which exceed the requirements of this program. The response of the visicorder galvanometer is flat down to pulse widths of approximately 40 microseconds (M-13000 galvanometer) which is adequate for measuring general transients and monitoring broadband noise as sensed by a wave analyzer. The effectiveness of the visicorder is considerably enhanced by operating in combination with a memory voltmeter. This instrument has a fast response (30-50 nanoseconds) and is either automatically or manually reset. The output is held by the memory voltmeter long enough (40 milliseconds) for the visicorder or other strip chart recording instrument to respond. For low energy signals, galvanometer power amplifiers are available to improve the data presentation. A typical configuration for simultaneous presentation of multiple signals is illustrated in Figure 3.4.7-1. The resulting data presentation is illustrated in Figure 3.5.7-2 (increasing time is from right to left). The general characteristics and capabilities of these instruments are summarized in Table 3.5.7-3.

4. Oscilloscope and Camera. The principle requirement for these instruments is the capability of photographing transient (single sweep) waveforms at sweep speeds up to one centimeter per microsecond. The spectrum of the transients to be observed is not known but it is estimated that signals with fundamental frequencies of 2.5 to 5.0 MHz will be generated on the 50 meter distribution cable due to echoes from the mismatched terminations. Noise due to contactor and fuse arcing will have lower energy density and broader spectrum than the cable resonance effects and will be measured by the broadband wave analyzer which has capability up to 1 GHz. All other significant noise effects on the cable then can be adequately observed with an oscilloscope with response up to 50 MHz. The characteristics of a Tektronix 547 oscilloscope with a 1A5 plug-in unit is:

| | |
|---|---|
| Deflection | 2 mv/cm to 20 v/cm |
| Bandwidth | DC to 45 MHz |
| Rise Time | 8 nanoseconds |

The Tektronix Model 544 and 546 oscilloscopes provide slightly better performance and any of these units would be acceptable. A dual beam oscilloscope would be quite advantageous for comparison of transients; however, the responses of dual beam oscilloscopes which have been reviewed do not appear to be adequate for the purposes of the test program.

5. Miscellaneous Instrumentation. Ammeters and voltmeters used should have scales and tolerances so that measurement accuracies approach 1%. Digital meters are far preferable where many measurements are to be performed. Due to the multiple ground systems in the test facility and the necessity for careful measurements, battery operated test equipment is preferred.

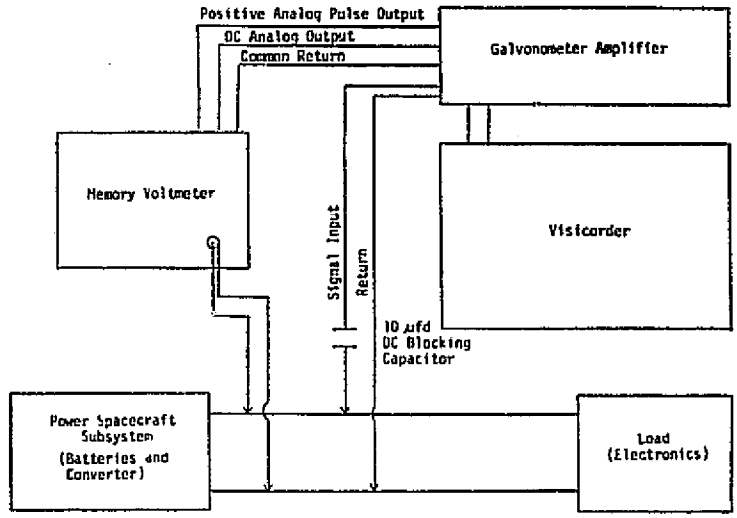



Figure 3.5.7-1. Transient Monitoring Test Setup

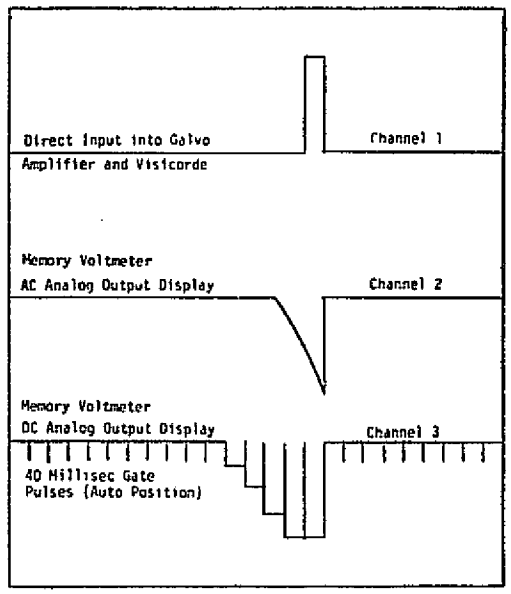



Figure 3.5.7-2. Typical Presentation of Pulse Displayed on Visicorder Using Direct Input and Memory Voltmeter Outputs

Table 3.5-7-3. Equipment Characteristics Memory Voltmeter (Micro Instrument Co. Model 5201C)

| | |
|---|---|
| Input Impedance | 30K ohms minimum (3.0V range) |
| Pulse Width Range | DC - 50 nano seconds |
| Accuracy | ±3% of full scale |
| Operating Modes | Reads peak positive |
| | Reads peak negative |
| | Reads peak positive or negative |

Outputs: DC analog 0-3.0 volts output on 3.0; 30.0; and 300 volt range 0-1.0 volts on 10 and 100 volt ranges. A 40 millisecond timing pulse is also present on this output.

AC Analog Output:

Simultaneous positive and negative outputs. 2.5 volt nominal, decay to zero in 100 μsec at full scale.

VISICORDER HONEYWELL MODEL 1508

| | |
|---|---|
| Speed Button | 1, 2, 4, 8 cps |
| Range Buttons (times speed button) | X.01; X1.0; X10 |
| Galvonometer Selection | Accepts all M series galvonometers |

GALVONOMETERS

| Model | Freq. Response | Maximum Pk-Pk Deflection | | Load Resistance Required |
|---|---|---|---|---|
| M-13000 | 0-13000 Hz | 2.0" | | 0 |
| M-8000 | 0-5000 Hz | 2.0" | | 0 |
| M-3300 | 0-2000 Hz | 8.0" | Series | 22 ohms |
| M-1650 | 0-1000 Hz | 8.0" | Series | 24 ohms |

GALVONOMETER AMPLIFIER HONEYWELL MODEL TG 6A-600

| | |
|---|---|
| Frequency Response | DC to 20,000 Hz |
| Input Impedance | 47K ohms |
| Input Voltage | 1.0 volt to ±50 volts |
| Output Impedance | 1 ohm DC -5000 Hz |
| Nominal 10 AD impedance | 37 ohms |
| Gain | 0 to Unity |
| DC Blocking Capacitor | 10 μfd for minimum distortion |

## 3.6 FILTERS AND ISOLATION CIRCUITS

The purpose in establishing EMI standards is to provide a basis for general design quality, and enable compatibility among equipments of different manufacture. It is inherent in the electrical design technologies that components can be designed to operate properly under almost any requirements. However, arbitrary specification of extreme requirements will increase weight, size and cost, and where additional equipment is required to meet unrealistic stress specifications, decrease reliability. Consequently, it is necessary that EMC standards be based on a balanced evaluation of the various aspects of the expected environment and be directed at a cost effective definition. Such a definition will be necessarily flexible to allow for environments containing significantly different equipment and performing dissimilar functions.

The HVDC Test Facility power distribution system is designed to simulate conditions on large space vehicles and aircraft. The power source and load simulator designs were primarily directed at space applications. Current EMC documents pertaining to these applications are listed below.

| | |
|---|---|
| MIL STD 461A | Electromagnetic Interference Characteristics For Equipment |
| MIL STD 462 | Measurement of Electromagnetic Interference Characteristics |
| MIL STD 704A | Characteristics And Utilization Of Aircraft Electric Power |
| MIL STD 704B | (Draft) |
| MIL STD 6181D | Interference Control Requirements, Aircraft Equipment |
| MIL STD 1541 | Electromagnetic Compatibility Requirements For Space Systems |
| AS-1212 | Characteristics and Utilization Of Electric Power, Aircraft |

The normal method to define an EMI specification is an iterative approach as illustrated by the functional flow diagram of Figure 3.6-1. Although the study may be initiated in any block, the most efficient starting point is the definition of susceptibility limits. Definition of the EMI limits in any functional block provide constraints for the next

block. The limits defined in each area form a hierarchy as shown in Figure 3.6-2. It should be noted that the three noise characteristics are plotted on the same chart in relative noise power only for the purpose of illustration. Conducted susceptibility requirements are normally shown in volts while emission characteristics are indicated by amperes; distribution system noise requirements are not usually specified. It should also be noted that specifications such as MIL-STD-461A are intended as guidelines rather than hardline constraints on all systems. Requirements for a specific system are negotiated by the procuring agency and the contractor during the initial phase of a contract. Generated interference as specified in MIL-STD-461A is illustrated in Figure 3.5-3 along with an example of the contractual requirement placed on a particular power converter. The details of the EMC plan design approach as presented in Figure 3.6-1 are shown in the flow diagram of Figure 3.6-4. The functions identified in the majority of the blocks may be implemented on the basis of available data and previous experience unless the problem under consideration involves new classes of equipment or more stringent program requirements. With respect to the HVDC Test Facility, the significant difference is the increased distribution voltage and the associated decreased line current.

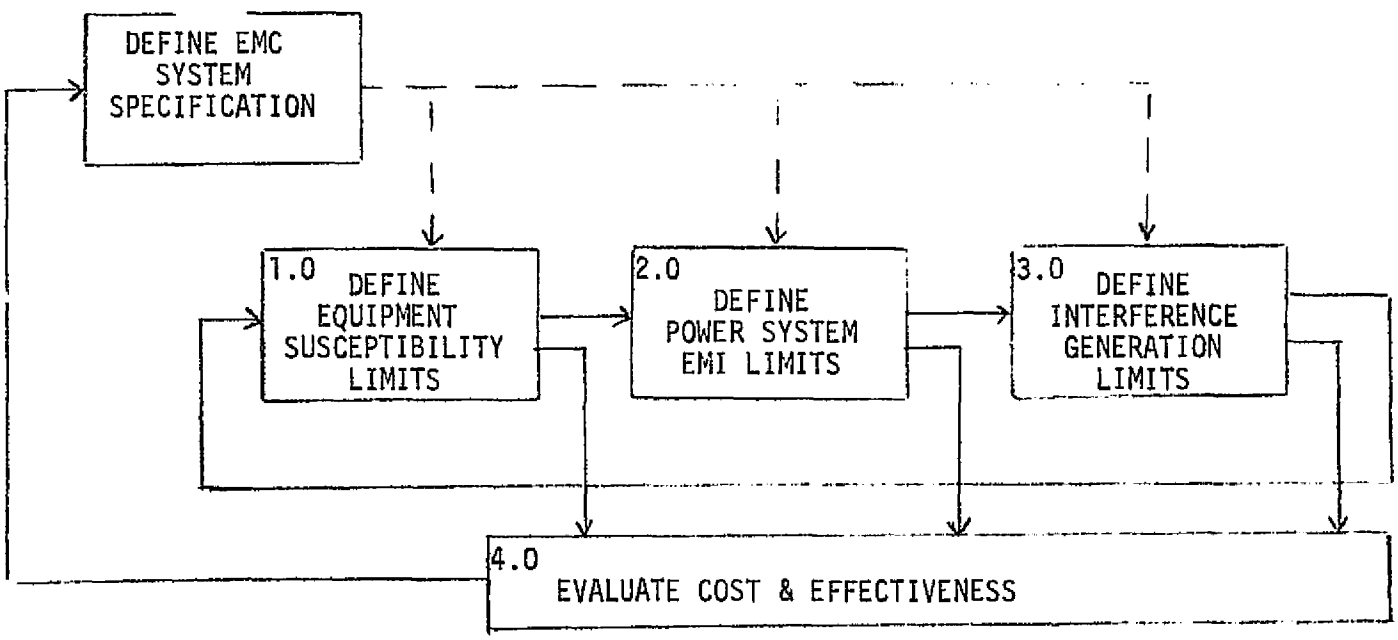



Figure 3.6-1. EMC Plan Definition

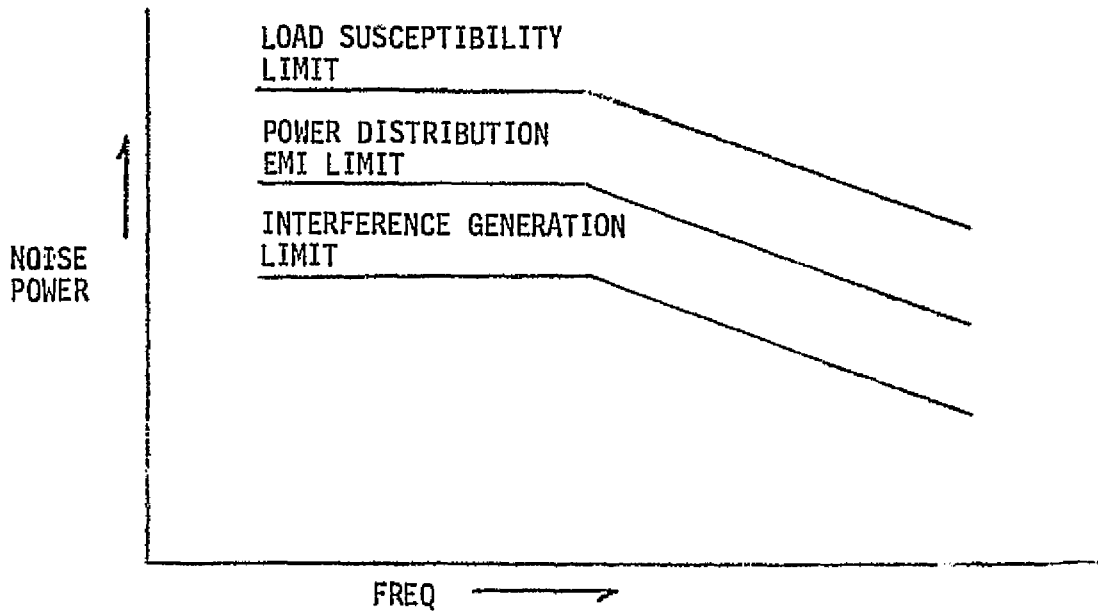



Figure 3.6-2. Relative Noise Limits

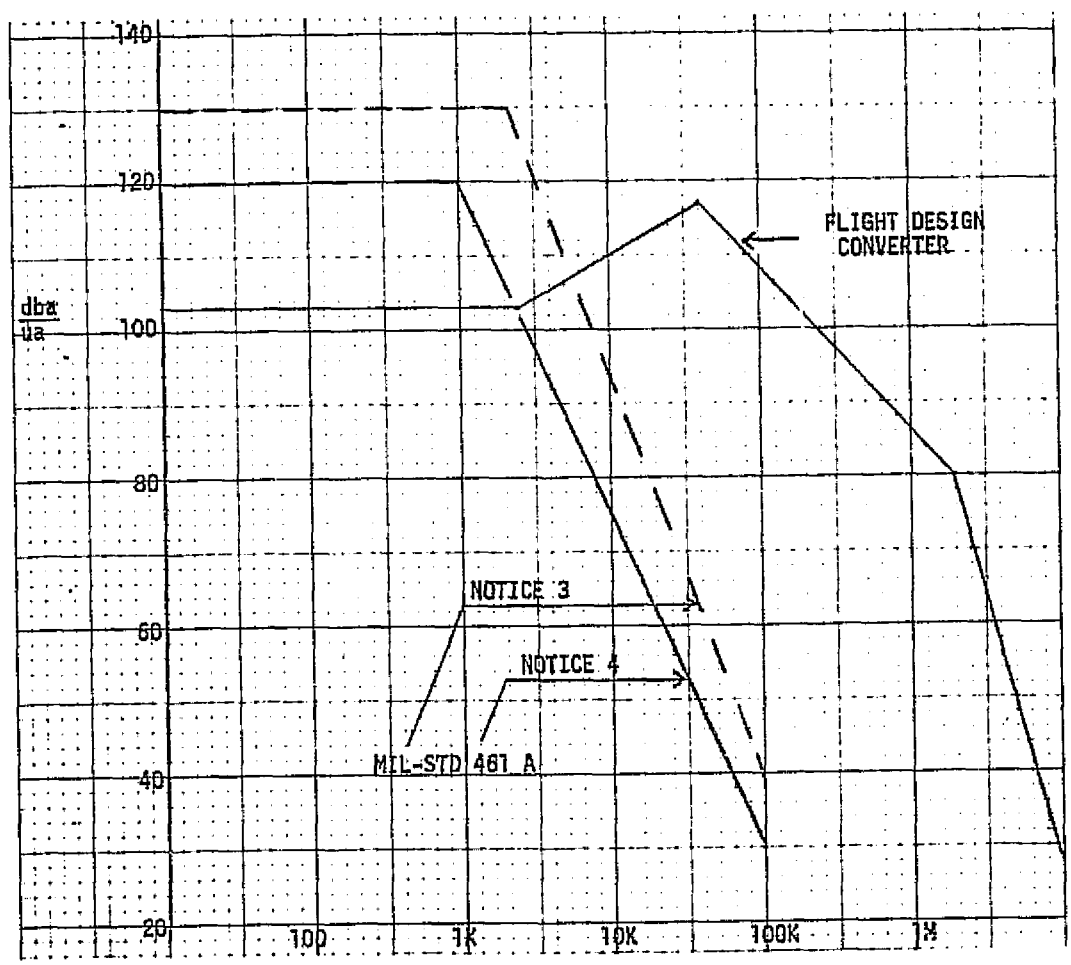



Figure 3.6-3. Narrow Band Noise

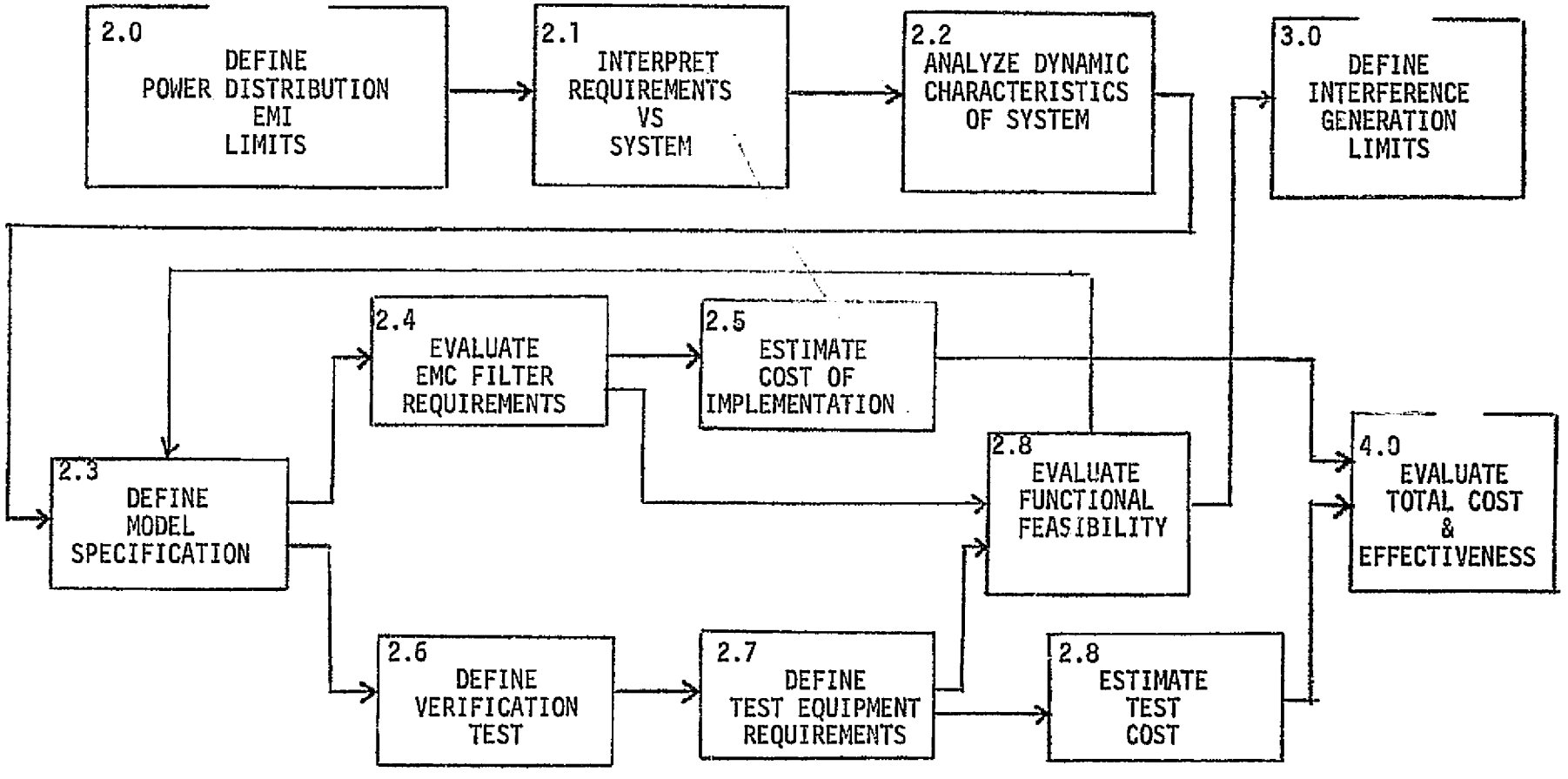



Figure 3.6-4. EMC Definition Detail

### 3.6.1 Steady-State Conducted Emission Baseline

The specification of steady-state noise requires knowledge of the power distribution configuration and the sensitivity of the loads for a particular program. Since this data is not specified in this study, the evaluation of permissible steady-state narrow band noise will be based on MIL-STD-461A susceptibility standards. The narrow band noise limits of CS01 are presented in Figure 3.6-5. The low frequency limits are specified as 10% of the line voltage or 3.0 volts RMS, whichever is less.

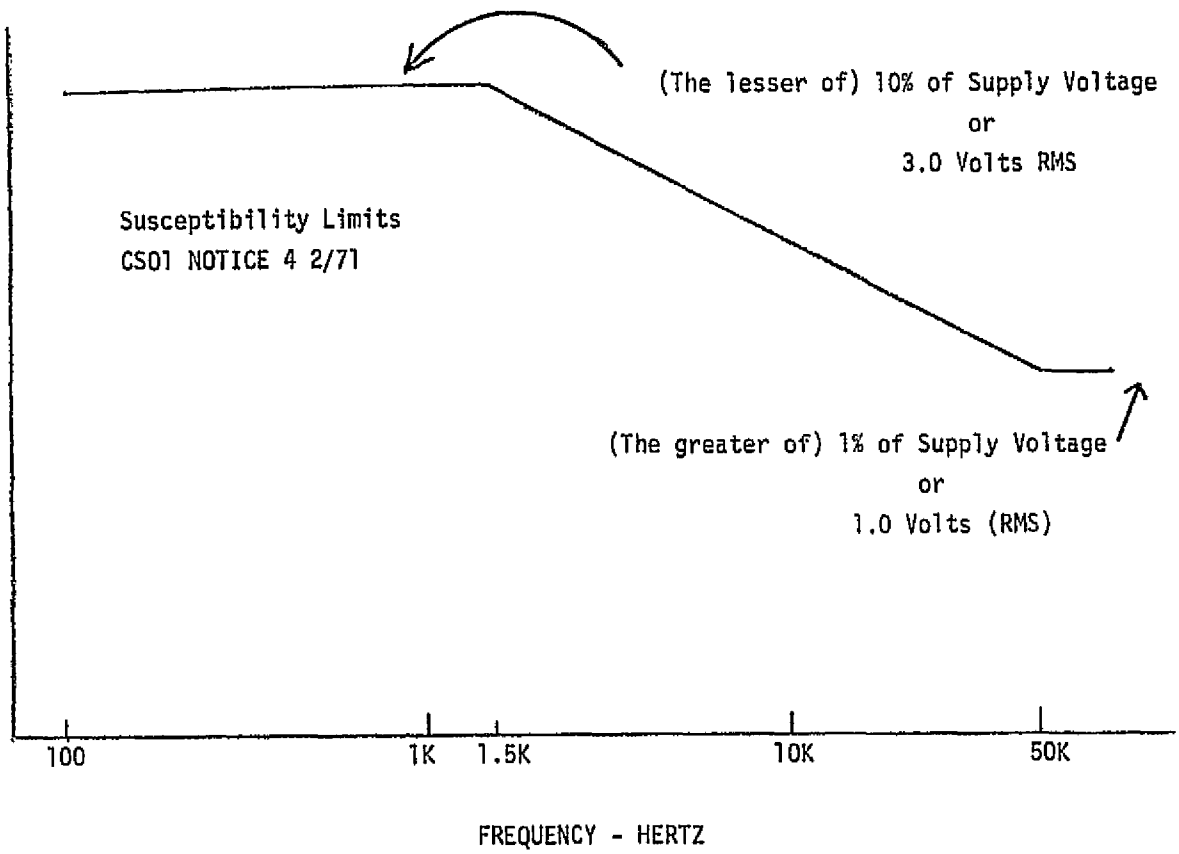



Figure 3.6-5. Load Terminal Voltage Susceptibility Requirements

The generation of this noise in small space vehicles is due to power source noise and interactions between emitted noise currents and power source impedance. In the large space vehicle under consideration, the fuel cell power source does not generate ripple currents and has very low output impedance. Line noise is generated primarily by interactions between

the power distribution harness and emitted noise currents. If it is considered that a maximum line drop of 5% occurred at 120 VDC the following calculation may be made.

$$\Delta E \text{ (Line)} = 0.01 \text{ (120)} = 7.0 \text{ volts} = I \text{ (Line)} R \text{ (Line)}$$
$$E \text{ (Max Ripple)} = 3.0 \text{ volts} = I \text{ (Ripple)} R \text{ (Line)}$$
$$I \text{ (Ripple)} \times 100/I \text{ (Line)} = 43\%$$

This is in excess of the ripple generated by space qualified equipment and does not provide a realistic low frequency emitted noise limit. Consequently, for this evaluation, the emitted noise limits will be based on the following guidelines.

1) Conducted narrow band emission, for any component, shall not exceed 10% of its nominal load current.

2) The conducted narrow band emission current shall not produce a voltage greater than a value 6db below the CSO1 profile (MIL-STD-461A) when injected into the load terminals of the power distribution harness.

Since noise does not add linearly, a load consisting of several components would have a less severe requirement than a load consisting of one component. Therefore, it will be assumed for the purposes of comparison that all the line current is supplied to one component.

3.6.1.1 Power Distribution System Characteristics

The initial system to be analyzed is defined below:

Conductors - #8 Nickel Plated Twisted Pair (MSFC Specification)
Length - 50 Meters
Current - 20A
Voltage - 120, 56, 28 VDC

The physical characteristics of the cable are defined in MSFC Specification 40M39513 (General Specification For Electrical Hook Up Wire). It should be noted that #8 conductor in this specification contains approximately 3% more cross-sectional area than the standard AWG #8 wire.

The effect of the nickel coating on the electrical and transmission parameters is negligible at low frequencies (<100 Hz) compared to silver plated or bare conductor. At higher frequencies, the effect of the nickel is to increase inductance and skin resistance. This is regarded as advantageous in power system design. A general analysis of the transmission parameters has been performed and automated and is presented in Appendix A. The program output for a shorted 50 meter pair is illustrated in Table 3.6-1. Column 4 lists the impedance of this cable at the load terminals as a function of frequency. The impedance of the power source was assumed zero for the purpose of generality. The inclusion of a fuel cell source (0.015-0.03 ohms) or a large capacitor at the power source output has negligible effect on the calculation.

Table 3.6-1. #8 Nickel Coated Wire

| Frequency Hertz | Attenuation Nepers | Phase Shift Degrees | Load Terminal Impedance ohms | Phase Degrees |
|---|---|---|---|---|
| F(W) | ALPHA | BETA | Z | THETA |
| 10 | .112E-03 | .113E-03 | .197E+00 | .576E+00 |
| 15.8 | .14E-03 | .143E-03 | .197E+00 | .913E+00 |
| 25.1 | .176E-03 | .181E-03 | .197E+00 | 1.45 |
| 39.8 | .22E-03 | .229E-03 | .197E+00 | 2.29 |
| 63.1 | .274E-03 | .292E-03 | .197E+00 | 3.63 |
| 100 | .338E-03 | .374E-03 | .198E+00 | 5.74 |
| 158 | .414E-03 | .485E-03 | .2E+00 | 9.04 |
| 251 | .499E-03 | .64E-03 | .204E+00 | 14.1 |
| 398 | .589E-03 | .866E-03 | .214E+00 | 21.5 |
| 631 | .68E-03 | .121E-02 | .238E+00 | 31.4 |
| .1E+04 | .769E-03 | .218E-02 | .414E+00 | 51.1 |
| .158E+04 | .107E-02 | .318E-02 | .553E+00 | 52.7 |
| .251E+04 | .15E-02 | .468E-02 | .748E+00 | 54.4 |
| .398E+04 | .21E-02 | .693E-02 | 1.02 | 56.3 |
| .631E+04 | .293E-02 | .103E-01 | 1.42 | 58.3 |
| .1E+05 | .411E-02 | .155E-01 | 2 | 60.4 |
| .158E+05 | .577E-02 | .235E-01 | 2.86 | 62.4 |
| .251E+05 | .814E-02 | .357E-01 | 4.15 | 64.3 |
| .398E+05 | .115E-01 | .546E-01 | 6.09 | 66.1 |
| .631E+05 | .165E-01 | .841E-01 | 9.06 | 67.8 |
| .1E+06 | .237E-01 | .13E+00 | 13.7 | 69.2 |

The method utilized to determine permissible emitted noise is illustrated in Figure 3.6-6. Curve A and B (CS01, 120V line) determine the voltage noise limit at the load terminals. Curve F is the cable impedance at the load terminals. Allowable noise signals are limited to 10% (2A) of line current at low frequencies. The resulting noise voltages are plotted by Curve E. This voltage rises with increasing frequency at approximately 13.9 db/decade and intersects Curve B (descending at 13.3 db/decade) at 5 KHz. Since Curve B is the assumed limit derived from CS01, the permissible noise current descends at 27.2 db/decade until it reaches 50 KHz. At 50 KHz the CS01 characteristic returns to zero db/decade; the current characteristic continues to descend at 13.9 db/decade. The current characteristic C(120) illustrates the maximum noise limits for the 120 VDC, 20A load.

A similar characteristic for 28 VDC line is obtained by substituting Curve D for Curve B in this process. Curve D is obtained by displacing Curve B -12.6 db. The intersection of E at D (point 2) occurs at 1.8 KHz. The resulting noise current limit is illustrated by C(28). Below 1.8 KHz, C(120) and C(28) are identical. The results for 120, 56 and 28 VDC are plotted in Figure 3.6-7 together with MIL-STD-461A, Notice 3 and 4 limits.

A similar calculation may be performed assuming a 100A load. The cable for this configuration consists of five twisted pairs of #8 wire. There is no accurate analysis at this time for transmission parameters at higher frequencies for a power cable bundle. Skin resistance and inductance is a function of the distribution of conductors in the harness. A reasonable assumption which has been applied in these circumstances is provided below:

$N$ = Number of pairs in harness

$Z_H(N)$ = High frequency impedance of cable

$Z_L(N)$ = Low frequency impedance of cable

$Z_L(N) = Z_L(1)/N$

$Z_H(N) = Z_H(1)/\sqrt{N}$

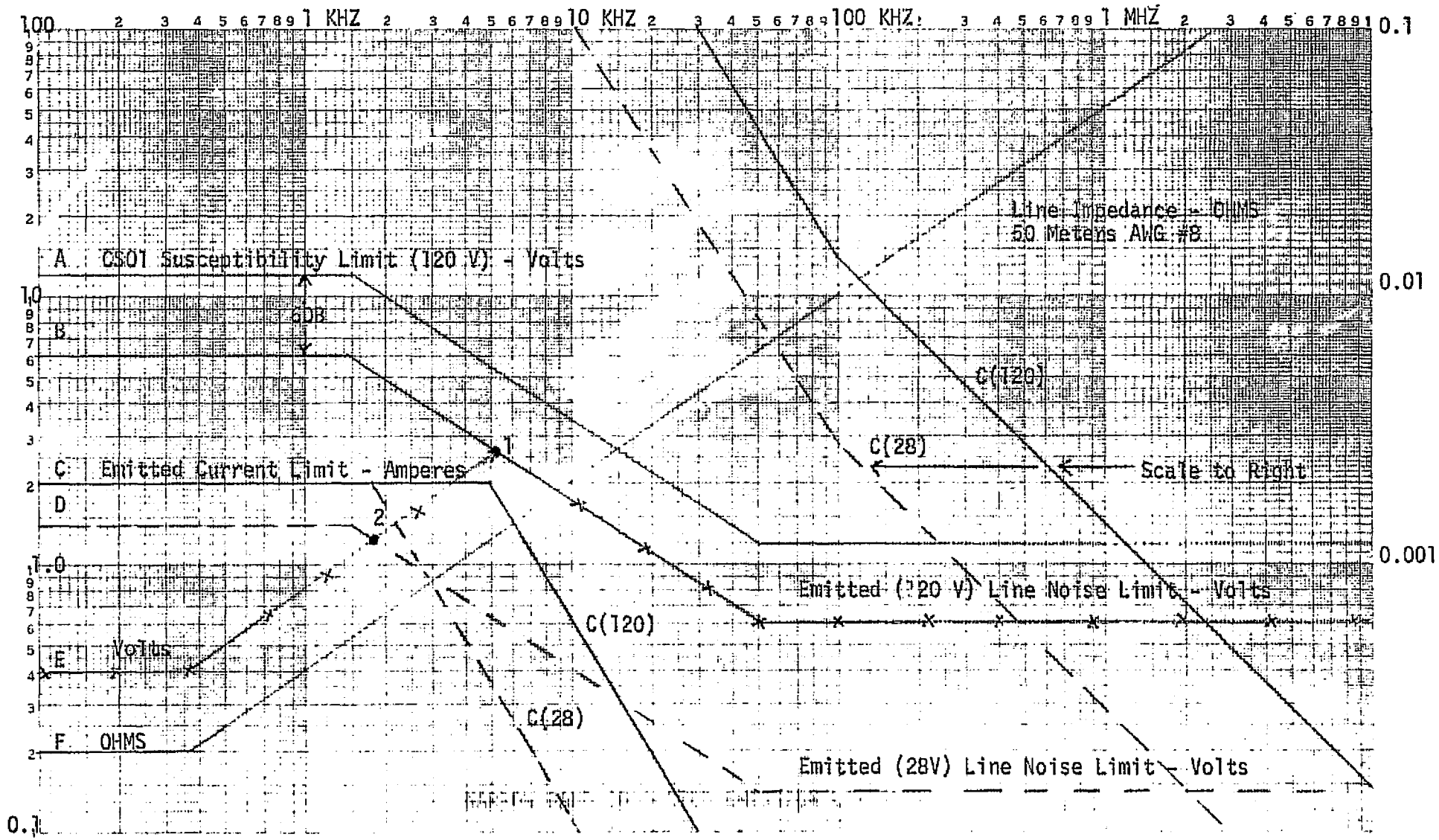



Figure 3.6-6. Narrow Band Conducted Emission Limits

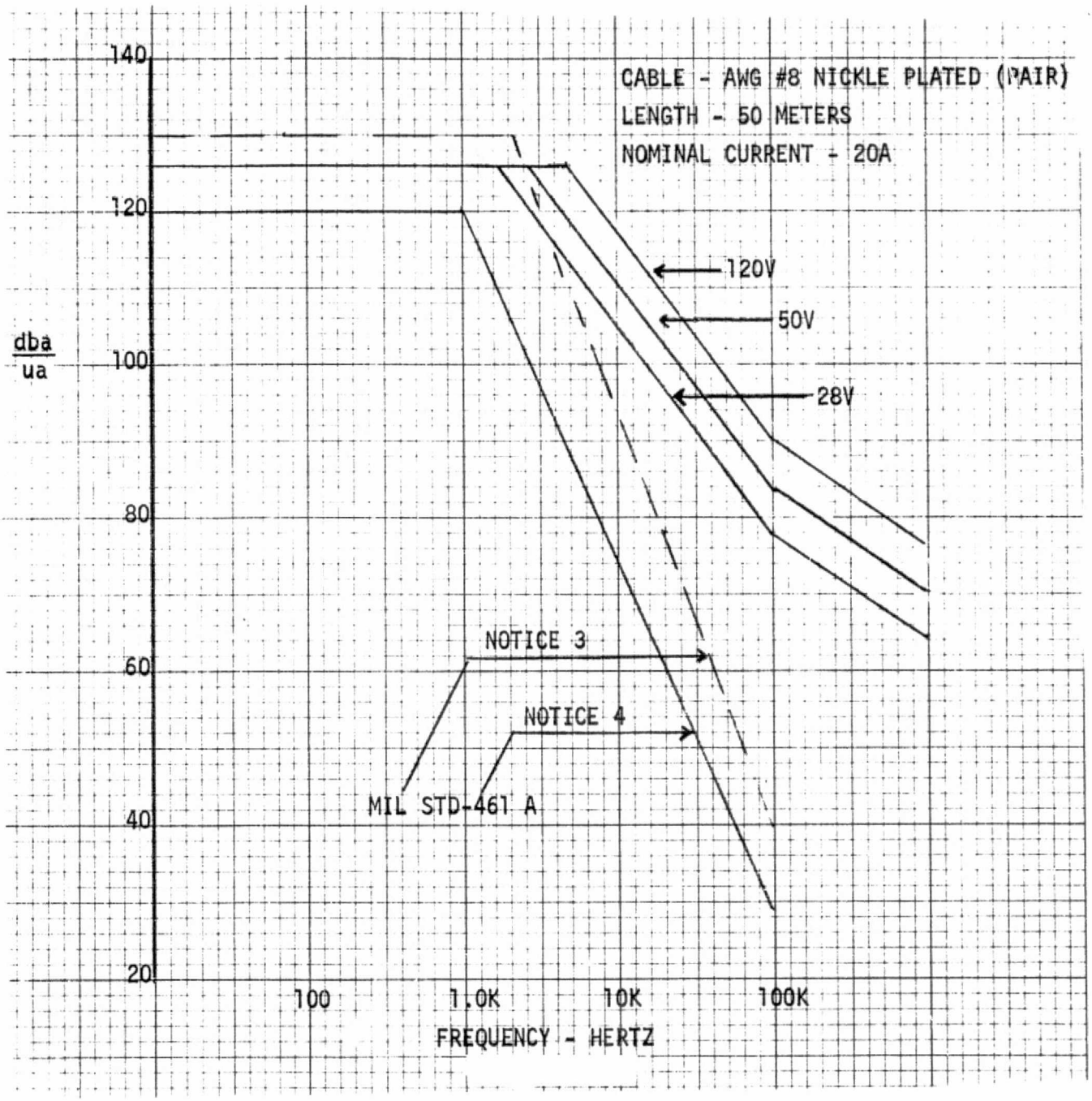



Figure 3.6-7. Narrow Band Noise Limits vs Line Voltage

Using these assumptions the previous calculation was repeated for 100 ampere loads. The results are shown in Figure 3.6-8. The additional step shown in the 28V case is due to the fact that generated noise intersected the noise limit profile (CSO1) prior to the first corner (1.5 KHz) of that characteristic.

3.6.1.2 Constant Power Comparison

The previous calculations serve the purposes of general comparisons of the effect of line voltage on conducted noise limitations. A less general but more informative point design for nominal 500 watt loads at 28 and 120 VDC provides a more definitive comparison. For this study the 5% maximum line drop was used to size the cable with the following results.

Case #1
P = 500 watts
E = 120 volts
I = 4.17 amperes
Conductor = #14 Nickel Plated Twisted Pair

Case #2
P = 500 watts
E = 28 volts
I = 17.86 amperes
Conductor = #4 Nickel Plated Twisted Pair

The cable parameters derived from the programmed analysis are illustrated in Tables 3.6-2 and 3.6-3. Calculations of allowable noise were performed as previously and the results are illustrated in Figure 3.6-9a. The presentation of the data in Figure 3.6-9a does not provide an effective comparison of the EMI filtering required in each case. If it is assumed that the loads at each line voltage perform equivalent functions, the spectral distribution of generated noise currents will have similar profiles with amplitudes proportional to the nominal line current. The significant criteria on which to base EMI filtering requirements is the ratio of the narrow band conducted interference limit to the nominal line current.

These characteristics are plotted in Figure 3.6-9b. The analysis indicates that the 120V line requires less filtering than the 28V line at frequencies above 2.8 KHz. At frequencies above 12 KHz, the 120V line requires 17.2 db less filtering than the 28V line.

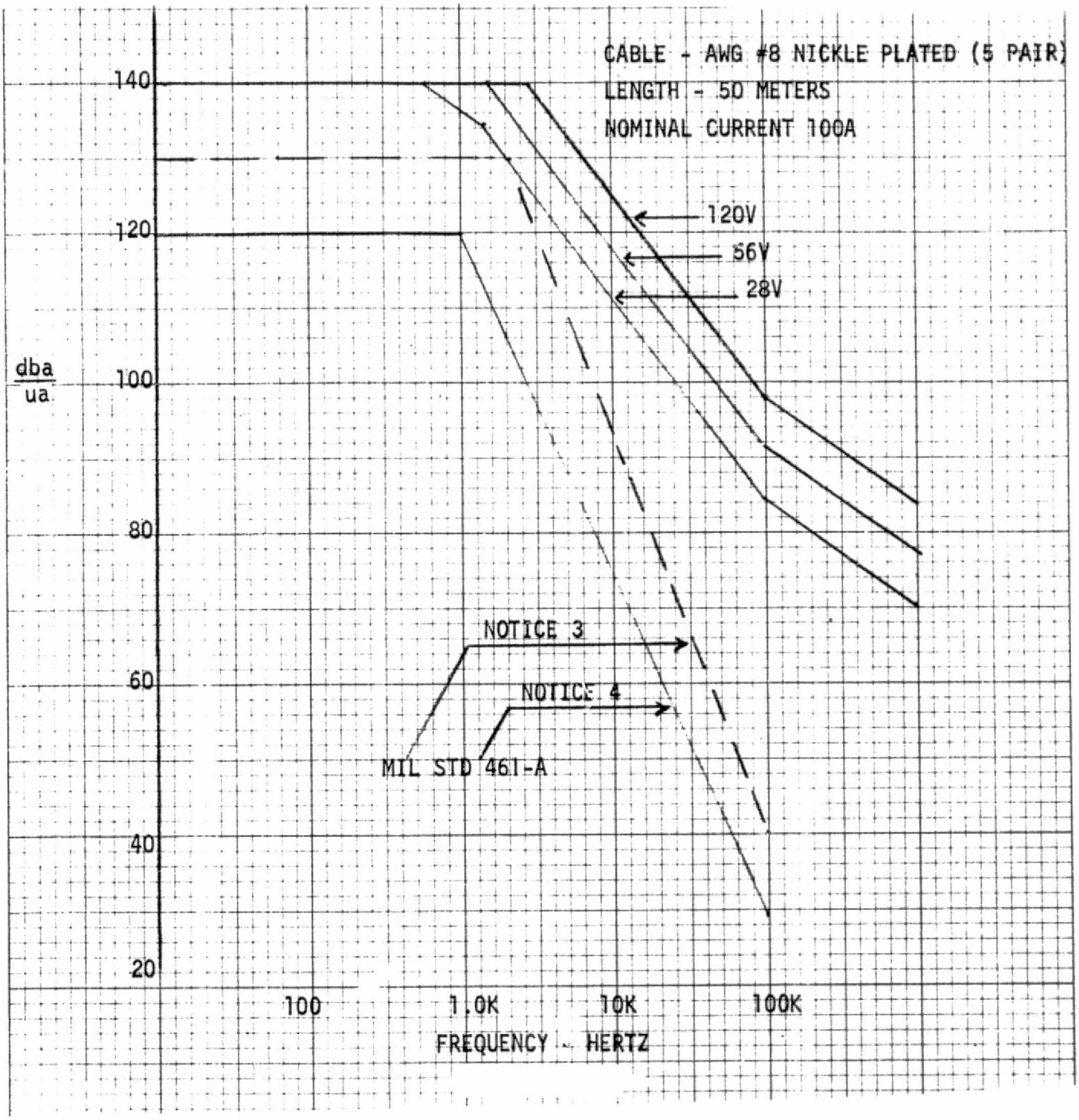



Figure 3.6-8. Narrow Band Noise Limits vs Line Voltage

Table 3.6-2. #4 Nickel Coated Wire

| Frequency Hertz | Attenuation Nepers | Phase Shift Degrees | Load Terminal Impedance ohms | Phase Degrees |
|---|---|---|---|---|
| F(W) | ALPHA | BETA | Z | THETA |
| 10 | .79E-04 | .806E-04 | .789E-01 | 1.09 |
| 15.8 | .99E-04 | .102E-03 | .79E-01 | 1.73 |
| 25.1 | .124E-03 | .13E-03 | .79E-01 | 2.74 |
| 39.8 | .153E-03 | .165E-03 | .792E-01 | 4.33 |
| 63.1 | .189E-03 | .213E-03 | .796E-01 | 6.84 |
| 100 | .23E-03 | .278E-03 | .806E-01 | 10.7 |
| 158 | .275E-03 | .369E-03 | .83E-01 | 16.6 |
| 251 | .251E-03 | .66E-03 | .123E+00 | 48.3 |
| 398 | .352E-03 | .954E-03 | .161E+00 | 49.5 |
| 631 | .492E-03 | .139E-02 | .213E+00 | 50.9 |
| .1E+04 | .687E-03 | .203E-02 | .283E+00 | 52.5 |
| .158E+04 | .959E-03 | .298E-02 | .382E+00 | 54.3 |
| .251E+04 | .134E-02 | .44E-02 | .522E+00 | 56.2 |
| .398E+04 | .187E-02 | .656E-02 | .723E+00 | 58.2 |
| .631E+04 | .261E-02 | .983E-02 | 1.02 | 60.2 |
| .1E+05 | .366E-02 | .148E-01 | 1.45 | 62.3 |
| .158E+05 | .515E-02 | .226E-01 | 2.09 | 64.3 |
| .251E+05 | .728E-02 | .345E-01 | 3.07 | 66.2 |
| .398E+05 | .104E-01 | .53E-01 | 4.55 | 67.9 |
| .631E+05 | .149E-01 | .819E-01 | 6.83 | 69.4 |
| .1E+06 | .215E-01 | .127E+00 | 10.4 | 70.7 |

Table 3.6-3. #14 Nickel Coated Wire

| Frequency Hertz | Attenuation Nepers | Phase Shift Degrees | Load Terminal Impedance ohms | Phase Degrees |
|---|---|---|---|---|
| F(W) | ALPHA | BETA | Z | THETA |
| 10 | .206E-03 | .206E-03 | .873E+00 | .163E+00 |
| 15.8 | .259E-03 | .26E-03 | .873E+00 | .258E+00 |
| 25.1 | .325E-03 | .328E-03 | .874E+00 | .409E+00 |
| 39.8 | .409E-03 | .413E-03 | .874E+00 | .649E+00 |
| 63.1 | .513E-03 | .522E-03 | .874E+00 | 1.03 |
| 100 | .642E-03 | .661E-03 | .874E+00 | 1.63 |
| 158 | .802E-03 | .839E-03 | .874E+00 | 2.58 |
| 251 | .996E-03 | .107E-02 | .876E+00 | 4.09 |
| 398 | .123E-02 | .138E-02 | .88E+00 | 6.46 |
| 631 | .15E-02 | .179E-02 | .889E+00 | 10.2 |
| .1E+04 | .179E-02 | .237E-02 | .912E+00 | 15.8 |
| .158E+04 | .21E-02 | .323E-02 | .967E+00 | 24 |
| .251E+04 | .239E-02 | .457E-02 | 1.09 | 34.7 |
| .398E+04 | .256E-02 | .772E-02 | 1.71 | 53.3 |
| .631E+04 | .362E-02 | .115E-01 | 2.35 | 55 |
| .1E+05 | .512E-02 | .171E-01 | 3.28 | 56.7 |
| .158E+05 | .727E-02 | .257E-01 | 4.64 | 58.4 |
| .251E+05 | .104E-01 | .389E-01 | 6.65 | 60.1 |
| .398E+05 | .149E-01 | .593E-01 | 9.68 | 61.7 |
| .631E+05 | .215E-01 | .908E-01 | 14.3 | 63.2 |
| .1E+06 | .314E-01 | .14E+00 | 21.3 | 64.6 |

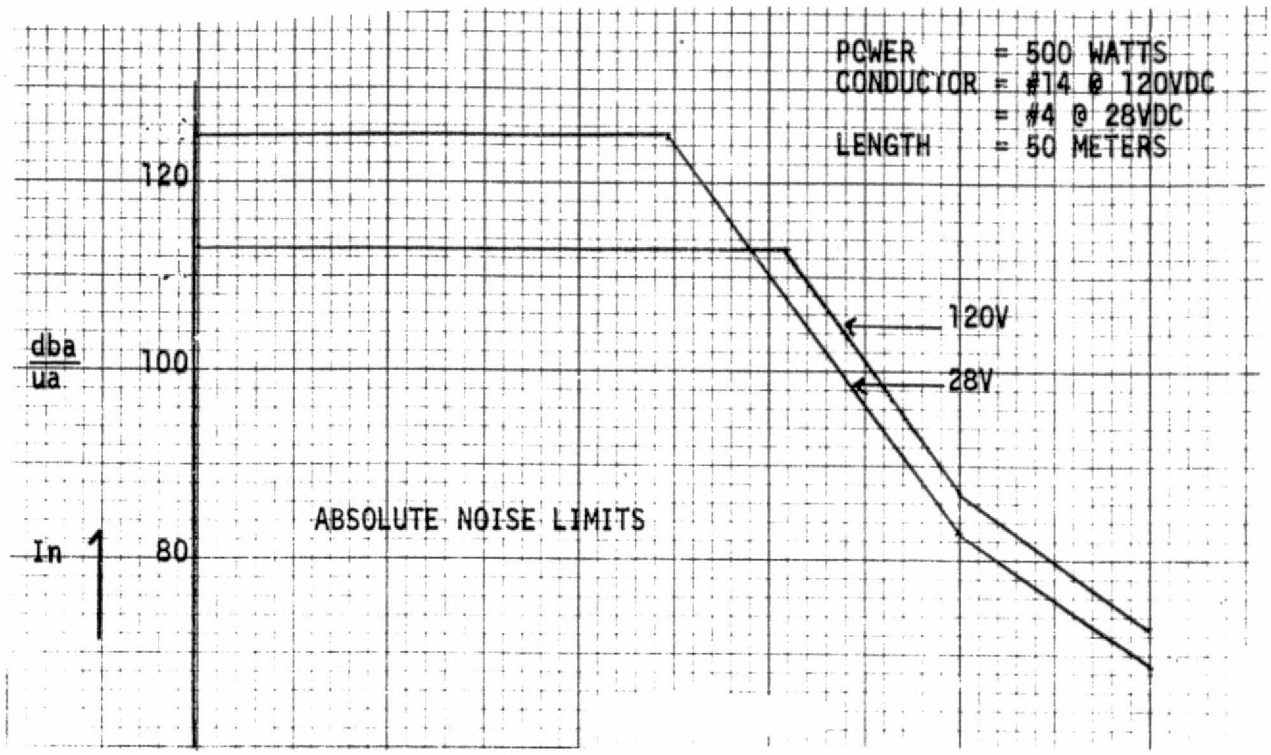



Figure 3.6-9a. Narrow Band Noise Limits at 500 Watts

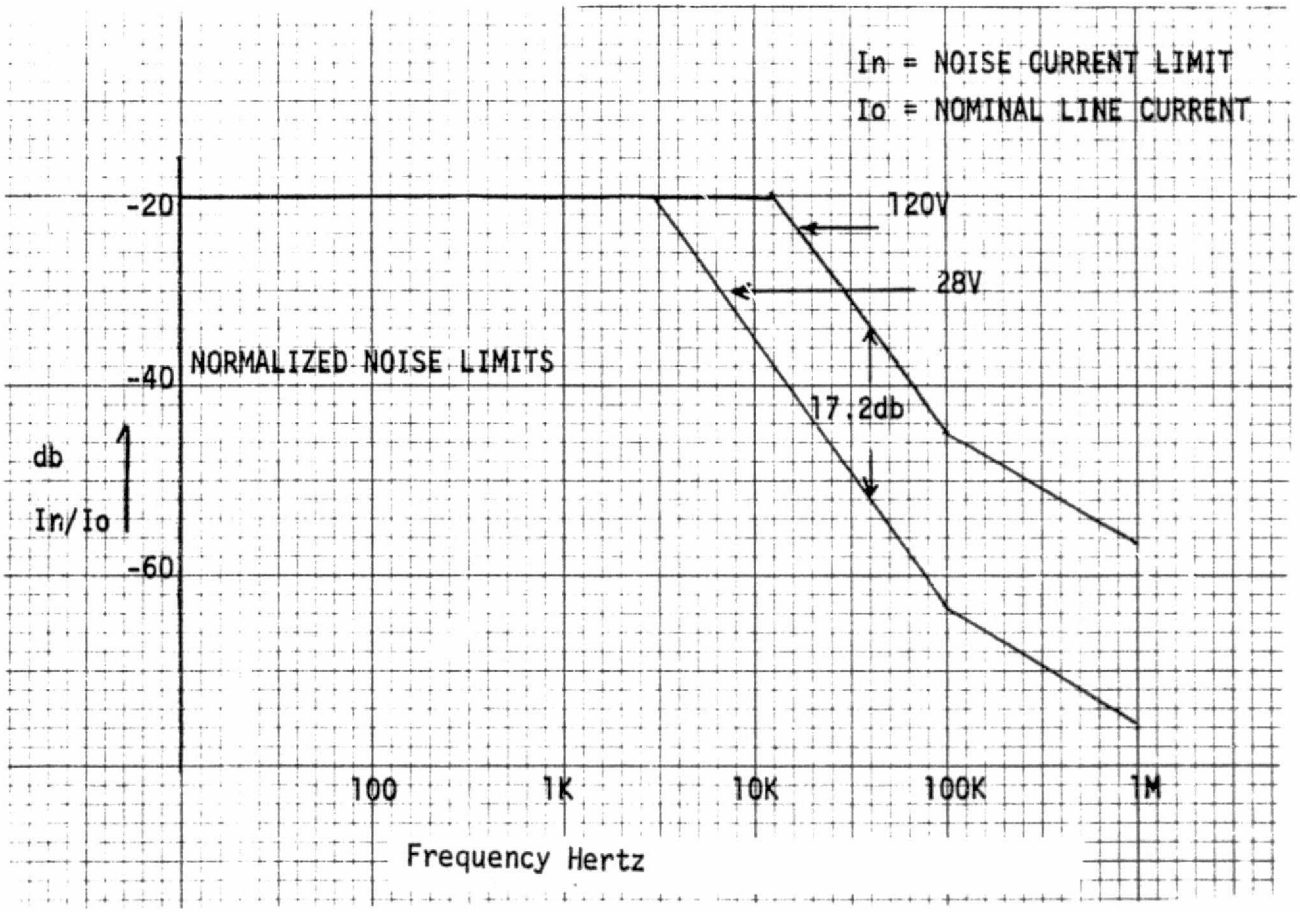



Figure 3.6-9b. Narrow Band Noise Limits at 500 Watts

### 3.6.1.3 Narrow Band Noise - Summary

An analysis of narrow band generated interference limits based on MIL-STD-461A, CS01 susceptibility limits has shown a significant advantage for 120V DC line voltage for equal power loads. The analysis assumed some system peculiar parameters which have significant bearing on the results. These assumptions included the method for selecting cable size (5% nominal line drop), 50 meter cable length and equivalent loads. Revising the cable parameters does not change the trends indicated but will influence the magnitudes of the variables calculated to some small degree. The assumption of equivalent loads included identical frequencies. It is unlikely that this would occur in an actual design, since the different currents and voltages for the 120 and 28 volt configuration would indicate the use of different solid state devices with dissimilar capabilities. However, it is not expected that the optimization of the load design will result in a significant modification of the preceding results.

### 3.6.2 Conducted Transients

Conducted transients occur in power lines due to switching events. In general, there are two types of transients.

1) The primary switching event due to abrupt change in the average line current.
2) Secondary effects due to relay arcing, transformer saturation, etc.

### 3.6.2.1 Primary Switching Effects

The need for control of line surges varies with the application. However, in large systems some constraints are desirable to provide reasonable guidelines for contractors. The recommended voltage limits under surge conditions are derived from MIL-STD-704B, paragraph 5.2.2.4 and Figure 3.6-6 of that document. Ordinate values were changed to percent of line voltage to be compatible with the variable line voltage capability in the HVDC test facility. Maximum voltage-time limits are illustrated in Figure 3.6-10. The rate of rise and fall of current transients should be restricted to those values which, when reacting with the

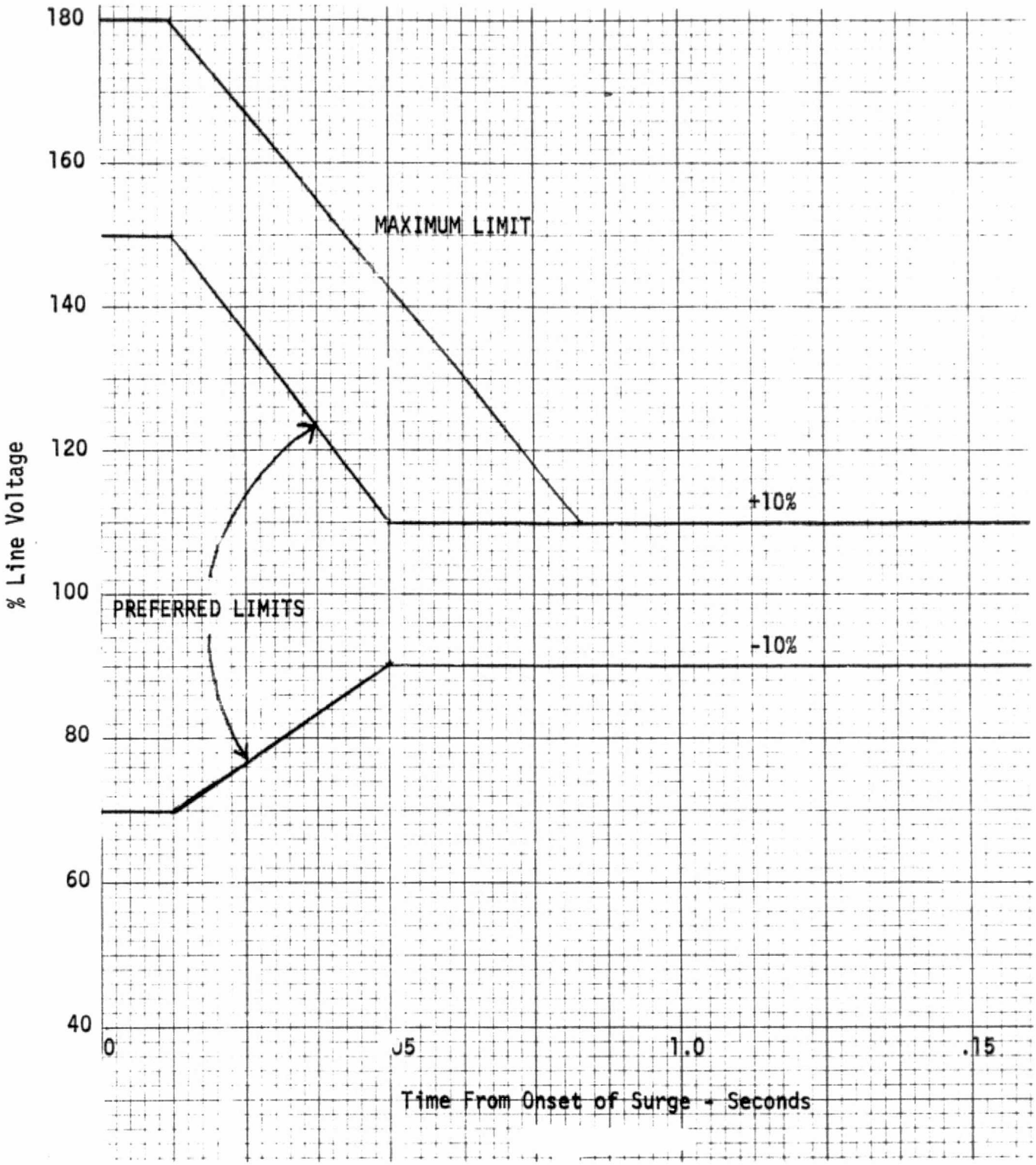



Figure 3.6-10. Envelope of DC Voltage Surge

power distribution harness, do not develop transient voltages in excess of the envelope of Figure 3.6-10. This is a function of the electrical length of the harness and must be calculated for each case.

### 3.6.2.2 Secondary Switching Effects

Secondary switching effects are characterized by isolated high impulses or bursts of high frequency EMI. Although most subsystems provide filters with cut-off frequencies well below the noise spectrum of these signals, stray capacitive and inductive paths permit coupling to the power distribution harness. Burst frequency and duration is controlled by subsystem circuit parameters, relay contact characteristics and the transmission coefficients of the power distribution harness. On the basis of data supplied in MIL-STD-704B, less than 1.4% of 1800 burst transient measurements on 25 aircraft indicated amplitudes in excess of 100 volts. The maximum recorded voltage was 250 volts. The general characteristics appear to be independent of line voltage, however there is insufficient evidence at this time to define a basis for maximum limits. This area will be studied when the test facility is in operation during the next phase of this contract.

### 3.6.3 EMI Filtering

Optimum design approaches must trade the overall cost of designing user systems to broader tolerances versus upgrading the quality of delivered power. These considerations as well as limitations on life, maximum power or total energy which are unique to space vehicles, establish the necessity to minimize the cost, weight and volume penalty of the total system which may be assessed to the power requirement. EMI susceptibility and interference limitations are representative of the results of this optimization study. It is normally necessary to provide filtering between all loads in a large space vehicle and the power distribution harness to maintain power quality and enable acceptable performance of user equipment. The design requirements on the filters are functions of the EMC plan criteria and the characteristics of the individual loads. It should be noted that even passive loads such as heaters may require filtering due to turn on transients. Furthermore,

all loads normally subtend a loop of significant size and consequently act as a receiver or transmitter of EMI coupled inductively, capacitively and electromagnetically.

### 3.6.3.1 Filter Design

The use of distribution voltages higher than 28V influences input filter design as indicated in Figure 3.6-9b. In general, the filtering requirement for equivalent loads and equal power is less at 120 VDC. Considerations of weight, initial surge and overshoot limitations indicate the use of the two stage filter design illustrated in Figure 3.6-11 for pulse width modulator and converter loads.

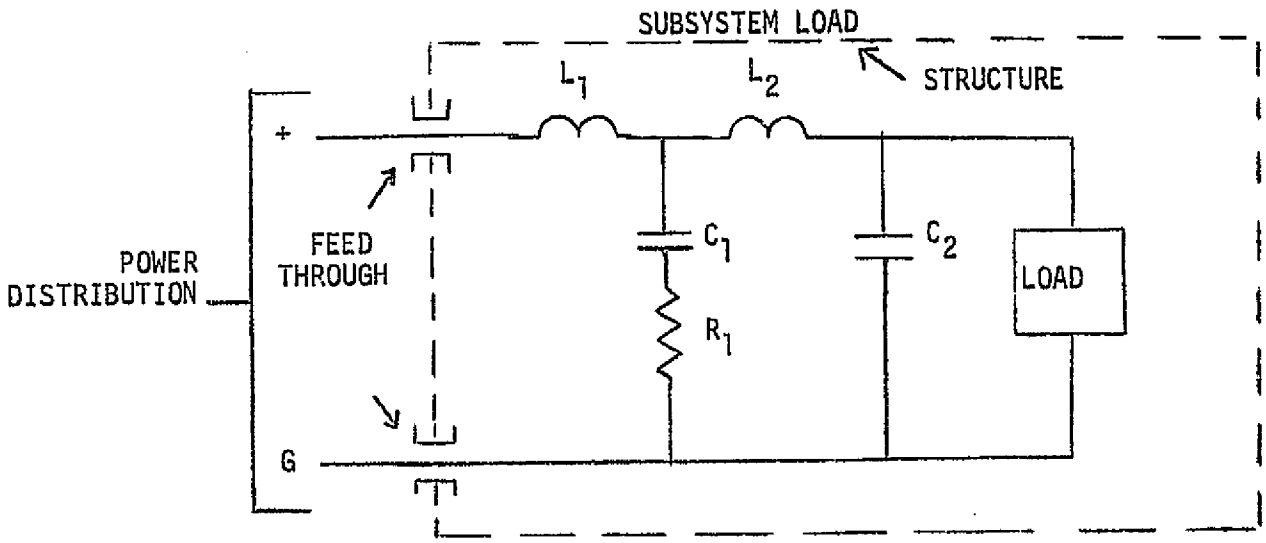



Figure 3.6-11. Power Input Filtering

A computer program was developed during the previous study to calculate electrical parameters and estimate size and weight of this filter. A discussion of this program may be found in Appendix A of the Phase 1 final report (Contract NAS8-28726) of this study program. An evaluation of filter designs for a 500 watt PWM load at 28 VDC and 120 VDC was performed for frequencies from 1.0 KHz to 20 KHz. The filter design program was modified to include the EMI requirements of Figure 3.6-9b.

The results of this evaluation are illustrated in Figure 3.6-12. A summary of the point designs may be found in Appendix B of this report. It should be noted that the curves are not smooth because the program is constrained to use capacitive values and sizes available commercially at each voltage rating. Powdered iron toroids are defined on the basis of an optimum coil design program developed at TRW. The electrical parameters for the filter are based on a model design which provides the required attenuation of load noise and limits input surge voltages to 150% of line voltage.

It should be noted that the values plotted in Figure 3.6-12 are based on weight and volume of parts and do not include allowances for mounting hardware or layout design.

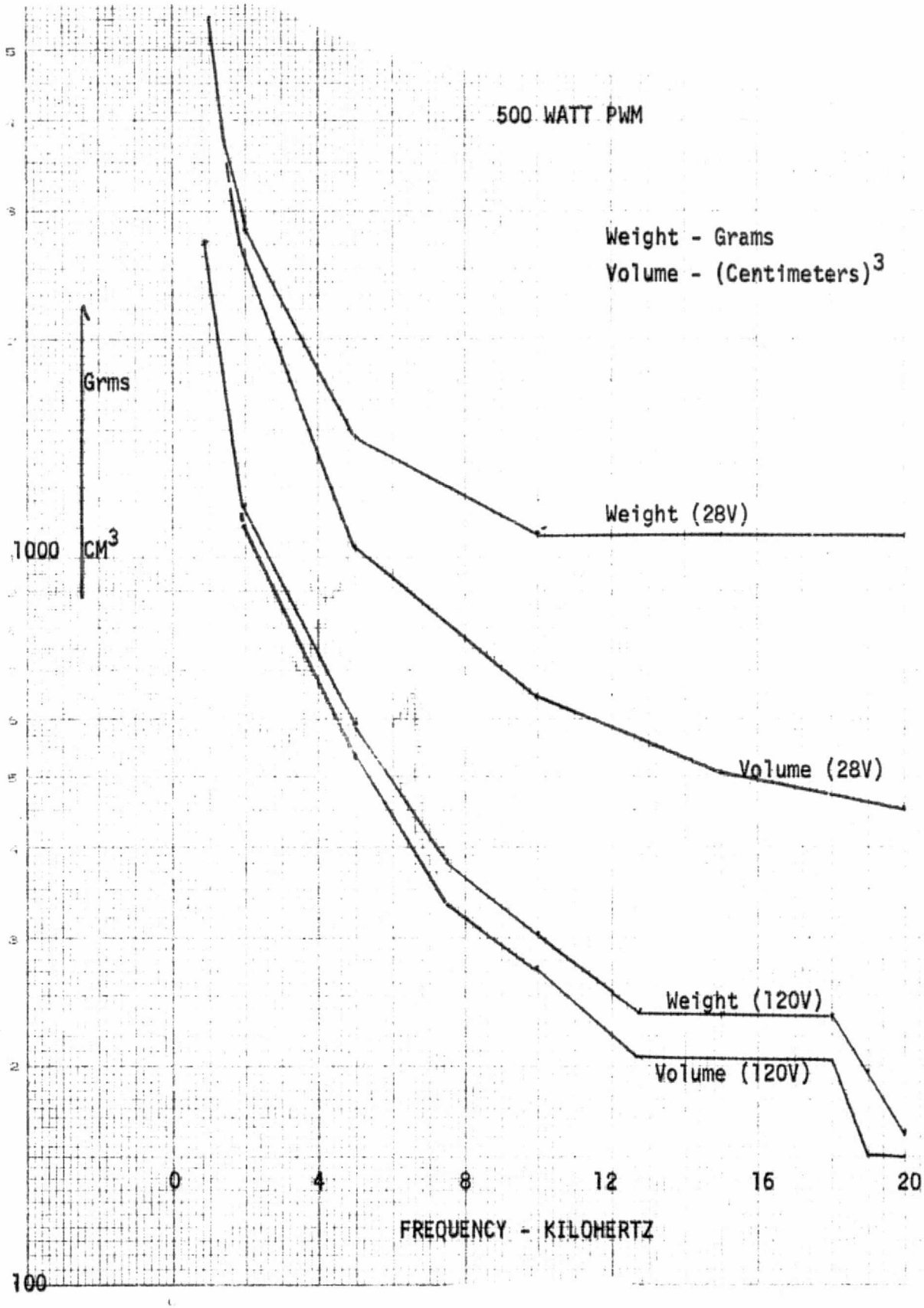



Figure 3.6-12. Input Filter Design

C-2

# APPENDIX A

## DISTRIBUTION CABLE CHARACTERISTICS

# APPENDIX A

# DISTRIBUTION CABLE CHARACTERISTICS

## 1.0 INTRODUCTION

The study of characteristics and behavior of aerospace power distribution cable deviates from similar studies made for radio frequency or large ground power systems; the former is concerned with high frequency transmission and the latter with low frequency and dc. Both of these applications employ cable designs which optimize their performance and the analyses may utilize simplified transmission line equations. Aerospace power distribution systems are usually simulated by lumped constant coupling circuits. The study for this program is concerned not only with the principle power distribution function of the cable, but also the manner in which the cable design for various applications influences the generation and transmission of line transients and noise. Analyses of fast transients require a model with distributed, frequency sensitive parameters which are a function of the total physical environment.

## 2.0 CONDUCTOR CHARACTERISTICS

The conductors in power distribution cable are selected with consideration for current capacity, resistance at low frequency and the ability to withstand the physical stress inherent in power distribution harness assembly and application. Wire is normally stranded to obtain flexibility and improve capability to withstand vibration and shock which might otherwise cause a break in a solid conductor. Plating is used to provide resistance to corrosion and improve solderability. Tin plating was used originally to inhibit chemical reactions between copper and sulphur in the then current rubber insulation. Although tin plating performed adequately with respect to corrosion, solding and crimping characteristics, the maximum temperature limit (150°C) for this wire was not sufficiently high for many applications or for use with the new teflon insulations. Silver coated wire may be used at higher temperatures (200°C) and also has excellent soldering and crimping characteristics. However, severe cuprous oxide corrosion (red plague) tended to occur in the presence of moisture and oxygen. These inclusions were due primarily to wet insulation

tests where water could enter through defects in the Teflon and travel considerable distances along the wire. Although instances of this corrosion are becoming increasingly rare with the dry insulation test now commonly used, considerations of reliability and safety have resulted in a shift toward nickel plating in manned spacecraft, commercial and military aircraft. Nickel offers some initial difficulties with respect to soldering and crimping which are resolved by improved assembly control processes and training programs. The primary advantage of nickel plating are high temperature capability (260°C, Teflon insulated wire) and resistance to corrosion. Nickel is regarded as undesirable in scientific spacecraft applications where the presence of magnetic material may interfere with operation of sensitive instruments. From the standpoint of the electrical systems engineer the use of nickel plating is normally considered academic. Inductance is higher at low frequencies and (skin) resistance is significantly increased at high frequencies when compared to silver plated wire. These parameters influence the frequency content and energy of switching transients and noise. Analysis of plated and bare copper wire was undertaken to enable the performance of quantitative analysis of power distribution harness transmission and coupling of signals.

## 3.0 ANALYSIS

The basic structure of a conductor suitable for use in a power distribution harness is given in Table A-1.

Table A-1. Conductor Characteristics

| | |
|---|---|
| Conductor Size | #8 (MSFC Specification 40M39513) |
| Nominal Conductor Area | 16,983 circular mils |
| Number of Strands | 133 |
| Strand Size | AWG #29 |
| Plating | Nickel |
| Plating Thickness | 0.2 mils |
| Resistance | 0.688 ohms/1,000 feet |
| Insulation | TFE or FEP (Teflon) |
| Insulation Thickness | 20 mils |

It should be noted that conductors meeting MSFC specifications differ slightly from standard American Wire Gauge cross sections.

Two conductor models were used in the analysis of power distribution conductors. A low frequency model consisted of a solid conductor with conductivity and permeability equal to the cross sectional averages of the real conductor and included the effects of voids and plating material. Use of this model enabled the application of equations which relate electrical parameters to the dimensions of solid cylindrical conductors. The high frequency model utilized thin walled shell approximations with the outer shell constants equivalent to the plating material conductivity, permeability and thickness; the inner shell used constants associated with copper. The equations for the two models are given below.

Low Frequency Model

$$Z_i = \frac{j R_s}{\sqrt{2}\,\pi r_o} \left[ \frac{\text{Ber } q + j\ \text{Bei } q}{\text{Ber}'q + j\ \text{Bei}'q} \right] \quad \text{ohms/meter} \qquad \text{Eq A-1}$$

$R_s$ = Skin Resistance

$$= \sqrt{\frac{\pi f \mu}{\sigma}}$$

$f$ = Frequency

$\mu$ = Permeability

$\sigma$ = Conductivity

$r_o$ = Conductor radius

$$q = \frac{\sqrt{2}\ r_o}{\delta}$$

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$

Ber q, Bei q = Real and imaginary part of Jo ($j^{\frac{1}{2}}q$)

Jo (x) = Bessel function

$$\text{Ber}'q = \frac{d}{dq}\ (\text{Ber } q)$$

$$\text{Bei}'q = \frac{d}{dq}\ (\text{Bei } q)$$

High Frequency Model

$$\frac{Z}{R_{s1}} = (1+j)\left[\frac{\text{Sinh}\tau_1 d + (R_{s2}/R_{s1})\ \text{Cosh}\ \tau_1 d}{\text{Cosh}\tau_1 d + (R_{s2}/R_{s1})\ \text{Sinh}\ \tau_1 d}\right] \qquad \text{Eq A-2}$$

$\tau = (1+j)/\delta$

$d$ = plating thickness

Subscripts

1 = Plating material

2 = Conductor core material

Eq A-2 will always have greater impedance than Eq A-1 at high frequencies due to the pure nickel plating. The logic in the program selects the greater of the two impedances. The crossover between models always takes place at frequencies for which the depth of penetration is small with respect to the radius of the conductor.

Standard approaches were used to calculate inductance and capacitance between wires. The program contains a data file for conductor wire sizes #4 to #28. Data includes plating thickness, stranding, cross section and insulation thickness. Program input/output characteristics are listed below.

Program Inputs

Plating (nickel, tin, silver or unplated)
Wire Spacing (inches)
Wire Length (meters)
Wire Size (#4 to #28)
Termination Impedance (Series R,L,C)

Program Outputs

Distributed impedance parameters
Characteristic line impedance
Propagation Constants
Input impedance (with specified load termination)

The program was designed primarily as a convenient tool for study of conducted noise problems in the HVDC test facility. Comparison between calculated impedance and measured impedance (Figure A-1) indicates good correlation for a ten foot length of #8 twisted pair for frequencies below 12 MHz. Deviation between measurement and calculation are due to slight differences in wavelength; resonant peaks are approximately equivalent. A comparison between the specific impedance of nickel and silver coated conductors is illustrated in Figure A-2. Study of these differences and correlation with facility test will enable a more general extrapolation of test results to future power distribution designs. This program was utilized to obtain the distributed impedance parameters for the calculations in Section 3.6 of this report. A listing of the program is provided in Table A-2.

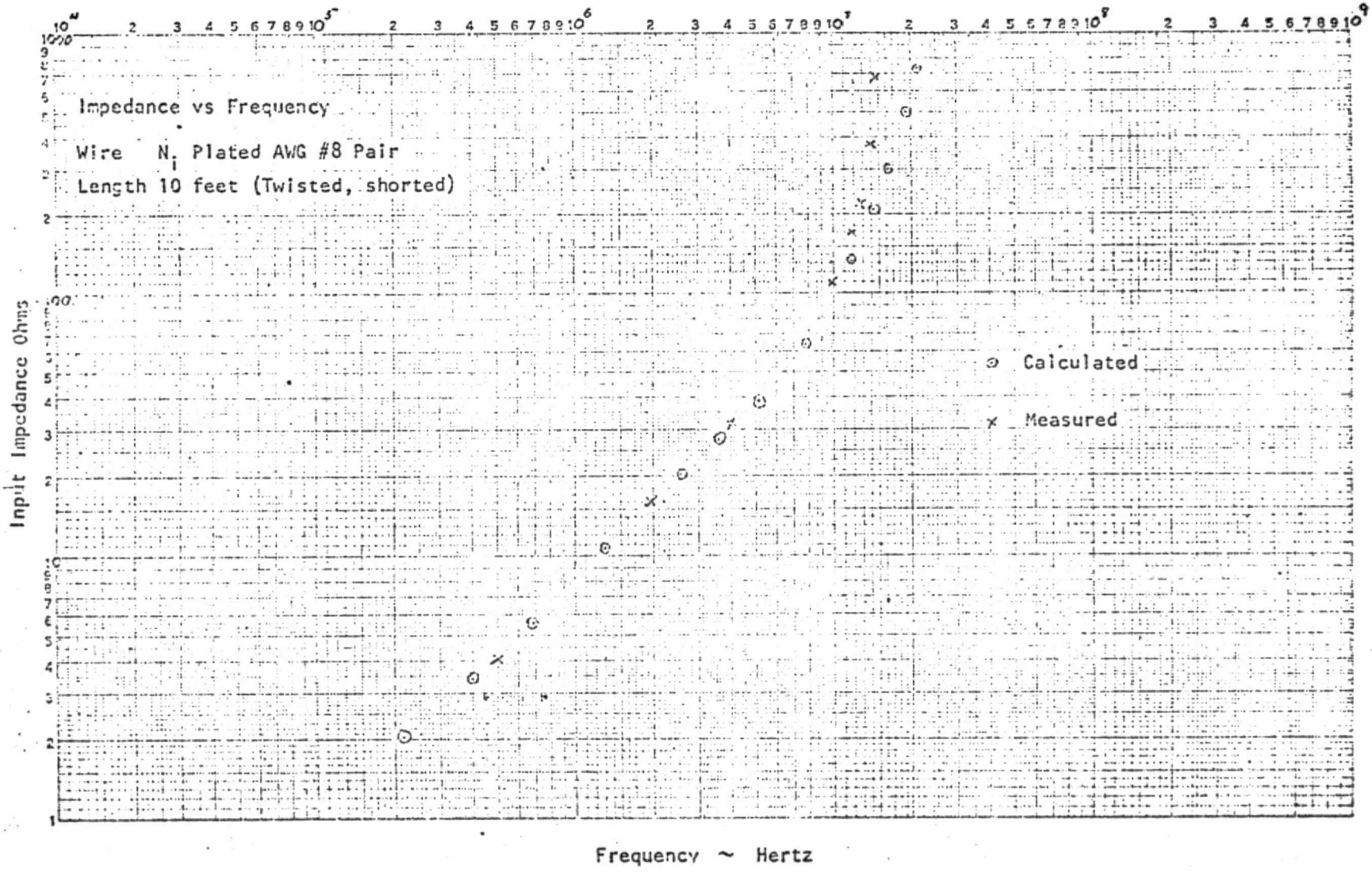

Impedance vs Frequency
Wire N, Plated AWG #8 Pair
Length 10 feet (Twisted, shorted)
Calculated
Measured
Input Impedance Ohms
Frequency ~ Hertz

Figure A-1

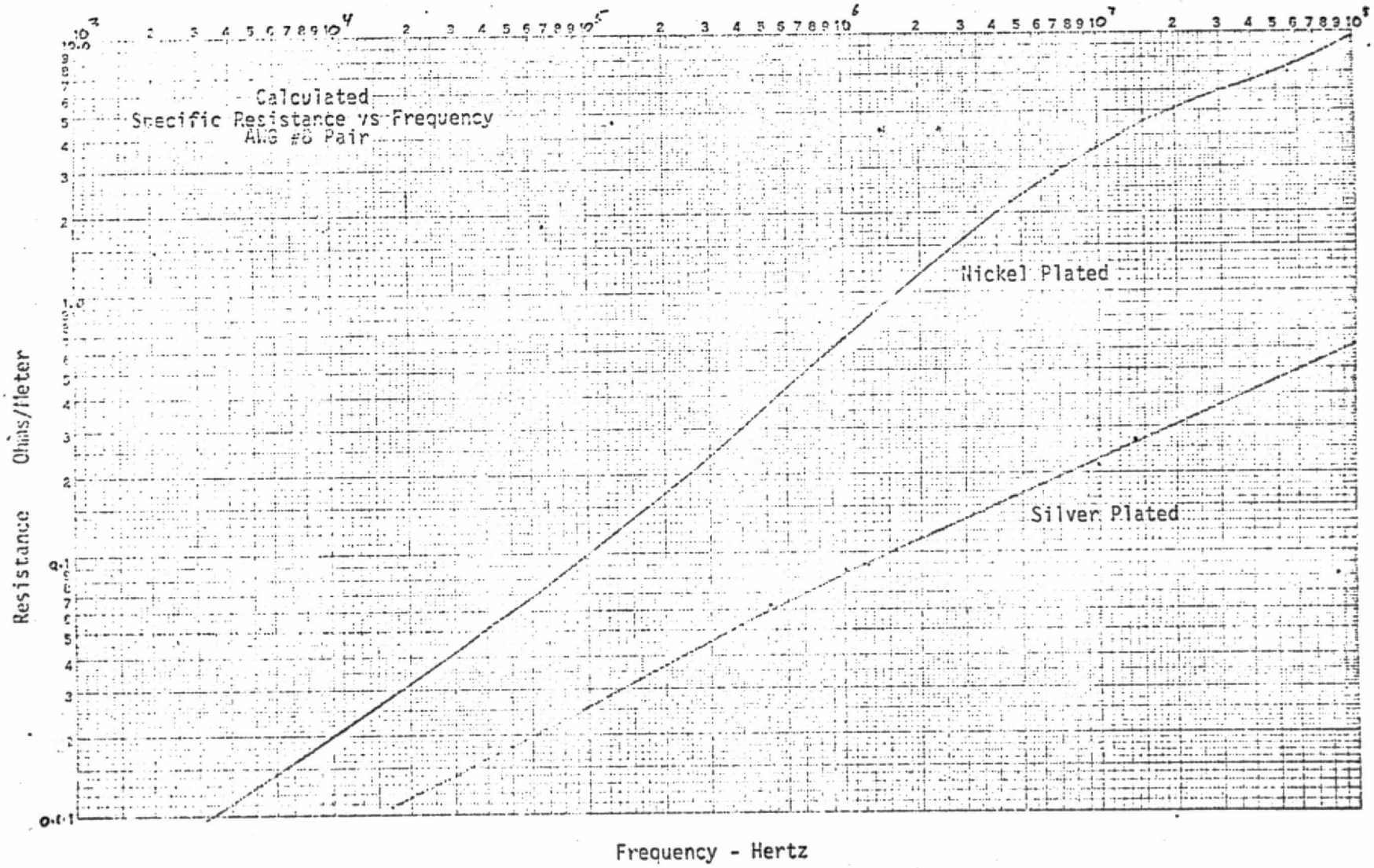

Calculated
Specific Resistance vs Frequency
AWG #8 Pair
Nickel Plated
Silver Plated
Resistance Ohms/Meter
Frequency - Hertz

Figure A-2

## Table A-2. Twisted Pair Impedance Analysis

```
100   *PRIMP-ANALYSIS OF TWISTED PAIR
110   PRINTEWIRE SIZE(4-28),PLATING:CU(1),AG(2),NI(3),TIN(4),GAP-INE
120   INPUT W,P,D3
130   PRINTEF1,F2,NO. OF PTS.,LOG(1) OR LINEAR(2) FREQ SCALEE
140   INPUT F1,F2,F3,F4
150   VAR=ZERO
160   DIM A(0:30)
170   DIM B(30)
180   DIM C(30)
190   DIM D(30)
200   DIM E(30)
210   DIM F(0:30)
220   DIM G(30)
230   DIM H(30)
240   DIM I(30)
250   DIM J(30)
260    DIM K(30,30)
270   DIM L(30)
280   DIM R(30)
290   DIM T(30)
300   DIM Q(30)
310   DIM Y(40)
320   DIM M(30)
330   DIM N(30)
340   DIM O(30)
350   DIM P(30)
360   DIM V(30)
370   DIM X(30)
380   DIM S(30)
390   DIM W(30)
400   PRINTEE
410   PRINTEE
420   ON P GOTO 430,450,470,490
430   PRINTENOE:W,EUNCOATED COPPER WIRE PAIRE
440   GOTO 500
450   PRINTENOE:W,ESILVER COATED COPPER WIRE PAIRE
460   GOTO 500
470   PRINTENOE:W,ENICKEL COATED COPPER WIRE PAIRE
480   GOTO 500
490   PRINTENOE:W,ETIN COATED COPPER WIRE PAIRE
500  PRINTERE,ELE,EVE,EZE,ETHETAE
510   W1=W/2-1
```

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## Table A-2. Twisted Pair Impedance Analysis (Continued)

```
520   N=N+1
530   READ A1,N1,D1,D2,D7
540   IF N<W1 THEN 520
550   DATA 42615,133,.0181,.267,.02
560   DATA 26818,133,.0142,.211,.02
570   DATA 16983,133,.0114,.1575,.02
580   DATA 9413,37,.0161,.1115,.015
590   DATA 6088,19,.0180,.088,.015
600   DATA 3831,19,.0142,.0695,.015
610   DATA 2426,19,.0114,.0565,.009
620   DATA 1900,19,.0101,.049,.009
630   DATA 1215,19,.0081,.038,.009
640   DATA 754,19,.0064,.031,.009
650   DATA 475,19,.0051,.0245,.009
660   DATA 304,19,.0041,.0195,.009
670   DATA 175,7,.0051,.015,.009
680   DATA 1.257E-6,5.8E7
690   DATA 1.257E-6,6.173E7
700   DATA 6.285E-5,1.45?E7
710   DATA 1.257E-6,.877E7
720   ON P GOTO 730  ,750  ,770  ,790
730   RESTORE 680
740   GOTO 800
750   RESTORE 690
760   GOTO 800
770   RESTORE 700
780   GOTO 800
790   RESTORE 710
800   READ U2,S2
810   S1=5.8*1E7
820   U1=1.257*1E-6
830   D4=D3+2*D7
840   D5=(D4+D2)/D2
850   D6=D5/SQR(D5↑2-1)          ↓HI FREQ FACTOR RE RAW
860   A2=2E-4*PI*D1*N1*6.45E-4                    ↓PL AR MSQ
870   A3=(PI*A1↑6.45E-10)/4                       ↓CU AR MSQ
880   R4=D2*.0254/2                               ↓R OF WIRE
890   A4=PI*(R4↑2)                              ↓AR OF WIRE
900   IF P=1 THEN 930
910   S4=(S1*A3+S2*A2)/A4                       ↓EQUIV SIGMA
920   GOTO 940
930   S4=S1*A3/A4
```

## Table A-2. Twisted Pair Impedance Analysis (Continued)

```
940   U4=(U2*A2+U1*(A4-A2))/A4
950   D8=LOG(D5+SQR(D5+2-1))                          +COSH-1 S/D
960   A(0)=1
970   K=K+1
980   A(K)=A(K-1)*(-1)/(((4*K)+2)*((4*K-2)+2))  +BESSELCOEFF BER
990   B(K)=-A(K)*((4*K)+2)                          +BEI
1000   C(K)=A(K)*4*K                                 +BER'
1010   D(K)=B(K)*(4*K-2)                             +BEI'
1020   IF K=20 THEN 1040
1030   GOTO 970
1040   K=0
1050   GOTO 1080
1060   F1=1/((PI*U1*S1*4*((D2*.0254)+2)))            +INITIAL FREQ
1070   F1=10+(INT(LGT(F1)))
1080   F2=LGT((F2/F1))/F3
1090   F5=(F2-F1)/F3
1100   Z=Z+1
1110   ON F4 GOTO 1120,1140
1120   F(Z)=F1*(10+(F5*(Z-1)))
1130   GOTO 1150
1140   F(Z)=F1+(Z-1)*F6
1150   N(Z)=1/SQR(PI*F(Z)*U1*S1)
1160   M(Z)=1/(N(Z)*S1)
1170   L(Z)=1/(SQR(PI*F(Z)*U4*S4))                   +DELTA WIRE EQ
1180   G(Z)=1/SQR(PI*F(Z)*U2*S2)                     +DELTA PL
1190   R(Z)=1/(L(Z)*S4)                              +R(SKN) WIRE
1200   T(Z)=1/(G(Z)*S2)                              +R(SKN) PL
1210   Q(Z)=1.414*R4/L(Z)                            +Q EQ WIRE
1220   A(30)=1
1230   K=K+1
1240   GOTO 1250
1250   J=A(K)*Q(Z)+(4*K))
1260   A(30)=A(30)+J
1270   IF K=20 THEN 1290
1280   GOTO 1230
1290   K=0
1300   B(30)=0
1310   K=K+1
1320   B(30)=B(30)+E(K)*(Q(Z)+(4*K-2))                +BEI Q
1330   IF K=20 THEN 1350
1340   GOTO 1310
1350   K=0
```

## Table A-2. Twisted Pair Impedance Analysis (Continued)

```
1360   C(30)=0
1370   K=K+1
1380   C(30)= C(30)+C(K)*(Q(Z)↑(4*K-1))          ↓BER≠ 0
1390   IF K=20 THEN 1410
1400   GOTO 1370
1410   K=0
1420   D(30)=0
1430   K=K+1
1440   D(30)=D(30)+D(K)*((Q(Z)↑(4*K-3)))         ↓BEI≠ 0
1450   IF K=20 THEN 1470
1460   GOTO 1430
1470   K=0
1480  Y(1)=5.08E-6/G(Z)      ↓Y(1)-Y(16) EQIV TUBE HI FREQ APPROX
1490  Y(2)=COS(Y(1))
1500  Y(3)=SQR(1-Y(2)↑2)
1510  Y(4)=EXP(Y(1))
1520  Y(5)=(Y(4)+1/Y(4))/2
1530  Y(6)=(Y(4)-1/Y(4))/2
1540  Y(7)=Y(6)*Y(2)+R(Z)*Y(5)*Y(2)/T(Z)
1550  Y(8)=Y(5)*Y(3)+R(Z)*Y(6)*Y(3)/T(Z)
1560  Y(9)=Y(5)*Y(2)+R(Z)*Y(6)*Y(2)/T(Z)
1570  Y(10)=Y(6)*Y(3)+R(Z)*Y(5)*Y(3)/T(Z)
1580  Y(11)=SQR(2*(Y(7)↑2+Y(8)↑2)/(Y(9)↑2+Y(10)↑2))
1590  Y(12)=PI/4+(ATN(Y(7),Y(8))-ATN(Y(9),Y(10)))
1600  Y(13)=COS(Y(12))
1610  Y(14)=COS(Y(13))*TAN(Y(13))
1620  Y(15)=D6*T(Z)*Y(11)*Y(13)/(PI*R4)
1630  Y(16)=D6*T(Z)*Y(11)*Y(14)/(2*F(Z)*(PI*PI)*R4)
1640  E(Z)=(A(30)*D(30)-B(30)*C(30))/((C(30)↑2+D(30)↑2)*1.414*R4)  ↓R
1650  J(Z)=2*R4*E(Z)*R(Z)
1660  H(Z)=(A(30)*C(30)+B(30)*D(30))/(C(30)↑2+D(30)↑2)              ↓WL
1670  I(Z)=1.414*R(Z)*H(Z)
1680  E(Z)=2*E(Z)*R(Z)/PI                    ↓R EQ WIRE
1690  H(Z)=2*H(Z)*R(Z)/(2.828*(PI↑2)*F(Z)*R4)      ↓L EQ WIRE
1700  O(Z)=ATN(I(Z),J(Z))-PI/4
1710  P(Z)=SQR(J(Z)↑2+I(Z)↑2)/(T(Z)*1.414)
1720  J(Z)=P(Z)*COS(O(Z))
1730  I(Z)=P(Z)*COS(O(Z))*TAN(O(Z))
1740  Y(18)=Y(6)*Y(2)-I(Z)*Y(6)*Y(3)+J(Z)*Y(5)*Y(2)  ↓E,H HOM WIRE
1750  Y(19)=Y(5)*Y(3)+I(Z)*Y(5)*Y(2)+J(Z)*Y(6)*Y(3)
1760  Y(20)=Y(5)*Y(2)-I(Z)*Y(5)*Y(3)+J(Z)*Y(6)*Y(2)
1770  Y(21)=Y(6)*Y(3)+I(Z)*Y(6)*Y(2)+J(Z)*Y(5)*Y(3)
```

Table A-2. Twisted Pair Impedance Analysis (Continued)

```
1780  Y(22)=SQR((Y(18)↑2+Y(19)↑2)/(Y(20)↑2+Y(21)↑2))
1790  Y(23)=ATN(Y(19),Y(18))-ATN(Y(21),Y(20))+PI/4
1800  Y(24)=COS(Y(23))
1810 Y(25)=COS(Y(23))*TAN(Y(23))
1820  Y(26)=2*T(Z)*Y(22)*Y(24)/(1.414*PI*R4)
1830  Y(27)=2*T(Z)*Y(22)*Y(25)/(1.414*PI*R4)
1840  Y(28)=Y(27)/(2*PI*F(Z)) ↓Y(16)-Y28) PL RND WIRE
1850 SIGNIFICANCE 3
1860  IF Y(15)>E(Z) THEN 1910
1870  IF Q(Z)>20 THEN 1910
1880  H(Z)=U1*D8/PI+Y(28)
1890  E(Z)=Y(26)
1900  GOTO 1930
1910  E(Z)=Y(15)
1920  H(Z)=Y(16)+U1*D8/PI
1930  Y(17)=1/(D8*36E9)
1940 V(Z)=1E-6/SQR(H(Z)*Y(17)*9)
1950  A(Z)=2*PI*F(Z)*H(Z)
1960 S(Z)=(ATN(X(Z)/E(Z))-PI/2)/2
1970  W(Z)=SQR(SQR((E(Z)/(2*PI*F(Z)*Y(17)))↑2+(H(Z)/Y(17))↑2))
1980  PRINT  E(Z),H(Z),V(Z),W(Z),S(Z)*180/PI
1990 IF Z>23 THEN 2020
2000   IF Z>F3 THEN 2020
2010 GOTO 1180
2020 PRINT ΞCΞ:Y(17)
2030  PRINTΞLΞ:U1*D8/PI
2040   PRINTΞINPUT LOAD R,L,C,LN LENGTH (METERS)Ξ
2050   INPUT Y(31),Y(29),Y(30),Y(32)
2060   PRINTΞF(4)Ξ,ΞALPHAΞ,ΞBΞTAΞ,ΞZΞ,ΞTHETAΞ
2070   Z=0
2080   Z=Z+1
2090   K(Z,26)=F(Z)*W(Z)*2*PI*Y(17)
2100   K(Z,1)=K(Z,26)*Y(32)
2110   K(Z,27)=S(Z)+PI/2
2120   K(Z,2)=K(Z,27)
2130   K(Z,3)=W(Z)*COS(S(Z))
2140   K(Z,4)=K(Z,3)*TAN(S(Z))
2150   K(Z,5)=Y(31)
2160   K(Z,6)=2*PI*F(Z)*Y(29)
2170   IF Y(30)=0 THEN 2190
2180   K(Z,6)=K(Z,6)-1/(2*PI*F(Z)*Y(30))
2190   K(Z,7)=K(Z,1)*COS(K(Z,2))
```

## Table A-2. Twisted Pair Impedance Analysis (Continued)

```
2200    K(Z,8)=K(Z,7)*TAN(K(Z,2))
2210    K(Z,9)=EXP(K(Z,7))
2220    GOTO 2240
2230    PRINT#1,2,7,9#:K(Z,1),K(Z,2),K(Z,7),K(Z,9)
2240    K(Z,10)=(K(Z,9)+1/K(Z,9))/2
2250    K(Z,11)=(K(Z,9)-1/K(Z,9))/2
2260    K(Z,12)=COS(K(Z,8))
2270    K(Z,13)=K(Z,12)*TAN(K(Z,8))
2280    K(Z,14)=K(Z,6)*K(Z,10)+K(Z,4)*K(Z,11)
2290    K(Z,15)=K(Z,5)*K(Z,11)+K(Z,3)*K(Z,10)
2300    K(Z,16)=K(Z,5)*K(Z,10)+K(Z,3)*K(Z,11)
2310    K(Z,17)=K(Z,4)*K(Z,10)+K(Z,6)*K(Z,11)
2320    K(Z,18)=K(Z,15)*K(Z,12)-K(Z,17)*K(Z,13)
2330    K(Z,19)=K(Z,14)*K(Z,12)+K(Z,16)*K(Z,13)
2340    K(Z,20)=K(Z,'5)*K(Z,12)-K(Z,14)*K(Z,13)
2350    K(Z,21)=K(Z,17)*K(Z,12)+K(Z,16)*K(Z,13)
2360    K(Z,22)=SQR(K(Z,18)↑2+K(Z,19)↑2)
2370    K(Z,23)=SQR(K(Z,20)↑2+K(Z,21)↑2)
2380    K(Z,24)=K(Z)*K(Z,22)/K(Z,23)
2390    K(Z,25)=ATN(K(Z,19),K(Z,18))-ATN(K(Z,21),K(Z,20))+S(Z)
2400    PRINT F(Z),K(Z,7),K(Z,8),K(Z,24),K(Z,25)*180/PI
2410  IF Z<F3 THEN 2430
2420    IF Z<24 THEN 2080
2430    END
```

# APPENDIX B

# FILTER DESIGN

# APPENDIX B

## FILTER DESIGN

The PWM power input filter design program developed during Phase 1 of this study has been updated to provide designs which are in accord with the EMI limits calculated in Section 3.6 of this report. The design is a two stage LC filter (Figure B-1) with a small damping resistance in series with the first stage capacitor. Output (second stage) capacitance values are calculated on the basis of allowable r.m.s. current and voltage, capacitors are selected from a file of CRC series 12 metallized polycarbonate capacitors contains within the program. The remaining inductance and capacitance values are then calculated to obtain the required attenuation and input surge characteristics. The values of the first stage polarized plain-foil capacitors are obtained from a file derived from Sprague Engineering Bulletin No. 3601C (Type 110D). The capacitor file includes size, weight and maximum permitted voltage. Inductors are calculated on the basis of an optimized coil design algorithm developed at TRW for powdered iron toroids. Weights and dimensions reflect actual and calculated values for capacitors, toroids, windings and inductor packaging and does not include circuit wiring, mounting hardware or factors introduced by layout configuration. Further discussion of this program may be obtained from Appendix A of the Phase 1 report.

Filter designs for the analysis of Section 3.6 were obtained through use of this program. Weight and volume for a 500 watt pulse width modulator input filter at 28VDC and 120VDC line voltages are illustrated in Figure B-2. Discontinuities in the curves are due to the step change associated with discrete values of acutal parts. These curves are based on program outputs presented in Table B-1. The revised Filter design program is attached as Table B-2.

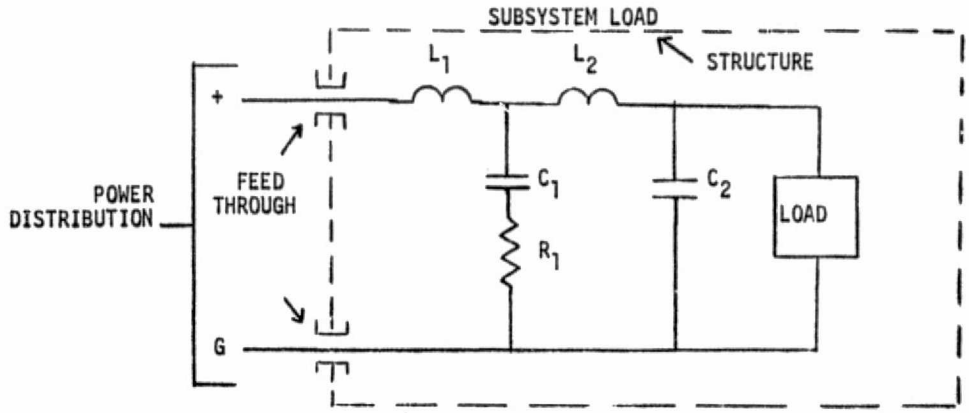


Figure B-1. Power Input Filtering

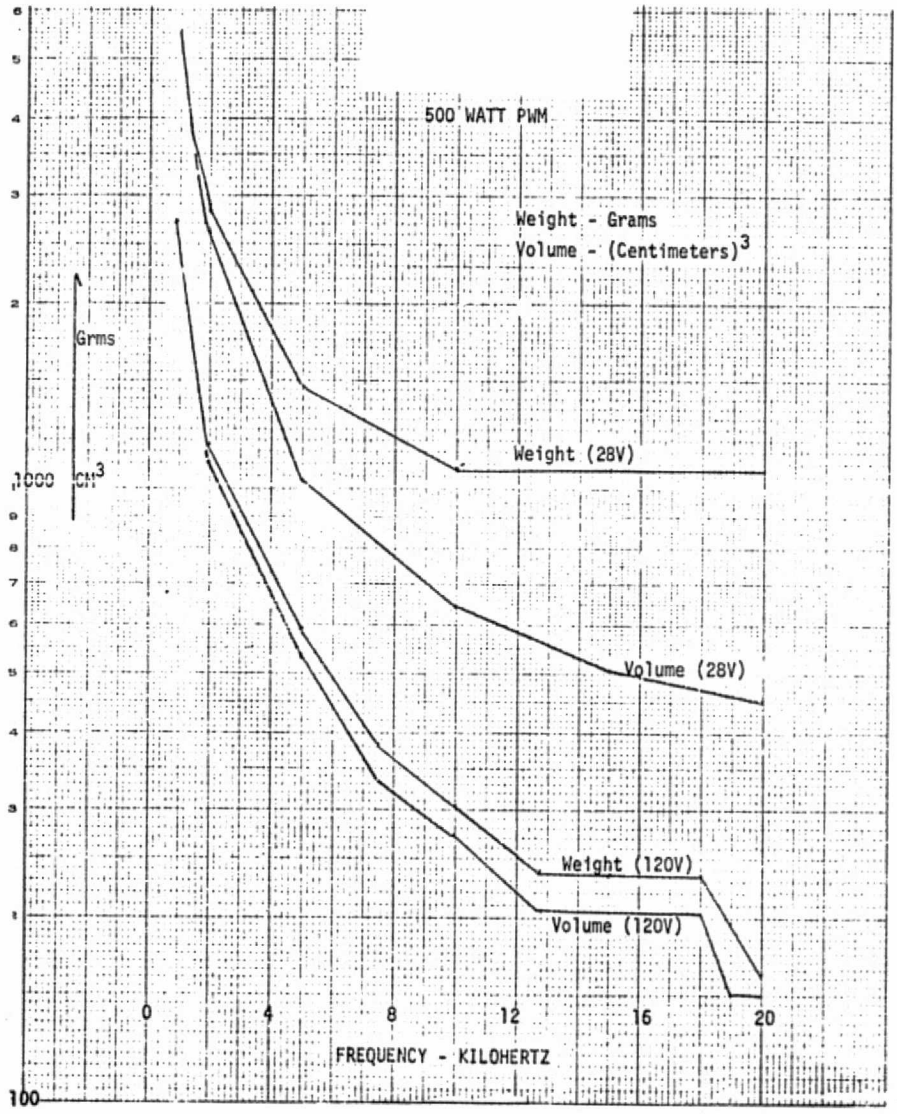


Figure B-2. Input Filter Design

Table B-1. Filter Design - 500 Watts

Line Voltage = 28 VDC
Frequency = 20 KHZ

| | | |
|---|---|---|
| ? 28,500,20 | | |
| INDUCTANCE(L1,L2),MH= | .113E+00 | .567E-01 |
| AREA,SQ-CM= | 1.61 | 1.14 |
| NUMBER OF TURNS= | 42 | 29.7 |
| MEAN MAG LENGTH,CM= | 16.3 | 13.7 |
| PERMEABILITY= | 51.8 | 61.6 |
| WEIGHT,GRAM= | 547 | 325 |
| VOLUME CU-CM= | 109 | 65 |
| DISSIPATION WATTS= | 2.72 | 1.62 |
| RESISTANCE OHMS= | .853E-02 | .507E-02 |
| CAPACITANCE(C1,C2),UF= | .108E+04 | 100 |
| WEIGHT,GRMS= | 48.5 | 215 |
| VOLUME,CU-CM= | 126 | 152 |
| RESISTANCE(R1),OHMS= | .48E+00 | |
| TOTAL WEIGHT,GRMS,LBS= | .114E+04 | 2.5 |
| TOTAL VOL,CU-CM,IN-CU= | 452 | 27.6 |
| TOTAL DISSIPATION,WATTS= | 4.34 | |
| EFFICIENCY,%= | .868E+00 | |

Frequency = 15 KHZ

| | | |
|---|---|---|
| INDUCTANCE(L1,L2),MH= | .992E-01 | .496E-01 |
| AREA,SQ-CM= | 1.5 | 1.06 |
| NUMBER OF TURNS= | 39.3 | 27.8 |
| MEAN MAG LENGTH,CM= | 15.7 | 13.2 |
| PERMEABILITY= | 53.6 | 63.7 |
| WEIGHT,GRAM= | 495 | 294 |
| VOLUME CU-CM= | 98.9 | 58.8 |
| DISSIPATION WATTS= | 2.46 | 1.46 |
| RESISTANCE OHMS= | .772E-02 | .459E-02 |
| CAPACITANCE(C1,C2),UF= | .132E+04 | 130 |
| WEIGHT,GRMS= | 59.2 | 280 |
| VOLUME,CU-CM= | 155 | 197 |
| RESISTANCE(R1),OHMS= | .406E+00 | |
| TOTAL WEIGHT,GRMS,LBS= | .113E+04 | 2.49 |
| TOTAL VOL,CU-CM,IN-CU= | 509 | 31.1 |
| TOTAL DISSIPATION,WATTS= | 3.92 | |
| EFFICIENCY,%= | .785E+00 | |

Table B-1 (cont.)
Filter Design - 500 Watts

Line Voltage = 28 VDC
Frequency = 10 KHZ

| | | |
|---|---|---|
| ? 28,500,10 | | |
| INDUCTANCE(L1,L2),MH= | .755E-01 | .377E-01 |
| AREA,SQ-CM= | 1.31 | .927E+00 |
| NUMBER OF TURNS= | 34.3 | 24.2 |
| MEAN MAG LENGTH,CM= | 14.7 | 12.4 |
| PERMEABILITY= | 57.4 | 68.2 |
| WEIGHT,GRAM= | 403 | 240 |
| VOLUME CU-CM= | 80.5 | 47.9 |
| DISSIPATION WATTS= | 2 | 1.19 |
| RESISTANCE OHMS= | .629E-02 | .374E-02 |
| CAPACITANCE(C1,C2),UF= | .192E+04 | 190 |
| WEIGHT,GRMS= | 86.2 | 409 |
| VOLUME,CU-CM= | 225 | 288 |
| RESISTANCE(R1),OHMS= | .294E+00 | |
| TOTAL WEIGHT,GRMS,LBS= | .114E+04 | 2.51 |
| TOTAL VOL,CU-CM,IN-CU= | 642 | 39.1 |
| TOTAL DISSIPATION,WATTS= | 3.2 | |
| EFFICIENCY,%= | .639E+00 | |

Frequency = 5 KHZ

| | | |
|---|---|---|
| INDUCTANCE(L1,L2),MH= | .476E-01 | .238E-01 |
| AREA,SQ-CM= | 1.04 | .736E+00 |
| NUMBER OF TURNS= | 27.2 | 19.2 |
| MEAN MAG LENGTH,CM= | 13.1 | 11 |
| PERMEABILITY= | 64.4 | 76.6 |
| WEIGHT,GRAM= | 285 | 170 |
| VOLUME CU-CM= | 57 | 33.9 |
| DISSIPATION WATTS= | 1.42 | .844E+00 |
| RESISTANCE OHMS= | .445E-02 | .265E-02 |
| CAPACITANCE(C1,C2),UF= | .372E+04 | 370 |
| WEIGHT,GRMS= | 167 | 796 |
| VOLUME,CU-CM= | 436 | 561 |
| RESISTANCE(R1),OHMS= | .168E+00 | |
| TOTAL WEIGHT,GRMS,LBS= | .142E+04 | 3.12 |
| TOTAL VOL,CU-CM,IN-CU= | .109E+04 | 66.4 |
| TOTAL DISSIPATION,WATTS= | 2.26 | |
| EFFICIENCY,%= | .453E+00 | |

Table B-1 (cont.)
Filter Design - 500 Watts

Line Voltage = 28 VDC
Frequency = 2 KHZ

```
? 28,500,2
INDUCTANCE(L1,L2),MH=          .463E-01        .231E-01
AREA,SQ-CM=                    1.03            .726E+00
NUMBER OF TURNS=               26.8            19
MEAN MAG LENGTH,CM=            13              10.9
PERMEABILITY=                  64.8            77.1
WEIGHT,GRAM=                   279             166
VOLUME CU-CM=                  55.8            33.2
DISSIPATION WATTS=             1.39            .826E+00
RESISTANCE OHMS=               .436E-02        .259E-02

CAPACITANCE(C1,C2),UF=         .924E+04        920
WEIGHT,GRMS=                   415             .198E+04
VOLUME,CU-CM=                  .108E+04        .14E+04

 RESISTANCE(R1),OHMS=          .105E+00

TOTAL WEIGHT,GRMS,LBS=         .284E+04        6.26
TOTAL VOL,CU-CM,IN-CU=         .257E+04        157
TOTAL DISSIPATION,WATTS=       2.22
EFFICIENCY,%=                  .443E+00
```

Frequency = 1.5 KHZ

```
INDUCTANCE(L1,L2),MH=          .615E-01        .308E-01
AREA,SQ-CM=                    1.18            .837E+00
NUMBER OF TURNS=               30.9            21.9
MEAN MAG LENGTH,CM=            14              11.7
PERMEABILITY=                  60.4            71.8
WEIGHT,GRAM=                   346             206
VOLUME CU-CM=                  69.1            41.1
DISSIPATION WATTS=             1.72            1.02
RESISTANCE OHMS=               .539E-02        .321E-02

CAPACITANCE(C1,C2),UF=         .124E+05        .123E+04
WEIGHT,GRMS=                   555             .264E+04
VOLUME,CU-CM=                  .145E+04        .187E+04

 RESISTANCE(R1),OHMS=          .105E+00

TOTAL WEIGHT,GRMS,LBS=         .375E+04        8.27
TOTAL VOL,CU-CM,IN-CU=         .342E+04        209
TOTAL DISSIPATION,WATTS=       2.74
EFFICIENCY,%=                  .549E+00
```

Table B-1 (cont.)
Filter Design - 500 Watts

Line Voltage = 28 VDC
Frequency = 1 KHZ

| | | |
|---|---|---|
| ? 28,500,1 | | |
| INDUCTANCE(L1,L2),MH= | .926E-01 | .463E-01 |
| AREA,SQ-CM= | 1.45 | 1.03 |
| NUMBER OF TURNS= | 37.9 | 26.8 |
| MEAN MAG LENGTH,CM= | 15.5 | 13 |
| PERMEABILITY= | 54.5 | 64.8 |
| WEIGHT,GRAM= | 470 | 279 |
| VOLUME CU-CM= | 93.9 | 55.8 |
| DISSIPATION WATTS= | 2.34 | 1.39 |
| RESISTANCE OHMS= | .733E-02 | .436E-02 |
| | | |
| CAPACITANCE(C1,C2),UF= | .185E+05 | .184E+04 |
| WEIGHT,GRMS= | 829 | .396E+04 |
| VOLUME,CU-CM= | .216E+04 | .279E+04 |
| | | |
| RESISTANCE(R1),OHMS= | .105E+00 | |
| | | |
| TOTAL WEIGHT,GRMS,LBS= | .553E+04 | 12.2 |
| TOTAL VOL,CU-CM,IN-CU= | .511E+04 | 312 |
| TOTAL DISSIPATION,WATTS= | 3.73 | |
| EFFICIENCY,%= | .745E+00 | |

Table B-1 (cont.)
Filter Design - 500 Watts

Line Voltage = 120 VDC
Frequency = 20 KHZ

```
? 120,500,20
INDUCTANCE(L1,L2),MH=          .704E-01        .352E-01
AREA,SQ-CM=                    .221E+00        .156E+00
NUMBER OF TURNS=               44.3            31.3
MEAN MAG LENGTH,CM=            6.04            5.08
PERMEABILITY=                  78.1            92.9
WEIGHT,GRAM=                   27.9            16.6
VOLUME CU-CM=                  5.57            3.31
DISSIPATION WATTS=             .444E+00        .264E+00
RESISTANCE OHMS=               .256E-01        .152E-01


CAPACITANCE(C1,C2),UF=         140             11.2
WEIGHT,GRMS=                   21.5            112
VOLUME,CU-CM=                  56.2            84.6


 RESISTANCE(R1),OHMS=          1.05


TOTAL WEIGHT,GRMS,LBS=         178             .392E+00
TOTAL VOL,CU-CM,IN-CU=         150             9.14
TOTAL DISSIPATION,WATTS=       .708E+00
EFFICIENCY,%=                  .142E+00
```

Frequency = 19 KHZ

```
INDUCTANCE(L1,L2),MH=          .716E-01        .358E-01
AREA,SQ-CM=                    .223E+00        .158E+00
NUMBER OF TURNS=               44.6            31.6
MEAN MAG LENGTH,CM=            6.06            5.1
PERMEABILITY=                  77.8            92.5
WEIGHT,GRAM=                   28.2            16.8
VOLUME CU-CM=                  5.64            3.35
DISSIPATION WATTS=             .45E+00         .268E+00
RESISTANCE OHMS=               .259E-01        .154E-01


CAPACITANCE(C1,C2),UF=         140             11.2
WEIGHT,GRMS=                   21.5            112
VOLUME,CU-CM=                  56.2            84.6


 RESISTANCE(R1),OHMS=          1.06


TOTAL WEIGHT,GRMS,LBS=         179             .394E+00
TOTAL VOL,CU-CM,IN-CU=         150             9.14
TOTAL DISSIPATION,WATTS=       .717E+00
EFFICIENCY,%=                  .143E+00
```

Table B-1 (cont.)
Filter Design - 500 Watts

Line Voltage = 120 VDC
Frequency = 18 KHZ

```
? 120,500,18
INDUCTANCE(L1,L2),MH=          .584E-01        .292E-01
AREA,SQ-CM=                    .201E+00        .142E+00
NUMBER OF TURNS=               40.3            28.5
MEAN MAG LENGTH,CM=            5.76            4.84
PERMEABILITY=                  81.9            97.4
WEIGHT,GRAM=                   24.2            14.4
VOLUME CU-CM=                  4.84            2.88
DISSIPATION WATTS=             .386E+00        .229E+00
RESISTANCE OHMS=               .222E-01        .132E-01

CAPACITANCE(C1,C2),UF=         175             16.8
WEIGHT,GRMS=                   26.9            168
VOLUME,CU-CM=                  70.3            127

 RESISTANCE(R1),OHMS=          .856E+00

TOTAL WEIGHT,GRMS,LBS=         234             .515E+00
TOTAL VOL,CU-CM,IN-CU=         205             12.5
TOTAL DISSIPATION,WATTS=       .615E+00
EFFICIENCY,%=                  .123E+00
```

Frequency = 17.5 KHZ

```
INDUCTANCE(L1,L2),MH=          .589E-01        .295E-01
AREA,SQ-CM=                    .202E+00        .143E+00
NUMBER OF TURNS=               40.5            28.6
MEAN MAG LENGTH,CM=            5.77            4.85
PERMEABILITY=                  81.7            97.1
WEIGHT,GRAM=                   24.4            14.5
VOLUME CU-CM=                  4.87            2.9
DISSIPATION WATTS=             .389E+00        .231E+00
RESISTANCE OHMS=               .224E-01        .133E-01

CAPACITANCE(C1,C2),UF=         175             16.8
WEIGHT,GRMS=                   26.9            168
VOLUME,CU-CM=                  70.3            127

 RESISTANCE(R1),OHMS=          .86E+00

TOTAL WEIGHT,GRMS,LBS=         234             .516E+00
TOTAL VOL,CU-CM,IN-CU=         205             12.5
TOTAL DISSIPATION,WATTS=       .62E+00
EFFICIENCY,%=                  .124E+00
```

Table B-1 (cont.)
Filter Design - 500 Watts

Line Voltage = 120 VDC
Frequency = 15 KHZ

```
? 120,500,15
INDUCTANCE(L1,L2),MH=          .623E-01        .311E-01
AREA,SQ-CM=                    .208E+00        .147E+00
NUMBER OF TURNS=               41.6            29.4
MEAN MAG LENGTH,CM=            5.85            4.92
PERMEABILITY=                  80.6            95.8
WEIGHT,GRAM=                   25.4            15.1
VOLUME CU-CM=                  5.08            3.02
DISSIPATION WATTS=             .405E+00        .241E+00
RESISTANCE OHMS=               .233E-01        .139E-01


CAPACITANCE(C1,C2),UF=         175             16.8
WEIGHT,GRMS=                   26.9            168
VOLUME,CU-CM=                  70.3            127


 RESISTANCE(R1),OHMS=          .884E+00


TOTAL WEIGHT,GRMS,LBS=         235             .519E+00
TOTAL VOL,CU-CM,IN-CU=         205             12.5
TOTAL DISSIPATION,WATTS=       .646E+00
EFFICIENCY,%=                  .129E+00
```

Frequency = 12.5 KHZ

```
INDUCTANCE(L1,L2),MH=          .668E-01        .334E-01
AREA,SQ-CM=                    .215E+00        .152E+00
NUMBER OF TURNS=               43.1            30.5
MEAN MAG LENGTH,CM=            5.96            5.01
PERMEABILITY=                  79.2            94.1
WEIGHT,GRAM=                   26.8            15.9
VOLUME CU-CM=                  5.35            3.18
DISSIPATION WATTS=             .427E+00        .254E+00
RESISTANCE OHMS=               .246E-01        .146E-01


CAPACITANCE(C1,C2),UF=         175             16.8
WEIGHT,GRMS=                   26.9            168
VOLUME,CU-CM=                  70.3            127


 RESISTANCE(R1),OHMS=          .916E+00


TOTAL WEIGHT,GRMS,LBS=         238             .524E+00
TOTAL VOL,CU-CM,IN-CU=         206             12.6
TOTAL DISSIPATION,WATTS=       .681E+00
EFFICIENCY,%=                  .136E+00
```

Table B-1 (cont.)
Filter Design - 500 Watts

Line Voltage = 120 VDC
Frequency = 10 KHZ

| | | |
|---|---|---|
| ? 120,500,10 | | |
| INDUCTANCE(L1,L2),MH= | .698E-01 | .349E-01 |
| AREA,SQ-CM= | .22E+00 | .156E+00 |
| NUMBER OF TURNS= | 44.1 | 31.2 |
| MEAN MAG LENGTH,CM= | 6.02 | 5.06 |
| PERMEABILITY= | 78.3 | 93.1 |
| WEIGHT,GRAM= | 27.7 | 16.5 |
| VOLUME CU-CM= | 5.53 | 3.29 |
| DISSIPATION WATTS= | .441E+00 | .262E+00 |
| RESISTANCE OHMS= | .254E-01 | .151E-01 |
| CAPACITANCE(C1,C2),UF= | 245 | 22.4 |
| WEIGHT,GRMS= | 37.7 | 224 |
| VOLUME,CU-CM= | 98.4 | 169 |
| RESISTANCE(R1),OHMS= | .791E+00 | |
| TOTAL WEIGHT,GRMS,LBS= | 306 | .674E+00 |
| TOTAL VOL,CU-CM,IN-CU= | 276 | 16.9 |
| TOTAL DISSIPATION,WATTS= | .704E+00 | |
| EFFICIENCY,%= | .141E+00 | |

Frequency = 7.5 KHZ

| | | |
|---|---|---|
| INDUCTANCE(L1,L2),MH= | .109E+00 | .543E-01 |
| AREA,SQ-CM= | .274E+00 | .194E+00 |
| NUMBER OF TURNS= | 55 | 38.9 |
| MEAN MAG LENGTH,CM= | 6.73 | 5.66 |
| PERMEABILITY= | 70.1 | 83.4 |
| WEIGHT,GRAM= | 38.6 | 22.9 |
| VOLUME CU-CM= | 7.71 | 4.58 |
| DISSIPATION WATTS= | .615E+00 | .366E+00 |
| RESISTANCE OHMS= | .354E-01 | .211E-01 |
| CAPACITANCE(C1,C2),UF= | 280 | 28 |
| WEIGHT,GRMS= | 43.1 | 280 |
| VOLUME,CU-CM= | 112 | 212 |
| RESISTANCE(R1),OHMS= | .923E+00 | |
| TOTAL WEIGHT,GRMS,LBS= | 385 | .848E+00 |
| TOTAL VOL,CU-CM,IN-CU= | 336 | 20.5 |
| TOTAL DISSIPATION,WATTS= | .98E+00 | |
| EFFICIENCY,%= | .196E+00 | |

Table B-1 (cont.)
Filter Design - 500 Watts

Line Voltage = 120 VDC
Frequency = 5 KHZ

```
? 120,500,5
INDUCTANCE(L1,L2),MH=          .15E+00        .752E-01
AREA,SQ-CM=                    .323E+00       .228E+00
NUMBER OF TURNS=               64.7           45.7
MEAN MAG LENGTH,CM=            7.3            6.14
PERMEABILITY=                  64.6           76.8
WEIGHT,GRAM=                   49.3           29.3
VOLUME CU-CM=                  9.84           5.85
DISSIPATION WATTS=             .785E+00       .467E+00
RESISTANCE OHMS=               .452E-01       .269E-01

CAPACITANCE(C1,C2),UF=         455            44.8
WEIGHT,GRMS=                   70             448
VOLUME,CU-CM=                  183            339

 RESISTANCE(R1),OHMS=          .852E+00

TOTAL WEIGHT,GRMS,LBS=         597            1.32
TOTAL VOL,CU-CM,IN-CU=         537            32.8
TOTAL DISSIPATION,WATTS=       1.25
EFFICIENCY,%=                  .25E+00
```

Frequency = 2 KHZ

```
INDUCTANCE(L1,L2),MH=          .394E+00       .197E+00
AREA,SQ-CM=                    .523E+00       .37E+00
NUMBER OF TURNS=               105            74.1
MEAN MAG LENGTH,CM=            9.28           7.81
PERMEABILITY=                  50.8           60.4
WEIGHT,GRAM=                   101            60.3
VOLUME CU-CM=                  20.3           12.1
DISSIPATION WATTS=             1.62           .961E+00
RESISTANCE OHMS=               .931E-01       .554E-01

CAPACITANCE(C1,C2),UF=         .109E+04       106
WEIGHT,GRMS=                   167            .106E+04
VOLUME,CU-CM=                  436            804

 RESISTANCE(R1),OHMS=          .893E+00

TOTAL WEIGHT,GRMS,LBS=         .139E+04       3.07
TOTAL VOL,CU-CM,IN-CU=         .127E+04       77.6
TOTAL DISSIPATION,WATTS=       2.58
EFFICIENCY,%=                  .516E+00
```

Table B-1 (cont.)

Filter Design - 500 Watts

Line Voltage = 120 VDC
Frequency = 1 KHZ

```
? 120,500,1
INDUCTANCE(L1,L2),MH=          .801E+00        .401E+00
AREA,SQ-CM=                    .745E+00        .527E+00
NUMBER OF TURNS=               149             106
MEAN MAG LENGTH,CM=            11.1            9.32
PERMEABILITY=                  42.5            50.6
WEIGHT,GRAM=                   173             103
VOLUME CU-CM=                  34.5            20.5
DISSIPATION WATTS=             2.75            1.64
RESISTANCE OHMS=               .159E+00        .943E-01

CAPACITANCE(C1,C2),UF=         .213E+04        213
WEIGHT,GRMS=                   328             .213E+04
VOLUME,CU-CM=                  857             .161E+04

 RESISTANCE(R1),OHMS=          .908E+00

TOTAL WEIGHT,GRMS,LBS=         .273E+04        6.02
TOTAL VOL,CU-CM,IN-CU=         .252E+04        154
TOTAL DISSIPATION,WATTS=       4.39
EFFICIENCY,%=                  .878E+00
```

Table B-2. PWM Input Filter Design

```
100 *INFLDES-PWM INPUT FILTER DESIGN
110 PRINT "ENTER LINE VOLTAGE,VOLTS;POWER,WATTS;FREQ,KCS
120 INPUT E1,P4,F0
130 I1=P4/E1
140 E2=.055*E1+3.333
150 J=E1
160 E1=1.25*E1
170 IF E1>400 THEN 1420
180 T=E1
190 E1=1.2*E1
200 IF E1>400 THEN 400
210 IF E1>375 THEN 420
220 RESTORE 440
230 IF E1>300 THEN 420
240 RESTORE 450
250 IF E1>250 THEN 420
260 RESTORE 460
270 IF E1>200 THEN 420
280 RESTORE 470
290 IF E1>150 THEN 420
300 RESTORE 480
310 IF E1>100 THEN 420
320 RESTORE 490
330 IF E1>75 THEN 420
340 RESTORE 500
350 IF E1>60 THEN 420
360 RESTORE 510
370 IF E1>50 THEN 420
380 RESTORE 520
390 GO TO 420
400 Y=400-T
410 PRINT "C2 SURGE VOLTAGE MARGIN,VOLTS    =";Y
420 READ X1,C1,E5,C2,E6,W1,W2
430 DATA 1,6,450,3,400,2.747,65
440 DATA 2,12,375,3,400,4.214,65
450 DATA 3,18,300,3,400,4.214,65
460 DATA 4,30,250,3,400,5.385,65
470 DATA 5,35,200,5.6,200,5.385,56
480 DATA 6,47,150,5.6,200,5.385,56
490 DATA 7,70,100,10,100,5.385,56
500 DATA 8,88,75,10,100,5.385,56
510 DATA 9,100,60,10,100,5.385,56
```

Table B-2 (cont.)

```
520 DATA 10,120,50,10,50,5.385,21.5
530 V1=2.61*W1
540 V2=.787*W2-1.75
550  C5=(1000*I1)/(2*F0*E2)
560  M=INT(C5/C2+1)
570  C2=M*C2
580  E2=(1000*I1)/(2*F0*C2)
590  I2=1.273*I1
600  I3=I1/10
610  IF F0<J/10 THEN 630
620  I3=I3*((J/(10*F0))↑2.72)
630  A=I2/I3
640  B=(29.64*A)↑(1/3)+.988
650  F1=F0/B
660  C6=10*C2
670  K=INT(C6/C1+.999)
680  C1=K*C1
690  L1=1000/(C1*((6.28*F1)↑2))
700  L2=L1/2
710  C=1.482
720  Z=1000*L1/C1
730  R1=1.482*SQRT(Z)
740 V1=K*V1
750 V2=M*V2
760 W1=K*W1
770 W2=M*W2
780 I=I1
790 L=L1/1000
800 G=1
810 GO TO 840
820 L=L2/1000
830 GO TO 840
840  A1=300*(I1↑1.4)
850 A2=A1
860 B=.3
870 F1=.3
880 A1=A1*5.067E-10
890 D1=8.94E3
900 D2=8.4E3
910 F2=2
920 S=((1+(12*F2*F1*D1)/D2)↑.5)-1
930 R=(L*I*A1)/(8*3.1416*F1)
```

## Table B-2 (cont.)

```
940 T=1/(S↑.5)+(S↑.5)/6
950 A=(R↑.5)*S/3
960 N(G)=(3/S)*(((L*I*3.1416*F1)/(A1*B))↑.5)
970 Z=10.8828*(R↑.25)*T
980 U=3.5276*((9/I)↑(5/4))*((A1/(3.1416*F1))↑(3/4))*(1/(L↑.25))*S*T
990 W=3.5276*D1*(R↑(3/4))*(1/(S↑.5))*(6*F2*F1+(D2/D1)*(S+(S↑2)/6))
1000 A(G)=A*1E4
1010 Z(G)=Z*1E2
1020 U(G)=U*(1/(4*3.1416*1E-7))
1030 W(G)=W*1E3
1040 V(G)=(Z(G)↑3)/39.48
1050 R(G)=2.72*N(G)*(A(G)↑.5)/A2
1060 P(G)=(I↑2)*R(G)
1070 G=G+1
1080 ON G-1 GO TO 820,1090
1090 W5=W(1)+W(2)+W1+W2
1100 W6=W5/453.6
1110 V5=V(1)+V(2)+V1+V2
1120 V6=V5/16.39
1130 P5=P(1)+P(2)
1140 Q=100*P5/P4
1150 L(1)=L1
1160 L(2)=L2
1170 SIGNIFICANCE 3
1180 PRINT #INDUCTANCE(L1,L2),MH=  #,L(1),L(2)
1190 PRINT #AREA,SQ-CM=            #,A(1),A(2)
1200 PRINT #NUMBER OF TURNS=       #,N(1),N(2)
1210 PRINT #MEAN MAG LENGTH,CM=    #,Z(1),Z(2)
1220 PRINT #PERMEABILITY=          #,U(1),U(2)
1230 PRINT #WEIGHT,GRAM=           #,W(1),W(2)
1240 PRINT #VOLUME CU-CM=          #,V(1),V(2)
1250 PRINT #DISSIPATION WATTS=     #,P(1),P(2)
1260 PRINT #RESISTANCE OHMS=       #,R(1),R(2)
1270PRINT#                #
1280 PRINT#    #
1290 PRINT#CAPACITANCE(C1,C2),UF=  #,C1,C2
1300 PRINT#WEIGHT,GRMS=            #,W1,W2
1310 PRINT#VOLUME,CU-CM=           #,V1,V2
1320 PRINT#  #
1330 PRINT#  #
1340 PRINT# RESISTANCE(R1),OHMS=   #,R1
1350 PRINT #
```

## Table B-2 (cont.)

```
1360 PRINT E
1370 PRINTETOTAL WEIGHT,GRMS,LBS=   E,W5,W6
1380 PRINTETOTAL VOL,CU-CM,IN-CU=   E,V5,V6
1390 PRINTETOTAL DISSIPATION,WATTS=E,P5
1400 PRINTEEFFICIENCY,E=            E,Q
1410 GO TO 1430
1420  RINT END CAP IN FILE FOR THIS VOLTAGEE
1430 END
```