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LARGE-AREA CCD IMAGERS FOR SPACECRAFT APPLICATIONS*

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Backside illuminated CCD imagers with 100 X 160 resolution elements have been fabricated using double-level metal technology. Detailed study of the optical performance of such arrays has been performed between 24° C and -40° C using data rates from 10 kHz to 1 MHz. A 400 X 400 array is presently being fabricated.

I. INTRODUCTION

Large-area charge-coupled device (CCD) imagers can be fabricated with any of several existing technologies (Refs. 1, 2, 3). Since a completely sealed electrode structure is very desirable to optimize device electrical performance, many arrays use polysilicon electrodes which are sufficiently transparent to allow optical radiation to enter the active region of the CCD. Electrode absorption and interference effects related to the device structure itself can result in a degradation of the optical performance, particularly at short wavelengths. Illumination of the CCD from the backside (Ref. 4) eliminates this problem but requires that the silicon chip be thinned to about 10 μm for optimum performance. This paper will discuss the characteristics of backside illuminated, three-phase (3 ϕ) (Ref. 5), buried-channel imagers fabricated using the double-level anodized aluminum technique (Ref. 6). A completely sealed structure with high charge transfer efficiency (CTE) and optimum optical responsivity is obtained. The electrical and optical performance of arrays with 160 × 100 resolution elements will be presented to confirm that this technology can be successfully

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applied to fabricate high-performance CCD imagers. The unique aspects of the double-level, backside illuminated structure will be discussed with emphasis on a 400 × 400 array presently being fabricated.

II. DESIGN AND FABRICATION

The 160 × 100 imager is an n-channel device designed to have a resolution element size of 0.9 × 0.9 mil^2. The organization is serial-parallel-serial, which allows the input of electrical signals to the parallel section. A double-level aluminum metallization separated by approximately 2500-Å $A\ell_2O_3$ forms the transfer electrode structure. Three-phase clocking is used so that in both the parallel and serial sections of the array a given phase occurs alternately on first-level and second-level metal electrode (Ref. 5). The signal charge packets are transferred to the (ϕ_3) output serial register electrodes through a composite gate region of width 0.3 mil. Overlap of first- and second-level electrodes is nominally 0.05 mil to achieve a 0.9 × 0.9 pixel. This requirement places extremely tight tolerances on photomask perfection, particularly for 400 × 400 size arrays.

An output amplifier is provided for both upper and lower serial registers to allow forward or reverse operation of the imager. This can increase array yield in the event of a malfunction of one amplifier. A balanced sample-and-hold design takes the precharge output from a source follower through a sampling MOSFET and to a second source follower, giving an amplifier bandwidth greater than 10 MHz. On-chip load MOSFETs are used in this design. A correlated clamping circuit is provided at the upper serial output to investigate on-chip low-noise video processing. This amplifier has a bandwidth of about 1 MHz. A micrograph of the 325 × 325 mil^2 chip is shown in Figure 1. Bond pads are extended some 50 mils from the active area so they remain over the thick silicon after a region slightly bigger than the array itself (90 × 144 mil^2) has been thinned. Thinning was performed by chemical etching either after the individual chips had been mounted on ceramic 40-pin headers or by etching a whole slice using an etch mask around each individual array. In this latter case, the slice was then scribed into individual chips and each subsequently mounted on headers. Either technique can provide uniformly thin membranes of thickness 10-12 μm. The surface of the membrane is highly reflective, although a light surface haze is sometimes found after removal from the etch. Membrane

stability is such that repeated temperature cycles from 24° C to -40° C do not fracture the CCD. Distortion of the membrane is observed in some cases at -40° but can be minimized by avoiding temperature gradients.

The imagers were operated in the full frame mode, and the readout sequence occurred while light was incident on the device. To reduce streaking in the displayed image, the ratio of integration time to readout time should be $\gtrsim$3:1, and a 5-second exposure at an output rate of 10 kHz (1.6-second readout) was used at -40°. A shuttered mode of operation is simulated by illuminating with a short light pulse during the integrate period only, and the imagery of a 160 X 100 operating in this mode at 24° C is shown in Figure 2.

High charge transfer efficiency is achieved by using a phosphorus implantation to achieve a 0.5-1.0 μm deep buried channel in nominally 10 Ω-cm p-type silicon. Typical buried-channel arrays operate at 6-8 volt clocks with a CTE of ≥0.9999 (measured in the serial register) with no electrically introduced fat zero. Equally good CTE in the parallel section is inferred from the square-wave amplitude response (SWAR) data discussed below. It does not appear that the transfer gate region to the output serial register is affecting array performance.

III. IMAGER CHARACTERISTICS

The successful incorporation of the CCD imager into a spacecraft system will require that a given array meet many performance specifications. High CTE and spectral responsivity must be combined with a low blemish count and dark current. Uniformity of both responsivity and dark current are very desirable. The arrays discussed in this paper are intended for operation at long exposure times and a 10-kHz data rate at -40° C. Array dark current is expected to decrease with the temperature T at $T^{3/2} \exp(-E_g/2kT)$ or a factor of 895 between 24° C and -40° C. Storage times of $\gtrsim$200 seconds should therefore be possible at -40° C without appreciable filling of the potential wells.

Performance parameters of two buried-channel 160 X 100 arrays are indicated in Table 1. The consistent achievement of high CTE requires tight control over substrate resistivity and implant dose to achieve the desired buried channel. Any metallization defects, particularly in the serial output registers, will also degrade CTE from the optimum for the buried channel. Using a voltage contrast mode with a scanning electron microscope allows correlation of

such defects with array CTE and allows processing optimization. There does not appear to be any significant effect of temperature (25° C to -40° C) or frequency (10 kHz to 1 MHz) on the measured transfer efficiency.

The dark current I_D of the buried-channel arrays is in the range 10-20 nA/cm^2 at room temperature as measured by a picoammeter in the precharge line of the output amplifier. While this method of measurement is generally reliable at 25° C, it fails completely at lower temperatures, where I_D becomes lower than the CCD leakage currents. Our measurements (Table 1) at -40° C are taken using an integration technique that allows the dark current to build up over a long period (~200 seconds at -40° C) to give a significant well population which results in an easily measured video voltage output. The CCD/amplifier is calibrated using a (large) current injected at the input diode in a separate measurement. This technique gives a decrease of 1000× between 24° C and -40° C in satisfactory agreement with that predicted above. In contrast, the precharge technique gives a decrease of 80-100, which merely reflects the degree of spurious dc leakage current from the CCD and ceramic package.

One advantage of the backside illuminated mode is high responsivity and smooth spectral responsivity (Figure 3). The log-log plot of signal current versus incident power has a slope (γ) of 1 ±0.1 under all operating conditions. The wideband responsivity to 2854-K radiation with no AR coating is 90 mA/watt with a 70% quantum efficiency at 4000 Å. Decreasing temperature to -40° appears to decrease the responsivity at all wavelengths below about 6000 Å by about 30% as measured on a device with peak QE of 40% at 8000 Å. This effect may be related to a change in surface recombination velocity and suggests that a passivation layer or antireflection coating be applied to the thin membrane surface. For a 100-μJ/m^2 exposure at the array during a 5-second exposure time, the ratio of signal to dark current (-40° C) implied by the data is 18.6 for 2854° radiation.

The squarewave amplitude response of the imager taken with a high-contrast bar chart is shown in Figure 4 out to the Nyquist frequency f_N = 21.9 line pairs/mm. The results in Figure 4 were taken at 1 MHz and -40° C, since detailed comparisons at 10 kHz (where data is less accurate) and 24° and -40° show no consistent change in the SWAR. This result would indicate that any distortion of the thin CCD membrane at -40° C is not sufficient to affect device resolution. High array CTE is reflected by measuring a constant SWAR across

the array (Figure 4), and only a very small SWAR loss can be attributed to CTE degradation. At f_N, the SWAR is 40% and 30% for bars parallel and perpendicular respectively to the serial register. The lower value for perpendicular bars is due to a bandwidth limitation in the external electronics in the 1-MHz data and is not a CCD effect. Without this limitation (device II), the SWAR for parallel bars is found to be 0.04 below the perpendicular value.

An estimate of the SWAR for device I can be made as follows: Using a substrate resistivity of 5 Ω-cm, and a buried-channel dose of 1.5×10^{12} cm^{-2} and drive-in of $2\sqrt{Dt} = 0.6$ μm, where D = diffusion coefficient for implanted phosphorus and t = drive time, one can calculate the depletion layer width to be 3.2 μm from the SiO_2-Si interface for 8-volt clocks. If the substrate has been thinned to 10 μm, this results in a neutral bulk layer thickness of 6.8 μm. By first substituting these values into the Crowell-Labuda formula (Ref. 7) for diffusion MTF, which has been shown by Seib (Ref. 8) to be an adequate approximation to the CCD case in essentially all instances; next, multiplying by the pixel collection aperture MTF ($\sin \pi fd/\pi fd$, d = pixel pitch = 0.0229 mm) and the lens MTF; and finally, substituting this total MTF function, $R_o(f)$, into the formula for SWAR,

$$SWAR(f) = \frac{4}{\pi} \sum_{m=0}^{\infty} \frac{(-1)^m}{2m+1} R_o[(2m+1)f]$$

one finds the SWAR at the Nyquist limit (f_N = 21.9 lp/mm) to be 0.53 for illumination having a 0.8-μm wavelength, the wavelength of peak sensor response. This is somewhat above the experimental value of 0.40 but possibly results from the monochromatic assumption in the model.

Isolated light blemishes in the arrays have been reduced to a low level by bulk gettering and annealing processes (Figure 2). Bulk lifetimes after processing are ~50 μsec, and interface states at the Si-SiO_2 boundary are $\lesssim 10^{10}/cm^2$-eV. However, the uniformity of response to 2854-K illumination has been found to depend on the thinning process itself. Nonuniform thinning can result in bands of higher (or lower) sensitivity, which in some cases correlate with a light surface haze remaining after the chemical thinning. The uniformity of the imager response (and also of dark current) is determined by sampling each pixel video

with a multichannel analyzer, and is defined as the standard deviation divided by the mean. This parameter is equal to 0.19 at 5% of full well and 0.14 at 50% of full well for a 2854-K source measured at 10 kHz and -40° C. Uniformity of 0.08 both for 2854-K and 4000-Å radiation at 24° C have been measured in a device at the 20% saturation level (Table 1). Uniformity of dark current is 0.96 at -40° C and 10 kHz. Device II is more uniform at 24° C but degrades at low temperature. It should be noted however that the array dark uniformity is affected by an apparent heating effect in the membrane from the on-chip load MOSFETs.

Preliminary measurements of dynamic noise of isolated pixels using the balanced sample-and-hold amplifier indicated about 400 electrons of noise at 1 MHz and -40° C, which is considerably higher than expected from a buried-channel device. More recent results (Ref. 9) using improved measurement technique indicate a noise as low as 67 electrons at 24° C and 1 MHz. However, even with a noise level of 400 electrons, the dynamic range of the imager is 3500:1 (full well 1.6×10^6 electrons with 7-volt clocks).

IV. DISCUSSION AND CONCLUSIONS

The performance of the 160 X 100 arrays appears sufficiently promising to allow fabrication of a larger 3 ϕ, double-level imager of similar basic design. Fabrication of this array is in progress, and several problems peculiar to this 0.5 X 0.5 chip have become apparent. Photomask perfection is extremely difficult to maintain over such large areas, and a single defect in a metal level mask can cause a fatal intralevel metal short in the array. This problem can be minimized in slice processing but at the expense of additional steps. The integrity of gate oxide is important, since a 400 X 400 will have 101,000 mil^2 of thin oxide. Defect (pinhole) levels of <0.5 cm^2 have been observed on test slices using dry-wet-dry or HCl doped oxides. The integrity of anodic Al_2O_3 is well recognized, but pinholes do exist and will give rise to interlevel shorts. This effect is minimized by the 0.05-mil overlap, but care must be exercised to maintain some overlap in order to allow buried-channel operation. These yield loss mechanisms are all expected to be of prime importance for the 400 X 400. The performance of such an array is expected to be comparable to that of the 160 X 100. Uniformity of thinning and membrane planarity for areas near 1 cm^2 may require further development, and some form of support for the membrane may be necessary to maintain planarity. The uniformity of response and of dark

current may also depend on silicon slice perfection and the effectiveness of bulk gettering over extended areas.

In conclusion, the results presented have shown that the double-level anodized aluminum technique can be used to fabricate high-performance 3 ϕ CCD imagers which operate at reduced temperatures and 10-kHz data rates.

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Table 1. Performance parameters of two buried-channel 160 × 100's

	I	II
CTE	0.9999 (7-V clocks)	>0.9999
Saturation level	1.6×10^6 electrons at 7 V	2×10^6 electrons
Dark current	0.0078 nA/cm^2 (-40° C)	–
	7.8 nA/cm^2 (+24° C)	6.5 nA/cm^2
Responsivity (2854 K)	90 mA/watt (24° C)--No AR coating	99 mA/watt
Quantum efficiency (4000 Å)	70% (24° C)	10% (24° C)
SWAR		
Parallel to serial	40%	37%
Perpendicular to serial	29%*	41%
Signal to dark current ratio (100-μJ/m^2 exposure for 5 sec at -40° C)	18.6	–
Response uniformity	0.14 (-40° C)	0.08 (24° C)
	50% full well	20% full well
Dark uniformity	0.96 (-40° C)	0.24 (24° C)

*Electronic limitation.

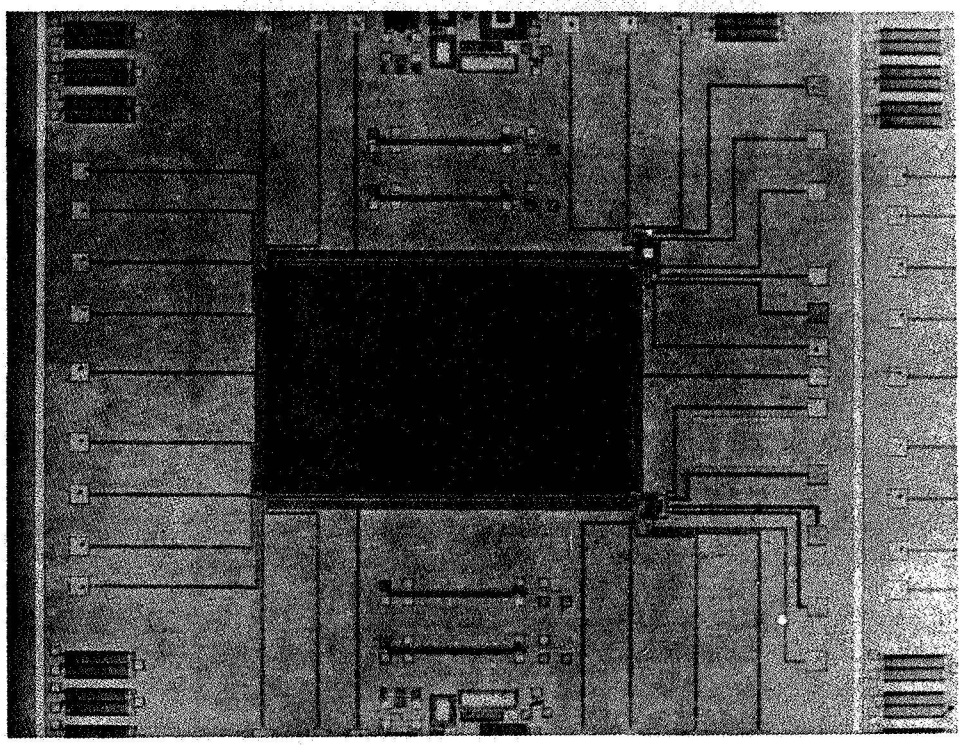

Figure 1. Photomicrograph of 160 × 100 CCD imager (Active area is 144 × 90 mil^2 and total chip is 322 × 325 mil^2.)

160 x 100 BURIED CHANNEL IMAGER

DATA RATE 1 MHz
TEMPERATURE 22°C
ILLUMINATION STROBED

Figure 2. Imagery at 24°C with buried-channel array using a strobed source to simulate shuttered operation

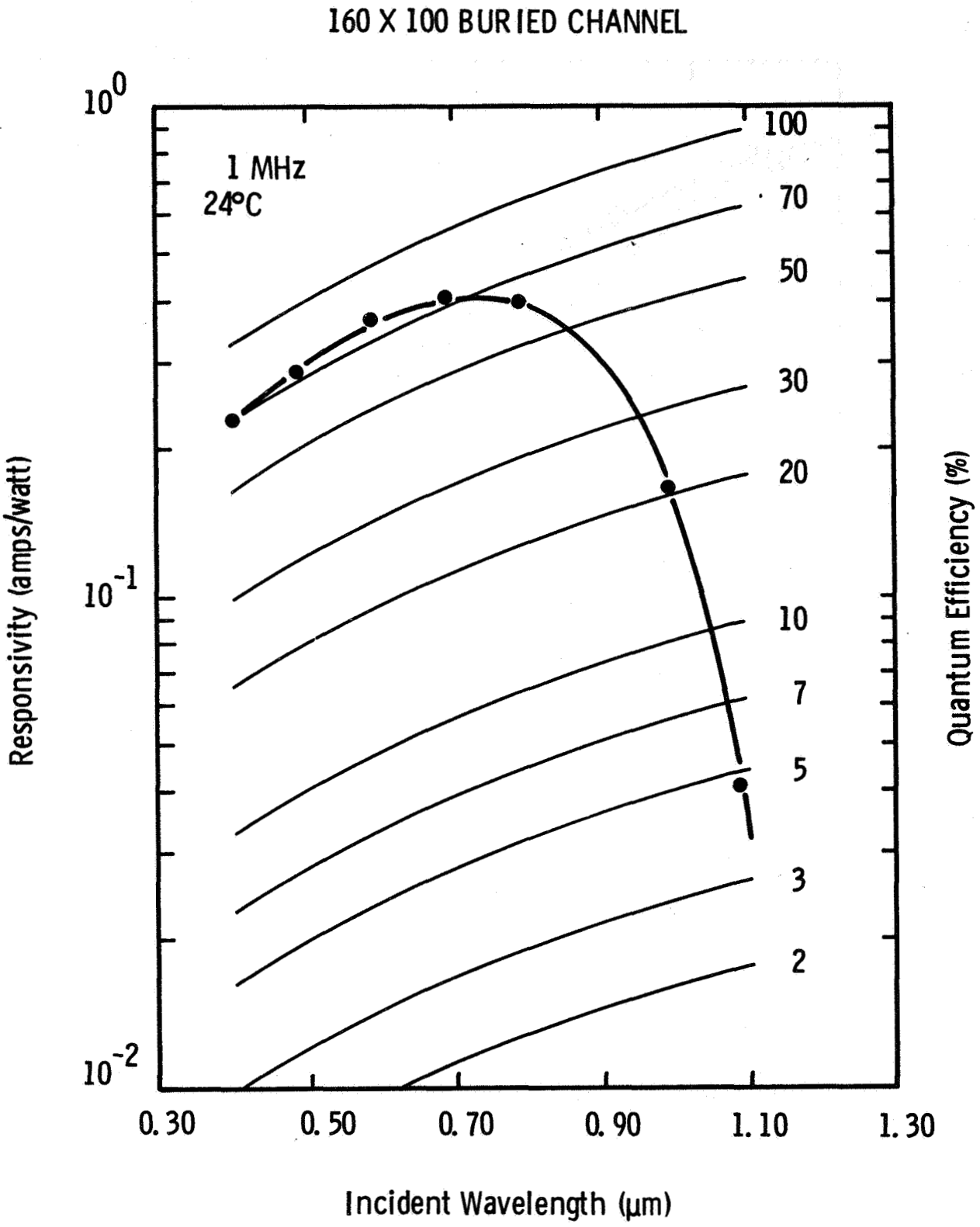

Figure 3. Spectral responsivity of 160 × 100 array (At -40°, there is an apparent decrease in responsivity below about 6000 Å by about 30%.)

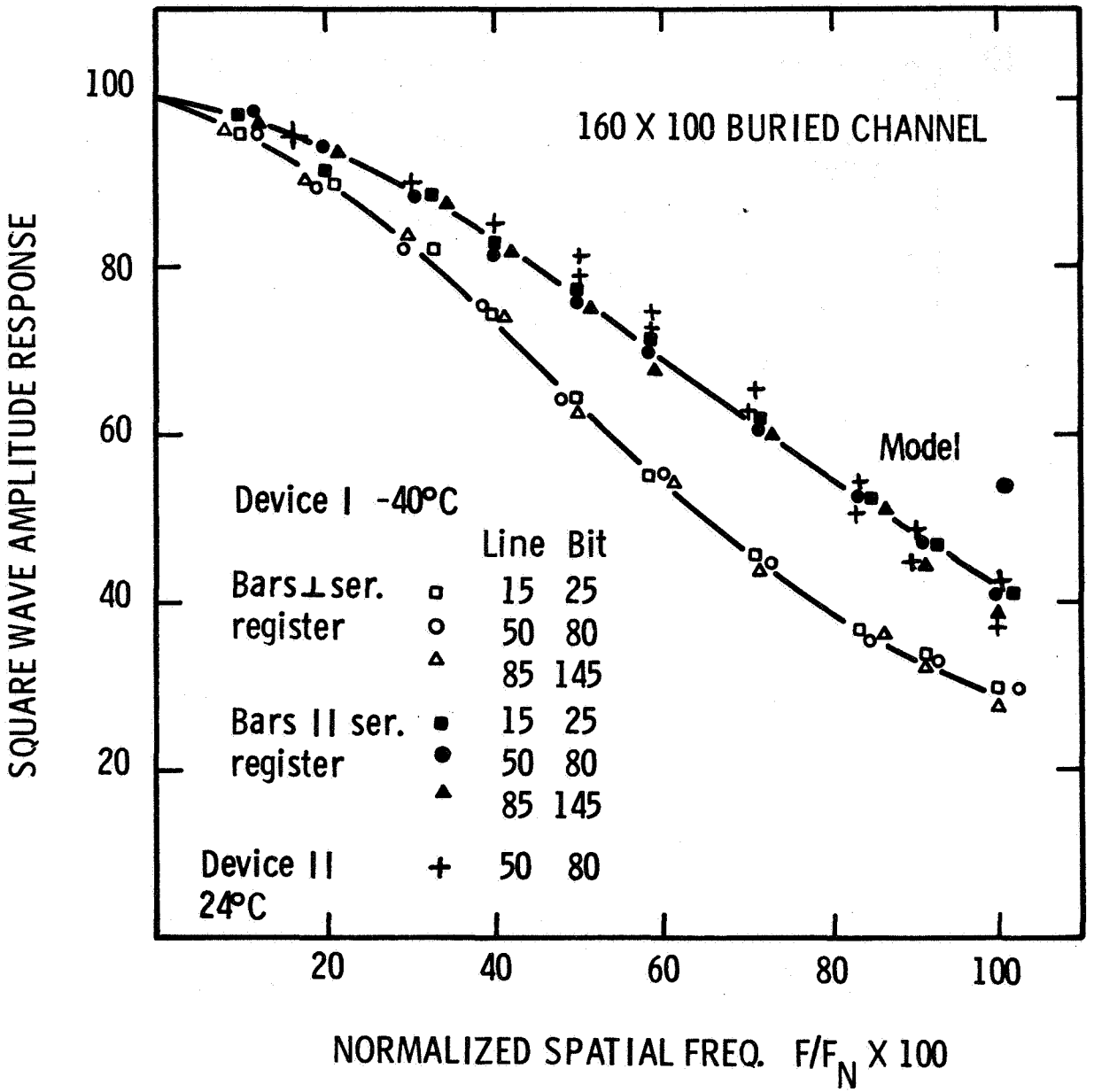

Figure 4. Squarewave amplitude response using a high-contrast bar chart (Essentially no change across the array is observed. The corrected value at the Nyquist frequency indicates the theoretical model for SWAR discussed in the text for device I.)