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# A 190 × 244 CHARGE-COUPLED AREA IMAGE SENSOR WITH INTERLINE TRANSFER ORGANIZATION

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A 190 × 244 element charge-coupled area image sensor has been designed, fabricated and tested. This sensor employs an interline transfer organization and buried n-channel technology. It features a novel on-chip charge integrator and a distributed floating-gate amplifier for high and low light level applications. The X-Y element count has been chosen to establish the capability of producing an NTSC-compatible video signal. The array size is also compatible with the Super-8 lens format.

The first few sample devices have been successfully operated at full video bandwidth for both high and low light levels with the charge amplifier system.

## I. DEVICE ARCHITECTURE

The successful development at Fairchild in 1973 of the CCD-201, a 100 × 100 element CCD area imaging device, led to the decision to follow it with a larger structure based on essentially the same design philosophy. This device is a 190 × 244 element buried-channel charge-coupled area imager designed with interline transfer organization and using topside illumination. The element count on the 190 × 244 was chosen to establish compatibility with the Fairchild type 3261 sync generator in order to facilitate the generation of TV compatible video. The X-Y format was selected to approximate that of the Super-8 movie camera. With the interline transfer organization employed, 50% of the imaging area is photosensitive.

Figure 1 shows a functional layout of the device. The area array portion is similar in architecture to that of the CCD-201, except for the number of elements involved and a higher packing density. There are 190 vertical register columns in the array, one corresponding to each column of photosensors. The vertical registers are of the $2\phi$ implanted barrier type. Their outputs parallel-couple into a high-speed output register which drives the amplifier system. Another high-speed register is located at the opposite end of the area array and permits the circulation of electrical information through the array. Both the input and output registers are of the four-phase type.

The amplifier section contains four separate amplifiers, enabling one to make sensitive performance comparisons between them. These amplifiers are (1) a gated charge integrator (GCI), (2) a distributed floating-gate amplifier (DFGA), (3) an input floating-gate amplifier (FGA1) located at the input to the DFGA and (4) an output floating-gate amplifier (FGA2) located at the end of the input channel of the DFGA. There are two charge steering gates, one located at the input to the GCI and the other at the floating-gate devices so that the array output can be channeled through either system.

A view of the 190 × 244 die is shown in Figure 2. It contains 33 bonding pads. The pad count is not minimal but reflects the desire to have maximum operating flexibility for the evaluation of the amplifiers. The die size is 248 × 242 mils. One of the design objectives was to constrain both the X and Y dimensions to ≤250 mils so that the masks would not have to be photocomposed. This resulted in the necessity to fold back the output register so that the amplifiers used space in the Y direction.

Figure 3 shows the portion of the output register which interfaces with the amplifier structure. Photo carriers are integrated at photosites 'A' for one frame time and moved to vertical register sites 'B' during one field and to sites 'C' during the next field. All vertical register columns are clocked simultaneously, transferring a row of data to the output register at the end of each horizontal scanning line.

## II. AMPLIFIER DESIGN

In Figure 3, two separate control gates are shown (shaded) which enable one to direct charges either to the GCI or to the DFGA channel itself. This channel was made approximately half the size of the output channel so that noise could be minimized. This sacrifice in charge handling ability was justified on the basis that the DFGA is primarily designed for low light level operation. A useful feature of this layout is that excess charge occurring while the DFGA is being used can be drained off to the GCI; therefore the GCI can function as a saturation control. Also it should be noted that DFGA analysis can be facilitated by injecting signals electrically into the DFGA through the reset circuit.

The GCI structure consists of an MOS signal amplifier and a reset circuit for resetting the amplifier gate after each charge packet has been sampled. In addition, there is a compensation amplifier, which does not receive the signal but is subjected to the reset transients seen by the signal amplifier. By taking the difference between the two outputs in an external amplifier, reset transients can be suppressed.

The theory and operation of the DFGA have been discussed previously (Ref. 1). In summary, the operation of a single floating-gate amplifier is based on the principle that the signal charge of a CCD channel can be nondestructively sensed by a floating-gate electrode. In a distributed floating-gate amplifier, the same signal charge is repeatedly sensed, thereby increasing the signal-to-noise power ratio by a factor equal to the number of times it is detected.

Figure 4 shows a view of the floating-gate amplifier system. Charge packets are transferred into the floating-gate input channel from the area array output register where they are first sensed by FGA1. As they are clocked through the input channel, they are subsequently sensed by the 12 floating-gate structures associated with the DFGA. Finally, they are detected by another single floating-gate amplifier (FGA2) and then terminate in a sink at the end of the channel.

Each of the twelve floating gates modulates its source-drain current, which flows under the large gates in the DFGA output channel. Charges clocked through the output channel are detected by a large floating gate at the end, which couples it to a large single floating-gate amplifier, designated FGA3. The current which flows into the output channel is under the control of a gate clocked at the data rate running between the two. Adjacent to it is a second gate, which is dc biased to reduce transient coupling from the clocked gate to the input channel.

## III. PHOTOCELL DESIGN

A plan view and cross-section through a typical cell of the area array are shown in Figure 5. A photosite is defined on three sides by a P+ channel stop region and on the fourth by a barrier controlled by the vertical clock phases. Running vertically over columns of photosites is a first polysilicon layer, the photogate, which performs the carrier integration function and is clocked at the frame rate. Adjacent to each photosite is a vertical shift register cell, characterized by a carrier storage region bounded by channel stops and by gated barriers. Transfer in and out of a vertical cell is controlled by a gate made from a second polysilicon layer and clocked at the television scanning rate.

The signal saturation charge level for the cell is 0.07 pc, based on barrier heights of 3 volts. The photogate has a terminal capacitance of 2200 pF and a time constant of 120 nsec. The total capacitance of the vertical gates is 1500 pF with a time constant of 230 nsec.

## IV. STRUCTURAL DETAILS

In the fabrication of the device, nine mask levels are involved. As Figure 4 indicates, the surface topography consists of two polysilicon layers with silicon nitride and thermal oxide dielectrics insulating them from each other and from the substrate. The vapox dielectric functions as a substrate for the aluminum, which in the area array serves to opaque the vertical registers.

In fabricating the device, the most critical process steps are the two masking operations, where the horizontal register gate structures are defined. The major phases, $\phi_{H1}$ and $\phi_{H2}$, are formed from the first polysilicon layer, while the minor phases, $\phi_{H3}$ and $\phi_{H4}$, are made from the second polysilicon layer. The overlap between the two sets of gates is 2 μm, which is the minimum design rule tolerance for all layers.

The definition of the floating-gate structure in the DFGA is also critical. In order to maximize sensitivity, the capacitance of the floating gates must be kept low. In this design, they are 5 μm wide and are defined in the first poly. The phase gates on either side of them are defined in the second poly and should ideally be positioned so that there is no gap on either side of the floating gates. This requirement results in a separation between the phase gates of 3 μm at this point.

In contrast to the etched gate structures which form the photogate and horizontal register gates, the vertical gates are formed by selectively doping the second polysilicon layer. Thus the gaps between vertical gates are bridged with undoped poly.

## V. DRIVE CONSIDERATIONS

The input register, output register and DFGA are driven from the same four-phase clocking circuit. While a line of information is clocked out of the array, another line can be clocked in. There are 190 information bits in each horizontal line. The longest path from the output register is that to the DFGA output. There are 24 transfers for each phase in the DFGA, and 19 in the connecting channel. The total number of high-speed transfers for each phase is therefore 190 ± 43 = 233.

For a horizontal clock rate of 7.16 MHz, the element time is 140 nsec; thus the high-speed sections are emptied in 32.6 μsec. Since the horizontal interval is 63.5 μsec for standard TV, the inhibit time is 30.9 μsec. The horizontal registers can be clocked in either a two- or four-phase mode.

In the vertical registers, there is a vertical gate per sensor row, i.e., 244, plus three extra to allow for the incorporation of circuitry at either end. The vertical clock rate is 15.75 kHz for a scan time of 15.6 msec/field and a vertical inhibit time of 1.07 msec (60-Hz field rate).

Figure 6 shows a four-phase timing diagram suitable for driving the device. In this implementation, 260 CCD bit pulses are generated. During the horizontal inhibit period, all horizontal phases except $\phi_{H1}$ are kept low until the next line of video has been transferred in from $V_1$, which is also low at this time. One hundred and twenty-eight vertical pulses are generated per field. One hundred and twenty-three are needed as a minimum.

Charges are transferred from the area array to the output register during the horizontal inhibit interval, and from the photosites to the vertical registers during the vertical inhibit interval.

## VI. PERFORMANCE

A number of 190 × 244 runs have been successfully fabricated to date. Good high light level imaging has been demonstrated. At very low light levels, the utility of the DFGA for the detection of signal levels on the order of 30 electrons has been confirmed. Figure 7 shows high light level images from the DFGA and

FGA1. The DFGA can handle approximately 90% of the saturation charge level of the area array. When all on-chip output amplifiers are biased as source followers with $R_S$ = 1 K, typical saturation output voltages are 30 mV for the GCI, FGA1 and FGA2, and 150 mV for the DFGA. These pictures were taken at data rates of 10 MHz. Transfer inefficiency is negligible to 20 MHz. Horizontal resolution is approximately 142 lines/picture height. Vertical resolution is approximately 244 lines/picture height.

Representative low light level images are shown in Figure 8. Here the DFGA output is being viewed at five different light levels, at a date rate of 10 MHz, and in a +25°C ambient. Figure 8a shows a high light level image of approximately 140,000 electrons. In the subsequent pictures, the light source was attenuated using neutral density filters, the final attenuation resulting in an image of about 70 electrons.

## VII. SUMMARY

A 190 × 244 CCD buried-channel area imaging array has been developed. An on-chip 12-stage distributed floating-gate amplifier significantly enhances the detectability of low light level images. Good array performance has been achieved at data rates up to 20 MHz.

## ACKNOWLEDGEMENT

The development of this imaging array was in part supported by the Naval Electronic Systems Command.

## REFERENCE

1. D. D. Wen, "A Distributed Floating Gate Amplifier in Charge Coupled Devices," ISSCC, 1975.

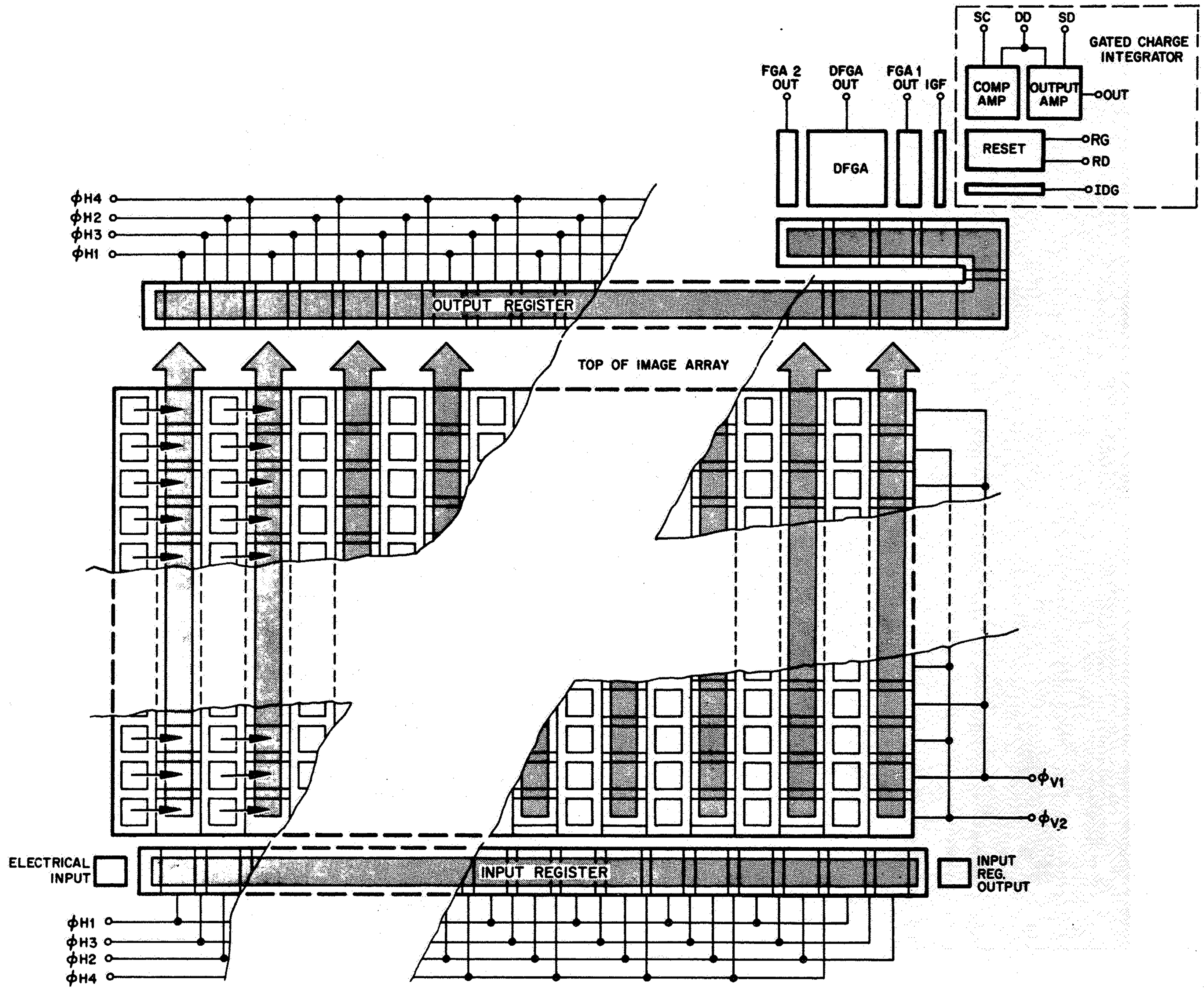



Figure 1. Functional layout of 190 × 244 array

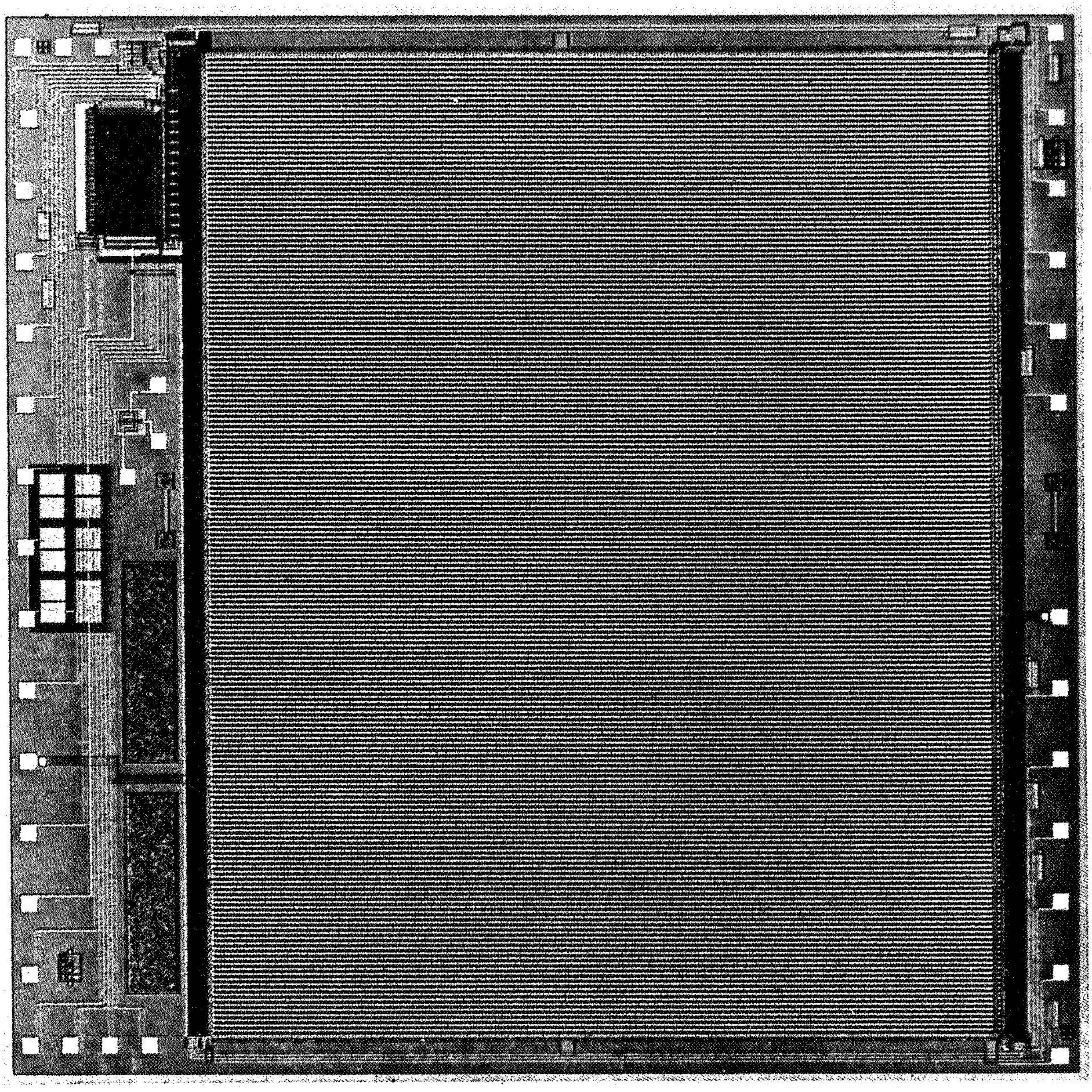


Figure 2. Photograph of die

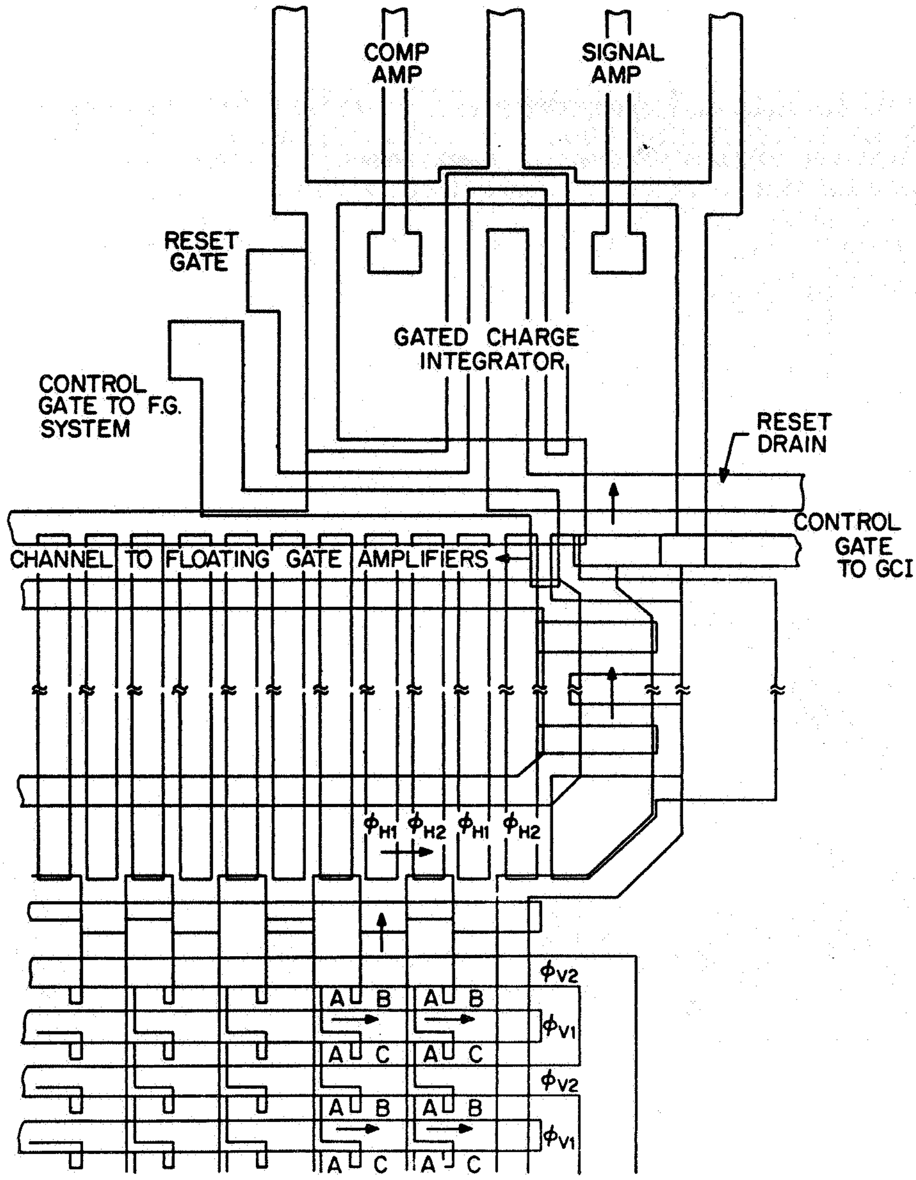



Figure 3. Detail view of array at amplifier interface

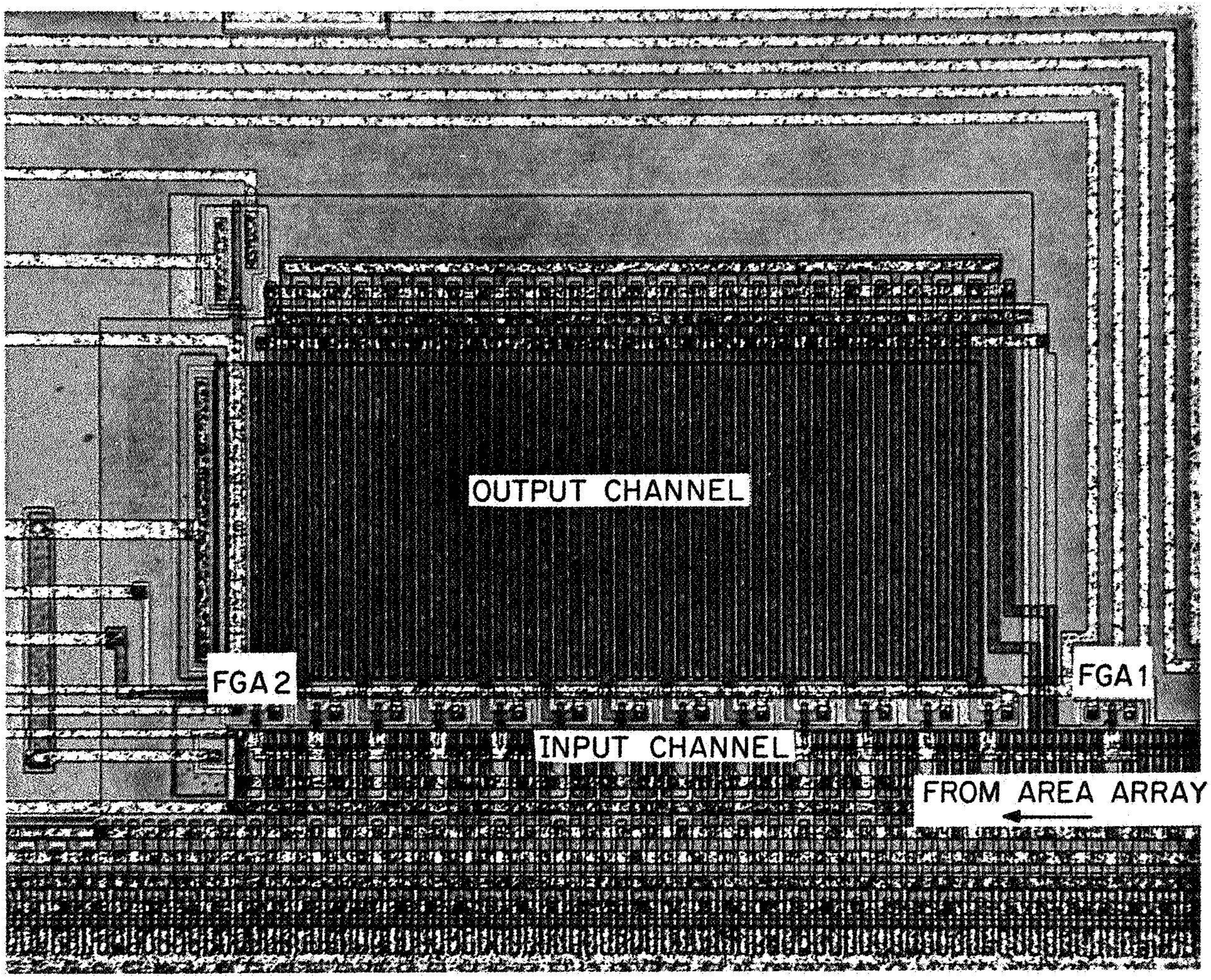



Figure 4. Floating-gate amplifier system

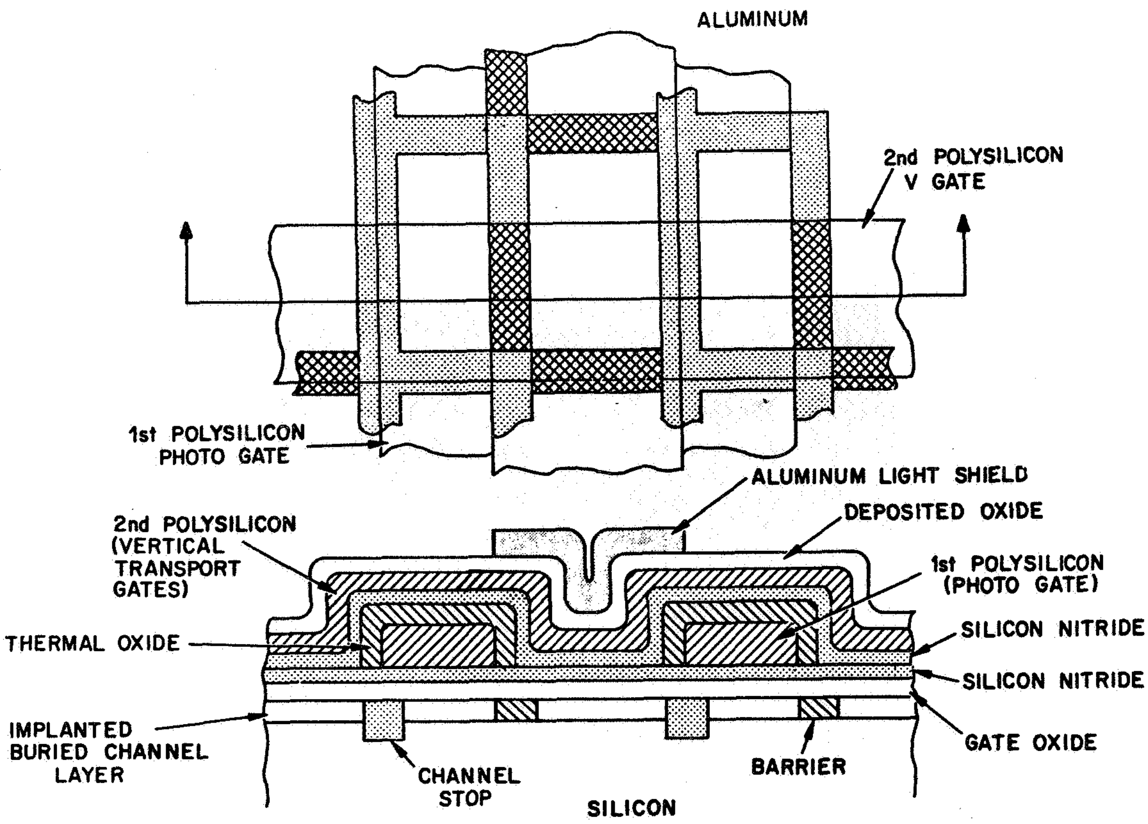
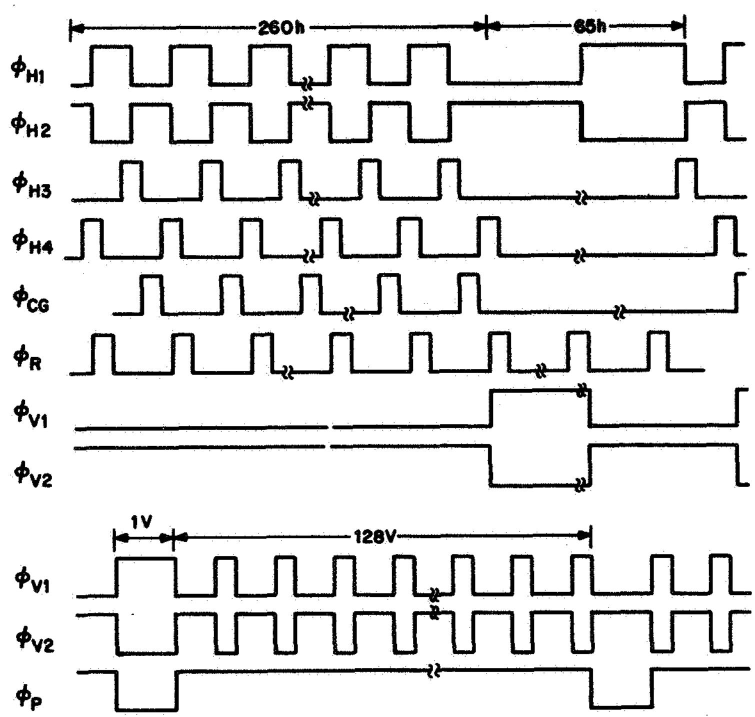



Figure 5. Cell structure in area array




For 2$\phi$ Operation, $\phi_{H1}$ and $\phi_{H3}$ are in Phase; also $\phi_{H2}$ is in Phase with $\phi_{H4}$

Figure 6. Timing diagram

(a)

(b)

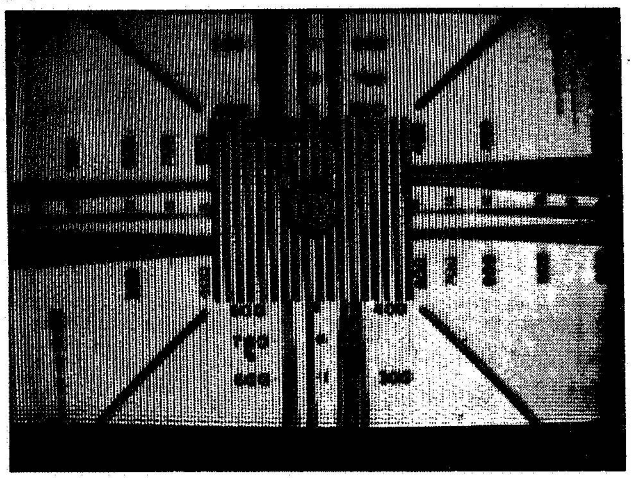
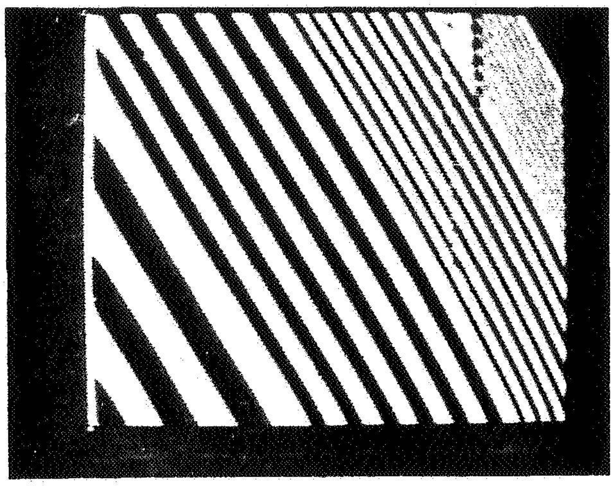
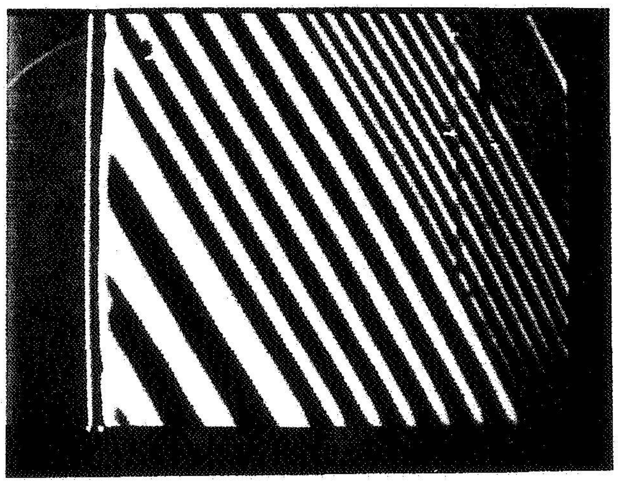


Figure 7. High light level images from (a) the DFGA and (b) FGA1 (To read the effective resolution, divide the test chart numbers by two.)

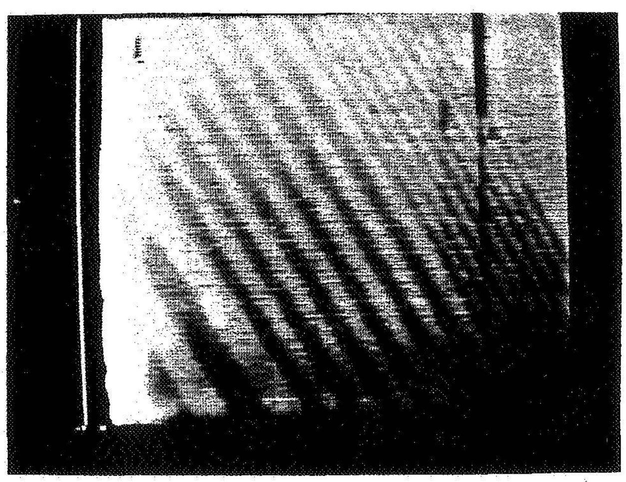
(a) ND=0, 140,000 electrons



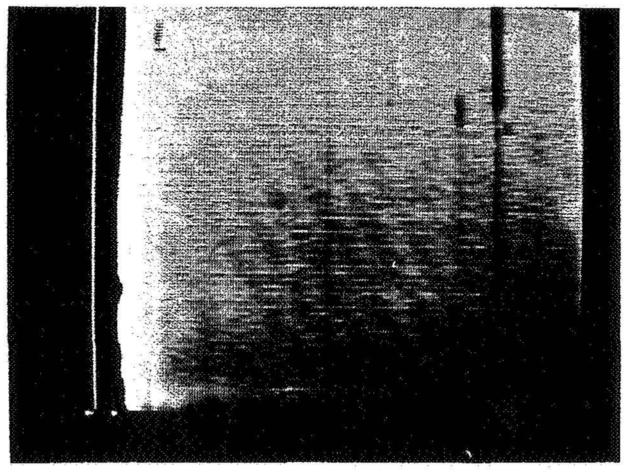
(b) ND= 1.0, 14,000 electrons



(c) ND=2.0, 1400 electrons



(d) ND=3.0, 140 electrons



(e) ND=3.3, 70 electrons

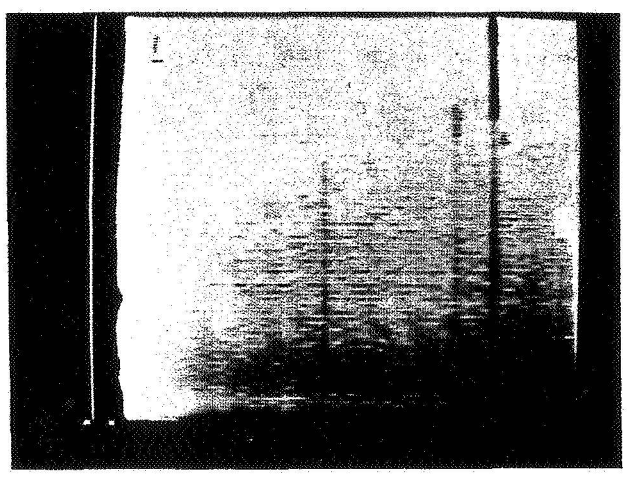


Figure 8. DFGA images at +25°C ambient, showing the effect of progressive light attenuation on image quality