X-933-75-217

NASA TM X- 70960

CONFIGURATION DESCRIPTION AND LOAD ANALYSIS FOR THE ATMOSPHERIC AND OCEANOGRAPHIC INFORMATION PROCESSING SYSTEM (AOIPS)

JOHN T. DALTON

JULY 1975

GSFC

GODDARD SPACE FLIGHT CENTER

GREENBELT, MARYLAND

X-933-75-217

Configuration Description

and

Load Analysis

for the

Atmospheric and Oceanographic

Information Processing System

(AOIPS)

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July 1975

Computer Systems Branch
Code 933

ABSTRACT

This paper describes the planned configuration of the Atmospheric and Oceanographic Information Processing System (AOIPS) being designed and implemented by the Computer Systems Branch (Code 933) of the Information Extraction Division. A system load analysis is performed and various reconfiguration options are discussed.

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I. Introduction

The Atmospheric and Oceanographic Information Processing System (AOIPS) is an interactive system designed to meet the image display, analysis, and data management needs of investigators in the disciplines of meteorology, hydrology, earth resources, and oceanography. In addition to providing analysis support, it will be used to develop new information extraction and analysis techniques and to provide a facility for use in future research and development efforts.

AOIPS, as shown in Figure 1, will consist of a modified General Electric (GE) IMAGE 100 Interactive Multispectral Image Analysis System, a Digital Equipment Corporation (DEC) PDP-11/70 computing system and a color image display and analysis terminal. In order to increase the accessibility of the IMAGE 100 to the larger on-line data base of the PDP-11/70, a 16K word core memory and a 88M byte disk drive will be shared by the two systems. The PDP-11/70 will also be interfaced to the GSFC Science and Applications Computing Center (SACC) IBM 360/91 via a 4800 baud communications line.

The following sections detail the various components that make up the IMAGE 100 and the PDP-11/70 computing system.

II. AOIPS System Description

AOIPS will basically consist of two minicomputer systems - (1) the PDP-11/45 system controlling the IMAGE 100 Image Analyzer Console and (2) the PDP-11/70 system controlling the GSFC-designed color image display and analysis terminal (hereafter referred to as the Image

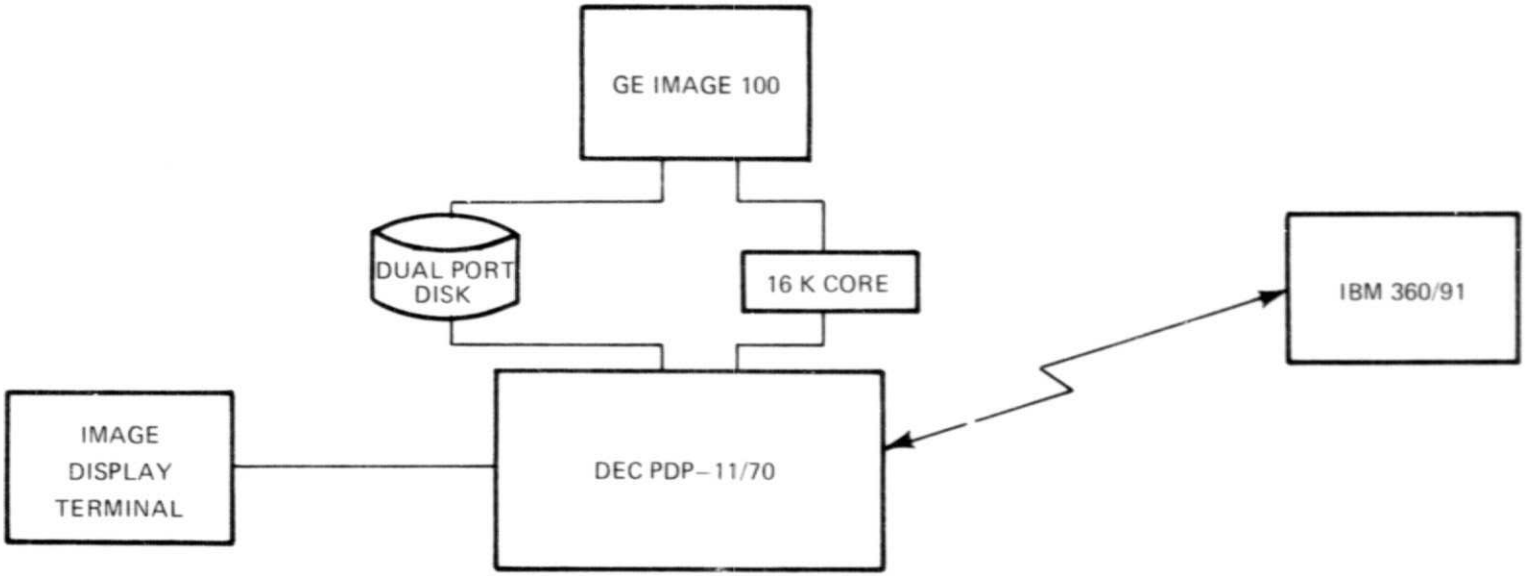

FIGURE 1. ATMOSPHERIC AND OCEANOGRAPHIC INFORMATION PROCESSING SYSTEM (AOIPS)

Display Terminal). The IMAGE 100 system is expected in September 1975 and is described in Section II.A. The PDP-11/70 system will be acquired in two phases. The equipment listed in Section II.B comprises the initial delivery expected in August 1975. Section II.C lists the system components to be acquired through an augmentation planned for the first half of calendar year 1976.

II.A. IMAGE 100 System Components

The GE IMAGE 100 (expected delivery September 1975) will consist of the following equipment:

- Image analyzer console
- Solid state image memory unit
- Process controller including:
  - DEC PDP-11/45 Central Processing Unit (CPU) with a Floating Point Unit (FPU) and a memory management unit
  - 64K (16-bit) word core memory
  - DEC writer
  - DEC DR11-B Direct Memory Access (DMA) interface unit
  - DEC KW11-L real time clock
  - DEC RK11-DE disk drive and controller (1.2M word)
  - DEC RK05-AA disk drive (1.2M word)
  - DEC DL11-E display terminal interface
  - DEC CR11 card reader
- Two Bucode model 4025-DD 9-track tape drives (125 ips, 800/1600 bpi)

- Datum model 5091-F11-DD controller
- Gould model 5000 line printer (132 column, 1200 lpm)
- Tektronix model 4012 graphics display terminal
- Scanner interface*
- IMAGE 100 - PDP-11/70 computer interface unit (to be delivered in November 1975) consisting of:
  - MA11-FA multiport memory unit (16K words)
  - MA11-FF control unit/control panel

A block diagram of the IMAGE 100 portion of AOIPS is shown in Figure 2.

II.B. PDP-11/70 Initial System Equipment

The PDP-11/70 portion of AOIPS will be delivered in two phases. The initial delivery (expected August 1975) will include the following equipment:

- PDP-11/70 CPU with 2K byte bipolar cache memory, memory management, and a Floating Point Unit (FPU)
- 128K 8-bit bytes (64K words) parity core memory with 1.02 μ sec cycle time for a 32-bit (double-word) transfer.
- ASR-35 teletype and control
- KW11-L line frequency clock
- RWP04 88M byte moving head disk drive and controller

* A TV scanner (which is not part of the initial system) digitizes hard copy images, maps, overlays, etc. The scanner interface allows the digitized data to be input to the computer.

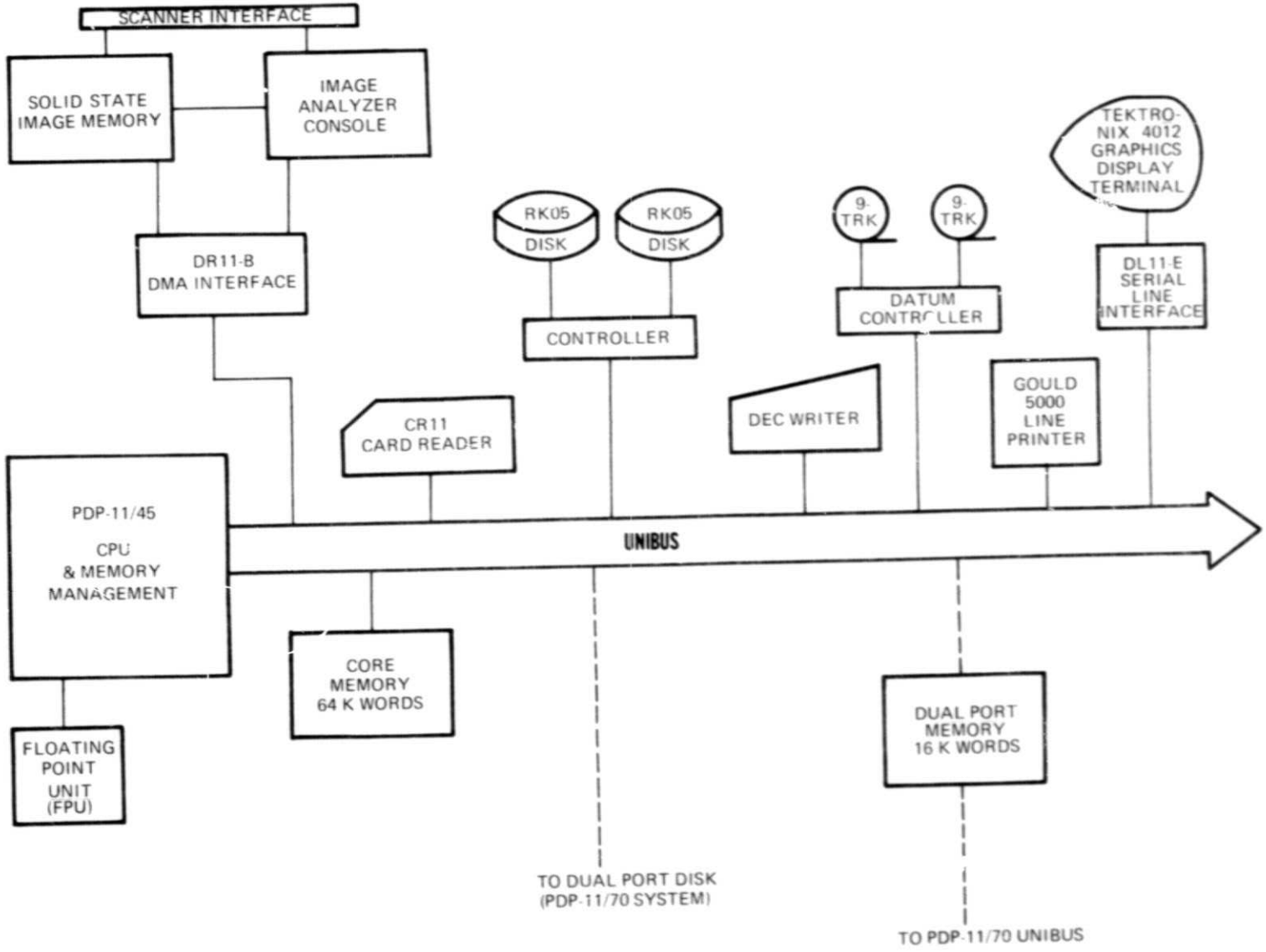

FIGURE 2. IMAGE 100 CONFIGURATION

- TWU45 800/1600 bpi, 75 ips magnetic tape drive and controller
- TU45 800/1600 bpi, 75 ips expansion magnetic tape drive
- CR11 300 cpm card reader
- LP11-VA 132 column, 64 character, 300 lpm line printer and control
- VT05-BA CRT terminal
- DL11-A controller for VT05
- KW11-P real time clock
- DR11-B DMA interface (4 each)

The planned initial configuration of these items is shown in Figure 3.

While the PDP-11 series before the 11/70 performed all I/O by means of a single data bus (the UNIBUS) with 16-bit (word) transfers, the PDP-11/70 provides for up to four high-speed control devices (DEC model RH70) in addition to the UNIBUS. These controllers are interfaced to the cache memory of the 11/70 via a 32-bit (double-word) high-speed data bus, thus allowing I/O operations to take advantage of the 32-bit data path from the cache to memory. As shown in Figure 3, two of these controllers will be provided in the initial delivery - one to control the RP04 disk drive and one to control the two 9-track tape drives.

II.C. PDP-11/70 Augmented System

The second phase of the PDP-11/70 delivery is an augmentation

*EXPECTED DELIVERY SEPTEMBER 1975
**EXPECTED DELIVERY NOVEMBER 1975

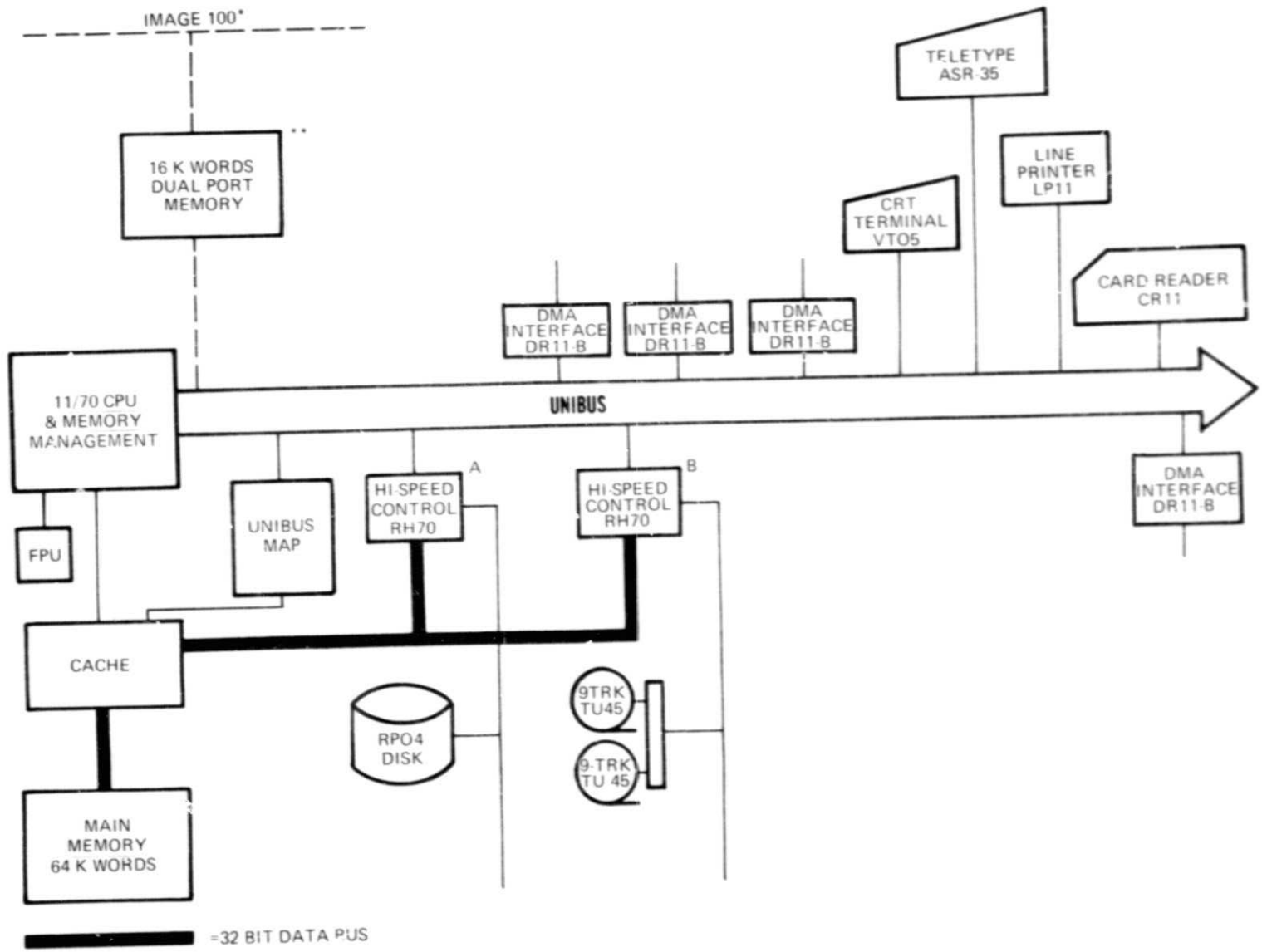

FIGURE 3. PDP–11/70 INITIAL CONFIGURATION

planned for the first half of CY 1976. The additions planned in this augmentation are listed below:

- 800/1600 bpi, 75 ips magnetic tape drive and UNIBUS controller
- Dual port 44M word disk drive to be interfaced with both the IMAGE 100 and the PDP-11/70
- 44M word swapping disk drive
- Interactive graphics terminal and interface
- 4800 baud half-duplex bi-synchronous transmission controller and modem
- 64K words of additional core memory

During the same time period, the Image Display Terminal is expected to be delivered with an additional high speed controller and a VT50 CRT terminal and controller. The addition of a High Density Digital Tape Drive (HDDT) is also planned. A special interface will be designed and implemented for the HDDT to allow it to share a high-speed controller with standard magnetic tape drives.

The planned configuration including the above items is shown in Figure 4. The dual port disk will be interfaced to the same high-speed controller as the RP04 drive provided in the initial delivery. One of the initial 9-track tape drives will be moved to the UNIBUS with the new tape drive. Its place on the high-speed controller will be taken by the HDDT. The swapping disk and the Image Display Terminal will be connected to the remaining two controllers. A DR11-B DMA interface between the Image Display Terminal and the UNIBUS is also planned for

*EXPECTED DELIVERY SEPT. 1975
**EXPECTED DELIVERY NOV. 1975

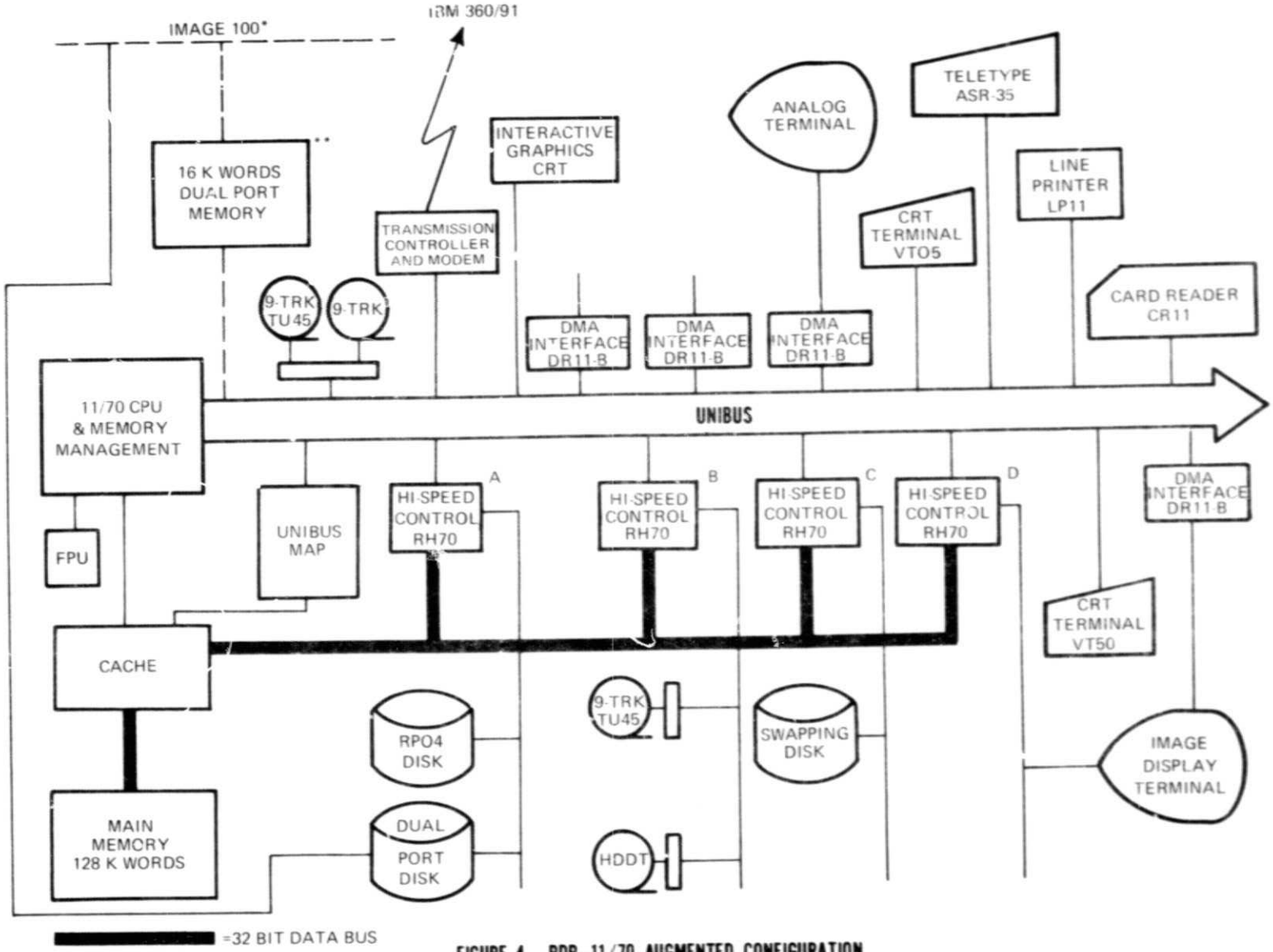

FIGURE 4. PDP-11/70 AUGMENTED CONFIGURATION

the purpose of transferring control information.

While the IMAGE 100 configuration is well defined, the presence of the four high-speed controllers on the PDP-11/70 allows some room for reconfiguration. Section III presents peak load estimates for the IMAGE 100 and PDP-11/70 systems. Additional peak load estimates are given in Section IV for PDP-11/70 reconfiguration options that may be considered in the future.

III. Peak Load Estimates

In order to evaluate the various configuration options available in designing a computer system or to identify potential bottlenecks in a specific system, it is necessary to identify the resources that limit throughput and to determine the peak loads on them. For example, overall system throughput is generally limited by the speed at which data can be transferred to and from memory. The total memory transfer capacity is determined by the memory cycle time, the data transfer width, and the degree to which memory is interleaved. The PDP-11 uses non-processor requests (NPR) to transfer data between high speed peripheral devices and memory. These transfers take place between bus cycles of an instruction execution and at a higher priority than CPU access to memory. Therefore, as the total aggregate transfer rate of these peripheral devices approaches the memory capacity, the CPU utilization decreases and system degradation becomes progressively worse.

Tables I and II give the transfer rates for the AOIPS peripherals. The peak load estimates for the IMAGE 100 and the initial and augmented phases of the PDP-11/70 system are based on these transfer rates.

III.A. IMAGE 100 Peak Load Estimate

The IMAGE 100 will contain a PDP-11/45 with 64K words of core memory with a basic cycle time of 980 nanoseconds. An additional 90 nanoseconds is required when the memory management unit is enabled. This results in a maximum memory transfer rate of 0.935M words/second. Table III gives a breakdown of the load imposed by each of the IMAGE 100 peripherals (including the dual port disk described in Section II.C) on the available memory cycles. All numbers are in terms of memory cycles per second (Hz), where each memory cycle results in the transfer of one 16-bit word.

As shown in Table III, the initial configuration of the IMAGE 100 will have an estimated peak load of 87.4% of the available memory cycles used for data transfers. When the dual port disk is connected however, the peak load will be 130% of the system capacity. It will therefore be necessary to synchronize the device handlers for the Image Analyzer Console DR11-B and the dual port disk so that simultaneous data transfers by both devices are not permitted.

III.B. PDP-11/70 Peak Load Estimate

As mentioned previously, the PDP-11/70 provides a 32-bit data path through the cache memory to main memory for up to four high speed

Table I

Transfer rates for AOIPS peripherals

Device Name	Model ** Number	Maximum Transfer Rate (Bytes/Second)
Moving head disk	RP04	0.8×10^6
Magnetic tape, 9-track	TU45	1.2×10^5
Alphanumeric display terminal	VT50	1200
Alphanumeric display terminal	VT05	300
* Card reader	CR11	570
Line printer	LP11	660
Teletype	ASR-35	10
Graphic display terminal		1200
Transmission controller (4800 baud)		600
Image display terminal		2×10^6
DMA interface	DR11-B	0.8×10^6 ***
HDDT		See Table II
* Disk cartridge	RK05	0.18×10^6
* Line printer	Gould 5000	2.64×10^3
* Magnetic tape, 9-track	Bucode 4025-DD	0.2×10^6
* Graphic display terminal	Tektronics 4012	1200

Table I

Transfer rates for AOIPS peripherals

Device Name	Model ** Number	Maximum Transfer Rate (Bytes/Second)
Moving head disk	RP04	0.8×10^6
Magnetic tape, 9-track	TU45	1.2×10^5
Alphanumeric display terminal	VT50	1200
Alphanumeric display terminal	VT05	300
* Card reader	CR11	570
Line printer	LP11	660
Teletype	ASR-35	10
Graphic display terminal		1200
Transmission controller (4800 baud)		600
Image display terminal		2×10^6
DMA interface	DR11-B	0.8×10^6 ***
HDDT		See Table II
* Disk cartridge	RK05	0.18×10^6
* Line printer	Gould 5000	2.64×10^3
* Magnetic tape, 9-track	Bucode 4025-DD	0.2×10^6
* Graphic display terminal	Tektronics 4012	1200

Table 1 (continued)

Device Name	Model ** Number	Maximum Transfer Rate (Bytes/Second)
* Image memory unit		1.25×10^6
* DEC writer	LA36	30

* Supplied with IMAGE 100

** All model numbers are DEC unless otherwise specified

*** Maximum rate of DMA interface on PDP-11/70

Table II

HDDT Data Rates

(bytes/sec)

Tape Speed (inch/sec)	Unpacked (8 channels of data)	Packed (11 channels of data)
1 7/8	3.0×10^4	4.125×10^4
3 3/4	6.0×10^4	8.25×10^4
7 1/2	1.2×10^5	1.65×10^5
15	2.4×10^5	3.3×10^5
30	4.8×10^5	6.6×10^5
60	9.6×10^5	1.32×10^6
120	1.92×10^6	2.64×10^6

Note:

- Tentative configuration of HDDT calls for 14 channels operating at 16000 bits/inch/channel.
- A maximum of 11 of the 14 channels available may be used to record data. The remaining channels are assigned for a data sync track, a search track and a time track.
- See Appendix, "Considerations Involved in Selecting HDDT Tape Speed".

Table III

IMAGE 100 Peak Load Estimate

Total memory cycle capacity = 0.935 MHz

1 Hz = 1 16-bit word transfer

Device	Memory Cycle Load (MHz)
Disk (RK05)	0.09
Line printer (Gould)	0.00132
Mag tape (Bucode)	0.10
Graphics display terminal	0.0006
Image memory unit	0.625
DEC writer	0.000015
Card reader	0.000285
Delivered system load =	0.817220
Percentage of total capacity =	87.4%
Remaining capacity =	0.117780
Dual-port disk load =	0.40 *
Total load =	1.217220
Percentage of total capacity =	130%
Overload =	0.282220

* Since the source of the augmentation equipment is not known at this time, the data rate used is that of similar equipment included in the PDP-11/70 initial delivery.

I/O controllers (DEC models RH70). For non-interleaved memory (as is the case in the initial configuration), the main memory cycle time is 1.02 μ sec for a double word (32 bit) access, yielding a 3.92M byte per second memory transfer rate, or a .98 MHz memory cycle rate (with one double word access per cycle). For interleaved memory (as will be the case in the augmented configuration), the effective cycle time is 690 nsec, yielding a 5.8M byte per second memory transfer rate or a 1.45 MHz memory cycle rate (with one double word access per cycle).

When data transfers are performed via the UNIBUS, only 16 bits are transferred at a time. Since 16-bit transfers are not affected by interleaving, this yields a basic cycle time of 1.02 μsec per 16-bit transfer. When the UNIBUS map is enabled, the map overhead increases this to approximately 1.2 μ sec. If the transfer is a read from main memory, the cache overhead of 0.3 μ sec must be added. However, assuming that the next transfer will be from the next sequential location (as is usually the case in block data transfers), that transfer will take advantage of the cache and will thus have a cycle time of 0.3 μ sec. Therefore, each double word transfer from main memory to a UNIBUS device will generally require 1.8 μ sec (1.5 μ sec for the first word and 0.3 μ sec for the second). This is equivalent to a 0.556 MHz memory cycle rate (at one double word access per cycle). When transfers from UNIBUS devices to main memory occur, the memory write cycle time (0.75 μ sec) plus the UNIBUS map overhead (approximately 0.18 μ sec) yields a cycle time of 0.93 μ sec per word or 1.86 μ sec per double-word, which is equivalent to a 0.538 MHz memory cycle rate

(one double-word access per cycle).

In determining the system load due to UNIBUS devices, the worst case of writes to main memory will be used. Therefore, the load factor increase for devices on the UNIBUS over devices on the high speed bus is:

$$\frac{1.86\ \mu \text{ sec/double-word on UNIBUS}}{.690\ \mu \text{ sec/double-word on high speed bus}} = 2.7$$

for interleaved memory; and

$$\frac{1.86\ \mu \text{ sec/double-word on UNIBUS}}{1.02\ \mu \text{ sec/double-word on high speed bus}} = 1.82$$

for non-interleaved memory.

Table IV gives a breakdown of the load imposed by each of the peripherals of the PDP-11/70 initial configuration. The load for each device is given by the transfer rate (M bytes/sec)/4 (bytes/double-word access) multiplied by the 1.82 load factor increase given above if the device is on the UNIBUS. As shown, the estimated peak load for the initial configuration is 23.5% of the total capacity.

Table V gives the peak load estimate for the augmented configuration. The load for each device is given by the transfer rate (M bytes/sec)/4 (bytes/double-word access) multiplied by the 2.7 load factor increase given above if the device is on the UNIBUS. As shown, the estimated peak load is 48% over the capacity. This analysis, however, assumes that the Image Display Terminal and the two DMA interfaces are operating simultaneously and at maximum capacity. Since the two

Table IV

PDP-11/70 Initial Configuration Peak Load Estimate

Total memory cycle capacity = 0.98 MHz

Device	Location	Memory Cycle Load (MHz)
Disk (RP04)	RH70-A	0.2
Tape (TU45)	RH70-B	0.03
Card reader (CR11)	UNIBUS	0.000259
Line printer (LP11)	UNIBUS	0.000300
Display terminal (VT05)	UNIBUS	0.000136
Teletype (ASR-35)	UNIBUS	0.000005
Total load	=	0.2307 MHz
Percentage of total capacity	=	23.5%
Remaining capacity	=	0.7493 MHz

DMA interfaces will be transferring control and status information and not high volumes of data, it is reasonable to assume that their rates (as determined by the user devices to which they are connected) could be much slower than the maximum rate of 800K bytes/second given in Table I. Also, the device handler software will be designed such that only one DMA interface can be transferring data at any one time. Thus, if the maximum data rate of any device connected to the system by a DMA interface were held to 100K bytes/second and if only one DMA interface could run at a time, the total DMA interface load would be 0.068 MHz, resulting in a total load of 1.134566 MHz and a remaining capacity of 0.315434 MHz. This analysis is shown in Table V(a). The estimated peak load in this case is 78% of the total capacity.

An additional reduction in the load can be achieved by decreasing the data transfer rate of the Image Display Terminal interface on the high-speed bus. The initial load of 0.5 MHz assumes data transfer in the cycle time of the refresh memory (2M byte per second). Since data transfers will generally be of TV-size (256K byte) images (which is too large to be held entirely in main memory), the data will probably be coming from (or going to) another peripheral device via main memory. Since the fastest device (an RP04 disk) has a transfer rate of 800K bytes per second (0.2 MHz load), the Image Display Terminal/high-speed bus transfer rate can be reduced to 800K bytes per second without a significant effect on overall response. This would reduce the total peak load to 0.834566 MHz (57.5% of total capacity), with a remaining capacity of 0.615434 MHz. This analysis is shown in Table V(b) and

Table V

PDP-11/70 Augmented Configuration Peak Load Estimate

Total memory cycle capacity = 1.45 MHz

Device	Location	Memory Cycle Load (MHz)
Disk (RP04)	RH70-A	0.2*
HDDT (Assuming 15 ips)	RH70-B	0.0825
Swapping disk	RH70-C	0.2*
Image Display Terminal	RH70-D	0.5
9-track tape (TU45)	UNIBUS	0.081*
Display terminal (VT50)	UNIBUS	0.000810
Card reader (CR11)	UNIBUS	0.000385
Line printer (LP11)	UNIBUS	0.000446
Display terminal (VT05)	UNIBUS	0.000203
Teletype (ASR-35)	UNIBUS	0.000007
DMA Interface (DR11-B) for Image Display Terminal	UNIBUS	0.54
DMA Interface (DR11-B) for analog terminal	UNIBUS	0.54
4800 baud transmission controller	UNIBUS	0.000405*
Interactive graphics terminal	UNIBUS	0.000810*

Table V (continued)

Total load = 2.146566 MHz

Percentage of total capacity = 148%

Overload = 0.696566 MHz

* Since the source of the augmentation equipment is not known at this time, the data rates used are those of similar equipment included in the initial delivery.

Table V(a)

PDP-11/70 Augmented Configuration - Peak Load Estimate

- Single DMA interface operation at maximum rate of 100K bytes/second

Total memory cycle capacity = 1.45 MHz

Device	Location	Memory Cycle Load (MHz)
Disk (RP04)	RH70-A	0.2*
HDDT (Assuming 15 ips)	RH70-B	0.0825
Swapping disk	RH70-C	0.2*
Image Display Terminal	RH70-D	0.5
9-track tape (TU45)	UNIBUS	0.081*
Display terminal (VT50)	UNIBUS	0.000810
Card reader (CR11)	UNIBUS	0.000385
Line printer (LP11)	UNIBUS	0.000446
Display terminal (VT05)	UNIBUS	0.000203
Teletype (ASR-35)	UNIBUS	0.000007
DMA Interface (DR11-B) for Image Display Terminal	UNIBUS	0.068
DMA Interface (DR11-B) for analog terminal	UNIBUS	
4800 baud trarsmission controller	UNIBUS	0.000405*
Interactive graphics terminal	UNIBUS	0.000810*
Total load	=	1.134566

Table V(a) (continued)

Percentage of total capacity	=	78%
Remaining capacity	=	0.315434

* Since the source of the augmentation equipment is not known at this time, the data rates used are those of similar equipment included in the initial delivery.

Table V(b)

PDP-11/70 Augmented Configuration - Peak Load Estimate

- Single DMA interface operation at maximum rate of 100K bytes/second
- Image Display Terminal transfers limited to 800K bytes/second

Total memory cycle capacity = 1.45 MHz

Device	Location	Memory Cycle Load (MHz)
Disk (RP04)	RH70-A	0.2*
HDDT (assuming 15 ips)	RH70-B	0.0825
Swapping disk	RH70-C	0.2*
Image Display Terminal	RH70-D	0.2
9-track tape (TU45)	UNIBUS	0.081*
Display terminal (VT50)	UNIBUS	0.000810
Card reader (CR11)	UNIBUS	0.000385
Line printer (LP11)	UNIBUS	0.000446
Display terminal (VT05)	UNIBUS	0.000203
Teletype (ASR-35)	UNIBUS	0.000007
DMA Interface (DR11-B) for Image Display Terminal	UNIBUS	0.068
DMA Interface (DR11-B) for analog terminal	UNIBUS	
4800 baud transmission controller	UNIBUS	0.000405*
Interactive graphics terminal	UNIBUS	0.000810*
Total load	=	0.834566

Table V(b) (continued)

Percentage of total capacity	=	57.5%
Remaining capacity	=	0.615434

* Since the source of the augmentation equipment is not known at this time, the data rates used are those of similar equipment included in the initial delivery.

Note: This table presents the expected peak load conditions under which the augmented system (Figure 4) will be operated.

delineates the expected peak load conditions under which the augmented AOIPS system (Figure 4) will be operated.

IV. Reconfiguration Options

The following major criteria were used in evaluating and selecting the PDP-11/70 configurations shown in Figures 3 and 4:

(a) Currently, only one device type may be connected to a high speed controller;

(b) The swapping disk should be connected to a different controller from the disks used for data and program storage in order to minimize controller contention problems;

(c) One 9-track magnetic tape drive should be connected to a different controller from the other two in order to provide more concurrent I/O for tasks requiring both input and output tapes; and

(d) The Image Display Terminal must be allowed a sufficiently high data transfer rate to provide satisfactory response.

While criteria (a), (b), and (c) are rigid, the subjective nature of (d) may allow the following alternative options to be considered.

Option 1.

Option 1 consists of the following:

Allow the DR11-B DMA interface to the Image Display Terminal to operate at the 800K byte per second rate and use it to transfer all data; remove the Image Display Terminal/high-speed controller interface. Move the two 9-track magnetic tape drives from the UNIBUS to the high-speed controller (controller D in Figure 4) vacated by the Image

Display Terminal.

The peak load estimate for this option is given in Table VI. As shown, this option results in a greater peak load than does the augmented configuration with the reduced DMA transfer rates (Table V(b)). Also, the DMA interface for the Image Display Terminal would now be transferring image data as well as control information, and would therefore have a much higher duty cycle resulting in a greater average load. For these reasons, this option is not being seriously considered.

Option II.

Option II consists of the following:

Interface the Image Display Terminal to the second port of a dual port disk; this necessitates the replacement of the single-port disk on controller A in Figure 4. Move the two 9-track magnetic tape drives from the UNIBUS to the high-speed controller (D) vacated by the Image Display Terminal.

The peak load estimate for this option is given in Table VII. As shown, this option provides a significant load advantage over the augmented configuration (40% vs. 57.5% of capacity used). However, main disadvantages of this option are as follows:

(a) The Image Display Terminal interface to the dual-port disk must be a smart one (for example, a small CPU).

(b) In order to prevent the disk from being seek-bound, the Image Display Terminal must wait until the disk is completely loaded before it begins reading from the disk. Assuming the entire disk pack is used (88 million bytes), approximately 2 minutes are required to load the

Table VI

PDP-11/70 Reconfiguration Option I Peak Load Estimate

Total memory cycle capacity = 1.45 MHz

Device	Location	Memory Cycle Load (MHz)
Disk (RP04)	RH70-A	0.2*
HDDT (assuming 15 ips)	RH70-B	0.0825
Swapping disk	RH70-C	0.2*
Tape (TU45)	RH70-D	0.03*
Display terminal (VT50)	UNIBUS	0.000810
Card reader (CR11)	UNIBUS	0.000385
Line printer (LP11)	UNIBUS	0.000446
Display terminal (VT05)	UNIBUS	0.000203
Teletype (ASR35)	UNIBUS	0.000007
DMA interface (DR11-B) for R&D terminal	UNIBUS	0.54
DMA interface (DR11-B) for analog terminal	UNIBUS	0.068
4800 baud transmission controller	UNIBUS	0.000405*
Interactive graphics terminal	UNIBUS	0.000810*

Table VI

Total 'oad	=	1.123566
Percentage of total capacity	=	77.5%
Remaining capacity	=	0.326434

* Since the source of the augmentation equipment is not known at this time, the data rates used are those of similar equipment included in the initial delivery.

Table VII

PLP-11/70 Reconfiguration Option II Peak Load Estimate

Total memory cycle capacity = 1.45 MHz

Device	Location	Memory Cycle Load (MHz)
Disk (RP04)	RH70-A	0.2*
HDDT (assuming 15 ips)	RH70-B	0.0825
Disk (RP04)	RH70-C	0.2*
Tape (TU45)	RH70-D	0.03*
Display terminal (VT50)	UNIBUS	0.000810
Card reader (CR11)	UNIBUS	0.000385
Line printer (LP11)	UNIBUS	0.000446
Display terminal (VT05)	UNIBUS	0.000203
Teletype (ASR35)	UNIBUS	0.000007
DMA interface (R&D terminal and analog terminal)	UNIBUS	0.068
4800 baud transmission controller	UNIBUS	0.000405*
Interactive graphics terminal	UNIBUS	0.000810*
Total load	=	0.583566

Table VII (continued)

Percentage of total capacity	=	40%
Remaining capacity	=	0.866434

* Since the source of the augmentation equipment is not known at this time, the data rates used are those of similar equipment included in the initial delivery.

disk.

(c) The Image Display Terminal is one step further removed from the computation power of the CPU and from the remaining peripherals.

Due to these reasons, this option is not being implemented at this time, but may be considered in the future.

V. Summary

The configuration of the IMAGE 100 subsystem of AOIPS is shown in Figure 2. The device handlers will be synchronized so that simultaneous data transfers involving the Image Analyzer Console and the dual port disk cannot occur. This will result (as shown in Table III) in a peak load on the PDP-11/45 due to the system peripheral devices of 87.4% of the available memory cycles.

The post-augmentation configuration of the PDP-11/70 subsystem of AOIPS is shown in Figure 4. All data transfers through the DR11-B DMA interfaces will be limited in rate (for example, 100K bytes/second), and the device handlers will be written so that only one DR11-B can be transferring data at any given time. Also, the data transfer rate of the Image Display Terminal on the high speed bus will be limited to the RP04 disk rate of 800K bytes/second. This will result (as shown in Table V(b)) in a peak load on the PDP-11/70 due to the system peripheral devices of 57.5% of the available memory cycles.

Two reconfiguration options were considered in light of the peak system load. Option I, which basically consisted of interfacing the Image Display Terminal only with the UNIBUS and moving all tape drives

from the UNIBUS to the high speed bus, resulted in an increased load of 77.5% and is not being considered for implementation.

Option II, which consisted of interfacing the Image Display Terminal to the PDP-11/70 through a dual port disk and moving all tape drives from the UNIBUS to the high speed bus, resulted in a reduced peak load of 40%. This option is not currently being pursued due to the additional hardware required and the altered nature of the relationship between the PDP-11/70 and the Image Display Terminal.

Acknowledgements

I would like to express my appreciation to Messrs. Peter Bracken and Jerry Linnekin of Code 933 and to Gene Hodges and Neel Price of Digital Equipment Corporation for their invaluable suggestions and guidance in the preparation of this document.

Appendix

Considerations Involved in Selecting HDDT Tape Speed

The basic rule to use in selecting HDDT tape speed is: data must not be transferred from the HDDT faster than the destination device can handle it.

For example, if data is being read from the HDDT directly into memory for processing and the entire block of data being transferred can be stored in memory, then the HDDT could probably be run at 120 ips (2.64M bytes/second). However, if data is simply being buffered in memory for subsequent transfer to another peripheral device, then the HDDT speed must be selected such that the data transfer rate is less than that of the final destination device. The difference between the two data transfer rates must be great enough to allow for interrupt service routine execution and for destination device latency.

The fastest device in AOIPS (other than the HDDT) is the 44M word RP04 disk. While the data transfer time per word is 2.5 μ seconds, the actual transfer rate for a block of data must be determined from the number of bytes per track and the rotation speed as follows:

bytes/track = 256 words/sector X 22 sectors/track
X 2 bytes/word
= 11264

rotational speed = 3600 RPM
= 60 revolutions per second

bytes/sec = 11264 bytes/revolution X 60 revolutions per second.

= 675840 bytes per second.

Comparing this to the HDDT data rates given in Table II, one finds that the RP04 could accept one disk track of data from the HDDT at the 30 ips speed. However, since the volume of data input from the HDDT will generally require more than one track (a typical image of 4096 by 4096 requires 16M bytes), the RP04 head positioning and rotational latency times must be taken into account.

The RP04 controller automatically increments the track address within the cylinder being written when the last sector of the current track has been accessed. In addition, an automatic seek to the next cylinder is issued when the last sector of the last track in the current cylinder has been accessed. Therefore, assuming data transfer begins at sector 0 of track 0, head positioning is only required when a cylinder has been filled. The time required to position to an adjacent cylinder is 7 milliseconds.

Whenever a new data transfer operation to disk is initiated (for example, when alternating buffers), the rotational latency must be considered. This is a maximum of 16.67 milliseconds.

Using a double buffering scheme, the time required to fill a buffer from the HDDT must be long enough to allow for head positioning and data transfer to disk for the previous buffer. Using two track-sized

buffers (5632 words each), a maximum of 33.3 milliseconds (2 disk rotations) would be required to transfer each buffer to disk (one rotation for head positioning and one for the actual data transfer).

The HDDT speed selected must therefore result in a 5632-word transfer time greater than 33.3 milliseconds. Since 15 ips would result in one buffer being filled every 34.1 milliseconds, this speed is theoretically realizable. In practice however, the narrow margin afforded by the difference of 0.8 milliseconds may require a reduction of HDDT speed to 7 1/2 ips or a modification of the buffering strategy.

If some intermediate processing which results in a reduction of data volume (such as subsampling, band selection, or averaging) is performed before transfer to disk, the HDDT may be allowed to run at a faster speed. This consideration, however, is dependent on the degree of reduction and the time required for processing.