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THE RELATIONSHIP BETWEEN RELIABILITY AND BONDING TECHNIQUES IN HYBRID MICROCIRCUITS

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16. ABSTRACT

Differential thermal expansion has been shown to be responsible for many observed failures in ceramic chip capacitors mounted on alumina substrates. The present work has shown that the mounting techniques used in bonding the capacitors have a marked effect upon the thermally induced mechanical stress and thus the failure rate. A mathematical analysis of a composite model of the capacitor-substrate system to predict the magnitude of thermally induced stresses has been conducted. It has been experimentally observed that the stresses in more compliant bonding systems such as soft lead/tin and indium solders are significantly lower than those in hard solder and epoxy systems. The marked dependence upon heating and cooling rate has proven to be a determining factor in the prediction of failure in the indium and tin/lead solder systems. This study has shown that the harder or higher melting solders are less susceptible to thermal cycling effects but that they are more likely to fail during initial processing operations. In the course of the study, strain gage techniques were used to determine thermally induced expansion stresses of the capacitors and the alumina substrates. Thus, the compliance of the different bonding mediums was determined. From the data obtained, several recommendations are made concerning the optimum bonding system for the achievement of maximum reliability.

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I. INTRODUCTION

This report is a review of previously reported studies [1-3] funded by NASA/Marshall Space Flight Center [4-6] which investigated high thermally induced failure rates in ceramic chip capacitors solder-bonded to alumina substrates. Failure modes took the form of capacitor chip rupture, capacitor termination debonding, solder joint failure, or substrate metallization lifting. Experimental observations indicated that considerable mechanical force was generated by differential thermal expansion between the substrate material and capacitor chip. Theoretical analyses developed indicate that stresses in rigidly bonded capacitor chips can be calculated from the expression

$$\sigma = E_{chip} (\alpha_{chip} - \alpha_{sub}) \Delta T$$

where σ is the stress, E_{chip} is Young's Modulus of the chip, α_{chip} and α_{sub} are the thermal expansion coefficient of the chip and substrate respectively, and ΔT is the temperature change.

A literature survey was conducted to collect the available thermal expansion, mechanical strength, and Young's Modulus data for each of the homogeneous, polycrystalline materials included in the investigations. These data from the literature are summarized with their sources in Table 1. These data are to be regarded only as starting points as the data vary considerably with sample purity and preparation technique. A further complicating factor in the capacitor property analysis is the composite conductor-dielectric structure of the capacitor. Strictly speaking, the properties of the capacitor should not be those of either conductor or dielectric.

The property behavior for the capacitor will thus be determined by dielectric layer thickness and conductor plate thickness as well as by the

TABLE 1. BULK MATERIALS PROPERTIES FROM LITERATURE SOURCES

	Young's Modulus, 10^{11} N/m^2 (10^6 psi)	Bond Strength, 10^7 N/m^2 (10^3 psi)	Thermal Expansion Coefficient (10^{-6}/°C)
$BaTiO_3$	1.10 (16)	6.6 - 16.3 (9.6 - 23.6)	12.5 - 13.1
TiO_2	2.82 (41)	5.2 - 13.8 (7.5 - 20)	5.39
Al_2O_3	3.93 (57)	2.1 (3.1)	7.91
Platinum	1.45 (21.3)	13.8 - 16.5 (20-24)	8.9
Palladium	1.10 (16.3)	14.5 (21)	11.76

properties of the conductor and dielectric separately. The nature of the dielectric forming and manufacturing technique, which is largely proprietary, may also cause anisotropic properties as a result of preferred orientation of the individual grains of the dielectric material. On the basis of conventional ceramic forming processes, it is anticipated that a thinner dielectric will exhibit a greater degree of anisotropy.

Thermal expansion measurements were made to use with the theoretical model to predict the magnitude of the thermally induced stress. The theoretical prediction was checked using a strain gage technique to allow actual measurement of the stress during thermal cycling. These actual measurements indicated stresses lower than the theoretical prediction. This observation led to the conclusion that compliance or shearing of the substrate/capacitor bond occurs during thermal cycling. Some of our measurements noted the time dependence of this compliance during the course of thermal cycling. Therefore, tests on the effects of thermal cycling upon the cumulative compliance of the bond are reported.

II. THEORY

If we consider a capacitor chip and substrate of the same length at room temperature then, after a temperature change (ΔT), the difference in length of the chip and substrate is given by:

$$\Delta \ell_{chip} = \ell_0 \alpha_{chip} \Delta T \tag{1a}$$

$$\Delta \ell_{sub} = \ell_0 \text{sub} \Delta T \alpha_{sub}$$

$$\text{Difference} = \Delta \ell_{chip} - \Delta \ell_{sub}$$

$$\text{Difference} = \ell_0 (\alpha_{chip} - \alpha_{sub}) \Delta T \tag{1b}$$

where ℓ_0 is the initial length and α is the expansion coefficient. The strain (ϵ) is then

$$\epsilon = \frac{\Delta \ell_{chip} - \Delta \ell_{sub}}{\ell_0}$$

$$\epsilon = (\alpha_{chip} - \alpha_{sub}) \Delta T \quad . \tag{2}$$

If we require that the final length of the chip and substrate be the same after a temperature change (i.e., if they are rigidly bonded together) the strain must be removed by a mechanical stress (σ). The mechanical stress (σ)-strain (ϵ) relationship is

$$E_{chip} = \sigma / \epsilon \tag{3}$$

where E_{chip} is Young's Modulus. This result also requires the justifiable assumption that the substrate is rigid with respect to the much smaller chip. Now, solving equation (3) for strain (ϵ) and equating this strain to the thermal strain given in equation (2), we obtain

$$\epsilon = \frac{\sigma_{chip}}{E_{chip}} = (\alpha_{chip} - \alpha_{sub})\,\Delta T \quad . \tag{4}$$

Solving equation (4) for stress (σ), we obtain

$$\sigma = E_{chip}\,(\alpha_{chip} - \alpha_{sub})\,\Delta T \quad . \tag{5}$$

Assuming that the substrate is rigid in comparison with the chip, equation (5) gives the stress (σ) in the chip for a given temperature change (ΔT). Deformation of the substrate reduces the magnitude of the stress in the chip, but this reduction is negligible. This indicates that the stress calculated above should be an upper bound of the true stress in the capacitor chip during thermal cycling. This derivation also assumes that the capacitor-chip bond is formed at room temperature. If the bond is formed at an elevated temperature, the system will have residual stresses at room temperature.

The force (P) on the chip can be calculated from the relationship

$$\sigma = P/A$$

where A is the cross-sectional area of the capacitor. Note that none of the previous results are dependent upon the capacitor length.

III. INVESTIGATION OF MATERIALS

The thermal expansion results are summarized in Tables 2 and 3. Except possibly in the smaller chips which are somewhat shorter samples, the

TABLE 2. THERMAL EXPANSION DATA SUMMARY FOR CHIP CAPACITORS

Thermal Expansion Coefficient (10^{-6}/°C)			
R11-K1200	R31-K1200	R11-NPO	R31-NPO
1.20	1.48	2.18	1.26
2.04	1.15	1.75	1.47
2.42	1.46	1.77	1.47
1.90	1.36	1.83	1.48
2.06	1.47	2.05	1.38
1.92 avg	1.38 avg	2.12 avg	1.42 avg

TABLE 3. THERMAL EXPANSION DATA SUMMARY FOR TYPE 614 ALUMINA SUBSTRATES

Thermal Expansion Coefficient (10^{-6}/°C)	
Parallel	Perpendicular
7.76	7.76
7.49	8.00
7.15	7.71
7.49	7.44
7.95	8.00
7.56 avg	7.79 avg

experimental error associated with the dilatometric measurements is less than 10 percent. The measured expansion coefficients for the type 614 alumina substrate is 7.68×10^{-6}/°C while that reported in the literature is 7.91×10^{-6}/°C. This result is clearly in good agreement as would be expected for the bulk homogeneous material. The statistical analysis of the parallel-perpendicular observations will not be undertaken because of the inherent lack of correlation of direction from sample to sample. We can conclude that the anisotropy of the substrate is small since, at worst, the expansion coefficient is 7.56×10^{-6}/°C and 7.79×10^{-6}/°C in orthogonal directions.

The thermal expansion coefficient for the R11-K1200 ($BaTiO_3$) capacitors is $1.92 \times 10^{-5}/°C$ as compared with $1.25 \times 10^{-5}/°C$ from literature sources. In a similar comparison the R31-K1200 ($BaTiO_3$) capacitors have an expansion coefficient of $1.38 \times 10^{-5}/°C$.

The thermal expansion coefficient for the R11-NPO (TiO_2) capacitors is $2.12 \times 10^{-5}/°C$ and that for the R31-NPO (TiO_2) is $1.42 \times 10^{-5}/°C$. This compares with $5.39 \times 10^{-6}/°C$ for the bulk TiO_2 reported in the literature.

The results of calculations of the stresses and forces induced by thermal cycles are given in Table 4. These results were calculated from the measured thermal expansion and Young's Modulus data from the literature. It should be noted that the modulus data for bulk materials are strictly applicable to the composite capacitor structure although the probable error for a high dielectric-conductor thickness ratio is small.

TABLE 4. CALCULATED STRESSES AND FORCES FROM THERMAL EXPANSION MISMATCH FOR CAPACITORS ON TYPE 614 ALUMINA SUBSTRATES

Capacitor Type	Reported Failure Stress 10^7 N/m² (psi)	Stress[c], 10^7 N/m² (psi)		Force, N (lb)	
		25 to -65°C	25 to 125°C	25 to -65°C	25 to 125°C
R31-NPO (TiO_2)	5.17-13.8 (7 500-20 000)[a]	16.5 (24 000)	23.0 (33 400)	596 (134.0)	832 (187.0)
R31-K1200 ($BaTiO_3$)	6.61-16.3 (9 600-23 600)[b]	4.88 (7 080)	6.78 (9 840)	176 (39.6)	252 (56.6)
R11-NPO (TiO_2)	5.17-13.8 (7 500-20 000)[a]	34.3 (49 800)	47.7 (69 290)	355 (79.7)	494 (111.0)
R11-K1200 ($BaTiO_3$)	6.61-16.3 (9 600-23 600)[b]	4.24 (6 160)	5.89 (8 550)	43.9 (9.86)	60.9 (13.7)

Note: a. Data from two sources.
b. Strength depends upon sample treatment — average as received strength is 11 700 psi.
c. Capacitors in tension from 25 to -65°C and in compression from 25 to 125°C.

Table 4 compares the tensile stresses in the capacitors with the reported mechanical strength of the materials. It is again important to note that the mechanical strengths are for homogeneous bulk samples which are considerably different from the capacitors. Although this introduces some uncertainty as to

the breaking strength of the capacitors, it is unlikely that the strength is significantly enhanced by the presence of the stronger conductor plates since they are much thinner than the dielectric material. It is evident that the NPO (TiO_2) type capacitors are clearly stressed above the failure strength of the capacitor body itself. The K1200 ($BaTiO_3$) capacitors are not stressed above their reported failure strength but they are loaded to the point where essentially no concentrators could cause the stress to locally exceed the breaking strength, thus causing the K1200 capacitors to fail.

This discussion considers only failure or rupture of the capacitor body. If we consider the load or force on terminations, further problems are evident. Table 5 summarizes the result of force calculations conducted in this work and the reported measurements from a recent NASA/MSFC report [5]. The data measured, e.g., 7.1 N (1.6 lb) for R11-K1200, are for rupture of two terminations while the calculated 44 N (9.86 lb) force is applied to only one termination. We thus have a situation where the calculations indicate a force of 44 N while an independent measurement indicates a breaking of the termination-solder bond at 3.6 N (0.8 lb). Similar large overloads are indicated in Table 5 for type R31-K1200 capacitors.

TABLE 5. CALCULATED FORCES UNDER CYCLING AND REPORTED SHEAR FORCE AT FAILURE

	Calculated Force, N (lb)		Measured Force, N (lb)	
Capacitor Type	25 to -65°C	25 to 125°C	Solder to Au Conductor	Solder to Au-Pd Conductor
R11-K1200	44.0 (9.9)	60.9 (13.7)	7.12 (1.6)	4.45 (1.0)
R11-NPO	3 5 (79.7)	494 (111.0)	—	—
R31-K1200	176 (39.6)	252 (56.6)	16.5 (3.7)	10.7 (2.4)
R31-NPO	596 (134.0)	832 (187.0)	—	—

This discussion of two failure modes indicates that in all cases the rigidly bonded capacitor-substrate system should fail in thermal cycling. In all instances it appears that the termination should fail before the capacitor body but it has been reported [6] that the capacitor body ruptures in some instances. The rupture of the apparently stronger link, e.g., the capacitor, indicates that this analysis predicts a higher value of failure load for the capacitor body rupture than is observed in practice. This is a consequence of the capacitor being weaker than the corresponding bulk material, r, of defects causing local stress concentrations.

It is thus clear that rigidly bonded capacitor chip-substrate assemblies should fail if a rigid bond exists. It is clear that solders are not truly rigid since many solder bonded capacitor chips survive some thermal cycling conditions. The failure under extended cycling tests appears to be a result of either fatigue or work hardening of the solder which leads to a more rigid bond. Although an ideally rigid bond is desirable from a mechanical reliability point of view, this semi-rigid bond is the immediate cause of thermal cycling failures.

IV. EXPERIMENTAL PROCEDURE

Representative samples of ceramic chip capacitors were bonded to alumina substrates using standard 10-Sn 90-Pb solder, 60-Sn 40-Pb solder, an indium solder, a two component conductive epoxy, and a nonconductive epoxy. A strain gage was attached to each capacitor as shown in Figure 1. A matching strain gage was attached to a capacitor bonded at one end only. This capacitor was allowed to expand and contract freely through temperature cycling and was used as a standard for the strain gage measurements. Two capacitors with attached strain gages were placed in a temperature chamber and cycled from -50 to 125°C while the strain was monitored using a standard strain gage bridge. The value of strain measured represents a difference in the dimensional changes of the two capacitors. Thus, the difference appears as a negative value in $\mu m/m$ for the high temperature range and a positive value in $\mu m/m$ for the low temperature range. Using these measured values, strain in $\mu m/m$ was plotted against time for each of the capacitor samples.

The modulus of elasticity was determined by attaching a strain gage to a chip capacitor and then mounting the capacitor/strain gage assembly vertically on the substrate. A compressive load (stress) was applied to the capacitor while the strain was monitored. The compressive load was plotted against strain to determine the modulus of elasticity. This assembly is illustrated in Figure 2.

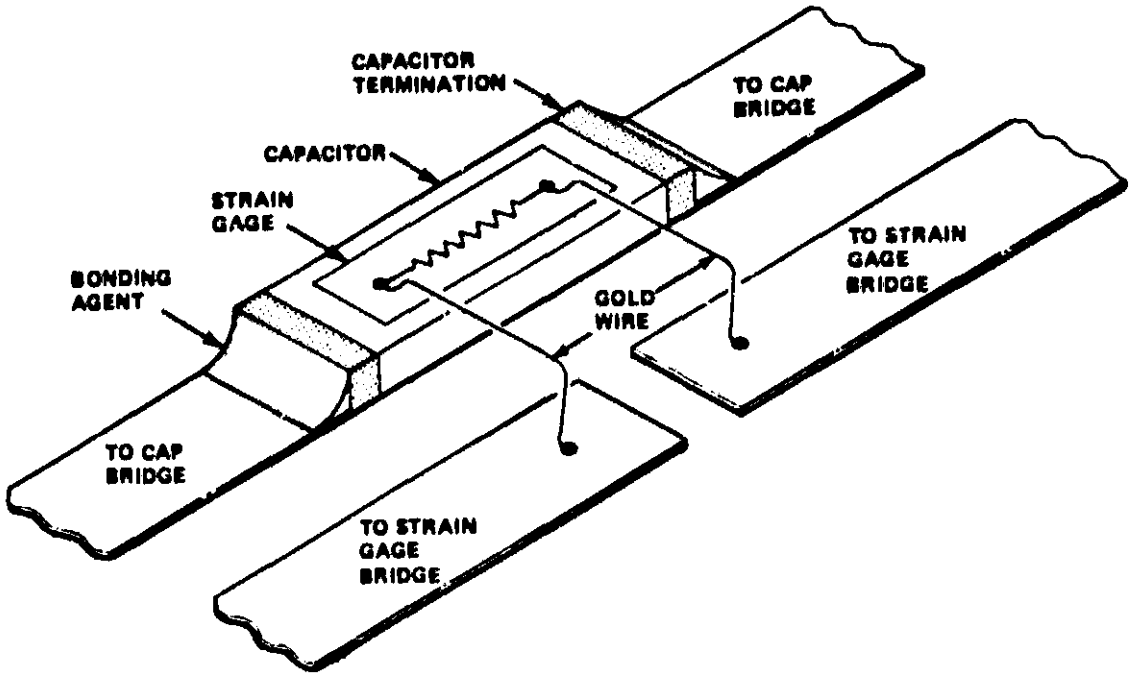

Figure 1. Capacitor assembly for strain measurements as a function of time and temperature.

As a separate part of this investigation, a capacitor chip of the same type was bonded with a low melting indium solder. This solder was employed because the higher melting temperatures necessary for conventional solders would have degraded the strain gage to capacitor bonding system and led to difficulties. The indium bonded capacitor was held at 165°C and the solder was allowed to melt. After the melting occurred, the substrate and chip were carefully removed from the environmental chamber and allowed to cool in ambient conditions. The strain introduced as solidification and cooling proceeding was monitored using the strain gage.

V. EXPERIMENTAL RESULTS

As a test of the reproducibility of the technique, three samples from the same lot of 0.1 μF capacitors were mounted directly on a substrate using non-conductive epoxy. The capacitor was held at 25°C and a strain gage reading was recorded. The capacitor/substrate was then cycled to 125°C as indicated

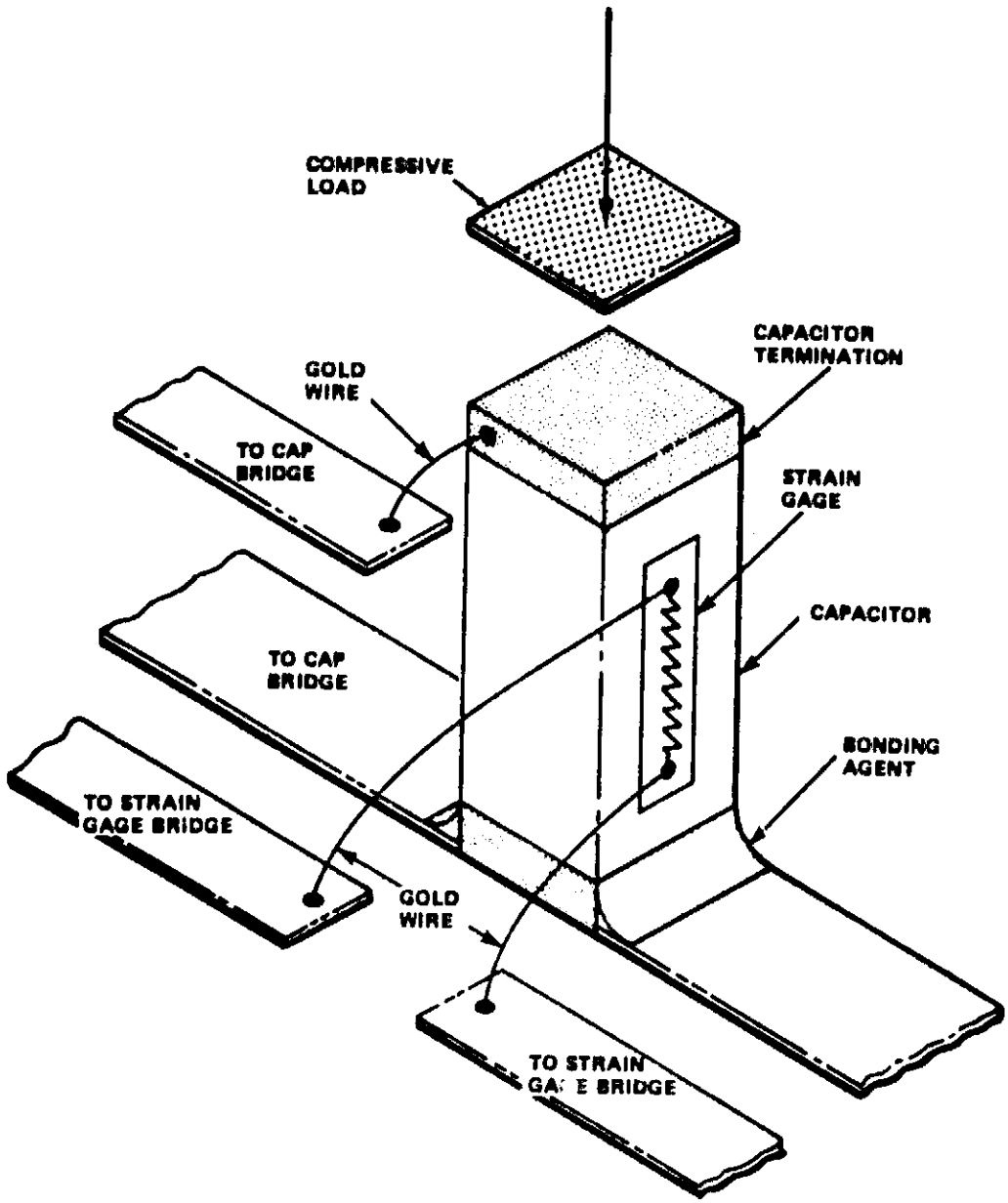

Figure 2. Capacitor assembly for modulus measurements.

in Figure 3. The general features of each capacitor are quite similar even though the transient features of the curves are slightly different. These transient features are discussed later in this report. The capacitor was compressed by the thermally induced force and the magnitude of the strain ranged from -40 to -580 μm/m. This thermal strain decreased slightly with time. When the samples were returned to room temperature, they were slightly elongated.

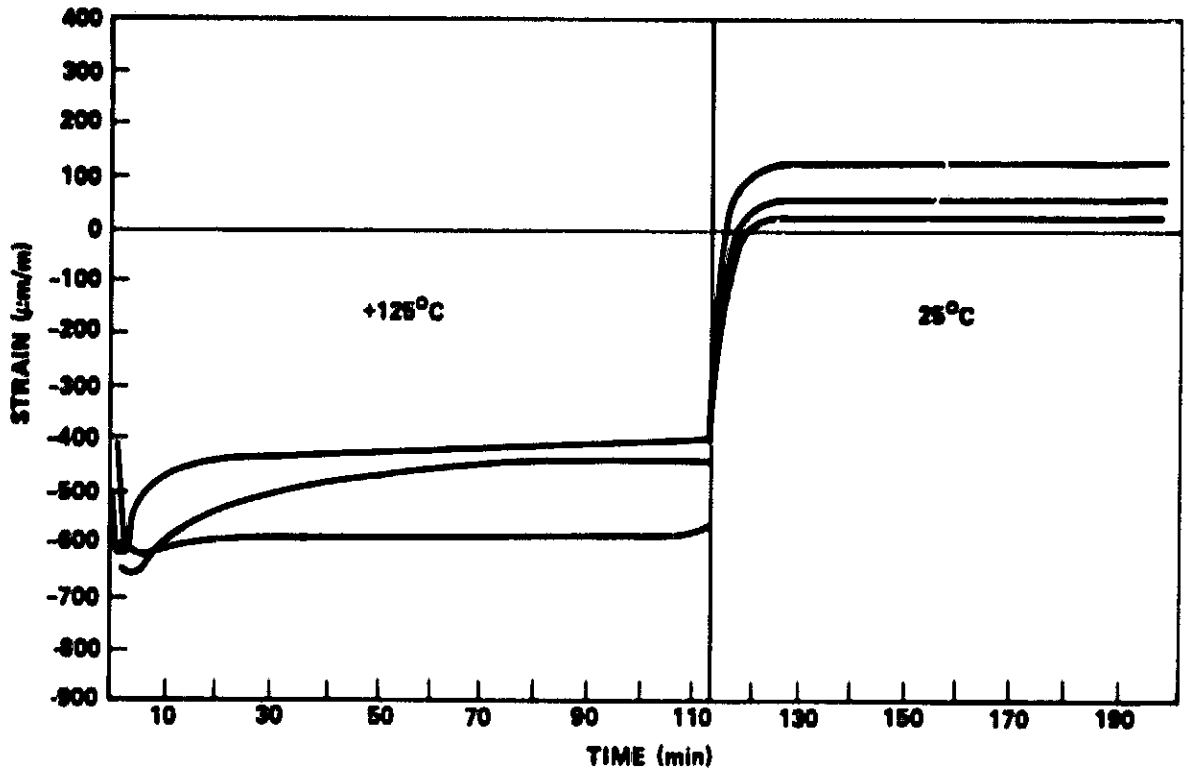

Figure 3. Strain plot as a function of time and temperature for 0.1 μF capacitor bonded to alumina substrate with nondestructive epoxy (3 samples).

To determine the magnitude of the force responsible for the observed strains, it was necessary to measure the modulus of elasticity of the capacitors. This measurement was carried out as previously described and the results are plotted in Figure 4. It should be noted that the modulus of elasticity of "pure" $BaTiO_3$ is 1.1×10^{11} N/m^2 (16×10^6 psi)[5] while that of the 0.1 μF chip is 5.5×10^{10} N/m^2 (8×10^6 psi) and the 0.27 μF chip is 2.2×10^{11} N/m^2 (32×10^6 psi). Considering the thermally induced strain of approximately -500 μm/m observed in Figure 3 and referring to the corresponding measurement in Figure 4, the thermal stress in the 0.1 μF capacitors during the 125°C cycle is roughly 2.75×10^7 N/m^2 (4×10^3 psi).

A similar experiment depicted in Figure 5 was conducted for a 0.1 μF capacitor mounted with a 60/40 solder. This sample was held at 25°C, cooled to -50°C, heated to 125°C, and returned to 25°C while the strain was monitored. The capacitor length increased by approximately 160 μm/m during the cycle at -50°C. However, during this period, the elongation decayed to approximately 150 μm/m. This decay, commonly known as the ratcheting phenomena, is a

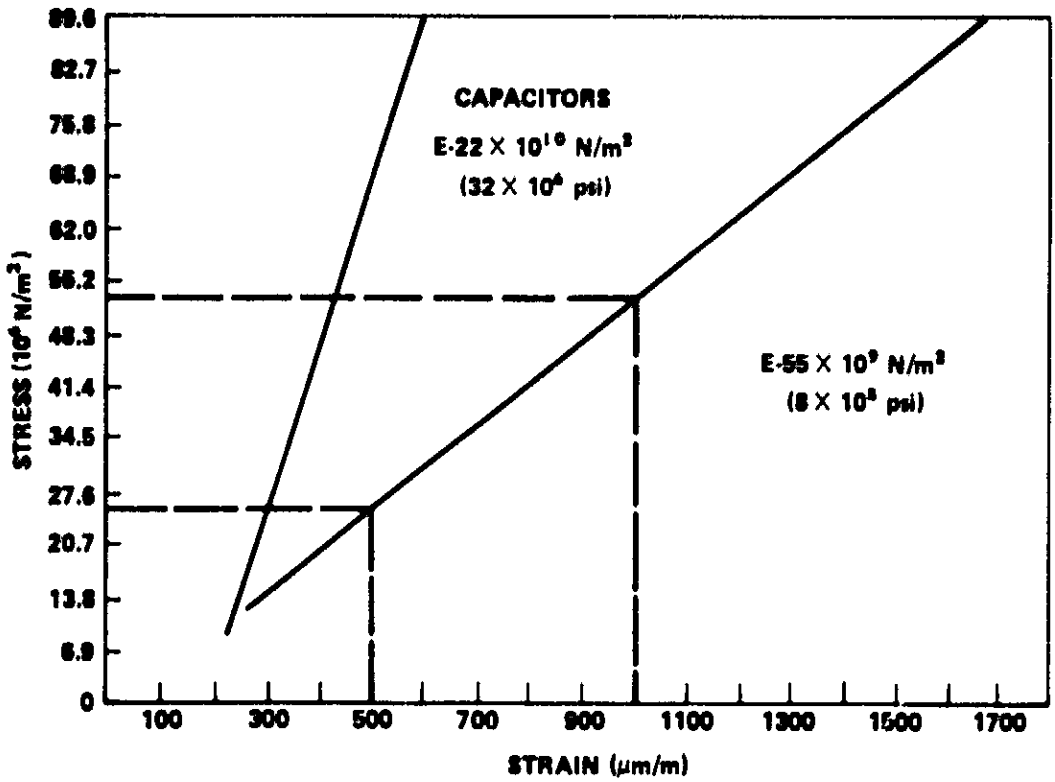

Figure 4. Stress-strain plot for 0.1 μF and 0.27 μF capacitors.

subject for more intensive study. Ratcheting is a term used to describe the effect caused by thermal cycling of a bond which allows flow and stress. After each cycle, during which flow occurs, the stress during the next cycle is larger by the amount of flow which occurred during the previous cycle. As the capacitor was cycled to 125°C, it was compressed by approximately -425 μm/m and upon cooling to 25°C, the capacitor was "permanently" shortened by approximately 50 μm/m.

The results of the same experiment on a 0.1 μF capacitor mounted with a gold conductive epoxy are shown in Figure 6. It should be noted that the strains in this capacitor are higher than those observed above and little decay of the strain occurred during holding at temperature.

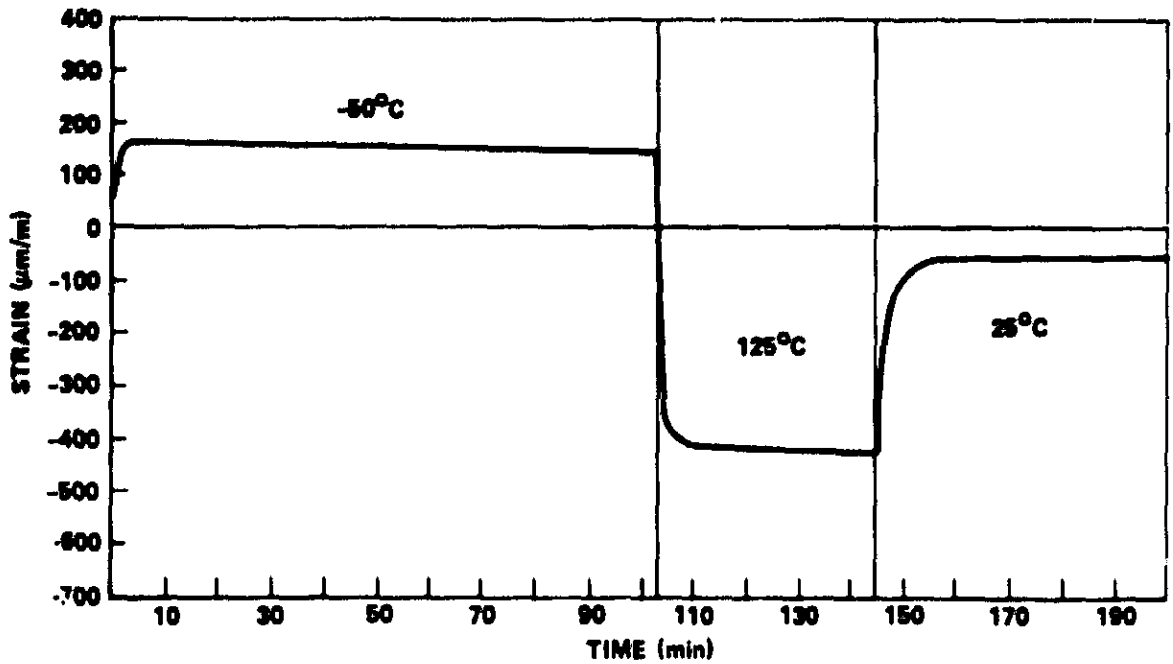

Figure 5. Strain plot as a function of time and temperature for 0.1 μF capacitor bonded to alumina substrate with 60/40 solder.

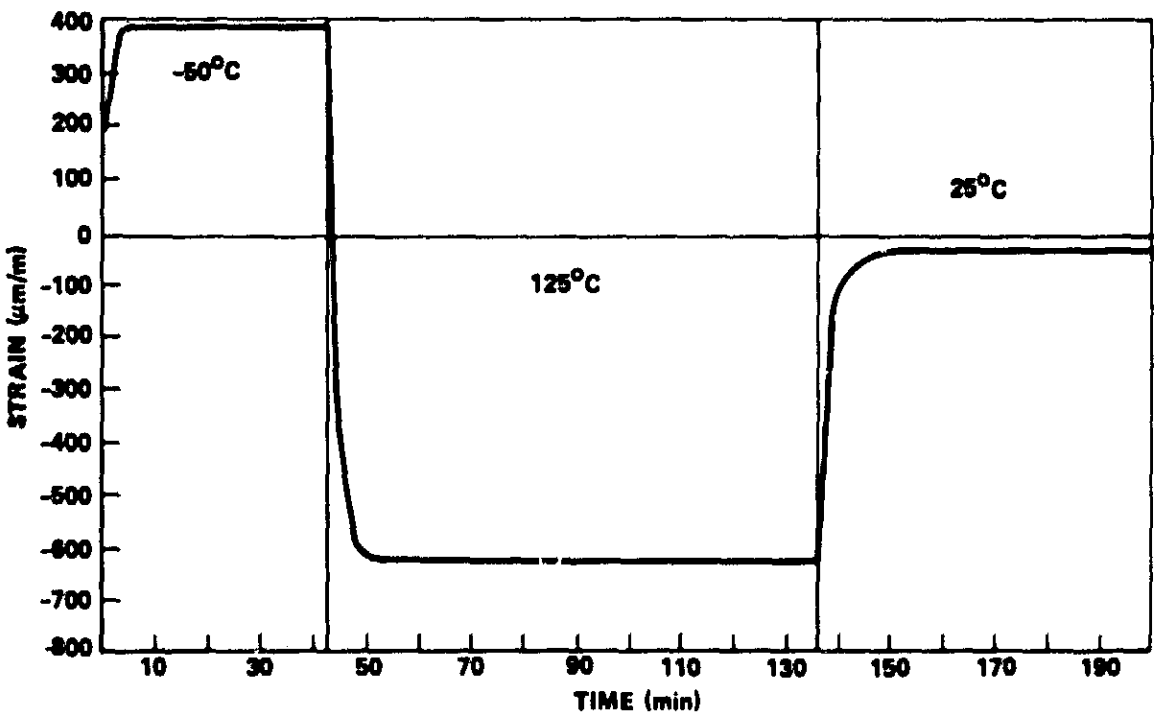

Figure 6. Strain plot as a function of time and temperature for 0.1 μF capacitor bonded to alumina substrate with gold conductive epoxy.

A similar experiment using indium solder was conducted and the results are shown in Figure 7. These results for the -50°C cycle are quite similar to those for other bonding techniques. However, the strain observed during the 125°C cycle was initially quite large but rapidly decayed to a small positive value. As this sample was cooled to 25°C, the strain increased to a positive value of 300 μm/m and decayed to approximately 175 μm/m. This result is quite unlike those of the other bonding techniques, indicating that the capacitors bonded with indium solder have very little strain at 125°C. Similar curves were obtained for a series of 0.27 μF capacitors using the same bonding techniques. The results of these experiments are summarized in Tables 6 and 7.

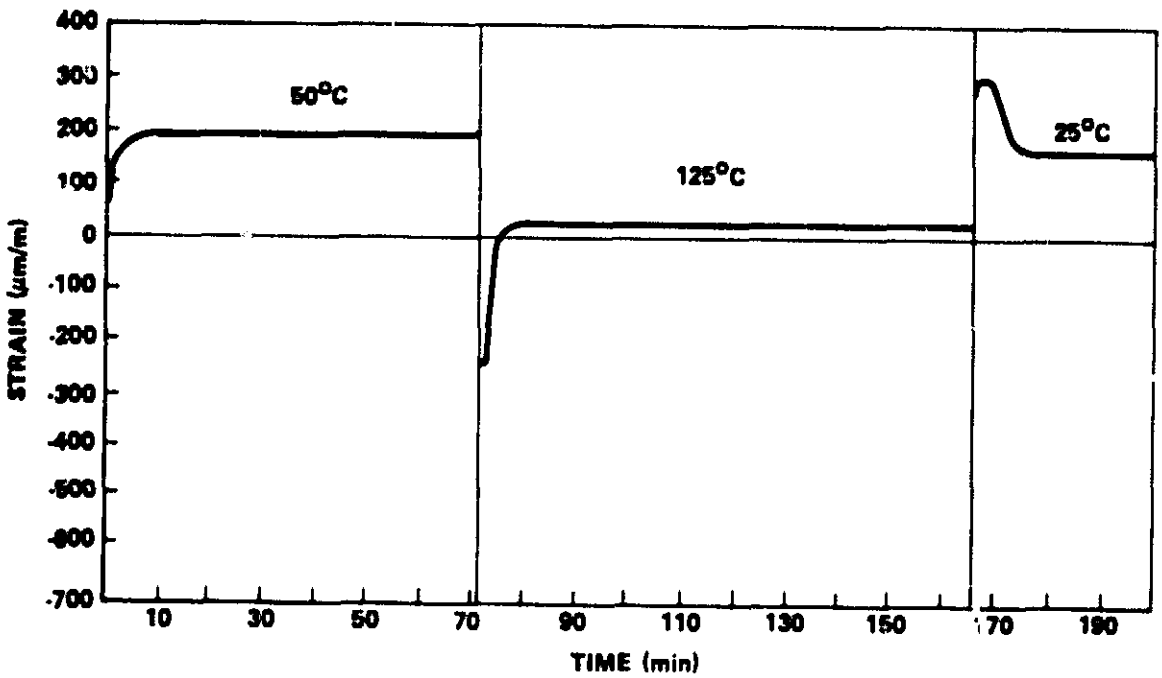

Figure 7. Strain plot as a function of time and temperature for 0.1 μF capacitor bonded to alumina substrate with indium solder.

Thermal cycling tests of four cycles -50 to 125°C were conducted to investigate cumulative strain. The results of the thermal cycling of a capacitor chip bonded with the 60/40 type solder are shown in Figure 8. This experiment indicates that as the measurements began at 25°C, the strain was initially zero and as the sample was heated to 125°C during the first 125°C cycle, the length of

TABLE 6. EXPERIMENTAL STRESS AND STRAIN VALUES FOR CERAMIC CHIP CAPACITORS

Sample Code	Strain (-50°C) μm/m	Strain (125°C) μm/m	Stress (-50°C) 10^6 N/m^2 (psi)	Stress (125°C) 10^6 N/m^2 (psi)
NCE 0.1	—	-500	—	1.6 (4 000)
AuCE 0.1	390	-630	2.15 (3 120)	34.7 (5 040)
60/40S 0.1	165	-425	9.1 (1 320)	23.4 (3 400)
InS 0.1	190	-240	10.5 (1 520)	13.2 (1 920)
NCE 0.27	55	-235	12.1 (1 760)	62.9 (9 120)
AuCE 0.27	170	-690	37.5 (5 440)	132.0 (22 080)
60/40S 0.27	70	-150	15.4 (2 240)	33.1 (4 800)

Notes: 1. Strain values represent the difference between the standard capacitor and the bonded capacitor.

2. Capacitors are in tension during the low temperature cycle and compression during the high temperature cycle.

3. Sample Code -- acronym + capacitance in μF:

NCE — noncond epoxy
AuCE — gold cond epoxy
InS — indium solder
60/40X — 60/40 solder

TABLE 7. COMPARISON OF OBSERVED AND THEORETICAL STRESSES

	25 to -50°C	25 to 125°C
Bonding Agent	10^6 N/m^2 (psi)	10^6 N/m^2 (psi)
Ideal (Theoretical)	40.7 (5 900)	67.8 (9 840)
Nonconductive Epoxy	—	27.6 (4 000)
Gold Conductive Epoxy	21.5 (3 120)	34.7 (5 040)
60/40 Solder	9.1 (1 320)	23.4 (3 400)
Indium Solder	10.5 (1 520)	13.2 (1 920)

Note: Capacitors are in tension during the low temperature cycle and compression during the high temperature cycle.

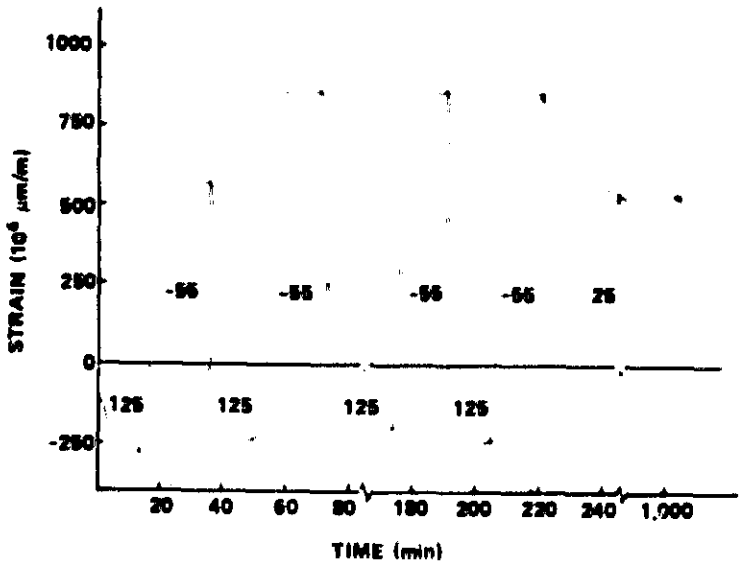

Figure 8. Strain as a function of time during thermal cycling for 0.1 µF capacitor bonded to alumina substrate with 60 Sn-40 Pb solder. Numbers refer to the temperature of each portion of the cycle.

the capacitor chip decreased by approximately 250 µm/m; that is, the length decreased by approximately 250 ppm. As the sample was cooled to -55°C, the length increased by approximately 600 ppm or the sample was stretched by the 600 ppm. During the next cycle to 125°C, the sample was compressed by somewhat less than the first cycle but the second cycle to -55°C shows a considerable increase in strain over the first cycle to -55°C. After this first cycle, the strains become almost reproducible between approximately 800 ppm elongation on the -55°C portion of the cycle and approximately 200 ppm compression on the 125°C portion of the cycle. It is especially noteworthy that after 4 cycles, the sample does not return to its original length at room temperature. There is a net elongation of the sample of approximately 550 ppm as a consequence of only four cycles.

The results of the thermal cycling of a chip bonded with type 90/10 solder are shown in Figure 9. This sample behaves in a manner quite similar to the 60/40, but the magnitude of the strain on the hot and cold side of the cycle is larger. The strain does not exhibit the transient behavior observed in the 60/40 sample, but there are minor differences in the first and subsequent cycles. The sample elongates by somewhat over 1200 ppm on the -55°C portion of the cycle and is compressed by slightly less than 500 ppm on the 125°C excursion.

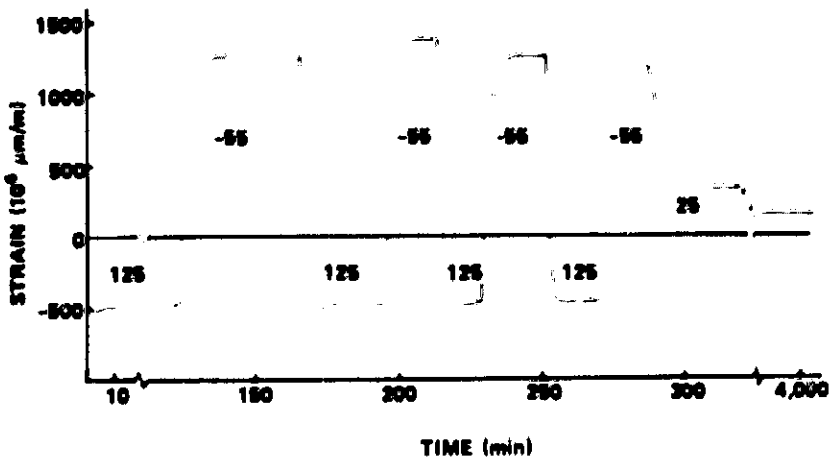

Figure 9. Strain as a function of time during thermal cycling for 0.1 μF capacitor bonded to alumina substrate with 90 Sn-10 Pb solder. Numbers refer to the temperature in centigrade for each portion of the cycle.

The experimental measurement of the strain in the chip as the indium solder solidifies and cools is shown in Figure 10. At zero time on this plot, the sample was at 165°C and was placed in ambient air at 25°C. As the sample cooled, some rapid changes in length were observed at times under 1 minute and these seem to be of the negative or compressive type. As the cooling proceeds, the strain changes to a large tensile elongation of almost 1200 ppm; and as time and cooling proceeds,this strain decays to a value near 1000 ppm. This value does not decay significantly over a period up to 3000 minutes.

VI. DISCUSSION

These results exhibit several effects which were anticipated and some which were unexpected. The data compared well with theoretical results from previous work in Table 7. The observed stresses are lower than the theoretical stresses for all capacitor bonds examined. Hence, all of the bond types were found to exhibit some degree of stress relaxation. The transient effects are quite different among the bonding systems examined and will be discussed individually.

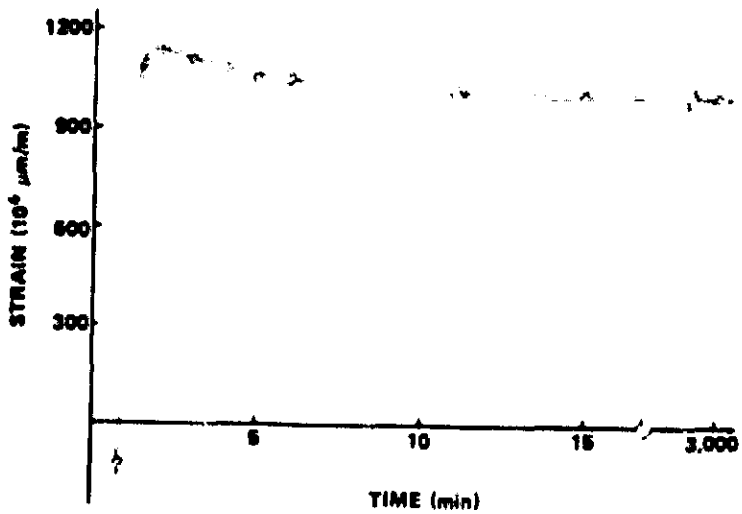

Figure 10. Strain as a function of time during cooling from 165°C to room temperature for a 0.1 μF chip bonded to alumina substrate with indium alloy 235 solder.

The nonconductive epoxy bond exhibits a large strain as it is heated and this strain decays slightly during holding at 125°C. As this sample is returned to room temperature, the decay in strain at 125°C appears as a "permanent" strain at room temperature, thus indicating a plastic flow in the capacitor/substrate bond. The 60/40 sample depicted in Figure 5 exhibits some strain decay with time at -50°C. After this sample is returned to room temperature, this strain remains but is of the opposite sign of that in the nonconductive epoxy. The gold conductive epoxy sample shown in Figure 6 differs from the others. No significant deformation of the bond and no decay of the strain during holding at temperature was evidenced, and this sample returned to its original length within the experimental error. This indicates that the gold conductive epoxy bond does not shear appreciably and thus has the highest stress of any of the bonding techniques examined.

The four cycle measurements on the 60/40 and 90/10 solders indicate that thermal cycling leads to a net cumulative strain in the capacitor chips. The softer or lower melting 60/40 solder seems to lead to a larger cumulative effect with thermal cycling. This difference is probably a consequence of the more compliant nature of the 60/40 solder. The experiments have not examined these systems after a large number of cycles where other effects may take

control; however, for the small number of cycles examined, it is clear that the 60/40 type bonding system is more markedly affected than the 90/10.

The indium solder shown in Figure 7 exhibits an especially peculiar behavior during thermal cycling. The sample appears to behave in a manner analogous to other samples during cycling to -50°C; however, as the sample is cycled to 125°C, the strain rises to a large value but decays to a value near zero within 5 minutes. This solder melts at 151°C and, according to the manufacturer, is plastic in the range of 115 to 125°C. The observed behavior is thus the result of plastic relaxation of the bond which totally relieves the thermal stress in the capacitor chip. This plastic relaxation leaves the sample matched to the substrate at 125°C. Upon cooling below the plastic flow temperature of the bonding alloy, the differential thermal expansion is reflected as a permanent strain of approximately 175 μm/m. If this sample is subsequently cycled to -50°C, the strain from differential thermal expansion will increase to much larger values and the chip will be stressed to very near its failure point.

This discussion of thermal cycling neglects the effect of the initial stress or strain built into the bonded capacitor during the initial soldering operation. All of our measurements except the soldering study take as their starting point the capacitor at room temperature. The capacitors are strained by the initial soldering operation as is illustrated in Figure 10. These results indicate that the capacitor is initially elongated by approximately 1000 ppm when a low melting indium solder is employed. It can be inferred that a higher melting solder will have a larger initial strain as the temperature change from solidification to room temperature is larger. This would suggest that the 90/10 solder probably has a larger initial strain than the 60/40; hence, if either sample fails during the soldering operation, it will more likely be the 90/10. The net effect is that the 60/40 is apparently more susceptible to the cumulative effects of thermal cycling, but the 90/10 is more likely to fail during the soldering or fabrication process. We would speculate that the lower melting indium solder would exhibit still more pronounced thermal cycling sensitivity, but this solder will likely behave somewhat differently because of the proximity of the 125°C temperature cycle to its melting point of 135°C.

VII. CONCLUSIONS

a. Thermal cycling of solder-bonded capacitor chips leads to cumulative length changes which are no doubt responsible for their eventual mechanical failure during thermal cycling.

b. The higher melting or harder solders appear to be less sensitive to the effects of thermal cycling. The largest strains observed were in the epoxy bonding system.

c. The higher melting solder apparently has a higher initial strain introduced by the soldering operation.

d. Strains introduced during the soldering operation with indium solder are large and decay somewhat upon cooling.

e. Due to the extreme compliance of the indium solder bond at 125°C, the reliability over the full temperature range is questioned. A small shock or vibration at this temperature could easily reorient or dislodge the capacitor.

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APPROVAL

THE RELATIONSHIP BETWEEN RELIABILITY AND BONDING TECHNIQUES IN HYBRID MICROCIRCUITS

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The information in this report has been reviewed for security classification. The report is determined to be unclassified and contains no information concerning Department of Defense or Atomic Energy Commission programs.

This document has also been reviewed and approved for technical accuracy.

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