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A FIELD-EFFECT TRANSISTOR (FET) MODEL

FOR ASAP

SPACE GUIDANCE CENTER
HUNTSVILLE ENGINEERING OPERATION

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LIST OF DEFINITIONS

A. Field-Effect Transistor (FET)

D, drain terminal

G, gate terminal

S, source terminal

V_{ds}, drain-source voltage

V_{gs}, gate-source voltage

V_p, pinch-off voltage, the gate-source voltage which reduces the drain current to the reverse saturation current of the gate-channel diode.

I_d, drain current

I_{dss}, saturation drain current with zero gate-source bias voltage at any drain-source voltage in the pinch-off region below breakdown.

$I_{d(on)}$, I_{dss} when measured at a specified drain voltage in the pinch-off region

B. Hypothetical Transistor in FET Model

I_b, base current

LIST OF DEFINITIONS

I_c, collector current

I_e, emitter current

V_{be}, base-emitter voltage

β, current gain = $\frac{I_c}{I_b}$

LIST OF ILLUSTRATIONS

I. INTRODUCTION

IBM has been applying ASAP (Automated Statistical Analysis Program) in the analysis of electrical circuits. Recently the field-effect-transistor (FET) has been appearing in many of these circuits. Since ASAP accepts circuits containing only resistors voltage and current sources, diodes, and conventional transistors, a FET model consisting of these components has to be derived to be able to use ASAP on circuits containing the FET.

This report describes the derivation of the circuitry of a FET Model, the procedure for adapting the Model to ASAP and the results of applying ASAP on this Model.

This work was done under NASA Contract Number 8-14000 for Marshall Space Flight Center.

II. THE FET MODEL

A FET Model was derived consisting of a resistor, a current generator and a hypothetical transistor. The schematic of the model is shown in Figure 1.

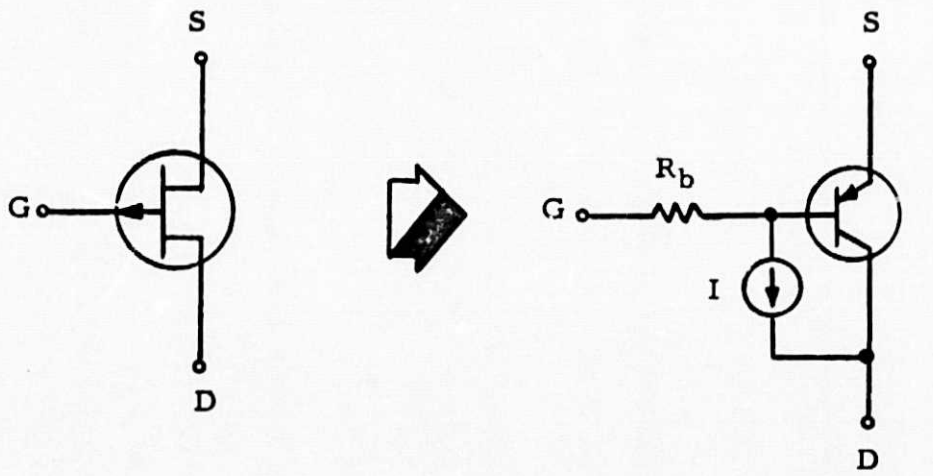


Figure 1. Schematic of a FET Model

In the Model R_b is a resistance in the order of megohms which simulates the high gate input impedance of the FET.

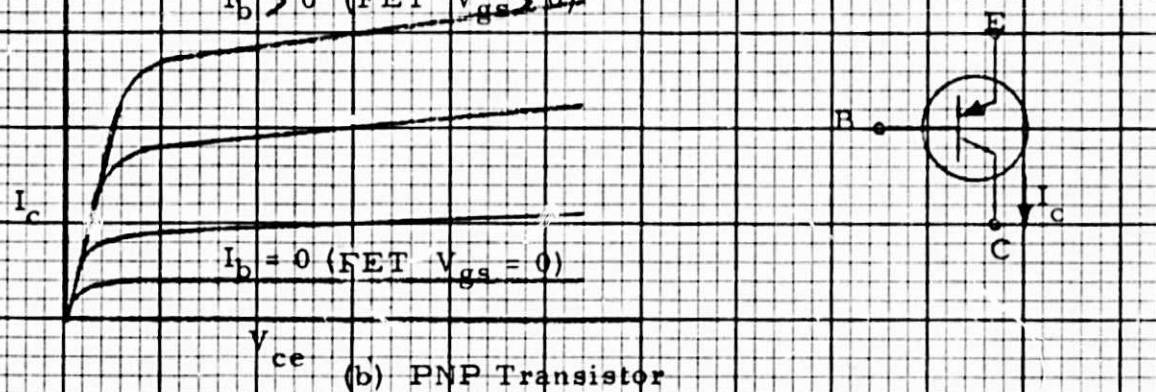
To simulate the FET electrical behavior, a constant current source is required to provide a source of transistor base saturation current independent of the base-collector voltage. The constant current source was derived through consideration of the characteristics of the transistor without any other elements and then with a feedback resistor. The transistor characteristics corresponding to the FET characteristics would be the collector current versus collector-emitter voltage curves for constant base currents where the collector current, collector-emitter voltage and base current of the transistor correspond respectively to the drain current, drain-source voltage and gate current or voltage of the FET. The characteristics of a PNP transistor operating in the common collector mode and of the FET are shown in Figure 2.

From Figure 2 it can be seen that for low base currents the transistor is almost turned off while the opposite condition must exist to give FET action. Thus a path for the base saturation current must be provided to allow the transistor to be saturated at low base currents. A resistor inserted between the base and collector terminals would provide such a path.

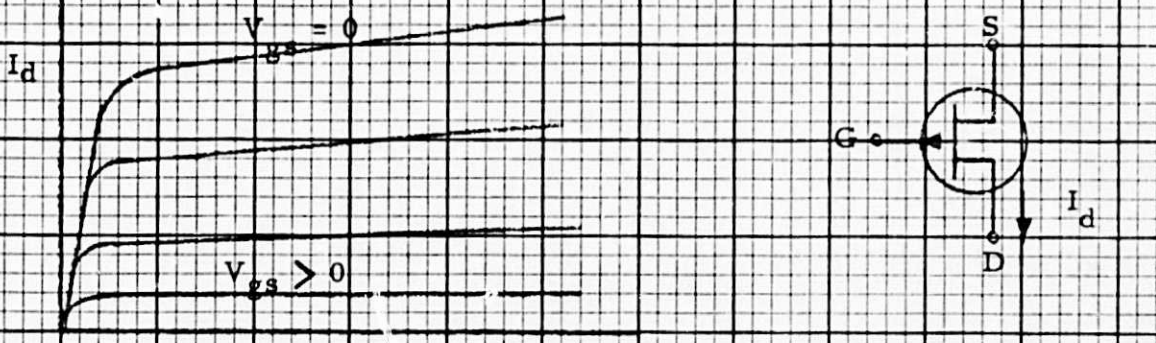
Figure 2

Characteristics of
(a) Field Effect Transistor
(b) PNP Transistor
(c) Transistor with Feedback Resistor

(c) Transistor with Feedback Resistor



(b) PNP Transistor



(a) Field-Effect Transistor

It was found that the transistor with the feedback resistor did not give the FET action. The characteristics of the transistor with feedback resistor are shown in Figure 2. This transistor circuit did not simulate the FET behavior because even though the resistor provided the base current path, the base current was now a function of the base-collector voltage. Thus, another condition had to be imposed. The condition was that the source of transistor base saturation current be independent of the base-collector voltage. The constant current source meets the description of the required element.

The above conditions may be described mathematically by the following expressions. From Figure 2 for the transistor with feedback resistor,

$$I = I_c + I_b + I_g$$

$$I_c = f(I_b) \qquad (1)$$

$$I_b = g(V_{bc})$$

$$I = F(V_{bc}) + I \text{ where } F(V_{bc}) = f\left[g(V_{bc})\right]$$

$$g(V_{bc}) \gg I_g$$

It may be noted that I_g accounts for the gate leakage current.

It is the last equation in (1) which controls the behavior of the characteristics of the transistor with feedback resistor and which must be modified to generate the FET characteristics.

To realize the FET behavior, the following condition must be satisfied.

$$g\,(V_{bc}) \ll I_g$$

Physically, the mathematical expressions define a requirement for a base current which is independent of the base collector voltage. And it is precisely the constant current source which enables this condition to be satisfied.

A PNP transistor is used for the Model to be consistent with the voltages applied to the FET terminals.

The validity of the Model was verified experimentally in the laboratory to the extent that the characteristics of the Model behaved in a similar manner to that of the FET.

III. THE APPLICATION OF THE MODEL IN ASAP

For application of the model in ASAP, the characteristic I_c vs. V_{be} and a β must be defined for a hypothetical transistor. For the determination of these two parameters, the circuit equations must be solved for the model.

Let the voltages and currents be defined as shown in Figure 3.

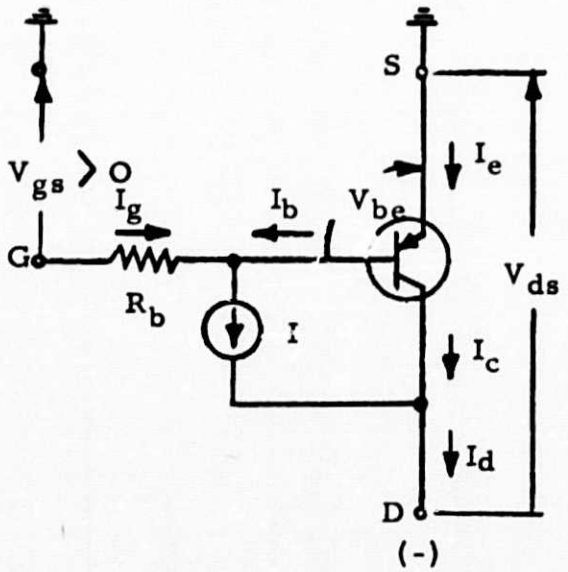


Figure 3. Currents and Voltages in the FET Model

Then $I_d = I + I_c = I_g + (\beta + 1) I_b$

$I = I_g + I_b = \text{constant}$

$$I_g = \frac{V_{gs} + V_{be}}{R_b}$$

$I_b = (1 - \alpha) I_e$

$I_c = \alpha I_e$

$$\beta = \frac{\alpha}{1 - \alpha}$$

A value for R_b is assumed. From the FET data a value I for the current source is calculated. A value for V_{be} is assumed from which β is calculated. Finally, from the FET data the I_c vs V_{be} curve is generated.

In application on a typical FET, the detailed steps will now be described to obtain the necessary information to use a 2N2497 P-channel FET.

The value I for the current source may be determined by considering the FET when it is pinched-off, and $V_{be} = O$, $I_b = 0$. Then, the only current flowing in the circuit is the gate leakage current or I_g. The pinch-off voltage, V_p, for the nominal static

characteristic of the 2N2497 data is

$$V_p = V_{gs\ (pinch\text{-}off)} = 2.07 \text{ volts}$$

Therefore, $I = I_g = \frac{V_{gs} + V_{be}}{R_b} = \frac{2.07}{10^7} = .207\ \mu a$

having assumed a value $R_b = 10$ Megohms.

Calculations will be made using data along a constant drain-source voltage line of the FET characteristics at $V_{ds} = 2$ volts. From the data

$$\left.\begin{aligned} I_d &= 1.65 \text{ ma} \\ V_{gs} &= 0 \end{aligned}\right\}$$

A value for V_{be} is now assumed. Since V_{ds} corresponds to V_{ce} of the transistor, V_{be} cannot exceed V_{ds}, or $V_{be} < V_{ds}$. Therefore, let

$$V_{be} = 1.90$$

$$I_g = \frac{V_{gs} + V_{be}}{R_b} = \frac{1.90}{10^7} = .190\ \mu a$$

$$I_b = I - I_g = .017\ \mu a$$

$$\beta = \frac{I_d - I_g}{I_b}$$

then, $$\beta = \frac{1.65 \times 10^{-3} - 2.07 \times 10^{-7}}{1.7 \times 10^{-7}} - 1 \approx 10^5$$

From the data $\left.\begin{aligned} I_d &= 1.30 \\ V_{gs} &= .2 \end{aligned}\right\}$

Thus, $$I_b = \frac{I_d - I_g}{\beta + 1} \approx \frac{I_d}{\beta} = \frac{1.30 \times 10^{-3}}{10^5} = .013\ \mu a$$

for $I_d \gg I_g$ and $\beta \gg 1$.

Then, $I_g = I - I_b = .207 - .013 = .194\ \mu a$

and $V_{be} = I_g R_b - V_{gs} = 1.94 - .2 = 1.74$

The process is continued until a sufficient number of points have been obtained to define the I_c vs V_{be} curve ($I_c = \beta I_b$). The transistor curve generated is shown in Figure 4.

The Model is now ready to be applied in ASAP. The circuit used to test the Model in ASAP is shown in Figure 5. To apply the circuit, a topological description of the circuit is required in the input data to ASAP.

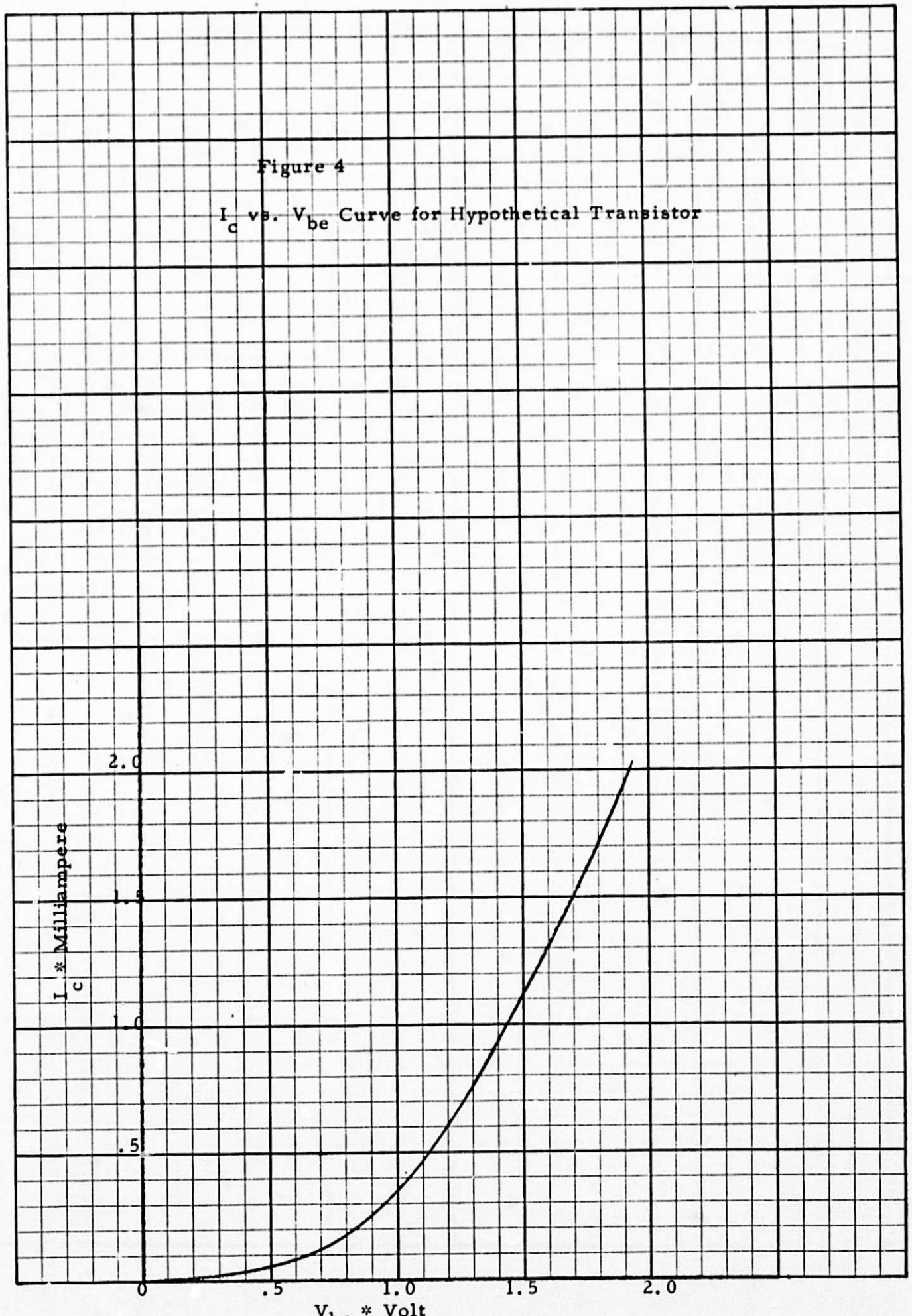


Figure 4

I_c vs. V_{be} Curve for Hypothetical Transistor

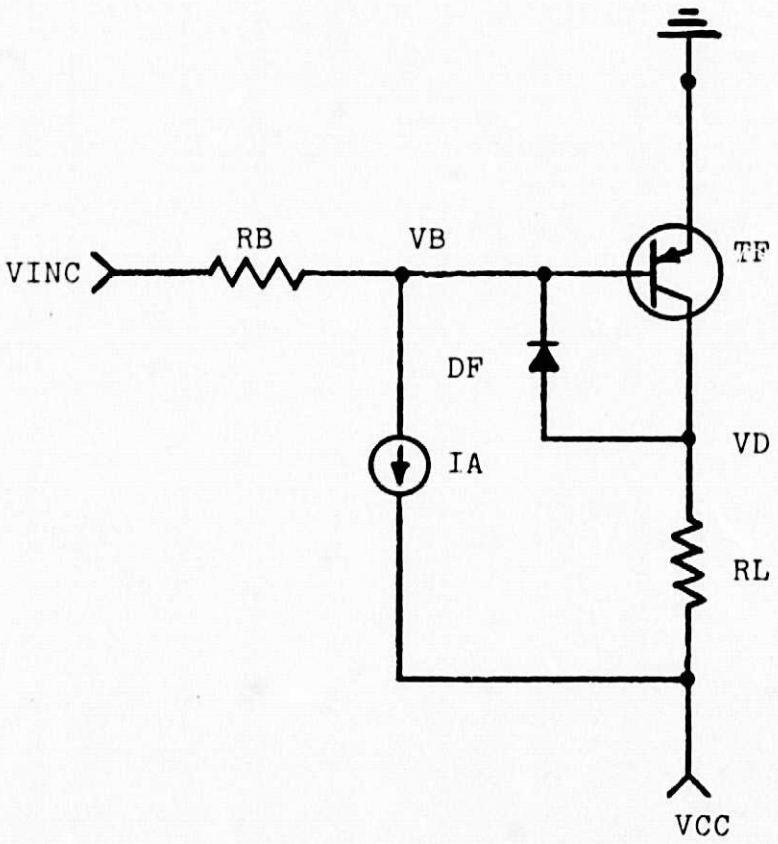


Figure 5. Schematic of FET Model Circuit for ASAP Test

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Punch, Debug, Recurse 8,1 Case

INPUTS
VCC=-20 TØL 0
RB, VINC TØ VB=1E4 TØL 0
RL,VCC TØ VD=2 TØL 0
IA,VB TØ VCC=2.07E-4 TØL 0
TF,PNP,VB,VD,GND,CURVE1,BETA1=1E5 TØL 0
DF,VD TØ VB,CURVE2
VINC=1E-20TØL 0
INCREMENTS-2

ØUTPUTS
VGS=VINC
VD
IRL=(-VCC+VD)/RL
VB
ITF=QI(1)
IDF=QI(2)
IGS=(VINC-VB)/RB
ITEST=IDF+ITF+IA

CURVE1 -1,-1E20,-1E20,0,0,0,1E-1,.66,.66,2E-1,.85,.85,
3E-1,1.04,1.04,5E-1,1.22,1.22,8E-1,1.39,1.39,10E-1,1.57,
1.57,13E-1,1.74,1.74,17E-1,1.90,1.90

CURVE2 -.25E-5,-20,-20,-.15E-5,-5,-5,-.12E-5,-4,-4,-.05E-5,
-3,-3,0,0,0,1E-6,.36,2E-6,.55,.55,3E-6,.74,.74,5E-6,.92,
.92,8E-6,1.09,1.09

END
```

Figure 6. Topological Input Data to ASAP

Figure 6 demonstrates the format of the topological input data which must be supplied to ASAP for the circuit in Figure 5. The data in Figure 6 indicates that the output is obtained for variations in supply voltage at a constant gate-source voltage. The same data with exception to the gate voltage is then used to obtain the output for variations in supply voltage at a different gate voltage. This process is continued to obtain the output for variations of gate and supply voltages for the purpose of obtaining the I_d vs V_{ds} characteristics.

Nominal Value of performance parameter V_{gs} = 1.000000E-20

Nominal Value of performance parameter V_d = 2.642582E 00

Nominal Value of performance parameter I_{rl} = 1.678709E 00

Nominal Value of performance parameter V_b = -1.891408E 00

Nominal Value of performance parameter I_{tf} = 1.678520E 00

Nominal Value of performance parameter I_{df} = 1.074178E-06

Nominal Value of performance parameter I_{gs} = 1.891408E-04

Nominal Value of performance parameter I_{test} = 1.678728E 00

Figure 7. Typical ASAP Output Data

Figure 7 contains the ASAP output data for the FET Model for particular values of gate and supply voltages. Similar ASAP output data for the Model were obtained for other values of gate and supply voltages. From the output data, the I_d vs. V_{ds} or Drain characteristics of the Model were constructed.

IV. RESULTS AND DISCUSSION

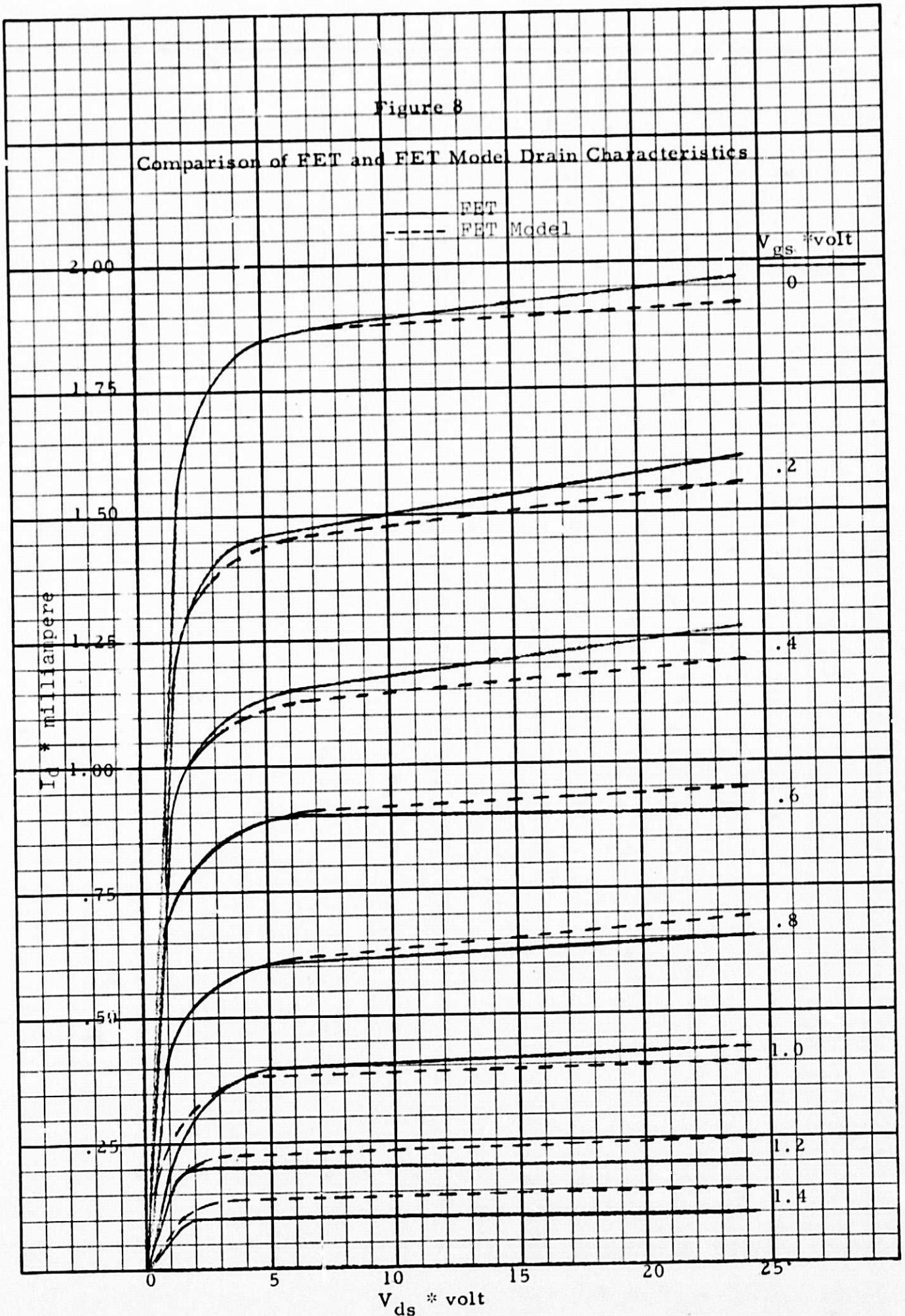
The first set of Drain characteristics obtained for the Model displayed extremely flat, non-sloping characteristics in the pinch-off region. This type of behavior is indicative of an extremely high output impedance. Thus, to adjust the Model characteristics for a better simulation of the FET characteristics, the high output impedance was effectively reduced through adjustment of the reverse characteristics of the base-collector diode, DF, of the Model. The Drain characteristics of the Model with this adjustment included are compared to those of the FET in Figure 8.

It may be noted that the characteristics of the Model behave in the same way as those of the FET as a function of the gate voltage. While all the Drain characteristics do not follow exactly along the constant gate voltage lines, the maximum error in drain current is 0.05 ma for any drain voltage.

Most of the remaining error exists in that the slope of the characteristics in the pinch-off region does not change as a function of the gate voltage. This change in slope is indicative of a varying input impedance. Thus, this error may be compensated

Figure 8

Comparison of FET and FET Model Drain Characteristics



for by making the input resistance R_b variable and describing the resistance with a curve in the ASAP input data.

Therefore, dependent upon the accuracy required the latter corrective measure may or may not be adopted.

Normally the FET characteristics for a particular unit vary with temperature changes. In addition FET characteristics vary from device to device as a result of manufacturing tolerances. In ASAP these variations would be accounted for by specifying tolerances about a mean characteristics. No tolerances were specified in the Model for test purposes.

The variation in the characteristics is the result of the change in I_{dss} the saturation drain current with zero gate-source bias voltage at any drain-source voltage in the pinch-off region below breakdown. I_{dss} when measured at a specified drain voltage in the pinch-off region, I_{dss} is approximately $I_{d\,(on)}$.

For the 2N2497, $I_{d(on)}$ is measured at a drain source voltage of 10 volts. The manufacturer's tolerances on $I_{d(on)}$ are $I_{d\,(on)}$ = 1 → 3 ma. With these values the effect of $I_{d(on)}$ on other curves of constant gate voltage are determined from the Bias Design Curves

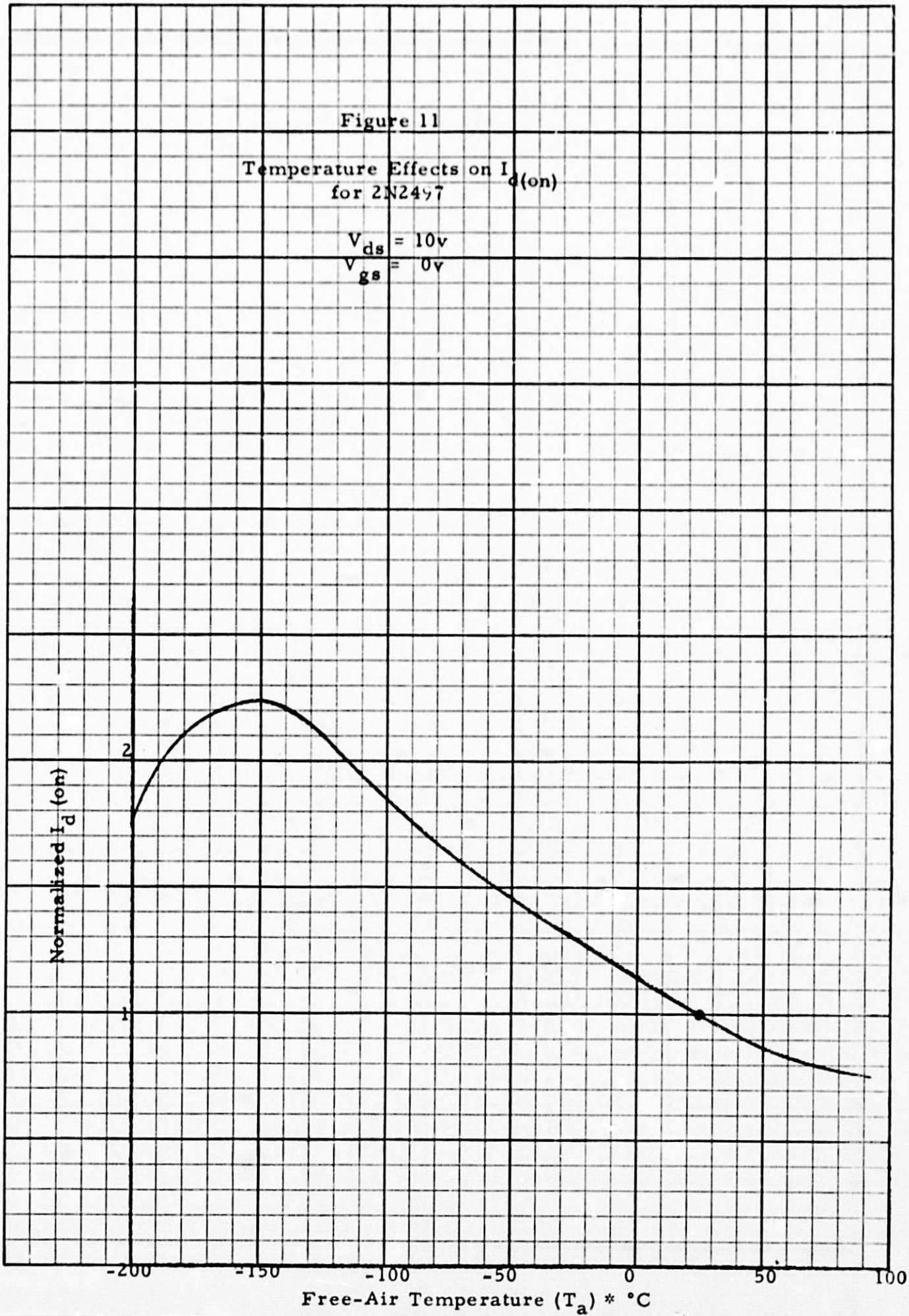
of Figure 9. Figure 10 shows the effects of the tolerances on $I_{d(on)}$ on the FET characteristics.

Temperature effects on the FET characteristics take place through $I_{d(on)}$ by the dependence of $I_{d(on)}$ on temperature. This dependence is shown in Figure 11.

Figure 11

Temperature Effects on $I_{d(on)}$
for 2N247

V_{ds} = 10v
V_{gs} = 0v



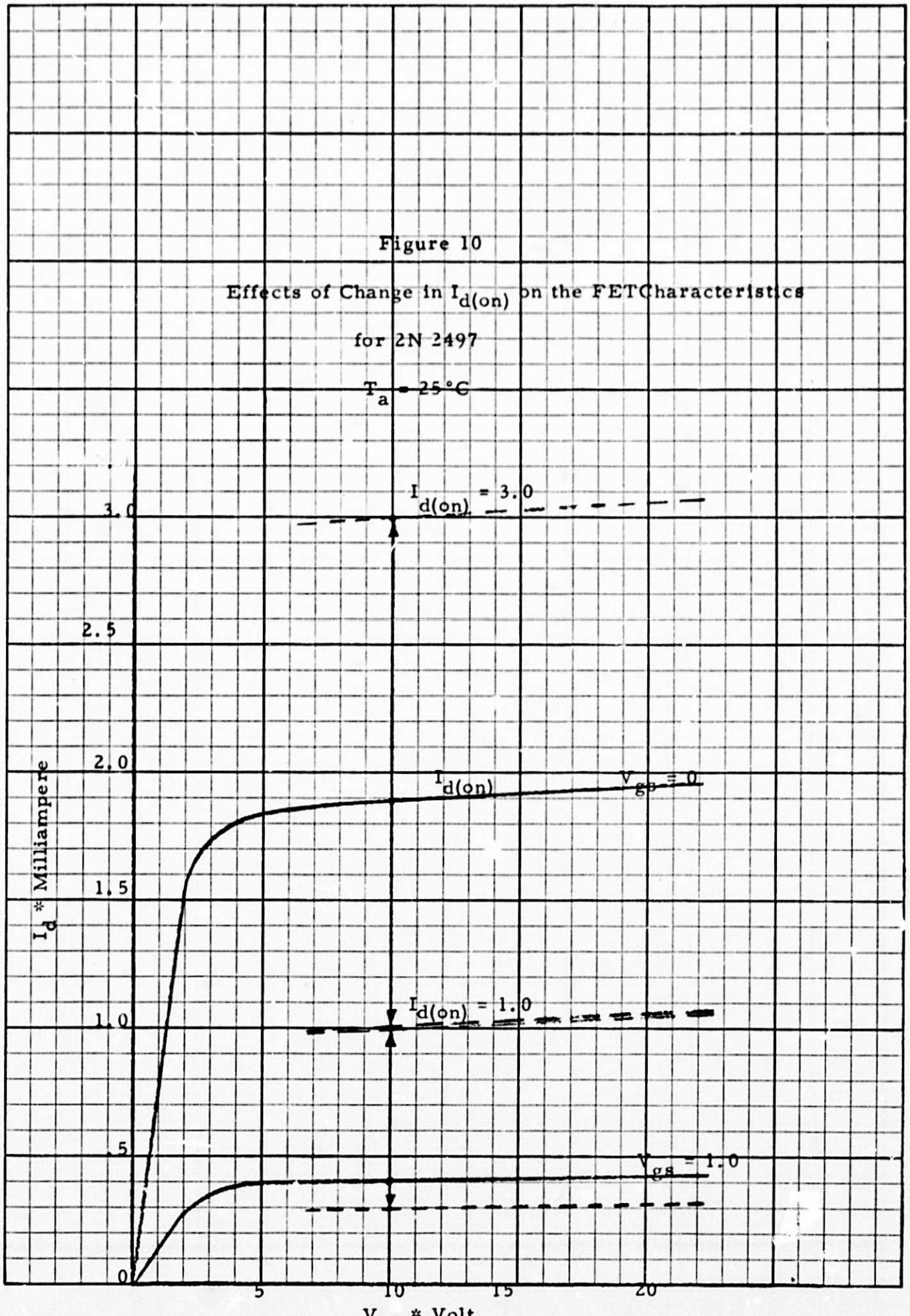
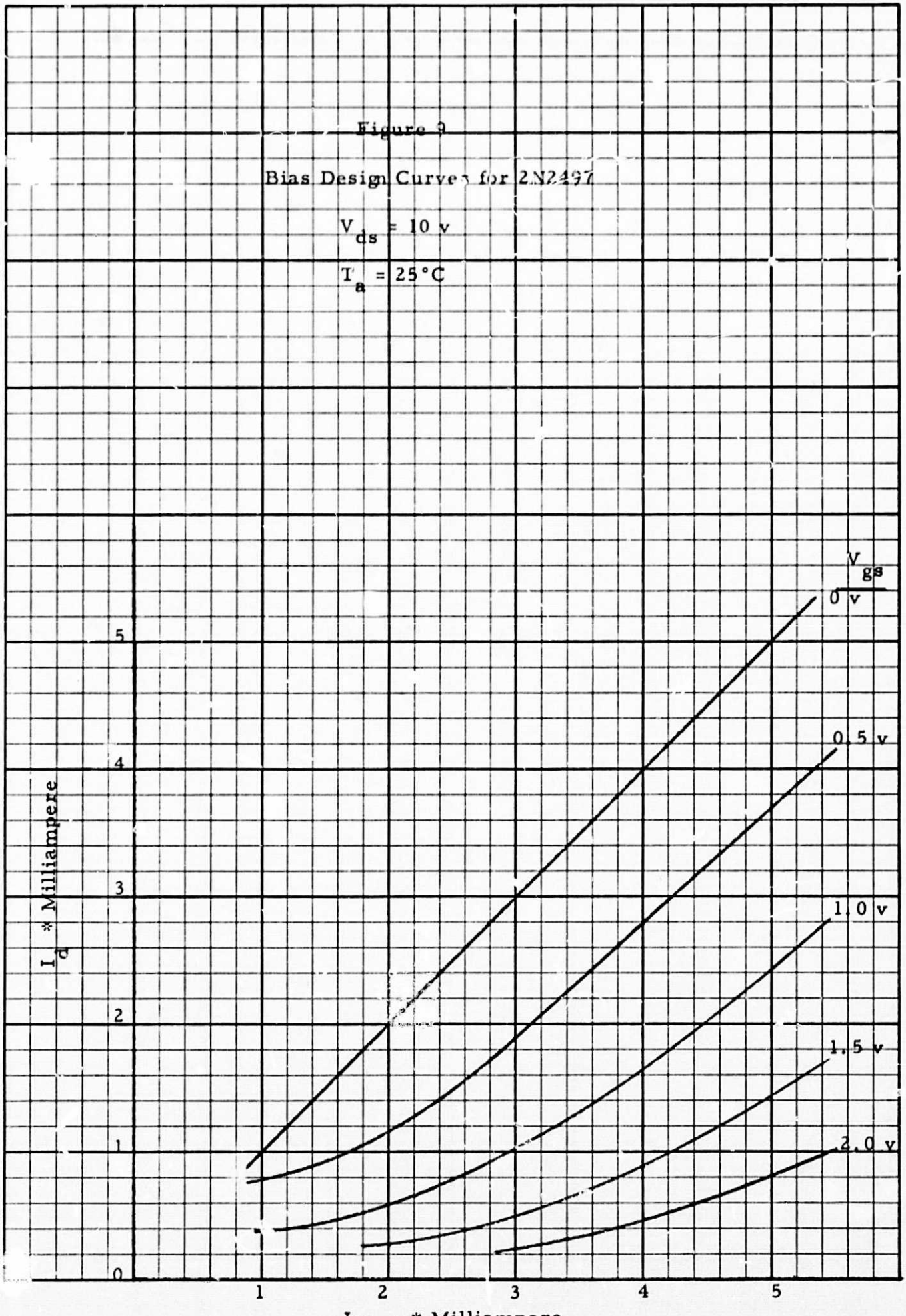


Figure 9

Bias Design Curves for 2N2497

V_{ds} = 10 v

T_a = 25°C



V. AN IMPROVED FET MODEL

The performance characteristics of a FET change and the changes are exhibited in the Drain characteristics. In Section IV it was pointed out that temperature had certain effects on the Drain characteristics. More specifically the changes effected by temperature are a manifestation of the variation of the gate input impedance and gain of the FET with the temperature.

The gate input impedance varies also with the applied gate voltage and the gain with the drain current. In Section IV these FET parameters were related to the corresponding parameters (R_b and β) in the Model. Also, suggestions were made for considering the variation of R_b and β with temperature and R_b with the applied gate voltage. In this section the suggestion is made for considering the variation of gain with the drain current.

To account for the latter consideration, it is required only that β for the transistor in the Model be described by a curve β vs I_c.

In the final analysis, it is obvious that the initial FET Model may be improved by including in the model all the factors which contribute to the performance characteristics of the FET. In addition,

an improved model would simplify elements where simplification is possible. Notably R_b may be replaced by a diode, and the current source may be described in the curve for the base-collector diode. The schematic of an Improved FET Model Circuit for ASAP is shown in Figure 12.

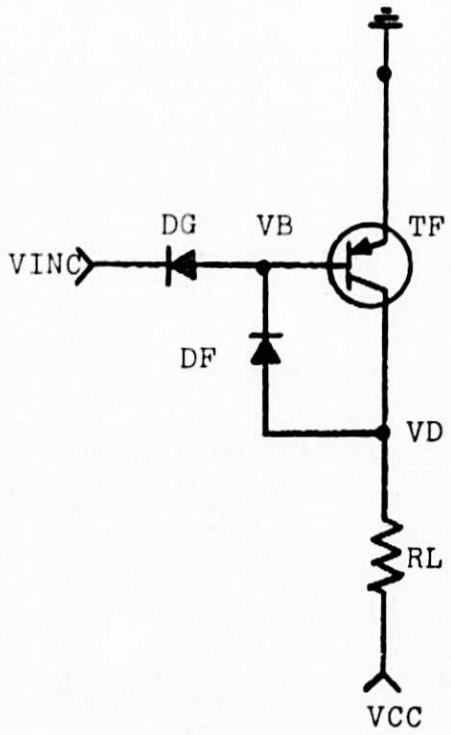


Figure 12. Schematic of An Improved FET Model for ASAP

VI. CONCLUSION

From the results of the application in ASAP of the FET model described in this report, the conclusion is that the Model (as shown in Figure 12) is a proper Model and that the Model may be made to behave in the same manner as the FET to any accuracy desired, even to the extent of exact duplication of the FET Drain Characteristics.

Although calculations were made for a specific FET (2N2497), the Model circuitry and procedures may be applicable to other FET types.