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TECHNICAL MEMORANDUM (NASA) 5

BINARY PHASE LOCK LOOPS FOR SIMPLIFIED OMEGA RECEIVERS

A sampled binary phase lock loop is proposed for
periodically correcting OMEGA receiver internal
clocks. The circuit is particularly simple to
implement and provides a means of generating long
range 3.4 KHz difference frequency lanes from
simultaneous pair measurements.

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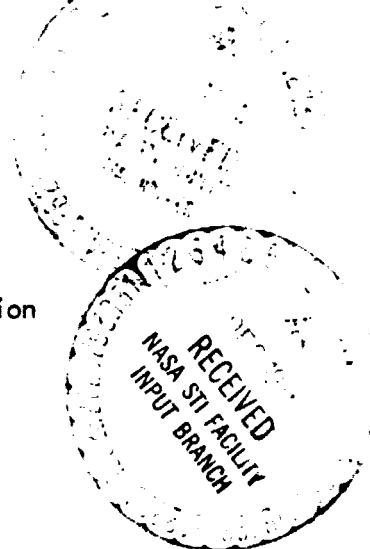
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INTRODUCTION

A previous report,"Simplified Omega Receivers", NASA TM 4, briefly mentioned phase detection methods where the clock stability is of consequence in a measurement sequence. This memorandum presents one method of providing a digital phase lock loop using a reasonably stable free running clock but correcting for slow phase drift by periodically incrementing the clock countdown rate in binary steps. A simple version of a binary rate multiplier related to digital phase lock loops used in more sophisticated receivers, can provide synchronization for each 10 second OMEGA sequence.

3.4 KHz SIMULTANEOUS PAIR LANES

If the housekeeping timer system can be kept accurately synchronized such that each time slot sampled 10 seconds later is at the same relative point within less than a 40.8 lane, then it is possible to track other combinations of lanes without complex arithmetic manipulations. In particular, long range navigation using 3.4 KHz difference frequency lanes is possible by dividing the incoming 10.2 signal by 3 and the 13.6 signal by 4 during simultaneous transmissions. The resulting 3.4 KHz signals can be directly compared using a phase detector width measuring system similar to the 40.8 KHz simultaneous pair scheme. The difficulty with this method is that a 40.8 KHz ambiguity of the start point for the ÷3 and ÷4 is observed unless the HKT clock samples the same relative 40.8 lane point (or within a few bits of the same 40.8 lane point at a 4 bit measurement level) at each successive 10 second time slot gate.

This problem is solved by phase-locking the clock rate to a common station. As long as the navigational velocity is such that a 40.8 KHz lane is not traversed in 10 seconds or a velocity of less than 360 knots is being considered, the same relative 40.8 lane can be

sampled 10 seconds later with a free-running clock offset even worse than 1×10^{-6}. However, if the clock is not corrected sooner or later, the clock will drift off more than one 40.8 cycle creating an ambiguity in the 3.4 KHz difference frequency lane starting position.

3.4 KHz lanes are very useful for long range navigation and when no diurnal corrections are available since the lane width of 24 miles on the pair baseline is greater than the usual diurnal variations. Thus if the navigator started out using 3.4 KHz LOP's from some known position and did not loose count of the lanes traversed, he would only be off 8 miles or so in the worst situations without any corrections applied over a long range mission. This is of significant interest for low cost OMEGA receiver methods.

In 3.4 KHz lane processors, the 40.8 KHz lanes become convenient 1/12th of a lane or 2 mile increments for fine resolution. A standard divide by 12 IC (7492) can be used with a 4 bit D/A and phase direction indicator similar to the 40.8 KHz processor phase display. The 16 x 16 OMEGA NAVMAP matrix would provide a 384 mile range for the 3.4 KHz lanes on the pair base lines.

PHASE-FREQUENCY DETECTOR

A phase detector integrated circuit, originally designed for driving analog VCO's when interfaced with digital input signals, provides a slow, fast, or equal logic output. The internal logic of the 4044 integrated circuit results in both phase and frequency sensing according to the truth table summarized in Figure 1. This circuit may be directly used to implement a binary phase locked loop which alters the countdown rates from the internal receiver clock.

SAMPLED BINARY PHASE LOCK LOOP

Figure 2 is a complete loop circuit suggested for periodically correcting the internal clock phase with respect to the D channel phase every 10 seconds. The countdown chain operates most of the time on the normal 40.8 x 16 division rate but is speeded up or slowed down according to the error observed every 10 seconds for the 625 millisecond sampling interval. The loop inherently has a quantization jitter of 1/16th of a 40.8 lane (or 1/64th of a 10.2 lane) in this example. The jitter is of little consequence when the primary use is for generating the same relative sample points for the + 3 and +4 counters used in the 3.4 KHz difference frequency processor. The free-running clock between correction will only drift off 2 counts even with a relatively poor crystal clock offset of 1×10^{-6} (always assuming here a 4 bit 40.8 KHz rate).

MULTIPLE PHASE LOCK LOOP RECEIVERS

In principle the sampled binary loop of Figure 2 can be expanded to provide a complete 10.2 or 13.6 KHz receiver by using a separate loop for each station and each frequency selected. Thus with four circuits like Figure 2, each one operated from a separate selected time slot with the outputs used to drive counter or subtractor type phase detectors in pairs, the circuit of Figure 3 results. This is an oversimplified block diagram of a complete digital phase locked loop processor system which is quite similar to the techniques used in some commercial receivers. In addition to Figure 3, multiple time slot averaging integrators are required and one of the same stations selected is used to synchronize the other countdown chains of the housekeeping timer as in Figure 2. Obviously this requires a lot of hardware which is one of the basic reasons why commercial OMEGA receivers start with a present lowest cost of $ 4000 and typically are more like $ 15,000 for systems using all possible combinations

of stations and frequencies with course computers built in. In practice commercial receivers invariably use more complex circuits for the digital phase lock loops with 8 bit processing precision.

The digital filtering provided by these phase lock loop methods is a function of the number of binary steps selected for slow-fast incrementing and the bit rate or division ratio chosen for the smallest increment of phase. Obviously an 8 bit system will do better than a 6 bit method in rounding off the quantization jitter but at the expense of more hardware. For low cost methods, the use of a single loop to synchronize within one 40.8 lane at 4 bit precision with counter-subtractor phase detectors, requires less hardware than the implementation of four 8 bit loops as used in some present systems. 4 bit readout systems could provide more than adequate capability but the lane transitions may be offset from the absolute value obtained with a very precise measurement system. This is not a problem as long as the end use of the data is for relative navigation purposes with respect to a known starting point as opposed to absolute determination of a particular position on the earth. The ultimate question is; how accurately can these simpler methods continue to provide data over a long duration and long range mission? This question cannot be answered at the present time. At this point it is not yet clear what is the best (from the standpoint of cost-complexity-utility) way of implementing a 4 bit OMEGA processor system. However, some combination of the relatively high precision possible with 4 bit 40.8 lanes and the simplicity of direct division phase processors for integration and long range housekeeping appears to be a proper approach.

(Note added in review)

Operation of the circuit of Figure 2 has been experimentally verified. Figure 5 is a recording of the 40.8 KHz local clock drift in the free running state versus the phase locked case when comparing the D channel phase to an external atomic clock. The internal receiver clock was purposefully offset to provide 40.8 KHz lane change every 3 minutes or so. In the locked condition a 2 bit jitter bandwidth is observed but the 40.8 KHz phase comes back to about the same relative phase point at every 10 second sample gate. The jitter bandwidth is a function of the 4044 phase detector response time which turns out to require two cycles of the input frequency to come to equilibrium after a transient. Thus a two bit change is possible depending on the exact signal phase comparison at the beginning and end of the sampling interval. A two bit error in the 40.8 KHz phase is less than one tenth of a 10.2 KHz lane and can be further reduced by multiple time slot averaging in the final output phase display. The phase jitter can also be reduced by tuning the local clock to reduce the offset error between each 10 second sample interval.

SUMMARY

3.4 KHz simultaneous pairs generated by direct division of 10.2 and 13.6 KHz signals, can provide long range navigation capability for low cost processing systems when a digital phase lock loop is used to correct for sampling time clock drift errors. A particularly interesting combination for simplified OMEGA processors appears to be the use of 40.8 KHz lanes for high resolution and 3.4 KHz lanes for long range at lower resolution with parallel processors utilizing similar 4 bit methods. A switched display system or dual display could provide cross checks on lane counts for increasing the reliability and utility of the results. A higher bit precision such as 8 bits at 10.2 KHz is used in some present commercial receivers with a related digital correction loop for clock-signal phase comparisons with parallel arithmetic subtraction techniques or up down counters to generate pair differences with clock offsets of 1×10^{-7} between subtractions. A functional block diagram of a Simplified OMEGA Receiver using the methods described in this report is shown in Figure 4.

ACKNOWLEDGEMENT

BINARY PHASE LOCK LOOPS FOR SIMPLIFIED OMEGA RECEIVERS

FIGURES 1 through 5

PHASE-FREQUENCY DETECTOR LOGIC

(Using MC4044P Phase Detector)

FIGURE 1

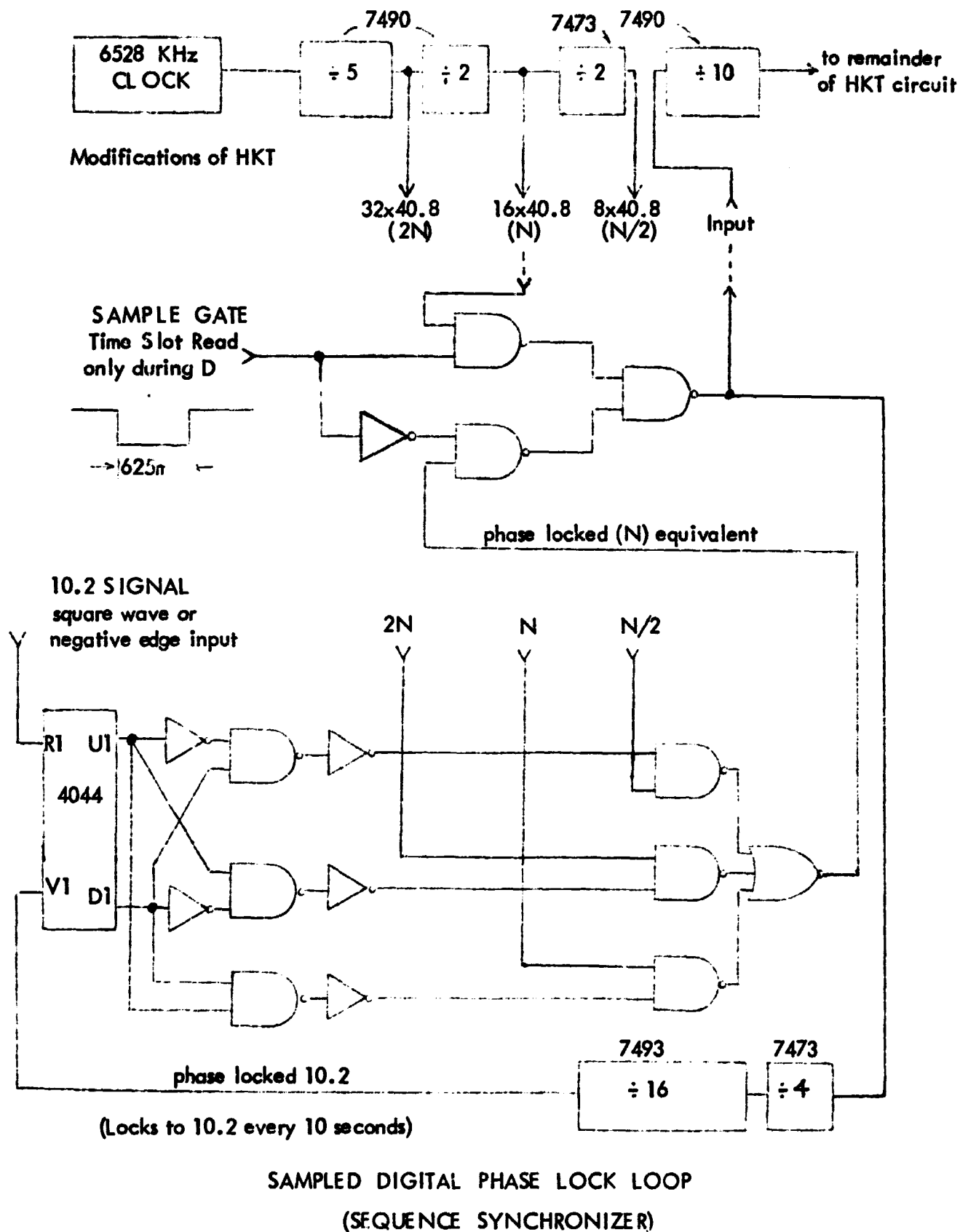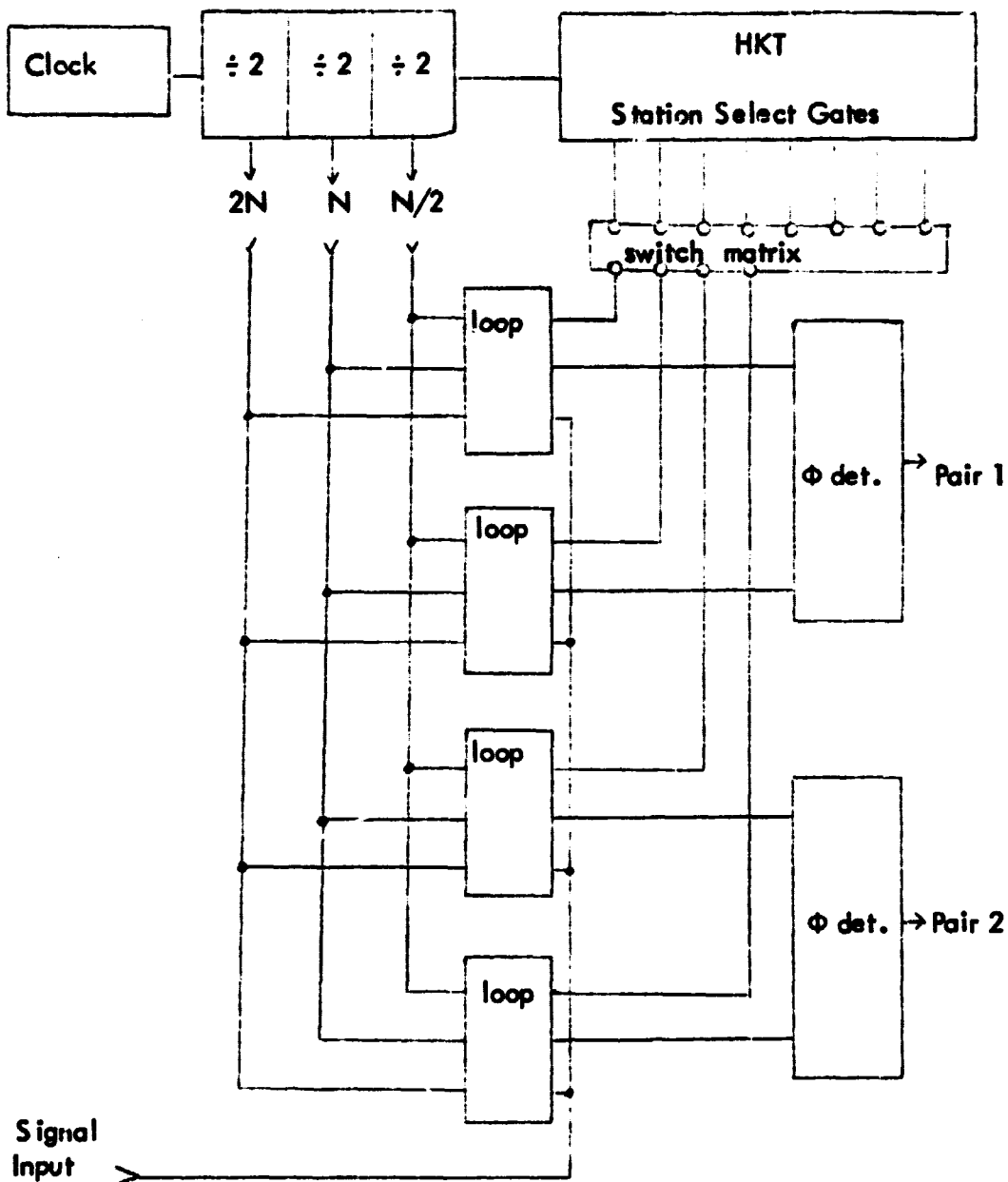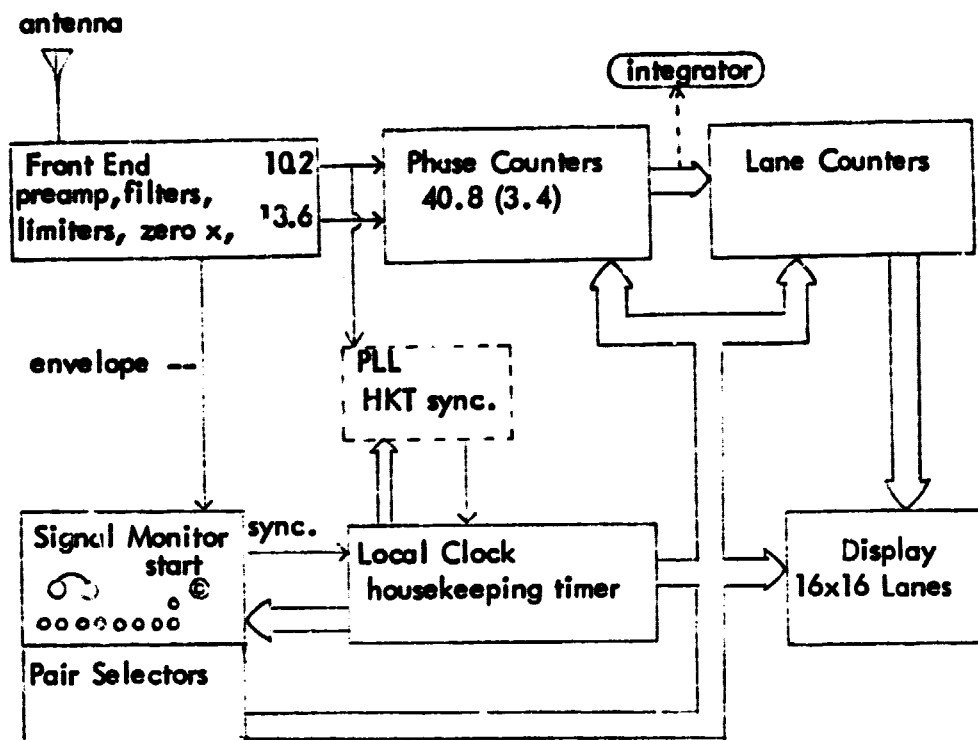SAMPLED DIGITAL PHASE LOCK LOOP
(SEQUENCE SYNCHRONIZER)

FIGURE 2

DIGITAL PLL OMEGA PROCESSOR

FIGURE 3

FUNCTIONAL BLOCK DIAGRAM
SIMPLIFIED OMEGA RECEIVER

FIGURE 4

40.8 KHz
Lane

(4 bits)

10 seconds

Unlocked, free running clock | Locked condition, every 10 seconds
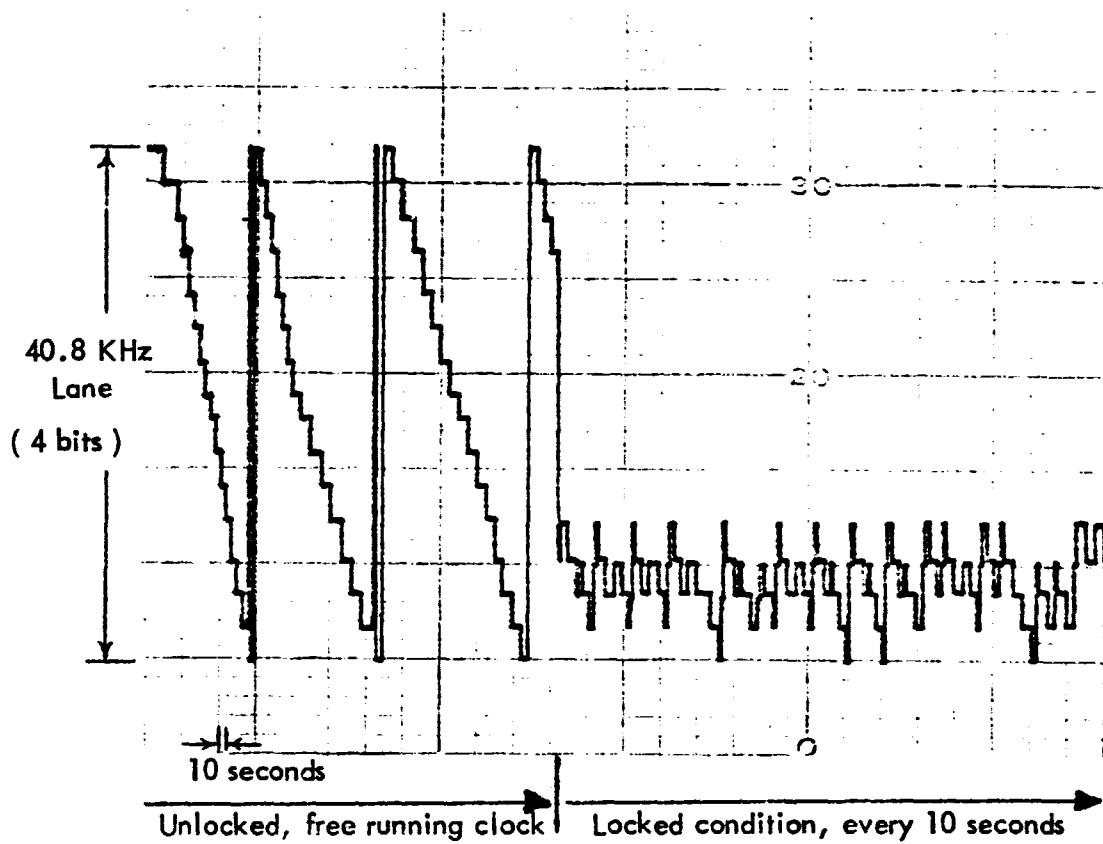
D CHANNEL 40.8KHz PHASE WITH BINARY PHASE LOCKED LOOP

FIGURE 5