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DEVELOPMENT OF A LOW-NOISE HIGH COMMON-MODE-REJECTION INSTRUMENTATION AMPLIFIER

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Final thanks are due my wife Mary without whose support this work could not have been a success.

ABSTRACT

This study examines several previously used instrumentation amplifier circuits to find limitations and possibilities for improvement. One general configuration is then analyzed in detail and methods for improvement are enumerated.

An improved amplifier circuit is described and analyzed with respect to common mode rejection and noise. Experimental data are presented showing good agreement between calculated and measured common mode rejection ratio and equivalent noise resistance.

The new amplifier is shown to be capable of common mode rejection in excess of 140 dB for a trimmed circuit at frequencies below 100 Hz and equivalent white noise below $3.0 nv/\sqrt{Hz}$ above 1000 Hz.

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CHAPTER I

INTRODUCTION

Instrumentation Amplifiers

An instrumentation amplifier is an electronic signal conditioning device designed to detect and amplify the difference of two electric signals. Instrumentation amplifiers find use in biomedical measurements, thermocouple temperature measurements, audio microphone amplification, analog computers, and many other data gathering and measurement instruments.

The most useful property of instrumentation amplifiers is their ability to amplify the difference of two signals while rejecting any signals common to the two inputs. This property is called "common mode rejection" and is quantified by the common mode rejection ratio (CMRR). The CMRR is defined as the ratio of differential gain to common mode gain. In a quality instrumentation amplifier this ratio will reach values of 10^5 and higher at low frequencies.

The common mode rejection property allows low level signals to be transmitted over a length of cable and be received with only slight increases in noise due to electromagnetic pickup on the cable. If the two signal lines in the cable running from the sensor are close to each other the electromagnetic pickup will be approximately a common mode signal and will be rejected by the amplifier.

Purpose of Study

The purpose of this study was to examine the characteristics of commonly used instrumentation amplifier circuits to determine the relationships governing signal to noise ratio (S/N) and CMRR. A new amplifier was developed, using these governing relationships and low noise circuit design theory to give state of the art performance in a low noise high common-mode-rejection instrumentation amplifier.

In systems designed to measure a parameter over many orders of magnitude such as pulse rebalance accelerometers [1] dynamic range of the system can be limited by preamplifier noise. Therefore, in such applications the S/N of the preamplifier must be maximized. This study will develop the design equations for the maximization of S/N and CMRR for one type of instrumentation amplifier. The amplifier is a low noise implementation of a well proven approach [2], [3].

Guidelines

The following guidelines were used in the amplifier development.

1. The differential voltage of the amplifier shall be set by a single resistor selection to have a value between five and five-hundred. The tolerance and stability of this gain shall depend only on the tolerance and stability of the resistor used.
2. The gain nonlinearity shall not exceed 0.1 % over the entire dynamic range.
3. The output dynamic range shall be such that a ten-volt peak sine wave at the output shall show no indication of overload distortion when applied across a 10 kΩ load.

4. The small signal 3 dB bandwidth of the amplifier shall be in excess of 100 kHz.
5. The input impedance of the amplifier shall be in excess of 100 MΩ in both the differential and common modes.
6. The output impedance shall be less than 200 Ω.
7. The amplifier shall be operable over a range of power supply voltages from ± 10 V to ± 18 V.
8. The input DC offset shall be less than 10 mV.
9. The output signal slew rate shall be in excess of 3 V/μs.
10. The common mode rejection ratio shall be in excess of 100 dB for frequencies below 100 Hz and greater than 60 dB at 20 kHz.
11. The input referred equivalent noise voltage ($\overline{e_n}$) shall not exceed 10 nV/$\sqrt{\text{Hz}}$, and shall preferably be less than 4 nV/$\sqrt{\text{Hz}}$ for differential gains above 20.

CHAPTER II

PRIOR WORK

Introduction

Several circuits commonly used as instrumentation amplifiers will be discussed in this chapter. The derived equations governing noise and common mode rejection will be presented. These equations will be used as the basis for a comparison of the circuits for typical amplifier gain and component matching.

Subtracter Circuit

The most popular and simple configuration used in instrumentation amplifiers is the single operational amplifier (Op-Amp) subtracter circuit shown in Figure 2-1.

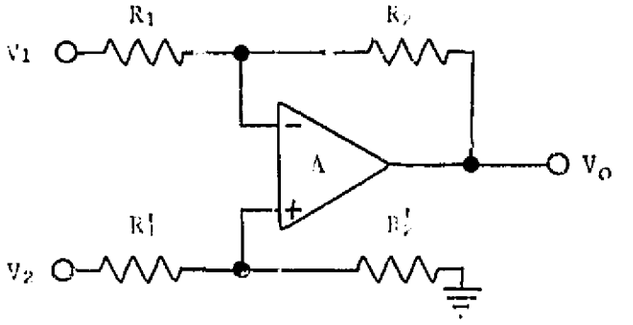

Figure 2-1. Simple Subtracter Circuit.

From this circuit the output voltage can be shown to equal that of Equation (2-1).

$$V_o = \frac{A\left(\frac{V_1 R_2'}{R_1' + R_2'}\left(1 \pm \frac{1}{CMRR}\right) - \frac{V_2 R_2}{R_1 + R_2}\right)}{A\left(\frac{R_1}{R_2 + R_1}\right) + 1} \qquad (2\text{-}1)$$

The differential input voltage is defined as

$$V_d \equiv V_1 - V_2. \qquad (2\text{-}2)$$

Assuming

$$\frac{R_1'}{R_2'} = \frac{R_1}{R_2}, \qquad (2\text{-}3)$$

and $$CMRR = \infty,$$

it can be shown that

$$\frac{V_o}{V_d} = \frac{A\left(\frac{R_2}{R_2 + R_1}\right)}{A\left(\frac{R_1}{R_1 + R_2}\right) + 1}. \qquad (2\text{-}4)$$

If $$A >> 1,$$

then

$$\frac{V_o}{V_d} \simeq \frac{R_2}{R_1}. \qquad (2\text{-}5)$$

The common mode input voltage is defined as

$$V_{cm} \equiv \frac{V_1 + V_2}{2}. \qquad (2\text{-}6)$$

To maintain clarity the sources of error leading to a finite common mode rejection ratio will be analyzed and presented separately. If each error is small, the interaction of errors will be a second order effect. The effect of each error source will be presented as an equivalent common mode rejection factor (CMR) assuming that all other sources of error have zero effect. As the errors can be either additive or subtractive depending on random selection of circuit components, a good approximation of the total error can be obtained by a square root of the sum of the squares combination of all the errors such as that of Equation (2-7).

$$CMRR = 20 \log_{10} \left[\sum_{n=1}^{m} \left(\frac{1}{CMR_n} \right)^2 \right]^{-\frac{1}{2}} . \qquad (2\text{-}7)$$

The common mode rejection factor is defined as the ratio of differential mode gain to common mode gain. Solving for the common mode rejection factors for the simple subtractor the following equations are obtained. For error due to mis-match in feedback resistors

$$CMR_1 = \left(\frac{R_1/R_2}{\Delta R_1/R_2} \right) \frac{R_2 + R_1}{R_1} . \qquad (2\text{-}8)$$

For error due to finite op-amp common mode rejection

$$CMR_2 = CMR_{op\text{-}amp.} \qquad (2\text{-}9)$$

For error due to source impedance mis-match

$$CMR_3 = \left(\frac{R_S}{\Delta R_S}\right) \left(\frac{R_2 + R_1 + R_S}{R_S}\right). \qquad (2\text{-}10)$$

This common mode rejection is limited by the resistor mis-match to about 100 dB using 0.1% tolerance resistors with a balanced source and gain of 100. The CMRR is seriously degraded however, by unbalanced source resistance.

Each resistor has a thermal noise source associated with it which can be represented by either of the two equivalent noise sources shown in Figure 2-2 (a and b).

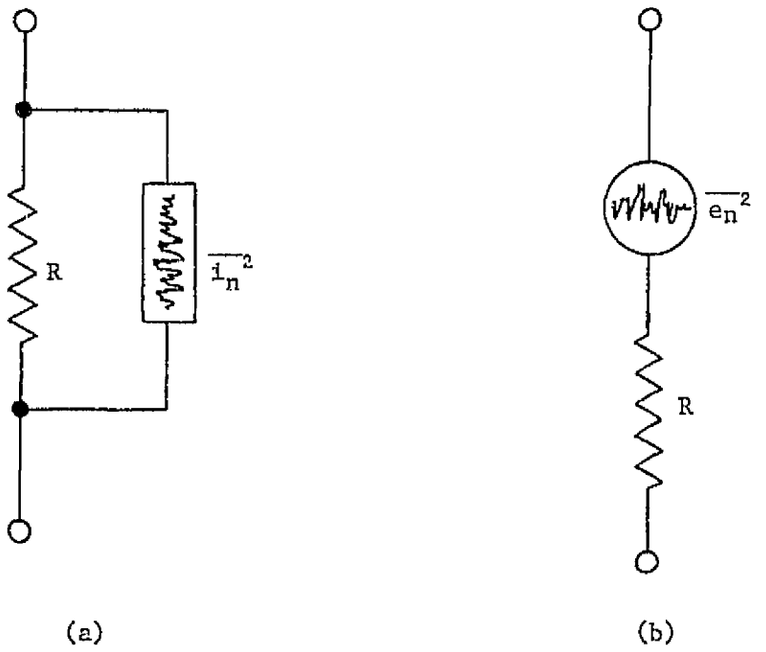

Figure 2-2. Resistor Equivalent Noise Models,

In Figure 2-2

$$\overline{i_n^2} = \frac{4\ kT}{R}\ A^2/Hz, \qquad (2\text{-}11)$$

and

$$\overline{e_n^2} = 4\ kT\ R\ V^2/Hz, \qquad (2\text{-}12)$$

where k is Boltzmann's constant (1.38×10^{-23} J/K) and T is the absolute temperature in Kelvins. One of these noise models will be substituted for each of the resistors in Figure 2-1 and the analysis will be performed to obtain equations for the total noise due to the resistors.

The noise model of the op-amp appears in Figure 2-3.

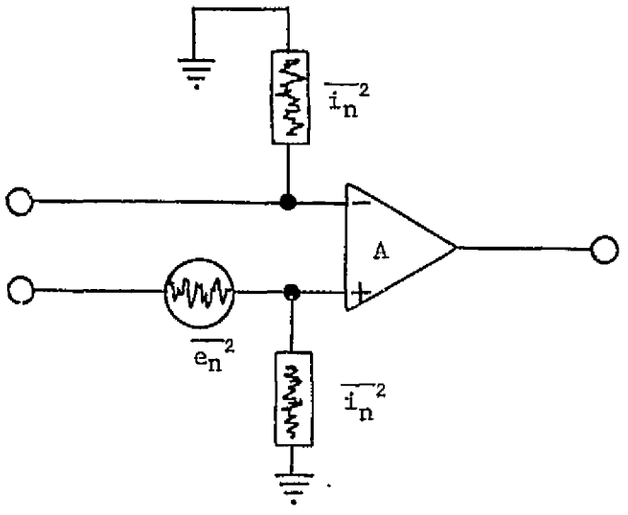

Figure 2-3. Operational Amplifier Noise Model.

The equivalent noise sources used in this model must be taken from manufacturers specification sheets, calculated from the amplifiers

circuit configuration or measured. The model of Figure 2-3 will be placed into the circuit of Figure 2-1 to derive the total noise due to the op-amp. Similar to the common mode analysis, the noise of each noise source will be analyzed separately and represented by an equivalent noise resistance R_{nj} at the input of the amplifier, then the total equivalent noise resistance will be given by

$$R_n = \sum_{j=1}^{m} R_{nj}. \tag{2-13}$$

For each source in the simple subtracter circuit the following equivalent noise equations were derived. For the thermal noise due to R_1, R_2, R_1' and R_2' together

$$R_{n1} = 2R_1 \left(\frac{R_1 + R_2}{R_2} \right). \tag{2-14}$$

For the equivalent noise voltage ($\overline{e_n^2}$) of the op-amp

$$R_{n2} = \frac{\overline{e_n^2}}{4kT} \left(\frac{R_1 + R_2}{R_2} \right)^2. \tag{2-15}$$

For the noise due to the equivalent input noise current of the op-amp

$$R_{n3} = \frac{2\overline{i_n^2}}{4kT} R_1^2. \tag{2-16}$$

The noise of the simple subtracter is at present limited to about 6 kΩ (about 10 nv/$\sqrt{\text{Hz}}$) by the equivalent noise voltage of the currently available low noise integrated circuit operational amplifiers.

Buffered Subtracter Circuit

The most severe handicap of the simple subtracter circuit is the low input impedance. This can be eliminated by buffering the inputs with voltage followers [4] as in Figure 2-4.

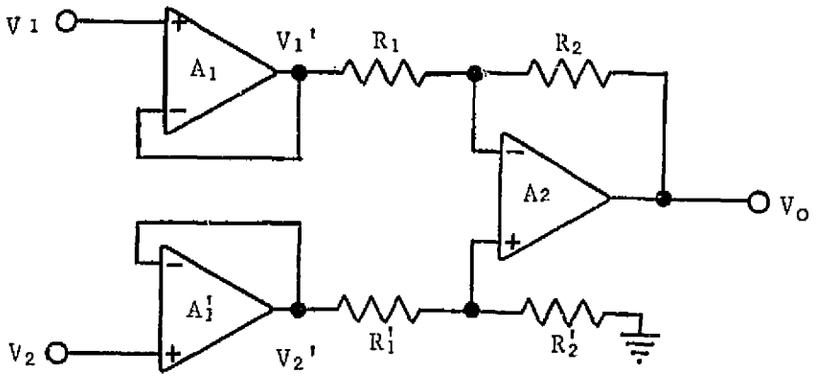

Figure 2-4. Buffered Simple Subtracter.

The gain of each voltage follower can be shown to be

$$\frac{V'}{V} = \frac{A_1}{A_1 + 1} \left(1 \pm \frac{1}{CMR_1}\right). \qquad (2\text{-}17)$$

The differential mode transfer function is given by Equation (2-18), if the circuit is matched.

$$\frac{V_o}{V_d} = \left(\frac{A_1}{A_1 + 1}\right) \left(\frac{A_2 \dfrac{R_2}{R_1 + R_2}}{A_2 \dfrac{R_1}{R_1 + R_2} + 1}\right). \qquad (2\text{-}18)$$

If $A_1 \gg 1$,

and $A_2 \gg 1$,

then

$$\frac{V_o}{V_d} \approx \frac{R_2}{R_1} . \tag{2-19}$$

The following error equations were derived for common mode rejection. For mis-match in feedback resistors

$$CMR_1 = \left(\frac{R_1/R_2}{\Delta R_1/R_2}\right) \frac{R_2 + R_1}{R_2} . \tag{2-20}$$

For finite CMR of op-amp 2

$$CMR_2 = CMR_{A2} . \tag{2-21}$$

For gain mis-match of op-amps A_1 and A_1'

$$CMR_3 = \left(\frac{A_1}{\Delta A_1}\right) A_1 . \tag{2-22}$$

For finite CMR of op-amp A_1

$$CMR_4 = CMR_{A1} \tag{2-23}$$

For finite CMR of op-amp A_1'

$$CMR_5 = CMR_{A_1'} \tag{2-24}$$

For gains below 100 the CMRR is limited by resistor mis-match a] for gains above 100 by the CMR of the op-amps used. Matching of the input op-amps is necessary at high frequencies where the op-amp gain falls off.

The noise of the buffered subtracter includes all the sources of the simple subtracter plus the equivalent noise sources of the two input op-amps. The following equivalent noise resistances were derived.
For noise due to resistors

$$R_{n1} = 2R_1 \left(\frac{R_1 + R_2}{R_2}\right). \tag{2-25}$$

For noise due to op-amp A_2 noise voltage

$$R_{n_2} = \frac{\overline{e_{n_2}}^2}{4kT} \left(\frac{R_1 + R_2}{R_2}\right). \tag{2-26}$$

For noise due to op-amp A_2 noise current

$$R_{n3} = \frac{2\overline{i_{n_2}}^2}{4kT} R_1^2. \tag{2-27}$$

For noise due to op-amps A_1 and A_1' noise voltage

$$R_{n_4} = \frac{2\overline{e_{n_1}}^2}{4kT}. \tag{2-28}$$

For noise due to op-amps A_1 and A_1' noise current, where R_s is the source resistance

$$R_{n5} = \frac{2\overline{i_{n_1}}^2 R_s^2}{4kT}. \tag{2-29}$$

Linear Gain Control

A linear gain control can be added to the circuit of Figure 2-4 with no degradation of CMRR and only slight increase in noise by adding an op-amp as in Figure 2-5.

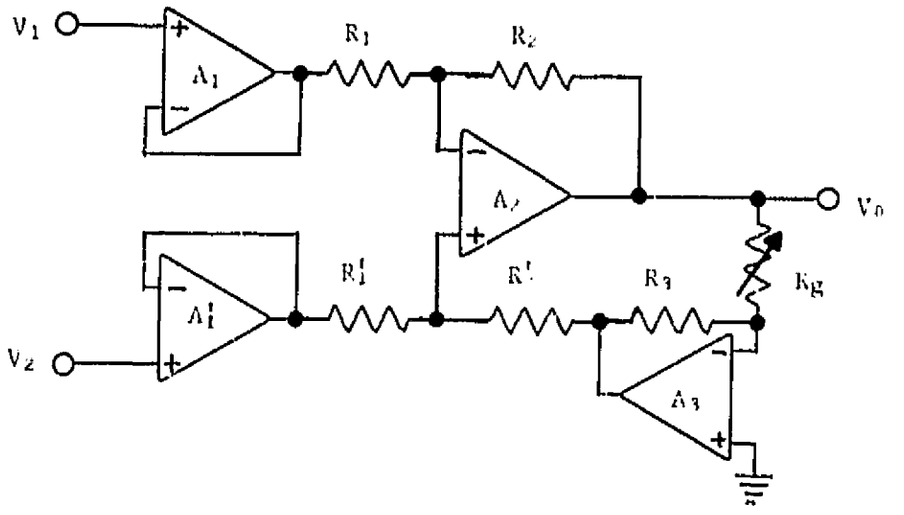

Figure 2-5. Buffered Subtracter With Linear Gain Control.

The CMR equations for this circuit are the same as Equations (2-20) through (2-24). The noise equations are the same as Equations (2-25) through (2-29) with the addition of the following:

$$R_{n6} = \left(\frac{\overline{e_{n_3}^2}}{4kT} + \frac{\overline{i_{n_3}^2}}{4kT} R_3^2 \right) \frac{1}{A_d^2} \qquad (2\text{-}30)$$

for noise of op-amp A_3;

$$R_{n7} = R_3 \left(1 + \frac{R_3}{R_g} \right) \frac{1}{A_{d2}} \qquad (2\text{-}31)$$

for the thermal noise of R_3 and R_g, where A_d is the differential gain given by

$$A_d = \frac{R_2}{R_1} \frac{R_g}{R_3} . \qquad (2\text{-}32)$$

Three Op-Amp Instrumentation Amplifier

Another op-amp configuration [5] incorporates gain into the input stage while at the same time providing single resistor gain selection. This circuit is shown in Figure 2-6.

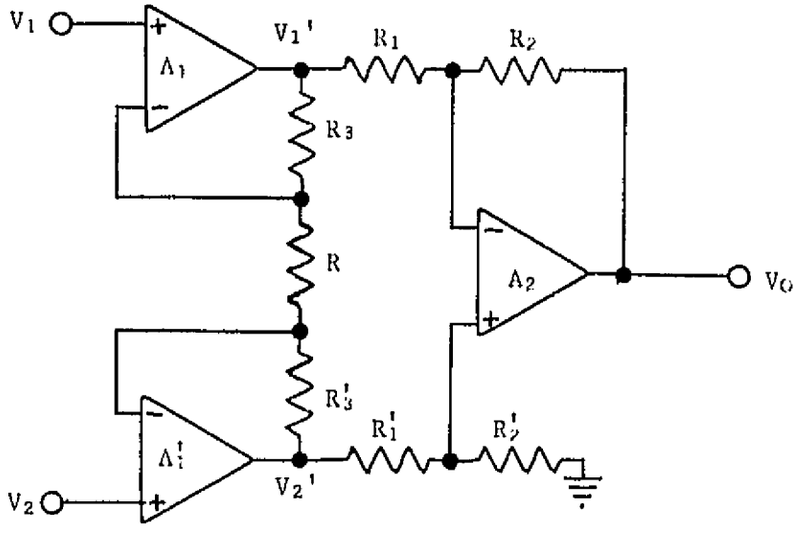

Figure 2-6. Three Op-Amp Instrumentation Amplifier.

The differential output voltage of the first stage is given by Equation (2-33).

$$V_1' - V_2' = \frac{\left(\frac{V_1 A_1}{1 + A_1} - \frac{V_2 A_2}{1 + A_2}\right)\left(R_g + R_3 + R_3'\right)}{R_g + \frac{R_3}{1 + A_1} + \frac{R_3'}{1 + A_2}} \qquad (2\text{-}33)$$

If the two input op-amps are matched the differential output for a common mode input is zero indicating that none of the other parameters affect the common mode rejection. Thus any mis-match between R3 and

R_3' has a second order effect on common mode rejection. Assuming matched components the differential gain of the circuit is

$$\frac{V_o}{V_d} = \left(\frac{A_1}{A_1 + 1}\right)\left(\frac{R_g + 2R_3}{R_g}\right)\frac{A_2\left(\frac{R_2}{R_1 + R_2}\right)}{A_2\left(\frac{R_1}{R_1 + R_2}\right) + 1}. \qquad (2\text{-}34)$$

If $A_1 >> 1$,

and $A_2 >> 1$,

then

$$\frac{V_o}{V_d} \approx \left(\frac{R_g + 2R_3}{R_g}\right)\left(\frac{R_2}{R_1}\right). \qquad (2\text{-}35)$$

The input circuit has a unity common mode gain giving a common mode rejection for the input stage of

$$CMR_{input} \approx \frac{R_g + 2R_3}{R_g}. \qquad (2\text{-}36)$$

This property tends to improve the effect of mis-matches in circuit components following the input stage. The unity common mode gain is not to be confused with common mode to differential mode transfers attributable to component mis-matches. The following common mode error equations were derived. For R_1/R_2 mis-match

$$CMR_1 = \left(\frac{R_1/R_2}{\Delta R_1/R_2}\right)\left(\frac{R_2 + R_1}{R_1}\right)\left(\frac{R_g + 2R_3}{R_g}\right). \qquad (2\text{-}37)$$

For finite CMR of op-amp A_2

$$CMR_2 = CMR_{A2}\left(\frac{R_g + 2R_3}{R_g}\right). \tag{2-38}$$

For op-amp A_1 and A_1' mis-match

$$CMR_3 = \left(\frac{A_1}{\Delta A_1}\right) A_1. \tag{2-39}$$

For finite CMR of op-amp A_1

$$CMR_4 = CMR_{A1'}, \tag{2-40}$$

For finite CMR of op-amp A_1',

$$CMR_5 = CMR_{A1'}, \tag{2-41}$$

The following noise equations for this configuration were derived. For thermal noise of R_g, R_3 and R_3'

$$R_{n1} = \frac{2R_3 R_g}{R_g + 2R_3}. \tag{2-42}$$

For thermal noise of R_1, R_1', R_2 and R_2'

$$R_{n2} = 2R_1 \left(1 + \frac{R_1}{R_2}\right) \left(\frac{R_g}{R_g + 2R_3}\right)^2. \tag{2-43}$$

For noise of op-amps A_1 and A_1' where R_s is the source resistance

$$R_{n3} + \frac{2\overline{e_{n_1}}^2}{4kT} + \frac{2\overline{i_{n_1}}^2}{4kT} (R_s^2 + R_3^2), \tag{2-44}$$

for noise of op-amp A_2

$$R_{n_4} = \frac{\overline{e_{n_2}}^2}{4kT}\left(\frac{R_1}{R_2} + 1\right)^2\left(\frac{R_g}{R_g + 2R_2}\right)^2 + \frac{2\overline{i_{n_2}}^2}{4kT} R_1^2 \left(\frac{R_g}{R_g + 2R_3}\right)^2. \quad (2\text{-}45)$$

Totum Pole Instrumentation Amplifier

Another configuration [5] of interest because of its simplicity is the two op-amp "totum pole" circuit of Figure 2-7.

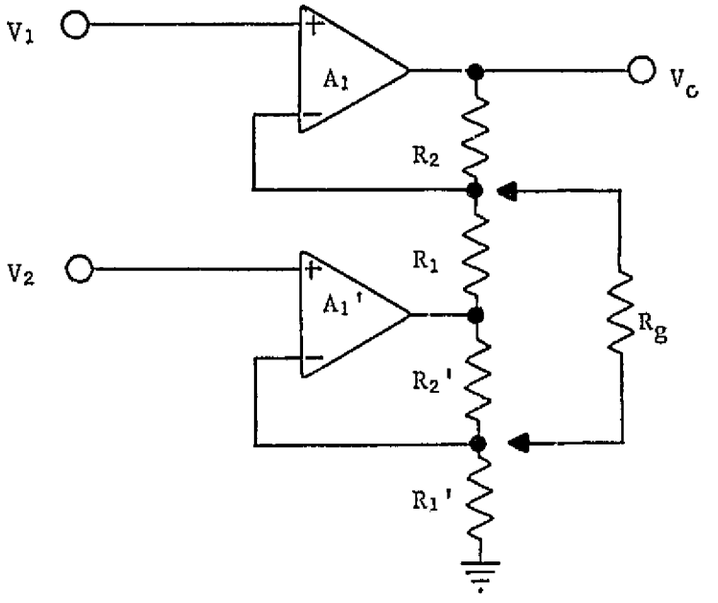

Figure 2-7. "Totum Pole" Instrumentation Amplifier.

The exact expression for the output voltage of this configuration is

$$V_o = \left(\frac{A_1}{1 + \frac{A_1 R_1}{R_1 + R_2}} \right) \left[V_2 \left(1 \pm \frac{1}{CMR_{A_1}} \right) - V_1 \left(1 \pm \frac{1}{CMR_{A_2}} \right) \frac{\frac{R_2 A_1'}{R_1 + R_2}}{1 + \frac{A_1' R_2'}{R_1' + R_2'}} \right]. \quad (2\text{-}46)$$

For the differential mode this reduces to

$$\frac{V_o}{V_d} \simeq 1 + \frac{R_2}{R_1} . \quad (2\text{-}47)$$

The following CMR equations were derived from Equations (2-46) and (2-47). For error due to finite gain of op-amp A_1'

$$CMR_1 = \frac{A_1' R_2}{R_1 + R_2} . \quad (2\text{-}48)$$

For mis-match in resistors

$$CMR_2 = \left(\frac{\frac{R_1}{R_2}}{\Delta \frac{R_1}{R_2}} \right) \left(\frac{R_1 + R_2}{R_1} \right). \quad (2\text{-}49)$$

For finite CMR of op-amp A_1

$$CMR_3 = CMR_{A_1}. \quad (2\text{-}50)$$

For finite CMR of op-amp A_1'

$$CMR_4 = CMR_{A1}'. \tag{2-51}$$

A one resistor gain control can be added to the circuit by the addition of R_g as shown in Figure 2-7. Then the gain changes to

$$\frac{V_o}{V_d} = 1 + \frac{R_2}{R_1} + \frac{2R_2}{R_g}. \tag{2-52}$$

The common mode gain does not change, however, resulting in a higher CMRR given by CMRR'.

$$CMRR' = CMRR + 20 \log \left(1 + \frac{2}{R_g} [R_1 || R_2]\right). \tag{2-53}$$

Notice that the voltage output of op-amp A_1' is higher than the common mode input voltage by a factor of $(R_1 + R_2)/R_2$. This fact restricts the common mode input swing for low gains.

The following noise equations for the amplifier were derived. For thermal noise of all resistors including R_g

$$R_{n1} = \frac{2R_2}{A_d}. \tag{2-54}$$

For noise of op-amps

$$R_{n2} = \frac{2\overline{e_n^2}}{4kT} + \frac{2\overline{i_n^2}}{4kT}\left(R_s^2 + \frac{R_2^2}{A_d^2}\right). \tag{2-55}$$

Bipolar Input Instrumentation Amplifier

The bipolar transistor differential amplifier operated open loop with unbypassed emitter resistance has been used [6], [7] as an instrumentation amplifier. The most basic circuit is that of Figure 2-8.

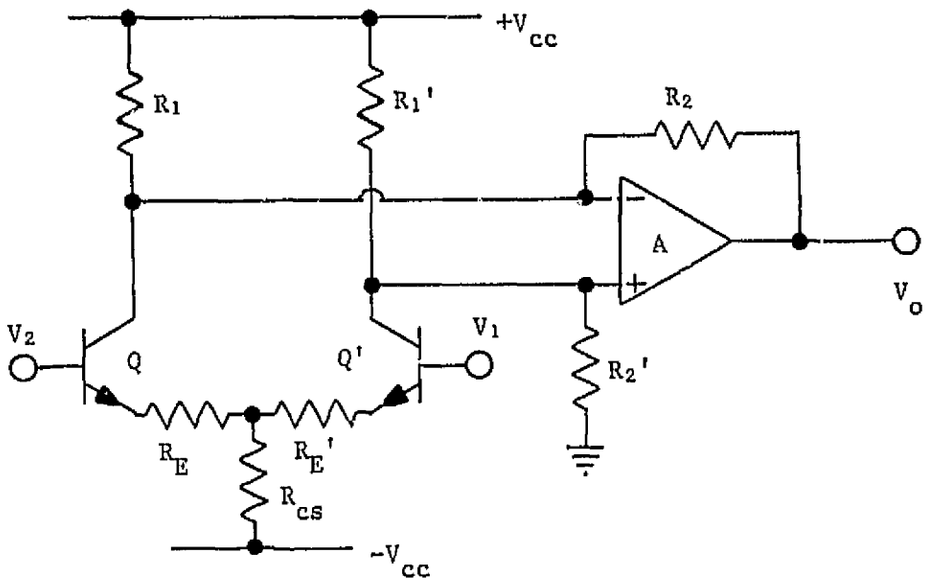

Figure 2-8. Bipolar Differential Instrumentation Amplifier.

If $$R_e = R_E + r_e$$

and if the circuit is balanced, then

$$\frac{V_o}{V_d} \simeq \frac{R_2}{R_e} . \qquad (2\text{-}56)$$

The CMR error equations are as follows:

For mis-match in R_e

$$CMR_1 = \left(\frac{R_e}{\Delta R_e}\right) \left(2 \frac{R_{cs}}{R_e} + 1\right). \tag{2-57}$$

For mis-match in source resistance

$$CMR_2 = \left(\frac{R_s}{\Delta R_s}\right) 2\beta \frac{R_{cs}}{R_s} . \tag{2-58}$$

For mis-match in transistor beta

$$CMR_3 = \left(\frac{\beta}{\Delta\beta}\right) 2\beta \frac{R_{cs}}{R_s} . \tag{2-59}$$

For mis-match in feedback resistors

$$CMR_4 = \left(\frac{R_1||R_2}{\Delta[R_1||R_2]}\right) \frac{R_{cs}}{R_e} . \tag{2-60}$$

For error due to transistor output resistance mis-match

$$CMR_5 = \left(\frac{r_{ce}}{\Delta r_{ce}}\right) \frac{\beta r_{ce}}{R_e} . \tag{2-61}$$

For r_{cb} mis-match

$$CMR_6 = \left(\frac{r_{cb}}{\Delta r_{cb}}\right) \frac{r_{cb}}{R_e} . \tag{2-62}$$

For the error due to a finite CMR of the op-amp

$$CMR = CMR_A \frac{R_{cs}}{R_e} . \tag{2-63}$$

For low distortion the value of R_e should be at least 100 times the value of the emitter dynamic resistance r_e [8].

The hybrid-π noise model for the bipolar transistor is shown in Appendix A and the basic analysis of the bipolar transistor noise is presented there.

The noise equations for the circuit of Figure 2-8 are as follows:

For the noise due to the base spreading resistance r_b of the transistors

$$R_{n1} = 2r_b. \tag{2-64}$$

For noise of both emitter resistors

$$R_{n2} = 2R_e. \tag{2-65}$$

For the collector shot noise of both transistors

$$R_{n3} = \frac{1}{r_e}\left(r_e + \frac{2}{\beta}R_e + \frac{R_s}{\beta}\right)^2. \tag{2-66}$$

For the base shot noise of both transistors

$$R_{n4} = \frac{1}{\beta r_e}(r_e + 2R_e + R_s)^2. \tag{2-67}$$

For the noise of R_1, R_2, R_1' and R_2'

$$R_{n5} = \frac{2R_e^2}{R_1 || R_2}. \tag{2-68}$$

For the noise of the op-amp

$$R_{n6} = \frac{\overline{e_n^2}}{4kT}\left(\frac{R_2 + R_1}{R_1}\right)^2\left(\frac{R_e}{R_2}\right)^2 + \frac{\overline{2i_n^2}}{4kT}R_e^2. \tag{2-69}$$

The noise is dominated by the large value of emitter resistor required to give low distortion. For this circuit both common mode rejection and noise performance are improved by lowering the value of R_e at the expense of linearity.

It has been shown [8] that the magnitude of the third harmonic distortion component of the bipolar differential amplifier can be approximated by

$$HD_3 = \left(\frac{q}{kT}\right)^2 \frac{V_d^2 \cdot 100\%}{48\ (1 + R_e/r_e)^3} . \qquad (2\text{-}70)$$

when the expression for the transistor diode static Volt-Ampere characteristic is

$$I_c = I_s \left(\exp\left(\frac{q\ V_{be}}{kT}\right) - 1\right), \qquad (2\text{-}71)$$

where I_c = collector current in amperes,

V_{be} = base-emitter voltage in volts,

q = electron charge,

I_s = reverse diode saturation current,

V_d = differential input voltage,

and r_e = diode dynamic resistance.

If the input stage dynamic range is not to be exceeded, Inequality (2-72) must hold.

$$V_d \leq I\ 2R_e. \qquad (2\text{-}72)$$

Recalling that

$$R_e = R_E + r_e, \qquad (2\text{-}73)$$

and that

$$r_e = \frac{kT}{qI} . \tag{2-74}$$

Equations (2-71), (2-72), (2-73), and (2-74) can be combined to give

$$HD_3 \leq \frac{1}{12} \frac{r_e}{R_e} \times 100\%. \tag{2-75}$$

For a resistance ratio of 100:1 the distortion would be about 0.083%. The resistance ratio should therefore be held to a ratio of about 100:1 for low distortion. If

$$V_d = 2R_e I, \tag{2-76}$$

then

$$HD_3 = \frac{1}{12} \frac{r_e}{R_e} \times 100\%. \tag{2-77}$$

This indicates that less distortion is obtained for a fixed input at high bias currents, however, the noise performance may be degraded for high currents.

Bipolar Input With Single Resistor Gain Selection

A slight modification of the circuit of Figure 2-8 yields single resistor gain selection as shown in Figure 2-9. If

$$R_g = R_g' + 2r_e, \tag{2-78}$$

and

$$R_{cs} = \infty,$$

then the gain is given by

$$\frac{V_o}{V_d} = \frac{2R_2}{R_g} . \qquad (2\text{-}79)$$

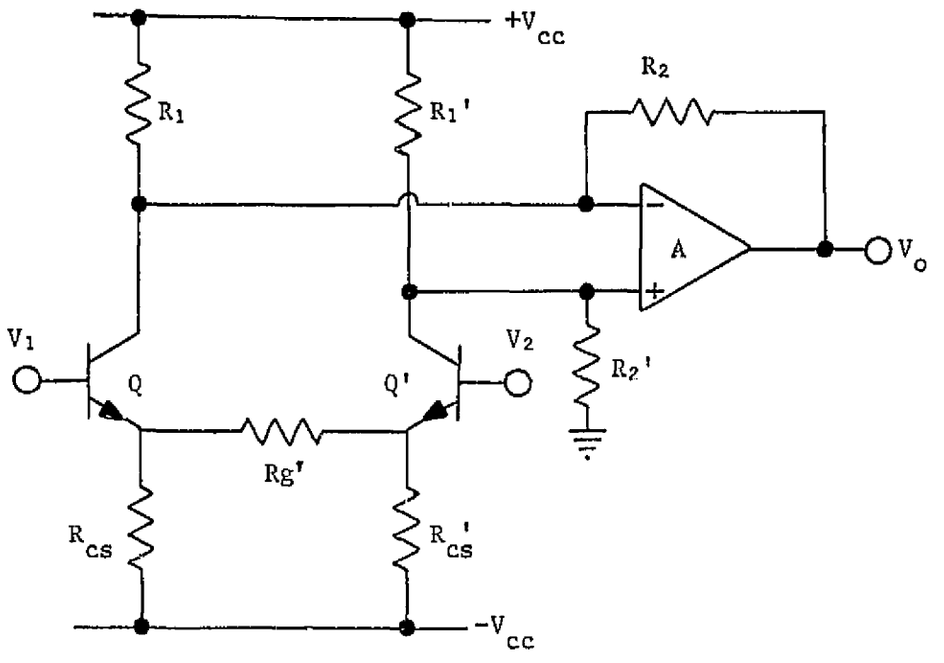

Figure 2-9. Open Loop Bipolar Instrumentation Amplifier With Single Resistor Gain Selection.

The third harmonic distortion is given by

$$HD_3 \leq \frac{1}{12} \frac{2r_e}{R_g} \times 100\%. \qquad (2\text{-}80)$$

The common mode error equations are as follows:

For error in current source output resistance matching

$$CMR_1 = \left(\frac{R_{cs}}{\Delta R_{cs}}\right) \left(\frac{2R_{cs}}{R_g}\right). \qquad (2\text{-}81)$$

For transistor mis-match in emitter dynamic resistance

$$CMR_2 = \left(\frac{r_e}{\Delta r_e}\right) \left(\frac{2R_{cs}^2}{r_e R_g}\right). \tag{2-82}$$

For mis-match in feedback resistors

$$CMR_3 = \left(\frac{R_1 || R_2}{\Delta(R_1 || R_2)}\right) \frac{2R_{cs}}{R_g}. \tag{2-83}$$

For finite CMR of op-amp

$$CMR_4 = CMR_A \left(\frac{2R_{cs}}{R_g}\right). \tag{2-84}$$

For mis-match in transistor beta

$$CMR_5 = \left(\frac{\beta}{\Delta\beta}\right) 2\beta \frac{R_{cs}}{R_s}. \tag{2-85}$$

For mis-match in source resistance

$$CMR_6 = \left(\frac{R_s}{\Delta R_s}\right) 2\beta \frac{R_{cs}}{R_s}. \tag{2-86}$$

For r_{ce} mis-match

$$CMR_7 = \left(\frac{r_{ce}}{\Delta r_{ce}}\right) \frac{2\beta r_{ce}}{R_g}. \tag{2-87}$$

For transistor base to collector resistance mis-match

$$CMR_8 = \left(\frac{r_{cb}}{\Delta r_{cb}}\right) \frac{2R_{cb}}{R_g}. \tag{2-88}$$

The noise equations are as follows:

For thermal noise of R_1, R_2, R_1', R_2', if $R_1' \simeq R_1$ and $R_2' \simeq R_2$,

$$R_{n1} = \frac{R_g}{2(R_1 || R_2)} . \tag{2-89}$$

For op-amp noise

$$R_{n2} = \frac{\overline{e_n}^2}{2kT} \left(\frac{R_g^2}{4(R_1 || R_2)^2} \right) + \frac{\overline{i_n}^2}{4kT} \left(\frac{1}{2} R_g^2 \right). \tag{2-90}$$

For thermal noise of R_g'

$$R_{n3} = R_g', \tag{2-91}$$

for noise of current source,

$$R_{n4} = \frac{\overline{i_n}^2}{4kT} 2R_g^2. \tag{2-92}$$

For collector shot noise of the transistors

$$R_{n5} = \frac{1}{r_e} \left(r_e + \frac{R_g}{\beta} + \frac{R_s}{\beta} \right)^2 . \tag{2-93}$$

For base shot noise of the transistors

$$R_{n6} = \frac{1}{\beta r_e} (r_e + R_g + R_s)^2. \tag{2-94}$$

For noise of base spreading resistance

$$R_{n7} = 2r_b. \tag{2-95}$$

The total noise is dominated by the thermal noise of R_g' for low distortion operation. Care must be taken in designing the current sources to insure high output impedance and low noise. For high values of R_g' the noise of the current source could be dominant.

Bipolar Input With Current Mirror

Another modification of the basic bipolar differential amplifier uses a current mirror to replace resistors R_1 and R_1' as in Figure 2-10.

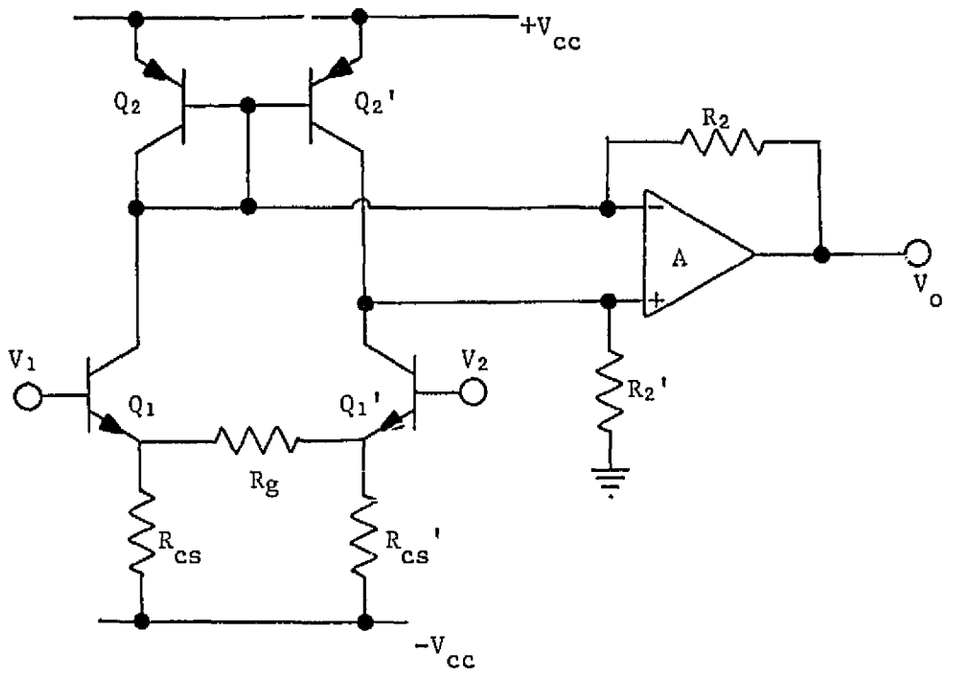

Figure 2-10. Bipolar Instrumentation Amplifier With Current Mirror.

The common mode error equations are as follows:

For Q_2 Beta mis-match

$$CMR_1 = \left(\frac{\beta_2}{\Delta\beta_2}\right) \frac{2\beta_2 R_{cs}}{R_g} . \qquad (2\text{-}96)$$

For finite beta of Q_2

$$CMR_2 = \frac{\beta_2}{1} \frac{R_{cs}}{R_g} . \qquad (2\text{-}97)$$

For Q_2 emitter resistance mis-match

$$CMR_3 = \left(\frac{r_e}{\Delta r_e}\right)_2 \frac{2R_{cs}}{R_g} . \tag{2-98}$$

For mis-match in R_2

$$CMR_4 = \left(\frac{R_2}{\Delta R_2}\right) \frac{R_2}{R_e} \frac{2R_{cs}}{R_g} . \tag{2-99}$$

For finite CMR of op-amp

$$CMR_5 = CMR_A \frac{2R_{cs}}{R_g} . \tag{2-100}$$

For Q_1 emitter mis-match

$$CMR_6 = \left(\frac{r_e}{\Delta r_e}\right)_1 \frac{2R_{cs}^2}{r_{e1} R_g} . \tag{2-101}$$

For current source mis-match

$$CMR_7 = \left(\frac{R_{cs}}{\Delta R_{cs}}\right) \frac{2R_{cs}}{R_g} . \tag{2-102}$$

For r_{ce} mis-match of Q_1

$$CMR_8 = \left(\frac{r_{ce_1}}{\Delta r_{ce1}}\right) \frac{2 \beta r_{ce}}{R_g} . \tag{2-103}$$

For r_{cb} mis-match of Q_1

$$CMR_9 = \left(\frac{r_{cb_1}}{\Delta r_{cb1}}\right) \frac{2r_{cb1}}{R_g} . \tag{2-104}$$

For Q_1 beta mis-match

$$CMR_{10} = \left(\frac{B_1}{\Delta B_1}\right) \frac{2B_1 R_{cs}}{R_g} . \tag{2-105}$$

For source mis-match

$$CMR_{11} = \left(\frac{R_s}{\Delta R_s}\right) \frac{2B R_{cs}}{R_g} . \tag{2-106}$$

The noise equations are as follows:

For thermal noise of R_2 and R_2'

$$R_{n_1} = \frac{R_g^2}{2R_2} . \tag{2-107}$$

For thermal noise of R_g

$$R_{n_2} = R_g. \tag{2-108}$$

For collector shot noise of Q_1 and Q_1'

$$R_{n_3} = \frac{1}{r_{e1}} \left(r_{e_1} + \frac{R_g}{\beta_1} + \frac{R_s}{\beta_1}\right)^2. \tag{2-109}$$

For base shot noise of Q_1 and Q_1'

$$R_{n_4} = \frac{1}{\beta r_{e1}} (r_{e_1} - R_g + R_s)^2. \tag{2-110}$$

For noise of current source

$$R_{n_5} = \frac{\overline{i_n^2}}{4kT} 2R_g^2. \tag{2-111}$$

For noise of op-amp

$$R_{n_6} = \frac{\overline{e_n^2}}{4kT} \frac{R_g^2}{4R_2^2} + \frac{2\overline{i_n^2}}{4kT} \frac{R_g^2}{4} . \qquad (2\text{-}112)$$

For base and collector shot noise of Q_2 and Q_2'

$$R_{n_7} = \frac{R_g^2}{4r_{e_2}} . \qquad (2\text{-}113)$$

The noise is dominated by the noise of Q_2 and Q_2' and is excessive being in the range of 250 kΩ (63 nv/$\sqrt{Hz}$). The noise of the current mirror can be lowered by adding emitter resistors to Q_2 and Q_2'; however, this new modified configuration would have the same characteristics as the circuit of Figure 2-9 (p. 25) and would have more noise than that circuit, therefore, the current mirror is not recommended for a low noise amplifier design.

Bipolar Input With Feedback

Another bipolar circuit proposed [9] uses feedback into the emitter circuit as in Figure 2-11. The differential gain of this circuit can be shown to be

$$A_d = 1 + \frac{R_2}{R_E} \qquad (2\text{-}114)$$

The common mode equations for the dominant sources of common mode error are as follows:

For mis-match in collector resistors

$$CMR_1 = \left(\frac{R_1}{\Delta R_1}\right) A_d . \qquad (2\text{-}115)$$

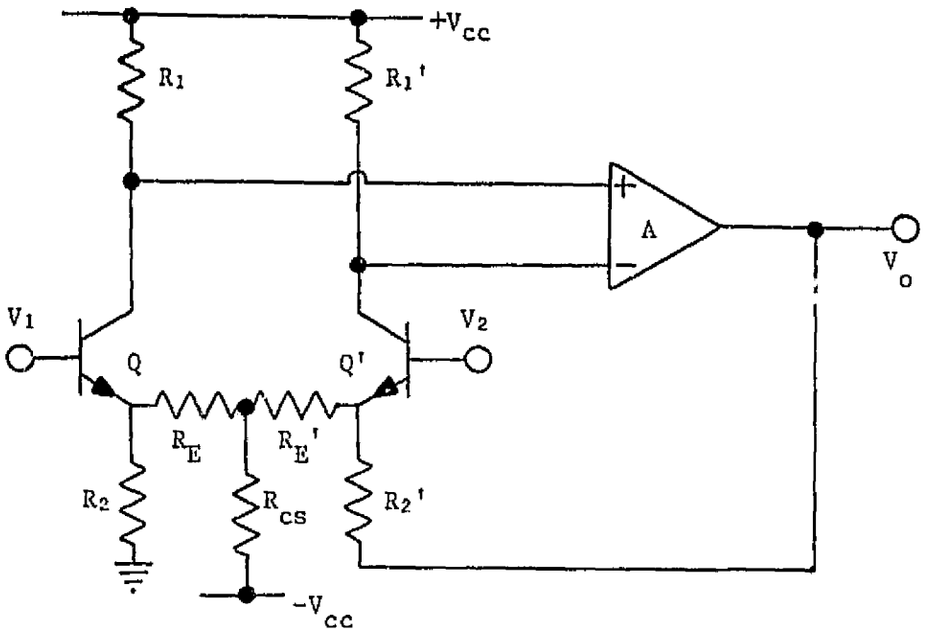

Figure 2-11. Bipolar Amplifier With Feedback.

For mis-match in feedback resistors

$$CMR_2 = \left(\frac{R_2}{\Delta R_2}\right) A_d. \qquad (2\text{-}116)$$

For transistor emitter mis-match

$$CMR_3 = \left(\frac{r_e}{\Delta r_e}\right) \left(\frac{Rf}{r_e}\right) + 1. \qquad (2\text{-}117)$$

For transistor beta mis-match

$$CMR_4 = \left(\frac{\beta}{\Delta\beta}\right) \frac{1}{2} A_d. \qquad (2\text{-}118)$$

This circuit exhibits very poor common mode rejection.

The noise analysis yields for the dominant noise sources, the following:

For thermal noise of R_2, R_2', R_E and R_E'

$$R_{n1} = 2R_E \,||\, \frac{R}{2} . \tag{2-119}$$

For noise of R_1 and R_1'

$$R_{n2} = \frac{2(2R_E||R_2/2)^2}{R_1} . \tag{2-120}$$

For collector shot noise of two transistors

$$R_{n3} = \frac{1}{r_e} \left(r_e + \frac{2R_E||R_2/2}{\beta} + \frac{R_s}{\beta} \right)^2 . \tag{2-121}$$

For base shot noise of the transistor

$$R_{n4} = \frac{1}{\beta r_e} (r_e + 2R_E \,||\, r_2/2 + R_s)^2 . \tag{2-122}$$

The total noise of this circuit is comparable to the noise of the other bipolar input circuits.

Amplifier Comparison

The equations presented previously can now be used to compare the relative merit of each circuit. Each circuit was analyzed for the same gain, bias, component matching tolerance and source resistance. This comparison is valid for one set of conditions only; however, all the circuits are characterized by increases in CMRR and/or decreases in noise for corresponding increases in gain, improvement in component matching, and reduction in source resistance. Therefore, the comparison presented here should prove useful.

Parameters for each circuit are chosen to give a differential gain of 100, harmonic distortion less than 0.1%, source resistance of 100 Ω, source resistance mis-match of 10 Ω, resistor matching of 1.0%, matching of all transistor parameters to 1.0%, op-amp gain matching of 1.0%, an op-amp gain greater than 10,000, and op-amp CMRR of 100 dB.

Table II-1 presents the calculated CMRR and equivalent noise resistance of each circuit indicated by the appropriate Figure number.

TABLE II-1

Noise and CMRR Comparison of Several Instrumentation Amplifiers

Figure	CMRR (dB)	R_n (kΩ)
2-1	77	8.2
2-4	80	18.4
2-5	86	12.2
2-6	86	12.2
2-7	80	15.2
2-8	108	10.3
2-9	107	37.0
2-10	107	243.0
2-12	72	37.0

CHAPTER III

A NEW APPROACH

Introduction

The purpose of this chapter shall be to set down the general ideas for improving the performance of differential amplifiers, to present one method of improving noise and common mode rejection and to outline a circuit capable of realizing these improvements.

The General Circuit

The input device for a differential stage can be represented by the model of Figure 3-1 (a) for low frequencies. The device will have an input resistance r_{in}, transconductance gm, output resistance r_o, and input to output resistance r_{io}.

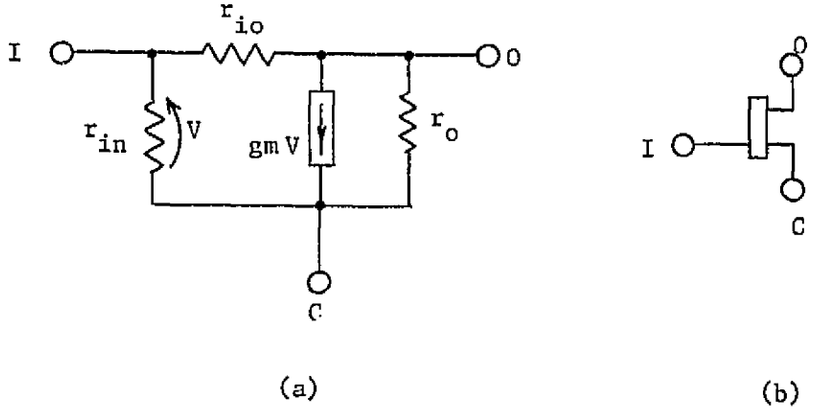

Figure 3-1. Basic Device Model

The symbol of Figure 3-1 (b) will be used to represent the general input device. The circuit for the general differential amplifier is shown in Figure 3-2.

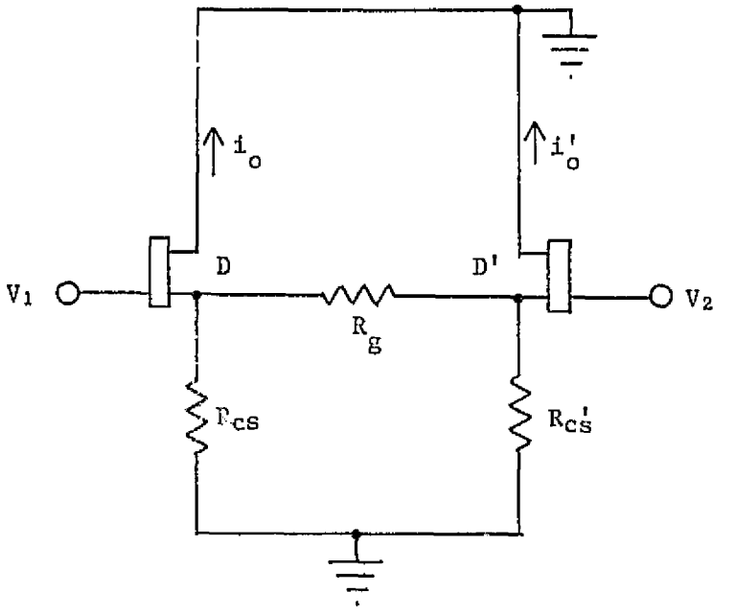

Figure 3-2. General Differential Amplifier.

This circuit allows for single resistor gain selection by setting R_g to give desired gain. R_{cs} and R_{cs}' are used to simulate required current sources. Substituting the general device model into the circuit of Figure 3-2 and solving for the differential and common mode gains, the following results are obtained. For the differential gain

$$\frac{\Delta i_o}{V_d} \cong \frac{1}{\frac{R_g}{2} + \frac{1}{gm}} . \qquad (3\text{-}1)$$

For the common mode rejection factor due to mis-match in device transconductance

$$CMR_1 \cong \left(\frac{gm}{\Delta gm}\right) \; gm(r_o||R_{cs}). \tag{3-2}$$

For mis-match in device output resistance

$$CMR_2 \cong \left(\frac{r_o}{\Delta r_o}\right) \; r_o \; gm. \tag{3-3}$$

For mis-match in device input resistance

$$CMR_3 \cong \left(\frac{r_{in}}{\Delta r_{in}}\right) \; \frac{2}{R_g} \; gm \; r_{in} \; (r_o||R_{cs}). \tag{3-4}$$

For mis-match in device input to output resistance

$$CMR_4 \cong \left(\frac{r_{io}}{\Delta r_{io}}\right) \; \frac{2}{R_g} \; gm^2 \; r_{io}. \tag{3-5}$$

For mis-match in source resistance

$$CMR_5 \cong \left(\frac{R_s}{\Delta R_s}\right) \; \frac{2}{R_g \; R_s} \; gm \; r_{in}^2 \; (r_o||R_{cs}). \tag{3-6}$$

For mis-match in current source output resistance

$$CMR_6 \cong \left(\frac{R_{cs}}{\Delta R_{cs}}\right) \; \frac{2}{R_g} \; R_{cs}. \tag{3-7}$$

These approximations are subject to the assumption that r_{in}, r_o, and R_{cs} are much larger than R_g, R_s, and 1/gm. This poses the restriction that R_g must have a relatively small value (typically less than 10 kΩ). Notice that increased common mode rejection can be obtained in every case by increasing the relatively high resistances (r_{in}, r_o, r_{io}, R_{cs})

and decreasing the relatively small resistances (R_g, $1/g_m$, R_s) providing parameter matching can be maintained. The common mode rejection can also be improved with better component matching.

For low distortion in a circuit of this type the resistance R_g should be kept at least 100 times greater than 1/gm [8]. This causes the input differential voltage to be impressed across R_g causing a current I to flow. This current is limited to the value of the quiescent bias current. Assuming that the differential output current of the stage will be transformed into a single ended output voltage and that the input stage should not saturate before the output reaches its maximum swing, the value of R_g is limited by the expression

$$R_g \geq \frac{V_o \text{ max}}{A_d I_q}, \tag{3-8}$$

where V_o max is the maximum output voltage swing, A_d is the differential gain, and I_q is the input stage bias current. In most applications this restriction will cause R_g to be the dominant source of electronic noise for low values of gain. The noise resistance of an amplifier in which R_g is the dominant noise source would be given simply by

$$R_n = R_g. \tag{3-9}$$

This limitation would hold in most cases until the value of R_g became less than about 1000 Ω to 500 Ω. A decrease in R_g will dictate an increase in bias current to maintain dynamic range and an increase in transconductance to maintain low distortion. Fortunately an increase in current is consistent with an increase in transconductance in both the bipolar and field effect transistors. The increased current is

consistent with lower noise in the FET but not necessarily so with the bipolar transistor.

The most advantageous parameter change in the input device for low noise and high common mode rejection would be to increase the transconductance allowing lower values of R_g and therefore lower noise while at the same time increasing common mode rejection as predicted by Equations (3-2) through (3-7).

A composite input device has been proposed [2], [3] to solve the distortion and common mode rejection problems simultaneously. In these circuits several bipolar devices are connected together to obtain a composite device of very high transconductance and very high output resistance. The common mode rejection obtained with these circuits is excellent; however, the circuits are biased at low currents requiring high values of R_g to avoid saturation of the input stage. The noise performance is therefore limited.

From the previous discussion the FET would seem to be the ideal input device. It has very high input resistance, low noise for high current, and very low equivalent input noise current. FET's do however have a relatively low transconductance, low output resistance, and are generally more difficult to match than bipolar transistors. Therefore, let us consider a composite device with an FET input stage to achieve low noise, high dynamic range and high common mode rejection all in one circuit.

The Composite Input Stage

To first understand the concept of a composite input stage the circuit of Figure 3-3 is helpful. The op-amp causes the input voltage

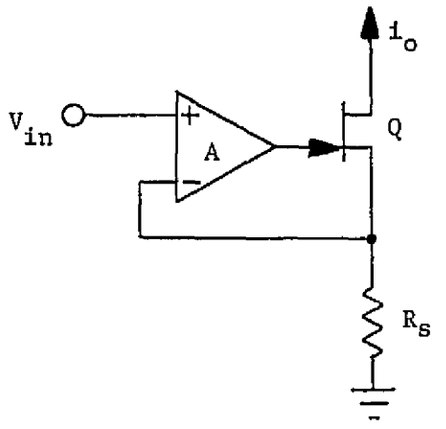

Figure 3-3. Precision Voltage Controlled Current Source.

to be matched by a similar voltage at the top of the resistor R_S causing a current $i_o = V_{in}/R_S$ to flow. This current must flow through the FET to the output. The output resistance of this circuit is approximately equal to the FET input resistance [9]. The op-amp and FET above form a composite input device with a transconductance of

$$Gm = A\ gm. \tag{3-10}$$

Two of these devices can be combined to form a differential input stage as in Figure 3-4. Using dual monolithic op-amps, common mode rejection can be achieved with this circuit equivalent to the common mode rejection of the op-amps alone; i.e., approximately 100 dB. The noise is dominated by the op-amp noise and is limited to about 12 kΩ noise resistance using an RC4136 quad op-amp.

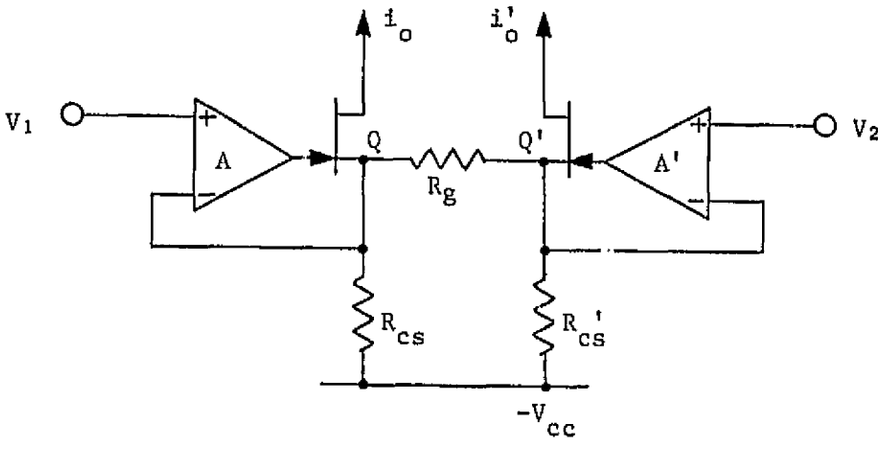

Figure 3-4. Precision Differential Input Stage.

A low noise input stage can be added to this circuit giving a new composite device as shown in Figure 3-5. The composite device model parameters for this circuit using the model of Figure 3-1 (p.35) are

$$gm = gm_1 R_d A gm_2, \tag{3-11}$$

$$r_o = r_{ds2} \tag{3-12}$$

$$r_{io} \simeq \infty, \tag{3-13}$$

$$r_{in} = r_{gs1}. \tag{3-14}$$

As pointed out in Equation (3-7), the matching of current sources is important in achieving high common mode rejection. If the polarity of the output transistor is changed and this transistor turned around

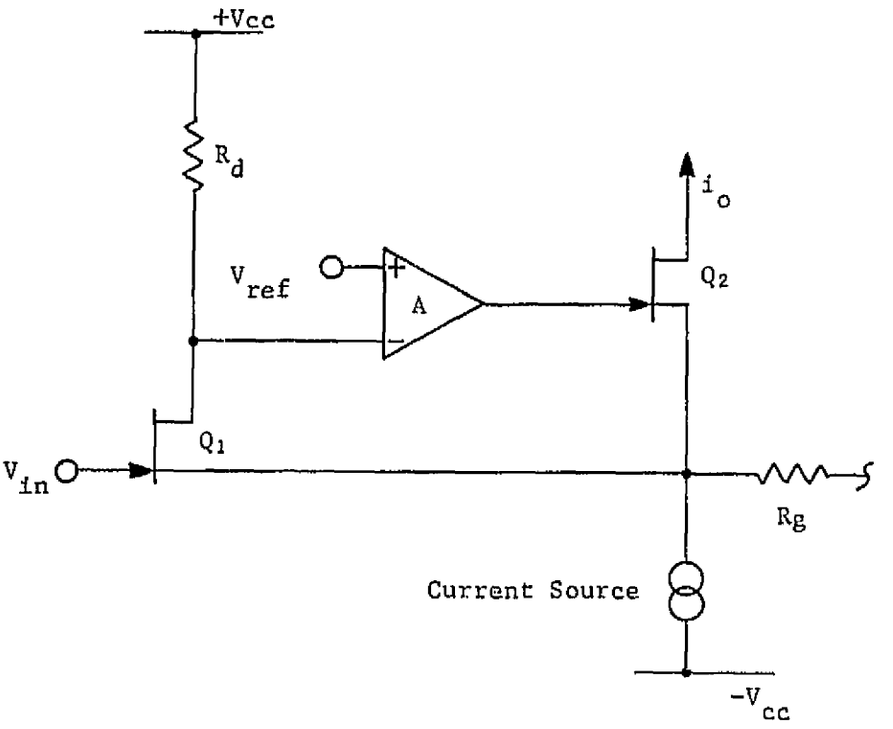

Figure 3-5. Low Noise Input Circuit.

the current source can be eliminated as shown in Figure 3-6. This configuration was chosen as the input stage for the amplifier to be developed in this study.

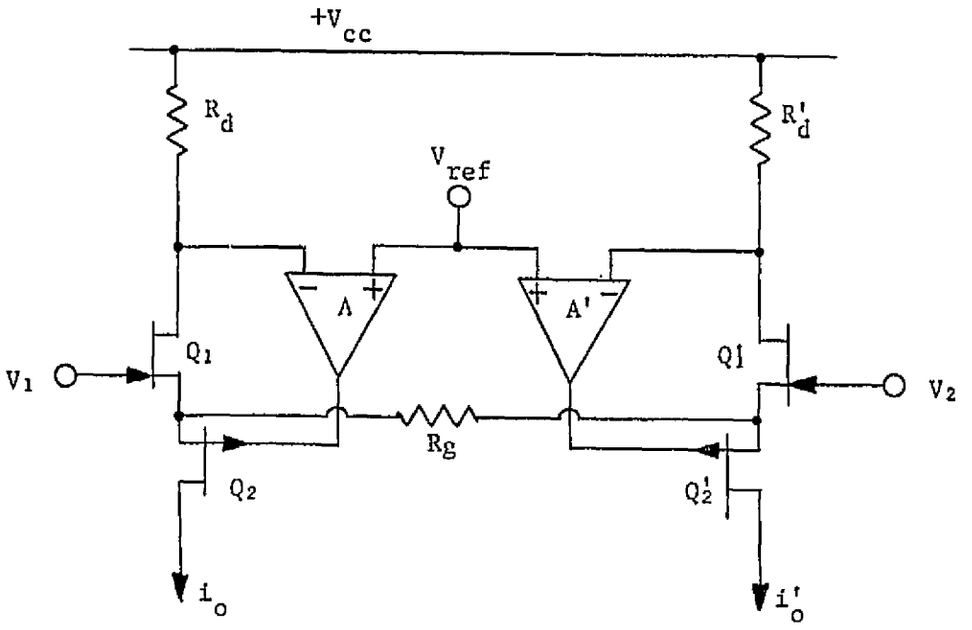

Figure 3-6. Low Noise, High Common Mode Rejection Input Stage.

The Output Stage

Several methods have been proposed to transform differential current signals intc single ended output voltages [2], [3], [6], [9]. The simplest of these circuits is illustrated by Figure 3-7. For an amplifier input common mode voltage swing to within 80% of the negative power supply, the two inputs of A_2 in Figure 3-7 must be biased at a

voltage at least 80% of the negative supply. Minimization of the amplifier noise requires relatively low value resistors for R_f (typically 2500 Ω) and the maximum value possible for R and R'. However, if the two inputs of A_2 are at -0.8 VCC then high bias currents I_f and I_f' must flow through R and R' along with high input stage bias currents I_b. Therefore by Ohms law the values of R and R' are low (typically 400 Ω) limiting noise performance. The bias current I_f also could cause unwanted heating of the op-amp chip and restrict output voltage swing.

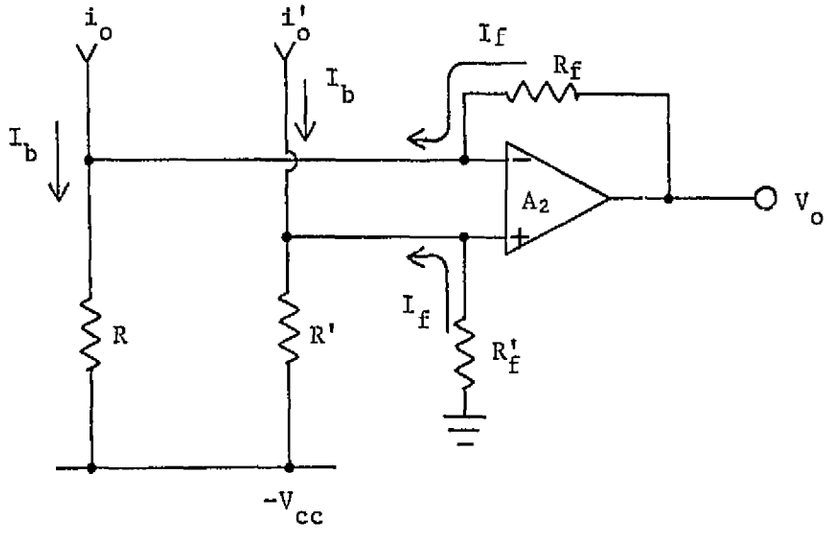

Figure 3-7. Simple Output Stage.

An improved version of the circuit in Figure 3-7 uses two current mirrors to turn the differential current around allowing large resistors for R and R' while eliminating the required bias current from the output amplifier. This circuit is shown in Figure 3-8. The current mirrors used [10] have very good current matching between input and output, very high output resistance and excellent linearity.

Another modification to the circuit of Figure 3-8 yields an extra degree of versatility in that two new control input terminals are created, [11] termed "output reference" (usually tied to the output circuit ground) and "output sense" (usually tied to the output terminal). This circuit is shown in Figure 3-9.

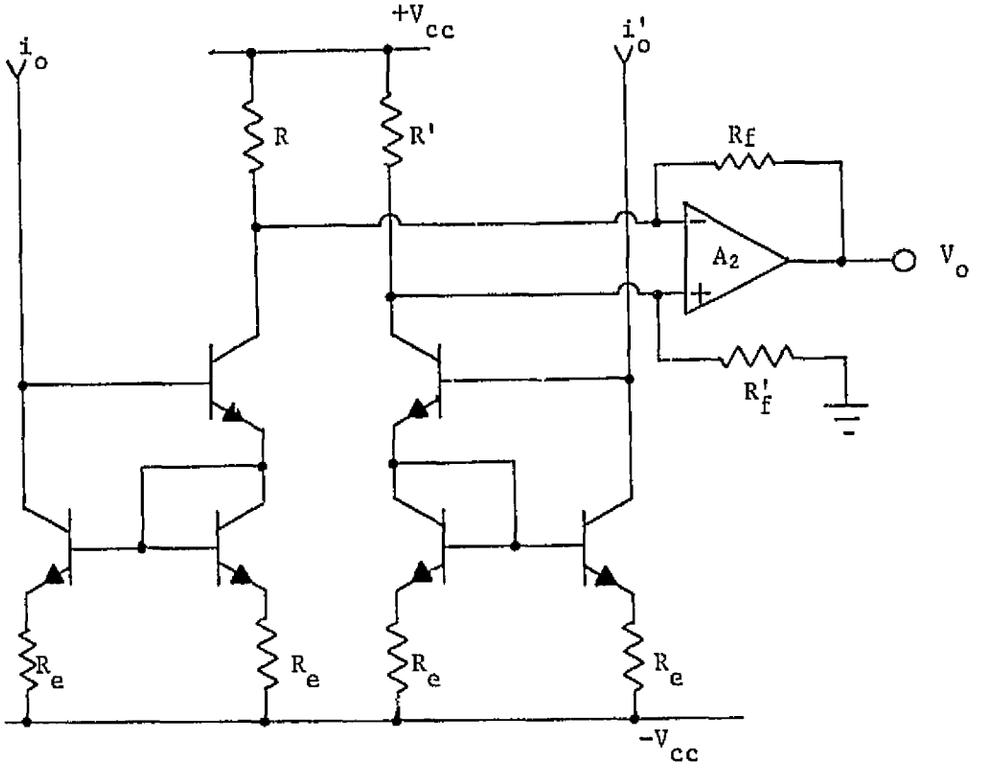

Figure 3-8. Output Stage With Current Mirrors.

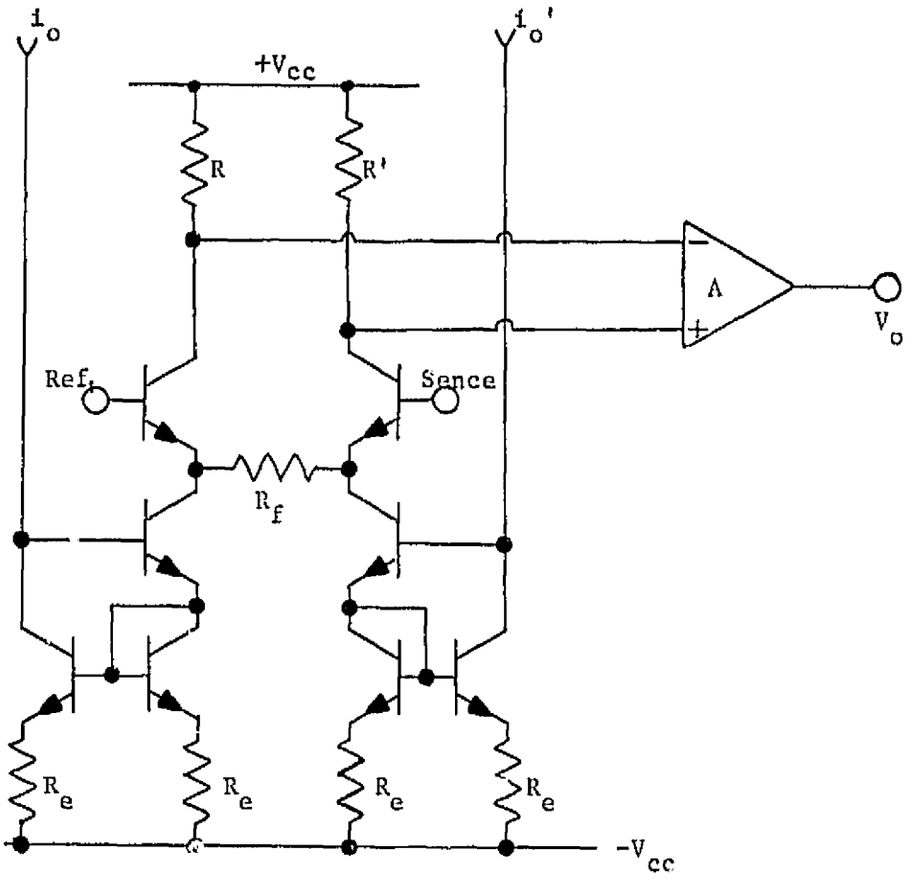

Figure 3-9. Output Stage With Sense And Reference Terminals.

This circuit again requires the inputs of A_2 to be biased to at least 80% of V_{cc} supply voltage, although there is no bias current required from the output of A_2.

The Complete Circuit

The circuit offering the best overall performance as suggested by this study appears in Figure 3-10. The output stage was chosen to

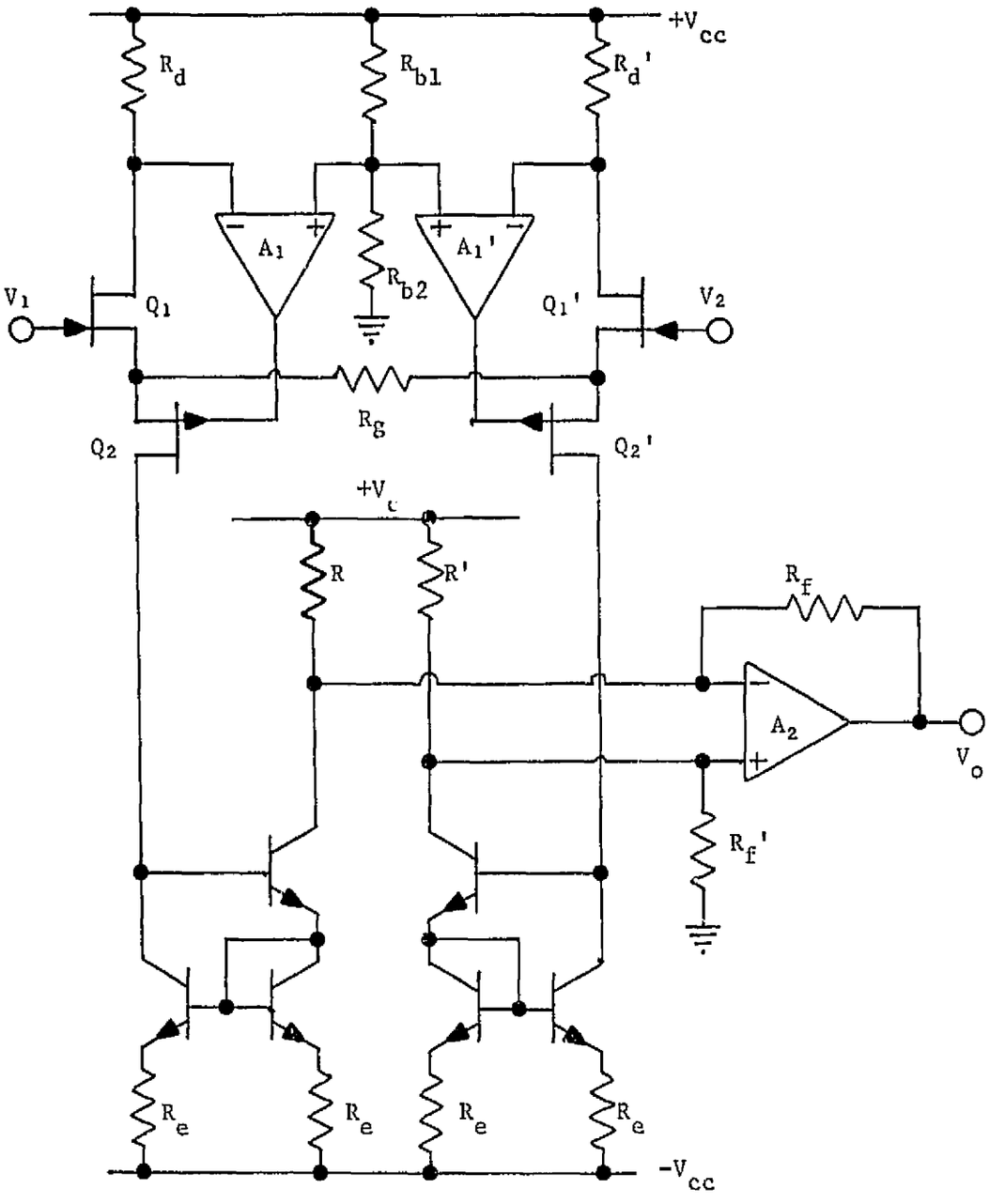

Figure 3-10. New Instrumentation Amplifier.

eliminate the need for operating the inputs of A_2 at high bias voltages. The circuit will be analyzed and component values assigned in subsequent chapters. The differential mode gain of this amplifier is given by

$$A_d = \frac{2 R_f}{R_g}. \qquad (3\text{-}15)$$

CHAPTER IV

NOISE ANALYSIS OF THE NEW INSTRUMENTATION AMPLIFIER

Introduction

In this chapter the dominant noise sources of a specific implementation of the new low noise instrumentation amplifier configuration will be quantitatively discussed and the circuit parameters will be optimized for minimum noise.

The Basic Parameters

There are four parameters of the amplifier in Figure 3-10 (p. 47) affecting electronic noise. These are maximum output voltage range, maximum input common mode range, input stage bias current and amplifier differential gain. For a quality op-amp the output range approaches the supply voltage that is

$$V_o \text{ max} \approx \pm V_{cc}. \tag{4-1}$$

The input common mode range is limited approximately to the Q_1 drain voltage in the positive direction and to the Q_2 drain voltage in the negative direction.

$$V_{D2} \leq V_{cm} \leq V_{D1}. \tag{4-2}$$

These voltages are controlled by the values of I_D, V_{cc}, R_D . that

$$V_{D1} = V_{cc} - I_D R_{D1}, \tag{4-3}$$

and

$$V_{D2} = -V_{cc} + 2V_{be} + I_D R_e. \tag{4-4}$$

The values of R_D and R_e can now be defined in terms of the basic parameters.

$$R_D = \frac{V_{cc} - V_{cm\ max}}{I_D}. \tag{4-5}$$

$$R_e = \frac{V_{cc} - V_{cm\ max} - 2V_{be}}{I_D}, \tag{4-6}$$

R_g should be minimized to achieve the lowest noise; however, its value is limited to some minimum value if the input stage is not allowed to saturate before the output voltage clips. This minimum is given by

$$R_g \geq \frac{V_{o\ max}}{A_d I_d}, \tag{4-7}$$

where A_d is the differential gain. The value of R_g is thus limited by three of the major parameters.

R and R' are selected to set the inputs of A_2 near zero volts.

$$R = \frac{V_{cc}}{I_D}. \tag{4-8}$$

R_f is defined to make the output voltage reach its limit just as the input stage saturates.

$$R_f = \frac{V_{o\ max}}{2I_D}, \tag{4-9}$$

The transconductance of the input FET's is approximately

$$gm_1 \simeq \left(\frac{2\sqrt{Id_{ss}}}{V_p}\right) \sqrt{I_d} \quad . \tag{4-10}$$

The noise of Q_1 is directly related to the transconductance and will be discussed in detail later.

Now all the amplifier parameters affecting noise have been defined in terms of four major parameters. The noise performance will later be optimized with respect to these parameters and the design trade-offs will be defined.

Noise of Input FET's

The amplifier will have an absolute minimum noise limited by the noise of the input transistors selected. This minimum noise due to each FET is

$$R_n = \left(\frac{T_j}{T_a}\right)\left(\frac{2}{3}\right) \frac{C}{gm}, \tag{4-11}$$

where T_j is the transistor chip temperature, T_a is the ambient temperature, and C is a factor varying between one and two depending on the particular process used to make the transistor [12], [13]. Normally the temperature ratio is unity; however, at high bias currents and voltage, device heating can cause an increase in output noise. The chip temperature is given by

$$T_j = T_a + \theta ja\ I_d\ V_{ds}, \tag{4-12}$$

where θja is the thermal resistance between chip and ambient, and V_{ds} is the drain to source voltage. If the FET's are operated near I_{dss} for minimum noise, V_{ds} will be approximately V_{D_1} as in Equation (4-3).

The transconductance is also dependent on temperature and varies as the fourth root of temperature [13], for I_d near I_{dss}.

$$gm = \left(\frac{2\sqrt{I_{dss}}}{V_p}\right) \sqrt[4]{\frac{T_a}{T_j}} \sqrt{I_d}. \tag{4-13}$$

The noise of two transistors Q_1 and Q_1' in the same package can then be written in terms of the major parameters.

$$R_{n1} = 2\left(1 + \frac{\theta ja\ 2I_d\ V_d}{T_a}\right)^{1.25} \left(\frac{2\ I_{dss}}{V_p}\right) \sqrt{I_d}. \tag{4-14}$$

Other Noise Sources

Using common circuit analysis techniques the other significant noise sources were found to be given by the following:

For noise of A_1 and A_1'

$$R_{n2} = 2\left(\frac{R_g}{2} + \frac{1}{gm_1}\right)^2 R_d^2 \frac{\overline{e_{na_1}}^2}{4kT}. \tag{4-15}$$

For noise of R_g

$$R_{n3} = R_g. \tag{4-16}$$

For noise of R_d and R_d'

$$R_{n4} = 2\ R_d \left(\frac{R_g}{2} + \frac{1}{gm}\right)^2. \tag{4-17}$$

For noise of all four resistors R_e

$$R_{n5} = \frac{R_g^2}{R_e}. \tag{4-18}$$

For noise of the current mirror transistors

$$R_{n6} = \frac{2R_g^2}{r_e \beta} . \qquad (4\text{-}19)$$

For noise of the output op-amp

$$R_{n7} = \frac{\overline{e_{nA_2}}^2}{4kT} \left(\frac{1.5}{A_d}\right)^2 . \qquad (4\text{-}20)$$

All these noise sources can be rewritten in terms of the four major parameters V_{cc}, V_{cm} max, I_d and A_d.

At this point a computer becomes handy in that all the noise sources and the total noise can rapidly be evaluated relative to the four major parameters.

Evaluation

Using specifications of the 2N5565 dual monolithic FET for Q_1 and Q_1' and typical low noise op-amp specifications (see Appendix B) Figure 4-1 shows the predicted equivalent noise resistance of the instrumentation amplifier of Figure 3-10 (p. 47) as a function of A_d and I_d with V_{cm} max and V_{cc} fixed. The noise has a minimum value for each gain within a narrow band of drain currents between 3 ma and 4 ma.

For a given gain this minimum noise changes with V_{cm} max as shown in Figure 4-2. Figure 4-2 indicates an engineering trade-off between noise and available common mode range.

A bias current of 3 ma would give low noise for a range of gains according to Figure 4-1. Using this bi :, Figure 4-3 gives the predicted noise as a function of gain.

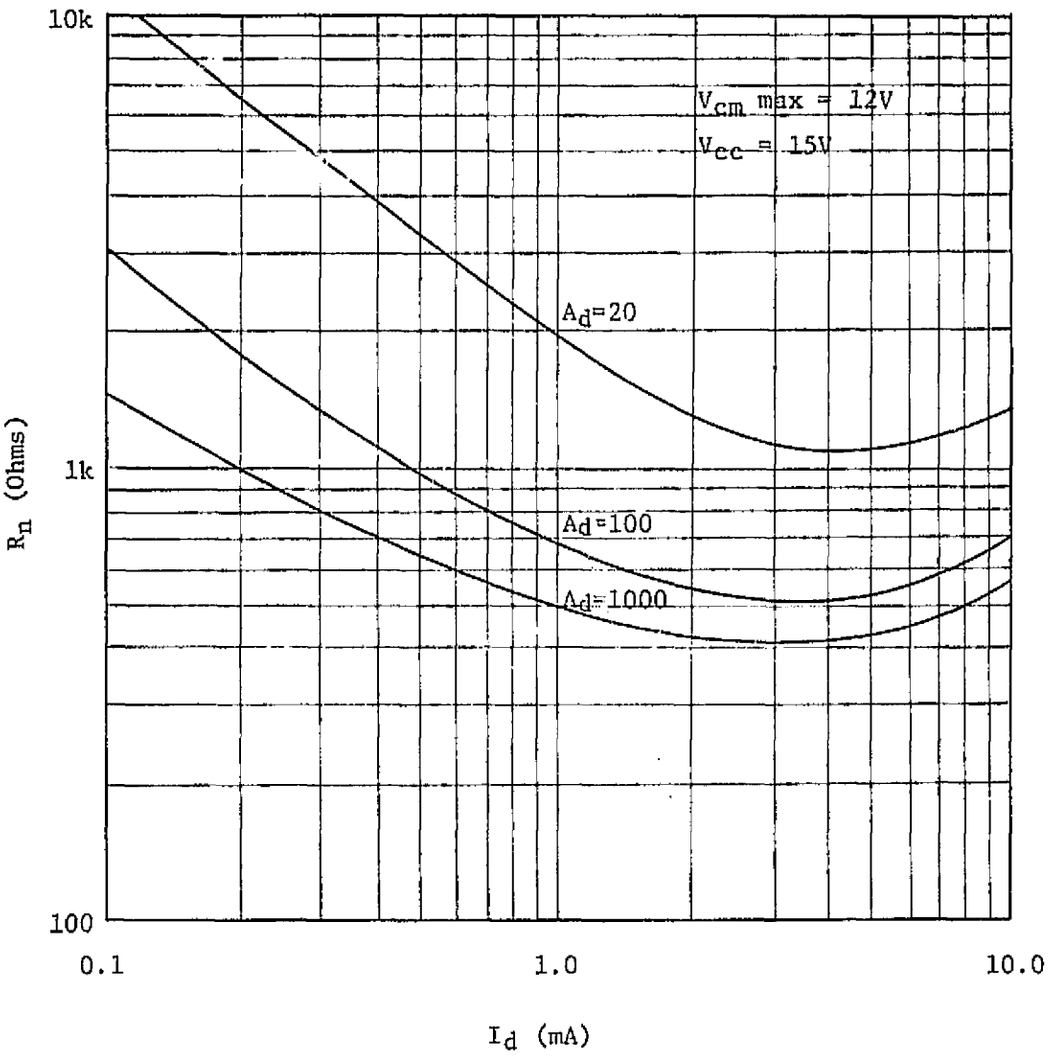

Figure 4-1. Equivalent Noise Resistance as a Function of Drain Current and Gain for the Circuit of Figure 3-10 (p. 47).

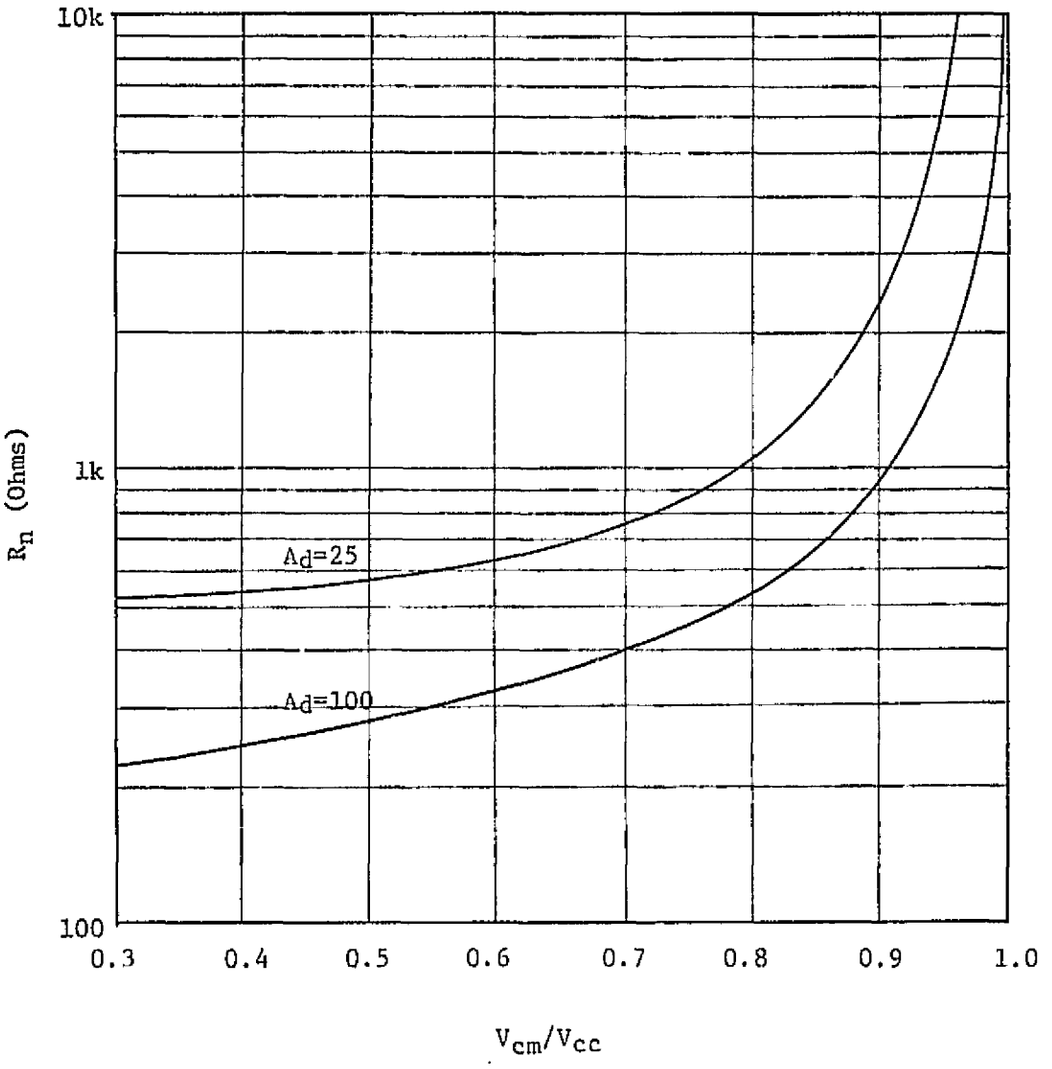

Figure 4-2. Equivalent Noise Resistance as a Function of Gain and Common Mode Range for Circuit of Figure 3-10 (p. 47).

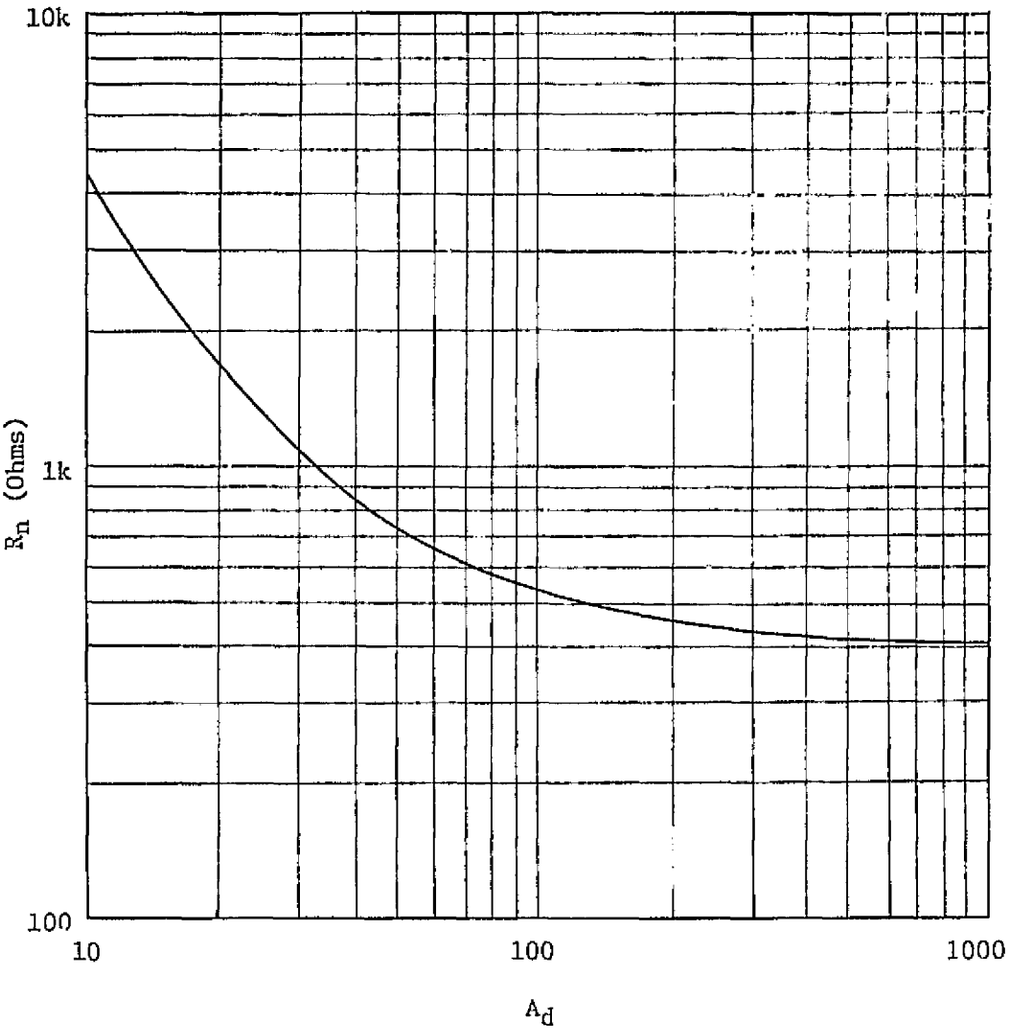

Figure 4-3. Equivalent Noise Resistance as a Function of Gain for Circuit of Figure 3-10 (p. 47).

CHAPTER V

COMMON MODE ANALYSIS OF NEW INSTRUMENTATION AMPLIFIER

Introduction

The basic sources of common mode error are discussed and a simple method for reducing the effect of these errors is presented. A technique for trimming the circuit to minimize common mode gain is proposed.

Basic Error Sources

The sources of common mode error in a differential amplifier were discussed in Chapter III (pp. 35,48). A composite input circuit was proposed to reduce these sources of error mainly by increasing the effective transconductance. Using the Equations of Chapter III and the parameters of the composite device listed in Equations (3-11) through (3-14) (p. 41), the common mode rejection should be very high, about 150 dB for low frequencies. However, the analysis of Chapter III did not include error effects inside the composite device. Including these effects, the primary source of common mode error becomes the non-infinite drain-source resistance of the input transistor.

There are three effects on common mode rejection. Common mode input signals generate an error current in each side of the input stage,

$$I_{error} = \frac{V_{cm}}{r_{ds_1}} . \qquad (5\text{-}1)$$

The degree of match between these two error currents and their magnitude govern the common mode rejection as follows:

$$CMR_1 = \left(\frac{r_{ds1}}{\Delta r_{ds1}}\right) r_{ds1}\, gm_1, \tag{5-2}$$

$$CMR_2 = \left(\frac{gm_1}{\Delta gm_1}\right)_1 r_{ds1}\, gm_1, \tag{5-3}$$

and

$$CMR_3 = \left(\frac{R_d}{\Delta R_d}\right) 2r_{ds1}\, gm_1. \tag{5-4}$$

The effect due to mis-matches in R_d is not a direct effect. A mis-match in R_d will cause mis-matches in the transistor bias current causing differences in transconductance.

$$\left(\frac{\Delta gm_1}{gm_1}\right)' = \frac{1}{2}\left(\frac{\Delta R_d}{R_d}\right). \tag{5-5}$$

The prime on the first term in Equation (5-5) is to distinguish it from the transconductance error at equal bias currents. This effect could be used to advantage in that an error in transconductance could be compensated by a negative error imposed by an appropriate trimming of R_d.

Since all the common mode factors are proportional to r_{ds1}, the most effective method of increasing common mode rejection would be to increase R_{ds1}. A cascode circuit has been proposed [14] to accomplish an improvement in CMRR. This same technique can be used with the composite device as illustrated by Figure 5-1, where Q_1 of Figure 3-10 (p. 47) has been replaced by two FET's.

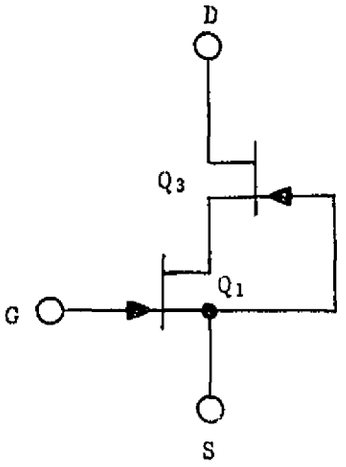

Figure 5-1. Cascode Input Transistor.

The output resistance of this cascode circuit is approximately

$$r_{o1} = (r_{ds3}\ g_{m3})\ \ r_{ds1}. \tag{5-6}$$

The common mode factor equations then become

$$CMR_1 = \left(\frac{r_{o1}}{\Delta r_{o1}}\right)\ g_{m1}\ r_{o1}, \tag{5-7}$$

$$CMR_2 = \left(\frac{g_{m1}}{\Delta g_{m1}}\right)\ g_{m1}\ r_{o1}, \tag{5-8}$$

and

$$CMR_3 = \left(\frac{R_d}{\Delta R_d}\right)\ 2g_{m1}\ r_{o1}. \tag{5-9}$$

An exact analysis reveals three other sources of error that become important at higher frequencies where the op-amp gain decreases.

$$CMR_4 = \left(\frac{gm_1}{\Delta gm_1}\right) \quad 2gm_1 \; R_d \; A_1 . \tag{5-10}$$

$$CMR_5 = \left(\frac{A_1}{\Delta A_1}\right) \quad \frac{2}{R_g} \; R_d \; A_1 . \tag{5-11}$$

$$CMR_6 = \left(\frac{R_d}{\Delta R_d}\right) \quad \frac{2}{R_g} \; R_d \; A_1 . \tag{5-12}$$

Notice that CMR_5 and CMR_6 depend on R_g and therefore vary with gain. These equations can be combined with Equations (5-7) through (5-9) to form four common mode factor equations that describe the dominant sources of common mode error. These are

$$CMR_1 = \left(\frac{r_{o1}}{\Delta r_{o1}}\right) \quad gm_1 \; r_{o1}, \tag{5-13}$$

$$CMR_2 = \left(\frac{gm_1}{\Delta gm_1}\right) \quad (gm_1 \; r_{o1} + 2gm_1 \; R_d \; A_1), \tag{5-14}$$

$$CMR_3 = \left(\frac{R_d}{\Delta R_d}\right) \quad \left(2gm_1 \; r_{o1} + \frac{2}{R_g} \; R_d \; A_1\right), \tag{5-15}$$

and

$$CMR_4 = \left(\frac{A_1}{\Delta A_1}\right) \quad \left(\frac{2}{R_g} \; R_d \; A_1\right) . \tag{5-16}$$

The complete circuit diagram for the new instrumentation amplifier now appears in Figure 5-2 with component values given for optimum noise and CMRR performance. The common mode rejection ratio predicted by Equations (5-13) through (5-16) is plotted in Figure 5-3 versus frequency. The op-amp A_1 is assumed to have a gain bandwidth product of 3 MHz, Q_1 and Q_3 are assumed to be 2N5565 transistor pairs biased at a drain current of 3 mA. All component matching is assumed to be 5%.

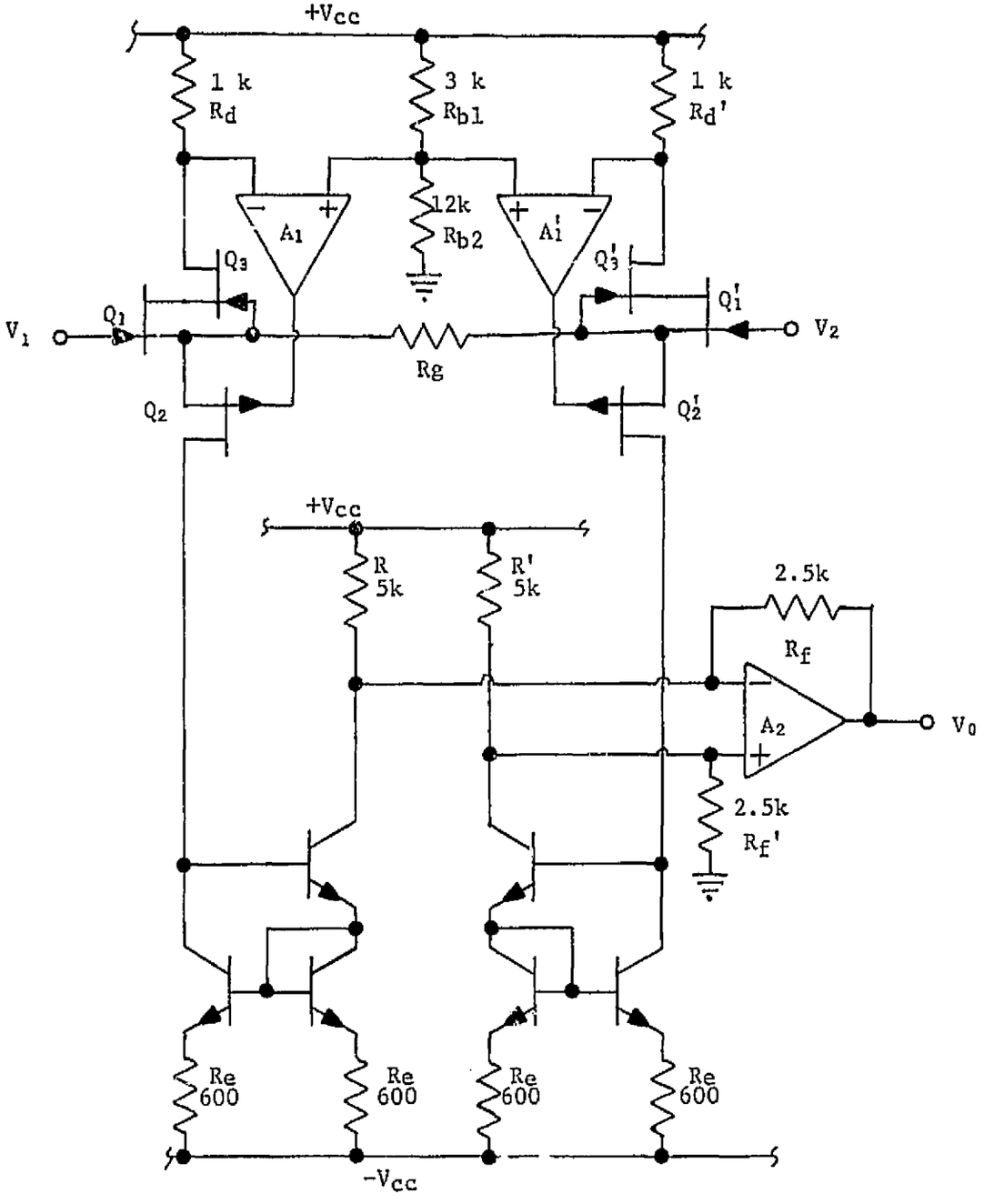

Figure 5-2. New Instrumentation Amplifier with Component Values Indicated.

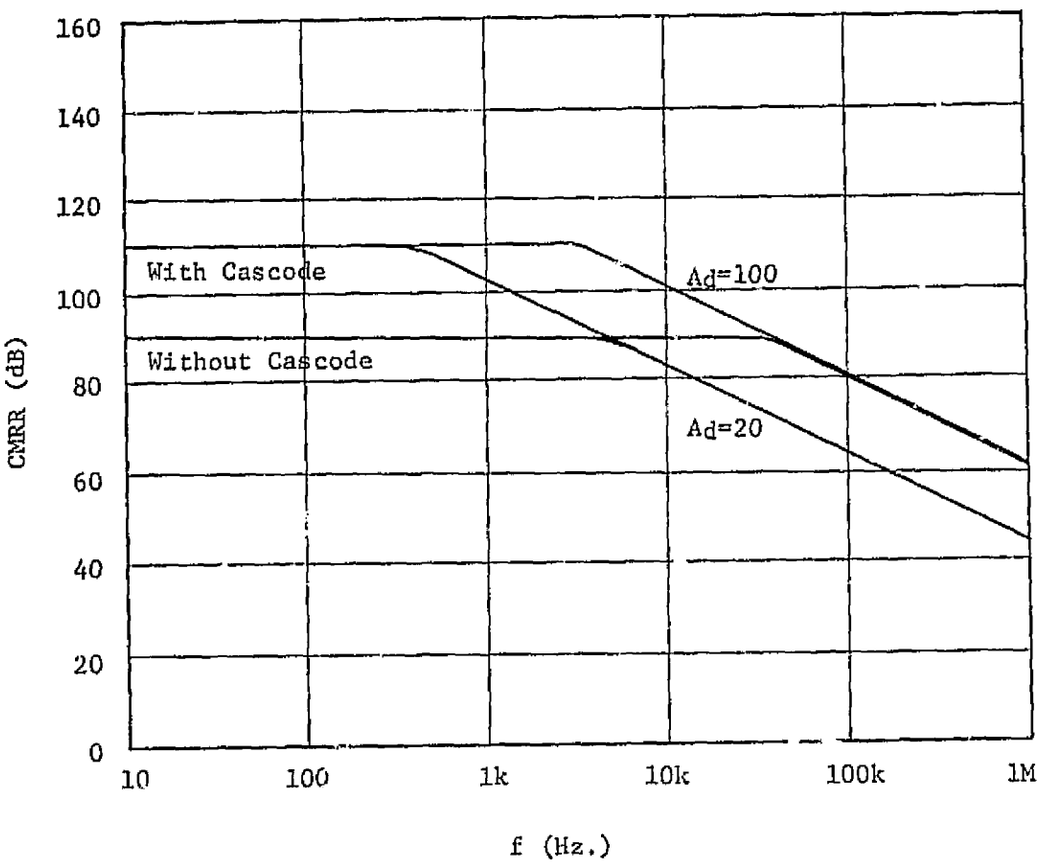

Figure 5-3. Predicted Common Mode Rejection Versus Frequency for the Circuit of Figure 5-2.

A Problem With The Cascode Circuit

It should be pointed out that the input transistor operates at a drain-source voltage equal to the source-gate voltage of the cascode transistor. Obviously the circuit cannot be operated at currents approaching the I_{dss} of the cascode transistor.

The cascode circuit adds a noise source equal to

$$R_{nc} = \left(\frac{1}{r_{ds1}\ g_{m3} + 1}\right) \frac{2}{3} \frac{1}{g_{m3}}. \qquad (5\text{-}19)$$

The factor in parenthesis is very small if Q_1 is biased at sufficient voltage to keep r_{ds1} high. This requires a voltage of at least 2 volts. The pinch-off voltage V_p of the cascode transistor must then be greater than two volts; in fact, the cascode transistor must be specified such that

$$\left(1 - \frac{\sqrt{I_d}}{I_{dss}}\right) V_p \geq 2V \qquad (5\text{-}20)$$

to insure that the noise and CMRR are not limited by biasing Q_1 in the triode region.

In the circuit of Figure 5-2 it is assumed that A_2 does not limit the bandwidth or compromise the noise. Typically, an LM-118 op-amp or equivalent would be used for A_2.

CHAPTER VI

EXPERIMENTAL RESULTS

Introduction

Results of experimental tests on the instrumentation amplifier of Figure 5-2 (p.61) are presented in comparison with predicted results. The limitations on further improvements are pointed out.

The Circuit

A dual monolithic FET pair 2N5565 was chosen as the input and cascode transistors. The transconductance of two devices was measured and found to be approximately

$$gm_1 \simeq 0.18 \sqrt{I_d}. \tag{6-1}$$

The noise for each FET above 1000 Hz was also measured to be approximately

$$R_{n1} \simeq \frac{2}{3} \frac{2.0}{gm_1} \tag{6-2}$$

for $T_j = T_a$. The cascode transistor was found to add very little noise to the circuit and did not decrease gm_1.

The op-amps A_1 and A_1' were quad monolithic RC-4136 amplifiers. The noise of these devices was measured at 10 nv/$\sqrt{Hz}$ above 1 KHz, and gain bandwidth product was 3.2 MHz. Transistors Q_2 and Q_2' were unmatched 2N5462 P channel FETS. The current mirrors were CA3183 NPN transistor arrays, with betas measured to be approximately 90.

The output op-amp was a TP-1322 high speed amplifier. All

resistors were 1% metal film. The circuit was biased to allow ± 12 V common mode swing, and the drain current was 3 mA.

Amplifier Noise

Figure 6-1 indicates the measured amplifier input noise above 1KHz versus gain along with that predicted by the Equations in Chapter IV. Figure 6-2 shows the measured input noise spectral density as a function of frequency for gain of 20 and 100.

Common Mode Rejection

The common mode rejection ratio was measured for three cases,

1. without cascode transistors,
2. with cascode transistors, and
3. R_d trimmed for maximum CMR.

Figure 6-3 is a plot of measured and and calculated CMRR for all three cases at a gain of 100. The CMRR is proportional to gain above the 3dB breakpoint; that is, if the gain is reduced 10 dB the CMRR will be reduced 10 dB. Gain does not affect CMRR below the 3 dB break point.

Other Characteristics

The gain of the amplifier was found to be within ± 0.5% of the predicted gain of

$$A_d = \frac{2R_f}{R_g} . \qquad (6-3)$$

The gain had a usable range from 0.1 to 1000 by changing R_g. Gain nonlinearity was estimated to be less than 0.5%. Output dynamic range was measured to be

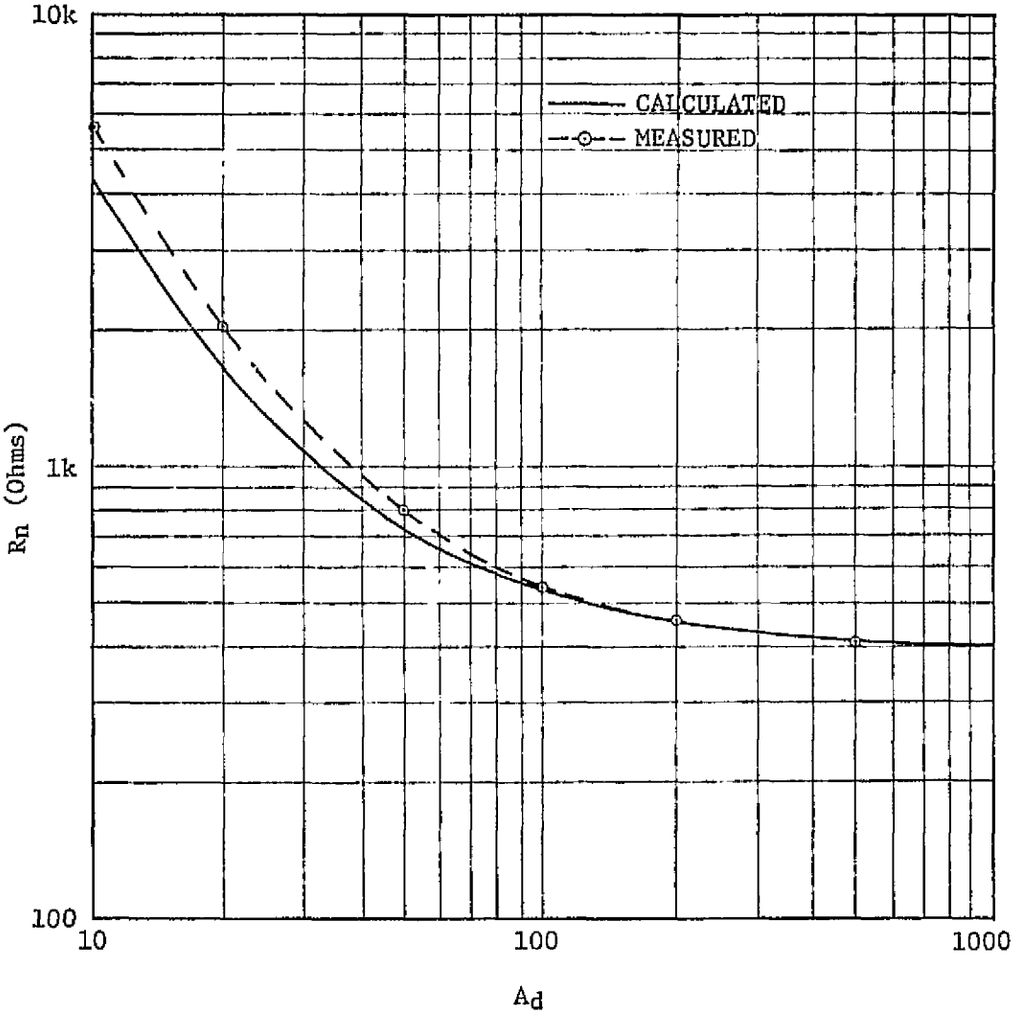

Figure 6-1. Amplifier Noise Resistance Versus Gain for Frequencies Above 1000 Hz.

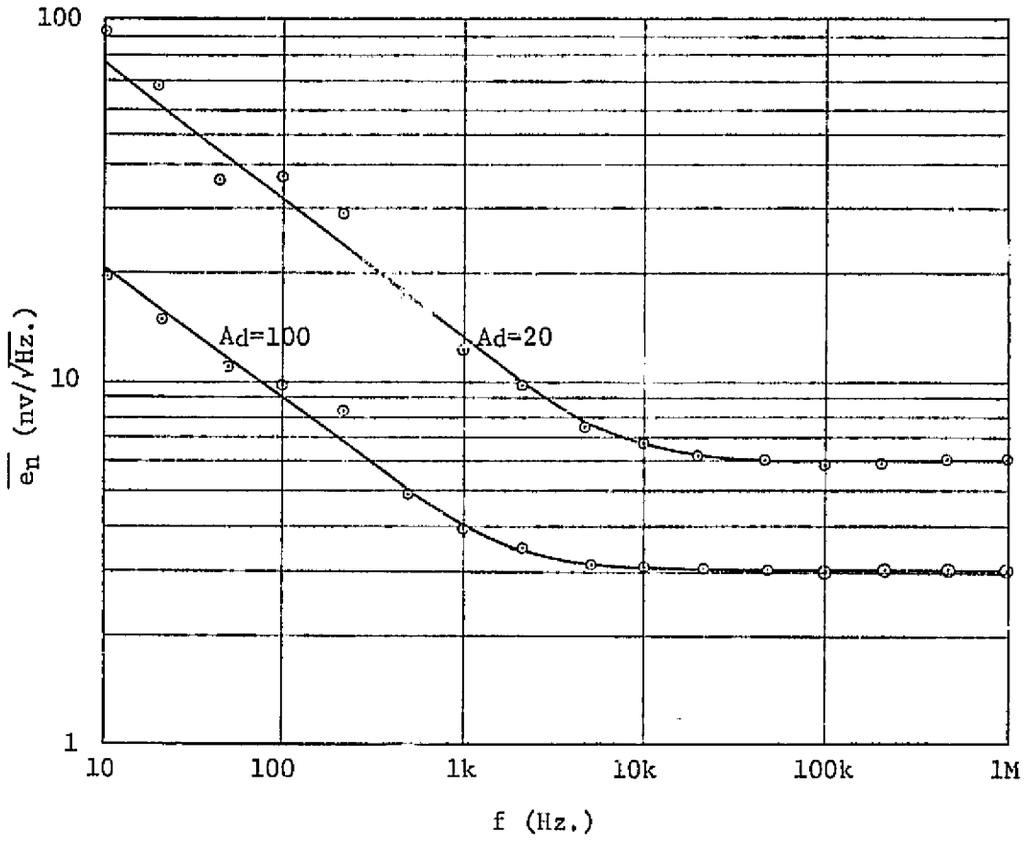

Figure 6-2. Amplifier Noise Spectral Density.

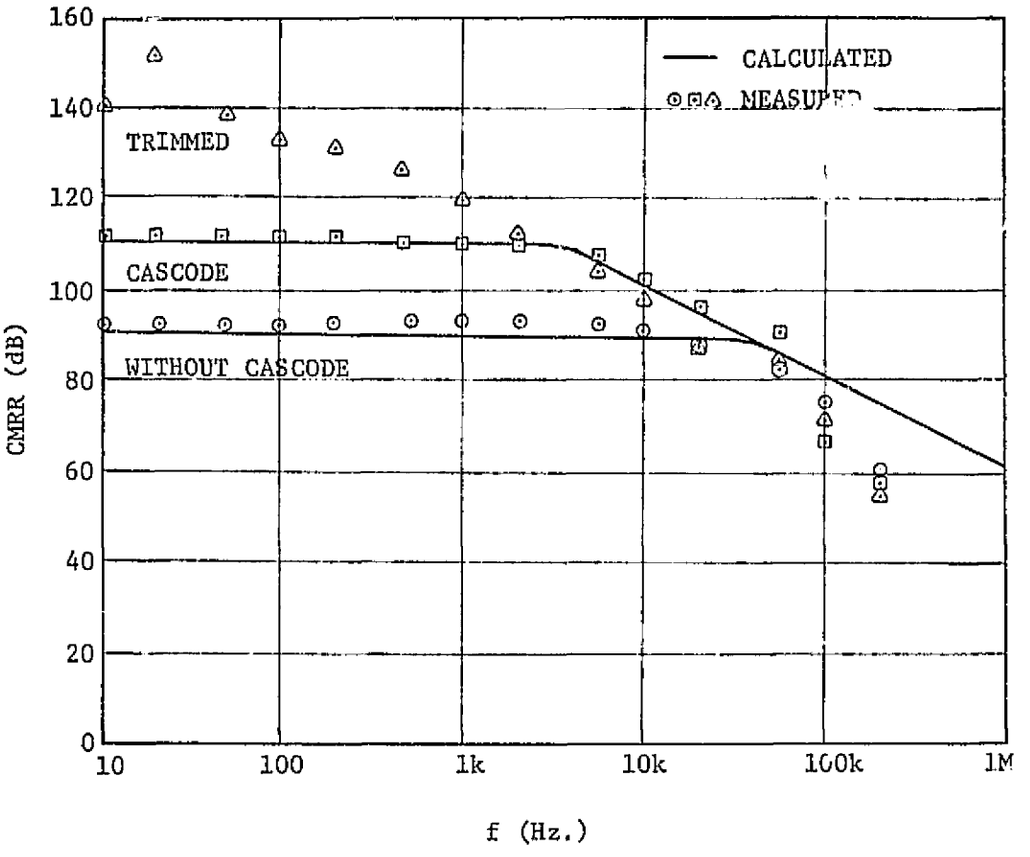

Figure 6-3. Amplifier Common Mode Rejection Versus Frequency.

$$-12V \leq V_o \leq 13V \ . \tag{6-4}$$

The small signal rise time was measured as

$$\tau_{rs} = 110 \text{ ns}, \tag{6-5}$$

giving

$$BW_s = 3.18 \text{ MHz},$$

for an overshoot of 30%. The small signal bandwidth was therefore limited only by the gain bandwidth product of A_1 and A_1'. For an output square wave going from -10 volts to +10 volts the large signal rise time was measured to be

$$\tau_{rs} \leq 6 \ \mu s \ . \tag{6-6}$$

The input offset voltage was measured to be

$$V_{os} = 17 \text{ mv} \tag{6-7}$$

and was primarily due to input transistor matching. The temperature dependent drift should also be dominated by input transistor drift.

CHAPTER VII

DISCUSSION AND CONCLUSIONS

Analytical studies presented in previous chapters demonstrated the inability of commonly used instrumentation amplifier circuits to give high common mode rejection, low noise and low distortion simultaneously. The limitations were outlined, and methods were demonstrated to improve both noise and common mode performance. A new amplifier was developed and evaluated. The tests indicate that the analysis presented accurately described the physical phenomena.

As a result of this study the new amplifier of Figure 5-2 (p. 61) has lower noise and higher CMRR than any instrumentation amplifier now commercially available. This amplifier does, however, lack the convenience of the monolithic instrumentation amplifiers such as the Analog Devices AD-521. The usefullness of the amplifier could be improved if a hybrid version were built allowing a smaller size and better temperature tracking of resistors. Table VII-1 is a comparison of the new amplifier with a few quality instrumentation amplifiers currently available. The noise is 10 Hz to 10 KHz input referred, and CMRR is at 60 Hz. Differential gain is 100 V/V.

The speed and noise performance of the new amplifier could be improved if low noise high speed discrete transistor circuits were substituted for the op-amps. This would further complicate the circuit, however, making the component matching problem more difficult. An ultimate performance instrumentation amplifier could be built using the general ideas of this study if several very carefully matched

TABLE VII-1

Comparison of New Instrumentation Amplifier
With Commercially Available Units
for Gain of 100

Manufacturer	Model	CMRR (dB) @ 60 Hz	$\overline{e_n}$ (μV) 10Hz - 10KHz
New Amplifier	1	135	0.30
Analog Devices [15]	AD520K	110	2.92
Analog Devices [16]	AD521K	114	1.24
Burr Brown [17]	3670K	94	3.30
Burr Brown [18]	3660K	100	2.30
Analog Devices [19]	606M	100	1.70

high transconductance FET's were paralleled to form the input devices, discrete circuits were used for the op-amps, and all circuit resistors were trimmed to minimize the common mode gain.

An amplifier could possibly be built having as low as 20 Ω noise resistance and as high as 100 dB common mode rejection at 10 KHz.

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APPENDIXES

APPENDIX A

BASIC NOISE ANALYSIS OF ACTIVE DEVICES

It will be the purpose of this analysis to find the equivalent output noise of an active device and its associated components. Most all active devices can be represented by the model in Figure A-1. Here conductances are used instead of impedances to simplify the analysis.

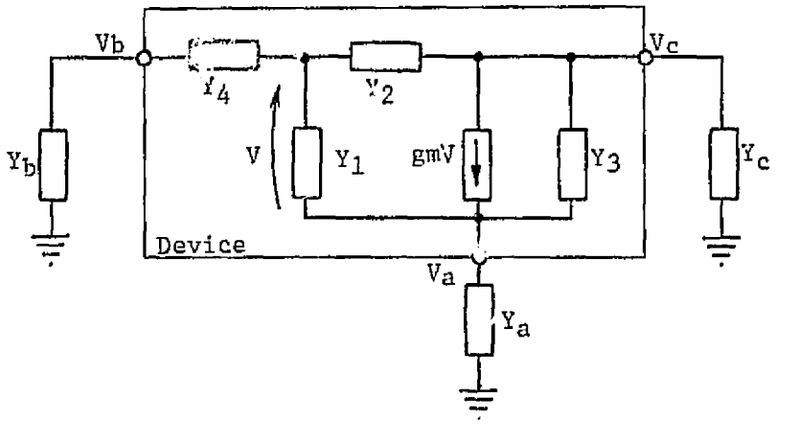

Figure A-1. Active Device Model With Associated Circuitry.

Y_a, Y_b and Y_c are representative of the associated input and output circuitry. The analysis can be simplified without loss in exactness if Y_4 is lumped into Y_b giving the model in Figure A-2. Any noise sources in the device can be simulated by an appropriate combination of the noise current sources i_a, i_b, and i_c.

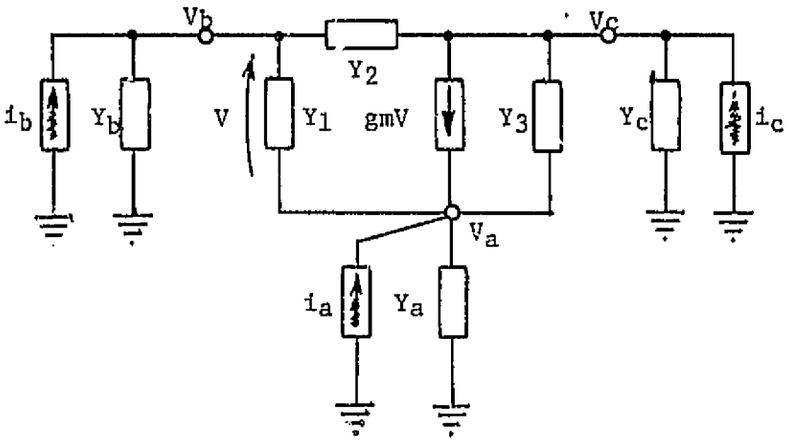

Figure A-2. Simplified Active Device Model With Noise Sources.

Given the model in Figure A-2 the node equations are

$$V_b(Y_b + Y_1 + Y_2) - V_a(Y_1) - V_c(Y_2) = i_b,$$

$$-V_b(Y_1 + gm) + V_a(gm + Y_a + Y_1 + Y_3) - V_c(Y_3) = i_a,$$

and (A-1)

$$-V_b(Y_2 - gm) - V_a(Y_3 + gm) + V_c(Y_c + Y_2 + Y_3) = i_c.$$

To solve for the Norton equiv lent noise at the output node C (collector of Bipolar transistor or drain of an FET), as shown in Figure A-3 the output admittance Y_{oc} and Norton current source must be found. Y_{oc} can be found from Equation (A-1) by letting

$$Y_c = 0$$

$$i_a = 0$$

$$i_b = 0$$

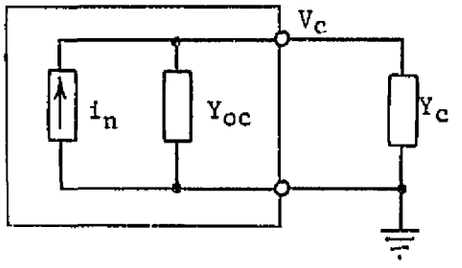

Figure A-3. Norton Equivalent Noise Model at Node C.

and solving for $i_c/V_c = Y_{oc}$. Making these substitutions and solving by Cramers rule, Equation (A-2) is obtained.

$$Y_{oc} = \frac{Y_bY_2gm + Y_bY_aY_2 + Y_bY_aY_3 + Y_bY_1Y_2 + Y_bY_1Y_3 + Y_bY_3Y_2}{Y_bgm + Y_bY_a + Y_bY_1 + Y_bY_3 + Y_1Y_a + Y_1Y_3} \quad \text{(A-2)}$$

$$\frac{+ Y_1Y_2Y_a + Y_1Y_2Y_a + Y_2Y_3Y_a + 2Y_1Y_2Y_3 + Y_2Y_agm}{+ Y_2gm + Y_2Y_a + Y_1Y_2 + Y_2Y_3}$$

The collector shot noise of a bipolar transistor or the drain channel noise of an FET appears in the model as a noise current source i_1 in the model of Figure A-4. This model can be made to fit the general node equation if

$$i_b = 0,$$

$$i_a = -i_1, \text{ and}$$

$$i_c = +i_1.$$

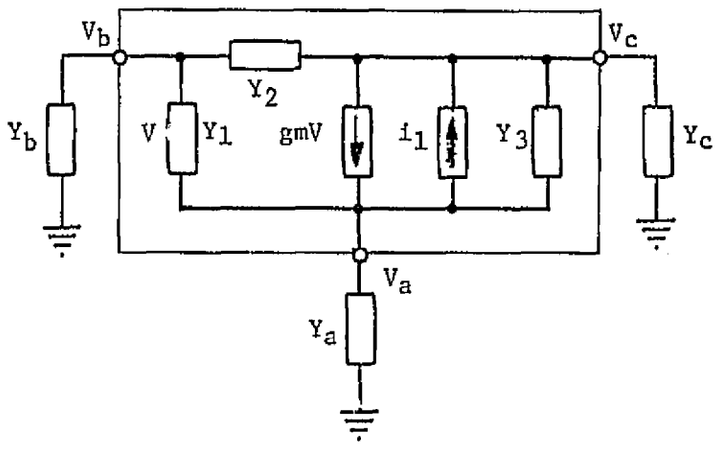

Figure A-4. Active Device Model With One Noise Source.

The Norton equivalent output current source can be found by finding the short circuit output current or the open circuit output voltage times the output admittance. The latter is easier to find using the node equation. Making the above substitution the Norton equivalent output current is given by Equation (A-3).

$$i_n = \frac{(Y_bY_a + Y_bY_1 + Y_1Y_a + Y_2Y_a)}{(Y_bY_a + Y_bY_1 + Y_1Y_a + Y_2Y_a)} \cdots \frac{i_1}{+ Y_bY_3 + Y_1Y_3 + Y_2gm + Y_1Y_2 + Y_2Y_3} \qquad \text{(A-3)}$$

For low frequencies the model admittances can be approximated as in Table A-1. Making these substitutions into Equation (A-3) for the bipolar transistor gives

TABLE A-1

Low Frequency Equivalents to Model Admittances

Admittance	Bipolar	FET
Y_1	$\frac{1}{r_b'_e} = \frac{1}{(\beta + 1)V_e}$	$\frac{1}{r_{gs}}$.
Y_2	0	0
Y_3	$1/r_{ce}$	$1/r_{ds}$
Y_b	$\frac{1}{R_b + r_b}$	$\frac{1}{R_g}$
Y_a	$\frac{1}{R_e}$	$\frac{1}{R_s}$
Y_c	$\frac{1}{R_c}$	$\frac{1}{R_d}$
gm	$\frac{\beta}{r_b'_e} = \frac{1}{r_e} \frac{\beta}{(\beta + 1)}$	gm

$$i_{n_1}\Big|_{\text{lowf}} = \frac{\left[(\beta + 1)\ \frac{r_e}{R_e} + \frac{R_b}{R_e} + 1\right]\ i_1}{(\beta + 1)\left(\frac{r_e}{r_{ce}} + \frac{r_e}{R_e}\right) + 1 + \frac{R_b}{r_{ce}} + \frac{R_b}{R_e}} \qquad \text{(A-4)}$$

assuming

$$\beta >> 1,$$

$$r_{ce} >> r_e,$$

$$\beta r_{ce} >> R_g,$$

and

$$i_1 = i_c.$$

Equation (A-4) reduces to

$$\frac{i_{nc}}{i_c}\Big|_{\text{lowf}} \simeq \frac{\beta r_e + R_e + R_b}{\beta(R_e + r_e) + R_b}\ . \qquad \text{(A-5)}$$

In the common base configuration

$$R_b \simeq 0$$

$$R_e >> \beta r_e.$$

Then

$$\frac{i_{nc}}{i_c}\Big|_{\substack{\text{lowf}\\ \text{CB}}} = \frac{1}{\beta}\ . \qquad \text{(A-6)}$$

In the common emitter configuration

$$R_e = 0,$$

then

$$\frac{i_{nc}}{i_c}\Big|_{\substack{\text{lowf}\\ \text{CE}}} = 1. \qquad \text{(A-7)}$$

For the differential amplifier case

$$R_e = r_e + R_b/\beta.$$

Then

$$\left.\frac{i_{nc}}{i_c}\right|_{\substack{\text{lowf}\\ \text{diff}}} = \frac{1}{2} . \qquad \text{(A-8)}$$

Making the appropriate substitution into Equation (A-3) for the low frequency FET MODEL gives, with $i_1 \simeq i_d$,

$$\left.\frac{i_{nd}}{i_d}\right|_{\text{lowf}} \simeq \frac{\frac{1}{R_g R_s} + \frac{1}{R_g r_{gs}} + \frac{1}{r_{gs} R_s}}{\frac{1}{R_g R_s} + \frac{1}{R_g r_{gs}} + \frac{1}{r_{gs} R_s} + \frac{gm}{R_g} + \frac{1}{r_{gs} r_{ds}} + \frac{1}{R_g r_{ds}}} . \qquad \text{(A-9)}$$

If $r_{gs} >> R_g$,

and $r_{gs} >> R_s$

then Equation (A-9) reduces to

$$\left.\frac{i_{nd}}{i_d}\right|_{\text{lowf}} \simeq \frac{1}{1 + gm\, R_s + \frac{R_s}{rd_s}} \qquad \text{(A-10)}$$

For the common gate case:

$$R_s \simeq rd_s$$

$$R_s >> \frac{1}{gm}$$

$$\left.\frac{i_{nd}}{i_d}\right|_{\substack{\text{lowf}\\ \text{CG}}} \simeq \frac{1}{gm\, R_s} . \qquad \text{(A-11)}$$

For the common source case:

$$R_S \approx 0 ,$$

$$\left.\frac{i_{nd}}{i_d}\right|_{\substack{\text{lowf}\\ \text{CS}}} \approx 1. \qquad \text{(A-12)}$$

For the differential amplifier

$$R_S = \frac{1}{gm} ,$$

$$R_S << r_{ds} ,$$

$$\left.\frac{i_{nd}}{i_d}\right|_{\substack{\text{lowf}\\ \text{diff}}} = \frac{1}{2} . \qquad \text{(A-13)}$$

APPENDIX B

PARAMETERS OF OP-AMPS AND FET'S

The following is a partial listing of specifications on the RG4136 quad op-amp [20]:

1. Gain-bandwidth product - 3 MHz.
2. DC gain - 300,000 V/V.
3. Input noise voltage above 1000 Hz - 10 nv/$\sqrt{\text{Hz}}$.
4. Input noise current above 1000 Hz - 0.5 pA/$\sqrt{\text{Hz}}$.

The following is a partial listing of the specifications of the dual N-channel FET number 2N5565 for V_{ds} = 15 V, and I_d = 2 mA [21].

1. gm_{ss} - 18 mmhos
2. I_{dss} - 15 mA.
3. V_p - 1.8 V
4. Output resistance - 66 kΩ.
5. Gate current - 15 pA.
6. Input noise voltage - 4.5 nv/$\sqrt{\text{Hz}}$.
7. Drift in V_{gs} - 9 μv/°C.
8. V_{gs} mis-match - 8 mv.

APPENDIX C

COMMON MODE REJECTION AND NOISE MEASUREMENT

An experimental apparatus was used to measure common mode gain and noise as in Figure C-1.

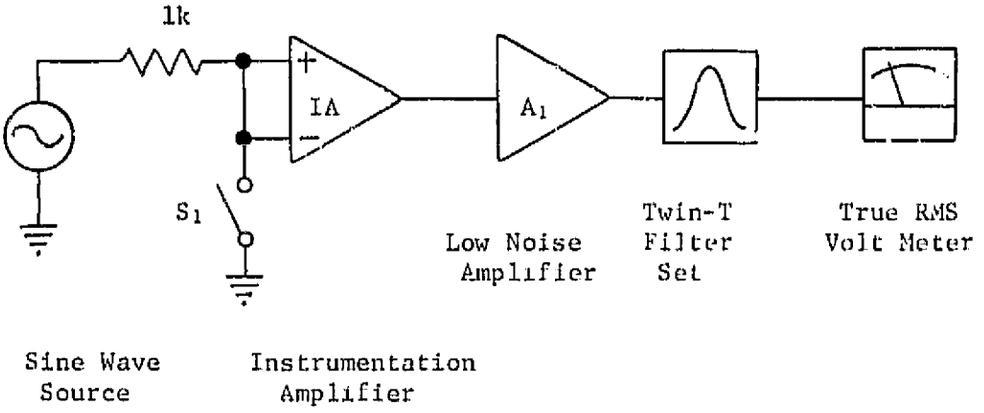

Figure C-1. Apparatus for Measuring Common Mode Gain and Noise.

The switch S_1 was used to switch from the common mode gain to noise measurement. The amplifier A_1 had an equivalent noise resistance of 10 Ω and a gain of 240. The twin-T filter set had a Q of about 10, a gain at midband of 40, and a calibrated noise bandwidth.

To obtain CMRR the ratio of differential gain to common mode gain at a particular frequency is taken.

To measure noise S_1 is closed to short both inputs of the amplifier under test to ground. To obtain the equivalent input noise voltage the meter reading was divided by the filter gain, the square-

root of filter bandwidth, the A_1 amplifier gain and the differential gain of the amplifier under test.

VITA

Kenneth Rush was born in [redacted] in [redacted], went to grade school in Decherd, Tennessee, and graduated from Franklin County High School in 1968. He attended The University of Tennessee and graduated with a B.S. in Aerospace Engineering in 1973. He worked with NASA Goddard Spaceflight Center on the Cooperative Engineering Scholarship Program from 1969 to 1972. He worked for the Mechanical and Aerospace Engineering Department of The University of Tennessee in 1973 and for the Electrical Engineering Department of The University of Tennessee in 1973 and 1974. He is currently employed by Union Carbide at the Oak Ridge National Laboratory. His wife is the former Mary E. [redacted] of Maryville, Tennessee.