DESIGN, PROCESSING, AND TESTING OF LSI ARRAYS FOR SPACE STATION

BY

A. C. IPRI

QUARTERLY TECHNICAL REPORT NO. 18

NOVEMBER 1975

PREPARED UNDER CONTRACT NO. NAS12-2207 BY
RCA LABORATORIES
PRINCETON, NEW JERSEY 08540

GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
HUNTSVILLE, ALABAMA 35812

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.

4. Title and Subtitle	5. Report Date
DESIGN, PROCESSING, AND TESTING OF LSI ARRAYS FOR SPACE STATION	November 1975
	6. Performing Organization Code
7. Author(s) A. C. Ipri	8. Performing Organization Report No. PRRL-75-CR-62
9. Performing Organization Name and Address RCA Laboratories Princeton, NJ 08540	10. Work Unit No.
	11. Contract or Grant No. NAS12-2207
12. Sponsoring Agency Name and Address George C. Marshall Space Flight Center National Aeronautics & Space Administration Huntsville, AL 35812	13. Type of Report and Period Covered Quarterly Technical Report No. 18 (7/1/75 to 9/30/75
	14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

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17. Key Words (Selected by Author(s))	18. Distribution Statement
Random access memory (RAM) Silicon-g e fabrication Integrated-circuit technology Reliability	

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
Unclassified	Unclassified	12	

*For sale by the Clearinghouse for Federal Scientific and Technical Information, Springfield, Virginia 22151.

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A. C. Ipri
RCA Laboratories
Princeton, New Jersey 08540

SUMMARY

This research program is being concetrated on an investigation of the Si-gate CMOS/SOS process used to manufacture integrated circuits. Despite traditional test vehicles being used in industry, several failure mechanisms that determine the final yield of a large array, often called "random defects," are statistical in nature, and must be found by a laborious inspection procedure that is frequently time-consuming and inaccurate. The objective of this study is to isolate those defect mechanisms which are most detrimental to yield, control, and reliability. By using a process analysis test structure it will be possible to determine and isolate the dominant failure mechanisms, obtain accurate in-process control, make process line comparison, and obtain reliable yield predictions.

I. INTRODUCTION

This program involves the study of the silicon-gate CMOS/SOS process used to manufacture integrated circuits. RCA currently has three such lines in operation. One of these lines is located in the Integrated Technology Center of RCA Laboratories in Princeton, NJ; the other two lines are located at an RCA facility in Somerville, NJ. One of these two lines is used to manufacture custom products for military applications as well as for RCA applications. The other line is part of the RCA Solid State Division which is responsible for the production of commercial silicon-on-sapphire circuits.

All three lines use a common base of technology to produce their circuits, although there are readily apparent differences in the details of the overall process that each uses. Some of these differences relate to the particular capabilities of the individual organizations. For example, the Solid State Division does not produce its own epitaxial wafers; rather, it obtains them from outside commercial sources. Even within a given process line there exist a variety of processes to achieve high and low threshold devices, for example. This diversity of processing techniques occurs, in part, because SOS/MOS is still an emerging technology and, in part, because trade-offs in the type of processing must be made when custom circuitry is produced or when the same technological base is used for a wide variety of applications.

The traditional type of test vehicle, which incorporates such items as MOS transistors, resistors, and capacitors, is useful in determining those failure mechanisms which generally cause the wafer yield to approach zero. These test structures are usually part of a wafer "knock-out" and, as such, yield no statistical information. In addition, these test devices are measured after the wafers have completed the fabrication sequence and are, therefore, a result of several processing steps.

There are, however, several failure mechanisms which dominate the final yield of a large array and have been characterized under the nebulus term of "Random Defects." These defects are statistical in nature and, hence, cannot be analyzed by a simple knock-out. In addition, each process step generates its own set of defects and, therefore, tests must be performed immediately after each step in order to determine if the number of defects generated by that step is statistically significant. At the present time this usually involves a laborious inspection procedure performed on the actual arrays, which is time-consuming and inaccurate. The problem is further complicated by the processing differences which comprise the fabrication lines at the three RCA locations. In effect, a different processing step or technique would generate a unique type of defect. What is needed therefore is a universal "Process Analysis Structure" which statistically determines the yield degradation of each significant process step and reflects the number of effective defects generated by that step.

II. PROCESS ANALYSIS

Random defects can be generated by any of the various process steps used in the fabrication of integrated circuits. There are, however, certain specific steps of a critical nature, which are used repeatedly and hence can be grouped together. These are:

(1) Thin-film deposition or growth
- Semiconductor layers
- Dielectric layers
- Metal layers

(2) Photoresist techniques

(3) Etching techniques

(4) Doping techniques

Nearly all integrated-circuit process technologies contain these categories. Different specific approaches, however, are used by different companies in each of these categories. Etching, for instance, may be the result of a wet chemical technique in one company while a second company may use a gaseous plasma approach. Ion implantation may be used as the doping source for some, while others use high-temperature gaseous sources. The number of different photoresist techniques is endless. The need to examine these steps to determine the degree to which they have been successfully accomplished is extremely important and returns one to the problem at hand.

In general, a process sequence involves depositing, growing or doping a thin film, defining the film, and etching it. These three sequential steps comprise one block which can be interrogated for defects and, if the number is found to be high, the film can be stripped and the steps repeated. Analyzing the CMOS/SOS silicon-gate process one finds that the first sequence of steps is the deposition and patterning of the thin silicon film. The process analysis structure must, therefore, be able to check for:

(1) Silicon island discontinuities

(2) Silicon island to silicon island short-circuits

The next step is the oxidation of the islands followed by the deposition of the polycrystalline silicon film. The polysilicon layer is then patterned and, hence, the test structure must examine for:

(3) Polycrystalline silicon discontinuities

(4) Polycrystalline-silicon island short-circuits

(5) Polysilicon to polysilicon short-circuits

A layer of silicon dioxide is deposited, and contact holes are etched in the layer to permit the metal interconnect pattern to make electrical contact to the silicon islands and polysilicon gates. A test must be performed, therefore, to determine:

(6) Contact hole open-circuits

The last layer which is deposited and defined is the metal interconnect pattern. The process analysis structure must, therefore, examine for:

(7) Metal discontinuities

(8) Metal to island short-circuits

(9) Metal to polysilicon short-circuits

(10) Metal-to-metal short-circuits

All of these data "must" be compiled on a statistical basis so that, for instance, the "probability" of opening a certain number of contacts can be ascertained.

III. USES OF THE PROCESS ANALYSIS STRUCTURE

A. Process Integrity

Once the number of defects associated with each of the critical parameters listed above has been determined over a significantly large sampling, it is a simple task to pinpoint major failure mechanisms. These mechanisms or defects are those whose number is significantly greater than any of the others and hence clearly points to the weak links in the process. Once these have been isolated, a determined effort can be made to reduce their number.

B. Process Control

Once a base-line has been established to relate the number of effective defects to the particular process step, it would be possible, through the use of a control wafer, to determine the number of defects generated during an actual processing run and compare this number with the base-line. If the number of defects is significantly larger than the base-line, the wafers could be reworked at that particular processing step. If the number is comparable to the base-line, they would continue through to the next processing step. It is necessary to use a control wafer instead of a knock-out because of the statistical nature of defects which are being analyzed.

C. Process Comparison

By fabricating and measuring the process analysis structure in different processing lines it would be possible to determine both the weak points and the strong points associated with each location. A comparison of etching techniques, for instance, may reveal that one technique is significantly better than any of the other approaches in minimizing metal open-circuits over steps.

In addition to being used to compare results of process lines at different locations, the structure would also be helpful in comparing various types of commercial equipment or novel processing techniques. For example, the use of plasma-etching in place of wet chemical etching may impact several processing parameters such as edge profile, and hence step coverage or oxide integrity and related polysilicon-to-metal short-circuits. Techniques for depositing various materials such as Si, SiO_2, SiO_2, Si_3N_4, and Al must be evaluated for their impact on the defect density of the particular process step. The usual evaluation technique of fabricating an array in a process sequence, which contains the new equipment, is insufficient for a proper evaluation because a significant reduction in the number of defects at one particular step will have only a slight effect on the overall yield of the array. This slight increase or decrease in yield could easily be "swamped out" by the randomness of the other defects generated in the process.

D. Yield Prediction

Given the number of defects generated by each processing step, it is also possible to "predict" the yield of any arbitrary array fabricated using the particular process and design rules as a function of array complexity. It should be pointed out that the number of effective defects is related to the particular design rules used. This results because defect is distributed in "size" and hence its effect is related to the physical dimensions of the particular process step. A 1-μm metal defect, for instance, will have no effect on 10-μm metal lines which are spaced 10 μm apart.

IV. CONCLUSIONS

An analysis has been made of the CMOS/SOS silicon-gate process; the objective of this study has been to isolate those defect mechanisms which, it was felt, had the the greatest impact on yield, control, and reliability of CMOS/SOS integrated circuits. By using a process analysis test structure which measures the probability of having performed basic operations satisfactorily, it will be possible to study each of these defect mechanisms and their respective process step or steps in an attempt achieve several goals. These goals include the isolation and elimination of dominant failure mechanisms, in-process control, process and equipment comparisons, and yield prediction.

Work during the second quarter will involve the layout of the Process Analysis Structure (PAS), which will be used to study the importance of each of the defect mechanisms described previously.