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SATELLITE ON-BOARD PROCESSING FOR EARTH RESOURCES DATA

SUMMARY REPORT

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

AMES RESEARCH CENTER

MOFFETT FIELD, CALIFORNIA

PREPARED BY

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1 STUDY OBJECTIVES

Most of the past effort in the field of earth resources data processing has been research oriented. Earth resources imagery has been provided by NASA to a number of researchers who have processed the data in various ways in order to determine what, if any, useful information could be extracted from the given images. These experiments have demonstrated that useful information can indeed be extracted from aircraft and satellite multispectral scanner imagery of the earth's surface. Economic studies have indicated potential cost-effective systems based on these techniques. Consequently, it is anticipated that during the 1980-1990 decade earth resources satellites will be designed and flown for specific purposes, i.e., to monitor severe weather systems, to monitor water pollution, and to survey and monitor world food production. In these applications it may be more cost effective to process the data on-board the satellite and transmit the data products directly to the users rather than transmit the raw data to a ground processing station for generating the data products and then distributing the data products to the users via another satellite system.

The purpose of this study was to investigate the feasibility of an on-board earth resources data processor launched during the 1980-1990 time frame.

2 STUDY PLAN

In order to determine the feasibility of on-board processing it is first necessary to define the on-board processor in detail. This requires that we define both the technology available for use in the design and the computational requirements of the processor. The computational requirements depend on the algorithms that the processor must implement, which, in turn, depend on the data products that must be extracted from the data to satisfy the users. Consequently, in order to determine the feasibility of on-board data processors it is necessary to start with a study of projected user applications to define the data formats (data throughput rate, number of spectral bands, etc.) and the information extraction algorithms that the processor must execute. Based on these constraints, and the constraints imposed by the available technology, on-board processor systems can be postulated and their feasibility evaluated. The study plan followed in this investigation is summarized in Figure 2(1).

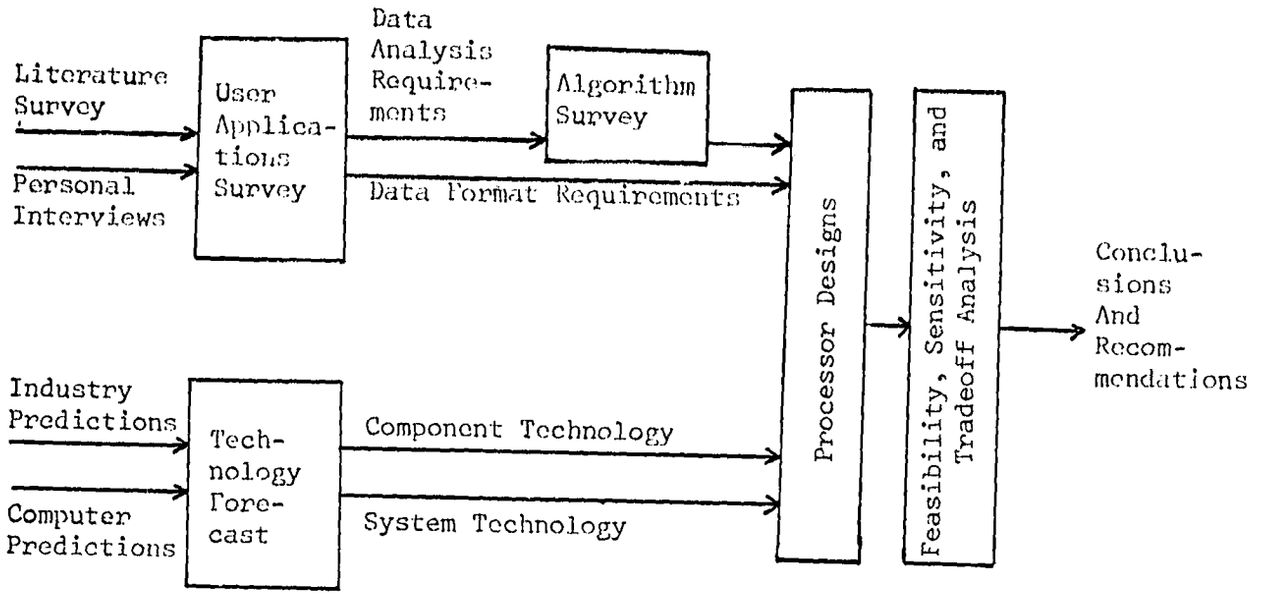

Figure 2(1) Study Plan

3 PRINCIPAL RESULTS OF THE STUDY

The significant results of this study may be subdivided into the following categories.

User Applications Survey

From a comprehensive review of the literature and personal interviews with researchers at a number of government and university laboratories, eight principal classes of earth resources data users were established. These classes are listed in Table 3(I), which also includes several specific application areas within each general category. The application areas shown emerged as the most likely candidates to benefit from the results of this study.

The following parameters were determined for each application area: (1) the minimum and the maximum resolution, (2) the minimum and maximum field of coverage, (3) the minimum and maximum number of spectral bands, and finally, based on these, (4) the minimum and maximum data rate out of the multispectral scanner (MSS). These results are tabulated in Table 3(II). The resolutions range from a minimum of 3 m to a maximum of 10 km. The fields of coverage range from 15-800 km. The number of spectral bands ranges from 1-20 and the resulting data rates range from a minimum of 312 bits/sec to 3470 megabits/sec.

Table 3(I) User Application Areas

Agriculture (A)

- A1. Agricultural Census
- A2. Plant Species Identification
- A3. Plant Stress (Due to Insects, Drought, or Moisture)
- A4. Soil Conservation Practices
- A5. Crop Yield Estimates

Coastal Studies (C)

- C1. Mapping of Shorelines
- C2. Mapping of Shoals
- C3. Wetlands Inventory
- C4. Bathymetry Determination
- C5. Bottom Topography Studies
- C6. Mean High/Low Water Line Determination
- C7. Pollution Detection

Forestry (F)

- F1. Forest-Nonforest Delineation
- F2. Forest Typing
- F3. Detection of Forest Fires
- F4. Plant Stress Detection

Geography (G)

- G1. Land-Use Change
- G2. Earth Resources Location
- G3. Delineation of Urban/Rural Areas
- G4. Detailed Urban Structure
- G5. Traditional Map Preparation

Geology (L)

- L1. Structural Geology (Faults, Folds, Lineaments)
- L2. Geomorphology (Landform Classification)
- L3. Lithologic Mapping
- L4. Geologic Hazards
- L5. Landslides
- L6. Volcano Studies

Hydrology (H)

- H1. Delineation of Land-Water Boundaries
- H2. Delineation of Hydrologically-Related Terrain Hectares
- H3. Hydrodynamics, Including Floods, Reservoirs, and Estuaries
- H4. Water Quality Evaluation
- H5. Snow Cover and Run-Off Evaluation

Meteorology (M)

- M1. Cloud Cover Survey
- M2. Prediction and Assessment of Natural Disasters

Table 3(I) User Application Areas (Continued)

Global Oceanography (0)

01. Study of Biological Processes
02. Sea-Ice Surveillance
03. Study of Current Patterns

Since the data requirements for the various users cover such a wide range, a single candidate data format was selected for subsequent study. This candidate data format has a swath width of 185 km, a resolution of 40 m, a satellite ground track velocity of 6500 m/sec, 7 spectral bands, and 6 bits per data word. The resulting data rate from the MSS is 32 megabits/sec. This data rate satisfies all but two of the minimum data rates and about half of the maximum data rates suggested by the users.

Data Analysis Algorithm Survey

Almost all of the data users surveyed indicated that their objectives could be satisfied using spectral signature analysis. Consequently, a detailed survey was made of algorithms for classifying n-dimensional vectors into one of M categories or classes, where n is the number of spectral bands. As a result of this survey it was determined that four algorithms warranted detailed analysis. These are (1) clustering, (2) maximum likelihood, (3) perceptron, and (4) table look-up.

Clustering is an unsupervised data analysis technique used to determine the natural or inherent data classes in a set of observations. Many such algorithms have been studied. Basically, all of these make a scatter plot of a subset of the data to determine the different groupings within the data. Each group is assigned a label, and all the data with this label are compared to ground truth to associate each label with one of the classes defined by the data user. After this training is completed, each data point is classified by measuring the distance between it and each of the cluster centers and classifying it according to the nearest cluster.

The maximum likelihood algorithm is a statistical procedure based on the probability density function of the data. For the case of Gaussian data, which is a valid model for multispectral imagery of the earth's surface, only first and second order statistics are required. A system based on this approach is designed by calculating these statistics from data samples of

Table 3(II) Typical Data Rate Ranges

Application	Resolution (m) min-max	Field of Coverage (km) min-max	No. of Channels min-max	Data Rates (M bits/sec) min-max
A1	30-50	185	4-7	11.5- 56.1
A2	30-50	185	4-7	11.5- 56.1
A3	30-50	185	4-7	11.5- 56.1
A4	10-30	50	4-7	8.7- 137.0
A5	30-50	185	4-7	11.5- 56.1
C1	30-50	200	6-20	18.7- 173.0
C2	30-50	200	6-20	18.7- 173.0
C3	30-50	200	6-20	18.7- 173.0
C4	50-100	200	6-20	4.7- 62.4
C5	50-100	200	6-20	4.7- 62.4
C6	3-10	40	6-20	93.6-3470.0
C7	30-300	200	6-20	.5- 173.0
F1	50-100	185	4-7	2.9- 20.2
F2	5-10	15-30	4-7	23.4- 328.0
F3	10-30	185	4-7	32.1- 505.0
F4	30-50	185	4-7	11.5- 56.1
G1	30-50	185	4	11.5- 32.1
G2	30-50	185	4	11.5- 32.1
G3	50-100	185	4	2.9- 11.5
G4	5-10	15-30	4	23.4- 187.0
G5	5-10	15-30	4	23.4- 187.0
L1	50-80	185	1-5	1.1- 14.7
L2	50-80	185	1-5	1.1- 14.4
L3	50-80	185	1-5	1.1- 14.4
L4	50-80	185	1-5	1.1- 14.4
L5	10-30	15	1-5	.7- 29.3
L6	100-200	185	1-5	.2- 3.6
H1	40-60	200	1-3	2.2- 14.6
H2	30-50	200	1-3	3.1- 26.0
H3	10-30	50	1-3	2.2- 58.5
H4	30-70	200	1-3	1.6- 26.0
H5	50-80	200	1-3	1.2- 9.4
M1	200-400	800	2	.4- 1.6
M2	200-400	800	2	.4- 1.6
O1	1-10km	400	4-20	0.0* 0.3
O2	30-100	200	4-20	3.1- 173.0
O3	1-10km	200	4-20	0.0** 0.2

* 624 bits/sec **312 bits/sec

known classes and then assuming that all data from the same class have these same statistics. Subsequently, data are classified by comparing their statistics to the statistics of each of the classes and deciding in favor of the class they most closely resemble.

The perceptron algorithm is based on a set of decision functions which are adjusted by an iterative technique to fit data of known classes and then used to classify subsequent data.

The table look-up algorithm essentially stores in a large table (computer memory) all possible outcomes of the data and associates with each possible outcome one of the classes. During the design phase, one of the classes is associated with each of the possible values of the input data. Subsequent data are then classified by using the data point to address the memory to look up the classification.

The clustering, maximum likelihood and perceptron algorithms require a significant amount of computation, mainly additions, multiplications and comparisons. The table look-up algorithm requires a much smaller amount of computation, but significantly more memory.

Preprocessing Algorithms

The extremely large volume of data generated by an MSS imposes a severe computational burden on the on-board processor. The possibility of using a preprocessor between the sensor and the processor to reduce the bulk of data by using data compression and feature selection techniques was studied. Two algorithms were studied in detail: (1) transform coding, and (2) BLOB.

Transform coding allows a data bulk reduction by a factor of 2 to 4 for most multispectral data without degrading the data quality.

The BLOB algorithm developed at Purdue University achieves data bulk reduction by a factor of 10 to 30, but requires more computation and more memory than transform coding.

Algorithm Computation Requirements

Each of the data analysis algorithms (clustering, maximum likelihood, perceptron, and table look-up) and the preprocessing algorithms (transform coding, and BLOB coding) were analyzed in detail relative to their computational requirements, i.e., the number of additions, multiplications, comparisons, etc., required to implement these algorithms along with the requirements

imposed by the sequence of operations (some operations can be done in parallel while others follow a sequence where one operation must be completed before the next can begin). The algorithm computational requirements were tabulated for each of the data analysis and preprocessing algorithms.

It was concluded that using a preprocessor to reduce the load on the processor is not a lucrative alternative. Even though the preprocessor can reduce the data load by a factor from 2 to 30 and thus reduce the complexity of the data processor by this amount, the total system complexity is not reduced because the savings in processor complexity are more than offset by the increase in the preprocessor complexity.

It was further determined that the perceptron and clustering algorithms require a more complex processor than the maximum likelihood and table look-up algorithms for all user requirements. Consequently, we concluded that only the maximum likelihood and table look-up algorithms are worthy of further consideration.

Technology Forecast and Assessment

A detailed survey of 1975 component technologies was carried out. A number of 1975 microelectronics technology families are listed in Table 3(III). The speeds, power, size, cost, reliability, etc., of each are tabulated.

Table 3(III) Some 1975 Component Technologies

FAMILY	DENSITY GATES/mm^2	LSI ON-CHIP POWER-DELAY PRODUCT, pJ 15V	5V	1V	SMALLEST DELAY, ns
SCHOTTKY BIPOLAR	30-40	-	5	-	2
CMOS	30-40	50	5	-	10
STATIC NMOS	80-120	50	5	-	20
CMOS/SOS	80-120	25	3	-	3
I^2L BIPOLAR	100-120	-	5	1	10

Component technology was also projected from 1975 to 1985 using estimates obtained from component manufacturers and other experts in the field. The major conclusions are that some parameters associated with microelectronic component technology are changing at rates between 1 or 2 orders of magnitude every 10 years, with the result that overall component performance is changing by several orders of magnitude in the same time frame. In particular, the number of components (gates, transistors, etc.) per chip increased by a factor

of 10 between 1965 and 1975 and is expected to increase by another factor of 10 between 1975 and 1985. In addition, propagation delays decreased by one order of magnitude between 1965 and 1975, and are expected to decrease by another order of magnitude between 1975 and 1985. With the equivalent number of gates in an IC chip increasing by a factor of 10 and the processing speed increasing by a factor of 10, the total number of computations per unit time (computational power) increases by a factor of 100.

Projections for computer system technology resulted in similar estimates, i.e., microcomputer cycle times, add times, etc., are projected to decrease by one order of magnitude during the next 10 years as they have for the past 10 years. The number of bits of memory contained in a given area on an IC chip are likewise projected to increase by an order of magnitude over the next 10 years as they have over the past 10 years. Meanwhile, the size and power dissipation per IC chip is expected to stay constant while the number of pins per package which increased by a factor of four between 1965 and 1975 is expected to increase by only a factor of two between 1975 and 1985.

A computer model that uses input data from past years to predict future values of these parameters was also developed. These computer-generated projections are in close agreement with the predictions made by experts from the microelectronics industry.

On-Board Processor Designs

A number of on-board processors capable of implementing the maximum likelihood and table look-up algorithms for the candidate input data format were designed. In order to operate in real time at the 32-megabit/sec required data rate, the designs are based on multiprocessor concepts using pipeline and parallel arrays of subprocessors. Sufficient subsystems were added in parallel to obtain the 32 megabit/sec throughput.

Two different design approaches were investigated in detail. One is a hardware approach consisting of logic circuits designed to efficiently implement the mathematical operations required by the algorithms. One special purpose hardware design was developed to implement the maximum likelihood algorithm and another to implement the table look-up algorithm.

The second design approach uses microprocessors which allows a number of different computations to be performed with the same hardware under software control. Computer programs for implementing all of the operations were written in order to determine the number of instruction cycles required to implement each

algorithm. This established the throughput data rate and, consequently, the number of parallel subsystems required to handle the 32 megabit/sec rate.

Applying both of these design approaches to both algorithms resulted in four system designs: (1) Hardware Maximum Likelihood (HML), (2) Hardware Table Look-Up (HTLU), (3) Microprocessor Maximum Likelihood (μPML), and (4) Microprocessor Table Look-Up (μPTLU). For each of these designs the number of IC's, power, volume, weight, and cost were determined based on 1975 technology.

Because microprocessors are significantly slower than TTL circuits, the hardware approaches require fewer IC's, less power and volume, and cost less than the microprocessor designs.

4 FEASIBILITY TRADE-OFF AND SENSITIVITY ANALYSIS

Each of the processor designs handle the 32-megabit input rate by distributing the processing load between many similar subprocessors. Consequently, the number of IC's, power, weight, volume, and cost are all essentially proportional to the number of subprocessors. Therefore, a system complexity function was defined for each of the four processors and its dependence on the following parameters was established using 1975 technology:

- R data bit rate (bits/sec)
- n number of spectral bands (channels)
- b number of bits per resolution element per spectral band (bits)
- M number of classes
- r pixel rate (resolution elements/sec)

From the results of the component and system technology forecasts, the complexity function dependence on time for 10 years into the future was also taken into account. The resulting complexity functions are listed in Table 4(I).

Table 4(I) Processor Complexity Functions

Processor	Complexity Function
Microprocessor Maximum Likelihood (μPML)	$P_1 = k_1\ M(n+1)\ R(1.5)^{-T}$
Hardware Maximum Likelihood (HML)	$P_2 = k_2\ M(n+1)\ R(1.5)^{-T}$
Microprocessor Table Look-Up (μPTLU)	$P_3 = k_3\ M\ R\ (1.6)^{nb}\ (1.5)^{-T}$
Hardware Table Look-Up (HTLU)	$P_4 = k_4\ M\ R\ (1.6)^{nb}\ (1.5)^{-T}$

The scale factors k_1, k_2, k_3, and k_4 were determined for each performance measure (number of IC's, power, volume, weight and cost) and are listed in Table 4(II).

Table 4(II) Scale Factors for the Complexity Functions of Table 4(I) for Each Performance Measure.

Scale Factor	#IC's	Power(w)	Volume(m^3)	Weight(kg)	Cost
k_1	1.6×10^{-5}	1.8×10^{-6}	2.67×10^{-10}	1.34×10^{-7}	9.08×10^{-4}
k_2	3.21×10^{-7}	1.6×10^{-7}	1.6×10^{-11}	8.01×10^{-9}	8.01×10^{-6}
k_3	3.03×10^{-9}	1.52×10^{-9}	2.53×10^{-14}	1.15×10^{-11}	7.59×10^{-8}
k_4	4.05×10^{-11}	2.02×10^{-11}	3.37×10^{-15}	1.21×10^{-12}	1.08×10^{-9}

These models for the four design approaches were then used to determine the sensitivity of the complexity to the various system parameters. This was accomplished by setting all system parameters to the baseline values n = 4 spectral bands, M = 12 classes, b = 6 bits, R = 32 megabits/sec, and T = 0. Figures 4(1), 4(2) and 4(3) show the sensitivity of the designs to variations in the data throughput rate R, the time T, the number of bits per data word b, and the number of spectral bands n.

Any feasibility analysis depends on a definition of what feasible means. For a particular processor to be "feasible" at a particular point in time requires that it meet certain constraints on performance, complexity, volume, weight, power, cost, reliability, and operating environment. Each of the four system architectures meets the performance constraint since each was designed to accomplish the required task. All four processors use standard integrated circuit technology and meet the data throughput rates by adding more components (IC's) in parallel. The volume, weight, and power dissipation of integrated circuits can be kept within limits simply by keeping the number of integrated circuits within limits. The radiation, temperature, and other environmental constraints can be met by each processor as discussed in Section 2 of the final report [1]. The limiting factors are cost and reliability which can also be kept within bounds by imposing a constraint on the number of components. Consequently, it was concluded that on-board processing using a particular processor is feasible provided the number of IC's in the processor is constrained to a reasonable number.

The parts cost of the on-board processor increases linearly as the number of IC's. The costs associated with check out increase as the square of the number of IC's. Limiting the number of IC's in the on-board processor to about 1000 appears to satisfy all constraints, i.e., cost is reasonable relative to the total system cost (launch, sensors, telemetry, etc.), reliability

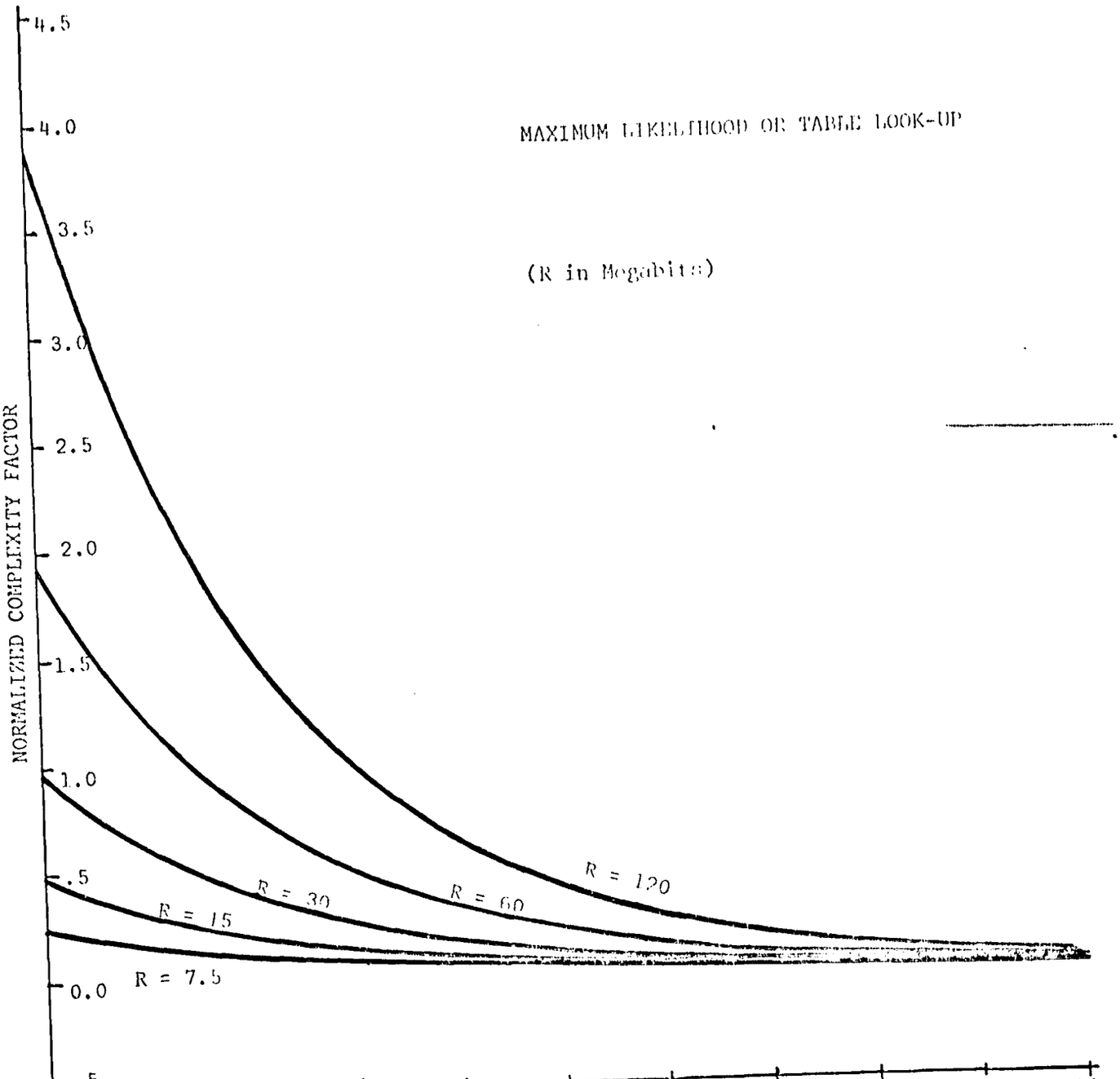

Figure 4(1) Complexity Function Sensitivity to R and T (all Processors)

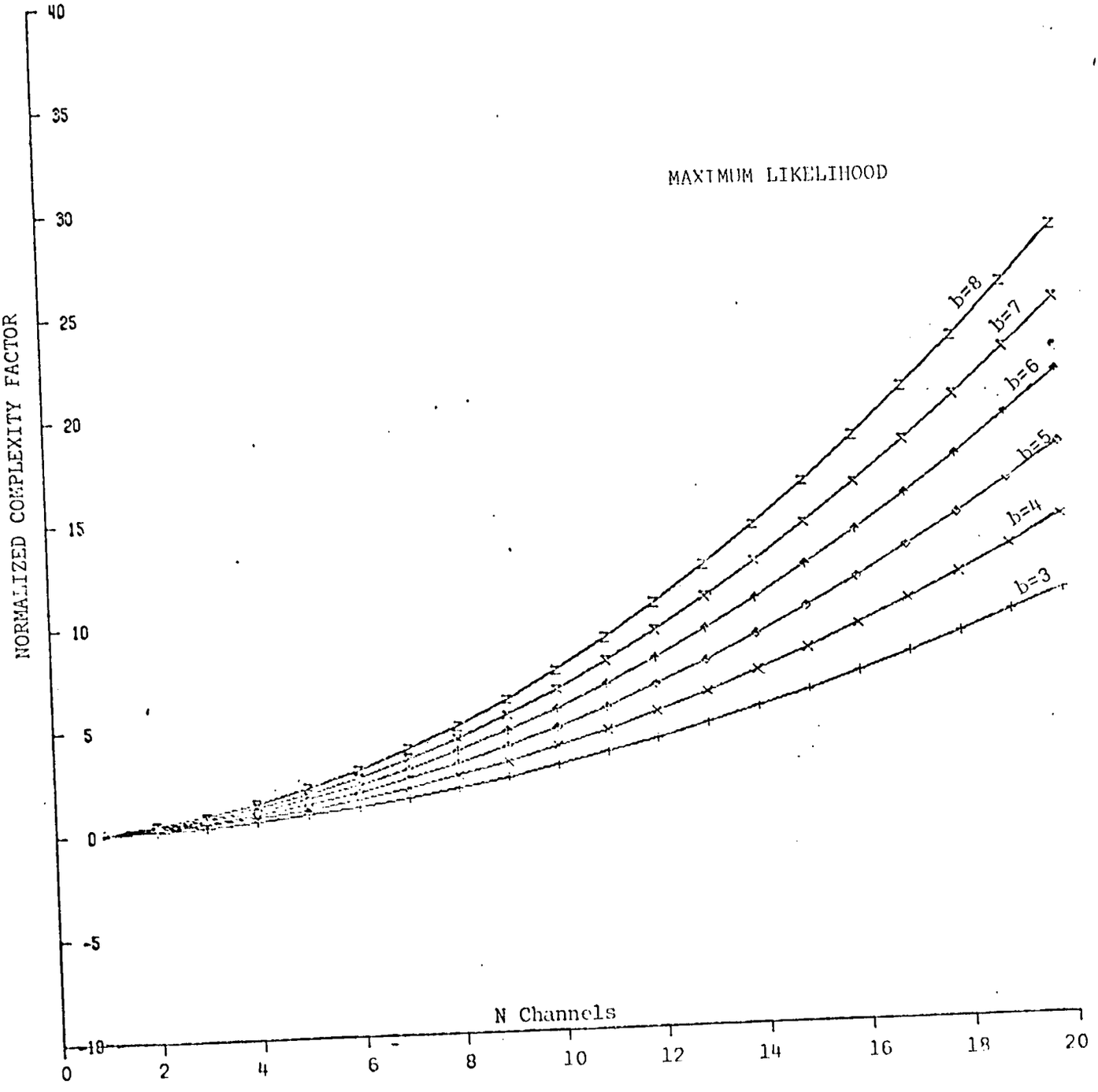

Figure 4(2) Complexity Function Sensitivity to b and n (ML Processors)

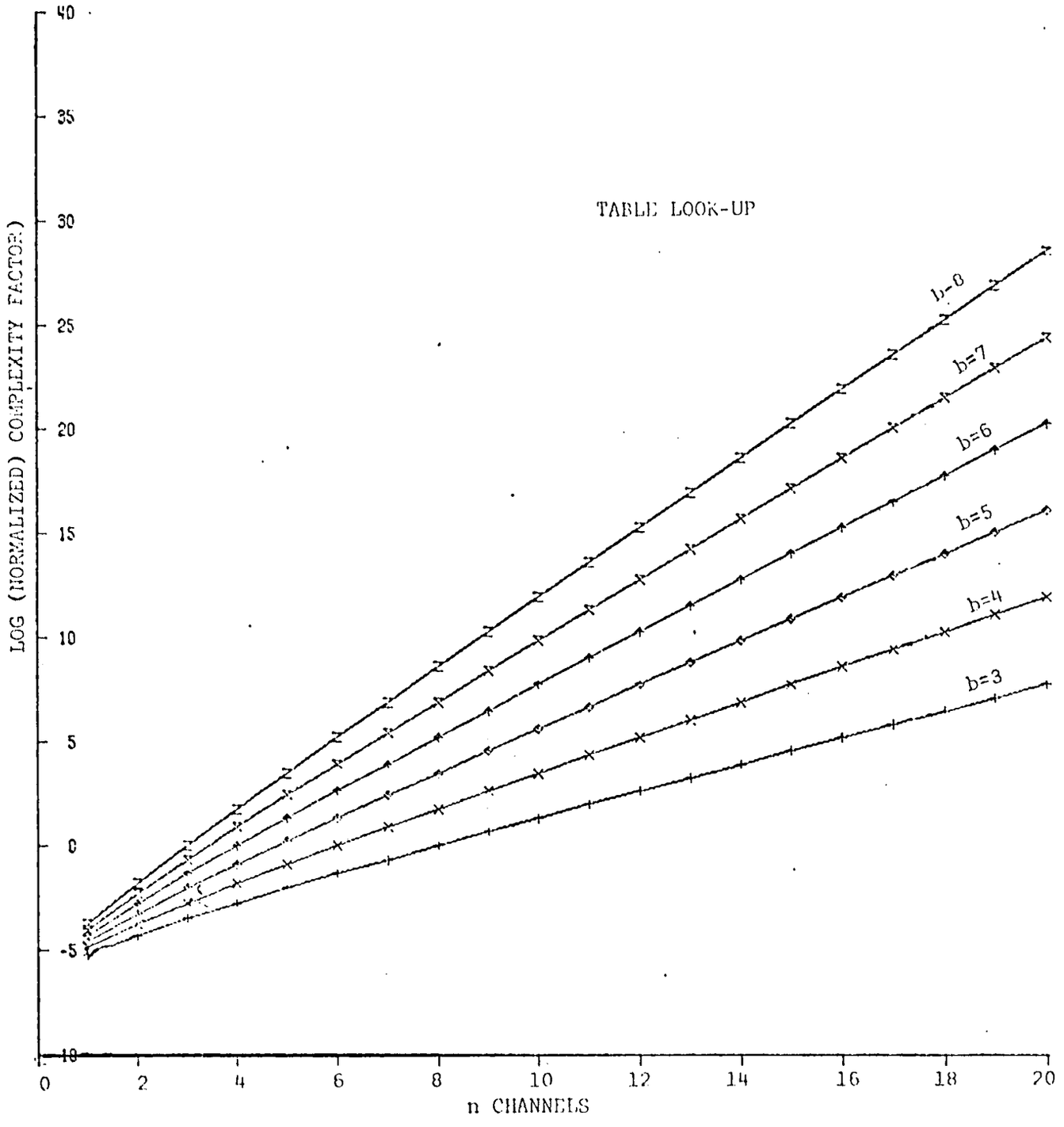

Figure 4(3) Complexity Function Sensitivity to b and n (TLU Processor)

is pushing the limits of present day technology, while volume, weight, and power dissipation do not appear to present serious difficulties.

Using the 1000 IC definition of feasibility, the year in which each user application first becomes feasible for each design approach was calculated. These results are summarized in Tables 4(III) and 4(IV). These results are summarized in more compact form in Figure 4(4), which shows the percentages of user applications that can be implemented by each of the four design approaches for both the minimum and the maximum user requirements.

Summary tables corresponding to other definitions of feasibility are easily generated from Figures 4.4.3(1)-4.4.3(12) of the final report. For example, Tables 4(V) and 4(VI) are similar to Tables 4(III) and 4(IV) except that the processor is limited to 500 IC packages. Figure 4(5) shows the percentage of user applications that can be implemented with 500 IC's using each of the four design approaches for both the minimum and maximum user requirements. Similarly, Tables 4(VII) and 4(VIII) and Figure 4(6) correspond to a more elaborate 2000 IC processor. A factor of 1.58 in the number of IC's corresponds to one year in the date the processor becomes feasible. Multiplying the number of IC's by 1.58 makes the processor feasible one year earlier. Or, stated the other way, waiting one year means the processor can be designed with 1/1.58 = .63 as many IC's.

Table 4.(III) For Each Application Listed in the First Column, the Succeeding Columns List the Year that the Processor Becomes Feasible (1000 IC's) for the Maximum Requirements Listed in Table 1.1.2(I): N means Not Feasible by 1990.

Application	Microprocessor Maximum Likelihood (μPML)	Hardware Maximum Likelihood (HML)	Microprocessor Table Look-Up (μPTLU)	Hardware Table Look-Up (HTLU)
A1	1989	1981	N	N
A2	1989	1981	N	N
A3	1989	1981	N	N
A4	N	1983	N	N
A5	1989	1981	N	N
C1	N	1985	N	N
C2	N	1985	N	N
C3	N	1985	N	N
C4	N	1983	N	N
C5	N	1983	N	N
C6	N	1983	N	N
C7	N	1985	N	N
F1	1987	1980	N	N
F2	N	1985	N	N
F3	N	1986	N	N
F4	1989	1981	N	N
G1	1987	1980	1989	1980
G2	1987	1980	1989	1980
G3	1985	1980	1987	1980
G4	N	1982	N	1984
G5	N	1982	N	1984
L1	1986	1980	N	1984
L2	1986	1980	N	1984
L3	1986	1980	N	1984
L4	1986	1980	N	1984
L5	1987	1980	N	1986
L6	1983	1980	N	1981
H1	1985	1980	1982	1980
H2	1986	1980	1983	1980
H3	1988	1980	1985	1980
H4	1986	1980	1983	1980
H5	1984	1980	N	1986
M1	1980	1980	1980	1980
M2	1980	1980	1980	1980
O1	1980	1980	N	N
O2	N	1985	N	N
O3	1980	1980	N	N

Table 4.(IV) For Each Application Listed in the First Column, the Succeeding Columns List the Year that the Processor Becomes Feasible (1000 IC's) for the Minimum Requirements Listed in Table 1.1.2(I): N means Not Feasible by 1990.

Application	Micro-processor Maximum Likelihood (μPML)	Hardware Maximum Likelihood (HML)	Micro-processor Table Look-Up (μPTLU)	Hardware Table Look-Up (HTLU)
A1	1985	1980	1988	1980
A2	1985	1980	1988	1980
A3	1985	1980	1988	1980
A4	1984	1980	1987	1980
A5	1985	1980	1988	1980
C1	1987	1980	N	N
C2	1987	1980	N	N
C3	1987	1980	N	N
C4	1984	1980	N	1988
C5	1984	1980	N	1988
C6	N	1982	N	N
C7	1980	1980	N	1983
F1	1982	1980	1984	1980
F2	1986	1980	1989	1980
F3	1987	1980	1989	1980
F4	1985	1980	1987	1980
G1	1985	1980	1987	1980
G2	1985	1980	1987	1980
G3	1982	1980	1984	1980
G4	1986	1980	1989	1980
G5	1986	1980	1989	1980
L1	1980	1980	1980	1980
L2	1980	1980	1980	1980
L3	1980	1980	1980	1980
L4	1980	1980	1980	1980
L5	1980	1980	1980	1980
L6	1980	1980	1980	1980
H1	1980	1980	1980	1980
H2	1980	1980	1980	1980
H3	1980	1980	1980	1980
H4	1980	1980	1980	1980
H5	1980	1980	1980	1980
M1	1980	1980	1980	1980
M2	1980	1980	1980	1980
O1	1980	1980	1980	1980
O2	1982	1980	1985	1980
O3	1980	1980	1980	1980

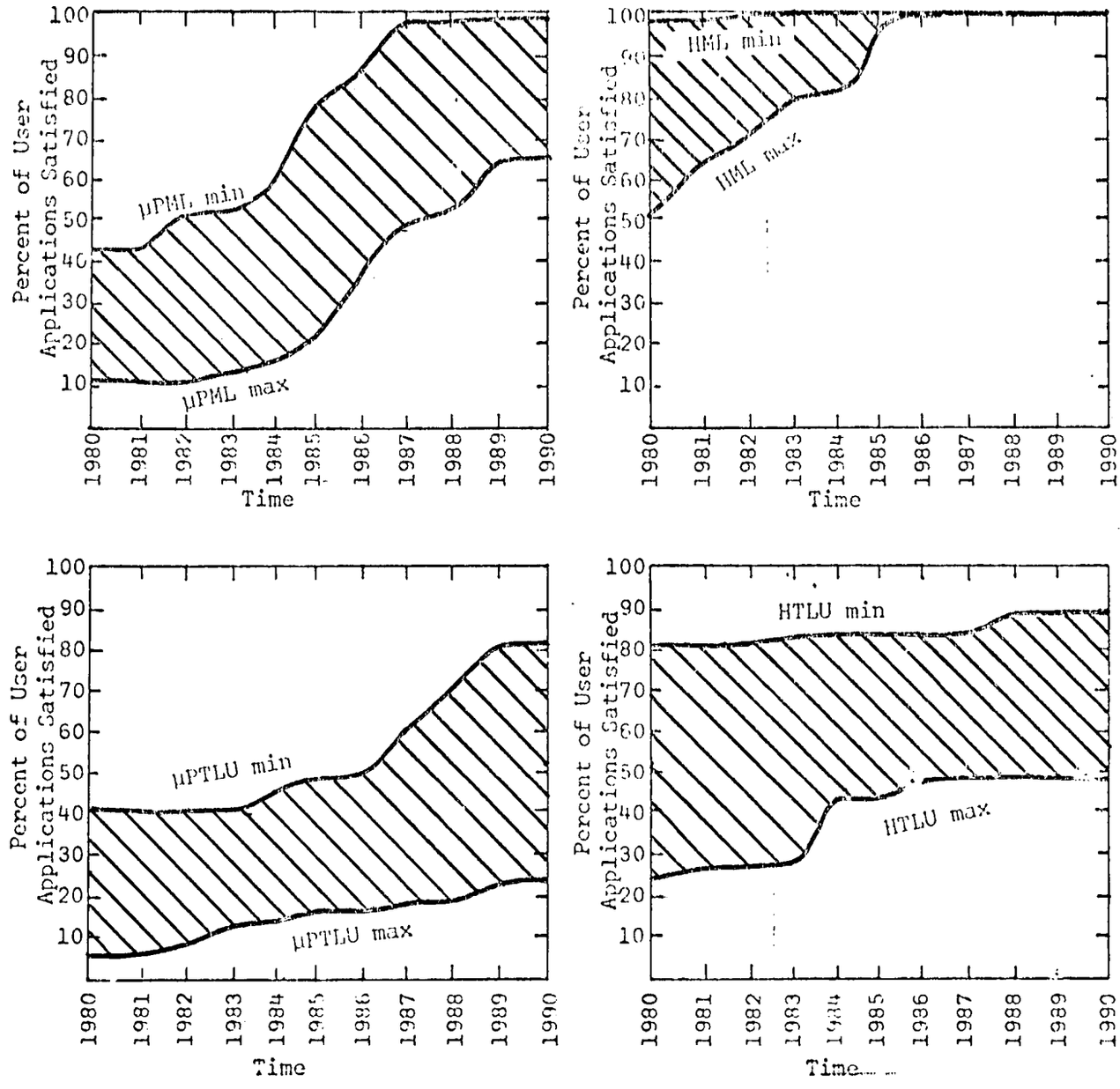

Figure 4(4) Percent of User Applications Satisfied as a Function of Time (1,000 IC's).

Table 4.(V) For Each Application Listed in the First Column, the Succeeding Columns List the Year that the Processor Becomes Feasible (500 IC's) for the Maximum Requirements Listed in Table 1.1.2(I): N means Not Feasible by 1990.

Application	Microprocessor Maximum Likelihood (μPML)	Hardware Maximum Likelihood (HML)	Microprocessor Table Look-Up (μPTLU)	Hardware Table Look-Up (HTLU)
A1	N	1982	N	N
A2	N	1982	N	N
A3	N	1982	N	N
A4	N	1984	N	N
A5	N	1982	N	N
C1	N	1986	N	N
C2	N	1986	N	N
C3	N	1986	N	N
C4	N	1985	N	N
C5	N	1985	N	N
C6	N	N	N	N
C7	N	1987	N	N
F1	1989	1980	N	N
F2	N	1986	N	N
F3	N	1987	N	N
F4	N	1982	N	N
G1	1988	1980	N	1982
G2	1988	1980	N	1982
G3	1986	1980	1989	1980
G4	N	1984	N	1985
G5	N	1984	N	1985
L1	1987	1980	N	1986
L2	1987	1980	N	1986
L3	1987	1980	N	1986
L4	1987	1980	N	1986
L5	1989	1980	N	1987
L6	1984	1980	N	1983
H1	1986	1980	1983	1980
H2	1987	1980	1985	1980
H3	1989	1981	1986	1980
H4	1987	1980	1985	1980
H5	1985	1980	1982	1980
M1	1981	1980	1980	1980
M2	1981	1980	1980	1980
O1	1982	1980	N	N
O2	N	1987	N	N
O3	1980	1980	N	N

Table 4.(VI) For Each Application Listed in the First Column, the Succeeding Columns List the Year that the Processor Becomes Feasible (500 IC's) for the Minimum Requirements Listed in Table 1.1.2(I): N means Not Feasible by 1990.

Application	Microprocessor Maximum Likelihood (μPML)	Hardware Maximum Likelihood (HML)	Microprocessor Table Look-Up (μPTLU)	Hardware Table Look-Up (HTLU)
A1	1987	1980	1989	1980
A2	1987	1980	1989	1980
A3	1987	1980	1989	1980
A4	1986	1980	1988	1980
A5	1987	1980	1989	1980
C1	1988	1980	N	N
C2	1988	1980	N	N
C3	1988	1980	N	N
C4	1985	1980	N	N
C5	1985	1980	N	N
C6	N	1983	N	N
C7	1980	1980	N	1985
F1	1983	1980	1986	1980
F2	1988	1980	N	1981
F3	1989	1980	N	1982
F4	1986	1980	1989	1980
G1	1986	1980	1989	1980
G2	1986	1980	1989	1980
G3	1983	1980	1986	1980
G4	1988	1980	N	1981
G5	1988	1980	N	1981
L1	1980	1980	1980	1980
L2	1980	1980	1980	1980
L3	1980	1980	1980	1980
L4	1980	1980	1980	1980
L5	1980	1980	1980	1980
L6	1980	1980	1980	1980
H1	1981	1980	1980	1980
H2	1981	1980	1980	1980
H3	1981	1980	1980	1980
H4	1980	1980	1980	1980
H5	1980	1980	1980	1980
M1	1980	1980	1980	1980
M2	1980	1980	1980	1980
O1	1980	1980	1980	1980
O2	1983	1980	1986	1980
O3	1980	1980	1980	1980

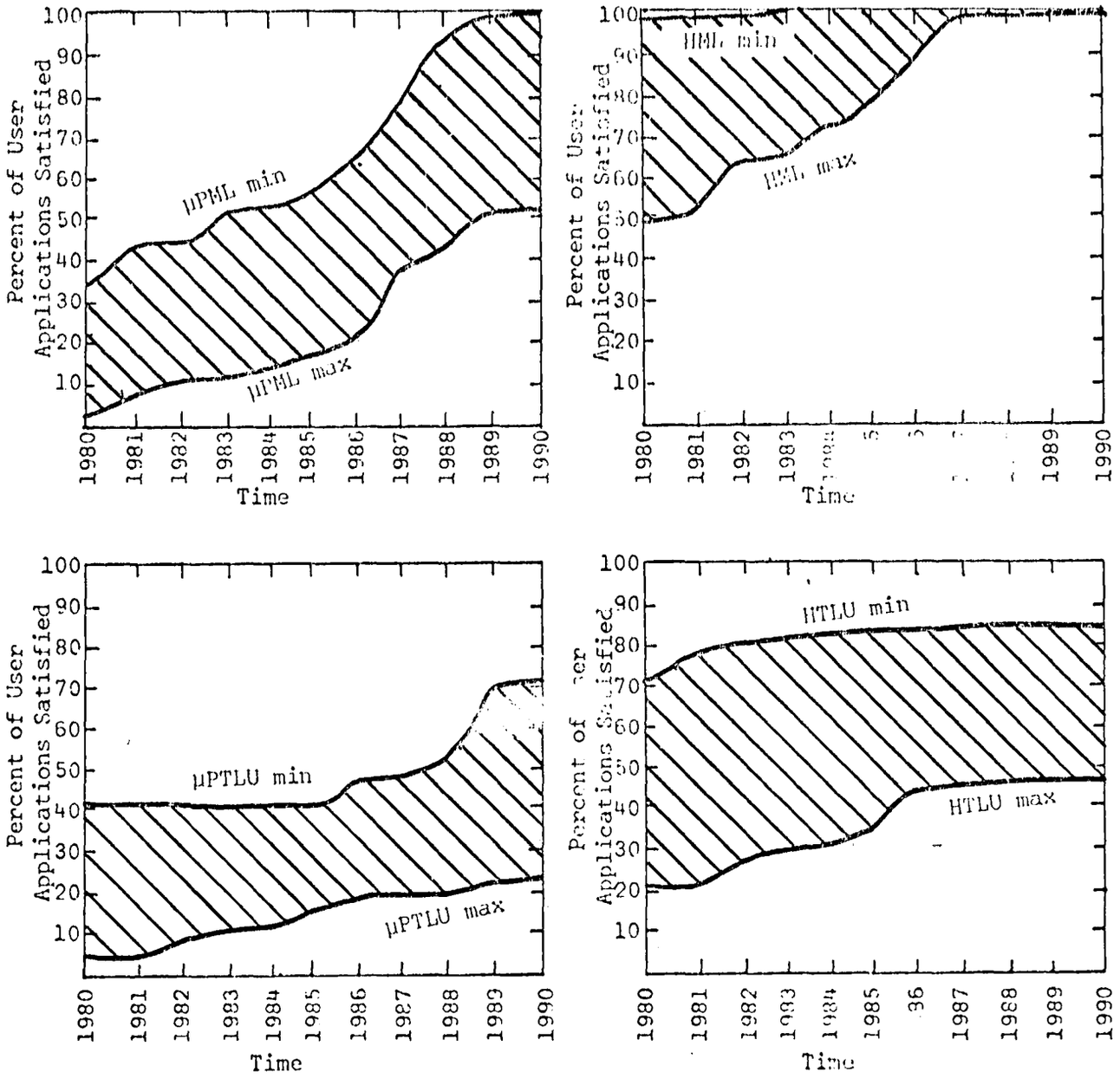

Figure 4(5) Percent of User Applications Satisfied as a Function of Time (500 IC's).

Table 4.(VII) For Each Application Listed in the First Column, the Succeeding Columns List the Year that the Processor Becomes Feasible (2000 IC's) for the Maximum Requirements Listed in Table 1.1.2(I): N means Not Feasible by 1990.

Application	Microprocessor Maximum Likelihood (μPML)	Hardware Maximum Likelihood (HML)	Microprocessor Table Look-Up (μPTLU)	Hardware Table Look-Up (HTLU)
A1	1988	1980	N	N
A2	1988	1980	N	N
A3	1988	1980	N	N
A4	N	1981	N	N
A5	1988	1980	N	N
C1	N	1983	N	N
C2	N	1983	N	N
C3	N	1983	N	N
C4	N	1981	N	N
C5	N	1981	N	N
C6	N	N	N	N
C7	N	1984	N	1984
F1	1985	1980	N	N
F2	N	1983	N	N
F3	N	1984	N	N
F4	1988	1980	N	N
G1	1986	1980	1988	1980
G2	1986	1980	1988	1980
G3	1983	1980	1986	1980
G4	1989	1981	N	1982
G5	1989	1981	N	1982
L1	1984	1980	N	1983
L2	1984	1980	N	1983
L3	1984	1980	N	1983
L4	1984	1980	N	1983
L5	1986	1980	N	1984
L6	1981	1980	1990	1980
H1	1983	1980	1980	1980
H2	1985	1980	1981	1980
H3	1986	1980	1983	1980
H4	1985	1980	1981	1980
H5	1982	1980	1980	1980
M1	1980	1980	1980	1980
M2	1980	1980	1980	1980
O1	1980	1980	N	N
O2	N	1984	N	N
O3	1980	1980	N	N

Table 4. (VIII) For Each Application Listed in the First Column, the Succeeding Columns List the Year that the Processor Becomes Feasible (2000 IC's) for the Minimum Requirements Listed in Table 1.1.2(I): N means Not Feasible by 1990.

Application	Microprocessor Maximum Likelihood (μPML)	Hardware Maximum Likelihood (HML)	Microprocessor Table Look-Up (μPTLU)	Hardware Table Look-Up (HTLU)
A1	1984	1980	1987	1980
A2	1984	1980	1987	1980
A3	1984	1980	1987	1980
A4	1983	1980	1985	1980
A5	1984	1980	1987	1980
C1	1985	1980	N	1990
C2	1985	1980	N	1990
C3	1985	1980	N	1990
C4	1982	1980	N	1986
C5	1982	1980	N	1986
C6	1988	1980	N	N
C7	1980	1980	N	1982
F1	1980	1980	1983	1980
F2	1985	1980	1988	1980
F3	1986	1980	1988	1980
F4	1983	1980	1986	1980
G1	1983	1980	1986	1980
G2	1983	1980	1986	1980
G3	1980	1980	1983	1980
G4	1985	1980	1987	1980
G5	1985	1980	1987	1980
L1	1980	1980	1980	1980
L2	1980	1980	1980	1980
L3	1980	1980	1980	1980
L4	1980	1980	1980	1980
L5	1980	1980	1980	1980
L6	1980	1980	1980	1980
H1	1980	1980	1980	1980
H2	1980	1980	1980	1980
H3	1980	1980	1980	1980
H4	1980	1980	1980	1980
H5	1980	1980	1980	1980
M1	1980	1980	1980	1980
M2	1980	1980	1980	1980
O1	1980	1980	1980	1980
O2	1980	1980	1983	1980
O3	1980	1980	1980	1980

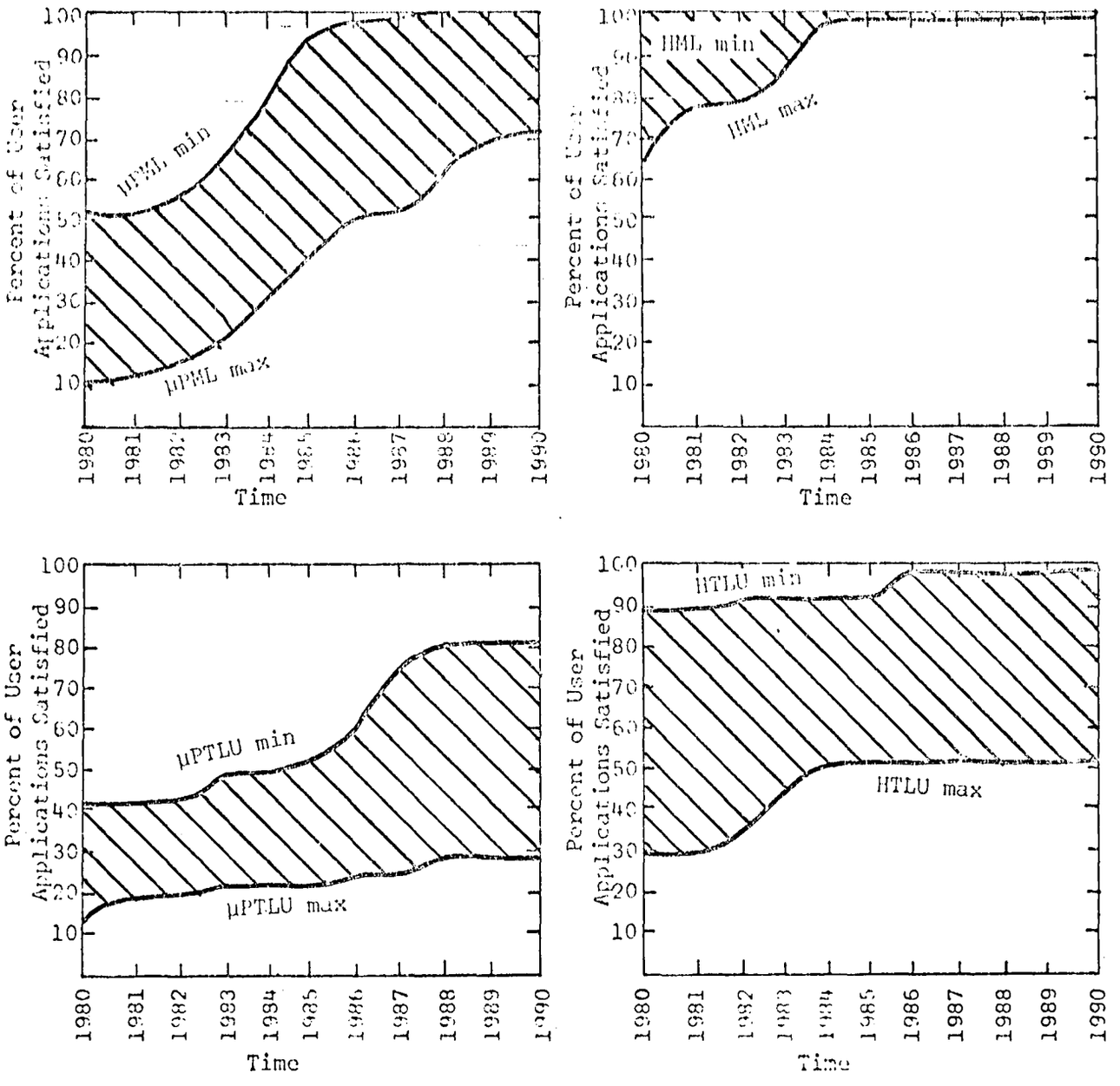

Figure 4(6) Percent of User Applications Satisfied as a Function of Time (2,000 IC's).

5 CONCLUSIONS

The basic conclusions of this study are:

(1) From results of the user applications survey we conclude that potential users will require a wide range of resolutions, a wide range of field of coverage, a wide range of number of channels, and these requirements, in turn, result in a wide range of data throughput rates.

(2) From the results of the survey of data analysis algorithms we conclude that the maximum likelihood and table look-up algorithms are superior to other known algorithms for all user requirements. The table look-up algorithm is superior to the maximum likelihood algorithm, except for situations requiring more than five spectral bands.

(3) From the results of the investigation of the possibility of using a preprocessor to reduce the data load on the processor, we conclude that the total on-board system complexity is minimized with no preprocessor.

(4) From the results of the component and computer system technology forecasts and assessment, we conclude that the on-board processor capability (the amount of throughput it will be able to handle) will increase by two orders of magnitude between 1975 and 1985.

(5) From the on-board processor designs and evaluations we conclude that implementations utilizing specially designed hardware require less hardware, power, volume, weight, and cost less than microprocessor (software) based systems.

(6) From the feasibility and sensitivity analysis, we conclude that most, but not all, user applications could be satisfied by an on-board processor sometime between 1980 and 1990.

6 RECOMMENDATIONS

Handling the On-Board Processor Output Data Products

While this study was directed towards determining the feasibility of on-board processors for the 1980-1990 time frame, the question remains as to how the output of an on-board processor could be treated. Now that this study has established the feasibility of on-board processing, the problem of compressing and distributing the on-board computer output needs to be addressed.

It is recommended that a study be made to investigate the users of on-board processor output with particular attention paid to data rates and formats.

Dates for Cost Effective Launches

Our study concludes that some users could be satisfied with a processor designed today and flown in 1980. Other users cannot be satisfied until 1990 and beyond. These conclusions are based on technical feasibility and do not address the question of economics. It is recommended, therefore, that a study be made to establish a projected time frame for the launch of cost effective earth resources missions.

Stimulation of Industry

Finally, it is recommended that no stimulus be given to industry to develop large-scale integration (LSI) technology for on-board earth resources processors. It is recommended instead that the resources be used to encourage the solution of problems peculiar to NASA which do not have a parallel in industry, such as improvements in multi-spectral scanners and special techniques such as parallel processing. While this philosophy may be contrary to NASA's "Spin off" philosophy, stimuli from other sources are already present in the LSI field and further stimulus by NASA would have little effect and would be wasteful of NASA resources.

REFERENCES

1. Satellite On-Board Processing for Earth Resources Data - Final Report, CR 137758, NASA/ARC, Moffett Field, California, 94035.

APPENDIX

SUMMARY OF THE FINAL REPORT BY SECTIONS

The following is a brief outline of the material contained in the final report [1].

Section 0 INTRODUCTION

This section contains a statement of the study objective, outlines the study plan, and describes the content of subsequent sections.

Section 1 EARTH RESOURCES ALGORITHMS AND DATA SETS

This section contains the results of a survey of earth-resources-user data requirements, earth resources multispectral scanner sensor technology, preprocessing algorithms for correcting the sensor outputs and for data bulk reduction, and a candidate data format to be used in subsequent sections.

Section 1.1 contains the results of the user requirements survey and their projected data needs in the 1980-1990 decade. The survey is based on existing literature and on personal interviews with earth resources experimenters. A survey of algorithms for carrying out the user requirements was also conducted. The maximum likelihood, perceptron, table look-up and clustering algorithms were examined in detail.

Section 1.2 deals with present-day and projected state-of-the-art technology relative to electro-mechanical and solid-state scanners and their characteristics.

Section 1.3 contains a discussion of preprocessing algorithms for radiometric, gain, and offset corrections. Preprocessing algorithms for reducing the data bulk passed to the on-board processor using data compression and redundancy removal techniques are surveyed and analyzed.

In Section 1.4 a candidate data format is developed. This is used in later parts of the study as a baseline format for designing on-board computer architectures.

Section 2 ON-BOARD PROCESSOR REQUIREMENTS

This section contains three principal subsections. Section 2.1 is devoted to a detailed analysis of computational requirements for the algorithms developed in Section 1. These algorithms are compared in terms of the number of arithmetic operations required for their computer implementation. The

total number of operations for a typical ERTS frame is also derived for each algorithm.

Section 2.2 contains several computer architectures and organizations with particular emphasis on pipeline, array processors and multiprocessors, since it is apparent that some sort of parallel processor will be required to keep up with the high data rates characteristic of MSS systems. Memory and software requirements are also discussed. A number of on-board processors are then designed to efficiently implement the maximum likelihood and table look-up algorithms at the required rates.

Finally, the environmental effects on the on-board processor for both earth-synchronous and sun-synchronous orbits are discussed in Section 2.3.

Section 3 TECHNOLOGY FORECAST AND ASSESSMENT

The ability of the on-board processors designed in Section 2 to implement the algorithms described in Section 1 in real time for the required throughput data rates depends on the components that will be available at the time of system design. The lead-time required for design, procurement, fabrication, checkout, and launch is about 5 years, so that 1980-1990 launches will utilize 1975-1985 technology. Consequently, accurate component and system technology forecasts are required for the next ten years.

Section 3.1 deals with performance measurement criteria and Section 3.2 contains a survey of the electronic component technology available in 1975. Future improvements in component technology from 1975 to 1985 are then projected from these figures.

Section 3.3 contains a review of computer system technology available in 1975 and a forecast of future system technology based on manufacturers' estimates and a technology forecasting model.

Section 3.4 contains a survey of existing satellite on-board computers and a discussion of future on-board processor technology.

In Section 3.5 a forecast feedback system is developed. This system allows the incorporation of the projected component and system technologies into the on-board processor architectures. The results are then used to obtain a better estimate of projected performances.

Finally, Section 3.6 contains a brief discussion of other technologies which may have an impact on future on-board systems. A very fast computer architecture being studied at the NASA Goddard Space Flight Center is one

example of predicted architectures which emphasize high parallelism. In terms of components, Josephson Tunneling Devices hold a promise of extremely high switching speeds at very low power levels.

Section 4 FEASIBILITY AND TRADEOFF ANALYSIS

A complexity function is derived in this section to evaluate the feasibility of the proposed computer architectures in terms of the most significant parameters related to the performance of on-board processors.

Section 4.1 examines the characteristics of the complexity function for each of the computer architectures developed in Section 2.

Section 4.2 deals with the complexity function dependence on time, and Section 4.3 contains an evaluation of parameters which are constant.

Section 4.4 is devoted to a sensitivity analysis of the complexity function in terms of the variable parameters defined in Section 4.1. These results are then used to evaluate the feasibility of the proposed architectures.

Finally, Section 4.5 contains a discussion of the possible effects of NASA stimulation to industry.

Section 5 SUMMARY, CONCLUSIONS AND RECOMMENDATIONS

This section contains a summary of the results obtained in Sections 1 through 4. Significant results and conclusions are presented, and recommendations are made for future NASA actions in the areas covered by the study.

Section 5.1 defines the study objectives, gives a description of the work tasks undertaken, and describes the significant results of each of the tasks.

Section 5.2 describes the overall conclusions resulting from the study, and Section 5.3 contains recommendations to NASA as a result of the study.