

PACKAGING PRINTED CIRCUIT BOARDS -

A PRODUCTION APPLICATION OF
INTERACTIVE GRAPHICS

Walter A. Perrill

General Dynamics, Pomona Division

INTRODUCTION

Packaging electronic circuits onto printed circuit boards (PCB's) is becoming an increasingly difficult task. The conflicting requirements of "smarter", more complex circuits occupying less space have resulted in smaller PCB's containing more components. The increased use of integrated circuits and hybrid devices has only partially alleviated this situation. The situation is especially acute at General Dynamics, Pomona, because of the variety of circuits used. The design engineers package DC, analog, high speed digital and high frequency RF circuits - often in combination on the same PCB. Computer assistance is required to package these complex PCB's effectively.

Several batch mode programs for packaging PCB's were evaluated (starting in 1970) but none was satisfactory. The major reasons for this included the excessive amount of computer time required and unduly restrictive assumptions concerning component shape and number of conductor layers. Many of these difficulties seemed to stem from the fact that the programs attempted to achieve total automation of the packaging process with little or no human intervention. An analysis of the problems involved led to the belief that total automation was not likely in the near future.

Therefore, it was decided to try another approach using interactive graphics. This approach would allow the designer to monitor and direct the computer's actions in all phases of the packaging process. The intent was to combine the data storage and manipulation power of the computer with the imaginative, intuitive power of a human designer. This approach resulted in a computer program called the Interactive Graphics Packaging Program (IGPP), which is now in production use. This paper describes the structure and use of the IGPP.

OVERVIEW OF HARDWARE AND SOFTWARE

The hardware currently in use at General Dynamics, Pomona, includes a CDC 6400 with 65,000 words of main memory and 125,000 words of extended core storage. A 30 inch Calcomp drum plotter is on line. The interactive graphics system (IGS) equipment consists of two CDC 777 terminals with 20 inch CRT screens, light pens, and keyboards (see Figure 1). The IGPP program is written in FORTRAN IV Extended with the exception of a few functions coded in COMPASS (assembly language). It executes in a field length of about 32,000 words. Each major function is implemented as a separate primary overlay to reduce the field length. The overlays reside on a random file in absolute code to reduce the time needed to locate and load the desired overlay. This improves system response to user commands.

The data base is maintained on a random disc file by an automatic data management system. This system partitions the data base into blocks and maintains the most frequently used blocks in a buffer in main memory. If the requested data is not in memory, the system automatically pulls the proper block into the buffer. If the buffer is full the least used block is written to the disc to make room for the new block.

The individual pieces of data are chained together in both random and sequential fashion. This structure permits rapid access to any piece of data as well as almost unlimited growth of the data base. The program continuously updates the data base so that it always reflects the current configuration of the PCB.

PROGRAM OPERATION

The IGPP performs four major functions for the designer:

- (1) Data input and display
- (2) Component placement (either automatic or manual)
- (3) Conductor path routing (either automatic or manual)
- (4) Data output

In addition, the program contains built-in functions for detecting system and operator errors, debugging, and insuring the integrity of the data base. Any of these functions may be entered by the operator at any time.

Data Coding and Entry

The initial action by the operator (i.e., the package design engineer) is to code the physical and electrical description of the circuit in a predefined data format. This includes the size and shape of the PCB, the basic grid size (typically .050 or .025 inches) and the window grid size (typically .5 or 1. inches). The window grid partitions the board surface into a set of squares for use in selecting "windows" to view areas of the PCB separately. Specific locations may or may not be assigned to each component. In addition, components may be locked into a fixed location, making them immovable even through operator error. The electrical schematic data is represented by assigning a unique number to each electrically distinct signal net. This number is associated with each component pin which is electrically common to the net. The data is punched into machine cards which are read by the program.

Data Display

The designer has the option of displaying the entire PCB, or selecting any rectangular subset of the window grid squares. The positions of the window grid squares are indicated by the letters A, B, C, D, ... displayed at the upper and right edges of the PCB. The designer selects the four letters which define the left, right, upper and lower boundaries of the desired area.

The components are displayed at their assigned locations on the PCB. Components without pre-assigned locations are automatically placed at the top of the screen (see Figure 2). This is done to avoid prejudicing the designers initial judgement.

Component Placement

The designer may select either of two modes of component placement, automatic or manual. In the automatic placement mode the computer uses a center of mass algorithm to determine the component locations. The designer may elect to have all of the components placed at once over the entire PCB surface, or he may select up to sixteen components to be placed into some specified area. The algorithm groups the components into electrically related families but does not attempt to rotate or move components to eliminate overlaps (see Figure 3). After the automatic mode is complete, the designer enters the manual placement mode to make the necessary adjustments.

In the manual mode the electrical schematic data is indicated by displaying a set of lines, called vectors, from the pins of the component being moved to all other electrically common pins (see Figure 4). The designer may display vectors from any or all of the pins on the selected component.

To move a component the designer selects it with the light pen, then moves the pen with the component following. Components may be rotated as well as translated, giving the designer complete control over component placement. When the component is released the program automatically rounds its position to the basic grid of the PCB. This process continues until the designer is satisfied (or nearly so) with the placement of all of the components (see Figure 5).

Conductor Path Routing

The conductor path routing function may be used in either the automatic or manual mode. In the automatic mode the computer uses a row/column algorithm to route the conductor paths. This algorithm is related to the concept of a channel router in which the width of the channels is equal to the basic grid of the PCB. The channels are horizontal on the front of the PCB (rows) and vertical on the rear (columns). Each channel may contain, at most, one conductor at any given point. Conductors are routed following the channels although short sideways jogs (up to two or three channels) are permitted when dodging small obstacles. Longer sideways runs are completed by making a via (a drilled hole plated with conductive solder) to the other side of the PCB and finishing the run there. The designer may elect to route the entire PCB or only a selected area. When the automatic routing function is complete (see Figure 6) the designer may enter the manual routing mode to make any necessary corrections.

In the manual mode each electrically distinct signal net is routed individually, with the designer selecting the net to be routed. Electrical schematic data is indicated by flashing dots in all component pins which are common to the selected net; electrically common conductors are also flashed. The conductor paths are routed by "drawing" them on the IGS screen with the light pen (see Figure 7). The designer may select the path width and layer of the conductor being routed; up to four layers of conductors are permitted. On the IGS screen the layer of each line is indicated by displaying the line in a different style (solid, dashed, or dotted). Lines may be changed from one layer to another or erased completely. Other options automatically round conductor positions onto the basic grid and align paths horizontal or vertical. Dimension checking options are also available. . Due to hardware limitations on the size of the display file (approximately 7500 16-bit words) only the center line of each path is displayed. However, the path width is indicated during routing by a small circle displayed at the point of the light pen.

Data Output

When the PCB design is complete the designer may select any of the following output options:

- (1) Pen plots showing component and conductor positions (see Figures 8 through 10). These plots are used both in verifying PCB producibility and in formal documentation.
- (2) Pen plot showing the size and location of each hole to be drilled. This plot is used in formal documentation and in the factory production process (see Figure 11).
- (3) Card deck for numerically controlled drilling machines. This deck, related to (2) above is used in the factory production process.
- (4) Card deck to drive a numerically controlled photoplotter (Gerber 1232). The photoplotter produces the artmaster which becomes part of the formal documentation and is used in the factory production process (see Figure 12).
- (5) Printed listing giving a summary of the entire program run.

Data Base Protection

The safety of the data base is insured by the checkpoint function. The designer selects this function at regular intervals during the program run, writing a copy of the current data base to a permanent disc file. A checkpoint file is also written automatically upon program termination. This permits the designer to terminate the program run at any time without loss of data. At some later time the designer may make another program run, access the latest checkpoint file and continue working. In the event of machine failure only the changes made since the last checkpoint are lost; the job may be restarted and continued from that point. For long term storage the data base may be saved on magnetic tape. In the event of later design changes the data base may be restored to the disc and the IGPP used to make the necessary changes.

Error Control

Minor debugging functions include printing the last ten light pen selections and the last five data base references, data base dumps and field length core dumps. These functions may be selected manually by the designer, or automatically by the program when certain error conditions are detected.

CURRENT DEVELOPMENT EFFORTS

The IGPP program is constantly being modified to expand its capabilities, and to meet changing requirements. Among the improvements currently under development are the following:

- (1) Automatic checking of conductor clearance and other design rules.
- (2) Display warning messages to the designer in case of violations.
- (3) Optimization of plotter data. This includes automatic fill-in of ground plane areas and reduction of wasted plotter motion.
- (4) Gate and lead swapping to allow the designer more freedom in digital circuits.

Although the IGPP was developed for packaging PCB's, it was designed to be as general as possible. This generality has permitted the use of the IGPP as a basis for new systems. The development time for new systems is being reduced since many of the display, data base and output functions already exist in the IGPP.

One version is being developed to package integrated circuits and hybrid devices (see Figure 13 and 14). This version contains functions to allow for jumper wire bonds (flying leads), thick film resistors, predefined conductor patterns and automatic checking of critical design rules.

In another project the IGPP is being merged with a set of programs which design passive microwave stripline and microstrip components. Used by a microwave engineer this program will accept electrical data (frequency, dielectric constant, etc.), design a selected component (filter, coupler, etc.) and store it in the data base (see Figure 15). The engineer may recall the stored components, position them on the substrate, and connect them into a completed circuit (see Figure 16). The program will generate the data to produce the artmaster and all other required documentation.

In another project the IGPP was interfaced with a program which simulated a naval weapons exercise. Ships and aircraft were displayed on the screen along with data on their position and motion. Additional data were displayed when the vehicles were selected with the light pen. The exercise planners were able to visually monitor the progress of the exercise and detect problem areas easily. Calcomp pen plots of each important event were included in the formal documentation.

CONCLUSION

The IGPP has been used in production applications since 1972. During this time it has been used to package over 130 PCB's containing an average of 50-75 components and two layers of conductors. Electrically the circuits were primarily analog and RF although digital circuits account for an increasing portion of the total. The most complex PCB packaged to date measured 16.5 cm (6.5 in.) by 19 cm (7.5 in.) and contained 380 components, two layers of ground planes and four layers of conductors mixed with ground planes. Electrically, the circuit contained RF signals extending into the microwave region, high speed digital signals and DC control signals. Conductor paths included stripline buried between ground planes as well as normal conductors. The IGPP produced the basic documentation for the board although the photoplotter data required a good deal of manual manipulation because of the extensive ground planes. The time required to package the board was just over four weeks, from schematic diagram to a finished set of artmasters. Figures 17 and 18 are reproductions of artmasters for two of the six layers.

We feel that the IGPP is a proven production tool now and has great potential for growth. We intend to improve its capabilities and expand its use until it is the main tool for packaging PCB's at General Dynamics.



Figure 1. - Design engineer seated at the graphics terminal. The display screen, keyboard and light pen are the interactive elements of the system.

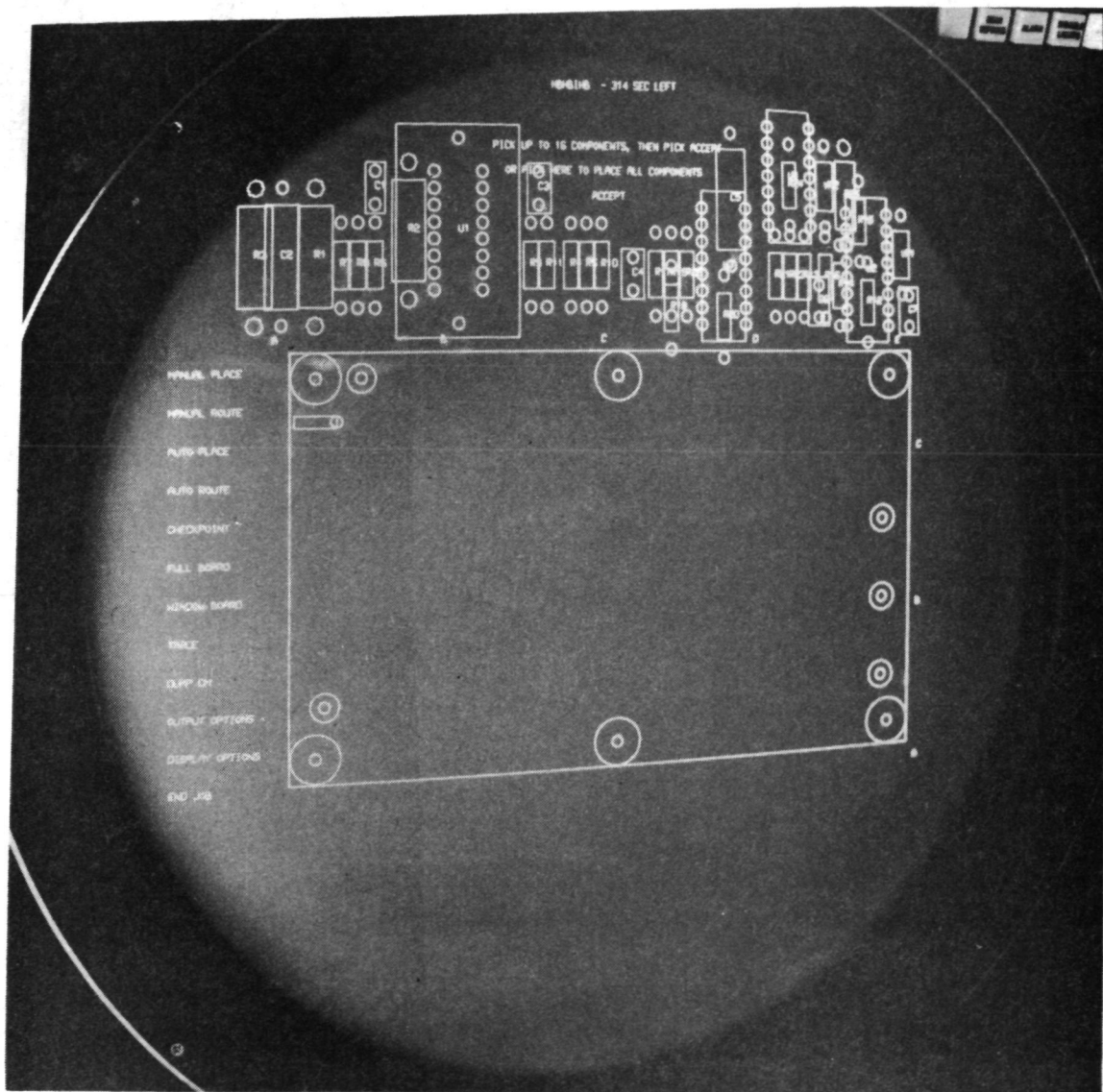


Figure 2. - Display of printed circuit board and components. Prior to the start of packaging, the components are positioned at the top of the screen. The text at the top of the screen indicates the start of the automatic component placement function.

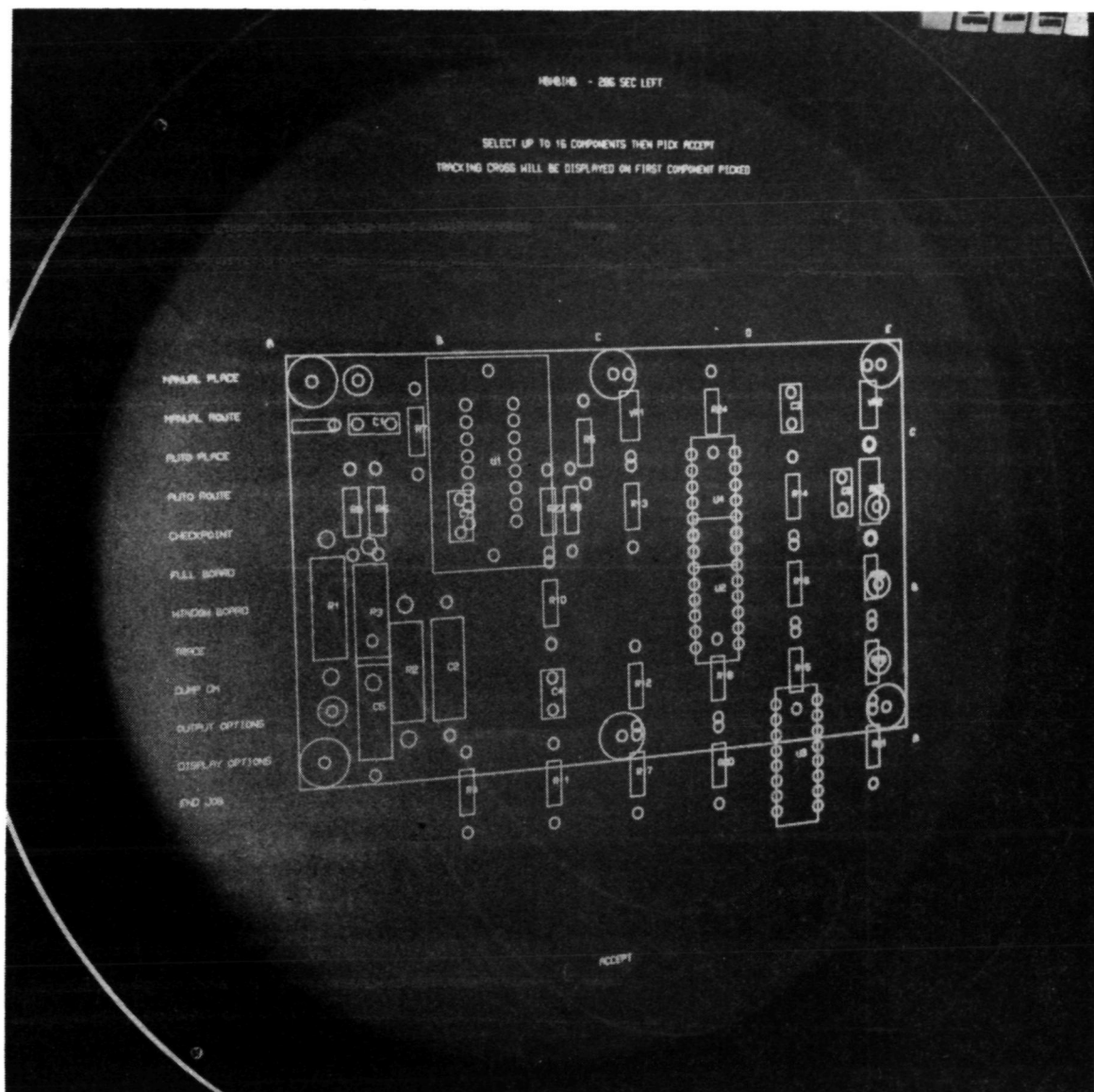


Figure 3. - PCB after completion of automatic component placement. The placement algorithm groups the components into electrically related families but does not optimize the placement to eliminate component overlap. This placement required about 10 seconds of computer time.

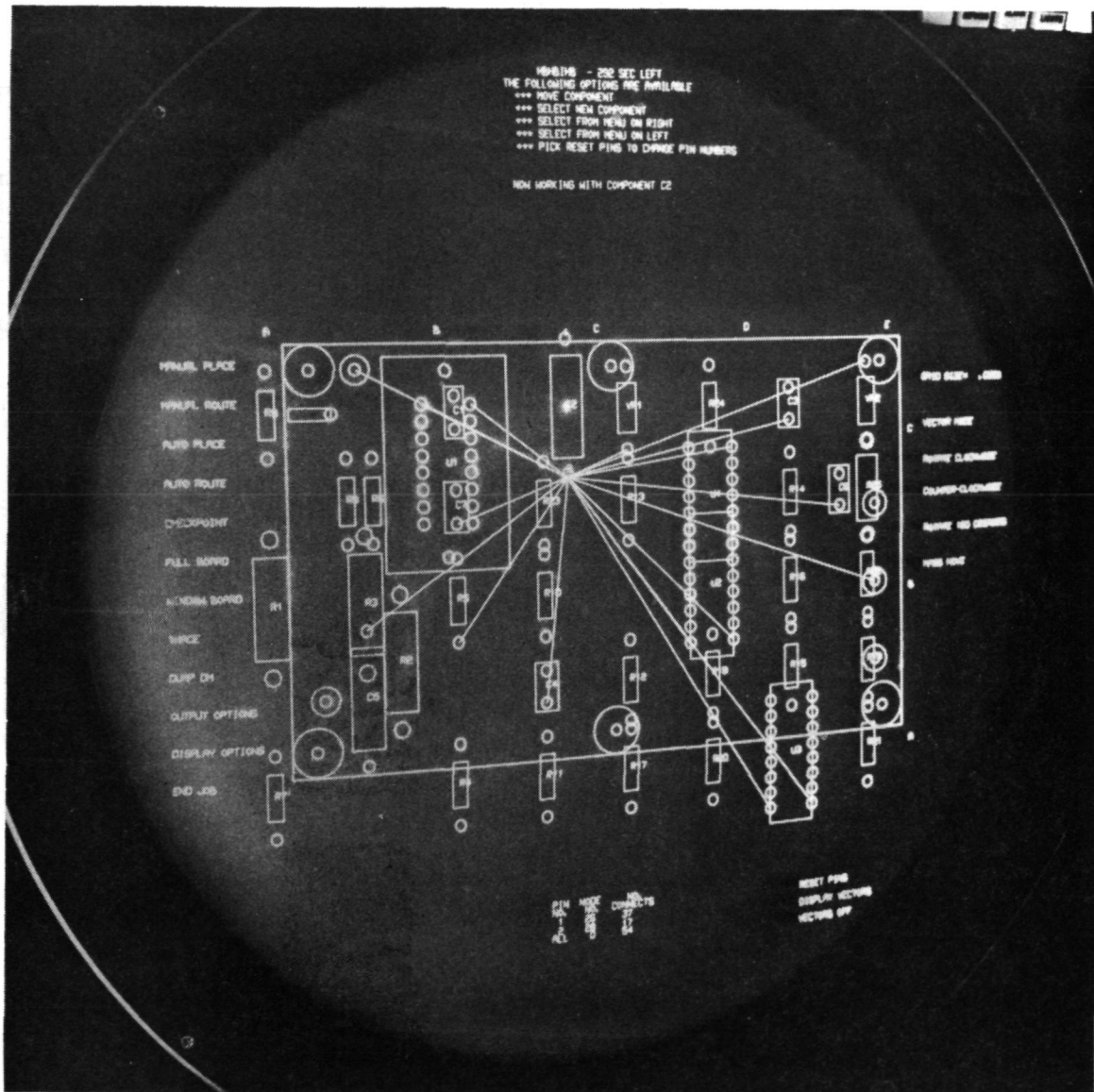


Figure 4. - Vector display during manual component placement. Vectors are displayed from pin 2 of component C2 (the one being moved) to all other electrically common pads.

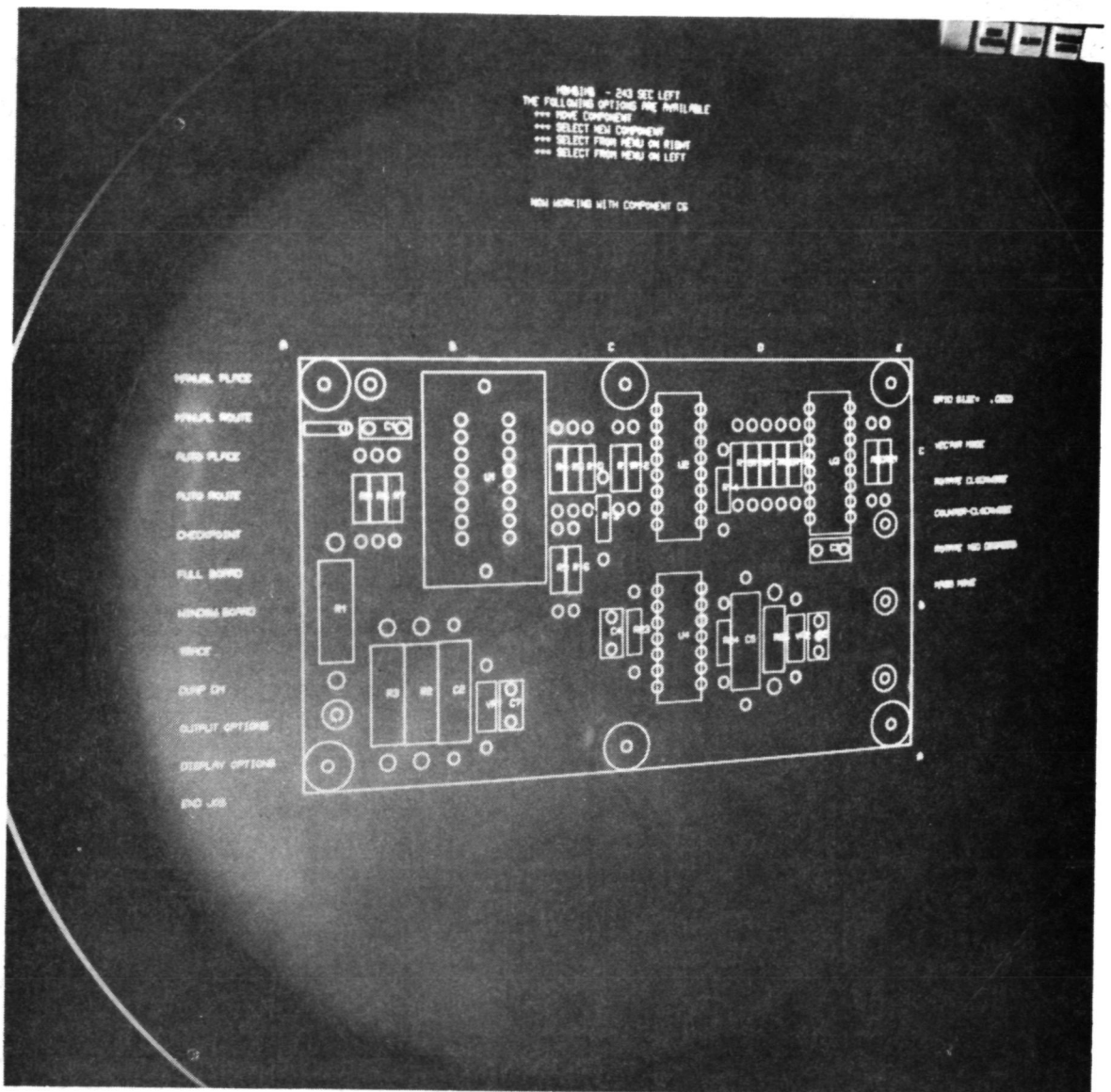


Figure 5. - Final component placement after completion of the manual placement function.

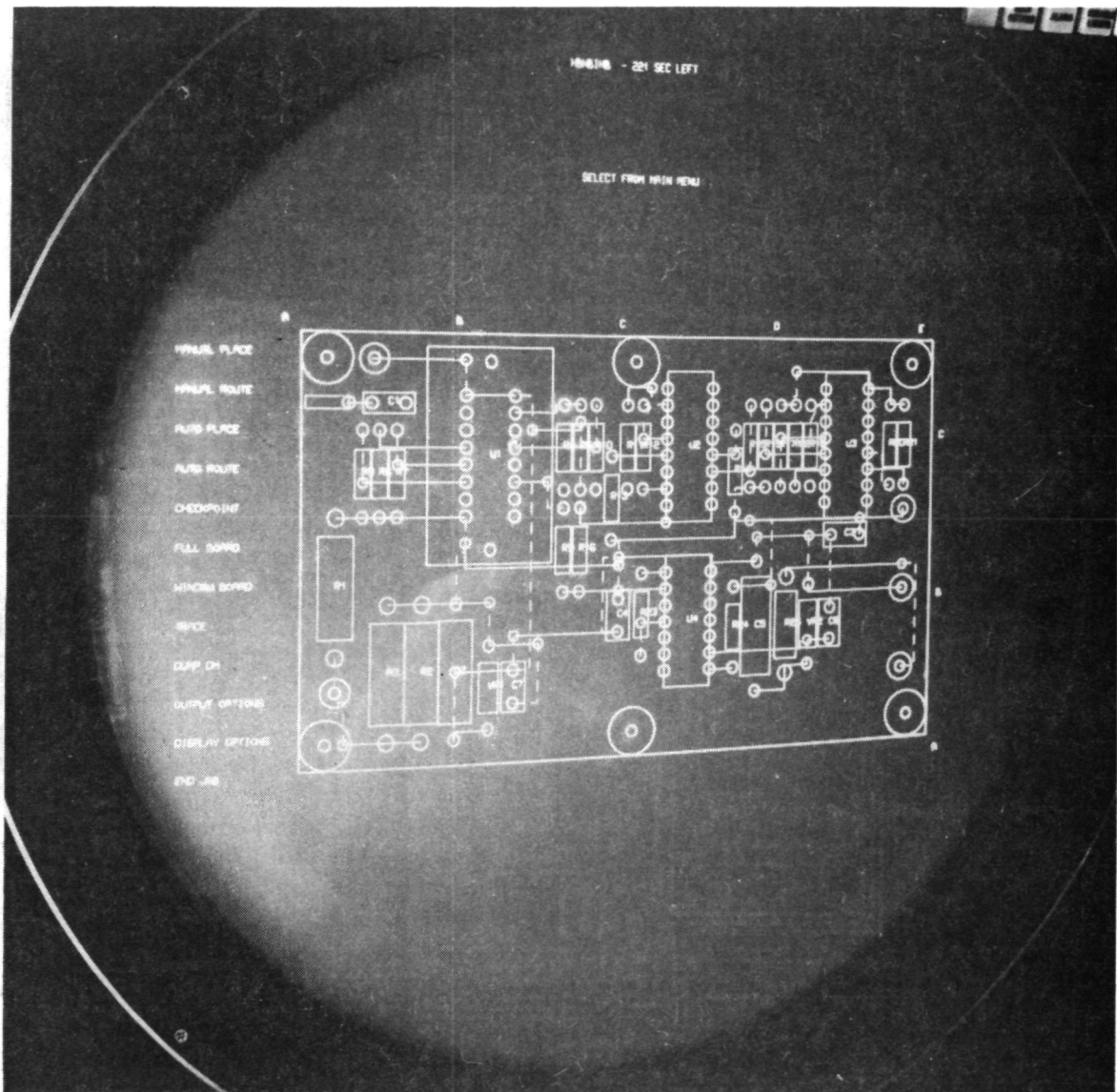


Figure 6. - PCB after completion of the automatic conductor path routing function. The solid paths are on the front side of the board and the dashed paths are on the rear. This route required about 15 seconds of computer time.

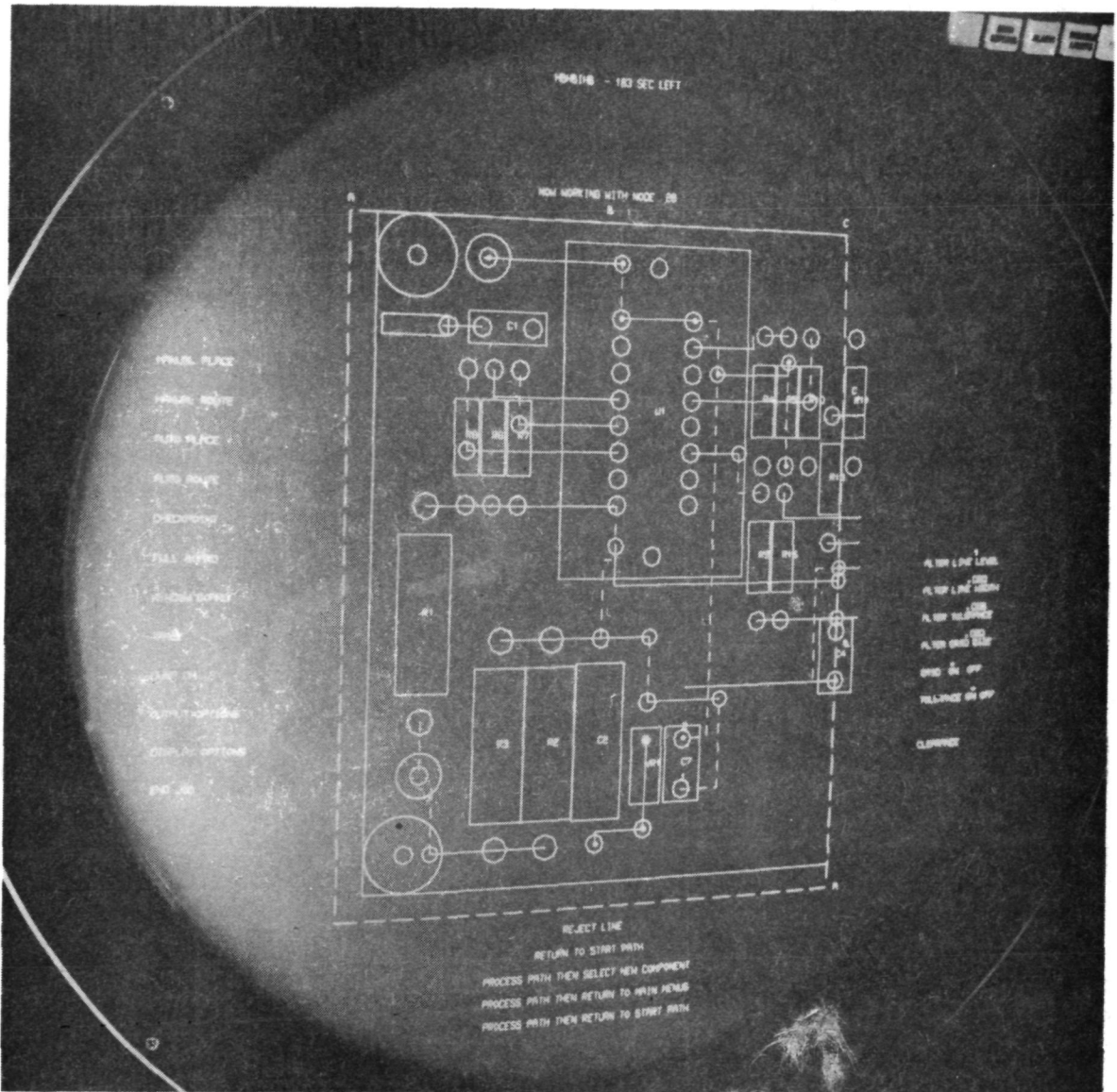


Figure 7. - Window view of the left half of the PCB during the manual conductor routing function. Bright dots appear in conductor pads which are electrically common to the signal net being routed. The conductor path terminating in a bright spot (the tracking symbol) in the lower center of the screen is the path being routed.

LAYER NO. 1

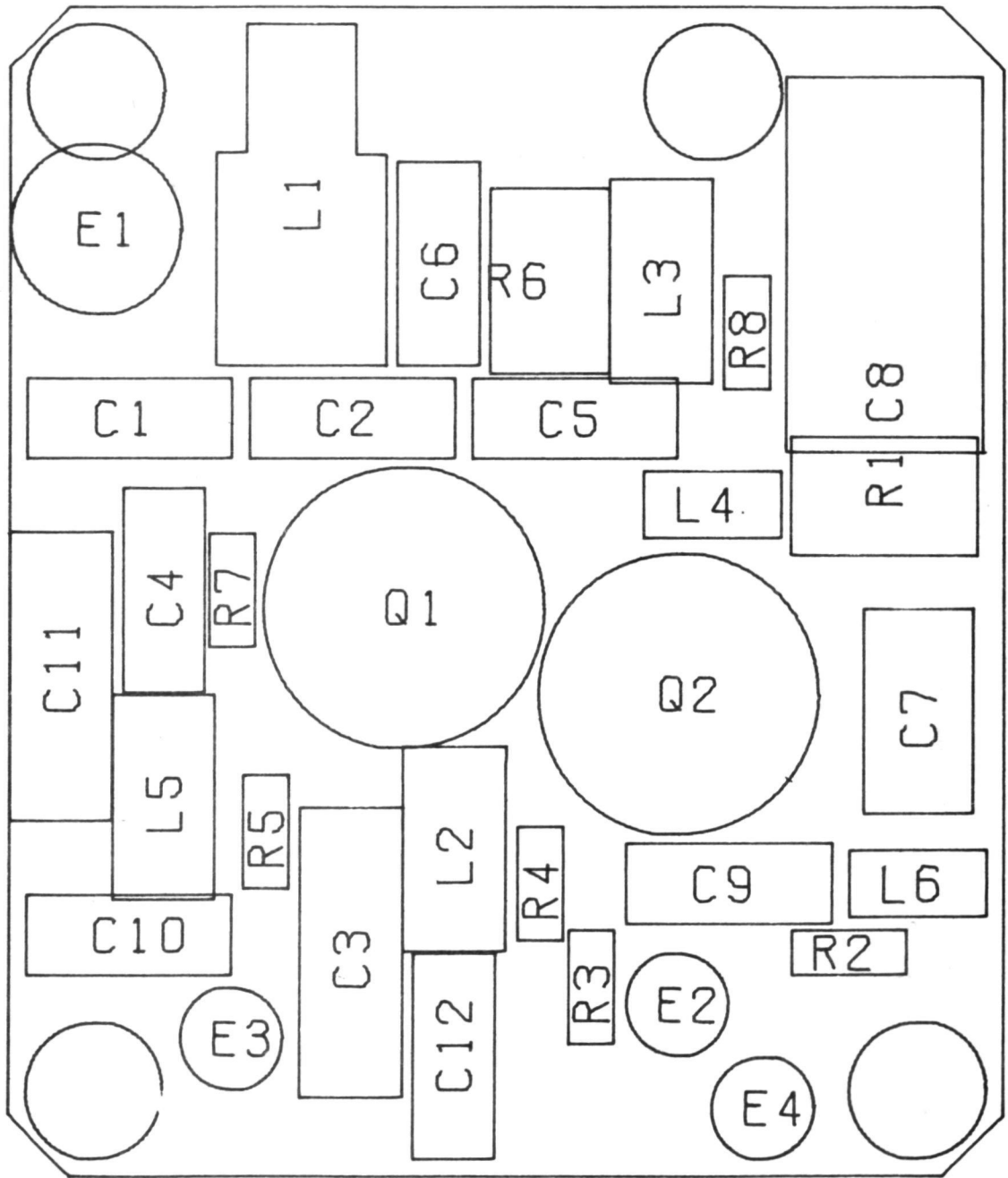


Figure 8. - Calcomp pen plot of a small RF board, 4 times actual size. This is the assembly plot showing the position of each component on the finished board.

LAYER NO. 1

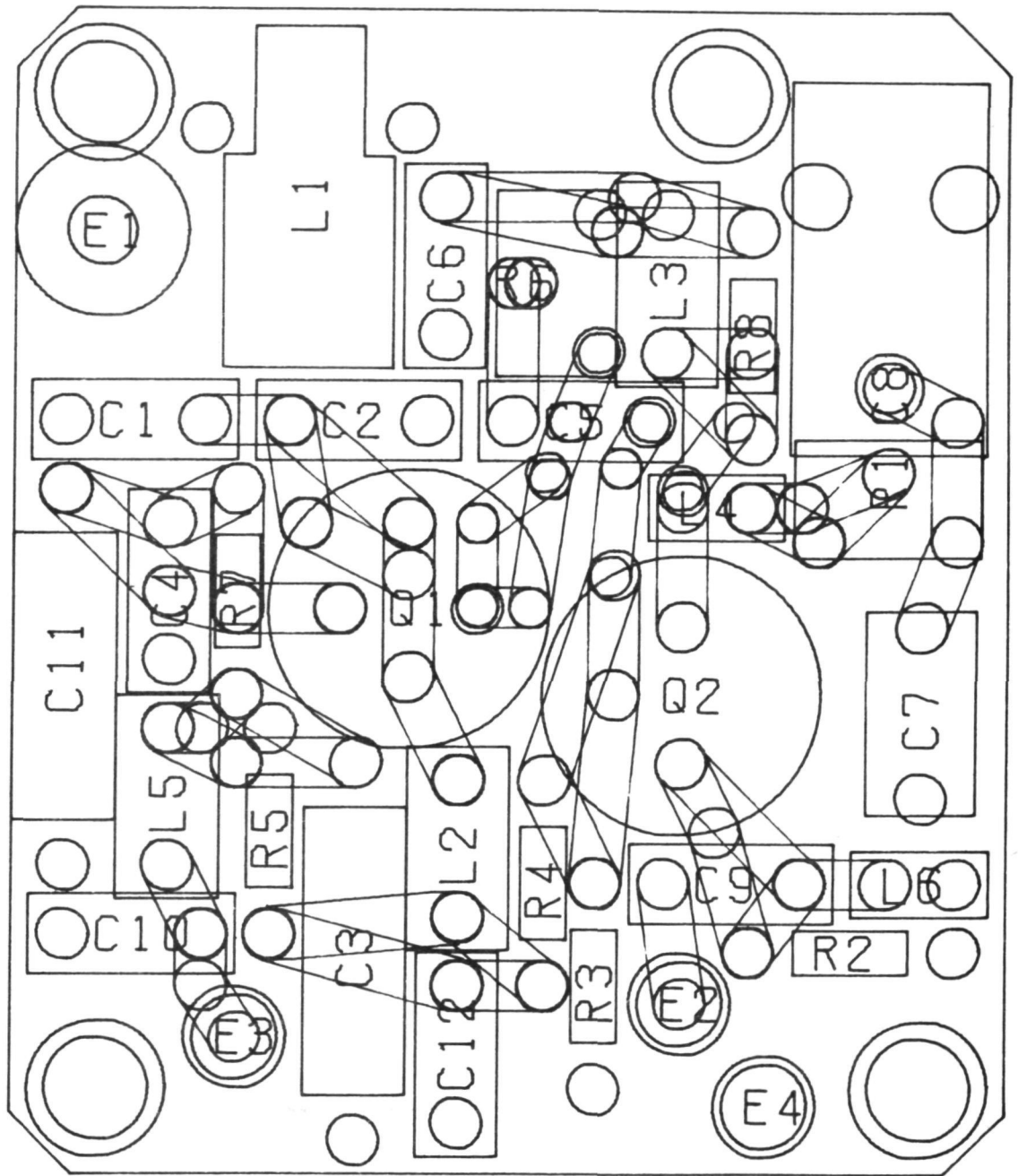


Figure 9. - Calcomp pen plot of the PCB of Figure 8. This is a check plot showing the components, their connection pads and the conductor paths on the front side of the board (layer no. 1). The conductors are plotted showing both edges of the path and circles at the end and turning points. This approximates the appearance of the finished artmaster, since the conductors are drawn with a round light beam.

LAYER NO. 3

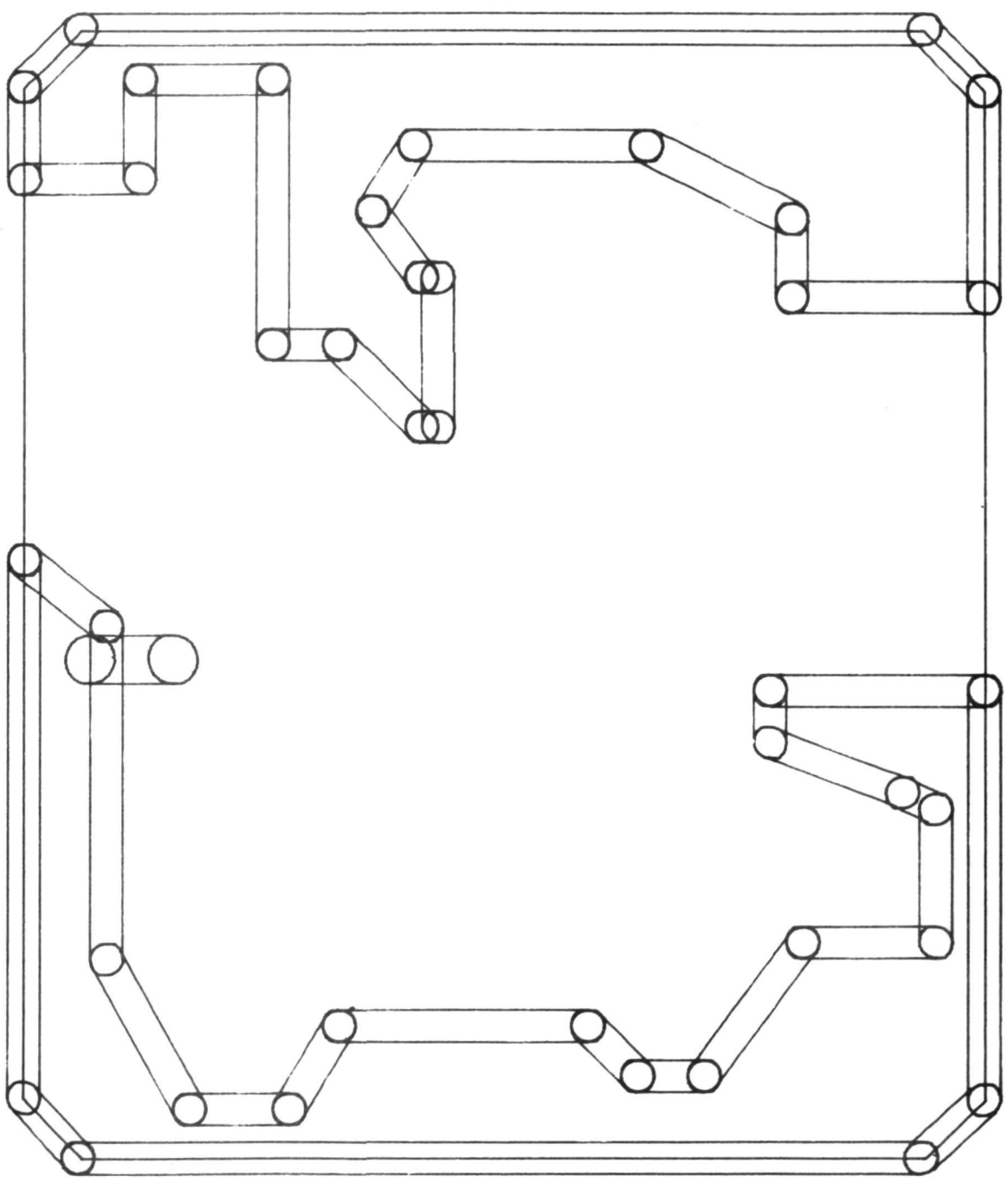


Figure 10. - Calcomp pen plot of the PCB of Figure 8. These conductors serve to outline areas which will become ground planes (areas of metal electrically connected to ground) on the finished board.

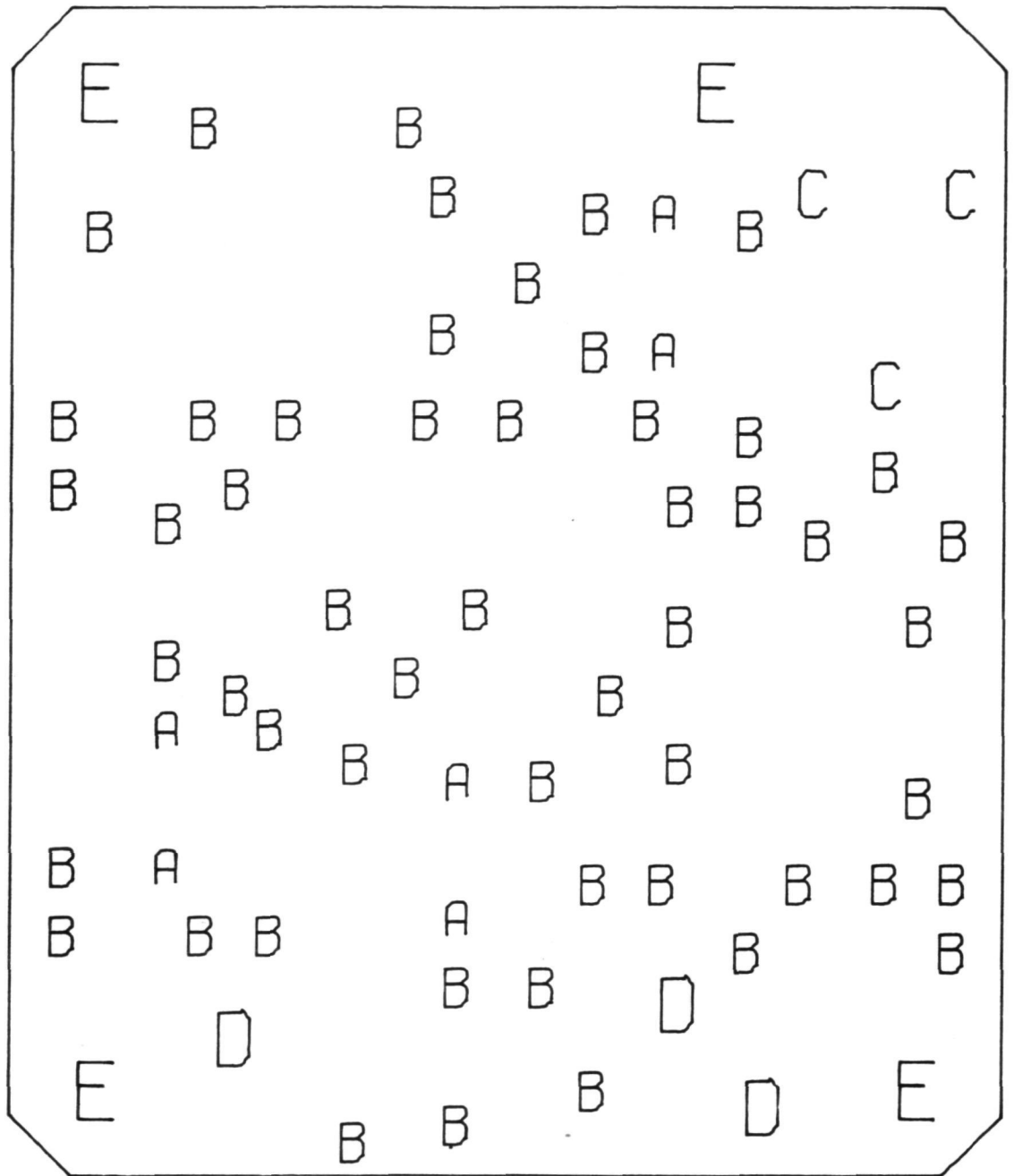


Figure 11. - Calcomp pen plot of the PCB of Figure 8. The letters indicate the size and location of each hole to be drilled.

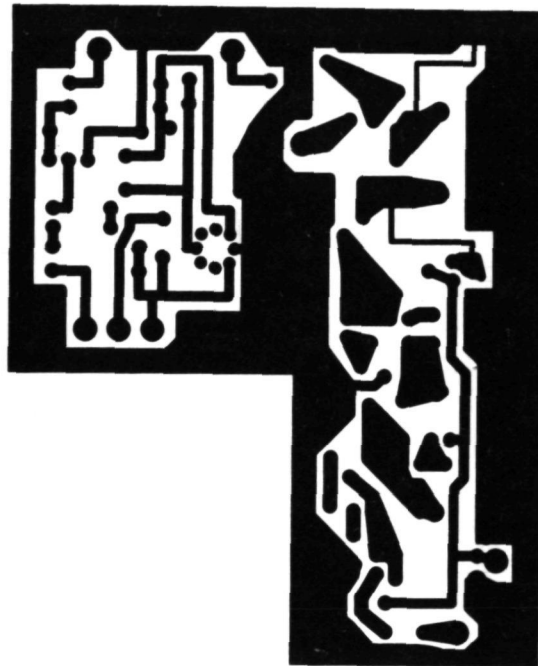


Figure 12. - Artmaster for another RF board, shown actual size. The dark areas represent areas of metal on the finished board. This artmaster (as well as Figures 17 and 18) was produced by a Gerber 1232 photoplotter.

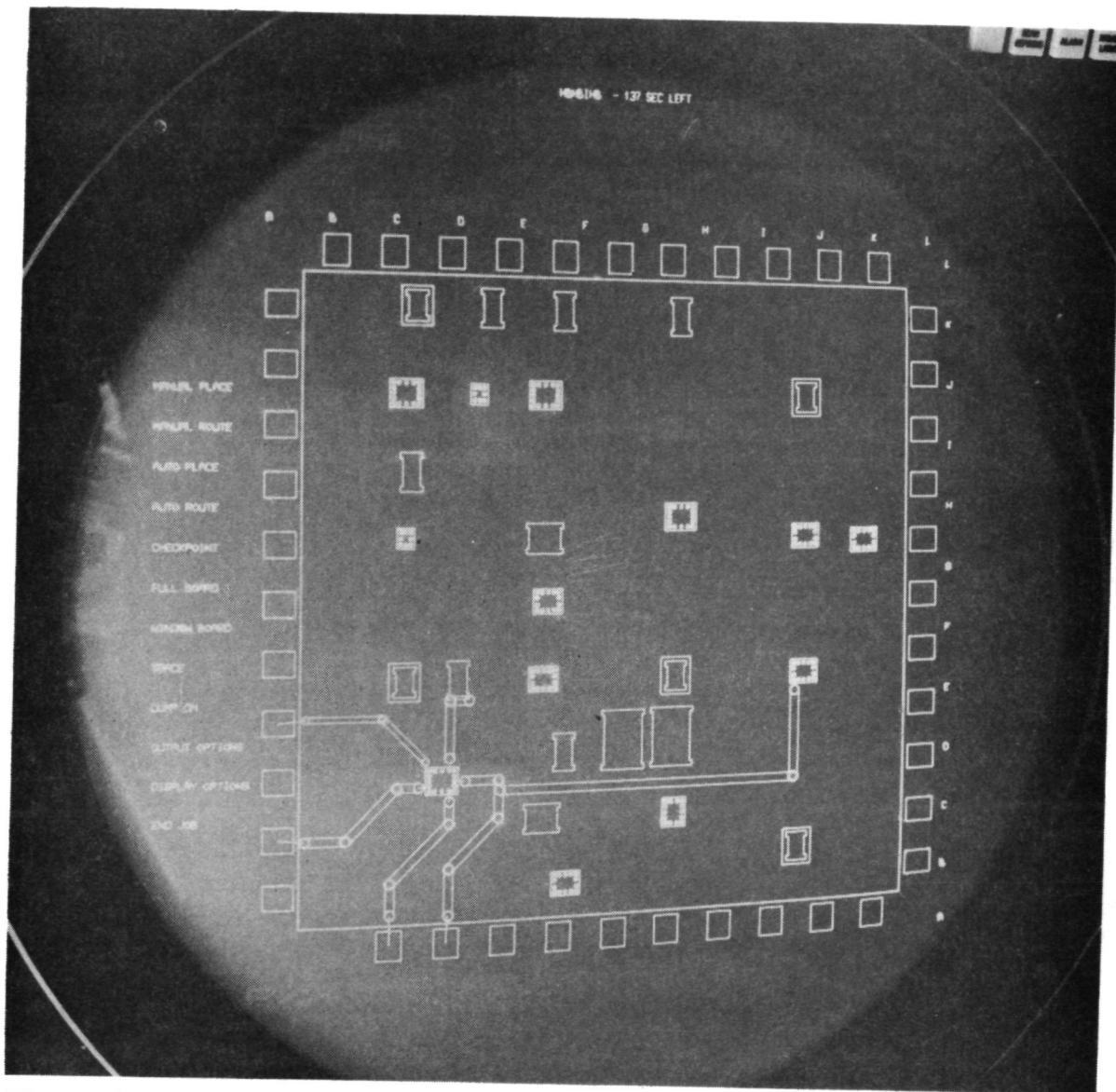


Figure 13. - Display of a hybrid microelectronic device. The components displayed represent integrated circuit chips and thick film resistors. The conductors illustrated include jumper wires (the short, straight lines) and conductors on the substrate. The actual size of the substrate is 2.54 cm (1 in.) square.

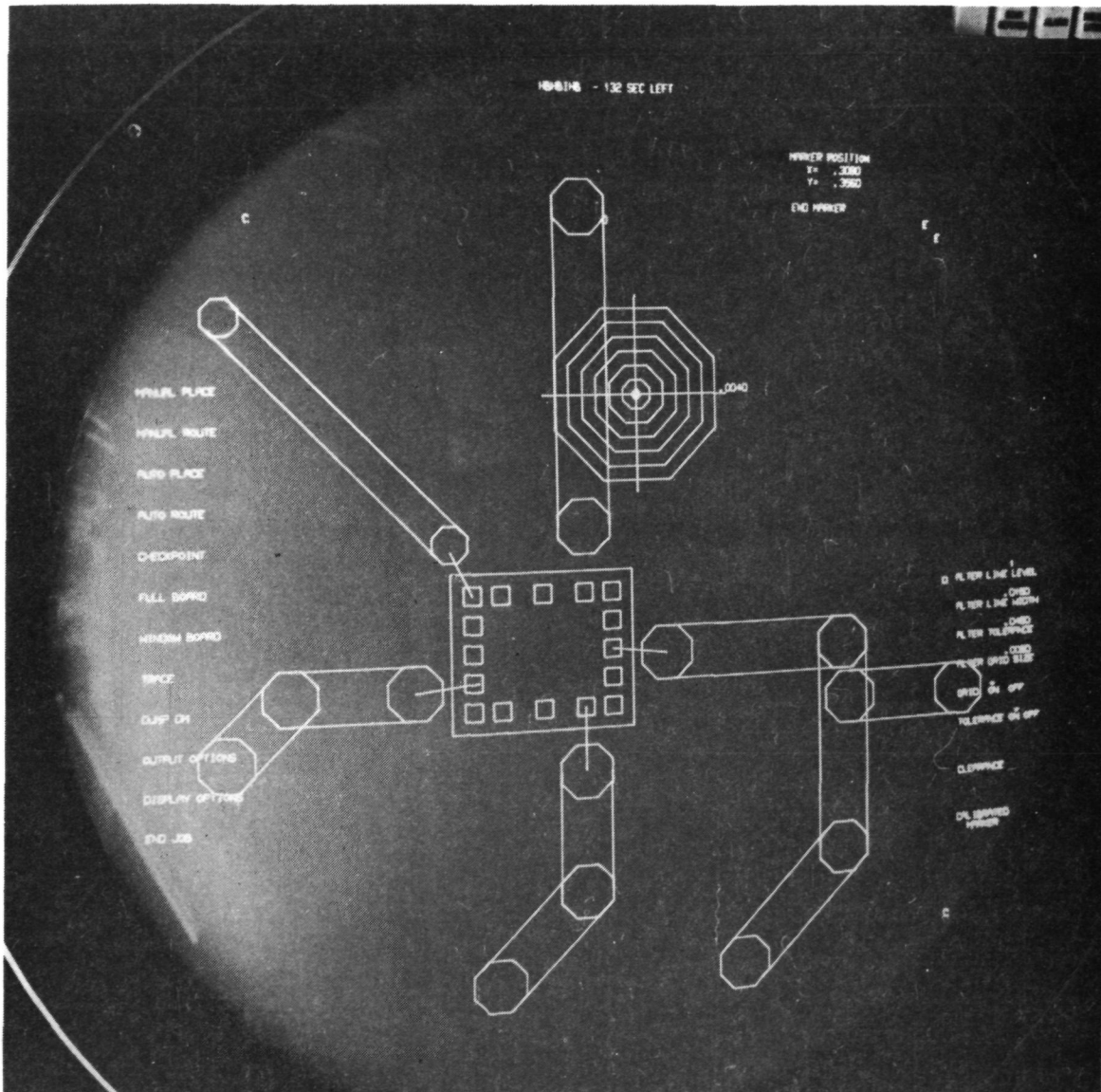


Figure 14. - Window view of lower left corner of the hybrid substrate showing a single integrated circuit (IC) chip. Jumper leads are shown connecting the substrate conductors to the bonding pads on the upper surface of the IC chip. Also shown is the calibrated marker (concentric octagons) for measuring critical dimensions.

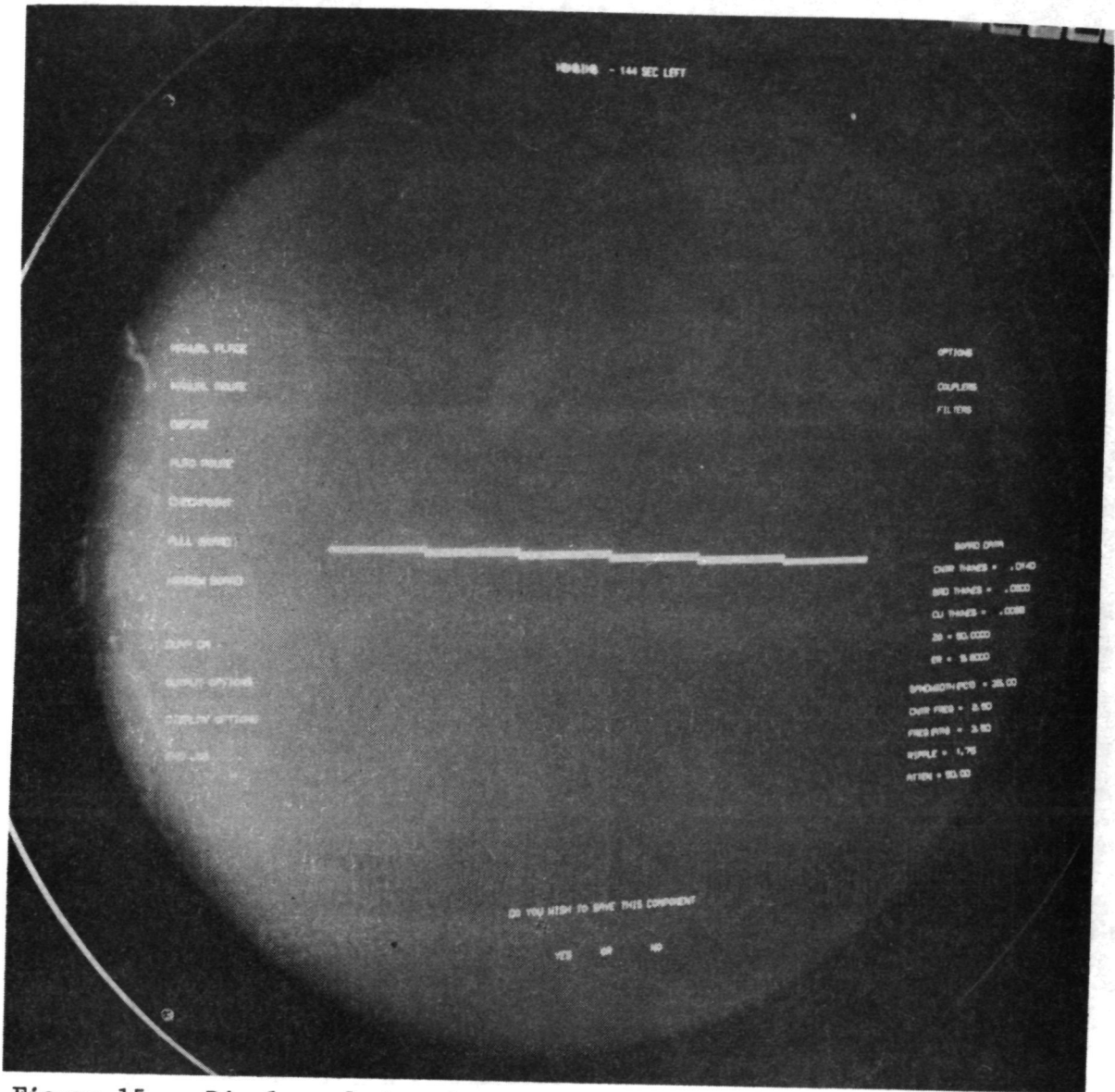


Figure 15. - Display of the microwave stripline program in the component design mode. The performance parameters entered by the designer are listed at the right side of the screen. The parallel line coupled filter displayed at the center was designed to meet those parameters.

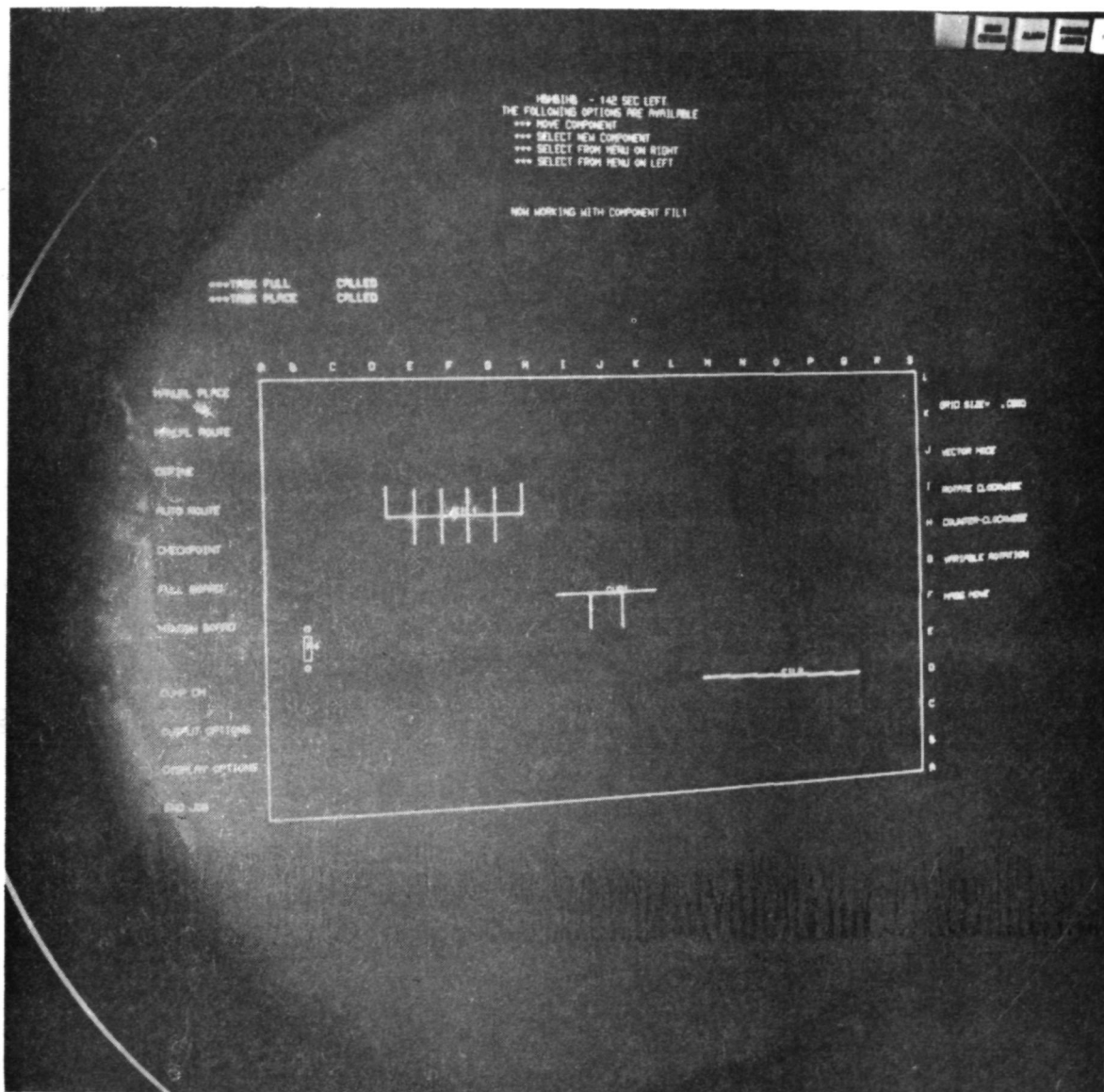


Figure 16. - Display of the microwave stripline program showing two filters and a coupler designed by the program, as well as a discrete resistor. Ultimately the program will allow the engineer to connect the components together with tuned sections of transmission line.

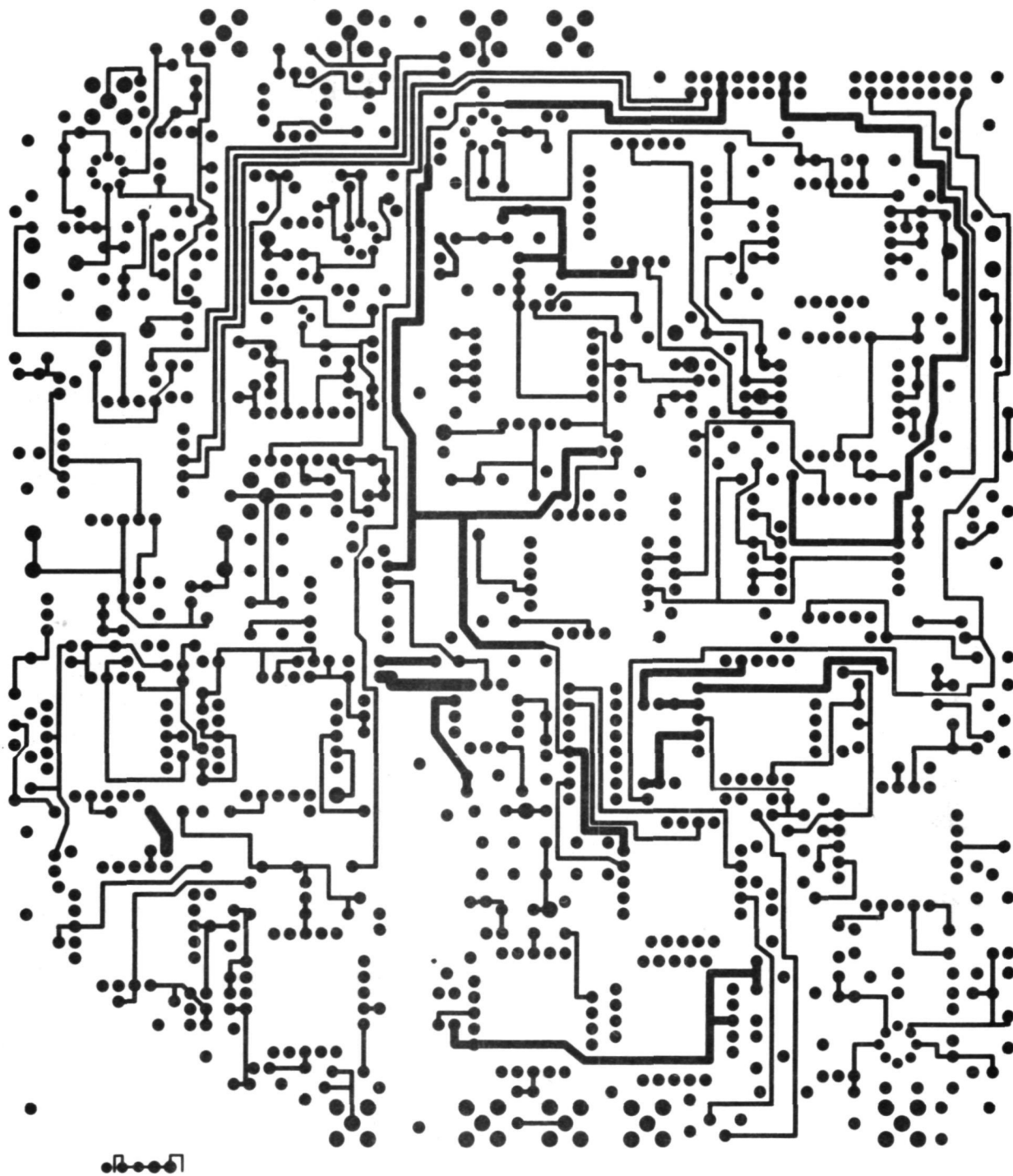


Figure 17. - Artmaster for one layer of a complex PCB, shown actual size.
This layer contains only component pads and conductors.

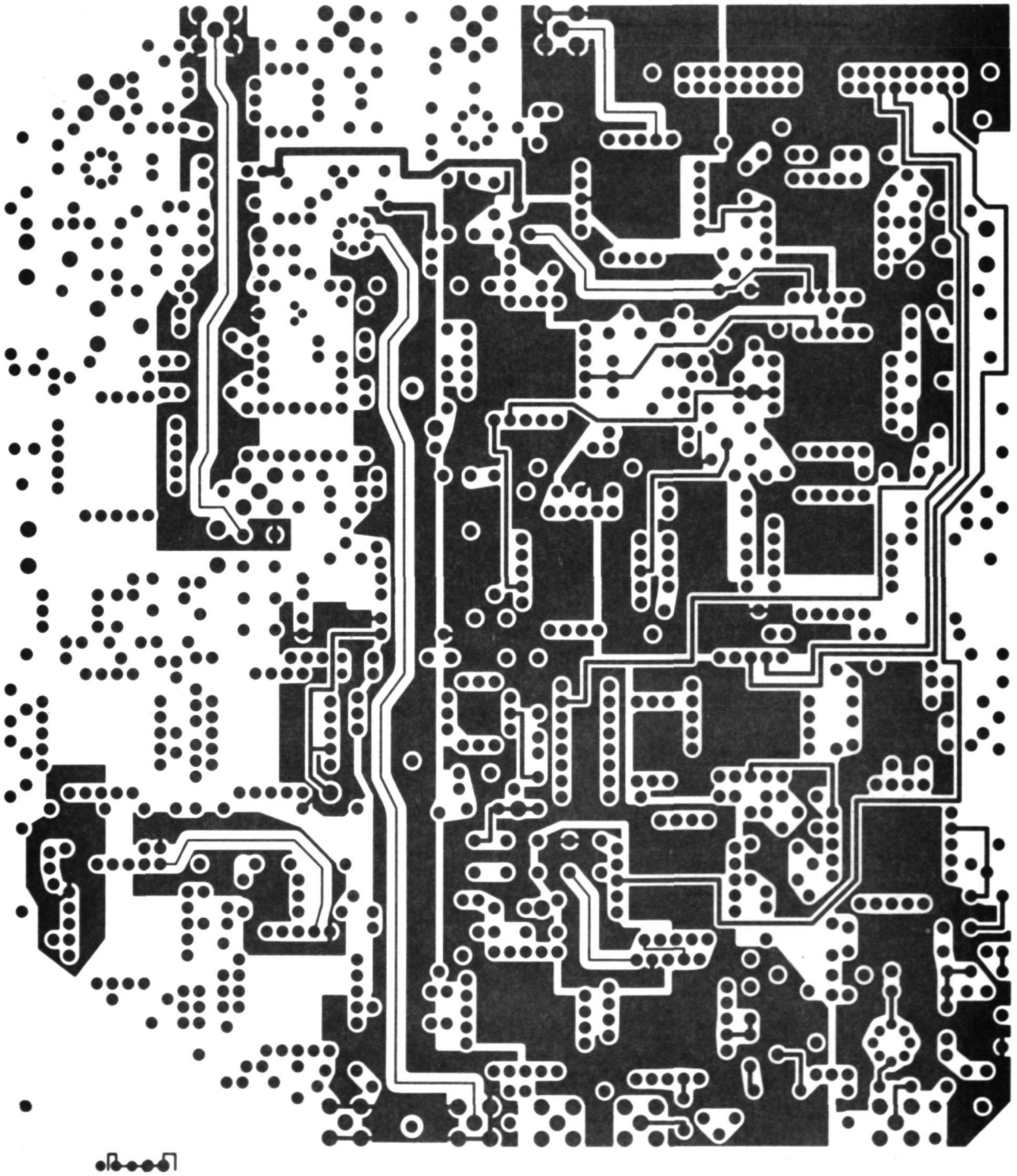


Figure 18. - Artmaster for another layer of the PCB of Figure 17. This layer contains extensive areas of ground planes.