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SOLID STATE TV CAMERA

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FINAL REPORT

CONTRACT NO. NAS 9-14477

PREPARED FOR

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PREFACE

This is the final report on the progress of the project "Solid State Television Camera," being performed by the Astro-Electronics Division of RCA for the Johnson Space Center of the National Aeronautics and Space Administration under Contract NAS 9-14477. The program has been developed around a large area, solid-state Charge-Coupled Imager, 512 x 320, and entails the design, development, test, and delivery of an engineering model television camera. The report covers work performed from January, 1975 through November, 1975 and responds to the documentation requirements set forth in Article II of the contract.

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I. INTRODUCTION AND SUMMARY

The Astro-Electronics Division (AED) of RCA submits to NASA/JSC this final engineering report covering the engineering design, development and test of an engineering model Solid-State Television Camera under Contract No. NAS 9-14477.

The primary purpose of this contract was to design, build, and test a solid state television camera using a new charge-coupled imaging device. An RCA charge-coupled device arranged in a 512 by 320 format and directly compatible with EIA format standards was the sensor selected for this purpose. This is a three-phase, sealed surface-channel array that has 163,840 sensor elements, which employs a vertical frame transfer system for image readout.

Camera development was focused on attaining desired camera performance and operational features that are critical in space flight applications. The vertical frame transfer principal employed for the operation of the charge-coupled imager (CCI) permitted attractive operational features, including anti-blooming and automatic exposure control. Test results obtained attest to an automatic light control range of 50:1 and a total operating light range including lens iris adjustment of greater than 5000:1.

Included in this report are test results of the complete camera system, circuit description and changes to such circuits as a result of integration and test, maintenance and operation section, recommendations to improve the camera system, and a complete set of electrical and mechanical drawing sketches.

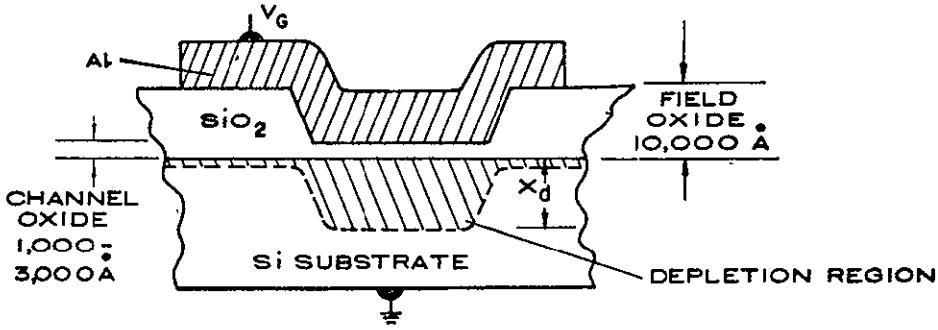
II. TECHNICAL DISCUSSIONS

A. Theory and Operation

1. Theory of CCD Operation

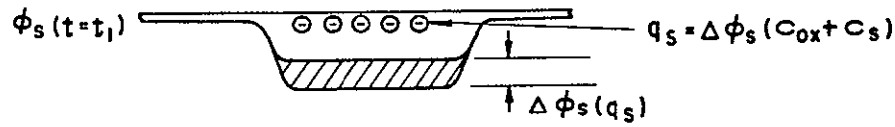
Since a CCD is physically a linear array of closely spaced MOS capacitors, it is important to understand the MOS capacitor and how the surface potential V_s (the potential at the Si-SiO_2 interface relative to the potential in the bulk of the silicon) depends upon the various parameters involved.

Figure 1 shows a cross-sectional view of an MOS capacitor with a p-type silicon substrate. When a positive step voltage is applied to the gate of such a structure, the majority carriers (holes) are repelled and respond within the dielectric relaxation time. This results in a depletion region of negatively charged acceptor states near the surface of the silicon. The applied gate voltage, V_s, is dropped across the series combination of the oxide and the depletion region in the silicon.



(a) Cross-Sectional View

(b) Electrical Potential at Si-SiO_2 Interface Just After Positive Voltage is Applied to the Gate



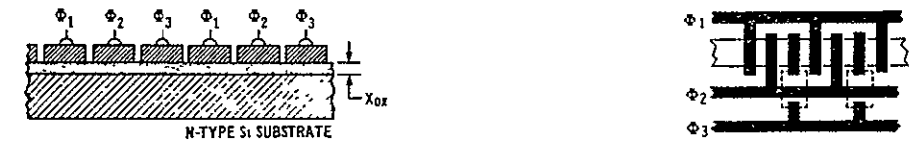
(c) Depth of Potential Well is Reduced as Negative Charge Accumulates

Figure 1. MOS Capacitor With P-Type Silicon Substrate

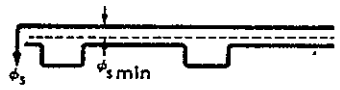
Just after the step voltage is applied to the gate and in the absence of signal charge, Q_{sig}, the silicon conduction band at the surface is well below the equilibrium Fermi level, and electrons (the minority carriers) will tend to gather there. However, it takes a rather long period of time for thermally generated minority carriers to accumulate in sufficient numbers to return the system to thermal equilibrium. Measured thermal relaxation times for MOS capacitors range from 1 to 100 seconds, in good agreement with the predicted values, assuming bulk thermal generation of minority carriers. When minority carriers do accumulate at the surface, they start to create an inversion layer which resides within 100 Å of the interface. This negative charge tends to reduce V_s. When V_s goes to zero, no more charge can be accumulated or stored in the potential well.

Thus, the following fluid model of the MOS capacitor emerges: A potential well for minority carriers can be created by applying a step voltage to the gate, and this well will take a relatively long period of time to accumulate charge thermally. For times much shorter than this thermal relaxation time, a potential well exists at the surface, and the depth of this well can be altered by changing the gate voltage. When minority carriers are introduced as signal charges in the potential well, they tend to reduce the depth of the well much like fluid filling a container.

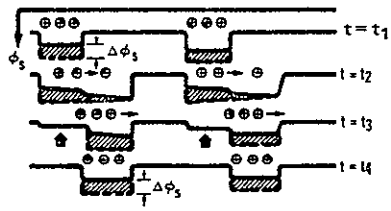
A three-phase CCD is just a line of these MOS capacitors spaced closely together, with every third one connected to the same gate, or clock voltage, as shown in Figure 2. If a higher positive voltage is applied to the Phase 1 clock line than to Phases 2 and 3, the surface potential variation along the interface will be similar to that shown in Figure 2. If the device is illuminated by light, a charge will accumulate in these wells. The charge can also be introduced electrically at one end of the line of capacitors from a source diffusion controlled by an



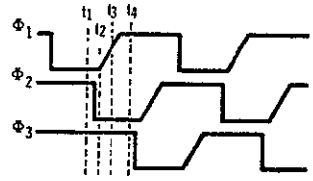
(a) CROSS-SECTIONAL VIEW



(b) SURFACE POTENTIAL PROFILE WHEN NEGATIVE VOLTAGE IS APPLIED TO PHASE 1 GATES ONLY



(c) MOVEMENT OF CHARGE AS VOLTAGE IS APPLIED TO PHASE 2 (t_2) AND REMOVED FROM PHASE 1 (t_3)



(d) WAVEFORMS OF THE PHASE VOLTAGES

Figure 2. Operation of a Three-Phase CCD Shift Register Consisting of Closely Spaced MOS Capacitors

input gate. To transfer this charge to the right to a position under the Phase-2 electrodes, a positive voltage is applied to the Phase-2 line. Initially, the potential well there goes deeper than that under a Phase-1 electrode (which is storing the charge), and the charge tends to move over to the Phase-2 electrodes.

The capacitors have to be close enough so that the depletion layers overlap strongly and the surface potential in the gap region is a smooth transition from the one region to the other. Next, the positive voltage on the Phase-1 line is removed to a small positive dc level, enough to maintain a small depletion region, increasing the surface potential under the Phase-1 gates in the process. Now, the Phase-2 wells are deeper, and any charge remaining under the Phase-1 gates spills into the Phase-2 wells. Most of the charge now resides under the Phase-2

gates one third of a stage to the right of its original location. The charge is prevented from moving to the left by the barrier under the Phase-1 gates. A similar process moves it from Phase 2 to Phase 3 and then from Phase 3 to Phase 1. After one complete cycle of a given clock voltage, the charge pattern has moved one stage (three gates) to the right. No significant amount of thermal charge accumulates in a particular well because it is continually being swept out by the charge transfer action.

The charge being transferred is eventually shifted into a reverse-biased drain diffusion, and it is returned from there to the substrate. The charging current required once each cycle to maintain the drain diffusion at a fixed potential can be measured to determine the signal magnitude (current sensing). Alternatively, a resettable floating diffusion (or floating gate) which controls the potential of a MOSFET gate can be employed (voltage sensing). This is the method utilized for the RCA-CCI.

2. The Charge-Coupled Imager

a. Operation

A CCD can be used to move charge packets over long distances of silicon without undue signal loss or distortion. This analog shift register capability is unique to the CCD. In the imaging application, the CCD is also used to sense the light and to collect and store the optically generated charge carriers (normally electrons) during the light integration period. This is done by placing a positive voltage on one of the phases for the duration of the integration period. This creates an array of potential wells which attract and store the photo-electrons. At the end of the integration period, a charge pattern exists in the register which represents the time integral of the light pattern incident on the devices. The light can be introduced from the top of the device through the gating structure, or from the back side if the substrate is thin.

At the end of the integration period, the CCD clocks are cycled in a manner to shift the charge packets serially to a single output point. A single CCD register operated in this manner constitutes a line array imager.

Several approaches are possible for the use of charge-coupled devices in making area image sensing arrays. The area array that will be used with the proposed camera is called the vertical frame transfer system. As shown in Figure 3, there are three functional regions which make up the array: the photosensitive area (A register), the temporary storage area (B register), and the output (C register). The A and B registers each consist of many adjacent vertical CCD channels which are driven in parallel by the same set of gates. ("A" gates are driven separately from "B" gates).

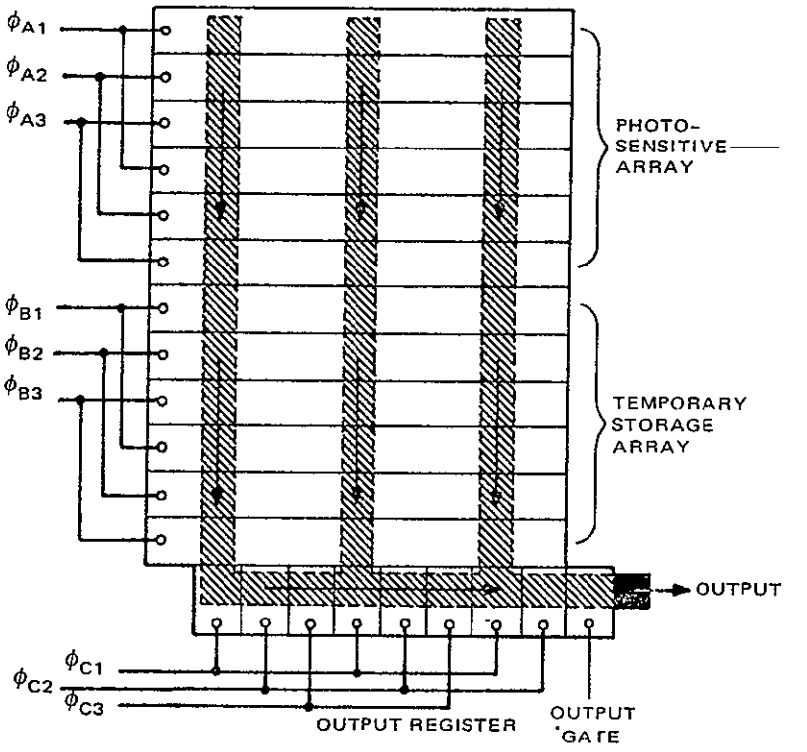


Figure 3. Vertical Transfer System With Separate Store

The optical image is detected during each field integration time in the photosensitive array (with the "A" clock voltages held fixed). During the vertical blanking interval, the detected charge pattern in the photosensitive elements are shifted to the temporary storage array. During the active vertical interval, the information is shifted in parallel one line at a time from the storage array to the output register. This output register is a line of CCD elements equal to the number of horizontal elements in the area array.

The information in the three-phase output register is shifted serially to the output by a high-speed clock signal via a floating diffusion element and an on-chip field effect transistor (FET). The clock rate is established so that all of the elements in the register are read out during the normal active portion of a line.

b. Interlacing

To be compatible with standard television scanning, an imager must be capable of interlace, the vertical interleaving of every other horizontal line in successive field times. In a charge-coupled imager, in addition to reducing flicker, interlacing increases the resolution capabilities of the device.

Consider a three-phase vertical frame transfer CCI (see Figure 3), where three gates are required to shift one charge packet, and the charge can be stored under any one gate during the integration time. Note that the built-in structure for storage is three times that for transfer. Interlacing in a three-phase CCI is illustrated in Figure 4. During Field 1 integration, Phase 1 electrodes are maintained at a higher potential than Phases 2 or 3. Thus, the center of charge collection is under the Phase 1 gates. Note, however, that the charge generated under the Phase 2 and 3 gates is also collected under Phase 1. Since the Phase 2 and 3 gates are biased into depletion, recombination is low and photogenerated electrons will diffuse to the Phase 1 wells. All light-generated carriers are collected.

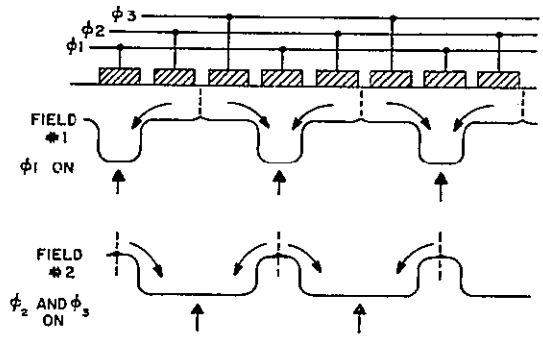


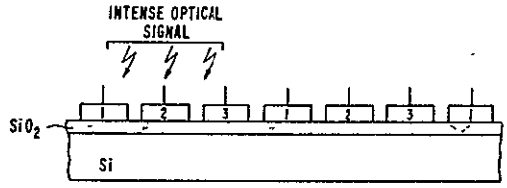
Figure 4. Cross-Sectional View of Three-Phase Vertical Transfer Imager Indicating How Interlace Can Be Accomplished

During Field 2, Phases 2 and 3 are kept higher so the center of charge collection is moved by one-half of a cell as indicated by the arrows in Figure 4. Thus, the light intensity is sampled in successive fields at centers shifted by one-half of a CCI element consisting of three gates. This effectively doubles the sampling spatial frequency from $2\pi/L$ to $4\pi/L$ and, correspondingly, reduces the distortion introduced by foldover effects. The net result is about double the single-field resolution. In this way, a three-phase vertical transfer system with N three-gate resolution elements in the imaging region in the vertical direction is capable of almost 2N television lines per picture height. However, in the horizontal direction, one must have one channel for each resolution element. In the vertical transfer system, interlacing results in increased resolution with all light collected and an integration time for each field of 1/60 Second.

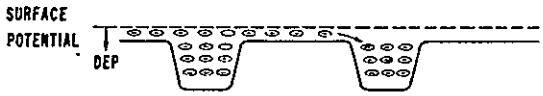
c. Blooming Control

Since CCDs are designed to permit motion of minority carriers over long distances without recombination, excess charge due to point light overloads will spread down the CCD channels and saturate large regions of the device. This effect is known as blooming and is also observed in silicon vidicons. Several techniques have been devised and successfully operated in line arrays for controlling blooming in CCDs. The method of blooming control utilized for the RCA-CCI is designated as the accumulation method.

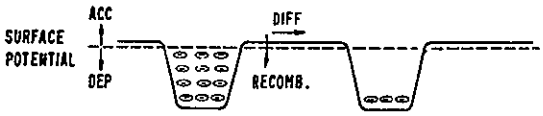
This is an operational method that does not require an additional structure to be built into the sensor. The concept of the accumulation mode is illustrated in Figure 5 for the case of a three-phase CCD with diffused channel stops. The standard mode and the accumulation mode are illustrated in the two surface potential diagrams. In the standard mode of operation, two phases



(a) Cross-Sectional View of a Three-Phase Device



(b) Normal Mode of Operation



(c) Accumulation Mode of Operation for Blooming Control

Figure 5. Normal and Accumulation Modes of Operation of a Charge-Coupled Imager

are biased into slight depletion, and the No. 2 electrodes are biased so as to form a deep depletion region for the collection of photogenerated carriers. In the case of an intense optical overload, the photogenerated carriers will fill up the wells and then spill down the channel into adjacent cells.

In the accumulation mode, the No. 1 and No. 3 electrodes are biased so that the underlying interface is in accumulation. This establishes a barrier and prevents the excess minority carriers from spilling freely down the channel, since they will tend to recombine with holes in the accumulation regions.

d. Exposure Control

The CCI is normally operated at maximum sensitivity by setting the voltages on the A (photosensitive) register to establish charge accumulation for the entire active vertical interval. During this interval, the potential wells continue to accumulate charges for later transfer to the B register. If the establishment of the well is delayed, the exposure interval is shortened.

This effect may be used to advantage to shorten the effective exposure time and prevent overload on brighter signals and has been incorporated into the camera design as part of an automatic light control loop. A limitation in shortening the accumulation time is imposed by smear effects introduced by the optical integration in the A register during the vertical blanking interval, when the charge is being transferred from the A to B register. For this camera design a 10 to 1 reduction in exposure was found to be acceptable without significant smear contribution.

3. Operational Sequence

a. Optical Integration

The photosensitive imaging array is exposed to the optical scene, the duration of exposure determining the system sensitivity. For an NTSC format monochrome television system, the active field

time is 1/60 second less the vertical blanking interval of 0.08V maximum (1.33 ms). The exposure time occurs during the active field time and is thus:

$$T_{exp} \leq 15.3 \times 10^{-3} \text{ second}$$

The exposure interval will be controlled by a closed-loop feedback scheme to vary the system sensitivity, as explained in Section II-B-1. Scene information is imaged on all 256 x 320 elements during this time interval.

b. Transfer to Storage Array

Exposure to the scene is followed by a transfer operation during the vertical blanking interval in which the charge pattern is read into the CCI 256 x 320 storage array. The transfer operation is initiated by the vertical drive signal from the TV sync generator and is concluded after a count of 268.

Note that a suitable vertical field of information can be generated from less than 262.5 lines of information contained in the NTSC signal. Actually, all that is required is a minimum of 241.5 lines of active information which is achieved by the use of the synchronized 15,750 Hz line rate signal and the vertical drive signal from the television generator. The additional lines of information occur during the vertical blanking interval and are readout of the CCI as useful-scan data. It may be feasible in the future to use this information as a means of controlling the insertion of "fat-zero" into the CCI or as a measure of average dark current changes with temperature.

c. Interlace Operation

The sequence of exposure and transfer to the storage array is controlled to provide a 2:1 interlace of picture lines. Two fields at the rate of 60 fields per second will generate one complete frame of information of 1/30 second. The spatial

extent and cell structure of each element in the vertical direction will be used as the basis of interlace. Interlace operation will be controlled by alternately shifting the electrical bias on the Phase 2 and 3 gates of the CCI imaging elements between successive fields. Identification of the odd field is available as an output from the television sync generator to control this mechanism.

d. Readout

The final operation for generating a suitable video signal is to read the information out of the CCI storage array. This operation begins at the end of the vertical blanking interval and entails the parallel shift of a single line of scene information from the storage array into the CCI output shift register. Parallel shifting of each line takes place during the horizontal blanking interval. The lines are then serially readout of the output register during the remaining active horizontal line time. Video readout requires two timing signals. One is the line rate of 15,750 Hz, and the other is the high speed readout clock which operates the serial output register. The line rate clock signal is available directly from the television sync generator output and the high speed readout clock is generated from a master oscillator.

e. Display Format

The CCI imaging array contains 320 horizontal elements on 1.2 mil centers and 256 vertical elements on 1.2 mil centers, but nominally only 242.5 vertical elements are actively utilized. This provides a horizontal dimension of 384 mils and a vertical dimension of 291 mils. An aspect ratio of 4:3 is thus achieved, the image format diagonal being 482 mils (12.2 millimeters).

4. Camera Operation

a. Camera Block Diagram

A block diagram of the basic camera system is shown in Figure 6. Scene luminance is collected and focused by the lens onto the photosensitive area of the 512 x 320 CCI array. Appropriate timing signals, generated by the timing and logic module, control the exposure time and generate a readout signal to the video processing circuits. A synchronization generator that provides all the necessary EIA standard waveforms operates the television camera in a manner which produces a properly formatted NTSC monochrome video signal at its output. All clocking signals that control the timing and logic circuitry as well as the sync generator are provided by a crystal-controlled master oscillator, ensuring proper synchronization throughout the logic circuitry.

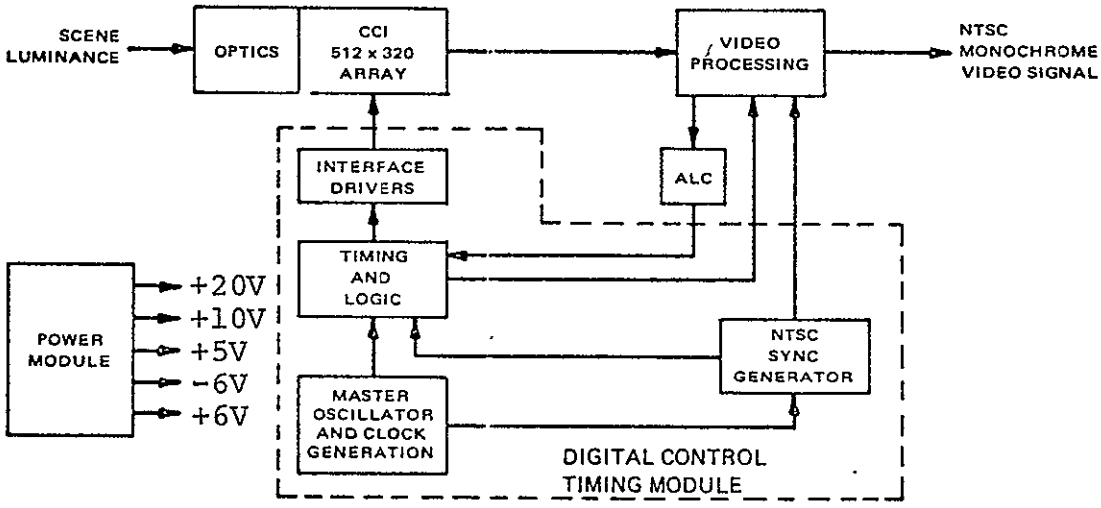


Figure 6. Simplified Block Diagram of CCI Television Camera

b. Clocking Requirements

The specified horizontal line rate, f_h, of 15,750 Hz results in a time per line of f_h = 63.492 microseconds. The part of this time allotted to blanking and horizontal sync is established from the sync generator as 10.91×10^{-6} second for an active video time of

$$t_a = 52.58 \times 10^{-6} \text{ second}$$

During this time interval the full 320 elements of the output shift register must be clocked out. This requires an element readout frequency for the C register of

$$f_r = \frac{\text{no. elements}}{t_a} = \frac{320}{52.58 \times 10^{-6}}$$

$$f_r = 6.086 \times 10^6 \text{ Hz}$$

The clocking frequency required for the NTSC sync generator, an MOS integrated circuit, is 504×10^3 Hz. As a practical requirement it seems reasonable to establish f_r as a whole multiple of the sync generator clock, yielding a new frequency of

$$f_r = 12 \times .504 \times 10^6 = 6.048 \times 10^6 \text{ Hz}$$

The new readout frequency will shift out 318 elements in 52.58×10^{-6} second.

In order to conveniently generate the three-phase clocks to operate the output readout register, it is necessary to incorporate a master clock at $3f_r$ or

$$f_m = 3 f_r = 18.1440 \times 10^6 \text{ Hz}$$

This will become the master oscillator from which all other timing signals will be derived.

The vertical blanking interval will be utilized to transfer signal charge from the photosensitive array, the A register, to the storage (B) array. This time is defined in the sync generator as 0.08V, or 1.33×10^{-3} second in which to transfer 268 rows of information. Maximum utilization of this time interval is desired. Assuming an available time of 1.20×10^{-3} second, the clocking frequency is established as

$$f_t \leq \frac{268}{1.20 \times 10^{-3}} = 223.3 \text{ kHz}$$

However, it would be convenient if this frequency were a whole multiple of the master oscillator. Since

$$f_t = \frac{f_m}{81} = \frac{18.1440 \times 10^6}{81} = 224.0 \text{ kHz},$$

this requirement is fulfilled.

c. Scanning Technique

The broadcast standard system (EIA Standard RS-170) consists of two 262.5 scan line fields, each 1/60 second long, and interlaced 2:1 to form one complete frame every 1/30 second. Blanking time for the display, representing a loss of active time in the scanning pattern of approximately 23 percent, is used to allow sufficient time for display retrace (and in the case of conventional vacuum tube cameras, for camera scanning retrace). This time is used to transfer charge from one register to another in a CCI camera.

The RS-170 vertical blanking interval is 0.075 $\pm$0.005 of the field interval, yielding 241.5 to 244.125 (243 nominal) active display lines per field. The next field is interleaved with the previous one, so that a total of 483 to 489 active scan lines occur in each frame. Since the number of horizontal intervals is 525 per frame, there is ample time to address all 256 rows in the array in each field.

The number of active scan lines per frame will need to correspond to the 4:3 aspect ratio requirement. For cells having square dimension (equal horizontal and vertical center-to-center spacing), 320 horizontal elements correspond to 240 unblanked vertical lines per field. Since the TV camera will operate at the RS-170 Standard requirement of 241.5 lines per field, the actual aspect ratio will be 320/241.5 = 1.325.

The composite video signal for the CCI format will conform timewise to the waveform specifications of RS-170. This format will permit the camera video output to be displayed on a conventional television monitor capable of reproducing an NTSC signal. In summary, the Picture Format Specifications are:

a) Frame Time - 1/30 second

b) Two Interlaced Fields - 1/60 second each

c) Active Scan Lines Per Frame - 483, 2.1 interlace

d) Horizontal Line Frequency - 15,750 Hz

e) Aspect Ratio - 4:3

B. Circuit Description

1. Video Processing

Video signals from the CCI serial shift register output are taken from the buffer MOSFET as shown in Figure 7. Once each clock period the potential on the floating diffusion is reset to the potential on the register drain by turning on the reset gate. The floating diffusion is operated as a reverse-biased diode, and the potential is stored on the diode capacitance. Signal charge is then transferred onto the diode, causing a potential change. The potential on the floating diffusion (diode) modulates the gate of the output MOS-FET, yielding an output signal current.

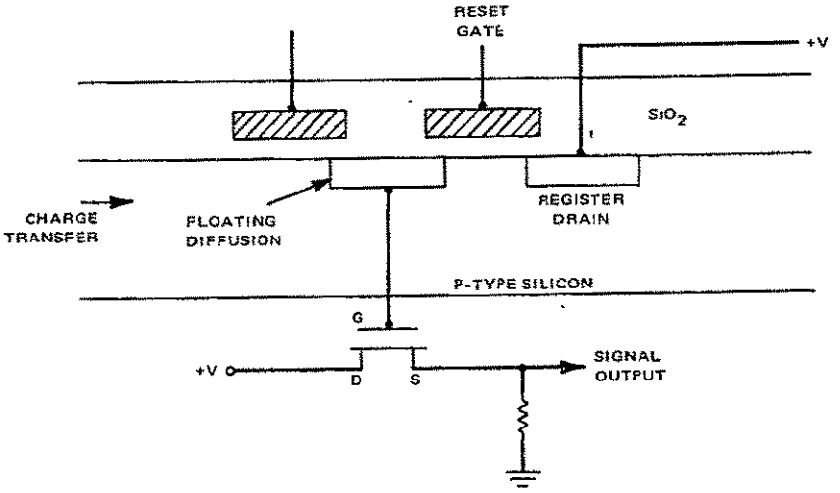


Figure 7. Output Circuit of CCI

The video processing to be performed upon the CCI signal information is shown in Figure 8. Buffered video data passes through a sharp cutoff low-pass filter which removes clocking transients and smooths the sampled information. A low-noise amplifier with adjustable gain amplifies the signal to its proper level followed by dc restoration to a dc reference. This data is then coupled to an automatic light control (ALC) circuit which varies the CCI exposure interval. A reference level, zero volts, is inserted during the horizontal blanking interval to be utilized by the following automatic gain control (AGC) circuit for clamping. The appropriate NTSC blanking and sync signals are inserted into the video information as well as black clipping at the porch level and white clipping at peak white plus 50 millivolts. An output amplifier provides the monochrome video signal in the required format.

2. Filter

The low-pass filter utilized in the camera design, Appendix B, SK 2282870, is a 6-stage Cauer filter which was selected for its amount of minimum attenuation in the stopband. Clocking of the CCI output register is performed at a frequency of

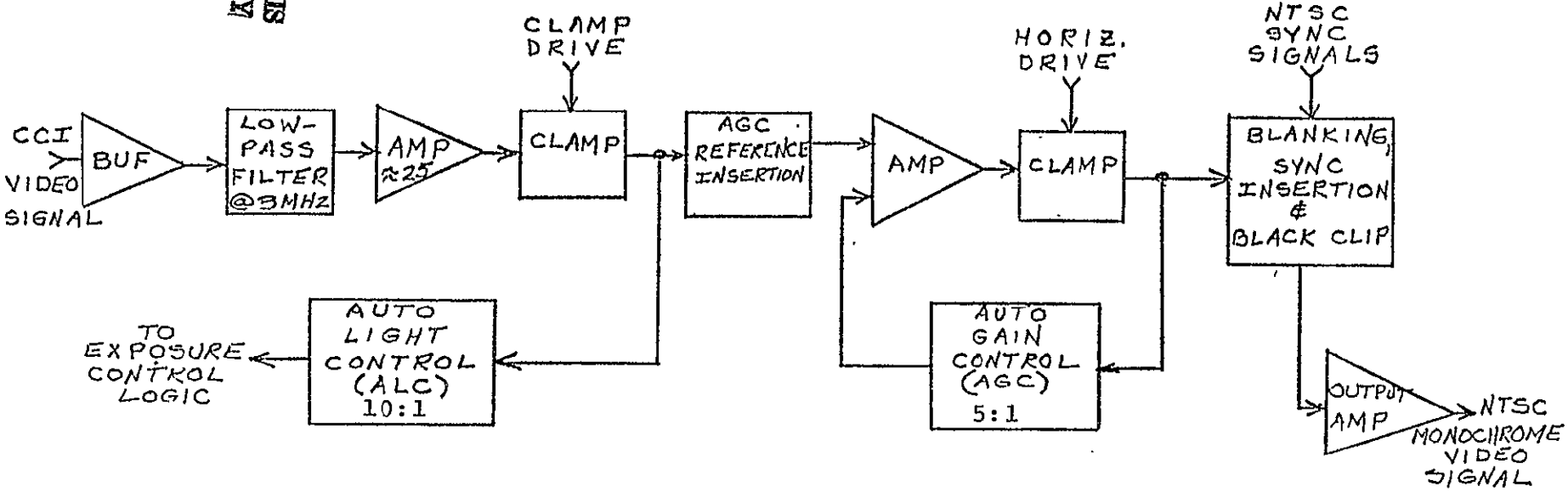


Figure 8. Video Processor, Block Diagram

6.048 MHz and the highest signal frequency of interest, to support 320 horizontal elements, is 3.0 MHz. Transients at the 6.048 MHz rate will appear with the video information at the CCI output buffer and must be attenuated. The frequency characteristics of the filter are such that it has a flat response to 3.0 MHz and a frequency null at 6.0 MHz with a minimum stopband attenuation of 60 decibels. No clocking transients were visible in camera video output as a result of this filter; all coherent clocking noise is well within the CCI random noise.

3. Automatic Exposure Control

Automatic exposure control is incorporated in the camera design to extend the light range over which the camera may be operated without iris adjustment. This is obtained through the utilization of ALC and AGC circuit functions as illustrated in Figure 9. At exposure level E1, the signal at point A will correspond to about 1/5 well, the cut-in point of the AGC function. Gain control is operative, maintaining a fixed output at point B, until exposure 5E1 is reached which approximately corresponds to full well operation of the CCI. The ALC function will begin operation at an exposure of 5E1 and will function to an exposure level of 50 E1. The ALC circuit will act to shorten the CCI integration time while maintaining a constant signal output at point A, from an exposure of 5E1 to 50E1. An exposure greater than 50E1 causes signal charge to exceed a full well, a saturated condition, but operational antiblooming will permit operation with exposure levels well in excess of 50E1. Of course the lens iris aperture may be reduced to avoid the overload.

In the design of both the AGC and ALC circuit functions, a requirement exists to dc restore the video information by utilizing the electrically inserted "C" register fat zero as a clamping reference. However, scene black information will not be at this level but will reside on a pedestal whose level is dependent upon the amount of optical background charge (typically 10% of the

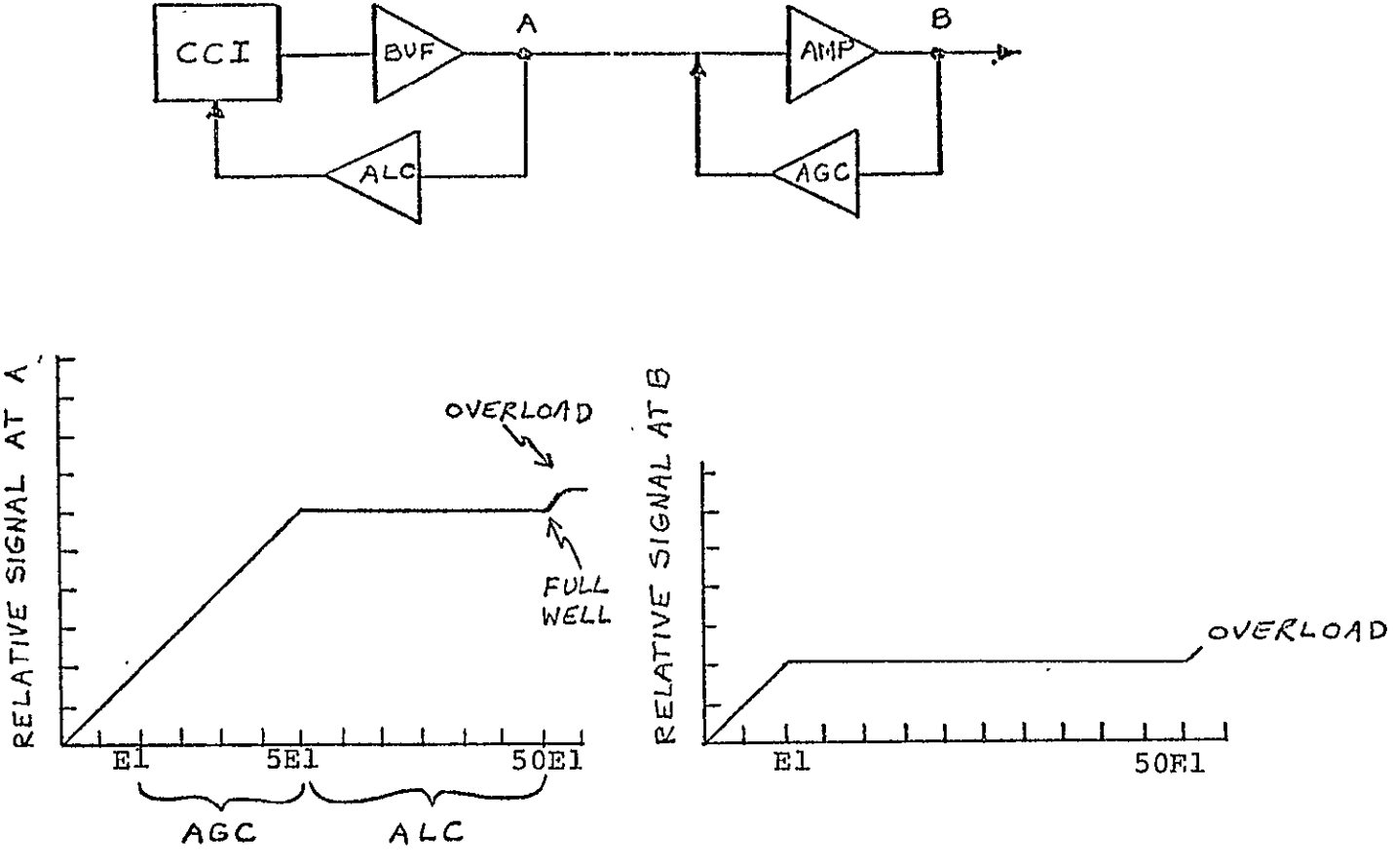


Figure 9. Automatic Exposure Control Block Diagram With Curves of Signal Levels at "A" and "B" in Video Chain

"A" register full well charge) required to compensate for trapping effects. This would result in a varying black level as the AGC gain changes as well as different levels of optical background charge as the ALC varies the exposure interval. To circumvent these effects the bias light utilized for the optical background charge will be flashed "ON" for the last 3 milliseconds of each field interval. This is near the end of the 10/1 range of the ALC function and will maintain a constant background charge in the "A" register well, independent of the ALC exposure control. The video information will be dc restored prior to the ALC and AGC, and scene black information adjusted to a zero level. This signal will feed the ALC and permit it to peak or average detect only the black-to-white video signal while excluding the optical background charge pedestal. Also, a zero reference level will be inserted during the clamp interval but prior to the AGC function, to permit only peak or average detection of the black-to-white video signal while in the AGC mode of operation.

a. Automatic Gain Control (AGC)

The AGC function block diagram is illustrated in Figure 10 and the schematic drawing in Appendix A, SK2282868. As may be observed from the block diagram, the video information is amplified, followed by dc restoration to a reference level of zero volts. Signal amplitude at this point has a black-to-white value of 1.32 volts. Scene information is either peak or average detected and a comparison is made with a reference voltage. The resultant signal modulates a J-FET which acts as a voltage controlled resistor to change the gain of the amplifier and hold the output signal constant.

A single amplifier is used to peak or average detect the video signal, the mode of operation selected via a relay which switches a capacitor to either ground (peak mode) or across the amplifier feedback resistor (average mode). In the average mode of operation a potentiometer setting, AGC average set, has been adjusted

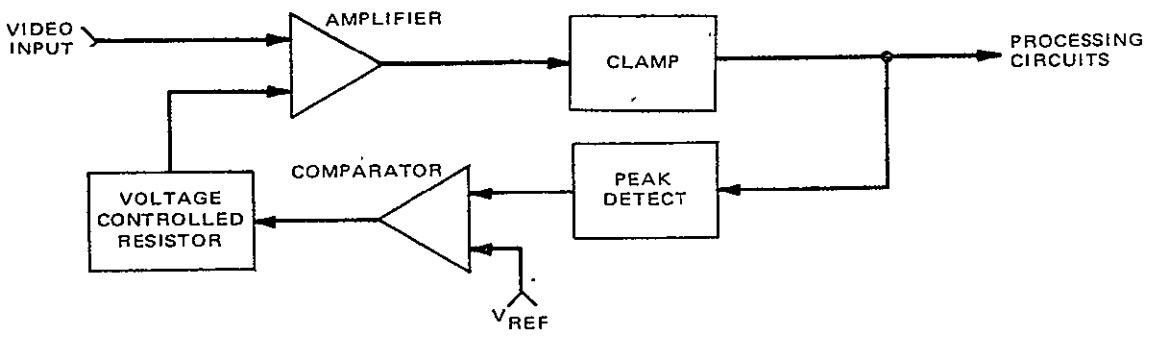


Figure 10. Automatic Gain Control (AGC) Block Diagram

for an average scene content of 50% white and 50% black. The small-signal bandwidth of the AGC loop (both predicted and measured) is 8 Hz and 2 Hz, for average and peak modes respectively. In the peak mode of operation the circuit is capable of detecting a scene highlight of 0.5% of the total area imaged upon the CCI.

Modifications to the circuit throughout the course of the program are as follows:

1) A low-pass filter on the input of the detector to attenuate peak transient signals.

2) Diode bounds were put into the comparator to limit its voltage excursions, thereby reducing the slewing required when swinging from maximum to minimum gain and vice versa.

Referring to the schematic drawing in Appendix B, SK2282868, the AGC function is followed by the video output and sync insertion amplifier. A potentiometer adjustment is available for setting the black level during camera setup and a white

clip circuit to limit the signal output to 1.05 volts peak white. Horizontal blanking and sync information, with controlled rise and fall times, are inserted prior to the final driver amplifier. The amplifier is designed to drive a 75-ohm load and has a frequency characteristic which is -3 decibels at 12.0 MHz. Video information will be black negative, with sync tip nominally at 0 volt dc and peak white at +1.0 volt.

b. Automatic Light Control (ALC)

The ALC function block diagram is shown in Figure 11, and the schematic drawing in Appendix A, SK2282869. As may be seen from the block diagram, the video information is low-pass filtered, amplified to a level of 1 volt black-to-white, and dc restored to an adjustable reference level. The output at this point is adjusted by means of the clamp reference so that scene black has a value of zero volts. Signal information is either peak or average detected and compared with a reference voltage. The resultant error signal is then compared with a vertical sawtooth at the 1/60 second field rate to generate a variable width pulse. This pulse will control the logic of the CCI "A" register clocks by inhibiting charge accumulation during a portion of the active vertical exposure interval. Limits have been incorporated into the comparator to establish the range of optical integration, the range being 10:1 for this camera design. A potentiometer is available to adjust the size of the vertical sawtooth utilized by the pulse-width modulator which will control the ALC function over a 5:1 to 10:1 range.

As with the AGC circuit, the detection amplifier utilizes a relay switched capacitor to convert from peak to average modes of operation and a potentiometer adjustment to set the average value. The time constant of the circuit is such that in the peak mode only 1% of the capacitor charge is lost on a field-to-field basis. Otherwise the gain of the circuit would not remain constant after peak detection of the highlight signal.

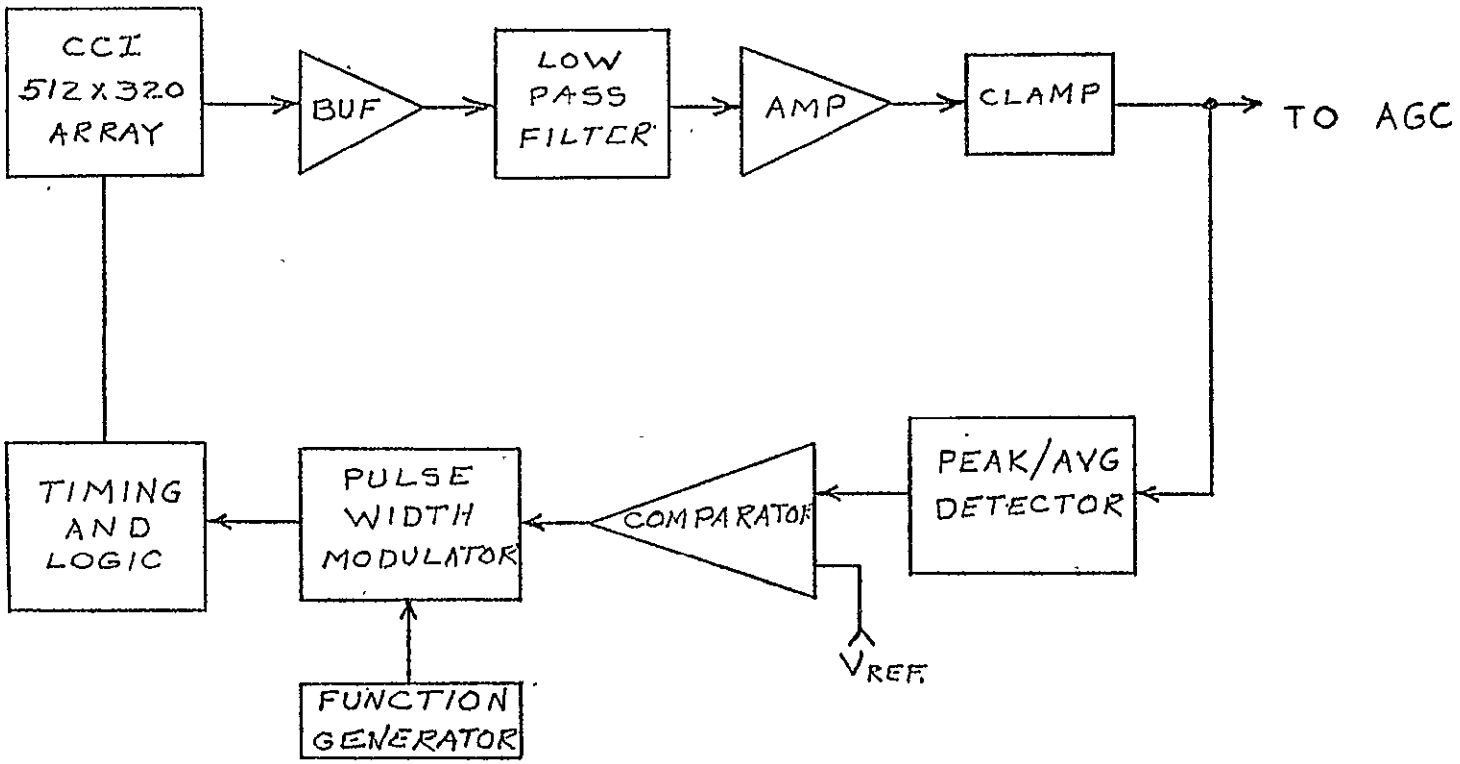


Figure 11. Automatic Light Control (ALC) Block Diagram

The small signal bandwidth of the ALC loop is approximately 3 Hz and 0.8 Hz in the average and peak modes respectively. Loop stability is maintained in both modes of operation by the switching of a capacitor via a relay across the feedback resistor of the comparator.

Modifications to the ALC circuit throughout the course of the program are as follows:

1) A low-pass filter on the input to the detection amplifier to attenuate peak transient signals.

2) Potentiometer addition to the vertical sawtooth generator to adjust its size over a limited range.

3) The video signal is clamped during the entire vertical blanking interval to attentuate the "A" to "B" clocking transients.

4. Timing and Logic

a. Digital Control Timing Unit

The digital control timing unit, shown in the block diagram of Figure 12, is synchronously timed by the crystal controlled master oscillator. All the required timing signals for the CCI array and the line and field rate pulses for the video processor are derived from this oscillator. In the actual camera design the master oscillator has an operating frequency of 18.125872 MHz which will produce a color horizontal line rate of 15,734.264 Hz. However, for ease of numbers an oscillator frequency of 18.1440 MHz will be shown in the diagrams which will result in an insignificant frequency difference. The CCI clocking waveforms are generated in the timing and logic circuits which utilize low-power TTL for the high speed logic (>2.0 MHz) and COS/MOS for the lower frequency logic (A and B register). The interface drivers convert the logic signals to the voltage levels required for the input terminals of the CCI array. Standard television

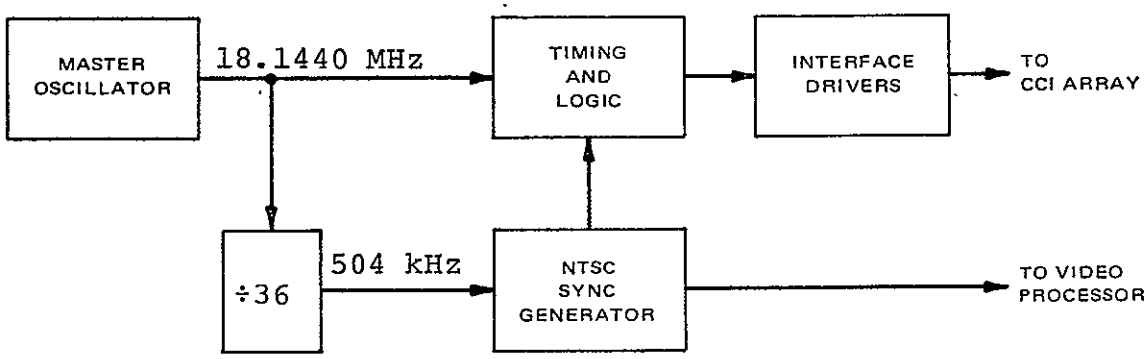


Figure 12. Digital Control Timing Unit Simplified Block Diagram

rate signals are generated in the NTSC sync generator, a single COS/MOS integrated circuit.

b. NTSC Sync Generator

The sync generator is a COS/MOS integrated circuit designed to supply the basic sync functions required for a monochrome 525 line/60 Hz interlaced television camera. This is a developmental RCA device, P/N TCC-040-608, which was selected for its low power consumption, 7 milliwatts, and the capability to operate from a single supply voltage of +6 to +15 volts dc. There are minor deviations to the specifications of RS-170 but these are corrected by decoding with the input clock signal. In addition to standard horizontal and vertical rate signals, it provides an odd field frame rate signal which is used in the timing and logic. This will ensure that the field being readout is in phase with the output odd/even field sequence of the sync generator.

c. Timing and Logic

The clock frequencies required for the timing and logic are:

1) Three times the A-B transfer rate to generate ϕ_{A1}, ϕ_{A2}, and ϕ_{A3} signals. This ϕ_A rate will continue for 268 transfers during the vertical blanking time.

2) Three times the C-register clock rate to generate ϕ_{C1}, ϕ_{C2}, and ϕ_{C3} signals. The required C-register rate is 6.048 MHz enabling 320 elements to be read out during the horizontal active time.

The highest frequency required, which determines the master oscillator frequency, is:

$$3 \times 6.048 \text{ MHz} = 18.1440 \text{ MHz}$$

The clocking rates derived from the master oscillator (MO) are as follows:

1) C-Register - MO divided by 3:

$$\frac{18.1440}{3} = 6.048 \text{ MHz}$$

2) Sync generator clock frequency - MO divided by 9:

$$\frac{18.1440}{36} = 504 \text{ kHz}$$

3) Three times A-B transfer rate - MO divided by 27:

$$\frac{18.1440 \text{ MHz}}{27} = 672 \text{ kHz}$$

The timing and logic simplified block diagram is illustrated in Figure 13.

The output register clocks ϕ_{C1}, ϕ_{C2}, and ϕ_{C3} are generated from the master oscillator in a divide by 3 counter, which is reset at the horizontal line rate. Pulses to reset the output floating

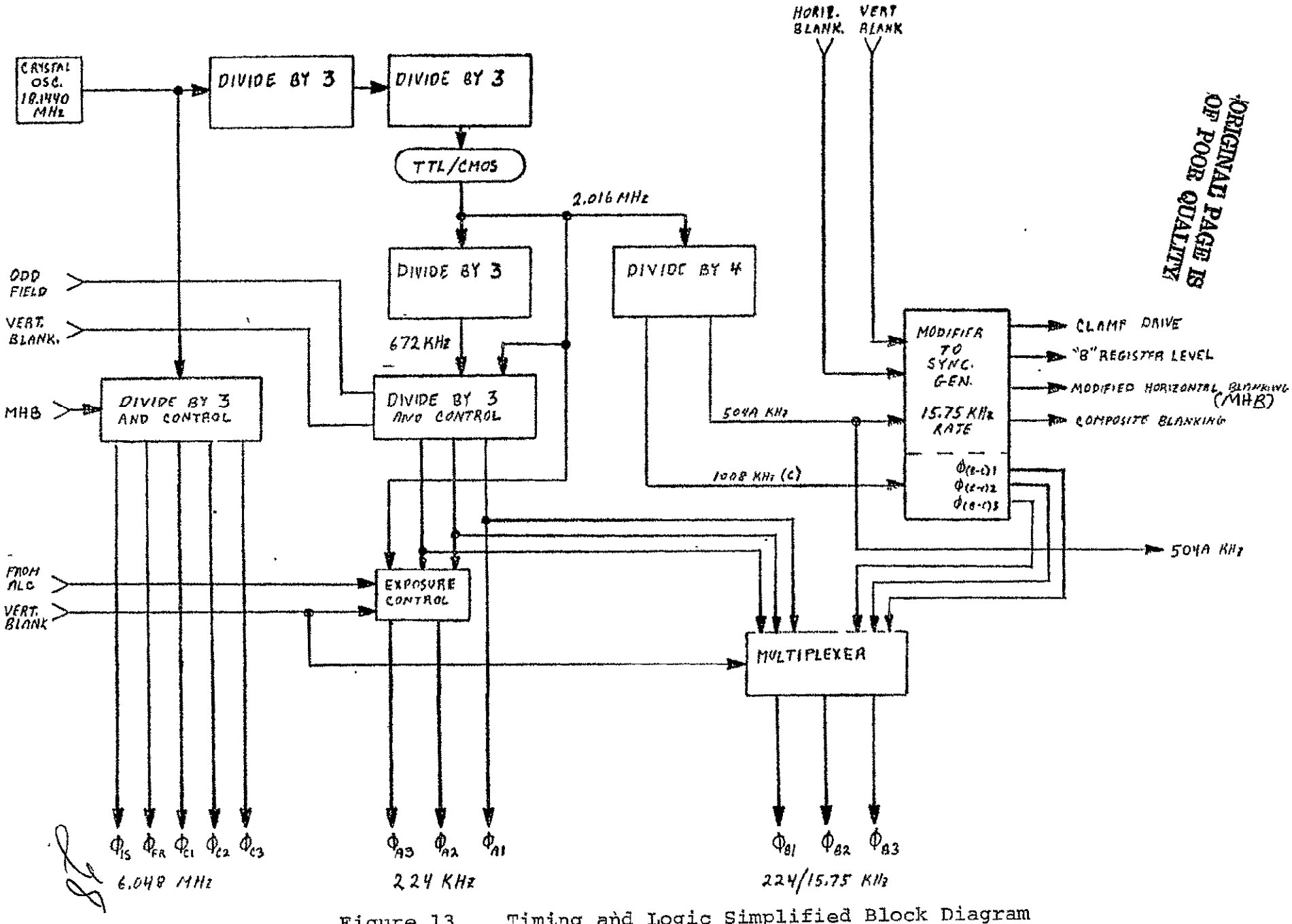


Figure 13. Timing and Logic Simplified Block Diagram

diffusion and insert the electrical background charge are derived from the phase C2 signal.

The A-register clock is derived from 18.1440 MHz by first dividing by 27 to generate a 672 kHz clock. Division by 3 then yields ϕ_{A1}, ϕ_{A2}, and ϕ_{A3} clock pulses. The divide by three that produces the A-register pulses is controlled by a two state sequencer which is in itself controlled by a counter and another two state sequencer. The counter will determine when to start and stop the production of A-register pulses during the vertical blanking interval, proper phasing of the pulses under control of the sync generator, odd field indicator and vertical blanking outputs. Exposure control will inhibit the ϕ_{A2} or ϕ_{A3} voltage level from being applied to the CCI photosensitive register, thereby varying the optical integration time in response to period changes derived in the ALC circuit.

A clock of 1008 kHz is developed to be utilized in conjunction with three flip flops connected in a shift register configuration. The outputs of the three flip flops comprise the three "B" to "C" register transfer clocks.

The multiplexer functions to permit selection of the source for the B-register clock. During A-B transfer, the A and B register clocks are the same, and consequently the multiplexer has its output ϕ_{B1}, ϕ_{B2}, ϕ_{B3} connected to the ϕ_{A1}, ϕ_{A2}, and ϕ_{A3} clocking inputs. During the active readout time, the B-register is clocked at the horizontal rate, transfer occurring during the blanking interval, and the multiplexer connects the B outputs to the B-C phase.

The modifier to the sync generator will alter some of the generator outputs to be consistent with the specifications of RS-170.

All timing signals utilized in the camera design are shown in Figure 14.

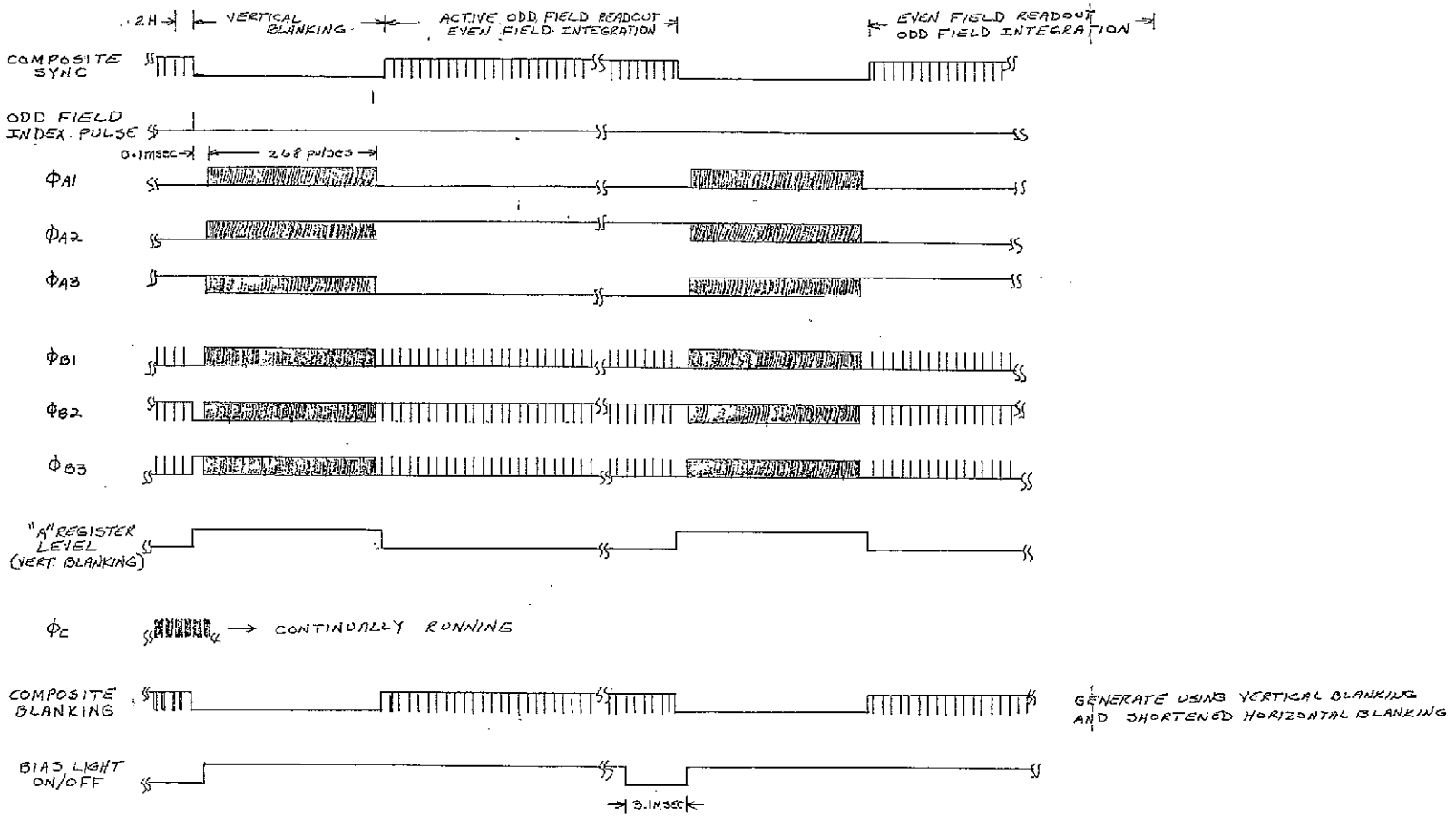


FIGURE 14a

CCI TIMING DIAGRAM

VERTICAL TIMING

M. Kravitz 8/1/7

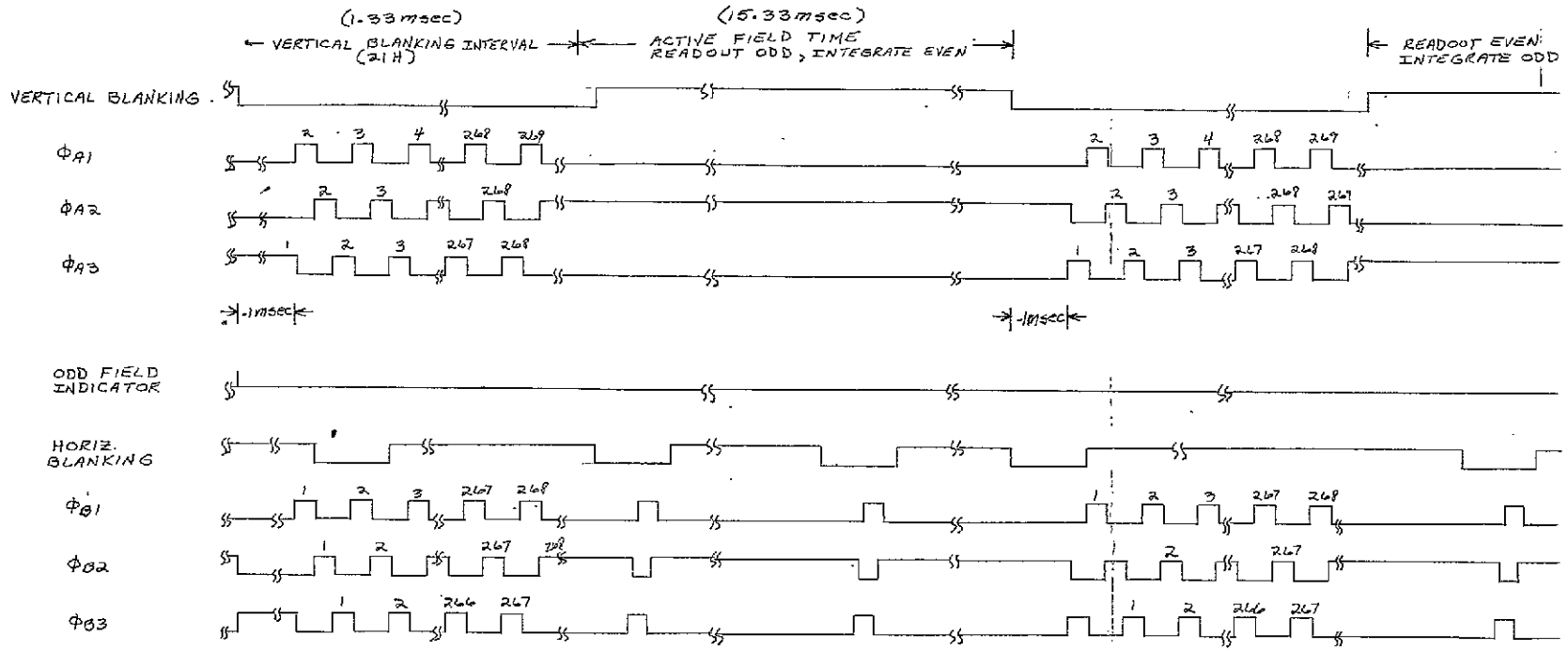


FIGURE 14b

"A" TO "B" TRANSFER

FOLDOUT FRAME 1

FOLDOUT FRAME 2

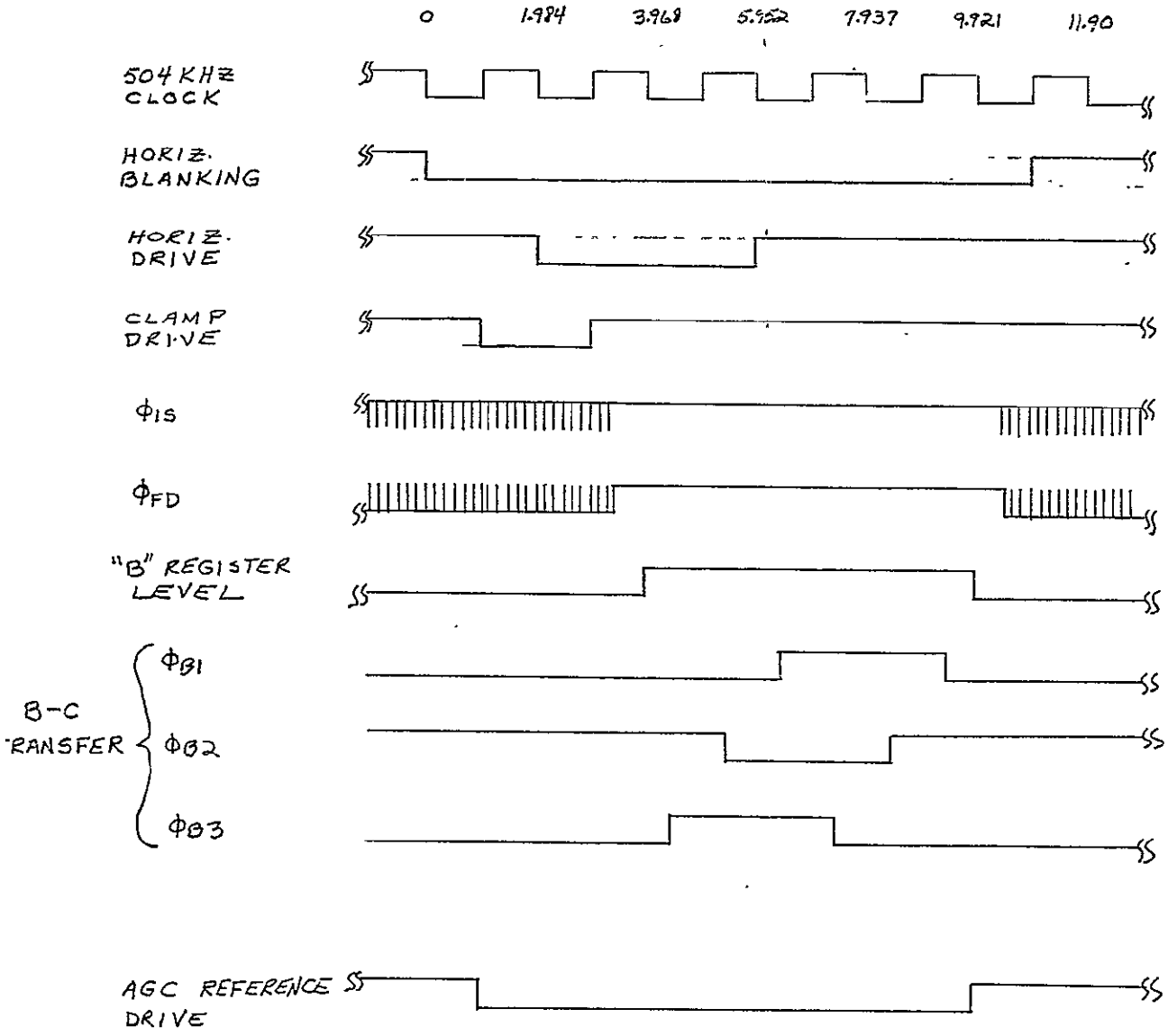


FIGURE 14c.

"B" TO "C" TRANSFER

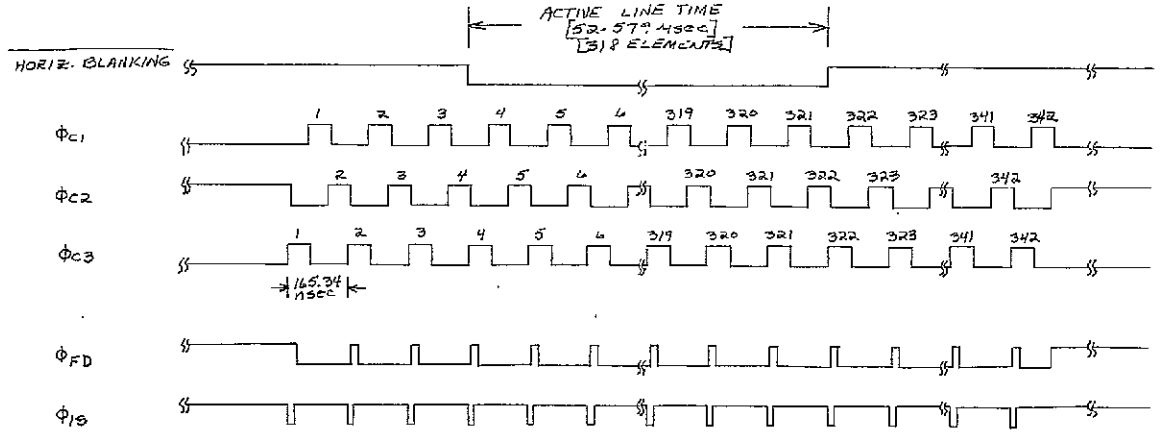


FIGURE 14d

"C" READOUT

C. Camera Integration and Debug

Integration of the camera system was performed on a systematic basis, commencing with an electrical checkout of all supply voltages to an appropriate pin on the harness board. Confirmation of the proper dc voltages was followed by installation of the three logic boards, A1 thru A3, and a check made of all timing and logic signals. A sample CCI was not inserted into its socket until it was verified that the proper signal was present at the appropriate pin of the CCI socket. It was found that except for minor discrepancies, all timing and logic signals were in agreement with the timing diagram as shown in Figure 14. There were no changes made to the basic block diagram of the logic circuitry as illustrated in Figure 13. Prior to installation of a CCI the remaining two boards, A4 and A5, containing the video processing circuitry, were inserted into the camera. A frequency response of the total video chain was performed, less the AGC and ALC loops, and found to perform as anticipated. The AGC loop was then closed, a test signal inserted at its input, and operation of gain control verified. Initially, it was found that the expected range of 5:1 was not achieved. This was attributable to noise pickup at the input of the comparator and required shielding the mixed sync, composite blanking, and horizontal drive logic signals, after which the proper range was achieved.

Testing of the ALC circuit was restricted to confirmation of open-loop parameters until a CCI could be installed to complete the loop.

At this point a sample CCI was inserted into the socket to verify the camera operation. A video signal was obtained through the complete camera system from optical input to monitor display. An initial problem of low level logic signal noise was observed and required further investigation. The AGC and ALC loops were disabled during this period of time. Initial tests revealed the presence of various clocking transients, 504 kHz to the sync generator,

2.016 MHz clock associated with the A-B transfer, and 6.048 MHz clock for the C register. Each of these clocking signals are routed through the harness board in close proximity to the CCI. Shielding of these signal lines considerably reduced the visibility of clocking noise on the monitor display. The remaining noise was eliminated by shielding the buffer emitter follower on the output of the CCI, placing a shield cover over the sync generator, and adding inductors to the decoupling of the +10 volt supply on the A2, A3, and A4 boards.

Examination of the logic signals at the CCI socket revealed considerable coupling within the CCI chip itself, from the A, B, and C gates to the FET output transistor. This necessitated a timing change in the pulses to reset the floating diffusion and inject the electrical background charge. Additional decoupling of the substrate, at the CCI socket, also improved the situation. Elimination of these spurious effects enabled the CCI to produce a video signal which appeared excellent on the monitor display. Measurement of the video information directly on the output of the CCI verified that a peak-to-peak signal of approximately 200 millivolts was obtainable.

Verification of circuit performance proceeded to the ALC/AGC functions upon completion of the noise debugging. The ALC circuit functioned as expected but a black horizontal line was observed on the monitor display. The line position followed the ALC control pulse as it was varied over a 5:1 light range. This was caused by a CCI substrate transient when switching the appropriate "A" register gate from accumulation to integration. Rise time control of the switching signal was incorporated to eliminate the effect as seen on the monitor display. A further improvement was added to the circuit by limiting the voltage excursions of the comparator thereby improving the large signal response time of the ALC loop.

Operation of the AGC circuit was previously verified but it was necessary to incorporate a low-pass filter at the input of the detector to attenuate A-B transfer transients during the vertical blanking interval. Gain control was extended to 5:1 and light control to 10:1 when it was found that camera performance was not seriously degraded.

The last obstacle to be encountered was the insertion of the optical fat zero as far as uniformity of light across the CCI image plane. The original concept of a ring containing four visible LED's did not prove adequate and an alternate approach was required. This took the form of a new assembly mounted directly adjacent to the CCI and utilized an acrylic plastic to diffuse the radiant energy from the LED's. The number of LED's remained at four but the type was changed to an RCA IR-emitting diode, SG1004. It was found that the RCA diode produced greater radiant power than the visible LED, requiring less drive current for the same CCI signal output. The change necessitated the modification of the camera front plate to provide more space in the area directly in front of the CCI. However, the uniformity of light across the CCI image plane was improved to the point of acceptance.

Performance parameters of the CCI were optimized to provide maximum transfer efficiency, S/N, and resolution. In establishing the parameter tradeoff between anti-blooming performance and dynamic range, greater weight was given to extending the dynamic range.

D. Physical Characteristics and Power

The mechanical design of the camera is essentially configured as an "L", consisting of the base and front plate. This is illustrated in the photographs of the actual TV camera in Figures 15 and 16. The base is a machined cavity which will contain the commercial power supply modules, feed-thru filters, and control switches. Included as an integral part of the base is a tripod mount adapter. A modular power supply configuration

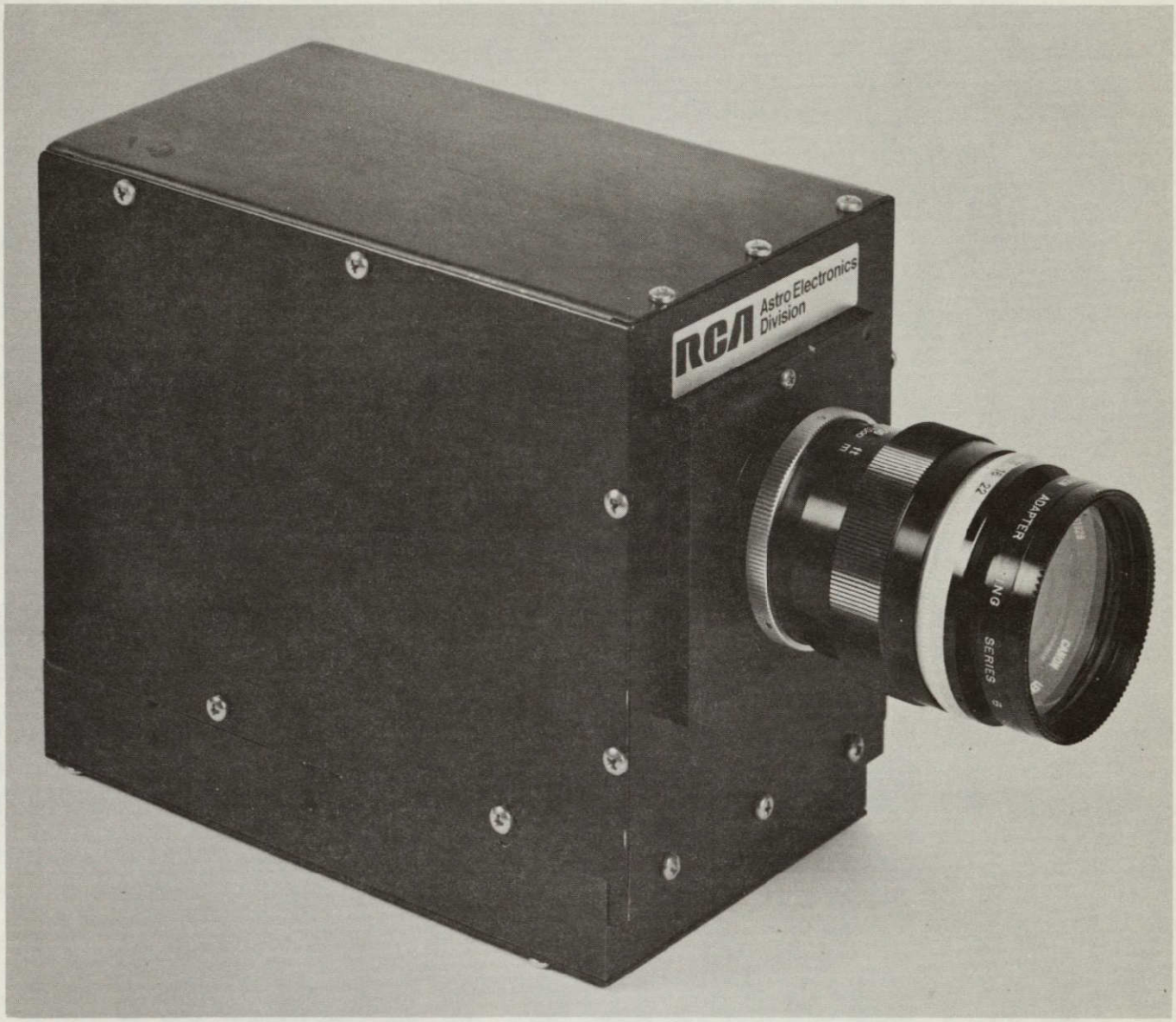


Figure 15. Solid State TV Camera

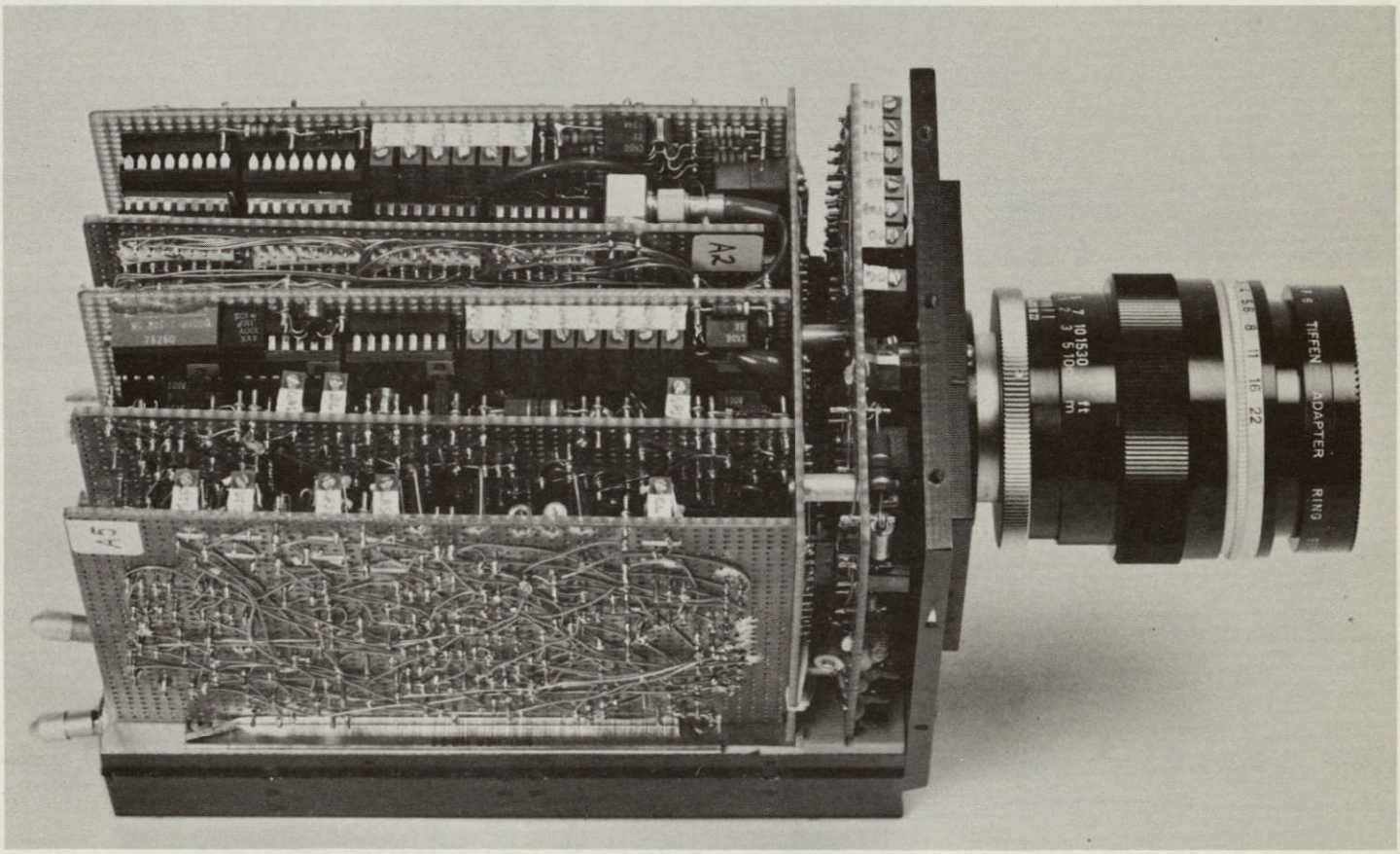


Figure 16. Solid State TV Camera (Cover Removed)

was selected, using a single dc/ac converter coupled to several ac/dc regulator modules. The regulator modules selected are: (1) dual 6 volts, (2) dual 5 volts, and (3) dual 10 volts. Since each output of a dual regulator is isolated, they can be stacked as required to provide the desired voltages while maintaining design versatility. Dimensions of the complete power supply package is 1" x 2" x 4".

Birtcher slides are attached to the upper surface of the base to secure the individual circuit boards. There are five circuit boards to perform all electronic functions; three contain the logic functions while the remaining two contain the video processing circuitry. Each of these boards contains a plug-in connector which mates with a matching receptacle on a harness board located at the front end of the camera. Attached to the harness board using stand-off posts and two 14-pin dip connectors is the CCI mounting board and bias light assembly. In addition the mounting board contains the low-pass filter, preamplifier stage, and decoupling circuits.

The upper portion of the housing consists of a formed aluminum cover with removable sides for accessibility to potentiometers. A lens adapter located on the front plate will accept any "C" mount type lens, the present camera utilizing a 50-millimeter f/1.4 lens with the option of a screw-in filter ring containing an IR rejection filter.

Overall dimensions of the housing including the power supply base are 3.6" W. x 5" H. x 6" L. The total weight of the package including the lens is 4.8 pounds.

The total average conditioned power of the TV camera not including the loss due to power supply efficiency is 3.93 watts.

E. Acceptance Testing

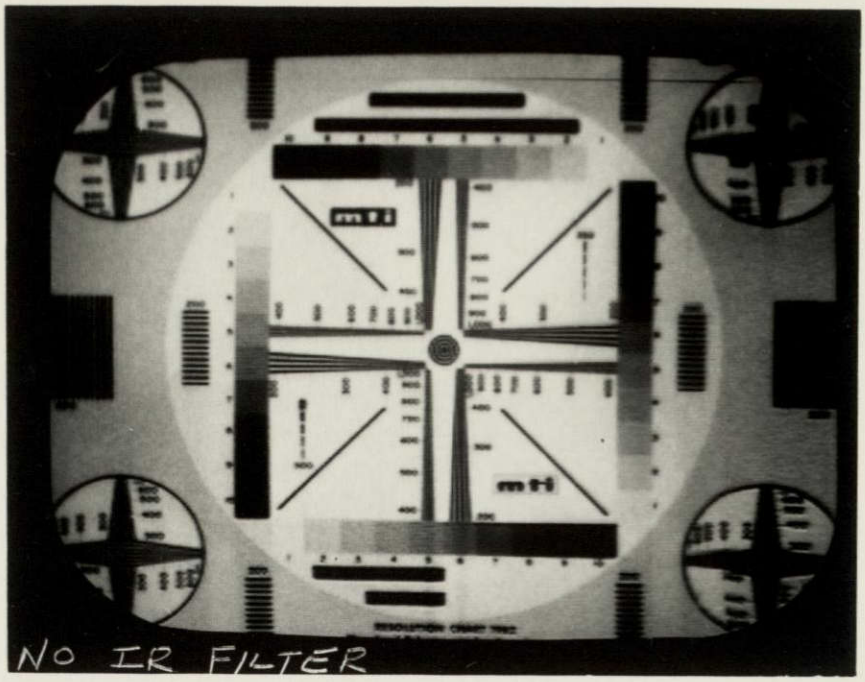
The final selected CCI device was tested for performance characteristics at the RCA Laboratories, using their standard test facility. General performance characteristics were considered to be excellent, particularly with regard to resolution (MTF response). A processing blemish, near the very top of the raster, causes a horizontal line to be visible in the monitor display from a region about 2/3 of the way across the raster. A few smaller spots, again due to processing, were much less visible at highlight illumination levels. However, these blemishes did not seriously degrade the overall performance of this particular CCI, which was considered one of the best samples of the current state-of-the-art. Typical monitor display presentations are shown in Figure 17.

The acceptance test was performed under ambient conditions and a sun gun of 3400°K color temperature was the source of illumination. A signal-to-noise ratio of 40 decibels was achieved at the cut-in point of the AGC function where circuit gain was at a maximum and the CCI was operating at approximately 15% of full well change. The signal-to-noise may well be greater than 40 decibels as it is difficult to discern between the true random noise and background non-uniformities. The operational anti-blooming functioned quite well, allowing virtual containment of an optical overload up to 10 times and greatly reduced blooming for overloads of 64 times. Table 1 is a summary of the cumulative results of the acceptance tests.

An operational mode study was performed by the RCA Laboratories, to investigate the following parameters:

1) Gamma at wavelengths of 1100 nm, 700 nm, and 450 nm.
2) Resolution (MTF) with and without infrared filtering.
3) Effect of A-B register transfer in vertical resolution and well size.

The results of this study are contained in Appendix A.



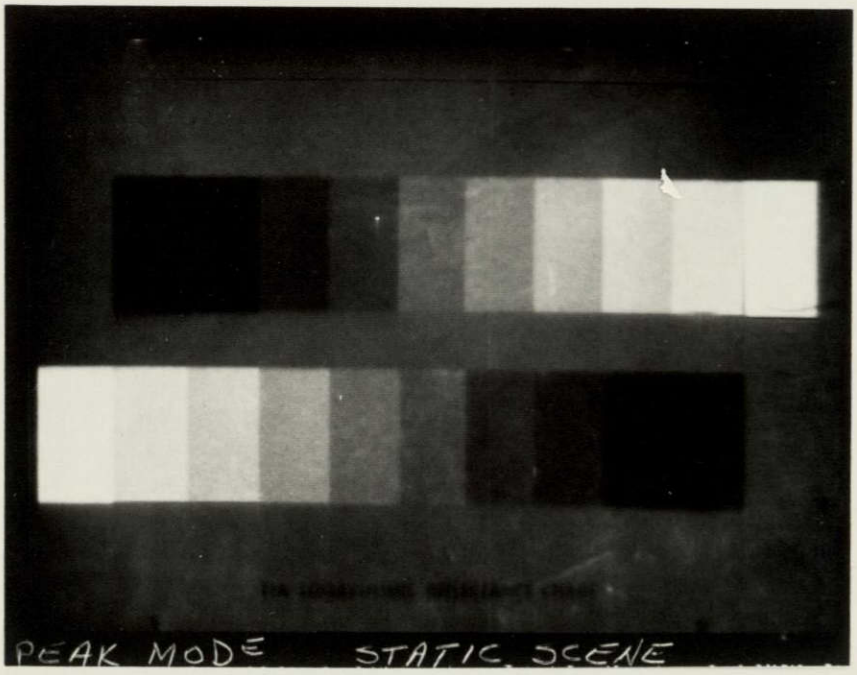


Figure 17. Monitor Display of Scenes Taken With Solid State TV Camera

TABLE 1. CUMULATIVE RESULTS OF ACCEPTANCE TEST

	PARAMETER	MEASURED	SPEC LIMIT
Video Levels	Peak White	1.0V	1.0 ±.05V
	Black Level	.05V	.05 ±.036V
	Sync Tip	.019V	0 ±.05V
	Capped Lens Black	.05V	.05 ±.036V
	Blanking Level	.280V	.286 ±.05V
Aspect Ratio	Horizontal	3.2813	
	Vertical	2.4031	
	Ratio	1.365	4:3
Resolution	Limiting Horizontal	320 TVL/PW	224 TVL/PW
	Limiting Vertical	400 TVL/PH	-
Geometric Distortion	Center Area	< ±1%	±2%
	Outside Center Area	< ±1%	±5%
	Rate of Change	< .5%	.5% PH
Horizontal Black Shading	Line No. 24	1.7%	10%
	72	4.7%	
	120	3.2%	
	169	4.7%	
	217	1.6%	
Horizontal White Shading	Line No. 24	18.3	10%
	72	21.9	
	120	17.5	
	169	21.9	
	217	9.8	
Vertical Shading	Black	6.25%	10%
	White	14.0%	10%

TABLE 1. CUMULATIVE RESULTS OF ACCEPTANCE TEST (Cont'd)

	PARAMETER	MEASURED	SPEC LIMIT
Static Scene Light Range	No. Gray Steps	>10	10 min.
	S/N	46 dB	35 dB
Gain Dynamic Light Range	S/N	40 dB	35 dB
	Range of Automatic Control	50:1	6:1
Total Operating Light Range (With IR Filter)	Min. Illumination	1.5 FL	4.5 FL
	Max. Illumination	8000 FL	-
	Total Range	5333:1	600:1
Total Operating Light Range (No IR Filter)	Min. Illumination	0.7 FL	4.5 FL
	Max. Illumination	4300 FL	-
	Total Range	6142:1	600:1
AGC/ALC Time Constant (Peak Mode)	50:1 Step Down	1.2 Sec	-
	1:50 Step Up	.56 Sec	-
AGC/ALC Time Constant (Avg. Mode)	50:1 Step Down	.2 Sec	-
	1:50 Step Up	1.1 Sec	-
Video Clip Levels	Peak White	1.05V	-
	Black	.27V	-

F. Television Camera Operation

There are a large number of potentiometer adjustments to be made when optimizing the performance characteristics of the CCI. These should not be altered once the camera becomes operational. However, there are a few adjustments which may be made if it is desired to optimize operation under a particular set of conditions. In order to make any adjustment it will be necessary to remove the camera top cover and refer to the applicable drawing in Appendix B. Each potentiometer is labeled with a set of letters in the camera which will aid in locating the appropriate one. Table 2 lists the parameters that are available for change and the adjustments to be made to accomplish the task.

Prior to delivery of the TV camera, all the CCI operating voltages were measured at the wiper of each potentiometer and are listed in Table 3.

TABLE 2. LIST OF OPERATIONAL CHANGES AND APPLICABLE ADJUSTMENTS

PARAMETER	ADJUSTMENT
DC level shift of output video signal.	1. Adjust R13 on the A4 board label "BL".
Optical bias light adjustment	1. Adjust R10 on the A7 board labeled "LED" to increase/decrease optical background charge. 2. View a black bar on an all white field and adjust exposure to be just at the end of the ALC range. 3. Observe the output video signal on an "A" scope. 4. Adjust R15 on the A5 board labeled "CL" until the scene black is at the same dc level as a capped lens condition. 5. It may be necessary to adjust R13 (BL) of the A4 board to obtain proper black setup.
ALC range between 5:1 and 10:1	1. Adjust R58 on the A5 board labeled "STS".
Setting average mode level	1. Adjust R23 (LAS) on the A5 board when in the ALC range. 2. Adjust R64 (GAS) on the A4 board when in the AGC range.

TABLE 3. LIST OF CCI OPERATING VOLTAGES

POT	VOLTAGE	TITLE
CL	+3.12 V	ϕC Low
CH	+20.0 V	ϕC High
ISL	+0.91 V	Input Source Low
ISH	+6.95 V	Input Source High
RL	+1.31 V	Reset Diffusion Low
RH	+13.81 V	Reset Diffusion High
B2H	+8.23 V	ϕB2 High
B3H	+8.25 V	ϕB3 High
ABH	+10.0 V	A-B Transfer High
AI	+4.33 V	A-Register Integrate
AA	-2.10 V	A-Register Accumulate
FB1	-5.0 V	ϕB1 Fall Time
FB2	-5.0 V	ϕB2 Fall Time
FB3	-5.0 V	ϕB3 Fall Time
B2L	+0.60 V	ϕB3 Low
OG	+10.22 V	Output Gate
OD	+14.46 V	Output FET Drain
VBB	-1.0 V	Substrate
RD	+10.08 V	C-Register Reset Drain
IG2	+4.30 V	C-Register Input Gate
IG1	+3.66 V	C-Register Input Gate
LED	-2.81 V	Optical Bias Lite

G. Comments and Recommendations

Performance of the RCA imager, including blooming control and automatic light control, has demonstrated that sensitivity, signal-to-noise, total light range, and most development objectives have been achieved. Future CCI devices show promise that developing process controls will soon reduce spots and blemishes to a level required for space flight applications. Custom design of the logic circuitry through the use of large scale integrated circuitry as well as a custom power supply design could result in a camera of approximately one-half its present volume with minimum power consumption.

The present camera configuration has achieved a gain-dynamic range, through the use of ALC/AGC, of 50:1. Possibly with the processing improvement of future CCI's the AGC range could be extended to 10:1 resulting in a total gain-dynamic range of 100:1. The ALC function is probably at its limit, an extension of its range causing a loss in vertical MTF and more noticeable smear due to the A-B transfer time. Should an improvement be made in the transfer efficiency of the A-B registers, the time to transfer 268 lines during the vertical blanking interval could be reduced. This would minimize the smearing effect and permit a further extension of the ALC range. Use of a mechanical shutter during vertical blanking is impractical and the solid state filter at present has too much transmission loss for low-light applications. Therefore, it would seem unlikely that the gain-dynamic range could be extended beyond 200:1, with 100:1 a reasonable design goal. Of course an ALC function utilizing the lens iris adjustment could extend this range.

The static scene light range (dynamic range) could be improved through the use of cooling, probably utilizing a thermo-electric cooler. Low-light level performance of CCI's is limited by non-uniformities in background dark current. Device cooling has been shown to be effective in reducing both the average

dark current and the amplitude of dark current spikes. Measurements performed on early CCI's have shown devices cooled to -10°C to have a dynamic range of up to 500:1. The degree of improvement obtainable via cooling of the device is related to the quality of the fabricated unit.

There does not appear to be a need for improvement in the total operating light range of the camera, the total range being well in excess of 2000:1.

The antiblooming characteristics of the CCI can be improved but only at the sacrifice of the static scene dynamic range. This is accomplished by reducing the size of the CCI full well charge capability, which tends to improve the operational antiblooming mode, but causes the CCI to saturate sooner. With the present ALC configuration it is felt that an optimum characteristic has been chosen, total containment of a 10 times overload and greatly reduced blooming for a 64 times overload.

Geometric distortion of the TV camera due to the CCI fixed geometry is insignificant. The measurement of less than 1% across the complete format is attributable solely to the lens.

There is room for improvement in the operating characteristics of the TV camera but this is based upon improvement of the CCI device itself. The electronic circuitry associated with the TV camera makes optimum use of the operational characteristics of the CCI at its present stage of development.

APPENDIX "A"

OPERATIONAL MODE STUDIES

The following pages contain the results of an investigation performed by the RCA Laboratories relating to measurements of gamma, MTF, and the effect of the A-B transfer frequency.

Internal Correspondence

RCA

To K. Zaininger Location Date May 6, 1975

From P. Levine Location Telephone 2923

Subject

Measurements have been performed on a 512 x 320 charge-coupled imager (No. 268-6) supplied to us by E.C. Lancaster. The sensor was made on their production line and is said to be typical in resolution and defects of device manufactured at that time. The measurements made were:

I. Gamma at wavelengths of 1100 nm, 700 nm and 450 nm
II. MTF with and without infrared filtering
III. Effect of image area to store area transfer frequency in vertical resolution and well size

I. Measurement of Gamma

Measurements were made of illumination versus current output at the output register drain as well as determination of the transfer function between the output register drain current and the on-chip, floating diffusing-MOS amplifier operated as a source follower.

The transfer function between sensor illumination and CCD drain current was measured in both the blooming and operational non-blooming modes. The illumination source was a monochrometer projecting a circle on the sensor. The diameter of the circle was equal to the picture height. Measurements were performed at wavelengths of 1100 nm, 700 nm and 450 nm. These wavelengths were chosen because they represent the longest usable wavelength, the wavelength of peak response and the shortest usable wavelength. Results are plotted in figures 1, 2 and 3.

We found a sensitivity reduction of 20% in the operational anti-blooming mode due to recombination of optically generated electrons under the accumulated anti-blooming gates.

Figure 4 gives the transfer function between output register drain current and the video output of the on-chip MOS floating diffusion amplifier operated as a source follower with a 5K load resistor.

II. Measurement of Modulation Transfer Function

MTF measurements were made at the center of the format using 40 w tungsten illumination. Horizontal MTF was measured with and without an infrared rejecting filter in place and vertical MTF was measured only with the filter. The lens used in our measurements was a Cosmicar, 25 mm, f 1.4 television lens (No. 20821).

A-2

The test pattern used varied sinusoidally in density with position. As the frequency of the sinewave approached the sensor pitch the camera was panned across the pattern. This smoothed out the peaking and nulling effect seen as a function of phase between the test pattern and the sensor sample locations. The vertical and horizontal MTF measured with an IR rejecting filter are plotted in figure 5. The faster than expected drop in MTF at lower spatial frequencies in the plateau from 200 to 250 lines/picture height may be due to dispersion effects of the image passing through the polysilicon device structure. This effect is illustrated in figure 6. The horizontal MTF, with and without IR filtering is given in figure 7. The response of the IR filter is plotted in figure 8.

III. Effect of A to B Register Vertical Transfer Rate

The maximum usable transfer rate from the image to storage register is determined by dispersion of the transfer pulses in the resistive polysilicon transfer electrodes. Because the A and B registers are double end connected this effect is worst in the center of the imager. The effect of pulse dispersion is to reduce transfer efficiency and well size. Our measurements consisted of vertical resolution in lines/picture height and relative well size in the center of the picture. Florescent illumination was used without IR filtering.

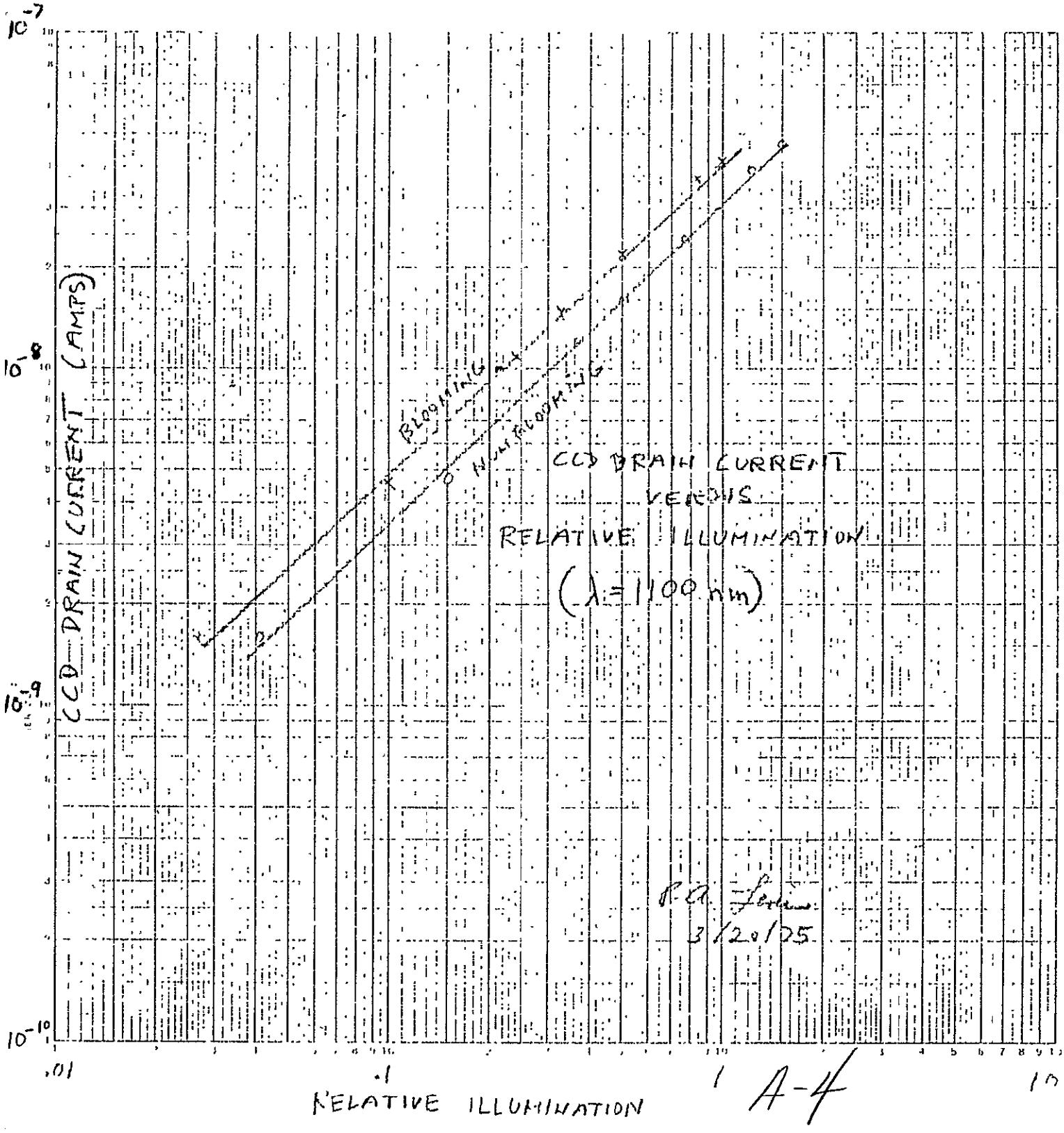
The results for an 8.6 peak to peak transfer pulse are given in figure 9.

P. A. Levine

P. Levine

/lam

Distribution: J. Carnes - Princeton
D. Giovachino - Lancaster
M. Kravitz - Astro
R. L. Rogers - Lancaster
B. Soltoff - Astro



A-4

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Fig. 1

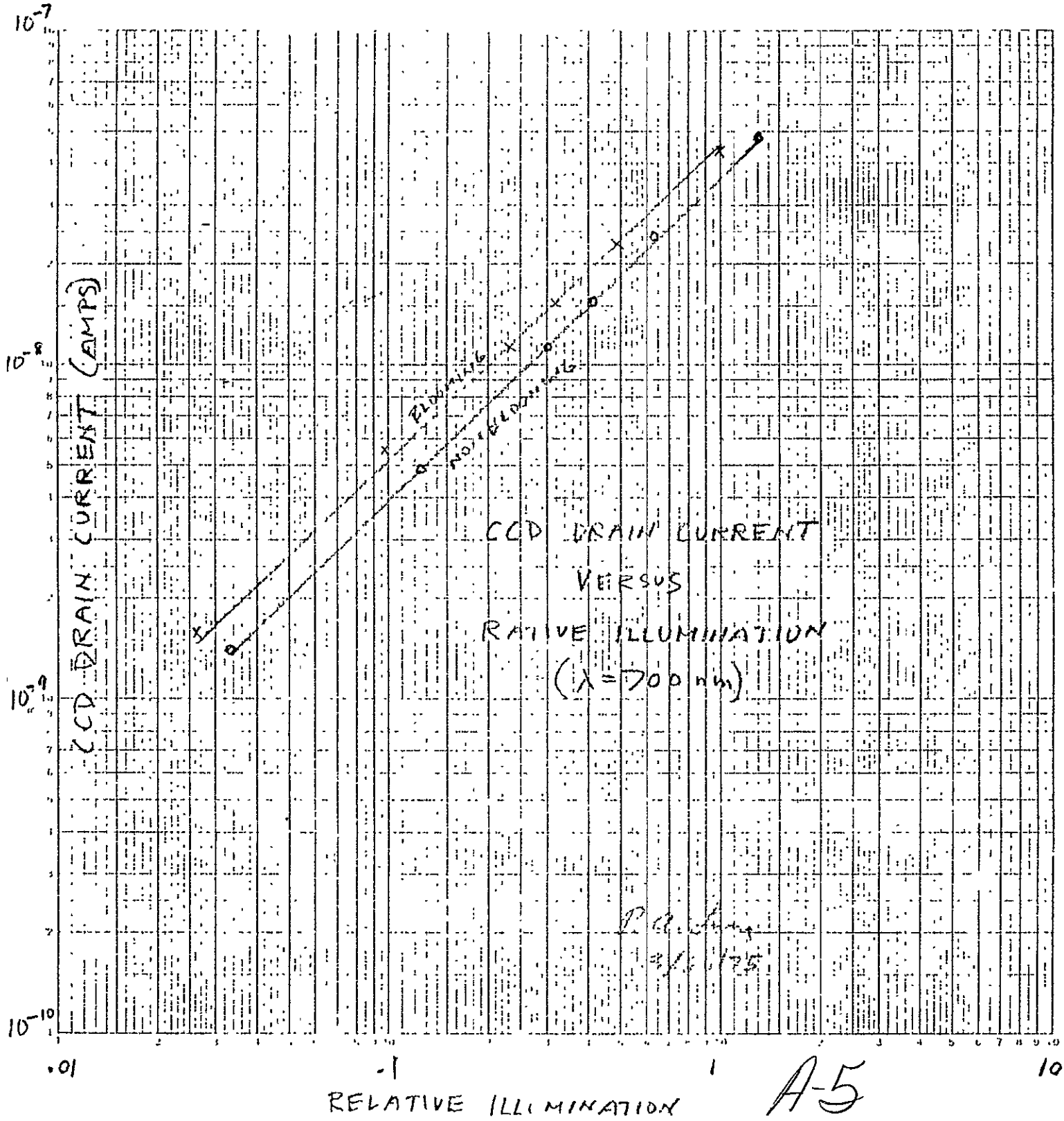

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Fig. 2

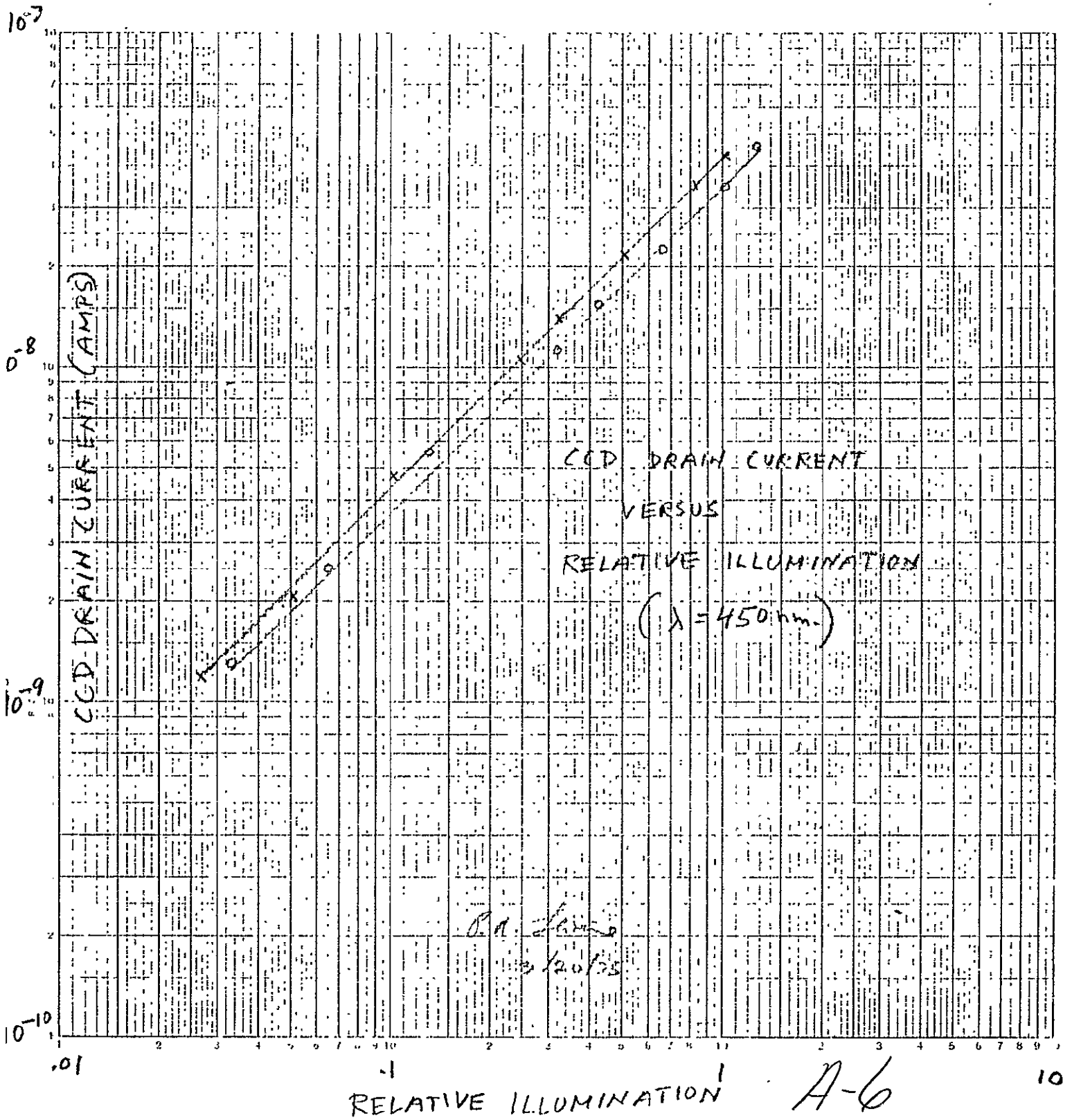

CCD DRAIN CURRENT VERSUS RELATIVE ILLUMINATION (λ = 450nm.)
CCD DRAIN CURRENT (AMPS)
RELATIVE ILLUMINATION
10^-7
10^-8
10^-9
10^-10
.01
.1
1
10
A-6

Fig. 3

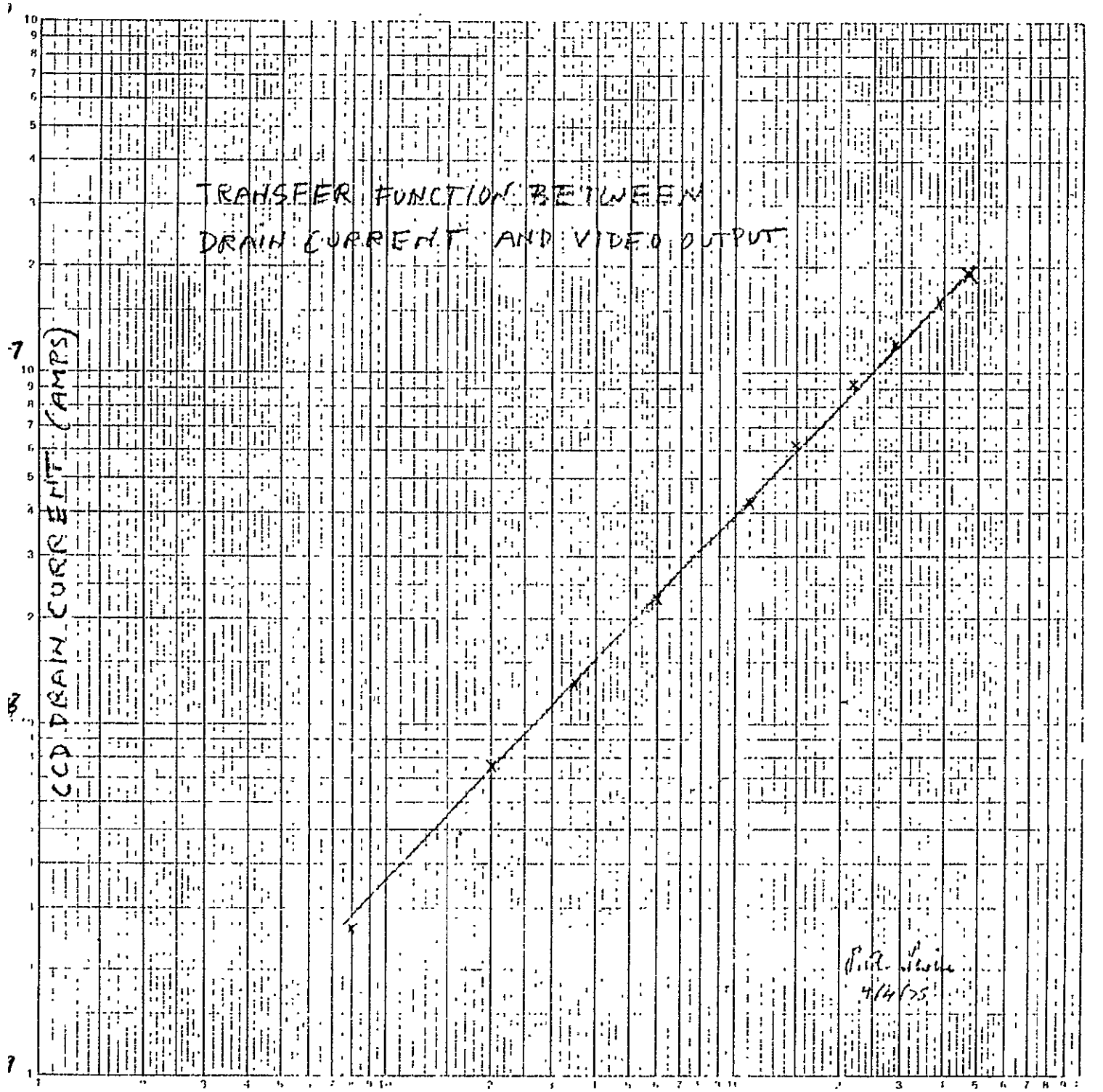


Fig. 4

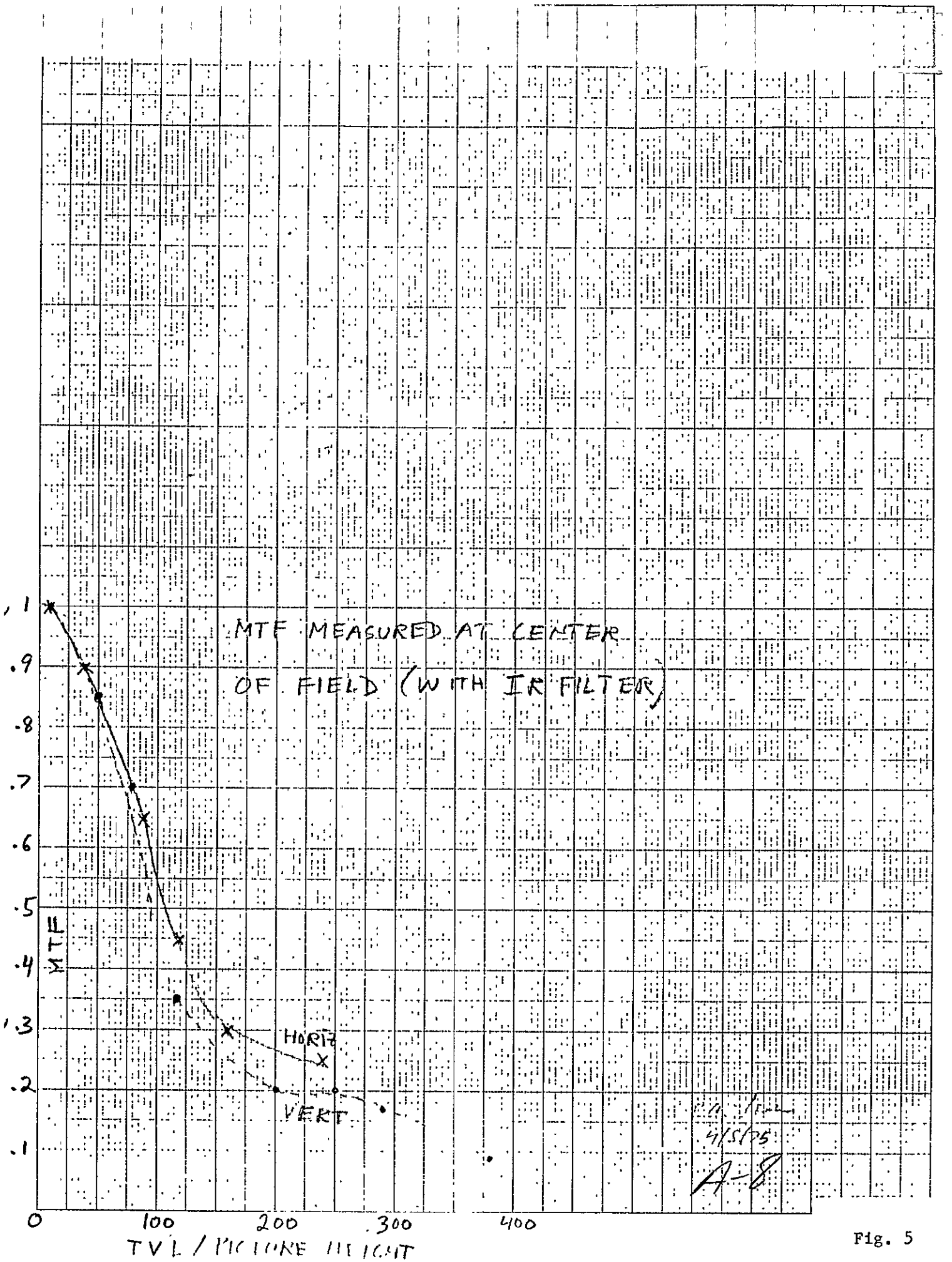

MTF MEASURED AT CENTER
OF FIELD (WITH IR FILTER)
MTF
1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1
HORIZ
VERT
0
100
200
300
400
TVL / PICTURE HEIGHT

Fig. 5

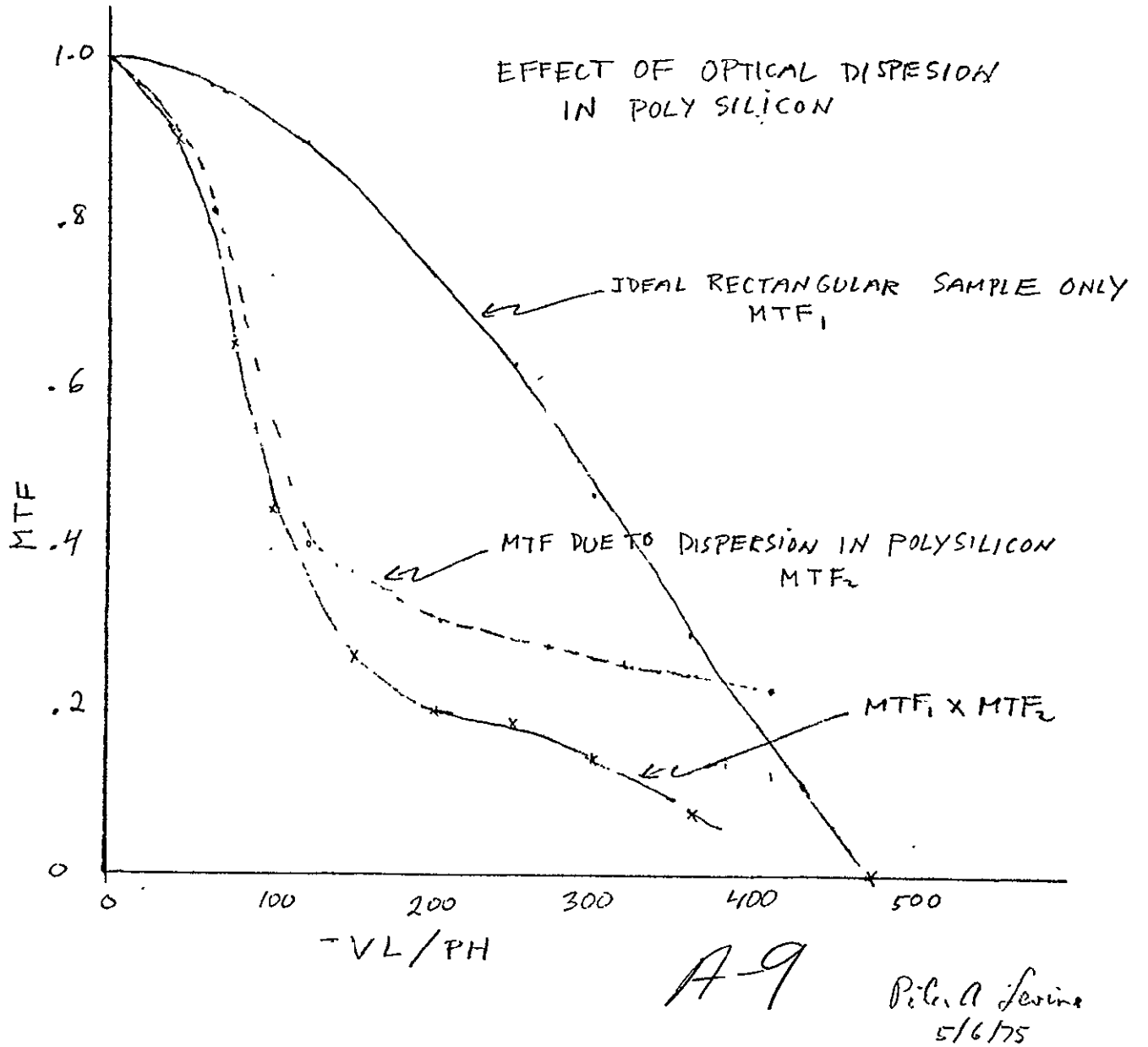


Fig. 6

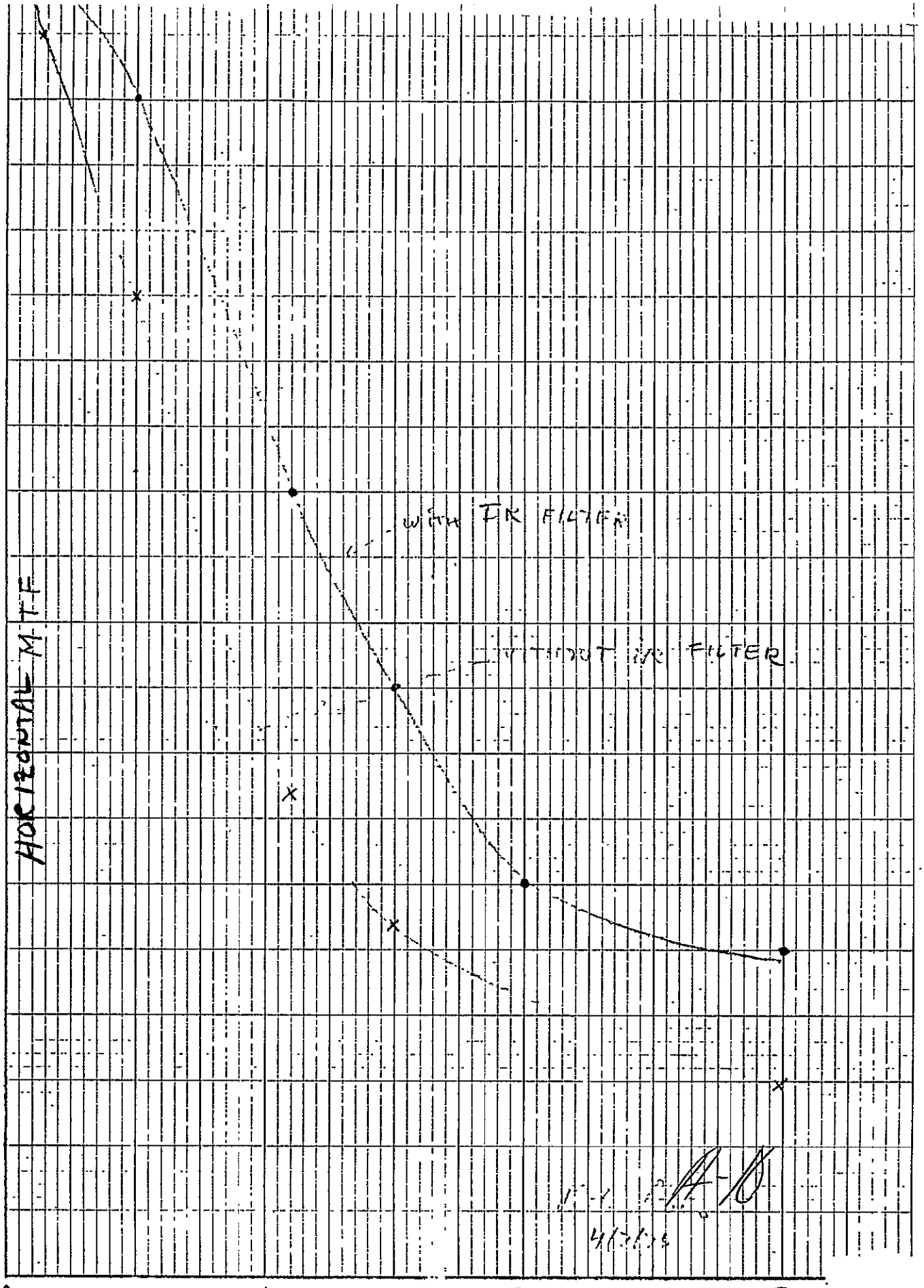
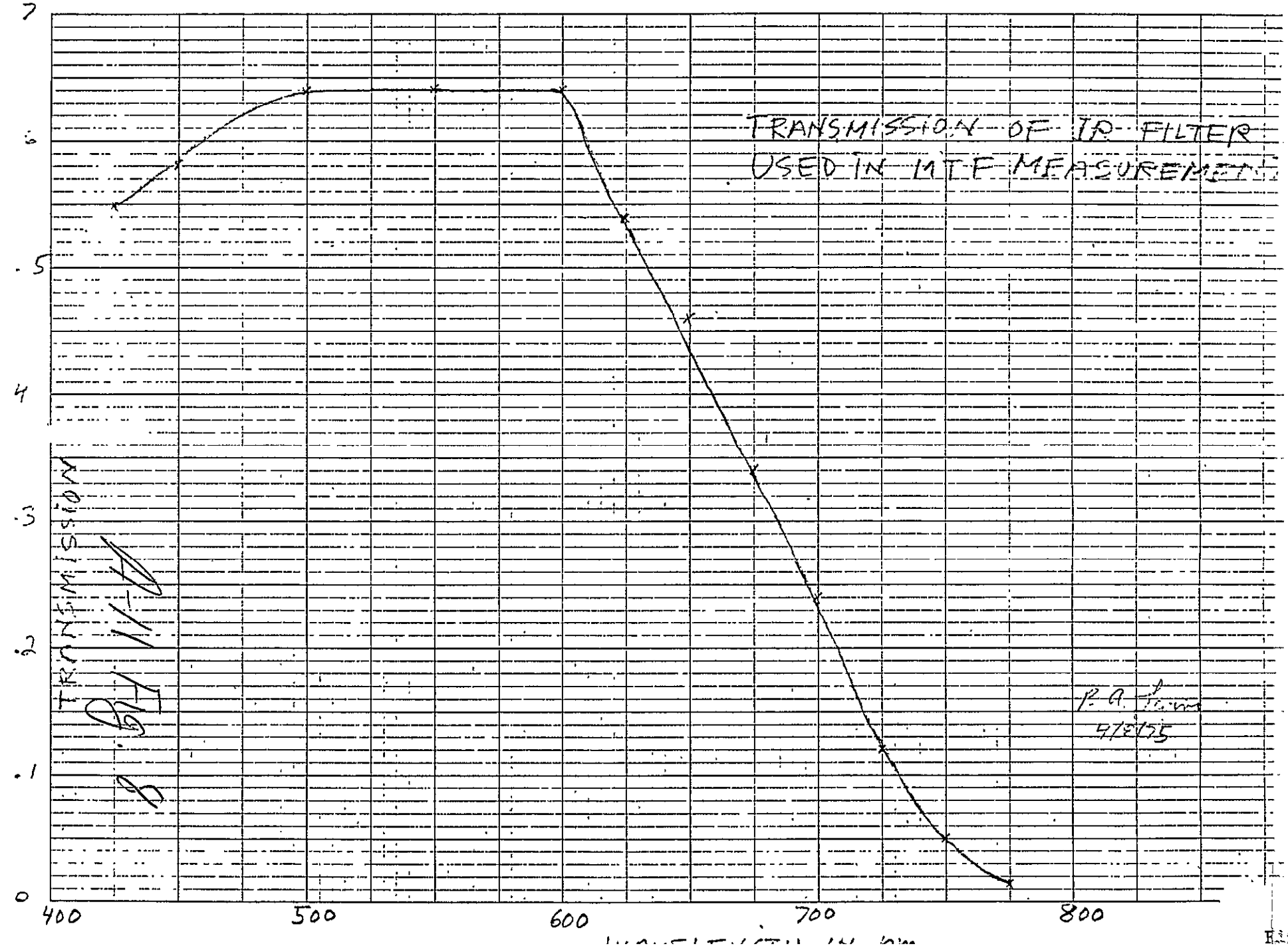
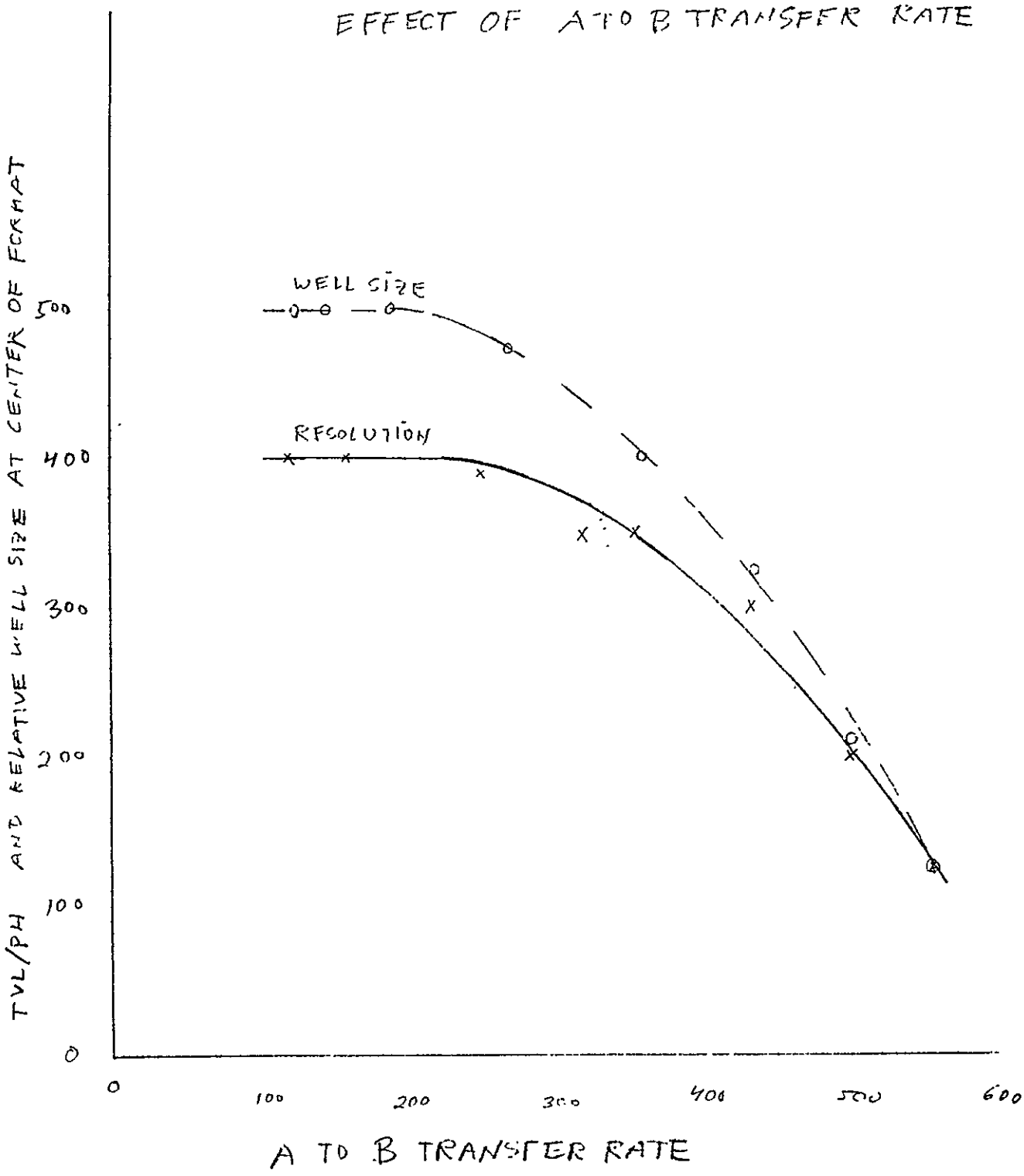

HORIZONTAL MTF
WITH FR FILTER
WITHOUT FR FILTER
0
1
2
3
MODULATION FREQUENCY

Fig.


TRANSMISSION OF ID FILTER
USED IN MTF MEASUREMENT
P.A. Lamm
4/8/05
TRANSMISSION
WAVELENGTH IN nm
0
.1
.2
.3
.4
.5
.6
.7
400
500
600
700
800



A-12

Peter A. Levine
May 5, 1975

Fig. 9

APPENDIX "B"

ENGINEERING DRAWINGS

The following pages contain copies of the applicable engineering drawings developed during the contract. These drawings are identified as follows:

Drawing No.	Title
SK 2282865	Schematic, A1 Board, Clock, C-Reg Ø
SK 2288230	Assembly, A1 Board, Clock, C-Reg Ø
SK 2282866	Schematic, A2 Board, Divider, Vertical Timing, A-B Reg Ø Generator
SK 2288229	Assembly, A2 Board, Divider, Vertical Timing, A-B Reg Ø Generator
SK 2288440	Schematic, A3 Board, Sync Generator, A&B Reg Drive
SK 2288228	Assembly, A3 Board, Sync Generator, A&B Reg Drive
SK 2282868	Schematic, A4 Board, AGC, Video Output
SK 2273625	Assembly, A4 Board, AGC, Video Output
SK 2282869	Schematic, A5 Board, ALC
SK 2273624	Assembly, A5 Board, ALC
SK 2288240	Assembly, A6 Board, Harness Board
SK 2282870	Schematic, A7 Board, CCD Mount
SK 2288241	Assembly, A7 Board, CCD Mount
SK 2282871	Interconnection Diagram
SK 2288259	Assembly, CCD Sensor Housing

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REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED

FOR REVISIONS ONLY

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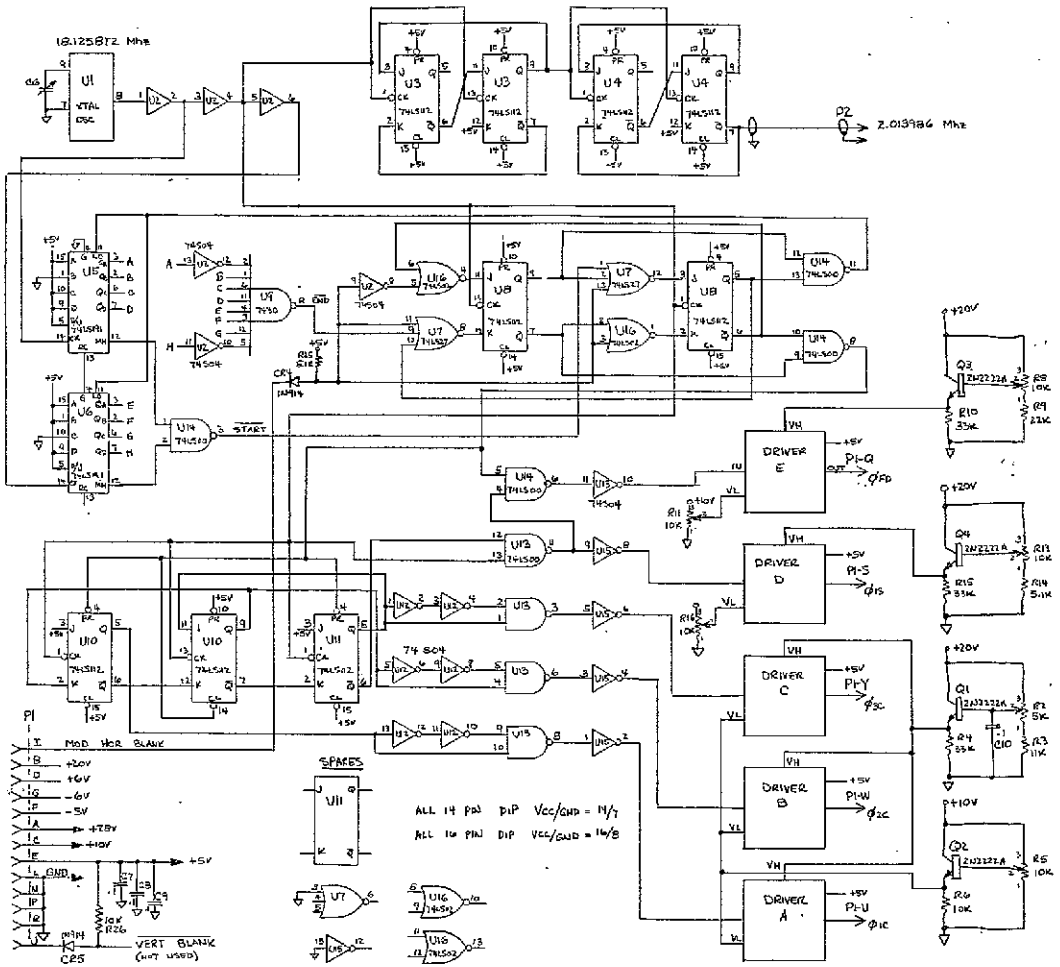

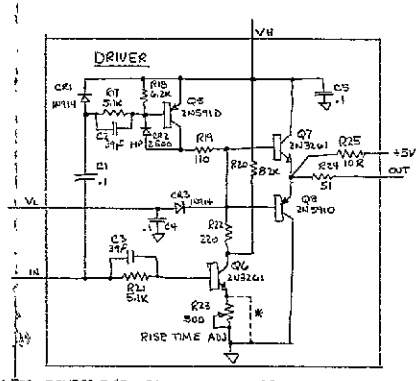

* FOR DRIVERS E-ED, Q6 EMITTER IS GROUND

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SKETCH

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THD DATA TO BE INTERPRETED USING HNDBK H28 AND MIL-STD-9

RCA COMMODITY CODE

SECURITY CLASSIFICATION

UNLESS OTHERWISE SPECIFIED THE SURF. FIN. OF MACHINED PARTS SHALL NOT EXCEED A MAX READING OF 125 PER MIL-STD-10 ✓

DIMENSIONS AND TOLERANCES PER MIL-STD 8

NEXT ASSY	USED ON

FIRST APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES ON			
BASIC DIMENSIONS	2 PLACE DECIMALS	3 PLACE DECIMALS	
UP TO 6	± .02	± .005	
ABOVE 6 TO 24	± .03	± .010	
ABOVE 24	± .06	± .015	

ANGULAR DIMENSIONS ± 1/2°

MATERIAL:

CONTRACT NO. NAS 9-14477

SHOP ORDER NO.

DRAWN BY R HETHERINGTON DATE 7-21-75

DESIGN ACTIVITY APPD. M. Krawitz DATE 7/22/75

RADIO CORPORATION OF AMERICA
NEW YORK, N.Y.
ASTRO-ELECTRONICS DIVISION, PRINCETON, N.J., PLANT

SOLID STATE TV CAMERA

SCHEMATIC A1 ~ CLOCK, C REG Ø DRIVE

SIZE	CODE IDENT NO.	
C	49671	SK 2282865

SCALE	WEIGHT	SHEET 1 OF 1

AED 739-2 3/66

REVISIONS				
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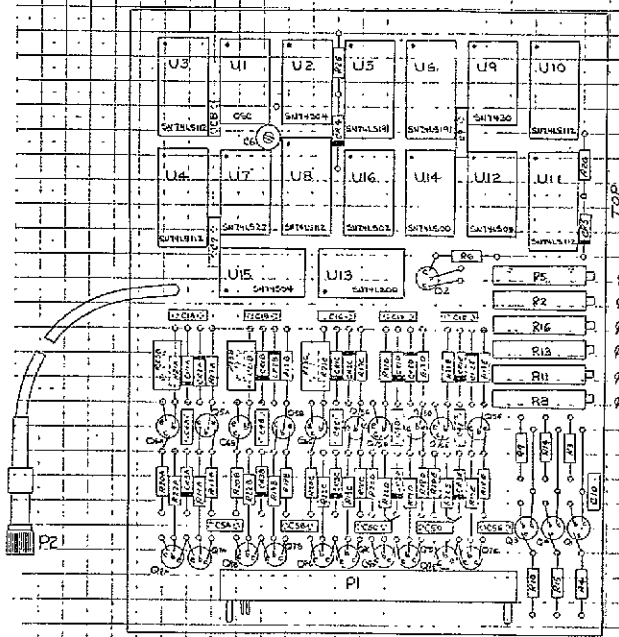
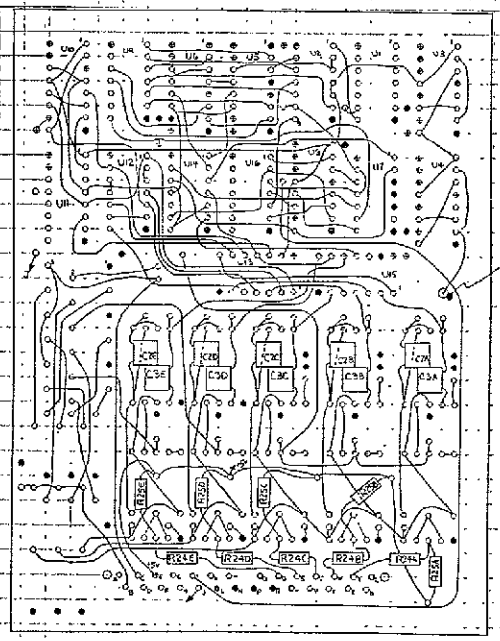
B		ADD R2, R45, C45, R24 DELETE R1, R12	10-13-15	RH





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-B	Q3C		+20V
-C	D2C		+10V
-D			+6V
-E	R25E		+5V
-F			-5V
-G			-6V
-H			
-I	CR4		MOD HOR BLANK
-J	CR5		VERT BLANK
-K			
-L			GND
-M			
-N			GND
-O			
-P			GND
-Q	R24E		GND
-R			GND
-S	R24D		
-T			
-U	R24C		
-V			
-W	R24B		
-X			
-Y	R24A		
-Z			
-a			
-b			

+15V
GND

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B-3

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LIST OF MATERIALS

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COMMODITY CODE	
DRAWN	DATE
R. HETHERINGTON	6-13-15
CHECKED	DATE
DESIGN ACTIVITY APPD	DATE

RADIO CORPORATION OF AMERICA
CAMDEN, N J
PLANT

SOLID STATE TV CAMERA

A1 ~ CLOCK, C REG Ø DRIVE

CODE IDENT NO	SIZE	
49671	D	SK 2288230
SCALE 2/1	WEIGHT	SHEET 1 OF 1

DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES ON FINISHED DIMENSIONS UNLESS OTHERWISE SPECIFIED

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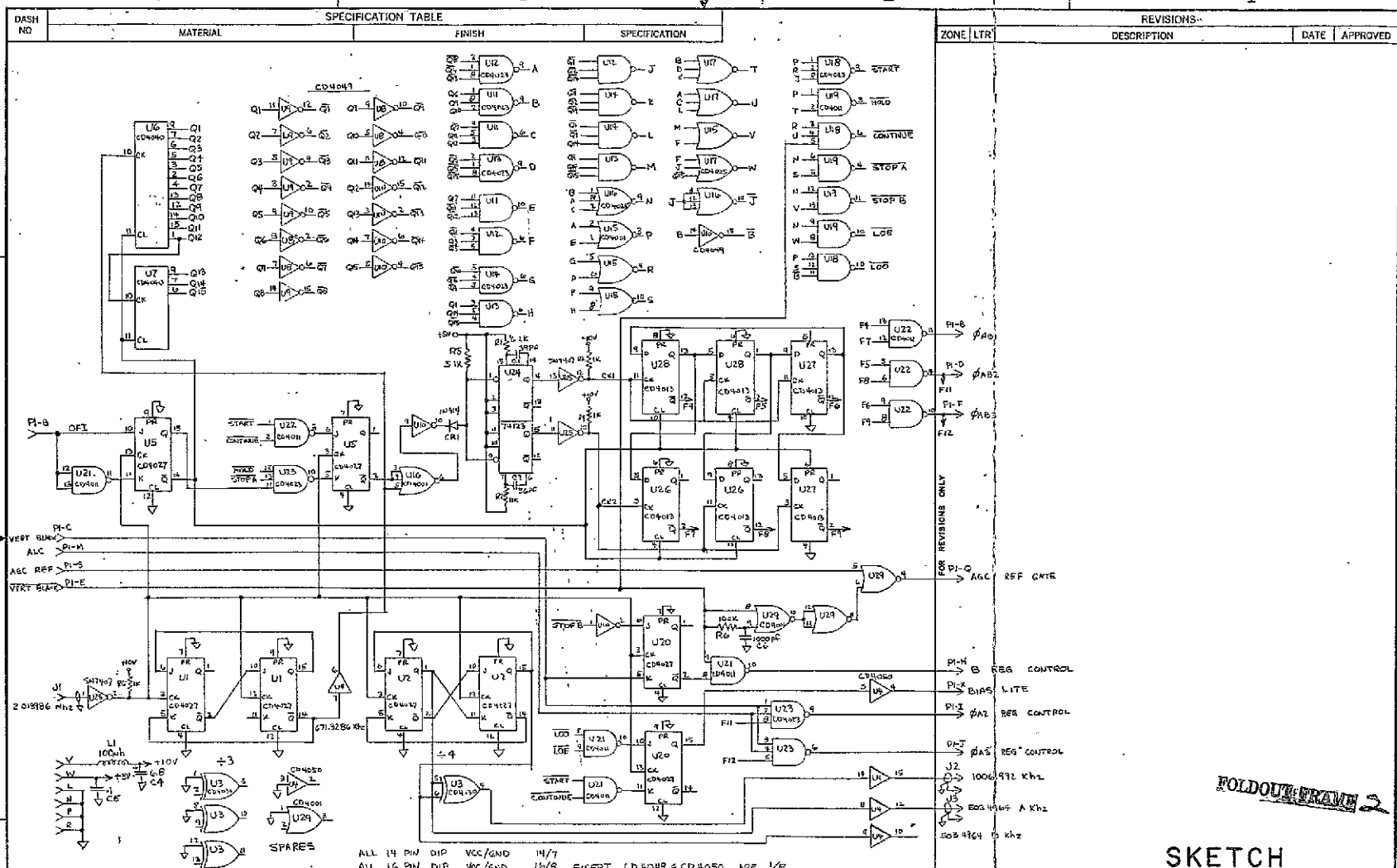
UP TO 6	± .02	± .005
OVER 6 TO 24	± .03	± .010
ABOVE 24	± .06	± .015
ANGULAR DIMENSIONS	± 1°	

SEE RCA PUNCH SPEC FOR STOCK SIZ.

ALL EXTERNAL THREADS TO BE CLASS 2A BEFORE PLATING AND CLASS 2 AFTER PLATING
ALL INTERNAL THREADS TO BE CLASS 2B UNLESS OTHERWISE SPECIFIED

FIRST MADE FOR	
NEXT ASS'Y	USED ON



DASH NO	SPECIFICATION TABLE		
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REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED

FOR REVISIONS ONLY

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THD DATA TO BE INTERPRETED USING HNDBK H28 AND MIL-STD 9

SECURITY CLASSIFICATION

UNLESS OTHERWISE SPECIFIED THE SURF. FIN. OF MACHINED PARTS SHALL NOT EXCEED A MAX READING OF 125/PER MIL-STD-10

DIMENSIONS AND TOLERANCES PER MIL-STD-8

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES ON		
BASIC DIMENSIONS	2 PLACE DECIMALS	3 PLACE DECIMALS
UP TO 6	± .02	± .005
ABOVE 6 TO 24	± .03	± .010
ABOVE 24	± .06	± .015

ANGULAR DIMENSIONS ± 1/2°

MATERIAL:

NEXT ASSY | USED ON

FIRST APPLICATION

RCA COMMODITY CODE

CONTRACT NO. NAS 9-14477

SHOP ORDER NO.

DRAWN BY R HETHERINGTON DATE 10-21-75

DESIGN ACTIVITY APPD. DATE

RADIO CORPORATION OF AMERICA
NEW YORK, N.Y.
ASTRO-ELECTRONICS DIVISION, PRINCETON, N.J. PLANT

SOLID STATE TV CAMERA

SCHEMATIC A2 ~ DIVIDER, VERT TIMING
A-B REG ϕ GEN

B-4

SIZE C | CODE IDENT NO. 49671 | SK 2282866

SCALE | WEIGHT | SHEET 1 OF 1

AED 739-2 3/66

REVISIONS			
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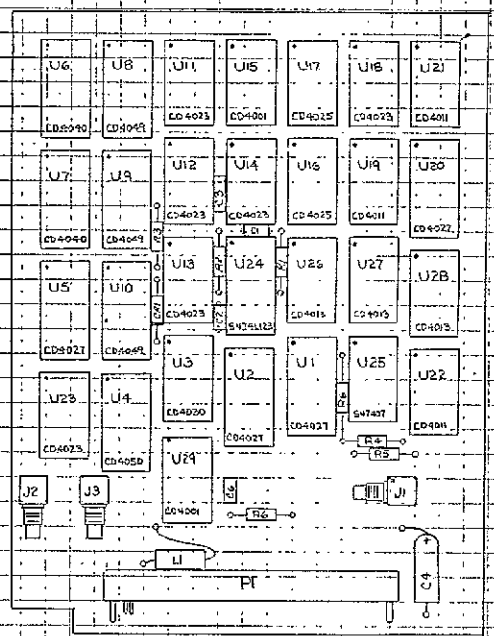
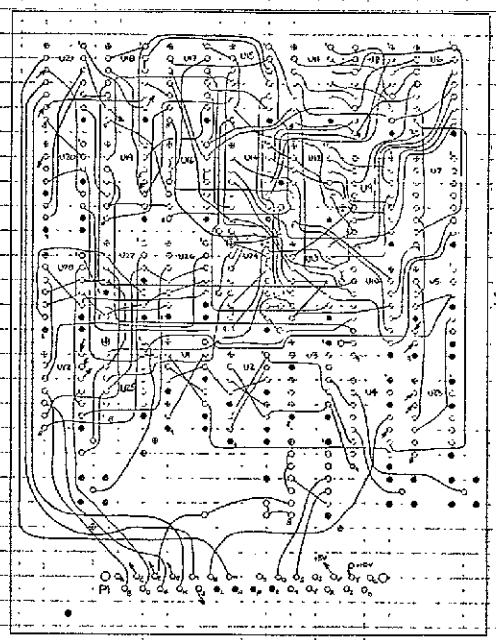
B		ADD L1, J1 J2 J5 C6, R4, U29	10-22-75 RH





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U18-6	U22-2	
U19-3	U23-12	
U19-4	U23-13	
U22-3	U5-6	
U5-2	U14-3	
U4-6	U16-5	
U16-6	U10-9	
U20-13	U5-5	
P1-A		
-B	U22-11	WACI
-C	U20-5	VERT BLANK
-D	U22-4	@A32
-E	U28-8	VERT BLANK
-F	U22-10	@A23
-G	U5-10	CPT
-H	U21-10	B REG CONT
-I	U23-9	@A2 REG CONT
-J	U23-6	@A3 REG CONT
-K	U24-4	BIRS LITE
-L		GND
-M	U23-2	AGC
-N		GND
-O		
-P		GND
-Q	U29-9	AGC REF GATE
-R		GND
-S	U29-5	AGC REF
-T		
-U		
-V		
-W		+5V
-X		
-Y		+10V
-Z		
-AA		
-BB		
	@ +10V	
	@ +5V	
	● GND	

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B-5

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CONTRACT NO. NAS9-14477

COMMODITY CODE

DRAWN [illegible] DATE 6-17-75

CHK'D DATE

ENGR ACTIVITY APPD DATE

RADIO CORPORATION OF AMERICA
CAMDEN N J
PLANT

SOLID STATE TV CAMERA

A2 - DIVIDER, VERT TIMING CONTROL, A-15 REG & GEN

CODE IDENT NO	SIZE	SK 2288229
49671	D	

SCALE 2:1 WEIGHT SHEET 1 OF 1

DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES ON UNDIMENSIONED DIMENSIONS UNLESS OTHERWISE SPECIFIED

BASIC DIMENSIONS	2 PLACE DECIMALS	3 PLACE DECIMALS
UP TO 5	± 02	± 005
OVER 5 TO 24	± 03	± 010
ABOVE 24	± 06	± 015

ANGULAR DIMENSIONS ± 1°

SEE [illegible] FOR STOCK TOL

FIRST MADE FOR	
NEXT ASS'Y	USED ON

ALL EXTERNAL THREADS TO BE CLASS 2A BEFORE PLATING AND CLASS 2 AFTER PLATING. ALL INTERNAL THREADS TO BE CLASS 2B UNLESS OTHERWISE SPECIFIED.

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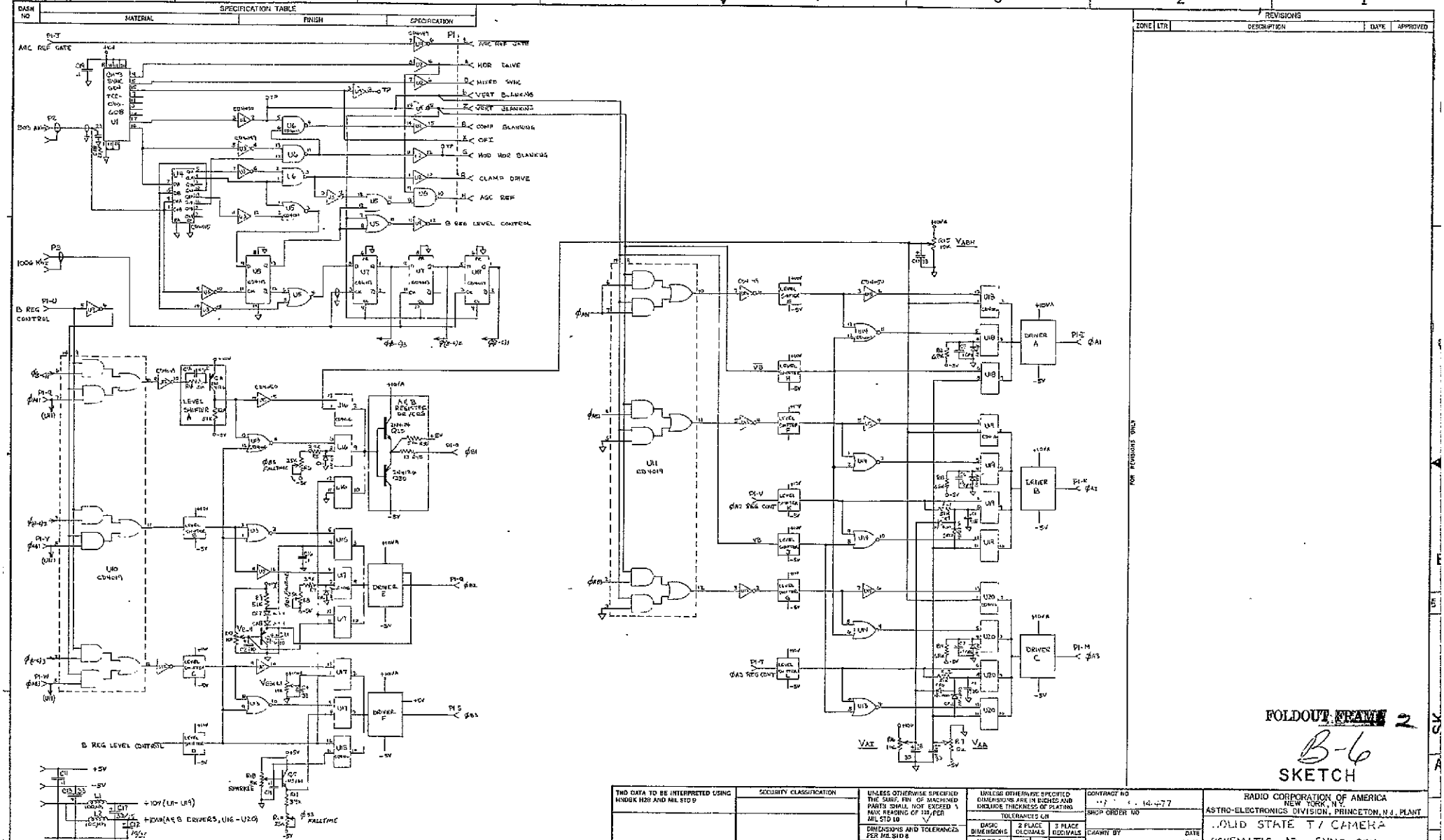

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B-6

SKETCH

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED

THD DATA TO BE INTERPRETED USING HNDBK H28 AND MIL STD 9	SECURITY CLASSIFICATION	UNLESS OTHERWISE SPECIFIED THE SURF. FIN. OF MACHINED PARTS SHALL NOT EXCEED ½ MAX READING OF 125 PER MIL STD 10
		DIMENSIONS AND TOLERANCES PER MIL STD 8
RCA COMMODITY CODE		NEXT ASSY / USED ON / FIRST APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING.

TOLERANCES ON

BASIC DIMENSIONS	2 PLACE DECIMALS	3 PLACE DECIMALS
UP TO 6	± .02	± .005
OVER 6 TO 24	± .03	± .010
ABOVE 24	± .06	± .015

ANGULAR DIMENSIONS ± 1°

MATERIAL

CONTRACT NO

SHOP ORDER NO

DRAWN BY — DATE 12-24-73

DESIGN ACTIVITY APPD — DATE 10/29/75

RADIO CORPORATION OF AMERICA
NEW YORK, N.Y.
ASTRO-ELECTRONICS DIVISION, PRINCETON, N.J. PLANT

SOLID STATE TV CAMERA
SCHEMATIC A8, SYNC GEN,
A&B REG DRIVE

SIZE D | CODE IDENT NO. 49671 | SK 2288440

SCALE — WEIGHT — SHEET 1 OF 1

AEO 730-2 3/66

REVISIONS			
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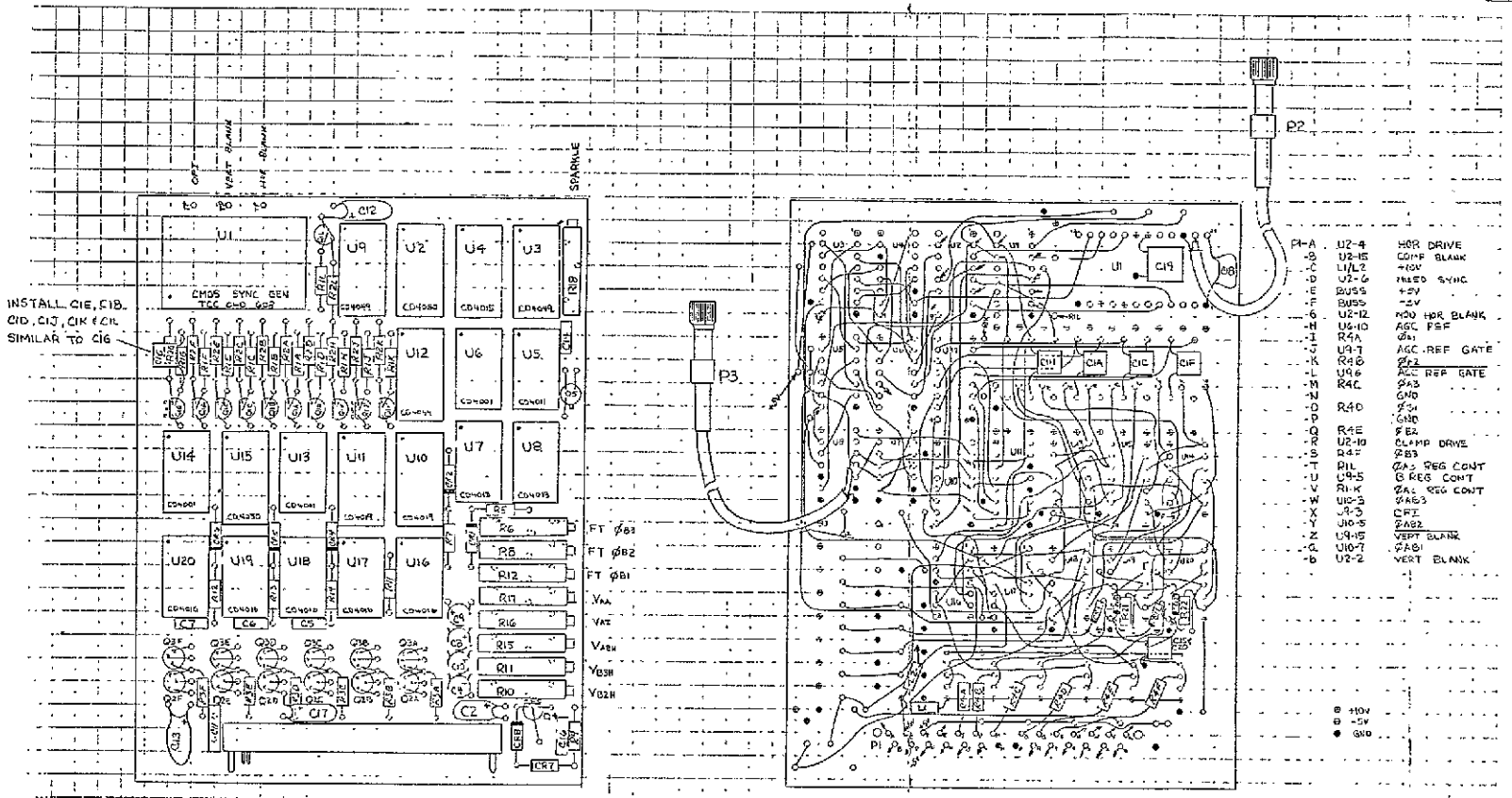

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B-7

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ORIGINAL PAGE IS OF POOR QUALITY

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							LIST OF MATERIALS

CONTRACT NO NAS 8-14477

COMMODITY CODE

DRAWN D. HETHERINGTON 6-19-75

CHECKED

DESIGN ACTIVITY APPD

RADIO CORPORATION OF AMERICA CAMDEN, N.J. PLANT

SOLID STATE TV CAMERA

SYNC GEN, 15.7 Khz REG, A&G REG DRIVE ~ A3

CODE IDENT NO 49671 SIZE D SK 2288228

SCALE 2:1 WEIGHT SHEET 1 OF 1

DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING.

BASIC DIMENSIONS	2 PLACE DECIMALS	3 PLACE DECIMALS
UP TO 6	± .02	± .005
OVER 6 TO 24	± .03	± .010
ABOVE 24	± .05	± .015

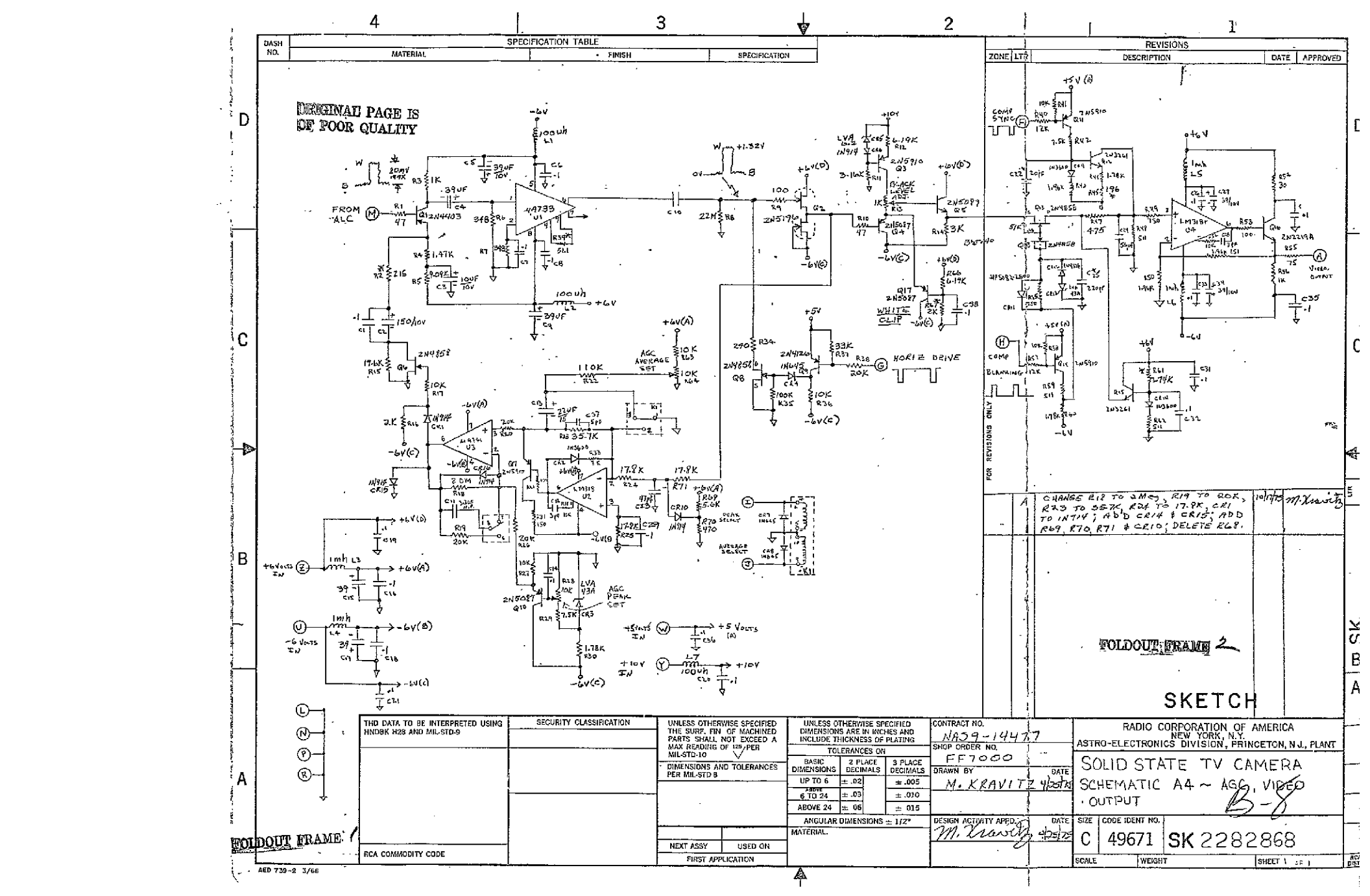
ANGULAR DIMENSIONS ± 1/2°

FIRST MADE FOR	USED ON
NEXT ASS'Y	

ALL EXTERNAL THREADS TO BE CLASS 2A BEFORE PLATING AND CLASS 2 AFTER PLATING ALL INTERNAL THREADS TO BE CLASS 2B UNLESS OTHERWISE SPECIFIED

SEE RCA PURCH SPEC FOR STOCK SIZES

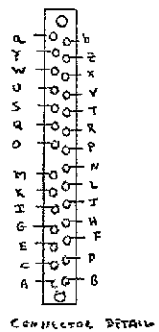
RCA 15168 PRINTED IN U.S.A. SPEIDEL & CO

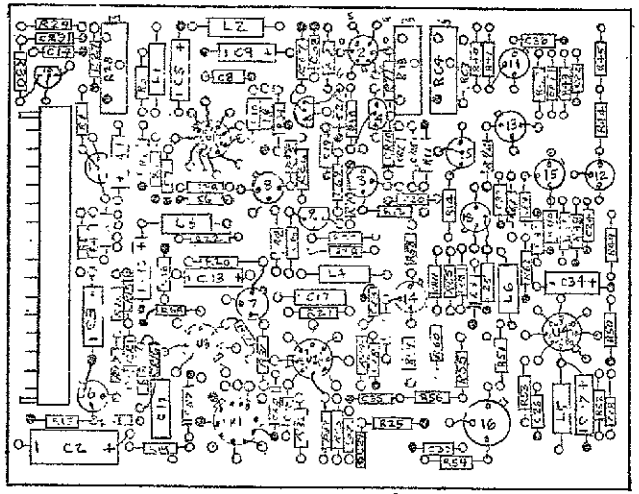

ORIGINAL PAGE IS OF POOR QUALITY
SPECIFICATION TABLE
DASH NO.
MATERIAL
FINISH
SPECIFICATION
REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
FOR REVISIONS ONLY
A
CHANGE R12 TO 3MEG, R19 TO 20K, R23 TO 35.7K, R24 TO 17.8K, CR1 TO 1N714; ADD CR14 & CR15; ADD R69, R70, R71 & CR10; DELETE R68.
10/17/75
M. Kravitz
FOLDOUT FRAME 2
SKETCH
FROM ALC
HORIZ DRIVE
COMP SYNC
COMP BLANKING
WHITE CLIP
BLACK LEVEL ADJ
AGC AVERAGE SET
AGC PEAK SET
VIDEO OUTPUT
FOLDOUT FRAME 1
THD DATA TO BE INTERPRETED USING HNDBK H28 AND MIL-STD-9
SECURITY CLASSIFICATION
UNLESS OTHERWISE SPECIFIED THE SURF. FIN OF MACHINED PARTS SHALL NOT EXCEED A MAX READING OF 125 PER MIL-STD-10
DIMENSIONS AND TOLERANCES PER MIL-STD 8
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING
TOLERANCES ON
BASIC DIMENSIONS
2 PLACE DECIMALS
3 PLACE DECIMALS
UP TO 6
± .02
± .005
ABOVE 6 TO 24
± .03
± .010
ABOVE 24
± .06
± .015
ANGULAR DIMENSIONS ± 1/2°
MATERIAL
NEXT ASSY
USED ON
FIRST APPLICATION
RCA COMMODITY CODE
CONTRACT NO.
NAS9-14477
SHOP ORDER NO.
FF7000
DRAWN BY
M. KRAVITZ
DATE
4/25/75
DESIGN ACTIVITY APPD.
M. Kravitz
DATE
4/25/75
RADIO CORPORATION OF AMERICA
NEW YORK, N.Y.
ASTRO-ELECTRONICS DIVISION, PRINCETON, N.J., PLANT
SOLID STATE TV CAMERA
SCHEMATIC A4 ~ AGC, VIDEO · OUTPUT
B-8
SIZE
C
CODE IDENT NO.
49671
SK 2282868
SCALE
WEIGHT
SHEET 1 OF 1
AED 739-2 3/66

FOLDOUT FRAME

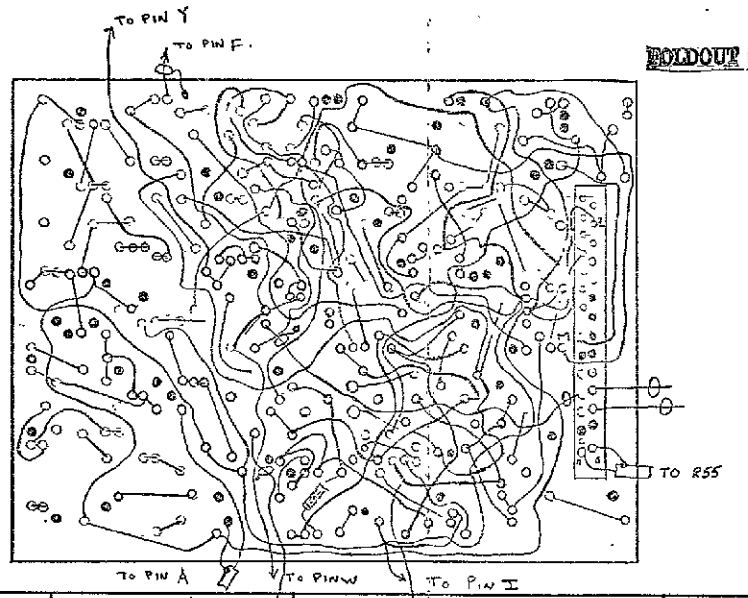
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ADD CR15, CR16, CR17, R69, R70, R71; MOVE R55, C27, & C25	10/23/75	M Zaworski

ORIGINAL PAGE IS OF POOR QUALITY





FOLDOUT FRAME 2



NOTES:
1. ALL TRANSISTORS AND INTEGRATED CIRCUITS SHOWN TOP VIEW
2. ● DENOTES CONNECTION TO GROUND PLANE
3. CR2 INSTALLED ON JUMPER WIRE SIDE OF BOARD
4. USE SHIELDED WIRE ON PINS A, F, G, H

QTY REQD PER DASH NO.	CODE IDENT	IDENTIFYING NO.	DESCRIPTION	SPECIFICATION	SEE NOTE NO.

MATERIALS AND SPECIFICATIONS

B-9

REVISION STATUS WHERE MORE THAN ONE SHEET			
SH	REV	SH	REV

THD DATA TO BE INTERPRETED USING NBS HDBK H28 AND MIL-STD-9

INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5-66

RCA COMMODITY CODE:

UNLESS OTHERWISE SPECIFIED THE SURFACE FINISH OF MACHINED PARTS SHALL NOT EXCEED A MAXIMUM READING 125 PER ANSI STD B46.1 — 1962

NEXT ASSY	USED ON
FIRST APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES ON: BASIC DIMENSIONS	2 PLACE DECIMALS	3 PLACE DECIMALS
UP TO 6	± .02	± .010
ABOVE 6 to 24	± .03	± .015
ABOVE 24	± .06	± .020

ANGULAR DIMENSIONS ± ½°

MATERIAL: SEE TABLE

CONTRACT NO. NAS9-14477 REL

DRAWN BY F.G. HUBIT DATE 6-10-75

CHECKED BY DATE

DESIGN ACTIVITY APPD Frank D Hubit 6-10-75 DATE

RCA CORPORATION | NEW YORK, NY

ASTRO ELECTRONICS DIV., PRINCETON, N.J. PLANT

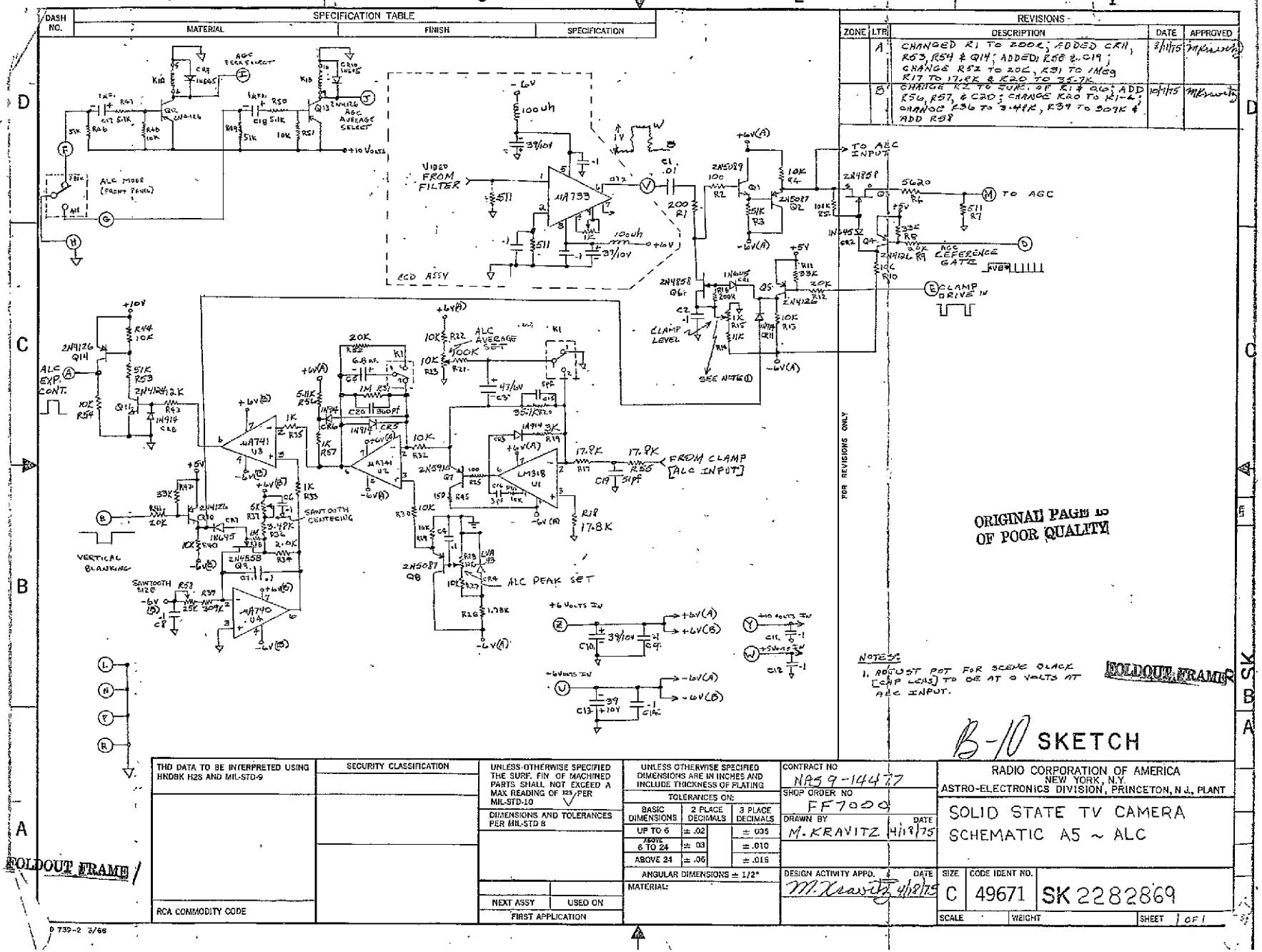
SOLID STATE TV CAMERA

A4 ~ AGC & VIDEO OUTPUT ASSY

SIZE	CODE IDENT NO.	
B	49671	SK2273625

SCALE WEIGHT SHEET 1 OF 1

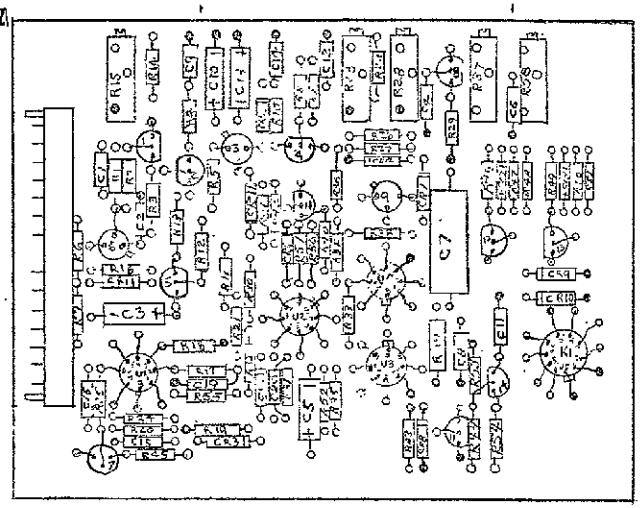
RCA 2417-3 (4-71) 7069

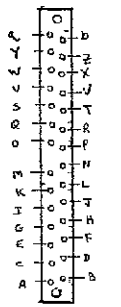

SPECIFICATION TABLE
DASH NO. | MATERIAL | FINISH | SPECIFICATION
REVISIONS -
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | CHANGED R1 TO 200K; ADDED CR11, R53, R54 & Q14; ADDED R56 & C19; CHANGE R52 TO 20K, R51 TO 1MEG R17 TO 17.8K & R20 TO 35.7K | 3/11/75 | MKravitz
B | CHANGE R2 TO SUM OF R1 & R6; ADD R56, R57, & C20; CHANGE R20 TO R1-4; CHANGE R36 TO 3.48K, R39 TO 309K & ADD R58 | 10/14/75 | MKravitz
ALC MODE (FRONT PANEL)
VIDEO FROM FILTER
ECD ASSY
TO ALC INPUT
TO AGC
AGC REFERENCE GATE
CLAMP DRIVE IN
CLAMP LEVEL
SEE NOTE 1
ALC AVERAGE SET
ALC EXP. CONT.
FROM CLAMP [ALC INPUT]
ALC PEAK SET
SAWTOOTH CENTERING
SAWTOOTH SIZE
VERTICAL BLANKING
FOR REVISIONS ONLY
NOTES:
1. ADJUST POT FOR SCENE BLACK [CAMP LEAD] TO BE AT 0 VOLTS AT ALC INPUT.
FOLDOUT FRAME
ORIGINAL PAGE IS OF POOR QUALITY
B-10 SKETCH
THD DATA TO BE INTERPRETED USING HNDBK H2S AND MIL-STD-9
SECURITY CLASSIFICATION
UNLESS OTHERWISE SPECIFIED THE SURF. FIN OF MACHINED PARTS SHALL NOT EXCEED A MAX READING OF 125/PER MIL-STD-10
DIMENSIONS AND TOLERANCES PER MIL-STD 8
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING
TOLERANCES ON:
BASIC DIMENSIONS | 2 PLACE DECIMALS | 3 PLACE DECIMALS
UP TO 6 | ± .02 | ± .005
ABOVE 6 TO 24 | ± .03 | ± .010
ABOVE 24 | ± .06 | ± .015
ANGULAR DIMENSIONS ± 1/2°
MATERIAL:
NEXT ASSY | USED ON
FIRST APPLICATION
RCA COMMODITY CODE
CONTRACT NO NAS9-14477
SHOP ORDER NO FF7000
DRAWN BY M. KRAVITZ 4/18/75
DESIGN ACTIVITY APPD. M. Kravitz 4/18/75
RADIO CORPORATION OF AMERICA
NEW YORK, N.Y.
ASTRO-ELECTRONICS DIVISION, PRINCETON, N.J., PLANT
SOLID STATE TV CAMERA
SCHEMATIC A5 ~ ALC
SIZE C | CODE IDENT NO. 49671 | SK 2282869
SCALE | WEIGHT | SHEET 1 OF 1
D 739-2 3/68

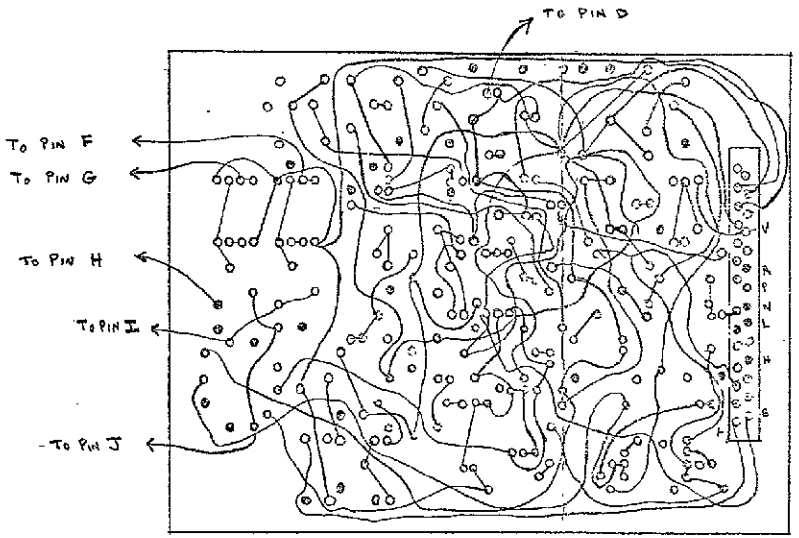
FOLDOUT FRAME 1

ORIGINAL PAGE IS OF POOR QUALITY

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	MOVE R6 & R7; ADD R56 & R57, R58 & C19, CR10, CR11, Q14, R53 & R54.	10/22/75	







FOLDOUT FRAME 2

NOTES:
1. ALL TRANSISTORS & INTEGRATED CIRCUITS SHOWN TOP VIEW
2. • DENOTES CONNECTION TO GROUND PLANE

QTY REQD PER DASH NO.	CODE IDENT	IDENTIFYING NO.	DESCRIPTION	SPECIFICATION	SEE NOTE NO.

MATERIALS AND SPECIFICATIONS

B-11

REVISION STATUS WHERE MORE THAN ONE SHEET			
SH	REV	SH	REV

THD DATA TO BE INTERPRETED USING NBS HDBK H28 AND MIL-STD-9

INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5-66

RCA COMMODITY CODE:

UNLESS OTHERWISE SPECIFIED THE SURFACE FINISH OF MACHINED PARTS SHALL NOT EXCEED A MAXIMUM READING 125 PER ANSI STD B46.1 — 1962

NEXT ASSY	USED ON
FIRST APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES ON:		
BASIC DIMENSIONS	2 PLACE DECIMALS	3 PLACE DECIMALS
UP TO 6	± .02	± .010
ABOVE 6 to 24	± 03	± .015
ABOVE 24	± 05	± .020

ANGULAR DIMENSIONS ± ½°

MATERIAL: SEE TABLE

CONTRACT NO. NAS9-14477 REL

DRAWN BY F.G.HUBIT DATE 7-8-75

CHECKED BY DATE

DESIGN ACTIVITY APPD DATE Emil P. Hubit 7-3-75

RCA RCA CORPORATION | NEW YORK, NY

ASTRO-ELECTRONICS DIVISION, PRINCETON, N.J. PLANT

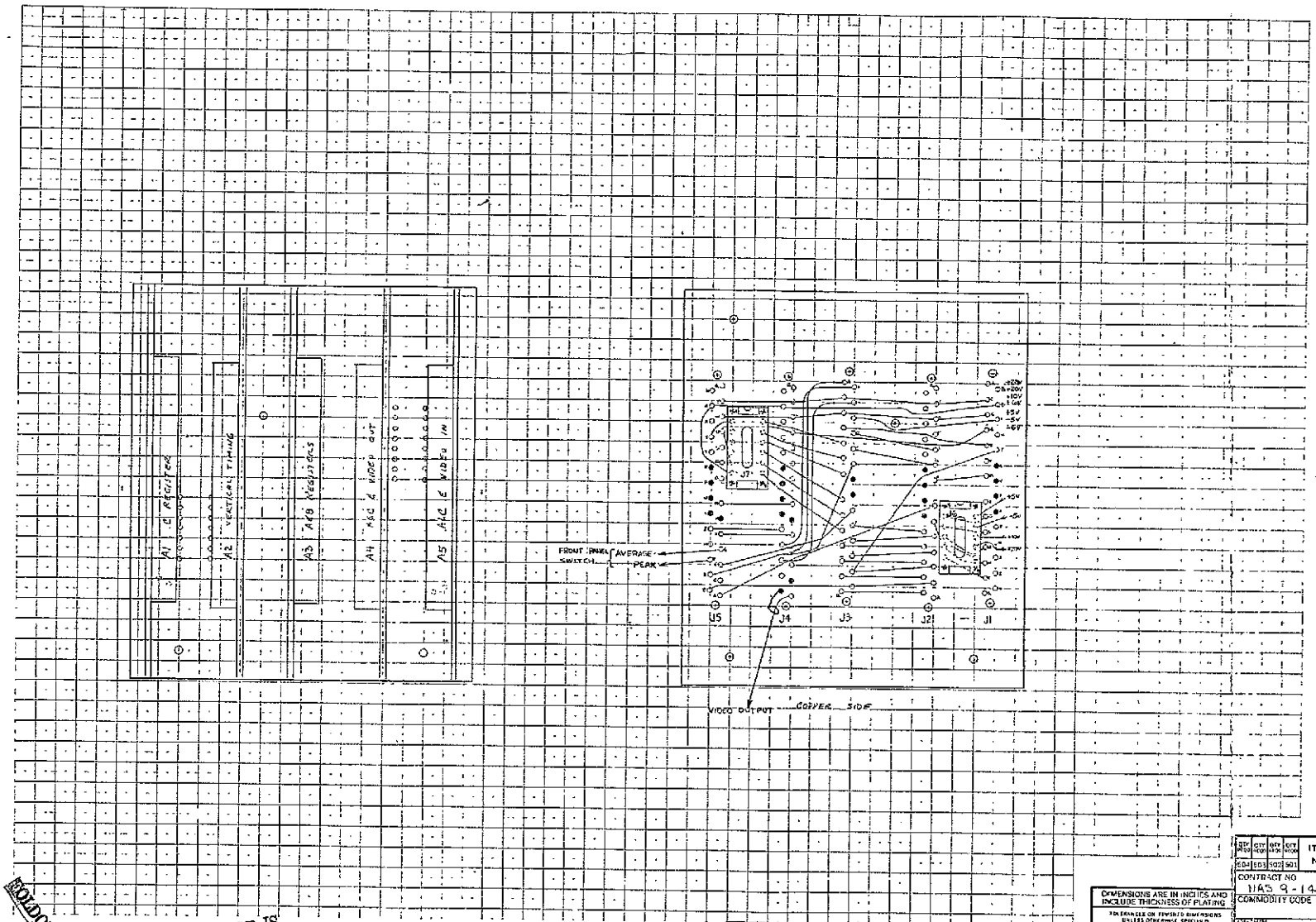
SOLID STATE TV CAMERA

A5 ~ ALC & VIDEO INPUT ASSY

SIZE	CODE IDENT NO.	
B	49671	SK2273624

SCALE WEIGHT SHEET 1 OF

RCA 2417-3 (4-71) 7069



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FOLDOUT FRAME 1

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REVISIONS

SYM	ZONE	DESCRIPTION	DATE	APPROVED

SEP MODEL	QTY MODEL	QTY MODEL	QTY MODEL	ITEM NO	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
504	503	502	501				

LIST OF MATERIALS

CONTRACT NO: NAS 9-14477

COMMODITY CODE:

DRAWN: S. HETHERINGTON 6-26-75

CHECKED:

DESIGN ACTIVITY APPD: DATE

RADIO CORPORATION OF AMERICA
CAMDEN, N J
PLANT

SOLID STATE TV CAMERA
A6 - HARNESS BOARD

CODE IDENT NO: 49671 | SIZE: D | SK 228240

SCALE: 2:1 | WEIGHT: | SHEET 1 OF 1

DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING
TOLERANCES ON FINISHED DIMENSIONS UNLESS OTHERWISE SPECIFIED

BASIC DIMENSIONS	2 PLACE DECIMALS	3 PLACE DECIMALS
UP TO 6	± .02	± .005
OVER 6 TO 24	± .03	± .010
ABOVE 24	± .06	± .015

ANGULAR DIMENSIONS ± ½°

SEE RCA PUBLICATION SPEC FOR STOCK SIZES

ALL EXTERNAL THREADS TO BE CLASS 2A BEFORE PLATING AND CLASS 2 AFTER PLATING
ALL INTERNAL THREADS TO BE CLASS 2B UNLESS OTHERWISE SPECIFIED

FIRST MADE FOR	USED ON
NEXT ASSY	

FORM 1514 C 4-61 PRINTED IN U.S.A. SPEIDEL & CO

DASH NO.	SPECIFICATION TABLE		
	MATERIAL	FINISH	SPECIFICATION

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE / APPROVED

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FOLDOUT FRAME 2

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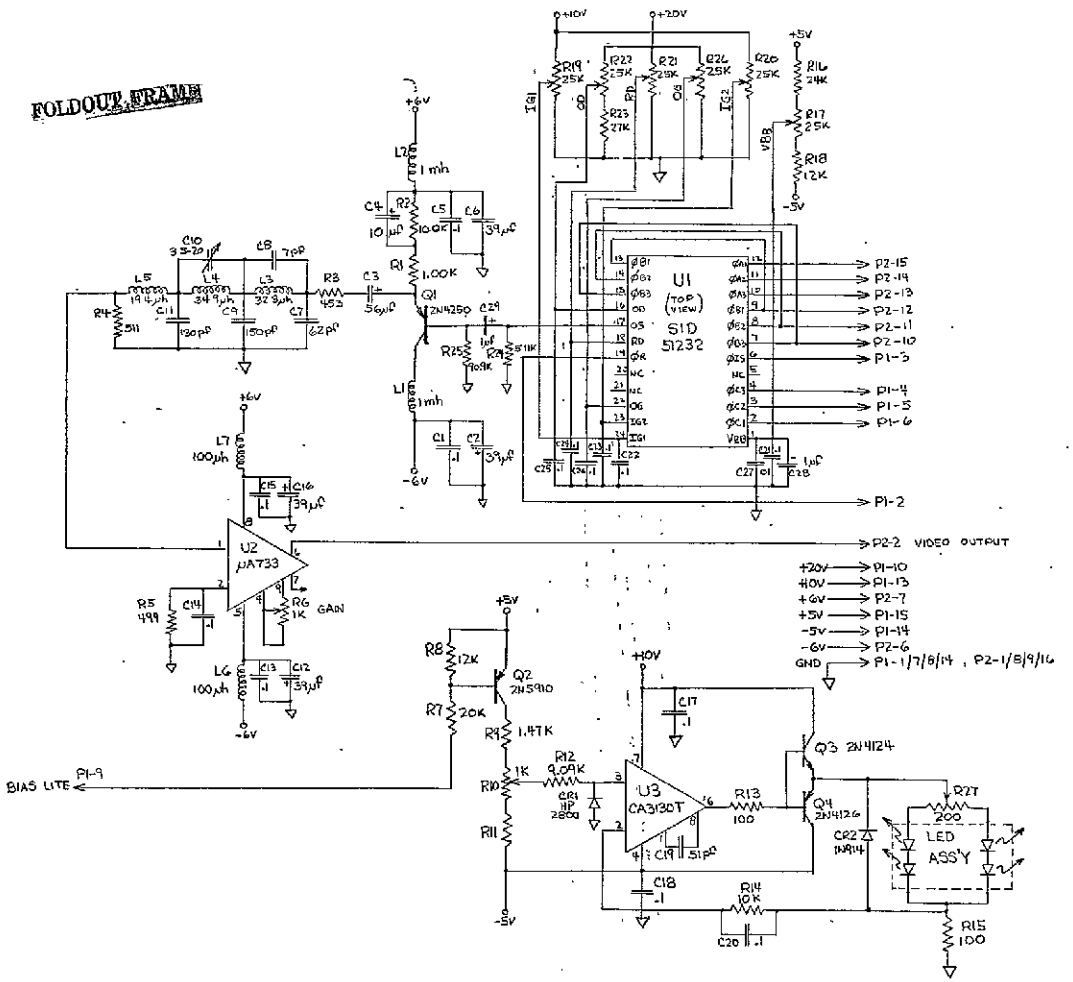
OF POOR QUALITY

FOR REVISIONS ONLY

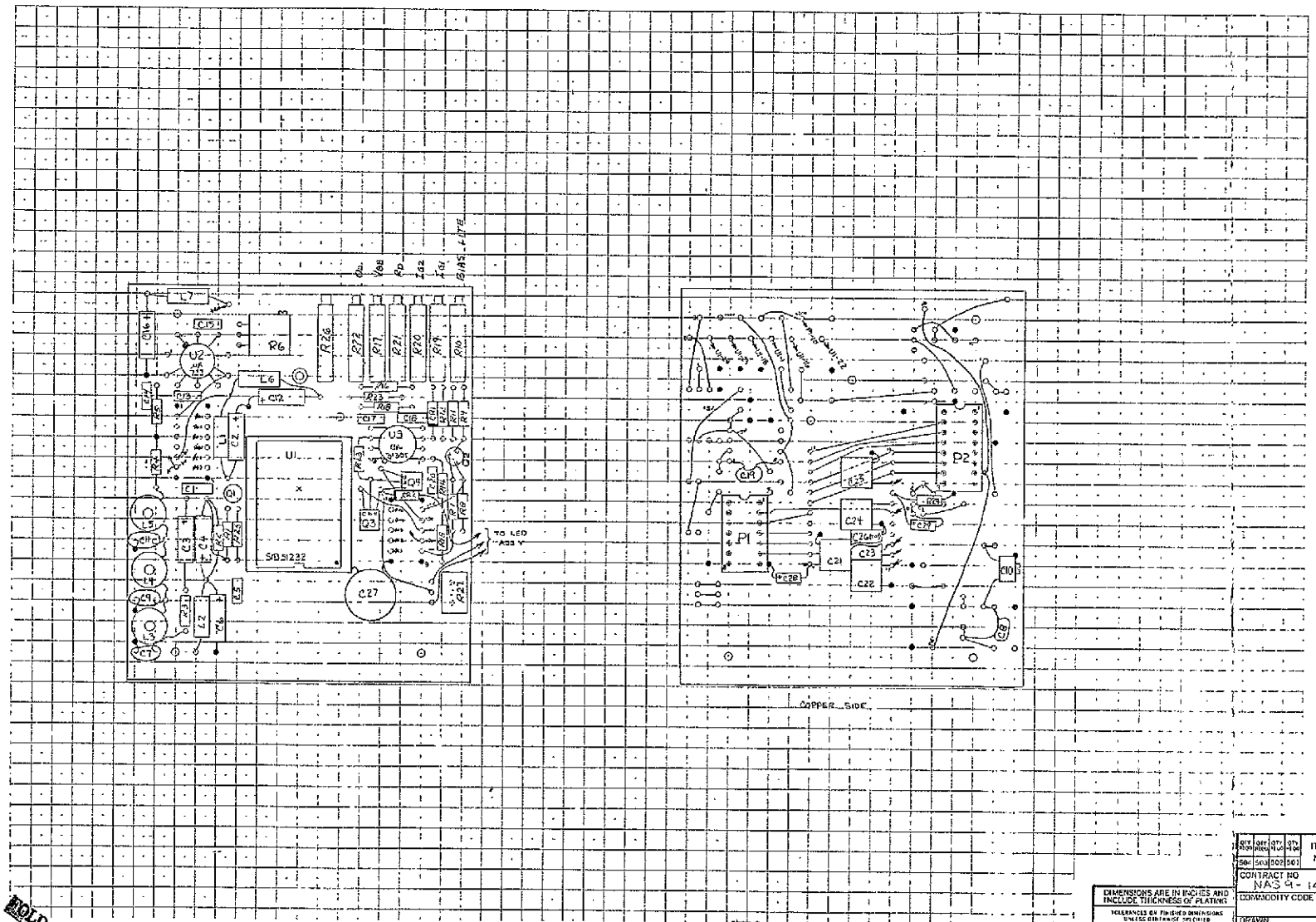


SKETCH

THD DATA TO BE INTERPRETED USING HNDBK H28 AND MIL-STD 9	SECURITY CLASSIFICATION	UNLESS OTHERWISE SPECIFIED THE SURF. FIN. OF MACHINED PARTS SHALL NOT EXCEED A MAX READING OF 125 PER MIL-STD-10	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING	CONTRACT NO NAS 9-14477	RADIO CORPORATION OF AMERICA NEW YORK, N.Y. ASTRO-ELECTRONICS DIVISION, PRINCETON, N.J., PLANT	
		DIMENSIONS AND TOLERANCES PER MIL-STD C	TOLERANCES ON: BASIC DIMENSIONS / 2 PLACE DECIMALS / 3 PLACE DECIMALS: UP TO 6 ± .02 ± .005; ABOVE 6 TO 24 ± .03 ± .010; ABOVE 24 ± .06 ± .015	SHOP ORDER NO.	SOLID STATE TV CAMERA SCHEMATIC A7 ~ CCD ASS'Y B-13	
			ANGULAR DIMENSIONS ± 1/2°	DRAWN BY R HETHERINGTON DATE 11-7-75	SIZE C	CODE IDENT NO. 49671 SK 2282870
RCA COMMODITY CODE		NEXT ASSY / USED ON FIRST APPLICATION	MATERIAL	DESIGN ACTIVITY APPD. M. Kravetz 11/8/75 DATE	SCALE	WEIGHT SHEET 1 OF 1

AED 739-2 3/66

REVISIONS			
SYM	ZONE	DESCRIPTION	DATE	APPROVED
A		ADDED R24-R27, C26-C28, C08	11-3-75	RH



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FOLDOUT FRAME 2

DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING		
TOLERANCES ON FINISHED DIMENSIONS UNLESS OTHERWISE SPECIFIED		
BASIC DIMENSIONS	2 PLACE DECIMALS	3 PLACE DECIMALS
UP TO 6	± .02	± .005
OVER 6 TO 24	± .03	± .010
ABOVE 24	± .05	± .015
ANGULAR DIMENSIONS ± 1°		
SEE MIL-STD-8 SPEC FOR SHOP TOL		

FIRST MADE FOR	
NEXT ASS'Y	USED ON

ALL EXTERNAL THREADS TO BE CLASS 2A BEFORE PLATING, CLASS 3 AFTER PLATING
ALL INTERNAL THREADS TO BE CLASS 2B UNLESS OTHERWISE SPECIFIED

QTY PER PRINTED WIRING	QTY PER ASSY	QTY PER UNIT	QTY PER SET	ITEM NO	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
							LIST OF MATERIALS

CONTRACT NO	NAS 9-14477	RADIO CORPORATION OF AMERICA CAMDEN, N J	
COMMODITY CODE		PLANT	
DRAWN	R HETHERINGTON 8-25-75	SOLID STATE TV CAMERA	
CHECKED	DATE	A7~ CCD ASS'Y	B-14
DESIGN ACTIVITY APPD	DATE	CODE IDENT NO	SIZE
		49671	D
		SCALE 2:1	WEIGHT
		SK 2288241	SHEET 1 OF 1

DASH NO.	SPECIFICATION TABLE		
	MATERIAL	FINISH	SPECIFICATION

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED

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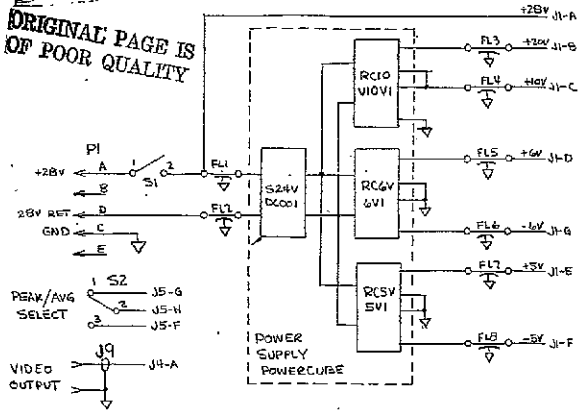
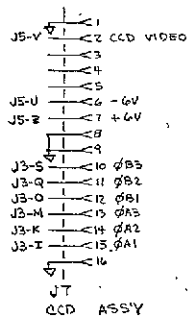
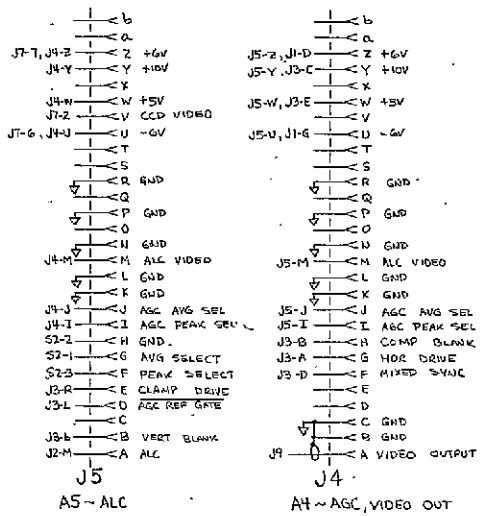






FOLDOUT FRAME 2

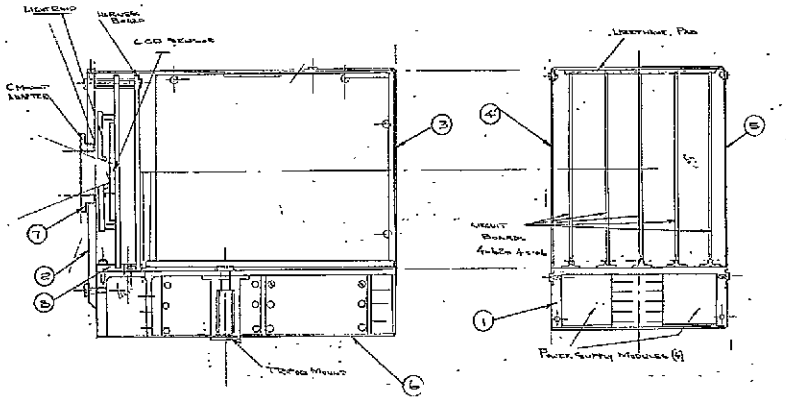
SKETCH

THD DATA TO BE INTERPRETED USING HNDBK H28 AND MIL-STD-9	SECURITY CLASSIFICATION	UNLESS OTHERWISE SPECIFIED THE SURF. FIN. OF MACHINED PARTS SHALL NOT EXCEED A MAX READING OF 125/PER MIL-STD-10	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING	CONTRACT NO. NAS 9-14477	RADIO CORPORATION OF AMERICA NEW YORK, N.Y. ASTRO-ELECTRONICS DIVISION, PRINCETON, N.J., PLANT	
		DIMENSIONS AND TOLERANCES PER MIL-STD-8	TOLERANCES ON: BASIC DIMENSIONS / 2 PLACE DECIMALS / 3 PLACE DECIMALS: UP TO 6 ± .02 ± .005; ABOVE 6 TO 24 ± .03 ± .010; ABOVE 24 ± .06 ± .015	SHOP ORDER NO.	SOLID STATE TV CAMERA	
			ANGULAR DIMENSIONS ± 1/2°	DRAWN BY R HETHERINGTON DATE 11-8-75	INTERCONNECTION DIAGRAM B-15	
RCA COMMODITY CODE		NEXT ASSY / USED ON / FIRST APPLICATION	MATERIAL:	DESIGN ACTIVITY APPD. M. Kravetz DATE 11/7/75	SIZE C / CODE IDENT NO. 49671 / SK2282871	
					SCALE / WEIGHT / SHEET 1 OF 1	

AED 739-2 3/66

DASH NO	SPECIFICATION TABLE		
	MATERIAL	FINISH	SPECIFICATION

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED



FOLDOUT FRAME 2

B-16

SKETCH

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OF POOR QUALITY

FOLDOUT FRAME 1

C-2

THIS DATA TO BE INTERPRETED USING ANSI Y14.5 AND MIL STD 9	SECURITY CLASSIFICATION	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DIMENSIONS AND TOLERANCES PER MIL STD 8	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE AS FOLLOWS:	CONTRACT NO SHOP ORDER NO DRAWN BY DESIGN ACTIVITY APPR

BASIC DIMENSIONS	2 PLACE DECIMALS	3 PLACE DECIMALS
UP TO 6	±.03	±.005
OVER 6 TO 24	±.10	±.010
ABOVE 24	±.15	±.015

ANGULAR TOLERANCE ±1/2°

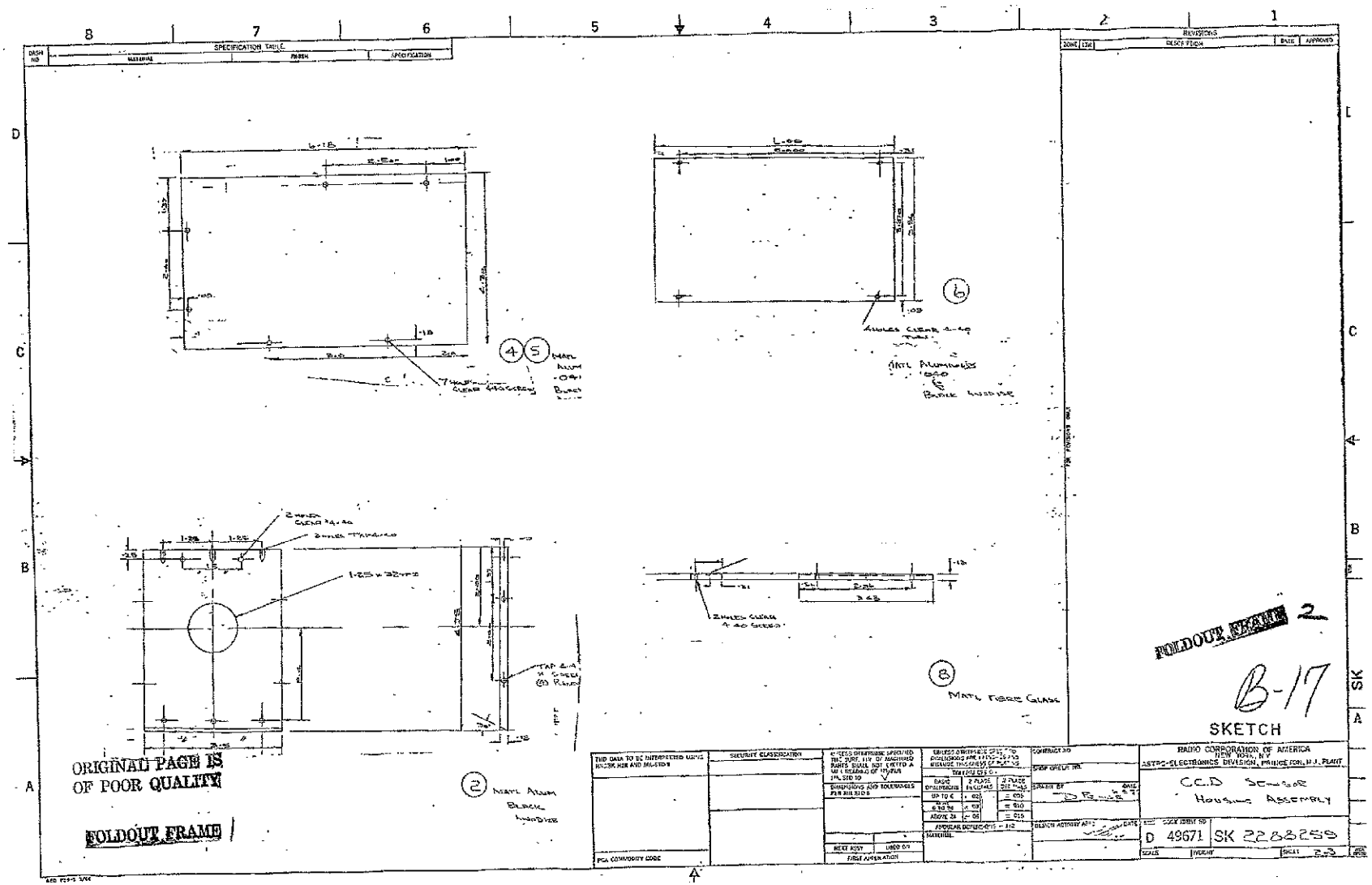
HEAT ADDY	USED ON
FIRST APPLICATION	

RADIO CORPORATION OF AMERICA
NEW YORK, N.Y.
ASTRO-ELECTRONICS DIVISION, PRINCETON, N.J., PLANT

CCD Sensor Housing Assembly

SIZE	CECIL ITEM NO	SK 2288259
D	49671	

SCALE | WEIGHT | SHEET 1 OF 1


SPECIFICATION TABLE
DASH NO
MATERIAL
FINISH
SPECIFICATION
REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
4 5
MATL ALUM
.040
BLACK
7 HOLES CLEAR
6
ANGLES CLEAR
MATL ALUMINUM
.040
BLACK
2 HOLES CLEAR
#40 SCREW
2 HOLES CLEAR #40
2 HOLES "TAPPED"
1.25 x 32 HOLE
TAP 4-40
THRU
2 HOLES CLEAR
#40 SCREW
8
MATL FIBER GLASS
2
MATL ALUM
BLACK
ANODIZE
FOLDOUT FRAME 2
B-17
SKETCH
THIS DATA TO BE INTERPRETED USING
ANSI Y14.5M AND MIL-STD-9
SECURITY CLASSIFICATION
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS
TWO PLACE DECIMALS
THREE PLACE DECIMALS
ANGULAR
MATERIAL
FINISH
DRAWN BY
DATE
DESIGN ACTIVITY APP'D
RADIO CORPORATION OF AMERICA
NEW YORK, N.Y.
ASTRO-ELECTRONICS DIVISION, PRINCE ST., N.J. PLANT
C.C.D Sensor
Housing Assembly
CODE IDENT NO
D 49671
SK 2288259
SCALE
WEIGHT
SHEET 2/3
NEXT ASSY
USED ON
FSCM COMMODITY CODE
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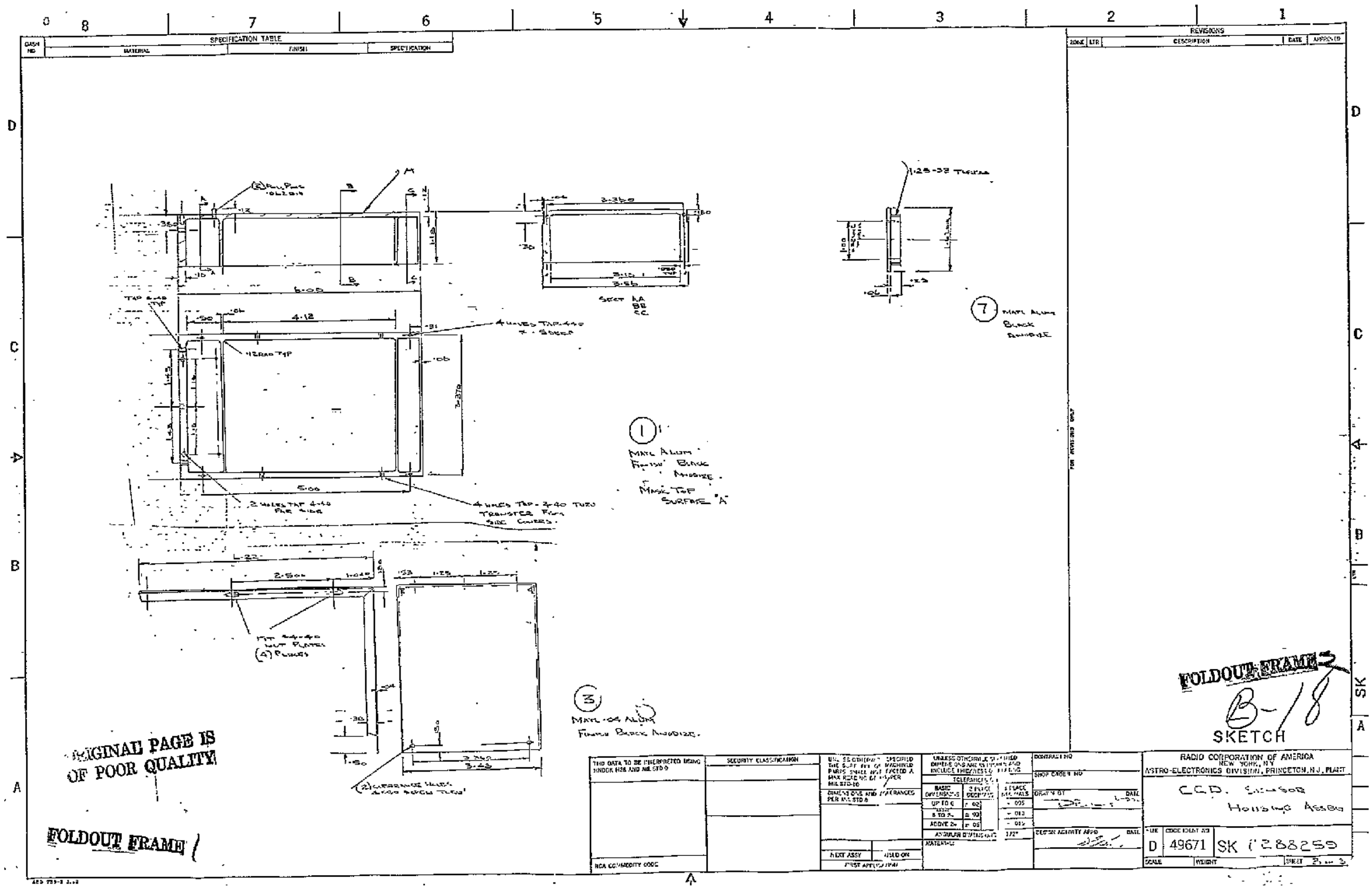
OF POOR QUALITY
FOLDOUT FRAME 1


SPECIFICATION TABLE
DASH NO
MATERIAL
FINISH
SPECIFICATION
REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
6.00
4.12
5.00
4 HOLES TAP 4-40
2 HOLES TAP 4-40 PER SIDE
4 HOLES TAP 2-40 THRU TRANSFER FROM SIDE COVERS
3.360
3.56
SECT AA BB CC
1
MATL ALUM
FINISH BLACK ANODIZE
MASK TOP SURFACE "A"
7
MATL ALUM BLACK ANODIZE
3
MATL .04 ALUM
FINISH BLACK ANODIZE
2.50
3.42
ORIGINAL PAGE IS OF POOR QUALITY
FOLDOUT FRAME
FOLDOUT FRAME
B-18
SKETCH
RADIO CORPORATION OF AMERICA
NEW YORK, N.Y.
ASTRO-ELECTRONICS DIVISION, PRINCETON, N.J. PLANT
C.C.D. Sensor Housing Assby
D
49671
SK (288259
SCALE
WEIGHT
SHEET 2 of 3