NASA CR-144898

ELECTRONIC DELAY IGNITION MODULE

FOR

SINGLE BRIDGEWIRE APOLLO STANDARD INITIATOR

By

R. D. WARD

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VOUGHT CORPORATION, SYSTEMS DIVISION
Dallas, Texas

for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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FOREWORD

This report presents the concept, design and testing to qualify an Electronic Delay Ignition Module for use as a Scout Fourth Stage motor ignition system. Included in this report are the criteria for component selection, design, and test results.

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1.0 SUMMARY

The Scout Fourth Stage Electronic Delay Ignition Module (EDIM) design and qualification program was authorized under NASA Contract NAS1-12500, Task R-59. An Engineering model and a Qualification model of the EDIM were constructed and tested to Scout flight qualification criteria at Vought Systems Division of LTV-Dallas, Texas. The qualification model incorporated design improvements resulting from the Engineering model tests. Ignition design concept was based on SBASI ignition energy requirements as shown in Reference 3 (NASA Contractor Report NAS CR-2461), Reference 1, and Reference 2 (NASA Technical Report 32-1556 and 32-1230). Compatibility with Single Bridgewire Apollo Standard Initiator (SBASI) was proven by test firing forty-five (45) SBASI's at NASA Langley Research Center (LRC) with worst case voltage and temperature conditions.

The EDIM was successfully qualified for Scout flight application with no failures during testing of the qualification unit. Included herein is a method of implementing the EDIM into Scout vehicle hardware and the Ground Support Equipment (GSE) necessary to check out the system.

2.0 INTRODUCTION

The design, development and testing of the EDIM was performed to provide an ignition system which can replace the existing Scout 4th stage pyrotechnic delay ignition system. Requirements of the EDIM ignition system are to provide ignition power to a SBASI, utilize existing power sources and accomplish the ignition function using a capacitive discharge technique.

Steps leading to the flight qualified unit were design, breadboard test, reliability evaluation, engineering evaluation test, production documentation, qualification test and SBASI compatibility tests. This report summarizes the results with detailed test data contained in the appendix to this report.

Appendixes D and E were prepared by members of the Vought Corporation, Systems Division Engineering Staff, J. D. Clark (Reliability Evaluation), W. L. Billow (Qualification Report), and C. L. Dyer (Electromatic Susceptibility Test Report).

3.0 DESIGN AND BREADBOARD EVALUATION

3.1 Design Criteria

Design of the EDIM is based on the following criteria developed during review of Scout requirements and trade-offs to optimize the design:

(a) Delay and ignition power will be obtained from existing Scout 3rd stage ignition battery. The energy necessary to power the delay circuit and SBASI ignition will be stored in capacitors.

(b) Power to charge the "Storage" capacitors will be initiated with the Scout Guidance Intervalometer command. Start of the ignition time delay will be a normally open switch which closes on 3rd to 4th stage separation.

(c) Environmental requirements included temperature, vibration, thermal shock, mechanical shock, humidity, high temperature altitude, acceleration and EMI (MIL-STD-461).

(d) SBASI firing energy requirements, firing switch selection and storage capacitor selection is based on results of Capacitive Discharge Ignition (CDI) study documented under Contract NAS1-10000, R-70 (Reference 3). During this referenced study, SBASI minimum firing energy requirement delivered from capacitive discharge was determined to be 34 millijoules. A SCR firing switch per specification shown in Appendix A was determined during CDI testing to be an adequate switch for ignition of a SBASI. Survey of the available capacitors for energy storage during the CDI study indicated that a hermetically sealed tantalum wet slug capacitor was the best choice based on size and reliability.

3.2 Design Analysis

Preliminary calculations on the energy requirement for the electronic delay showed that it is not feasible to use the same storage capacitor to provide power for the delay circuit and for SBASI firing. Based on 24 volts being the minimum allowable SBASI ignition voltage (from CDI study) and a steady state current drain of 4 ma, a storage capacitor of 5500 μf would be required for a 5.5 second delay. This capacitance was determined using capacitor energy equation as follows.

$$Q = CE$$

where

Q = charge on capacitor
C = capacitance
E = voltage on capacitor

Assume

(1) 4 ma constant current drain to power delay circuit
(2) E_1 = 28 volt initial capacitor charge voltage
(3) E_2 = 24 volt minimum allowable charge voltage on capacitor at 5.5 sec.
(4) Total time circuit requires power = 5.5 sec.

Therefore,

$$Q_{required} = (4 \times 10^{-3})\ (5.5) = 22 \text{ mc}$$

$$Q_{required} = (E_1C) - (E_2C)$$

$$C = \frac{Q}{E_1 - E_2} = \frac{22 \times 10^{-3}}{4} = 5500\ \mu f$$

This value of capacitance will require too much packaging space. For use in this design, from a capacitance size standpoint it is more efficient to allow decay of the delay circuit storage capacitors to a lower voltage than can be tolerated on the ignition storage. Therefore, two storage banks of capacitors isolated from each other and the power source by diodes are used in this design.

The electronic delay ignition system physical size is determined for the most part by the amount of storage capacitance required. Scout requirements were reviewed to determine minimum delay required for 4th stage firing. Results of this review are presented in Figure 1.

Curve A represents the normal separation rate between 3rd and 4th stages of Scout with proper 3rd stage retro motor operation ("retro"). Curve B represents the 3rd to 4th stage nominal separation rate without "retro", the dashed lines corresponding to curve B represent the predicted maximum and minimum limits of separation rate without "retro". The horizontal dashed line at 50 inches separation represents the minimum separation distance needed for proper Scout control operation. The intersection of the lower limit with the 50 inch separation line at three seconds is the minimum recommended time for ignition of the 4th stage motor. Based on this information, a delay of 4.0 seconds ± 0.5 second was chosen for the design limits for the electronic delay ignition.

In order to achieve the ± 0.5 second accuracy over the environmental limits some type of voltage stabilization of the capacitor delay voltage is required. Likewise the capacitance variation with temperature (−60% @ − 55°C and +25% @ 85°C) ruled out the possibility of utilizing RC time delay directly as a delay time generator. Generation of the 4.0 second time delay with active electronic components directed some type of voltage regulation. The linear integrated circuit precision voltage regulator per Appendix B will perform this function so that voltage variations do not affect the generated delay time. A linear integrated circuit voltage regulator was chosen for this design because of its small size (10 lead metal can), low standby current, minimum external components required and voltage regulation.

Figure 2 illustrates how the power consumed in the delay circuit affects required storage capacitance. The plot of Figure 2 was obtained by evaluating

$$C = \frac{Q}{E_1 - E_2}$$ where;

E_1 = 28 volts initial capacitor charge voltage

E_2 = 11 volts minimum capacitor charge voltage that the regulator will maintain 9 volt output

Q = current x delay time

Delay time = 5.5 second (4.0 second ignition delay plus 1.5 second spin motor to separation delay)

Figure 3 illustrates the effect of increased delay time on required storage capacitance. Figure 3 was obtained in the same manner as the previous figure except current was held constant while varying delay time. For the breadboard evaluation test, a storage capacitance of 1320 MFD (1410 MFD actual measured value) was chosen.

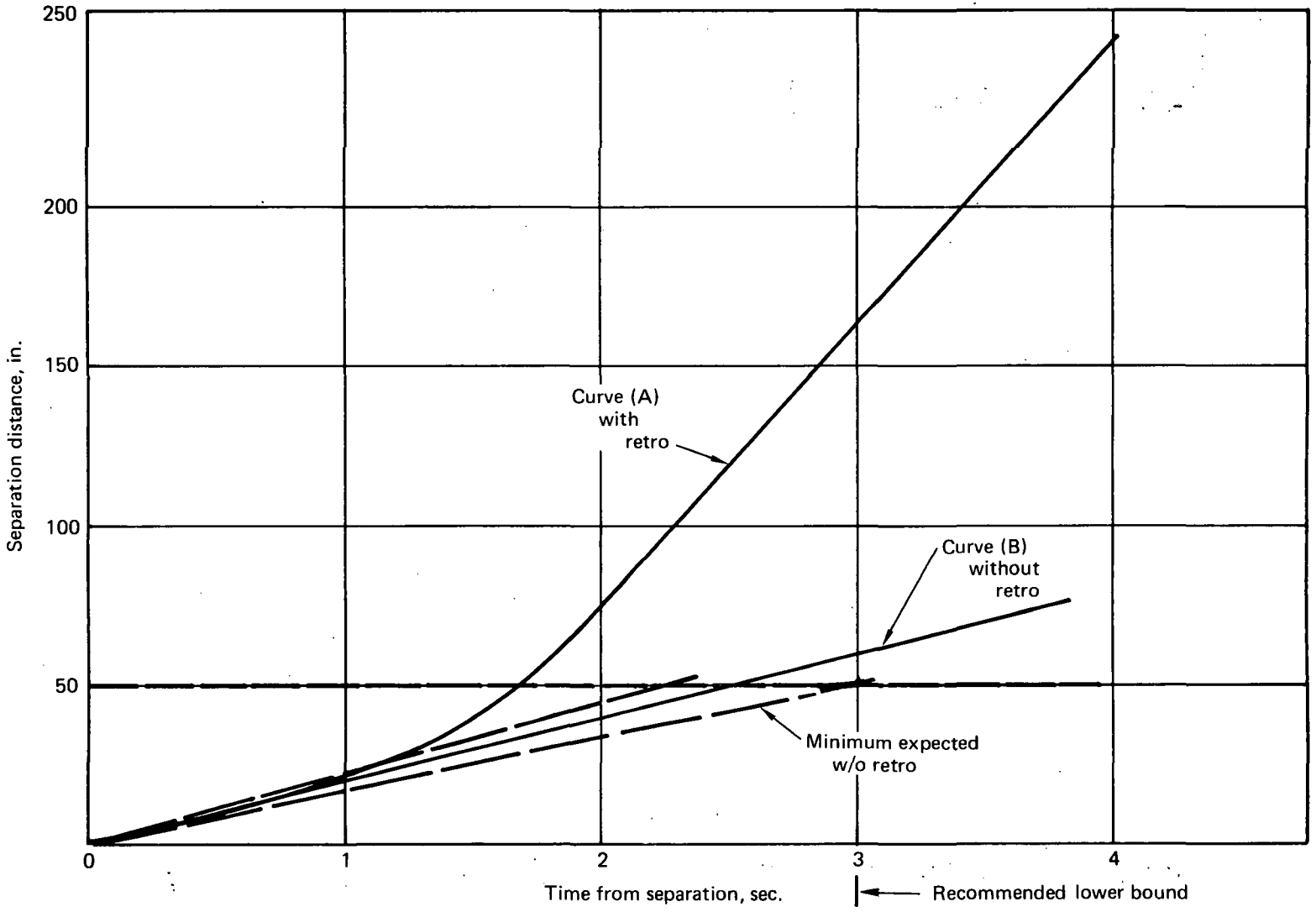


FIGURE 1. – DISTANCE BETWEEN 3RD & 4TH STAGES FOR SEPARATION MAXIMUM PAYLOAD WEIGHT

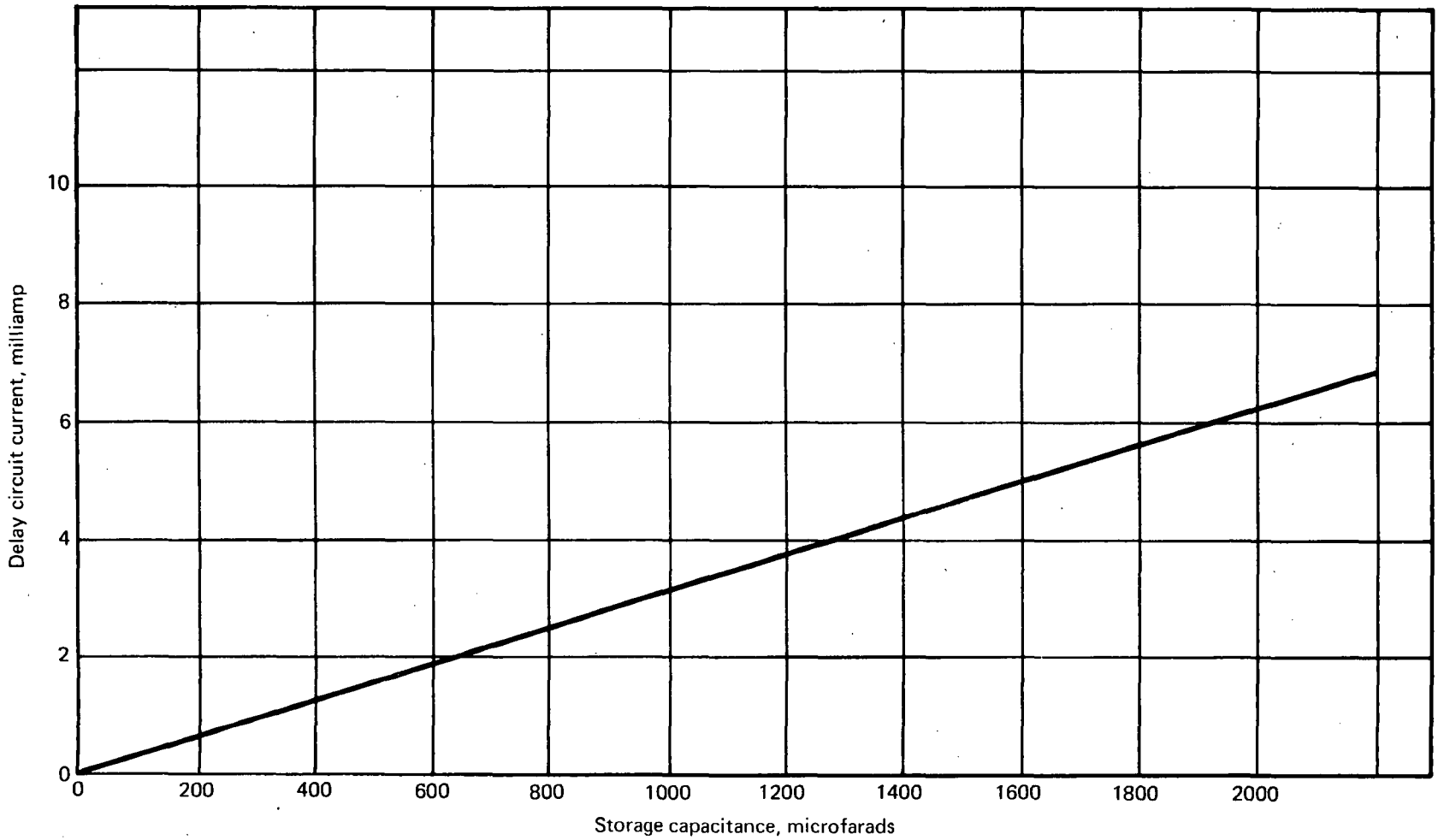


FIGURE 2. – AVERAGE REGULATOR CURRENT DRAIN VS. STORAGE CAPACITANCE @ 5.5 SEC. DELAY

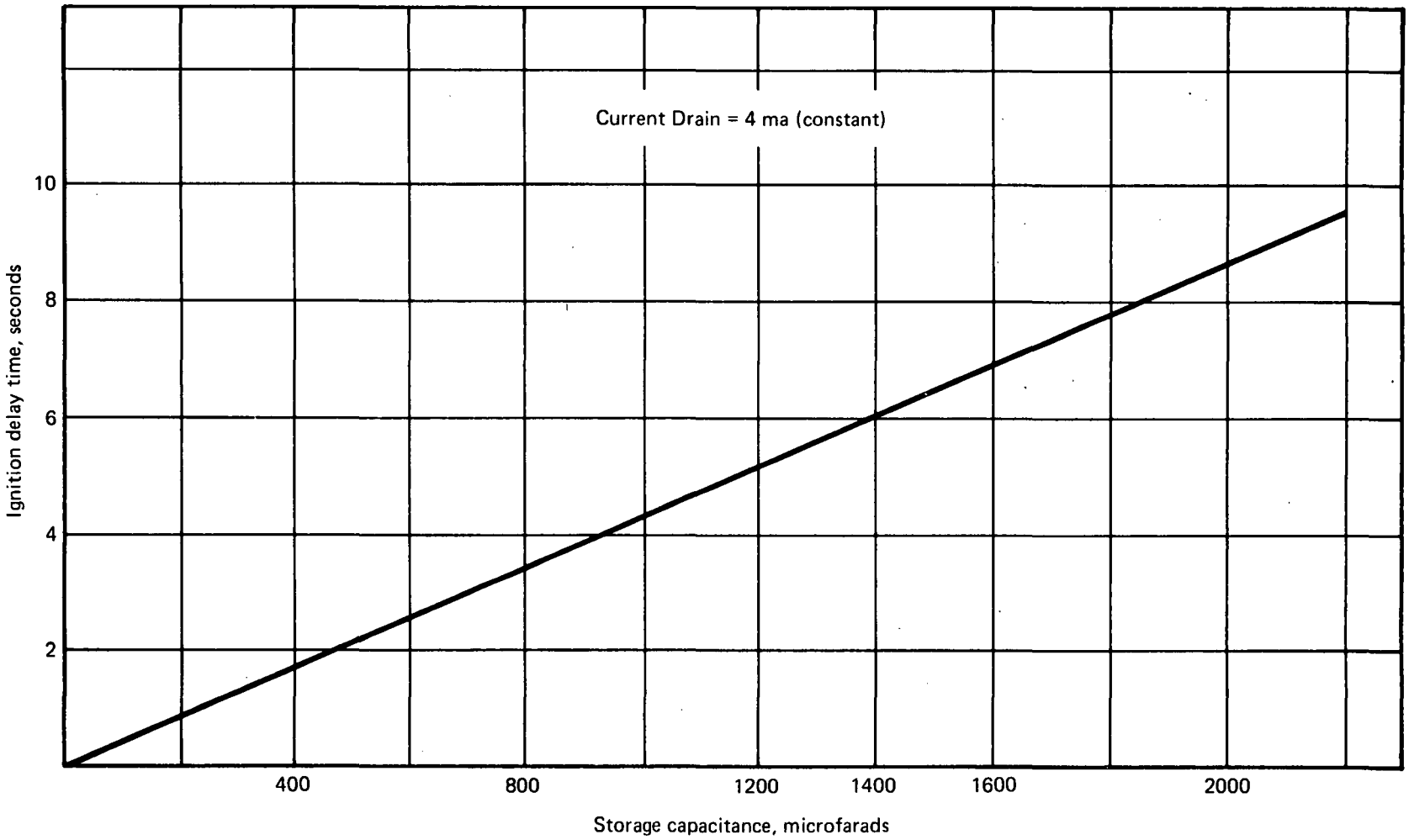
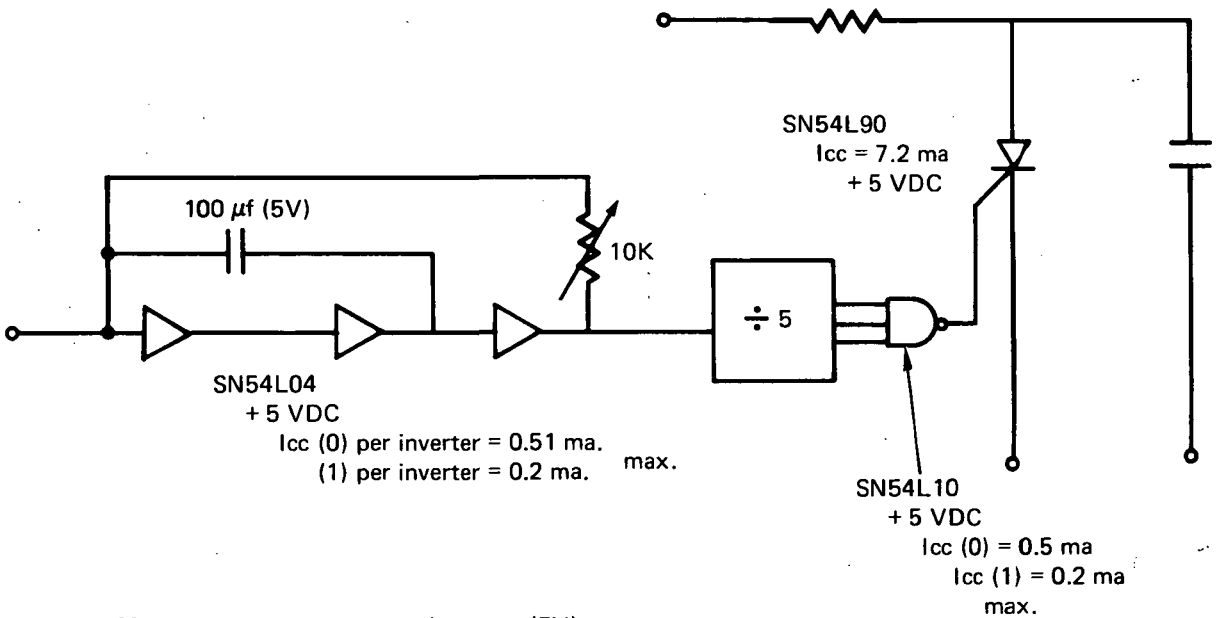


FIGURE 3. – DELAY TIME VS. STORAGE CAPACITANCE @ 4 MA.

3.3 Breadboard Circuits

Several methods of generating the 4.0 second ignition delay such as pre-package timer, TTL Oscillator/Divider, COS/MOS, and unijunction transistor were evaluated. Under consideration were pre-packaged programmable units which are available off-the-shelf, but were rejected on the basis of power consumption. Also considered were circuits built from available components such as the circuits shown in Figures 4, 5, and 6. The prime consideration in evaluating these circuits was the power required for operation. Circuits as shown in Figures 5 (COS/MOS) and 6 (Unijunction Transistor) were selected for breadboard tests. These two circuits were selected on the basis of pre-directed power consumption requirements. The COS/MOS circuit as breadboarded is shown in Figure 7 and the unijunction circuit as breadboard in Figure 8.



Max. worst case current requirements (5V)
divider = 7.2 ma
3 input gate = 0.5 ma
3 ea inverter = 1.53
total 9.23 ma.

FIGURE 4. – TTL OSCILLATOR/DIVIDER

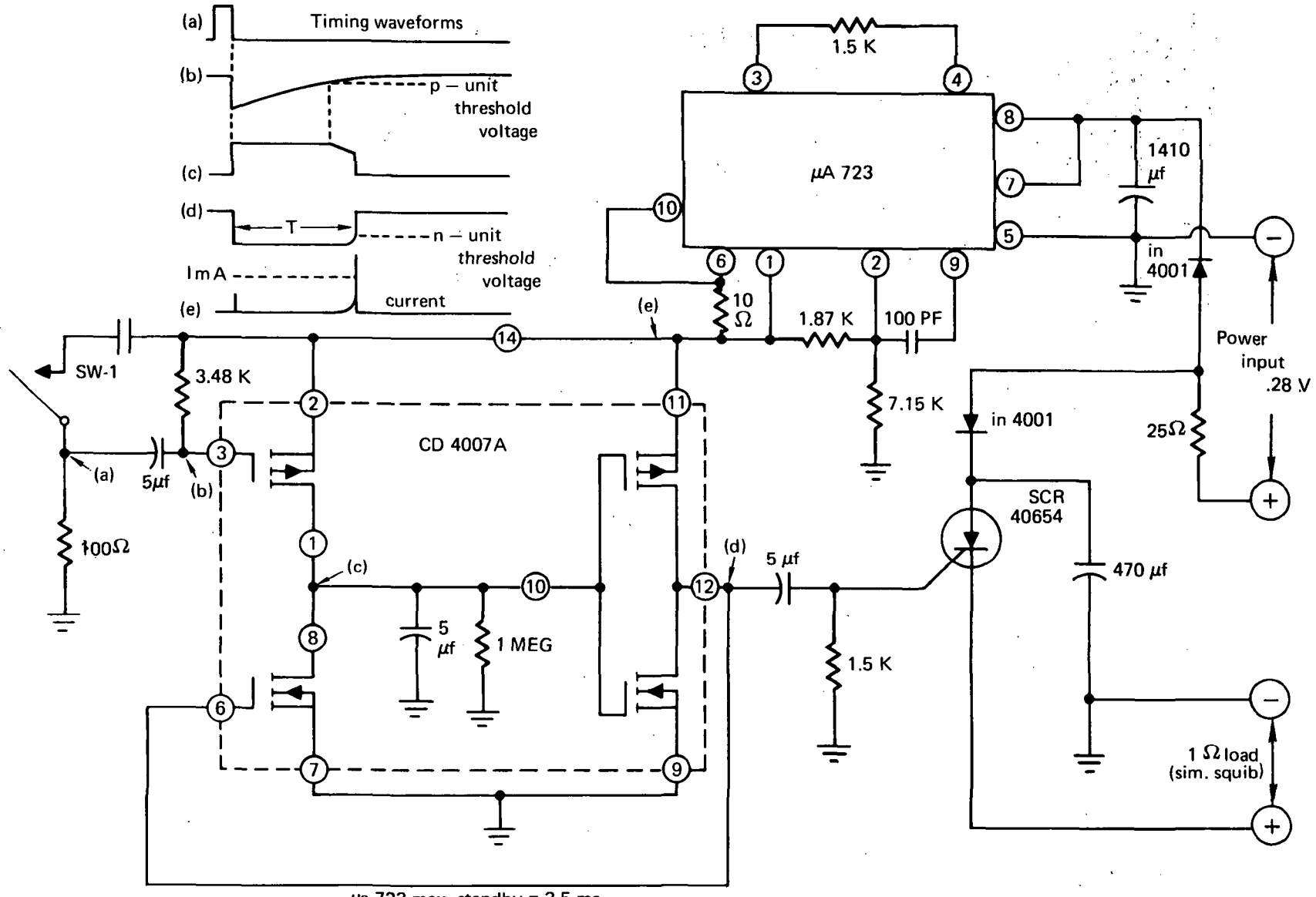


FIGURE 5. – COS/MOS MONOSTABLE

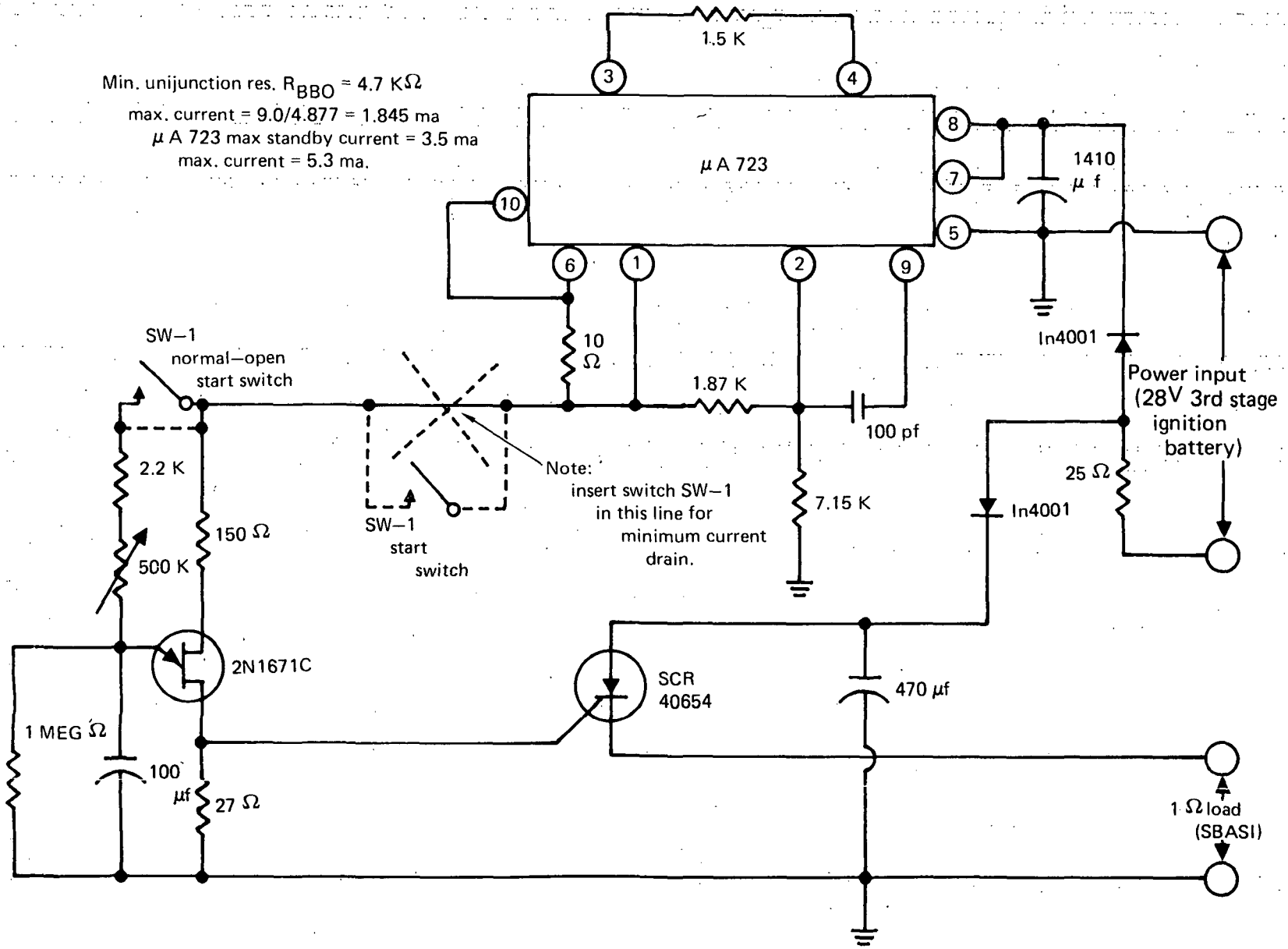


FIGURE 6. – UNIJUNCTION TRANSISTOR DELAY CIRCUIT

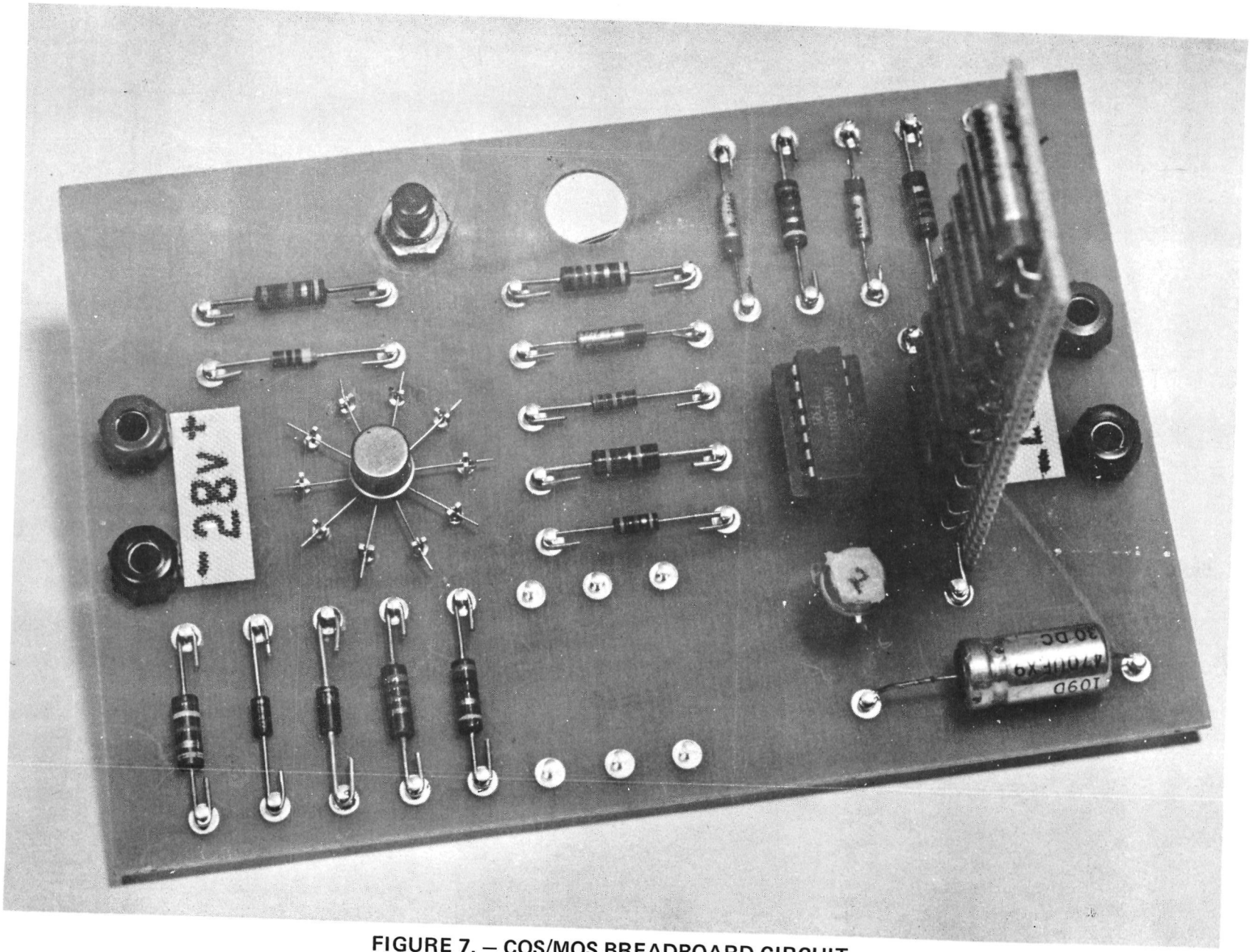


FIGURE 7. – COS/MOS BREADBOARD CIRCUIT

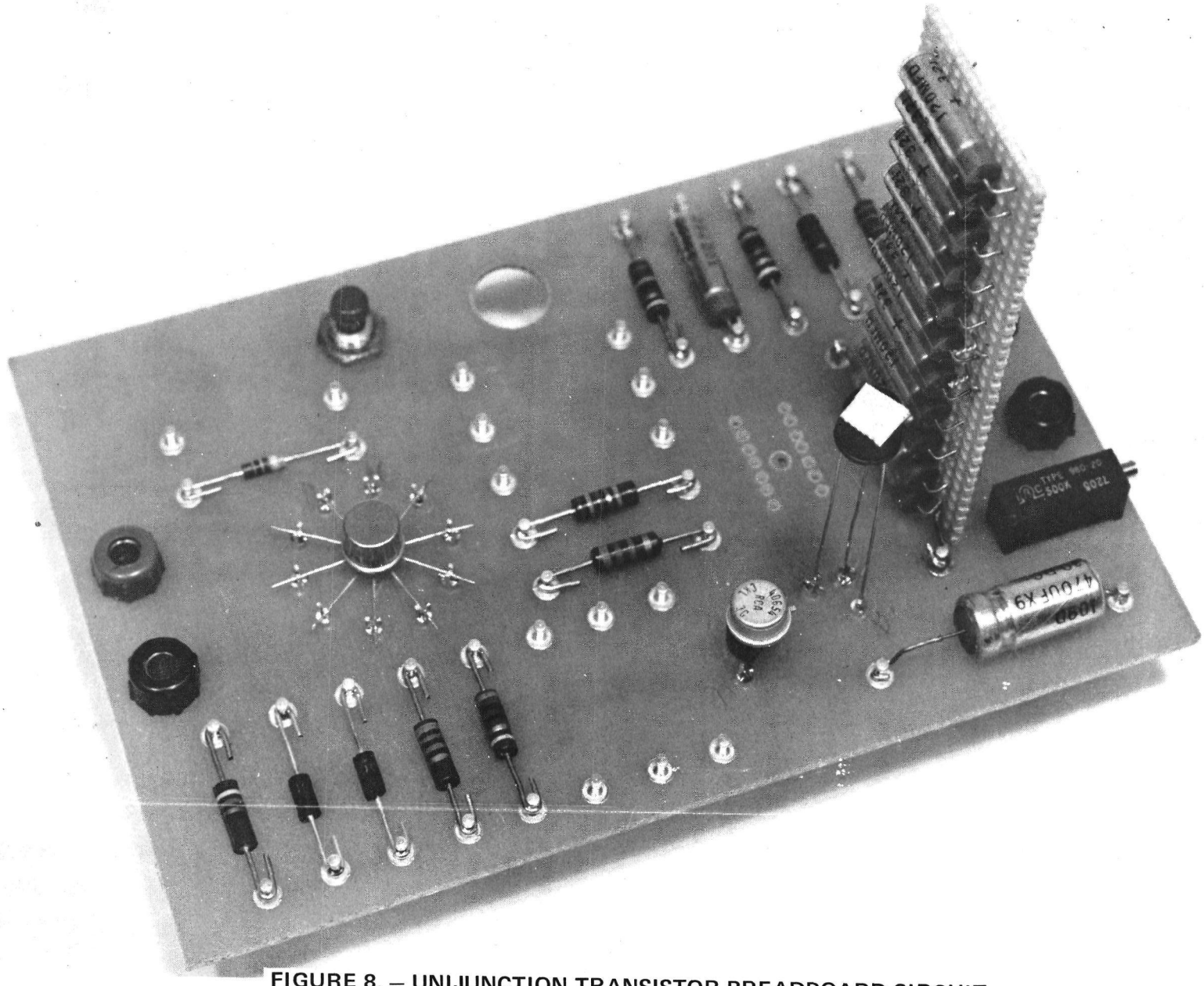


FIGURE 8. – UNIJUNCTION TRANSISTOR BREADBOARD CIRCUIT

3.4 Breadboard Test

Objective of the tests on the COS/MOS and unijunction delay circuits was to verify operation, timing accuracy and current necessary for operation. Both circuits were subjected to operation at increased temperature using a heat lamp as a heat source. In all tests, delay time was measured with a stop watch.

3.4.1 – Voltage Regulator – with the voltage regulator connected as shown in Figures 5 and 6, the standby current was measured to be 2.0 ma. The output voltage regulation with input line variation from 30 to 11 volts was measured. No change in regulated output could be measured until the input reached 10 volts, then the output decreased at the same rate as the input. The voltage regulator circuit regulated at 8.73 volts output with the circuit components values as shown.

3.4.2 – COS/MOS – the power required for operation of the circuit as shown in Figure 5 was measured with the following results: (NOTE: These measurements do not include voltage regulator standby current.)

(a) Steady state current after closure of the start switch = 0.8 ma.

(b) At "Time-Out" current pulsed to $\approx$ 1.3 ma (see Figure 5). Table I shows the time from removal of the power source until the output of voltage regulator is affected. Table II shows the delay stability of this circuit at ambient temperature ($\approx 23.9^{o}C$), while undergoing application of heat (temperature of board increased to $\approx 82^{o}C$) and while cooling down. This data indicated that the COS/MOS would be adequate from a timing accuracy standpoint.

TABLE I. – COS/MOS TIME DELAY BREADBOARD

Time to voltage regulator output voltage drop

Without start pulse	With start pulse
14 seconds	9.3 seconds
13.5	9.0
13.5	8.9
14.0	9.1
13.7	9.2
13.6	9.1
13.6	9.3

Time measured with stop watch.

TABLE II. – COS/MOS TIME DELAY BREADBOARD

Time stability with application of heat

Time Delay		
@ Ambient temperature	*Heated ≈ 82°C	Cooling down
6.7 seconds	7.0 seconds	7.1 seconds
6.74	7.0	7.1
6.8	7.5	7.0
7.0	7.35	7.0
6.9	7.3	7.1
7.0	7.35	7.1
7.0	7.3	7.0
6.9	7.2	6.9
6.9	7.35	7.0
7.0	7.3	6.82

*Temperature measured with thermometer near surface of board.
Time measured with stop watch.

A problem was encountered with this circuit due to marginal capability to furnish gate drive current to the SCR. Ten SCR's were tested with the COS/MOS circuit, three of these SCR's could not be gated on. Test of the SCR's proved that all were operational and within specification limits for gate drive requirements. Re-evaluation of the COS/MOS circuit indicated insufficient output drive capability to reliably trigger the selected SCR. In order to use this circuit, an additional drive circuit must be added. Since the additional circuit would have to be AC coupled and biased "OFF", current drain in excess of 1 ma would be required. Therefore, this circuit would be unacceptable from a power consumption standpoint.

3.4.3 – Unijunction Circuit – capability to temperature compensate the time delay circuit plus the ability to drive the SCR gate directly makes the unijunction transistor a good device to use for generating the ignition delay. The unijunction breadboard (Figure 6) was evaluated in the same manner as the COS/MOS circuit. Power measurement results were as follows:

Steady stage current (Including voltage regulator standby current) =
3.3 ma (before start switch closure)
= 3.35 ma (after start switch closure)
Voltage Regulator output voltage = 8.73 volts.

Time from removal of power to start of voltage drop (w/o start) at the voltage regulator output was as follows:

7.4 sec
7.2 sec
7.3 sec
7.2 sec
7.3 sec
7.15 sec

In order to evaluate circuit operation at a lower Base-1, Base-2 unijunction current the 150 ohm Base-2 resistor was changed to 1500 ohm with the following results:

Total Current w/o start pulse = 2.8 ma
Total Current with start pulse = 2.95 ma
Voltage Regulator output voltage = 8.73 volts

At ambient temperature the time repeatability of the minimum current circuit was:

4.3 sec
4.3 sec
4.3 sec
4.3 sec
4.3 sec
4.3 sec

The same ten SCR's tested with the COS/MOS circuit were tested with the minimum current configuration unijunction circuit and all were gated "ON" with a 1 ohm load simulating a bridgewire.

Another circuit configuration evaluated with the unijunction (with 150 ohm in Base-1) was to move the start switch so that upon closure, power is furnished to the unijunction circuit. (Reference the SW-1 changes indicated by dotted lines to Figure 6).

Power requirements for this configuration:

Total current w/o start pulse = 2.0 ma
Total current with start pulse = 3.3 ma
Voltage Regulator output voltage = 8.73

This configuration was desirable because the only power consumed between power disconnect and delay start (1.5 sec) is the voltage regulation standby current. However, the SCR will be gated "ON" if the start switch opens after the timing capacitor is charged to a level sufficient to gate the SCR ($\approx$ 1.5 volts). A failure of this type appears to be possible and could cause early ignition of the 4th stage motor. With the start switch in the timing circuit only (as shown in Figure 6) switch chatter or a switch momentarily open would only increase the delay time equal to the time the switch is open. Table III shows the time stability at ambient temperature and the repeatability with increasing and decreasing temperature. Two different unijunction transistors were checked at ambient temperature without adjusting the calibration resistor in order to evaluate variations in unijunction transistors (Table III).

Based on power consumption and circuit simplicity the unijunction circuit per Figure 6 was selected as the best choice for 4th stage delay ignition and was selected for Engineering test evaluation.

TABLE III. – UNIJUNCTION TIME DELAY CIRCUIT

Time Stability

Note: All time measurements are with stop watch

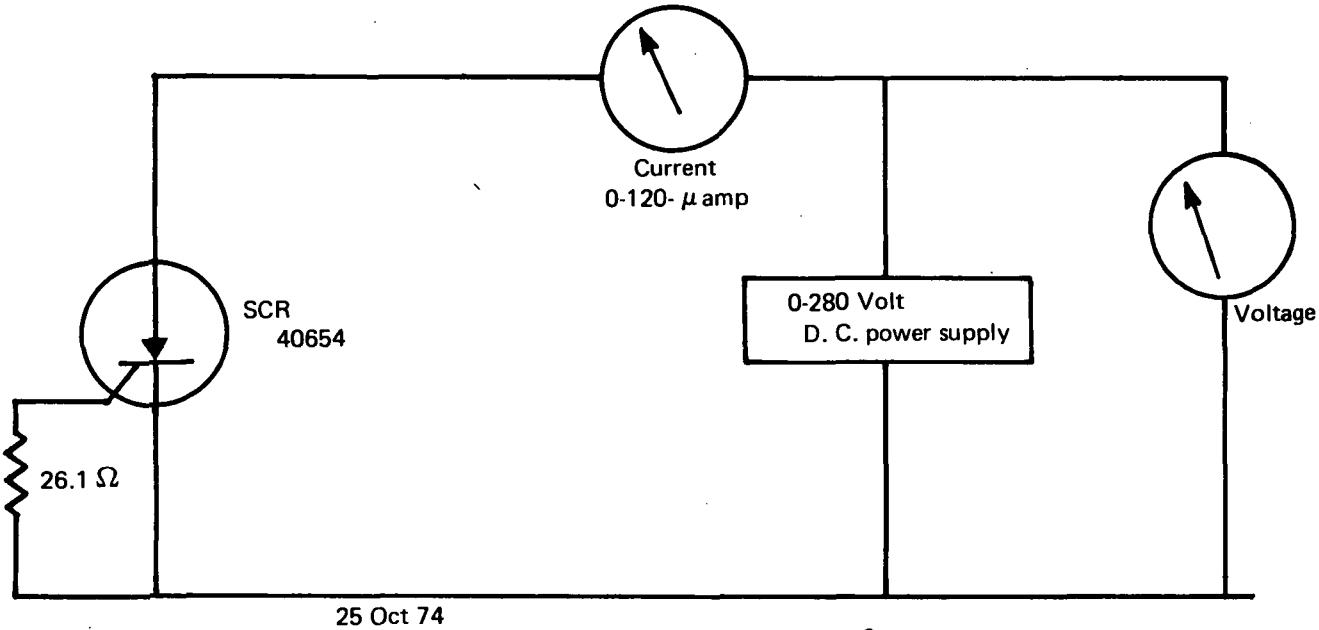
Ambient Temperature	With Heat Application (with heat lamp)	
5.0 seconds	5.5 second	increasing temperature
4.9	5.3	
5.1	5.3	
5.3	5.3	
5.0	5.3	
5.1	5.3	
5.2	5.3	
5.0	5.7	77°C*
5.4	5.7	77°C*
5.1	5.7	77°C*
5.2	5.5	Decreasing temperature
5.2	5.55	
	5.5	
	5.6	
	5.45	
	5.6	
	5.55	
	5.5	
	5.5	Ambient temperature

Unijunction No. 2 (without readjusting time delay resistor)

Ambient Temperature
5.5 seconds
5.4
5.3
5.25
5.3
5.3
5.3
5.35
5.2
5.3 seconds

*Temperature measured with thermometer near surface of board.

3.4.4 – SCR Test – the SCR specification for the maximum forward current in the "OFF" state at 200 volts is 0.5 ma. This leakage current at 30 volts could affect energy available to ignite a SBASI with 4 seconds delay. Therefore, in order to evaluate the forward leakage current as a function of voltage 19 SCR's were checked per Figure 9. The maximum forward current measured was eight microamps at 200 volts. At 30 volts the forward current was too small to be measured on any of the units checked. Results of this test indicate that forward leakage current of the SCR would not be a factor in the energy available to ignite a SBASI from the 600 μf capacitors at 5.5 sec storage time.



25 Oct 74
19 ea. SCR'S tested 200v = fwd voltage, $\approx 25^{o}C$,
15 ea. = fwd, off current less than 0.5 μ amp
4 ea. fwd, off current greater than 1.0 μ amp
1 = 4.5 μ a
1 = 5.0 μ a
1 = 3.0 μ a
1 = 8.0 μ a

FIGURE 9. – SCR FORWARD LEAKAGE TEST

4.0 ENGINEERING UNIT DESIGN

The circuit as shown in Figure 10 was packaged as an Engineering Test Unit and subjected to operational and environmental tests.

4.1 Operation in Scout Vehicle

EDIM circuit operation is as follows: (Ref. Figure 10)

a. Power will be supplied to the unit on command of the guidance timer through a relay contact; probable time of power application would be during 3rd stage coast. (J1 Pin 5)

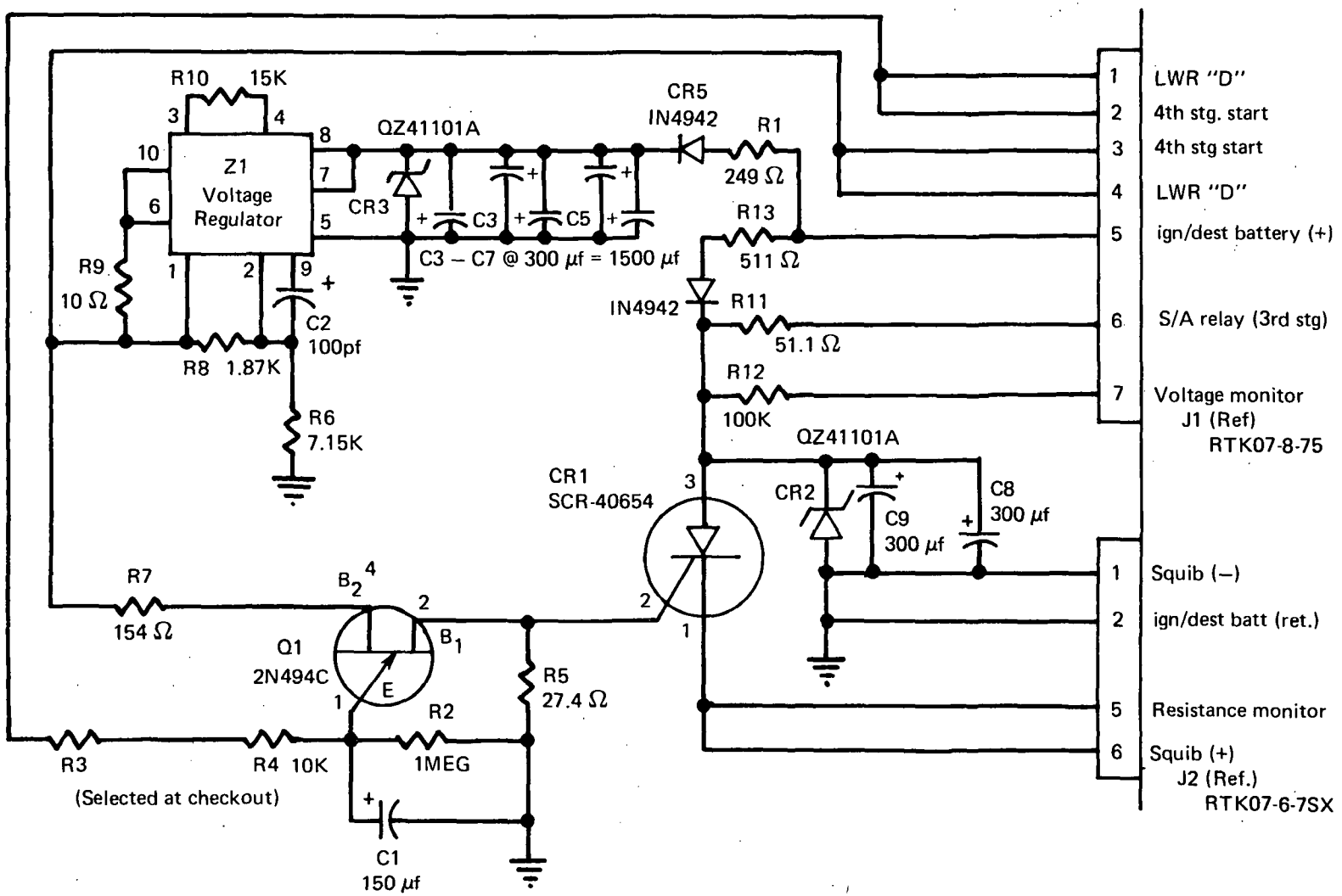


FIGURE 10. – CIRCUIT FOR ENGINEERING TEST

b. Capacitors C3 – C7 (delay module power) and capacitors C8 and C9 (ignition power) receive current from the 3rd stage ignition battery to a maximum voltage of 30 volts limited by CR2 and CR3. The latest time in mission profile which power can be applied to J1-5 is determined by the charge time of C3 – C7 [approx. 4 x rc; 4 (250 x 1500 x 10^{-6}) = 1.5 seconds].

c. Coincident with the voltage rise across C3 – C7 the output of the voltage regulator Z1 will rise to the regulation voltage of ≈ 9 volts.

d. Diodes CR4 and CR5 prevent discharge of the capacitors from one circuit to the other and discharge through a possible external short circuit after separation.

e. Resistors R1 and R13 limit the input current surge and in conjunction with zener diodes CR2 and CR3 provide a voltage drop to limit voltage across storage capacitors to 30 volts maximum.

f. Circuit Z1 is a precision voltage regulator so that a constant voltage can be maintained on the delay generator. Input of Z1 can vary from 30 volts to 12 volts with a constant 9 volts output. Regulation accuracy is 0.01% line and load (with 65 ma output).

g. Resistors R6 and R8 form the voltage divider which controls the voltage regulator output voltage.

h. C2 – provides a frequency compensation path to improve transient response of the regulator.

i. R10 – provides temperature compensation for the voltage regulator.
R9 – provides a current limit for a short circuit on the output.

j. Q1 is a unijunction transistor which is the switch for the timing network R3, R4 and C1. When C1 changes to the peak point voltage of Q1, at the peak point voltage C1 discharges emitter to Base-1 to provide gate current for CR1 the SCR firing switch.

k. On separation of the Scout 4th stage from 3rd stage, a switch closure between J1 pins 2 and 3 will charge capacitor C1 through R3 and R4 to slightly above the unijunction peak point voltage (≈ 4.5 volts) and then gate the SCR (CR1) "ON".

(Note: J1-1 and -4 are to provide capability for remote start checkout from blockhouse.)

The R3 and R4 resistance is selected so that the unijunction turn-on point is reached in four seconds, within the limits that can be selected in standard 1% resistors.

4.2 Interface Description

a. J1-1 to 4, remote start capability to check out ignition time delay and a test point to measure regulator output voltage

b. J1-2 to 3, separation switch start of ignition time delay

c. J1-5 to J2-2, input power from 3rd stage ignition battery or external power supply during checkout

d. J1-6 to J2-2, safe arm relay connect to provide discharge of firing capacitor

e. J1-7 to J2-2, firing voltage monitor

f. J2-1 to J2-6, squib (SBASI bridgewire)

g. J2-5 to J2-2, external measurement of squib resistance during checkout.

4.3 Engineering Unit Test

The circuit as shown in Figure 10 was constructed on a printed circuit board which is shown on Figure 11. The completed module which was subjected to environmental testing is shown in Figure 12.

4.3.1 – Test Conditions – test of the EDIM Engineering Unit consisted of the following:

(1) Component Evaluation
(2) Operational Test at Ambient Temperature
(3) Operational Test Through 10 Temperature Cycles + 71°C to −17.8°C
(4) Operational Test During 9 Random Vibration Cycles at 6.1G RMS (S^2 ET* Levels) in each of three orthogonal axes
(5) Operational Test During 1 Random Vibration Cycle at 9.2G RMS (Qualification Level) in each axis
(6) Operational Test During 9 S^2 ET* Level and Mechanical Shock Cycles at 50G's (Each axis)
(7) Operational Test During one Qualification Level Mechanical Shock Cycle at 75G's (Each axis)
(8) Operational Test During 1 Random Vibration Cycle at Qualification + 20% Level (11 RMS)
(9) Operational Test During 1 Mechanical Shock Test at Qualification + 20% (90G's)
(10) Post-Environmental Visual Inspection

4.3.2 – Test Results – test results from the EDIM Engineering Unit are summarized in Table IV. Review of the data presented in Table IV showed the EDIM design to be capable of meeting Scout Flight requirements. The voltage regulator (Z1 – Figure 10) selected for use in the Engineering Unit exhibited a higher standby current than was anticipated, although the 3.3 ma measured standby current is within specification limit for this voltage regulator. Use of this regulator would require test screening based on a maximum standby current of 2.0 ma in order to assure a safe timing margin for a production unit.

*Scout Standard Environmental Tests

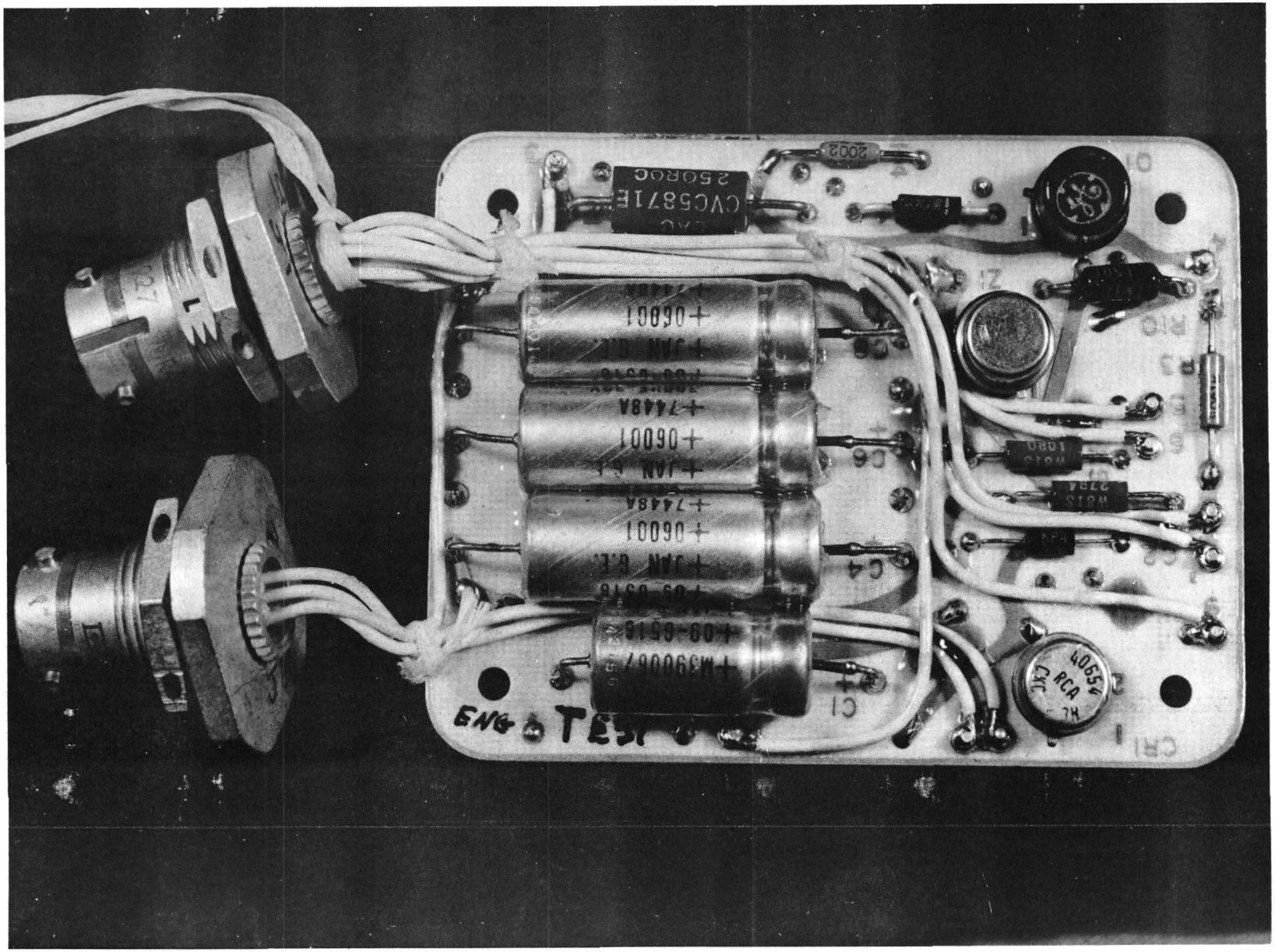


FIGURE 11. – PRINTED CIRCUIT-ENGINEERING TEST UNIT

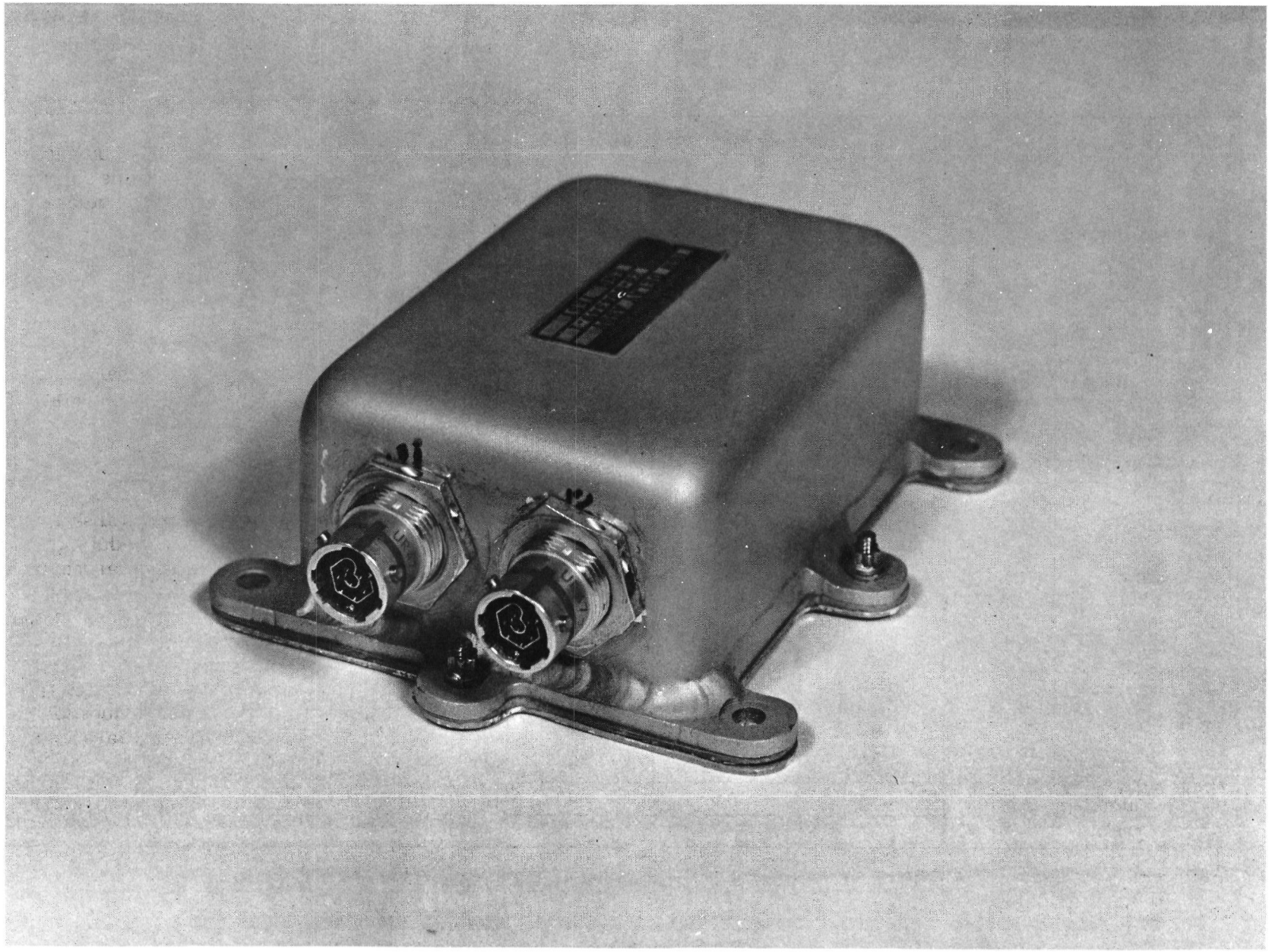


FIGURE 12. – EDIM – ENGINEERING TEST MODULE

TABLE IV. – TEST RESULTS EDIM ENGINEERING UNIT – Continued

	Measured data			Data points	Calculated nominal
	Low	AV	High		
Voltage regulator standby current at 29.2 volts input, amb temp.		3.3 MA		1	2.3 MA
UJT standby current 30V input, amb. temp.	1.05	1.1 MA	1.1	24	1.2 MA
Voltage regulator min input-output differential at amp temp.		1.55V		1	1.5V
Voltage regulator output voltage at amb temp, 30V input	8.791 V	8.830V	8.840V	34	9.0V
Voltage regulator output voltage at amb temp, 35V input	8.818V	8.823V	8.831V	34	8.982V
Voltage regulator output voltage at 71°C, 30V input	8.738	8.747V	8.756	2	9.060V
Voltage regulator output voltage at 71°C, 35V input	8.728	8.739V	8.749	3	9.042V
Voltage regulator output voltage at –17.8°C, 30V	8.895	8.896	8.897	2	9.05V
Voltage regulator output voltage at –17.8°C, 35V		8.88		1	9.032V
Power storage capacitor charge voltage at amb. temp 30V input		28.68V		1	29.79V
Power storage capacitor charge voltage at amb. temp 35V input		30.88V		1	30.51V
Ignition storage capacitor charge voltage at amb temp, 30V input	29.048V	29.2V	29.347V	34	29.79V
Ignition storage capacitor charge voltage at amb temp, 35V input	30.277V	30.3V	30.426V	35	30.51V

TABLE IV. – TEST RESULTS EDIM ENGINEERING UNIT – Concluded

	Measured data			Data points	Calculated nominal
	Low	AV	High		
Ignition storage capacitor charge voltage at 71°C, 30V input	29.669	29.7	29.73V	2	31.05V
Ignition storage capacitor charge voltage at 71°C, 35V input	31.22V	31.3V	31.369V	3	30.59V
Ignition storage capacitor charge voltage at −17.8°C, 30V input	28.35V	28.4V	28.388	2	28.63V
Ignition storage capacitor charge voltage at −17.8°C, 35V input		29.7		1	29.51V
Time to loss of voltage regulator regulation, amb temp, 30V input	6.3 sec	6.79 sec	7.2 sec	13	7.63 sec
Time to loss of voltage regulator regulation, 71°C, 30V input	7.15 sec	7.5 sec	7.7 sec	4	10.06 sec
Time to loss of voltage regulator regulation, −17.8°C, 30V input	5.4 sec	5.7 sec	6.0 sec	6	4.11 sec
Time to loss of voltage regulator regulation, amb temp, 35V input	7.0 sec	7.3 sec	7.7 sec	17	8.22 sec
Time to loss of voltage regulator regulation, 71°C, 35V input	8.85 sec	9.2 sec	9.5 sec	3	3.065 sec
Time to loss of voltage regulator regulation, −17.8°C, 35V input	6.2 sec	6.4 sec	6.9 sec	8	4.24 sec
Percent capacitance change from 25°C for the M39006/09-6518					
Tantalum wet slug capacitors at 71°C	+6.93%	+8.16%	+10.52%	13	+19.32%
at −17.8°C	−17.81%	−19.66%	−21.5%	13	−32.1%
Power storage capacitance at amb temp		1423.8 μf		1	1500 μf ± 10%
Weight of EDIM		245.64 grms (8.687 oz)			

Review of available voltage regulator components for use in EDIM application revealed a pin for pin replacement which would guarantee a standby current of less than 2.0 ma. The voltage regulator selected for use in the qualification EDIM unit is described in Appendix C. Use of this voltage regulator eliminates the need for R-10 since provision for temperature compensation is internal to the new voltage regulator.

After completion of the operational and environmental test the EDIM was disassembled and a thorough visual examination was conducted. The visual examination revealed no evidence of any failure or discrepancies that had occurred as a result of the Engineering evaluation tests.

5.0 RELIABILITY EVALUATION

During and subsequent to the test of the Engineering Unit, a reliability evaluation was performed. (Reference Appendix D) This evaluation revealed possibilities for problems to develop, especially during production of the EDIM. As a result of the evaluation, changes were made to the EDIM circuit and controls added to the component procurement specification to alleviate the marginal conditions. A marginal condition is discussed in Appendix D whereby the possibility exists that the SCR cannot be gated with worst case components and environmental conditions occurring simultaneously. To prevent this occurrence, a parameter control was placed on the procurement specification of the SCR gate circuit to limit the maximum gate current needed to 15 ma (specification limit is 20 ma.). Also as recommended in the Reliability evaluation, the unijunction transistor type was changed to increase the gate drive margin. Another conclusion of the Reliability evaluation was that a marginal condition could exist on the amount of stored energy (energy stored by C3 – C7) available for delay circuit operational worst case conditions. This potential problem was corrected by selection of another voltage regulator (Z1) which required less standby current. This problem was discussed in paragraph 4.3.2. A comprehensive quantitative analysis documented in the Reliability evaluation of energy required to ignite a SBASI showed the EDIM as designed would deliver more than two times the maximum energy required to fire a SBASI at worst case conditions.

In order to achieve the level of component reliability necessary to assure Scout flight success, component selection criteria was placed on EDIM hardware. The component selection criteria is summarized in Table V.

6.0 QUALIFICATION UNIT DESIGN

Utilizing information generated during test of the Engineering Unit and the Reliability Evaluation, the circuit per Figure 13 was constructed for Qualification testing. Figure 14 shows the completed Qualification EDIM which was subjected to Flight Qualification and SBASI compatibility testing.

TABLE V. – COMPONENT TEST/SCREENING

Part No./Name	VSD Receiving Inspection	Screened at Vendor	Comments
Z1-SE550 voltage regulator	Functional test	Military grade	Tested for operation @ -55°C to + 125°C
Q1-2N494C transistor	Functional test	Pre-cap. visual inspection	
CR1-40654 SCR	Functional test	Pre-cap. visual inspection	After acceptance test units will be screened to limit max. gate current to 15 ma.
CR4,5-IN4942 Diode	Functional test	JANTX screening	Unitrode diode
CR2, CR3-GZ41101A	Functional test	Selected to 1% voltage	Selected by operational test. General semiconductor industries
C3-C9-M39006/09-6518 Capacitor 300 μf	Functional test	MIL-C-39006/09 failure rate P	Lowest failure rate available for tantalum wet slug capacitors
C1-M39006/09-6476 Capacitor 120 μf	Functional test	MIL-C-39006/09 failure rate P	Lowest failure rate available for tantalum wet slug capacitors
C1-M39014/05-2819 Capacitor	Functional test	MIL-C-39014/05	Ceramic capacitor
R3, R4, R6, R8, R10, R11, R12 RNR55CXXXFS resistor	Functional test	MIL-R-55182 established rel.	Highest reliability resistor available.
R1, R3 RNC65HXXX	Functional test	MIL-R-55182 established rel.	Highest reliability resistor available
R2, RNC60H1004 FS resistor	Functional test	MIL-R-55182 established rel.	Highest reliability resistor available
R5, R9, R7 RWR81510R0 FR	Functional test	MIL-R-55182 established rel.	Highest reliability resistor available

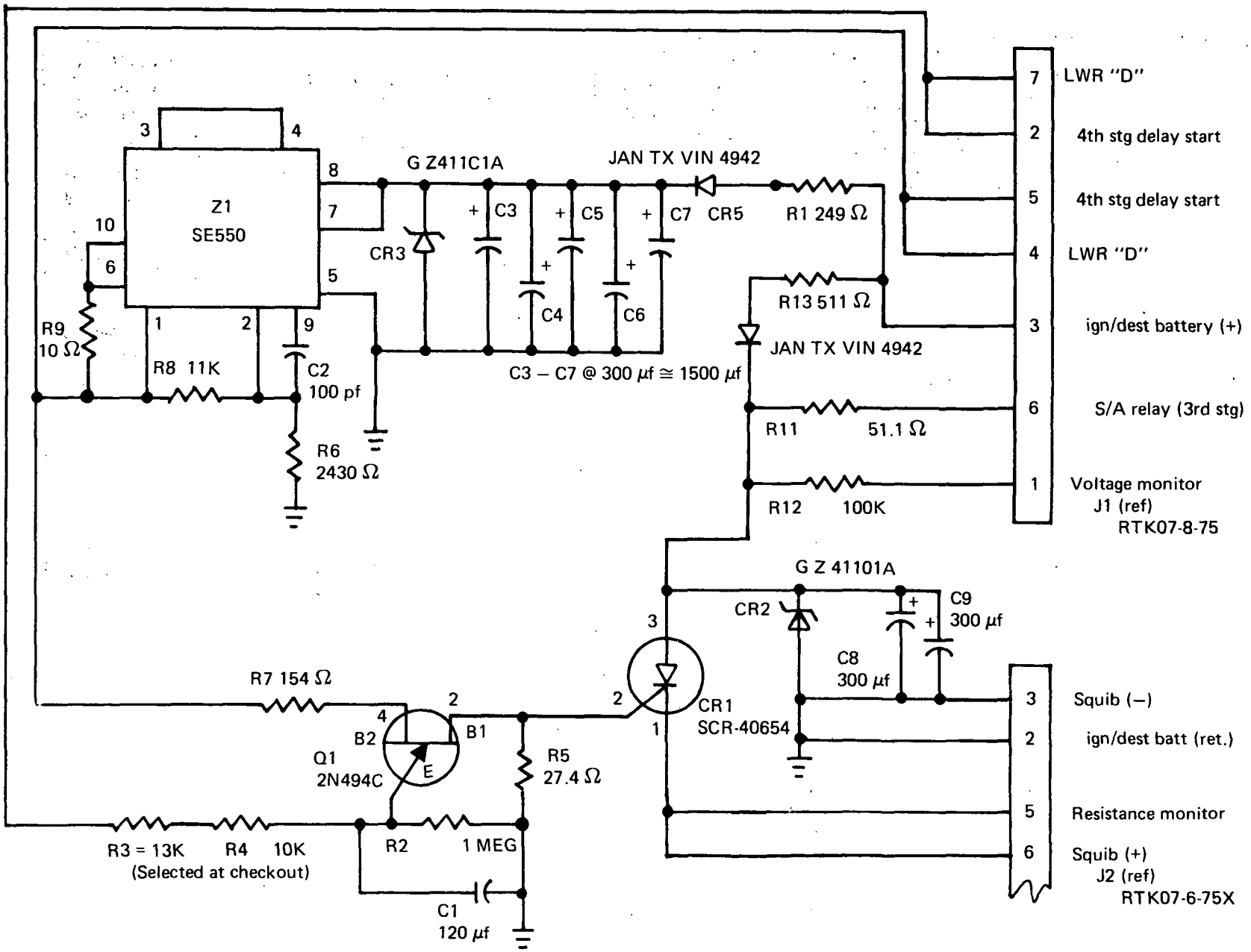


FIGURE 13. – EDIM CIRCUIT FOR QUALIFICATION TEST

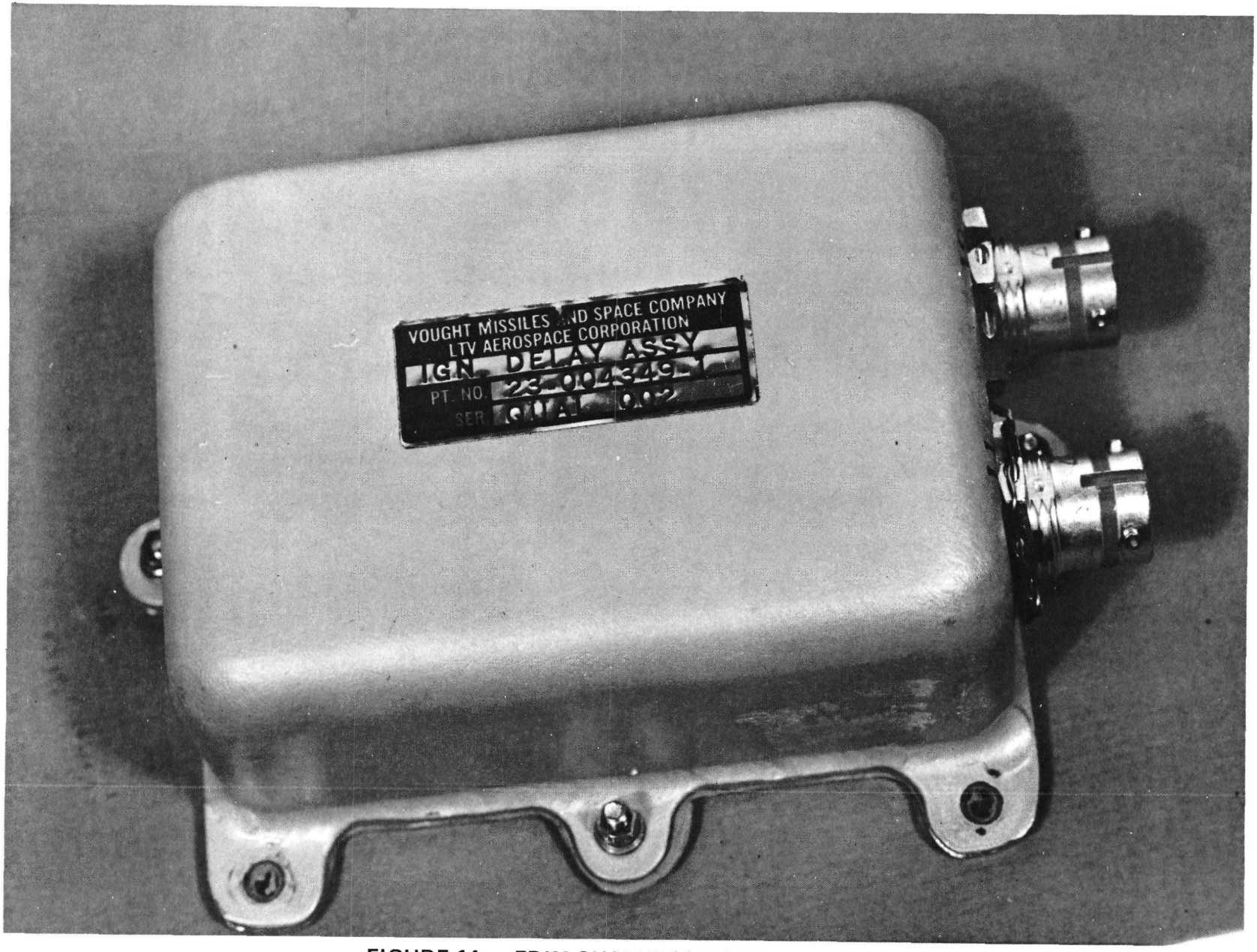


FIGURE 14. – EDIM QUALIFICATION MODULE

6.1 Qualification Test

The EDIM was qualified for Scout flight application by successful execution of the functional requirements during and after exposure to the Scout Standard Design Qualification Environment. The EDIM test specimen was subjected to the following operational environments:

a. High Temperature/Low Temperature (71°C/−17.8°C)
b. Temperature Shock
c. High Temperature-Altitude (71°C; Altitude = 0.148 mm of Hg)
d. Vibration/Mechanical Shock (Vibration = 9.1G RMS Random; Shock = ± 75G's 6 millisec sawtooth)
e. Acceleration (33.5 G's)
f. Environmental Cyclic Life (Scout Standard Environmental Test for vibration and shock for a total of 10 cycles)
g. Electromagnetic Susceptibility Test (Requirements per MIL-STD-461A, Notice 2)
h. Humidity (Non-operational test with relative humidity 95% at 49°C)

6.2 Test Results

Details and results of the Qualification testing listed above is shown in Appendix E. The EDIM functioned as designed without an operational failure during and after exposure to the environmental tests as delineated in Appendix E. The only corrective action indicated by the EDIM Qualification program was improper bonding of the silver filled epoxy paint. Review of the paint process specification indicated an incomplete call-out for the paint operation. Before SBASI compatibility testing at LRC the EDIM test specimen was repainted then endured temperature cycling during SBASI testing without paint failure.

7.0 SBASI COMPATIBILITY TEST

In order to prove capability of the EDIM to meet the design requirement of SBASI ignition, forty-nine igniters were fired at LRC. Test variables during these tests were input voltage and temperature. The SBASI's used were Part Number SEB 26100001-211, manufactured in August 1969, lot number 13-31077. Table VI depicts SBASI serial numbers and the test conditions under which each was ignited. Table VII is a summary of the SBASI firing data. Igniter serial numbers 0562 and 0514 were subjected to increasing input voltage, starting at 12 volts and increasing in two-volt steps until the igniter fired. The achieved ignition at 16 volts compares to the predicated analytical worst case value of 17 volts (reference Appendix D, addendum).

TABLE VI. – TEST SUMMARY SBASI FIRING

	SBASI Serial No.	Test Temp. °C	Input Voltage Volts	Comment
1	0562	23.9	16	Fired to collaborate analytical calculations
2	0514	23.9	16	
3	0653	23.9	30	3 SBAS's fired at amb. temp., 30 volts input to EDIM
4	0546	23.9	30	
5	0643	23.9	30	
6	0493	23.9	35	5 SBASI's fired at amb. temp., 35 volts input to EDIM
7	0465	23.9	↓	
8	0490	↓	↓	
9	0428	↓	↓	
10	0538	23.9	35	
11	0471	71	30	5 SBAS's fired at hot temp., 30 volts input to EDIM
12	0519	↓	↓	
13	0655	↓	↓	
14	0414	↓	↓	
15	0693	↓	30	
16	0451	↓	35	5 SBASI's fired at hot temp., 35 volts input to EDIM
17	0675	↓	↓	
18	0610	↓	↓	
19	0555	↓	↓	
20	0412	71	35	
21	0501	−17.8	30	10 Total SBASI's fired at this condition cold temp., 30 volts input to EDIM
22	0557	↓	↓	
23	0603	↓	↓	
24	0422	↓	↓	
25	0406	↓	↓	
26	0398	↓	↓	
27	0405	↓	↓	
28	0660	↓	↓	
29	0397	↓	↓	
30	0395	↓	30	
31	0360	↓	35	10 Total SBASI's fired at this condition cold temp., 35 volts input to EDIM
32	0463	↓	↓	
33	0551	↓	↓	
34	0518	↓	↓	
35	0536	↓	↓	
36	0608	↓	↓	
37	0672	↓	↓	
38	0695	↓	↓	
39	0425	↓	↓	
40	0244	−17.8	35	
41	0590	23.9	30	5 SBASI's fired at amb. temp., 30 volts input to EDIM post test evaluation
42	0520	↓	↓	
43	0396	↓	↓	
44	0566	↓	↓	
45	0692	23.9	30	

TABLE VII. – ENVIRONMENTAL LAB FIRING SHEET

Serial No.	EDIM Input Voltage	Firing Bridge Ohms	Conditioning Temp °C	Function Time Pressure MS	Delay Time Sec.	Squib Voltage	Function Time BW Break MS
0653	30	1.104	23.9	.205	3.728	24.96	.176
0562	16	1.023	23.9	.833	2.447	12.74	.833
0514	16	1.028	23.9	2.222	2.443	13.13	2.31
0546	30	.987	23.9	.196	3.726	23.96	.162
0643	30	.974	23.9	.219	3.726	24.57	.167
0493	35	1.033	23.9	.195	3.735	25.61	.162
0465	35	1.019	23.9	.186	3.731	25.61	.186
0490	35	.989	23.9	.176	3.731	25.61	.162
0428	35	.969	23.9	.195	3.731	25.48	.167
0538	35	.997	23.9	.190	3.734	25.87	.152
0501	30	1.001	– 17.8	.248	3.703	21.97	.214
0557	30	1.005	– 17.8	.248	3.701	22.1	.219
0603	30	1.019	– 17.8	.209	3.701	22.23	.209
0422	30	1.025	– 17.8	.228	3.701	21.97	.205
0406	30	1.076	– 17.8	.243	3.702	22.23	.219
0398	30	1.062	– 17.8	.233	3.700	21.97	.214
0405	30	1.067	– 17.8	.248	3.702	22.23	.219
0660	30	.984	– 17.8	.248	3.700	21.97	.219
0397	30	.985	– 17.8	.238	3.701	21.97	.195
0395	30	.985	– 17.8	.209	3.706	21.58	.190
0360	35	1.023	– 17.8	.238	3.704	22.49	.214
0463	35	1.012	– 17.8	.243	3.702	22.23	.209
0551	35	.990	– 17.8	.219	3.704	22.1	.190
0518	35	1.108	– 17.8	.248	3.704	22.62	.228
0536	35	1.008	– 17.8	.233	3.705	22.36	.209
0608	35	.982	– 17.8	.224	3.705	22.36	.195
0672	35	10.23	– 17.8	.224	3.705	22.49	.205
0695	35	.997	– 17.8	.228	3.707	22.1	.205
0425	35	1.025	– 17.8	.243	3.707	22.75	.209
0244	35	1.075	– 17.8	.224	3.706	23.01	.200
0471	30	.991	71	.200	3.768	26.65	.152
0519	30	.989	71	.190	3.772	26.65	.152
0655	30	1.007	71	.195	3.767	26.15	.143
0414	30	1.006	71	.205	3.772	26.65	.162
0693	30	1.040	71	.205	3.769	26.65	.150
0451	35	1.035	71	.214	3.776	27.95	.157
0675	35	1.038	71	.200	3.776	27.43	.148
0610	35	1.049	71	.214	3.765	27.67	.162
0555	35	1.014	71	.209	3.774	27.69	.143
0412	35	.996	71	.224	3.777	27.69	.143
0590	30	1.029	23.9	.200	3.730	25.48	.162
0520	30	1.041	23.9	.186	3.728	25.22	.143
0396	30	1.064	23.9	.205	3.728	25.22	.167
0566	30	1.038	23.9	.190	3.733	25.35	.152
0692	30	1.032	23.9	.195	3.728	25.09	.162

It should be noted that ignition was achieved at the lowest voltage level that would gate the SCR "ON", which indicated the 16 volts level is an SCR gate drive requirement and not necessarily an indication of SBASI minimum firing energy. Initiator Serial Nos. 0244, 0693, 0451, 0675, 0610, 0555, 0412, 0590, 0520, 0396, 0566 and 0692 (12 total) were subjected to a firing cycle with the safe-arm switch closed before firing at the listed input voltage. This verified that the initiators would not fire during checkout of the EDIM with the safe-arm relay closed. With the safe-arm relay closed, a 2.8 volt/600 μf pulse of energy is discharged into the initiator. From the data shown in Table VII it is noted that Bridgewire break function time (time from current application to bridgewire break) is shorter than pressure function time (time from current application to first indication of pressure) except the two initiators fired at minimum voltage (0562 and 0514). The shorter bridgewire break time is an indication that melting the bridgewire was caused by the level of current applied rather than burning propellant. This is another indication of energy margin for firing SBASI.

Results of these tests prove capability to meet design requirements of SBASI ignition at worst case environmental conditions.

8.0 SCOUT INTEGRATION

8.1 Existing System

A representation of one of the redundant pair of existing Scout 4th Stage Ignition Systems is shown in Figure 15. The chronological sequence of ignition for one system of the redundant pair is as follows:

1. 2nd Stage Ignition, K3 closes
2. Heatshield Separation, K15 closes
3. 3rd Stage Ignition, K5 closes
4. 3rd Stage Burn and Coast Phase ($\approx$ 300 sec)
5. Spin Motor and 4th Stage Delay (5.5 to 7.2 sec), K9 closes
6. 4th Stage Cable is disconnected during spin up
7. Explosive Bolts; 3rd, 4th stage separation clamps; K7 closes (1.5 sec delay from spin motor ignition)
8. 4th Stage Motor Ignition (5.5 to 7.2 sec. delayed from Step 5 above)

Note should be taken of the shaped charge shown in the ignition diagram of the existing Scout system. This shaped charge is part of the destruct system which is designed to remove ignition power from unused initiators in the event that the vehicle must be destroyed. The Range Safety destruct requirement effectively directs the time in the ignition sequence that power can be applied to the EDIM since after the firing capacitors are charged, the shaped charge will not remove initiator power. Figure 16 shows the delay initiator presently used for Scout 4th stage ignition. Weight of the existing unit is approximately 90.7 gram (0.2 pound) not including connectors and associated cabling. Delay time at 23.88^{o}C $\pm$ 2.77^{o}C (75^{o}F $\pm$ 5^{o}F) varies from 5.5 seconds to 7.2 seconds. Maximum operational temperature range is +4.44^{o}C to +37.77^{o}C (40^{o}F to 100^{o}F) with no specified delay accuracy at these limits. The initiator used to start the delay train is similar to the SBASI in that it is a "one amp-one watt no fire device" with one ohm bridgewires. It differs from a SBASI by being a dual bridgewire device with less stringent specifications (i.e. Bridgewire resistance = 1.0 – 1.8 ohms, SBASI = 1.05 $\pm$ 0.1 ohms).

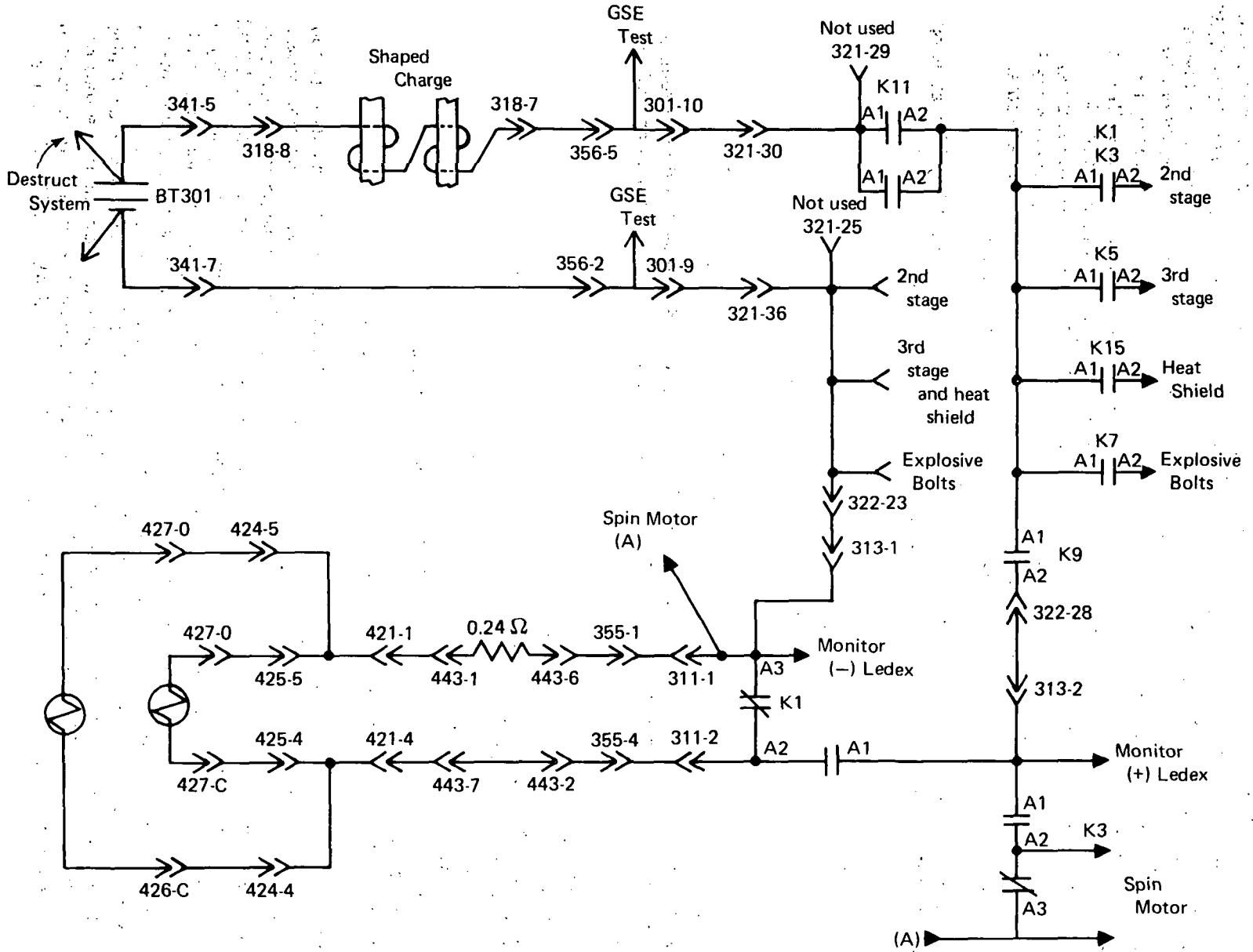


FIGURE 15. – EXISTING SCOUT 4TH STAGE IGNITION SYSTEM 1

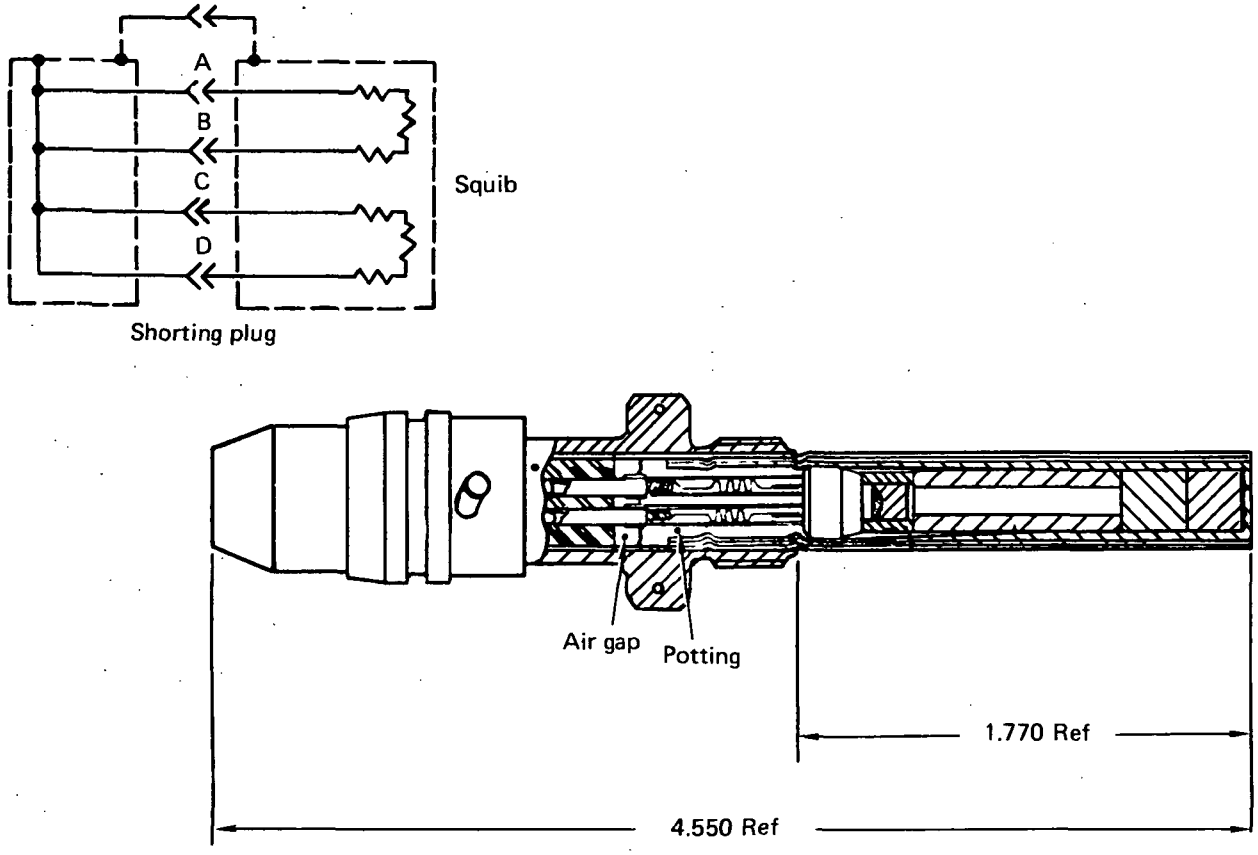


FIGURE 16. – SD60A1 DELAY SQUIB

8.2 EDIM System

The EDIM (Figure 14) weighs 237 grams (8.359 ounces). It is estimated that implementation of the EDIM system will increase 4th stage weight approximately 544 grams (1.2 pounds) for a totally redundant system. Proposed vehicle mounting of the EDIM is on the Upper "D" Section with standoff pads to eliminate the need for fitting the curvature of the conical section. The EDIM system is more complex from a component count standpoint, but the test and checkout capability inherent with the system enhances the reliability (Reference Appendix D, paragraph 5.0).

8.3 Vehicle Integration

8.3.1. – Lower "D" Interface – one method of integrating the EDIM into vehicle wiring is to interface the Ground Support Equipment (GSE) through the Lower "D" Section. Figure 17 depicts the wiring changes necessary to implement the EDIM. The relay (K16) shown added to the Power Control Relay Box (PCRB) could be added to the vehicle at any place and is shown in the PCRB for convenience only. Relay K16 is necessary since spare isolated contacts do not exist in the guidance system. One disadvantage to the EDIM checkout being through the Lower "D" Section is an umbilical connector would have to be added. Although sufficient spare pins are available in the existing Lower "D" umbilical connector, use of these pins would violate range safety guidelines by intermixing ignition wiring with other vehicle wiring.

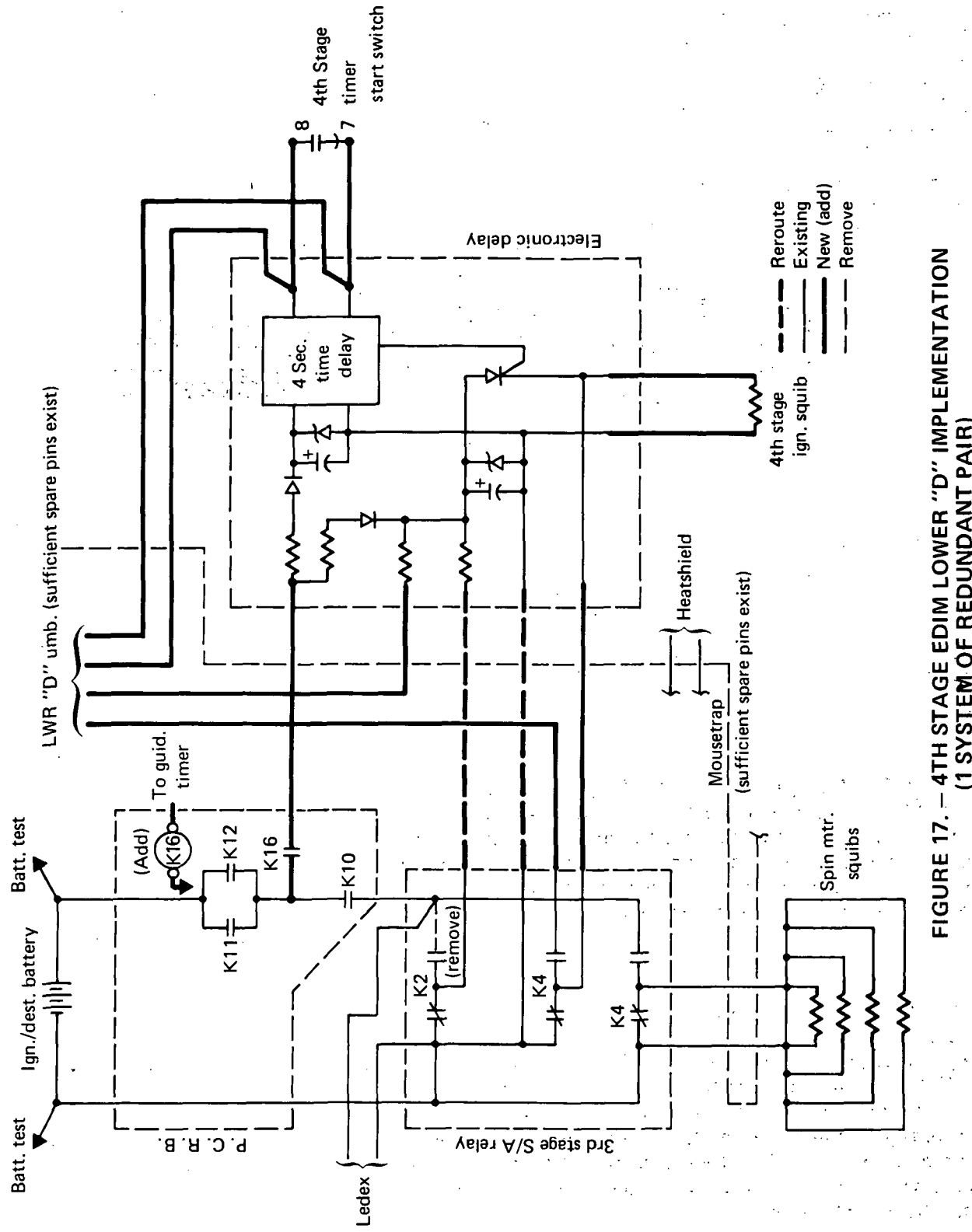


FIGURE 17. – 4TH STAGE EDIM LOWER "D" IMPLEMENTATION (1 SYSTEM OF REDUNDANT PAIR)

8.3.2. – 4th Stage Interface – a second method of integrating the EDIM into the Scout vehicle is to interface the GSE through the 4th stage module umbilical connector. As can be seen from Figure 18, the vehicle wiring modifications are very similar with either alternative. The existing payload umbilical connector has enough unused pins to accommodate a redundant pair of EDIM's. However, all Scout missions do not require a 4th stage module; therefore, an option would have to be provided so that an umbilical connector is always available. This vehicle modification would consist of a mounting bracket, connector and associated wiring for the case where 4th stage payload ring (umbilical connector mounting) is not used.

8.4 Vehicle Checkout

8.4.1 – Method – the EDIM can be functionally tested on the vehicle by use of the remote start and monitor points provided in the design. Operationally the following measurements will be made at the vehicle level checkout:

1. Delay Time – Use an electronic counter with time interval measurement capability. Start counter with remote start switch and stop the counter with current pulses across simulated squib (one ohm resistor).

2. Length of Time Voltage Regulator (Z1) (Figure 11) will maintain regulation after power removal. Monitor J1-4, J2-2 (Figure 11) with digital voltmeter, then remove power to EDIM, measure with a stop watch the time to loss of regulation (LOR). The LOR measurement verifies that the power storage capacitors, Z1 (voltage regulator), zener diode (CR3), diode (CR5) and associated resistors are in the same condition as during component level test.

3. Firing capacitor charge voltage – Monitor J1-1, J2-2 with high impedance (10 megohms) digital voltmeter to verify proper voltage level and after input power removal to verify leakage rate of firing capacitors.

4. Firing Energy can further be verified by connecting an oscilloscope across the dummy load (1 ohm) and obtaining a photograph of the voltage during capacitor discharge. Comparison of this voltage trace at 100 microsecond and 2 millisecond with the component level test data will verify proper energy transfer for ignition.

8.4.2 – Ground Support Equipment (GSE) – with either of the vehicle modifications (Reference Paragraphs 8.3.1 and 8.3.2), launch pad to blockhouse wiring (Cables, J-box and connectors) will have to be provided. No special test equipment other than a test panel such as shown in Figure 19 will be needed. Checkout equipment needed for the EDIM is: (a) Power Supply 0-35 volt, (b) Oscilloscope, (c) Oscilloscope Camera, (d) Digital Voltmeter ($>$ 10 megohm input impedance), (e) Stop Watch, (f) Test Panel (Figure 19).

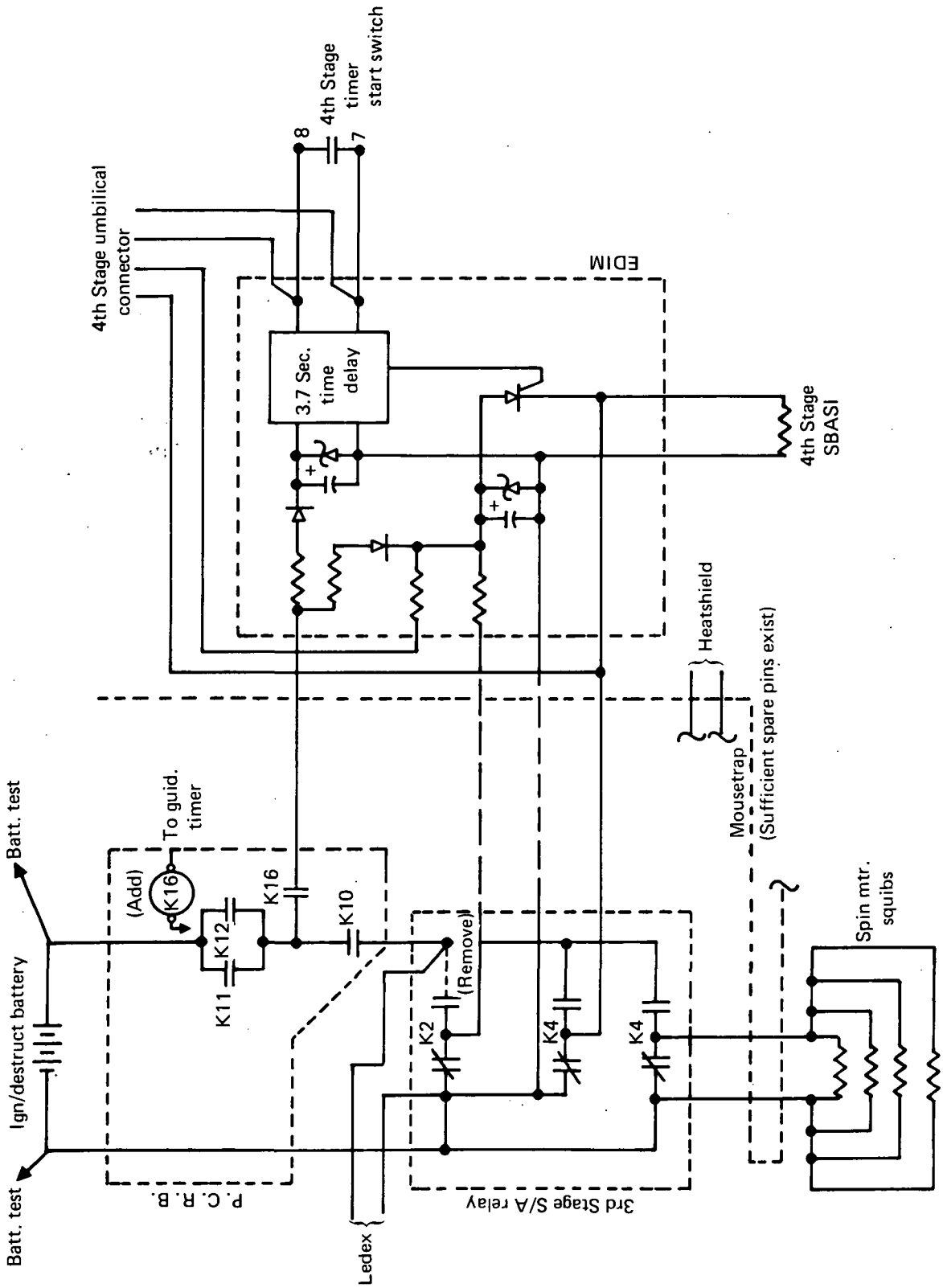


FIGURE 18. – 4TH STAGE EDIM IMPLEMENTATION GSE ACCESS THRU 4TH STAGE (1 SYSTEM OF A REDUNDANT PAIR)

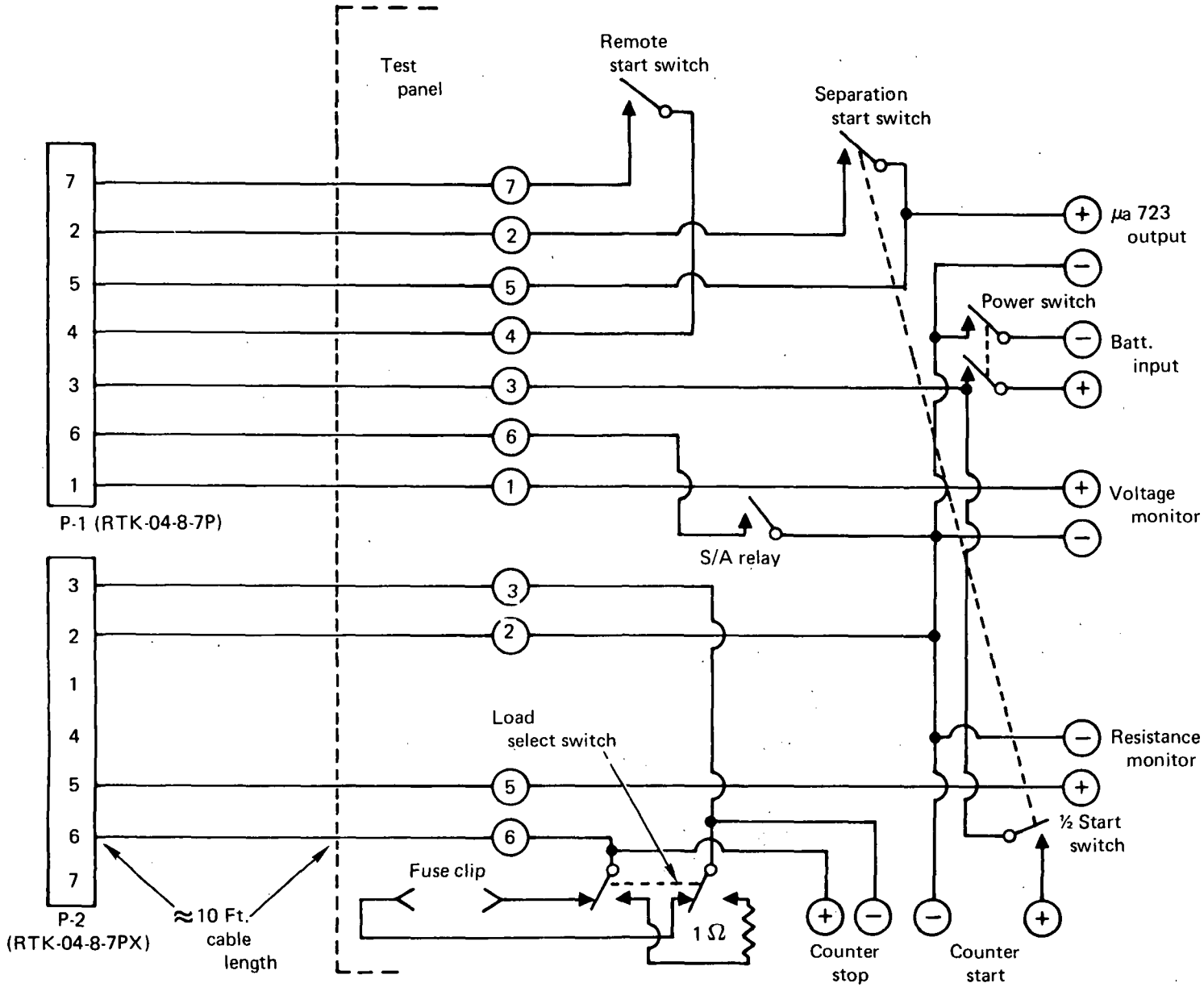


FIGURE 19. – EDIM TEST PANEL

9.0 CONCLUSIONS

The EDIM has been fully qualified by analysis and test for Scout flight application. Exhaustive testing as documented in Appendix E and Reliability analyses documented in Appendix D showed the EDIM to be adequately designed. Analysis showed the worst case SBASI ignition requirements to be exceeded by more than 2 to 1 (i. e., 157% safety factor). Forty-five SBASI's were successfully ignited at voltage and temperature extremes during tests at LRC substantiating the EDIM's SBASI ignition capability. The EDIM reliability prediction contained in Appendix D indicates a mission reliability value greater than 0.9999. This value is a quantitative estimate of the probability that no catastrophic piece-part failure will occur during the EDIM mission function period. To assure achievement of the predicted high reliability during production, piece-part selection/screening criteria were included in the EDIM drawings. As a result of the increased checkout capability and separation of the 4th stage ignition wiring from the spin motor ignition wiring, a fourth stage weight penalty will be incurred. The fourth stage weight increase incurred by implementing the EDIM will not exceed 544 grams (1.2 pounds) for a totally redundant system. As part of the qualification test program, the EDIM successfully passed an electromagnetic interference (EMI) test which exceeded Scout requirements. Based on the test results, GSE and vehicle integration impact, the EDIM is suitable for use in the Scout vehicle.

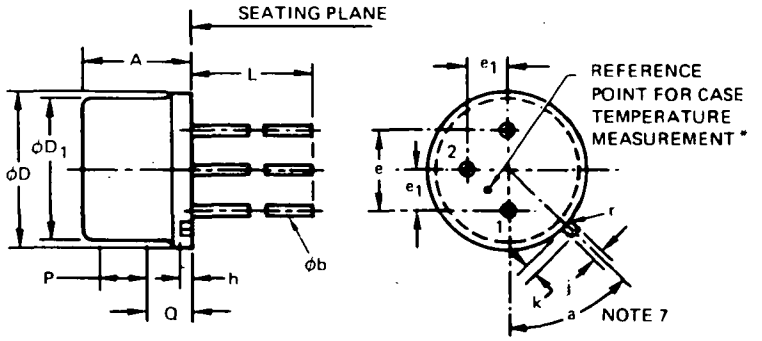
APPENDIX A
SPECIFICATION FOR SILICON CONTROLLED RECTIFIER

I. SILICON CONTROLLED RECTIFIER (SCR) TO BE DESIGNED FOR POWER SWITCHING CIRCUITS.

II. ELECTRICAL CHARACTERISTICS;

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
INSTANTANEOUS FORWARD BREAKOVER VOLTAGE: GATE OPEN AT T_C = +100°C	$V_{F(BO)O}$	250	–	–	V
PEAK OFF-STATE CURRENT: (GATE OPEN, T_C = +100°C) FORWARD, $V_{DO} = V_{DROM}$	I_{DOM}	–	0.1	0.5	mA
REVERSE (REPETITIVE), $V_{RO} = V_{RROM}$	I_{RROM}	–	0.05	0.5	mA
INSTANTANEOUS ON-STATE VOLTAGE: FOR i_T = 30 A AND T_C = +25°C	v_T	–	1.9	2.6	V
DC GATE TRIGGER CURRENT V_D = 12V (DC) R_L = 30Ω T_C = +25°C	I_{GT}	–	6	15	mA
DC GATE TRIGGER VOLTAGE: V_D = 12V (DC) R_L = 30Ω T_C = +25°C	V_{GT}	–	0.65	1.5	V
INSTANTANEOUS HOLDING CURRENT: GATE OPEN AND T_C = +25°C	i_{HO}	–	9	20	mA
CRITICAL RATE-OF-RISE OF OFF-STAGE VOLTAGE: $V_{DO} = V_{F(BO)O}$ MIN. VALUE EXPONENTIAL RISE, T_C = +100°C	dv/dt	20	200	–	V/μs
GATE CONTROLLED TURN-ON TIME: $V_D = V_{F(BO)O}$ MIN. VALUE, i_T = 4.5A I_{GT} = 200 mA, 0.1 μs RISE TIME T_C = +25°C	t_{gt}	–	1.5	–	μs
CIRCUIT COMMUTATED TURN-OFF TIME: $V_D = V_{F(BO)O}$ MIN. VALUE, i_T = 2A PULSE DURATION = 50μs dv/dt = −20V/μs, di/dt = −30 A/μs I_{GT} = 200 mA AT TURN ON, T_C = +75°C	t_q	–	15	50	μs

III. DIMENSIONAL OUTLINE:



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.160	.180	4.06	4.57	
ϕb	.017	.021	.432	.533	2
ϕD	.355	.366	9.017	9.296	
ϕD_1	.323	.335	8.204	8.51	
e	.190	2.10	4.83	5.33	
e_1	.100 TRUE POSITION		2.54 TRUE POSITION		4, 5
h	.015	.035	.381	.889	
j	.028	.035	.711	.889	5
k	.029	.045	.737	1.14	3, 5
L	.985	1.015	25.02	25.78	2
P	.100		2.54		1
Q					6
r		.007		.179	
a	42^{O}	48^{O}			5, 7

NOTES:

1. THIS ZONE IS CONTROLLED FOR AUTOMATIC HANDLING. THE VARIATION IN ACTUAL DIAMETER WITHIN THE ZONE SHALL NOT EXCEED .012 IN. (.279 MM).
2. (THREE LOADS) ϕb APPLIES BETWEEN SEATING PLANE AND 1.015 IN. (25.78 MM).
3. MEASURED FROM MAXIMUM DIAMETER OF THE ACTUAL DEVICE.
4. LEADS HAVING MAXIMUM DIAMETER .021 IN. (.533 MM) MEASURED AT THE SEATING PLANE OF THE DEVICE SHALL BE WITHIN .007 IN. (.178 MM) OF THEIR TRUE POSITIONS RELATIVE TO THE MAXIMUM WIDTH TAB.
5. THE DEVICE MAY BE MEASURED BY DIRECT METHODS OR BY THE GAGE AND GAGING PROCEDURE DESCRIBED ON GAGE DRAWING GS-1 OF JEDEC PUBLICATION 12E, MAY 1964.
6. DETAILS OF OUTLINE IN THIS ZONE OPTIONAL.
7. TAB CENTERLINE.

*CASE TEMPERATURE MEASUREMENT

THE SPECIFIED TEMPERATURE-REFERENCE POINT SHOULD BE USED WHEN MAKING TEMPERATURE MEASUREMENTS. A LOW-MASS TEMPERATURE PROBE OR THE THERMOCOUPLE HAVING WIRE NO LARGER THAN AWG NO. 26 SHOULD BE ATTACHED AT THE TEMPERATURE REFERENCE POINT.

APPENDIX B
723 VOLTAGE REGULATOR

723

Electrical characteristics (See Note)

Parameter	Conditions	Min.	Typ.	Max.	Units
Line regulation	V_{IN} = 12V to V_{IN} = 15V		0.01	0.1	% V_{OUT}
	V_{IN} = 12V to V_{IN} = 40V		0.02	0.2	% V_{OUT}
	$-55^{o}C \leq T_A \leq +125^{o}C$, V_{IN} = 12V to V_{IN} = 15V			0.3	% V_{OUT}
Load regulation	I_L = 1 mA to I_L = 50 mA		0.03	0.15	% V_{OUT}
	$-55^{o}C \leq T_A \leq +125^{o}C$, I_L = 1 mA to I_L = 50 mA			0.6	% V_{OUT}
Ripple rejection	f = 50 Hz to 10 kHz		74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		0.6		dB
Average Temperature Coefficient of output voltage	$-55^{o}C \leq T_A \leq +125^{o}C$		0.002	0.015	%/^{o}C
Short circuit current limit	R_{SC} = 10 Ω, V_{OUT} = 0		65		mA
Reference voltage		6.95	7.15	7.35	V
Output noise voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20		μV_{rms}
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μf		2.5		μV_{rms}
Long term stability			0.1		%/1000 hrs
Standby current drain	I_L = 0, V_{IN} = 30V		2.3	3.5	mA
Input voltage range		9.5		40	V
Output voltage range		2.0		37	V
Input/output voltage differential		3.0		38	V

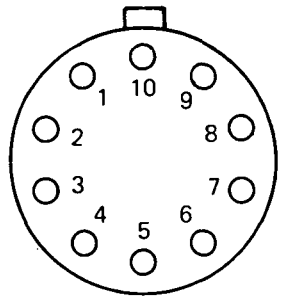
Note:

Unless otherwise specified, $T_A = 25^{o}C$, $V_{IN} = V+ = V_C = 12$ V, V– = 0, $V_{OUT} = 5.0$ V, $I_L = 1.0$ mA, $R_{SC} = 0$, C1 = pF, $C_{REF} = 0$ and divider impedance as seen by error amplifier $\leq$ 10K Ω connected.

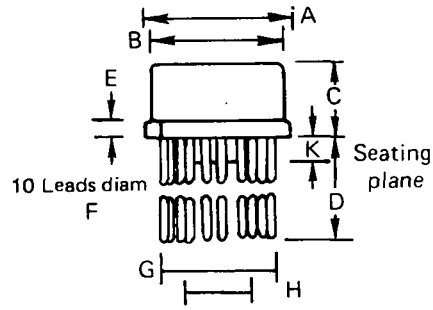
Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

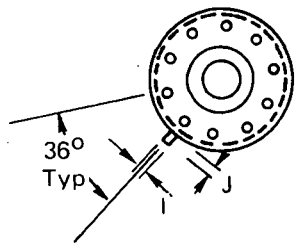
723

Electrical Characteristics (Continued)

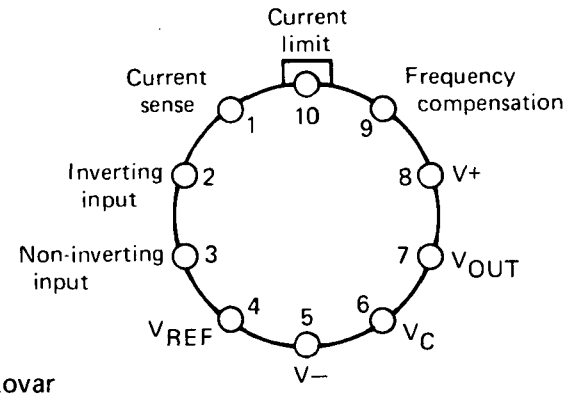


1. Current Sense
2. Inverting Input
3. Noninverting Input
4. V_{REF}
5. V−
6. V_{OUT}
7. V_C
8. V+
9. Frequency Compensation
10. Current Limit





Notes
Leads are gold plated kovar
package weight is 1.32 grams
high thermal resistance package
nine leads through, lead no. 5
is connected to case



	Inches			Millimeters		
Dim	Min	Typ	Max	Min	Typ	Max
A	0.335		0.370	8.51		9.40
B	0.305		0.335	7.75		8.51
C	0.165		0.185	4.19		4.70
D	0.500			12.70		
E			0.040			1.02
F	0.016		0.019	0.41		0.48
G		0.230			5.84	
H		0.115			2.92	
I	0.028		0.034	0.71		0.86
J	0.029		0.045	0.74		1.14
K			0.040			1.02

APPENDIX C
550 VOLTAGE REGULATOR

(T_A = 25°C unless otherwise specified) (Notes 1 and 2)

Parameter	Min	Typ	Max	Units	Test Conditions
			NE550		
Line regulation		.08	0.3	% V_{OUT}	V_{IN} = 8.5 to 40V
			0.35	% V_{OUT}	0°C ≤ T_A ≤ 70°C V_{in} = 12 to 40V
Load regulation		.03	0.2	% V_{OUT}	I_L = 1 mA to 50 mA
			0.4	% V_{OUT}	0°C ≤ T_A ≤ 70°C, I_L = 1 mA to 50 mA
Ripple rejection		75		dB	f = 50 Hz to 10 kHz, CREF = 0
		90		dB	f = 50 Hz to 10 kHz, CREF = 5 μF
Average temperature coefficient of output voltage		.002	.015	%/°C	0°C ≤ T_A ≤ 70°C
Start circuit current limit	50	60	70	mA	RSC = 10 Ω V_{OUT} = 0
Reference voltage	1.53	1.63	1.73	V	
Output Noise Voltage		20		μV rms	BW = 100 Hz to 10 kHz, CREF = 0
		2.5		μV rms	BW = 100 Hz to 10 kHz, CREF = 5 μF
Long term stability		0.1		%/1000 hrs.	
Standby current drain		1.6	3.0	mA	I_L = 0, V_{IN} = 40V
Input voltage range	8.5		40	V	
Output voltage range	2.0		37	V	
Input–output voltage differential	3.0		38	V	

Notes:

1) Unless otherwise specified, T_A = 25°C, V_{IN} = V+ = V_C = 12V, V– = 0V, V_{OUT} = 5V, I_L = 1 mA, R_{SC} = 0, C_1 = 100 pF, and divider impedance as seen by error amplifier ≃ 2k Ω when connected as shown in Figure 1.
2) The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high or varying dissipation.

550 Voltage regulator ($T_A = 25^oC$ unless otherwise specified) (Notes 1 and 2)

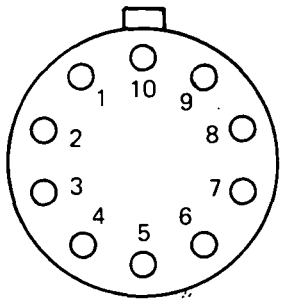
SE550					
Parameter	Min	Typ	Max	Units	Test Conditions
Line regulation		0.05	0.1	% V_{OUT}	V_{IN} = 12 to 40V
		0.2	0.6	% V_{OUT}	V_{IN} = 8.5 to 50V
			0.25	% V_{OUT}	$-55^oC \leqslant T_A \leqslant +125^oC$, V_{IN} = 12 to 40V
Load regulation		0.3	.10	% V_{OUT}	I_L = 1mA to 50mA
			.6	% V_{OUT}	$-55^oC \leqslant T_A \leqslant +125^oC$, I_L = mA to 50mA
Ripple rejection		75		dB	F = 50 Hz to 10 kHz, CREF = 0
		90		dB	F = 50 Hz to 10 kHz, CREF = 5μF
Average temperature coefficient of output voltage		.002	.012	%/^{o}C	$-55^oC \leqslant T_A \leqslant +125^oC$
Short circuit limit	50	60	70	mA	RSC = 10Ω, V_{OUT} = 0
Reference voltage	1.58	1.63	1.68	V	
Output noise voltage		20		μV rms	BW = 100 Hz to 10 kHz, CREF = 0
		2.5		μV rms	BW = 100 Hz to 10 kHz, CREF = 5μF
Long term stability		0.1		%/1000 hrs.	
Standby current drain		1.3	2.0	mA	I_L = 0, V_{IN} = 50V
Input voltage range	8.5		50	V	
Output voltage range	2.0		40	V	
Input-output voltage differential	3.0		45	V	

Notes:

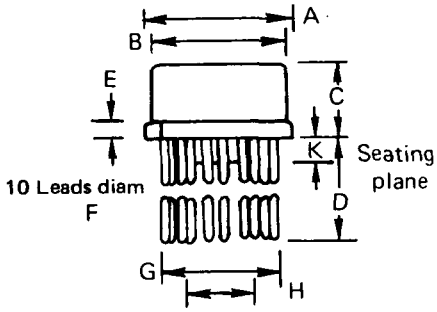
1) Unless otherwise specified, $T_A = 25^oC$, $V_{IN} = V+ = V_C = 12V$, $V- =)V$, $V_{OUT} = 5V$, $I_L = 1$ mA, $R_{SC} = 0$, $C_1 = 100$ pF, and divider impedance as seen by error amplifier $\cong$ 2k Ω when connected as shown in Figure 1.
2) The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high or varying dissipation.

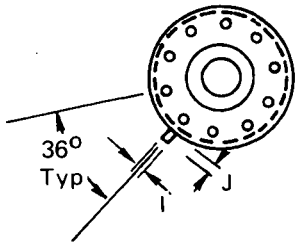
550 Voltage Regulator

(T_A = 25°C unless otherwise specified) (Continued)

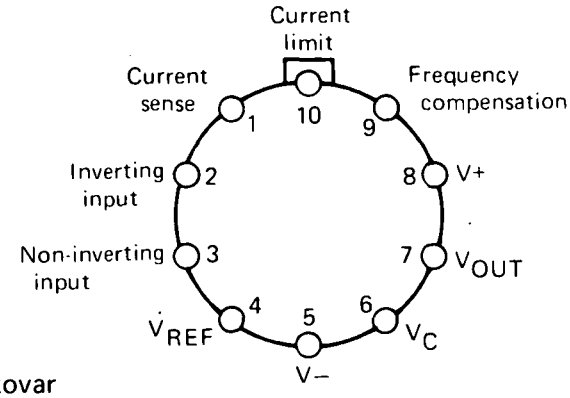


1. Current Sense
2. Inverting Input
3. Noninverting Input
4. V_{REF}
5. V−
6. V_{OUT}
7. V_C
8. V+
9. Frequency Compensation
10. Current Limit





Notes
Leads are gold plated kovar
package weight is 1.32 grams
high thermal resistance package
nine leads through, lead no. 5
is connected to case



	Inches			Millimeters		
Dim	Min	Typ	Max	Min	Typ	Max
A	0.335		0.370	8.51		9.40
B	0.305		0.335	7.75		8.51
C	0.165		0.185	4.19		4.70
D	0.500			12.70		
E			0.040			1.02
F	0.016		0.019	0.41		0.48
G		0.230			5.84	
H		0.115			2.92	
I	0.028		0.034	0.71		0.86
J	0.029		0.045	0.74		1.14
K			0.040			1.02

APPENDIX D
RELIABILITY EVALUATION REPORT

TITLE

RELIABILITY EVALUATION OF SCOUT FOURTH STAGE ELECTRONIC DELAY IGNITION MODULE

SUBMITTED UNDER	
Task R-59	
REPORT NO.	DATED
2-54232/5R-23013	9 June 1975
PROJECT	CONTRACT NO.
Scout	NAS1-12500

F. H. Harrison Jr.
F. H. Harrison
Supervisor - Reliability
Design & Control

J D Clark Jr.
PREPARED
J. D. Clark

REVIEWED

Joe Martinez
J. Martinez
Manager - Scout
Quality & Reliability

REV.	DATE	REV. BY	PAGES AFFECTED	REMARKS

SUMMARY

The reliability evaluation revealed that the Electronic Delay Ignition Module (EDIM) has a predicted potential reliability performance capability equal or superior to the existing pyrotechnic type delay unit. To achieve this potential the circuit design will require some changes due to several problem areas identified at worst case circuit/environmental conditions. Except for the problem areas identified, the functional design margin achieved was consistent with good reliability practices and component stress values imposed by the design were within specification limits. The functional checkout capability of the design is deemed to be a strong design advantage over the presently used pyrotechnic type (Model SD60A1) squib delay unit.

TABLE OF CONTENTS

1.0 INTRODUCTION

A reliability evaluation of the Scout Fourth Stage Electronic Delay Ignition Module (EDIM) was performed in accordance with the requirements of paragraph 2.3 of the EDIM statement of work and satisfies the Reliability Engineering provisions of Section 3 of the Reliability Program Plan for Scout Program Support (LTV Report No. 23.203H, 1 November 1973).

This reliability evaluation applies to the EDIM Engineering Unit design as it exists at this time. The reliability evaluation will be updated to reflect any design changes which result from the Design Review, Engineering Model/Qualification Tests and this reliability evaluation.

The primary objective of this evaluation was to define and examine critical design elements then evaluate these for their impact on system reliability. Reliability impact was assessed in terms of a criticality rating for failure modes and in terms of a safety factor or design margin valuation for critical functional design parameters. In addition, a numerical reliability prediction and a piecepart component stress analysis were also performed. The reliability prediction was performed in order that a reliability comparison could be made between the EDIM and the existing pyrotechnic type delay ignition system. The piecepart stress analysis was performed in order to determine the worst case electrical and/or thermal stresses imposed on the components by the EDIM functional operation and environment. The resulting stress values were evaluated for their impact on reliability.

The results of the evaluation were reviewed and recommendations for corrective action were made based on these results.

The results of the failure mode analysis are presented in Table 3.3-I herein. These results include identification of the EDIM single failure modes (to the piecepart component level) and the corresponding effects. Each of the EDIM single failure modes was assessed a criticality value during the analysis. The criticality values obtained define the relative criticality ranking of the failure modes. The higher the assessed criticality ranking, the greater the probability of occurrence of the failure and/or mission impact in the event of its occurrence. The criticality ranking presented is useful in identifying priorities for apportioning any future reliability improvement effort. In addition, the failure mode and effects analysis is also useful in assessing the importance of testing techniques so as to assure that the higher criticality areas receive proportional emphasis during testing procedures.

The results of the functional analysis, presented in Section 3.1 herein, indicate the design margins/safety factors inherent to the circuit design for each of the critical circuit functions required to generate the ignition event. Any functional deficiency is also reflected in these results.

The results of the Component Stress Analysis are presented in Section 3.2.2. These results indicate the levels of electrical and/or thermal stress imposed on the EDIM components for the worst case combination of functional demands, environmental requirements and component parameter values.

Section 4.0 presents a brief summary and discussion of functional and environmental testing of the EDIM. The role of this testing in assuring reliable EDIM performance is examined.

2.0 ELECTRONIC DELAY IGNITION MODULE DESCRIPTION

This section presents a brief physical and functional description of the EDIM.

2.1 Physical Description

The 4th Stage EDIM is depicted in detail in the preliminary assembly drawing 23-004349. The unit measures 4.5 inches by 3.5 inches at the baseplate. Total assembly height is 1.6 inches and the weight is approximately 0.6 pounds. Two connectors provide all of the required electrical interface functions for the EDIM.

Internally the unit contains one Printed Circuit Board (PCB) mounted on four supports. All of the electronic components are mounted on this PCB. The PCB is conformally coated with Type 1B15 conformal coating per 308-9-22, Type II, Class B.

2.2 Functional Description

The Scout Fourth Stage Electronic Delay Ignition Module provides the delayed ignition function for the Scout fourth stage motor. The EDIM provides this function by means of Single Bridgewire Apollo Standard Initiator (SBASI) activation after an electronically timed delay of 3.0 seconds (minimum) from the third/fourth stage separation event. The SBASI initiation is provided by means of capacitive discharge from the EDIM at the end of the timed delay.

A schematic of the EDIM is presented by Figure 2.2-1. Power is provided to the EDIM by the Ignition/Destruct Battery. It is envisioned that Battery Power will be applied to the system by means of a Power Control Relay Box (PCRB) relay closure and then removed at the time of third-fourth stage spin-up event by separation of the "mouse trap" connection.

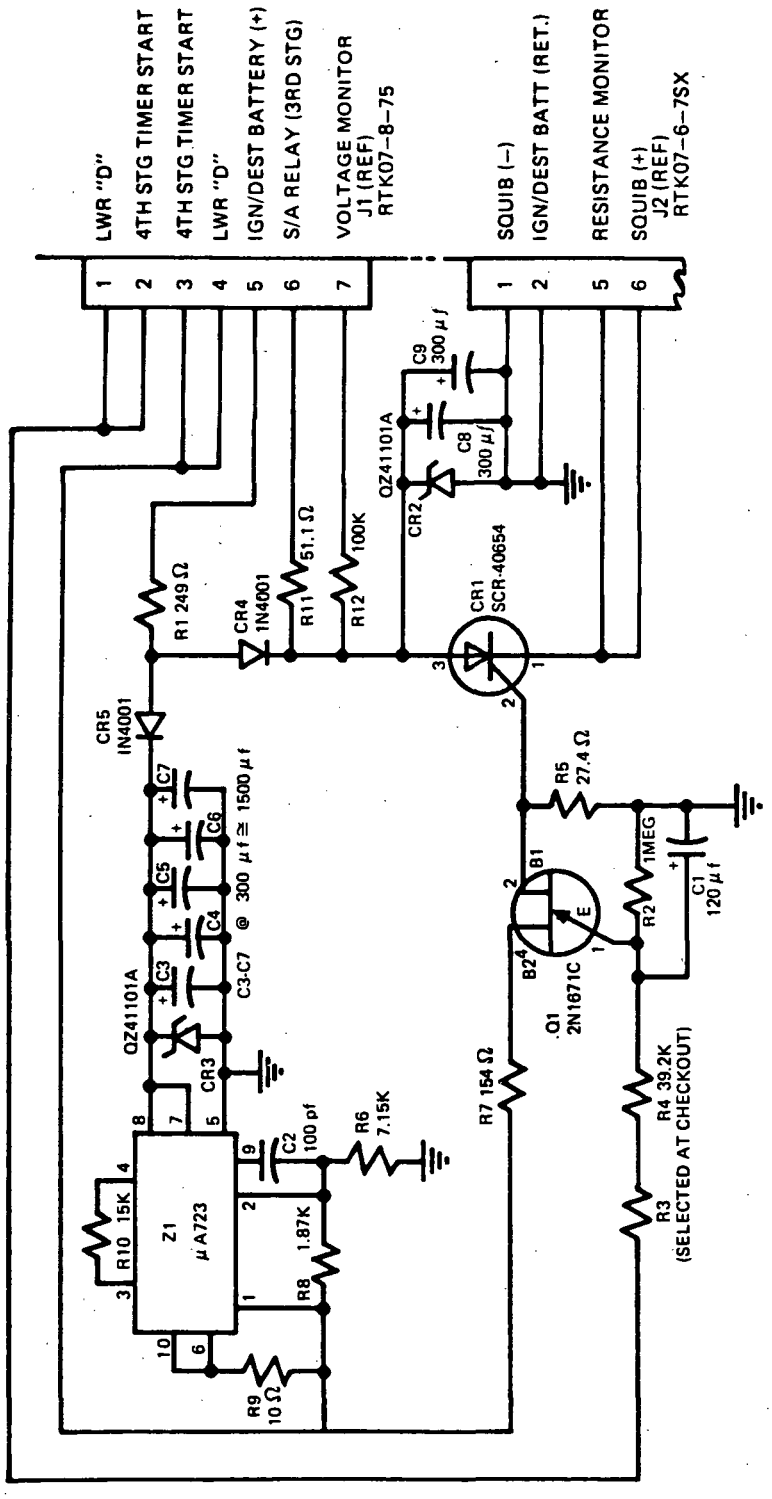


FIGURE 2.2.1 EDIM SCHEMATIC (ENGINEERING UNIT CONFIGURATION)

After battery power is removed from the EDIM the unit completes its function using energy stored in capacitors C3 through C7. These capacitors provide the energy required for the circuitry to complete the delay and ignition functions. The third/fourth stage separation event closes a switch resulting in pins 2 and 3 of connector J1 to become electrically common. This condition causes timing capacitor C1 to begin charging by means of the current through timing resistors R3 and R4. The charging voltage is 9.0 volts regulated by the integrated circuit element Z1. Minimum delay time from the separation event until SBASI initiation is 3.0 seconds. The delay time is determined by the value of the RC time constant of the timing circuit and the peak point voltage (V_P) of the Unijunction Transistor (UJT) designated as Q1. When the voltage at C1 reaches the value "V_P", Q1 turns on and conducts the energy stored in C1 to the gate of SCR (CR1). This action transfers the SCR into the "latched" or "conduction" state. In the conducting state CR1 transfers the stored energy in firing capacitors C8 and C9 into the SBASI squib thereby affecting SBASI initiation and ignition of the 4th stage motor.

The battery voltage provided to the EDIM by the Ignition/Destruct Battery exceeds 30 volts and open circuit voltage is approximately 35 volts. The EDIM is designed to operate under the full range of battery voltage conditions. The circuit includes zener diodes CR2 and CR3 which limit charging voltage at the capacitors C3 to C9 to a nominal value of 30 volts.

3.0 ANALYSIS

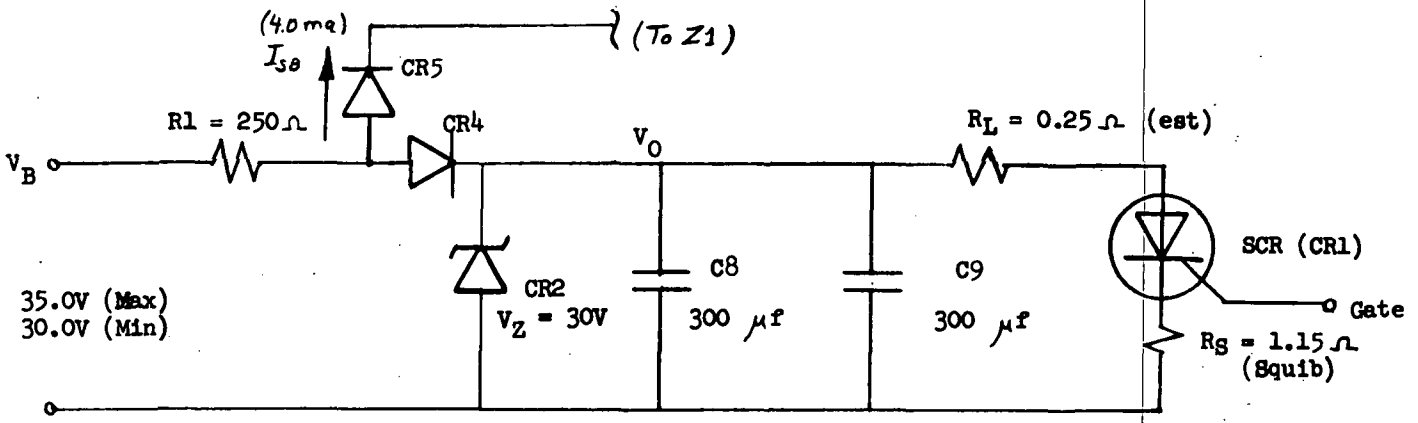
This section presents the EDIM Functional Analysis and Component Stress Analysis. The degree of design margin is assessed and problem areas are identified. The impact of the design margins and/or problem areas is given.

3.1 Functional Analysis

3.1.1 Firing Circuit Analysis

The purpose of this section is to present the results of a functional analysis of the firing circuit under worst case conditions. The worst case conditions imposed include the minimum temperature and worst case extremes for critical component parameters. The analysis was performed to determine if adequate firing circuit performance is achieved under these conditions. Figure 3.1.1-1 is a schematic diagram of the EDIM firing circuit. This circuit performs the SBASI function at the end of a 4.5 second period from the time of battery disconnect. This includes a 1.5 second spin-up time and a 3.0 second (minimum) time delay after the 3rd/4th stage separation event. Worst case values for the critical component parameters are noted in the figure.

Firing capacitors C8 and C9 provide a combined nominal capacitance of 600 microfarads for firing charge storage. The firing capacitance may reach a minimum of 366 microfarads at $0^{\circ}F$ ($-17.8^{\circ}C$). The value of 366 microfarads was obtained from vendor data sheets using linear interpolation to $-17.8^{\circ}C$. Minimum battery voltage to the circuit is 30 volts and the firing capacitors are maintained at 28.3 volts minimum (due to CR4 and R1 voltage drops) for as long as battery power is applied. The firing capacitors must maintain adequate SBASI firing energy after the battery is disconnected, at spin-up, until timed delay has expired. At the end of the electronically timed delay the SCR is triggered into the conduction state allowing the stored firing energy in C8 and C9 to be transferred to the SBASI bridgewire (BW) thereby causing the SBASI to actuate. Resistor R1 and zener CR2 limit maximum capacitor voltage to 30V for those times when maximum Ignition/Destruct Battery voltage is applied. The battery voltage is 35 volts (maximum) at full charge open circuit conditions. Figure 3.1.1-1 resistors R_L and R_S represent the lumped conductor loop resistance and squib resistance respectively.



C8 = C9 = 183 μf (Worst Case Min. @ -17.8°C) Reference Data Sheets

C (Total) = 366 μf (Worst Case)

V_B = 30V (Min., Reference Ign./Dest. Battery Characteristic)

R_L = 0.25 Ω (Estimate)

R_S = 1.15 Ω (Max. Cold Resistance of SBASI Squib)

V_F (SCR) = 2.0V (Maximum Avg. Fwd.Voltage Drop for Applicable Current Range)

I_L (SCR) = 8.0 μa (Worst Measured Leakage of 19 Devices Tested @ 25°C)

V_Z (CR2) = 30V ± 1% (Reference 4)

I_L (CR2) = 1.0 μa (Estimated Leakage)

FIGURE 3.1.1-1
EDIM FIRING CIRCUIT SCHEMATIC

A brief evaluation of the firing circuit parameters obtained from the component data sheets at the temperature extremes to be imposed revealed that worst case SBASI firing conditions occur at the minimum temperature ($0^{\circ}F$). The minimum temperature condition will be imposed during environmental testing even though actual launch temperatures will not be less than the launch constraint values (approximately $20^{\circ}F$) at launch and should increase by an estimated $20^{\circ}F$ by the time of fourth stage ignition.

The EDIM firing circuit design was evaluated in the worst case temperature state using the worst case values for component parameters. The evaluation was performed to determine if adequate design margin for reliable firing of SBASI's has been achieved. As a result of the evaluation it was determined that the design margin achieved was indeed sufficient to justify high confidence in the circuit function. A safety factor was calculated to evaluate numerically the amount of design margin achieved. The safety factor calculated employed the equation:

$$F_S = \frac{E_U - E_C}{E_C}$$

where: E_U = Energy available for heating the SBASI bridgewire during firing capacitor discharge

E_C = Characteristic SBASI firing energy required for the SBASI bridgewire to reach the initiation temperature.

The analysis results given in this section were obtained by modeling the SBASI as in Reference 2. This reference derives a mathematical model using an electro-thermal analogy of the squib which permits definition of bridgewire temperature as a function of power delivered. In the case of capacitive discharge ignition, the following expression for instantaneous bridgewire temperature holds.

$$\theta = I_o^2 R_s \frac{RC\,r}{2rc-RC}\left(e^{-t/rc} - e^{-2t/RC}\right)$$

where: Θ = instantaneous bridgewire temperature
I_0 = initial bridgewire current (@ t = 0)
R_S = bridgewire resistance
RC = firing circuit electrical time constant
rc = squib thermal time constant
t = elapsed time after SCR firing

Differentiating this expression and letting $d\Theta/dt = 0$ the time at which maximum possible bridgewire temperature occurs can be obtained. This time, referred to herein as t(max), is the time beyond which the squib will never fire, because it has passed the point of maximum temperature and is cooling off. The expression for t(max) is as follows.

$$t(max) = \frac{\ln (2rc/RC)}{(2/RC) - (1/rc)} \qquad \text{(Reference 2)}$$

Instantaneous bridgewire power delivered by the EDIM capacitive discharge firing circuit can be expressed as:

$$P_i = I_0^2 R_S \text{ (Eff.)} \, e^{-2t/RC} \quad ; \text{ Instantaneous Bridgewire Power}$$

$$= \left(\frac{V_0 - V_T}{R_T} \right)^2 R_S \text{ (Eff)} \, e^{-2t/RC}$$

where:

V_0 = Voltage on Firing Capacitors at t = 4.0 (used herein)
V_T = SCR Forward Voltage Drop In Conduction State
R_T = Total Resistance of Firing Circuit Squib & Conductor
R_S (Eff) = Effective Resistance of Squib (See Reference 3)
t = Elapsed Time After SCR Triggered "ON"
RC = Firing Circuit Electrical Time Constant ($R_T C$)

The value of R_S (Eff.) used in the analysis was $1.3R_0$ (see Reference 3) where R_0 is the maximum cold resistance of the bridgewire. This value of effective bridgewire resistance accounts for the thermally induced increase in bridgewire resistance.

Integration of the instantaneous bridgewire power from t = 0 to t = t (max) gives an expression for the total energy available to increase bridgewire temperature. All energy delivered after t(max) is delivered at such a slow rate that the dissipation rate exceeds the input rate and the bridgewire cools. Therefore, the available squib initiation energy (E_A) is given by:

$$E_A = \int_o^{t(max.)} P_i dt = \left(\frac{V_o - V_T}{R_T}\right)^2 R_S\,(eff.) \left(\frac{-R_T C}{2}\right)\left(e^{-2t\,(max.)/RC} - 1\right)$$

V_0 can be found by adjustment of the initial capacitor voltage value (V_I = 28.3) for the voltage decrease due to leakage current through CR1 (in "off" state) and CR2.

V_0 = 30V - V (CR4) - I_{SB} R(R1) - ΔV; I_{SB} = EBIM Standby Current to Z1

V_0 = 28.3 - Δ V; Δ V = Voltage change due to leakage current

Q_i (Initial Capacitor Charge) = 28.3 (366×10^{-6}) = 10.36 millicoulombs (mc)

$I_L = I_L$ (CR1) + I_L (CR2); leakage current

= 8 μa + 1 μa

= 9 μa

Q = (9 μa)(5.5 seconds)

= .05 millicoulombs

$$V = \frac{Q}{C} = \frac{.05 \times 10^{-3}}{366 \times 10^{-6}} = 0.1366 \text{ volts}$$

V_0 = 28.3 - 0.1366

= 28.16V

rc = 3.14 ms (3σ minimum) Reference 1

$R_T = R_S$ (Eff.) + R_L

= R_S (Eff.) = 1.3 R_S (Effective Bridgewire Resistance Due to Thermal Effects, Reference 3)

R_T = 1.3 (1.15) + 0.25

= 1.745 Ω

$R_T C = (1.745)(366 \times 10^{-6})$

$= 0.6387$ ms

$$t(max) = \frac{\ln (2 \times 3.14 \times 10^{-3}/0.6387 \times 10^{-3})}{(2/0.6387 \times 10^{-3}) - (1/3.14 \times 10^{-3})} = \frac{\ln(9.8325)}{3131 - 318.5} = \frac{2.28569}{2813}$$

$= 0.813$ ms

$$E_A = \left(\frac{28.16 - 2.0}{1.745}\right)^2 1.495\left(\frac{1.745 \times 366 \times 10^{-6}}{2}\right)\left[e^{-(2 \times .813 \times 10^{-3}/.6387 \times 10^{-3})} - 1\right]$$

$$= (224.74)(1.495)(-3.1934 \times 10^{-4})(e^{-2.5458} - 1)$$

$$= -0.1073\ (.0784 - 1) = 0.1073\ (.9216)$$

$= 0.09889 = 98.89$ millijoules

Examination of the expression for E_A reveals the following:

a) 107.3 millijoules is total discharged energy at $t = \infty$

b) 0.9216 is the fraction of dischargeable energy available for ignition during t(max)

c) .0784 is the fraction of dischargeable energy left in firing capacitors at t(max).

During the time t(max) some of the energy delivered to the bridgewire is dissipated as heat losses away from the bridgewire. The fraction representing heat losses is approximately: $(1 - e^{-t/rc})$. See Reference 2.

At $t = t(max)$: $(1 - e^{-t/rc}) = 1 - e^{-.813/3.14} = 1 - e^{-0.25892}$

$= 1 - 0.77188$

Heat Fraction Loss $= 0.22812$

Summarizing the distribution of total energy:

a) $e^{-t/rc} - e^{-2t/RC} = 0.77188 - 0.07838 = 0.6935$ Fraction Heating B.W.
b) $1 - e^{-t/rc} = 1.0 - 0.77188 = 0.2281$ Heat Loss Fraction
c) $e^{-2t/RC} = 0.0784$ Fraction Left in Capacitor

1.0000

0.6935 (107.3 mj) = 74.41 mj = Energy Used in Heating BW (E_U)
0.0784 (107.3 mj) = 8.41 mj = Energy Left in Capacitor
0.2281 (107.3 mj) = 24.48 mj = Heat Loss at t(max)

74.41 + 24.48 = 98.89 Total Energy Delivered to BW at t(max).

Reference 3 gives 34.2 mj as the energy required to fire a SBASI. This quantity represents the total energy delivered at the initiation time of .070 milliseconds (ms). Calculations similar to those above indicate conservatively that at .070 ms the heat loss factor for the Reference 3 SBASI is 0.0102. This means that 1.35 mj was dissipated as heat losses. Therefore the characteristic SBASI firing energy (E_C) is (34.2 - 1.35 = 32.85 mj).

Using the values for E_U and E_C previously found the applicable "Safety Factor" (F_S) can be calculated:

$$F_S = \frac{E_U - E_C}{E_C} = \frac{74.41 - 32.85}{32.85} = 126\%$$

The EDIM firing circuit design margin at worst case conditions is 126% (or $E_U = 2.26\ E_C$). This safety factor was calculated using the actual energy E_U used in heating the SBASI bridgewire during the elapsed time t(max) and the SBASI characteristic ignition energy (E_C) determined from Reference 3 data.

Reference 3 gives a firing time of .070 milliseconds. The approximate SBASI firing time for the EDIM firing circuit at worst case conditions can be determined by calculating the time necessary to deliver 32.85 millijoules to the worst case SBASI bridgewire.

$$t_f = \frac{-RC}{2} \ln\left(\frac{E}{-K} + 1\right); \quad K = .1073 \text{ (From } E_A \text{ Calculation)}$$

$$= \frac{0.6387}{2} \ln\left(\frac{32.85 \times 10^{-3}}{-.1073} + 1\right)$$

$$= -0.31935 \ln (-0.30615 + 1)$$
$$= -0.31935 \ln (+0.6938)$$
$$= -0.31935 (-0.365)$$
$$= 0.117 \text{ milliseconds}$$

This approximation can be improved by determining what amount of energy is heat loss at 0.117 milliseconds then adjusting the value of E to compensate for this loss and then recalculating (t_f) using the adjusted energy value. By repeating this process for several iterations the approximation of t_f can be improved as much as desired. Two additional iterations yield t_f (1) = .123 ms and t_f (2) = .128 ms. The value t_f = 0.128 milliseconds is a good approximation for the worst case time required for the EDIM firing circuit to initiate a SBASI. Therefore, at worst case conditions the EDIM requires 0.128 milliseconds to deliver 32.85 millijoules of bridgewire heat and has the capability of delivering 74.41 millijoules of bridgewire heat within 0.813 milliseconds ($\bar{t}$ max).

The assumptions made throughout the EDIM firing circuit analysis are considered conservative. The SBASI sample size employed by Reference 3 is small but the SBASI firing energy (34.2 millijoules) characteristic given by this reference is corroborated by Reference 1 which gives approximately the same value. The analysis herein also deals with the problem of SBASI variance by employing a conservative (-3 sigma) SBASI thermal time constant (based on Reference 1 data) in the calculations. The employment of a small thermal time constant results in simulation of maximum SBASI thermal losses in the calculations. The conservative assumptions employed in the firing circuit analysis and the resulting 126% performance safety factor combine to generate a high level of confidence in the EDIM firing circuit design.

3.1.2 Timing and SCR Trigger Circuit Analyses

Figure 3.1.2-1 presents a schematic of the EDIM Timing and Trigger Circuit. This is the part of the EDIM which times the 3.0 second delay period and supplies a gate trigger pulse to the SCR thereby gating the SCR into the conduction state. The RC time constant is determined by R3, R4 and C1. The delay time (t_d) is determined by the RC time constant and the UJT peak point emitter voltage (V_P). Capacitor C1 charges to the voltage value V_P at which time the UJT Q1 turns on and transfers energy from C1 into the SCR gate circuit.

3.1.2.1 Timing Circuit Analysis

This section presents the results of an analysis performed to verify that the timing circuit will provide a time delay of 3.0 seconds minimum at worst case conditions. Figure 3.1.2-2 depicts 3rd/4th stage separation distance as a function of time. The minimum acceptable separation at the time of 4th Stage Ignition is 50 inches. This distance is required to assure that no significant 4th stage motor exhaust deflection occurs off of the 3rd stage in such a way so as to induce excessive coning of the 4th stage. As indicated by Figure 3.1.2-2, the minimum acceptable separation distance is achieved at 3.0 seconds (worst case, without "retro"). A design requirement for the EDIM is to assure that a minimum delay time of 3.0 seconds is achieved under all conditions.

Integration of the expression for instantaneous timing capacitor voltage (V_c) at C1 between the limits 0 and t results in an equation which can be solved for t_d.

$$t_d = -RC \ln \left(\frac{V_r - V_c}{V_r} \right)$$

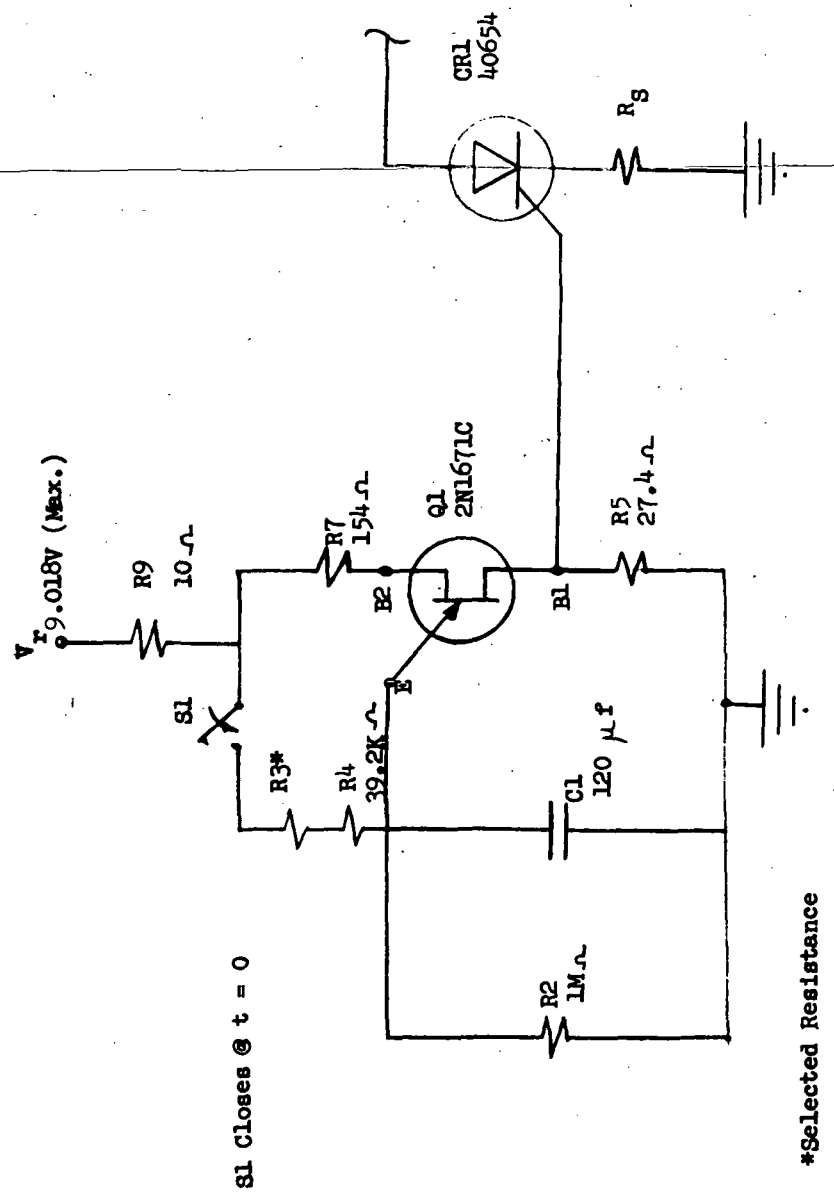


FIGURE 3.1.2-1
TIMING AND SCR TRIGGER CIRCUIT

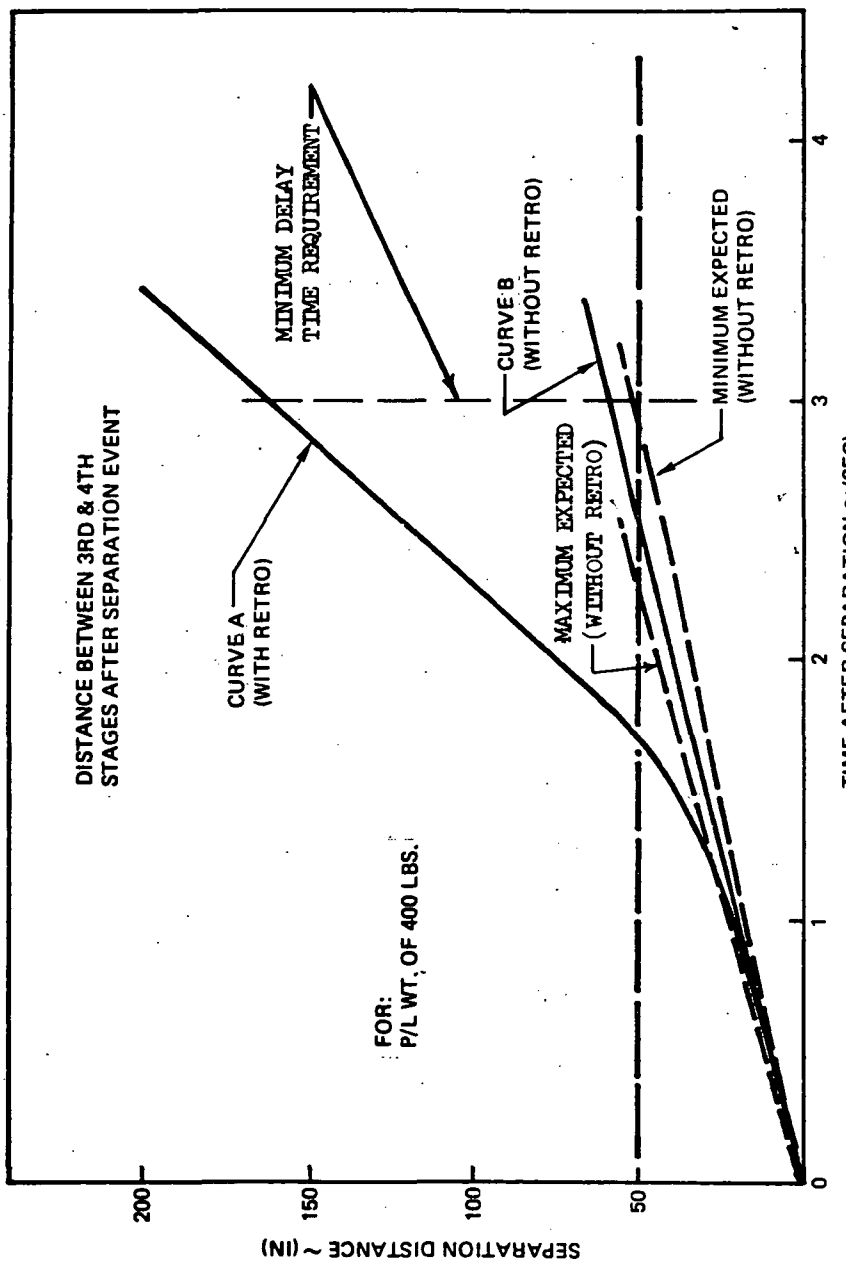


FIGURE 3.1.2-2 RECOMMENDED LOWER BOUND SEPARATION LIMIT

The delay time is defined as the time required for the C1 voltage (V_C) to reach the Q1 peak point emitter voltage (V_P) therefore:

$$t_d = -RC \ln \left(\frac{V_r - V_P}{V_r} \right)$$

$$V_P = \eta V_{BB} + \frac{200}{T_J}$$

where: η = UJT Intrinsic Standoff Ratio

V_{BB} = UJT Interbase Voltage

T_J = UJT Junction Temperature (^oK)

V_P = UJT Peak Point Emitter Voltage

$V_{BB} = 200/T_J$ = UJT Emitter Diode Junction Voltage

V_r = Regulated Voltage

The design requirement for the EDIM time delay is 3.0 seconds minimum. No deviation below 3.0 seconds is allowable in order to assure at least a 50 inch 3rd/4th stage minimum separation distance at 4th stage ignition as depicted in Figure 3.1.2-2.

The worst case deviation of the time delay value will occur during low temperature operation of the circuit. The primary (most significant) cause of the delay time deviation at high or low temperature is the change in the capacitance of C1 at these temperatures. Temperatures above 25°C cause C1's capacitance to increase above the nominal value and a decrease in capacitance will result when the temperature is below 25°C. The decreased capacitance at low temperature is the most critical parameter variation since it will cause a corresponding decrease in the delay time.

The selection of R3 during EDIM buildup will fix the circuitry delay time for an ambient temperature of approximately 25°C. This selection of an R3 resistance value must take into account the maximum possible excursion of the delay time due to worst case circuit parameters and temperature extremes.

The UJT parameters which change with temperature and will cause the value of V_P (and therefore t_d) to change are the interbase resistance (R_{BBO}) and the UJT emitter diode junction voltage (V_{ED}). The intrinsic stand-off ratio (η) remains essentially constant with temperature. The temperature coefficient of output voltage (T_{CV}) for the IC regulator Z1 will also affect the resultant value of V_P at the temperature extremes. The effects of the temperature induced changes in R_{BBO} and V_{ED} are in opposite directions in terms of the resultant change in V_P. However, the magnitudes of the influence of R_{BBO} and V_{ED} on V_P are not equal and the resultant effect is that V_P is more sensitive to changes in V_{ED} except at minimum R_{BBO}.

The most severe changes in delay time will occur as a result of the temperature induced capacitance change in C1. The nominal capacitance value is 120 microfarads at 25°C. This value will increase to 139 microfarads at 80°C and decrease to 102 microfarads at -17.8°C.

Calculations were performed to investigate the magnitude of the changes in delay time resulting from the temperature extremes to be imposed. To perform these calculations the full range of UJT parameter variations and regulator (Z1) temperature effects were considered. The results of the calculations are presented in Table 3.1.2.1-I, a table of temperature induced t_d changes. A value for R3 (which resulted in a 3.0 second t_d value) was selected for each of the possible worst case UJT parameter sets at 25°C. Then, the t_d value resulting from high and low temperature effects was calculated for each of the UJT parameter sets (with R3 constant) thereby generating the maximum t_d changes (Δt_d's) for each of these sets. The Δt_d values due to temperature induced changes in peak point voltage (ΔV_p) and C1 capacitance changes (ΔC), each acting alone, were also calculated and listed in the table. The $\Delta_T t_d$ column represents total resultant t_d change with ΔV_p and ΔC acting together.

TABLE 3.1.2.1-I

Temperature Induced t_d Changes

T (°C)	η	R_{BBO} (KΩ)	R3 (KΩ)	C (μf)	t_d (Sec.)	Δt_d (Δ C) (Sec.)	Δt_d (ΔV_p) (Sec.)	Total Δt_d (Sec.)
25	0.47	4.7	33.48	120	3.0	---	---	---
	0.47	9.1	32.65			---	---	---
	0.62	4.7	22.17			---	---	---
25	0.62	9.1	21.83	120	3.0	---	---	---
-17.8	0.47	3.29	33.48	102	2.59	-.46	+.05	-.41
	0.47	6.37	32.65		2.61	-.47	+.08	-.39
	0.62	3.29	22.17		2.53	-.45	-.02	-.47
-17.8	0.62	6.37	21.83	102	2.60	-.46	+.06	-.40
80	0.47	7.05	33.48	139	3.42	+.47	-.05	+.42
	0.47	13.83	32.65		3.38	+.45	-.07	+.38
	0.62	7.05	22.17		3.55	+.48	+.07	+.55
80	0.62	13.83	21.83	139	3.40	+.46	-.06	+.40

These data show that the Δt_d values resulting from capacitahce change alone are 0.48 volts maximum and for ΔV_P alone, 0.08 volts maximum. These deltas partially compensate for one another except at η (maximum) and R_{BBO} (minimum). A conclusion drawn from these data is that the value of R3 should be selected such that the time delay is high enough at 25°C to compensate for the worst case decrease expected at -17.8°C. The worst case decrease indicated in the Δt_d data is -0.47 seconds. Fixing the delay time at a nominal value of 3.6 seconds at 25°C will assure that the minimum delay time is no less than 3.1 seconds at -17.8°C.

In conclusion it has been determined that the UJT timing circuit will meet the EDIM design requirement for achieving a minimum 3.0 second delay time. However, to do so, the nominal t_d setting (by R3 selection) should approximately be 3.6 seconds at 25°C in order to assure compliance with the 3.0 seconds minimum delay time at worst case low temperature conditions. As a consequence of this approach the maximum delay time at 80°C could be as great as approximately 4.08 seconds. The calculated delay time extremes were predicted for the temperature extremes to be imposed during environmental testing. These extremes are more severe than expected in actual flight. Actual flight temperatures are expected to result in a much smaller spread of possible t_d values.

3.1.2.2 SCR Trigger Circuit Analysis

This section presents the results of a reliability analysis of the SCR trigger circuit. The analysis was performed to examine functional performance adequacy of the UJT trigger circuit under worst case conditions. The sole functional requirement of the SCR trigger circuit is to generate the necessary SCR gate voltage and current required to reliably fire the SCR at the end of the timing circuit delay.

It was determined during the analysis that the circuit configuration as it exists for the preliminary Engineering Model design cannot be assured of firing the SCR at worst case conditions. Under the conditions of a worst case state of the circuit component parameters at low temperature (-17.8°C) the maximum UJT emitter saturation voltage V_E (SAT) will exceed the value consistent with SCR triggering. The following SCR parameter values represent the worst case SCR firing requirements.

I_{GT} = 21 ma (Max. @ -20°C)

V_{GT} = 1.78V (Max. @ -20°C)

where:

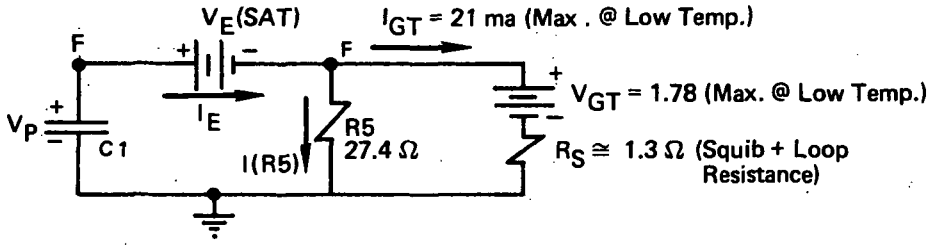
I_{GT} is the SCR DC gate trigger current (per Data Sheet)

V_{GT} is the SCR DC gate trigger voltage (per Data Sheet)

Figure 3.1.2-1 presents the SCR trigger circuit configuration applicable to the Engineering Model. The voltage at point E (V_E) will reach a maximum value equal to the UJT peak point emitter voltage (V_P) at 3.0 seconds after the switch S1 closes (at 3rd/4th Stage separation). At $V_E = V_P$ the UJT is turned "on" and the energy stored in C1 is applied to the SCR gate trigger circuit through the UJT base B1. At the "turn-on" point the trigger circuit must achieve the necessary SCR triggering conditions or the SCR will not become conductive and the squib cannot be fired. At worst case conditions the UJT (2N1671C)

V_E (SAT) can be as high as 5 volts at an emitter current of 50 milliamperes. At the worst case maximum value of V_{GT} the current through R5 will be 65 milliamperes (1.78/27.4). This current plus the current through the SCR gate (I_{GT}) will result in a current value considerably greater than the 50 milliamperes value of I_E given by the UJT data sheet at V_E (SAT) = 5.0V (Max.).

The following is a simplified equivalent circuit relating the pertinent component and circuit parameters involved in the SCR triggering problem.



The range of V_P values will be between 4.8 and 6 volts. The values of V_{GT} are likely to include cases wherein V_F is too small (less than V_{GT}) since $V_E = V_P$, $V_F = V_P - V_E$ (SAT), and since V_E (SAT) can have values as great as 5 volts. The following equations describe the SCR triggering problem mathematically.

$$I_{GT} = \frac{V_F - V_{GT}}{R_S} = .21 \text{ ma (Max., Reference SCR Data Sheet)}$$

V_{GT} = 1.78V (Max., Reference SCR Data Sheet)

$$\frac{V_F - 1.78}{1.3} = .021 \text{ a}$$

$$V_F = .0273 + 1.78$$

$$\cong 1.81\text{v}$$

$$I_E = .021\text{a} + \frac{1.81}{27.4}$$

$$= .021\text{a} + .066$$

$$= 87 \text{ ma}$$

$V_F = V_P - V_E$ (SAT) = 1.81V (Max.)

V_E (SAT) = $V_P - V_F$; $4.8V \leq V_P \leq 6.0V$ holds for EDIM design

V_E (SAT) = 4.8 - 1.81 = 2.99 (Max. Allowable)

The UJT emitter saturation voltage must not exceed 2.99V at -17.8°C in order to assure that the SCR can be triggered with worst case SCR parameters at this temperature.

In summary, the SCR trigger circuit will not successfully trigger the RCA Type 40654 SCR under all the possible conditions of temperature and at the worst case state for the SCR and UJT Type 2N1671C parameters. The range of possible values for the UJT emitter saturation voltage, SCR (V_{GT}) and SCR (I_{GT}) is such that the SCR triggering state will not be achieved even at some points somewhat less than worst case. The EDIM circuit design, component selection and/or the regulated voltage setting will require changes for the Qualification Unit in order to correct for the UJT/SCR compatibility problem discussed herein. It will be possible to work around the problem in the Engineering Unit EDIM by means of selecting a UJT for acceptable V_E (SAT) before installation.

3.1.3 Energy Budget Analysis

Battery power is applied to the EDIM until fourth stage spin-up occurs. At spin-up the battery power disconnects and EDIM operation is powered by means of the energy stored in five energy "source" capacitors C3 through C7 (Referred to herein as C_S). These capacitors supply a total nominal capacitance (C_S) of 1500 microfarads (300 μf each at 25°C) charged to 28.3 volts minimum at the beginning of the 4.5 second internal power operating period. This 4.5 second period includes a 1.5 second operating

period (during 4th stage spin-up) prior to closure of the start switch (at 4th stage separation) and a 3.0 second (minimum) programmed ignition delay. During the 4.5 second (minimum) of internal power operation the voltage on C_S drops from the initial value of 28.3 volts to some final value which depends on the amount of power required by the EDIM during the 4.5 second internal power operating period. This section presents the results of an analysis performed to investigate the adequacy of the EDIM circuit to perform normally at worst case conditions using the energy available in C_S for the full 4.5 seconds.

The energy budget analysis for the EDIM circuitry at worst case conditions indicates that the source capacitance C_S will not supply the worst case EDIM energy demand for 4.5 seconds at -17.8°C. The EDIM energy budget was divided into three elements for convenience. These elements are the following:

*1. Capacitor C1 Circuit - This circuit requires sufficient energy to charge C1 to the UJT Peak Point Emitter Voltage (V_p). Also, some energy is lost through R2 during C1 charging.

2. UJT Drain Circuit - This is the series circuit through the UJT which draws current throughout the internal power period so as to maintain a V_p bias.

3. Regulator Standby Current - The current required for regulator internal requirements and bias is equal to the regulator standby current. This current must be maintained throughout the internal power period.

*This applies only during the 3.0 second delay period.

Additional leakage currents due to the capacitors were not significant.

The following calculations were performed for the development of an energy budget for each of the five elements listed above.

Usable Charge Calculation (Available Energy on C_S)

Vin (Min.) = 28.3V Minimum Initial Voltage at C_S (30V - 0.7 - 1.0)

C_S (Min.) = 1500 - 0.1 (1500) = 1350 μf @ 25°C

C_S (Min. @ -17.8°C) = 1350 - 1350 (.0075)(42.8°C) = 917 μf

V_d (Min.) = 3.0V Minimum Input/Output Voltage Differential for Z1 Voltage Regulator

V_{OUT}(Min.) = 8.942V Regulated Voltage at -17.8°C

$V_f = V_{OUT}$(Min.) + V_d (Min.) = 8.942 + 3.0 = 11.942, Lowest Voltage permitted at C_S for normal regulator operation

$Q_f = C_S V_f = (917 \times 10^{-6})(11.942) = 10.95$ millicoulomb (mc), Residual charge on C_S at V_f @ -17.8°C

$Q_I = (917 \times 10^{-6})(28.3) = 25.95$ mc, Initial Charge on C_S at t = 0, T = -17.8°C

$Q_u = 25.95 - 10.95 = 15.00$ mc, Usable Charge on C_S for normal operation of EDIM during 4.5 second internal power operating time.

1) Capacitor C1 Circuit

a) C1 Charge

V_P (Max.) = 6.0V

C1 = 102 μf @ -17.8°C

$Q(C1) = 6.0 (102 \times 10^{-6})$

= 0.612 mc

b) R1 Drain

V(R1) = 4.0V (average for 3.0 second)

$I(R1) = 4.0/1 \times 10^{6} = 4 \mu a$

$Q(R1\ drain) = (3.0)(4.0 \times 10^{-6})$

= .012 mc

Q(1) = 0.612 +.012

= 0.624 mc

2) UJT Drain Circuit

R_{BBO} (Min) = 0.7 (4.7K) Ω

= 3.29K @ -17.8°C

R (9 + 7 + 5) = 10 + 154 + 27.4

= 0.191K

R_T = 3.29K + 0.191K

= 3.481K Ω

I (2) = 8.942/3.481K

= 2.57 ma

Q (2) = (2.57 ma)(4.5 sec)

= 11.57 mc

3) Regulator Standby Current

$I(ZI.)_{SB}$ = 3.5 ma (Max.)

Q (4) = 4.5 (3.5 ma)

= 15.75 mc

Q(T) = Q(1) + Q(2) + Q(3)

= 0.624 + 11.57 + 15.75

= 27.94 mc

Deficiency = Q(T) = Q(U)

= 27.94 - 15.00

= 12.94 mc

The above calculations show a 12.94 mc deficiency in the available charge in C_S for normal operation for 3.0 seconds delay. The charge deficiency can be solved by some combination of several possible actions

to decrease the energy demand during EDIM operation and/or increase the usable charge. A listing of possible steps is given below.

(a) Increase the value of C_S to a value which will store the total charge required for the worst case state at -17.8°C.

(b) Screen components to assure parameter values less than worst case. Candidate components and parameters for screening are indicated below.

1. UJT - Screen for R_{BBO} higher than worst case minimum.
2. C_S (C_3, C_4, C_5, C_6, C_7) - Screen for high side tolerance capacitance.
3. Z1 Regulator - Screen for typical (2.3 ma) or lower value for Standby Drain Current. Screen for 1.5V minimum input-output voltage differential.

(c) Relief of EDIM requirements at low temperature.

(d) Change component type(s) to those which have a more favorable range of the critical parameter(s). This would be an alternative to screening of the existing component types.

It should be noted that the probable failure mode for the EDIM in the event of insufficient energy in C_S is a short delay time. This short delay time would occur as a result of a decreased regulated voltage when the C_S voltage dropped below about 12 volts. At this point the regulated voltage would continue to drop below the nominal 9.0 volts at about the same rate as the voltage on C_S dropped. At some point in time the decreasing UJT peak point voltage (V_P) and the timing capacitor voltage would reach a cross-over point thereby turning the UJT "on". The SCR would then fire normally unless the timing capacitor voltage was too low. The failure to fire the SCR (and therefore the SBASI) would be an extreme case resulting when the energy

in C_S was far short of the amount required to operate the EDIM. The short delay time condition and SCR firing energy margin should be investigated during the Engineering Model Testing in order to gain insight into the phenomena. The delay time effects are at least partially self-compensating and the minimum SCR firing energy condition may be simulated by applying low initial voltage to C_S.

3.2 Component Analysis

3.2.1 Component Descriptions

This section presents a description of the electronic piece-part components which compose the EDIM. The following is a listing and description of the parts used.

1. Integrated Circuit; Fairchild μa 723 P/N U5R7723312
   Regulator Z1 Monolithic, Planar, epitaxial-10 Lead Metal Can
2. Transistor, Silicon, Unijunction; Q1 GE Type 2N1671C
   TO-5 Can, 3 Lead
3. Zener Diode, V_Z = 30, 1%; CR2 and CR3
   General Semiconductor - GZ41101A (Type 1N5256B)
4. Diode, Rectifier, Silicon; CR4 and CR5 PIV = 50V, I_O = 1.0 amp
   Peak Surge = 30.0 amp
5. Resistor, RNR55C; R3, R4, R6, R8, R10, R11 & R12
   Metal Film, 1%, 1/10 watt, MIL-R-55182
6. Resistor RNR65C; R1 Metal Film, 1%, $\frac{1}{4}$ watt, MIL-R-55182
7. Resistor, RWR81S1540FR; R7 Wirewound, Dale, MIL-R-39007,1.0 watt, 1%
8. Resistor RWR81S27R4FR; R5 Wirewound, Dale, MIL-R-39007,1.0 watt, 1%
9. Resistor, MFF1/8 1 MEG 1% T-0; R2
   Wirewound, Dale, MIL-R-22684B; 1/8 watt, 1%

10. Resistor, RWR81S10ROFR; R9
    Wirewound, Dale, MIL-R-39007, 1/10 watt, 1%
11. Capacitor, GE Type No. 69F4236G137; C1
    Hermetically Sealed, Tabular, Tantalum
    Wet Slug Capacitor, M39006/09-6476
    120 μf, 15V
12. Capacitor, Fixed, Ceramic Dielectric; C2
    General Purpose, M39014/05-2819, 100 pf
13. Capacitor, GE Type No. 69F4455G136; C3, C4, C5, C6, C7, C8, C9
    Hermetically Sealed, Tabular Tantalum
    Wet-Slug Capacitor, M39006/09-6518
    300 μf, 30V
14. Connector, Shell Size 12, 10 Sockets
    Deutsch DBA54-12-10 SN
15. Connector, Shell Size 10, 19 Pins
    Deutsch RTK 07-18-19 PN

The GIDEP ALERTS at VSD have been reviewed to determine if any of the above components are on "alert" status. It was determined that only the RNR55C (Item 5 above) and the RNR65C (Item 6 above) resistors were the subjects of an ALERT at this time. The alert in question was ALERT No. MSFC 74-02. dated 14 August 1974. This alert specifically dealt with all RNR/RNC55, 60, 65, 70 resistors manufactured by Wagner Electric Corporation, VAMISTOR Division, Livingston, N.J. All applicable resistors used in the EDIS should be obtained either from another manufacturer or from later lot/date codes of Wagner Electric Corporation manufacturer which have been corrected for the problem referred to in ALERT No. MSFC 74-02.

3.2.2. Stress Analysis

This section presents the results of a piecepart component electrical stress analysis which was performed for each of the EDIM circuit components. The purpose of the analysis was to determine the level of electrical and/or thermal stress imposed on the components by the EDIM functional and environmental requirements. The stress levels thus determined were evaluated in terms of the maximum specified allowables determined from component data sheets. Results of the analysis are summarized in the following sections herein. The stress levels determined were found to be adequate to assure reliable operation of the EDIM under the worst case extremes of environment and electrical stress combinations.

3.2.2.1 Resistor Stress Levels

Maximum ratings and the EDIM imposed stress levels for each of the resistors R1 through R12 are presented in Table 3.2.2-I. All of the resistors were found to be adequately derated to assure reliable operation of the circuit. The stress values presented represent the percent of maximum specified power actually dissipated during the worst case conditions of circuit operation.

Only one resistor (R1) was found to be stressed at a significant percentage of the allowable dissipation. This resistor is exposed to two significant stress conditions during EDIM operation. The first stress condition arises as a consequence of a transient current surge which occurs during initial charging of capacitors C3 through C9 when battery power is first applied to the EDIM circuit. This transient surge current occurs during a period of 1.22 seconds during which an average stress level of 86.2% is applied resulting in approximately a 10°C temperature rise. The 86.2% stress level of 862 milliwatts for 1.22 seconds compares

TABLE 3.2.2-I

EDIS RESISTOR STRESS LEVELS

Reference Designator	Component Rating P(Max.) (mw)	Component Rating T(Max.) (°C)	Stress Levels Imposed P(Max.) (mw)	Stress Levels Imposed T(Max.) (°C)	Stress (%)
R1	250	175	85	97	34
R1 (Transient)	1000 (3600 sec overload)	175	862 (1.22 sec)	90	86.2
R2	125	175	.0763	80	.06
R3	100	175	.0387	80	.0387
R4	100	175	2.26	81.1	2.26
R5	1000	275	.0898	80	.00898
R6	100	175	7.2	84	7.2
R7	1000	275	.505	80	.0505
R8	100	175	1.883	81	1.883
R9	1000	175	1	80	.1
R10	100	175	1	80	1
R11	100	75	1	80	1
R12	100	175	1	80	1

favorably with the specified maximum (1000 milliwatts for 3600 seconds) overload condition.

3.2.2.2 Capacitor Stress Levels

Table 3.2.2-II presents the maximum ratings and worst case stress levels imposed on the EDIM capacitors. The stress factor presented is the maximum percentage of the rated voltage imposed on the capacitors during worst case circuit operation conditions.

All capacitors were found to be operated within their maximum rated voltage at the corresponding maximum temperatures. Capacitors C1 and C2 are operated well within the voltage limits specified at maximum temperature. The voltage applied to capacitors C3 through C9 at worst case zener (CR2 and CR3) conditions (high side of tolerance and 80°C) is 32.2 volts. This value is within the maximum specified DC surge voltage of 34.5 volts at 85°C. The maximum DC surge voltage rating is defined as the maximum DC voltage applied for 30 seconds or less at intervals of 5 minutes or more. These conditions are compatible with the EDIM flight conditions and should also be observed during ground testing of the EDIM for maximum reliability of these capacitors. The worst case stress state (32.2 volts, 80°C) can only occur during environmental testing and no operational problems are expected (See Table 3.2.2-II Note).

3.2.2.3 Semiconductor Stress Levels

The worst case stress level for each of the EDIM semiconductors is presented in Table 3.2.2-III. These stress levels were determined for each of the semiconductor components under the worst case combination of circuit imposed conditions and component parameter values. All of these components were determined to be well within the desirable range of stress consistent with good derating practices.

TABLE 3.2.2-II

EDIM CAPACITOR STRESS LEVELS

Reference Designator	Component Rating V_{DC} (Surge) (volts)	Component Rating T(Max.) (°C)	Worst Case Stress Levels Imposed V_{DC}(Surge) (volts)	Worst Case Stress Levels Imposed T(Max.) (°C)	Worst Case Stress Levels Imposed Stress Factor
C1	17.2	85°C	6.0V	80°C	34.9%
C2	100	175	30V	80°C	30%
C3	34.5	85°C	32.2	80°C	93%*
C9	34.5	85°C	32.2	80°C	93%*

*NOTE:

1. This stress condition cannot occur during the expected flight environment.
2. These capacitors are lot sample tested to assure a minimum of 10,000 hr. life at 85°C.
3. 100% of those capacitors will be inspected for low capacitance and leakage at VSD.

TABLE 3.2.2-III

EDIM SEMICONDUCTOR STRESS LEVELS

A. Diodes, General Purpose, 1N4001

	Ratings		Applied Stress Values		
	I_F(Max.)	PIV	I_F(Max.)	PIV	Stress (I_F)
CR4	1000 ma	50	137 ma	20V	13.7%
CR5	1000 ma	50	137 ma	0V	13.7%

B. Zeners, QZ4110lA, V_Z = 30V, 1%

	Max. Rated Junction Temperature (T_J)	Worst Case Applied T_J	Worst Case Stress (T_n)*	Stress Factor %
CR2	200°C	149.5°C	0.596	59.6%
CR3	200°C	149.5°C	0.596	59.6%

*T_n = Normalized Junction Temperature (derating starts at 75°C)

C. UJT (Q1) 2N1671C

P_{max} (RATED) = 235 mw @ 80°C

P_{max} (APPLIED)= 16 mw

Stress = 16/235 = 6.8% (Max.)

D. SCR (CR1) 40654

Maximum Ratings

V_{DSOM} (Non-Repetitive Peak Forward Voltage) = 250V

I_{TSM} (Peak Surge) = 80A

P_{GM}(Peak Forward Gate Dissipation, for 1 sec) = 40w

Operating Case Temperature Range = 65°C to 100°C

Maximum Applied Stress

V_{DSOM} = 30.8V

I_{TSM} = 30.8A Stress = 30.8/80 = 38.5%

P_{GM} = 4.0w Stress = 4.0/40 = 10%

T(Max.) = 80°C

In Table 3.2.2-III zener diodes CR2 and CR3 are indicated as having the highest level of stress (59.6%) of all the semiconductors. This stress level is expressed in the form of the normalized junction temperature (T_n) which is calculated by use of the following expression.

$$T_n = \frac{T_J - T_S}{T_J(Max) - T_S}$$ (Reference No. 6)

where:

T_n = Normalized Junction Temperature

T_J = Junction Temperature

T_S = Temperature at Which Power Derating Begins ($75^{\circ}C$)

$T_J(Max)$ = Maximum Rated Junction Temperature Determined from Device Specification

3.3 Failure Mode, Effects and Criticality Analysis

Failure modes and effects can be analyzed and presented qualitatively, without numerical parameters. However, a quantitative criticality is useful as an aid in proportioning effort and establishing priorities for such effort to be expended in reliability improvement. Quantitative criticality is expressed herein in terms of a rate of occurrence of mission failures per million flights. Each criticality value presented in Table 3.3-I is that value attributable to the failure of the corresponding component in the designated failure mode. Mathematically, criticality is defined by the following relation:

Criticality = $Wt \times \lambda_G \times K \times$ (Effect Level)

where: Wt = Environmental Exposure ("Use") Factor

λ_G = Generic Failure Rate

K = Operational History Modifier

Effect Level = Mission Failure Probability Given a Particular Failure Mode

To arrive at the criticality value for a specific component failure mode, the component failure rate (λ_G) attributable to that mode is required.

TABLE 3-3-I

COMPONENT: EDIM
DRAWING NO:
VENDOR:

SINGLE FAILURE MODE CRITICALITY ANALYSIS

SYSTEM Scout
SUBSYSTEM 4th Stage EDIM

CODE NO.	ELEMENT	FAILURE MODE	EFFECT CATEGORY: FAILURE EFFECT a. SUBSYSTEM b. MISSION	EFFECT LEVEL	FAILURE RATING: GENERIC λ (x 10^{-6})	"USE" FACTOR Wt	OPERATIONAL HISTORY K	FAILURE RATING K Wt λ (x 10^{-6})	CRITICALITY (EFFECT LEVEL) x (FAILURE RATING)	REMARKS
Q1	Unijunction Transistor	Short	a) EDIS will not operate.							
			b) Mission Failure	1.0	0.205	99.85	1.0	20.47	20.47	
		Open	a) EDIS will not operate.							
			b) Mission Failure	1.0	0.205	99.85	1.0	20.47	20.47	
Z1	Voltage Regulator (IC)	Regulation High	a) Long or short delay time possible depending on extent of the out-of-specification condition and resultant rate of excessive energy depletion during delay period.							
			b) Possible Degradation	.01	0.20	99.85	1.0	10.0	0.20	
		Regulation Low	a) Short Delay Time Probable							
			b) Probable Degradation	.05	0.10	99.85	1.0	10.0	0.5	
		Internal Short or Open	a) No Output							
			b) Mission Failure	1.0	0.20	99.85	1.0	20.0	1.0	
CR1	SCR	Short	a) Early or no squib firing.							
			b) Mission Failure	1.0	0.5	99.85	1.0	49.93	49.93	
		Open	a) No squib firing.							
			b) Mission Failure	1.0	0.5	99.85	1.0	49.93	49.93	
CR2 or CR3	Zener Diodes	Short (of either)	a) No energy to fire squib.							
			b) Mission Failure	0.0	0.300	99.85	1.0	29.96	29.96	
		Open (of either)	a) Excessive voltage on C3 C9							
			b) Possible Loss	0.1	0.625	99.85	1.0	62.41	6.241	
		Drift (of either) zener voltage change	a) Possible low energy for squib firing.							
			b) Possible Failure	0.1	0.325	99.85	1.0	32.45	3.25	

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TABLE 3-3-I

COMPONENT: EDIM
DRAWING NO:
VENDOR:

SINGLE FAILURE MODE CRITICALITY ANALYSIS

SYSTEM
SUBSYSTEM

CODE NO.	ELEMENT	FAILURE MODE	EFFECT CATEGORY: FAILURE EFFECT a. SUBSYSTEM b. MISSION	EFFECT LEVEL	FAILURE RATING: GENERIC λ (x 10⁻⁶)	"USE" FACTOR Wt	OPERATIONAL HISTORY K	FAILURE RATING K Wt λ (x 10⁻⁶)	CRITICALITY (EFFECT LEVEL) x (FAILURE RATING)	REMARKS
CR4 and CR5	Diode	Short (of CR5)	a) Loss of reverse voltage protection. b) Possible mission delay	0.0	0.205	99.85	1.0	20.47	0.0	
		Open (of either)	a) EDIS will not operate. b) Mission Failure	1.0	0.205	99.85	1.0	20.47	20.47	
		Short (of CR4)	a) Squib firing energy will be depleted during delay time. b) Mission Failure	1.0	0.205	99.85	1.0	20.47	20.47	
C1	Capacitor	Short	a) SCR will not fire. b) Mission Failure	1.0	0.192	99.85	1.0	19.17	19.17	
		Open (Capacitance Zero)	a) Delay time zero. b) Possible Failure	0.1	0.096	99.85	1.0	9.59	0.96	
		Drift	a) Long or short delay time. b) Possible Mission Degradation	0.01	0.096	99.85	1.0	9.59	0.096	
C2	Capacitor	Short	a) Regulator Failure b) Mission Failure							
		Open	a) No Significant Effect b) No Effect							
		Drift	a) No Significant Effect b) No Effect							

COMPONENT: EDIM
DRAWING NO:
VENDOR:

TABLE 3-3-I

SINGLE FAILURE MODE CRITICALITY ANALYSIS

SYSTEM
SUBSYSTEM

CODE NO.	ELEMENT	FAILURE MODE	EFFECT CATEGORY: FAILURE EFFECT (a. SUBSYSTEM b. MISSION)	EFFECT LEVEL	FAILURE RATING: GENERIC λ (x 10⁻⁶)	"USE" FACTOR Wt	OPERATIONAL HISTORY K	FAILURE RATING K Wt λ (x 10⁻⁶)	CRITICALITY (EFFECT LEVEL) x (FAILURE RATING)	REMARKS
C3 ↓ C7	Capacitors	Short (of any one)	a) EDIM will not operate. b) Mission Failure	1.0	0.192	99.85	1.0	19.17	19.17	
		Open (of any one)	a) Decreased operating energy during delay time causing short delay time. b) Possible Degraded Mission at low temperature.	0.01	0.096	99.85	1.0	9.95	0.10	
		Drift (of any one)	a) Possible decreased operating energy during delay period causing short delay time. b) Possible Degraded Mission	0.01	0.096	99.85	1.0	9.95	0.10	
C8 ↓ C9	Capacitors	Short (of either)	a) Squib cannot be fired. b) Mission Failure	1.0	0.192	99.85	1.0	19.17	19.17	
		Open (of either)	a) Possible no squib firing. b) Possible Failure	0.1	0.096	99.85	1.0	9.95	1.0	
		Drift (of either)	a) Possible no squib firing. b) Possible Failure	0.1	0.096	99.85	1.0	9.95	1.0	

TABLE 3-3-I

COMPONENT: EDIM
DRAWING NO:
VENDOR:

SINGLE FAILURE MODE CRITICALITY ANALYSIS

SYSTEM
SUBSYSTEM

CODE NO.	ELEMENT	FAILURE MODE	EFFECT CATEGORY		FAILURE RATING				CRITICALITY	REMARKS
			FAILURE EFFECT a. SUBSYSTEM b. MISSION	EFFECT LEVEL	GENERIC λ (x 10⁶)	"USE" FACTOR Wt	OPERATIONAL HISTORY K	FAILURE RATING K Wt λ (x 10⁶)	(EFFECT LEVEL) x (FAILURE RATING)	
R1	Resistor	Short	a) Zener diodes CR1 and CR2 cannot regulate voltage at C3 through C9 to 30V maximum. Zeners will be destroyed by excessive power dissipation.							
			b) Probable Loss	0.5	0.005	99.85	1.0	0.5	.025	
		Open	a) Loss of battery power.							
			b) Loss of Mission	1.0	.0038	99.85	1.0	0.379	0.379	
		Drift	a) Non-optimum zener action and possible zener burn-out due to over-current.							
			b) Possible Loss	0.1	.0004	99.85	1.0	0.40	.004	
R2	Resistor	Short	a) SCR cannot be fired.							
			b) Loss of Mission	1.0	.004	99.85	1.0	0.40	0.40	
		Open	a) Capacitor C1 cannot be bled to zero volts readily during testing. Could cause delay time changes during ground testing.							
			b) No effect during flight.	0.0	.032	99.85	1.0	3.20	0.0	
		Drift	a) Could result in excessive current short or long delay times depending on circumstances of failure.							
			b) Possible Failure	0.1	0.004	99.85	1.0	0.40	0.04	

TABLE 3-3-I

COMPONENT: EDIM
DRAWING NO: _____
VENDOR: _____

SINGLE FAILURE MODE CRITICALITY ANALYSIS

SYSTEM _____
SUBSYSTEM _____

CODE NO.	ELEMENT	FAILURE MODE	EFFECT CATEGORY		FAILURE RATING				CRITICALITY	REMARKS
			FAILURE EFFECT a. SUBSYSTEM b. MISSION	EFFECT LEVEL	GENERIC λ (x 10^6)	"USE" FACTOR Wt	OPERATIONAL HISTORY K	FAILURE RATING K Wt λ (x 10^6)	(EFFECT LEVEL) x (FAILURE RATING)	
R3	Resistor	Short	a) Will result in out-of-tolerance delay times.							
			b) Possible Degraded Mission	0.01	.0005	99.85	1.0	.05	.0005	
		Open	a) No SCR firing or squib initiation.							
			b) Mission Failure	1.0	.0038	99.85	1.0	.38	.38	
		Drift	a) Could result in short or long delay time depending on direction of drift.							
			b) Possible Degradation	0.01	.0005	99.85	1.0	.05	.0005	
R4	Resistor	Short	a) Very short delay time.							
			b) Possible Mission Degradation	0.01	.0005	99.85	1.0	.05	.0005	
		Open	a) No SCR or squib firing.							
			b) Mission Failure	1.0	.0038	99.85	1.0	.38	.38	
		Drift	a) Short or long delay time.							
			b) Possible Mission Degradation	0.01	.0005	99.85	1.0	.05	.0005	
R5	Resistor	Short	a) SCR will not fire.							
			b) Mission Failure	1.0	.004	99.85	1.0	0.40	0.40	
		Open	a) Possible premature SCR firing.							
			b) Possible Mission Failure	.1	.032	99.85	1.0	3.2	.32	
		Drift	a) No Effect							
			b) No Effect	0.0	.004	99.85	1.0	0.40	0.0	

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TABLE 3-3-I

COMPONENT: EDIM
DRAWING NO:
VENDOR:

SINGLE FAILURE MODE CRITICALITY ANALYSIS

SYSTEM
SUBSYSTEM

CODE NO.	ELEMENT	FAILURE MODE	EFFECT CATEGORY: FAILURE EFFECT (a. SUBSYSTEM b. MISSION)	EFFECT LEVEL	FAILURE RATING: GENERIC λ (x 10⁻⁶)	"USE" FACTOR Wt	OPERATIONAL HISTORY K	FAILURE RATING K Wt λ (x 10⁻⁶)	CRITICALITY (EFFECT LEVEL) x (FAILURE RATING)	REMARKS
R6	Resistor	Short	a) Regulator will fail. b) Mission Failure	1.0	.0005	99.85	1.0	.05	.05	
		Open	a) Regulator output will equal input minus three volts. Excessive power drain will occur in EDIM. b) Probable Mission Failure	0.5	.0038	99.85	1.0	0.38	0.19	
		Drift	a) Long or short delay time and possible SCR no fire. b) Possible Mission Failure	0.1	.0005	99.85	1.0	0.05	.005	
R7	Resistor	Short	a) Long delay time. b) Mission Degradation Probable	0.05	.004	99.85	1.0	0.40	.02	
		Open	a) Delay time will be zero. b) Possible Mission Failure	0.10	.032	99.85	1.0	3.20	.320	
		Drift	a) Long or short delay time. b) Possible Mission Degradation	0.01	.004	99.85	1.0	0.40	.004	
R8	Resistor	Short	a) Regulator output will equal input minus three volts. b) Probable Mission Failure	0.5	.0005	99.85	1.0	.05	.025	
		Open	a) Output of regulator will equal input less three volts. b) Probable Mission Failure	0.5	.0038	99.85	1.0	.38	.19	
		Drift	a) Long or short delay and possibly no SCR firing. b) Possible Mission Failure	0.1	.0005	99.85	1.0	.05	.005	

COMPONENT: EDIM
DRAWING NO:
VENDOR:

TABLE 3-3-I

SINGLE FAILURE MODE CRITICALITY ANALYSIS

SYSTEM:
SUBSYSTEM:

CODE NO.	ELEMENT	FAILURE MODE	EFFECT CATEGORY: FAILURE EFFECT a. SUBSYSTEM b. MISSION	EFFECT LEVEL	FAILURE RATING: GENERIC λ (x 10^6)	"USE" FACTOR Wt	OPERATIONAL HISTORY K	FAILURE RATING K Wt λ (x 10^6)	CRITICALITY (EFFECT LEVEL) x (FAILURE RATING)	REMARKS
R9	Resistor	Short	a) No regulator current since possible regulator damage during tests.							
			b) Possible Delay	0.0	.004	99.85	1.0	.40	0.0	
		Open	a) No firing of SCR.							
			b) Mission Failure	1.0	.032	99.85	1.0	3.2	3.2	
		Drift	a) Possible current since degradation.							
			b) Possible Delay	0.0	.004	99.85	1.0	0.40	0.0	
R10	Resistor	Short	a) Regulator Output will equal input.							
			b) Possible Degradation	.01	.0005	99.85	1.0	0.05	.0005	
		Open	a) No Effect							
			b) No Effect	0.0	.0038	99.85	1.0	0.38	0.0	
		Drift	a) Negligible Effect							
			b) No Effect	0.0	.0005	99.85	1.0	0.05	0.0	
R11	Resistor	Short	a) Possible overstress of resistor R1 during S/A "Safe" condition.							
			b) No effect. Any damage to R1 should be detected during tests.	0.0	.0005	99.85	1.0	0.05	0.0	
		Open	a) "Safe" condition cannot be achieved.							
			b) No Effect except possible delay.	0.0	.0038	99.85	1.0	0.38	0.0	
		Drift	a) No Significant Effect							
			b) No Effect	0.0	.0005	99.85	1.0	.05	0.0	

TABLE 3-3-I

COMPONENT: EDM
DRAWING NO:
VENDOR:

SINGLE FAILURE MODE CRITICALITY ANALYSIS

SYSTEM
SUBSYSTEM

CODE NO.	ELEMENT	FAILURE MODE	EFFECT CATEGORY		FAILURE RATING				CRITICALITY	REMARKS
			FAILURE EFFECT a. SUBSYSTEM b. MISSION	EFFECT LEVEL	GENERIC λ ($\times 10^{6}$)	"USE" FACTOR Wt	OPERATIONAL HISTORY K	FAILURE RATING K Wt λ ($\times 10^{6}$)	(EFFECT LEVEL) x (FAILURE RATING)	
R12	Resistor	Short	a) No Effect b) No Effect	0.0	.0005	99.85	1.0	.05	0.0	
		Open	a) Loss of Voltage Monitor b) Possible Delay	0.0	.0088	99.85	1.0	.38	0.0	
		Drift	a) No Effect b) No Effect	0.0	.0095	99.85	1.0	.05	0.0	

In addition, the probability that a particular failure mode will actually result in a mission failure is also needed. The failure rates used in Table 3.3-I were obtained from Reference 6. The portion of each component/ generic failure rate attributable to a specific failure mode is based upon data from Reference 7, engineering judgment and estimates of the component complexity dedicated to the functions involved in a specific component failure mode.

The probability that a particular failure mode will result in a mission failure was represented herein by the "Effect Level". The "Effect Level" values are estimated for each failure mode using the following table as a baseline.

TABLE OF "EFFECT LEVEL" NUMBERS

Guidelines	
Actual Loss	1.0
Probable Loss	0.5
Possible Loss	0.1
Negligible	0.01
No Effect	0.00

Adjustment of the failure rates for the effects of the component operating environments and the time exposure to these environments was achieved by the use of an environmental exposure factor (Wt). The "W" component varies with the stage of flight as indicated in Table 3.3-II. The "t" component is the time during which each value of the weighting factor "W" is applicable. The cumulative value of "Wt" is applied to adjust the generic failure rates for the cumulative effects of the imposed EDIM environment.

TABLE 3.3-II

TYPICAL SCOUT OPERATING TIMES AND ENVIRONMENT

	Flight Phase	Duration t (hours)	Weighting Factor (W)	Wxt	Cumulative Wxt
1	1st Stage Burn	.0220	1000	22.00	22.00
2	1st Stage Coast	.0035	500	1.75	23.75
3	Second Stage Burn	.0114	1000	11.40	35.15
4	Second Stage Coast	.0014	500	0.70	35.85
5	Third Stage Burn	.0104	1000	10.40	46.25
6	Third Stage Coast	.1052	500	52.60	98.85
7	Spin Coast	.0020	500	1.00	99.85

The Single Failure Mode and Criticality Analysis form (Table 3.3-I) has a column for an operational history modifier (K). For this analysis K is assigned the value "1" because insufficient history is available for the Scout EDIM to justify the use of this factor as a criticality modifier. In the analysis charts given by Table 3.3-I the calculations proceed as follows.

Failure Rating = (Wt) K λ_G

From the Failure Rating, the Criticality is obtained as follows:

Criticality = (Effect Level) X (Failure Rating).

The Failure Rating is not intended for use in reliability calculations. It should be interpreted only as a factor of component criticality. The criticality value itself is intended only as a relative figure of significance between the EDIM component failure modes. The absolute value of the criticality has no real significance except as a relative measure of criticality.

Table 3.3-II presents the failure mode, effects and criticality analyses for the EDIM. Only single order failures are considered (no multiple failures) and all components are assumed to be operating properly just prior to the occurrence of any failure.

4.0 TESTING

This section presents a discussion of the EDIM testing needs and capabilities. The discussion presents information regarding critical design elements which should be considered during formulation of the detailed acceptance testing and checkout procedures in order to realize the full reliability performance potential of the EDIM.

The EDIM design includes features which will enable a comprehensive functional verification prior to flight. These features are listed below.

A. A Voltage Monitor is provided to allow a voltage check at firing capacitors C8 and C9. The voltage indication at the Voltage Monitor allows verification of adequate firing capacitor voltage and may be employed to detect any excessive firing capacitor leakage. Any firing capacitor capacitance change may also be detected by discharging the firing capacitor through the Voltage Monitor Resistor R12 to obtain an energy signature (time constant measurement). Also, with battery power applied, any significant change in the EDIM standby current or zener regulation will cause a change in the Voltage Monitor indication.

B. Remote start capability is provided so that the EDIM can be started so as to verify proper time delay performance.

C. Included in the EDIM design are provisions which can be employed to verify firing of the SCR with the EDIM in the "Safe" condition.

D. The EDIM voltage regulator (Z1) output can be monitored to verify proper voltage and to measure available internal power operating time prior to loss of regulation. The internal power operating

time check will reflect any degradation in capacitors C3 through C7 in that any significant decrease in capacitance or increase in capacitor leakage will decrease the internal power operating time/energy available before regulation degrades.

The above provisions/capabilities can be used to obtain a very comprehensive functional integrity verification of the EDIM just prior to launch. Utilization of all of these capabilities is desirable in order to achieve the best possible verification of the EDIM functional integrity.

Verification/detection of the following critical parameters/conditions just prior to launch is deemed desirable to enhance EDIM reliability to the fullest extent possible.

1. Capacitor Charge Voltage (C8 & C9)
2. Capacitor Degradation, Leakage and Capacitance Change (C3 to C9)
3. Firing Capacitor Energy Signature (Time Constant as measured through R12)
4. Internal Power Operating Time Capability
5. Regulator Output Voltage
6. Time Delay and SCR Firing

Comparisons of the quantitative values from these measurements with prior test data will detect degradation processes even before they have advanced to the severity level wherein failure to function will result.

Additional parameters (to the six listed above) which should be measured directly during acceptance testing are EDIM standby current drain, firing capacitance (C8 and C9) and source capacitance (C3 through C7).

Planned environmental testing of the EDIM Engineering Model includes high and low temperature (0°F to 176°F), mechanical shock, and random vibration. See SEI 3225 for detail delineation of the environmental test levels.

5.0 EDIM RELIABILITY PREDICTION

A quantitative reliability prediction has been performed for the EDIM. The prediction was performed in order to obtain an EDIM reliability estimate to be used in comparing the EDIM reliability with that of the existing pyrotechnic type delay initiator. The prediction resulted in an estimated EDIM reliability value greater than 0.9999. This value is a quantitative estimate of the probability that no catastrophic piece-part failure will occur during its mission function period given 100% piece-part integrity at the time of launch. The estimate is the EDIM reliability based on the inherent reliability of its piece-parts.

The EDIM reliability prediction is presented in Figure 5.0-1. The piece-part failure rates and environmental modifiers used in the prediction were obtained from Reference 6. Operating time for the EDIM was assumed to be 15 seconds. Non-operating failure rates were assumed to be 10% of operating failure rates. Total flight time was assumed to be 560 seconds of which 545 seconds was spent with the EDIM in the non-operating state.

A reliability estimate for the presently used Model SD60A1 delay initiator was obtained using Reference 8 failure rate (λ) data. A failure rate of 400×10^{-6} failures per hour is given for this unit when subjected to the environmental stresses of a Scout launch. The reliability estimate for the SD60A1 unit was obtained as shown below using a flight time of 560 seconds:

$$R = e^{-\lambda t} \approx e^{-(400 \times 10^{-6})(560/3600)} = e^{-62.2 \times 10^{-6}} > .9999$$

This estimate indicates that the EDIM and the existing SD60A1 have inherent reliability values of the same order of magnitude. However, the SD60A1 pyrotechnic delay initiator cannot be subjected to a comprehensive function check, since it is a one-shot item, whereas the EDIM will receive such a verification prior to launch. The high value of the predicted EDIM reliability and the comprehensive check-out capability of the EDIM are deemed to be adequate bases to expect equal or superior reliability performance for the EDIM as compared to the existing pyrotechnic-type delay.

FIGURE 5.0-1

EDIM RELIABILITY PREDICTION

	Component	N	λ_G (10^{-6}) f/hr.	K	$N\lambda_G$ (10^{-6})f/hr.	$KN\lambda_G$ (10^{-6})f/hr.
1.	Xister (UJT), 2N1671C	1	0.410	25	0.410	10.250
2.	Diode (SCR), RCA40654	1	1.000	25	1.000	23.000
3.	Diode, 1N4001	2	0.410	10	0.820	8.200
4.	IC, μa 723	1	0.400	10	0.4000	4.000
5.	Capacitor, Ceramic	1	0.0052	15	0.0052	0.078
6.	Capacitor, Tantalum	8	0.0480	1	0.3840	0.384
7.	Resistor(s), Fixed Film RNR55C; R3, R4, R6, R8, R10, 11, 12	7	0.0047	10 est	0.0329	0.329
	RNR65C; R1	1	0.0047	10 est	0.0047	0.047
8.	Resistor, Wirewound RWR815; R5, R7, R9	3	0.040	10 est	0.1200	1.200
9.	Resistor, Film R2; Dale MMF-1/8	1	0.040	10 est	0.040	0.400
10.	Diode, Zener, GZ4001A	2	1.25	10	2.500	25.000
						$\Sigma KN\lambda_G = 74.888$

$$\text{Reliability} = e^{-\Sigma KN\lambda_G(t_o + 0.1t_{no})}$$

$$= e^{-74.888\,(15 + 0.1 \times 545)\,\left(\frac{10^{-6}}{3600}\right)} = e^{-1.4458 \times 10^{-6}} > 0.9999$$

where: $\Sigma KN\lambda_G$ = Summation of Weighted Failure Rates (10^{-6} failures/hr.)

t_o = Operating Flight Time (hours)

t_{NO} = Non-operating Flight Time (hours)

6.0 CONCLUSIONS AND RECOMMENDATIONS

This section presents the conclusions and recommendations resulting from the analysis results presented in this report. The conclusions are based upon the analyses and evaluations of the proposed EDIM Engineering Model design. The recommendations are proposed for implementation in the EDIM Qualification and/or production units, as applicable. Documentation of the Final EDIM design will be included in an update to this report to be issued after completion of the Engineering Model tests.

Conclusions

1. The EDIM is capable of delivering 226% (126% Safety Factor) of the SBASI energy required for initiation under worst case conditions. The EDIM firing circuit design is considered adequate to assure reliable initiation of SBASI's (Reference Section 3.1.1 herein).
2. THE EDIM timing circuit design is capable of meeting the design requirement for a minimum 3.0 second initiation delay if adequate allowances are made to compensate for low temperature effects when selecting timing resistor R3. (Reference Section 3.1.2.1 herein)
3. The SCR Trigger Circuit design will not fire the SCR under worst case conditions of component parameters and low temperature ($0^{\circ}F$) (Reference Section 3.1.2.2 herein).
4. The worst case electrical/thermal stress levels imposed on the EDIM pieceparts are within specification limits during operation of the EDIM. (Reference Section 3.2.2 herein).
5. The failure mode analysis indicates the following top five critical failure modes in their order of criticality.

Criticality	Failure Mode
1. 49.93	Short of SCR CR1
2. 49.33	Open of SCR CR1
3. 29.96	Short of Zener Diode CR2
4. 29.96	Short of Zener Diode CR3
5. 20.47	Short or Open of UJT Q1

None of the criticality levels are deemed to be problem areas and the EDIM test capability is available for a comprehensive check of these five failure modes (Reference Section 3.3 herein).

6. The energy analysis presented in Section 3.1.3 herein indicates that there will be insufficient energy in source capacitors C3→C7 to assure normal operation of the EDIM for the required 4.5 second (minimum) operating period at worst case conditions.

7. The EDIM reliability prediction indicates that the EDIM and the Model SD60A1 delay unit both have inherent flight reliability values greater than 0.9999. The high predicted reliability value and the comprehensive check-out capability for the EDIM is expected to result in a reliability performance equal to or better than the existing pyrotechnic type SD60A1 delay initiator (Reference Section 5.0 herein).

Recommendations

1. Although the analysis results of Section 3.1.1 herein show that the firing circuit design will provide adequate SBASI initiation energy, even at worst case conditions, it is recommended that some form of quantitative energy verificatinn measurement be performed as a part of production acceptance testing.

2. As a result of the SCR triggering problem (discussion in Section 3.1.2.2) which could occur with the SCR (Type 40654) used in conjunction with the UJT (Type 2N1671C) a circuit change is indicated. It is recommended that a solution to this problem be found and implemented in the EDIM qualification unit. Preliminary analysis indicates that selection of another UJT type in combination with a higher regulated voltage is a promising approach.

3. It is recommended that some measures be taken to assure that adequate energy will be available to meet EDIM design requirements for operating time under the worst case conditions defined in Section 3.1.3 herein.

4. All RNR55C or RNR65C resistors should be purchased so as to avoid the problems referenced in ALERT No. MSFC 74-02. (Reference Section 3.2.1 herein)
5. Further evaluation of the options and requirements is recommended regarding determination of the most desirable approach to the matter involving selection of timing resistor R3 during EDIM build-up. (Reference Section 3.1.2.1 herein)
6. In the event that improved capacitors with a higher surge voltage rating (which also meet the other EDIM requirements) become available in the future, replacement of C3 C9 with the improved components should be pursued to improve stress margin and to enhance EDIM reliability.

REFERENCES

1. NASA Technical Report 32-1556, Evaluation of Electroexplosive Devices by Non-destructive Test Techniques and Impulsive Waveform Firings, V. J. Menichelli, 15 June 1972

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5. Drawing No. 23-004349; Assembly, 4th Stage Squib Electronic Delay Ignition System

6. MIL-HDBK-217A, Reliability Stress and Failure Rate Data for Electronic Equipment

7. ASD-R-05-61-1, Information for Reliability Prediction, G.E. Technical Memorandum

8. Scout Report No. 23.302A, "Failure Mode, Effects and Criticality Analysis of the Scout Ignition System"

TITLE

RELIABILITY EVALUATION
SCOUT FOURTH STAGE
ELECTRONIC DELAY IGNITION MODULE

ADDENDUM A

SUBMITTED UNDER	
Task R-59	
REPORT NO.	DATED
2-54232/5R-23025	1 August 1975
PROJECT	CONTRACT NO.
Scout	NAS1-12500

APPROVED: F. H. Harrison, Jr.
F. H. Harrison, Jr.
Supervisor - Reliability
Design & Control

J. D. Clark Jr.
PREPARED
J. D. Clark, Jr.

R. L. Brodsat
REVIEWED

J. Martinez
J. Martinez
Manager - Scout
Quality & Reliability

REV.	DATE	REV. BY	PAGES AFFECTED	REMARKS

RELIABILITY EVALUATION
SCOUT FOURTH STAGE ELECTRONIC DELAY IGNITION MODULE - ADDENDUM A

1.0 GENERAL

This addendum provides the information, data and analyses necessary to update the original EDIM reliability evaluation document (Report No. 2-54232/5R-23013, released 9 June 1975) to reflect the EDIM design as implemented in the EDIM Qualification Unit Configuration. Included herein is information regarding all design changes with their purpose and reliability impact. Also included is the status of recommendations and conclusions presented in the original EDIM reliability evaluation document and final conclusions regarding the EDIM design as implemented in the Qualification Unit Configuration. Section 4.0 herein presents some additional data not presented in the original evaluation.

The following definitions are employed in this addendum for convenience in the discussion of the EDIM design evolution.

1. Preliminary Design Configuration - This is the first documented EDIM design configuration. It was this configuration which was subjected to the reliability evaluation documented in the original report. This configuration was subjected to informal Engineering testing to obtain operational data.

2. Engineering Model Configuration - This is the configuration as modified to incorporate most of the changes resulting from the reliability evaluation and informal Engineering test results. This unit was subjected to Design Verification Tests.

3. Qualification Unit Configuration - This is the EDIM configuration incorporating the remaining design changes resulting from the reliability evaluation. This unit successfully completed all environmental qualification testing per 23-TRA-0244.

4. Original Evaluation - This term will be used herein for convenience to refer to the original EDIM evaluation report of 9 June '75, Report No. 2-54232/5R-23013.

2.0 DESIGN CHANGES

The following is a listing of the EDIM design changes or refinements which have been incorporated into the EDIM (Qualification Configuration, Figure 1) since the reliability evaluation of the Preliminary Design Configuration.

1. UJT designated Q1 was changed from a 2N1671C to a 2N494C type.

Discussion: This change was incorporated in order to eliminate the possibility of an SCR "no-fire" condition due to excessive UJT emitter saturation voltage, V_E (SAT), which can occur at low temperature with the 2N1671C. The replacement UJT Type 2N494C has a number of inherent parameter advantages including lower maximum V_E (SAT), higher minimum intrinsic stand-off ratio and higher minimum interbase resistance. Each of these advantages combine to achieve reliable SCR firing conditions even at minimum temperature. This UJT component selection change solves the SCR "no-fire" problem identified in the original evaluation as Conclusion 3/Recommendation 2.

2. Voltage regulator Z1, a Fairchild μa 723 type in the Engineering Model Configuration, has been changed to a Signetics SE550 type regulator as of the Qualification Unit Configuration.

Discussion: The component selection change for Z1 was made due to the source capacitor energy budget shortage problem identified as Conclusion 6/Recommendation 3 in the original evaluation.

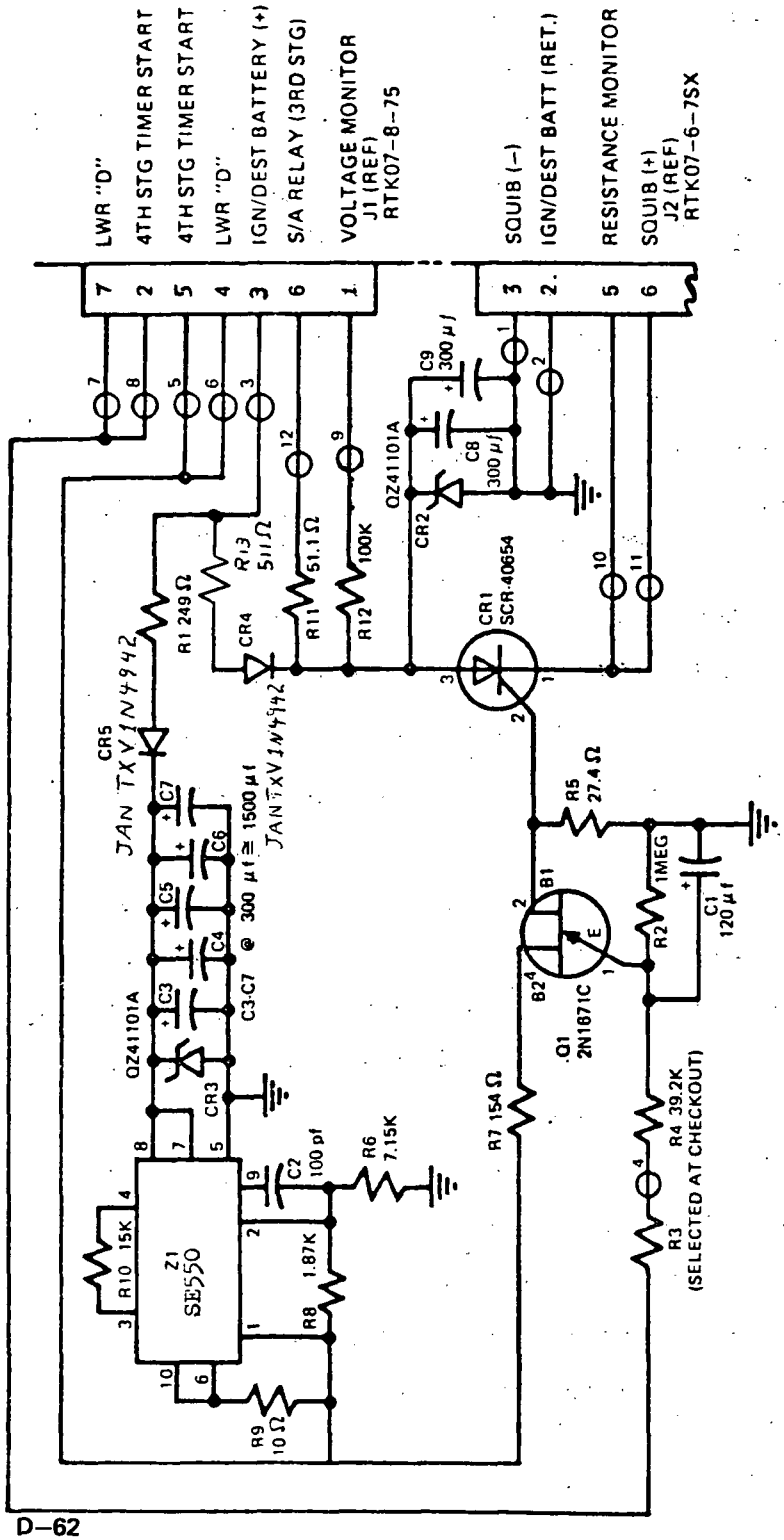


FIGURE 1 EDIM SCHEMATIC
(QUALIFICATION CONFIGURATION)

The relatively high maximum stand-by current applicable to the μa 723 type was the principal contributor to the source capacitor energy deficiency. Selection of the SE550 type regulator in combination with the UJT change successfully resolved the energy problem.

3. Circuit diodes CR4 and CR5, which were type 1N4001 in the Preliminary Design Configuration, were changed to a JANTXV1N4942 type.

Discussion: This diode selection change was made in response to the parts construction and reliability information obtained during a diode investigation resulting from a Scout flight anomaly. The increased vendor screening and superior construction of the JANTXV1N4942 type diode will enhance the EDIM reliability.

4. The EDIM J1 and J2 connector pin assignment used for the Engineering Model Configuration was subjected to reliability evaluation from the standpoint of EDIM function and Scout mission effects resulting from single adjacent pin to pin shorts in the connectors. As a result of this evaluation the pin function assignments for J1 pins 1 and 7 were interchanged. For J2 the pin function assignment for pin 1 was transferred to pin 3 (previously unassigned) leaving pin 1 unassigned (see Figure 1 for new pin assignment).

Discussion: The pin assignment changes resulted in elimination of five critical EDIM failure modes which could have resulted from adjacent pin-to-pin shorts.

5. A slight change from the EDIM Preliminary Design Configuration circuit architecture was incorporated as of the Engineering Model Configuration. This modification consisted of addition of resistor R13 and a change of the firing circuit branch point from the low potential side of R1 to the high potential side of R1 (directly to IGN/DEST BATTERY (+) potential). This new architecture can be seen in Figure 1.

Discussion: This circuit architecture modification was necessary for circuit checkout operation in the S/A Relay "Safe" mode but, additionally, the change improved firing circuit energy performance since the firing capacitors (C8 and C9) charge voltage will not now be degraded by the voltage drop across R1 as it had been in the Preliminary Design Configuration.

6. Minimum component screening requirements have been defined and are given by Table 1. These screening requirements were defined in order to assure adequate parts reliability and in response to EDIM problems identified in the reliability evaluation.

Discussion: Of special significance among the requirements of Table 1 is the 15 ma maximum gate current (I_{GT}) limit imposed on the SCR-40654 (CR1). This limit is a factor in the assurance of reliable firing of the SCR at worst case conditions.

3.0 STATUS OF CONCLUSIONS, RECOMMENDATIONS AND PROBLEMS

This section presents the status of the recommendations and problems delineated in the original EDIM reliability evaluation. Any significant change in the previous conclusions as presented in the original evaluation are also discussed herein.

TABLE 1

MINIMUM COMPONENT TEST/SCREENING REQUIREMENTS

PART NO./NAME	VSD RECEIVING INSPECTION	SCREENED AT VENDOR	COMMENTS
Z1-SE550 Voltage Regulator	Functional Test	Military Grade	Tested for operation @ -55°C to +125°C
Q1-2N494C Transistor	Functional Test	Pre-cap. Visual Inspection	
CR1-40654 SCR	Functional Test	Pre-cap. Visual Inspection	After acceptance test units will be screened to limit maximum gate current to 15 ma. (to trigger SCR)
CR4, 5-1N4942 Diode	Functional Test	JANTXV Screening	Unitrode Diode
CR2, CR3-GZ41101A	Functional Test	Selected to 1% Voltage	Selected by operational test. General Semiconductor Industries
C3-C9, M39006/09-6518 Capacitor 300 μ f	Functional Test	MIL-C-39006/09 Failure Rate P	Lowest failure rate available for Tantalum Wet Slug Capacitors
C1-M39006/09-6476 Capacitor 120 μ f	Functional Test	MIL-C-39006/09 Failure Rate P	Lowest failure rate available for Tantalum Wet Slug Capacitors
C1-M39014/05-2819 Capacitor	Functional Test	MIL-C-39014/05	Ceramic Capacitor available
R3, R4, R6, R8, R10, R11, R11 RNR55CXXXFS Resistor	Functional Test	MIL-R-55182 Established Rel.	Lowest Failure Rate available
R1, R3 RNC65HXXXX	Functional Test	MIL-R-55182 Established Rel.	Lowest Failure Rate available
R2, RNC60H1004 FS Resistor	Functional Test	MIL-R-55182 Established Rel.	Lowest Failure Rate available
R5, R9, R7 RWR81510RO FR	Functional Test	MIL-R-55182 Established Rel.	Lowest Failure Rate available

3.1 Single Bridgewire Apollo Standard Initiator (SBASI) Firing Safety Factor

Conclusion 1 in the original evaluation stated that the EDIM is capable of delivering 226% (126% Safety Factor) of the energy required for SBASI initiation under worst case component and low temperature conditions assuming the SBASI had its minimum (-3 sigma) bridgewire thermal time constant. As a result of the circuit architecture change (see 2.0-5, this addendum) the voltage applied to the firing capacitors C8 and C9 is not degraded by the voltage drop across R1. This configuration results in increased energy available to fire SBASI initiators and improves the margin above the 126% value.

Since the original evaluation, test data (see Table 2) has been obtained indicating that the capacitance degradation of the firing capacitors due to the effects of low temperature will be only 19.66% at -17.8°C as referenced to the value at 25°C. This degradation effect was previously calculated to be 32.1% at -17.8°C as documented in the original evaluation. The original value was based on a linear extrapolation of vendor data. The new value is based on VSD temperature test data taken with thirteen samples of the subject capacitor at the applicable temperatures of 25°C and -17.8°C. Both percent change calculations assume that the 25°C capacitance value for C8 plus C9 is equal to 540 microfarads which is the minimum expected value due to the applicable 10% tolerance for these devices. The smaller temperature degradation effect now expected will result in an improvement of the expected worst case minimum capacitance to a value of 433.84 microfarads for the C8/C9 combination. This new value represents a significant improvement relative to the 366.66 microfarads calculated for the original evaluation. The smaller degradation results in a greater amount of stored energy available to fire the SBASI.

TABLE 2

TEMPERATURE DEGRADATION OF C8/C9 CAPACITANCE

Original Evaluation Values (C8 + C9)

Nominal Value @ 25°C	Minimum Value 25°C	Minimum Value -17.8°C	Temperature Degradation @ -17.8°C
600 μf Total (±10% Tolerance)	540 μf	366.66 μf	* 32.1%

*Vendor specifies 60% decrease over a temperature range of 25°C to -55°C.

New Data Values (C8 + C9)

Nominal Value @ 25°C	Minimum Value 25°C	Minimum Value -17.8°C	Temperature Degradation @ -17.8°C
600 μf Total (±10% Tolerance)	540 μf	433.84 μf	**19.66%

**VSD Test of 13 devices gave 19.66% decrease over a temperature range of 25°C to -17.8°C.

NOTE: Difference in 32.1% value calculated and 19.66% value measured is due to apparent non-linearity of the temperature characteristic over a temperature range of 25°C to -55°C.

The combined effects of the improved circuit architecture and larger minimum capacitance result in a total SBASI bridgewire heating energy of 257% (157% Safety Factor) of that required for SBASI initiation at worst case conditions. This 157% safety factor represents a 25% improvement over the safety factor developed by the Preliminary Design Configuration and reported in the original evaluation.

Recommendation 1 in the original evaluation advised that a quantitative energy verification measurement be performed for production acceptance testing. The results obtained during EDIM Engineering and Qualification testing support the feasibility of such a measurement and the recommendation stands.

3.2 EDIM Timing Circuit

Conclusion 2 of the original evaluation indicates that the timing circuit design is capable of meeting the 3.0 second minimum time delay if adequate compensation is made for the expected low temperature effects when selecting timing resistor R3. Recommendation 5 dealt with the need to establish an approach for dealing with this EDIM characteristic. The approach selected for the Engineering Model and Qualification Unit Configurations was to select R3 so that the time delay was 3.5 seconds minimim at 25°C. This approach is deemed adequate since it will assure that the minimum 3.0 second delay requirement is satisfied even at low temperature. Temperature effects will not cause a delay time decrease greater than the 0.5 second margin available at 3.5 seconds as shown by the calculation in the original evaluation. No further action is indicated for this area of concern.

3.3 SCR Trigger Circuit Problem

Conclusion 3 of the original evaluation indicates that the SCR trigger circuit will not fire the SCR for the worst case condition of circuit parameters and temperature. Recommendation 2 also addressed this problem and suggests one promising approach to a solution. In response to this problem a different UJT (2N494C) with better parameters than the 2N1671C unit was selected and SCR screening selection criteria limiting the maximum SCR gate trigger current (I_{GT}) to 15 milliamperes was imposed (see Table 1). Revised calculations using the new UJT parameters and I_{GT} maximum show that these features do result in adequate gate drive to assure SCR firing at worst case conditions. No further action is deemed necessary.

3.4 Worst Case Electrical/Thermal Stress Levels

The MDIM design changes imposed since the original reliability evaluation have not significantly changed the stress levels as presented in the original report. Each of the existing corresponding piece-part/component stress levels have remained within specification limits and no further action is deemed necessary.

3.5 Additional Failure Modes

As a consequence of the design changes delineated in this addendum one additional component (R13) has been added since the original evaluation. An open of this resistor during flight could cause a loss of mission. However, due to the low failure rate for this device, the resultant failure mode criticality is low and will not rank among the top five failure modes listed in Conclusion 5 of the original evaluation. It should be noted that in the original circuit architecture an open of R1 would also cause the failure effects now related to a short of R13. Therefore, this failure effect is not a new one and only be probability of its occurrence is affected by the

addition of R13. A short of R13 would cause problems only during ground check-out of the EDIM. The criticality of R13 is not deemed to be a problem area.

3.6 Source Capacitor Energy Budget

Conclusion 6 of the original evaluation identified an energy budget deficiency problem for operation of the EDIM on internal circuit power (with energy stored in capacitors C3 through C7). With the Preliminary Design Configuration there was not sufficient energy stored in the C3 through C7 source capacitors to operate the EDIM for the minimum required 4.5 seconds with worst case circuit parameters at low temperature. Recommendation 3 stated that some action or combination of actions be taken to rectify the energy deficiency. Some possible corrective options were identified in Section 3.1.3, Page 27, of the original evaluation.

The energy budget problem was rectified in the Qualification Unit Configuration by a combination of three factors as indicated below.

1. Replacement of the UJT 2N1671C with the 2N494C device.

2. Replacement of the Fairchild μa 723 IC regulator (Z1) with a Signetics SE550 IC regulator.

3. Test data finding that less source capacitance degradation occurred at low temperatures than predicted by linear extrapolation of vendor data for the original evaluation. (32.1% degradation predicted, 19.66% measured)

Factors 1 and 3 above were the most significant in affecting improvement of the predicted energy budget. The IC regulator (Z1) change was made specifically to correct the energy budget deficiency. The selected SE550 regulator has a significantly lower maximum stand-by current demand than the μa 723 (2 ma versus 3.5 ma). Selection of the 2N494C was made to resolve the SCR firing problems but also mitigated the energy budget deficiency because of its increased minimum R_{BBO} as compared with the 2N1671C of the Preliminary Design Configuration (R_{BBO} is 6.21K Ω minimum for 2N494C versys 4.9K Ω minimum for the 2N1671C). The higher UJT R_{BBO} results in less current drain. Test data verifying less than predicted capacitance degradation at low temperature means that more energy will be available in the source capacitors at the beginning of the 4.5 second internal power period. The combination of more source capacitance in C_S (C3 through C7) and lower current demand by regulator Z1 and UJT Q1 has resulted in the energy budget performance improvement necessary to operate on internally stored energy for the minimum required 4.5 seconds at worst case conditions. No further action is deemed necessary relative to the EDIM energy budget.

3.7 EDIM Reliability Prediction

The changes in the EDIM design have not been extensive enough to significantly affect the reliability prediction as presented in the original evaluation (Conclusion 7). The magnitude of the effect of the changes made is within the expected error of the original prediction so as to not affect the reliability value of 0.9999 previously predicted.

3.8 Alert Status

Recommendation 4 identified GIDEP Alert Number MSFC 74-02 for particular attention because of applicability to all RNR55C and RNR65C resistors. Purchase of these resistor types for any future EDIM production should be performed in such a way as to avoid the problem described in the ALERT. The new component types incorporated into the Qualification Unit Configuration EDIM were compared to the Alerts on file at VSD and no new ALERT problem areas were detected.

3.9 Surge Voltage Rating (C3 through C9)

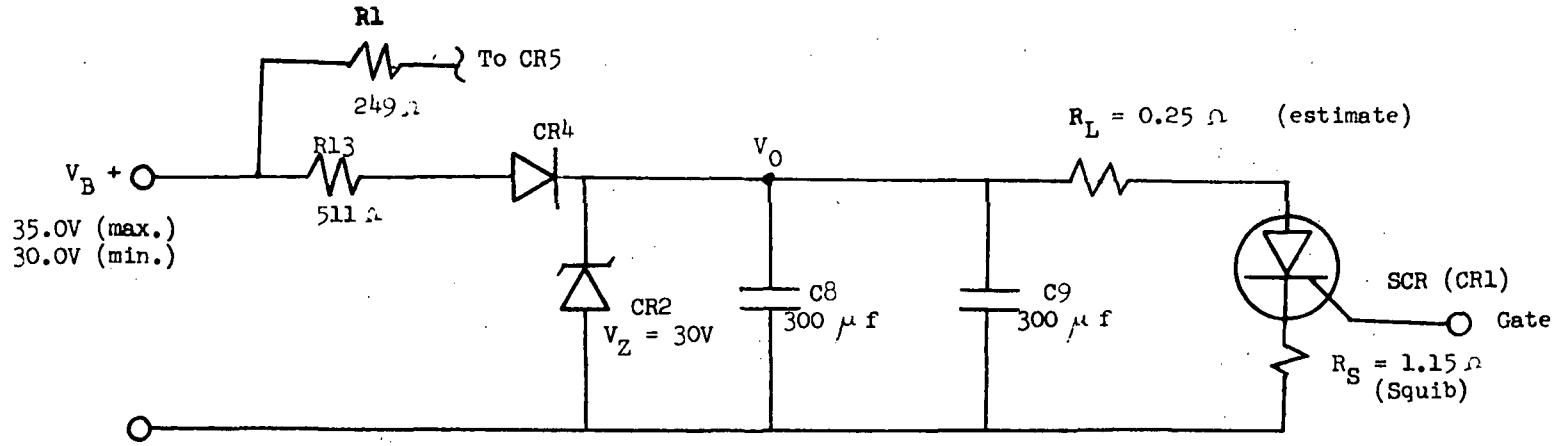
The original evaluation recommended (Recommendation 6) consideration of replacement of C3 through C9 by devices of higher surge voltage rating should such an appropriate higher rated device become available. Such a replacement would be intended to improve the stress margin achieved in the EDIM and thereby enhance EDIM reliability. This recommendation remains valid for any future production of EDIM units for Scout. However, the maximum surge voltage stress ratio imposed (see Table 3.2.2-II in the original evaluation) is within the vendor's specification and is not deemed to be a reliability problem at this time due to the low duty cycle of this applied surge voltage.

4.0 MINIMUM EDIM FIRING VOLTAGE FOR SBASI

Figure 2 depicts the EDIM Firing Circuit Schematic as it exists in the EDIM Qualification Unit Configuration. By proceeding in a manner like that described in detail in the original evaluation the available squib initiation energy (E_A) is given by:

$$E_A = \int_o^{t\,(max)} P_i dt = \left(\frac{V_O - V_T}{R_T}\right)^2 R_S\,(eff) \left(-\frac{R_T C f}{2}\right) \left(e^{-2t\,(max)/R_T C f} - 1\right)$$

Table 3 presents a description of the parameters and changes in the evaluation from that presented in the original evaluation.



C8 = C9 = 216.92 μf (Worst Case Min. @ -17.8°C) Reference Data Sheets

C_f(Total) = 433.84 μf (Worst Case)

V_B = 30V (Min., Reference Ign./Dest. Battery Characteristic)

R_L = 0.25 Ω (Estimate of Conductor Loop Resistance)

R_S = 1.15 Ω (Max. Cold Resistance of SBASI Squib)

V_T (SCR) = 1.60461 (Maximum Constant Fwd. Voltage Drop-in Conduction State)

I_L (SCR) = 8.0 μa (Worst Measured Leakage of 19 Devices Tested @ 25°C)

V_Z (CR2) = 30V ± 1% (Reference 4)

I_L (CR2) = 1.0 μa (Estimated Leakage)

FIGURE 2
EDIM FIRING CIRCUIT SCHEMATIC
(QUALIFICATION CONFIGURATION)

TABLE 3

DESCRIPTION OF FIRING CIRCUIT PARAMETERS

V_O = Voltage on Firing Capacitors at t = 4.0 seconds (when SBASI fires)

$V_O = V_Z$ (CR2, min.) - ΔV_L

where:

V_Z (CR2, min.) = 28.4417V (Qualification Test Data)

ΔV_L = 0.1366V (Original Evaluation)

V_O = 28.4417 - 0.1366

= 28.31V

V_T = SCR Maximum Constant Forward Voltage Drop In Conduction State

V_T = 1.60461V

This quantity revised from original evaluation by separating the constant and current sensitive SCR forward voltage components. This technique requires revising the quantity R_T as shown below.

R_T = Total Ohmic Resistance of Firing Circuit Including Squib, Conductor and SCR

$R_T = 1.3R_S + R_L + S$

where: $1.3R_S = R_S$ (eff) = Maximum Effective Squib Resistance

R_L = Conductor Loop Resistance (.25 Ω)

S = SCR max. Voltage/Current Slope (ohms)

R_T = 1.3 (1.15) + 0.25 + 0.0417

= 1.7867 Ω , Note R_S (eff) = 1.495 Ω

C_f = 433.84×10^{-6} μ f = Minimum Firing Capacitance @ -17.8°C

t(max) = Time to Maximum Bridgewire Temperature

= 0.92491 milliseconds (Evaluated same method as original evaluation)

V_O = 28.4417 - 0.1366 = 28.31V; Value applicable to Qualification Unit

V_T = 1.60461V

R_T = 1.7867

R_S (eff) = 1.3 R_S = 1.495 Ω

C_f = 433.84 x 10^{-6} μf

t (max) = 0.92491 ms

E_A = -0.1294 ($e^{-2.3864}$-1) joules (j)

= -0.1294 (-0.90804) j

= 117.5 millijoules (mj)

The value 117.5 mj is the total energy delivered to the SBASI. The value 129.4 mj is the total energy delivered to the SBASI plus that remaining in the capacitor C_f (C8 + C9). This quantity (129.4) is broken down into its components, shown below, using the same technique as presented in the original evaluation.

a) Fraction Heating Bridgewire (E_u) = 0.652899 (129.4) = 84.485 mj

b) Heat Loss Fraction = 0.255141 (129.4) = 33.015 mj

c) Fraction Left in Capacitor (C_f) = 0.091960 (129.4) = 11.900 mj

129.400 mj

Check: E(a) + E(b) = 84.485 + 33.015

= 117.500; thus verified

$$\text{Safety Factor} = \frac{E_u - E_c}{E_c} = \frac{84.485 - 32.85}{32.85} = 157\% \text{ margin}$$

Using the equation for E_A the minimum voltage required to fire a worst case SBASI at worst case circuit conditions can be calculated.

$$V_O\ (min) = R_T \frac{E_A\ (min)}{R_S\ (eff)\left(\frac{-R_T C_f}{2}\right)\left(e^{-2t\ (max)/R_T C_f} - 1\right)} + V_T$$

$$E_A\ (min) = \frac{E_c}{\left(1 - e^{-2t\ (max)/R_T C_f}\right)} = \frac{E_c}{\mathcal{S}}$$

E_c = SBASI characteristic energy (32.85 mj)

$\mathcal{S}$ = Fraction of Total C_f Energy Available (.90804)

$$E_A\ (min) = \frac{32.85\ mj}{.90804} = 36.172$$

$$V_O\ (min) = 1.7867 \sqrt{\frac{36.172 \times 10^{-3}}{(-5.7942 \times 10^{-4})(-0.90804)}} + 1.60461$$

$$= 1.7867 \sqrt{68.7502} + 1.60461$$

$$= 16.491V$$

V_f (min) = Minimum voltage on C_f at t = 0 which will supply E_c

$= V_o\ (min) + \Delta V\ (leakage)$

$= 16.419 + 0.1366$

$= 16.5556V$

V_A (min) = Minimum applied voltage (to EDIM) which will result in initiation of worst case SBASI at worst case conditions.

$= V_f\ (min) + V\ (CR4)$

$= 16.5556 + 0.7$

$= 17.256V$

The value of V_A (min) calculated above is the minimum battery voltage at which a worst case (with -3 σ thermal time constant) SBASI would fire at worst case circuit and thermal conditions. It should be noted, however, that the value V_A (min) = 17.256 is applicable only to the EDIM SBASI firing circuit and it is not intended to represent the minimum voltage at which the total EDIM circuitry will function.

5.0 FINAL CONCLUSIONS

The EDIM has been subjected to a comprehensive reliability evaluation and qualification test (see 23-DIR-1779 for qualification test details). The results of the reliability evaluation and qualification testing indicate that the EDIM design will satisfy the Scout flight requirements.

APPENDIX E
QUALIFICATION REPORT

DESIGN INFORMATION [redacted] - RELEASE 8-14-75

MO (S) AND EFF. Qualification of Scout 4th Stage Electronic Delay Ignition Module (EDIM)		DIR. NO. 23-DIR-1779	REV.
		DATE 14 August 1975	PAGE 1 OF 12
	SYSTEM Scout	REF. G. O. NUMBER 3384 CV 1220	

Fill in block below for Information Request

TO _____ GROUP _____

REQ. BY _____ GROUP _____

REASON _____

LTV ONLY ☐ EWR ☐ BUWEPS ☐ ☐

Fill in block below for Information Release

IN REPLY TO DIR. NUMBER _____

REL. TO R. G. Urash GROUP 2-58100

PREPARED BY	DATE	CHECKED BY	DATE
W L Bilbo	8/14/75	[signature]	7-25-75
GROUP APP.	DATE	PROJ OFFICE	DATE
F H Harrison Jr	8/14/75	[signature] J R Sylvester	8-11-75

CC A. Gardsbane, F. H. Harrison, J. Martinez, P. R. Provost, R. D. Ward, W. C. Pitts, E. D. Walters, R. G. Urash, J. D. Clark, A. J. Marek E. B. STEWART 19

DESIGN INFORMATION:

I. ENCLOSURES

(1) Test Information Release (TIRA) 2-45202/5R-2 "Qualification and S^2ET of Scout 4th Stage Electronic Delay Ignition Module (EDIM)"

(2) Test and Evaluation Report/Reliability Assurance Laboratory Report No. 2-45202/5R-47, "Ignition Delay Assembly"

(3) Electromagnetic Susceptibility Test Report for the 23-004349-1 Electronic Delay Ignition Module

II. REFERENCES

(1) Drawing 23-004349 - Assembly, 4th Stage Squib Elect. Delay Ign. Sys.

(2) Engineering Test Laboratory Test Request (TRA) 23-TRA-246, "EMI Qualification Test for Scout 4th Stage Electronic Delay Ignition Module (EDIM)"

III. INTRODUCTION

The Electronic Delay Ignition Module (EDIM) was designed for replacement of the NASA - SD60A1 "Pyrotechnic Delay Initiator" as used for

flight application on the Scout Vehicle. To qualify and demonstrate the suitability of the EDIM for flight application, the EDIM was subjected to tests outlined in the test program of enclosure (1). The results of the tests indicate the EDIM has satisfactorily met the requirements of the test program and is, therefore, qualified and suitable for its intended application on the Scout vehicle. A summary of the tests and results thereof are presented below.

IV. QUALIFICATION TESTS

Functional performance and environmental tests were accomplished as outlined by enclosure (1) and enclosure (3). Additional tests were added per Qualification Test Failure Report 23-QTFR-008 in Enclosure (1) to qualify the replaced voltage regulator of the EDIM for flight application. The type, sequence and details of the tests are further delineated below.

1. Pre-Environmental Tasks

The EDIM was weighed and was visually inspected per drawing (reference (1)) for physical defects. Then an insulation resistance test was made between each EDIM connector pin and housing with a megohmeter set at 500 VDC. At the completion of the "MEG" test, a functional acceptance test was performed. This test included two (2) types of checkout; namely, Test A, Delay Timing Cycle Test and Test B, Loss of Regulation Time Test. Both of these tests were accomplished with 30 VDC and 35 VDC alternately applied to the input of the EDIM. The test measurements performed for each type of test is noted below.

Test A - Delay Timing Cycle Test

A. Ignition Charge Voltage

B. Squib Voltage

C. Voltage Regulator Output

D. EDIM Input Voltage

E. Time Delay

Test B - Loss of Regulation Time Test

A. Ignition Charge Voltage

B. Squib Voltage

C. Voltage Regulator Output

D. EDIM Input Voltage

E. Loss of Regulation Time

The above measurements are further defined in paragraphs following the summary of Post-Environmental Tasks.

2. Environmental Performance Tasks

The EDIM was subjected to the following sequence of environmental tests during the qualification test program. A summary of each test is outlined with each environmental test. Functional performance tests were accomplished before, during, and after each environmental test as delineated by Enclosure (1). These functional performance tests included Test A and Test B noted above under Pre-Environmental Tasks. The pre- and post- environmental functional performance tests, with 30 VDC applied at room ambient, will not be noted in the summary. Test measurements of Test A and Test B during each performance test are further defined in paragraphs following the summary of Post-Environmental Tasks.

A. High Temperature/Low Temperature - 1 cycle

1. Stabilized at 160°F and 0°F for a maximum of four (4) hours.

2. Functional Performance Tests when stabilized at each temperature with 30 VDC and 35 VDC alternately applied.

B. Temperature Shock - 3 cycles

1. One hour minimum at $0^{\circ}F$ and $160^{\circ}F$
2. Two shocks per cycle giving a total of six (6) shocks for three (3) cycles.
3. Functional Performance Test at the fifth shock at $160^{\circ}F$ with 30 VDC and 35 VDC alternately applied. EDIM was then monitored with 30 VDC input via oscillograph for the period of the fifth shock.

C. High Temperature - Altitude - 2 cycles

1. After stabilization at $160^{\circ}F$, the chamber internal pressure was decreased to simulate 200,000 feet within five (5) minutes and maintained for a minimum period of ten (10) minutes. The chamber was then returned to room ambient pressure completing one cycle. The cycle was again repeated.
2. Functional Performance Test at the start of each ten (10) minute period at the simulated 200,000 foot altitude with 30 VDC and 35 VDC alternately applied. The EDIM was then monitored with 30 VDC input via oscillograph after completion of test at 35 VDC for the rest of the environmental exposure.

D. Vibration and Mechanical Shock - 1 cycle

1. Vibration - 9.1 GRMS for 80 seconds between 20 Hz and 2000 Hz for each of three (3) orthogonal axes.

2. Mechanical Shock - Three (3) shocks of 75 G's applied to each direction of the three (3) orthogonal axes. A Total of 18 shocks were applied to the EDIM.

3. Functional Performance Test during and between environmental test of each axis with 30 VDC applied. The EDIM was continuously monitored via oscillograph with 30 VDC input.

E. Acceleration - 1 cycle

1. 33.5 G's acceleration applied for two (2) minutes to each direction of three (3) orthogonal axes. A total acceleration time of 12 minutes.

2. Functional Performance Test during and between environmental test of each axis direction with 30 VDC applied. The EDIM was continuously monitored via oscillograph with 30 VDC input.

F. QFTR - No. 23-QTFR-008

The voltage regulator Z-1 was damaged during the post-acceleration functional performance test as explained under the Qualification Test Results. Additional tests were added via the QTFR to qualify the EDIM with the replaced regulator. These additional tests included the repeat of the Temperature Shock test of paragraph B above and 10 cycles of S^2ET Vibration/Mechanical Shock rather than 8 cycles.

G. Temperature Shock - 3 cycles

1. One hour minimum at $0^{\circ}F$ and $160^{\circ}F$
2. Two shocks per cycle giving a total of six (6) shocks for the three (3) cycles.
3. Functional Performance Test at the fifth shock at $160^{\circ}F$ with 30 VDC and 35 VDC alternately applied. EDIM was then monitored with 30 VDC input via oscillograph for the period of the fifth shock.

H. Electromagnetic Susceptibility (EMI)

The EDIM was functional operated while exposed to Electromagnetic Susceptibility Tests per MIL-STD-461 and MIL-STD-462. These tests were as follows:

1. Test CS01 - Conducted susceptibility - 30 Hz to 50 KHz, Power leads
2. Test CS02 - Conducted susceptibility - 50 KHz to 400 MHz, Power leads
3. Test CS06 - Conducted susceptibility - Spike power leads
4. Test RS01 - Radiated susceptibility - 30 Hz to 30 KHz, Magnetic field
5. Test RS02 - Radiated susceptibility, Magnetic Induced (400 Hz and Spike)
6. Test RS-3 - Radiated susceptibility, Electric Field, 14 KHz to 10 GHz

The EDIM was deemed to have passed the susceptibility tests if it "fired" on time and had no spurious firings.

I. S^2ET Acceptance Level Vibration/Mechanical Shock - 10 cycles

1. Vibration - 6.1 G RMS for 40 seconds between 20 Hz and 2000 Hz for each of three (3) orthogonal axes. A total of 30 vibration periods.
2. Mechanical Shock - 50 G's for each of three (3) orthogonal axes in both directions. A total of 60 shocks.
3. Functional Performance Test during and between environmental test of each axis with 30 VDC applied. The EDIM was continuously monitored via oscillograph with 30 VDC input.

J. Humidity - 3 cycles

1. The EDIM was placed in a chamber with 95% humidity and room temperature (humidity was maintained at 95% throughout the environmental test). The temperature was then raised to $120^{\circ}F$ within a period of two (2) hours. The $120^{\circ}F$ temperature was maintained for a period of six hours after which it was reduced to $68^{\circ}F$ over a period of 16 hours, giving a total of 24 hours for one humidity cycle. This test was repeated for three (3) humidity cycles or a total of 72 hours.

2. The EDIM was not operated during the three (3) cycles.

K. Post-Environmental Tasks

An insulation resistance test was performed between each EDIM connector pin and housing with a megohmeter set at 500 VDC. At the completion of the "MEG" test, a functional acceptance test (Test A and Test B) was performed with 30 VDC and 35 VDC alternately applied to the input of the EDIM. The EDIM was then disassembled for visual examination. Enclosure (2) contains the results of this visual examination. At the conclusion of the visual examination, the EDIM was reassembled and a functional acceptance test (Test A and Test B) was performed on the unit with 30 VDC and 35 VDC alternately applied to the input of the EDIM.

The functional performance tests (Test A and Test B noted under Pre-Environmental Tasks) included the following measurements outlined herein. (See reference (1) for schematic).

1. Ignition Charge Voltage:

   Voltage applied to the anode of the SCR via the charged capacitors C8 and C9. This voltage is applied to the squib when the SCR is "fired".

2. Squib Voltage:

   The voltage drop across a one (1) ohm resistor (to simulate a squib) in series with the output of the SCR.

3. Regulator Output:

   The output voltage of the EDIM voltage regulator Z-1.

4. Input Voltage:

   The voltage applied to the EDIM from a power source.

5. Time Delay:

   Time between a start command to the EDIM and the EDIM "firing" pulse output event.

6. Loss of Regulation (LOR) Time: The time between power source turn off to the EDIM and when the voltage regulator Z1 voltage begins to decrease.

V. QUALIFICATION RESULTS

1. Irregularities During Tests

There were two (2) irregularities which occurred during qualification tests, these were:

1. Paint became loose from the surface of the EDIM housing.
2. Voltage regulator Z-1 was damaged during tests, due to test equipment miswiring.

Each of the irregularities is further explained below.

An investigation of the painting process indicated that the paint process specification was not complete. A cleaning step had been inadvertently omitted from the drawing. This deficiency was corrected by EOV 39170. The housing was then repainted and inspected in conformance with the required manufacturing process. The repainted housing did not show any peeling during subsequent temperature cycling at Langley Research Center (LRC).

The Voltage regulator damage, as noted by 23-QTFR-008 in Enclosure (1), was caused by misapplied voltage during the post-acceleration functional test. The functional tests during the acceleration environmental test required additional cables to connect the EDIM located at the Centrafuge and the EDIM Test Panel located outside the Centrafuge. The EDIM test power input cable connector was wired to conform to these additional cables. At the completion of the acceleration environmental tests, the EDIM test power input cable connector was not changed back to its original configuration. Therefore, at the resumption of the post-acceleration functional test using the regular cable configuration between the EDIM and Test Panel, the voltage regulator was damaged. The EDIM power input cable connector was then rewired to its original configuration as required by the

schematic in reference (1). The voltage regulator was replaced in the EDIM and additional tests were added and performed to ensure the EDIM would meet the requirements for flight application.

2. Test Summary

The EDIM passed all environmental tests to which it was subjected. A comparison of data of all the applied tests indicated the EDIM had no degradation. Visual examination of the printed circuit board and components, after completion of qualification tests , showed no evidence of component deterioration. Particular attention was given to the tantalum capacitors. No evidence of electrolyte leakage was noted.

Also, the EDIM passed the EMI requirements during the susceptibility tests. Special "spike" tests, which deviated from the applicable MIL-SPEC, were performed. These tests could make the EDIM "fire" but this "fire" condition is not considered significant to the application of the EDIM on the Scout vehicle because "spike" generating devices such as relays, switches, etc., are not used in the power input lines. Enclosure (3) contains results of the EMI tests.

VI. CONCLUSION AND RECOMMENDATION

The EDIM has met and satisfactorily passed all requirements of the test program. However, one caution should be noted relative to transients on the power lines of the EDIM. If in any future configuration a transient-causing device is connected into the EDIM power lines, evaluation and testing should be performed to assure that the device will not cause spurious EDIM firings.

The results of the test program have shown the EDIM to have no degradation of performance or deterioration of components during the testing. In addition, the EDIM operation met requirements through all environmental and EMI tests. Therefore, the EDIM has demonstrated acceptability for flight application on the Scout vehicle.

TEST INFORMATION RELEASE

DISTRIBUTION			TR NO. 23TRA0244	RELEASE NO. 2-45202/5R-2
			PAGE 1 OF 6	DATE 11 June 1975
			MODEL SCOUT	
TESTED BY Wayne Berry	TR ☐ COMPLETE ☐ INCOMPLETE		APPROVED BY [illegible]	
TITLE OF TEST	QUALIFICATION AND S^{2}ET OF SCOUT 4th STAGE ELECTRONIC DELAY IGNITION MODULE (EDIM)			

Encl: (1) 23TRA0244
(2) 23QTFR-008

DATA OR RESULTS:

1.0 Test Requirements

This test was performed to qualify the test specimen to vibration, mechanical shock, high/low temperature, temperature/altitude, acceleration and humidity environments which are more severe than anticipated for Scout Vehicle.

2.0 Test Procedure

The following tests were performed per enclosure (1), except that 23QTFR-008 (enclosure (2)) was performed between the acceleration test and the S^{2}ET vibration and shock. During post-acceleration functional, it was noted that the regulated voltage read 4.4 VDC; it should have read 9.3 VDC. Investigation revealed the specimen had been inadvertently connected wrong. QTFR 23-QTFR-008 was written and troubleshooting procedure was initiated. After completion of the QTFR, normal testing continued, except there were ten (10) cycles of S^{2}ET instead of eight (8). Order of test:

(1) Pre-environmental
(2) High temperature/low temperature (qual)
(3) Temperature Shock (qual)
(4) Temperature/altitude (qual)
(5) Vibration (qual)
(6) Mechanical Shock (qual)
(7) Acceleration (qual)
(8) QTFR #23QTFR-008
(9) Vibration & Shock (S^{2}ET)
(10) Humidity
(11) Post-environmental

The test specimen was operated and monitored per enclosure (1) for each of the environmental conditions listed above.

3.0 Test

3.1 Test Specimen

The test specimen was a Scout 4th Stage Electronic Delay Ignition Module (EDIM), P/N 23-004349-1.

3.2 Test Facilities

Test equipment utilized to perform the above mentioned tests is presented in Table 3.2, below:

Table 3.2 - Test Facilities

Item No.	Equipment	Manufacturer	Model
1	Sine/Random Control	Ling	SRC-503
2	Power Amplifier	Ling	PP60/100
3	Electrodynamic Exciter	Ling	335
4	Accelerometer	Endevco	2221D
5	Accelerometer Amplifier	Endevco	2711A
6	Magnetic Tape Recorder	CEC	VR2800
7	Oscillograph	CEC	S-123
8	Rotary Accelerator	Schaevitz	--
9	Temperature/Altitude Chamber	American Research	--
10	Humidity Chamber	Tenney	27-0200
11	Real Time Analyzer	Spectral	301D

3 Test Set UP

Typical set-ups for the tests in paragraph 2.0 are shown in Figures 3.1 through 3.6.

3.4 Test Results

No anomalies were noted due to environmental testing.

4.0 Test Data

The random vibration input was analyzed using the Real Time Analyzer and is presented herein as g^2/HZ plots for Qual and S-ET. The Real Time Analyzer settings were as follows:

Analyzer Range - 15 Hz bandwidth and 5K Hz upper limit
Number of ensembles - 64.

The mechanical shock was recorded on memo-scope and a Polaroid picture, and is presented in Figures 4.1 and 4.2. The squib spike voltage was recorded on film and is presented in Figure 4.3. The data pertaining to the operation of the test specimen is recorded in the data sheets of reference (a) and is presented herein.

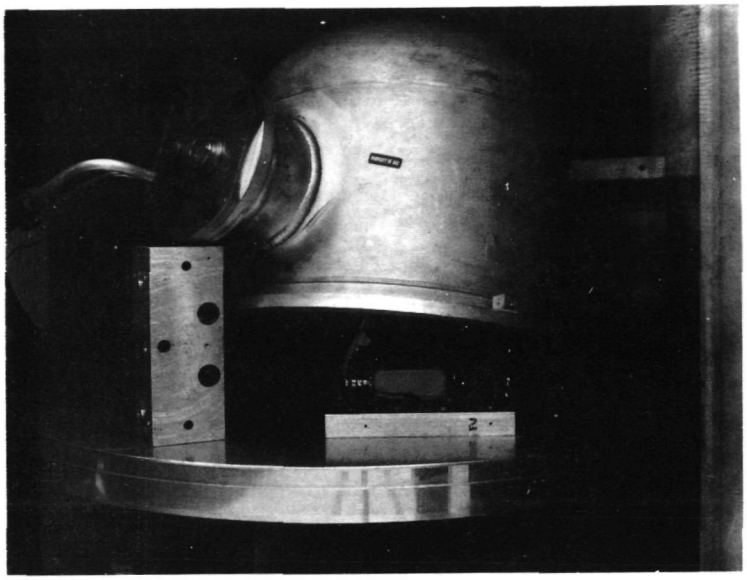


Figure 3.1 - Typical Temperature/Altitude and Temperature Set-Up

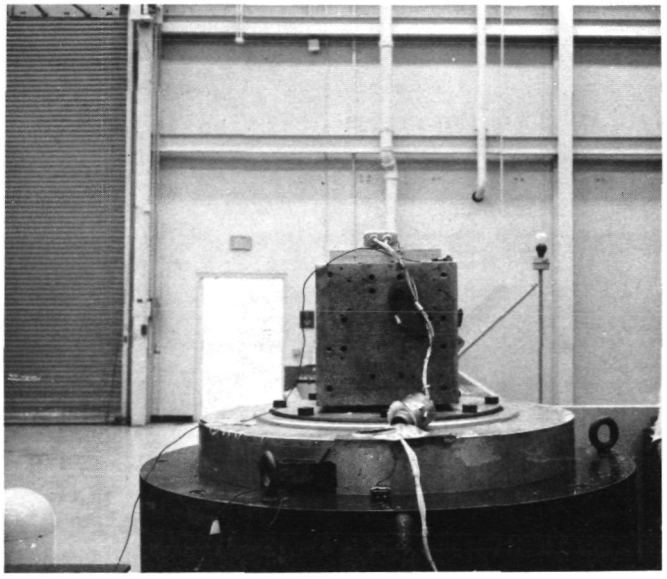


Figure 3.2 - Typical Vibration and Mechanical Shock in the "Y" Axis

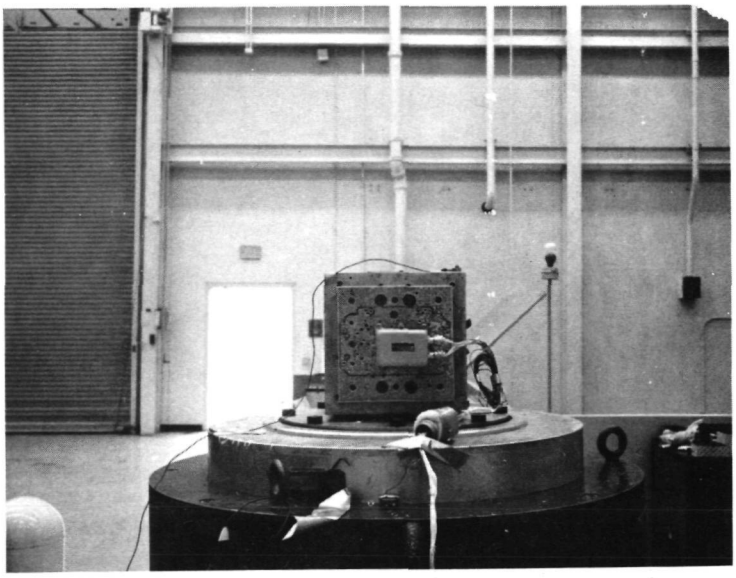


Figure 3.3 - Typical Vibration and Mechanical Shock in the "Z" Axis

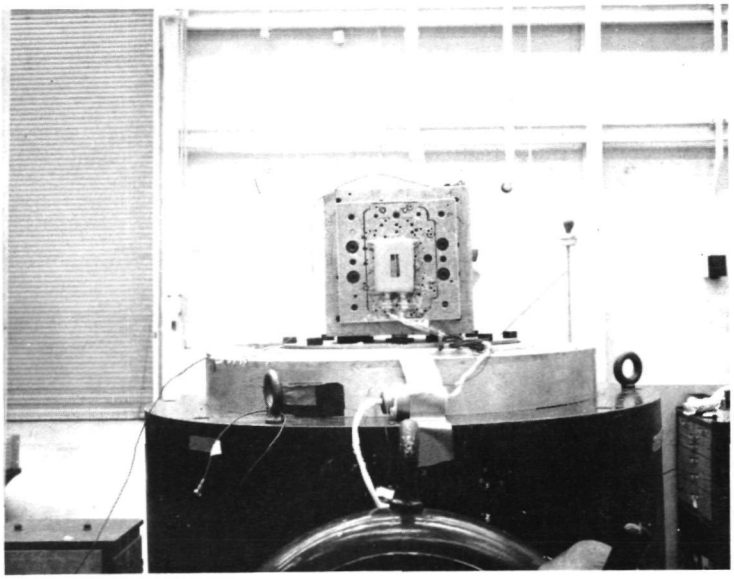


Figure 3.4 - Typical Vibration and Mechanical Shock in the "X" Axis

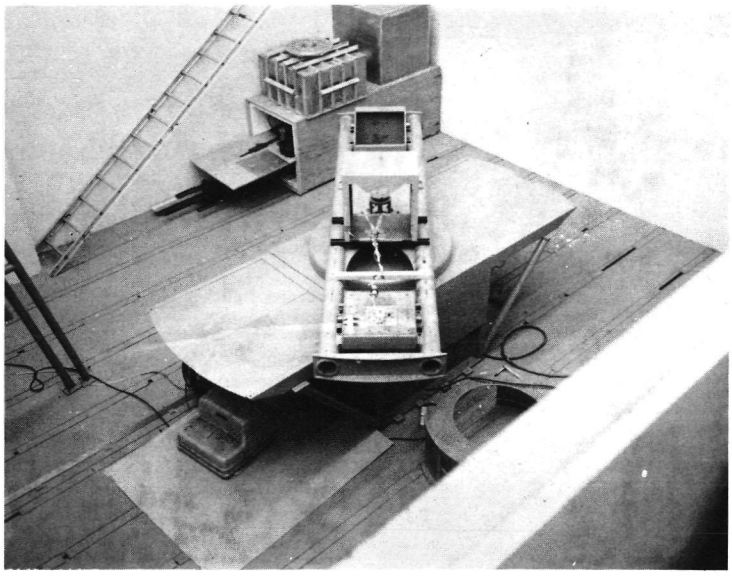


Figure 3.5 - Typical Acceleration Set-Up

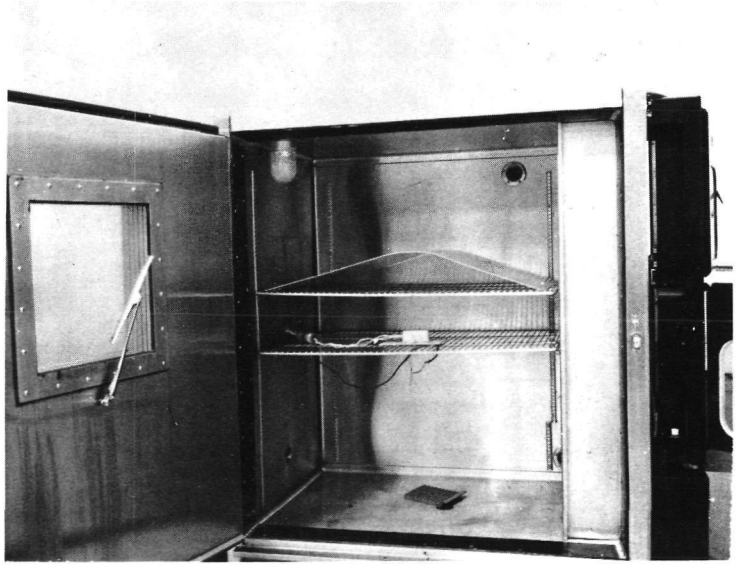


Figure 3.6 - Typical Humidity Set-Up

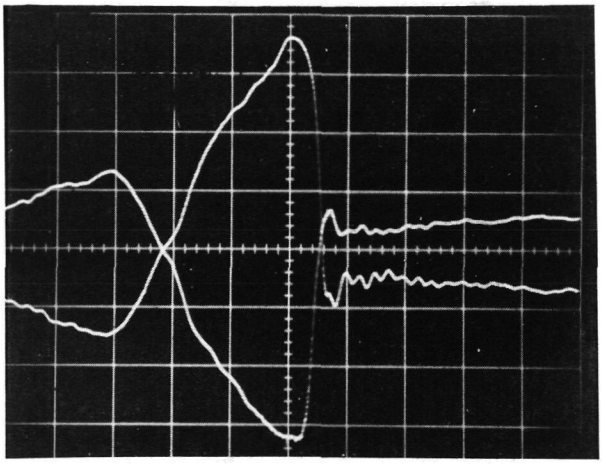


Figure 4.1 - Mechanical Shock Qual
Vert - 20 g/cm
Horiz - 2 ms/cm

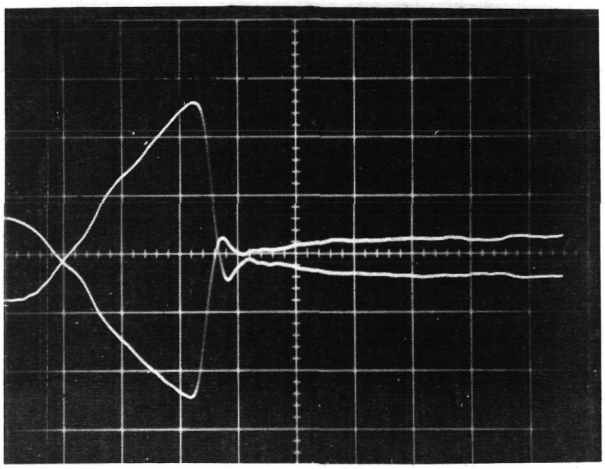


Figure 4.2 - Mechanical Shock S^2ET
Vert - 20 g/cm
Horiz - 2 ms/cm

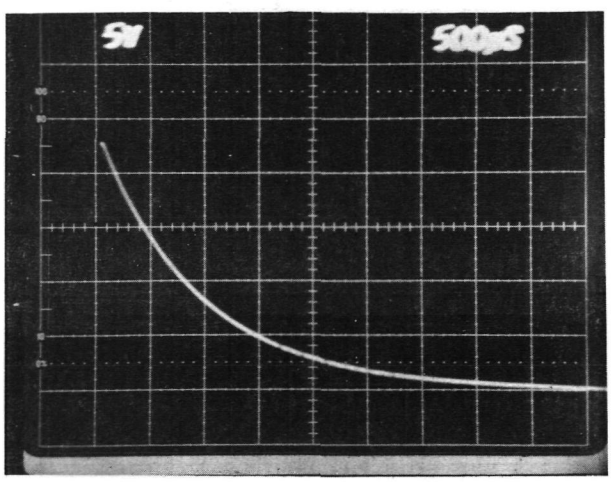
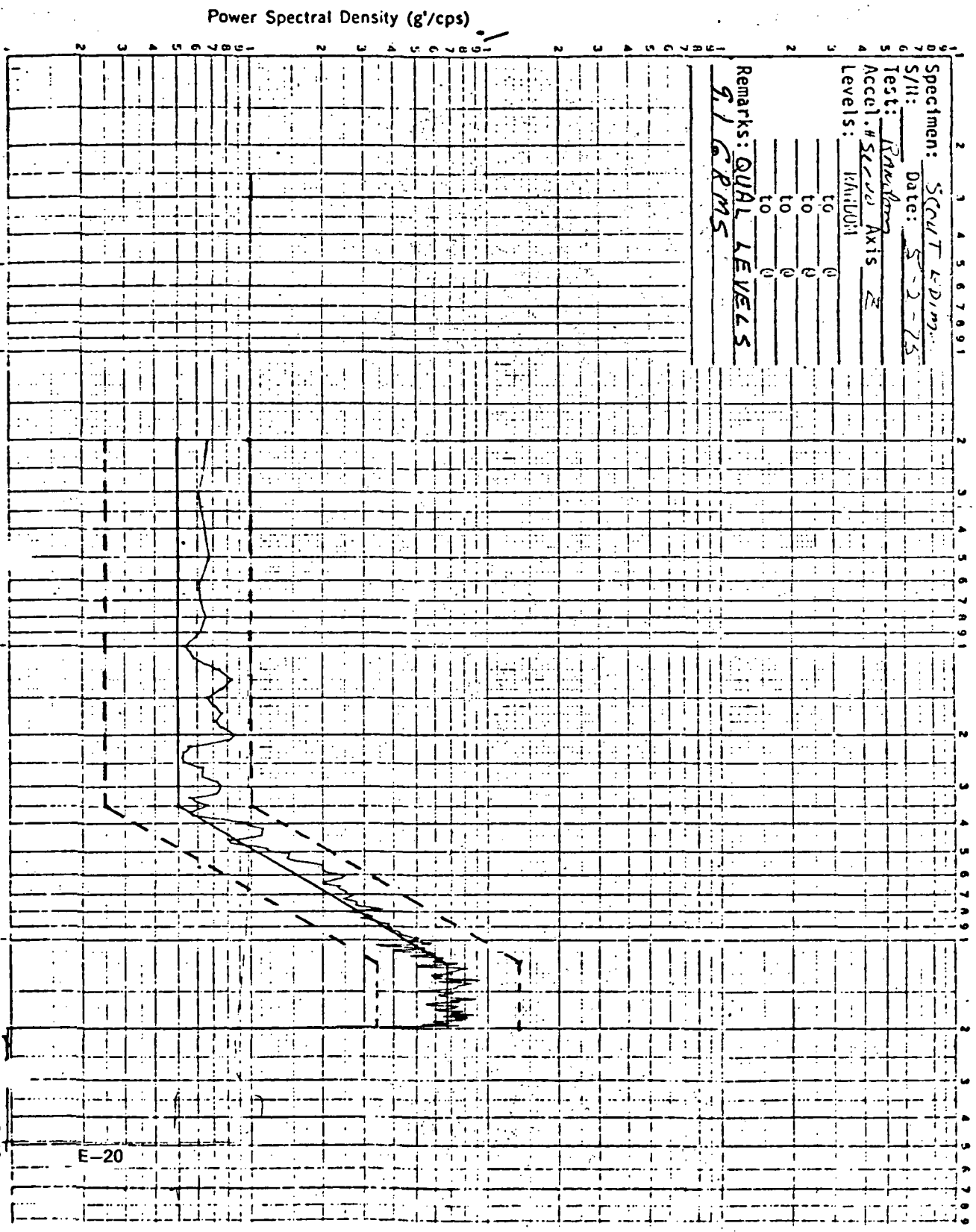
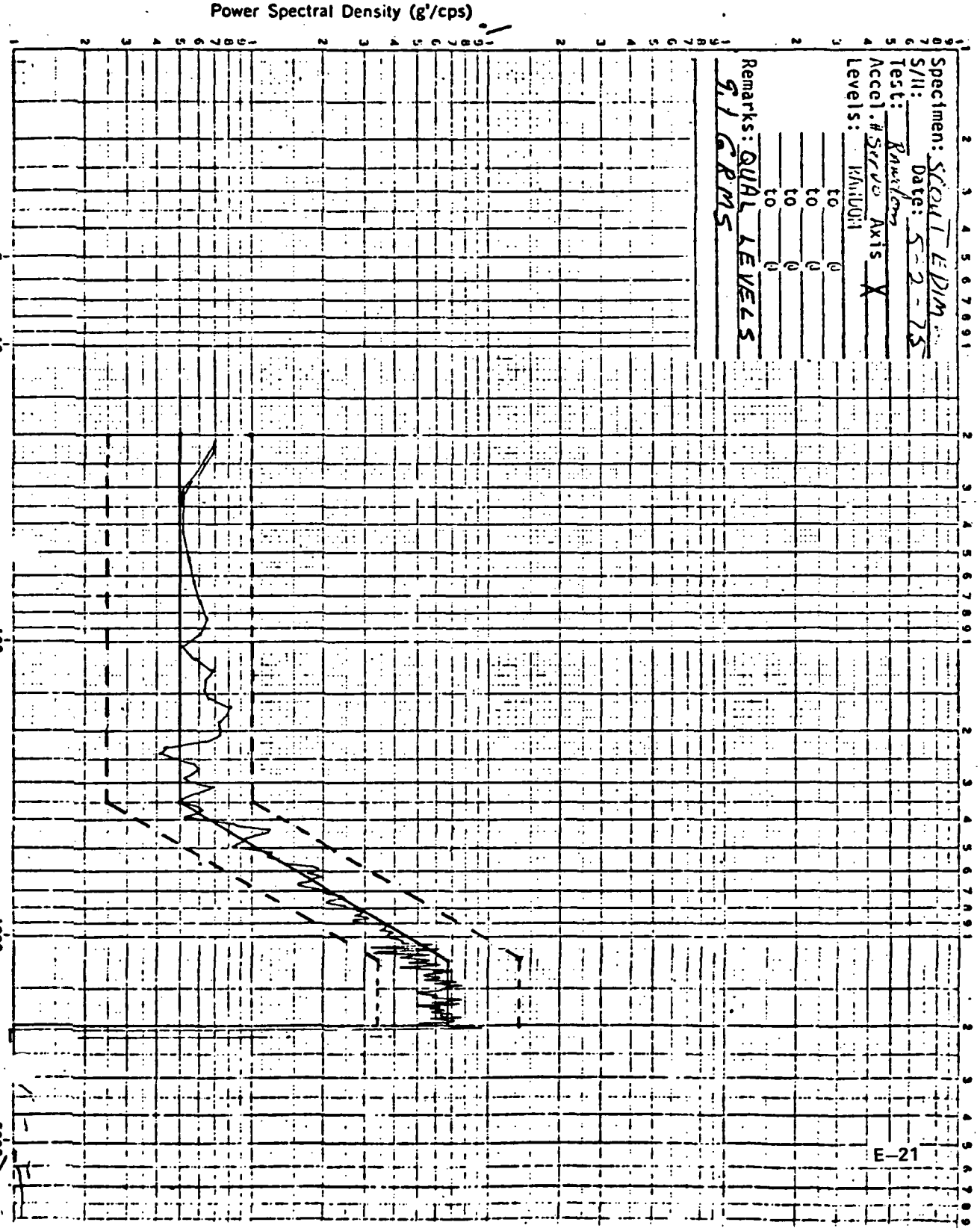
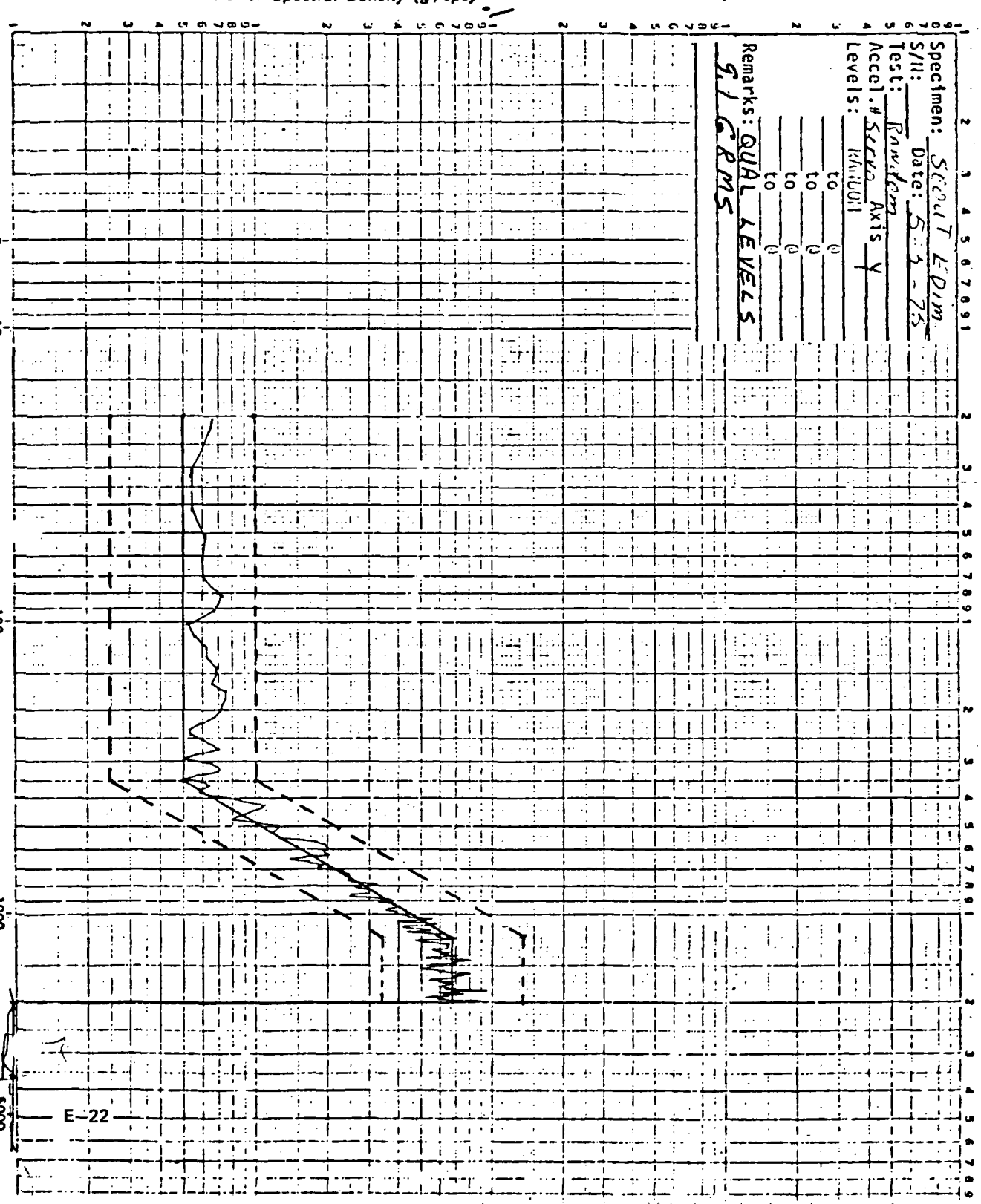
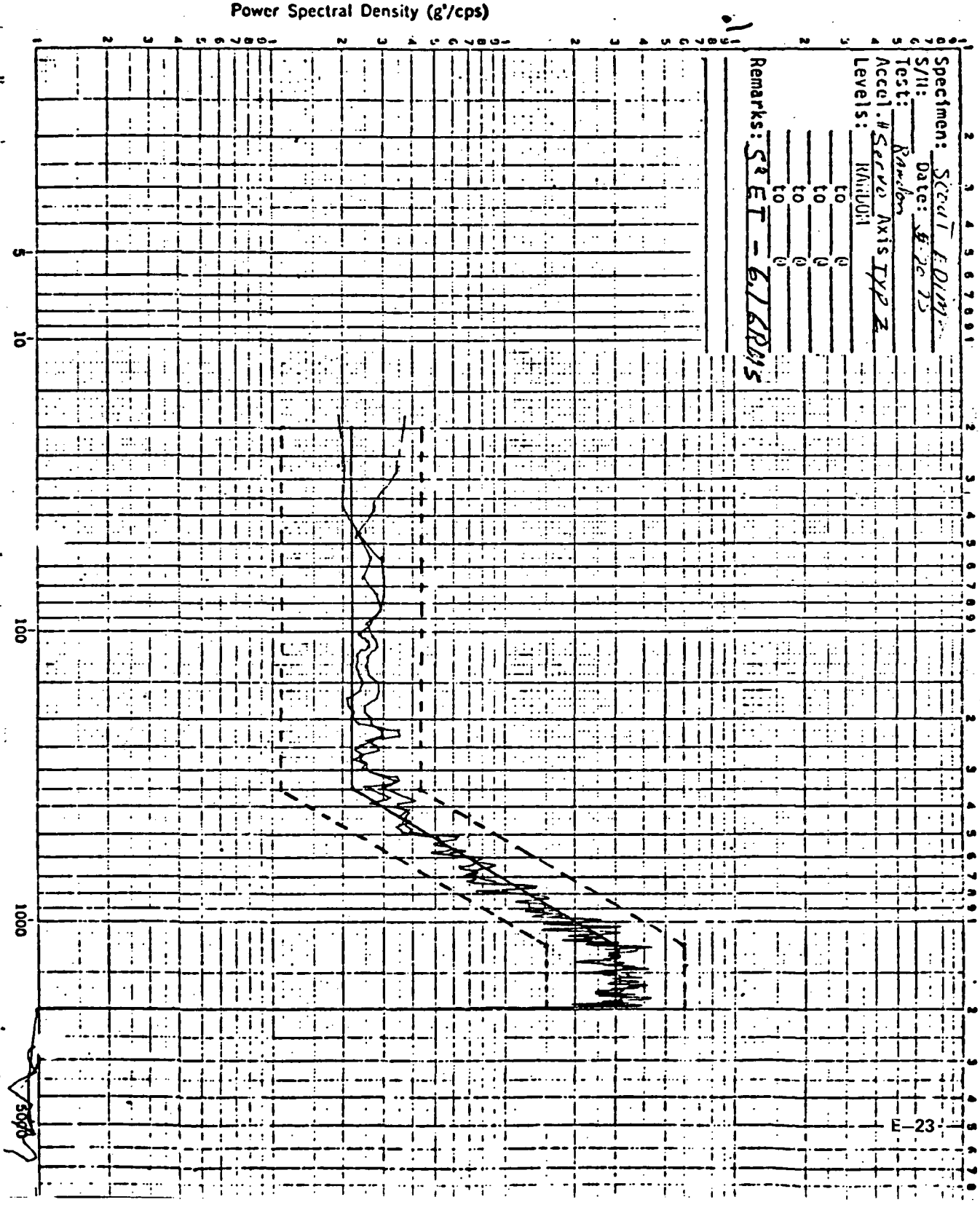


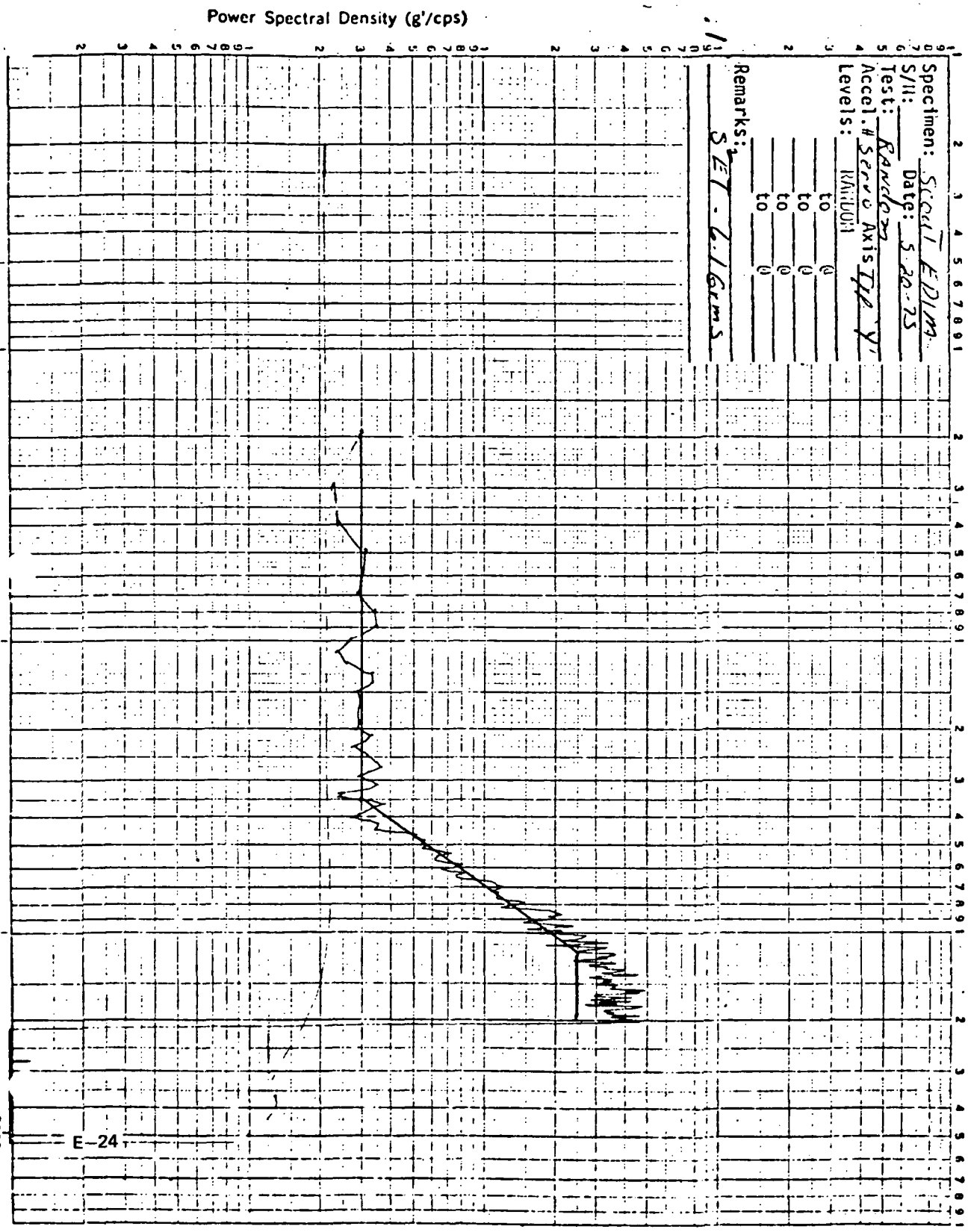
Figure 4.3 - Typical Squib Voltage Spike
Vert - 5 V/cm
Horiz - 500 ns/cm

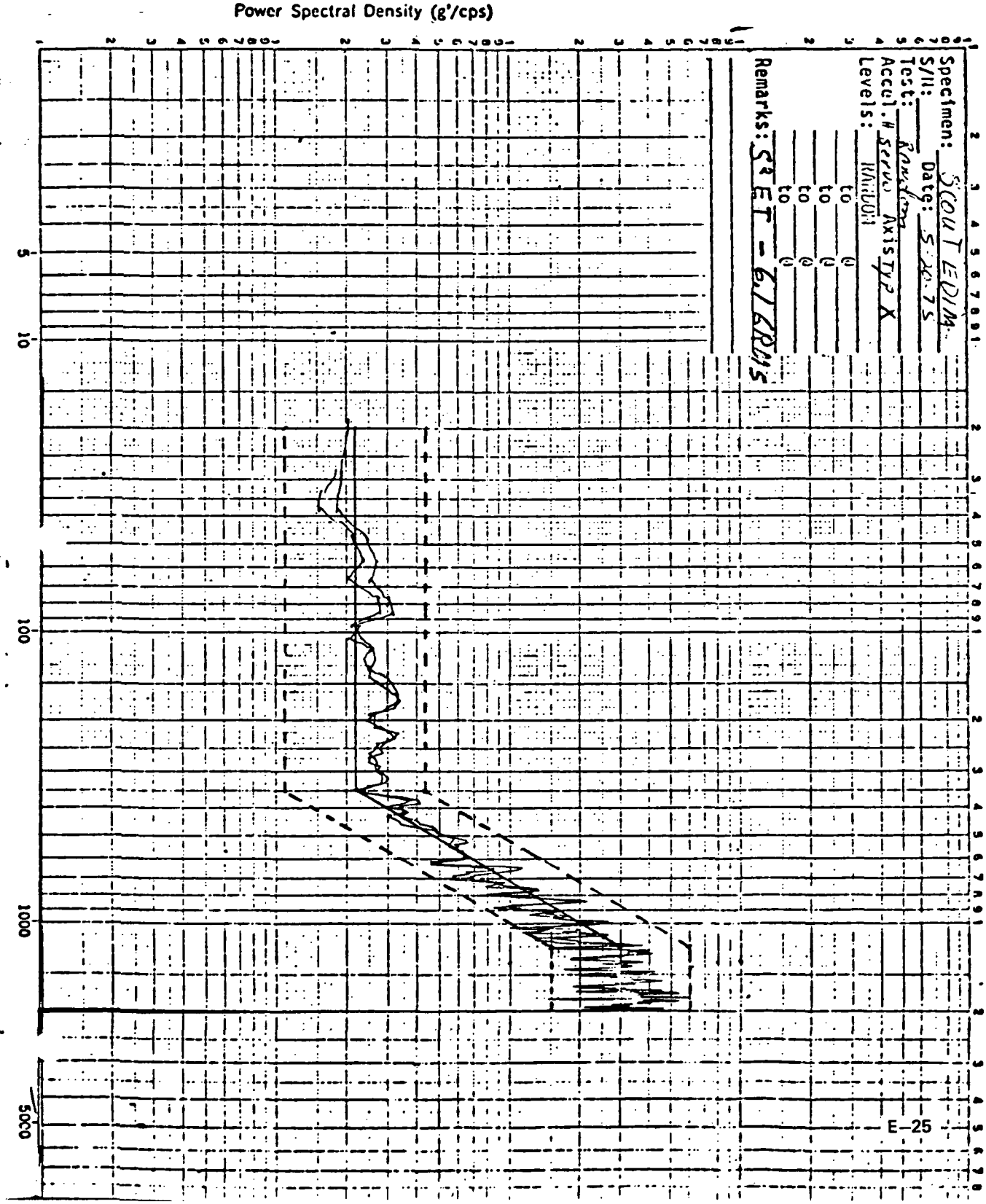

Power Spectral Density (g²/cps)
Specimen: SCOUT ADAPTER
S/N:
Date: 5-2-75
Test: Random
Accel. # Sweep Axis Z
Levels: MAXIMUM
to @
to @
to @
to @
Remarks: QUAL LEVELS
9.1 GRMS
5
10
100
1000
5000


Power Spectral Density (g²/cps)
Specimen: SCOUT EDM
S/N:
Test: Random
Accel. # Servo Axis X
Levels: RANDOM
to
to
to
to
to
Remarks: QUAL LEVELS
9.1 GRMS
5
10
100
1000
5000


Power Spectral Density (g²/cps)
Specimen: Scout LEM
S/N:
Date: 5-2-75
Test: Random
Accel.# Servo Axis Y
Levels: RANDOM
to @
to @
to @
to @
Remarks: QUAL LEVELS
9.1 GRMS
5
10
100
1000
5000


Power Spectral Density (g²/cps)
Specimen: Scout Dummy
S/N:
Test: Random
Accel. # Servo Axis Typ Z
Levels: Random
to
to
to
to
to
Remarks: SET - 6.1 GRMS
5
10
100
1000
3000


Power Spectral Density (g'/cps)
Specimen: SCOUT EDM
S/N: 1
Date: 5-20-75
Test: Random
Accel. # Servo Axis Typ Y
Levels: RANDOM
to @
to @
to @
to @
Remarks:
SET - 6.16 grms
5
10
100
1000
5000


Power Spectral Density (g²/cps)
Specimen: SCOUT EDM
S/N: Date: 5 DEC 75
Test: Random
Accel. # Servo Axis Type X
Levels: Number
to
to
to
to
to
Remarks: SET - 6 LEADS
5
10
100
1000
5000

TR. NO. 23-TRA-02-[illegible]

PAGE 1 OF 63 (67)

ENGINEERING TEST LABORATORY TEST REQUEST c 40758

TITLE	DATE	CHARGE NO.
Environmental Qualification Test for Scout 4th Stage Electronic Delay Ignition Module (EDIM) P/N 23-00434-1	4-10-75	3284-CV-1220
	MODEL: Scout	REQ. BY: J.D. Clark / GROUP: 2-[illegible]232
	DATE DATA REQ.	MANHOURS: STR. T.L. / EST. / ACTUAL

PROJECT TEST ENGINEER: N/A	APPROVAL: ORIG. GRP. QD Clark 4-10-75	WITNESSES	YES	NO	STR. T.L. HRLY.	
UNIT ASSIGNMENT: N/A	PROJECT: 4/14/75	CUSTOMER	X			N/A
LAB. OR DEPT. RESP. FOR TEST: 2-45202	LABORATORY: 4/11/75	COMPANY	X			
REFERENCE					TOTAL	

PURPOSE & DESCRIPTION OF TEST

1.0 PURPOSE, OBJECTIVE, SCOPE

1.1 Purpose

The purpose of this environmental qualification test is to qualify the Electronic Delay Ignition Module (EDIM) design for Scout flight application by successful execution of the functional requirements during and after exposure to the Scout Standard Design Qualification Environments specified herein.

1.2 Objective

The objective of this test is to qualify the test specimen to the following environments/tests.

a) High Temperature/Low Temperature
b) Temperature Shock
c) High Temperature-Altitude
d) Vibration/Mechanical Shock
e) Acceleration
f) Humidity
g) Environmental Cyclic Life (S^2ET Vibration/Shock)

Revision A: Pages 15 and data pages 23-63 reflect changes made during testing. No retest required.

REVISION A APPROVALS:

[illegible] 6/3/75

J. Martinez 6/6/75

[illegible] 6/6/75

The level of these environments as specified herein exceeds those levels anticipated for the intended Scout application of the EDIM. In addition to verification of the test specimen to the qualification envornments (a through f above) the specimen will be subjected to 8 Scout Standard Environmental Test (S^2ET) Acceptance Level vibration/shock cycles

TEST REQUEST DISTRIBUTION

See attached distribution list

REPORT DISTRIBUTION

6/6/75

The completion of the eight S^2ET acceptance level vibration/shock environments in combination with the qualification environment exposure will qualify the design for the required level of Environmental Cyclic Life.

1.3 Scope

The scope of this test is to establish a level of confidence in the design and construction of the test specimen.

1.4 Schedule

The schedule of test shall be coordinated with the Scout Program Office.

2.0 TEST SPECIMEN

The test specimen is the Scout 4th Stage Electronic Delay Ignition Module, P/N 23-004349-1, Qual Unit.

3.0 TEST FACILITY

This qualification test shall be conducted in the Environmental Test Laboratory, Unit 2-45202. The following test equipment or equivalent shall be provided.

3.1 Test Equipment

(a)	Vibration Exciter System	Ling Model 335
(b)	Storage Oscilloscope	
(c)	Megohmmeter	Freed Model 1020B
(d)	Temperature-Altitude Chamber	American Research Corporation
(e)	Power Supply 0-35 Volt	
(f)	Rotary Accelerometer	Schaevitz B-12
(g)	Test Panel (Per Figure I, Fabricated by Lab)	
(h)	Oscilloscope Camera	
(i)	Electronic Counter	
(j)	Digital Voltmeter	
(k)	Recorders	CEC or Sanborn (Mag. Tape & Oscillograph)

(l) Accelerometer — Endevco Model 2221

(m) Humidity Chamber

(n) Stop Watch

3.2 Test Conditions

Tolerances on test conditions shall be as follows:

(a) Time: Plus or minus 10 percent (except when stopwatch is used)

(b) Random (rms) Vibration Amplitude: ±10 percent overall

(c) Mechanical Shock: ±10 percent

(d) Accelerometer: ±10 percent

(e) Temperature: Laboratory Ambient, $72^{\circ}F \pm 10^{\circ}F$

Test Condition, $\pm 5^{\circ}F$ as measured on specimen at baseplate

(f) Voltage: ±1 percent

(g) Humidity: 95% ± 5% Relative Humidity

(h) Altitude: ±5 percent

If any of these test conditions cannot be obtained during the testing, the actual test condition shall be specified on the data sheets.

3.3 Personnel Requirements

3.3.1 Test Director - The Test Director shall be designated by the Environmental Test Laboratory.

3.3.2 Test Monitor - The Test Monitor shall be assigned by Reliability Engineering and will be responsible for reviewing and approving all test set-ups and coordination.

3.4 Test Witness

Government witness of test is required.

3.5 Data Recording

The data obtained during performance of this test shall be recorded on data sheets provided herein.

4.0 TEST PROCEDURE

The test specimens shall be subjected to the test sequence given below while connected as shown in Figure I.

A. Pre-Environmental Tasks

1. Visual Inspection
2. Insulation Resistance Check
3. Functional Performance Verification

B. Environmental Performance (Qualification Levels)

1. High Temperature/Low Temperature
2. Temperature Shock
3. High Temperature-Altitude
4. Vibration/Mechanical Shock
5. Acceleration
6. Humidity
7. Cyclic Life - S^2ET Acceptance Level Vibration/Mechanical Shock

NOTE: Application of environments shall be in any order except Cyclic Life exposure shall occur following successful exposure to the qualification environments listed in 1 through 6 above.

C. Post-Environmental Tasks

1. Visual Inspection
2. Insulation Resistance Check
3. Functional Performance Test

4.1 Pre-Environmental Tests

4.1.1 Visual Inspection and Weighing - Upon receipt of the test specimen, the environmental laboratory shall visually inspect the test item to dwg no. 23-00434-1 for any physical defects. Measure and record weight.

4.1.2 Insulation/Resistance Check - Using a megohmmeter, set to 500 VDC, verify insulation resistance between each pin and case for each connector. Record values obtained on the data sheet. See Figure 1 for schematic.

4.1.3 Functional Performance Test - During the performance of pre-environment, environment and post-environment testing the following two operational tests will be required repetitively and are given here in detail for convenience.

Test A - Delay Timing Cycle (DTC) Test

1) Adjust input voltage to 30 or 35 volts (as required).
2) Verify discharge jumper (J1-2 to J2-2) has been in place for 30 seconds (minimum).
3) Verify ignition charge voltage has reached a steady-state value.
4) Remove discharge jumper.
5) Turn power switch to "off" position and simultaneously start stopwatch.
6) After power switch has been in "off" position for $1.5\ ^{+0.2}_{-0.0}$ seconds, transfer the start switch to "Start" position.

NOTE: Stopwatch low side (-0.0 seconds) tolerance is critical. However, the high side (+0.2 seconds) tolerance is not critical from the standpoint that values greater than 1.5 +0.2 seconds could cause an apparent but "false" failure symptom. Therefore, the high side tolerance may be allowed to exceed 0.2 seconds so long as the resulting value does not adversely affect performance indications. Experience has found that high side tolerance values of 0.2 to 0.3 seconds are reasonable with a stopwatch for this measurement.

7) Record delay time (T_d) indication on electronic counter.

8) Obtain output voltage spike photograph (as required).

NOTE: In the event that a required photograph is missed due to test equipment problems or operator error, another photograph shall be obtained without resubjecting the specimen to applicable environment(s). Where no photograph is required, verify spike output on scope visually.

Test B - Loss of Regulation (LOR) Time Test

1) Adjust input voltage to 30 or 35 volts (as required).

2) Verify ignition charge voltage has reached a steady state value.

3) Simultaneously start stopwatch and turn power off.

4) Monitor regulator output voltage on digital voltmeter and stop the stopwatch immediately when regulated voltage begins to decrease at LOR.

NOTE: The digital voltmeter sample rate should be at maximum rate setting for this test.

5) Record elapsed time to LOR.

4.1.4 Pre and Post-Environmental Operational Test - Prior to the start of environmental testing perform Test A and Test B of paragraph 4.1.3 as specified below. After completion of environmental testing, perform this test again.

Test A at 30 volts - Output Voltage Spike Photograph required.

Test B at 30 volts

Test A at 35 volts - Output Voltage Spike Photograph required.

Test B at 35 volts

Test A at 30 volts - Select test panel switch marked "Load Select" to "fuse" position. Determine capability to open $\frac{1}{4}$ amp fuse.

Test A at 35 volts - Select test panel switch marked "Safe/Arm Relay" to "ON" position. Measure voltage at "Voltage Monitor" jacks. Record in charge voltage blank of data sheet. Determine that $\frac{1}{4}$ amp fuse does not open.

4.2 Scout Standard Environmental Tests - Design Qualification

The qualification level environments specified in this section (paragraphs 4.2.3 through 4.2.8) shall be applied in any order. The Environmental Cyclic Life Test (paragraph 4.2.9) shall be performed after completion of the qualification level environments.

4.2.1 Monitoring and Performance Requirements During Environmental Application - During environmental application the following points shall be monitored:

Channel No.	Connector Pins	Name of Output	Approximate Nominal Voltage Levels
1	J1-1	Ignition Charge Voltage	30 VDC
2	J2-6	Squib Voltage	0V, 20V Spike
3*	J1-4	Regulator Output	9 VDC
4	J1-3	Input Voltage	30VDC, 35VDC

*NOTE: Instrumentation impedance at this channel shall be 200K ohms or greater to avoid excessive effect on measured LCR time and delay time.

4.2.2 Operational Test Between Environmental Tests - Upon completion of a single environmental test (i.e., High Temperature/Low Temperature, Temperature Shock, Vibration/Mechanical Shock, etc.) and prior to the start of the next environmental test, the specimen shall be returned to ambient conditions and subjected to the operational test of paragraph 4.1.3 Test A (at 30V, output voltage spike photograph required) and Test B (at 30V).

4.2.3 High Temperature/Low Temperature - The test specimen, with power off shall be placed in a test chamber wherein the temperature is maintained at 160°F. The specimen shall be kept in this 160°F environment for four hours or until specimen temperature as measured at baseplate is stabilized**, whichever occurs first. After four hours of exposure to 160°F or at stabilization, apply 30V power and perform the following functional test with the specimen remaining at 160°F. (Reference paragraph 4.1.3 Test A and Test B)

**Stabilization is defined as three successive readings five minutes apart within ±5°F of the specified test temperature.

a) Perform Test A at 30V Input

Monitor and record the following during the test:

1) Channels 1 through 4

2) Obtain photograph of Channel 2 output spike.

3) Delay Time

b) Perform Test B at 30V Input

Monitor and record the following during the test:

1) Channels 1 through 4

2) LOR Time

c) Perform Test A at 35V Input

Monitor and record the following during the test:

1) Channels 1 through 4

2) Obtain photograph of Channel 2 output spike.

3) Delay Time

d) Perform Test B at 35V Input

Monitor and record the following during the test:

1) Channels 1 through 4

2) LOR Time

Remove power.

Remove the specimen from the high temperature chamber and place in another temperature chamber maintained at $0^{\circ}F$. The specimen shall be kept in this $0^{\circ}F$ environment for four hours or until stabilized, whichever occurs first. After four hours of exposure to $0^{\circ}F$ or at stabilization, apply 30V power and perform the following functional test with the specimen remaining at $0^{\circ}F$.

a) Test A at 30V, same as a) at $160^{\circ}F$
b) Test B at 30V, same as b) at $160^{\circ}F$
c) Test A at 35V, same as c) at $160^{\circ}F$
d) Test B at 35V, same as d) at $160^{\circ}F$

Remove power, allow the specimen to attain ambient temperature then perform a functional test per paragraph 4.2.2.

4.2.4 Temperature Shock - The test specimen with power off, shall be placed in a test chamber wherein the temperature is maintained at $0^{\circ}F$. The specimen shall be subjected to this environment for a period of one hour or until the temperature of the component becomes stabilized, whichever is longer (Stabilization is defined as 3 successive readings five minutes apart within $0^{\circ} \pm 5^{\circ}F$).

After stabilization has been achieved the specimen shall be transferred (transfer time shall be one minute or less) to a chamber wherein the internal temperature is maintained at $160^{\circ}F$. The specimen shall be subjected to this temperature for one hour or until the temperature becomes stabilized, whichever is longer. This constitutes the first temperature shock.

Transfer the specimen back into the low temperature chamber (transfer time shall be one minute or less) and again maintain the low temperature exposure for a period of one hour or until the specimen temperature becomes stabilized, whichever is longer. This step shall be construed as the second temperature shock and the first temperature shock cycle.

Two additional temperature shock cycles shall then be implemented, they being identical to the first temperature shock cycle. During the final high temperature exposure the specimen shall be operated per paragraph 4.2.4.1 below. At the conclusion of three temperature shock cycles (six temperature shocks) the component shall be removed from the chamber, allowed to reach ambient temperature and then subjected to the Operational test of paragraph 4.2.2.

4.2.4.1 Operational Test for Temperature Shock - The specimen shall be operated per paragraph 4.2.2 at ambient temperature prior to and subsequent to environmental exposure. Power shall be removed prior to placing the specimen into the temperature chamber. During the final high temperature exposure (corresponding with the fifth temperature shock) and immediately after being placed in the high temperature chamber, power shall be reapplied and the specimen operated per paragraph 4.1.3, Tests A and B at 30V then Tests A and B at 35V. After completion of the 35V test reduce the power to 30V and continued to monitor the specimen for the full period of high temperature exposure. Just before placement of the specimen back into the low temperature chamber, remove power.

4.2.5. High Temperature-Altitude - The specimen with power off shall be placed in a test chamber. The internal temperature of the chamber shall be increased and stabilized at 160°F. After stabilization* the internal pressure of the chamber shall be decreased to simulate 200,000 feet altitude (i.e., 0.148 mm of Hg) within five minutes. This simulated altitude shall be maintained for a period of ten minutes minimum. Initiate environmental functional test per paragraph 4.2.5.1 below at the beginning of the ten minutes altitude period. After completing the altitude exposure the internal chamber pressure shall be increased to laboratory ambient. This constitutes one complete temperature-altitude cycle. The specimen shall be subjected to two such cycles, at the conclusion of which the component shall be removed from the chamber, returned to laboratory ambient conditions and operated per paragraph 4.2.5.1 below.

*Stabilization is defined as three successive readings five minutes apart within ±5°F of the specified test temperature.

4.2.5.1 Operational Test for Temperature-Altitude - The specimen shall be operated per paragraph 4.2.2 at ambient temperature prior and subsequent to environmental exposure. Power at 30V shall be applied immediately after reaching the simulated 200,000 feet altitude. During both of the ten minute temperature-altitude exposures perform an operational test per paragraph 4.1.3 Tests A and B at 30V then Tests A and B at 35V. After the 35V test is complete, reduce the applied voltage to 30V and monitor the specimen until the end of environmental exposure. Re-establish ambient conditions prior to performance of the paragraph 4.2.2 operational test after temperature-altitude exposure.

4.2.6 Vibration/Mechanical Shock

4.2.6.1 General

A. The test specimen shall be rigidly attached to the exciter and shall be functioning in accordance with the provisions of this test request during the entire test period.

B. The test specimen shall be performance evaluated during vibration/mechanical shock test.

C. The magnitude of applied vibration and mechanical shock shall be monitored on the test fixture near the specimen mounting points.

D. The vibration and mechanical shock shall be applied sequentially in each axis prior to changing to the next axis for test.

4.2.6.2 Qualification Level Vibration Environmental Test - Vibration test shall consist of performing the test sequence specified in Table A in each of three orthogonal axes. The axes are defined in Figure II.

TABLE A

VIBRATION TEST LEVEL

TEST DURATION PER AXIS (SECONDS)	FREQUENCY RANGE (Hz) Lower	Upper	ACCELERATION RANDOM (G RMS) Ref.
80	20	2000	9.1

Qualification Test Spectra
Per Figure III

4.2.6.3 Mechanical Shock Environmental Test

A. The test specimen shall be subjected to impact shocks; each pulse shape shall be terminal sawtooth having a duration α 6 $\pm$ 1 milliseconds.

B. There shall be 3 shocks of 75 g's applied in each of the two directions for each of the three mutually perpendicular axes (18 shocks total).

C. A poloroid photograph or equivalent shall be made of the first pulse in each direction in each axis of shock applied to each specimen. (It shall not be necessary to photograph every shock pulse provided the first ones are within tolerances or unless the test set-up is changed.)

4.2.6.4 Performance Requirements During Vibration/Mechanical Shock - Prior to the start of environmental testing, an operational test per paragraph 4.2.2 shall have been completed. During environmental test in each axis, the specimen shall be monitored per paragraph 4.2.1 and operated per paragraph 4.1.3 A at 30V (Output Voltage Spike Photograph required). Between axes, operate the specimen per paragraph 4.1.3 B at 30V. After completion of the Vibration/Mechanical Shock Test, perform the operational test of paragraph 4.2.2.

4.2.7 Acceleration

4.2.7.1 General

A. The test specimen shall be rigidly attached to the centrifuge.

B. The test specimen shall be mounted and oriented so as to receive the specified acceleration along the axes defined in Figure II .

C. The specified acceleration applies to the geometric center of the specimen.

D. The centrifuge arm (as measured to the geometric center of the specimen) shall be at least five times the dimension of the specimen (measured along the arm).

E. The test specimen shall be operated and evaluated during the acceleration test.

F. The specified acceleration level shall be applied sequentially in each direction in each axis.

4.2.7.2 Acceleration - Apply 33.5 g's acceleration in each direction along each orthogonal axis for two minutes each application. Perform operation and monitoring as specified in paragraph 4.2.7.3 below.

4.2.7.3 Performance Requirements During Acceleration - Prior to the start of environmental testing, an operational test per paragraph 4.2.2 shall have been completed. During each acceleration application the specimen shall be monitored per paragraph 4.2.1 and operated per paragraph 4.1.3A at 30V (Output Voltage Spike Photograph required). Between acceleration applications, operate the specimen per paragraph 4.1.3B at 30V. After completion of the Acceleration Test, perform the operational test of paragraph 4.2.2.

4.2.8 Humidity

4.2.8.1 General - The specimen shall not be operated while within the humidity chamber.

4.2.8.2 Humidity Environmental Test - The timer shall be placed in a humidit test chamber where the relative humidity is 95% at ambient temperature after which the temperature of the chamber shall be increased to 120°F within a period of two hours. The relative humidity throughout the environmental test shall be maintained at 95%. Maintain 120°F temperature for a period of six hours after which the temperature shall be reduced to 68°F over a period of 16 hours. The end of the 16-hour period shall constitute one humidity cycle. Beginning at the 68°F temperature point, another cycle shall be completed and then another for a total of three complete humidity cycles. At the completion of three humidity cycles, remove the specimen from the environmental chamber and wipe away any excess moisture accumulated during humidity testing. At this time, perform the functional test per paragraph 4.2.8.3 below.

4.2.8.3 Pre and Post-Humidity Operational Test - Prior and subsequent to the humidity test operate the specimen per paragraph 4.2.2.

4.2.9 Environmental Cycle Life

4.2.9.1 General

A. The specimen shall be subjected to eight cycles of Acceptance Level Vibration/Shock environments.

B. General notes specified in paragraph 4.2.6.1 also apply here.

4.2.9.2 S^2ET Acceptance Level Vibration - Perform the test sequence specified in Table B in each of 3 orthogonal axes. The S^2ET Acceptance level Vibration Test Spectra are given in Figure II. Eight cycles of vibration are required.

TABLE B

VIBRATION TEST LEVEL

TEST DURATION PER AXIS (SECONDS)	FREQUENCY RANGE (Hz) Lower	Upper	ACCELERATION RANDOM (G RMS) Ref.
40	20	2000	6.1

Perform operational test and monitoring per paragraph 4.2.9.4.

4.2.9.3 Acceptance Level Shock

A. The test specimen shall be subjected to impact shocks with a terminal sawtooth pulse shape having a 6 ± 1 millisecond duration.

B. There shall be one shock of 50 g's applied in each of the two directions for each of the axes defined in Figure II for each shock cycle. Eight cycles of shock are required.

C. A photograph shall be made of the first pulse in each direction. (It shall not be necessary to photograph every shock pulse provided the first ones are within tolerance and no set-up changes are made.)

4.2.9.4 Performance Requirements During Acceptance Level Vibration/ Mechanical Shock - Prior to the beginning of the vibration/shock environmental exposure, an operational test per paragraph 4.2.2 shall have been completed. During environmental test in each axis, the specimen shall be monitored per paragraph 4.2.1 and operated per paragraph 4.1.3 A at 30V. Between axes, operate the specimen per paragraph 4.1.3 B at 30V. After completion of the Vibration/ Mechanical Shock Test, perform the operational test of paragraph 4.2.2.

4.3 Post Environmental Tasks

4.3.1 Post-Insulation Resistance Check - Perform insulation resistance test per paragraph 4.1.2.

4.3.2 Post-Environmental Test - Perform operational test per paragraph 4.1.4.

4.3.3 Visual Inspection - After completion of environmental testing, remove the cover and perform visual inspection for any physical defects.

5.0 SUCCESS/FAILURE CRITERIA

Non-compliance with the requirements specified herein shall be considered a failure.

6.0 REPORTING OF MALFUNCTIONS

Failure of the test specimen to meet the requirements of this test request shall be recorded on Qualification Test Failure Report (QTFR) Form No. 3-53201. All applicable items on the report shall be completed by the originator.

The originator's copy of the QTFR shall be retained by the Test Lab. The master and all remaining copies shall be forwarded to Reliability Assurance.

7.0 DATA SHEETS

A reproducible copy of this test request and completed data sheets shall be placed in the components logbook upon completion of tests.

FIGURE NO. I

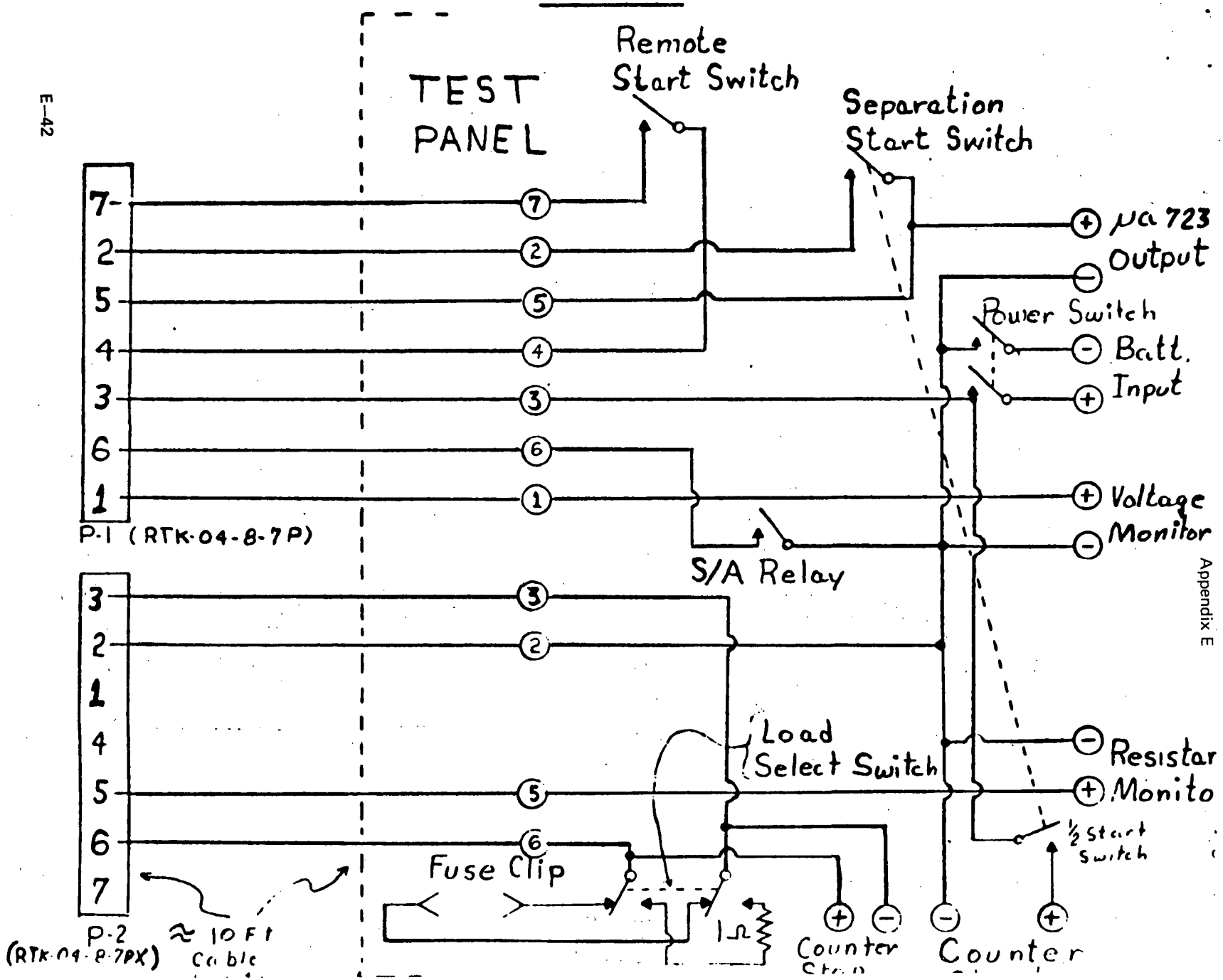
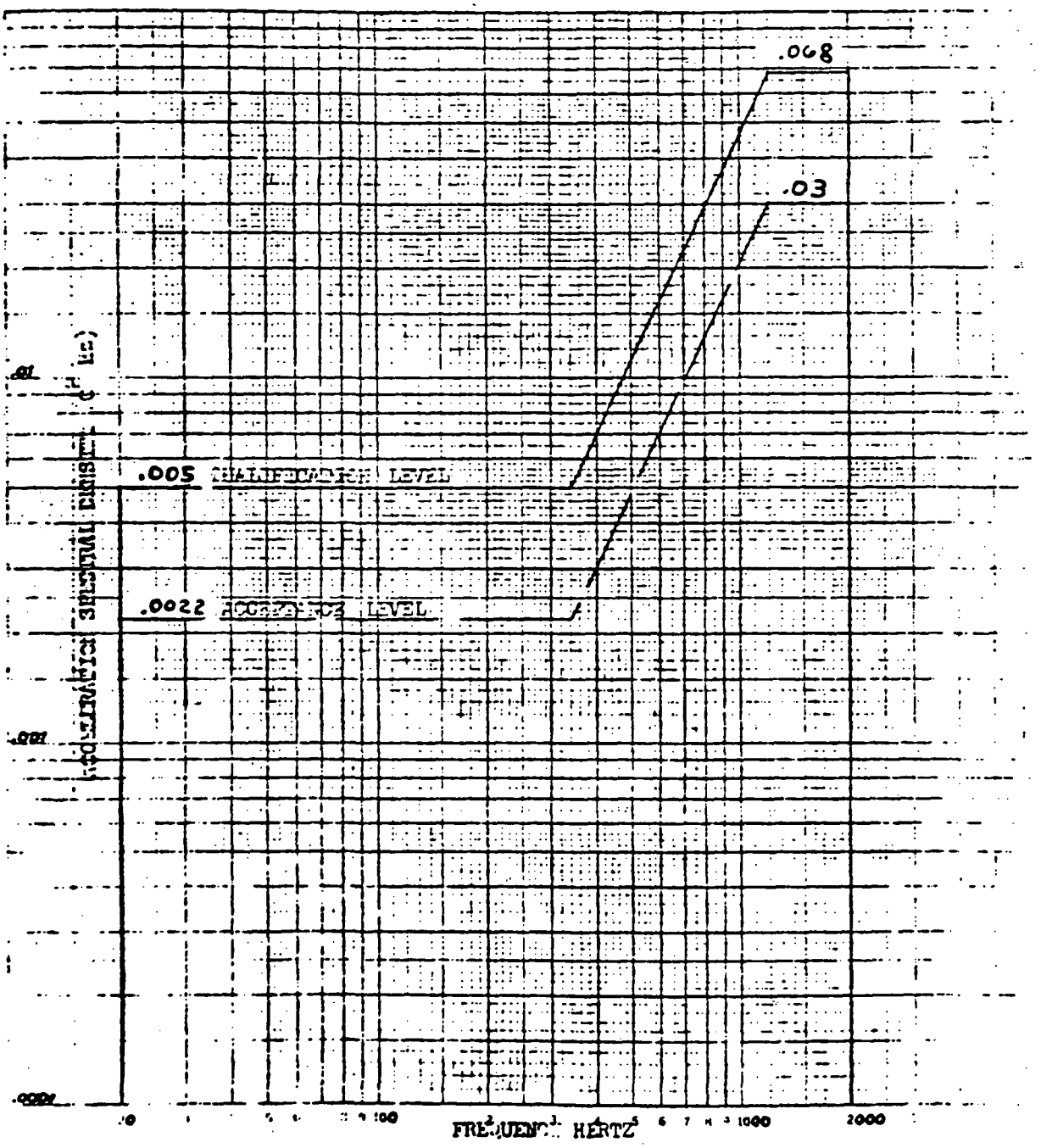

TEST PANEL
Remote Start Switch
Separation Start Switch
7
2
5
4
3
6
1
P-1 (RTK-04-8-7P)
μa 723 Output
Power Switch
Batt. Input
Voltage Monitor
S/A Relay
3
2
1
4
5
6
7
P-2 (RTK-04-8-7PX)
≈ 10 Ft Cable
Load Select Switch
Resistar Monito
½ start switch
Fuse Clip
1Ω
Counter Stop
Counter

FIGURE II
TEST AXES

FIGURE III
VIBRATION TEST SPECTRA

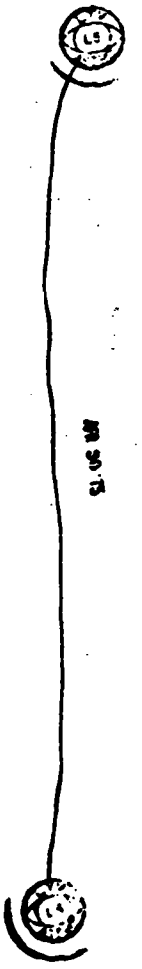


PRE-ENVIRONMENTAL TEST DATA SHEET

4.1.1 Visual Check - ✓ (✓ if ok); Weight 237 grams

4.1.2 Insulation Resistance Check

Pin to Case Pin No.	Resistance Required Minimum (megohms)	Verify (✓)
J1-1	5	✓
-2	5	✓
-3	1	✓
-4	1	✓
-5	1	✓
-6	1	✓
J1-7	1	✓
J2-1	2	✓
-2	2	✓
-3	1	✓
-4	1	✓
-5	1	✓
-6	1	✓
J2-7	1	✓



PRE-ENVIRONMENTAL TEST DATA SHEET

4.1.4 Functional Performance Test

Test A at 30 V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.65	29.8 ± 1.6V. Before t_d	
2	Squib Voltage	0	0 ± .01V Before t_d	
	Squib Voltage Spike*	21.5	20^{+10V}_{-2V} Peak at t_d	A
3	Regulator Output	9.32	9.0 ± 0.5V Until LOR	
4	Input Voltage	29.99	30 ± .01V	
N/A	Time Delay (t_d)	3.716	3.7 ± 0.6 Seconds	

Test B at 30V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.9	29.8 ± 1.6V Before t_d	
2	Squib Voltage	0	0 ± .01V Before t_d	
3	Regulator Output	9.317	9.0 ± 0.5V Until LOR	A
4	Input Voltage	30.01	30 ± .01V	
N/A	LOR Time	6.8	5.2 Seconds (Minimum)	

*Measure Spike Peak Voltage From Photograph

PRE-ENVIRONMENTAL TEST DATA SHEET

4.1.4 Functional Performance Test

Test A at 35V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	30.16	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
	Squib Voltage Spike*	22	20 $^{+10V}_{-2V}$	Peak at t_d
3	Regulator Output	9.32	9.0 ± 0.5V	Until LCR
4	Input Voltage	35	35V ± .01V	
N/A	Time Delay (t_d)	3.733	3.7 ± 0.6	Seconds

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Test B at 35V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	30.25	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
3	Regulator Output	9.32	9.0 ± 0.5V	Until LCR
4	Input Voltage	35.0	35V ± .01V	
N/A	LCR Time	10	5.2 Seconds	(Minimum)

APR 30 '75 A

*Measure Spike Peak Voltage From Photograph

PRE-ENVIRONMENTAL TEST DATA SHEET

4.1.4 Functional Performance Test

Test A at 30V Input (Load Select in "Fuse" Position)

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.8	29.8 ± 1.6V. Before t_d	
2	Squib Voltage	0	0 ± .01V Before t_d	
	Squib Voltage Spike	✓	Verify Fuse Opens	
3	Regulator Output	9.28	9.0 ± 0.5V Until LOR	A
4	Input Voltage	29.99	30V ± .01V	
2	Squib Voltage Spike	3.719 ✓	Verify Spike Output at t_d	A

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PRE-ENVIRONMENTAL TEST
DATA SHEET

4.1.4 Functional Performance Test

Test A at 35 V Input ("Safe Arm Relay" Switch "On")

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	3.01	3.15 ± 0.2V Before t_d	A
2	Squib Voltage	0	0 ± .01V Before t_d	
	Squib Voltage Spike	✓	Verify Fuse Does not Open	
3	Regulator Output	9.30	9.0 ± 0.5V Until LCR	A
4	Input Voltage	35.0	35 ± .01	
2	Squib Voltage Spike	✓	Verify Spike Output at t_d	A

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DATA SHEET

4.2.2 Operational Test

Pre-test for High Temperature/Low Temperature

Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.65	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
	Squib Voltage Spike*	21.5	20V $^{+10V}_{-2V}$ Peak at t_d
3	Regulator Output	9.32	9.0 ± 0.5V Until LOR
4	Input Voltage	29.99	30V ± .01V
N/A	Time Delay (t_d)	3.716	3.7 ± 0.6 Seconds

APR 30 75 A

Test B at 30V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.9	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.317	9.0 ± 0.5 V Until LOR
4	Input Voltage	30.01	30 ± V
N/A	LOR Time	8.8	5.2 Seconds (Minimum)

APR 30 75 A

*Measure Output Spike Peak Voltage From Photograph

DATA SHEET

HIGH TEMPERATURE/LOW TEMPERATURE

4.2.3 High Temperature

Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	29.52	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
	Squib Voltage Spike*	22	20^{+10V}_{-2V}	Peak at t_d
3	Regulator Output	9.32	9.0 ± 0.5V	Until LCR
4	Input Voltage	30.00	30V ± .01V	
N/A	Time Delay (t_d)	3.75	3.7 ± 0.6	Seconds

4/8 30 75 A

Test B at 30V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	29.5	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
3	Regulator Output	9.33	9.0 ± 0.5V	Until LCR
4	Input Voltage	30.0	30V ± .01V	
N/A	LCR Time	10.4	5.2 Seconds	(Minimum)

4/8 30 75 A

*Measure Spike Peak Voltage From Photograph

DATA SHEET

HIGH TEMPERATURE/LOW TEMPERATURE

4.2.3 High Temperature

Test A at 35V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	30.9	29.8 ± 1.6V. Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
	Squib Voltage Spike*	23	20V $^{+10V}_{-2V}$ Peak at t_d
3	Regulator Output	9.33	9.0 ± 0.5V Until LCR
4	Input Voltage	35.0	35V ± .01V
N/A	Time Delay (t_d)	3.77	3.7 ± 0.6 Seconds

4R 30 75 A

Test B at 35V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	30.95	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.33	9.0 ± 0.5V Until LCR
4	Input Voltage	35	35 ± .01V
N/A	LCR Time	11.8	5.2 Seconds (Minimum)

4R 30 75 A

*Measure Spike Peak Voltage From Photograph

DATA SHEET

HIGH TEMPERATURE/LOW TEMPERATURE

4.2.3 Low Temperature

Test A at 30V Input , Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.2	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
	Squib Voltage Spike*	20	20 $^{+10V}_{-2V}$ Peak at t_d
3	Regulator Output	9.30	9.0 ± 0.5V Until LOR
4	Input Voltage	30.0	30V ± .01V
N/A	Time Delay (t_d)	3.708	3.7 ± 0.6 Seconds

APR 30 75 (15) A

Test B at 30V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.2	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.30	9.0 ± 0.5V Until LOR
4	Input Voltage	30.0	30V ± .01V
N/A	LOR Time	7.7	5.2 Seconds (Minimum)

APR 30 75 (15) A

*Measure Spike Peak Voltage From Photograph

DATA SHEET

HIGH TEMPERATURE/LOW TEMPERATURE

4.2.3 Low Temperature

Test A at 35V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	29.1	29.8 ± 1.6V. Before t_d
2	Squib Voltage	0	0 $\pm^{+.01V}_{+10V}$ Before t_d
	Squib Voltage Spike*	21	20 -2V. Peak at t_d
3	Regulator Output	9.30	9.0 ± 0.5V Until LOR
4	Input Voltage	35	35 ± .01V
N/A	Time Delay (t_d)	3.708	3.7 ± 0.6 Seconds

APR 30 '75

A

Test B at 35V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	29.24	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.30	9.0 ± 0.5V Until LOR
4	Input Voltage	35	35 ± .01V
N/A	LOR Time	8.4	5.2 Seconds (Minimum)

APR 30 '75

A

*Measure Spike Peak Voltage From Photograph

DATA SHEET

4.2.2 Operational Test

Post-Test for High Temperature/Low Temperature

Test A at 30V Input , Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.85	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
	Squib Voltage Spike*	21.8	20 $^{+10V}_{-2V}$	Peak at t_d
3	Regulator Output	9.31	9.0 ± 0.5V	Until LCR
4	Input Voltage	30.0	30V ± .01V	
N/A	Time Delay (t_d)	3.711	3.7 ± 0.6	Seconds

A

Test B at 30 V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.87	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
3	Regulator Output	9.31	9.0 ± 0.5 V	Until LCR
4	Input Voltage	30.0	30V ± .01V	
N/A	LCR Time	8.2	5.2 Seconds (Minimum)	

A

*Measure Output Spike Peak Voltage From Photograph

DATA SHEET

TEMPERATURE SHOCK

4.2.2 Operational Test

Pre-Test for Temperature Shock

Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.85	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
	Squib Voltage Spike*	21.8	20^{+10V}_{-2V} Peak at t_d
3	Regulator Output	9.31	9.0 ± 0.5V Until LOR
4	Input Voltage	30.0	30V ± .01V
N/A	Time Delay (t_d)	3.711	3.7 ± 0.6 Seconds

MAY 1 '75

Test B at 30 V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.87	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.31	9.0 ± 0.5V Until LOR
4	Input Voltage	30.0	30 ± .01V
N/A	LOR Time	8.2	5.2 Seconds (Minimum)

MAY 1 '75

*Measure Output Spike Peak Voltage From Photograph

DATA SHEET

4.2.4 Temperature Shock

Test A at 30V Input,

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.40	29.8 ± 1.6V. Before t_d	REV 1 75
2	Squib Voltage	0	0 ± .01V Before t_d	
	Squib Voltage Spike	21V	Verify (✓) at t_d	
3	Regulator Output	9.30	9.0 ± 0.5V Until LCR	A
4	Input Voltage	29.99	30 ± .01V	
N/A	Time Delay (t_d)	3.691	3.7 ± 0.6 Seconds	

Test B at 30V Input

REV 1 75

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage.	28.6	29.8 ± 1.6V Before t_d	
2	Squib Voltage	0	0 ± .01V Before t_d	
3	Regulator Output	9.31	9.0 ± 0.5V Until LCR	A
4	Input Voltage	30	30V ± .01V	
N/A	LCR Time	8.8	5.2 Seconds (Minimum)	

DATA SHEET

4.2.4 Temperature Shock

Test A at 35V Input,

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	30.2	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
	Squib Voltage Spike	✓	Verify (✓) at t_d
3	Regulator Output	9.31	9.0 ± 0.5V Until LOR
4	Input Voltage	35.0	35 ± .01V
N/A	Time Delay (t_d)	3.690	3.7 ± 0.6 Seconds

Test B at 35V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	30.25	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.31	9.0 ± 0.5V Until LOR
4	Input Voltage	35	35 ± .01V
N/A	LOR Time	10.6	5.2 Seconds (Minimum)

DATA SHEET

TEMPERATURE SHOCK

4.2.2 Operational Test

Post-Test for Temperature Shock

Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.87	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
	Squib Voltage Spike*	21.5	20 $^{+10V}_{-2V}$	Peak at t_d
3	Regulator Output	9.31	9.0 ± 0.5V	Until LOR
4	Input Voltage	30	30V ± .01V	
N/A	Time Delay (t_d)	3.715	3.7 ± 0.6	Seconds

NOV 1 75 A

Test B at 30V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.86	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
3	Regulator Output	9.31	9.0 ± 0.5V	Until LOR
4	Input Voltage	30	30V ± .01V	
N/A	LOR Time	8.2	5.2 Seconds (Minimum)	

NOV 1 75 A

*Measure Output Spike Peak Voltage from Photograph

DATA SHEET

HIGH TEMPERATURE-ALTITUDE

4.2.2 Operational Test

Operational Pretest for High Temperature-Altitude

Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.87	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
	Squib Voltage Spike*	21.5	20 $^{+10V}_{-2V}$ Peak at t_d
3	Regulator Output	9.31	9.0 ± 0.5V Until LOR
4	Input Voltage	30.0	30 ± .01V
N/A	Time Delay (t_d)	3.715	3.7 ± 0.6 Seconds

MAY 1 75 A

Test B at 30V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.86	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.31	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30 ± .01V
N/A	LOR Time	8.2	5.2 Seconds (Minimum)

MAY 1 75 A

*Measure Output Spike Peak Voltage from Photograph

DATA SHEET

HIGH TEMPERATURE-ALTITUDE

CYCLE 1

4.2.5.1 Operational Test for Temperature-Altitude

Test A at 30V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	29.5	29.8 ± 1.6V. Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
	Squib Voltage Spike	✓	Verify (✓) at t_d
3	Regulator Output	9.33	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30 ± .01V
N/A	Time Delay (t_d)	3.76	3.7 ± 0.6 Seconds

Test B at 30 V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	29.5	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.33	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30 ± .01V
N/A	LOR Time	10.2	5.2 Seconds (Minimum)

DATA SHEET

HIGH TEMPERATURE-ALTITUDE

CYCLE 1

4.2.5.1 Operational Test for Temperature-Altitude

Test A at 35V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	30.01	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
	Squib Voltage Spike	✓	Verify (✓) at t_d
3	Regulator Output	9.33	9.0 ± 0.5V Until LOR
4	Input Voltage	35.0	35 ± .01V
N/A	Time Delay (t_d)	3.76	3.7 ± 0.6 Seconds

MAY 1 75

A

Test B at 35V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	31.05	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.33	9.0 ± 0.5V Until LOR
4	Input Voltage	35.0	35 ± .01V
N/A	LOR Time	11.9	5.2 Seconds (Minimum)

MAY 1 75

A

DATA SHEET

HIGH TEMPERATURE-ALTITUDE

CYCLE 2

4.2.5.1 Operational Test for Temperature-Altitude

Test A at 30V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	29.5	29.8 ± 1.6V Before t_d	
2	Squib Voltage	0	0 ± .01V Before t_d	
	Squib Voltage Spike	✓	Verify (✓) at t_d	
3	Regulator Output	9.33	9.0 ± 0.5V Until LOR	A
4	Input Voltage	30.0	30 ± .01V	
N/A	Time Delay (t_d)	3.76	3.7 ± 0.6 Seconds	

Test B at 30 V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	29.5	29.8 ± 1.6V Before t_d	
2	Squib Voltage	0	0 ± .01V Before t_d	
3	Regulator Output	9.33	9.0 ± 0.5V Until LOR	A
4	Input Voltage	30	30 ± .01V	
N/A	LOR Time	10.4	5.2 Seconds (Minimum)	

DATA SHEET

HIGH TEMPERATURE-ALTITUDE
CYCLE 2

4.2.5.1 Operational Test for Temperature-Altitude

Test A at 35V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	30.9	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
	Squib Voltage Spike	✓	Verify (✓) at t_d
3	Regulator Output	9.33	9.0 ± 0.5 V Until LOR
4	Input Voltage	35.0	35 ± .01V
N/A	Time Delay (t_d)	3.77	3.7 ± 0.6 Seconds

MAY 1 75 A

Test B at 35V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	30.9	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.33	9.0 ± 0.5V Until LOR
4	Input Voltage	35.0	35 ± .01V
N/A	LOR Time	11.8	5.2 Seconds (Minimum)

MAY 1 75 A

DATA SHEET

HIGH TEMPERATURE -ALTITUDE

4.2.2 Operational Test

Operational Post-Test for High Temperature-Altitude
Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.89	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
	Squib Voltage Spike*	21.5	$20^{\mp 10V}_{-2V}$	Peak at t_d
3	Regulator Output	9.31	9.0 ± 0.5V	Until LOR
4	Input Voltage	30.0	30 ± .01V	
N/A	Time Delay (t_d)	3.711	3.7 ± 0.6	Seconds

NOV 1 '73

A

Test B at 30V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.9	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
3	Regulator Output	9.31	9.0 ± 0.5V	Until LOR
4	Input Voltage	30.0	30 ± .01V	
N/A	LOR Time	8.2	5.2 Seconds (Minimum)	

NOV 1 '73

A

*Measure Output Spike Peak Voltage from Photograph

DATA SHEET

VIBRATION/MECHANICAL SHOCK

4.2.2 Operational Test

Operational Pre-Test for Vibration/Mechanical Shock

Test A at 30V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.89	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
	Squib Voltage Spike*	21.5	20 $^{+10V}_{-2V}$	Peak at t_d
3	Regulator Output	9.31	9.0 ± 0.5V	Until LOR
4	Input Voltage	30.0	30V ± .01V	
N/A	Time Delay (t_d)	3.711	3.7 ± 0.6	Seconds

MAY 2 '75 (LS) A

Test B at 30V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.9	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
3	Regulator Output	9.31	9.0 ± 0.5V	Until LOR
4	Input Voltage	30.0	30V ± .01V	
N/A	LOR Time	8.2	5.2 Seconds (Minimum)	

MAY 2 '75 (LS) A

*Measure Output Spike Peak Voltage from Photograph

DATA SHEET

VIBRATION/MECHANICAL SHOCK

4.2.6.4 Performance Requirements During Vibration/Mechanical Shock

Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement X	Measurement Y	Measurement Z Axis	Required Value	
1	Ignition Charge Voltage	28.9	28.9	28.9	29.8 ± 1.6V Before t_d	NV 2 '75
2	Squib Voltage	0	0	0	0 ± .01V Before t_d	
	Squib Voltage Spike*	21.5	21.5	21.0	20 $^{+10V}_{-2V}$ Peak at t_d	A
3	Regulator Output	9.31	9.31	9.31	9.0 ± 0.5V Until LCR	
4	Input Voltage	30	30	30	30V ± .01V	
N/A	Time Delay (t_d)	3.70	3.719	3.71	3.7 ± 0.6 Seconds	

Test B at 30V Input (Between Axis Test)

Cha No.	Description	Measurement		Required Value	
1	Ignition Charge Voltage	28.9	28.9	29.8 ± 1.6V Before t_d	NV 2 '75
2	Squib Voltage	0	0	0 ± .01V Before t_d	
3	Regulator Output	9.31	9.31	9.0 ± 0.5V Until LCR	A
4	Input Voltage	30	30	30 ± .01V	
N/A	LCR Time	8.1	8.0	5.2 Seconds (Minimum)	

*Measure Spike Peak Voltage From Photograph

DATA SHEET

VIBRATION/MECHANICAL SHOCK

4.2.2 Operational Test

Operational Post-Test for Vibration/Mechanical Shock Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.9	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
	Squib Voltage Spike*	21.5	20 $^{+10V}_{-2V}$ Peak at t_d
3	Regulator Output	9.31	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30 ± .01V
N/A	Time Delay (t_d)	3.719	3.7 ± 0.6 Seconds

MAY 2 75 LS A

Test B at 30V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.9	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.31	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30V ± .01V
N/A	LOR Time	8.2	5.2 Seconds (Minimum)

MAY 2 75 A

*Measure Output Spike Peak Voltage from Photograph

DATA SHEET

ACCELERATION

4.2.2 Operational Pre-Test for Acceleration

Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.88	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
	Squib Voltage Spike*	23	20 $^{+10V}_{-2V}$ Peak at t_d
3	Regulator Output	9.31	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30V ± .01V
N/A	Time Delay (t_d)	3.673	3.7 ± 0.6 Seconds

Test B at 30V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.88	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.31	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30V ± .01V
N/A	LOR Time	7.8	5.2 Seconds (Minimum)

*Measure Output Spike Peak Voltage from Photograph

DATA SHEET

ACCELERATION

4.2.7.3 Performance Requirements During Acceleration

Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement (AXIS) X	-X	Y	-Y	Z	-Z	Required Value
1	Ignition Charge Voltage	28.89	28.9	28.87	28.89	28.9	28.89	29.8 ± 1.6V Before t_c
2	Squib Voltage	0	0	0	0	0	0	0 ± .01V Before t_d
	Squib Voltage Spike*	23	23.5	23.2	23.2	23	23	20 $^{+10V}_{-2V}$ Peak at t_d
3	Regulator Output	9.31	9.31	9.31	9.31	9.31	9.31	9.0 ± 0.5V Until LCR
4	Input Voltage	30	30	30	30	30	30	30V ± .01V
N/A	Time Delay (t_d)	3.711	3.35	3.41	3.35	3.37	3.34	3.7 ± 0.6 Seconds

Test B at V Input (Between Axis Test)

Cha No.	Description	Measurements (AXIS) X	-X	Y	-Y	Z	Required Value
	Ignition Charge Voltage	28.73	28.89	28.9	28.89	28.91	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0	0	0	0	0 ± .01V Before t_d
3	Regulator Output	9.31	9.31	9.31	9.31	9.31	9.0 ± 0.5V Until LCR
4	Input Voltage	30	30	30	30	30	30 ± .01V
N/A	LCR Time	8.0	8.3	8.1	8.1	8.2	5.2 Seconds (Minimum)

*Measure Spike Peak Voltage From Photograph

DATA SHEET

ACCELERATION

4.2.2 Operational Post-Test for Acceleration

Test A at 30 V Input , Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	_____	29.8 ± 1.6V.	Before t_d
2	Squib Voltage	_____	0 ± .01V	Before t_d
	Squib Voltage Spike*	_____	20 $^{+10V}_{-2V}$	Peak at t_d
3	Regulator Output	_____	9.0 ± 0.5V	Until LOR
4	Input Voltage	_____	30 ± .01V	
N/A	Time Delay (t_d)	_____	3.7 ± 0.6	Seconds

A

Test B at 30 V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	_____	29.8 ± 1.6V	Before t_d
2	Squib Voltage	_____	0 ± .01V	Before t_d
3	Regulator Output	_____	9.0 ± 0.5V	Until LOR
4	Input Voltage	_____	30 ± .01V	
N/A	LOR Time	_____	5.2 Seconds (Minimum)	

A

Refer to 23-QTFR-008

AUG 5 73

*Measure Output Spike Peak Voltage from Photograph

DATA SHEET

HUMIDITY

4.2.2 Operational Pre-Test for Humidity

Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.714	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
	Squib Voltage Spike*	20	20^{+10V}_{-2V}	Peak at t_d
3	Regulator Output	9.238	9.0 ± 0.5V	Until LCR
4	Input Voltage	30	30 ± .01V	
N/A	Time Delay (t_d)	3.721	3.7 ± 0.6	Seconds

A

Test B at 30V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.914	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
3	Regulator Output	9.238	9.0 ± 0.5V	Until LCR
4	Input Voltage	30	30 ± .01V	
N/A	LOR Time	8.2	5.2 Seconds (Minimum)	

A

*Measure Output Spike Peak Voltage from Photograph

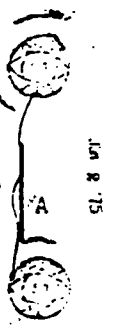
DATA SHEET

HUMIDITY

4.2.2 Operational Post-Test for Humidity

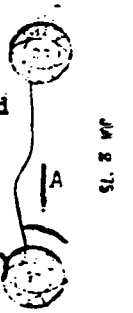
Test A at 30V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.964	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
	Squib Voltage Spike*	20	20 $^{+10V}_{-2V}$ Peak at t_d
3	Regulator Output	9.240	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30 ± .01V
N/A	Time Delay (t_d)	3.729	3.7 ± 0.6 Seconds



Test B at 30V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.964	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.240	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30 ± .01V
N/A	LOR Time	8.4	5.2 Seconds (Minimum)



*Measure Output Spike Peak Voltage from Photograph

DATA SHEET

CYCLIC LIFE

4.2.2 Operational Pre-Test for Cyclic Life

Test A at 30V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.90	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
	Squib Voltage Spike*	20	20 $^{+10V}_{-2V}$	Peak at t_d
3	Regulator Output	9.257	9.0 ± 0.5V	Until LOR
4	Input Voltage	30	30V ± .01V	
N/A	Time Delay (t_d)	3.723	3.7 ± 0.6	Seconds

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Test B at 30V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.90	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
3	Regulator Output	9.257	9.0 ± 0.5V	Until LOR
4	Input Voltage	30	30V ± .01V	
N/A	LOR Time	8.4	5.2 Seconds (Minimum)	

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*Measure Output Spike Voltage From Photograph

DATA SHEET

CYCLIC LIFE (CYCLE 1)

4.2.9.4 Performance Requirements During Acceptance Level Vibration/Shock

Test A at 30V Input

	Cha No.	Description	Measurement (Axis) X	Y	Z	Required Value
	1	Ignition Charge Voltage	28.89	28.93	28.94	29.8 ± 1.6V Before t_d
	2	Squib Voltage	0	0	0	0 ± .01V Before t_d
		Squib Voltage Spike	✓	✓	✓	Verify Output
A	3	Regulator Output	9.258	9.256	9.255	9.0 ± 0.5V Until LOR
	4	Input Voltage	30	30	30	30V ± .01V
	N/A	Time Delay (t_d)	3.721	3.721	3.720	3.7 ± 0.6 Seconds

Test B at 30V Input (Between Axis Operation)

	Cha.No.	Description	Measurement XY	YZ	ZZ	Required Value
	1	Ignition Charge Voltage	28.89	28.89	28.89	29.8 ± 1.6V Before t_d
	2	Squib Voltage	0	0	0	0 ± .01V Before t_d
A	3	Regulator Output	9.258	9.258	9.255	9.0 ± 0.5V Until LOR
	4	Input Voltage	30	30	30	30V ± .01V
	N/A	LOR Time	8.4	8.4	8.4	5.2 Seconds (Minimum)

DATA SHEET

CYCLIC LIFE (CYCLE 2)

4.2.9.4 Performance Requirements During Acceptance Level Vibration/Shock

Test A at 30V Input

	Cha No.	Description	Measurement (Axis) X	Y	Z	Required Value
	1	Ignition Charge Voltage	28.95	28.95	28.94	29.8 ± 1.6V Before t_d
	2	Squib Voltage	0	0	0	0 ± .01V Before t_d
		Squib Voltage Spike	✓	✓	✓	Verify Output
A	3	Regulator Output	9.253	9.254	9.255	9.0 ± 0.5V Until LOR
	4	Input Voltage	30	30	30	30V ± .01V
	N/A	Time Delay (t_d)	3.722	3.723	3.722	3.7 ± 0.6 Seconds

Test B at 30V Input (Between Axis Operation)

	Cha.No.	Description	Measurement XY	YZ	ZZ	Required Value
	1	Ignition Charge Voltage	28.95	28.95	28.94	29.8 ± 1.6V Before t_d
	2	Squib Voltage	0	0	0	0 ± .01V Before t_d
A	3	Regulator Output	9.253	9.254	9.255	9.0 ± 0.5V Until LOR
	4	Input Voltage	30	30	30	30V ± .01V
	N/A	LOR Time	8.6	8.6	8.6	5.2 Seconds (Minimum)

DATA SHEET

CYCLIC LIFE (CYCLE 3)

4.2.9.4 Performance Requirements During Acceptance Level Vibration/Shock

Test A at 30V Input

Cha No.	Description	Measurement (Axis) X	Y	Z	Required Value
1	Ignition Charge Voltage	28.93	28.96	28.96	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0	0	0 ± .01V Before t_d
	Squib Voltage Spike	✓	✓	✓	Verify Output
A 3	Regulator Output	9.253	9.252	9.252	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30	30	30V ± .01V
N/A	Time Delay (t_d)	3.725	3.723	3.722	3.7 ± 0.6 Seconds

Test B at 30V Input (Between Axis Operation)

Cha.No.	Description	Measurement XY	YZ	ZZ	Required Value
1	Ignitinn Charge Voltage	28.93	28.96	28.96	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0	0	0 ± .01V Before t_d
1 3	Regulator Output	9.253	9.252	9.252	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30	30	30V ± .01V
N/A	LOR Time	8.4	8.4	8.4	5.2 Seconds (Minimum)

DATA SHEET

CYCLIC LIFE (CYCLE 4)

4.2.9.4 Performance Requirements During Acceptance Level Vibration/Shock

Test A at 30V Input

Cha No.	Description	Measurement (Axis) X	Y	Z	Required Value
1	Ignition Charge Voltage	28.96	28.96	28.96	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0	0	0 ± .01V Before t_d
	Squib Voltage Spike	✓	✓	✓	Verify Output
A 3	Regulator Output	9.252	9.251	9.253	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30	30	30V ± .01V
N/A	Time Delay (t_d)	3.723	3.724	3.723	3.7 ± 0.6 Seconds

Test B at 30V Input (Between Axis Operation)

Cha.No.	Description	Measurement XY	YZ	ZZ	Required Value
1	Ignition Charge Voltage	28.96	28.96	28.96	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0	0	0 ± .01V Before t_d
A 3	Regulator Output	9.252	9.251	9.253	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30	30	30V ± .01V
N/A	LOR Time	8.4	8.4	8.4	5.2 Seconds (Minimum)

DATA SHEET

CYCLIC LIFE (CYCLE 5)

4.2.9.4 Performance Requirements During Acceptance Level Vibration/Shock

Test A at 30V Input

Cha No.	Description	Measurement (Axis) X	Y	Z	Required Value
1	Ignition Charge Voltage	28.92	28.96	28.96	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0	0	0 ± .01V Before t_d
	Squib Voltage Spike	✓	✓	✓	Verify Output
3	Regulator Output	9.252	9.251	9.252	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30	30	30V ± .01V
N/A	Time Delay (t_d)	3.727	3.723	3.724	3.7 ± 0.6 Seconds

Test B at 30V Input (Between Axis Operation)

Cha.No.	Description	Measurement XY	YZ	ZZ	Required Value
1	Ignition Charge Voltage	28.92	28.96	28.96	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0	0	0 ± .01V Before t_d
3	Regulator Output	9.252	9.252	9.252	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30	30	30V ± .01V
N/A	LOR Time	8.4	8.4	8.5	5.2 Seconds (Minimum)

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DATA SHEET

CYCLIC LIFE (CYCLE 6)

4.2.9.4 Performance Requirements During Acceptance Level Vibration/Shock

Test A at 30V Input

	Cha No.	Description	Measurement (Axis) X	Y	Z	Required Value
	1	Ignition Charge Voltage	28.96	28.95	28.96	29.8 ± 1.6V Before t_d
	2	Squib Voltage	0	0	0	0 ± .01V Before t_d
		Squib Voltage Spike	✓	✓	✓	Verify Output
A	3	Regulator Output	9.252	9.252	9.252	9.0 ± 0.5V Until LOR
	4	Input Voltage	30	30	30	30V ± .01V
	N/A	Time Delay (t_d)	3.724	3.723	3.724	3.7 ± 0.6 Seconds

Test B at 30V Input (Between Axis Operation)

	Cha.No.	Description	Measurement XY	YZ	ZZ	Required Value
	1	Ignition Charge Voltage	28.96	28.95	28.96	29.8 ± 1.6V Before t_d
	2	Squib Voltage	0	0	0	0 ± .01V Before t_d
A	3	Regulator Output	9.252	9.252	9.252	9.0 ± 0.5V Until LOR
	4	Input Voltage	30	30	30	30V ± .01V
	N/A	LOR Time	8.5	8.4	8.35	5.2 Seconds (Minimum)

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CYCLIC LIFE (CYCLE 7)

4.2.9.4 Performance Requirements During Acceptance Level Vibration/Shock

Test A at 30V Input

	Cha No.	Description	Measurement (Axis) X	Y	Z	Required Value
	1	Ignition Charge Voltage	28.97	28.97	28.97	29.8 ± 1.6V Before t_d
	2	Squib Voltage	0	0	0	0 ± .01V Before t_d
		Squib Voltage Spike	✓	✓	✓	Verify Output
A	3	Regulator Output	9.251	9.250	9.250	9.0 ± 0.5V Until LOR
	4	Input Voltage	30	30	30	30V ± .01V
	N/A	Time Delay (t_d)	3.724	3.725	3.724	3.7 ± 0.6 Seconds

Test B at 30V Input (Between Axis Operation)

	Cha.No.	Description	Measurement XY	YZ	ZZ	Required Value
	1	Ignition Charge Voltage	28.97	28.97	28.97	29.8 ± 1.6V Before t_d
	2	Squib Voltage	0	0	0	0 ± .01V Before t_d
A	3	Regulator Output	9.251	9.250	9.250	9.0 ± 0.5V Until LOR
	4	Input Voltage	30	30	30	30V ± .01V
	N/A	LOR Time	8.5	8.4	8.4	5.2 Seconds (Minimum)

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CYCLIC LIFE (CYCLE 8)

4.2.9.4 Performance Requirements During Acceptance Level Vibration/Shock

Test A at 30V Input

	Cha No.	Description	Measurement (Axis) X	Y	Z	Required Value
	1	Ignition Charge Voltage	28.97	28.97	28.97	29.8 ± 1.6V Before t_d
	2	Squib Voltage	0	0	0	0 ± .01V Before t_d
		Squib Voltage Spike	✓	✓	✓	Verify Output
A	3	Regulator Output	9.250	9.249	9.250	9.0 ± 0.5V Until LOR
	4	Input Voltage	30	30	30	30V ± .01V
	N/A	Time Delay (t_d)	3.725	3.724	3.724	3.7 ± 0.6 Seconds

Test B at 30V Input (Between Axis Operation)

	Cha.No.	Description	Measurement XY	YZ	ZZ	Required Value
	1	Ignition Charge Voltage	28.97	28.97	28.97	29.8 ± 1.6V Before t_d
	2	Squib Voltage	0	0	0	0 ± .01V Before t_d
A	3	Regulator Output	9.250	9.249	9.250	9.0 ± 0.5V Until LOR
	4	Input Voltage	30	30	30	30V ± .01V
	N/A	LOR Time	~~3.725~~ 8.4	8.4	8.4	5.2 Seconds (Minimum)

DATA SHEET

CYCLIC LIFE (CYCLE 9)

4.2.9.4 Performance Requirements During Acceptance Level Vibration/Shock

Test A at 30V Input

	Cha No.	Description	Measurement (Axis) X	Y	Z	Required Value
	1	Ignition Charge Voltage	28.97	28.97	28.97	29.8 ± 1.6V Before t_d
	2	Squib Voltage	0	0	0	0 ± .01V Before t_d
		Squib Voltage Spike	✓	✓	✓	Verify Output
A	3	Regulator Output	9.249	9.248	9.248	9.0 ± 0.5V Until LOR
	4	Input Voltage	30	30	30	30V ± .01V
	N/A	Time Delay (t_d)	3.724	3.725	3.724	3.7 ± 0.6 Seconds

Test B at 30V Input (Between Axis Operation)

	Cha.No.	Description	Measurement XY	YZ	ZZ	Required Value
	1	Ignition Charge Voltage	28.97	28.97	28.97	29.8 ± 1.6V Before t_d
	2	Squib Voltage	0	0	0	0 ± .01V Before t_d
A	3	Regulator Output	9.249	9.249	9.248	9.0 ± 0.5V Until LOR
	4	Input Voltage	30	30	30	30V ± .01V
	N/A	LOR Time	8.5	8.5	8.4	5.2 Seconds (Minimum)

TEST PERFORMED PER 23-ATFR-008

DATA SHEET

CYCLIC LIFE (CYCLE 10)

4.2.9.4 Performance Requirements During Acceptance Level Vibration/Shock

Test A at 30V Input

	Cha No.	Description	Measurement (Axis) Z	Y	X	Required Value
	1	Ignition Charge Voltage	28.98	28.98	28.97	29.8 ± 1.6V Before t_d
	2	Squib Voltage	0	0	0	0 ± .01V Before t_d
		Squib Voltage Spike	✓	✓	✓	Verify Output
A	3	Regulator Output	9.249	9.249	9.248	9.0 ± 0.5V Until LOR
	4	Input Voltage	30	30	30	30V ± .01V
	N/A	Time Delay (t_d)	3.725	3.725	3.724	3.7 ± 0.6 Seconds

Test B at 30V Input (Between Axis Operation)

	Chn.No.	Description	Measurement ZY	YX	XX	Required Value
	1	Ignitinn Charge Voltage	28.98	28.98	28.97	29.8 ± 1.6V Before t_d
	2	Squib Voltage	0	0	0	0 ± .01V Before t_d
A	3	Regulator Output	9.249	9.249	9.248	9.0 ± 0.5V Until LOR
	4	Input Voltage	30	30	30	30V ± .01V
	N/A	LOR Time	8.5	8.4	8.5	5.2 Seconds (Minimum)

TEST PERFORMED PER 23-QTCR-008

DATA SHEET

CYCLIC LIFE

4.2.2 Operational Post-Test for Cyclic Life

Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.97	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
	Squib Voltage Spike*	19	20^{+10V}_{-2V} Peak at t_d
3	Regulator Output	9.248	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30V ± .01V
N/A	Time Delay (t_d)	3.723	3.7 ± 0.6 Seconds

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Test B at 30V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.97	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.248	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30V ± .01V
N/A	LOR Time	8.5	5.2 Seconds (Minimum)

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*Measure Output Spike Peak Voltage From Photograph

POST-ENVIRONMENTAL TEST DATA SHEET

4.1.1 Visual Check - ✓ (✓ if ok); Weight 2.37 grms

4.1.2 Insulation Resistance Check

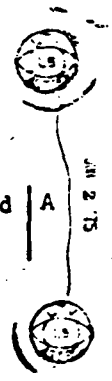
Pin to Case Pin No.	Resistance Required Minimum (megohms)	Verify (✓)
J1-1	5	✓
-2	5	✓
-3	1	✓
-4	1	✓
-5	1	✓
-6	1	✓
J1-7	1	✓
J2-1	2	✓
-2	2	✓
-3	1	✓
-4	1	✓
-5	1	✓
-6	1	✓
J2-7	1	✓

POST-ENVIRONMENTAL TEST DATA SHEET

4.1.4 Functional Performance Test

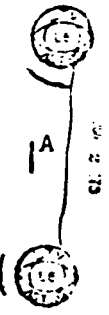
Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.967	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
	Squib Voltage Spike*	20	20 $^{+10V}_{-2V}$ Peak at t_d
3	Regulator Output	9.237	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30V ± .01V
N/A	Time Delay (t_d)	3.727	3.7 ± 0.6 Seconds



Test B at 30V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.967	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.237	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30V ± .01V
N/A	LOR Time	8.4	5.2 Seconds (Minimum)



*Measure Spike Peak Voltage From Photograph

POST-ENVIRONMENTAL TEST DATA SHEET

4.1.4 Functional Performance Test

Test A at 35 V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	30.198	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
	Squib Voltage Spike*	21	20^{+10V}_{-2V}	Peak at t_d
3	Regulator Output	9.238	9.0 ± 0.5V	Until LOR
4	Input Voltage	35	35 ± .01V	
N/A	Time Delay (t_d)	3.730	3.7 ± 0.6	Seconds

Test B at 35 V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	30.198	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
3	Regulator Output	9.238	9.0 ± 0.5V	Until LOR
4	Input Voltage	35	35 ± .01V	
N/A	LOR Time	9	5.2 Seconds (Minimum)	

*Measure Spike Peak Voltage From Photograph

POST-ENVIRONMENTAL TEST DATA SHEET

4.1.4 Functional Performance Test

Test A at 30V Input (Load Select in "Fuse" Position)

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	29.07	29.8 ± 1.6V Before t_d	
2	Squib Voltage	0	0 ± .01V Before t_d	
	Squib Voltage Spike	✓	Verify Fuse Opens	
3	Regulator Output	9.235	9.0 ± 0.5V Until LOR	A
4	Input Voltage	30	30V ± .01V	
2	Squib Voltage Spike	3.735	Verify Spike Output at t_d in Channel 2	A

POST-ENVIRONMENTAL TEST DATA SHEET

4.1.4 Functional Performance Test

Test A at 35 V Input ("Safe Arm Relay" Switch "On")

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	3.07	3.15 ± 0.2V Before t_d	A
2	Squib Voltage	0	0 ± .01V Before t_d	
	Squib Voltage Spike	✓	Verify Fuse Does Not Open	
3	Regulator Output	9.234	9.0 ± 0.5V Until LOR	A
4	Input Voltage	35	35 ± .01V	
2	Squib Voltage Spike	✓	Verify Spike Output at t_d	A

DATA SHEET

TEMPERATURE SHOCK

4.2.2 Operational Test

Pre-Test for Temperature Shock

Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.91	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
	Squib Voltage Spike*	20	20 $^{+10V}_{-2V}$	Peak at t_d
3	Regulator Output	9.28	9.0 ± 0.5V	Until LOR
4	Input Voltage	30	30V ± .01V	
N/A	Time Delay (t_d)	3.71	3.7 ± 0.6	Seconds

A

Test B at 30V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.91	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
3	Regulator Output	9.28	9.0 ± 0.5V	Until LOR
4	Input Voltage	30	30 ± .01V	
N/A	LOR Time	8.4	5.2 Seconds	(Minimum)

A

TEST PER 23-QTFR-008

*Measure Output Spike Peak Voltage From Photograph

DATA SHEET

4.2.4 Temperature Shock

Test A at 30V Input,

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.06	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
	Squib Voltage Spike	18	Verify (✓)	at t_d
3	Regulator Output	9.274	9.0 ± 0.5V	Until LOR | A
4	Input Voltage	30	30 ± .01V	
N/A	Time Delay (t_d)	3.696	3.7 ± 0.6	Seconds

Test B at 30V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.06	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
3	Regulator Output	9.274	9.0 ± 0.5V	Until LOR | A
4	Input Voltage	30	30V ± .01V	
N/A	LOR Time	7.8	5.2 Seconds	(Minimum)

TEST PER 23-GTFR-008

DATA SHEET

4.2.4 Temperature Shock

Test A at 35V Input,

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	30.03	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
	Squib Voltage Spike	19	Verify (✓) at t_d
3	Regulator Output	9.28	9.0 ± 0.5V Until LCR
4	Input Voltage	35	35 ± .01V
N/A	Time Delay (t_d)	3.695	3.7 ± 0.6 Seconds

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Test B at 35V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	30.03	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.28	9.0 ± 0.5V Until LCR
4	Input Voltage	35	35 ± .01V
N/A	LCR Time	9.0	5.2 Seconds (Minimum)

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TEST PER 23-ATP-008

DATA SHEET

TEMPERATURE SHOCK

4.2.2 Operational Test

Post-Test for Temperature Shock

Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.83	29.8 ± 1.6V Before t_d	MAY 15 '75
2	Squib Voltage	0	0 ± .01V Before t_d	
	Squib Voltage Spike*	20	20 $^{+10V}_{-2V}$ Peak at t_d	A
3	Regulator Output	9.26	9.0 ± 0.5V Until LOR	
4	Input Voltage	30	30V ± .01V	
N/A	Time Delay (t_d)	3.724	3.7 ± 0.6 Seconds	

Test B at 30V Input

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.83	29.8 ± 1.6V Before t_d	MAY 15 '75
2	Squib Voltage	0	0 ± .01V Before t_d	
3	Regulator Output	9.26	9.0 ± 0.5V Until LOR	A
4	Input Voltage	30	30V ± .01V	
N/A	LOR Time	8.3	5.2 Seconds (Minimum)	

TEST PER 23-QTFR-008

*Measure Output Spike Peak Voltage from Photograph

DATA SHEET

TEMPERATURE SHOCK

4.2.2 Operational Test

Post-Test for Temperature Shock

Test A at 30V Input, Output Spike Photograph Required

Cha No.	Description	Measurement	Required Value	
1	Ignition Charge Voltage	28.83	29.8 ± 1.6V	Before t_d
2	Squib Voltage	0	0 ± .01V	Before t_d
	Squib Voltage Spike*	20	20 $^{+10V}_{-2V}$	Peak at t_d
3	Regulator Output	9.26	9.0 ± 0.5V	Until LOR
4	Input Voltage	30	30V ± .01V	
N/A	Time Delay (t_d)	3.724	3.7 ± 0.6	Seconds

MG 15 75

A

Test B at 30V Input

Cha No.	Description	Measurement	Required Value
1	Ignition Charge Voltage	28.83	29.8 ± 1.6V Before t_d
2	Squib Voltage	0	0 ± .01V Before t_d
3	Regulator Output	9.26	9.0 ± 0.5V Until LOR
4	Input Voltage	30	30V ± .01V
N/A	LOR Time	8.3	5.2 Seconds (Minimum)

MG 15 75

A

TEST PER 23-GTFR-008

*Measure Output Spike Peak Voltage from Photograph

Appendix E

QUALIFICATION TEST FAILURE REPORT

C.: FR NO. 23-QTFR-008

PROGRAM SCOUT

DATE 5-5-75 | PAGE 1 OF 13

	NAME	MSD DRAWING NO.	CUSTOMER DWG. NO.	SERIAL NO.
TEST ITEM	Electronic Delay Ignition Module (EDIM)	23-004349-1		002
SUBASSEMBLY	NAME	MANUFACTURER	PART OR DWG. NO.	SERIAL OR LOT NO.
COMPONENT	NAME	MANUFACTURER	PART OR DWG. NO.	SERIAL OR LOT NO.

G.O. NUMBER (ENGINEERING EFFORT)	G.O. NUMBER (QUALITY EFFORT)	G.O. NUMBER (MANUFACTURING EFFORT)
3384-CV-1220	3384-CV-1220	3384-CV-1220

TEST LABORATORY	TEST DOCUMENT NUMBER	REV.	DATE
2-45202	23-TRA-0244	--	4-14-75

PREVIOUS ENVIRONMENTAL TESTS
1. Hi-Temp/Low Temp 4-2-3 3. Hi-Temp-Altitude - 4-2-5
2. Temp. Shock 4-2-4 4. Vib/Mech Shock 4-2-6 5. Accel. 4-2-7

TOTAL OPERATING TIME/CYCLES: ∠ 3 hours

FAILURE DESCRIPTION

During operational test of para. 4.2.2, after completion of the acceleration test per para. 4.2.7.3, voltage measurements performed according to para. 4.2.2 were incorrect. The regulator voltage measured 4.4 volts; should be 9.0 ± 0.5 VDC.

NOTE: See Continuation Page 2 for Failure Description.

TEST MONITOR	DATE	RELIABILITY ENGINEER	DATE	BREAK OF INSPECTION REQ'D.	DATE
[signature]	5-6-75	[signature]	5-6-75	☐	

FAIL INVESTIGATION REQ'D.	INVESTIGATION ASSIGNED TO	PROJECT ENGINEER	DATE	PROJECT ENGINEER
☒	R D WARD	[signature]		[signature]

FAILED PT. ANAL. REQ'D.	PROJECT ENGINEER	DATE	FAILED PART ANALYSIS REPORT NO.	QUALITY
☐				[signature]

FAILURE INVESTIGATION SUMMARY

Investigation showed that Z-1 (Voltage Regulator SE550) was damaged due to improperly applied voltage. No other components indicated damage due to miswired cable. The EDIM operated properly after replacing Z-1.

R.D. Ward 9 may 75

CUSTOMER: [signature] 5-6-75

*See Page 2 for continuation of Failure Investigation Summary.

CORRECTIVE ACTION ASSIGNED TO	PROJECT ENGINEER	DATE
C.D. PEACOCK	[signature]	5/9/75

CORRECTIVE ACTION DESCRIPTION

Technician rewired connector to a configuration more compatible with cantiage wiring and did not notify engineer. Connector was not reconfiguring when reconnected directly to the unit. Personnel involved were cautioned not to reconfigure wiring without approval and wiring diagram. [signature] 5/12/75

WORK INSTRUCTIONS

Conformal coat the EDIM printed circuit board. Then return the EDIM to its original configuration per print 23-004344. After assembly perform an operational test per para. 4.2.2. See pages 12 and 13 for details.

PROJECT ENGINEER	RELIABILITY ENGINEER	WORK COMPLETED			
		QUALITY	DATE	CUSTOMER	DATE
QUALITY [signature]	CUSTOMER [signature] 5/12/75	[signature]	MAY 19 '75	[signature]	5-13-75

QUALIFICATION RETEST REQUIREMENTS: 1. Reperform Temperature Shock Test per para. 4.2.4.
2. Conduct the EMI Test per para. 5 of SEI 1683. 3. Conduct 10 cycles of S²ET Vibration and Mechanical Shock per para. 4.2.9. 4. Conduct Humidity Test per para. 4.2.8.

5. This completes the qualification test program of the EDIM; return to para. 7 of SEI 1683A.

RELIABILITY ENGINEER	DATE	PROJECT ENGINEER	DATE	CUSTOMER	DATE
[signature]	5-13-75	[signature]	[illegible]	[signature]	5/14/75

3-5322

	QTFR NO. 23-QTFR-008
CONTINUATION SHEET – QUALIFICATION TEST FAILURE REPORT	PAGE 2 OF

FAILURE DESCRIPTION

A review of the test results indicated the regulator voltage measured 9.31 VDC before the EDIM was disconnected at the completion of the acceleration tests, but measured 4.4 VDC when reconnected for the operational test. Upon the discovery of the voltage discrepancy, it was realized that the power cable connector connected to the EDIM input cable was wired incorrectly. This connector was rewired according to print. The incorrect wire configuration of the connector was not recorded and, therefore, is unknown. The EDIM was retested with the revised connector. The voltage measurements according to para. 4.2.2 were still incorrect.

FAILURE INVESTIGATION SUMMARY (Continued)

NOTE: The first SE550 installed in the board was affected by temp-shock from amb temp to -17.8°C and back to amb (increased standby current, reference step 21 of continuation sheet). This SE580 was inoperable after removal from the EDIM board.

FAILURE INVESTIGATION:

1. Connect the EDIM and apply power per ENGINEERING DIRECTION. ✓

2. PERFORM OR VERIFY VOLTAGE MEASUREMENTS FOR THE FOLLOWING POINTS; RECORD VOLTAGE:

a)	REGULATOR OUTPUT:	4.4 VDC
b)	VOLTAGE MONITOR:	26.67 VDC
c)	OUTPUT VOLTAGE:	0 VDC
d)	J1-1:	28.66 VDC
e)	J1-2:	0 VDC
f)	J1-3:	30 VDC
g)	J1-5:	4.45 VDC
h)	J1-6:	28.94 VDC
i)	J1-7:	0 VDC
j)	J2-1:	0 VDC
k)	J2-2:	0 VDC
l)	J2-5:	0 VDC
m)	all other J2 PINS.	0 VDC

QTFR NO. 23-GTFR-008

CONTINUATION SHEET – QUALIFICATION TEST FAILURE REPORT | PAGE 3 OF

2. Verify and record EDIM current. 3.0 ma.

3. Verify and record Time delay. 4.997 sec.

4. Remove power and disconnect the EDIM from the TEST PANEL. Unit was accidently pulled into the floor by the attached cable, Unit dropped approximately 30" with no apparent damage. V

5. Remove the cover of the EDIM, then remove the bottom plate from the printed circuit board. V

6. Connect the EDIM printed circuit board to the TEST PANEL and apply power per ENGINEERING DIRECTION. V

7. measure and record voltages for the following locations / components.

a)	R 13	440.4 mV
b)	CR4	545 mV
c)	R1	539 mV
d)	CR5	577 mV
e)	R9	4.76 V
f)	SE 550 - PIN 2	813.3 mV
g)	R7	.95 mV
h)	Input voltage	29.98V
i)	CR3	28.87V
j)	SE 550 - PIN 1	4.474V
k)	SE 550 - PIN 4	1.682V
l)	SE 550 - PIN 5	0V
m)	SE 550 - PIN 6 & 10	4.491V
n)	SE 550 - PIN 7 & 8	28.87V
o)	SE 550 - PIN 9	21.43V

5-5-75

	QTFR NO. 23 - GTFR -00F
CONTINUATION SHEET – QUALIFICATION TEST FAILURE REPORT	PAGE 4 OF

7. Summary of the above failure investigation steps:

A review of the above steps indicates that the SE 550 IC is defective. Steps 6f and 6k indicate that the gain of the IC, either the operational amp input or regulator output, ~~gain~~ has changed. These two voltages should be the same, approximately 1- 6.82 V. Since step 6 g indicates only -.813 VDC, the conclusion is that the IC has been damaged by incorrect applied voltage. Therefore, the SE 550 IC should be replaced.

8. Remove and replace the SE 550 IC network. Do not conformal coat at this time ✓

CO [stamp] GOVT [stamp]

5-7-25 [stamp]

9. Reconnect the EDIM without covers to the TEST PANEL and reverify test parameters for unit performance per para. 4.2.2 ✓

TEST A.

Ignition charge voltage	28.95V
Squib Voltage	0 V
Squib Voltage Spike	22.5V
Regulator output	9.33V
Input Voltage	30 V

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CONTINUATION SHEET – QUALIFICATION TEST FAILURE REPORT | PAGE 5 OF

9 - TEST A Con't.

5-7-79 Time Delay 3.719 Seconds.

TEST B

Ignition charge Voltage	28.95V
Squib Voltage	0V.
Regulator output	9.33 V
Input Voltage	30V
LOR Time	8-1 Secs.
Total EDIM current is	4.1 MA

5-7-79

10. Results of the performance test of para. 4.2.2 in step 9 above indicate that the EDIM without covers, is performing according to functional requirements.

5-7-79

11. Put the EDIM without covers into a sealed plastic bag, then place the unit into a thermal chamber, that has stabilized at 0°F, for a temperature test. ✓

5-7-79

12. After 30 minutes with the EDIM in the chamber, perform a functional test per para. 4.2.2; record the voltages etc as required. ✓

TEST A.

Ignition charge Voltage	28.035V
Squib Voltage	0
Squib Voltage Spike	21V

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CONTINUATION SHEET – QUALIFICATION TEST FAILURE REPORT | PAGE 6 OF

12. TEST A Con't.

5-7-75

Regulator output	9.327 V
Input Voltage	30 V
Time Delay	3.687 sec.

TEST B

Ignition charge Voltage	28.035 V
Squib Voltage	0V
Regulator output	9.327 V
Input Voltage	30 V
LOR Time	6.7 secs
Total EDIM INPUT current	7.5 MA

5-7-75

B. Verify LOR Time and EDIM input current. ✓

5-7-75

LOR TIME 6.7 secs. INPUT I 7.5 MA.

5-7-75

14. Remove the EDIM from the thermal chamber ✓ and remove plastic bag.

15. after 30 minutes, perform operational test per para. 4-2-2 and record results as required below.

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CONTINUATION SHEET – QUALIFICATION TEST FAILURE REPORT | PAGE 7 OF

15 cont.

TEST A.

Ignition	Charge Voltage	28.82 V
Squib	Voltage	0 V
Squib	Voltage Spike	22 V
Regulator	output	9.33 V
Input	Voltage	30 V
Time	Delay	3.709 sec.

TEST B.

Ignition	Charge Voltage	28.82 V
Squib	Voltage	0 V
Regulator	output	9.33 V
Input	Voltage	30 V
LOR	Time	8.05 sec.

Total EDIM INPUT current 4.8 MA

16. Disconnect the EDIM from its input cable and blow the surface of the board with dry nitrogen. ✓

17. Reconnect the EDIM to the Test Panel and measure input current, record current. 4.45MA

18. after 30 minutes, again measure input current and record. 4.55 MA

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CONTINUATION SHEET – QUALIFICATION TEST FAILURE REPORT	PAGE 8 OF

19. measure and record voltage for the following locations/components. (05-07-75)

a) R13 — 510 mV

b) CR4 — 556 mV

c) R1 — 870.3 mV

d) CR5 — 602.4 mV

e) R9 — 19.68 mV

f) SE 550 – PIN 2 TO GND — 1.684 V.

g) R7 — 197 mV

h) Input voltage — 30 V.

i) CR3 — 28.55 V.

j) SE 550 – PIN 1 TO GND — 9.336 V.

k) " " 4 TO GND — 1.685 V.

l) " " 5 TO GND — 0.04 MV.

m) " " PIN 6 & 10 TO GND. — 9.355 V.

n) " " PIN 7 & 8 TO GND — 28.56 V.

o) SE 550 – PIN 9 TO GND — 9.353 V

20. (next Day - 05-08-75) measure and record the following parameters of the EDIM:

INPUT current — 4.45 MA

Regulator output — 9.342 V

Charge voltage — 28.64 V

Trip Delay — 3.717 sec.

LOR TIME — 8.7 sec.

NOTE: Input current went down to 4.4 MA after Trip Delay.

	QTFR NO.
CONTINUATION SHEET – QUALIFICATION TEST FAILURE REPORT	PAGE 9 OF

21. Summation of Steps 9 thru 20:

25 Test parameters tested per para. 4.2.2 were within specifications. However as noted, input current to the EDIM changed after being subjected to a 0°F environment and brought back to ambient temperature. That is, it started out at 4.1 MA at ambient, went to 7.5 MA and came back to 4.45 MA at ambient. Because of the offset current before and after temperature cycle, 4.1 MA versus 4.45 MA, it was decided to run another IC on a breadboard test through a temperature cycle. This breadboard test was performed on an IC just with its associated circuit components, but not with the complete EDIM. The current input of this IC at 30 VDC was 3.3 MA room ambient, 3.3 MA at 0°F after 1 hour stabilization, and 3.35 MA after 5 hr room ambient. Based on the results that the IC input current changed very little during the breadboard test, the SE 550 IC now mounted on the EDIM board should be replaced with the one tested on the breadboard setup. Remove the unit from the test panel.

22. Remove the SE 550 IC from the EDIM board and replace with the provided SE550IC. DO NOT conformal coat the board.

Co [signature] 8 MAY '75 Govt [signature] 181 Shop [signature] (F121) 8 MAY '75

23. Reconnect the EOIM to the TEST PANEL; measure and record the following parameters, voltages, components:

a)	R13	485 MV
b)	CR 4	538 MV
c)	R1	846 MV
d)	CR6	604 MV
e)	R9	23 MV
f)	SE 550 - PIN 2 TO GND	1.67 V
g)	R7	198 MV
h)	Input Voltage	30 V
i)	CR3	28.52 V
j)	SE 550 - PIN 1 TO GND.	9.27 V
k)	" PIN 4 TO GND.	1.675 V
l)	" PIN 5 TO GND.	0.0 V
m)	" PIN 6 & 10 TO GND.	9.2938 V
n)	" PIN 7 & 8 TO GND.	28.52 V
o)	" PIN 9 TO GND.	10.58 V
p)	Input current	4.25 MA
q)	Regulator output.	9.265 V.
r)	Charge Voltage	28.92 V
s)	Sine Delay	3.713 secs.
t)	LOK Delay	8.35 secs.

24. Place the EDIM board into a plastic bag and put the unit into a thermal chamber which has been stabilized at 0°F. ✓

25. after 30 minutes, measure and record the following test parameters.

Input voltage	30 V
Input current	6.85 MA.
Regulator output	9.263 V.
Charge voltage	28.13 V.
Trip Delay	3.704 sec.
LOR Delay	7.5 sec.

26. Remove the EDIM from the thermal chamber and leave unit stabilized at room ambient. ✓

27. after 30 minutes minimum, measure and record the following test parameters:

Input voltage	30. V
Input current	4.4MA
Regulator output	9.273V
Charge voltage	28.87 V
Trip Delay	3.717 sec.
LOR Delay	8.4 sec.

28. Iteration of steps 24 thru 27.

29. The recal SE 550 IC was installed onto the EDIM board. Ambient and low temperature tests were performed to verify functional operation, also, to provide reference data. The EDIM performed as required. Therefore, reassemble the EDIM back to its required configuration, as noted below. (Refer to page 5 of PC Board Assy Log Book attached sheets).

29-75

29a. Clean, inspect and OK to apply conformal coating.

9 MAY 75 GOVT. 151

30. Apply 1B 15 conformal coating to the PC board on both sides, per spec 30B-9-22, Type II, Class-B. F65

31. Inspect coating. 12 May 75

32. Reassembly the EDIM according to drawing 23-00 43 49. F65

A. Mounting gasket found defective, due to disassembly. Have gasket made from 85-30170 stock as noted on print 23-00 43 49.

B. Continued to reassembly EDIM according to 13 MAY drawing 23-00 4349.

E-107

3-83205

CONTINUATION SHEET – QUALIFICATION TEST FAILURE REPORT	PAGE 13 OF

33. Perform an operational test per para. 4.2.2 after connection to Test Panel. Record readings. ✓

TEST A.

Ignition charge voltage	28.92V
Squib voltage	0V
Squib voltage spike	verify ✓
Regulator output	9.275V
Input voltage	30V
Time Delay	3.72 sec.

TEST B.

Ignition charge voltage	28.92V
Squib voltage	0V
Regulator output	9.275V
Input voltage	30V
LOR Time	8.2 sec.
Total EOM current	4.25 MA

TEST AND EVALUATION REPORT / RELIABILITY ASSURANCE LABORATORY

3-43199

MOI	DATE OF FAILURE (MO. / DAY / YR.)	LOCATION OF FAILURE		No.
SCOUT				2-45202/5R-47
SYSTEM: Ignition	MR NO.	MRA NO.		PAGE 1 OF 1
COMPONENT: Ignition Delay Assembly	P/N: 23-004349-1	S/N: Qual 002	CODE	MANUF.: VSD/Marshall Street
PART	P/N	S/N	CODE	MANUF.

OBJECTIVE(S):

Subject the Scout Fourth Stage Electronic Delay Ignition Module to a thorough visual examination for evidence of damage and capacitor leakage after completion of flight qualification tests. This assembly had been subjected to altitude, temperature shock, high-low temperature, vibration, humidity, acceleration, mechanical shock and EMI susceptibility tests.

EVALUATION PROCEDURES AND RESULTS:

Figures 1, 2, 3 and 4 are top, end, side and bottom views, respectively, of the assembly. Visual examination of the exterior revealed several areas (arrows in Figures 1, 3 and 4) where the paint had loosened and peeled away from the metal surface.

The bottom cover plate was removed for examination of the interior. Figure 5 is a view of one side of the circuit board before its removal from the case. An oblique view of the circuit board mounted on the bottom cover is shown in Figure 6. Figure 7 is a view of the opposite side of the circuit board after its removal from the bottom cover plate. Examination of the circuit board and the interior of the case revealed no evidence of moisture or corrosion as a result of the humidity test. However, the paint had loosened and pulled away from the metal in one of the inside covers of the case as shown in Figure 8, arrow.

Visual examination of the circuit board revealed no cracked solder joints or anomalies as a result of the qualification tests. The ends of all the capacitors were examined and exposed to litmus paper with no evidence of electrolyte leakage.

In conclusion, other than the paint which had loosened and peeled away from the metal surfaces, there was no evidence of component deterioration after the flight qualification tests.

NOTE: This report contains two (2) pages of photographs.

ANALYSIS BY	DATE	REVIEWED BY	DATE
J. V. Sanders	7-15-75	[signature]	7/16/75

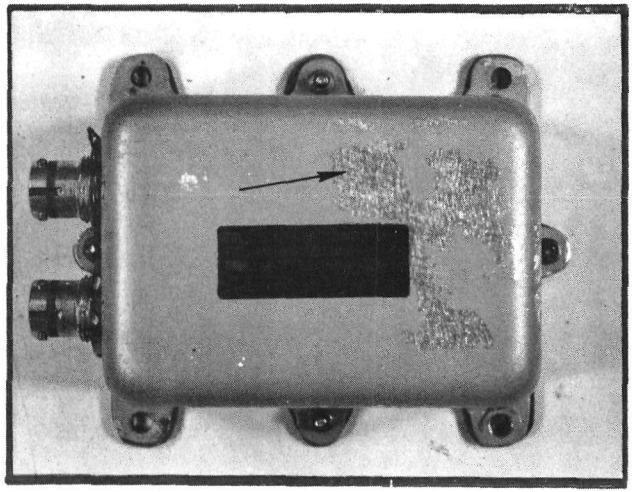

Figure 1. Top view of assembly.

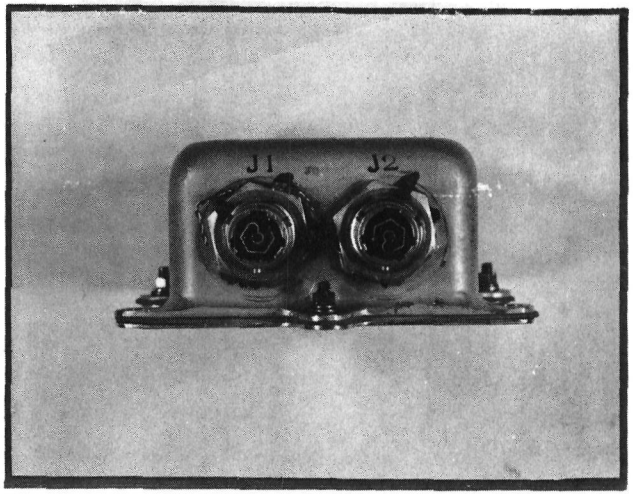

Figure 2. End view of assembly.

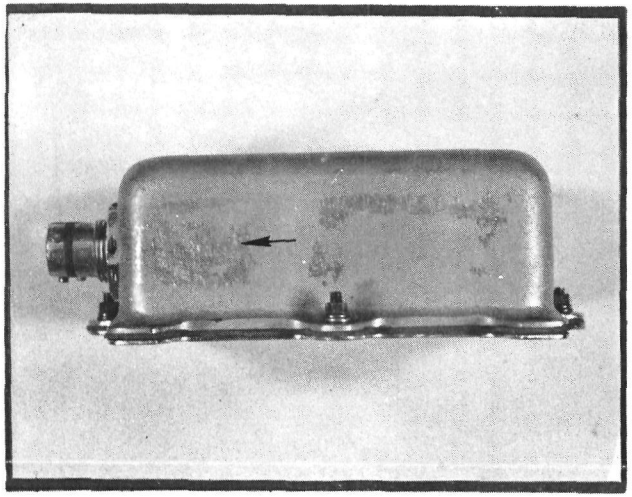

Figure 3. Side view of assembly.

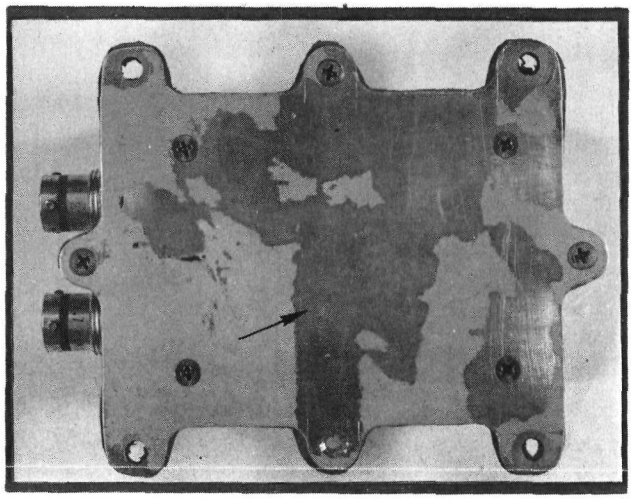

Figure 4. Bottom view of assembly.

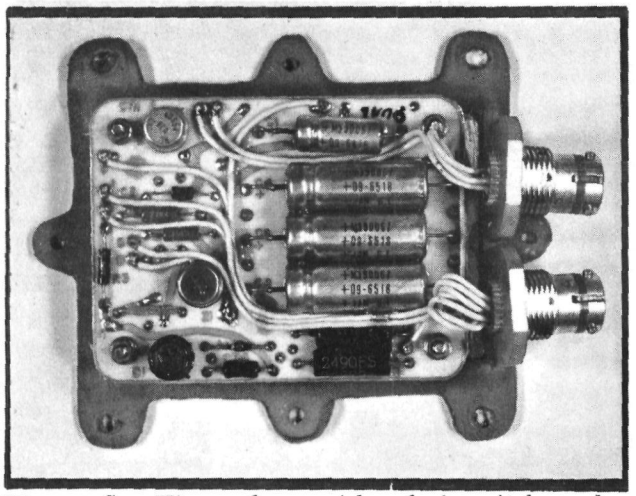

Figure 5. View of one side of circuit board before its removal from the case.

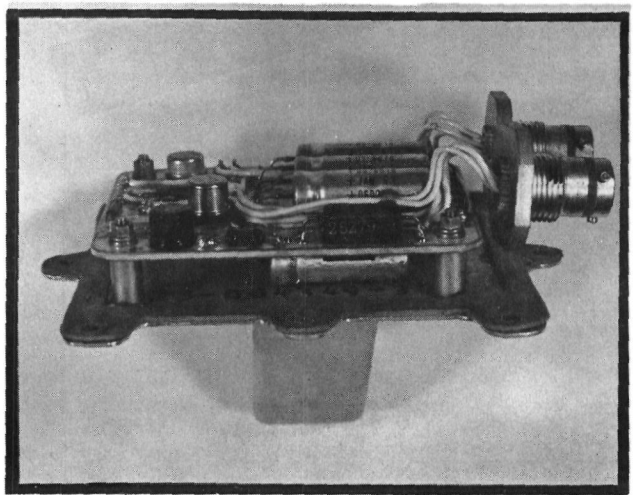

Figure 6. Oblique view of circuit board mounted to bottom cover plate.

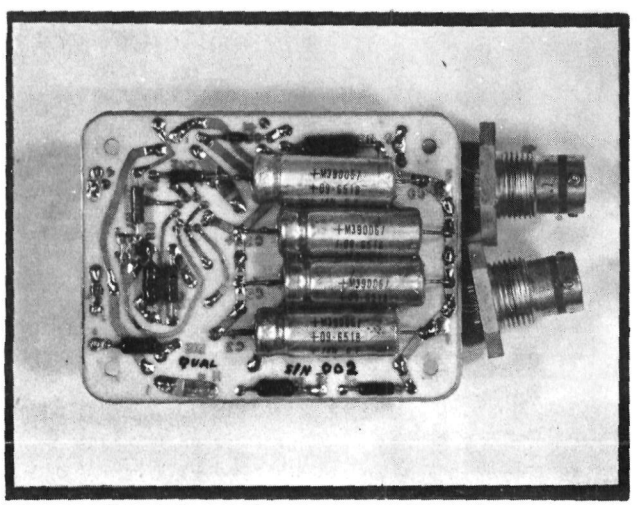

Figure 7. View of opposite side of circuit board.

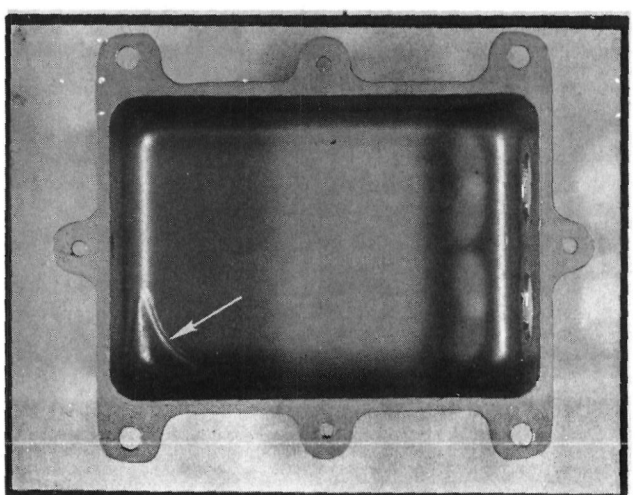

Figure 8. Arrow points to area inside case where paint had come loose from the metal.

Enclosure (3) to
REPORT NO. 23-DIR-1779

PAGE NO. 1 OF _____

COPY NO. _____

TITLE

Electromagnetic Susceptibility Test Report for the 23-004349-1 Electronic Delay Ignition Module

SUBMITTED UNDER	
REPORT NO.	DATED 11 July 1975
MODEL SCOUT	CONTRACT NO.
DATE ISSUED	SUPERSEDING

C. L. Dyer
PREPARED
C. L. Dyer

A. R. Tomme
REVIEWED
A. R. Tomme

APPROVED
RDW

REVISIONS

DATE	REV BY	PAGES AFFECTED	REMARKS

TABLE OF CONTENTS

ADMINISTRATIVE DATA

Purpose of Test

To qualify the Electronic Delay Ignition Module for Scout flight application. This was accomplished by performing the following tests:

1. Conducted Susceptibility
2. Radiated Susceptibility

Manufacturer

Vought Systems Division
LTV Aerospace Corporation
Dallas, Texas

Interference Specifications

MIL-STD-461A, Notice 1
MIL-STD-462, Notice 1

Security Classification

Unclassified

Disposition of Test Article

To be retained at LTV

References

a) VSD Test Request 23-TRA-0246, EMI Qualification Test for Scout 4th Stage Electronic Delay Ignition Module (EDIM) P/N 23-004349-1, dated 8 May 1975.

LIST OF FIGURES

LIST OF TEST EQUIPMENT

	Test Equipment	Characteristics Required
1.	Automated Spectrum Surveillance System Fairchild FSS-250 Ser - 005	30 Hz to 1 GHz 50 ohms
2.	Current Probe Fairchild Electrometrics Mod - PCL-10 Ser - 005	30 Hz - 50 KHz 50 ohms
3.	Current Probe Fairchild Electrometrics Mod - PCL-25 Ser - 005	14 KHz to 25 MHz 50 ohms
4.	Field Strength Meter Instruments for Industry Mod - EFS-1	14 KHz to 1 GHz
5.	Antenna EMCO Mod - 3105 Ser - 2039	1 GHz to 12 GHz 50 ohms Double Ridge Waveguide Horn
6.	R. F. Power Source Airborn Instruments Laboratory Mod - AIL-25 Ser - 117	200 MHz to 3 GHz 50 ohms
7.	R. F. Power Source Hewlett-Packard Mod - HP 6188 Ser - 1100	3.8 GHz to 7.0 GHz 50 ohms
8.	R. F. Power Source Hewlett-Packard Mod - HP 620B Ser - 740-00534	7 GHz to 11 GHz 50 ohms
9.	TWT Amplifier Keltec Florida Mod - SR630-200 Ser - 4429-045	1 GHz to 2 GHz 50 ohms 200 watts
10.	TWT Amplifier Keltec Florida Mod - CR630-200 Ser - 4428-009	2 GHz to 4 GHz 50 ohms 200 watts

LIST OF TEST EQUIPMENT (Continued)

	Test Equipment	Characteristics Required
11.	TWT Amplifier Keltec Florida Mod - CR 630-200 Ser - 4428-010	4 GHz to 8 GHz 50 ohms 200 watts
12.	TWT Amplifier Keltec Florida Mod - XR630-200 Ser - 4429-048	8 GHz to 12 GHz 50 ohms 200 watts
13.	Signal Generator Spectral Dynamics Mod - SD 104-5 Ser - 5957	50 Hz to 50 KHz
14.	Signal Generator Hewlett-Packard Mod - HP 608D Ser - 1527	10 MHz to 480 MHz 0.1 v. into 50 ohms
15.	Signal Generator Hewlett-Packard Mod - HP 606B Ser - 811-01791	50 KHz to 50 MHz 0.1 v. into 50 ohms
16.	Power Amplifier Krohn Hite Corp. Mod - U F 101A Ser - 983	50 Hz to 15 KHz 3v open circuit
17.	Isolation Transformer Solar Electronics Mod - 6220-1A5 Ser - None	
18.	Field Strength Meter Singer Mod - EMA-310 Ser - 123-135	1 - 10 GHz 50 ohms
19.	TWT Driver Keltec Mod - SR620-1 Ser - 4440-032	2 - 4 GHz 1 watt
20.	TWT Driver Keltec Mod - DR620-1 Ser - 4428-010	4 - 8 GHz 1 watt

LIST OF TEST EQUIPMENT (Continued)

	Test Equipment	Characteristics Required
21.	TWT Driver Keltec Mod XR620-1 Ser - 4428-011	8 - 12 GHz 1 watt
22.	Antenna Instruments for Industry Mod - EFG - 2 Ser - 45	10 KHz - 200 MHz 50 ohms
23.	Antenna EMCO Mod - 3106 Ser - 2005	200 MHz - GHz 50 ohms Double Ridge Waveguide Horn
24.	VTVM Hewlett - Packard Mod - HP-403	
25.	Oscilloscope Tektronix Mod - 545	
26.	RF Power Amplifier Instrument for Industries Mod - 406 Ser - 0674969	10 KHz - 200 MHz 1000 watts
27.	Antenna EMCO Mod - 3102 Ser - 2352	1 - 10 GHz Log Conical
28.	Choke	.010 Hys. 12.5 Amps DC
29.	Oscilloscope Hewlett - Packard Mod - HP 184A with 1805 plug in Ser - 1301A 00357	
30.	Digital Voltmeter Data Precision Mod - 3500 Ser - 1798	
31.	Electronic Counter Hewlett - Packard Mod - NP 5326A Ser - 1240A 01880	

1.0 General

1.1 TEST SAMPLE DESCRIPTION

The test article was the Scout 4th Stage Electronic Delay Ignition Module (EDIM), P/N 23-004349-1, S/N 002.

1.1.1 Purpose of Test Sample - The Electronic Delay Ignition Module is designed to ignite an SBASI after a 3.7 second delay from an external command (switch closure between J1-2 and J1-3).

1.1.2 Electrical and Hardware Description - The EDIM circuit diagram is shown in Figure 1. Power to the unit is supplied from the Scout 3rd stage ignition battery through connector J1-5 and J2-2. In flight operation, power will be removed (3rd to 4th stage separation) from the unit 1.5 seconds before the start command. Power for generation of the delay and ignition of the SBASI is stored in capacitors for the operational life of the unit (5.2 seconds, 1.5 + 3.7). The capacitors used for energy storage are hermatically sealed tantalum wet slug capacitors. Time delay is generated with an unijunction transistor and a RC integrator circuit, an op. amp voltage regulator is used to stabilize the unijunction voltage during decay of the power storage capacitors. The unijunction transistor provides a gate signal to turn on an SCR which dumps ignition capacitor energy through a SBASI for 4th stage motor ignition. For EMI and grounding considerations, the unit is sealed with an EMI gasket and painted with conductive epoxy silver paint.

1.2 TEST EQUIPMENT

1.2.1 Calibration of Equipment - Test equipment is maintained in calibration accuracy through periodic calibration by the Calibration and Support Laboratory in accordance with the requirements of Specification MIL-C-45662A and calibration procedures that are periodically reviewed by NAVPRO Quality Assurance Division Audit Branch.

1.2.2 Measurement Techniques

1.2.2.1 CS01 - Susceptibility signal levels were measured using an HP - 403B AC voltmeter connected to the voltmeter winding of a Solar 6220-1A isolation transformer.

1.2.2.2 CS02 - Susceptibility signal levels were measured using a Fairchild EMC-25 connected across the system input power leads through a 1 uf capacitor as shown in Figure 9. With the EMC-25 set in the peak detector function, both the signal level and frequency at the system power connector could be accurately measured. Since a signal source of much greater than 1 watt of output power was being used, it was also necessary, if any susceptibility was evident, to measure the signal power level being delivered to the test sample. Below 50 MHz, the input power was determined by using the EMC-25 and a PLC-25 current probe to measure the current being supplied to the test sample. (PLC-25 current probe factors are included in Figure 4.) Above 50 MHz, the input power was determined by calculating the impedance to ground of the 1 uf capacitor (all other impedance to ground can be neglected above 50MHz). Using either the current delivered or the impedance to ground, the power being delivered to the test sample was calculated and set to exceed 1 watt.

1.2.2.3 CS06 - Spike amplitudes were measured at the test sample's input power connector using an oscilloscope.

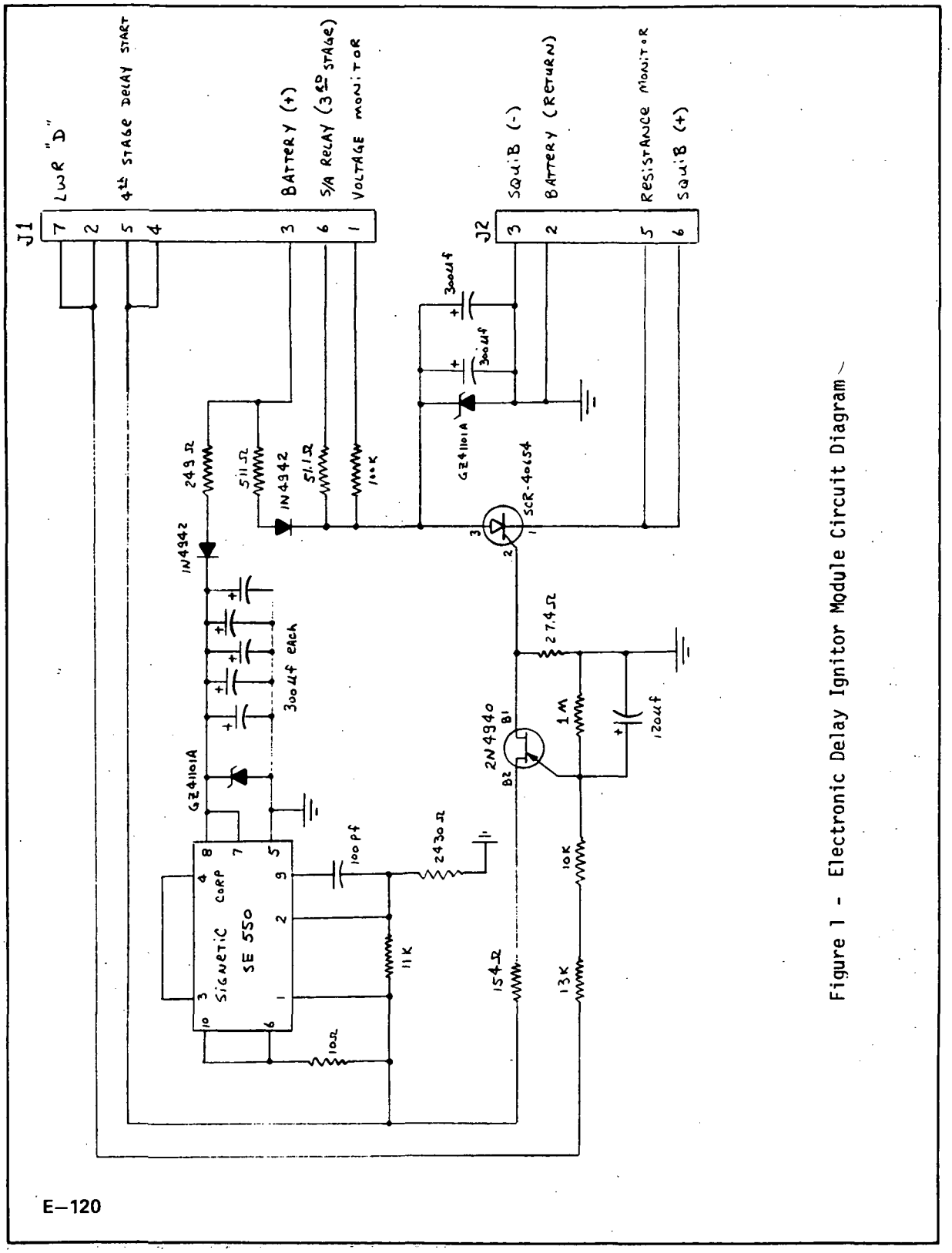

Figure 1 - Electronic Delay Ignitor Module Circuit Diagram

1.2.2.4 RS01 - The magnetic field levels required in Figure 20 of MIL-STD-461A were generated using a loop antenna which was constructed per Figure 1A of MIL-STD-461A. The amplitude and frequency of the current supplied to the loop antenna were measured using a PLC-10 current probe and an EMC-10 receiver. (PLC-10 current probe factors are included in Figure 5.) The current levels used to generate the required fields were as follows:

Frequency	Field (db pT)	Current (Amps)
30 Hz to 100 Hz	160	2.1
100 Hz to 300 Hz	140	.21
300 Hz to 1 KHz	120	$21(10^{-3})$
1 KHz to 3 KHz	100	$2.1(10^{-3})$
3 KHz to 10 KHz	80	$.21(10^{-3})$
10 KHz to 30 KHz	60	$21(10^{-6})$

1.2.2.5 RS02 - Spike amplitudes were measured at the spike generator with an oscilloscope. An RMS ammeter was used to measure the 400 Hz current.

1.2.2.6 RS03 - Between 14 KHz and 1 GHz, an Instruments for Industry EFS-1 field strength meter was was used to measure the radiated field strength. Between 1 GHz and 10 GHz, field strength measurements were made using an EMCO 3102 conical log-spiral antenna, positioned alongside the test sample, and a Singer EMA-910 receiver. Figure 6 contains the applicable antenna factors which were added to the EMA-910 receiver readings to obtain field strength levels.

1.3 TEST ARRANGEMENT

The general arrangement of the test sample, interconnecting cables, and test equipment was as shown in Figure 2. The test sample was bonded to a copper ground plane, 10 mils thick, 12 square feet in area, 30 inches wide, and attached to a wall of the shielded enclosure in three places. The shielded enclosure is a double-walled, solid, shielded enclosure 16 feet wide by 20 feet long. All test equipment was isolated from the ground plane by placing the test equipment cases on a 1/4" phenolic board and by not utilizing a case ground in the power cords. An interconnecting cable approximately 5 feet in length was used from the EDIM to the test monitor panel. This cable was routed within 10±2 cm of the front edge of the ground plane on 2 inch standoffs above the ground plane. The test panel and test equipment wiring is shown in Figure 3.

1.4 CRITERIA FOR SUSCEPTIBILITY

The EDIM was monitored for a pass or fail condition by a counter connected to the test monitor panel. The EDIM was considered as passing the susceptibility tests if the SCR turned on at the preselected time (3.7 seconds) after the start command within the accuracy of the equipment specification (± 0.6 second). The EDIM was considered as failing the susceptibility tests if the SCR turned on without a start command having been given or if the time delay after the start command was outside of the specification limits.

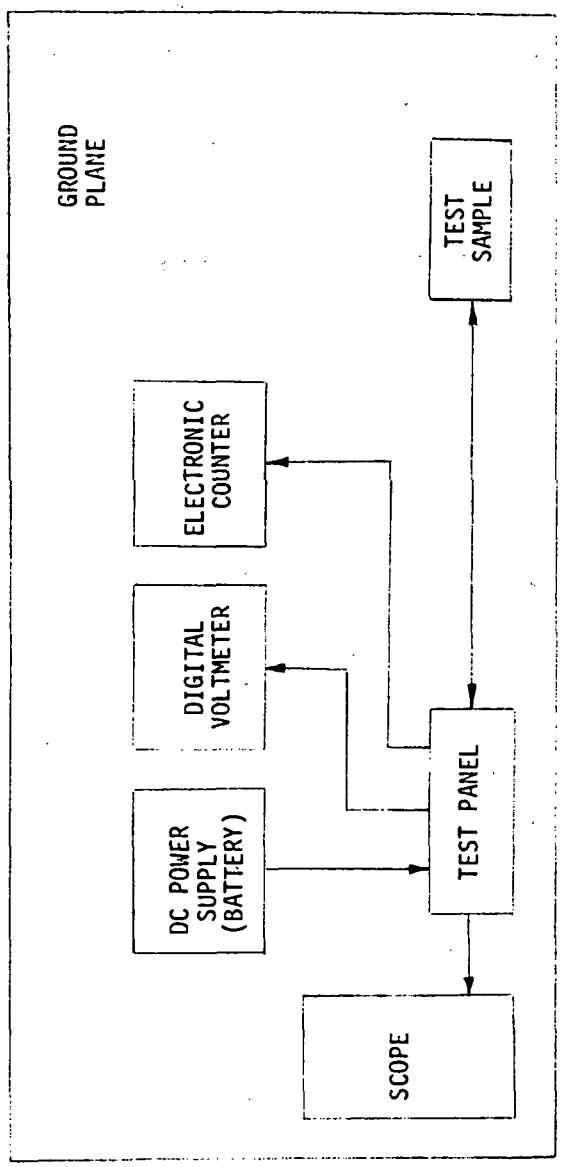

Figure 2 -General Test Set-Up

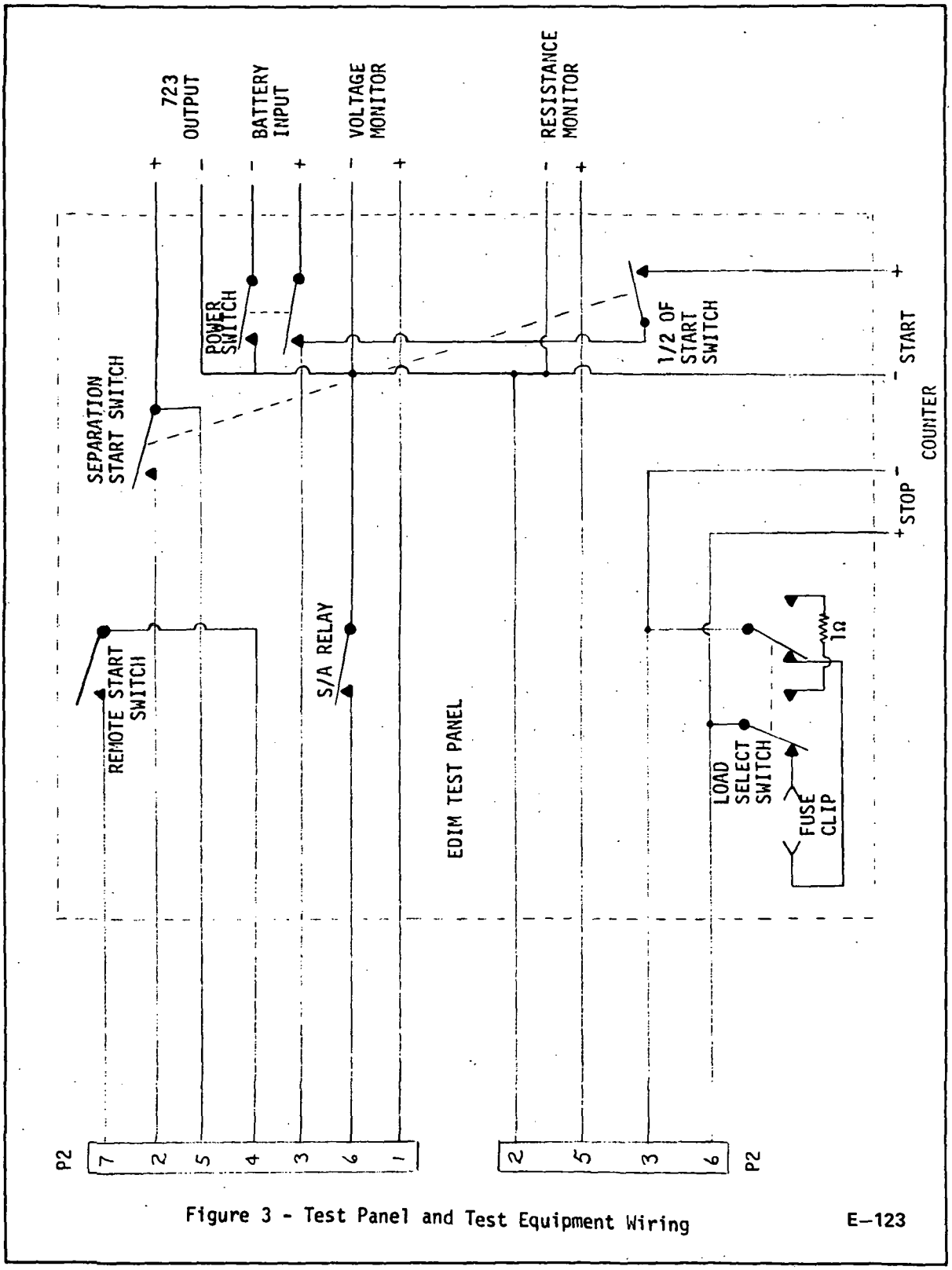

Figure 3 - Test Panel and Test Equipment Wiring E–123

2.0 TESTS PERFORMED

The following tests were performed in the VSD shielded room facility:

MIL-STD-461A Method	Description
CS01	.03 to 50 KHz, Power Leads Susceptibility
CS02	.05 to 400 MHz, Power Leads Susceptibility
CS06	Spike Test, Power Leads Susceptibility
RS01	.03 to 30 KHz, Magnetic Field Susceptibility
RS02	Magnetic Induction, Cable Susceptibility
RS03	150 KHz to 10GHz, System Susceptibility to Radiated Electric Fields

The above tests were performed in accordance with reference (a) using the test methods of MIL-STD-462. A functional performance test was performed prior to commencing each test method, during each test, and after each test method in order to verify proper performance of the test sample. The performance test consisted of the following steps:

1) Verify discharge jumper (J1-2 to J3-2) has been in place for a minimum of 30 seconds.

2) Verify ignition charge voltage has reached a steady state value.

3) Remove discharge jumper.

4) Turn power switch to "OFF" position.

5) After power switch has been in "OFF" position for approximately 1.5 seconds, transfer the start switch to "START" position.

6) Record delay time indication displayed on electronic counter.

3.0 TEST RESULTS

3.1 CS01

The CS01 test was performed on the +30 volt power line with no indication of susceptibility evidenced. The data sheet showing the test frequencies at which functional tests were performed is included as page A-2 of Appendix A.

3.2 CS02

3.2.1 +30 Volt Line - The CS02 test was performed on the +30 volt power line without any incidents of inadvertant firing and with all time delays within specification limits. The time delay did vary from the nominal range of values by as much as 0.14 seconds when test frequencies of 2 MHz, 5 MHz, and 25 MHz were injected. The voltage threshold at which the time delay began to deviate from normal was 110 db uv at each frequency. The test data for these three frequencies is given below, and the data sheets showing the test frequencies at which functional tests were performed is included as pages A-3 and A-4 of Appendix A.

Frequency (MHz)	Signal Level (db uv)	Time Delay (Sec)
2	120	3.623
2	120	3.625
2	110	3.715
2	100	3.723
5	120	3.582
5	120	3.689
5	110	3.710
5	100	3.723
25	120	3.719
25	110	3.718

3.2.2 Ground Line - During CS02 tests on the ground line, several test equipment problems were encountered. Several ground loops were present in the initial test equipment set-up. These ground loops were eliminated by isolating the test equipment cases from the ground plane and by isolating the test equipment power line case ground from the shield room power line safety ground. A regulated DC power supply ceased to operate when the interference signal injected on the ground line reached 25 MHz at a level of 1 volt. This power supply was replaced with a 31 volt battery for the remainder of the tests. One item which was evidence of susceptibility during CS02 tests performed on the ground line was the inability of the test sample to fire at certain test signal frequencies and levels. The only other evidence of susceptibility was a shortening to the time delay at a test frequency signal of 250 MHz. The data for these cases is as follows:

Frequency (MHz)	Signal Level (db uv)	Signal Level (watts)	Time Delay (Sec)
200	110 *	63	-
200	112	100	3.503
200	114	158	-
200	120	628	-

(Continued)

(Continued)

Frequency (MHz)	Signal Level (db uv)	(watts)	Time Delay (Sec)
250	100	7.9	3.723
250	102	12.5	3.719
250	104	19.7	3.717
250	104 *	19.7	3.720
250	105	24.8	2.101
250	106	31.2	1.443
250	107	39.3	1.514
250	110	78.5	1.224
250	120	78.5	-

* Threshold level (Specification limit = 120 db v or 1 watt whichever is less)
\- Did not fire

In all of the above cases, the input RF signal power level was well above 1 watt which, according to paragraph 6.5.1 of MIL-STD-461A, is evidence of compliance with CS02 requirements. Signal power level was maintained at 1 volt utilizing a 1000 watt source. Whenever evidence of susceptibility was noted. The signal power level was measured to assure specification compliance. The data sheets showing the test frequencies at which functional tests were performed are included as pages A-5 and A-6 of Appendix A.

3.3 CS06

3.3.1 Required Tests - The CS06 test was performed using the test set-up and methods of reference (a) and MIL-STD-462 with no indication of susceptibility evidenced. The data sheet for this test is included as page A-7 of Appendix A.

3.3.2 Additional Tests - Since the choke in the positive DC power line used in the MIL-STD-462 CS06 test method would not be present in the actual installation of the test sample, additional CS06 tests were performed using parallel injection on the DC power lines without using the choke in the positive power line. Using configuration, the ignition system fired at a spike level of +18 volts measured with the spike generator connected to the power lines. There was no sensitivity to pulse repetition rate. It was discovered that the most effective method of modifying the test sample to make it less sensitive to conducted spikes was to add a series choke in the line connected to P2-6 of the test sample. Using a 120 uh choke, the ignition system fired at a spike voltage of -40 volts and had a time delay of 2.895 seconds (outside specification limits) at a spike voltage of +60 volts. Using a 700 uh choke, the ignition system would not fire inadvertently at spike voltages up to ±100 volts, although, the time delay was still affected, as shown below (all spike repetition rates were 10 PPS).

Spike Level (Volts)	Time Delay (Sec)
+20	3.664
+20	3.720
+20	3.721
+25	3.658
+25	3.628
+30	3.499
+35	3.382

(Continued)

(Continued)

Spike Level (Volts)	Time Delay (Sec)
+40	3.261
+45	3.147
+50 *	3.135
+60	2.908
+60	2.775
-60	3.720

* Threshold level. (Spec. limit = ±60v)

3.4 RS01 - The RS01 test was performed on the test sample case (two axis) and connectors with the radiating loop antenna oriented as shown in Figure 13. No indication of susceptibility was evidenced. The data sheet showing the test frequencies at which functional tests were performed is indicated as page A-9 of Appendix A.

3.5 RS02 - The RS02 test was performed on the test sample case and cable using both spikes and 400 Hz current as the field source. No evidence of susceptibility was indicated. The data sheet showing the field source levels at which functional tests were performed is included as page A-10 of Appendix A.

3.6 RS03 - The RS03 test was performed with no indication of susceptibility evidenced at a field strength of 1 volt/meter. It was necessary to add a band rejection filter on the electronic counter start gate line when tests were conducted between 47 MHz and 220 MHz due to the fact that the counter start gate was susceptible to noise being picked up on its start gate input line. A field strength of 10 volts/meter was maintained for most RS03 tests with only isolated cases of variations in time delay. At no test frequency, even at a field strength of 10 volts/meter, was the time delay outside of the specified duration. The data sheets showing the test frequencies and field strength levels at which functional tests were performed are included as pages A-11 and A-12 of Appendix A.

4.0 CONCLUSIONS

The Electronic Ignition Delay Module met all of the susceptibility requirements of MIL-STD-461A, Notice 1, with all system performance within the equipment specification limits. Although the test sample met the specification requirements, a potential problem does exist in the area of spike voltages conducted on the input power lines. The spike amplitudes at which inadvertent firing occured during the tests detailed in paragraph 3.3.2 are well within the range which could be expected to be generated if any other equipment were being operated on the same power bus. Accordingly, the strictest control must be exercised over the ignition system power lines, both positive and return, to prevent the generation of voltage transients. This control should consist of the prohibition of the addition of any voltage transient producing circuitry, both in the present design and in the future, to the ignition system power lines; and the isolation of the return line from the vehicle chassis ground, i.e., using a return wire to the low side of the ignition system battery.

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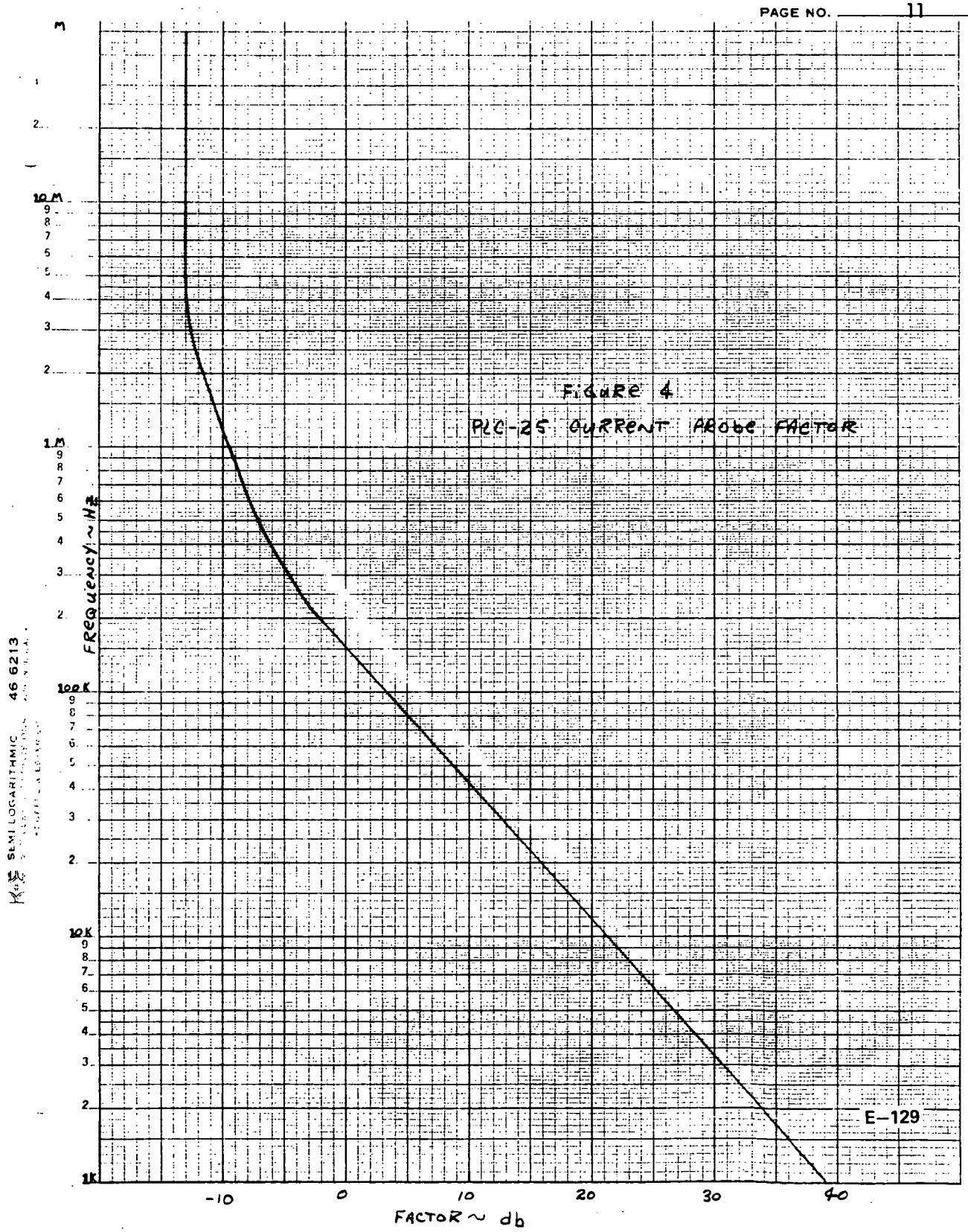


Figure 4

PLC-25 CURRENT PROBE FACTOR

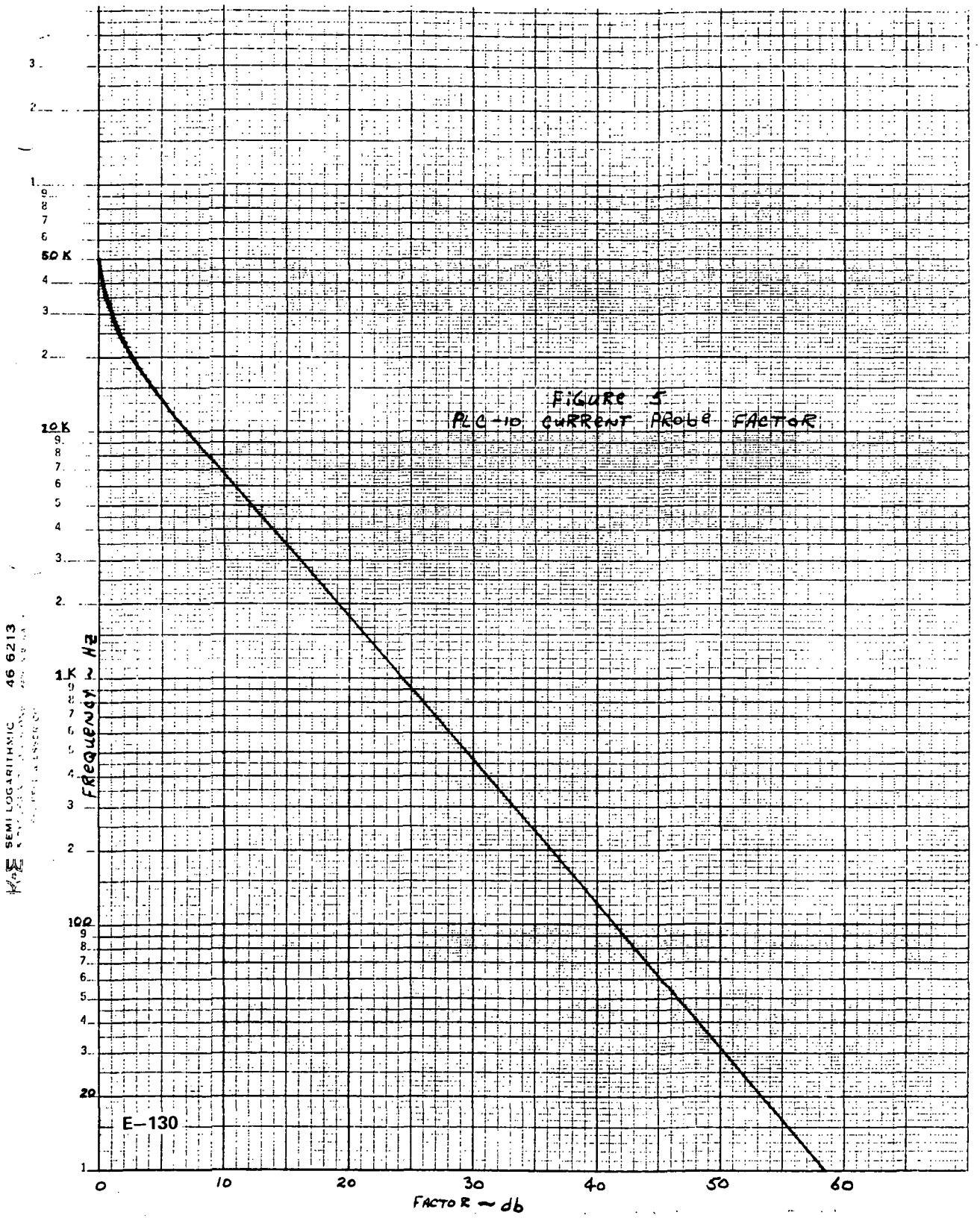


FIGURE 5
PLC-10 CURRENT PROBE FACTOR

Frequency (G Hz)	Antenna Factor (db)
1	26.3
2	31.8
3	36.4
4	39.0
5	39.8
6	42.6
7	43.5
8	45.2
9	46.2
10	49.0

Figure 6 - EMCO 3102 Antenna Factors

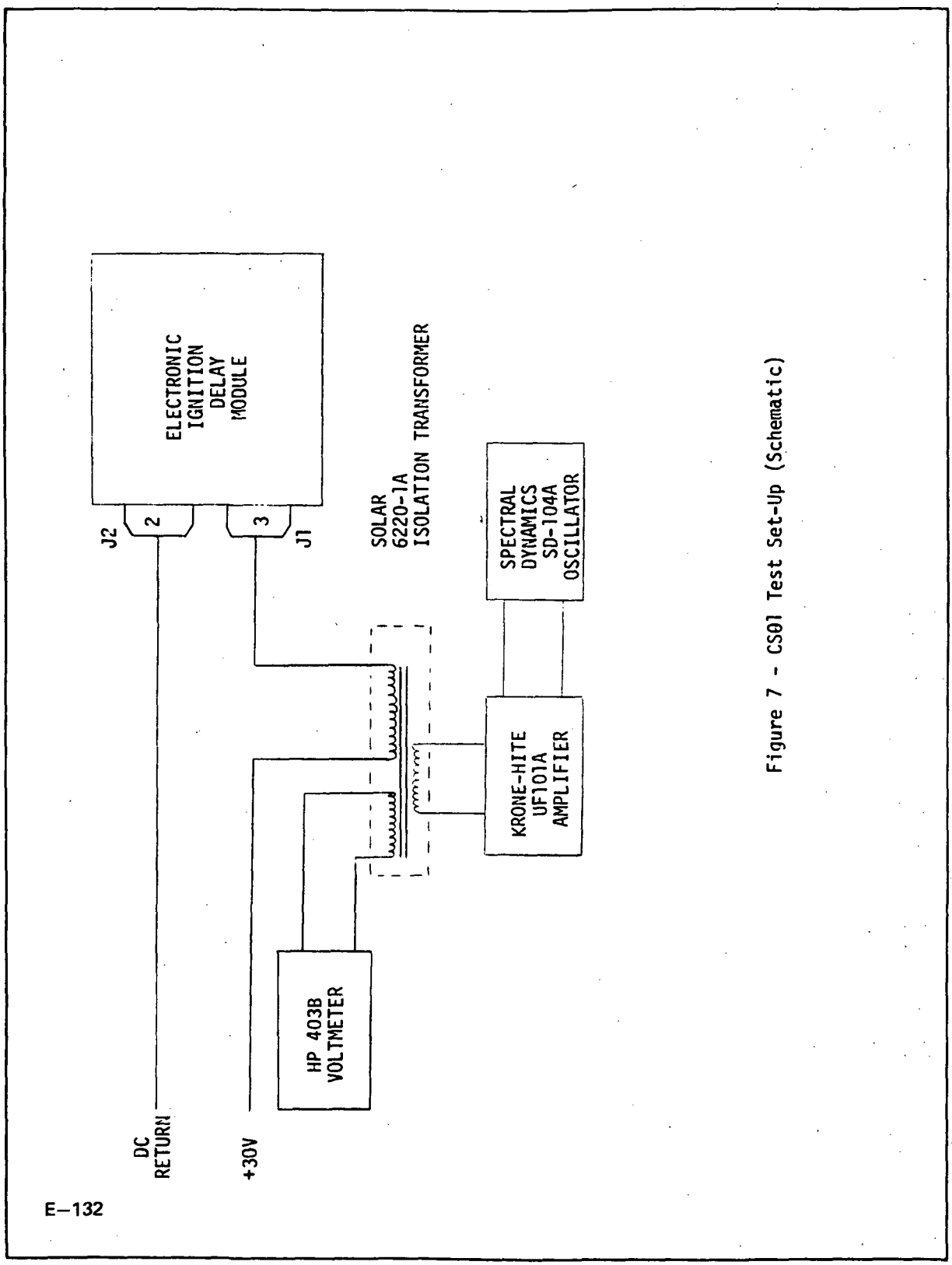


Figure 7 - CS01 Test Set-Up (Schematic)

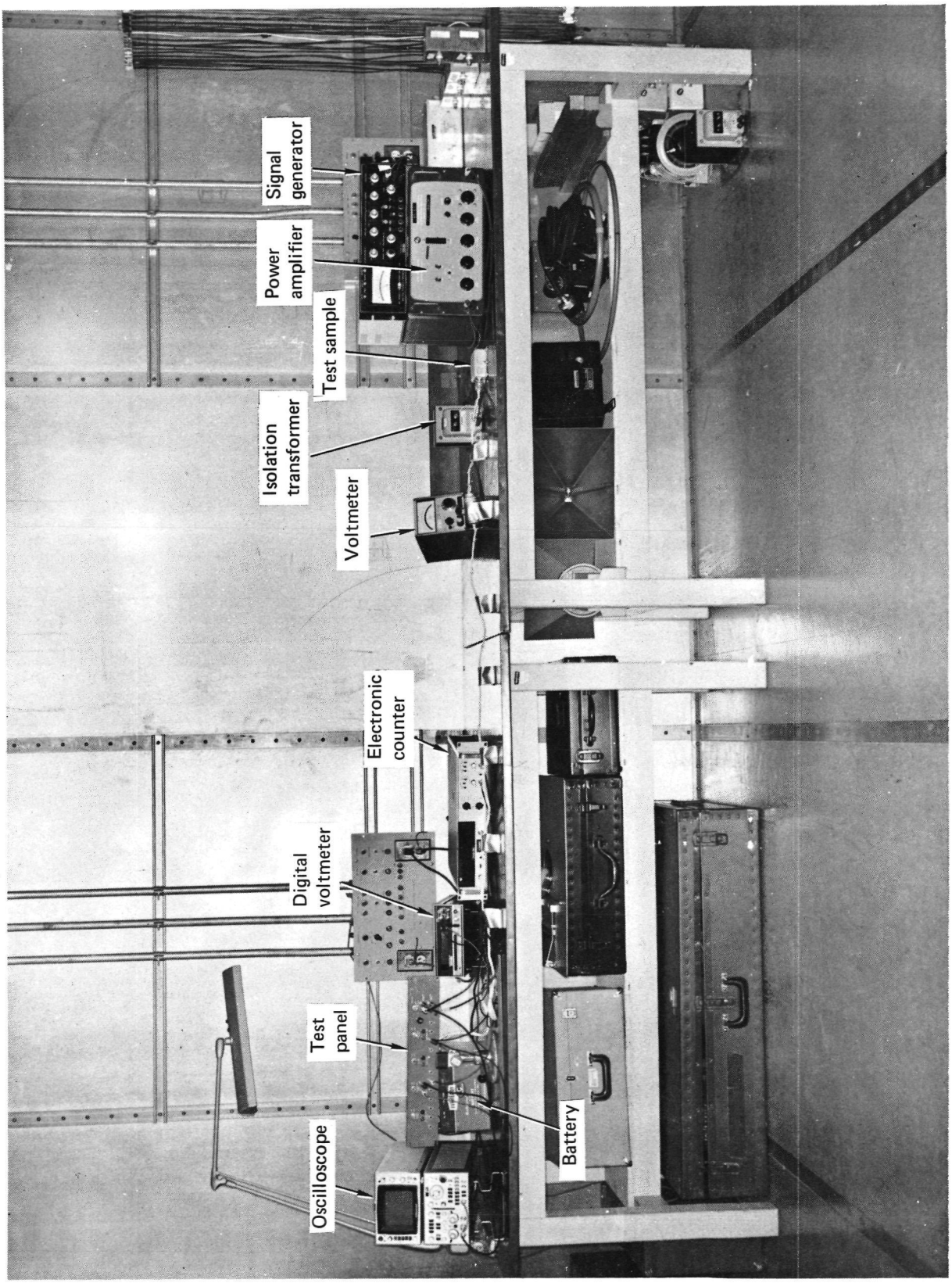


FIGURE 8. – CS01 TEST SET-UP (PICTURE)

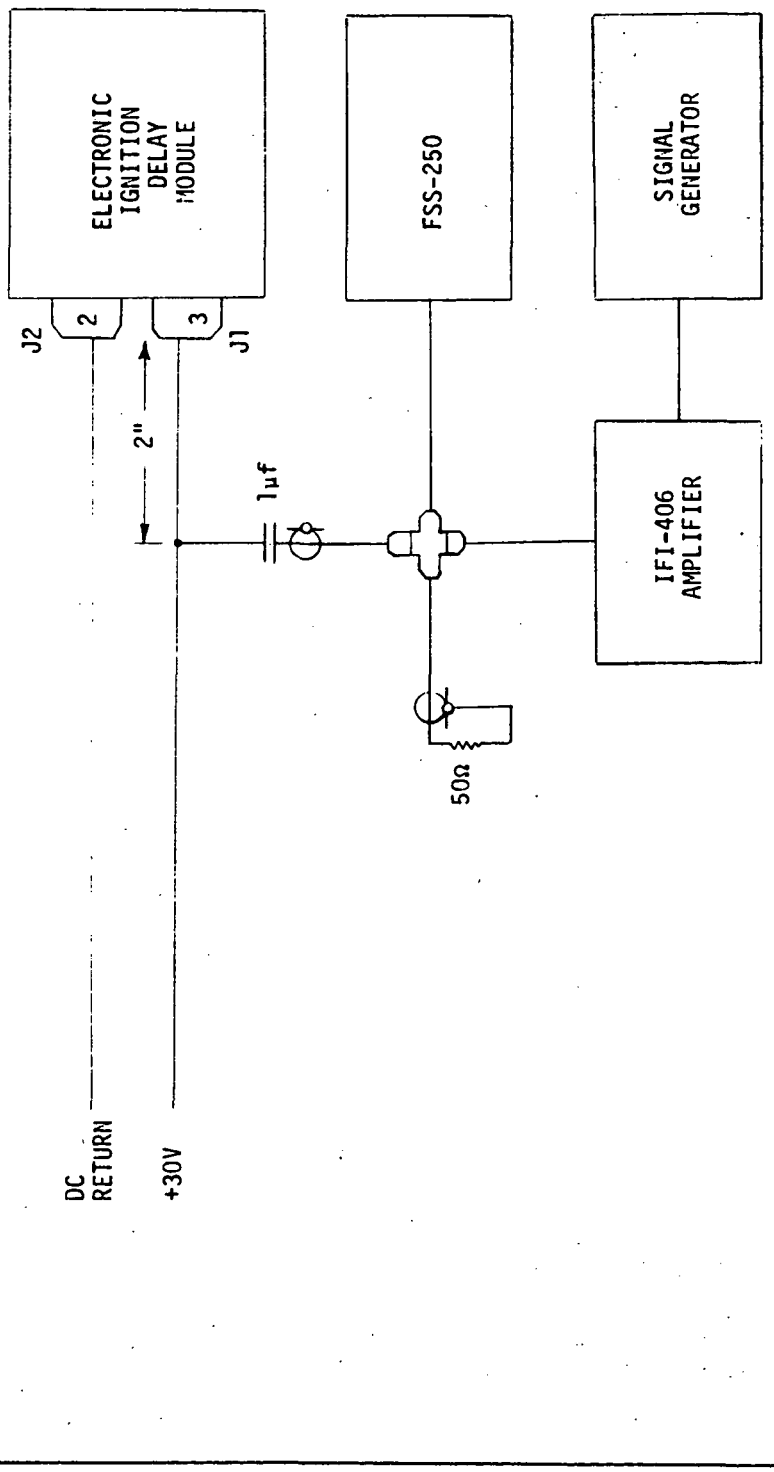


Figure 9 - CS02 Test Set-Up (Schematic)

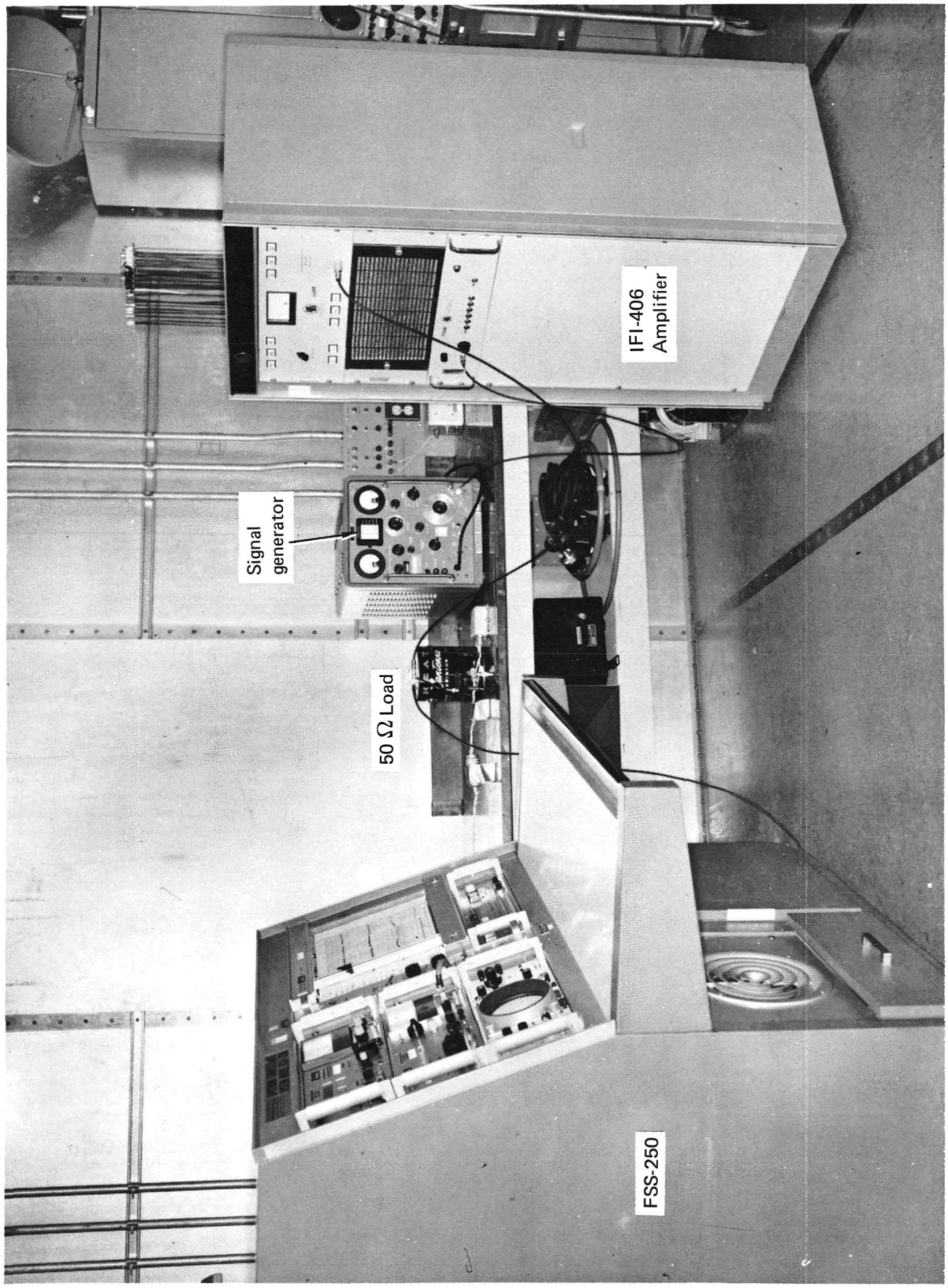


FIGURE 10. – CS02 TEST SET-UP (PICTURE)

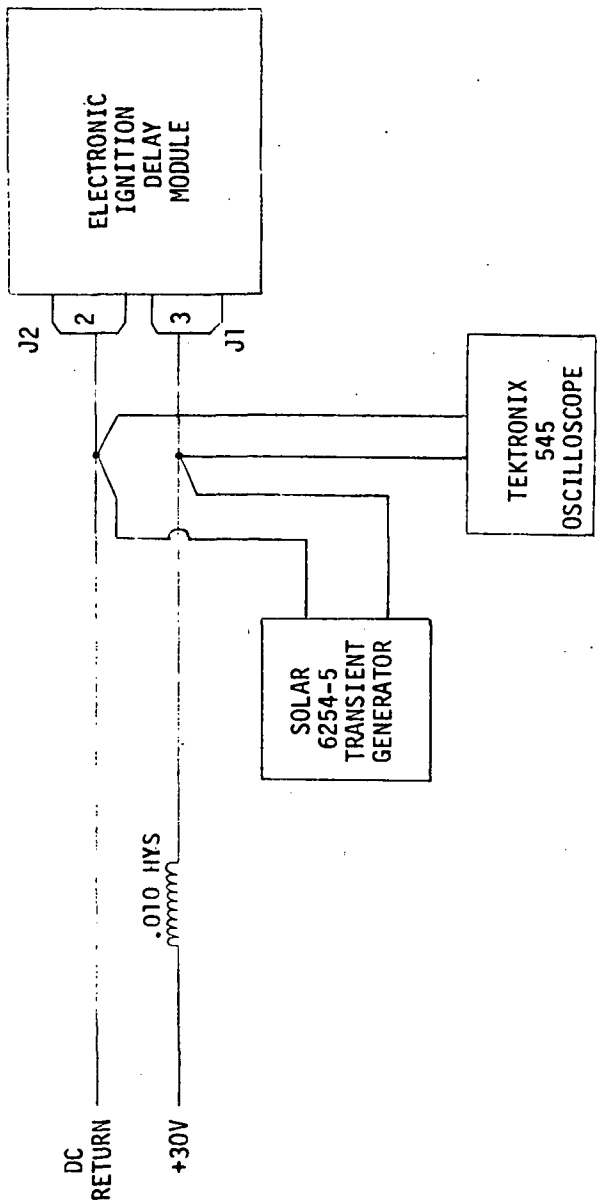


Figure 11 - CS06 Test Set-Up (Schematic)

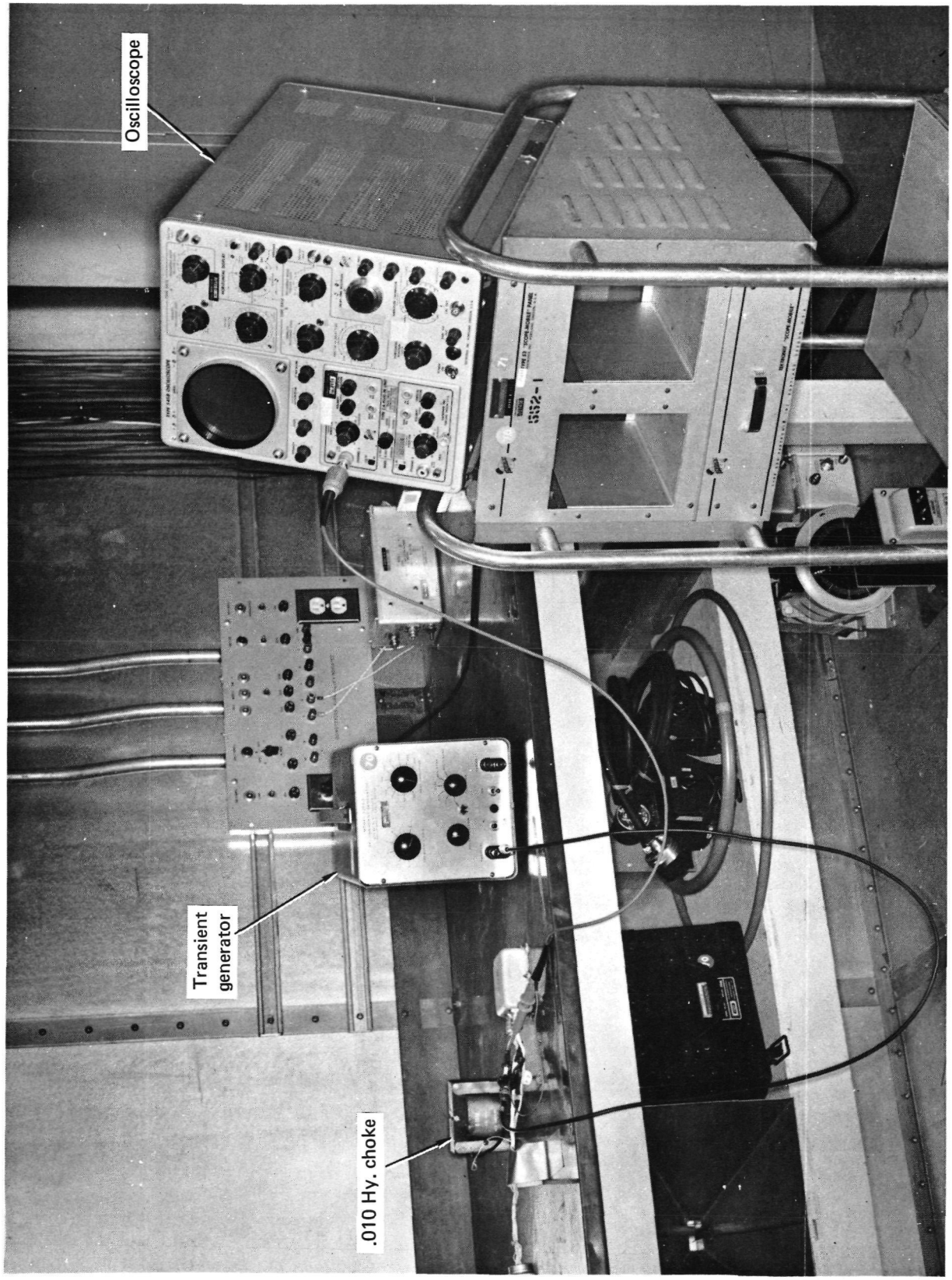
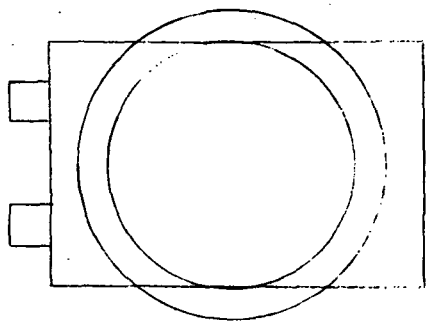
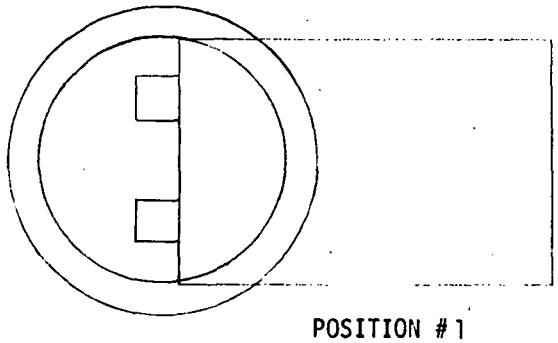


FIGURE 12. – CS06 TEST SET-UP (PICTURE)



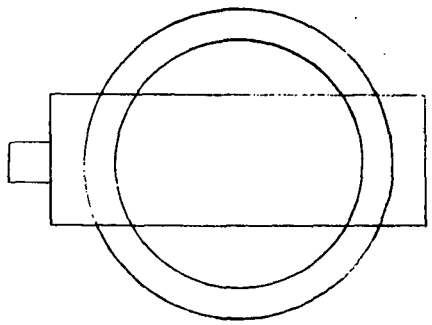
TOP VIEW

POSITION # 3



TOP VIEW

POSITION # 1



SIDE VIEW

POSITION # 2

Figure 13 - RS01 Antenna Positions

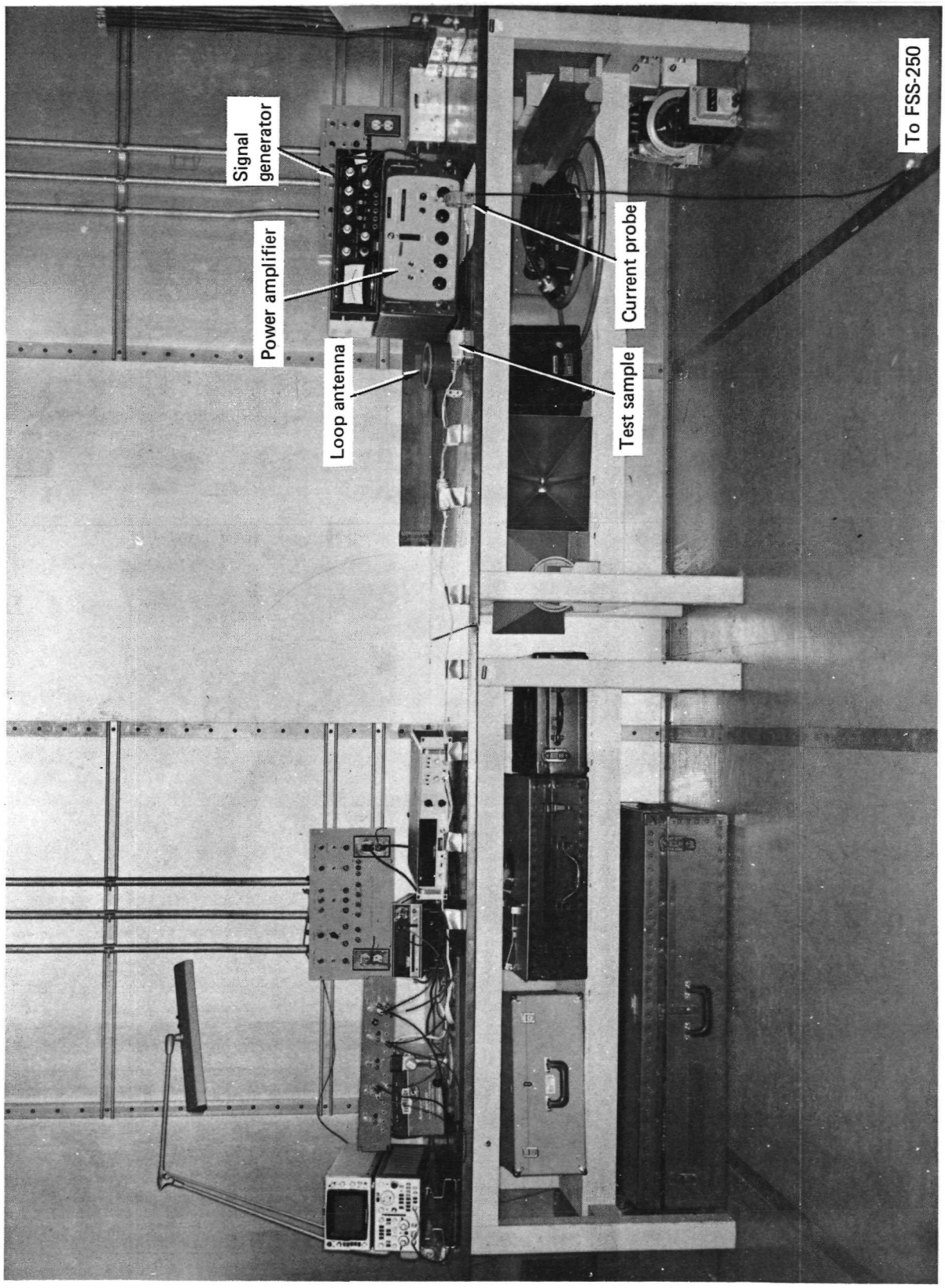


FIGURE 14. – RS01 TEST SET-UP (PICTURE)

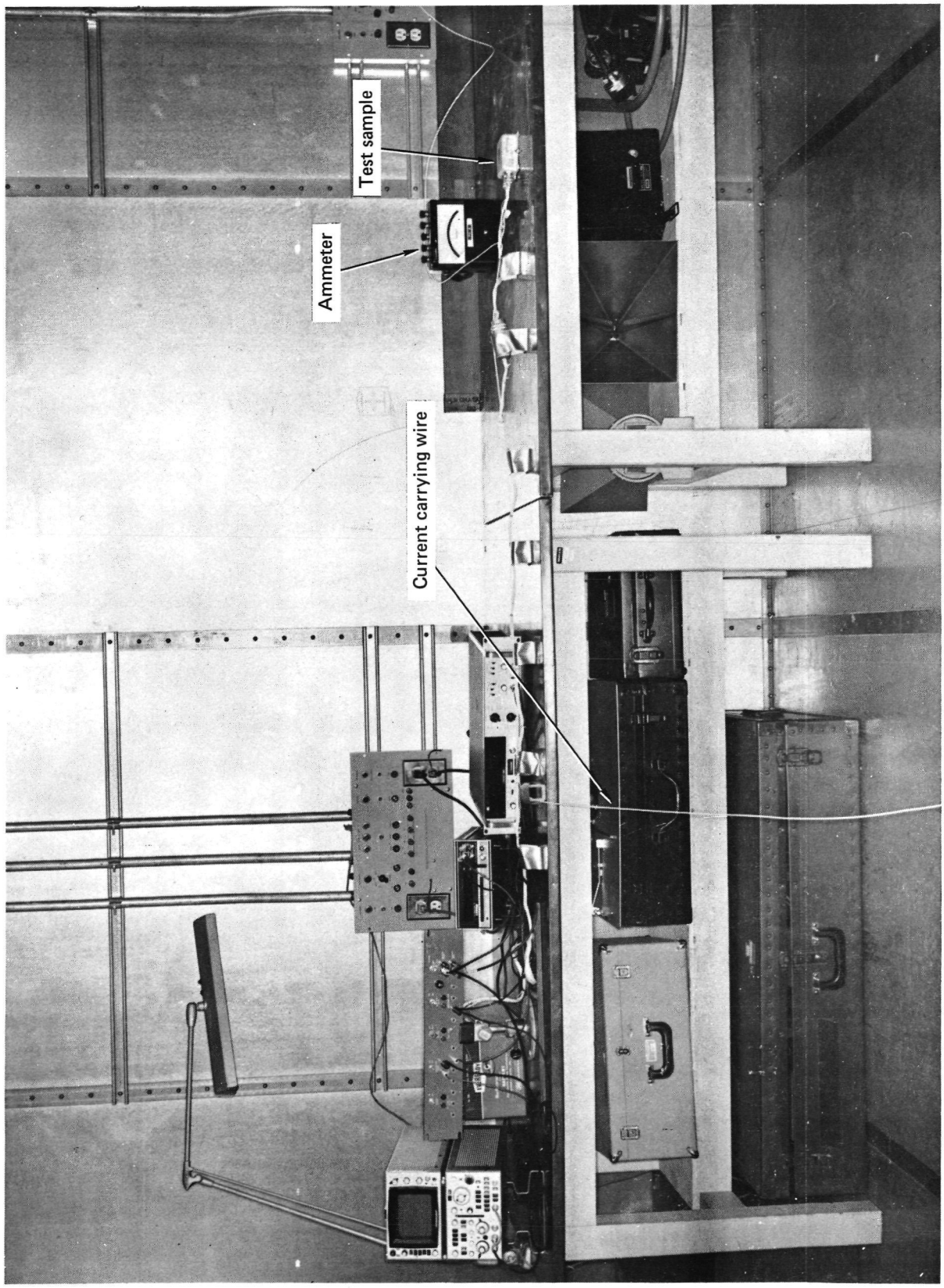


FIGURE 15. – RS02 TEST SET-UP (PICTURE)

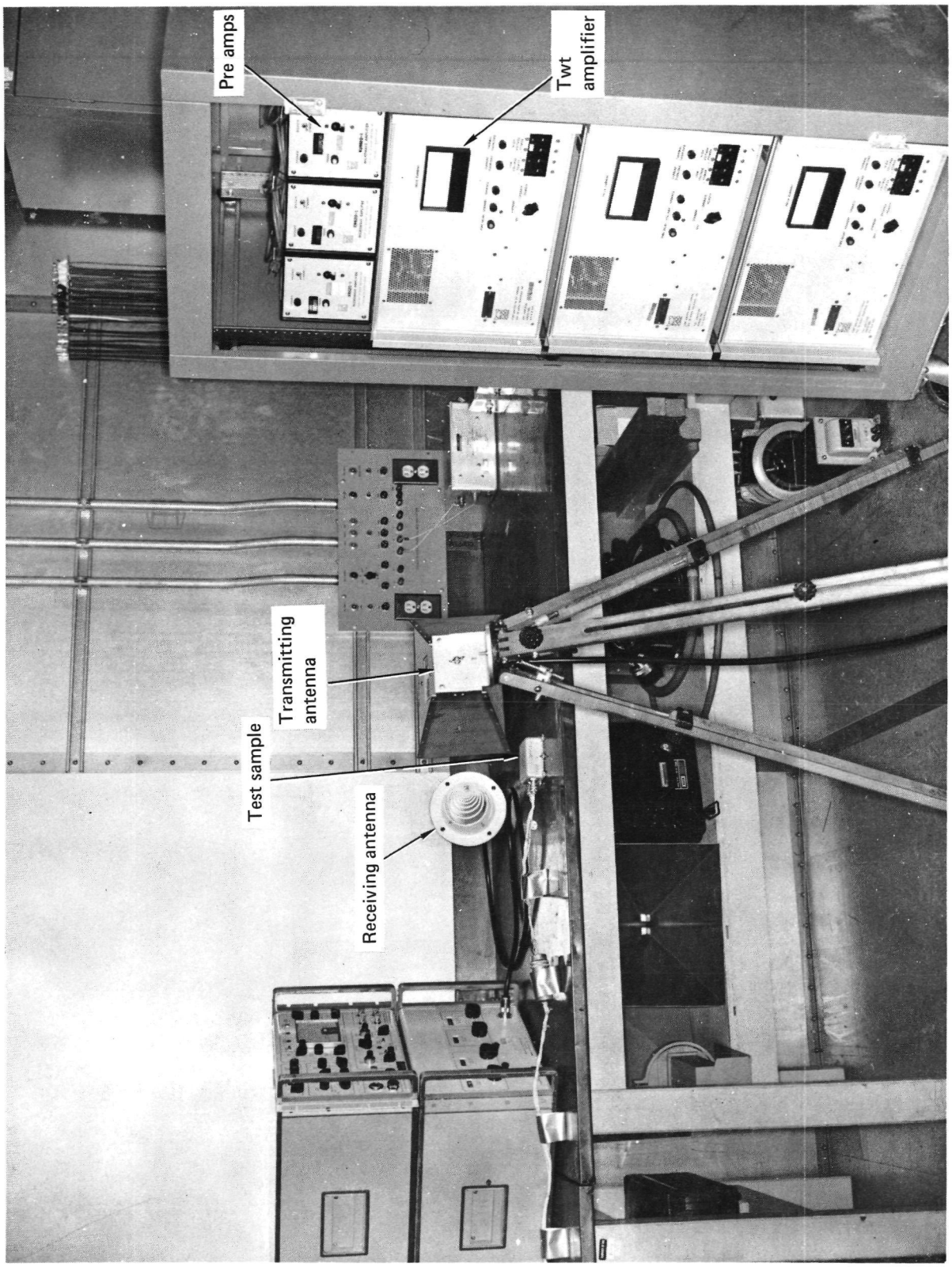


FIGURE 16. — RS03 TEST SET-UP (PICTURE)

APPENDIX A

DATA SHEETS

DESCRIPTION OF TEST SAMPLE (Nomenclature, Model No., Serial No.)

TYPE OF SUSCEPTIBILITY TEST	TEST SIGNAL APPLIED TO:	TEST PERFORMED BY - Date	TEST SPECIFICATION
CS01	+30V LINE	C.L. DYER	-461

TEST FREQ.	APPL'D SIGNAL LEVEL	THRESH-OLD	SPEC. LIMIT	CIRCUIT OR OUTPUT MONITORED	SENS. OF MONITOR	RESPONSE OBSERVED Ignition Time Delay sec.		REMARKS
——	——	——						NORMAL OUTPUT
~~4~~						3.723		PRE CS01
400	3V					3.723		
2K	3V					3.722		
10K	3V					3.722		
25K	3V					3.725		
50K	3V					3.724		
—						3.726		POST CS01

NOTES:

A. No change in normal output response directly due to the applied signal was observed over the frequency range indicated.

B. Deviations observed in monitored circuit response resulting from the applied signal voltage were detectable over the frequency range indicated.

ABBREVIATIONS:

MDR - Minimum Discernible Response

DESCRIPTION OF TEST SAMPLE (Nomenclature, Model No., Serial No.)
TDG DELAY ASSY 23-004349-1 QUAL 002

TYPE OF SUSCEPTIBILITY TEST	TEST SIGNAL APPLIED TO:	TEST PERFORMED BY - Date	TEST SPECIFICATION
CS02 (C=1mf)	+30 V Line	C.L. DYER	-461

TEST FREQ.	APPL'D SIGNAL LEVEL	THRESH-OLD	SPEC. LIMIT	CIRCUIT OR OUTPUT MONITORED	SENS. OF MONITOR	RESPONSE OBSERVED Ignition Time Delay sec.		REMARKS
———	———	———				3.726		NORMAL OUTPUT
150K	120db					3.724		
500K	120db					3.723		
2m	120db					3.623		DELAY WITHIN SPEC
2m	120db					3.625		DELAY WITHIN SPEC
2m	0db					3.724		
2m	110db	110db				3.715		
2m	100db					3.723		
2.5m	120db					3.691		
2.5m	110db					3.721		
1.8m	120db					3.698		
1.8m	110db					3.722		
m	100db					3.723		
5m	110db	110db				3.710		
5m	120db					3.582		
5m	120db					3.689		
10m	120db					3.719		
25m	110db	110db				3.718		
25m	120db					3.672		
65m	120db					3.764		
65m	110db					3.726		
400m	120db					3.722		
350m	120db					3.723		
300m	120db					3.721		
250m	120db					3.722		
100m	120db					3.722		

NOTES:

A. No change in normal output response directly due to the applied signal was observed over the frequency range indicated.

B. Deviations observed in monitored circuit response resulting from the applied signal voltage were detectable over the frequency range indicated.

120 db = 1V

ABBREVIATIONS:

E—144

MDR – Minimum Discernible Response

DESCRIPTION OF TEST SAMPLE (Nomenclature, Model No., Serial No.)

TYPE OF SUSCEPTIBILITY TEST	TEST SIGNAL APPLIED TO:	TEST PERFORMED BY – Date	TEST SPECIFICATION
CS02 (1uf cap)	+30v Line	C.L DYER 5-20-75	-461

TEST FREQ.	APPL'D SIGNAL LEVEL	THRESHOLD	SPEC. LIMIT	CIRCUIT OR OUTPUT MONITORED	SENS. OF MONITOR	RESPONSE OBSERVED Ignition Time Delay sec.		REMARKS
———	———	———						NORMAL OUTPUT
150 m	120db					3.723		
200m	120db					3.717		
—	—					3.729		Post CS02

NOTES:

A. No change in normal output response directly due to the applied signal was observed over the frequency range indicated.

B. Deviations observed in monitored circuit response resulting from the applied signal voltage were detectable over the frequency range indicated.

ABBREVIATIONS:

MDR = Minimum Discernible Response

DESCRIPTION OF TEST SAMPLE (Nomenclature, Model No., Serial No.)

TYPE OF SUSCEPTIBILITY TEST: CS02 (CEIMF)				TEST SIGNAL APPLIED TO: GND Line		TEST PERFORMED BY - Date: C.L. DYER		TEST SPECIFICATION: - 461
TEST FREQ.	APPL'D SIGNAL LEVEL	THRESH-OLD	SPEC. LIMIT	CIRCUIT OR OUTPUT MONITORED	SENS. OF MONITOR	RESPONSE OBSERVED Ignition Time Delay Sec.		REMARKS
——	——	——				3.719		NORMAL OUTPUT
50K	120db					3.711		
73K	118db	118db	120db			—		CAPACITOR DISCHARGED
—	(GROUND LOOPS IN TEST EQUIPMENT)							I = 121 db μA @ 73KHz
73K	120db	(GRND Loop Eliminated)				3.725		
73K	120db					3.725		
150K	120db					3.716		
500K	120db					3.721		
2M	120db					3.719		
5M	120db					3.698		
10M	120db					3.715		
25M	120db					3.710		CLAMPED Beam Power
50M	120db					3.737		SUPPLY TO BATTERY
100M	120db					3.720		31V
150M	120db					3.719		
200M	120db					—	©	P=124dBμW INTO 50Ω WONT FIRE
200M	112db	112db				3.503		
200M	114db					—	©	WONT FIRE
200M	110db					3.701		
200M	108					3.705		
200M	105					3712		
200M	100					3714		
200M	90					3721		
200M	120db					3.522		
200M	120db					3.487		
200M	120db					3.513		

NOTES:

A. No change in normal output response directly due to the applied signal was observed over the frequency range indicated.

B. Deviations observed in monitored circuit response resulting from the applied signal voltage were detectable over the frequency range indicated.

© Removed GND Power wire from bundle, problem eliminated.

ABBREVIATIONS:

E-146

MDR - Minimum Discernible Response

DESCRIPTION OF TEST SAMPLE (Nomenclature, Model No., Serial No.)

TYPE OF SUSCEPTIBILITY TEST: CS02	TEST SIGNAL APPLIED TO: GND Line	TEST PERFORMED BY - Date: C.L. DYER	TEST SPECIFICATION: -461

TEST FREQ.	APPL'D SIGNAL LEVEL	THRESH-OLD	SPEC. LIMIT	CIRCUIT OR OUTPUT MONITORED	SENS. OF MONITOR	RESPONSE OBSERVED Ignition Time Delay sec.		REMARKS
———	———	———						NORMAL OUTPUT
200m	120db					3.490		
200m	110db	110db				3.689		
200m	105db					3.710		
250m	120db					—		no fire
250m	110db					1.224		
250m	100db					3.723		
250m	105db					2.101		
250m	102db					3.719		
250m	107db					1.514		
250m	104db					3.717		
75m	106db					1.443		
0m	104db	104db				3.720		
300m	120db					3.726		
250m	120db					3.676		
250m	120db					2.835		
250m	120db					3.648		
250m	120db					3.656		
350m	120db					3.718		
350m	120db					3.723		
400m	120db					3.666		
400m	120db					3.709		
400m	120db					3.699		
200m	105db					3.699		
200m	108db					3.649		
200m	110db							won't fire

NOTES:

A. No change in normal output response directly due to the applied signal was observed over the frequency range indicated.

B. Deviations observed in monitored circuit response resulting from the applied signal voltage were detectable over the frequency range indicated.

ABBREVIATIONS:

MDR - Minimum Discernible Response

DESCRIPTION OF TEST SAMPLE (Nomenclature, Model No., Serial No.)

TYPE OF SUSCEPTIBILITY TEST	TEST SIGNAL APPLIED TO:	TEST PERFORMED BY - Date	TEST SPECIFICATION
CS06	DC Power Lines	C.L. DYER 5-27-75	-461

TEST FREQ.	APPL'D SIGNAL LEVEL	THRESH-OLD	SPEC. LIMIT	CIRCUIT OR OUTPUT MONITORED	SENS. OF MONITOR	RESPONSE OBSERVED Ignition Time Delay sec.		REMARKS
———	———	———						NORMAL OUTPUT
10 PPS	+60V	—	+60V			3.724		
10 PPS	-60V	-	-60V			3.668		
10 PPS	-60V		-60V			3.723		

NOTES:

A. No change in normal output response directly due to the applied signal was observed over the frequency range indicated.

B. Deviations observed in monitored circuit response resulting from the applied signal voltage were detectable over the frequency range indicated.

C. TEST SET-UP PER MIL-STD-462

ABBREVIATIONS:

E-148

MDR - Minimum Discernible Response

DESCRIPTION OF TEST SAMPLE (Nomenclature, Model No., Serial No.)

TYPE OF SUSCEPTIBILITY TEST: CS06 | TEST SIGNAL APPLIED TO: Power Lines (PARALLEL INJECTION) | TEST PERFORMED BY - Date: CL. DYER 5-2 | TEST SPECIFICATION: -75- -461

TEST FREQ.	APPL'D SIGNAL LEVEL	THRESH-OLD	SPEC. LIMIT	CIRCUIT OR OUTPUT MONITORED	SENS. OF MONITOR	RESPONSE OBSERVED Ignition Time Delay sec.		REMARKS
———	———	———						NORMAL OUTPUT
10PPS	+60V	ON	+30V	DC Line		2.908	700uh choke in P2-6 Line	
"	"					2.881		"
"	"					2.874		"
"	"					2.775		"
"	"					2.878		"
10PPS	-60V	ON	+30V	DC Line		3.720		"
10PPS	+60V		"			2.895	120 uh	Choke in P2-6 Line
"	-40V	-40V	"				Fires	"
"	-35	-35				3.667	120 uh	CHOKE IN P2-6 LINE
10PPS	+100V	3	700uh	Choke in P2-6 wire				
PPS	-100V	3	WILL	NOT FIRE INADVERTENTLY				
—	—					3.722		
10PPS	+50V	ON	+30V	Line		3.135	700uh choke in P2-6 Line	
"	+45V		"			3.147		"
"	+40V		"			3.261		"
"	+35V		"			3.382		"
"	+30V		"			3.493		"
"	+20V		"			3.664		"
"	+20V		"			3.720		"
"	+20V		"			3.721		"
"	+25V		"			3.658		"
"	+25V		"			3.628		"

NOTES:

A. No change in normal output response directly due to the applied signal was observed over the frequency range indicated.

B. Deviations observed in monitored circuit response resulting from the applied signal voltage were detectable over the frequency range indicated.

C. NO CHOKE IN +30VDC LINE.
D. 50% AMPLITUDE ON OVERSHOOT.

ABBREVIATIONS:

MDR - Minimum Discernible Response

DESCRIPTION OF TEST SAMPLE (Nomenclature, Model No., Serial No.)

TYPE OF SUSCEPTIBILITY TEST	TEST SIGNAL APPLIED TO:	TEST PERFORMED BY - Date	TEST SPECIFICATION
RS01	—	C C. DYER 5-29-75	- 461

TEST FREQ.	APPL'D SIGNAL LEVEL	THRESHOLD	SPEC. LIMIT	CIRCUIT OR OUTPUT MONITORED	SENS. OF MONITOR	RESPONSE OBSERVED (Ignition Time Delay sec.)		REMARKS
———	———	———						NORMAL OUTPUT
30Hz	125db					3.724		Pos. #1
"	"					3.724		Pos #2
"	"					3.722		Pos #3
300Hz	115db					3.723		Pos #1
"	"					3.723		Pos #2
"	"					3.723		Pos #3
500Hz	112db					3.723		Pos #1
"	"					3.724		Pos #2
"	"					3.724		Pos #3
1000Hz	106db					3.723		Pos #1
"	"					3.723		Pos #2
"	"					3.724		Pos #3
2000Hz	100db					3.724		Pos #1
"	"					3.725		Pos #2
"	"					3.724		Pos #3
3000Hz	100db					3.724		Pos #1
"	"					3.724		Pos #2
"	"					3.723		Pos #3
6000Hz	91					3.724		Pos #1
6KHz	"					3.724		Pos #2
"	"					3.726		Pos 3 #3
10K	87					3.725		Pos #1
"	"					3.725		Pos #2
"	"					3.724		Pos #3
20K	83					3.724		Pos #1
"	NOTES:					3.724		#2
"	"					3.725		#3

A. No change in normal output response directly due to the applied signal was observed over the frequency range indicated.

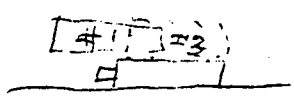
B. Deviations observed in monitored circuit response resulting from the applied signal voltage were detectable over the frequency range indicated.

20K	82	3.724	#1
"	"	3.724	#2
"	ABBREVIATIONS:	3.724	#3

E–150

MDR – Minimum Discernible Response

Sweeping on Position #1



DESCRIPTION OF TEST SAMPLE (Nomenclature, Model No., Serial No.)

E OF SUSCEPTIBILITY TEST	TEST SIGNAL APPLIED TO:	TEST PERFORMED BY – Date	TEST SPECIFICATION
RS02	—	C.L.DYER 5-28-75	461

TEST FREQ.	APPL'D SIGNAL LEVEL	THRESH-OLD	SPEC. LIMIT	CIRCUIT OR OUTPUT MONITORED	SENS. OF MONITOR	RESPONSE OBSERVED Ignition Time Delay sec.		REMARKS
——	——	—— *						NORMAL OUTPUT
10 PPS	+200 V					3.678		CABLE
10 PPS	+100 V					3.724		
10 PPS	+80 V					3.722		
10 PPS	+65 V					3.566		
500 PPS	+80 V					3.712		
200 PPS	+150 V					3.701		
150 PPS	+150 V					3.708		
10 PPS	-200 V					3.723		
500 PPS	-80 V					3.718		CABLE
500 PPS	+80 V					3.723		CASE
PPS	-80 V					3.720		
10 PPS	-200 V					3.720		
10 PPS	+200 V					3.722		CASE
20 AMPS	400 Hz					3.726		CABLE
"	"					3.723		CABLE
"	"					3.722		CASE

NOTES:

A. No change in normal output response directly due to the applied signal was observed over the frequency range indicated.

B. Deviations observed in monitored circuit response resulting from the applied signal voltage were detectable over the frequency range indicated.

* 100 VOLTS CALCULATED INTO 5Ω. 200 V WITH WIRE ONLY. ALL MEASUREMENTS ARE MADE WITHOUT 5Ω RESISTOR.

ABBREVIATIONS:

M D R – Minimum Discernible Response

DESCRIPTION OF TEST SAMPLE (Nomenclature, Model No., Serial No.)

E OF SUSCEPTIBILITY TEST: RS03	TEST SIGNAL APPLIED TO: —	TEST PERFORMED BY - Date: C.L.DYER 5-27-75	TEST SPECIFICATION: 4-61

TEST FREQ.	APPL'D SIGNAL LEVEL	THRESH-OLD	SPEC. LIMIT	CIRCUIT OR OUTPUT MONITORED	SENS. OF MONITOR	RESPONSE OBSERVED: Ignition Time Delay sec.		REMARKS
———	———	———						NORMAL OUTPUT
17K	7V/m					3.726		
25K	5V/m					3.723		
50K	7V/m					3.724		
100K	10V/m					3.725		
200K	7V/m					3.725		
500K	7.5V/m					3.724		
1M	7.5					3.725		
2M	10					3.726		
5M	10					3.725		
10M	10					3.725		
15M	10					3.725		
20M	10					3.350		
30M	1.0					3.726		
30M	5	5				3.688		
30M	8					3.634		
42M	9					3.724		
—	—					3.724	← ADDED REJECTION FILTER	
47M	10					3.717	ON COUNTER START LINE.	
65M	10					3.671		
65M	10					3.659		
65M	3					3.710		
65M	1					3.720		
100M	10					3.717		
140M	10					3.741		
180M						3.724		

NOTES:

A. No change in normal output response directly due to the applied signal was observed over the frequency range indicated.

B. Deviations observed in monitored circuit response resulting from the applied signal voltage were detectable over the frequency range indicated.

ABBREVIATIONS:

E—152

MDR – Minimum Discernible Response

DESCRIPTION OF TEST SAMPLE (Nomenclature, Model No., Serial No.)

E OF SUSCEPTIBILITY TEST RS03				TEST SIGNAL APPLIED TO: —		TEST PERFORMED BY - Date C.C. DYER 5-28-75		TEST SPECIFICATION -461
TEST FREQ.	APPL'D SIGNAL LEVEL	THRESH-OLD	SPEC. LIMIT	CIRCUIT OR OUTPUT MONITORED	SENS. OF MONITOR	RESPONSE OBSERVED Ignition Time Delay sec.		REMARKS
—	—	—						NORMAL OUTPUT
220M	10 V/m					3.729	←	Removed BAND REJECT FILTER
—	—					3.744		
250M	10 V/m					3.723		
300M	10					3.729		
350M	10					3.724		
400M	10					3.723		
500M	10					3.722		
600M	10					3.723		
700M	10					3.725		
800M	10					3.718		
900M	10					3.724		
G	10V/m					3.722		
1.56	140db uV/m					3.710		
2	140db uV/m					3.716		
3	141db					—	NOISY →	NO FIRE
3	139					—	PREAMP/FWT	NO FIRE
3	125					3.723		
4	125					3.722		
4	157					3.672		
5	148					3.725		
6	152					3.724		
7	153					3.722		
8	140					3.724		
9	158					3.723		
10	151					3.723		

NOTES:

A. No change in normal output response directly due to the applied signal was observed over the frequency range indicated.

B. Deviations observed in monitored circuit response resulting from the applied signal voltage were detectable over the frequency range indicated.

E—153

ABBREVIATIONS:

MDR - Minimum Discernible Response

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NASA publications. –

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3. Ward, R. D.: Capacitance Discharge System for Ignition of Single Bridge Apollo Standard Initiators (SBASI). NASA CR-2461, November 1974.