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TECHNOLOGY UTILIZATION

ELECTRONIC CIRCUITS

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A COMPILATION

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Foreword

The National Aeronautics and Space Administration has established a Technology Utilization Program for the dissemination of information on technological developments which have potential utility outside the aerospace community. By encouraging multiple application of the results of its research and development, NASA earns for the public an increased return on the investment in aerospace research and development programs.

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When the subject matter of a particular Compilation is more narrowly defined, its title describes the subject matter more specifically. Successive Compilations in each broad category above are identified by an issue number in parentheses: e.g., the (03) in SP-5972 (03).

This Compilation contains articles on newly developed electronic circuits and systems. It is divided into two sections: Section 1 on circuits and techniques of particular interest in communications technology, and Section 2 on circuits designed for a variety of specific applications.

Additional technical information on items in this Compilation can be requested by circling the appropriate number on the Reader Service Card included in this Compilation.

The latest patent information available at the final preparation of this Compilation is presented on page 42. For those innovations on which NASA has decided not to apply for a patent, a Patent Statement is not included. Potential users of items described herein should consult the cognizant organization for updated patent information.

We appreciate comment by readers and welcome hearing about the relevance and utility of the information in this Compilation.

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Contents

Section 1. Communications Circuits and Techniques

AUTOMATIC PULSE-CODE-MODULATION [PCM], DATA-POLARITY INVERSION

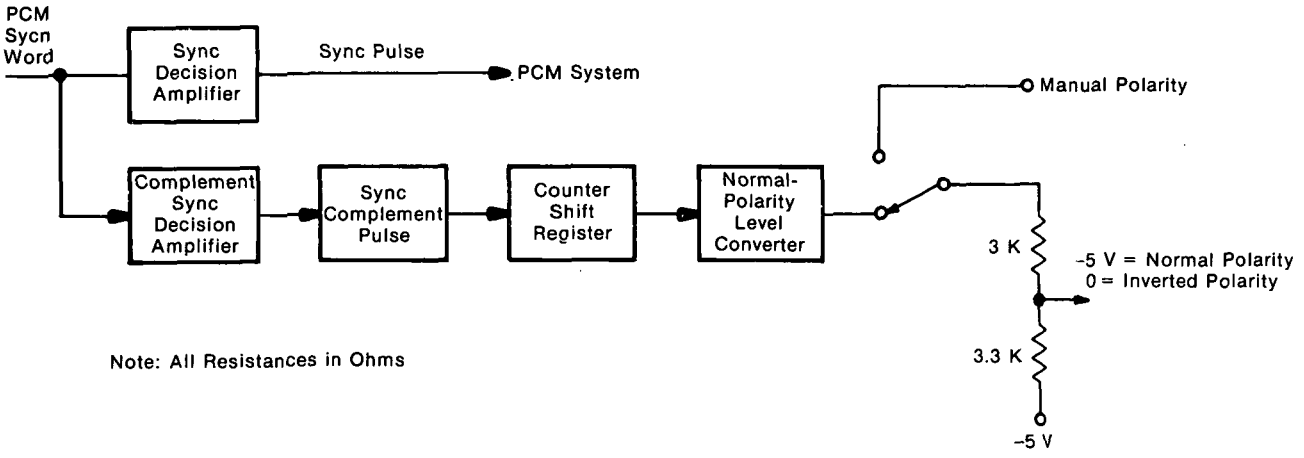
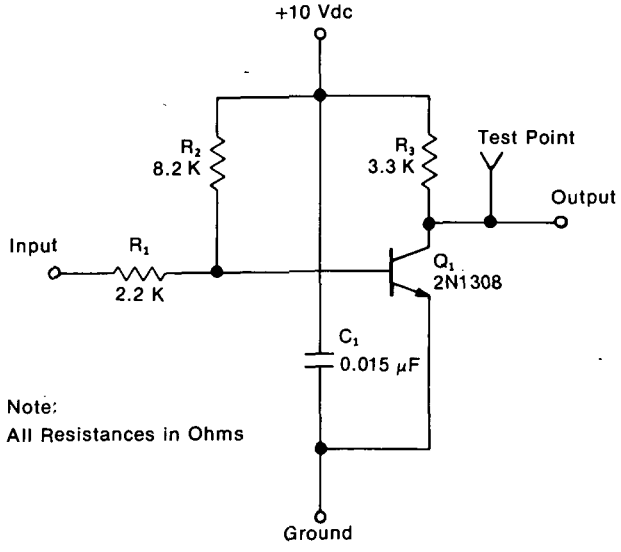


Figure 1. PCM Polarity-Inversion System

One kind of noise that can occur in a PCM recovery system is the inversion of polarity (i.e., "0" and "1" bits are switched). When this occurs, the recovery system will become improperly synchronized and data will be lost. The resynchronization of conventional PCM systems requires several steps by the operator: When the sync is lost, the polarity is switched manually; if this resynchronizes the system, the job is restarted and the polarity is switched manually at the time of the data-polarity inversion.

An improved signal-conditioning circuit causes the recovery-system polarity to change automatically in response to data-polarity inversion, thus preventing loss of data. The system is shown in Figure 1. The PCM data are conditioned by a signal conditioner and then are decoded. If the polarity of the data inverts, the complement sync decision amplifier recognizes the sync word and issues a pulse. This pulse sets a flip-flop, which changes the output level of the normal-polarity-level converter (Figure 2). This level shift causes the signal conditioner to invert the data automatically. The sync decision amplifier recognizes the PCM sync word and issues a pulse indicating good data.



INPUT	OUTPUT	LOAD
0 Vdc	0 Vdc	
-10 Vdc	+10 Vdc	No Load
-10 Vdc	+ 5 Vdc	Load

Figure 2. Normal-Polarity-Level Converter

Source: W. J. Goulding of
Rockwell International Corp.
under contract to
Johnson Space Center
(MSC-17866)

No further documentation is available.

FOUR-PHASE DIFFERENTIAL PHASE SHIFT RESOLVER

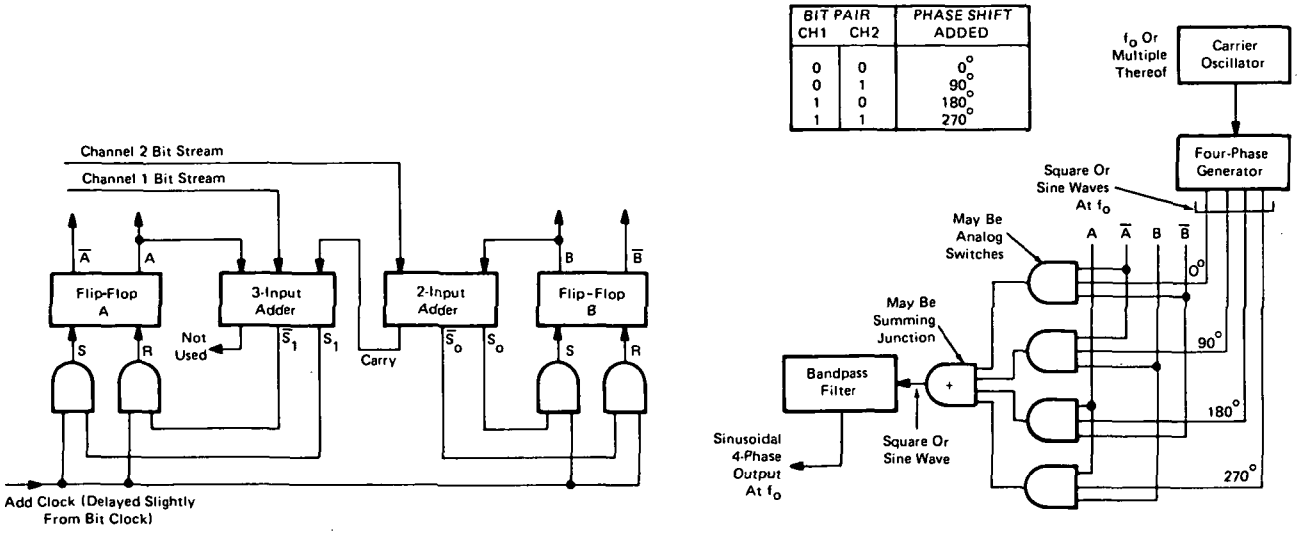


Figure 1. Adding Encoder/Modulator

Four-phase differential phase shift (DPSK) systems require a phase reference to resolve phase uncertainty during demodulation. Of the systems currently used, locally generated phase references introduce a phase uncertainty; references derived from a single received bit are noisy; and transmitted phase references use up a portion of the bandwidth and signal power, resulting in a reduction in the signal-to-noise ratio.

Two similar systems have been developed, both of which resolve phase uncertainty without transmitting reference signals or compromising the signal in any way. In both methods the signal is impressed on the carrier as a differential, rather than an absolute, phase shift. A transmitter-encoder uses a two-bit accumulating adder to put a phase-shift code on a selected phase of the subcarrier. At the receiver, a four-phase demodulation and logic process unambiguously resolves the differential phase shift of the input carrier. Two receiving methods have been developed. In one method, a two-bit subtractor extracts the reference code and, in the second method, a decoder with a more general algorithm is used for the decoding.

In both systems, the signal is encoded upon transmission as shown in Figure 1. At the input to the encoder, the two synchronized bit streams are applied to the input of a two-bit adder. Also input to the adder are two bits representing the accumulated sum of all past inputs. The four outputs A, $\overline{A}$, B, and $\overline{B}$ are combined logically in the quadriphase modulator with the four outputs from the four-phase generator. It is the phase shift and not the absolute phase that is the important parameter. The four-phase output from the modulator passes through a bandpass filter to remove unwanted harmonics and can be transmitted directly over a telephone line or as a carrier (or subcarrier) in an RF transmission link.

At the reception point, the signal is demodulated as shown in Figure 2. The frequency of the incoming signal is doubled twice (multiplied by four), by squaring and filtering, to give a signal at four times the carrier frequency ($4f_0$). Since sine waves at the same frequency separated by 360° are indistinguishable, the fourth-harmonic signal, divided by four, is phase-invariant and may be used as a phase demodulator reference. At this point there is an unavoidable uncertainty in phase. However, the reference phase can be made to match the carrier phase within 90°. A 45° phase shift places the demodulator reference-phase equidistant between two of the received phases.

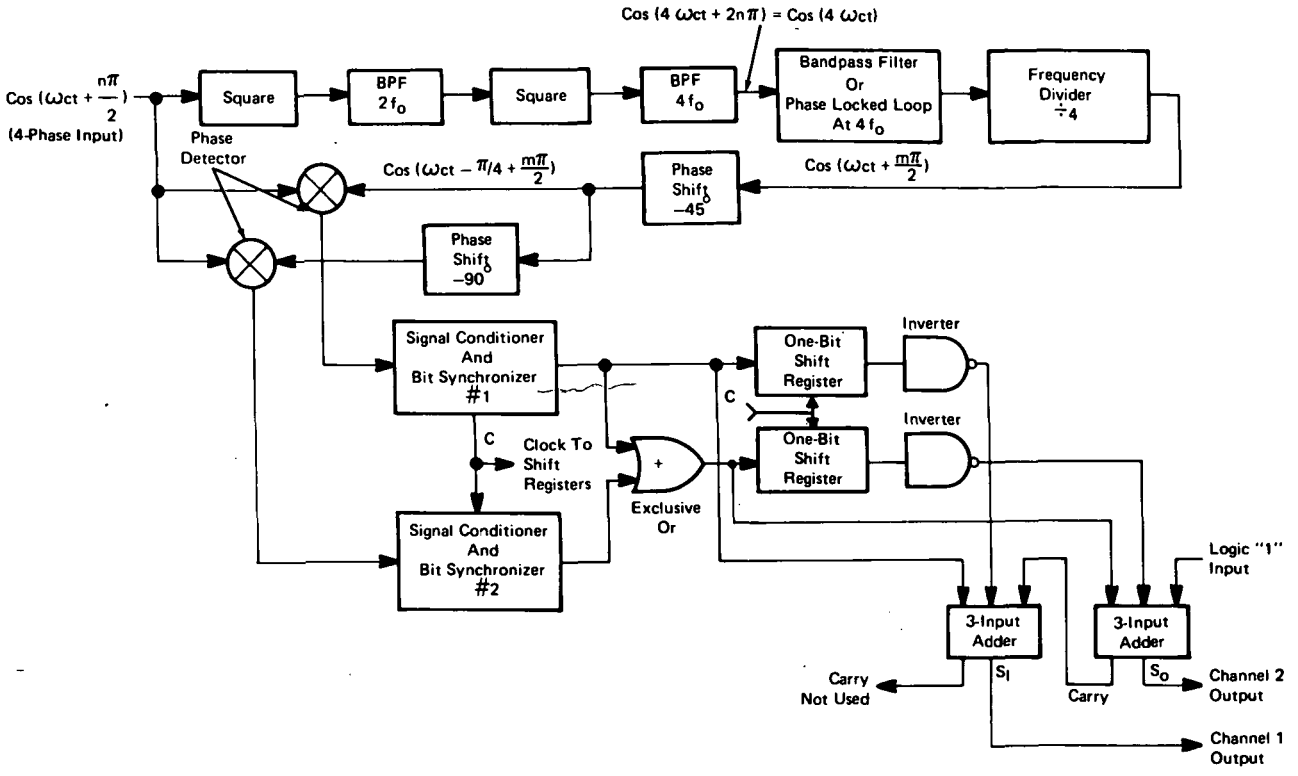


Figure 2. Demodulator/Subtracting Decoder

It is not necessary to determine the absolute phase of the reference signal; an unambiguous signal may be constructed by detecting the differential phase shift of the carrier between successive bit periods. One method of doing this is shown in Figure 2. A two bit accumulating subtractor is used to decode the signal. Signal conditioners and bit synchronizers are used to remove noise and produce two synchronized binary bit streams that are input to the subtracting decoder. In the decoder, the "exclusive-or" gate performs a count correction to produce an output identical to the output of the accumulating adder in the encoder.

The input data can be retrieved by taking successive differences between the bit pair output from the count corrector and the previous bit pair stored in the shift register. Subtraction is accomplished with a binary two-bit adder.

Another decoding technique (not shown) uses a phase resolver with a more general algorithm in place of the two-bit subtractor. As before, the two one-bit shift registers serve as a one-bit-period memory. The outputs of the bit synchronizers are compared with the outputs of the shift registers. A transition logic detects differences between the input phase status signals and the stored phase status signals and inputs a signal representing this change to the resolver logic.

The resolver logic forms phase shift indicator signals which are decoded into output data bits. The output data bits are assigned in accordance with the encoding performed at the transmitter.

Both of these systems transmit and receive data without ambiguity and allow unique identification of two data channels without transmitting identification sequences.

Source: P. M. Hopkins and
W. M. Wallingford of
Lockheed Electronics Co.
under contract to
Johnson Space Center
(MSC-14065)

Circle 1 on Reader Service Card.

DIGITAL PHASE-LOCKED LOOP

Analog phase-locked loops usually include analog filtering elements, voltage-controlled oscillators, and integrators. These components are subject to drift and nonlinearity, and lack precise repeatability from system to system. The digital phase-locked loop shown in Figure 1 overcomes these problems.

An exclusive OR gate receives an input signal and the loop output signal. The duty cycle of the error signal V_e (see Figure 2) is representative of the phase difference between the input (V_{in}) and output (V_{out}) signals. Selection of one of two clocks (V_1 or V_2) depends upon the state of V_e. When V_e is "0", the output of AND gate 1 is V_1 and the output of AND gate 2 is "0". When V_e is "1", the output of AND gate 1 is "0", and the output of AND gate 2 is V_2. The resulting waveshape, V_c, is fed into an accumulator (e.g., a divide-by-K counter) which produces V_{out}.

The phase lag between V_{in} and V_{out} may be represented by a parameter a, equal to the fraction of 90° by which V_{out} deviates from a 90° phase lag of V_{in}. (Thus if a is "0", V_{out} lags V_{in} by 90°.) The output frequency as a function of a is shown in Figure 3. The loop adjusts V_{out} until the output frequency equals the input frequency and thus locks the loop at a phase lag of

$$a \cdot 90° = \frac{f_2 + f_1 - 2K\, f_{in}}{f_2 - f_1}\, 90°$$

Where f_{in} is the input frequency, and f_1 and f_2 are clock frequencies as shown in Figure 1.

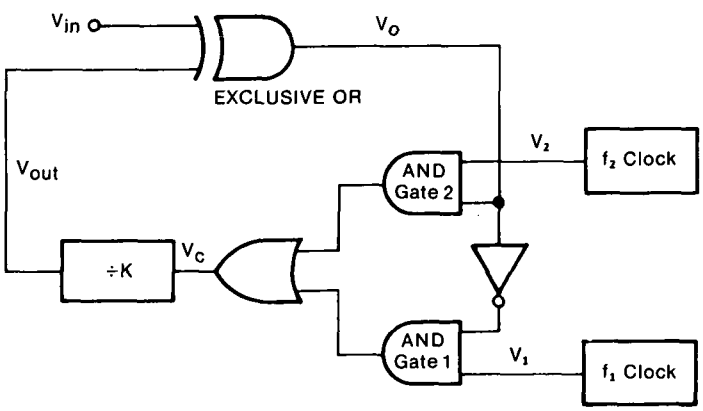


Figure 1. Phase-Locked Loop

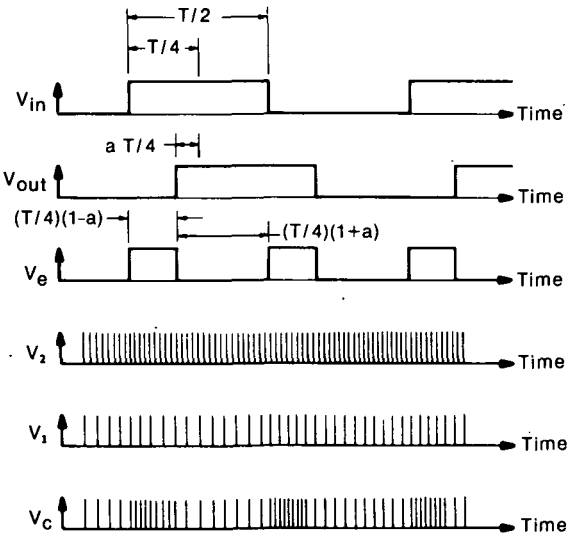


Figure 2. Signal For Phase-Locked Loop

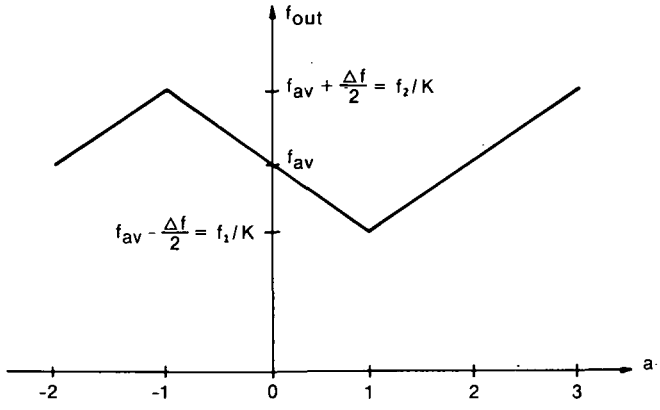


Figure 3. Plot of f_{out} Vs. a

Source: Rodger A. Cliff
Goddard Space Flight Center
(GSC-11623)

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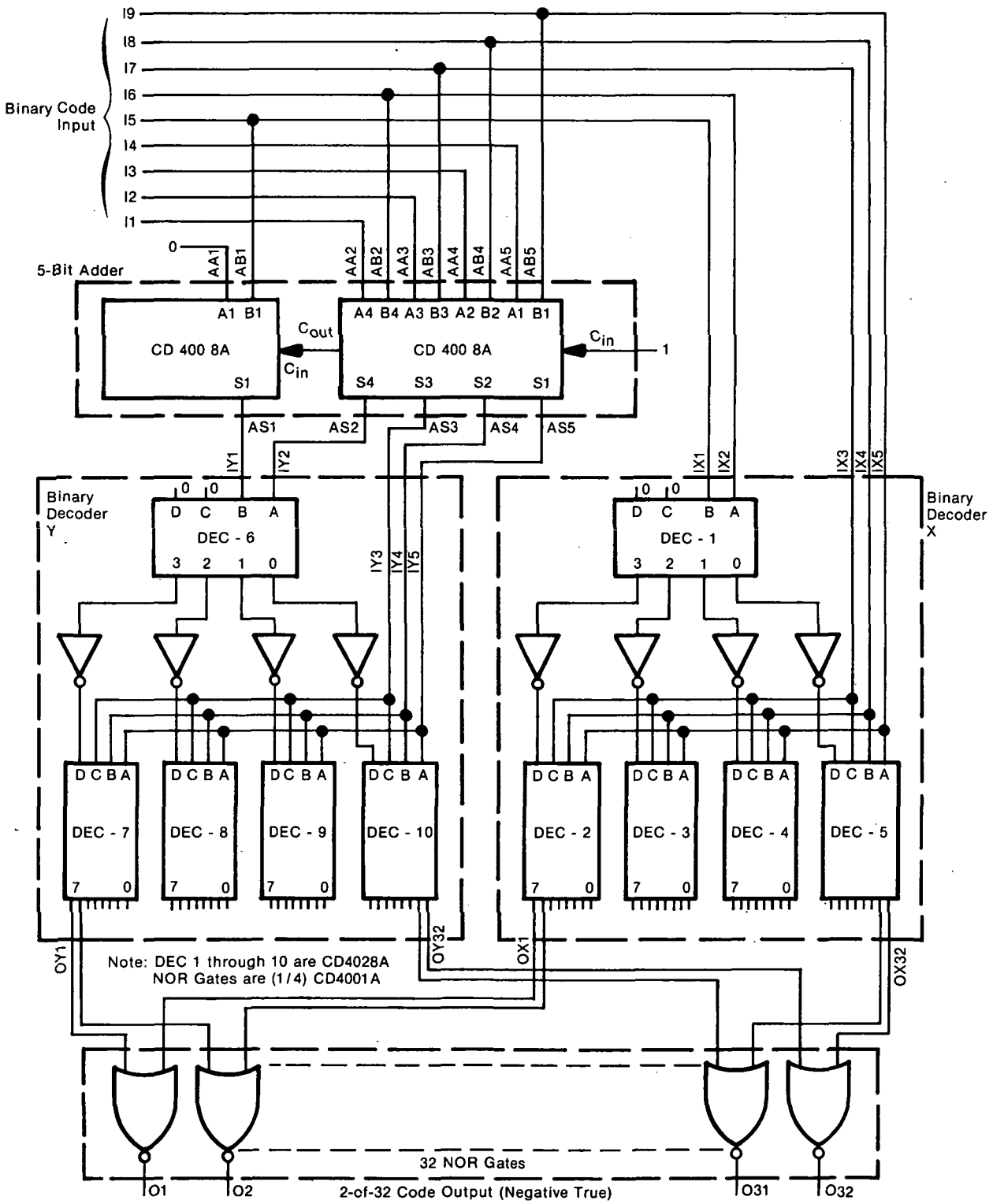
BINARY CODE TO RATIO CODE CONVERSION CIRCUIT



Conversion Circuit:9-Bit Binary Code to 2-of-32 Ratio Code

Certain digital data are most efficiently transmitted as a binary code but are most efficiently decoded as a ratio code (m of n lines true). Therefore an interactive digital circuit has been designed to convert binary-encoded data into ratio-encoded data without altering the data content. The circuit as designed to convert a 9-bit binary code to a 2-of-32 ratio code is shown in the figure.

The circuit employs complementary MOS integrated circuits and may be considered to contain four functional blocks composed of IC logic elements as follows:

1. One 5-bit adder;
2. Two 5-bit binary decoders: X and Y; and
3. NOR gate array.

The input code is a 9-bit binary number on lines I1 through I9 (with the most significant bit on line I9). Lines I5 through I9 are presented as IX1 through IX5 to binary decoder X. This decoder places a logic 1 signal on one of the 32 output lines (OX1 through OX32) and a logic 0 on the other 31 lines. A different output line is high for each of the 32 possible combinations of logic levels on the five input lines (IX1 through IX5).

Lines I5 through I9 are also presented as AB1 through AB5 to the adder. The second number presented to the adder comprises a hard-wired 0 bit as AA1, and lines I1 through I4 are presented as AA2 through AA5. The carry-bit input to the adder is a hard-wired 1. The adder carry output is ignored so that the adder output on lines AS1 through AS5 represents the modulo 32 sum of the two input numbers plus one.

Lines AS1 through AS5 are presented as IY1 through IY5 to binary decoder Y. The action of this block is similar to that of binary decoder X and results in a 1 level on one of 32 lines (OY1 through OY32). Lines OY1 through OY32 and OX1 through OX32 are combined by 32 NOR gates which output a single set of 32 lines (01 through 032) carrying the desired 2-of-32 ratio code. The output is in inverted form (two lines 0 and 30 lines 1).

Source: Victor Auerbach of
RCA Corp.
under contract to
Goddard Space Center
(GSC-11646)

No further documentation is available.

FM TRANSMITTER WITH PRECISE MODULATION INDEX CONTROL: A CONCEPT

The modulation index (peak-to-peak deviation divided by bit rate) of a PCM/FM modulator depends on both the amplitude and the frequency of the modulating wave. Thus the index is difficult to control precisely. A new PCM/FM transmitter has been proposed which can closely control a selected index and thus conserve the RF spectrum. The modulator can be used with coherent and noncoherent detectors.

The transmitter (Figure 1) includes two carrier quadrature modulators fed by sine and cosine waves. The FM signal is generated from the output of the two modulators. An FM signal s(t) may be represented as:

$$s(t) = A\cos[\omega_c t + \beta M(t)]$$

where $M(t) = \int_0^t m(\tau)d\tau$,

β = the modulation index, and

ω_c = the angular frequency of the carrier word.

Using a trigonometric identity, this expression may be rewritten as:

$$s(t) = \frac{A}{2}[\cos\omega_c t \cos\beta M(t) - \sin\omega_c t \sin\beta M(t)].$$

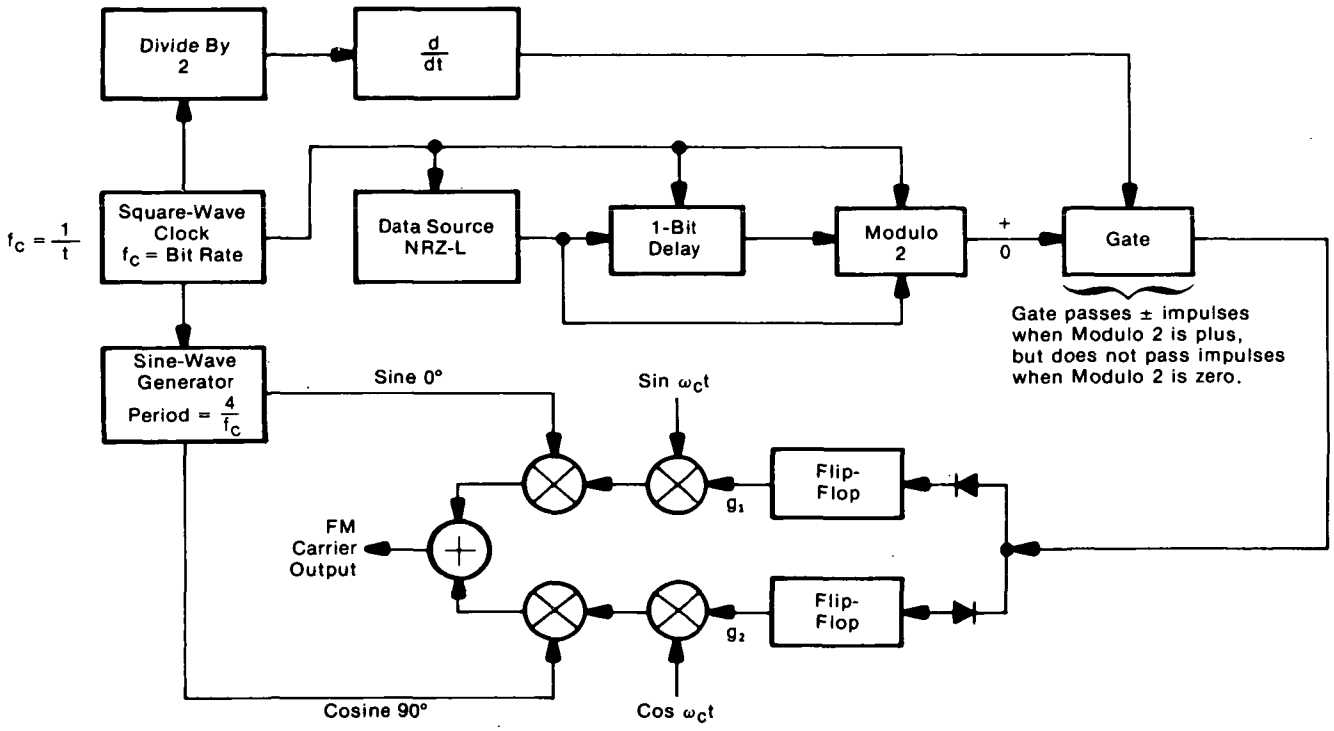


Figure 1. FM Transmitter for Precise Modulation Index = 0.5

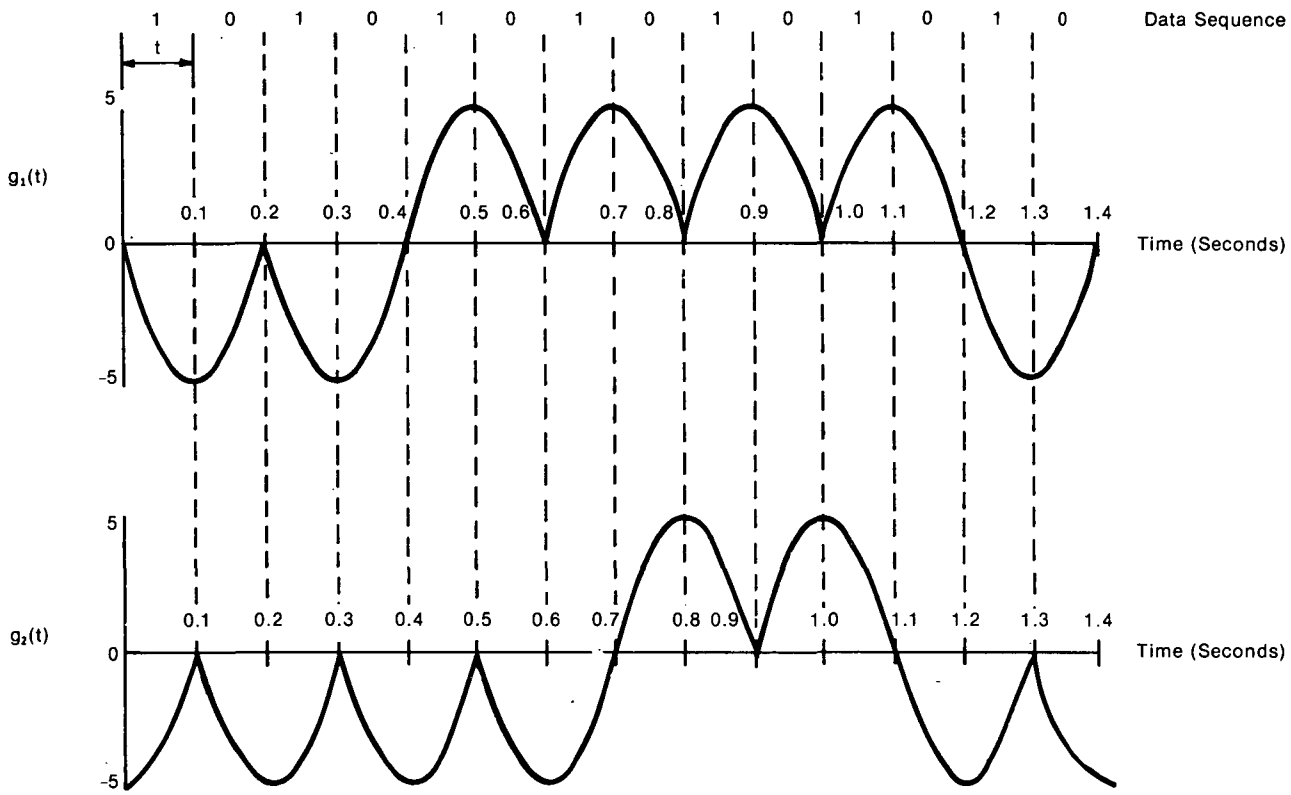


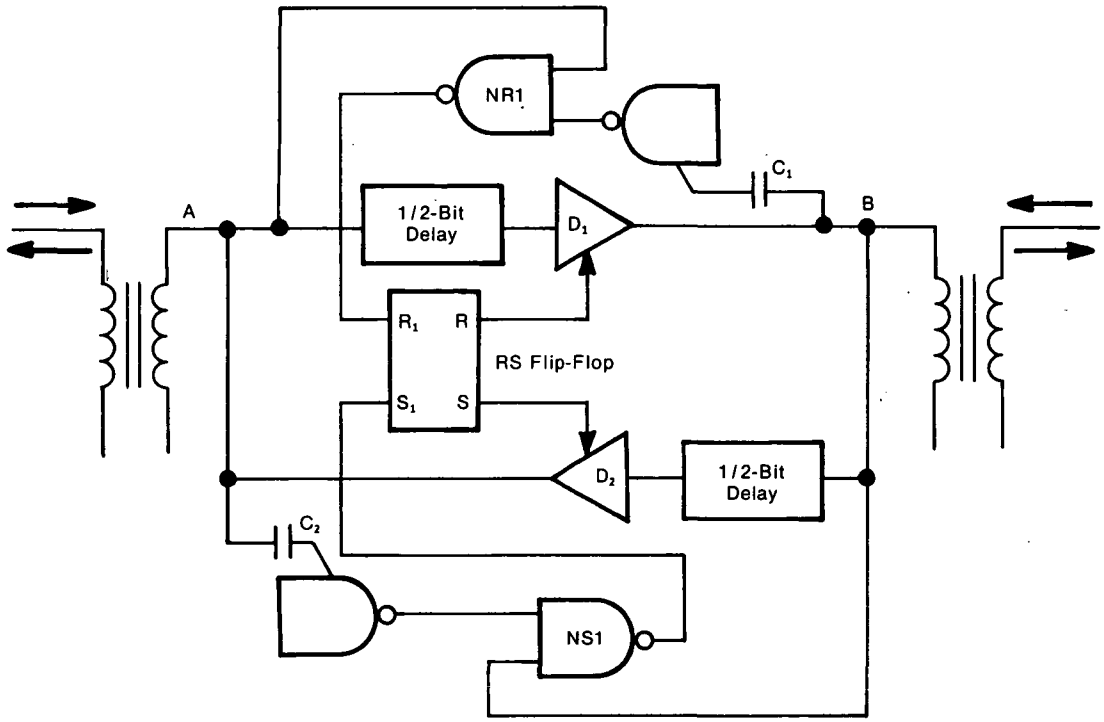
Figure 2. Waveforms for Quadrature Modulators
(Modulation Index = 0.5)

As shown by this equation, the FM signal can be formed by the superposition of independently-generated sine and cosine signals. Figure 2 shows the waveforms, $g_1(t) = -\sin \beta M(t)$ and $g_2(t) = \cos \beta M(t)$, required for an FM transmitter with a modulation index of 0.5. These waveforms are related to the bit rate as shown in Figure 2.

Source: J. Neil Birch of
The Magnavox Co.
under contract to
Goddard Space Flight Center
(GSC-11594)

No further documentation is available.

PHASE-DETECTING, SELF-DIRECTING DIGITAL COUPLERS: A CONCEPT



Phase-Detecting, Self-Directing Digital Coupler

Present data-bus coupling devices require control lines or address decoding circuits to select and control the mode of operation; either transmission or reception. A phase-detecting, self-directing digital coupler could operate autonomously as a transmitter or a receiver, as required, and therfore could be utilized in many applications as a line buffer, a line extender, or for modular add-ons.

The circuit is shown in the illustration. The direction of signal flow is determined by digital IC circuits which sense the input-to-output transit delay. Input/output amplifiers (D_1/D_2) are automatically enabled or disabled by the sensing circuit according to the signal direction.

Suppose, initially, that no signals are flowing in either direction. Under these conditions points A and B are normally high (logic 1), and the outputs of NAND gates NR1 and NS1 are thus held at 1 by the capacitor-coupled inverting networks. The negative-going edge of a signal at A or B, whichever occurs first, will then drive NS1 or NR1, respectively, with a pulse generated by the coupling capacitor. Gates NR1 and NS1 set the state of the RS flip-flop which in turn controls amplifiers D_1 and D_2. A phase difference between input and output signals, sufficient to insure detection, is generated by the 1/2-bit data delay units. This pulse delay technique utilizes the delay between input and output signals to sense signal direction. Thus if a signal arrives at A, the RS flip-flop is set to enable amplifier D_1 and to disable amplifier D_2. Exactly the reverse action occurs if a signal arrives first at B.

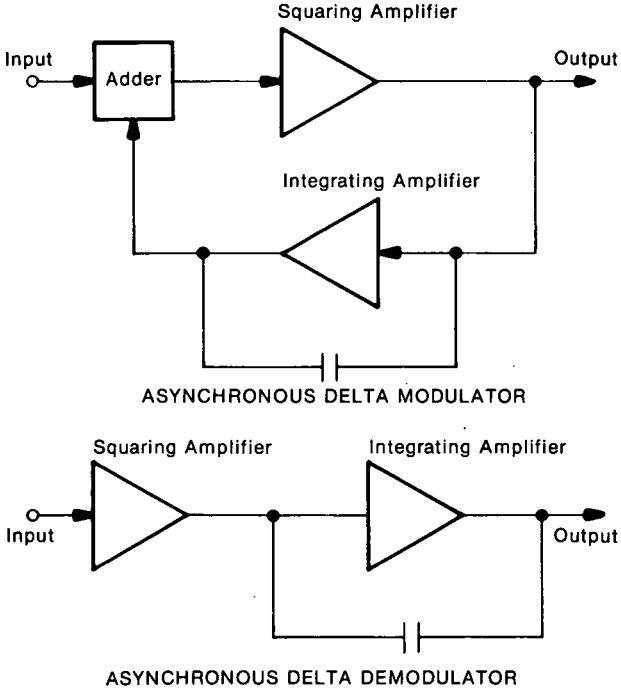
The concept has excellent modularity and flexibility. The various sections can be removed and replaced without affecting the operations of the other sections. Enable/disable control lines are eliminated, and the total length of data transmission is limited only by the delay of the coupler and the transmission line.

Source: G. R. Enoki and
L. E. Alderman of
Rockwell International Corp.
under contract to
Marshall Space Flight Center
(MFS-24426)

Circle 3 on Reader Service Card.

ASYNCHRONOUS DELTA MODULATOR REPLACES CLOCKED SYSTEMS

An asynchronous delta modulator has been designed for use in communications systems. The modulator system converts analog audio signals into trains of digital pulses. It operates in an asynchronous mode requiring no clock pulses and thus, at the same bit rate as a clocked or synchronous delta modulator, provides a higher degree of intelligibility.



Functional Block Diagram of Asynchronous Delta Modulator and Demodulator

The circuit (see figure) consists of an add network, a squaring amplifier, and an integrator. With no input signal, the circuit operates as a bistable oscillator with a characteristic free-running frequency. This frequency appears as a square wave at the output. With an input signal applied, the squaring amplifier tends to remain at one stable state for longer periods of time, in order to conform to the characteristics of the input signal. The output frequency is therefore lower than the free-running frequency.

The advantages of the asynchronous delta modulator over a clocked delta modulator are: (a) its ability to maintain the same levels of intelligibility for a given bit rate and (b) its lower noise level, due to the elimination of undesirable noise caused by clock transitions. It therefore should be of interest to manufacturers of digital communications equipment.

Source: J. A. Webb of
Lockheed Electronics Co.
under contract to
Johnson Space Center
(MSC-13812)

Circle 4 on Reader Service Card.

UHF PIN DIODE SWITCHES

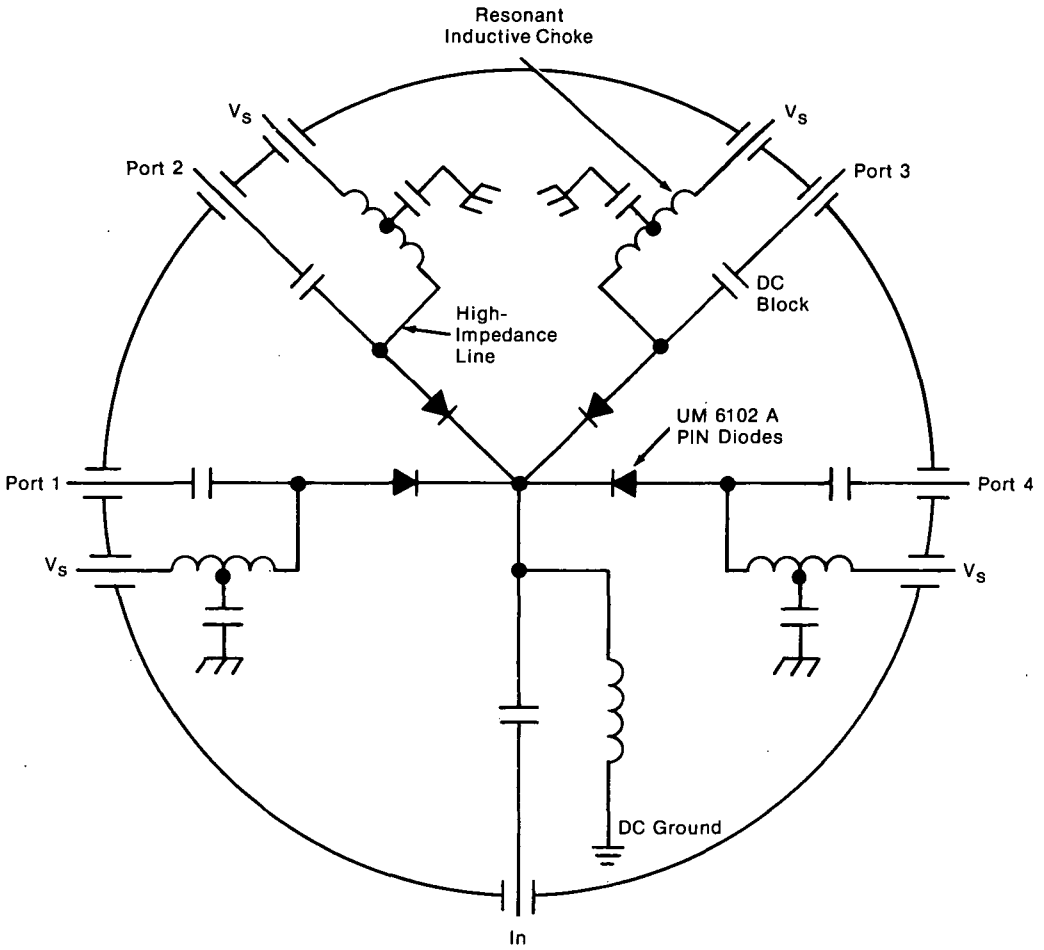


Figure 1. UHF SP4T PIN Diode Switch

Single-pole-double-throw (SPDT) and single-pole-4-throw (SP4T), ultrahigh-frequency (UHF), power-switching circuits have been constructed using cathode-connected rectifying diodes. The circuits include the associated inductors and capacitors, and a high-impedance conduction line. These switches are constructed using strip-line techniques and are suitable for ultralow loss, high-efficiency, high-power, broadband switching applications.

Figure 1 shows the schematic of the UHF SP4T PIN diode switch. DC bias is supplied to the series diode through an inductive choke, consisting of a high-impedance section of transmission line connected to the center conductor of the strip-line. The dc return is similarly provided by grounding the input through a high-impedance line which forms a choke to block the RF. When the diode is forward biased, RF is passed. When the diode is reverse biased, high isolation is achieved. The switch is constructed in air-dielectric strip transmission line. A special beryllium oxide shunt mounting technique is employed to heat sink the PIN diode to the case for good thermal dissipation.

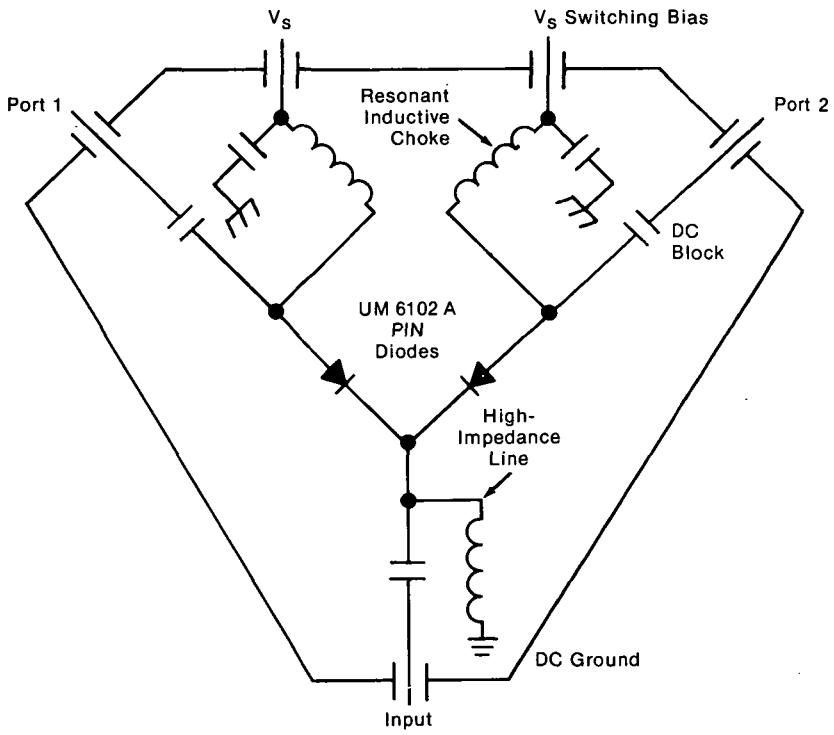


Figure 2. UHF SPDT PIN Diode Switch

The schematic of the UHF SPDT PIN diode switch is shown in Figure 2. The design for this switch is very similar to that of the SP4T switch described earlier.

Test reports show the insertion loss to be less than 0.3 dB for the SP4T switch and less than 0.2 dB for the SPDT switch. Isolation is greater than 20 dB for both switches. Although the design application called for operation over narrow bands centered at 401.9 and 463.825 MHz, tests showed that both switches could operate from 370 to 500 MHz. Junction temperature measurements proved that the glass axial-lead PIN diodes could handle the required 40 watts. The switches have been operated at power as high as 60 watts without failure. Each switch requires only 125 mW of dc power to operate.

These devices have proved superior to ferrite devices or conventional diode switches in insertion loss, isolation, and efficiency. In addition, they are smaller in size, weigh less, and are insensitive to temperature and magnetic effects.

Source: M. A. Ikemoto and
R. C. Chapman of
Philco-Ford Corp.
under contract to
Goddard Space Flight Center
(GSC-11678)

No further documentation is available.

FLEXIBLE PLAYBACK SPEED CONTROL FOR TAPE RECORDED DATA

Tape recorded data can normally be played back only at speeds differing from the recording speed by factors of 2 (e.g., 1/2, 1/4, 1/8 ... of the recorded speed). If some other playback speed is required, an external generator is usually used to control the recorder oscillator during playback. The use of such external equipment, as opposed to direct multiplication of internal frequencies, introduces errors due to the variances between the recorder oscillator and the external oscillator.

A new technique allows the playback speed to be any desired fraction of the recording speed. During recording, a track is designated as a pseudo control track. It can be any unassigned track or the normal control track. A sine wave is recorded on the pseudo control track, as selected from the following formula:

$$F_P = F_N \cdot \frac{R}{K}$$

where F_P = the pseudo control track frequency,
F_N = the inherent frequency of the recorder control track,
R = the desired record-to-playback speed ratio, and
K = a constant selected from the table shown (at right).

As an example, assume the data are recorded at 60 ips with a control frequency of 100 kHz, and a playback speed 1/22 (3-3/4 ips) of the recording speed is desired. The pseudo control track frequency is

$$F_P = (100 \text{ kHz}) \frac{22}{16} = 137.5 \text{ kHz}.$$

Range of R	K	Desired Record Speed (IPS)	Playback Speed (IPS)
1 to 2	1	120 60 30 15 7-1/2 3-3/4 1-7/8	120 60 30 15 7-1/2 3-3/4 1-7/8
2 to 4	2	120 60 30 15 7-1/2 3-3/4	60 30 15 7-1/2 3-3/4 1-7/8
4 to 8	4	120 60 30 15 7-1/2	30 15 7-1/2 3-3/4 1-7/8
8 to 16	8	120 60 30 15	15 7-1/2 3-3/4 1-7/8
16 to 32	16	120 60 30	7-1/2 3-3/4 1-7/8
32 to 64	32	120 60	3-3/4 1-7/8
64 to 128	64	120	1-7/8

Table for Selection of Constant K

Source: R. A. Hall and R. J. Leifeld of McDonnell Douglas Corp. under contract to Marshall Space Flight Center (MFS-22972)

Circle 5 on Reader Service Card.

ERROR-DECODING ALGORITHM

A new error-decoding algorithm provides better performance than either sequential or Viterbi decoding of comparable complexity. The amount of computation required is independent of the constraint length. This allows the use of large values with resulting low-error probability at lower signal-to-noise levels.

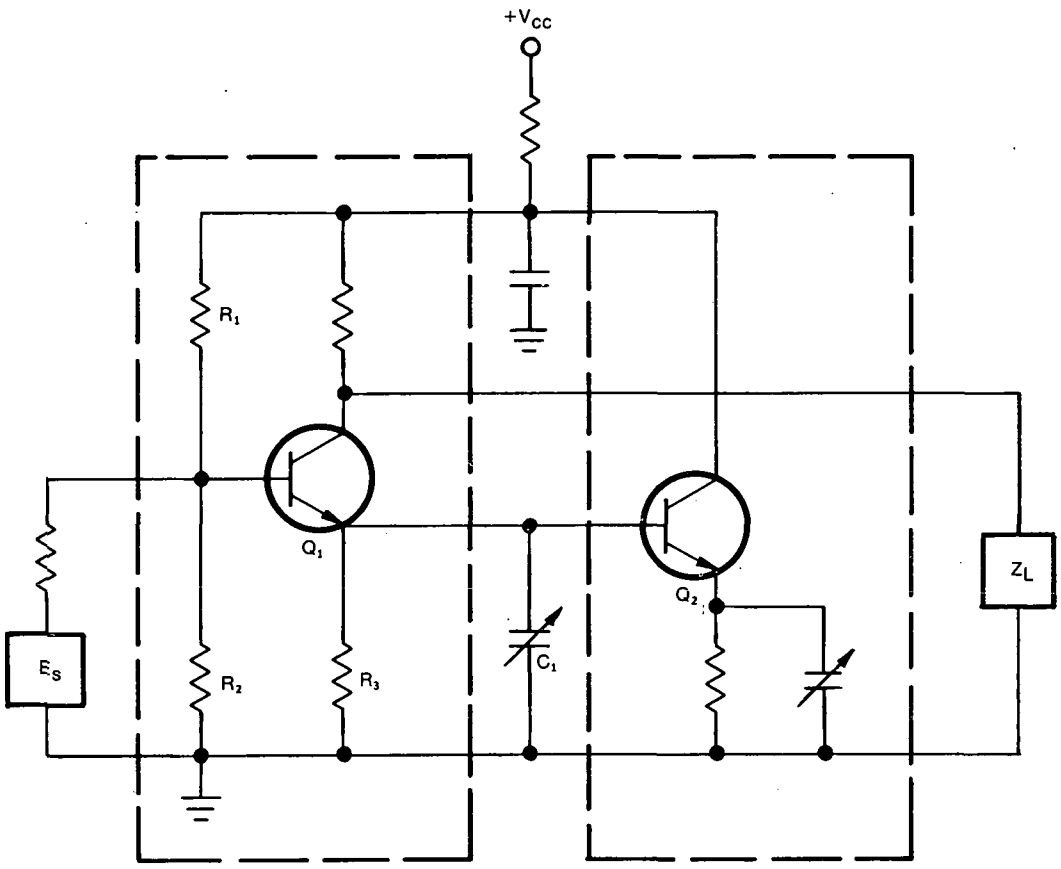
The algorithm is self-starting and recovers from a decoding failure without the transmission of a known message. Since the constraint lengths can be large enough to span short periods of time, the algorithm will not be susceptible to fading signals. It is capable of operating at data rates up to the channel capacity. A prototype decoder has been successfully operated at data rates of 11 megabits per second.

Source: R. B. Blizard of
Martin Marietta Co.
under contract to
Johnson Space Center
(MSC-13823)

Circle 6 on Reader Service Card.

Section 2. Specialized Circuits for Instrumentation

ACTIVE TUNED CIRCUIT



Active Tuned Circuit

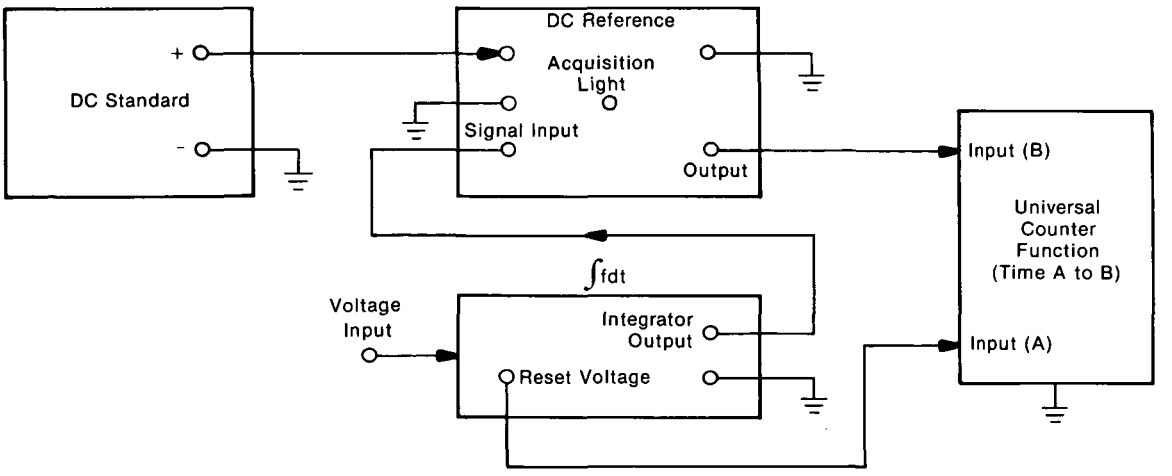
The circuit shown in the figure is a narrow-band, high-Q, selectively tunable circuit that may easily be designed as either a filter, an amplifier, or an oscillator. The low-noise temperature-stable circuit can be designed for any frequency near the transition frequency, F_t, of any selected transistor without requiring inductors. Accordingly, the design lends itself both to high-frequency and to lower frequency applications.

In the figure external signal-source E_S is applied to the resistive divider R_1 and R_2, and to the base of the first transistor Q_1. Near F_t the impedance presented at the emitter of Q_1 is the equivalent of a low-Q inductor. The emitter of Q_1 is connected to resistor R_3, capacitor C_1, and the base of transistor Q_2, and its impedance is a combination of negative resistance and capacitive reactance. The combination of these two effects provides a circuit that is well suited for microelectronic fabrication. The design may be useful as a low-cost means of reducing the size and weight of filter and oscillator circuits.

Source: Leonard L. Kleinberg
Goddard Space Flight Center
(GSC-11340)

Circle 7 on Reader Service Card.

LOW-FREQUENCY PEAK DETECTOR



Application of Low-Frequency Peak Detector

A new dc measurement device consists of operational amplifiers coupled to discrete solid-state components, to generate variable-width low-frequency pulses and to measure integrator current gain and low-frequency amplitude changes. Normal instrumentation alone, such as oscilloscopes, Pen motors, and meters, do not offer the accuracy of the new device.

The equipment (shown in the figure) must be so connected that uncaging the integrator simultaneously starts the counter. When the integrator output equals the dc reference voltage applied to the low-frequency peak detector, the peak detector output switches from negative to positive saturation, stopping the counter with a positive-going pulse approximately 30 volts in amplitude. The integrator gain (G) is given by

$$G = \left(\frac{V_{REF}}{V_{IN}}\right)\left(\frac{1}{TIME}\right),$$

where time is measured in seconds. The acquisition (AQS) lamp (LT) is lighted whenever the signal input is greater than the dc reference voltage.

In general, the loop gains of control systems or electronic networks having dc amplifiers and dc integrators can be measured with great accuracy in a matter of minutes. The typical accuracy obtainable is approximately 0.2 percent. The circuit shown in the figure also can be used to measure control-system integrator dc gains and the amplitude of low-frequency positive or negative pulses, with pulse-widths greater than approximately 10 ms and positive or negative dc peak amplitude.

Source: L. Wright, Jr., D. E. Pack, and D. H. Vickery, Jr., of Lockheed Electronics Corp. under contract to Johnson Space Center (MSC-13750)

Circle 8 on Reader Service Card.

INPUT CIRCUIT FOR THERMAL-CONDUCTIVITY GAS-CHROMATOGRAPH DETECTOR

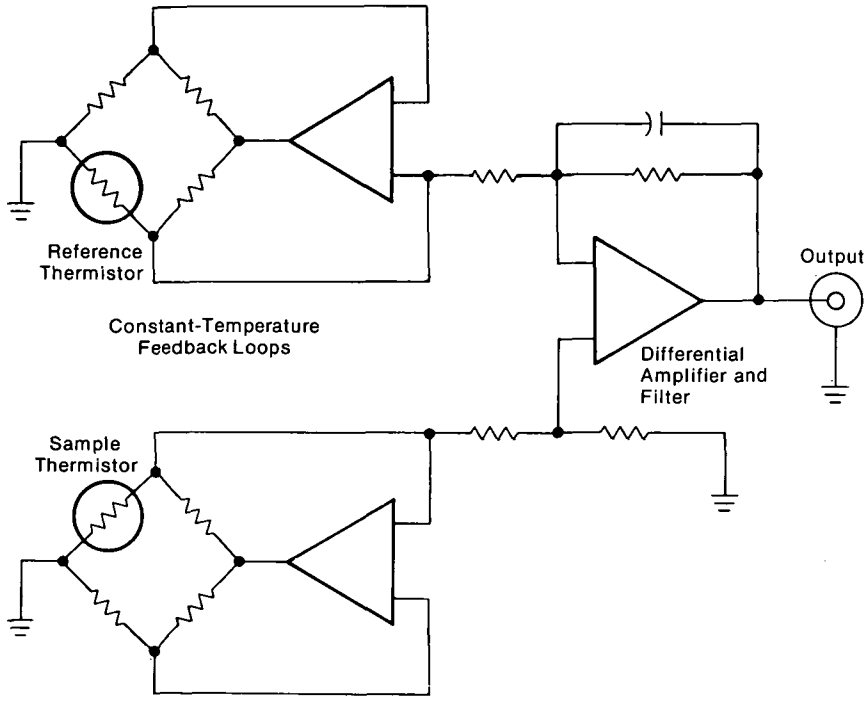


Figure 1. Input Circuit for Thermal-Conductivity Gas-Chromatograph Detector

The input circuit of a sensitive gas-chromatographic detector has a considerable influence on the overall performance of the instrument, including reliability, response, signal/noise ratio, dynamic range, linearity, the effects of power supply drift, and electronics temperature drift. A new input circuit has been designed, using a variation on the conventional wheatstone bridge circuit. It has greater linearity than conventional input circuits, does not need critical adjustments, and resists power supply drift. This circuit can be miniaturized and is adaptable to fully-automated remote operation.

Instead of placing the sample and reference thermistors each into one of the two lower arms of the same Wheatstone bridge, as is normally done, two independent resistor bridges are used (Figure 1): one containing the reference thermistor, the other the sample thermistor. The output of each bridge is connected to a separate operational amplifier (op-amp) in a feedback configuration which balances temperature induced changes in the thermistor resistance by varying tne current flow through the bridge and thus the voltage drop across the thermistor. In this way the thermistor resistance, the ratio of the voltage drop to the current flow, may be kept constant. In this case the circuit is designed to lock the resistance of the sample and reference thermistors at a constant value of 800 ohms, corresponding to a thermistor temperature of 30° C (86° F).

The resultant output signals from the sample and reference bridges are connected to a differential op-amp and filter circuit with high common-mode rejection. As the reference thermistor is maintained in steady-state gas flow conditions, only the differential signal resulting from the action of the sample thermistor is amplified.

The operating point of the circuit is highly stable because the circuit loadline intersects the thermistor V-I characteristic at almost a right angle (Figure 2). Although the response is less than could be obtained with a loadline intersecting at a more acute angle, the choice taken here is completely free from latchup

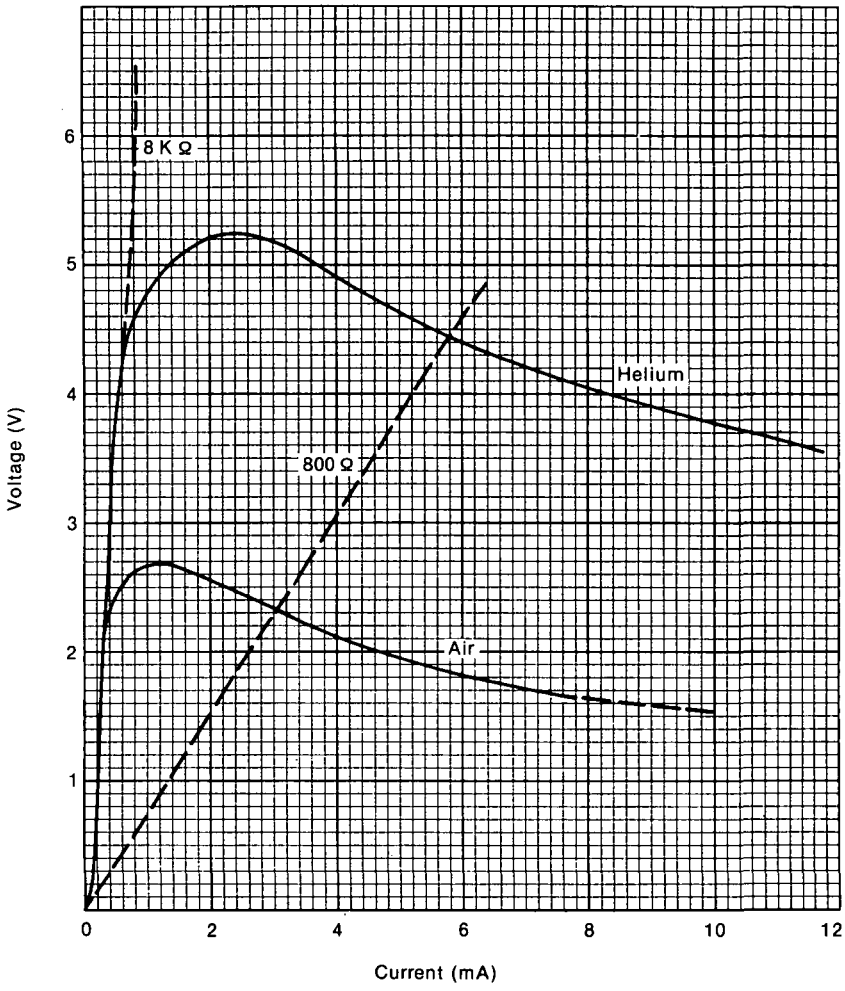


Figure 2. Static V-I Characteristic of 0.013-in. Diameter Thermistor Bead Suspended in a Flowthrough Gas Cavity. (The 800-Ohm Loadline Shown Dashed)

states. The output does not reflect supply voltage variations (a problem in conventional circuits), because of the common-mode rejection of the operational amplifiers in the constant-temperature feedback loops. Thus there is no special requirement for supply regulation.

Analysis is significantly simplified. The detector/electronics are described by the equation

$$V^2/R = K(T_T - T_D) + P_L$$

where V is the thermistor voltage, R is its resistance, K is a constant proportional to the thermal conductivity of the carrier-plus-unknown, T_T and T_D are thermistor and detector temperatures, and P_L is stray power loss through the thermistor supports. In operation, using a helium carrier, R, T_T, and T_D are constants and P_L is negligible. K and V make small excursions around the operating point, which accounts for the linearity of the detector response. Finally, operation of the thermistors at a fixed temperature permits close specification of thermistor matching at that temperature.

Source: Daniel Webster McMorris
of TRW, Inc.
under contract to
Langley Research Center
(LAR-11452)

No further documentation is available.

INVERTED, VOLTAGE-CONTROLLED OSCILLATOR

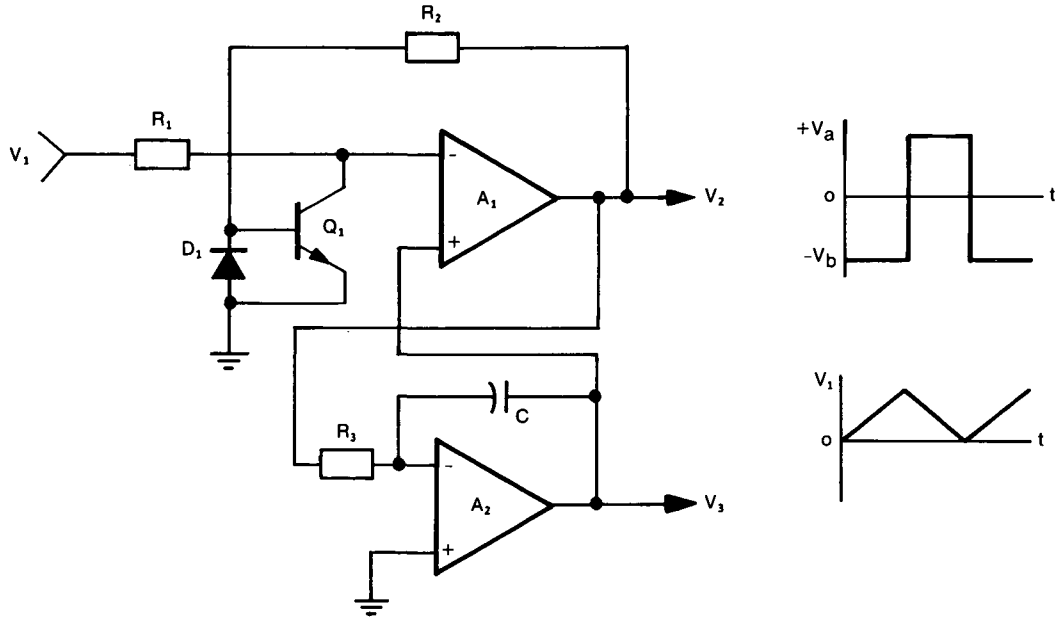


Figure 1. Inverted, Voltage-Controlled Oscillator

The inverted, voltage-controlled oscillator circuit shown in Figure 1 contains two operational amplifiers (A_1 and A_2), a switching transistor (Q_1). a capacitor (C), a reverse protection diode (D_1), and three resistors (R_1, R_2, and R_3). The control voltage V_1 can be varied over some range, typically 0.1 to 10 volts. This voltage is fed through resistor R_1 to the inverting input of amplifier A_1. Transistor Q_1 in the off state allows voltage V_1 to appear at the negative input of A_1 and in the on state Q_1 shorts the inverting input of A_1 to common.

The transistor, Q_1, is controlled by the output of amplifier A_1. When the voltage at the inverting input of A_1 is positive, V_2 is negative; when it is negative, V_2 is positive. This causes the output of amplifier A_1 to latch in either the positive or the negative state. The output V_2 changes state only when the difference voltage between the inputs changes sign. This sign change is caused by the second amplifier A_2. Amplifier A_2 is used as an integrator, with the integration rate controlled by the level of V_2. The output, V_3, of this integrator is fed to the positive input of A_1. The circuit will now oscillate with the waveforms shown.

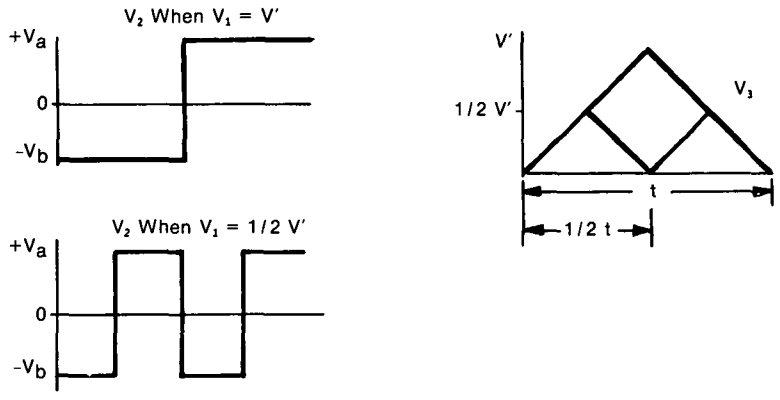


Figure 2. Output Waveforms

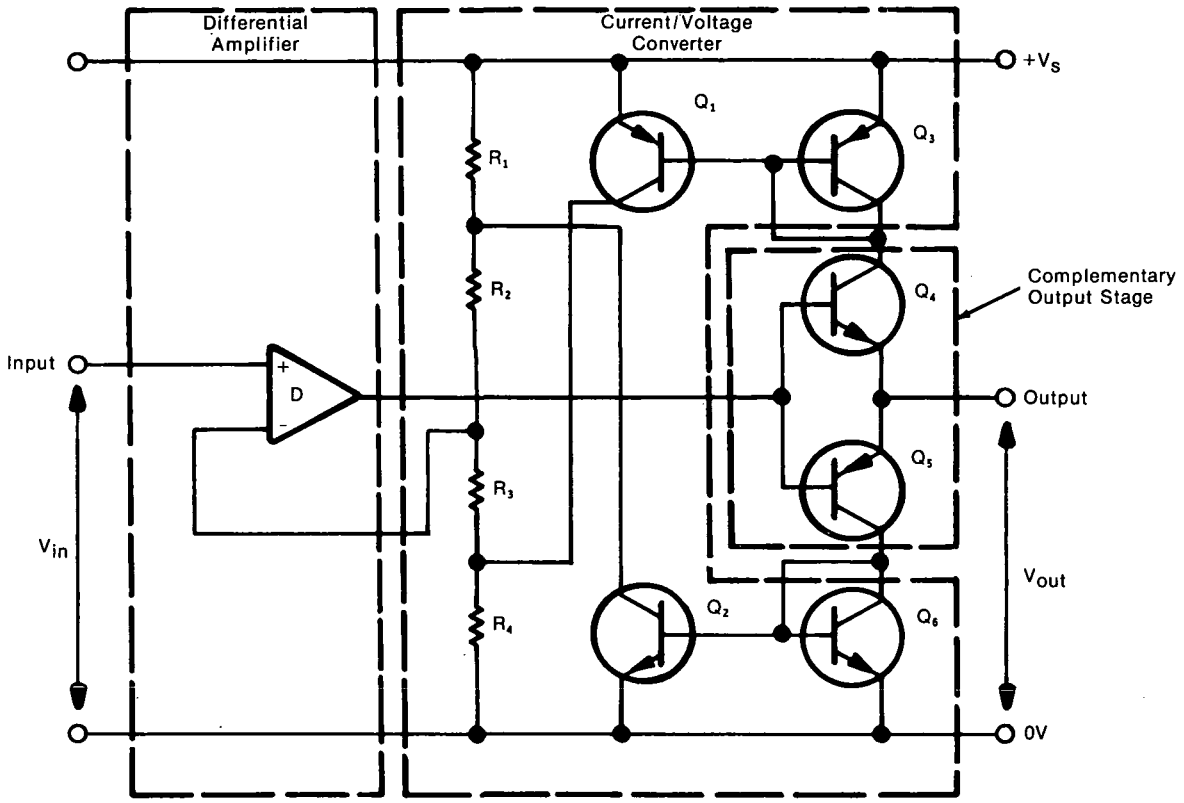
The relationship between the input voltage and the output frequency may be seen in Figure 2. The graph V_3 shows the output of the integrator as a function of time. Note that the large triangular wave and the small triangular wave have the same slopes. With this in mind, assume that V_1 is equal to V' volts. The integrator will integrate between 0 and $+V'$ volts and will cycle over a period T. Now if V_1 is reduced to $V'/2$, the period T is reduced by one-half. Thus the period of oscillation is directly proportional to the input voltage V_1; and since the reciprocal of the frequency is equal to the period, V_1 must be inversely proportional to the frequency. Graph V_2 shows the same relationship for voltage V_2.

The circuit is an efficient means of converting an analog signal to an inverse digital signal. It is constructed from a small number of components and would therefore be economical to produce. It should be of interest to those concerned with information transfer systems.

Source: James R. Currie
Marshall Space Flight Center
(MFS-22924)

Circle 9 on Reader Service Card.

INTEGRABLE POWER GYRATOR



Simplified Circuit Diagram Of The Noninverting VCCS

Gyrators have been in existence for some time now. Synthesis of gyrators by different methods such as a voltage-controlled current-source (VCCS) approach, decomposition of the Z-matrix, approaches using operational amplifiers, etc., has produced gyrators having very low efficiency on the order of 1 percent. The result has been that these gyrators cannot handle signals above several milliwatts without excessive dissipation of dc power.

A further study of the Y-matrix (VCCS) approach and the Z-matrix configuration has led to development of efficient, dependable high-quality gyrators. The basic configuration used for the Y-matrix gyrator comprises two essentially similar VCCS's in a loop with one producing a 180° phase reversal and the other producing zero phase change. This circuit is reciprocal, and the input signal may drive either the amplifier with phase reversal or the one without.

The basic circuit of the noninverting VCCS is shown in the figure. It consists of the differential amplifier, the complementary output stage, and the current/voltage converter connected in a feedback loop. The current/voltage converter performs the same function as the ordinary gyration resistor in conventional gyrators: it produces a voltage that is proportional to the output current. This voltage is fed back to the differential amplifier. This type of feedback is called current proportional voltage feedback which stabilizes the VCCS transconductance and, at the same time, enhances the output resistance of the output stage and the input resistance of the differential amplifier. The configuration provides stable transconductance and high input and output resistances which are all necessary for a high quality Y-matrix gyrator.

In general, high efficiency of the circuit is provided by the following:

1. Class B output stage
2. Small current flow through gyration resistors R_1 and R_4 as compared with the output current
3. Current flow through the differential amplifier and of the transistors Q_1 and Q_2 is small compared to the output current.

Performance of this current with a 10-V supply voltage may be summarized as follows:

1. Voltage amplification factor = 600
2. Transconductance = 1.8 millisiemens
3. Output resistance = 300 kilohms
4. Input resistance $\gg$ output resistance
5. Efficiency = 38 percent.

The inverting VCCS is essentially similar to the noninverting one. However, to invert the phase, the inputs of the differential amplifier have to be interchanged. Since the feedback has to stay negative, further phase reversal in the feedback path is necessary. This is accomplished by insertion of another differential amplifier connected as an inverter (amplification factor = -1). Because the efficiency of the inverting VCCS is also 38 percent, efficiency of the complete circuit is 19 percent - a significant improvement over the previous 1 percent.

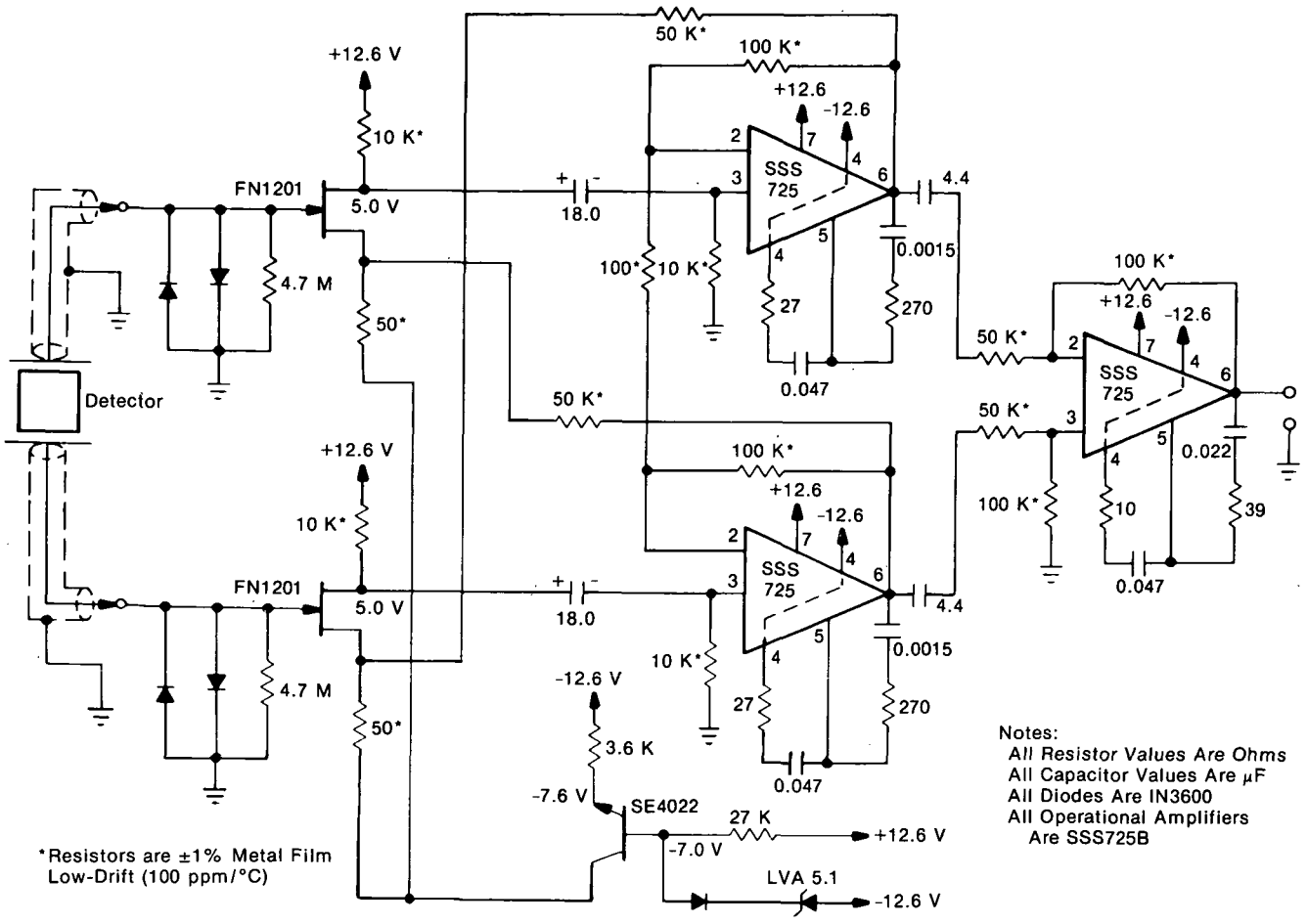
The Z-matrix gyrator incorporates the same basic building blocks of the Y-matrix type but combines them in a different way. As in the case of the Y-gyrator, the output of each differential amplifier is connected to a complementary output stage which in turn is connected to a current/voltage converter. The current/voltage converter produces a voltage that is proportional to the current flowing into the corresponding port (input or output) of the gyrator (see figure). This voltage, however, is not fed back to the differential amplifier, but drives either directly or by insertion of an inverter (voltage gain = -1) to the noninverting input of the other differential amplifier. In order to ensure a low output resistance and a high input resistance, the output voltage at each port of the gyrator is fed back to the inverting input of the corresponding differential amplifier.

Results from either approach have been favorable. With further improvements in design details, efficiency of the new gyrators may now approach the theoretical limit of 78.5 percent. This will allow handling of signals of considerable power with moderate dc power dissipation. Improvements in quality factor Q have reached 300 for Y-matrix and 1300 for Z-matrix gyrators. Finally, both designs are comparatively easy to integrate by implementing the same technology as used with conventional operational amplifiers.

Source: E. Hochmair of
National Academy of Sciences
under contract to
Marshall Space Flight Center
(MFS-22342)

Circle 10 on Reader Service Card.

LOW-NOISE INSTRUMENTATION AMPLIFIER FOR LOW-FREQUENCY APPLICATIONS



Low-Noise Instrumentation Amplifier

The instrumentation amplifier shown in the figure can recover low-frequency, low-amplitude geophysical signals. The characteristics of the amplifier include low 1/f noise, high common-mode rejection, high input impedance, and high gain stability for changes in temperature and supply voltage.

A matched pair of field-effect transistors, selected for low 1/f noise, and a current source comprise the differential-input section of the amplifier. The second stage of the amplifier is a differential-input, differential-output stage made with commercial amplifiers. The cross-coupled feedback from the second stage to the input section establishes the gain of the first two stages. The final stage of the amplifier is a signal subtractor.

The amplifier has a midband gain of 1815. Gain is down 3 dB at 1.5 and 500 Hz. The common-mode rejection is greater than 90 dB from 4 to 500 Hz without resistor trimming. Equivalent input noise voltage is 14 $nV/\sqrt{f}$ from 20 to 500 Hz, with 1/f noise evident below 20 Hz. Equivalent input noise voltage increases to 35 $nV/\sqrt{f}$ at 5.78 Hz, the signal frequency for which the amplifier was designed.

Source: Dale M. Sipma and Charles S. Martin of
Hughes Aircraft Co.
under contract to
Langley Research Center
(LAR-11407)

No further documentation is available.

RAPID BATTERY ACTIVATION AND CELL-BY-CELL VOLTAGE MEASUREMENT

A device has been developed to simultaneously activate batteries and evaluate their performance. Previous methods required a separate activation procedure, either cell by cell, using a syringe, or on an activation rack. Such methods required more time and could not provide a cell-by-cell electrical check during activation.

The new device combines these two operations. It is clamped on top of the battery, forming a vacuum-tight seal between itself and the battery cells. A probe-plate makes contact with each cell terminal. A previously measured quantity of electrolyte then is poured into the compartments located immediately above each cell. The top of the device is placed into position and is sealed with rapid-connect/disconnect clamps. A vacuum is applied to force electrolyte into each cell. At the same time the vacuum is applied, voltage measurements are made on each cell to note any irregularities.

Source: W. J. Britz and W. A. Boshers
Marshall Space Flight Center
(MFS-22749)

Circle 11 on Reader Service Card.

SCATTEROMETER PREPROCESSOR SYSTEM

The well-known techniques used in microwave-processor spectrum unfolding and spectral analysis (doppler filtering) can now be applied to resolve problems in microwave scatterometry. A microwave signal preprocessor is now developed to preprocess the data from several scatterometers. Its advantages are that it reduces the computer preprocessing time, permits a quick-look display, and verifies the data; it also eliminates analog-to-digital conversion.

Functionally the preprocessor can be considered as a two-part system: (1) a signal manipulation section, comprising a single sideband modulator mixer and a low-pass filter network, and (2) a processor-and-display section, consisting of a digitizer and a multiplexer. Sideband modulation unfolds the spectrum of the outputs of several scatterometers, which is then analyzed by mixing and low-pass filtering with a set of generated frequencies. This spectral analysis is then normalized, multiplexed and digitized for recording, and finally projected as a real-time display. As a substantial improvement in the state of the art, this technique can be useful to engineers and technicians concerned with the design and maintenance of airborne ground-mapping and doppler radars.

Source: R. E. Chapman, K. L. Dienes, D. G. Killion,
H. C. Loewer, and W. F. Smith of
Teledyne Ryan Aeronautical
under contract to
Johnson Space Center
(MSC-13734)

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SOLID-STATE POWER SWITCH

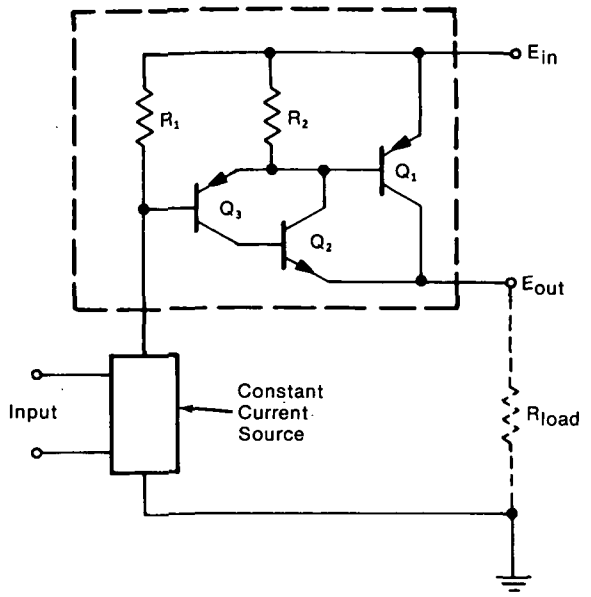


Figure 1. Darlington, PNP-NPN Compound Amplifier

A new solid-state power switching circuit provides an efficient means of switching power to high-current loads. The switch provides a low-impedance path between the power source and the load.

The dc power switch shown in Figure 1 is a Darlington, pnp-npn compound amplifier consisting of three transistors. Resistors R_1 and R_2 provide bias. The switch is a combination of two common transistor circuits. Q_1 and Q_2 form a direct-coupled pnp-npn compound amplifier with feedback, with Q_1 and Q_3 in a Darlington amplifier configuration. The inherent advantages of each circuit result in a very efficient power switch that could be used in solid-state remote power controllers, circuit breakers, relays, and related devices.

The design takes advantage of the low collector-to-emitter voltage (V_{ce}) of a simple saturated transistor at low and rated load currents and the Darlington efficiency at higher load currents. When the load currents are at rated values or below, the primary power transistor Q_1 operates in the saturated state (Figure 2) with a low V_{ce}, (typically 200 mV or less). The base-to-emitter junction of transistor Q_2 is in reverse bias, blocking Q_3 collector current. Thus transistor Q_1 obtains the necessary base current through the emitter-base junction of Q_3.

Using typical circuit voltage values

$$V_{ce_1} = 200 \text{ mV},$$
$$V_{be_1} = 700 \text{ mV, and}$$
$$V_{ce_3} < 100 \text{ mV},$$

the base-to-emitter voltage of Q_2 is -600 mV. The base-to-emitter junction of transistor Q_2 is therefore reverse biased. Area 1 of Figure 3 shows the low V_{ce_1} values exhibited when the compound power switch is operating in the saturated state.

When V_{ce_1} increases enough to forward-bias the base-to-emitter junction of Q_2, collector current is conducted through Q_2 and Q_3. V_{ce_1} must be greater than 800 mV before the base-to-emitter junction of Q_2 will be forward biased. To be fully conducting, however, V_{be_2} must be on the order of 700 mV.

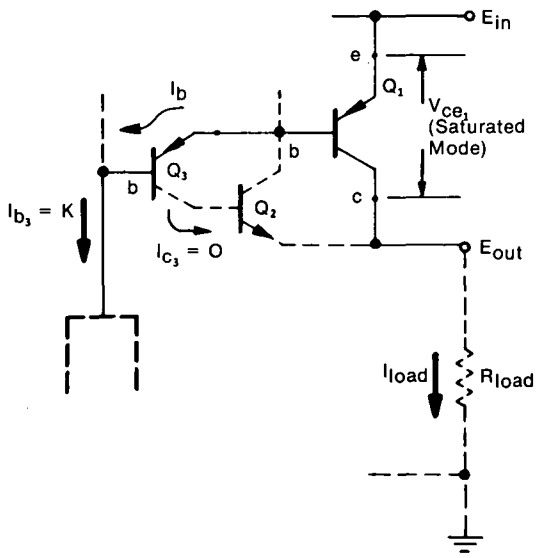


Figure 2. Compound Amplifier in Saturated Mode

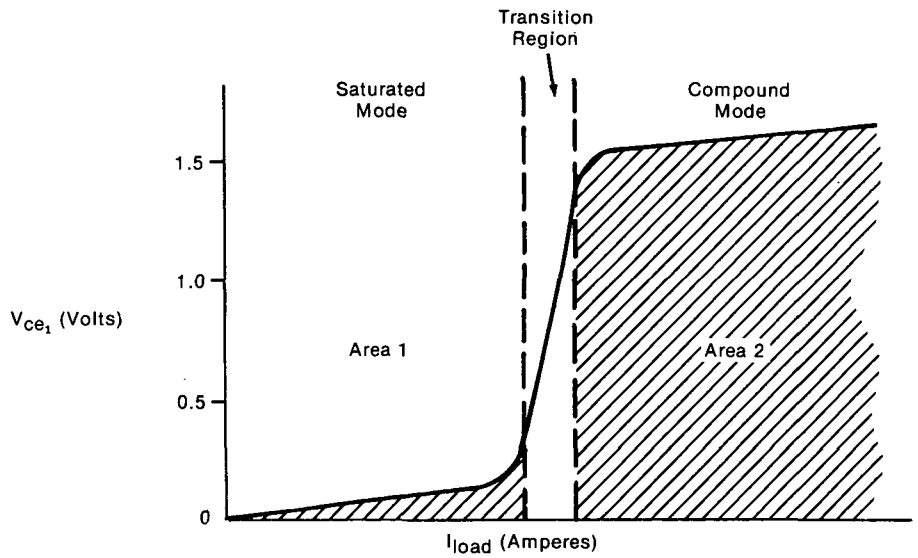


Figure 3. V_{ce_1} Versus I_{load} Characteristics

Therefore, the voltage between the collector and the emitter of transistor Q_1 must be approximately 1.5 Vdc to benefit fully from the efficiency of the compound switch. The resultant increase in the base current of Q_1 further inhibits the rapid increase of V_{ce_1}. This is a result of diverting the base current of Q_1 through Q_2 to the load.

The effect is to maintain Q_1 at a relatively low V_{ce_1} for high or overload currents. Furthermore, the Q_2 and Q_3 collector currents flow through the power output terminal (E_{out}) to the load to increase the efficiency of the power switch. Unlike conventional switches, this mode of operation reduces power losses caused by a major increase in the base current of Q_1, due to the additional conduction through the collector-to-emitter junction of Q_2. This increased current flows through the load resistor and does not reduce the efficiency of the compound switch. The V_{ce_1} characteristics of the compound amplifier in full conduction are shown in area 2 of Figure 3.

The significant advantages of the compound power switch over conventional switches are higher efficiency, higher input impedance, and higher overall switch gain. These advantages result in further desirable qualities, such as a reduction of thermal stresses within the components, a smaller physical package, a reduced loading of base drive circuits, and easier feedback control.

Source: D. E. Williams
Marshall Space Flight Center and
L. C. Maus of
Sperry Rand Corp.
under contract to
Marshall Space Flight Center
(MFS-22880)

Circle 13 on Reader Service Card.

IMPULSE COMMUTATING CIRCUIT WITH TRANSFORMER TO LIMIT REAPPLIED VOLTAGE

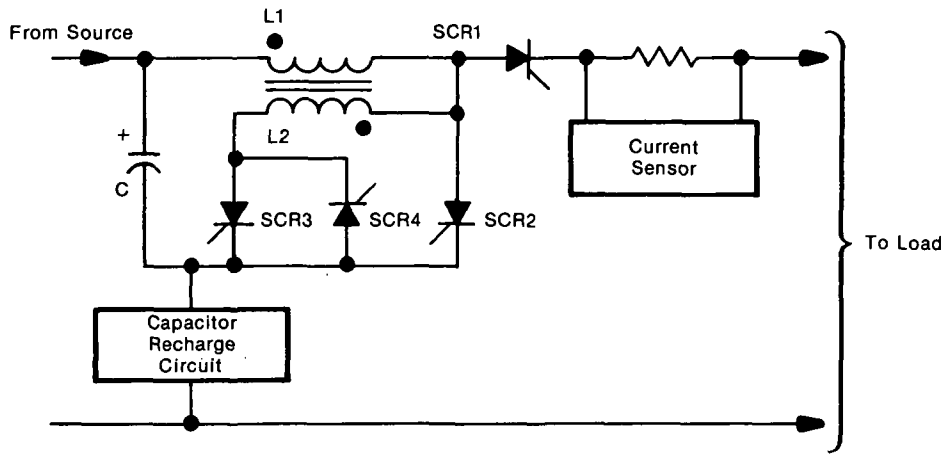


Figure 1. Basic Commutating Circuit

A new circuit to achieve commutation of a switching silicon controlled rectifier (SCR) has been developed to open a circuit with currents flowing up to values of 30 amperes. This circuit utilizes a new concept of switching, which halves both current and voltage in the middle of the commutating cycle thereby lowering the size and weight requirements.

The commutating circuit has performed successfully throughout the temperature range of 218 to 373 K (-67 to 212° F). It can be turned on or off by command and will remain on in the absence of a load due to the continuous gate.

A schematic diagram of the commutating circuit is shown in Figure 1; its operation is illustrated in Figure 2. In operation, SCR 1 carries the load current. Capacitor C is precharged to 450 volts in the polarity shown. A manual shut down or trip level overcurrent is sensed at the time t_0. SCR 2 is triggered on at this time dumping the capacitor across L1 and driving the anode of SCR 1 negative so that it stops conducting almost instantly. The current flowing through L1 continues to flow but now goes through SCR 2. When the voltage on SCR 1 comes up to zero at time t_1, the voltage has been negative on SCR 1 long enough to keep SCR 1 from conducting with no gate even though the voltage on the anode is now reapplied in the positive direction.

At time t_2, the voltage on the capacitor is zero and the current through the inductor is at maximum. SCR 3 is now gated on. Until this time, L2 has been in an open circuit with no current flow. Now that current can flow through L2, the magnetic field in the inductor is the same but the number of windings has doubled so that the current, almost instantly, goes to half the peak value. The oscillation of the circuit continues at half the frequency. The current flows through L1 and L2 in series, which have capacitor voltage across them, so that SCR 2 now has half the capacitor voltage across it, in reverse. Thus, it is turned off. The same voltage is applied to SCR 1; i.e., half of the voltage that would be applied if SCR 3 did not conduct. This permits lower ratings for SCR 1.

As the oscillation continues, the current goes through zero and SCR 4 is gated on to permit the current to flow in the opposite direction. This is at time t_3. The capacitor is now charged to a voltage representing the energy of its initial charge plus the energy stored in the inductor L1 at time t_0, exclusive of losses. At time t_4, the voltage across SCR 1 is back down below source voltage, the capacitor voltage is going through zero, and SCR 4 is carrying maximum current. By time t_5, the capacitor is nearly recharged (except for losses), SCR 3 is turned off, current ceases

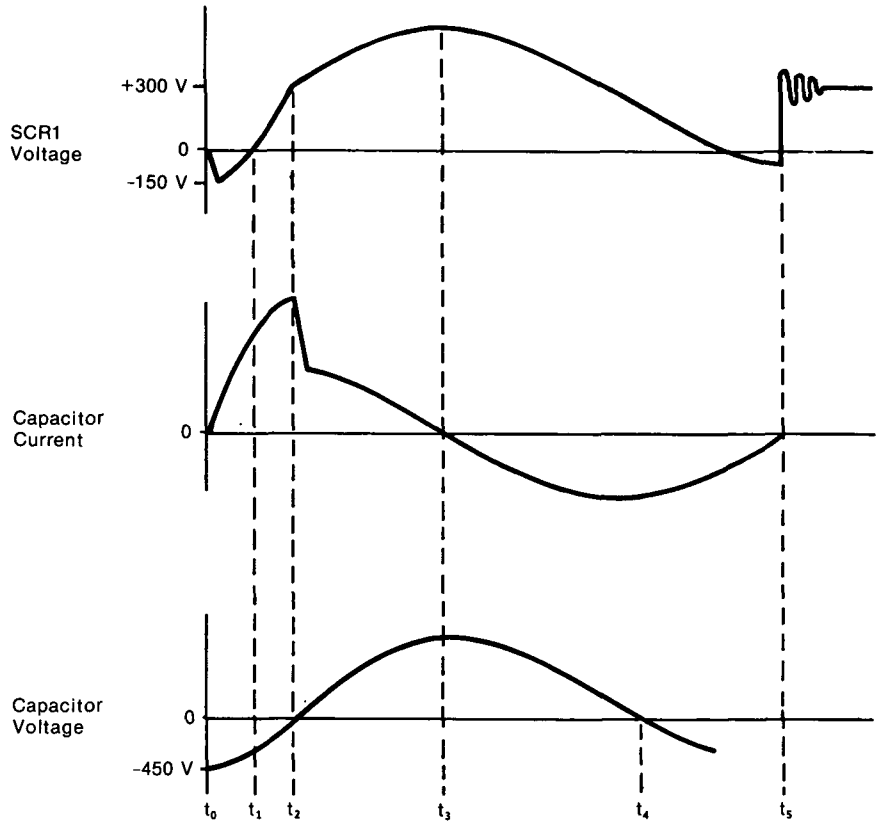


Figure 2. Principal Waveforms of Commutating Circuit

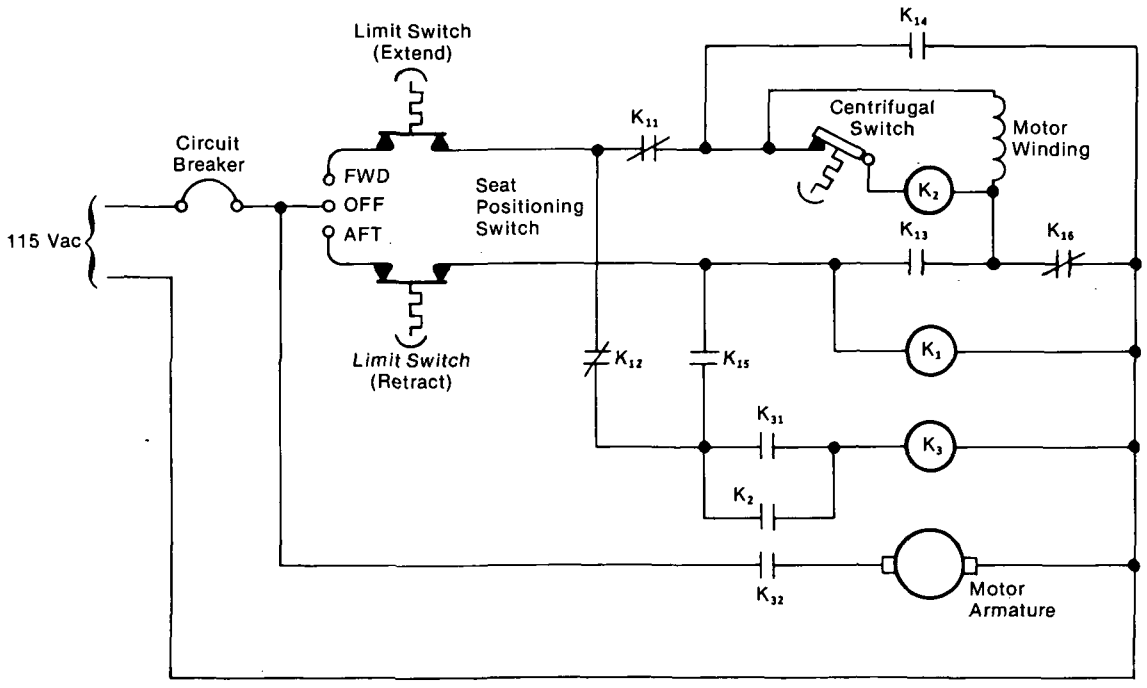
to flow and the voltage on SCR 1 goes back to source voltage. The circuit is now reset and is nearly ready to be turned on again. In reality, the charge on the capacitor will be built up to its final precharge value by the capacitor recharge power supply before it is desirable to turn the circuit on again. The whole commutation cycle takes place in less than 1/2-millisecond and occurs with no reference to the return circuit of the power source so that minimum transient disturbances are caused.

The commutation circuit is ideal for use in direct current switching where SCR's are used as the principle switching element, because the network interrupts the supply and load current immediately upon initiating the commutation cycle. The circuit does not induce transient current in the supply or load and limits the transient voltages. This solid state innovation should have potential use in spacecraft and aircraft electrical systems, in transportation systems, and in hazardous areas such as mining. The commutation scheme can also be extended to chopper circuits where the voltage is controlled by switching and filtering.

Source: J. H. McConville
Martin Marietta Corp.
under contract to
Lewis Research Center
(LEW-11849)

No further documentation is available.

OVERLOAD CONTROL CIRCUIT FOR REVERSING SPLIT-PHASE MOTORS



Overload Control Circuit

A non-flight-rated seat-positioning system incorporated into a flight simulator utilizes two split-phase motors on each seat: one for tilt and one for forward-and-aft travel. If the motors are direct wired to the seat position switch, current surges and circuit-breaker activation may result if the direction of seat travel is rapidly reversed.

A novel circuit provides an inexpensive solution to this problem. When the seat positioning switch is activated, the centrifugal switch in the motor (see figure), together with relays, causes the motor to decelerate prior to reversing direction. If the seat switch is positioned FWD, relay K_2 closes, heavy-duty relay K_3 latches, and the motor drives the seat forward. The centrifugal switch then opens, and thus relay K_2 opens. The motor begins to decelerate.

Now assume that the seat switch is positioned AFT. Relay K_1 closes and relay K_3 opens. The motor continues to decelerate until the centrifugal switch closes again, at which time relay K_2 closes and relay K_3 again latches. The motor reverses direction; and the seat moves AFT until the centrifugal switch again opens, causing the motor to again decelerate and relay K_2 to open. The seat switch is then returned to the OFF position, and relays K_1 and K_2 open.

The problem could also be solved by installing servomotors rated to handle the peak loads. However, this would be significantly more expensive. This circuit could be used in other situations to permit the use of available motors not rated to handle the peak loads, which occur during field-reversed times/periods.

Source: F. R. Yerian and W. F. Iceland of
Rockwell International Corp.
under contract to
Johnson Space Center
(MSC-19405)

No further documentation is available.

PULSE-GENERATING NETWORK FOR MAGNETO PLASMA DYNAMIC THRUSTERS

Although there are existing networks that generate desired pulse shapes, the experimental network shown in Figure 1, using a closely packed spiral pattern of capacitors, is exceptionally compact and light. It stores enough energy so that the full potential of quasi-steady magneto plasma dynamic (MPD) thrusters is realized (high-power operation for a long-enough period to establish steady operating conditions). In addition, the network may have application in high-powered pulse laser systems.

A substantial reduction in the size and weight of such circuits can be obtained by eliminating the bulky and heavy induction coils ordinarily required. For a given total length of conductor, circuit inductance can be increased by arranging the leads in a spiral so that the current in each of the loops is in the same direction about the centerpoint. By stacking the capacitors as closely together as possible, the size of the conductor loops is reduced, while the number of turns used in forming the connections is increased correspondingly. The result is a net increase in inductance with a minimal increase in conductor length beyond what is required to connect the capacitors. Thus, in addition to savings in weight and bulk, there is a reduction in resistive power loss.

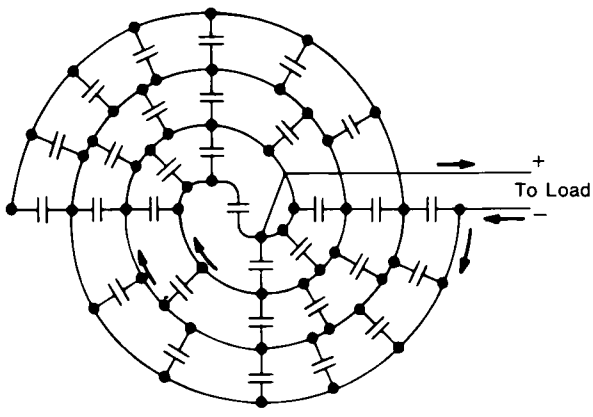


Figure 1. Experimental Pulse-Generating Network With Capacitors Connected in a Spiral Pattern That Increases Bus-Bar Inductance

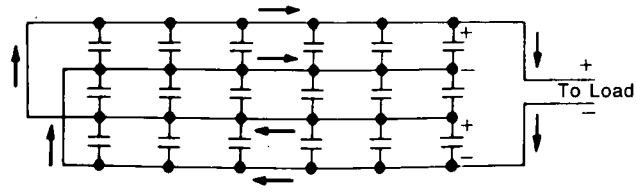


Figure 2. Arrangement of Conductors Connecting Three Rows of Capacitors in a Manner That Increases Network Inductance

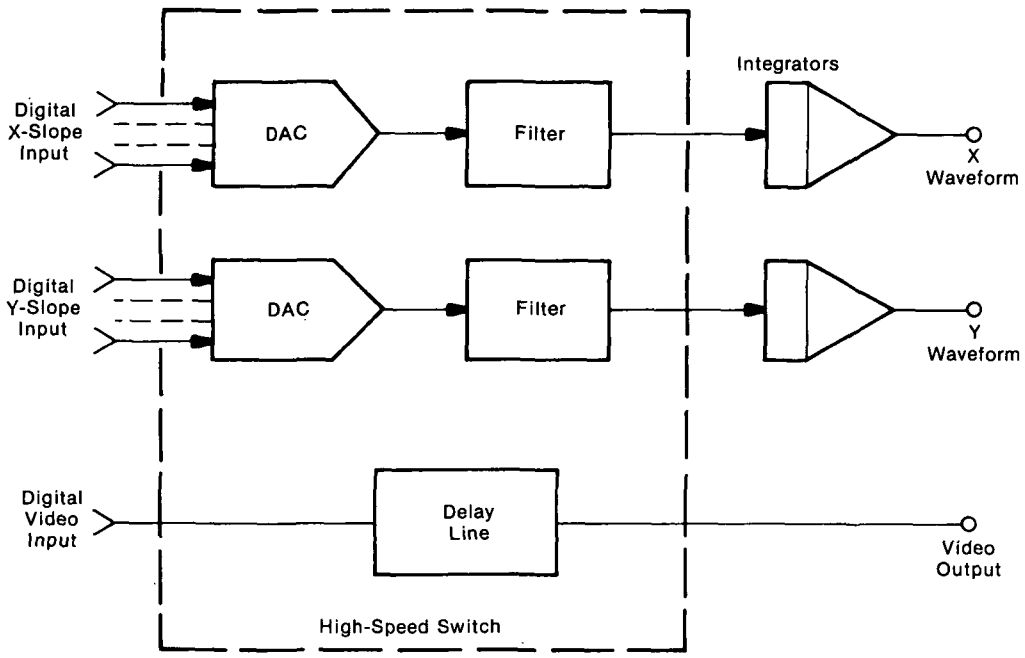
With circuits that depend on bus-bar geometry for inductance, pulse shaping is accomplished by moving the connection point of the flexible capacitor leads to different locations on the bus bar. When the connection spacing is widened, more of the bus bar is utilized for inductance in that particular mesh. The action is similar to that obtained with the rail-and-slide type of adjustment that is used with the ladder-type networks.

A pulse generator, with a nominal 5000 joule discharge, was constructed from 60 electrolytic capacitors arranged as those in Figure 2. Its dimensions were 107 cm (42 in.) long and 46 cm (18 in.) in diameter when enclosed in a protective canister. The generator weighed about 140 kg (308 lb). With an initial charge of 400 volts, the discharge current was 25 to 30 kiloamps for about a millisecond. When operating at one pulse per second, the numbers of pulses required to reach a temperature of 50° C (122° F) were 4500 and 700, for charge levels of 200 and 400 volts respectively.

Source: A. C. Ducati of
Geotel, Inc.
under contract to
Langley Research Center
(LAR-11033)

No further documentation is available.

HIGH-SPEED ANALOG SWITCH FOR CRT-DISPLAY STROKE-WAVEFORM GENERATORS



Stroke-Waveform Generator Using DAC Switches

The slow switching transients of a digital-to-analog converter (DAC) limit its applicability as a switch in alphanumeric-waveform generator circuits to those that produce symbols in an average time of 10 microseconds or more. A faster analog switching system for a high-speed stroke-waveform generator for CRT display is shown in the figure. The circuit can be incorporated into both existing and new designs for high-speed alphanumeric-generator and vector-generator circuits using DAC switching and wideband analog integrators.

The principal switching element of the device is a digital-to-analog converter (DAC) that produces a switched stroke slope current that is applied to an impulse filter. The filter attenuates spikes before the current enters the integrator. The circuit increases speed in digital-to-analog switched integration by a factor of five. It produces symbols in an average time of 2 microseconds per character, or 100 nanoseconds per stroke, with low distortion.

Source: M. E. Casciolo of
United Aircraft Corp.
under contract to
Johnson Space Center
(MSC-14547)

No further documentation is available.

IMAGE ENHANCER FOR AIRBORNE SCANNERS

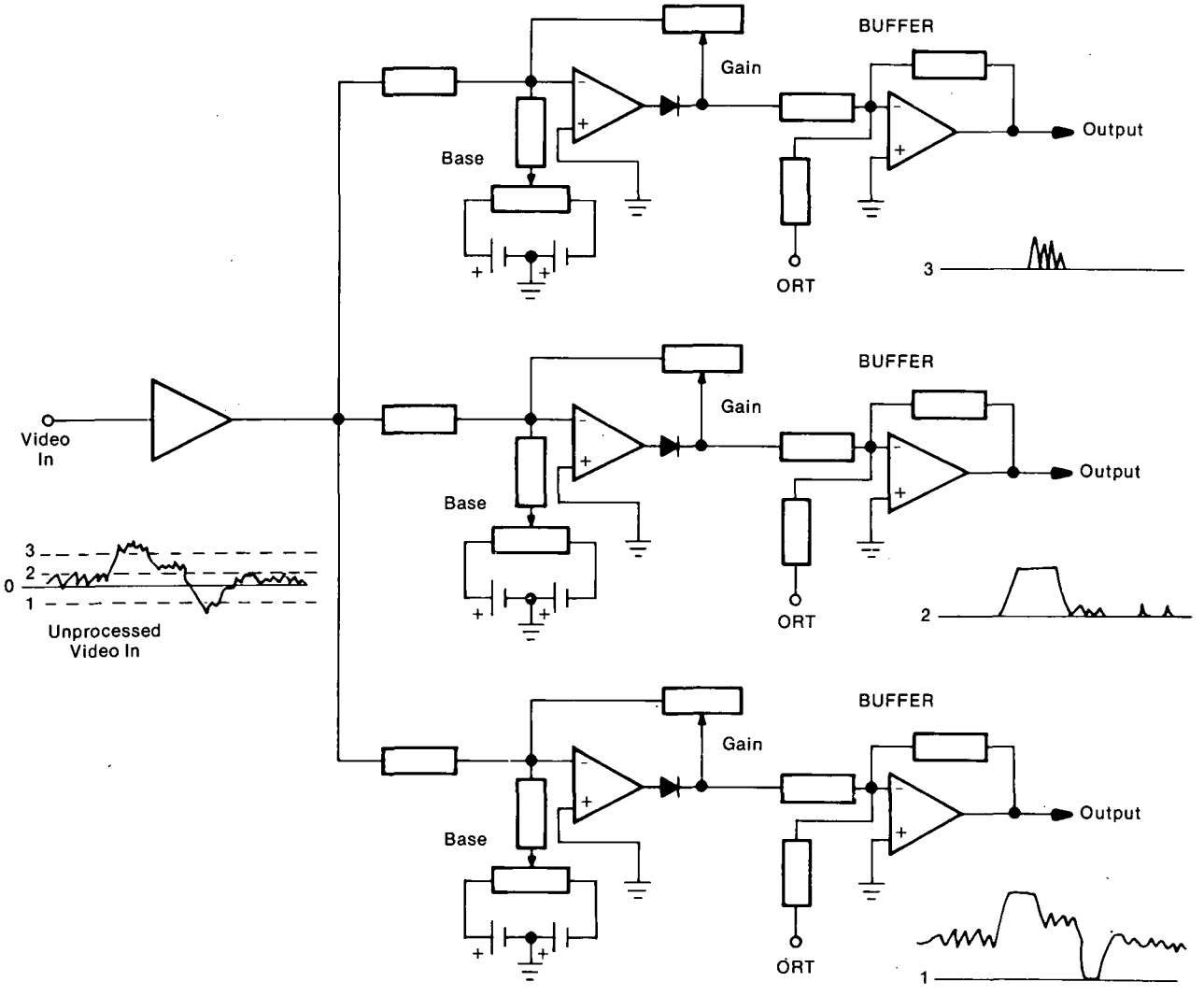


Image Enhancer

The image enhancer diagramed in the figure enables contrast enhancement of selected portions of a video transmission to provide magnified thermal resolution over a wide range of temperature. Temperature differences of 0.01° C (0.02° F) can be resolved over a 100° C (180° F) range. All signals below an output reference threshold (ORT) are inhibited; all signals above the ORT are amplified according to the gain setting on each of the three amplifiers. All signals above a maximum permissible amplitude set on each of the three amplifiers are clipped.

Threshold and gain adjustments are stable since they are contained within feedback loops. Quantitative information is obtained after post-flight calibration due to gain stability and temperature accuracy. This is the first known use of such a device on infrared scanners.

Source: R. W. O'Neill and
R. F. Merkel of
Lockheed Electronics Co.
under contract to
Johnson Space Center
(MSC-14480)

No further documentation is available.

IMPROVED ELECTRON-GUN BEAM DEFLECTION AND FOCUSING

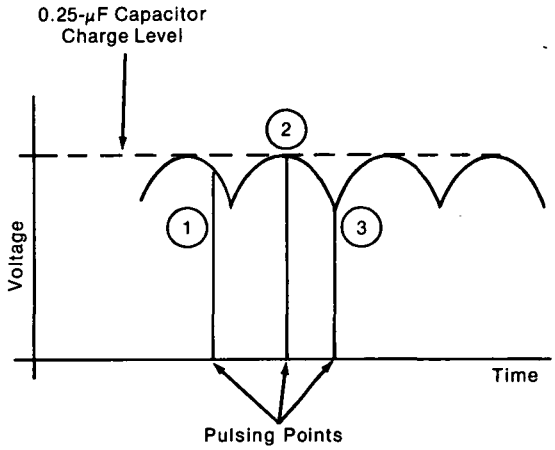


Figure 1. High-Voltage Power-Supply Commutation Voltage

When a high-current electron gun is aimed at a point target and pulsed, the accelerating potential provided by the power source drops, due to the no-load to full-load current demand. Figure 1 shows the three-phase commutation waveform of the high-voltage power supply. A 0.25-μF capacitor at the output charges up to its peak value when no current is drawn. When the beam is pulsed, drawing current, the capacitor loses its charge and the voltage drops. After this initial drop, the voltage is dependent on the output impedance, that is, the current drawn and the commutation voltage of the power supply. Thus, if the beam is pulsed at three different points, as shown in Figure 1, the voltage drops in these three cases are different, since they occur at three different phases of the commutation voltage.

The drop in voltage has two effects: (1) change in beam focus and (2) deflection of the beam. Because of the uneven voltage drops, there is no point at which an operator can direct and focus the beam. Referring to Figure 1, if the beam is focused and directed when the pulse occurs at point 2, both the focus and the direction are different when the pulse occurs at points 1 or 3. Conventional methods of correcting this problem, by adding additional capacitors to the output of the power supply, are expensive. Also, in the event of a short circuit or arcing inside the electron gun, the capacitor discharge can damage the gun or the associated wiring. This system monitors the output voltage drop, and the beam is cut off when a predetermined voltage drop is reached. Thus, the voltage drop is held to a constant and manageable level, and the aim of the electron gun is improved under pulsed conditions.

Figure 2 illustrates the circuit used to achieve beam equalization. The cathode voltage is attenuated 1000 times and ac coupled, blocking the dc component so that only the fluctuation of voltage is passed. This voltage variation is amplified and applied to a Schmitt trigger, which can be adjusted to fire at a particular cathode voltage. The output of the Schmitt trigger is applied to a gate via a monostable multivibrator, the output of which is normally a logic 1. When the external pulser applies a logic 1, it is passed through the gate and inverted to produce a pulse at the output of the level changer/amplifier, which turns on the beam.

When the voltage at the input of the Schmitt trigger falls to a level determined by the variable resistor on its input, the trigger fires, changing the state of the multivibrator and closing the gate. This ensures that the cathode voltage always falls to the same potential and minimizes defocusing and drift. The multivibrator remains set for 10 milliseconds. This delay serves to prevent the gate from being enabled again on the same external trigger pulse. This could occur if the cathode voltage is allowed to rise to the point where the Schmitt trigger resets, before the external pulse ends.

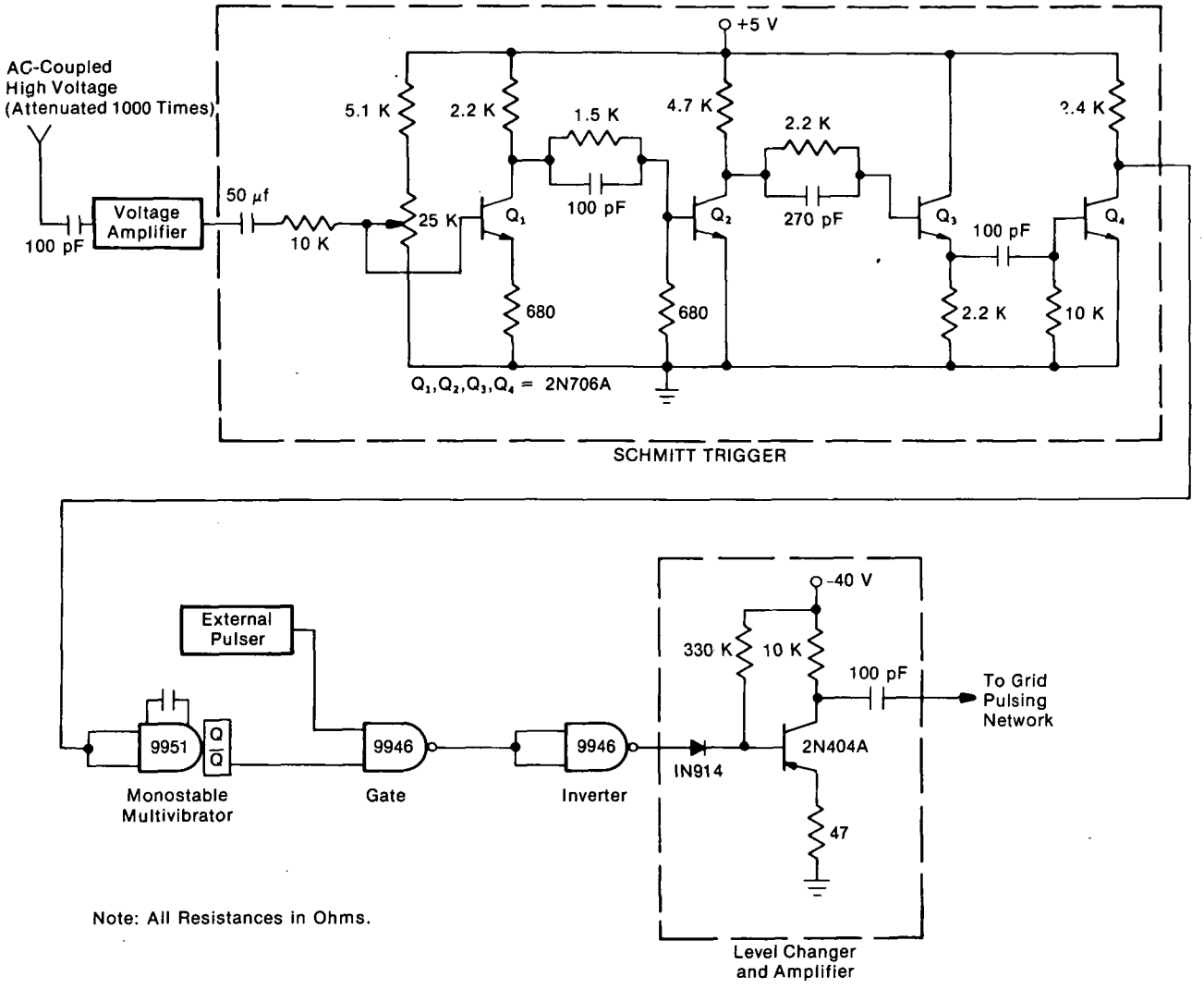


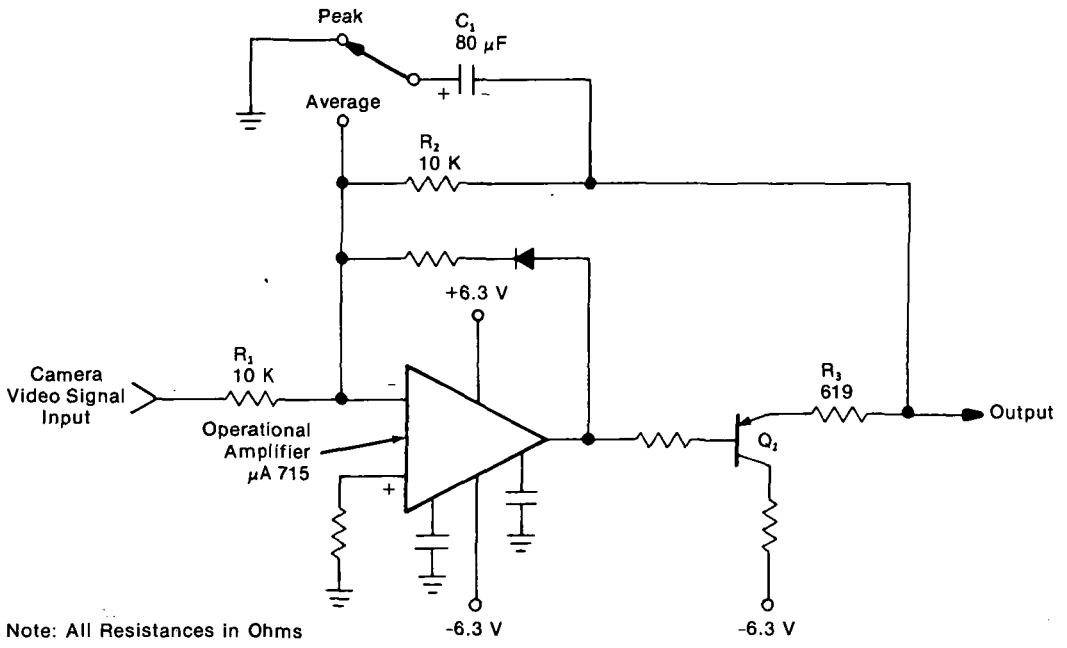
Figure 2. Beam Equalization Circuit

It should be noted that the total energy in the beam will vary for each pulse. For a particular application, the energy variation should be observed and, if the minimum available energy is less than that required to perform a particular function, the beam current can be increased. In many applications this variation of energy is of no particular significance.

Source: S. K. Dalal of Wyle Laboratories under contract to Langley Research Center (LAR-11475)

Circle 13 on Reader Service Card.

VIDEO PEAK/AVERAGE DETECTOR



Video Peak/Average Detector

A new circuit detects either peak or average signals. The mode of operation can be switched by a single-pole, double-throw switch. The circuit (shown in the figure) can be used in automatic light-control systems for television cameras, where the video output must be constant over large ranges of input light level.

The main advantage of this circuit is that it does not require the conventional double-pole, double-throw switch. In addition, an operational amplifier (op-amp) with feed-back makes the device precise and temperature stable. The detector is basically a unity-gain, inverting amplifier with feedback. Components shown in the figure, but not described, are used for biasing and stabilization.

In the peak mode one side of capacitor C_1 is grounded. When a positive-going video signal is applied to the input, the other side of C_1 is charged negatively by the op-amp through transistor Q_1. The charging process stops when the output is the negative equivalent of the positive input peak. Between peaks the voltage on C_1 decays through R_2 and R_1 and not through Q_1, because Q_1 emitter has no positive return. Thus Q_1 acts as a rectifier. R_3 sets the charge time so that when a minimum-width input pulse is received the circuit cannot detect it. In practical terms this limits the portion of a scene highlight that can be peak detected.

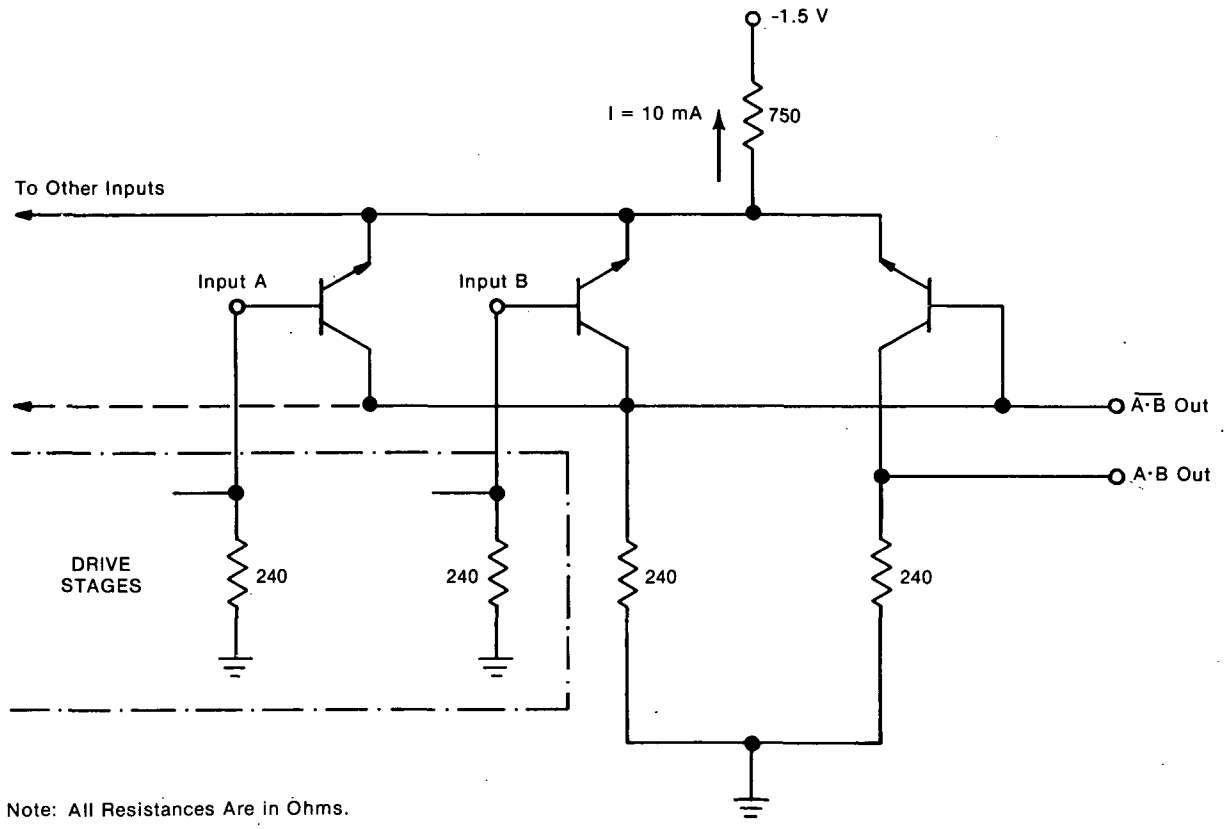
In the average mode, C_1 is connected in parallel with the feedback resistor R_2. Then the circuit acts as a low-pass filter, and the output is a dc potential equal to the input average.

A positive voltage return path for the emitter of Q_1 is not necessary. This path is provided by R_2 into the inverting input of the operational amplifier. The elimination of a positive voltage return for Q_1 emitter makes the circuit unique. It allows Q_1 to play a dual role: a rectifier in the peak mode, an emitter-follower in the average mode. Thus no additional switching is required at Q_1. In addition, since the output of the detector is the feedback point, temperature variations in the emitter-base drop of Q_1 are automatically compensated.

Source: J. D. Bingley of
RCA Corp.
under contract to
Johnson Space Center
(MSC-14482)

No further documentation is available.

FAST LOW-POWER-DRAIN LOGIC CIRCUITS



Note: All Resistances Are in Ohms.

AND - NAND Gate

The AND-NAND gate logic circuit in the figure has a fast (in the nanosecond range) response time, a low (in the milliwatt range) power drain, and does not use tunnel diodes. Tunnel diode circuitry, although exhibiting low power drain and fast response time, is difficult to manufacture because of the severe temperature limitations imposed by the tunnel diode.

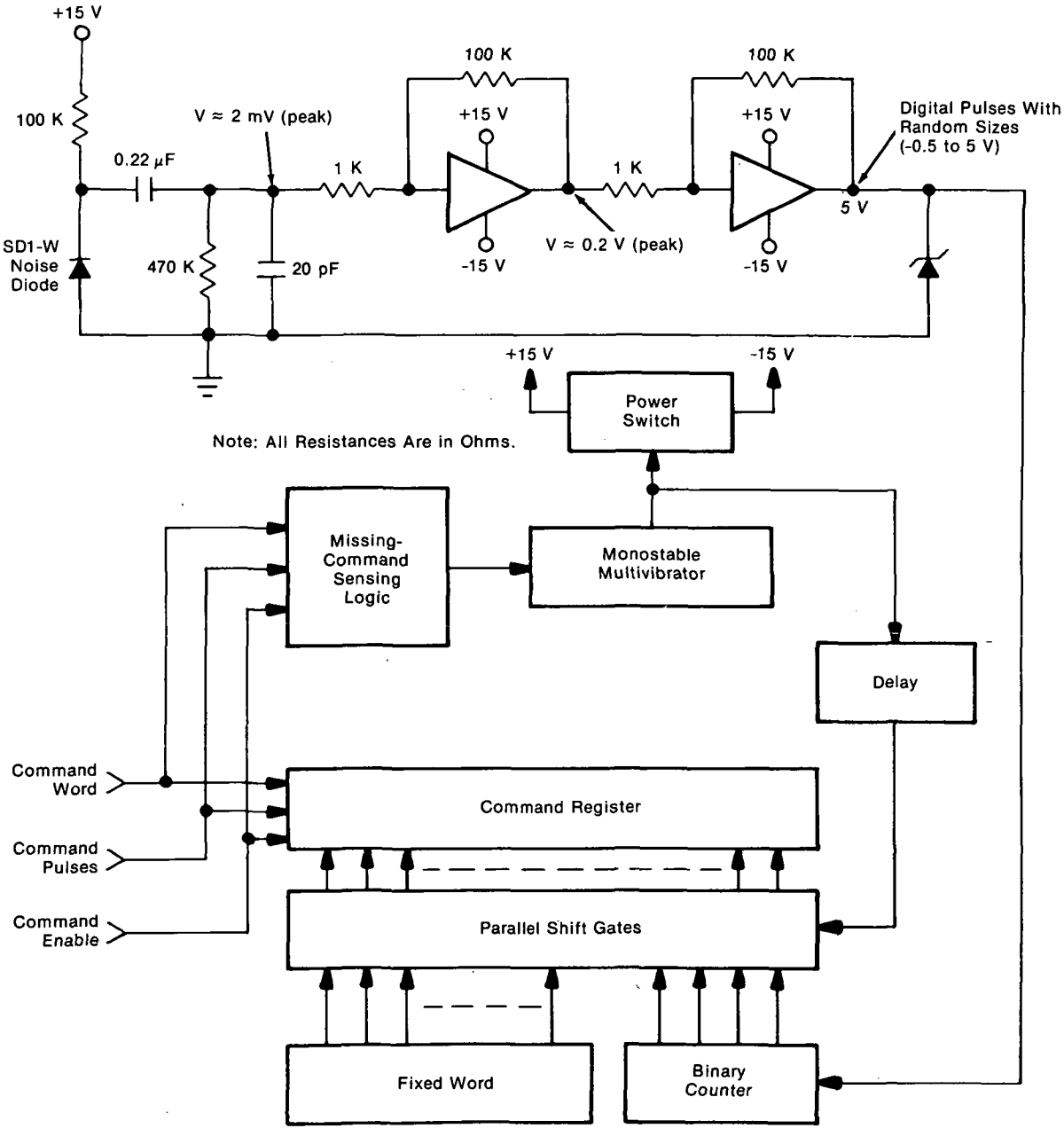
In addition to the 240-ohm output impedance circuit in the figure, a bistable version of the same logic family as well as an AND-NAND gate with a 50-ohm output impedance and a power drain of 7.2 mW have been investigated. The circuits may be constructed using a power supply with opposite polarity. Instead of npn transistors, pnp transistors are used to obtain signals of opposite polarity.

Two features of the circuits are believed to be new: (1) the use of current switching with a feedback arrangement, giving a snap-on effect, and (2) the operation of a fast, reliable logic circuit with a single supply voltage as low as 1.25 V.

Source: Ciro A. Cancro
Goddard Space Flight Center
(GSC-11366)

Circle 15 on Reader Service Card.

RANDOM AUTOMATIC SEQUENCING WITHOUT A MEMORY



Random Automatic Sequence Circuit

The circuit illustrated in the figure randomly selects one of 16 modes each time power is applied to a system, without the use of a nonvolatile memory or permanently applied power. This circuit was designed to keep a system operating in the event of a computer failure. Three lines connect the system to the computer. All three lines must be operating in order to inhibit the random-word generator. If one or more of these lines fail, the sensing logic triggers a monostable multivibrator that turns on a noise generator for several milliseconds. Each time it is operated, the noise generator provides a different number of pulses to a four-stage counter, producing a different 4-bit word each time.

The 4-bit word is shifted into a fixed-length command register after the monostable multivibrator pulse has terminated; the other bits in the command register are transferred from a fixed, preset word register at the same time. These other bits contain system parameters that remain fixed during the random selection of system modes. The circuit has application as a random-number generator for statistical applications, such as the automatic random selection of production items for acceptance testing.

Source: Jules J. Dishler and David F. Stout of
Martin Marietta Corp.
under contract to
Langley Research Center
(LAR-11080)

No further documentation is available.

COMPLEMENTARY MOS FOUR-PHASE LOGIC CIRCUITS

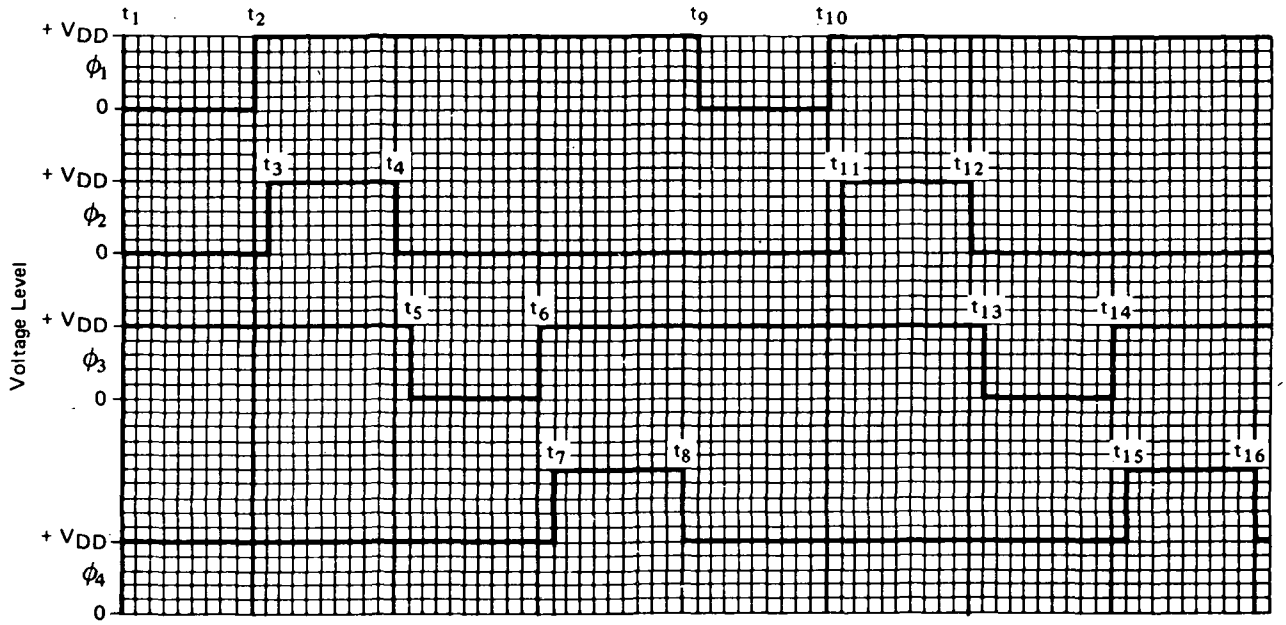


Figure 1. Complementary Four-Phase Clock Waveforms

Logic circuits often use a four-phase clocking technique in conjunction with p-channel MOS (metal oxide semiconductor) devices to charge and discharge capacitors without providing a direct path from the power supply to ground. This arrangement saves considerable power compared to circuits having a load resistor between the power supply and ground. However, the p-channel, four-phase circuit has several disadvantages. Since it requires a four-phase clock, it cannot be used as a subassembly in a single-phase clock system without making prior provision for the clock generation. In addition, p-channel, four-phase circuits require two power supply voltages which makes it difficult to interface these circuits with other types.

A complementary four-phase logic can provide a four-phase clock signal from a single-phase clock and requires only one power supply voltage.

The circuit uses complementary MOS devices as switches which charge and discharge capacitors in accordance with circuit requirements, but without a direct connection between the power supply and ground. Figure 1 shows the four-phase clock waveforms, and Figure 2 is a schematic of the four-phase circuits.

The Type 2 circuit described in detail as an example operates as follows: during clock time t_1 to t_2 (Figure 1), Φ_1 turns transistor Q_3 (Figure 2 - Type 2) on and holds transistor Q_2 off. This changes capacitor C_2 to $+V_{DD}$. From time t_3 to t_4, Φ_1 turns Q_3 off and Φ_2 turns Q_2 on. If at this time the input to Q_1 (LOGIC$_2$) is a logic "1" ($+V_{DD}$), Q_2 and Q_1 will form a conductive path which discharges C_2 to ground or logic "0". If, however, the input to Q_1 is a logic "0" (ground is zero volts), then C_2 remains charged to $+V_{DD}$ (logic "1"). The voltage on C_2 or the output of

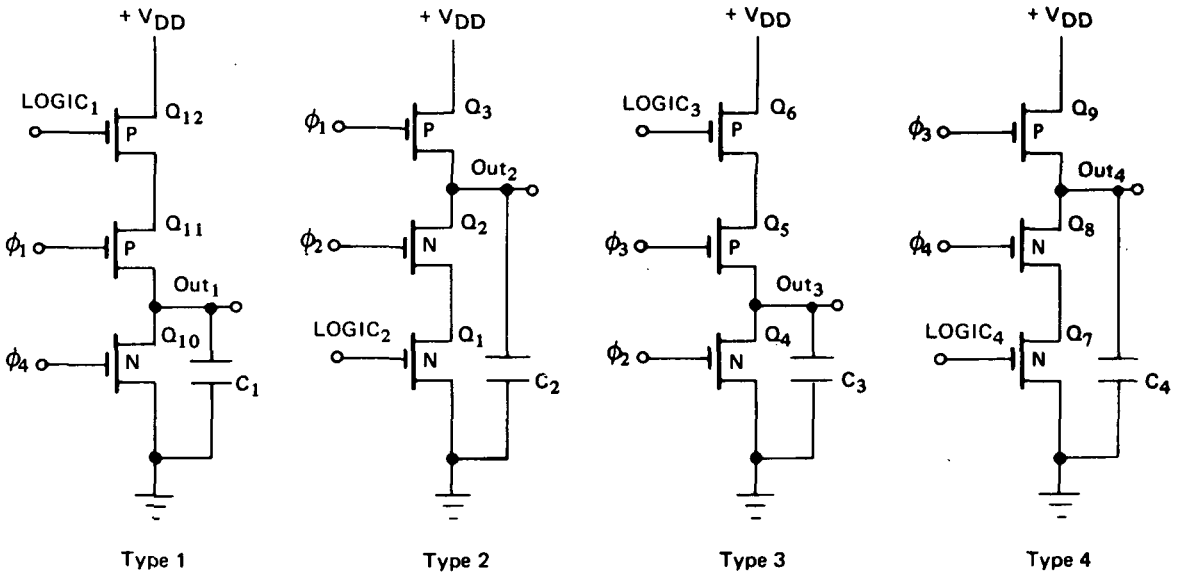


Figure 2. Complementary Four-Phase Circuits

this circuit then remains unchanged and is valid during time t_4 to t_9. This circuit thus operates as an inverter which is precharged during t_1 to t_2, evaluated during t_3 to t_4, and valid during t_4 to t_9.

The Type 3 circuit operates in a similar manner and is also an inverter; it is precharged during t_3 to t_4, evaluated during t_5 to t_6, and valid during t_4 to t_9. Circuit Type 4 is similar to Type 2, and Type 1 similar to Type 3.

The four-phase clock waveform can be generated by the circuit from a single phase input. This can be done because the complementary inverter has a finite and predictable propagation delay. Thus, the output of the inverter is the inverse of the input, but is delayed by a small time. The output of a number of inverters can be joined in series and connected to logic gates to produce the required four-phase clock pulses shown in Figure 1.

Source: H. L. Petersen and D. K. Kinell of
Lockheed Missiles and Space Co.
under contract to
Johnson Space Center
(MSC-14240)

Circle 16 on Reader Service Card.

Patent Information

The following innovations, described in this Compilation, have been patented or are being considered for patent action as indicated below:

Four-Phase Differential Phase Shift Resolver (Page 2) MSC-14065
and
Complementary MOS Four-Phase Logic Circuits (Page 40) MSC-14240

These inventions are owned by NASA, and a patent application has been filed. Inquiries concerning nonexclusive or exclusive license for their commercial development should be addressed to:

Patent Counsel
Johnson Space Center
Code AM
Houston, Texas 77058

Digital Phase-Locked Loop (Page 4) GSC-11623

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Goddard Space Flight Center
Code 704.1
Greenbelt, Maryland 20771

Phase-Detecting, Self-Directing Digital Couplers: A Concept (Page 10) MFS-24426
and
Flexible Playback Speed Control for Tape Recorded Data (Page 14) MFS-22972
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Inverted, Voltage-Controlled Oscillator (Page 20) MFS-22924
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Integrable Power Gyrator (Page 22) MFS-22342
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Rapid Battery Activation and Cell-by-Cell Voltage Measurement (Page 25) MFS-22749
and
Solid-State Power Switch (Page 26) MFS-22880

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