HIGH RESOLUTION INFRARED RADIATION SOUNDER (HIRS) FOR THE NIMBUS F SPACECRAFT

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16. Abstract

Flown on Nimbus F in June 1975, the HIRS scans with a geographical resolution of 23KM and samples radiance in seventeen selected spectral channels from visible (.7 micron) to far IR (15 micron). Vertical temperature profiles and atmospheric moisture content can be inferred from the output. This report describes system operation and test results.

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PREFACE

The High Resolution Infrared Radiation Sounder (HIRS) program is intended to provide an experimental approach to infrared radiation sounding combining the three bands of longwave (6.7 to 15 micron) shortwave (centered on 4.3 microns) and visible (0.69 microns). The sixteen infrared channels are chosen to provide information from atmospheric constituents at selected altitudes from sea level to 150,000 feet (1000 to 2 millibars). Data from single or multiple samplings may be combined to infer vertical temperature profiles, water vapor content, cloud height and cloud water vapor content. The visible channel data is used to infer albedo, cloud albedo, and the planetary albedo.

Design details of the HIRS system are described in this report to provide the background for understanding system operation and to aid in system evaluation. This information is also useful relative to spacecraft interfaces and orbital performance.

Results of tests on the protoflight system are described in detail. Some information from early orbital data are included to evaluate instrument performance. No attempt is made in this report to define or evaluate the scientific results of the HIRS system.

Instrument performance in orbit verified the quality established during acceptance testing. The quality of early data and the apparent reliability of the system establish the capability of multichannel infrared sensing using the selected techniques. Evaluation of design limitations indicates a need in future systems for a higher power capacity radiative cooling system to increase the response of the longwave channels and the desirability of an improved technique for a driven chopper that does not include a high speed gear mechanism. With these alterations, the basic HIRS design can be expected to provide for future sounding requirements.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

LIST OF TABLES (Continued)

1.0 HIRS SYSTEM

1.1 System Description

The High Resolution Infrared Radiation Sounder (HIRS) is intended to provide radiometric measurements which can be used to determine global atmospheric temperature profiles from the surface to 2 millibars atmospheric pressure. The instrument is on the Nimbus 6 Spacecraft and can provide global atmospheric temperature profiles twice each day.

Seventeen selected spectral channels provide a visible window (.693μ) a surface temperature window (3.71μ) and a long wave window (11.11μ). Seven of the long wave channels provide CO_2 absorption data for temperature sounding, two provide water vapor sounding, and five short wave channels provide N_2O and CO_2 temperature sounding data. Sampling of the individual channels is performed by time multiplexing three detectors by means of a single telescope and a filter wheel containing the seventeen spectral filters.

High spatial resolution of 23.3Km (12.6 n miles) at nadir and near continguous geographic sampling enable profiles to be taken under all but extensive overcast cloud conditions. A cross course scanning system provides 1820 Km path width coverage with 42 sample points per scan. Sampling is obtained when the scanning mirror is stopped at each of the 42 locations.

In-flight calibration of the HIRS system is provided by two stable references on the instrument, (290K and 265K) and a space look which are examined after a sequence of twenty scan lines. A scan grid of twenty scan lines and the three calibration scans occurs approximately once every 112 seconds, sufficient to maintain short term calibration in the order of .02%. Electronic calibration of the signal amplifier chain occurs on every scan retrace period, providing a system check every 4.9 seconds.

Data from the HIRS instrument is digitally multiplexed to a single data stream and fed to the Nimbus High Data Rate Subsystem (HDRSS). At the ground station this data is reduced for processing via computer by the NASA/Goddard Institute for Space Studies on an orbit-by-orbit basis and by NOAA/NESS for backup processing.

The HIRS unit as shown in Figure 1.1-1 is a single instrument having combined scanning, collecting and sampling functions and electronics in a single package. The major features of the instrument are shown in Figure 1.1-2. A summary of basic system parameters is given in Table 1-1, and a list of the spectral bands and characteristics are given in Table 1-2.

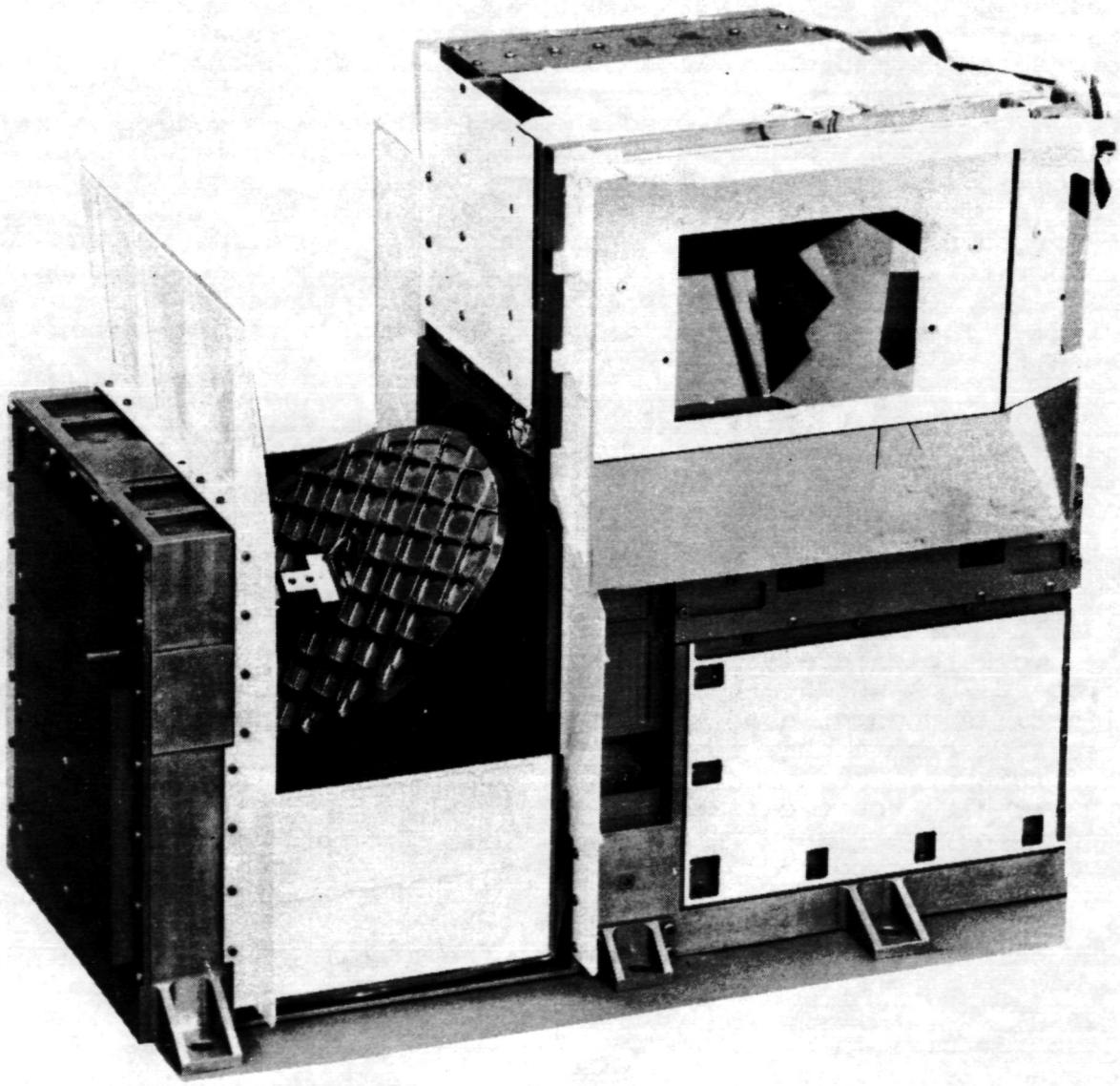


FIGURE 1.1-1 HIGH RESOLUTION INFRARED RADIATION SOUNDER (HIRS)

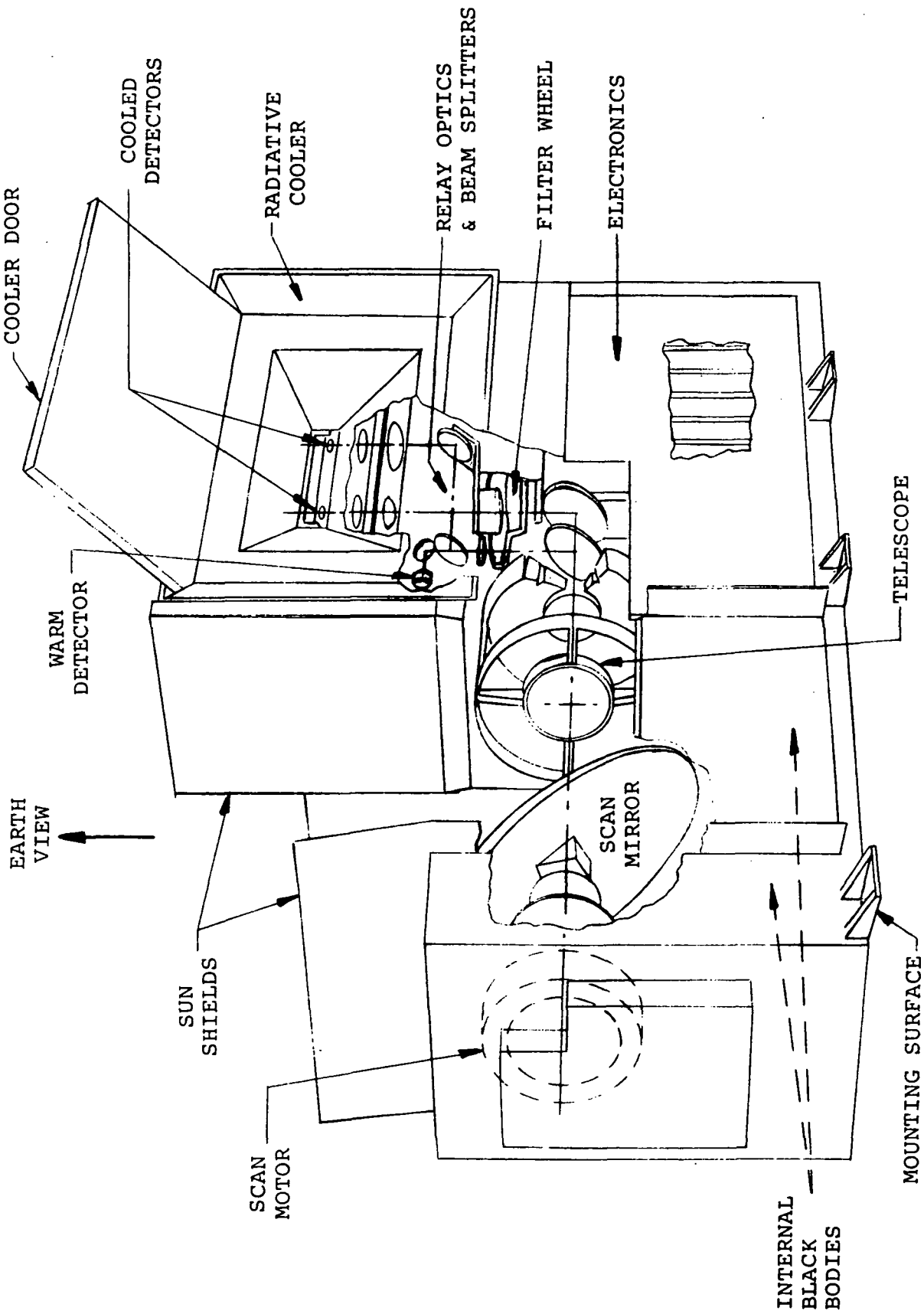


FIGURE 1.1-2 HIRS STRUCTURE

TABLE 1-1 HIRS SYSTEM PARAMETERS

SPACECRAFT	NIMBUS F
ALTITUDE	600 N.M.
OPTICAL FIELD OF VIEW	1.2 DEGREES
SINGLE TELESCOPE	5.9 INCH DIA.
LONG WAVE DETECTOR	HgCdTe
LONG WAVE CHANNELS	10 (6.7 TO 14.95 MICRONS)
SHORT WAVE DETECTOR	InSb
SHORT WAVE CHANNELS	6 (3.7 TO 4.57 MICRON)
VISIBLE SPECTRUM DETECTOR	SILICON
VISIBLE SPECTRUM CHANNEL	1 (.69 MICRON)
RIGISTRATION, ALL CHANNELS	.06 DEGREES
IFOV ON EARTH SURFACE	13 N.M. DIA. AT NADIR
SCAN STEP INTERVALS	1.8 DEGREES
EARTH SCAN COVERAGE	$\pm$ 37.5°
EARTH SWATH COVERAGE	1820 KM
IR CALIBRATIONS	290K TARGET, 265K TARGET, SPACE
SIZE	13 X 21 X 18 INCHES
WEIGHT	73 POUNDS
POWER	23 WATTS AVE
DATA OUTPUT	SERIAL BI PHASE, 3389.8 BPS
DIGITAL RESOLUTION	12 BITS PLUS SIGN
COMMANDS	22
DIGITAL TELEMETRY	11
ANALOG TELEMETRY	23
RADIANT COOLER TEMP	124 K CONTROLLED 118 K UNCONTROLLED
COOLER DECONTAMINATION	CLOSE DOOR, HEAT COLD PARTS
FILTER WHEEL SIZE	7 INCH DIA.
FILTER WHEEL ROTATION	565 RPM
LW CHOPPER ROTATION	3390 RPM

TABLE 1-2
HIRS SPECTRAL BANDS

PURPOSE	CHANNEL		WAVELENGTH	WAVE NUMBER	HALF BW
	1	CO_2	14.95μ	669.1 cm^{-1}	2.8
	2	CO_2	14.73	678.8	13.7
TEMPERATURE	3	CO_2	14.49	690.1	12.6
SOUNDING	4	CO_2	14.25	701.6	15.9
	5	CO_2	13.99	716.5	17.5
	6	CO_2/H_2O	13.66	732.3	18.4
	7	CO_2/H_2O	13.35	749.1	18.4
WINDOW	8	WINDOW	11.12	899.6	34.6
WATER VAPOR	9	H_2O	8.14	1228.2	63.4
SOUNDING	10	H_2O	6.69	1494.9	87.6
	11	N_2O	4.56	2190.8	20.6
TEMPERATURE	12	N_2O	4.52	2211.9	22.5
SOUNDING	13	CO_2/N_2O	4.46	2244.2	21.6
	14	CO_2/N_2O	4.40	2274.5	35.2
	15	CO_2	4.24	2357.6	23.0
SURFACE TEMP	16	WINDOW	3.71	2692.4	296.9
CLOUD DETECTION	17	WINDOW	.693	14443.0	892.2

1.2 Development Program

The High Resolution Infrared Radiation Sounder Program (Contract NAS5-21651) evolved from a preliminary study (Contract NAS5-11801) and the results of the early design activity resulting in a Design Study Report, February 1972. Scientific requirements were defined by NASA Goddard which included spectral bands, resolution, coverage, and noise equivalent radiance. Some modification of the scientific requirements were generated after the study program and included in the instrument.

A program of development, fabrication and test resulted in the fabrication of an engineering model, prototype, and flight model. The program was modified to upgrade the prototype to protoflight status, and complete the Flight Model as a backup unit. The majority of data presented in this report will relate to the Protoflight Unit. Special test equipment fabricated for the test, calibration, and data reduction consisted of one bench test unit for operation at the integrator's facility and a more complex bench test unit and data processing system for operation, test, and calibration of the unit at the manufacturer's facility.

Delivery of the Protoflight Unit on December 16, 1974 to General Electric Valley Forge Space Facility was followed by spacecraft integration, test, and launch. Operating characteristics and test data from the system qualification tests and from the spacecraft qualification test are included in this report.

1.3 Protoflight Event Chronology

1.3.1 General

The Protoflight unit was physically complete in late January 1974. A sequence of acceptance tests was started in early February but was halted when various electrical and mechanical deficiencies were found. The following chronology is not intended to describe each event, these are documented in periodic reports. The quarterly report for Jan-March 1975 lists the key test results relating to each equipment specification. Those results appear in appropriate places in this report.

1.3.2 Chronology, 1974

Feb.	7	Functional Testing Started
	9	Preliminary Electrical Test Complete
	10	Scan System Tests Completed
	11-16	Video noise and motor jitter investigation

Feb.	16-18	Optics FOV and alignment test
	16	Motor changes for jitter reduction begin
	20	Circuit changes for jitter effect reduction
Mar.	15	Transmitted first data to GSFC over land line
Apr.	25	Chamber checkout of modified assembly
May	11-28	RFI test
June	4	Chamber test of modified assembly
	5-12	Alignment on bench cooler and optical tests
	12-14	Chamber Test
	15-19	Bench Adjustment to reduce jitter
	20	Chamber test of system changes
	21-30	Latest double anti-backlash filter wheel gearing installed, system tested on bench cooler
July	5-7	Pre-vibration Chamber Test, NOAA review of data
	9-12	Vibration tests at GSFC. Problem of scan mirror loosening. Patch failure. Component lead failure
	14-19	Analyses and Correction of Failures
	20-21	Bench Cooled Tests
	22-27	Chamber Tests with backup cooler
Aug.	1-10	Deliver to GE for integration test
	12-30	System reassembled after modification
Sep.	5	Vibration test of System less cooler
	7-13	Chamber test, cooler performance
	15	Bench cool tests and optic alignment start
Oct.	25	Final alignment. Functional acceptance tests
Nov.	1-8	Pre-Vibration Thermal Vacuum Test
	9-12	Vibration Test
	14-26	Thermal-Vacuum Test, Thermal Cycling and Calibration Tests
Dec.	6	Final System Tests complete
	9	Vacuum Chamber test of scan system
	12-13	Low level vibration test to check encoder
	16	Delivery to G.E.
Jan.	1975	Unit mounted on Spacecraft. Functional tests.

Feb.	4	Modification of cooler door cam and change to increase cone heat.
	23	Vacuum-Thermal Test 2 started
	27	Door problem and cooling problems
Mar.	7	Chamber test complete
	8-17	Tests and mod of door spring and cooler shroud
	25	Spacecraft RFI Test
	31	Spacecraft vibration test
Apr.	6	Illumination test
	17	Orbital Operation Tests
	23	RFI test
May	2-7	Confidence Test
	18	Ship to WTR
	23	Confidence Test, check door position
June	6,8,10	Confidence Tests
	12	Launch 08:12:45 Z Cone and Cooler Housing Heat ON
	13	Electronics ON 19:30:39 Z, Orbit 20

1.4 Summary of Results

The evaluation of the HIRS system has centered on the review of one characteristic of the system, the noise equivalent radiance NEΔN of each channel. A method of definition and the number of samples used in making this measurement have not always been consistent, and will be discussed in greater detail later in the report. Because of the dependence of the long wave channels on detector temperature, the results are summarized here for two conditions, a temperature controlled patch operating at 124^{o}K and an uncontrolled patch operating as it might in orbit with a partial duty cycle on the long wave detector bias, at a temperature of 118^{o}K. These are compared to the NEΔN designated by NASA and shown in Table 1-3. Channel 17 is shown on the chart without a definite system specification and a noise output equivalent to only .04% of maximum sun illumination on a diffuse earth having 100% reflectance. The system performance data has been reviewed by NASA and NOAA and is considered acceptable for flight conditions and highly useful for the scientific missions.

Optical registration of all channels is aided by the single telescope, and is disrupted only by the separation of the bands into two optical paths and by the use of three detectors. A comparison of bands and their registration shows a separation of .03^{o} for the visible to long wave and visible to short wave,

TABLE 1-3
HIRS SENSITIVITY
NOISE EQUIVALENT RADIANCE

($MW \cdot M^{-2} \cdot ST^{-1} \cdot CM$)

DETECTOR TEMP. / EARTH COVERAGE		SPEC.	118°K UNREGULATED 14%	122°K UNREGULATED COMPLETE	124°K REGULATED COMPLETE
CHANNEL	(CM^{-1})				
1	669.1	1.68	3.2	5.3	6.4
2	678.8	.56	.54	.90	1.1
3	690.1	.28	.40	.65	.79
4	701.6	.28	.26	.39	.46
5	716.5	.28	.40	.58	.68
6	732.3	.28	.28	.39	.45
7	749.1	.28	.30	.38	.43
8	899.6	.112	.24	.28	.30
9	1228.2	.168	.14	.19	.22
10	1494.9	.112	.11	.13	.15
11	2190.8	.002	.010	.011	.011
12	2211.9	.002	.0029	.0029	.0029
13	2244.2	.002	.0049	.0049	.0049
14	2274.5	.002	.0018	.0018	.0018
15	2357.6	.003	.0026	.0026	.0026
16	2692.4	.002	.0010	.0010	.0010
17	14443.	-	.04% Albedo		

NOTE: Protoflight Acceptance Test, ITT Chamber, F/C High Mode

and .06° for the long wave to short wave. The optical field of view is 1.28° for the visible, 1.24° for short wave and 1.17° for long wave.

Performance of the signal processing system is excellent. The 13 bit encoding system quantizes all signal data, electronic calibration data, and the digital telemetry. Non-linearity of the video processing electronics with electronic calibration signals as the input is within 1% of full scale and repeatable. The non-linearity and offset errors thus obtained are used to correct the received signal data. The system is calibrated on each grid by averaging the 42 samples taken at each of the calibration targets (Internal Warm, Internal Cold, Space), calculating the slope and intercept for each channel and applying that calibration to the scene radiance data. This calibration takes place in the ground station computer using the raw data from the instrument. A similar measurement during system qualification used this calibration data to predict the signal coming from the Earth Target in the test chamber. A general indication of the quality of the instrument is recognized when this prediction was generally accurate to within the noise limit of the system (about one count in short wave channels).

1.5 Early Orbital Flight Results

The Nimbus 6 Spacecraft was launched on June 12, 1975 into a near perfect 1100 Km orbit. Operation of the HIRS instrument followed a prepared program of outgas and operation. The HIRS launch configuration had the motors running (Scan slew, F/C High Mode), the electronics off, and cooler door closed. During the first orbit the cooler door position was verified, then cone and cooler housing outgas heat was turned on. This added input brought the cooler housing to 20°C, the cooler cone to 37°C and the patch to +8°C. The HIRS baseplate stabilized near 16°C, about one degree warmer than its mount. Temperature conditions are given in Table 1-4 for orbit 20. Electronics power was turned on during orbit 20, with early verification that the morror system was operating normally. In this mode we received data from the visible channel, confirming that portion of system operation. The cone and housing heat remained on and the cooler door closed until orbit 179 on day 14. Data during this outgas period is shown in Table 1-4 at orbit 179 prior to opening the door. During this period we noted that the internal calibration targets were near their nominal temperatures. Figure 1.5-1 shows the orbital variation of the warm and cold internal targets. This characteristic continues during the flight.

Cooled system operation began on June 25, 1975 when the cooler door was opened and the cone and housing heaters were

TABLE 1-4 HIRS DATA FROM ORBIT

Function			
Orbit Number	20	179	200
Scan Mirror Temp.	12.0C	12.0C	9.3C
Pri. Tel. Mirror	19.9C	19.0C	15.6C
Sec. Tele. Mirror	10.5C	12.0C	8.0C
F/C Housing T. 1	301.75K	303.50K	303.5K
F/C Housing T. 2	301.60K	304.00K	304.0K
F/C Housing T. 3	301.55K	303.30K	302.94K
F/C Housing T. 4	301.35K	303.50K	303.5K
F/C Motor Temp.	29.0C	29.0C	26.4C
Radiant Cone T.	307K	307.5K	173.04K
Rad Cooler Hsg. T.	20.0C	20.7C	0.4C
Baseplate Temp	16C	18.5C	15.6C
Electronics Temp	15.5C	18.7C	15.6C
Patch Temp	281K	280K	125.52K
Scan Motor Temp	17C	19.6C	17.7C
S/C Temp		16C	16C

turned off. Electronics remained ON during the cool down period for evaluation of the temperature changes. Temperatures stabilized after 48 hours as shown in the table for orbit 200. Note that the anticipated temperatures for the cooler housing was +3.5°C, cone 167°K and patch 123°K compared to values of +1°C, Cone 173K and patch 125K. An apparent deviation of cone performance from that anticipated and from chamber simulated tests is most noticeable. Coupling from the cone to patch is approximately 2:1 where a change in cone temperature to 168°K would have reduced patch temperature to the predicted 123°K.

HIRS radiant data began to appear at patch temperatures near 134°K. By the time the patch reached stable temperatures NOAA had a complete earth coverage data set. Table 1-5 lists the data from orbit 202. The sensitivity (slope of counts output to energy input) is precisely the anticipated values for that patch temperature. In tabulating the standard deviations a decrease in level is noted in both the long wave and short wave channels. We noted this effect in system tests when the filter wheel jitter was low and speculate that the gravity free condition of the system aids smooth operation of the gear assembly, resulting in reduced noise in the system. At this lower noise level the noise equivalent radiance (NEΔN) for each channel is at or below the values last measured in chamber tests.

Other characteristics noted from the orbital operation are the low number of sync losses attributable to filter wheel speed variation (approximately once per ten orbits), the early appearance then absence of a scan mirror temperature telemetry anomaly, and the continuation of a tendency toward odd or even numbers preference in some channels. All effects seen to date were known in earlier tests and are not affecting system quality.

An analysis of the temperature variation of the internal cold target (270°K) shows its rate of change to be within limits acceptable to data processing and calibration. It is noted from some evaluation of data that the 270K target has a slight offset in radiance when compared to a straight line fit of space, 270K and 300K target output for all channels. This causes a slight difference in calibration when a target radiance is determined by a slope based on the space and 270K target as compared to a slope based on the 270K target and 300K target. The difference in these slopes is of the order of .5%, not affecting the data seriously.

Since the initial operation of the system, when the patch reached 125.1°K on orbit 202 a gradual increase in patch temperature was noted. After 100 orbits the temperature reached 125.8°K and after 200 orbits it reached 126.2°K. At the same time it was noted that the slopes for all channels were decreasing, with approximately 15% loss after 200 orbits. In the long wave channels part of the degradation is related to patch

temperature increase (See section 6), with some indication of water vapor contamination and other broad band contamination. The degradation is tapering off and is expected to continue at lower rates with time. An outgas cycle is expected to be effective, since there was no apparent loss of transmission to the warm optic elements during the thirteen days of preconditioning. Evaluation of system operation and performance will continue during the flight and will be reported separately.

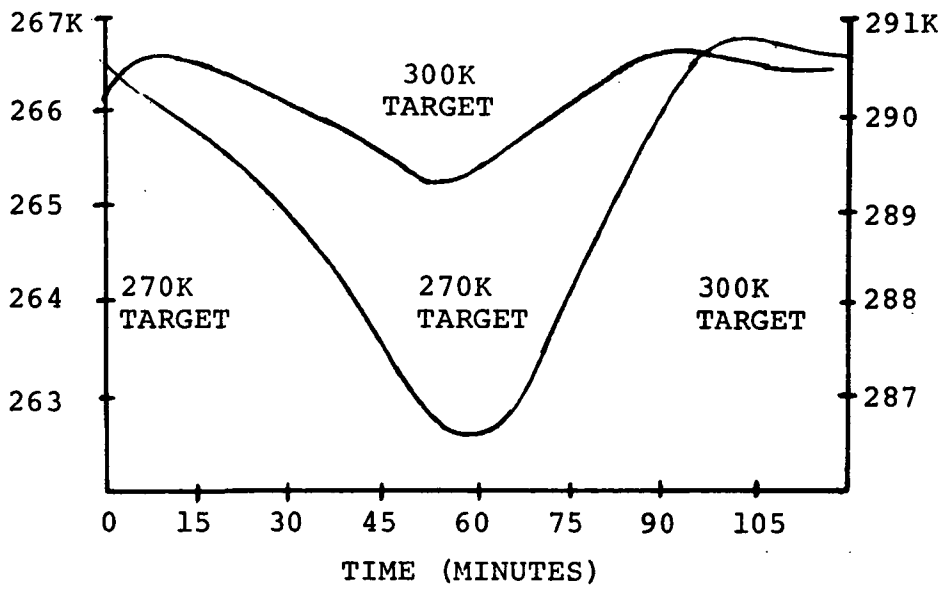


FIGURE 1.5-1

ORBITAL VARIATION OF HIRS INTERNAL CALIBRATION TARGETS

TABLE 1-5 SYSTEM PERFORMANCE (NEΔN) IN ORBIT

	ORBIT 202 PATCH TEMP 125.23K			V/T TEST 124.0K	SPEC
CHANNEL	SLOPE	σ	NEΔN	NEΔN	NEΔN
1	.717	4.0	5.58	6.4	1.68
2	2.460	3.3	1.34	1.1	.56
3	3.988	2.5	.63	.79	.28
4	6.743	3.9	.58	.46	.28
5	4.215	2.1	.50	.68	.28
6	6.832	2.8	.41	.45	.28
7	7.340	2.8	.38	.43	.28
8	7.599	2.3	.30	.30	.112
9	8.182	1.7	.21	.22	.168
10	16.499	2.2	.13	.15	.112
11	418.32	2.4	.0056	.011	.002
12	506.68	0.9	.0018	.0029	.002
13	445.38	1.1	.0025	.0049	.002
14	712.97	0.7	.0010	.0018	.002
15	591.10	1.4	.0027	.0026	.003
16	1326.2	1.2	.0009	.0010	.002

SLOPE is radiance input (ergs) for one quantized level (counts) at system output.

σ is standard deviation (1 σ) of output in counts when viewing a fixed scene.

NEΔN is the differential radiance equivalent to a 1 σ variation in the system output.

2.0 INSTRUMENT DESCRIPTION

2.1 General

The High Resolution Infrared Radiation Sounder consists of a single instrument containing all of the functions shown in Figure 2.1-1. The single surface, 6.0 inch (152 mm) diameter scanning mirror rotates 360° in 1.8 degree increments, driven by a permanent magnetic stepping motor. Electronic control of the stepping motor commands the motor through preselected sequences of scan, slew to each target and to start of scan. A slip-ring type pin encoder provides position reference points for each major position, while a tachometer and torque motor on the same shaft as the mirror provide velocity control and damping to aid slew rates and settling of the mirror at each step position. The timing sequences are given in Figure 2.1-2 showing that the complete grid takes place in 112 seconds and repeats continuously.

Radiant energy reflected from the scan mirror enters the cassegrain telescope having a 5.9 inch (150 mm) entrance aperture and a focal length of 10.4 inches (264 mm), producing an f/1.76 system.

A beamsplitter reflects the shortwave band and transmits the long wave bands, all of which are reflected to respective field stops, and through spectral filters in the filter wheel.

The filter wheel assembly is a single wheel containing the seventeen filters in two concentric rings. Short wave and visible filters on the outside ring set the spectral bandwidth and data period for these spectral channels. A chopper mounted integrally to the wheel converts the signal to an alternating signal with the black chopper tooth as the reference. The same general approach applies to the ten long wave channels on the inner circle, except that a separate high speed chopper provides a modulating frequency approximately 2.3 times that of the short wave channels. To improve the thermal stability of both the black surface chopper references and the filter transmission the complete filter wheel assembly is contained in a thermally isolated housing having precise proportional temperature control.

From the filter wheel the beams are relayed to the detectors, with the visible channel being split off to a warm Silicon diode detector while the short wave bands go to a cooled Indium Antimonide detector and the long wave bands to a cooled Mercury Cadmium Telluride (HgCdTe) detector. The cooled detectors are mounted on a radiating surface directed toward space. The cooler assembly consists of the cooled patch as a second stage radiant cooler mounted in a first stage cooler (cone). The cooler housing which holds the cone and patch

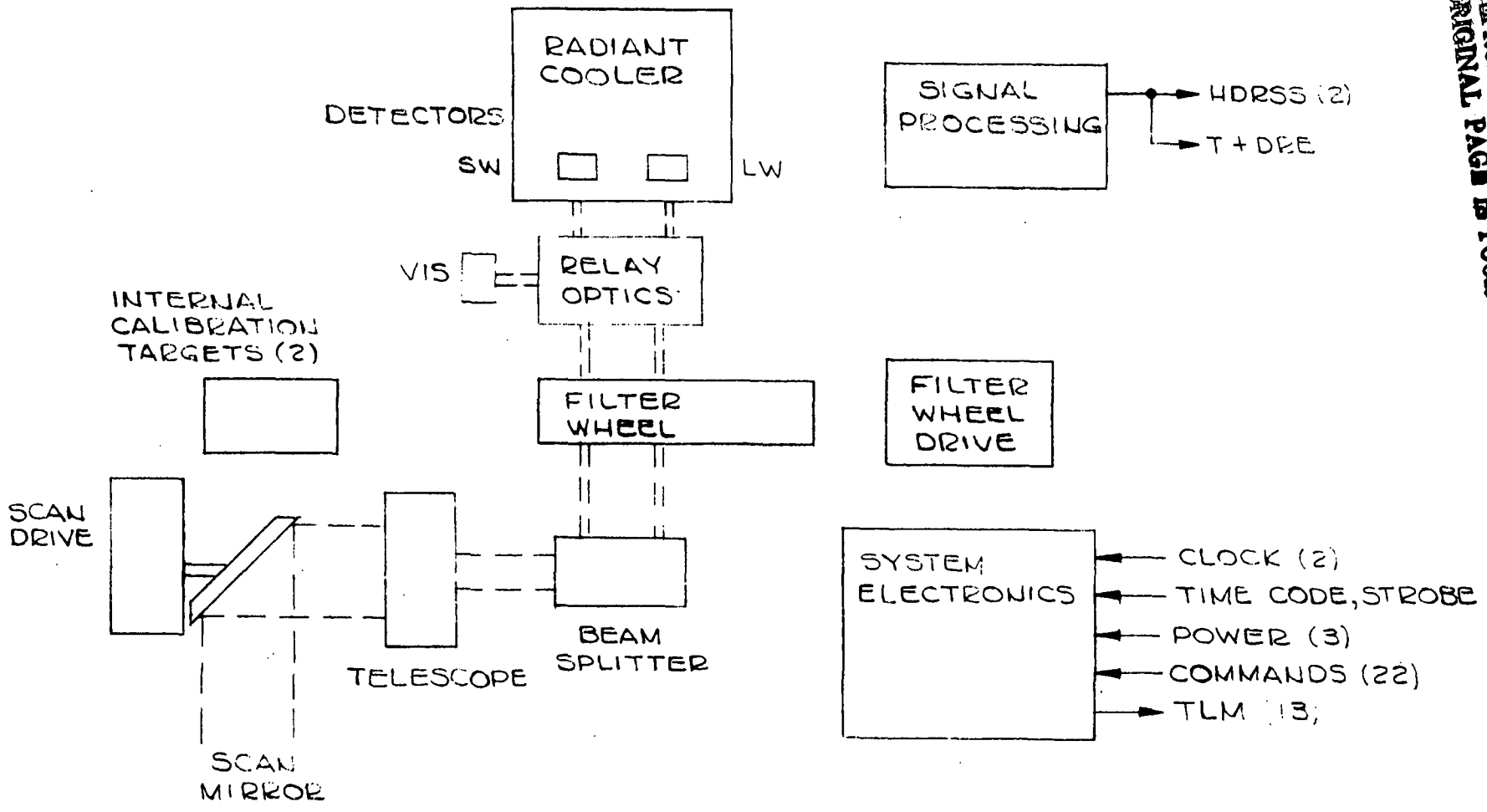


FIGURE 2.1-1 FUNCTIONAL BLOCK DIAGRAM

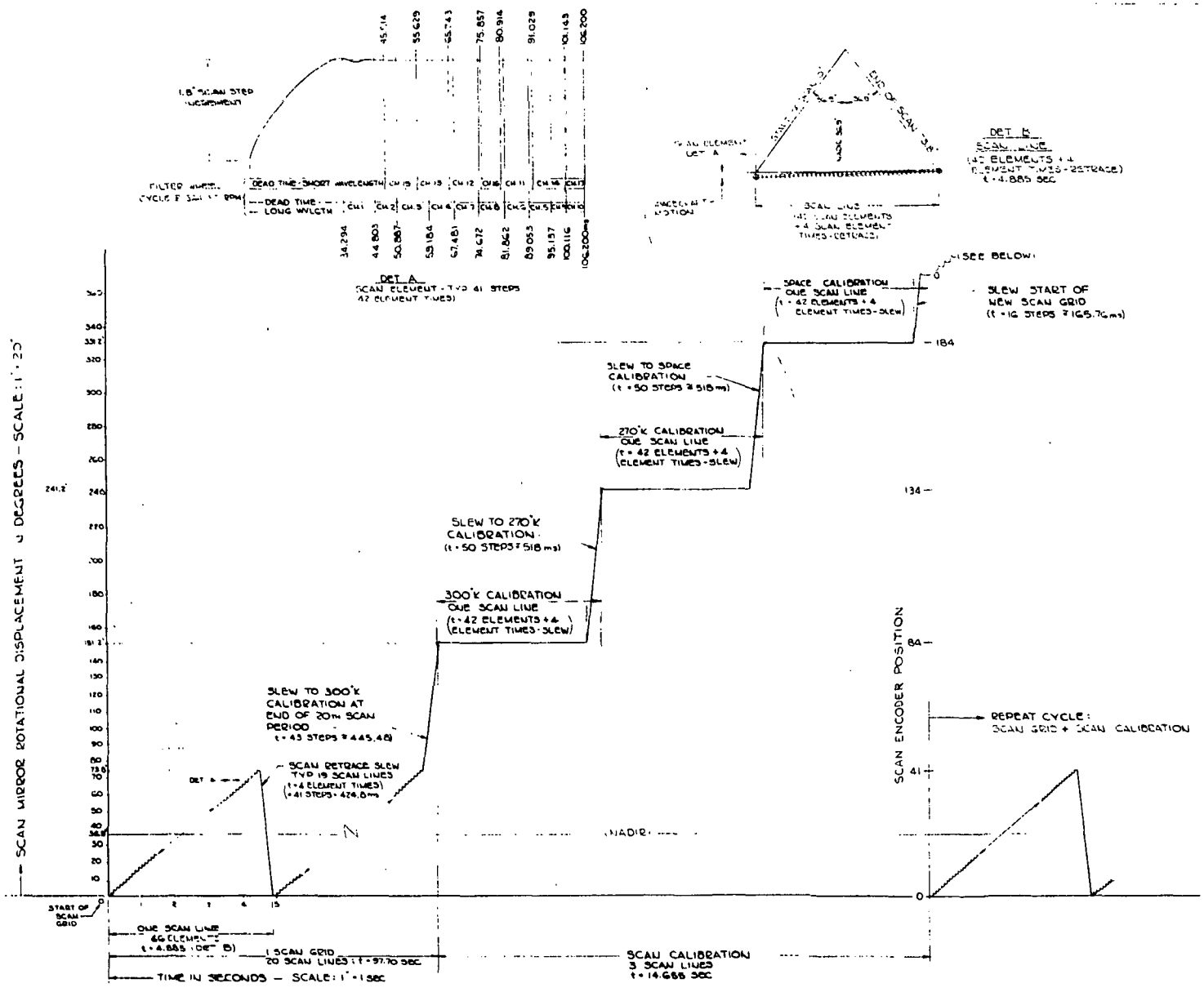


FIGURE 2.1-2 HIRS SCAN PATTERN TIMING DIAGRAM

assemblies is itself isolated from the main frame of the system to reduce heat input and aid thermal stability. Typical temperatures of the housing is $+4^{\circ}C$, while the cone is at $167^{\circ}K$ and the patch at $124^{\circ}K$.

The cooler housing is equipped with a door which closes over the cone radiating surface to permit heating of the cone and housing for driving of water vapor and other contaminants soon after launch or duing orbit when decontamination is desired. Applying heat brings the patch, cone, and housing above $0^{\circ}C$. The door is also an albedo shield in the deployed position.

Signal processing takes place in three amplifier chains, one for each detector, each designed for the particular detector characteristics. Low noise linear amplification of the chopper to scene a.c. signal precedes synchronous demodulation and electronic integration of these signals, resulting in a d.c. signal level suitable for analog to digital conversion, approximately -6.3 volts for a maximum signal. Unique characteristics of the HIRS instrument include selection of different integration times for many channels as the energy input is related to an optimizing of the amplifier range and time available. Some channels have only one cycle of input while others have up to seven. Electronic calibration voltages are inserted early in the amplifier stages and feed through the complete system to provide a reference for all data reduction. The accuracy of these calibration levels are in the order of .02% and remain stable over long periods.

Simultaneous integration of input signals occurs in the long and short wave bands. Multiplexing of the data occurs by selected timing of the analog to digital conversion process. Once converted to a straight binary plus sign digital format the data goes to storage registers, then is combined with other data for output.

In addition to the scene data and electronic calibration data, the output data stream includes time code, angular position of the scan mirror, command status, scan element number, scan mode, and temperature readings of the patch and warm and cold reference targets. The data rate is 3389.8 bits per second, bi-phase, and compatible with the Nimbus HDRSS system.

Power for the HIRS unit comes from the spacecraft minus 24.5 volt supply. Four separate power distributions are brought into the unit for mirror scan power, filter wheel drive, electronics and full time telemetry. The full time telemetry power input provides an unswitched source for

continuous monitoring of several internal temperatures, and cooler cover position. Scan motor current and F/C Motor current can be monitored when these sub-systems are on even though electronics is not on. The 23 telemetry points are listed in Table 2.1-1.

All operation of the HIRS is by means of remote commands. These commands are listed in Table 2.1-2. There are few restrictions on the sequency or time limit of any of the commands. The operator has options of selecting scan sequences that inhibit the calibration target sequences (Target Mode OFF), or in case of near failure condition of the scan system the mirror can be commanded to nadir (Scan off). Patch temperature may be controlled at 124K or at 112K. At the low temperature control selection it is anticipated that the patch will reach some stable temperature depending on the operating duty cycle that adds heat input to the patch through the long wave detector bias current. The power mode of the Filter/Chopper motor is selectable, with either condition capable of satisfactory system performance. The high power mode was intended to be used if failure of the drive system appears imminent. The added power would overcome an increase in bearing friction. It has been found that the high power mode changes the magnetic characteristics of the motor and may be used to improve motor damping with a consequent reduction of gear induced jitter noise and providing slightly improved performance at a cost of the added power demand.

Interfaces to the spacecraft include the use of separate spacecraft 400 KHz clock inputs (primary and redundant), the time code strobe and the time code signal. The internal operation of the HIRS signal and data processing are synchronized to the 400 KHz clock at any time that the electronics is on. Internal clock sources (normally externally synchronized) are automatically enabled and used in the event that the filter/chopper system or scan system is operated independently or if there is a failure of both 400 KHz clock inputs.

2.1.1 Digital Data Output

The HIRS output is a serial stream of Bi-phase digital signals available at four High Data Rate Sybsystem (HDRSS) outputs; HDRSS A and B, a spare, and at a test connector output. The signals come from separate line drives and have an amplitude of zero to +5.6 volts from a source impedance of less than 600 ohms. The data stream has a fixed format consisting of sync recognition words, telemetry, channel data, and housekeeping data. Parity bits are provided as the last bit in each eighteen bit word. A data block has a total of twenty words with a fixed format for the forty-two scan elements where atmospheric input is monitored. The format changes during the four scan

TABLE 2.1-1

ANALOG TELEMETRY

Analog TM Channel No.	Function Nomenclature
1. *	Scan Mirror Temperature
2. *	Pri. Tel. Mirror Temperature
3. *	Sec. Tel. Mirror Temperature
4.	F/C Housing Temp. 1
5.	F/C Housing Temp. 2
6.	F/C Housing Temp. 3
7.	F/C Housing Temp. 4
8. *	F.C Motor Temp.
9.	Radiant Cone Temp.
10. *	Rad. Cooler Hsg. Temp.
11. *	Baseplate Temp.
12. *	Electronics Temp.
13.	Patch Temp.
14.	Patch Power
15.	Cooler Cover Position
16.	+15 VDC Electronics
17.	-15 VDC Electronics
18.	+10 VDC Logic
19.	+5 VDC Logic
20. *	-24.5 VDC TLM
21. *	Scan Motor Temp.
22.	F/C Motor Current
23.	Scan Motor Current

* Full time telemetry

TABLE 2.1-2

HIRS COMMANDS

Electronics Power ON
Electronics Power OFF
Filter/Chopper Motor ON
Filter/Chopper Motor OFF
Scan Motor ON
Scan Motor OFF
Filter/Chopper Motor Mode High
Filter/Chopper Motor Mode Normal
Cooler Cover Store
Cooler Cover Deploy
Cooler Cone Heater ON
Cooler Cone Heater OFF
Calibrate Enable
Calibrate Inhibit
Cooler Cover Motor ON
Cooler Cover Motor OFF
Patch Temp. High
Patch Temp. Low
Filter/Chopper Heat ON
Filter/Chopper Heat OFF
Scan Mode ON
Scan Mode OFF

elements of mirror retrace, allowing insertion of electronic calibration signals, time code, and temperature measurements of the patch and internal calibration targets.

2.1.1.1 Main Sensor Data

The main sensor data is summarized as follows:

1. Bit rate clock is 3,389.83 Hz.

2. Data is organized in 18 bit words. See Figure 2.1-3a for typical data block.

   a. 12 bits of active spectral data (absolute value straight binary)

   b. Data sign bit

   c. Last bit of the word for odd parity bit insertion

   d. 4 bits word separation (all zeros)

3. Words are grouped in a block of 20 per scan element, a time period of 106.2 mS.

   a. 1 scan element (or data block) sync word

   b. 1 time code and encoder position word

      (1) 8 bits for encoder position
      (2) 4 bit time code (units seconds)
      (3) 4 bit calibrate level number (0 thru 15)

   c. 1 status word (mode, command and element number)

   d. 17 spectral data words

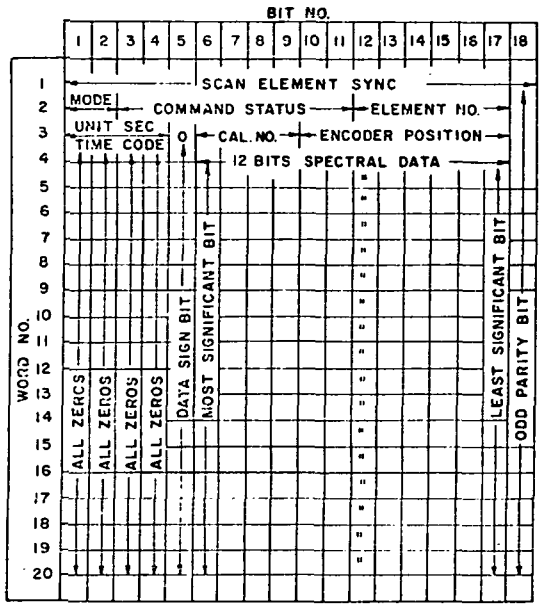
4. There are 42 active data blocks (1 for each scan element).

5. There are 4 secondary data blocks (during the four element intervals of scan mirror retrace).

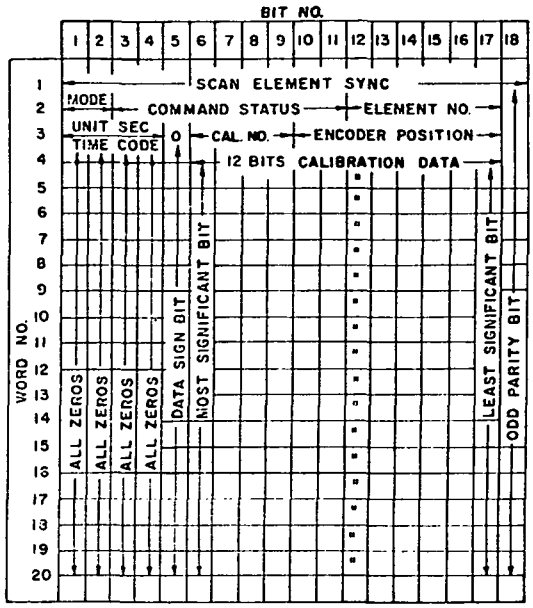
   a. Electronics calibration (34 words)

   b. TM calibration (29 words)

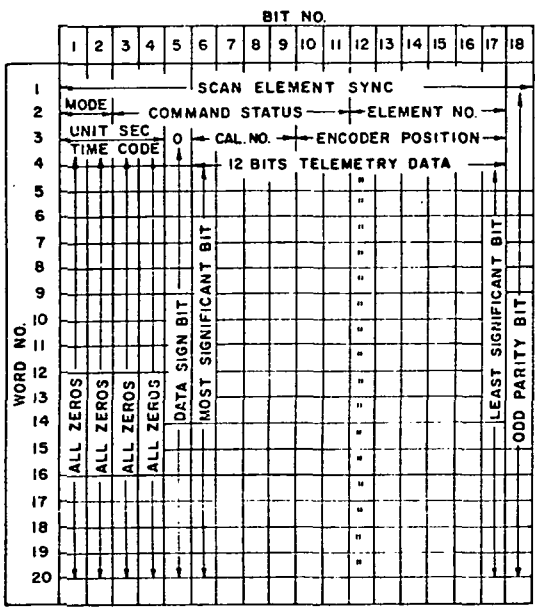
   c. Element sync (4 words)



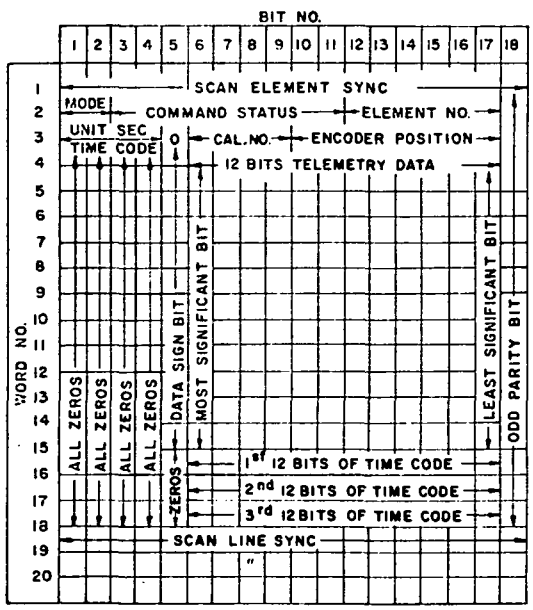
a. Scan Element 1-42



b. Scan Element 43-44



c. Scan Element 45



d. Scan Element 46

FIGURE 2.1-3 TYPICAL DATA BLOCKS

d. Time code (units-seconds) and encoder position (4 words)

e. Status word (4 words)

f. Time code complete (36 bits) (3 words)

g. Line sync (2 words)

Figures 2.1-3b through 2.1-3d give the data block format for scan lines 43 through 46.

2.1.1.2 Main Data Output

The main data outputs are listed in Section 2.1.1.1 with the following coding information applying:

The scan element sync is 17 bits plus a parity bit as follows:

1 1 1 1 1 0 0 1 1 0 1 0 1 0 0 0 0 0

The 2 bit mode status code indicates whether we are scanning the 300K target, the 270K target, space, or Earth. The scan line counter is reset to zero at the 300K target and the mode code is 1-1. For scan line binary "1" the instrument is looking at the 270K target and the mode code is 1-0. For the space look, (scan line binary "2") the code is 0-1. The earth scan includes scan lines indicated by the counter as "3" through "22" and the code is 0-0.

There are nine bits allotted for command status. Neither the Filter/Chopper Motor ON-OFF nor the Electronics ON-OFF commands will be "reported." The other nine commands will be reported in the order and with the binary indicator shown below:

Slot	Command	Binary Indicator
1.	Scan Motor ON	1
	Scan Motor OFF	0
2.	Filter/Chopper Motor Mode High	0
	Filter/Chopper Motor Mode Normal	1
3.	Cooler Cone Heater ON	1
	Cooler Cone Heater OFF	0
4.	Calibrate Enable	0
	Calibrate Inhibit	1

5.	Cooler Cover Store	1
	Cooler Cover Deploy	0
6.	Cooler Cover Motor ON	1
	Cooler Cover Motor OFF	0
7.	Patch Temperature High	1
	Patch Temperature Low	0
8.	Filter Wheel Heater ON	1
	Filter Wheel Heater OFF	0
9.	Scan Mode OFF	1
	Scan Mode ON	0

The first scan element (during earth look) corresponds to the start of scan position at -36.9 degrees with respect to nadir. The scan element number will be binary zero for that position (0 - 0 - 0 - 0 - 0 - 0). The forty-second and last earth scan element at +36.9 degrees with respect to nadir is encoded binary 41 (1 - 0 - 1 - 0 - 0 - 1). The highest scan element count , binary 45, (1 - 0 - 1 - 1 - 0 - 1) occurs at the end of retrace.

The scan encoder is encoded in complementary binary. When complemented it is identical to the scan element number during the earth scan. During retrace the positional information may be repetitive or it may be meaningless. At the 300K target position the encoder will read (in complemented binary) digital 84, at the 270K target, digital 134, at the space look, digital 184, at nadir, digital 20, and at start of scan, digital 0. For additional description of Protoflight Encoder, refer to Section 5.3.

The main data channel telemetry will be inserted as follows:

	T M Point	Element No.	Word No's.
1.	270K Target Temp #1	45	4,5,6
2.	270K Target Temp. #2	45	7,8,9
3.	270K Target Temp. #3	45	10,11,12
4.	270K Target Temp. #4	45	13,14,15
5.	Cooler Patch Temperature	45	16,17,18,19,20
6.	300K Target Temp. #1	46	4,5,6
7.	300K Target Temp. #2	46	7,8,9
8.	300K Target Temp. #3	46	10,11,12
9.	300K Target Temp. #4	46	13,14,15

The time code will appear as words, 16, 17, and 18 in element 46. Each word will consist of 5 zeros, 12 bits of time code, and a parity bit.

The scan line sync occurs in the nineteenth and twentieth words of element number 46. It is a 36 bit code that satisfies word and parity requirements and reads as follows:

Word 19	0	1	1	1	0	1	0	1	1	1	1	1	0	1	0	1	1	1	-	1
Word 20	0	0	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	-	0

The last 29 bits of the two words is the 29 bit sync code word suggested as optimum by GSFC Document X-560-63-2.

The order in which the IR and Visible Channel are read out is as follows:

SEB #1 through #42 Word No.	Channel No.	Integration Time (Cycles)
4	1	7
5	2	4
6	15	3
7	3	5
8	13	3
9	4	5
10	7	4
11	12	3
12	16	1
13	8	2
14	6	4
15	11	3
16	5	3
17	9	2
18	14	3
19	10	3
20	17	1

The Calibration Voltage Levels are contained in SEB 43 and 44, Words 4 through 20. SEB 43 has the positive cal level and SEB 44 has the negative cal level.

During any given scan line, one cal level will be presented. The cal level will change (0 through 15 levels) on each scan line.

For any given cal level, the counts will be different in each channel location due to the different integration times of each channel.

During the electronics calibration SEB's, the calibration voltage signal is inserted after the first preamplifier in the IR channels.

2.1.2 Power and Control

The power for HIRS operation comes from the spacecraft -24.5 volt regulated buss in four separate paths.

Full Time Telemetry
Electronics Power
Filter Chopper Motor Power
Scan Motor Power

The full time telemetry power circuit is applied to those temperature sensors noted in Table 2.1-1 whenever the S/C power buss is turned on external to the HIRS. The other sources are controlled by the first three sets of commands of Table 2.1-2. These three power sources are fused in the spacecraft power supply and are relay controlled at entry into the HIRS. There is no connection between supplies within the instrument. Power and return leads are wired to separate connector terminals and carried to the power source and to a unipoint ground at the S/C power supply. Figure 2.1-4 shows the power distribution within the HIRS instrument. It may be noted that the -24.5 volt telemetry is a measure of the full time telemetry. The F/C Power provides voltage for the door mechanism, the cone and housing heaters, and the filter wheel housing heaters and control system.

The Electronics Power supplies regulated voltages for all of the timing, data processing, and signal generating circuits. Without Electronics Power on, the scan system will not be controlled and will run in a separate mode (Launch Mode), not the normal scan pattern. An estimate of power demand for the different operating modes is given in Table 2.1-3.

The Scan Motor Power is used exclusively for mirror scan system drive. The source is not used for the scan signal generation or encoder position detection circuitry. The scan motor current telemetry is not dependent on the Electronics power source, and is available during launch and standby operation.

2.1.3 Electronic System

Details of each electronic system are given in following sections, but are shown in a simplified block diagram in Figure 2.1-5. From this diagram we may see the circuit and system definitions that are mentioned later. The HIRS electronics has several basic unique features. Among these are the nearly complete use of complementary symmetry metal oxide semiconductors (CMOS), permitting a compact and low power

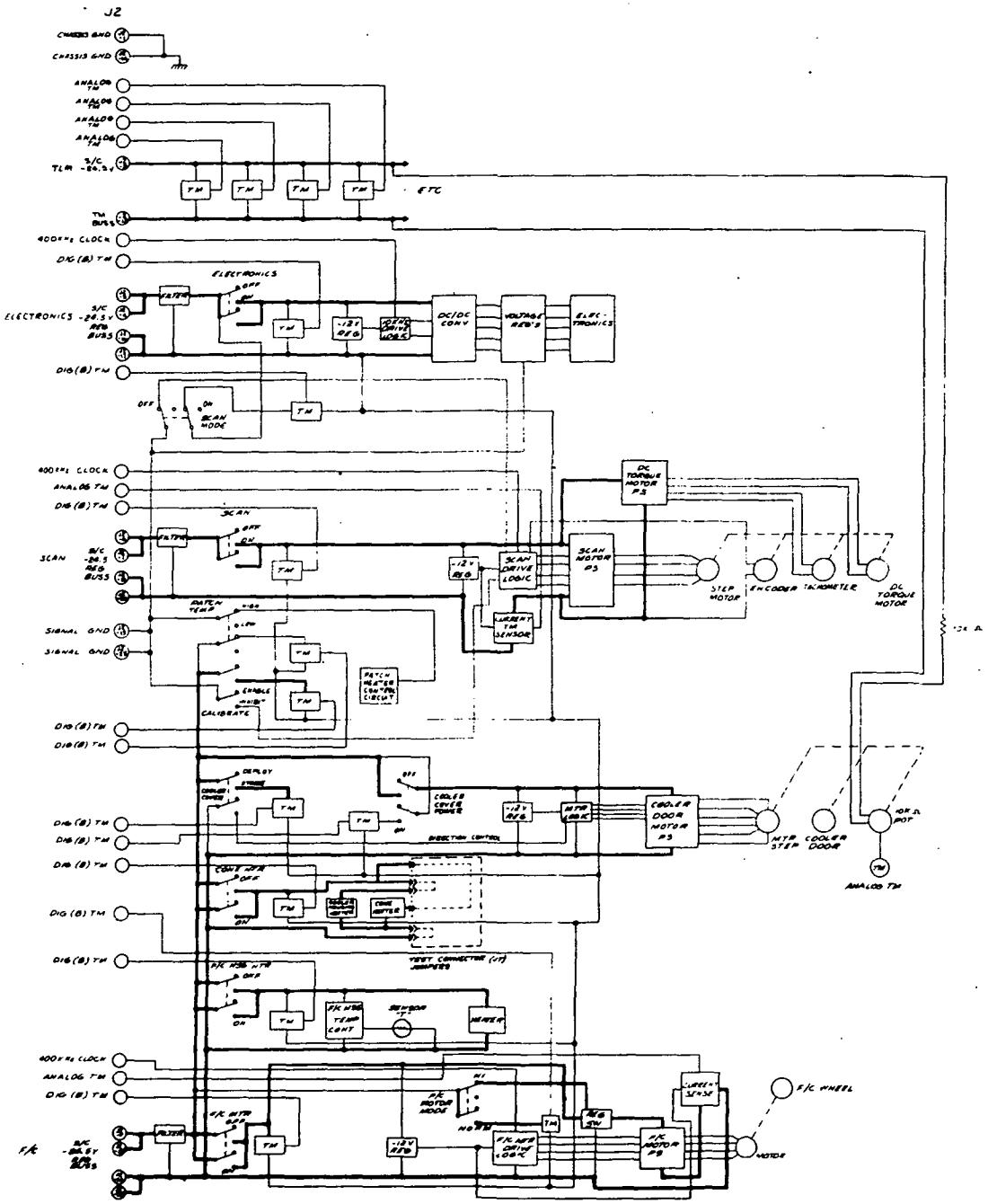


FIGURE 2.1-4 HIRS POWER DISTRIBUTION

Table 2.1-3

POWER USAGE

Operating Modes	Source	Power	(watts)
Min. Sat.	None	0	
Standby	Filter Wheel Htr.	1.23	7.88
	Electronics	6.65	
Launch	F/C Motor	6.32	12.94
	Scan Motor	6.62	
Preconditioning	F/C Motor	6.32	35.9
	Scan Motor	8.94	
	Electronics	6.65	
	Cooler Cone Htr.	2.77	
	Filter Wheel Htr.	1.23	
	Cooler Hsg. Htr.	10.0	
Operation	F/C Motor	6.32	23.1
	Scan Motor	8.94	
	Electronics	6.65	
	Filter Wheel Htr.	1.23	
All	Full Time Telemetry	.14 *	

* Add to above for total system power.

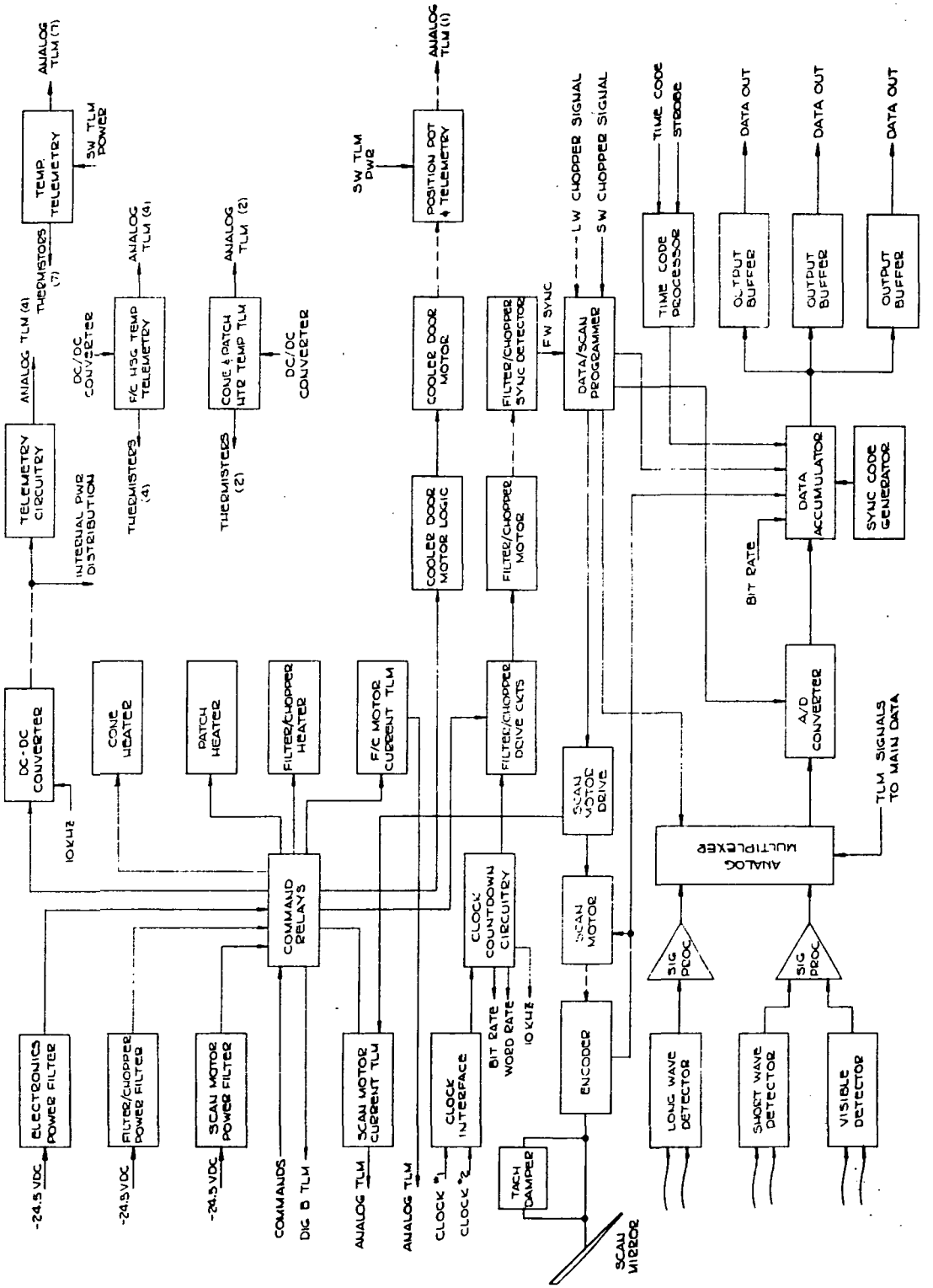


FIGURE 2.1-5 HIRS BLOCK DIAGRAM

configuration. On the fifty three electronic modules we have over 3000 digital elements, using multiple function packages and new design techniques to keep the total electronics power below seven watts. Nearly all electronic components are mounted on plug-in circuit boards, with heat sinking where necessary and all parts conformally coated. The use of low power logic with high noise immunity permitted the use of small wire in interconnecting cables and close packaging of circuit boards and modules. It is interesting to note that the system was literally free of signal coupling problems or noise in the cable assemblies. We strongly recommend the use of this type of circuitry in applications where it may be used.

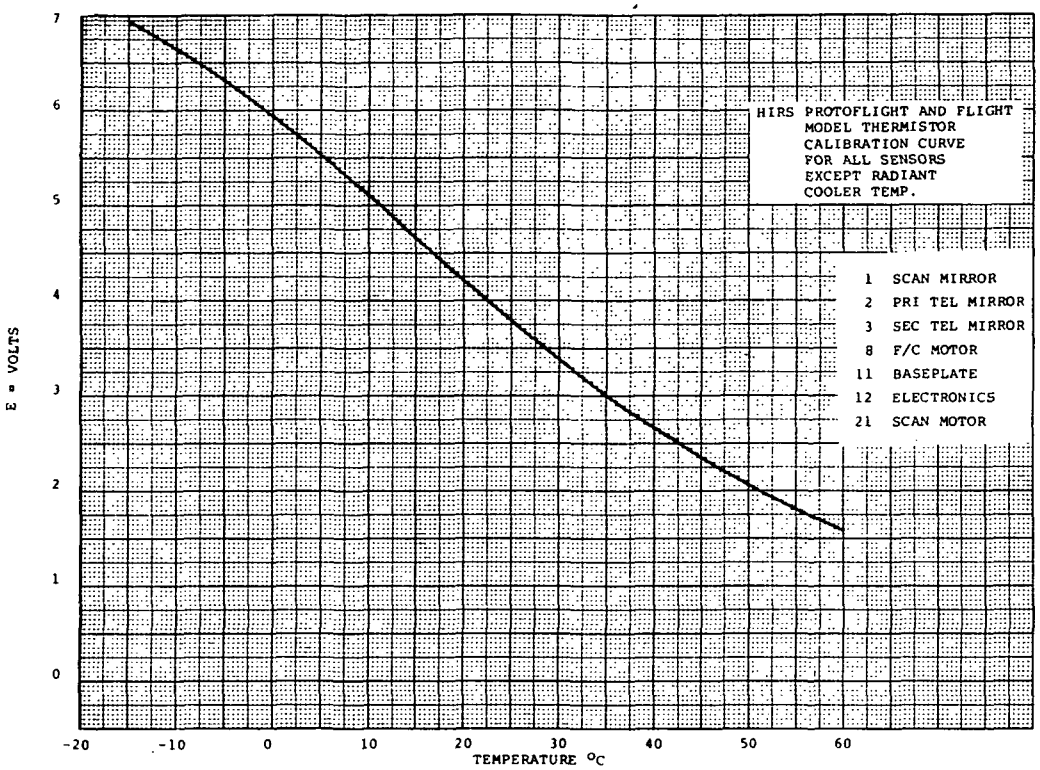
2.1.4 Telemetry Characteristics

Housekeeping data from the HIRS instrument is outputted in both analog and digital formats. The digital output is strictly for command relay state monitoring. The analog data consists of highly accurate temperature sensors (platinum resistance devices) for the critical functions of internal calibration targets, patch, and filter wheel housing, and thermistor devices with nominally linear characteristics for sensing variation in scan mirror, telescope mirrors and housing temperatures. Other analog telemetry is self-generated, such as the scan and filter chopper motor current sensors, and some are direct voltage divider sensors that detect changes in input or derived voltage sources. These telemetry points are measured once every sixteen seconds. The range of the telemetry signals is 0 to -6.375 volts, with the spacecraft telemetry circuit having 8 bit encoding capability, resulting in a resolution of 0.025 volts. In order to provide a sufficient accuracy for system definition and calibration the patch sensor output is also transmitted to the HDRSS encoder where it has twelve bit resolution, and the filter wheel housing temperature range is expanded to permit detection of temperature changes of $.08^{o}$. Table 2.1-4 lists the telemetry and the information of most interest. Telemetry curves for the temperature conversions are given in Figure 2.1-6 through 2.1-8. These curves are not used operationally (computer data reduction of algorithms are used exclusively). They are included for information only. The algorithms given in Table 2.1-5 are used for computer data reduction and provide more accuracy than is possible to show on the curves. In each case the algorithm makes use of calibration data from a given sensor and the related protoflight circuit.

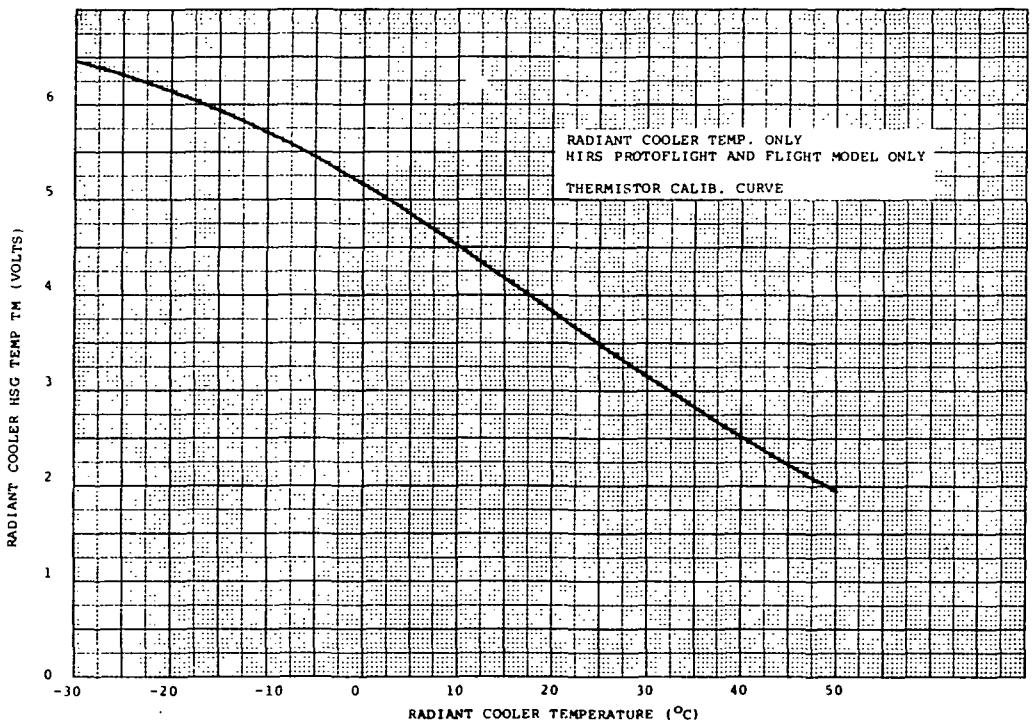
TABLE 2.1-4

ANALOG TELEMETRY

Function	Typical Range	Typical TM Volts	Slope	GRAN (.025V)
Scan Mirror Temp	8 to 12°C	5.10V	-.10 V/°	.25°
Primary Mirror Temp	12 to 18°C	4.20V	-.08 V/°	.31°
Secondary Mirror Temp	6 to 14°C	5.10V	-.09 V/°	.28°
F/C Housing Temp #1	29.6 to 30.6C	3.00	+.28 V/°	.09°
F/C Housing Temp #2	29.6 to 30.6C	2.95	+.28	.09°
F/C Housing Temp #3	29.6 to 30.6C	3.05	+.28	.09°
F/C Housing Temp #4	29.6 to 30.6C	3.05V	+.28	.09°
F/C Motor Temp	27 to 30C	3.50V	-.08V/o	.31°
Radiant Cone Temp	165 to 170K	1.71V	+.04 V/°	.63°
Cooler Housing Temp	0 to 10C	4.85V	-.065V/°	.38°
Baseplate Temp	15 to 20C	4.42V	-.09V/°	.28°
Electronics Temp	15 to 20C	4.42V	-.09 V/°	.28°
Patch Temp	118 to 124C	0.88V	+.036 V/o	.69°
Patch Power	0 to 5 mw	1.47V	.3V/mw	.08 mw
Cooler Cover Position	Open	1.10V	.04V/°	.63°
+15V DC Electronics	+14.78V	2.14V	.14V/V	.18V
-15V DC Electronics	-14.93V	4.97V	.34V/V	.07V
+10V DC Logic	+10.07V	1.63V	.16V/V	.16V
+5V DC Logic	+5.26V	2.40V	.46V/V	.05V
-24.5V DC Logic	-24.5V	5.48V	.18V/V	.14V
Scan Motor Temp	16 to 20C	4.40V	-.09V/°	.28°
F/C Motor Current	320 ma NORM	1.62V	5.0V/a	5 ma
Scan Motor Current	650 ma	1.60	2.5V/a	10 ma

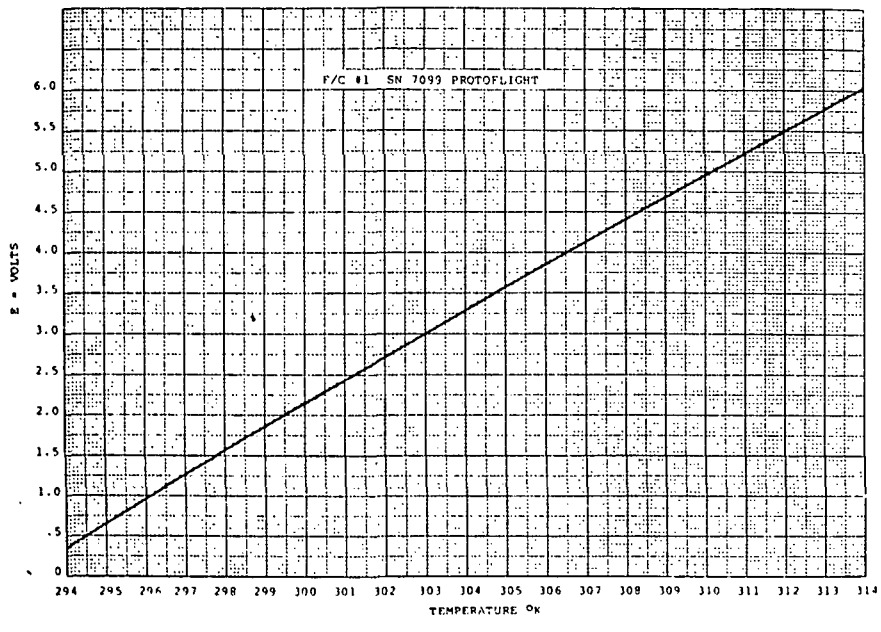


a. All Sensors Except Cooler Housing

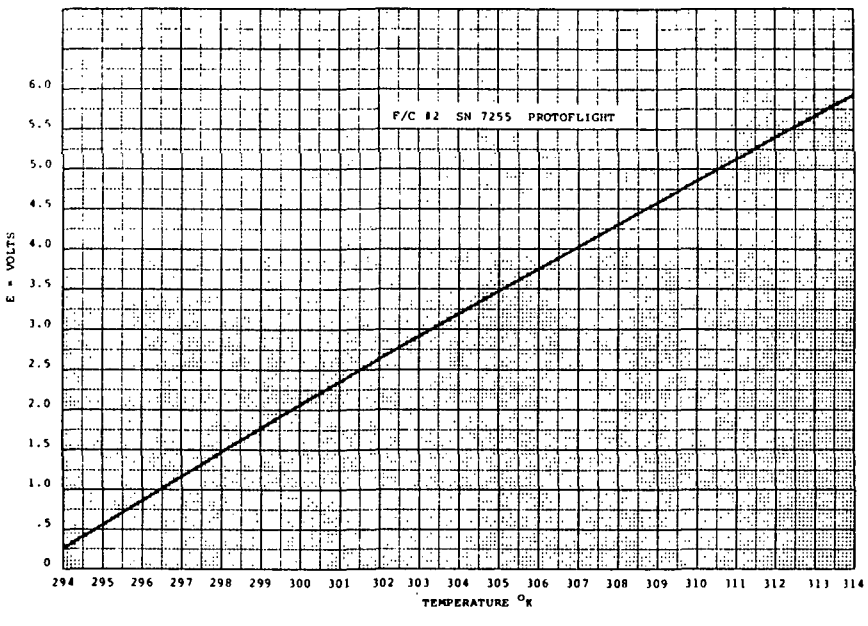


b. Cooler Housing

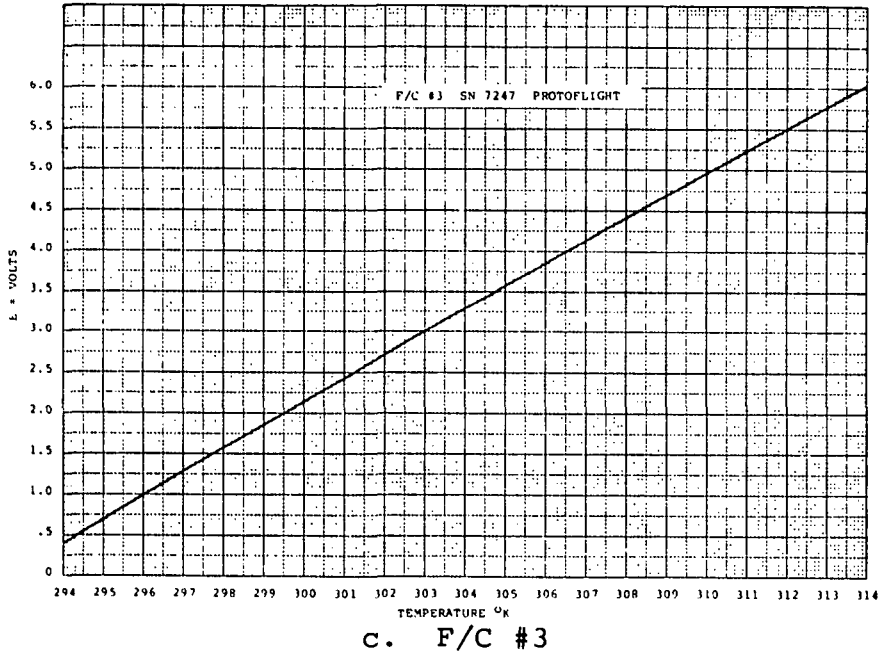
FIGURE 2.1-6 THERMISTOR TEMPERATURE SENSORS



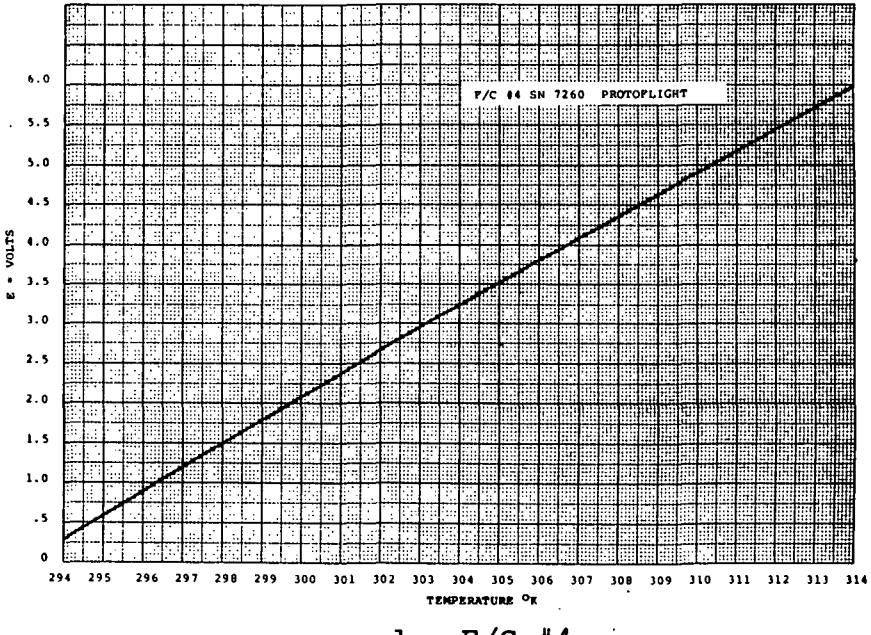
a. F/C #1



b. F/C #2

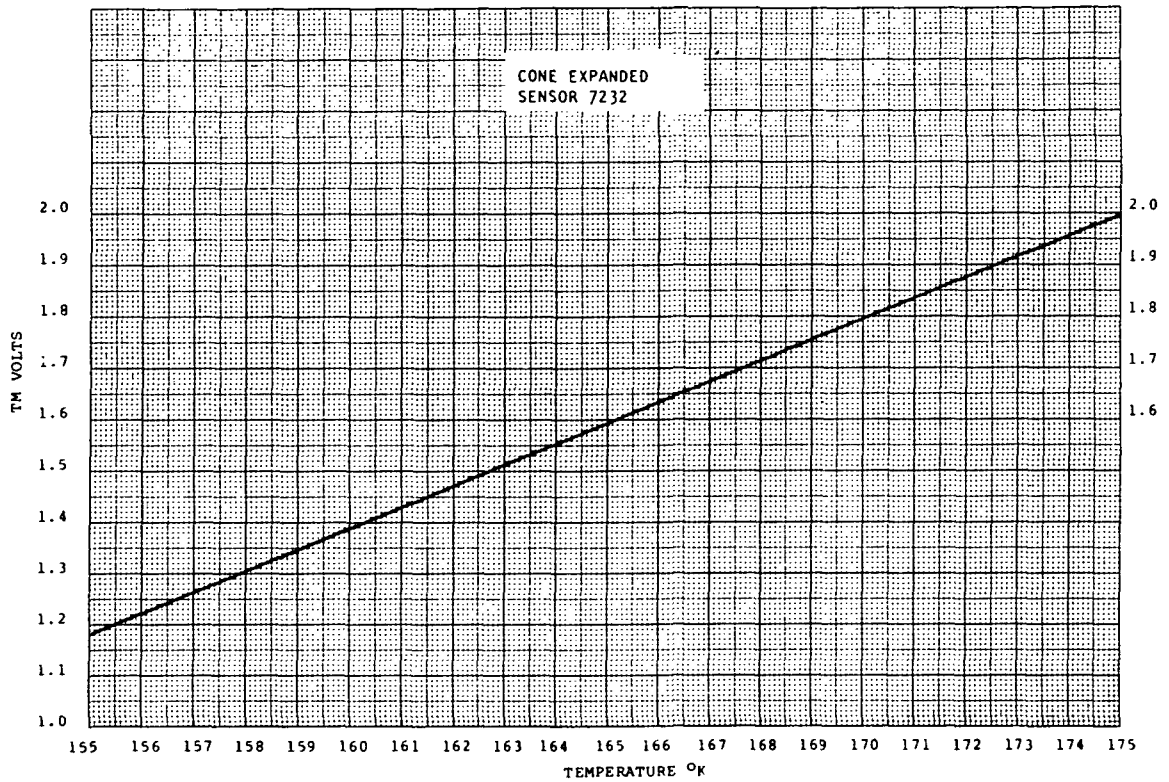


c. F/C #3

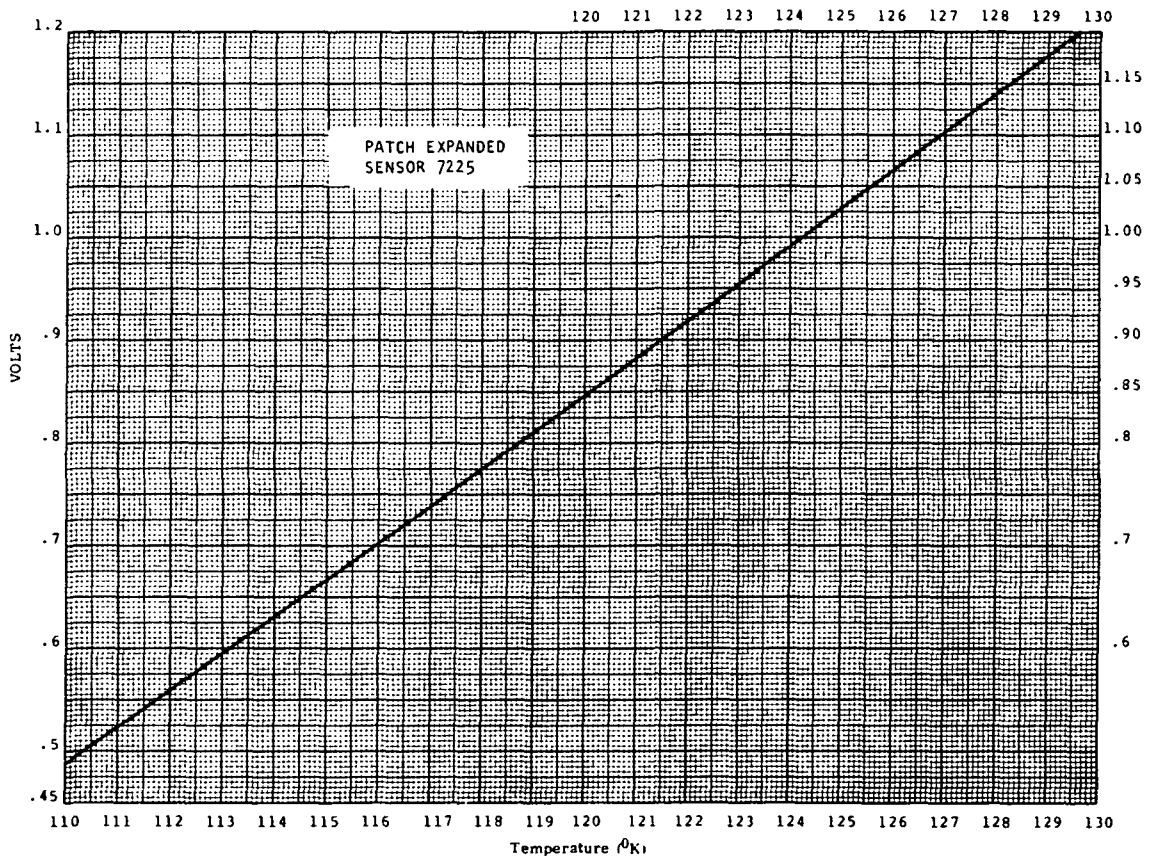


d. F/C #4

FIGURE 2.1-7 FILTER WHEEL HOUSING TEMPERATURE



a. Cone Temperature, Expanded



b. Patch Temperature, Expanded

FIGURE 2.1-8 CONE AND PATCH TEMPERATURES

Table 2.1-5 Telemetry Data Conversion

FUNCTION	ALGORITHM
Patch Power	$P\mu w = 1.16\ (VTM)^2 \times 1000$
Cone Cover Deployed Voltage	$VTM = -1.2 \pm 0.5V$
Cone Cover Stored Voltage	$VTM = -5.34 \pm 0.5V$
+15 VDC TM +10 VDC TM +5 VDC TM	$V_X = K \left\{(R1) \left[(4.5158)\ 10^{-4}\ (VTM) - 1.503\ (10^{-4})\ V_{-15} \right] + VTM \right\}$ where X, R_1, K:

X	R_1	K
+15	13.3×10^3	1.0
+10	7.87×10^3	0.99
+5	6.65×10^3	1.0

-15 VDC TM	$V_{-15} = 2.991\ (VTM)$
-24.5 VDC TM	$V_{-24.5} = 4.48\ (VTM)$
F/C Motor Current	$I = 0.198\ (VTM)$
Scan Motor Current	$I = 0.40486\ (VTM)$

Scan Mirror Temp
Pri Telescope Temp
Sec Telescope Temp
F/C Motor Temp
Baseplate Temp
Electronics Temp
Scan Motor Temp

$$E_o = VTM$$

$$VCC = V_{-24.5}$$

(1) $$R_T = (3.48 \times 10^4 \times E_o) / (VCC - 2.955\ E_o)$$

(2) $$T_c = \left\{ 1 / \left[(1.02674 \times 10^{-3}) + (2.39508 \times 10^{-4}) \times (\text{LOG}_e\ R_T) + 1.55404 \times 10^{-7} \times (\text{LOG}_e\ R_T)^3 \right] - 273.15 \right\}$$

Cooler Housing Temp

(1) $R_T = (3.48 \times 10^4 \times E_o)/(VCC - 3.540\ E_o)$

(2) $T_C = \{1/\ [1.02674 \times 10^{-3} + (2.39508 \times 10^{-4}) \times (LOG_e\ R_T) + 1.55404 \times 10^{-7} \times (LOG_e\ R_T)^3]\ -273.15\}$

PFM conversions of Volts to Kelvin ($T_K = K_2 V^2 + K_1 V + K_O$)

ANALOG TM CHANNEL	K_2	K_1	K_0
F/C HSG #1	3.3385×10^{-2}	-3.3172	293.01
F/C HSG #2	3.3312×10^{-2}	- 3.3158	293.09
F/C HSG #3	3.255×10^{-2}	- 3.3148	292.84
F/C HSG #4	3.3326×10^{-2}	-3.3109	292.82
Patch (143K to 323K)	1.7787	-24.087	98.61
Patch (103K to 143K)	1.6727	-24.585	97.98
Cone (183K to 323K)	2.4163	-16.320	133.21
Cone (153K to 183K)	2.2414	-17.390	131.56

2.2 System Analysis

2.2.1 General

A description of the system characteristics is reviewed here to provide the background characteristics of the optics, filters and detectors that make up the sensing function of the HIRS. Development of the system performance includes the effects of amplifier characteristics and extraneous noise influences. From this we are able to compare the theoretical and measured system performance and establish guidelines for data review and analysis.

The individual subsystems are described in detail in following sections and may be referenced for greater understanding of the system design.

2.2.2 System NEΔN Calculations

The sensitivity of the HIRS system can be measured in Noise Equivalent Change in Radiance (NEΔN) which is the change in scene radiance to produce an instrument signal output equal to the instrument noise output. This is measured in ergs/ (sec. $\bullet$ cm^2 $\bullet$ st $\bullet$ cm^{-1}). The NEΔN can be calculated by starting with the equation for S/N,

$$S/N = \frac{A_o \bullet \Omega_o \bullet T_o \bullet R_\nu \bullet N_\nu \bullet \Delta_\nu}{\alpha_T \bullet V_n \bullet \sqrt{\Delta_f}}$$

Where $\alpha_T = \alpha_1 \bullet \alpha_2 \bullet \alpha_3$

α_1 = increase in noise due to electronics and pickup

α_2 = increase in noise bandwidth compared to signal bandwidth

α_3 = decrease in signal due to modulation and demodulation

A_o = area of entrance aperture

Ω_o = field of view (solid angle)

T_o = total optical transmission including obscurations

R_ν = detector responsivity

N_ν = scene radiance

Δ_ν = spectral bandwidth

V_n = detector noise

Δ_f = electrical bandwidth

The electrical integrator acts as an ideal, low-pass filter. Its normalized frequency response is $\sin \pi t_d f / \pi t_d f$, where t_d is the integration time and f is the electrical frequency. For white noise, the equivalent output bandwidth is given by

$$\Delta f = \int_o^\infty (\sin \pi t_d / \pi t_d f)^2 \, df = \frac{1}{2 t_d}$$

To find $NE\Delta N$ the S/N is set equal to one, and the equation is solved for N_ν.

$$NE\Delta N = \frac{\alpha_T \bullet V_n}{A_o \bullet \Omega_o \bullet T_o \bullet \Delta_\nu \bullet R_\nu \bullet \sqrt{2 t_d}}$$

Next the appropriate values are determined for the above equation. The optic entrance aperture area is determined by the 5.9 inch primary telescope,

$$A_o = \frac{\pi}{4} (5.9 \times 2.54)^2$$

$$= 176.4 \text{ cm}^2$$

The effective field of view was determined during optics test as,

LW $\Omega_o = 3.28 \times 10^{-4}$ st. (EFOV = 1.17^o)

SW $\Omega_o = 3.68 \times 10^{-4}$ st. (EFOV = 1.24^o)

VIS $\Omega_o = 3.92 \times 10^{-4}$ st. (EFOV = 1.28^o)

The values for V_n for the LW were taken from the Honeywell data. The SW detector noise was measured with the detector in the HIRS unit which gave 4×10^{-5} amp background current. The visible detector had 5×10^{-7} amp dark current at its manufacturer.

LW $V_n = 7.5 \times 10^{-7}$ volts/ $\sqrt{\text{Hz}}$

SW $V_n = 3.6 \times 10^{-12}$ amps/ $\sqrt{\text{Hz}}$

VIS $V_n = 4.0 \times 10^{-13}$ amps/ $\sqrt{\text{Hz}}$

The values for the noise due to electronics and pickup (α_1) is derived using the results of Section 8.3. In the LW the input noise is .75 nV/ $\sqrt{Hz}$ while the output is 1.57 nV $\sqrt{Hz}$ giving $\alpha_1 = 2.1$. For the SW the input is 3.6×10^{-12} amps/ $\sqrt{Hz}$ with the output of 6.2×10^{-12} amps/ $\sqrt{Hz}$ giving $\alpha_1 = 1.7$. For the visible channel no data exists as to the increase in noise due to electronics, it is expected that the major noise source will be quantization noise. Here the degradition will be assumed one, $\alpha_1 = 1$.

The degradation factors α_2 and α_3 occurred because the incoming signal is chopped producing a peak-to-peak signal instead of a steady signal. The fact that the noise is over a 2 Δf bandwidth increases the NEΔN by $\sqrt{2}$ and the modulation-demodulation produces a larger NEΔN by a factor $\pi^2/4$ (IF). Where IF is an improvement factor depending on the signal waveform. It is given by,

$$IF = m \sin \frac{\pi}{2m}$$

Where m is the ratio of chopper tooth width to field stop width.

LW m = .550/.204 = 2.70 (for EFOV = 1.17°).
SW m = .284/.217 = 1.31 (for EFOV = 1.24°).
VIS m = .284/.224 = 1.27 (for EFOV = 1.28°).

Substituting the m values to determine IF, α_3 and multiplying by α_2 and α_1, the total degradation factor (α_T) is determined.

LW $\alpha_T = 4.94$

SW $\alpha_T = 4.86$

VIS $\alpha_T = 2.06$

The values for the optical transmission T_o is given in Table 2.2-1. Many of the values were made from witness samples to simulate the actual optical element. The filter transmissions are taken for the filters used in the Protoflight Unit. The integration time (t_d), filter center wavelength and $\Delta\nu$, and detector responsivity is given in Table 2.2-2. The LW detector responsivities are for 11.4 millampere bias at 124°K. The expected NEΔN values and observed NEΔN values are also given in Table 2.2-2. The LW channels agree very well, but there is a large amount of disagreement in the SW channels. This is probably due to the effects of jitter in the SW filter-chopper wheel and emissivity variations on some of the SW filters. The calculated value for the VIS channel is much lower than that observed because of the quantization noise of the A/D converter.

Transmission Prototype S/N 2 CHANNEL	Primary & Secondary Mirror & Scan Mirror	LW Folding Mirror	LW Window	LW Lens -1 & Lens -2	LW Aplanat	SW Lens -1	Vis Lens -1	Vis Lens -2	IR-Vis Beamsplitter	SW Folding Mirror	SW Lens -2	SW Window	
	R	R	T	T	T								
1	$.98^3$	.95	.81	$.77^2$	.78								
2	$.98^3$	.95	.81	$.79^2$	.81								
3	$.97^3$	.95	.81	$.80^2$	.84								
4	$.97^3$	.96	.80	$.79^2$	.86								
5	$.97^3$	.96	.79	$.79^2$	.88								
6	$.97^3$	.96	.78	$.78^2$	.90								
7	$.97^3$	.96	.77	$.78^2$	.92								
8	$.97^3$	.96	.87	$.78^2$	.94								
9	$.97^3$	.96	.80	$.78^2$	.94								
10	$.97^3$	.95	.85	$.85^2$	.94								
	R					T			R	R	T	T	
11	$.97^3$					.81			.95	.96	.95	.87	
12	$.97^3$					.81			.95	.96	.95	.85	
13	$.97^3$					.82			.95	.96	.95	.82	
14	$.97^3$					.87			.95	.96	.95	.83	
15	$.97^3$					.88			.95	.95	.93	.87	
16	$.96^3$					.98			.94	.94	.93	.92	
	R					T	T	T					
17	$.85^3$					.89	.97	.98					

TABLE 2.2-1

HIRS PROTOTYPE OPTIC PARAMETERS

Transmission Prototype S/N 2 (Continued) CHANNEL	SW Aplanat	Vis. Folding Mirror	IR Beamsplitter Lot-1	Total Optical Transmission (not filters)	Filter Bandwidth eff ν (cm^{-1}) Avg. of 3 sets (from Annable memo)	Filter Transmission	Loss due to Obscuration	Total τ
			T					
1			.62	.20	N/A	.37	.687	.074
2			.63	.22		.60	.687	.13
3			.62	.23		.65	.687	.14
4			.61	.22		.69	.687	.15
5			.60	.22		.62	.687	.13
6			.65	.24		.64	.687	.15
7			.72	.26		.58	.687	.15
8			.81	.36		.59	.687	.21
9			.84	.33		.70	.687	.23
10			.83	.41		.68	.687	.27
	T		R					
11	.96		.96	.51		.54	.687	.27
12	.96		.96	.50		.59	.687	.30
13	.96		.95	.48		.53	.687	.25
14	.96		.95	.52		.55	.687	.28
15	.96		.95	.53		.68	.687	.36
16	.95		.88	.55		.88	.687	.48
		R	R					
17		.82	.25	.097	N/A	.87	.687	.085

TABLE 2.2-1
(Continued)

TABLE 2.2-2

NEΔN CALCULATIONS

Channel	Wavelength $\nu(cm^{-1})$	Half Bandwidth $\Delta\nu$ (cm^{-1})	R_ν (V/W)	(x 10^{-3} sec)	Calculated NEΔN (ergs...)	Observed NEΔN (ergs...)
1	669.1	4.2	4.28	7.77	5.7	6.4
2	678.8	13.6	5.42	3.33	1.2	1.1
3	690.1	12.3	5.84	5.55	.89	.79
4	701.6	16.1	6.84	5.55	.50	.46
5	716.5	18.1	7.70	3.33	.56	.68
6	732.3	17.9	8.55	4.44	.41	.45
7	749.1	19.3	8.84	4.44	.39	.43
8	899.6	31.7	8.27	2.22	.25	.30
9	1228.2	57.1	5.56	2.22	.20	.22
10	1494.9	79.4	4.42 (A/W)	3.33	.12	.15
11	2190.8	20.7	3.6	5.08	.0022	.011
12	2211.9	23.0	3.6	5.08	.0018	.0029
13	2244.2	21.6	3.6	5.08	.0023	.0049
14	2274.5	35.0	3.6	5.08	.0014	.0018
15	2357.6	23.0	3.5	5.08	.0014	.0026
16	2692.4	295.6	3.4	1.91	.00015	.0010
17	14443.0	949.4	0.3	1.91	3.7×10^{-5}	.90).04% Albedo)

3.0 MIRROR SCAN SYSTEM

3.1 General

The pointing mirror of the HIRS system is a beryllium mirror having a 6.0 inch circular aperture on a 45° plane. It is driven by a permanent magnet stepping motor having 200 poles per revolution, 1.8° per pole. The mirror stepping motor is advanced one step during earth scanning (to one of 42 adjacent step positions) coincident with each filter wheel rotation (a period of 106.2 milliseconds). During each step interval a total of seventeen spectral channels are sampled. The filter wheel rotation is controlled by a separate hysteresis synchronous motor, continuously rotating and driven from a clock controlled input. This same clock is used to derive signals for the stepper motor to insure that the step sequence takes place during an interval of filter wheel rotation when there are no filters in the optic field of view. The available time for stepping is fixed partly by this dead space interval and by the requirements for pointing accuracy and stability. The 1.8° step must occur in 45 milliseconds. For the remainder of the 106.2 milliseconds in a step period, the pointing angle should remain fixed to ±1% of a single step, approximately 1.1 arc minutes. This infers that the step and settling characteristics must be uniform and reliable.

After scanning the earth for a total of 42 positions (start of scan plus 41 steps) the mirror is retraced to the start of scan position in four scan element time intervals. The step cycle is then repeated for twenty such scans. After the twentieth scan, the mirror is "forward" slewed to each of four positions, the first three of which are radiometric calibration target positions:

1) End of Scan to Warm Target
2) Warm Target to Cold Target
3) Cold Target to Space Look
4) Space Look to Start-of-Scan.

In each of the four slews described above, the slewing takes place in four scan element times (424.8 ms). The mirror will dwell for 42 element times before slewing to the next position.

Details of these scan motions are listed in Table 3.1-1 and a plot of the scan pattern is in Figure 2.1-2.

3.2 System Description

The scan mirror control subsystem is independently commandable and is used to provide orderly pre-programmed angular

TABLE 3.1-1

MIRROR SCAN PARAMETERS

Scan Element Period	106.2 milliseconds
Step	45 milliseconds
Dwell	61.2 milliseconds
Slew Time (maximum)	424.8 milliseconds
Slew Angles, Retrace	73.8^{o}
Warm Target	77.4^{o}
Cold Target	90^{o}
Space Look	90^{o}
Start Scan	28.8^{o}
Maximum Slew Rate Average	3.74 rad/sec.
Motor Type	Permanent Magnet
	1.8^{o} per step
	28 oz inches at 100 pps
	47 oz inches at stall
	Two Phase
Mirror Inertia	.08 oz. in sec^2
Motor Bearing and Encoder Friction	.15 oz. in.
Motor Magnetic Indent Torque	1.5 oz. in.

position control for the final instrument optical element (as viewed by the infrared and visible radiometric detectors). This element is an eliptically shaped optically flat mirror which redirects radiant energy through by an angle of 90^{o} into the instrument all reflective Cassegrain-type telescope. The mirror is mounted upon the shaft of a 200 step per revolution permanent magnet stepping motor which is capable of continuous unrestricted angular rotation. This enables the optical instantaneous field of view to be incrementally positioned to any one of 200 discrete 1.8^{o} motor steps which complete a 360^{o} arc within a plane that is normal to the telescope optical input axis.

This subsystem consists of a Scan Housing Assembly (8119301G1) which contains the following principal components in addition to mounting the permanent magnet stepping motor and mirror; 1)a scan mirror shaft encoder 8117367-1; 2) a DC Torque Motor 8120481-2; 3) a brushless DC Tachometer 8120482-1; 3) a resistor assembly Phase Control 8120612; 5) two transistor assemblies - 8120588 and 8120589 and 6) three printed circuit boards; the Scan Motor Regulator 8120022, the Step/Slew Bridge Driver 8120026 and the Tach Damper Electronics 8120486. This assembly mounts to the instrument baseplate from which all electrical connections are made by means of two floating pin connectors on the baseplate. In addition to the components with the scan housing, the subsystem consists of five printed circuit boards within the main electronics unit; 1) the Clock Logic and Decoder Board 8120362, 2) the Motor Phase Control 8120358 and 3) the Step/Slew Control Logic boards numbers one through three, (8120345, 8120372 and 8120423).

3.3 Mechanical Assembly

3.3.1 General

The HIRS Mirror Scan Assembly makes use of a direct drive stepping motor as the primary drive system and whose shaft and bearing assembly provide the mechanical reference for the system components. As shown in Figure 3.3-1 the motor shaft extends through the system, with the scan mirror seated by key and set screws to one end of the shaft, wires for the mirror temperature sensor feed through a hole in the center of the shaft, and the pin encoder wheel, torque motor and tachometer all attach to the shaft inside the scan housing. In addition to the mechanical components of the scan motor and assembly the scan housing has three printed circuit boards and hard mounted resistor and transistor assemblies associated with the power drive section of the scan system.

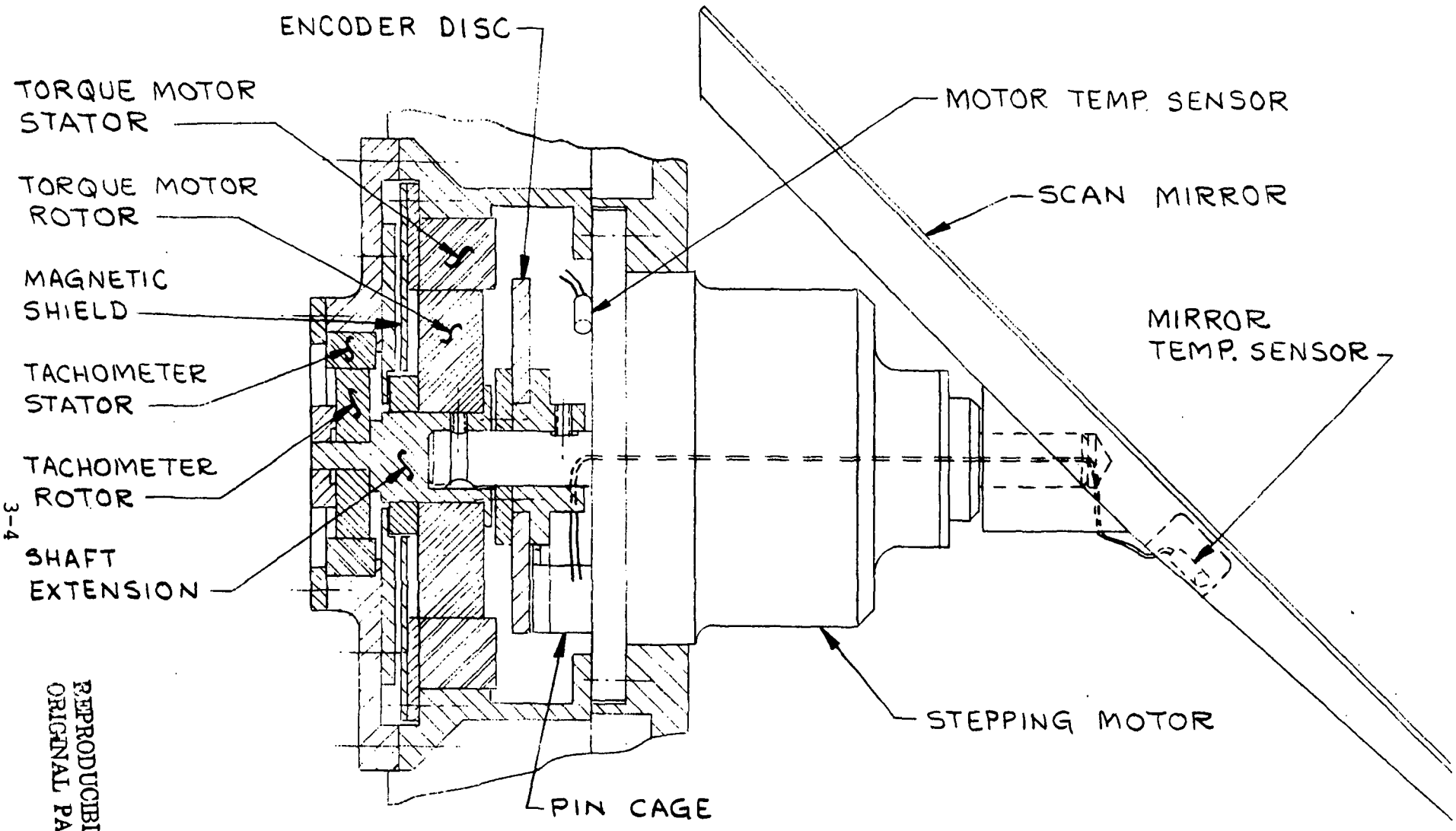


FIGURE 3.3-1 MIRROR SCAN DRIVE ASSEMBLY

The drive inertia of the scan system is made up of the following:

Scan Mirror	.077 oz-in-sec^2
Rotor	.003
Shaft	.001
Encoder Disc	.0022
Tachometer	.0024
Torque Motor	.0042
Total	.0898 oz in sec^2

3.3.2 Scan Mirror

The scan mirror is a beryllium single piece mirror machined for direct mounting to the motor shaft. Waffle structure on the reverse side provide structural rigidity and stability. The front surface is optically polished to a mirror surface specified to meet the system requirements. A power limit of 10 fringes at $\lambda = .546 \times 10^{-4}$ cm and D = 5.9 inches was set to cause an angular ray aberration of less than 1.1% of the side of an IFOV. An irregularity specification of 1 fringe maximum over the clear aperture of 6.25 inches minor axis and 8.83 inches major axis was set to keep aberrations to less than 0.2% of the side of an IFOV. After polishing to the specification, an aluminum reflective layer was evaporated on to the surface, followed by a thin protective coating of magnesium fluoride. The reflectance of the completed surface was specified at 0.95 or greater at wavelengths from 3.5 to 16.0 microns and 0.85 or greater at wavelengths from 0.65 to 0.75 microns. When completed the weight of the finished mirror was 214 grams.

The mirror is mounted to the shaft by a slotted key that sets the 0° position of the motor assembly. Set screws and staking compound are both used to bond the mirror to the shaft.

The mirror is left unbalanced to reduce system weight. The c.g. of the mirror is .464 inches from the axis. The weight required for dynamic balance would have been nearly that of the mirror itself. Inertia of the scan mirror is .077 ounce-inch-seconds^2.

3.3.3 Scan Motor

The mirror drive motor was purchased from Computer Devices Corporation and is a permanent magnet D.C. synchronous stepping motor. The shaft and bearing design was specified by ITT, with bearings and lubricant supplied to the manufacturer. The rotor is an integral part of the shaft assembly. Design of the motor includes requirements for operating at 1.8° steps at

100 pulses per second with a torque output of a minimum of 20 ounce inches and an unpowered torque of 3 ounce inches. The accuracy of the steps is 1.8^{o} ± 3% non-accumulative, which sets the final system positioning accuracy. In final tests we found the accuracies to generally be within 1%. The rotor inertia of the stepper is less than .10 $lb\text{-}in^2$.

The bearings supplied to CDC were Barden Bar Temp bearings. A duplex pair with 2 pounds of preload are used in the mirror end and a single bearing at the housing end of the motor. The bearings were cleaned and lubricated by NASA using G300 grease. Design of the motor end caps minimize the loss of lubricant to space by means of a labryinth type seal. The rear seal enters the scan cavity which is expected to maintain a low vapor pressure, aiding the retention of lubricant in both the motor and the pin encoder.

3.3.4 Position Encoder

The position of the mirror is continuously monitored by a special encoder assembly that provides unique outputs for each scan condition (nadir, start of scan, internal targets, space targets) and for position monitoring during scan and operation. The encoder is a Litton pin type encoder specifically designed for the HIRS system. The encoder disc is a printed pattern of 19 functions in a disc 2.5 inches diameter. The outputs from the disc are detected by spring loaded pins riding on the commutator surface. Table 3.3-1 lists the outputs from the encoder and the number of pins for each encoder segment. Note that the most vital functions have the most redundancy.

The pin cage is mounted fixed to the motor housing, requiring careful alignment in all axes. The pins are lubricated by F-50 oil in each pin mounting hole, effectively providing a long term reservoir. Electrical connections to the pins are by short wires looped from pin to pin and a terminal. From the terminal a flexible wire leads to a terminal board. In the proto-flight unit, after vibration tests, it was noted that the output from the 2^3 track was intermittent. This continued during all succeeding tests, to the extent that there is now no output from that track. From a review of the design and test results it was concluded that only this one pin set was involved, and that the most likely cause was a set in the wire holding the pins away from the contact. An added vibration test showed no change in this track and no deterioration of other tracks. Data utilization programs by NOAA have been modified to accept each encoder position and the eighth count less than that position.

TABLE 3.3-1

SCAN POSITION ENCODER

Pin	Function	Position	No. of Pins
A	Start of Scan	0^{o}	3
B	Nadir	36.0^{o}	3
L	Int. Warm Tgt	151.2^{o}	3
V	Common	All	4
C	Space	331.2^{o}	3
N	Int. Cold Tgt	241.2^{o}	3
E	Position 2^{0}		2
P	2^{1}		2
D	2^{2}		2
R	2^{3}		2
T	2^{4}		2
F	2^{5}		2
S	2^{6}		2
G	2^{7}		2
J	Chamber Earth Tgt	23.4^{o}	3
K	Chamber Space Tgt	66.6^{o}	3
M	Reference 0 Mark	0^{o}	1
H	Slip Ring		2
U	Slip Ring		2

3.3.5 Torque Motor

The torque motor was added to the motor drive system to provide a control torque for damping of the mirror motion at the end of retrace. It was found necessary to add a dynamic control loop of tachometer velocity detection and torque motor power to prevent overshoot at scan element zero. The torque motor selected is identical to that used in a prior spacecraft instrument for controlled mirror scanning. The motor is 2.5 inches in diameter, .500 inches thick, has a peak torque of 18 oz inches and a continuous torque rating of 6 oz-in. Although it is designed for angular excursions of $\pm 60^{\circ}$ we aligned the unit for prime operation at the start of scan. This motor is encapsulated, weighs 3.5 ounces, and has a rotor inertia of 9×10^{-4} oz-in-sec^2. Care in mounting of the rotor on the shaft and in alignment of the rotor and stator were important to provide uniform gap and consistent operation. The unit was purchased from Aeroflex Corporation.

3.3.6 Tachometer

Velocity sensing of the mirror motion is made possible by the tachometer mounted on the shaft extension from the scan drive motor. The tachometer is from Aeroflex Corporation and has a $\pm 60^{\circ}$ operating angle similar to the torque motor. It is only 1.7 inches in diameter, .350 inches thick and has an output sensitivity of 0.17 volts/rad/sec. This unit is also from a series used in previous space programs, and is encapsulated for space use. The tachometer rotor is mounted to a shaft extension and is carefully aligned to ensure free movement and uniform rotor to stator spacing.

3.3.7 Scan Housing

The design of the scan housing included consideration of ease of alignment and test as well as structural and thermal soundness. The housing is a machined aluminum box with a cover plate. The cover is sealed to the box with one vent hole to space. Two electrical connectors provide mating to the main electronics while flat machined surfaces, dowel pins, and screws together determine the rigidity of the system. Both the internal warm and cold targets tie in to the scan housing, providing a structural bridge to the optics block. The cold target is mounted on synthane heat blocking spacers while the warm target is tied in solidly with screws.

The three printed circuit cards have heat sinks that contact the surface of the housing for thermal conduction. Most of the heat from the scan housing is thermally conducted to the baseplate, but some is conducted to the sun shield and emitted to space. The temperatures of the scan mirror and the scan motor are

monitored by thermistor sensors. The scan mirror typically varies from 8.5 to 12.5°C during an orbit. The scan motor temperature runs approximately 1.5° above baseplate temperature.

3.4 Electrical System

3.4.1 General

A permanent magnet stepping motor steps or rotates in response to an orderly sequencing of current within its phase windings. The direction which the motor rotates is also dependent upon this orderly sequencing. The rate of rotation is controlled only by the rate at which current in the windings is sequenced.

The HIRS utilizes a two-phase permanent magnet stepping motor to drive the scan mirror. It has a total of 200 distinct 1.8° steps per revolution when driven by a two-phase motor driver. Two phase motor drives can be in either of two basic forms, providing the motor has split-phase windings; 1) the unipolar drive and 2) the bipolar drive. The bipolar drive is the type used on the HIRS scan mirror drive motor.

A desirable characteristic of unipolar drive is circuit simplicity, which results in both high packaging density and high reliability. These features recommended it for use in implementing the phase sequencing electronics of the cooler cover drive motor (a very similar 200 step per revolution permanent magnet step motor also used on HIRS). A simplified schematic diagram and timing diagram of this motor control electronics is found in Section 8.10. However, where high inertia loads are used on a motor and both rapid angular acceleration and deacceleration is required, as is the case in the scan mirror subsystem, the bipolar drive excels, despite its relatively high circuit complexity. This is due to the fact that motor output torque increases in the bipolar compared to the unipolar design with no increase in motor input power. Referring to Figure 3.4-1, this can be shown to be the result of doubling the turns through which winding currents flow, for motor torque is proportional to the ampere-turns product. In the bipolar drive, current "i" is always flowing (in one direction or another) in windings A, B, C, and D, while in the unipolar drive, current "i" is flowing only in either A or B and in either C or D.

For both an arbitrary motor position θ_o (where both i_{AB} and i_{CD} are assumed positive) and an arbitrary positive rotational direction where one step of 1.8° is termed $\Delta\theta$, a step sequence is shown in the table below.

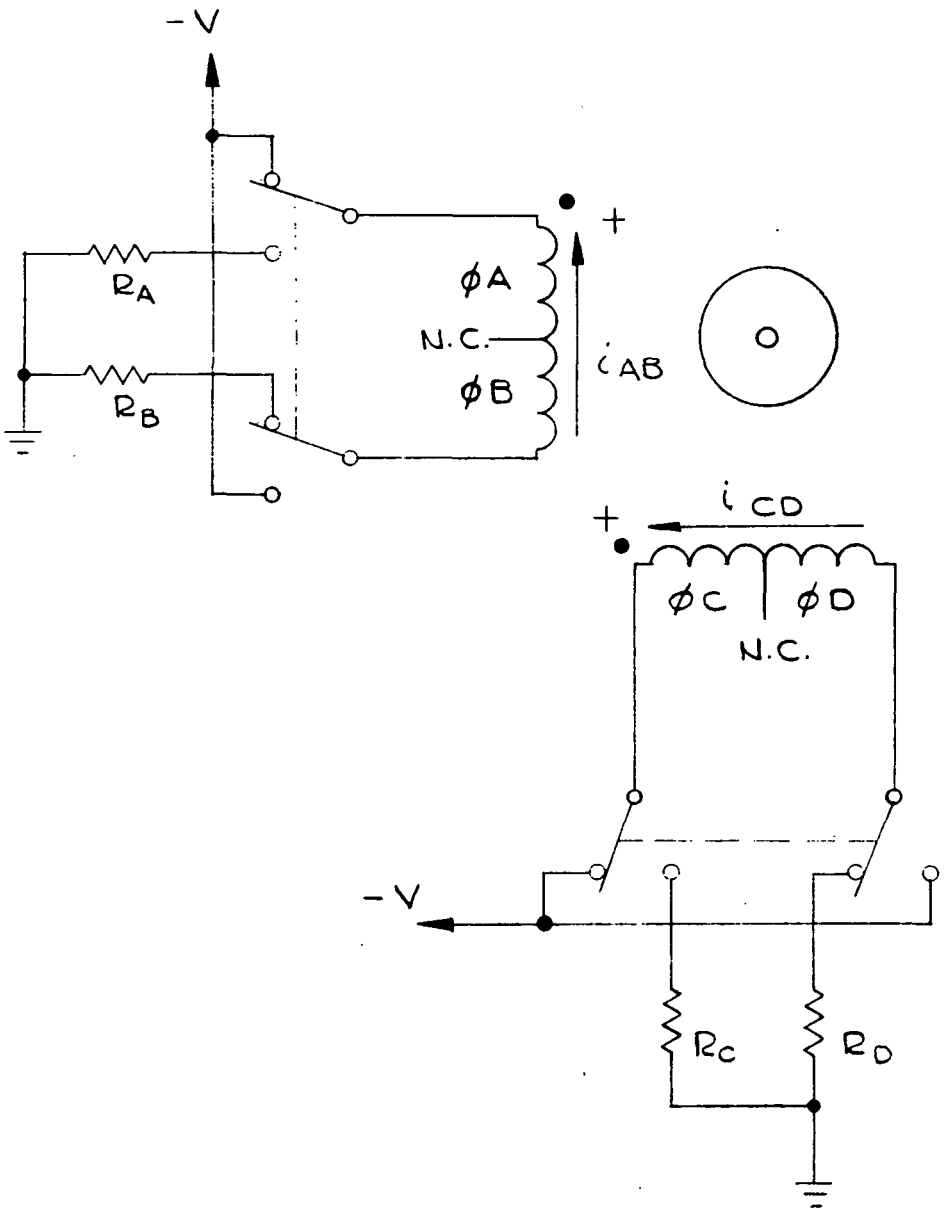


FIGURE 3.4-1 SIMPLIFIED BI-POLAR PM STEPPING MOTOR DRIVE

Mirror Angular Position	Motor Winding Current i_{AB}	Motor Winding Current i_{CD}
$\theta_o - 3\Delta\theta$	+	-
$\theta_o - 2\Delta\theta$	-	-
$\theta_o - \Delta\theta$	-	+
θ_o	+	+
$\theta_o + \Delta\theta$	+	-
$\theta_o + 2\Delta\theta$	-	-
$\theta_o + 3\Delta\theta$	-	+
$\theta_o + 4\Delta\theta$	+	+
$\theta_o + 5\Delta\theta$	+	-

Positive directional rotation from this sequence ↓

3.4.2 Operating Modes

The scan motor is under digital control with the following stable sub-modes of operation.

3.4.2.1 Launch Mode

The launch slew mode results from two coincident HIRS commands; Electronics Power "OFF" and Scan Motor Power "ON". In this mode the scan mirror is rotated at a constant angular velocity of approximately thirty revolutions per minute. This mode exists for the purpose of reducing the possibility of brinelling the stepping motor bearings during the time that high vibration "g" forces are encountered during spacecraft launch.

3.4.2.2 Earth Scan Mode

The earth scan mode during which the mirror is incrementally advanced one step of 1.8^o coincident with the end of radiometric data taking (as defined by the spectral filter locations upon the rotating filter-chopper wheel.) Filters again

begin to pass through the optical path precisely 35 ms following the initiation of a mirror step. As the HIRS instrument spectral data for obtaining accurate "sounding" must be from within a non-oscillatory instantaneous field of view, a particular requirement of these single mirror steps is that both a mirror stepping angle of 1.8^{o} and settling to within a ± 1% error band of this step angle must be accomplished within a time of 45 msec. The technique of driving the motor for single step operation is by the use of a torque-retrotorque - torque (T-R-T) pulse train. This wave train is controlled over a 32 millisecond period; within that interval the T-R-T transitions can be varied with precisely one-half millisecond resolution. In the HIRS Protoflight, to achieve proper individual step response, e.g., result in best electronic dampening, the first torque pulse to the next pole (new step position) is on for 13.5 ms, then the retrotorque pulse (previous pole position) is on for 10.5 ms. The remaining 8 ms of this 32 ms period is again torque to the next pole. This entire 32 ms period, as well as the remaining 74.2 ms of an element, is at low motor power as the voltage on the bridge driver is the output of the scan electronics switching regulator, approximately minus eight volts dc rather than minus twenty-four volts dc.

The technique works in the following manner. During the first torque period, the velocity builds up to a maximum and the momentum of the system is at a peak. At the retrotorque point, the previous set of windings are energized, tending to reverse the rotor motion. Energy is therefore dissipated in slowing the rotating mass. If the retrotorque energy matches that of the torque energy, the rotation will be stopped. If these are properly balanced and timed, the motion will be precisely 1.8^{o}. If the timing is not absolutely precise, the position error can be corrected by reapplying torque. The actual timing points (within the 32 ms period) are somewhat critical to proper dampening, yet when digitally set, they will never change. To further improve the electronic dampening, the output of the switching regulator is adjusted to optimize the step response.

3.4.2.3 Slew Mode

The "slew mode" describes mirror motion in "retrace slew" the reverse direction to earth scanning for repositioning the mirror to the origin of a new earth scan line, and in the "forward slew" or earth scan direction to each of the three radiometric calibration positions. Two of these are internal blackbody calibration targets while the third is a view to "cold space." The slew mode occurs during the last four elements of each line, under the control of the scan element and scan line counters described in Section 8.2. During this mode power to the motor bridge drivers is switched from the lower voltage switching regulator output to the input buss voltage of -24.5 VDC to greatly increase the torque of the motor.

3.4.2.4 Dwell Mode

The mirror dwell mode is a mode which allows the mirror to hold its position for 42 element times on each of the three calibration positions for data taking and is implemented in the subsystem by disabling the earth scan mode described in "2" above.

3.4.2.5 Nadir Mode

The commandable scan mode OFF or Nadir mode, a higher priority mode which when commanded, drives the mirror field of view to the approximate center of the earth scan arc and holds the mirror in this orientation until such time that either scan mode ON is commanded or the HIRS electronics or scan motor subsystems are commanded OFF. This mode is a back-up mode intended for use in the event that the normal pre-programmed scan-pattern control circuitry develops a serious malfunction which prevents normal scan system operation.

3.4.2.6 Mirror Over-ride Mode

The mirror over-ride mode, a mode with higher priority than NADIR mode above (when both the scan motor and instrument electronics are ON) is used only during contractor vacuum-thermal chamber tests. This mode is controlled through two Test Connector pins, one of which when grounded interrupts the normal scan pattern routine and causes mirror slewing to the nearest of two V/T chamber radiometric targets (always in a "forward slew" direction.) While maintaining the electrical ground on the test connector pin mentioned above, a momentary ground applied to the second test connector pin discussed above always results in mirror slewing to the other chamber target position. The entry to this mode, it must be remembered, is not possible during orbital operation or at the integration contractor facility for in neither instance, by prior agreement, are the two control lines to the test connector wired into the external system cabling.

3.4.3 Circuit Implementation

The Mirror Scan subsystem can be independently commanded on and off with only one operating constraint; the scan mode must be in the on state when scan motor power is applied coincident with electronics power on to prevent a high power dissipation mode of operation of the subsystem. This condition is not destructive to the mirror scan subsystem, but must be avoided because of the unnecessary spacecraft power drain.

The motor control logic is completely implemented with CMOS logic elements powered by a subsystem -12 VDC integrated linear regulator (REG 1) contained on the Scan Motor Regulator board (Schematic 8120019).

Motor phase currents are controlled by two latch-back-NAND R-S type flip-flops on the Motor Phase Control board (Schematic 8120255). Two input NAND gates on this board decode two fully decoded hexadecimal digits developed on the Slew/Scan Clock Logic and Decoders board (Schematic 8120359) which directly determine the state of the two phase control R-S latches.

A total of four "four line to eight line" decoders (logic circuits A5, B5, C5 and D5 of the Schematic 8120359) convert the eight bit outputs of the bi-directional binary counters A4 and B4 to two fully decoded hexadecimal digits. Since two hexidecimal digits count to 256 (decimal) which control the repetitive pattern of four motor steps, one motor step, therefore, requires a total of 64 clock pulses to the bi-directional counters. The 64 clock pulses (at a 2 KHz rate) per motor step determine the 32 ms torque-retrotorque - torque technique (with 0.5 ms resolution) of reverse pulse electronic dampening of the stepping motor. This is further described in Paragraph 3.4.3.2.

Frequency control of motor stepping is provided by two cascaded gated astable multivibrators (separated by a divide by 100 circuit). The first astable is driven by the 400 KHz instrument clock;the second astable is synchronized by the 4 KHz clock which is further divided by two to obtain the 2 KHz symmetrical bi-directional counter clock used for individual motor steps during "Earth Scan Mode." Additional gating on the Slew/Scan Clock Logic and Decoders board provides for forward/reverse control of the eight-bit counter (the UP/DOWN control input), counter clock inhibit control either in the Earth Scan Mode (see Paragraph 3.4.3.2) or the Slew Mode (see Paragraph 3.4.3.2) and a triangular ramp voltage input (Accel. Slew) which effectively results in a slew velocity profile linearily controlled by the ramp voltage. This is accomplished by modifying the 4 KHz gated astable multivibrator to a voltage controlled configuration and by enabling its free-running mode by means of the "Slew/Scan Control" input to the board.

The triangular ramp is developed on the Step-Scan Control Logic #3 board (Schematic 8120420) by means of an eight bit bi-directional presettable binary counter driving an R-2R resistor ladder network. Suitable control gating (at Board Pins 6 and 8) presets the counter to a count of 64 and enables a separate gated astable multivibrator on this board to clock the counter. At the full count of 255 decimal, circuit gating detects and stores the event, reversing the counting direction. When the counter counts down to zero, the event is detected and stored. This disables further clocking of the counter until the entire sequence is repeated by an input at both Pins 6 and 8.

Step/Scan Control Logic No. 2 board (Schematic 8120369) contains negative edge triggered one-shot multivibrators which

interface the main system control electronics. Edge triggered circuitry is used for logic level translation (0 VDC to +10 VDC electronic system logic to -12 VDC to 0 VDC of the mirror scan system logic). In this way the scan system can be controlled by the data format circuitry of the instruments electronics system. Necessary element/line number information, filter wheel sync or "once around pulse" and electronics status are the board inputs. Outputs are the Slew Mode - Earth Scan Mode control (Slew/Scan on board pin 5) and motor direction control (UP/DOWN on Board 19). Also contained on the board is a four position electronic switch used to attenuate the triangular voltage ramp so that peak slewing velocity can be matched to the four distinct angular magnitudes which are a part of each twenty-three line grid pattern.

Step/Scan Control Logic No. 1 (Schematic 8120342) contains the gating which interfaces the mirror/motor shaft "pin-encoder." Circuitry contained herein establishes mode priority control described in Section 3.4.3 as well as that involved in mandating a correct start-up sequence of the mirror system when entering or exiting various operating modes. A comparator on the board determines if the electronics subsystem is on or off for the mirror scan subsystems internal use. A logic level converter provides an output to the electronics subsystem line counter so that the data output circuitry can become initialized with respect to the mirror position.

Entrance to the normal operational mode called Earth Scan Mode (see Paragraph 3.4.3.2) following electronics and scan motor power turn on is only by way of stopping the mirror at the encoder 300K target track (encoder position 84 decimal). Following data taken with a stopped mirror, the next slew is to the encoder "Space" target (encoder position 184). Following data taking with the mirror stopped, the mirror then slews 16 motor steps to the encoder "Start of Scan" position (encoder position 0).

Data will then be taken at position 0 in element 0 through position 41 in element 41 by means of incremental stepping of the mirror coincident with each new element. Mirror retrace slew then occurs in the last four element times of this line to reposition the mirror at the start of scan position. Twenty total lines of data utilizing single step incrementing of the scan mirror will then be followed by a repeat of the slew to the encoder 300K target position with the previously described scan pattern repeating each twenty-three lines.

A command input called Target Mode ON/OFF, which may be initiated at any time in the twenty-three line pattern, will interrupt the scan line counter clocking input. The effect (when commanded OFF) is to prevent subsequent mirror slews to the three calibration target positions. Note that it does not prevent an initial entry to normal operation via the three calibration

target positions nor does it inhibit if the command is initiated during the twentieth scan line (it will, however, prevent further slewing to the calibration target positions after earth scanning is resumed).

Following mirror/data system initialization at turn-on scan mirror position is dictated solely by the programmed scan pattern generation circuitry and the fact that only four encoder tracks are permitted (when AND'ed with correct motor phase logic signals) to halt the motor. Should synchronization between the mirror/data system be somehow lost due to an unforseen transient condition, the motor control logic continuously checks, on each retrace slew, that the start of scan encoder track position is reached before the four element times of slew have elapsed. If this logic condition is not verified as correct on each retrace slew, the mirror scan system jumps from normal electronics control of the scan pattern to an unaccelerated high power slew to the encoder 300K target position, concurrently resetting the line counter to zero (the 300K target line). In this way mirror operation in an out of correct logic sequence is continuously monitored, and an immediate logic decision is made to correct an abnormal mirror scan operation.

The eight bit complemented natural binary code output of the encoder (each line having two pins for redundancy) is not utilized by the scan subsystem; it is only inserted into the instrument data format as a mirror position read-out. Only the four positions described above and the NADIR track (encoder position 20) can result in stopping mirror slew. Each track has three pins for redundancy and the detection circuitry with the mirror scan subsystem requires only a momentary contact sufficient to clock an event storage flip-flop.

3.4.4 Linear Electronic Dampening

The scan system, late in the design, had an active linear electronic damper added, consisting of a D.C. torque motor and tachometer mounted to the scan motor shaft, and an interconnecting amplifier. A block diagram of the damper and scan system is shown in Figure 3.4-2.

During retrace slew, the stepper motor has a 40 Hz velocity component due to system electro-mechanical resonances. This 40 Hz component represents great changes in step motor acceleration during retrace. This is reduced to achieve controlled retrace. To accomplish this, the signal proportional to motor shaft velocity from the tachometer is partially differentiated to give a signal at 40 Hz proportional to acceleration. This signal, after amplification and phase inversion, is applied to the DC torque motor to reduce the 40 Hz acceleration component but not materially affect the desired velocity profile of the retrace slew.

The 40 Hz acceleration component was substantially reduced in this manner. The damping system transfer function during the retrace mode is given below.

$$\frac{E_o}{E_{in}} = \frac{10(.079\ S + 1)}{(.0079\ S + 1)\ (.0014\ S + 1)}$$

In normal step mode the step motor drive power is reduced and the system requires a different transfer function for best operation. This is accomplished by reversing the positions of Switches S1 and S2 of Figure 3.4-1. It must be realized that this linear electronic dampening method complements the torque-retrotorque -torque dampening described earlier.

3.5 Scan Mirror Position Measurement

The step position accuracy of the HIRS Protoflight scan mirror system was measured with a Laser setup as shown in Figure 3.5-1.

The scan housing was mounted on an optical bench fitted with an indexing head, permitting the mirror assembly to be rotated on axis through the scan arc. A sync signal was provided externally allowing the mirror to either scan normally or in discrete steps upon command.

Beginning at SE $\emptyset$ (start of scan position) the Laser spot was centered on the target reference line.

The command was then given for the mirror to step to the next position and the spot deflection (h) measured and recorded. After each measurement, the spot was again centered on the reference line by rotating the indexing head prior to advancing to the next step. This process was repeated for each of the 41 steps and for 4 complete scan lines.

From the recorded data, the step angle (θ) was calculated as:

$$\theta = \tan^{-1} \frac{h"}{443"}$$

This data was further processed in both tabular form and graphically to show the percent deviation for each step from the nominal 1.8^o. A cross check for validity of these measurements was performed by allowing the mirror to scan in the normal manner and measuring the deflection (h) at a number of step positions.

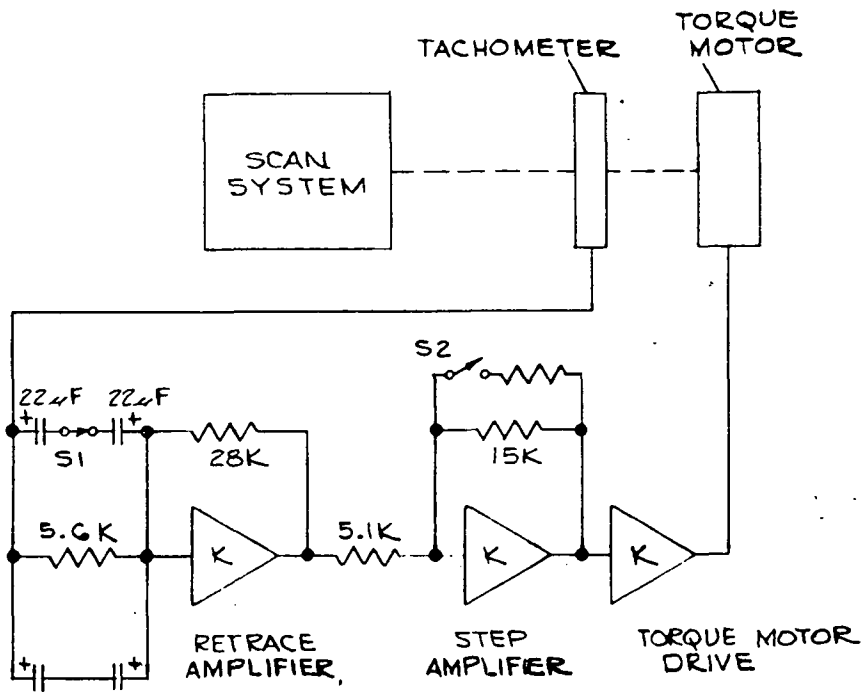


FIGURE 3.4-2 BLOCK DIAGRAM HIRS SCAN SYSTEM WITH ACTIVE DAMPER

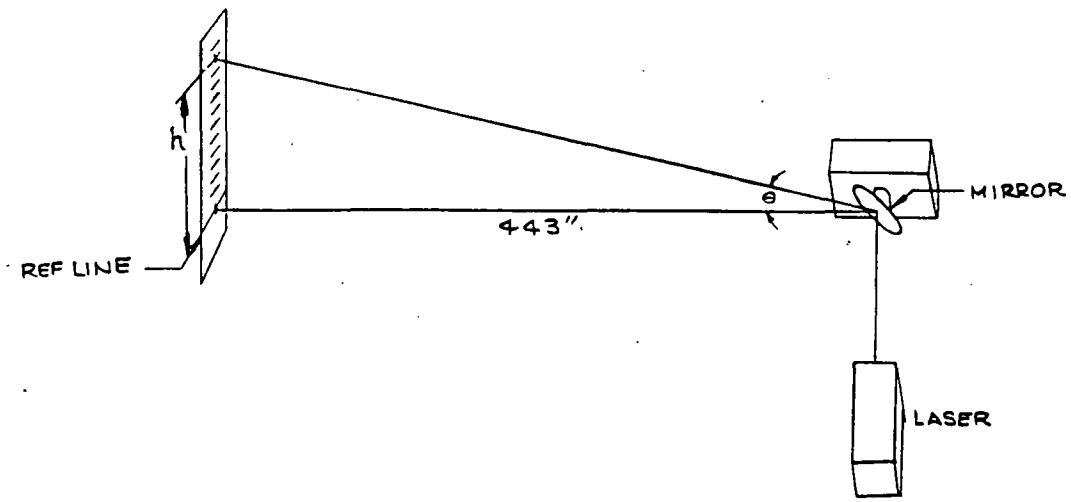


FIGURE 3.5-1 MIRROR SCAN TEST METHOD

Comparing these results with that previously recorded verified that the initial method of measurement was valid.

The test results are tabulated in Table 3.5-1. It may be noted that the first step is shorter than the others indicating that the initial minor position is approximately 0.19^{o} away from nominal. At all subsequent positions the maximum deviation is less than 2.5% or 0.05^{o}, well within the 3% tolerance specified by the motor manufacturer as the absolute step position error.

Table 3.5-1 HIRS Scan Mirror Test Data (Protoflight)

RUN
HIRS PROTOFLIGHT MODEL
SCAN MIRROR REGISTRATION
DATE 4/11/74
PROGRAM TR-41174
INPUT IS VIA DATA STATEMENTS AT END OF PROGRAM

DATA INPUT

STEP	SAMPLE 1	2	3	4
1	12.35	12.35	12.45	12.35
2	14.15	14.25	14.3	14.35
3	14	14.1	14	13.95
4	13.9	14	14	13.95
5	14	14	14	13.9
6	14.1	14	14.05	14.1
7	13.95	14	13.95	13.95
8	13.9	13.95	13.95	13.9
9	14	14.1	14	14
10	14	14	14	14
11	13.95	13.9	13.95	13.95
12	13.9	13.9	14	13.95
13	14.1	14	14.05	14
14	14	14.1	14.05	14.1
15	13.85	13.9	14	13.95
16	13.9	13.85	14.9	13.9
17	14.1	14.15	14.1	14.1
18	14.1	14.05	14	14.05
19	13.85	13.85	13.8	13.8
20	13.9	13.8	13.8	13.9
21	14.15	14.15	14.15	14.1
22	14.15	14.1	14.1	14.1
23	13.8	13.8	13.8	13.85
24	13.95	13.9	13.95	13.9
25	14.15	14.1	14.1	14.1
26	14.15	14.15	14.15	14.1
27	13.75	13.8	13.8	13.8
28	13.9	13.9	13.9	13.9
29	14	14	14.05	14.05
30	14.2	14.2	14.15	14.15
31	13.8	13.75	13.75	13.75
32	13.9	14	14	13.95
33	14	14	14.05	14
34	14.3	14.25	14.25	14.25
35	13.7	13.8	13.8	13.7
36	13.9	13.9	13.95	13.95
37	14	14	14	14.1
38	14.25	14.3	14.25	14.25
39	13.75	13.7	13.7	13.75
40	13.9	13.9	13.85	13.9
41	14	14.1	14	14

SCAN MIRROR REGISTRATION

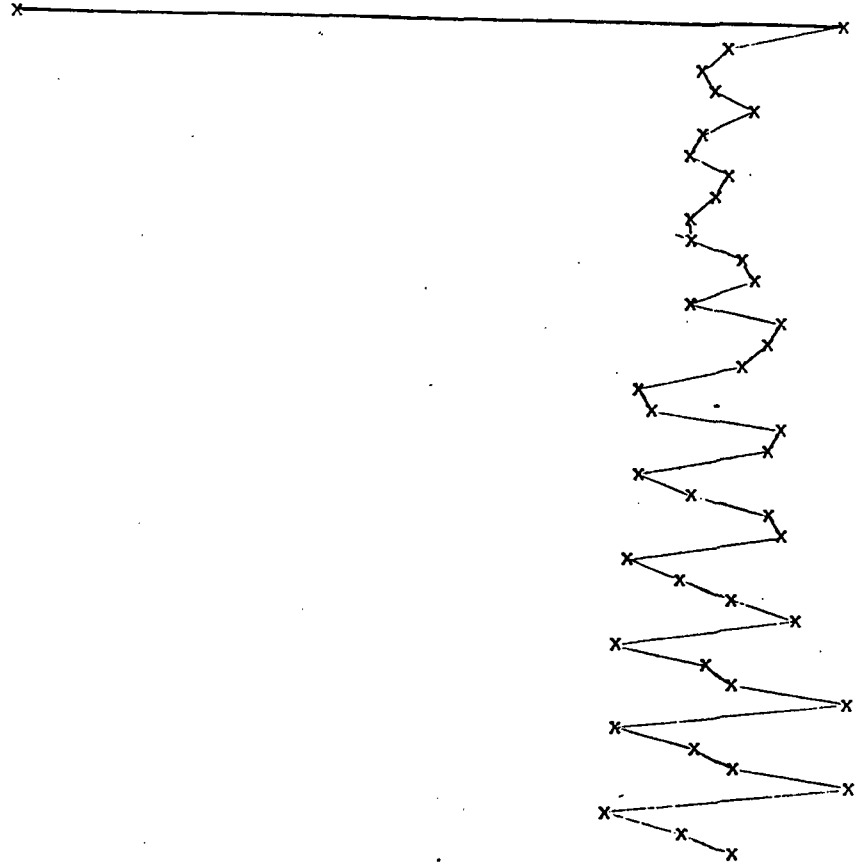
	DEGREE				
SAMPLE 1	2	3	4	AVERAGE
1.59668	1.59668	1.6096	1.59668	1.59991
1.82924	1.84216	1.84862	1.85508	1.84378
1.80986	1.82278	1.80986	1.80341	1.81148
1.79695	1.80986	1.80986	1.80341	1.80502
1.80986	1.80986	1.80986	1.79695	1.80663
1.82278	1.80986	1.81632	1.82278	1.81794
1.80341	1.80986	1.80341	1.80341	1.80502
1.79695	1.80341	1.80341	1.79695	1.80018
1.80986	1.82278	1.80986	1.80986	1.81309
1.80986	1.80986	1.80986	1.80986	1.80986
1.80341	1.79695	1.80341	1.80341	1.80179
1.79695	1.79695	1.80986	1.80341	1.80179
1.82278	1.80986	1.81632	1.80986	1.81471
1.80986	1.82278	1.81632	1.82278	1.81794
1.79049	1.79695	1.80986	1.80341	1.80018
1.79695	1.79049	1.92613	1.79695	1.82763
1.82278	1.82924	1.82278	1.82278	1.8244
1.82278	1.81632	1.80986	1.81632	1.81632
1.79049	1.79049	1.78403	1.78403	1.78726
1.79695	1.78403	1.78403	1.79695	1.79049
1.82924	1.82924	1.82924	1.82278	1.82763
1.82924	1.82278	1.82278	1.82278	1.8244
1.78403	1.78403	1.78403	1.79049	1.78564
1.80341	1.79695	1.80341	1.79695	1.80018
1.82924	1.82278	1.82278	1.82278	1.8244
1.82924	1.82924	1.82924	1.82278	1.82763
1.77757	1.78403	1.78403	1.78403	1.78241
1.79695	1.79695	1.79695	1.79695	1.79695
1.80986	1.80986	1.81632	1.81632	1.81309
1.8357	1.8357	1.82924	1.82924	1.83247
1.78403	1.77757	1.77757	1.77757	1.77918
1.79695	1.80986	1.80986	1.80341	1.80502
1.80986	1.80986	1.81632	1.80986	1.81148
1.84862	1.84216	1.84216	1.84216	1.84378
1.77111	1.78403	1.78403	1.77111	1.77757
1.79695	1.79695	1.80341	1.80341	1.80018
1.80986	1.80986	1.80986	1.82278	1.81309
1.84216	1.84862	1.84216	1.84216	1.84378
1.77757	1.77111	1.77111	1.77757	1.77434
1.79695	1.79695	1.79049	1.79695	1.79533
1.80986	1.82278	1.80986	1.80986	1.81309

Table 3.5-1 (Continued)

PERCENT STEP VARIANCE FROM 1.8 DEGREE

STEP	PERCENT DEVIATION
1	-11.1163
2	2.432
3	.63773
4	.27887
5	.368595
6	.99659
7	.278884
8	9.73543E-03
9	.727442
10	.548018
11	9.94470E-02
12	9.94470E-02
13	.817153
14	.99659
15	9.73543E-03
16	1.53479
17	1.35546
18	.906865
19	-.707984
20	-.528561
21	1.5349
22	1.35546
23	-.797696
24	9.73543E-03
25	1.35546
26	1.5349
27	-.977145
28	-.169701
29	.727442
30	1.80405
31	-1.15659
32	.27887
33	.63773
34	2.432
35	-1.24631
36	9.73543E-03
37	.727455
38	2.432
39	-1.42576
40	-.259413
41	.727442

PLOT OF DELTA STEP IN DEGREES AS A FUNCTION OF SCAN ELEMENT.
MAX VALUE= 1.84378
MIN VALUE= 1.59991
Y AXIS VALUE = 3.75182E-03 DEGREES PER UNIT
Y AXIS++



READY

4.0 FILTER WHEEL SYSTEM

4.1 General Description

The filter wheel system is composed of the following basic parts: filter wheel assembly, drive motor assembly, long wave chopper, and temperature controlled enclosure. Figure 4.1-1 illustrates these four main parts.

The purpose of the filter wheel system is threefold:

1. Mechanically chop the optical signal in two specific bands at two separate chopping rates.

2. To optically filter the input visible and infrared radiant energy into seventeen (17) different spectral bands or channels.

3. To thermally control these filters and optical choppers at a nominal background temperature of 30°C ± 0.6°C.

The filter wheel system is detailed by both Drawing No. 8119305 (Figure 4.1-2) and the exploded view drawing of Figure 4.1-3.

Unique features of the Filter Wheel Assembly include the extreme compactness of the motor and filter wheel system, with the motor rotor becoming an integral part of the wheel. Gearing for the longwave chopper drive to achieve a 6:1 rotational rate increase is provided by a planetary and sun gear within the wheel volume. The longwave chopper blade extends only far enough above the filter wheel to provide clearance for optical pickups.

The thermal design of the assembly is as important as the mechanical. Heat from the motor stator windings is directly coupled to the main frame of the system. The wheel and rotor are separated from the stator by bearings, breaking a direct path for heat transfer. The filters on the wheel are mounted in insulating material and therefore change temperature slowly. The temperature of the filter wheel and longwave chopper are primarily controlled by radiant coupling from the internal surfaces of the housing. This housing interior is painted black has two controlled heaters, four platinum temperature sensors and a platinum control sensor. A feedback temperature control circuit maintains the housing at a fixed temperature of 30°C ± 0.6°C over a wide range of baseplate temperatures. All mounts for the housing are low heat conductive synthane, and radiant heat loss is controlled by four layers of an alternately applied aluminized mylar and silk blanket. During normal operation the short term temperature variation of the housing and its internal components is less than .05°C.

The filter wheel assembly is mounted firmly to the optics block where it is pinned in place. The relay optic element enters a portion of the housing, nearly sealing the volume against radiant heat loss. The relay optics are housed in a synthane block which has a relatively high thermal resistance, and therefore does not affect the filter wheel temperature significantly.

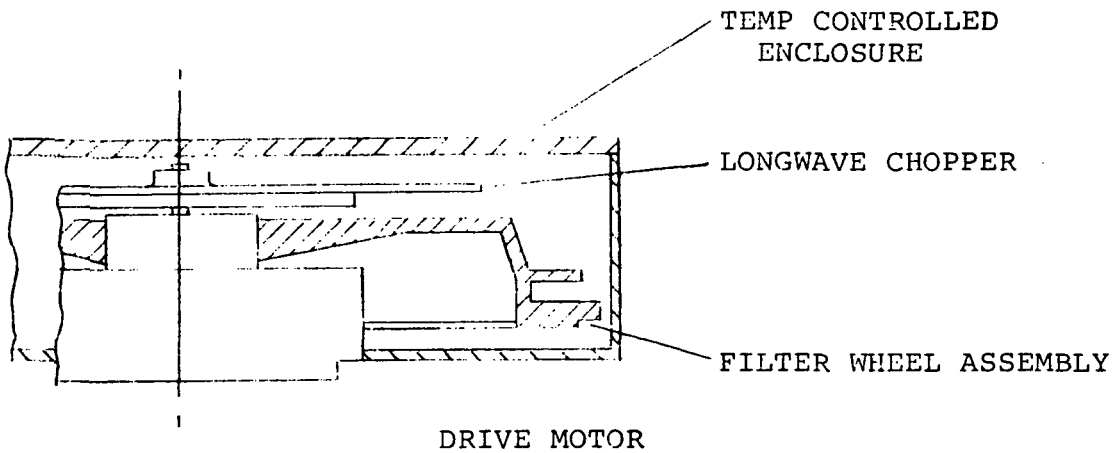


FIGURE 4.1-1 BASIC FILTER WHEEL SYSTEM

The basic filter wheel system parts can be studied separately for functional requirements and engineering data.

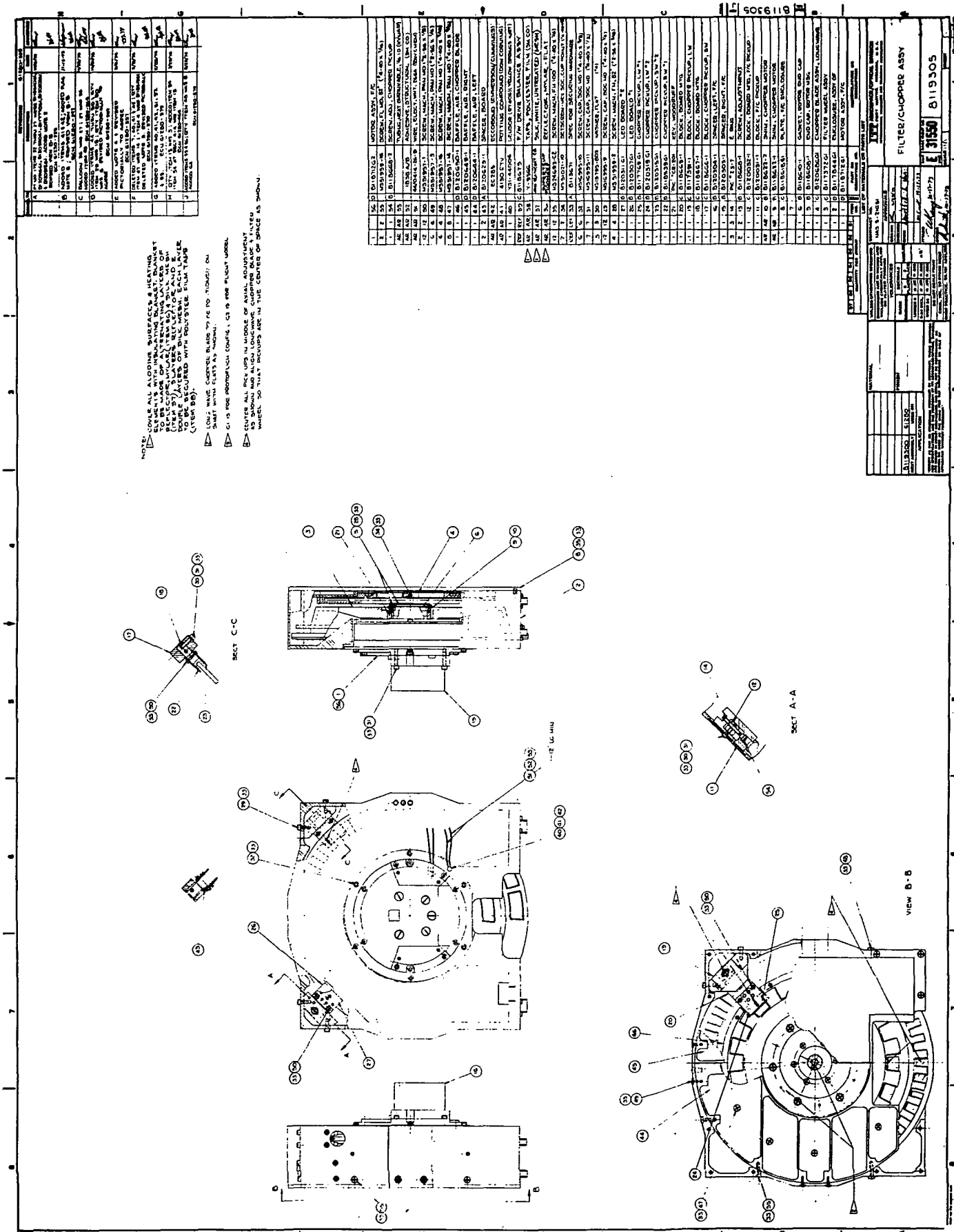
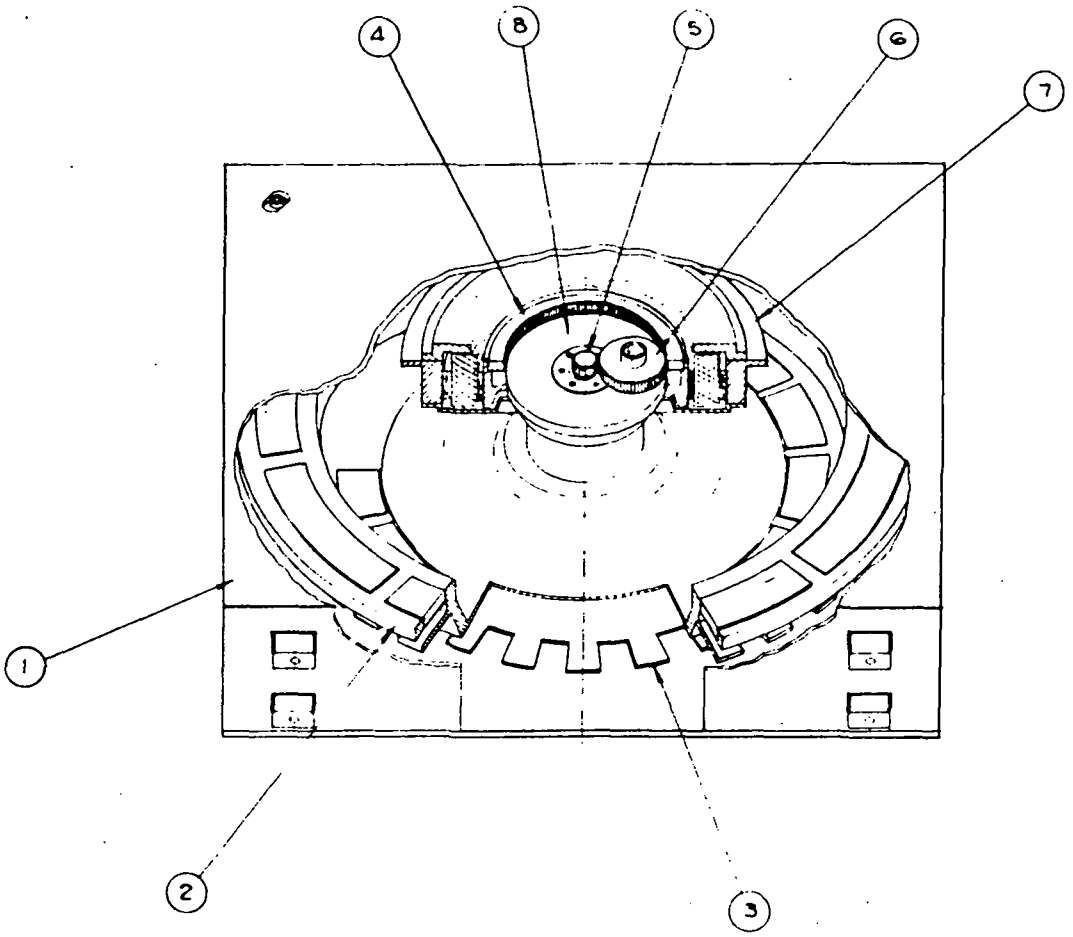


FIGURE 4.1-2 FILTER CHOPPER ASSEMBLY



1. TEMPERATURE CONTROLLED ENCLOSURE.
2. FILTER WHEEL
3. LONGWAVE CHOPPER
4. INNER GEAR & ROTOR
5. SUN GEAR LONGWAVE SHAFT.
6. PLANET GEAR
7. MOTOR WINDINGS
8. ROTOR & BEARINGS SUPPORT

FIGURE 4.1-3 FILTER/CHOPPER SYSTEM

4.1.1 Filter Wheel Assembly

The filter wheel assembly is illustrated in Figure 4.1-4 (ITT Drawing No. 8117372). The basic purpose of the filter wheel assembly is to house the seventeen optical filters that are used to separate the input radiant signal into seventeen channels.

The filter wheel assembly performs the following functions:

1) Mechanically clamps the germanium filters in place and isolates the filters from external vibration to ensure vibration survival.

2) Rotates at constant speed of approximately 564.7 rpm.

3) The filter wheel is physically divided into two separate bands (the shortwave and the longwave band).

4) The filter wheel positions the filters radially and in an angular position consistent with electrical integration times.

As illustrated in Figure 4.1-4, the wheel is circular shaped. The shortwave band filters are located on a 3.80 in. filter center radius. The longwave band filters are located on 2.80 in. filter center radius.

The basic engineering data regarding the filter wheel (including motor rotor) are tabulated below.

FILTER WHEEL PROPERTIES

Inertia	.486 oz-in sec^2
Rotational Speed	564.97 rpm
Kinetic Energy	53.2 in#
Base Material	Aluminum 6061-T6
Weight (with filters)	1.27 pounds
Surface finish	Alodined with areas of "bare" aluminum
Outside diameter	8.50 in.

The filter wheel is mounted on a G-10 synthane bushing on the 564.97 rpm shaft. The synthane bushing is incorporated in the design to thermally isolate the filter wheel conductively from the drive shaft. The thermal isolation is needed for thermal control of filter wheel at 30 degrees C.

The filter wheel assembly was dynamically balanced at 1600 rpm to within .0007 oz in of unbalance torque.

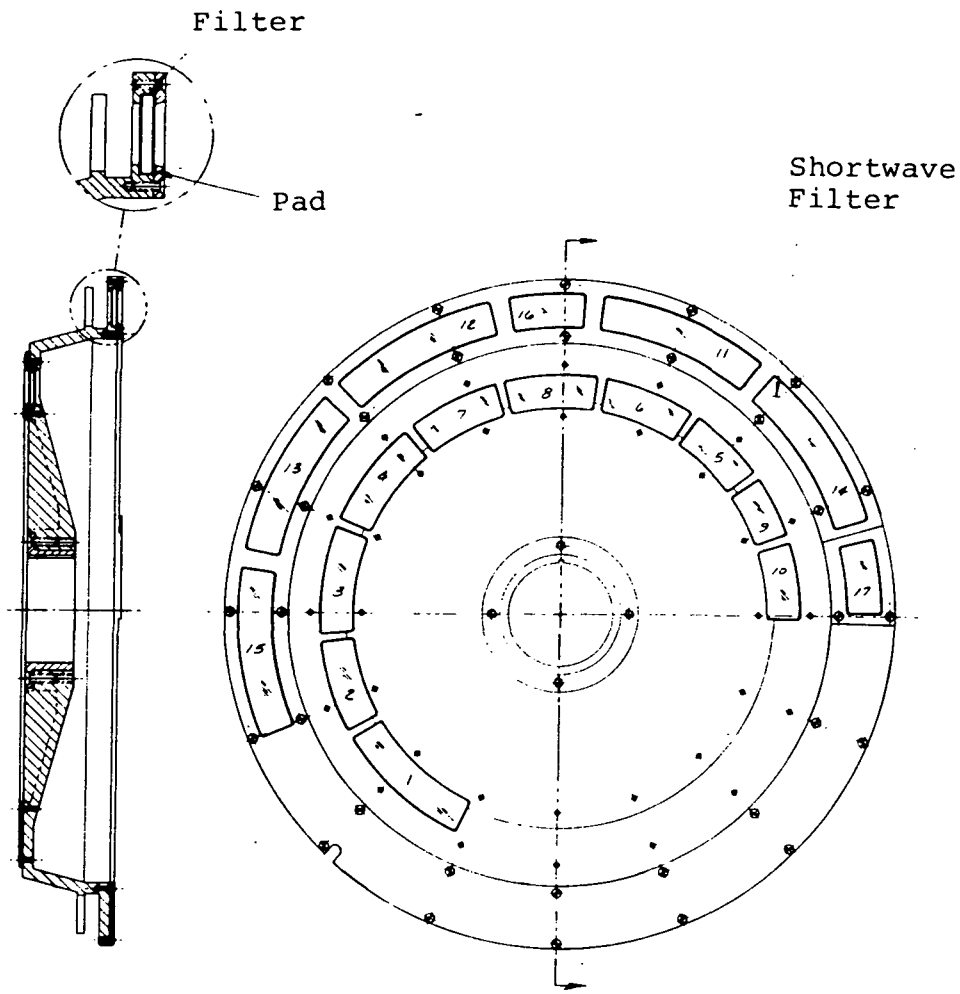


FIGURE 4.1-4 FILTER WHEEL ASSEMBLY

4.1.2 Spectral Filters

The filters that are clamped in the filter wheel are made of Germanium substrate and coated per ITT Specification No. 8117362-1. The detail description of the filters is contained in Drawing No. 8117353.

4.1.3 Drive Motor Assembly

The basic purpose of the drive motor assembly is to drive the filter wheel assembly and the longwave chopper at a constant speed.

4.1.3.1 Purpose

In meeting this purpose the drive motor is required to perform the following functions:

1) Mechanically mount and drive the filter wheel assembly at a constant speed of 564.97 rpm.

2) Mechanically mount and drive the longwave chopper assembly at six times the filter wheel speed, in an opposite direction, to the filter wheel.

3) Maintain angular momentum compensation to within contract specification.

Figure 4.1-5 is an enlarged view of the drive motor assembly illustrating the key components for this assembly. In meeting the above functions and purpose as defined for the drive motor there exists certain engineering data applicable to each of the basic components. Engineering data is presented in the following paragraphs for the basic motor drive components; the bearings, gears, materials, and motor.

4.1.3.2 Bearings

Tabulated below are the basic bearing shafts and bearing size used.

		Size
Rotor Bearing	.75 Dia	A539
Planet Bearing	.125 Dia	SR-2-6
Sun Bearing	.25 Dia	SR-188

Bearing size and type were selected based upon the following parameters, life electrohydrodynamic lubrication, lubrication, speed and bearing torque. Table 4.1-1 gives a basic summary of pertinent bearing data for the bearings used.

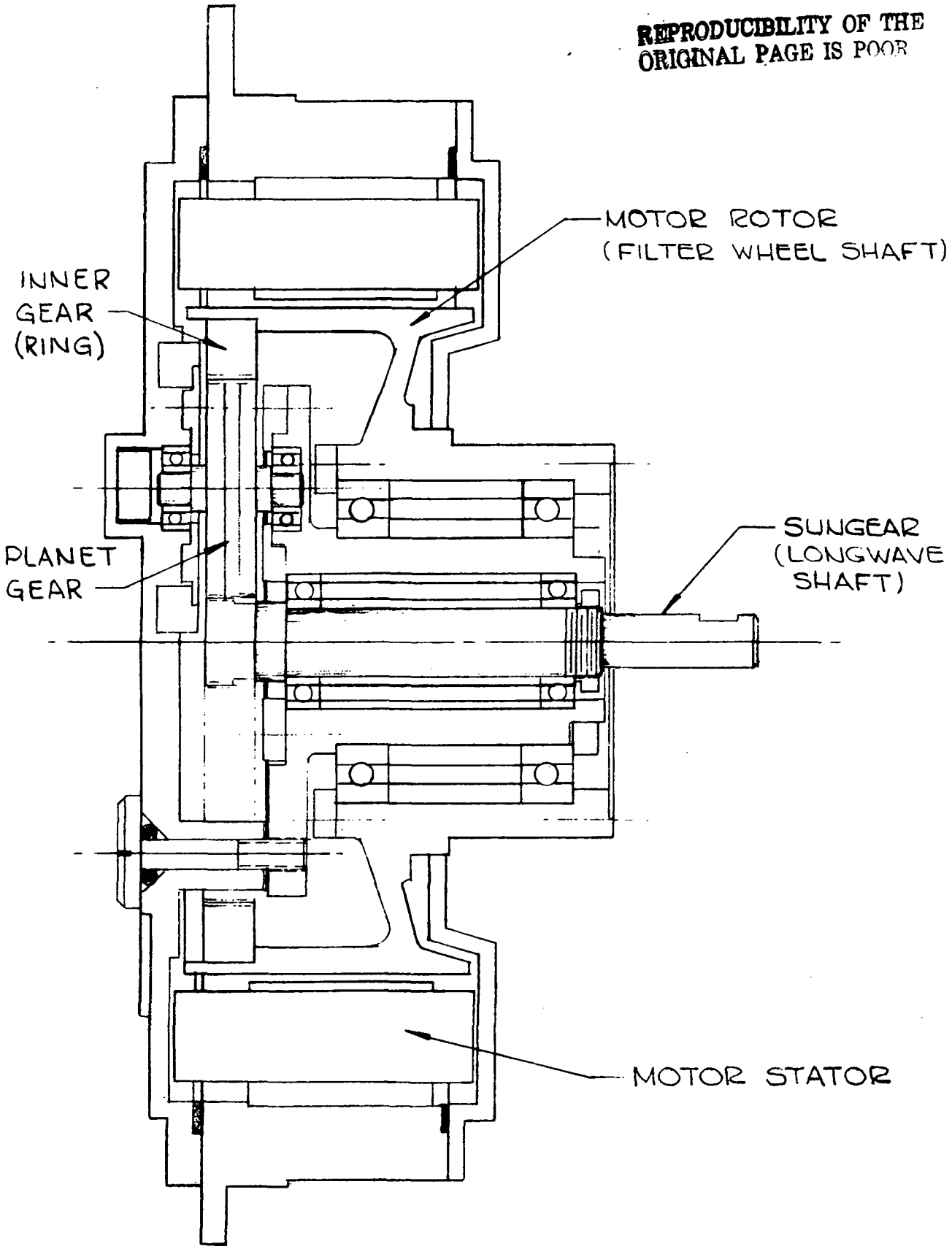


FIGURE 4.1-5 SECTION VIEW OF THE FILTER, CHOPPER DRIVE MOTOR ASSY

4.1.3.3 Gears

The gears used in the drive motor assembly consists of three fine pitch gears. The basic gear data for each gear is listed in Table 4.1-2.

4.1.3.4 Motor Material

The motor material is fabricated from 17-4 Ph stainless and 304 stainless. A temperature coefficient of expansion versus material was performed.

4.1.3.5 Motor

The drive system is driven by a 36 pole, 2 phase hysteresis synchronous a.c. motor. Basic engineering data is summarized in Table 4.1-3.

The motor torque characteristic is shown in Figure 4.1-6 where the increase in current is related to torque demand.

4.1.4 Longwave Chopper

The longwave chopper mounts to the high speed (x 6) drive shaft of the drive motor. The chopper rotates at 3380 rpm in opposite direction to filter wheel. The longwave chopper contains 16 symetrical tooth-space pairs which optically chops the longwave infrared signal at a frequency of approximately 904 Hz. The basic properties of the longwave chopper are listed in Table 4.1-4. A mass is added to the longwave chopper hub for moment of inertia control. The chopper is balanced with this mass in place.

4.1.5 Jitter Characteristic

As system tests reached the point of evaluation of system noise from the radiant channels it was observed that the velocity fluctuation of the filter wheel and choppers was having an effect on integration time period that was non-trivial. A program of analysis, definition, and reduction of these effects became very important in the continuation of system development.

Jitter was found to be predominantly related to the tooth to tooth coupling of the ring gear, planet, and sun gear. Energy applied to the ring gear was transmitted unevenly to the sun gear where a high inertial load from the longwave chopper blade caused a barrier to the energy. Some energy was absorbed in the chopper wheel as a velocity increase; remaining energy was reflected through the gear train, affecting the filter wheel velocity again. Other jitter sources studied included bearing uniformity and condition and the possibility of bearing swirl.

TABLE 4.1-1 SUMMARY OF BEARING DATA

NAME	TYPE	RUNNING TORQUE (oz-in)	SPEED (RPM)	DIA. OF BALLS (INCHES)	NUMBER OF BALLS PER BEARING
ROTOR BEARING	A539	.42	565	.125	14
PLANET BEARING	SR2-6	.013	1356	.0625	7
SUN BEARING	SR1-88	.133	3380	.0625	11

NOTE: ALL BEARINGS LUBED WITH APIEZON C OIL

TABLE 4.1-2 BASIC GEAR DATA

- QUALITY 13-D - 80 PITCH -20° PA
- AGMA SPEC = .0004 TCE
  .0002 T-TE
- RING GEAR (INNER) 156 TEETH
- PLANET (EXT) 65 TEETH
- SUN (EXT) 26 TEETH

- RING GEAR P.D. = 1.950 DIA
- PLANET P.D. = .8125 DIA
- SUN P.D. = .325 DIA

- MATERIAL - 17-4-PH
  R_C = 26-32
  32-38

- LUBRICATION - APEIZON C WITH LITHIUM STEARATE FILLER TO PROVIDE NON-TRACKING LUBRICANT

TABLE 4.1-3 F/C MOTOR DRIVE

MOTOR PERFORMANCE DATA (S/N - 005)

NORMAL OPERATING MODE (18V)

POWER	= 5.6 WATTS
SYNCH TORQUE	= 3.7 OZ. IN.
STALL TORQUE	= 2.2 OZ. IN.
CURRENT	= .275 AMP.

HIGH POWER MODE (24V)

POWER	= 8.64 WATTS
SYNCH TORQUE	= 5.2 OZ. IN.
STALL TORQUE	= 4.2 OZ. IN.

MOTOR INERTIA .022 OZ. IN. SEC^2

TABLE 4.1-4 LONGWAVE CHOPPER PROPERTIES

INERTIA, CHOPPER BLADE	.0436 oz in sec^2
INERTIA, COMPENSATION	.0374 oz in sec^2
ROTATIONAL SPEED	3380 rpm
KINETIC ENERGY	319.0 in#
BASE MATERIAL	ALUM 6061-T6
WEIGHT	.34 POUNDS
SURFACE FINISH	GOLD PLATING
DETECTOR SIDE	3M -401-
OUTSIDE DIA.	6.1 INCH DIA.

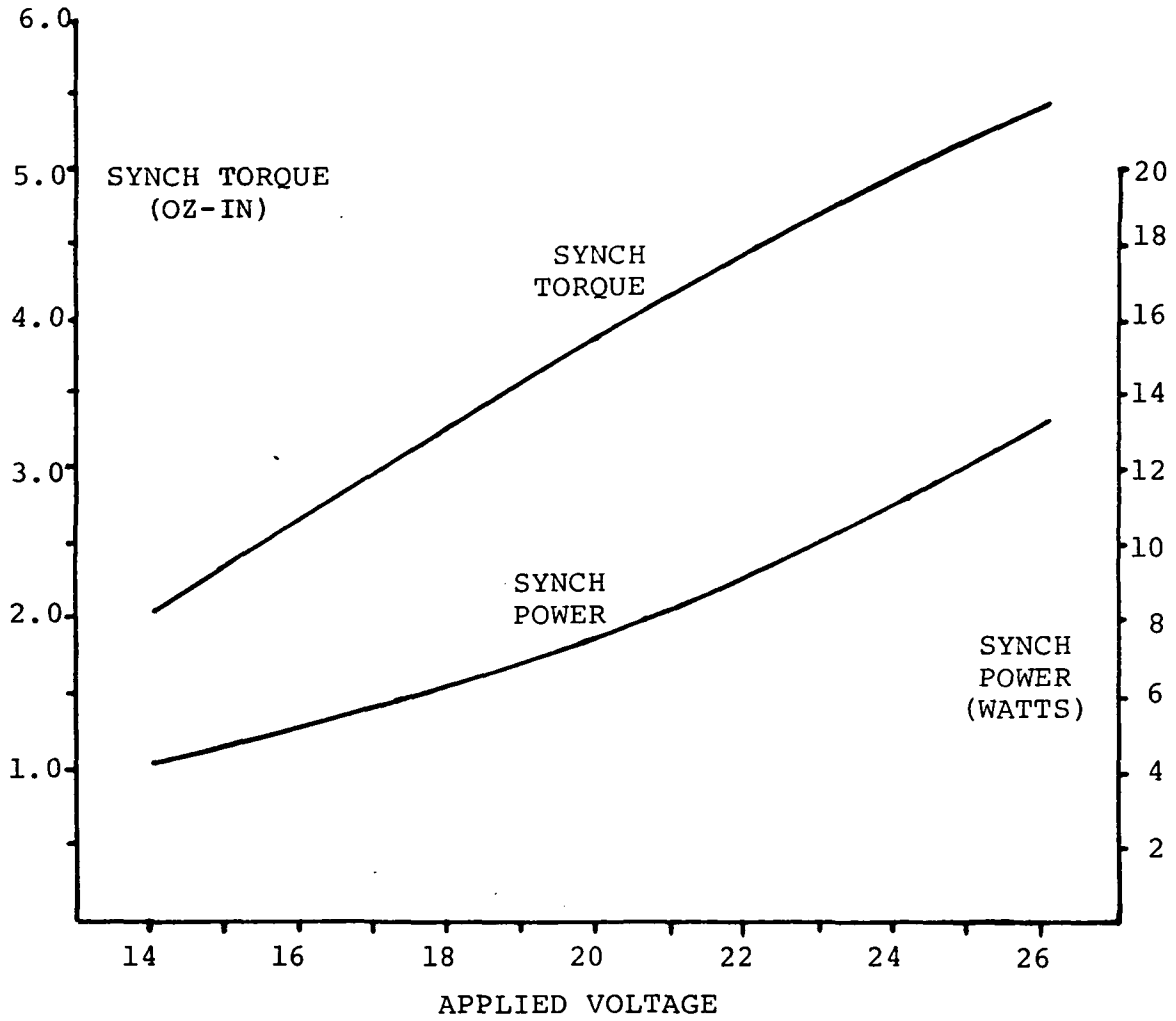


FIGURE 4.1-6 F/C MOTOR CHARACTERISTICS

Gear quality and run-in condition were reviewed after study of the data from the Engineering Model, where run-in had caused severe fritting of the gears but a relatively low jitter, probably because of a low run-out error. The protoflight and life test ring gears were fabricated slightly differently and had a measurable run-out of as much as .0015 inches in a cyclic pattern. Unfortunately, we did not have time to fabricate new ring gears. In order to reduce tooth to tooth errors we had special planet and sun gears fabricated and tested in the assembly. This improved the jitter significantly for a time, but after run-in the cyclic noise and higher jitter levels returned.

The final configuration included matched gear sets with a special planet gear having three gear sections. The center section mated the ring and sun gear while the other two sections were each connected to the center by a single turn spring. One section contacted the ring gear only, and the other contacted the sun gear. Experimentation with the degree of spring tension led to a selected spring tension that provided an anti-backlash action on each of the mating gears. This technique has proven fairly successful in reducing the jitter effect to near 50% of the worst case level; reducing the cyclic noise associated with the ring gear variation, and provides a consistent characteristic over an extended life period.

In addition to the use of the double anti-backlash gear we found that the use of kapton washers in the gear retainers and the use of a filler in the Apiezon C oil all helped reduce and maintain velocity uniformity.

Bearing studies were conducted by ITT and Draper Labs, with Draper assembling several bearing sets for the planet and sun gear that were to minimize retainer swirl. These bearings had slightly mismatched ball sizes. Tests on the completed system were inconclusive in establishing that swirl had been present or that jitter had been reduced by use of the special bearings.

Final system assembly of the protoflight had the anti-backlash gears with three teeth offset to provide a relatively low but definite holding force. The gears were lubricated with Apiezon C oil and the gear surfaces with an oil and filler combination using Lithium Stearate base compound. Tests on the life test unit and a tear down after several months operation indicated no hot spots and minimal wear. The life test motor assembly has operated over 3000 hours with no sign of failure.

4.2 Electrical Subsystem - Filter Wheel Drive

4.2.1 General

This independently commandable electrical subsystem contains two printed circuit boards primarily due to packaging

considerations, although a logical sectioning for testing purposes existed between the two-phase square wave generator that controls the motor speed and the switching regulator power static inverter which then directly drives the filter chopper assembly hysteresis synchronous drive motor.

4.2.1.1 Electrical Description

Figure 4.2-1 is a simplified schematic of the Filter Chopper Motor Drive two phase square wave generator. Figure 4.2-2 is the logic timing diagram for this circuitry. The timing originates from a gated astable multivibrator which free-runs at very nearly 400KHz and is completely synchronized to the S/C 400 KHz clock frequency when the Electronics Power is commanded ON (with the F/C Motor Power ON). This 400 KHz square wave is divided by 590 in a ripple counter to generate a 1.25 μs positive going pulse train having a constant periodicity of 1.475 ms. These pulses are divided again by four to obtain four phase symetrical square wave outputs, each with a period of exactly 5.9 ms. The square wave at pin Y precisely leads the square wave at 1) Pin S by $\pi/2$ radians, 2) Pin W by π radians and 3) Pin U by $3\pi/4$ radians. The 1.4725 ms pulse at A_2 - 10 is removed 1.25 μs prior to the point in time that flip-flop, E_1-1 (Q) and E_1-2 ($\bar{Q}$), is clocked to ensure that clocking of flip-flop B_1-1 (Q) and B_1-2 ($\bar{Q}$) is never inhibited.

These four square waves then go to the Filter Chopper Power Supply (in board location J401) shown in a simplified schematic form in Figure 4.2-3.

An examination of one of two identical bridge inverters (having complementary inputs at Pin W and U) shows how the motor drive operates. Assume Pin W is at -12 VDC and Pin U is at OV DC. Transister Q7 will be in saturation (a V_{CE} of nearly OVDC) with about 2.4 ma of base current. Since the collector of Q7 has a direct connection to the base of Q6, Q6 will saturate causing $-V_{OUT}$ to be connected to Pin R, the motor lead. The collector of Q7 will concurrently cause saturation of Q4 which pulls up Pin S, the other motor lead to nearly OVDC. The OVDC on the base of Q8 will in the same time interval cause transistors Q3 and Q5 to open (have virtually no collector current). When the signals reverse on the bases of Q7 and Q8, Q4 and Q6 open, then Q3 and Q5 close. This action impresses an AC square wave on the motor winding equal to twice the absolute value of V_{OUT} of the waveforms on the bases of either Q7 or Q8. The base input resistor dividers of both Q7 and Q8 (composed of a 5KΩ and 4KΩ resistor in series) ensures that the transistors of the bridge (Q3, Q4, Q5 and Q6) are operated in a break-before-make switching action. The bridge is opened for approximately 2 μs.

Two relays control this subsystem: 1) the F/C Motor

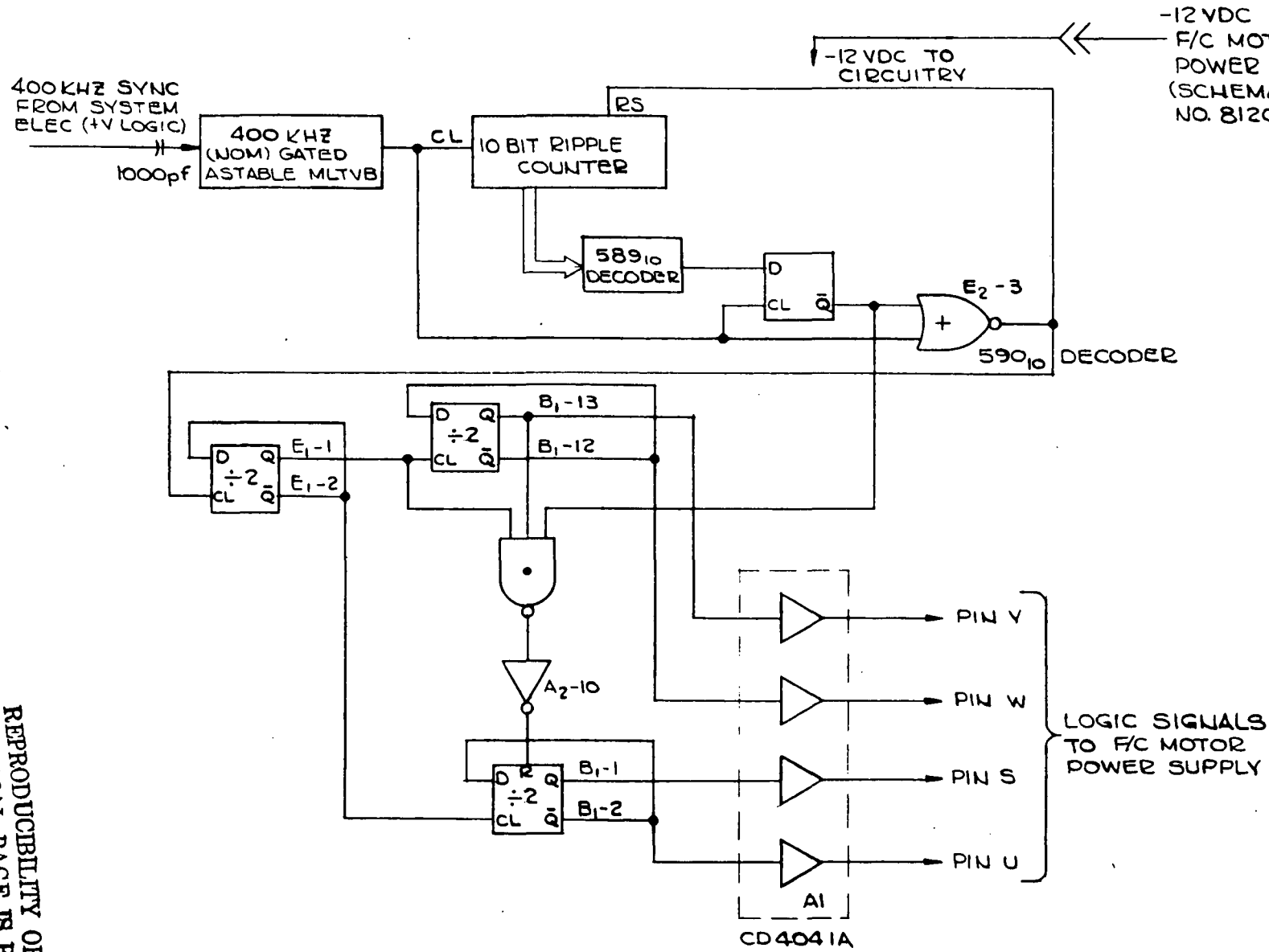
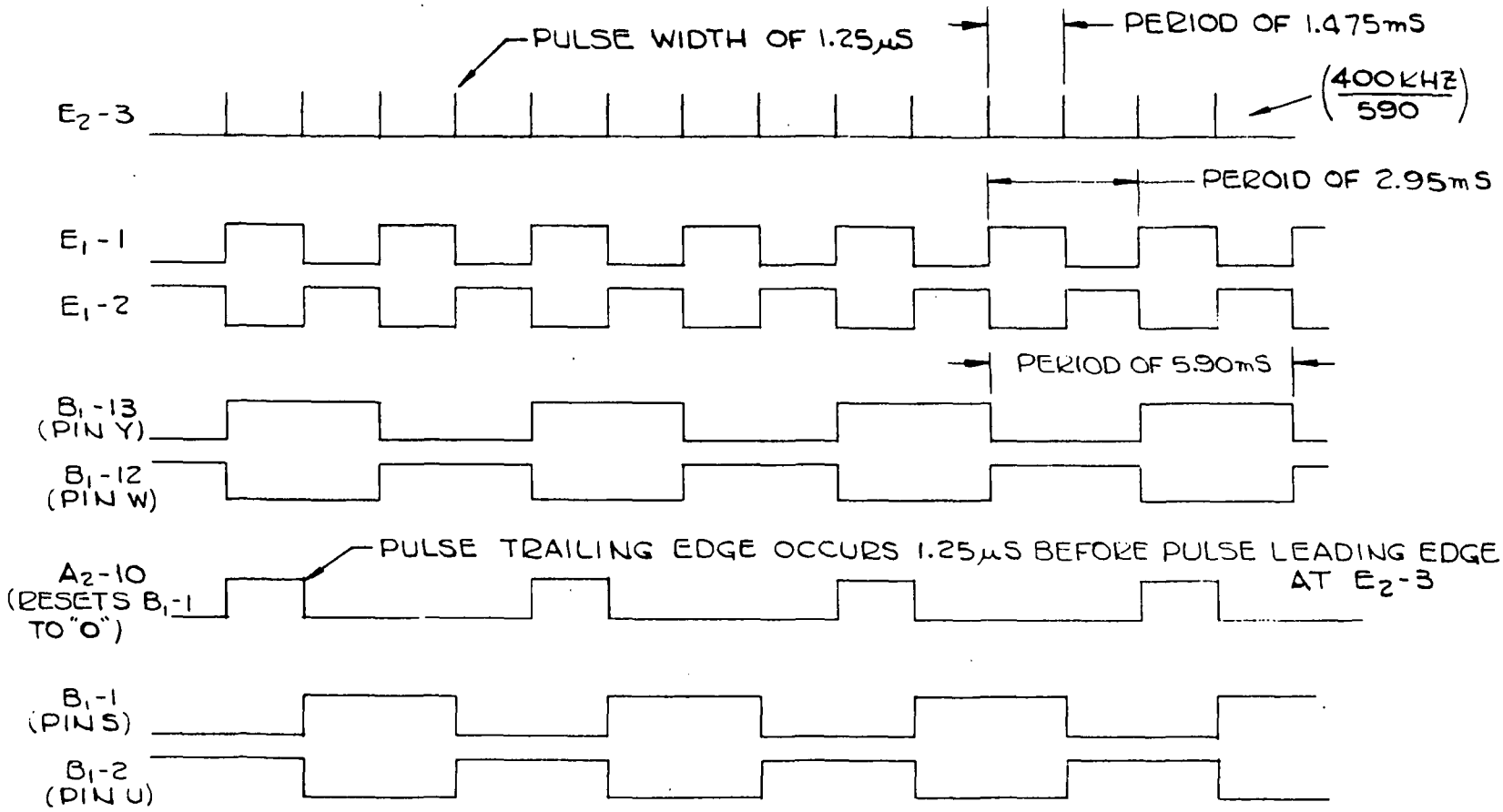


FIGURE 4.2-1 SIMPLIFIED SCHEMATIC OF THE FILTER CHOPPER MOTOR DRIVE SCHEMATIC NO. 8118515



RESET PULSE AT A_2-10 INSURES THAT SIGNAL ON PIN Y (B_1-13) LEADS SIGNAL ON PIN S (B_1-1) BY 90°. IN SAME MANNER PIN W ALLWAYS LEADS PIN U BY 90°.

FIGURE 4.2-2 LOGIC TIMING DIAGRAM OF FILTER CHOPPER MOTOR DRIVE ASSY

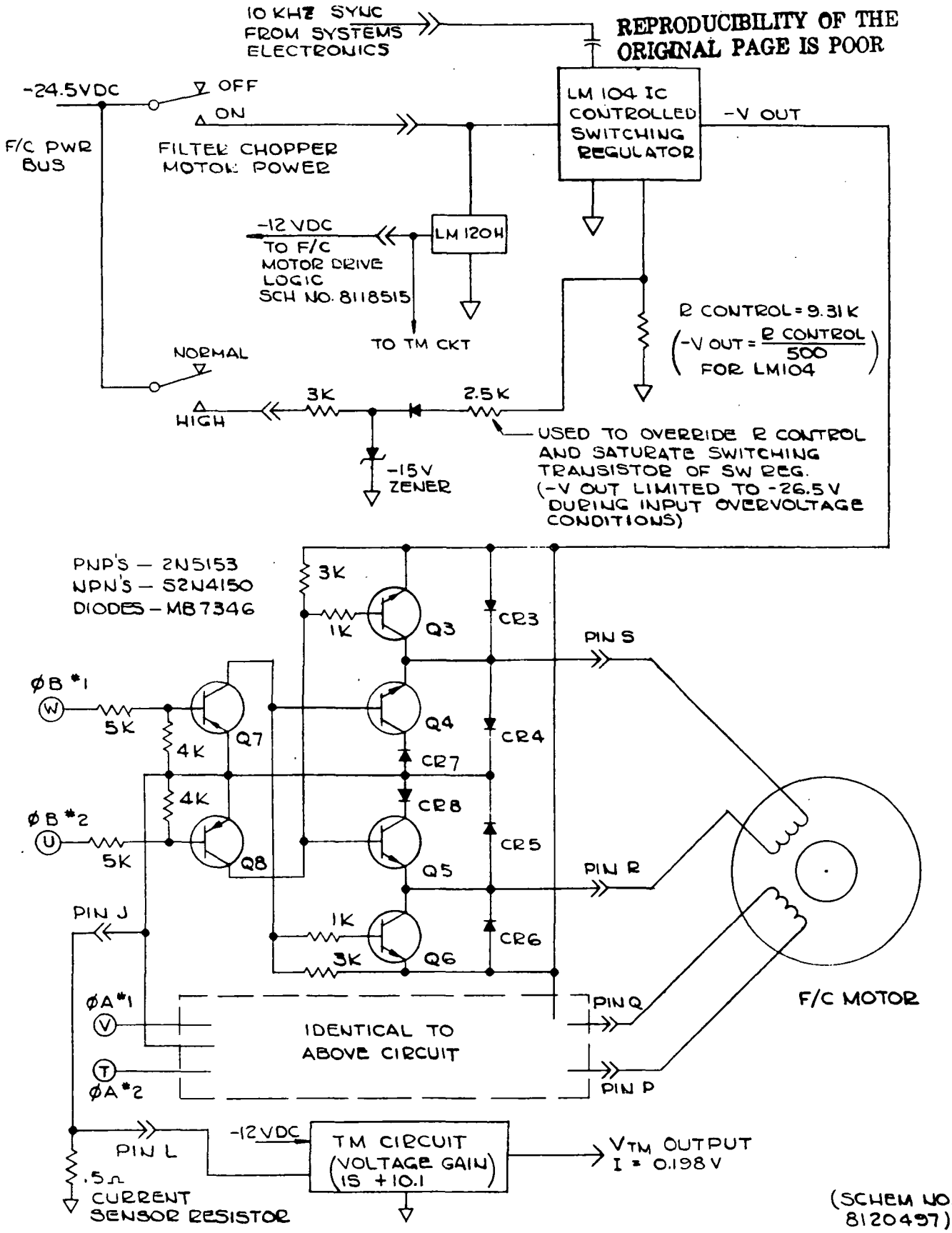


FIGURE 4.2-3 SIMPLIFIED SCHEMATIC OF F/C POWER SUPPLY

Power ON/OFF relay supplies or removes power to the phase generating logic and to the switching regulator input and 2) the F/C Motor Mode Normal/High relay which, in the "HIGH" command position, results in an override potential being applied to the R control used to set the regulator output voltage. This causes $-V_{OUT}$ to become virtually the bus input voltage.

An additional circuit on this subassembly, used to scale the motor current for the VIP Analog TM, measures the voltage drop across a 0.5 ohm current sensing resistor through which all the bridge and motor current must flow. This voltage is amplified with a voltage gain of +10.1 which results in an overall transfer function of: $I_m = 0.198\ V_{TM}$.

The motor is a 36 pole hysteresis synchronous type which must rotate with a period of exactly 106.2 ms. (The reason for the preciseness of this time is explained in Section 8.2).

The period of one rotation of this motor type is defined as one-half the number of poles times the period of the electrical drive period. Therefore the electrical drive period is 106.2ms/18 or 5.9 ms. Since the period of one cycle of the 400KHz clock is 2.5 μs, the total division required is $\frac{5.9 \times 10^{-3}}{2.5 \times 10^{-6}}$ or 2360 as can be seen in Figure 4.2-2.

4.3 Electrical Subsystem - Filter Wheel Assembly Proportional Heater

4.3.1 General

The F/C Housing Heater is an independently commandable proportional heater controller which obtains its input power from the -24.5 VDC F/C Power Buss within the HIRS.

4.3.2 Electrical Description

This controller consists of a true differential input instrumentation amplifier that amplifies (with a closed loop gain of 1,001) the difference between the voltages appearing at two resistor dividers excited by the same -12 VDC linear I.C. regulator (a LM120H). The output voltage e_o of the instrumentation amplifier then becomes the control voltage for a LM104 I.C. regulator operating in the switching mode. The LM104 contains an internally set non-inverting voltage gain of two. A simplified circuit diagram is shown in Figure 4.3-1.

4.3.2.1 Circuit Analysis

An analysis of the circuit of Figure 4.3-1 is shown below:

$R_1 = R_4 = 1$ M ohm

$R_2 = R_3 = 1$K ohm

$E_{OUT} = 2e_o$

Therefore,

$$E_{OUT} = 2 (V_1 - V_2) \left(1 + \frac{10^6}{10^3}\right)$$

$$E_{OUT} = 2.002 \times 10^3 \quad (V_1 - V_2)$$

$$V_1 = \frac{ER_o}{2 R_o} = \frac{E}{2} \quad \text{and} \quad V_2 = \frac{ER_o \ (1 + \alpha)}{R_o + R_o \ (1 + \alpha)} = \frac{E(1 + \alpha)}{2 + \alpha}$$

α = 0.0035 (ΔT) for ΔT values in the range of 25°C to 35°C

Therefore:

$$E_{OUT} = 2.002 \times 10^3 \left[\frac{E}{2} - \frac{E \ (1 + \alpha)}{2 + \alpha} \right]$$

Since $\frac{E}{2} \doteq \frac{E}{2 + \alpha}$

$$E_{OUT} = 1.001 \times 10^3 \left(\frac{-E \ \alpha}{2 + \alpha} \right)$$

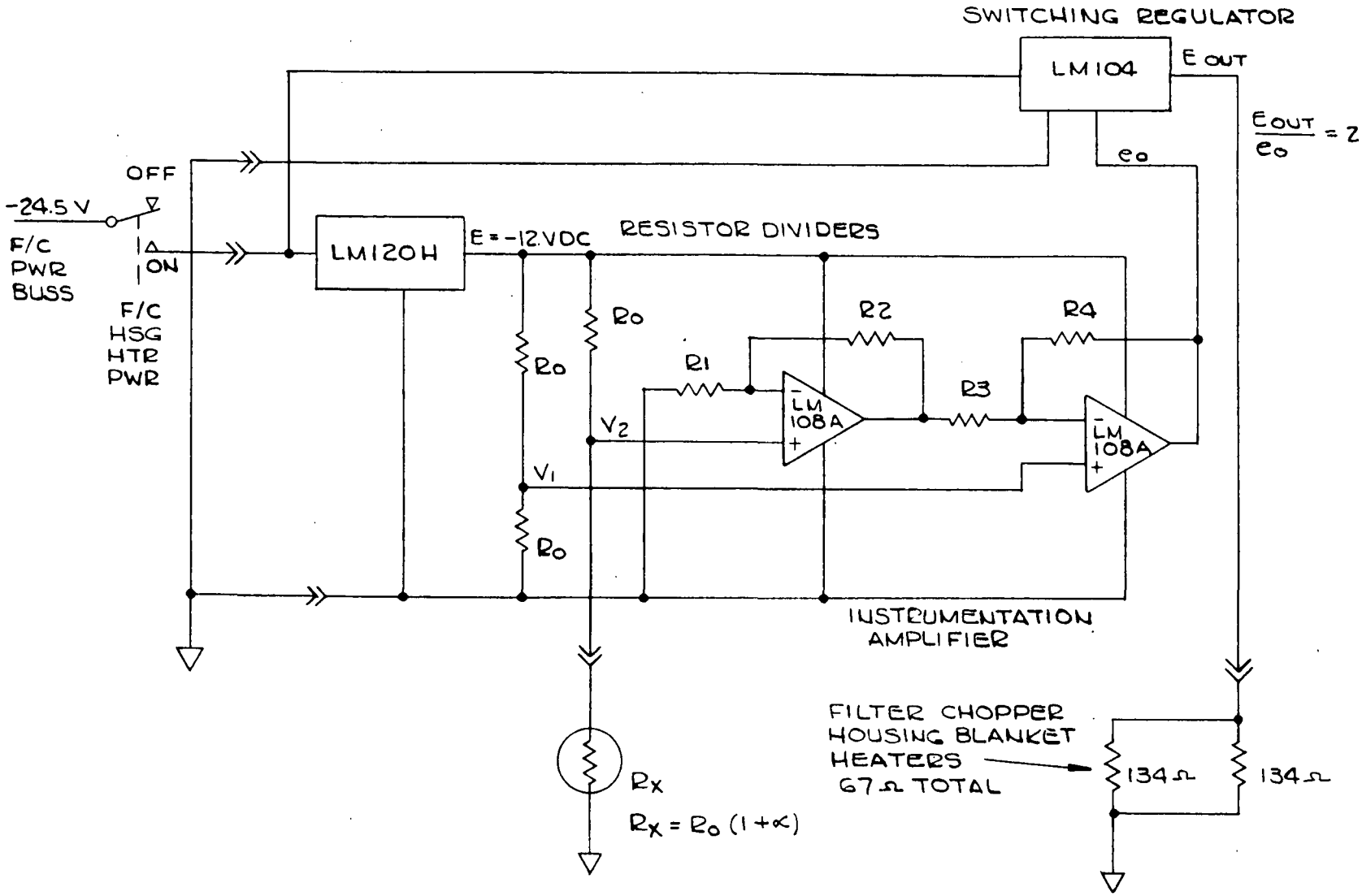


FIGURE 4.3-1 SIMPLIFIED SCHEMATIC OF F/C HOUSING HEATER POWER

Substituting $0.0035\ (T-T_o)$ for α and -12 VDC for E;

$$\Delta E_{OUT} = \frac{12\ (0.0035)\ (1.001 \times 10^3)\ \ (\Delta T)}{2 + 0.0035\ \ (\Delta T)}$$

$$= \frac{42.04\ (T - 30.5^oC)}{2 + 0.0035\ (\Delta T)}$$

Since $0.0035\ (\Delta T) << 2$ for small values of ΔT

$$E_{OUT} \doteq \frac{42.04\ (\Delta T)}{2}$$

Therefore $E \doteq 21\ (\Delta T)$

If $\Delta T = -1^oC$; $E = -21V$

Since $\Delta T = T - T_o$ for $T_o = 30.5^oC$

4.3.2.2 Circuit Performance

Circuit performance (stability) of this controller is almost totally dependent upon the stability of the resistors (R_o) used in the voltage dividers ahead of the instrumentation amplifier. The effects of amplifier and switching regulator drift is negligible as is the absolute value of the -12 VDC (LM120H output) used on the dividers (within reason), as these components are within the feedback loop.

A plot of this voltage and power to the 67 ohm heater vs. temperature is shown in Figure 4.3-2.

From this data the equation of the voltage plot between 29.5^oC and 30.5^oC can be shown to be $V = 21T-643.5$ where T is in degrees centigrade. Power to the heater is $\frac{V^2}{R_{HTR}}$, with a heater resistance of 67 ohms. Heater power is therefore $P_{(\text{in watts})} = 6.58T^2 - 403.4T + 6180$. Differentiating this equation will determine the slope of the power versus temperature $\frac{(\Delta P)}{(\Delta T)}$ which is the best method for characterizing the circuit.

$$\frac{dP}{dT} = 12.16T - 403.4$$

The heat input to the F/C housing necessary to maintain a given temperature has been calculated to be approximately 250 mw per ^oC difference between the baseplate and the F/C housing. Therefore, for a baseplate temperature of 22^oC, about 2 watts will be necessary to maintain the F/C housing at 30.1^oC

(from Figure 4.3-2). The slope $\frac{dP}{dT}$ at 30.1°C is 7.3 watts/°C. Dividing this slope of 7.3 watts/°C by the slope of the calculated power versus temperature characteristics of the F/C housing to baseplate thermal coupling of 0.25 watts/°C, yields an overall closed loop gain (A_{ce}) of this circuit of 29.2. Therefore, since the housing baseplate thermal sensitivity is reduced by $\frac{1}{A_{ce}}$ a one degree change of baseplate temperature about +22°C (± 0.5°C) will cause only a ±0.017°C change in the F/C housing temperature. The closed loop gain at lower baseplate temperatures is even higher. As an example, a baseplate temperature of +10°C yields a closed loop gain of 47.6 and likewise a ±0.5°C change about this baseplate temperature causes only a ±0.01°C change in the F/C housing temperature.

C-2

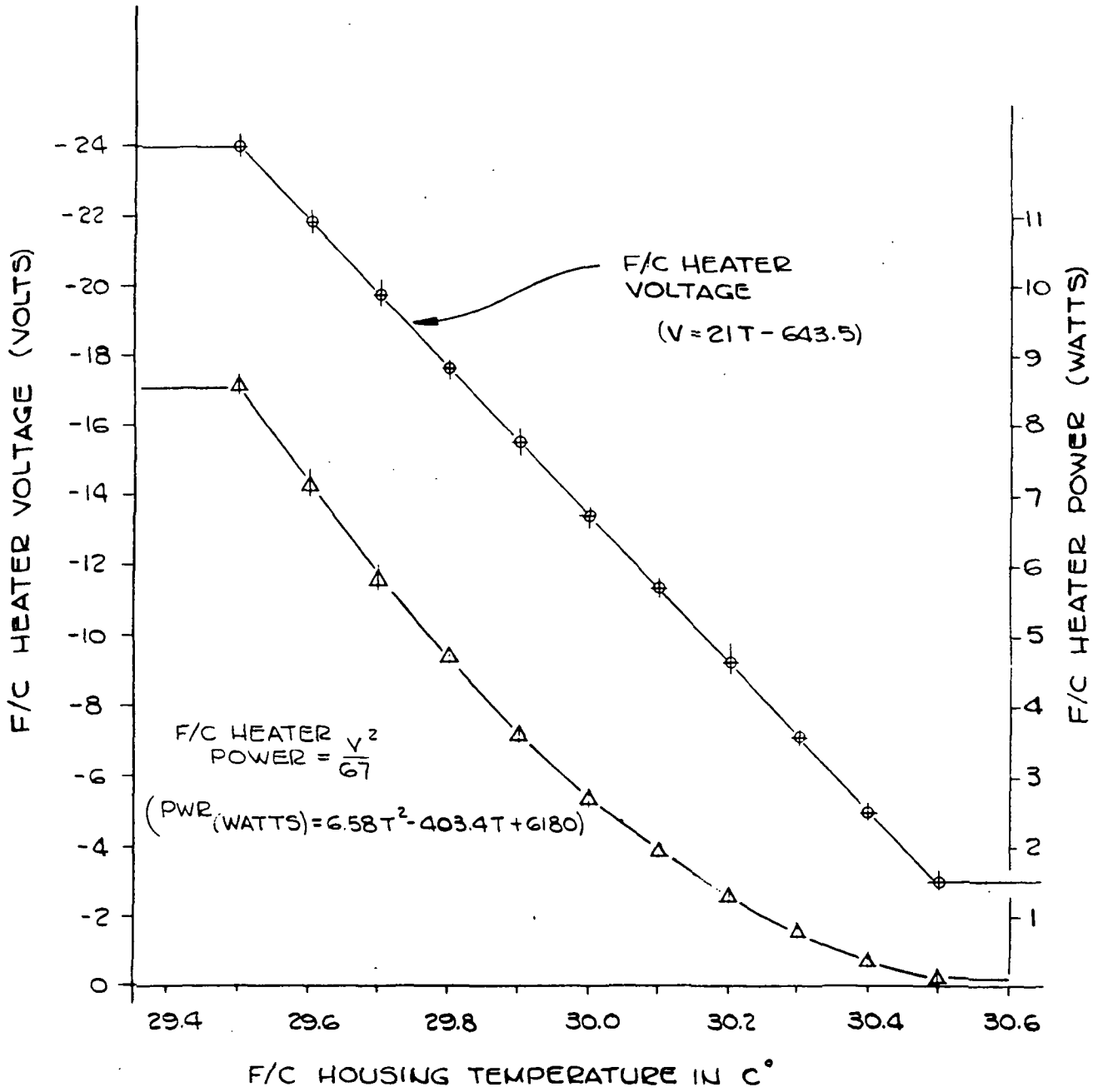


FIGURE 4.3-2 F/C HOUSING POWER INPUT

5.0 OPTICS

5.1 System Description

The HIRS optical system transfers the received energy in seventeen spectral channels onto a pair of cooled IR detectors and a visible detector. The design is of classic radiometric philosophy, with the field imaged on the field stops and the system aperture reimaged on the detectors. Spectral channels are selected by a combination of dichroic beam splitters and spectral bandpass filters. The general layout is shown in Figures 5.1-1 and 5.1-2.

The scan mirror which redirects the source of energy into the telescope is made of beryllium with aluminum and silicon monoxide overcoating. The entrance aperture (5.90 inches) of the system is defined by an edge just in front of the secondary mirror. The telescope is a full Cassegrain reflecting system with a 10.377 inch effective focal length producing an f/1.76 system. The parabolic primary mirror has a focal length of 4.27 inches, or f/0.72, and secondary obscuration is 3.00 inch diameter. Primary and secondary mirrors have cervit substrates for thermal stability and are aluminum coated with a SiO overcoating. The germanium substrate beamsplitter located at the center of the primary mirror reflects the shortwave band and transmits the longwave band. A folding mirror reflects the longwave band so that both bands are directed to the filter/chopper and field stops. The field stops are 0.262 inches in diameter to define a 1.5 degree field of view. Figure 5.1-3 shows the main optic block. Note the thin telescope section and the placement of the dichroic beamsplitters and relay optics to allow the filter wheel to rotate between the field stops and relay.

Both beams are chopped by the filter chopper wheel before reaching the field stops. The longwave (LW) chopper wheel is not fixed to the filter wheel but is driven by the same motor producing a chopping rate of 904 Hz. The shortwave (SW) chopper is fixed to the filter wheel in front of the SW filters. The layout of the filters on the filter wheel is shown in Figure 5.1-4. The optical properties of each filter is shown in Table 5.1-1. The filter wheel and longwave chopper are shown in Figure 5.1-5.

The relay optics transfer the radiation passed through the field stop and filters to the detectors. Visible light is passed by a dichroic beamsplitter in the SW channel and is transferred to the visible detector. The two IR channels are transferred to the sensors by radiometric type imaging of the entrance aperture on the detector. The SW window which is on the cone of

the cooler has a special shortwave pass filter on it to increase the sensitivity of the SW detector. LW and SW aplanats are used to decrease the linear size of the detectors by a factor of four.

The optical transmissions of each component is shown in Figures 5.1-6 through 5.1-12. Most of these transmissions were made on flat witness samples that were coated at the same time as the actual optical element was coated. This was done since most spectrometers are incapable of measuring transmission for a curved element. The total transmission for each channel is shown in Table 5.1-2. A summary of all optic element characteristics are given earlier in Table 2.2-1 where system performance was estimated.

5.2 System Characteristics and Test Results

The HIRS optical system was recognized as a difficult design and development program with a number of significant restrictions and limitations. The design selected early in the program proved successful within certain limits. In particular, the high efficiency telescope requirement and restricted space resulted in a difficult secondary mirror fabrication task that delayed delivery of the optics and a reduced test and evaluation effort on the engineering model, but met the design requirements when delivered. Volume restrictions within the instrument required optic elements to be used at their full aperture, with some loss in efficiency, and the necessary interfaces of field stops, filter wheel, relay and cooled detectors limited the capability of simple alignment and test methods. We found that the registration of the spectral bands was limited by the physical features of the parts and not simply by the placement of field stop and detector. Much time was spent in the optimizing of cooler position and field stops to make up for the fact that the individual detectors could not be moved relative to each other.

The specially purchased narrow band filters were within spectral tolerances and transmission specifications. One problem arose in the use of Channel 13 filters where two of them exhibited high reflectance out of band, causing the detector to see a high and uneven thermal input. Selection of filters reduced the problem but left a signal baseline shift that causes some deviations in the output signal. The residual signal is a constant that is inherent in all data and does not affect system quality significantly.

The loss of field of view became a serious problem. The system had been designed for the field stop to completely define the field of view and the registration between bands. Unfortunately, this was not the case. Fields of view of 1.24^{o}

were measured, rather than 1.5°. The major cause of the discrepancy was determined to be the antireflection (AR) coating on the outer radius of the aplanat. The aplanats are coated by a point evaporation source in front of the aplanat, so that points away from the center of the aplanat have a thinner coating than at the center. The effect of this was probably to turn the AR coating into a reflective coating near the edge of the coating. The positions and angles at which rays strike the aplanats are shown in Figure 5.2-1.

Examining the optical layout it would be expected that the FOV would not be affected at this point in the system since the aperture stop is focused onto the detector. After careful study with a computer it was found that this coating can affect the FOV. From Figure 5.2-1 it can be seen that the rays from the edge of the field of view are farther from the center of the aplanat than rays from the center of the field of view and therefore are affected more by the spectral runoff of the coating. Below are listed several indications that the aplanat coating was the major problem for the FOV.

1) The visible channel had a 1.4° FOV before being restricted to match the IR FOV. This indicated that at least 1.4° was getting through the field stop.

2) An uncoated aplanat with a SW detector has approximately a 1.4° FOV.

3) The calculation of the background flux falling on the SW detector with a coated aplanat indicated that the background flux being collected was from a 1.2° equivalent FOV.

The effect of this was that the optimum FOV and registration could not be obtained. The results of the measurements is shown in Figure 5.2-2. These measurements were made by taking readings at one hundred points within the FOV and computing the effective FOV as the circle containing the total of the integrated flux using the peak signal as unity. The registration of bands is computed by finding the centroid for the one hundred points.

Optic system test results given above are for the system in full operating condition. In addition to system tests, the individual telescope and relay assemblies were tested at time of delivery, for field stop measurements, transmittance and reflectance of all optic elements, alignment, vignetting, spatial resolution and encircled energy. Each of the optic assemblies completed these tests successfully. During system tests it was recognized that improved techniques using the cooled detectors and computer aided data analysis would be required to fully establish the registration and field characteristics of every channel.

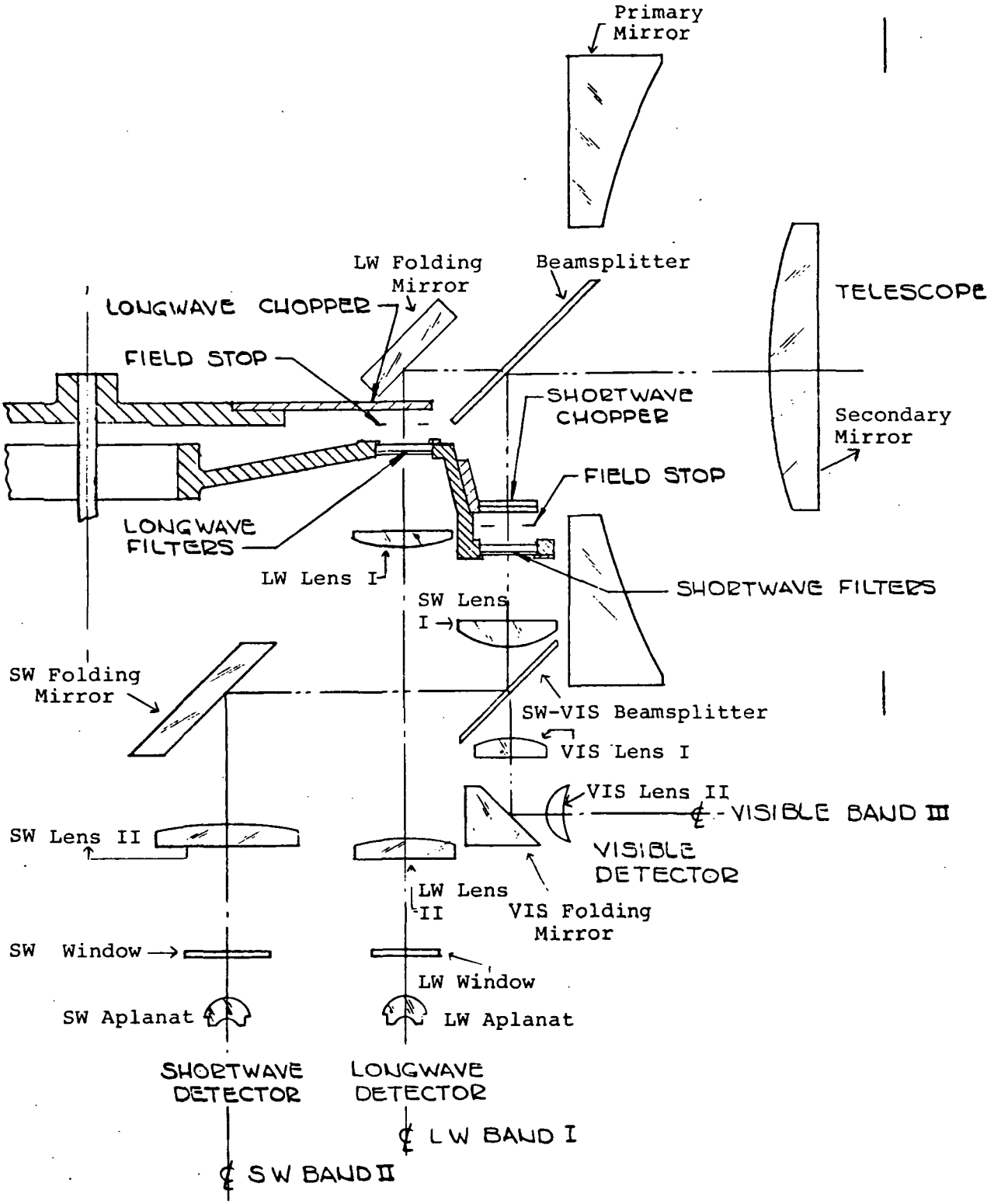
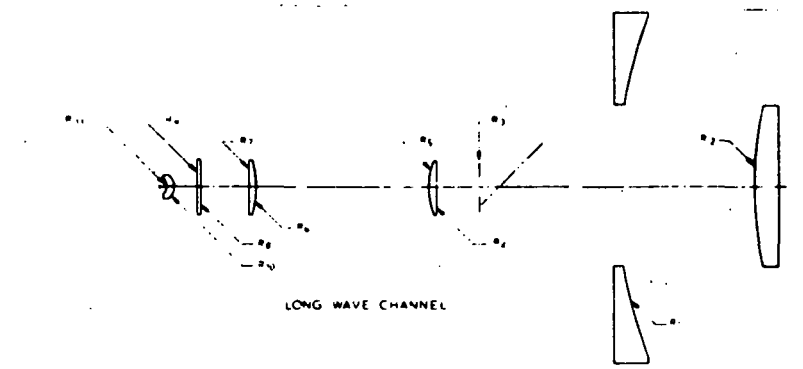


FIGURE 5.1-1 HIRS OPTICAL LAYOUT

SURFACE NO.	RADIUS (INCHES)	DISTANCE (INCHES)	MATERIAL
1	5.9055	-1.726	Reflection (Parabolic)
2	3.5501	4.160	Reflection (Hyperbolic)
3	-	.950	Air (Stop)
4	58.335	.197	Irtran 6
5	-1.404	2.850	Air
6	1.807	.180	Irtran 4
7	14.629	.838	Air
8	-	.060	Irtran 4
9	-	.530	Air
10	0.2362	.199	Germanium
11	0.1228	.065	Air to Detector
12	-	.950	Air (Stop)
13	-39.757	.276	Sapphire
14	-.749	4.397	Air
15	3.215	.230	Germanium
16	11.800	.963	Air
17	-5.517	.024	Sapphire
18	5.517	.444	Air
19	0.2308	0.184	Germanium
20	0.1256	.065	Air to Detector



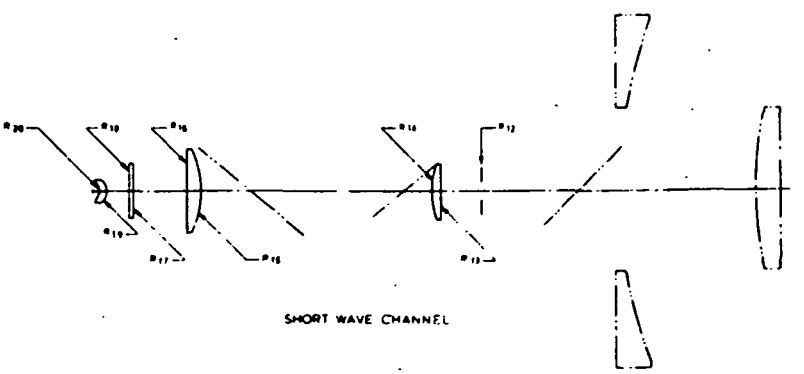


FIGURE 5.1-2 OPTICAL SCHEMATIC

a. Telescope

b. Relay and Dichroic Assy

FIGURE 5.1-3 TELESCOPE AND RELAY OPTICS

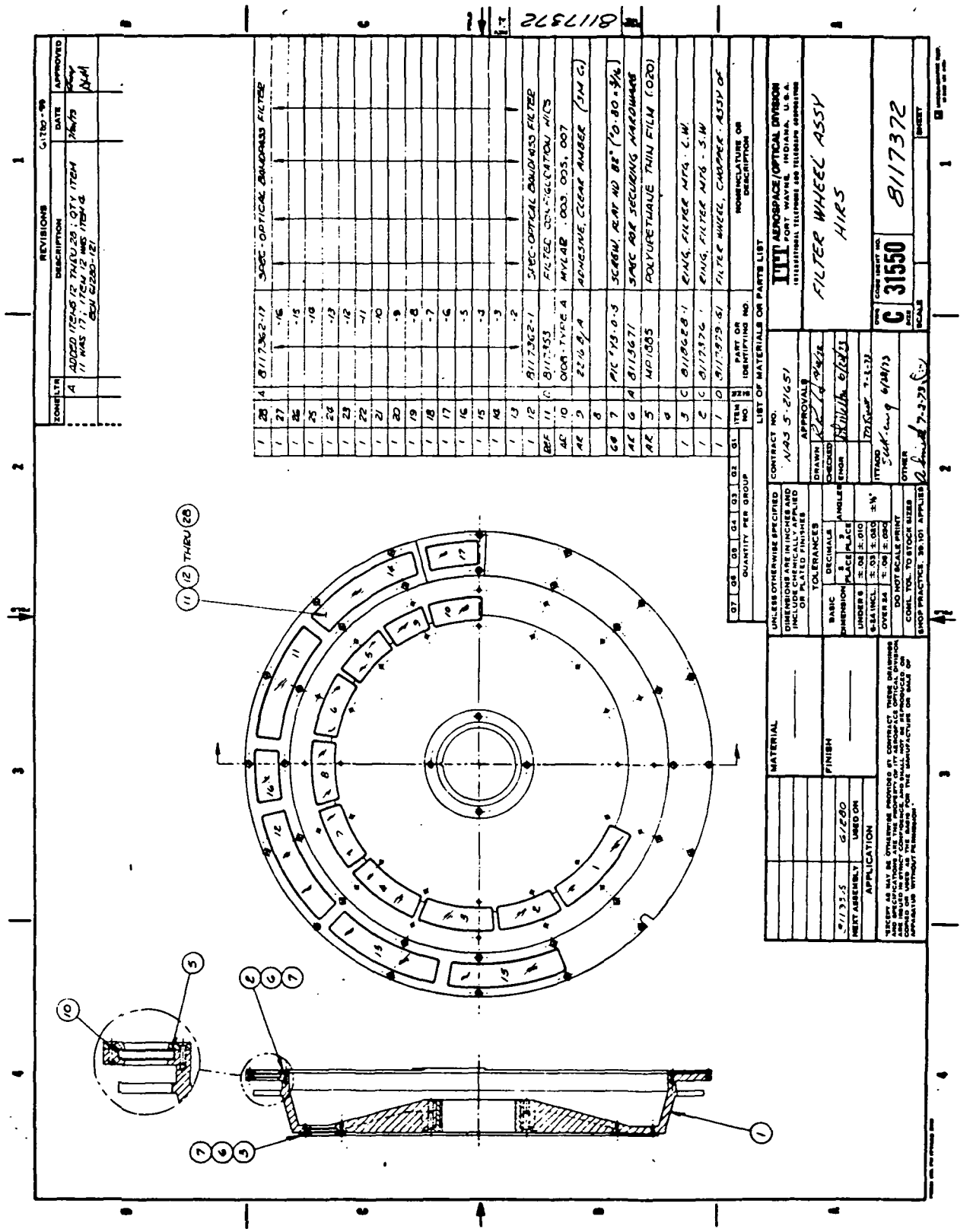
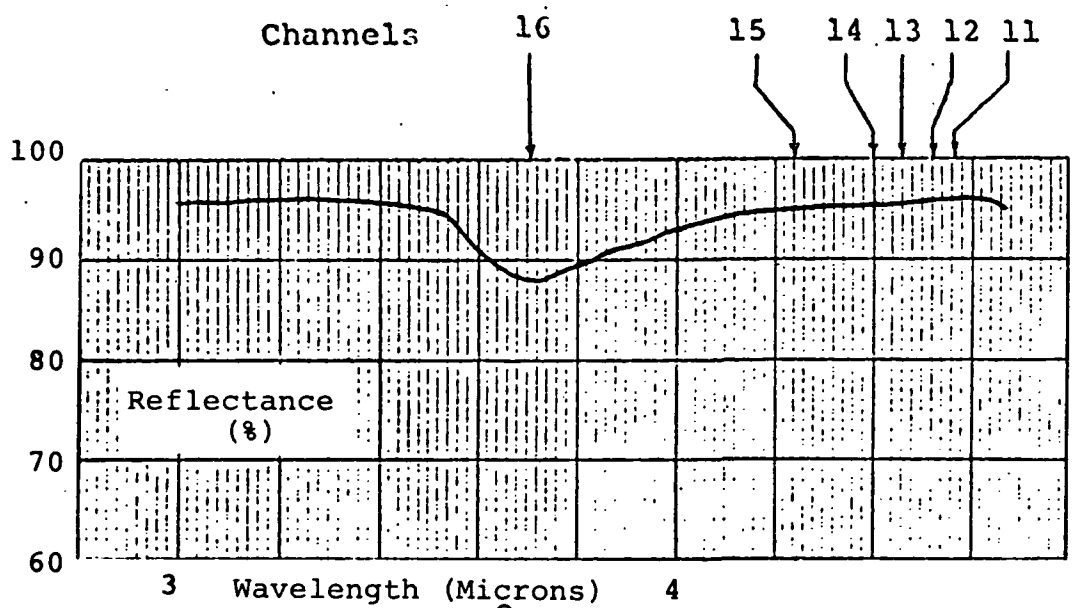


FIGURE 5.1-4 FILTER WHEEL ASSEMBLY

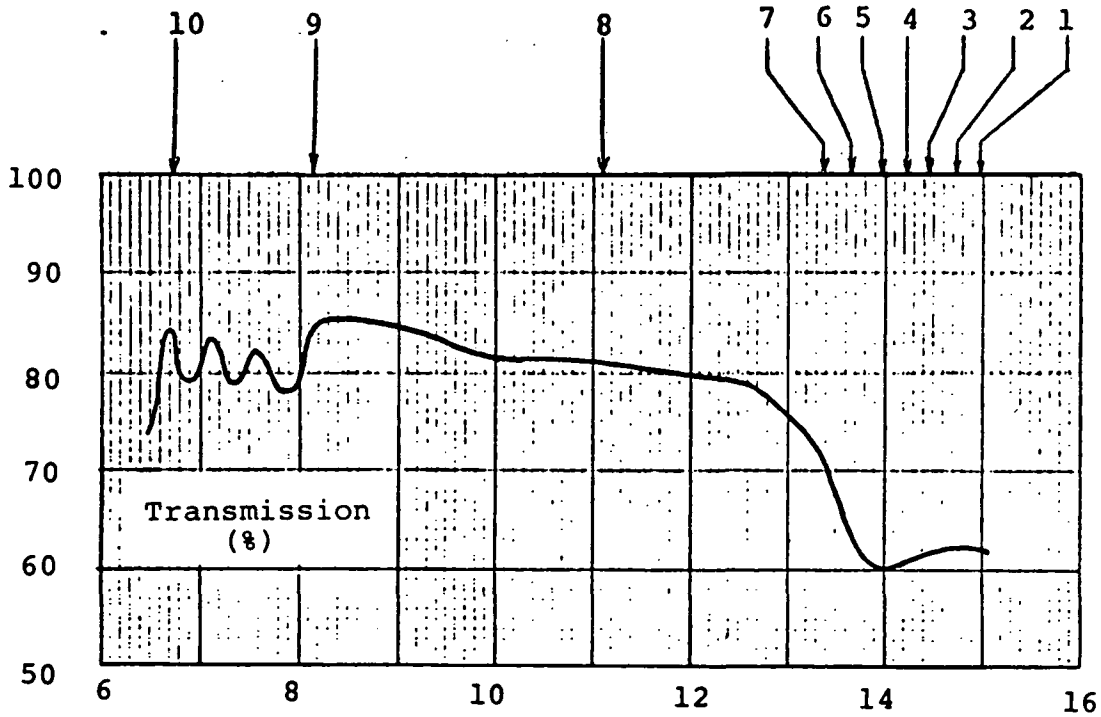
TABLE 5.1-1 BANDPASS/SPECTRAL DATA SUMMARY SHEET (Protoflight)

Filter Channel Set	CM-1 Center Freq.	CM-1 Half Bandwidth	CM-1 Effective Bandwidth	CM-1 1.0%T-ABS Bandwidth	CM-1 0.1%-ABS Bandwidth	Peak Transmission	CM-1 HBW Centering	Uniformity	Leaks	* Temperature Shift
1 Proto	669.1	2.8	4.2	17.3	30.6	37.6%	-0.1	OK	2400-588 OK	OK
2 Flight-2	678.8	13.7	13.6	26.3	37.2	59.9	0	OK	2350-588 OK	OK
3 Proto.	690.1	12.6	12.3	28.0	41.2	64.7	-0.2	OK	2350-588 OK	OK
4 Flight-1	701.6	15.9	16.1	36.8	52.8	70.3	+0.2	OK	2300-588 OK	OK
5 Flight-1	716.5	17.5	18.1	37.4	55.7	63.3	+0.1	OK	2500-588 OK	OK
6 Flight-1	732.3	17.6	17.9	39.2	59.4	63.7	-0.2	OK	2500-588 OK	OK
7 Proto.	749.1	18.4	19.3	38.6	60.2	58.2	0	OK	2500-588 OK	OK
8 Flight-2	899.6	34.6	31.7	59.3	79.5	59.0	-0.2	OK	2500-588 OK	OK
9 Flight-1	1228.2	63.4	57.1	90.5	111.1	70.3	-2.7	OK	2500-588 OK	OK
10. Flight-2	1494.9	87.6	79.4	150.4	192.1	68.7	+0.2	OK	2500-588 OK	OK
11 Flight-1	2190.8	20.6	20.7	44.7	67.3	54.7	+0.4	OK	6250-1755 OK	OK
12 Proto.	2211.9	22.5	23.0	46.7	71.1	60.7	-0.3	OK	6250-1755 OK	OK
13 Flight-1	2244.2	21.6	21.6	41.0	62.4	53.7	+0.3	OK	6250-1755 OK	OK
14 Flight-1	2274.5	35.2	35.0	75.5	121.0	54.3	+0.6	OK	6250-1755 OK	OK
15 Flight-1	2357.6	23.0	23.0	46.8	73.0	68.4	+0.1	OK	6250-1755 OK	OK
16 Proto.	2692.4	296.9	293.5	474.9	707.1	89.0	-3.4	OK	6250-1755 OK	OK
17 Proto.	14,443	892.2	N/A	N/A	N/A	88.3	N/A	OK	OK	N/A

FIGURE 5.1-5 FILTER WHEEL AND LONG WAVE CHOPPER



a) Reflectance of 60° Incidence Angle



b) Transmission at 60° Incidence Angle

FIGURE 5.1-6 BEAMSPLITTER TRANSMISSION AND REFLECTANCE

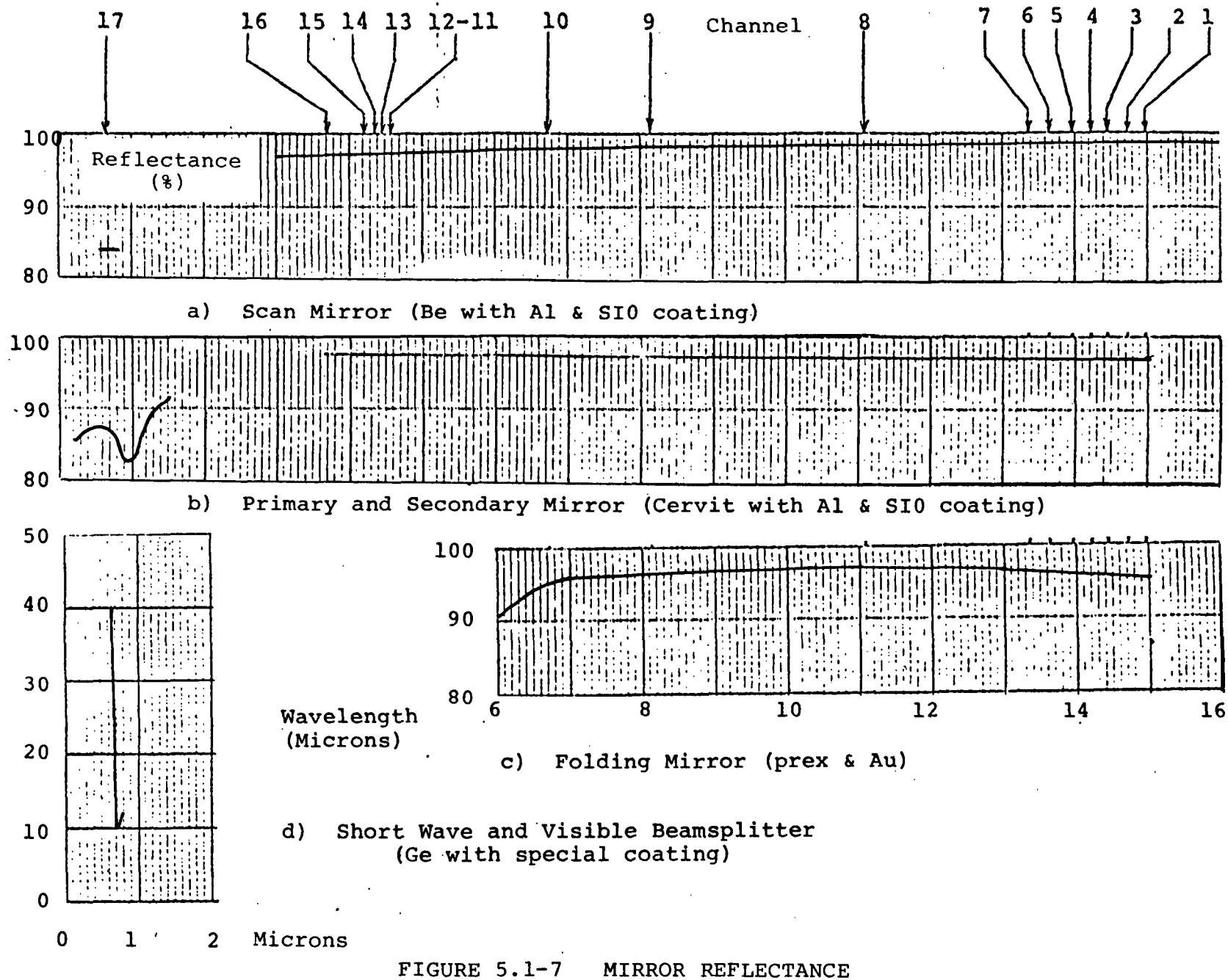


FIGURE 5.1-7 MIRROR REFLECTANCE

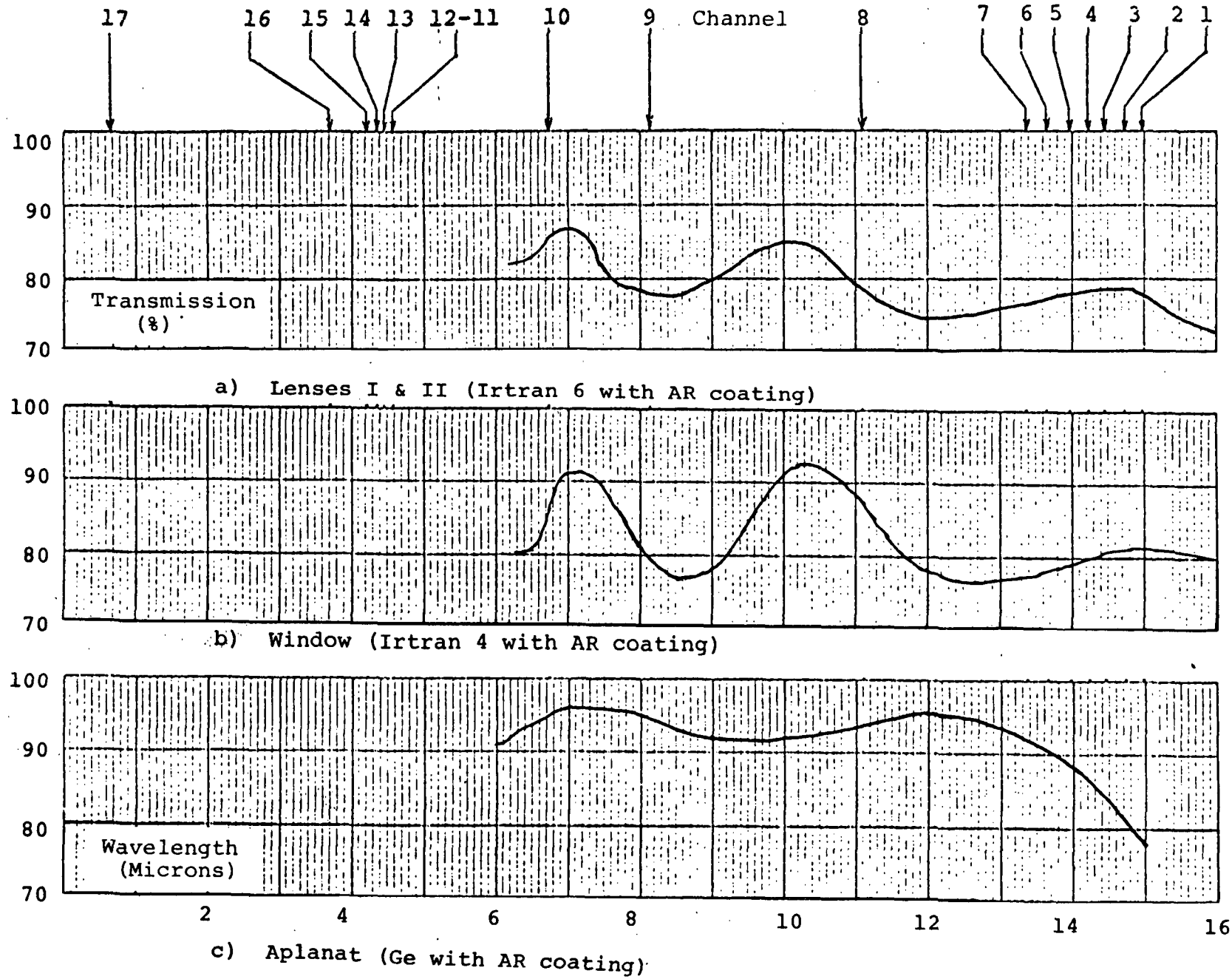


FIGURE 5.1-8 LONGWAVE OPTICAL COMPONENT TRANSMISSION

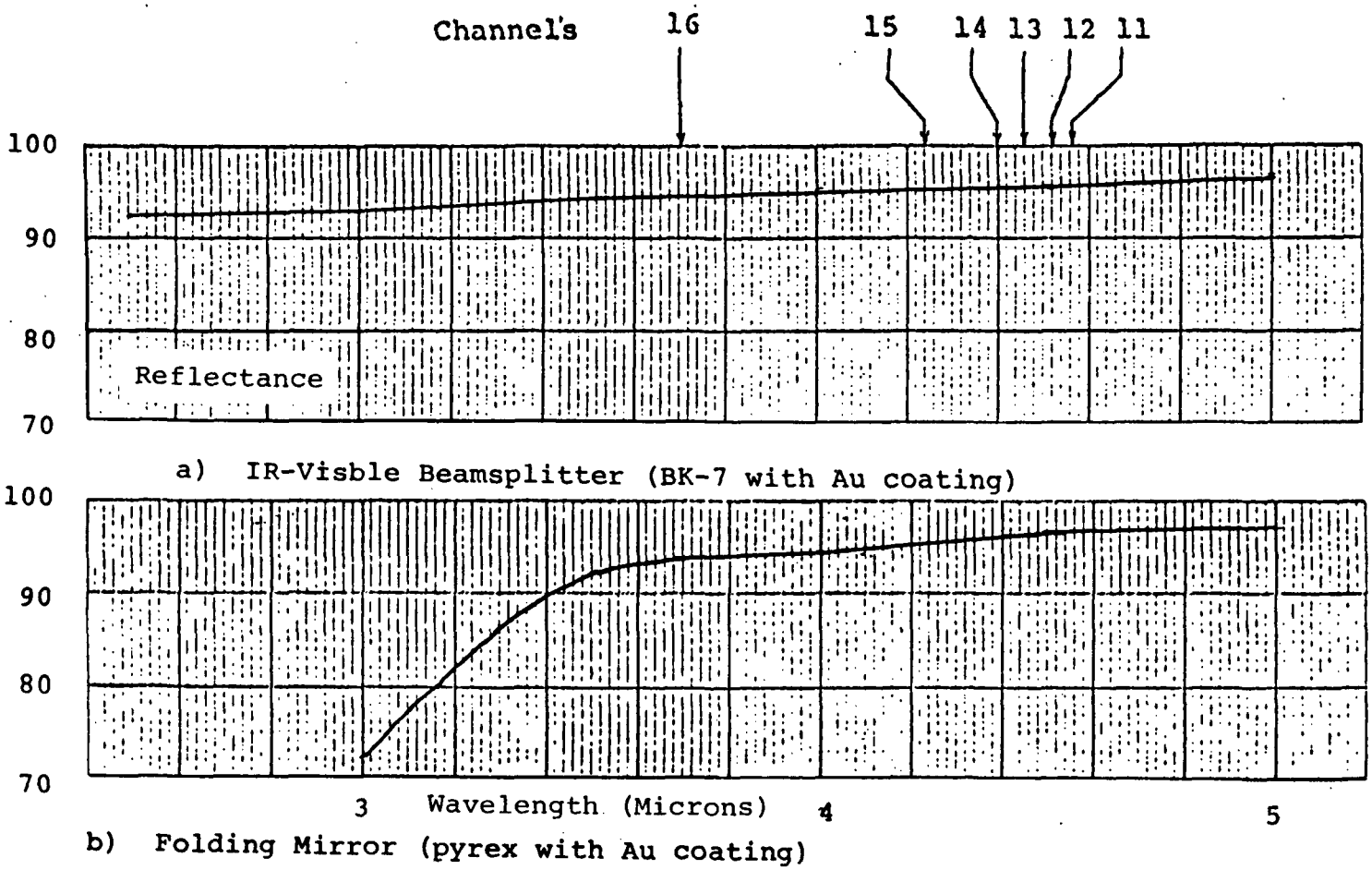


FIGURE 5.1-9 SHORTWAVE OPTICAL COMPONENT REFLECTANCE

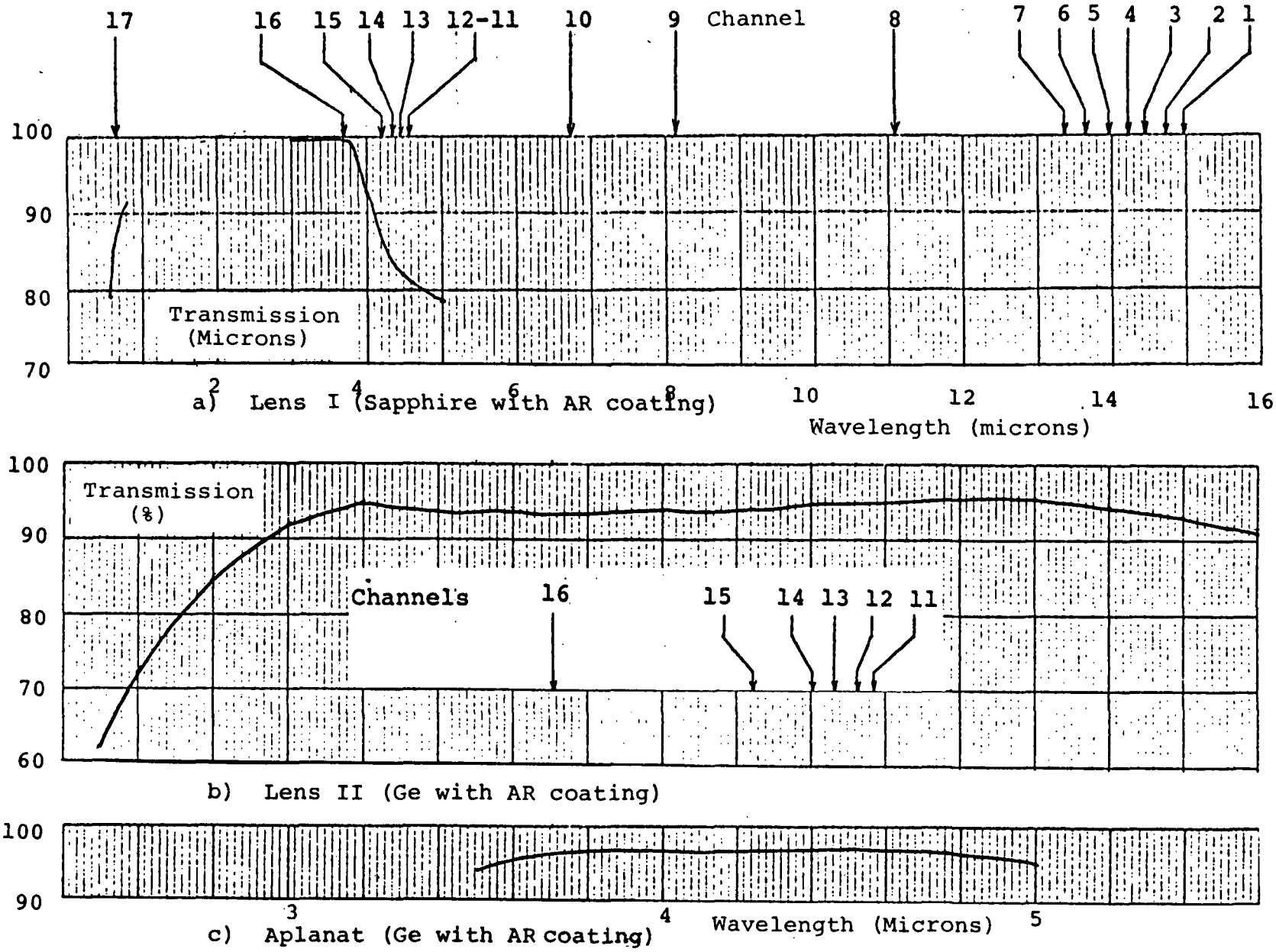


FIGURE 5.1-10 SHORTWAVE OPTICAL COMPONENT TRANSMISSION

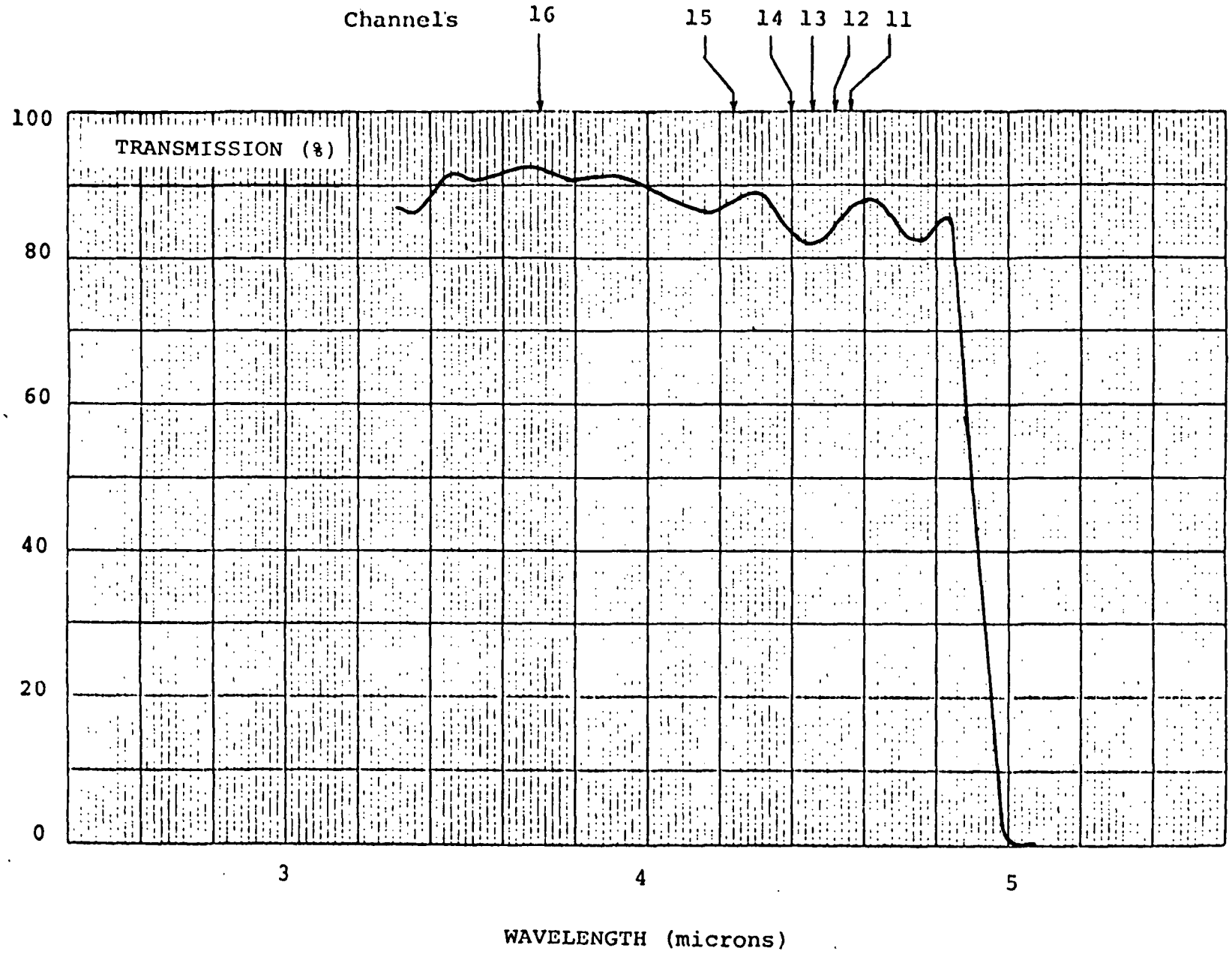
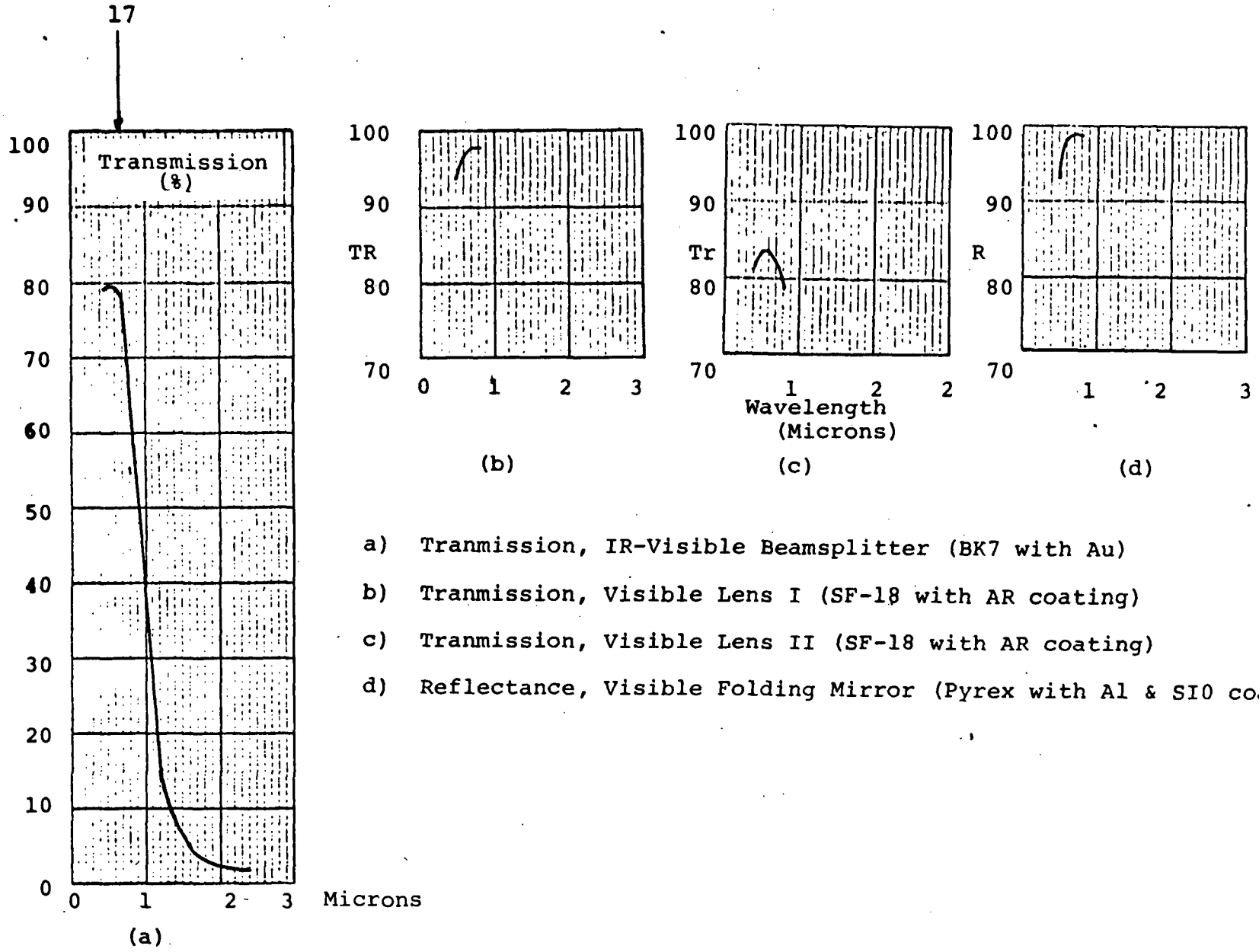


FIGURE 5.1-11 TRANSMISSION SHORTWAVE WINDOW @ 180°K AND 20° ANGLE (SAPPHIRE WITH AR COATING)



a) Tranmission, IR-Visible Beamsplitter (BK7 with Au)

b) Tranmission, Visible Lens I (SF-18 with AR coating)

c) Tranmission, Visible Lens II (SF-18 with AR coating)

d) Reflectance, Visible Folding Mirror (Pyrex with Al & SI0 coating)

FIGURE 5.1-12 VISIBLE OPTICAL COMPONENT REFLECTANCE AND TRANSMISSION

TABLE 5.1-2

OPTICAL TRANSMISSION

Channel	Optical Elements Excluding Filters	Filters	Total
1	.20	.37	.074
2	.22	.60	.13
3	.23	.65	.14
4	.22	.70	.15
5	.22	.63	.13
6	.24	.64	.15
7	.26	.58	.15
8	.36	.59	.21
9	.33	.70	.23
10	.41	.68	.27
11	.51	.54	.27
12	.50	.60	.30
13	.48	.53	.25
14	.52	.54	.28
15	.53	.68	.36
16	.55	.88	.48
17	.097	.88	.085

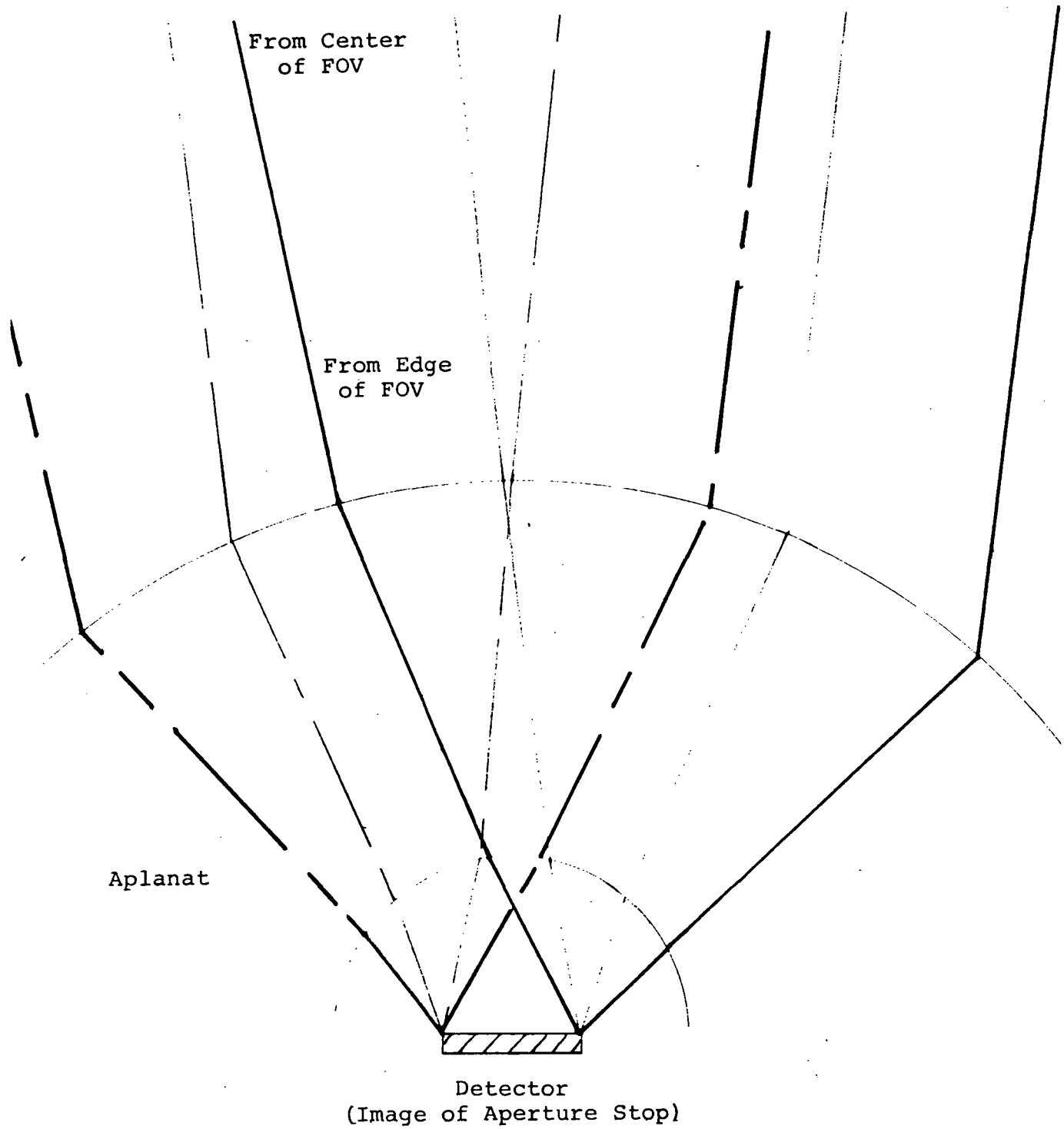
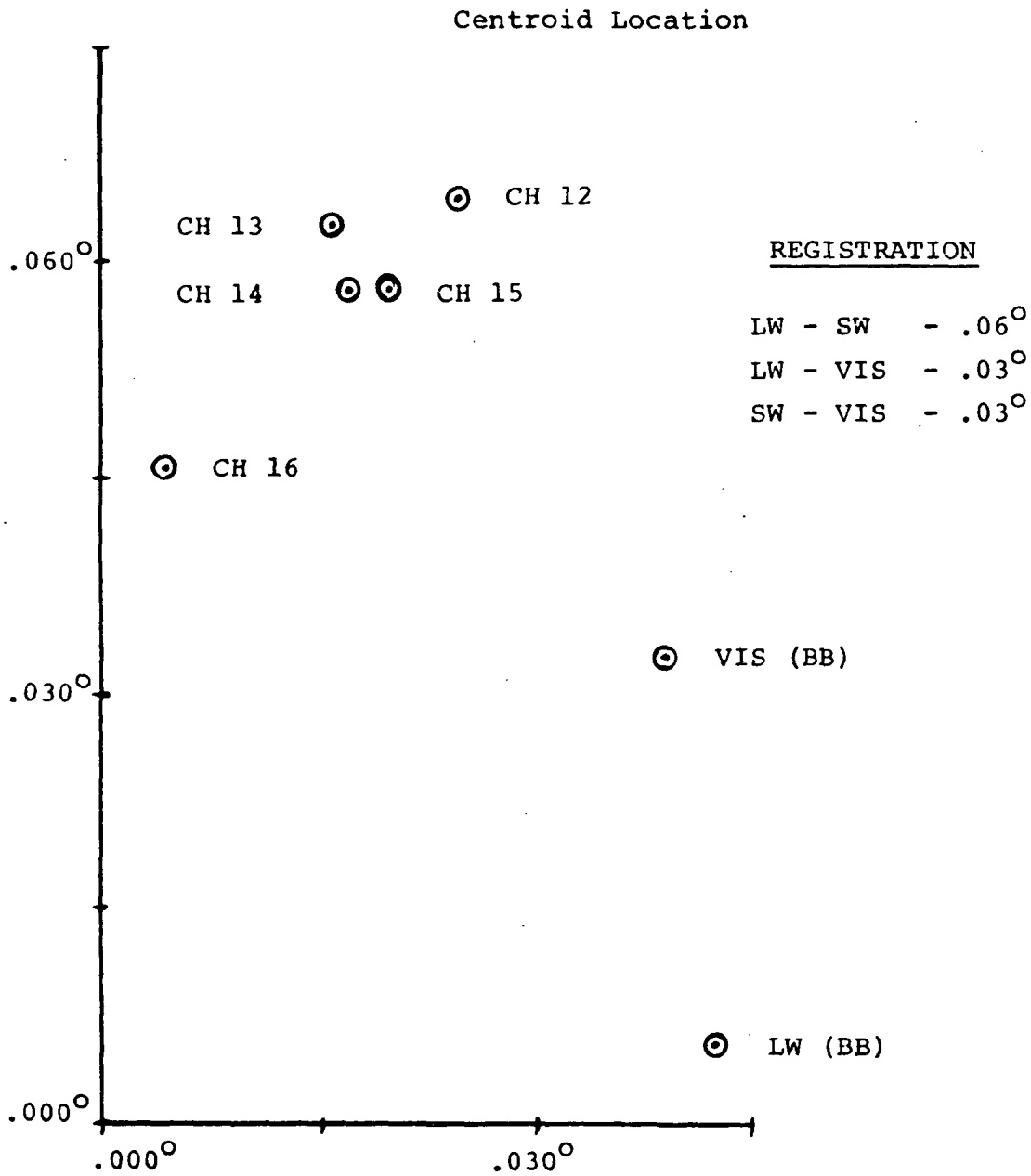


FIGURE 5.2-1 RAYS TRACED THROUGH APLANAT TO DETECTOR



EFFECTIVE FIELD OF VIEW

LW (BB)	1.17°	CH 15	1.24
CH 12	1.24	CH 16	1.25
CH 13	1.22	VIS (BB)	1.28
CH 14	1.24		

NOTES: (BB) - Broad Band Spectral Filter
Individual LW Channel Output too low to test

Test Procedure 8120619A, Completed 10-25-74

FIGURE 5.2-2 OPTICS FIELD OF VIEW

6.0 DETECTORS

6.1 General

The radiation from the three spectral bands that have been separated by the optics are detected by two cold detectors and one ambient temperature detector. Because of the required sensitivity a cold HgCdTe detector was used for the longwave channels and a cold InSb detector for the shortwave channels. The visible radiation is detected with a silicon detector.

6.2 Longwave Detector

The longwave detector was made of HgCdTe with a peak responsivity of 13 microns at 120°K. The detector had to be made large enough to collect the energy within the image of the entrance aperture which is produced at the detector location. This necessitated a detector size of .085 inches diameter, but because of problems in making a circular detector it was made .085 inches square. With this large sized detector the responsivity was very low; to increase it the detector was made of two chips connected in series. The test data measured by the manufacturer, Honeywell Radiation Center, was taken using eight milliamperes of bias, the results are shown in Tables 6.2-1 and 6.2-2. Shown in Figure 6.2-1 is the effect temperature of the detector has on the responsivity. This can be almost directly related to the signal to noise ratio. Also the S/N will increase linearly with an increasing bias current up to about 25 milliamperes; this also increases the detector temperature. Because the detector had these properties, the analysis is discussed below to show the relationship between detector responsivity, bias current and bias current heating to determine optimum bias current.

Normalized responsivity data vs temperature for the LW detector X-2 is listed in Table 6.2-3. These data were taken from the data sheets provided by Honeywell with the detector. The data labeled B.B. is the normalized responsivity of the detector looking at an unfiltered 500°K blackbody and is the data used for determining optimum bias current for Channels 5-10. Channels 1-4 vary more rapidly with temperature.

TABLE 6.2-1

S/N X-2 HIRS LONGWAVE DETECTOR DATA (Hg Cd Te DETECTOR) (Protoflight)

D* VALUES IN cm $(Hz)^{1/2}$/WATT

RAW DATA	115K	120K	125K
Signal	1.64MV	1.25MV	0.895MV
Noise	.008	.008	.008
System Noise	.0075	.0075	.0075
System Gain	5000	5000	5000
Spectral Conversion Factor (K)	1.97	2.02	2.07
Window Conversion Factor (T)	1.43	1.43	1.43
D^*_{bb} CALCULATION (TOTAL NOISE)			
Corrected Signal (Signal x T)	2.35MV	1.78MV	1.28MV
Noise	.008	.008	.008
Signal To Noise Ratio	294	223	160
D^*_{bb} (500,900,1)	1.57×10^9	1.20×10^9	8.59×10^8
D^*_λ CALCULATION			
D^*_λ (D^*_{bb} x K) Peak	3.09×10^9	2.42×10^9	1.78×10^9

D^*_λ SPECTRAL

λ	Spec. D^*_λ	% Resp.	D^*_λ	% Resp.	D^*_λ	% Resp.	D^*_λ
6.7μ	5.7×10^8	50.3	1.55×10^9	49	1.19×10^9	48	8.54×10^8
8.2μ	6.2×10^8	62.5	1.93	60.3	1.46	58.1	1.03×10^9
11.1μ	1.25×10^9	88.1	2.72	88.8	2.15	89.5	1.59
13.0μ	1.24×10^9	98.5	3.04	99.3	2.40	100	1.78
13.4μ	1.24×10^9	100	3.09	97.8	2.37	95.5	1.70
13.6μ	1.44×10^9	100	3.09	95.8	2.32	91.5	1.63
14.2μ	1.24×10^9	94	2.91	83.0	2.01	72	1.28
14.5μ	1.51×10^9	83	2.57	72.3	1.75	61.5	1.10×10^9
14.7μ	1.45×10^9	75	2.32	65.5	1.59	56	9.97×10^8
15.0μ	1.32×10^9	64	1.98	55	1.33	46	8.19×10^8

TABLE 6.2-2

S/N X-2 HIRS LONGWAVE DETECTOR DATA (Honeywell) (Protoflight)

	115K	120K	125K
R_{bb} CALCULATION			
Corrected Signal (Signal x T)	2.35MV	1.78MV	1.28MV
Area (mm^2)	4.606	4.606	4.606
$R_{bb} = \frac{5.3 \times 10^7 \cdot \text{Signal}}{\text{Gain} \cdot \text{Area}} =$	5.41 V/W	4.10 V/W	2.95 V/W
R_λ CALCULATION			
R_λ (R_{bb} x K) Peak	10.65 V/W	8.28 V/W	6.10 V/W

R_λ SPECTRAL

λ	% Resp.	R_λ	% Resp.	R_λ	% Resp.	R_λ
6.7μ	50.3	5.36	49	4.06	48	2.93
8.2μ	62.5	6.66	60.3	4.99	58.1	3.54
11.1μ	88.1	9.39	88.8	7.35	89.5	5.46
13.0μ	98.5	10.49	99.3	8.22	100	6.10
13.4μ	100	10.65	97.8	8.09	95.5	5.82
13.6μ	100	10.65	95.8	7.93	91.5	5.58
14.2μ	94	10.02	83.0	6.87	72	4.39
14.5μ	83	8.84	72.3	5.98	61.5	3.75
14.7μ	75	7.99	65.5	5.42	56	3.41
15.0μ	64	6.82	55	4.55	46	2.81

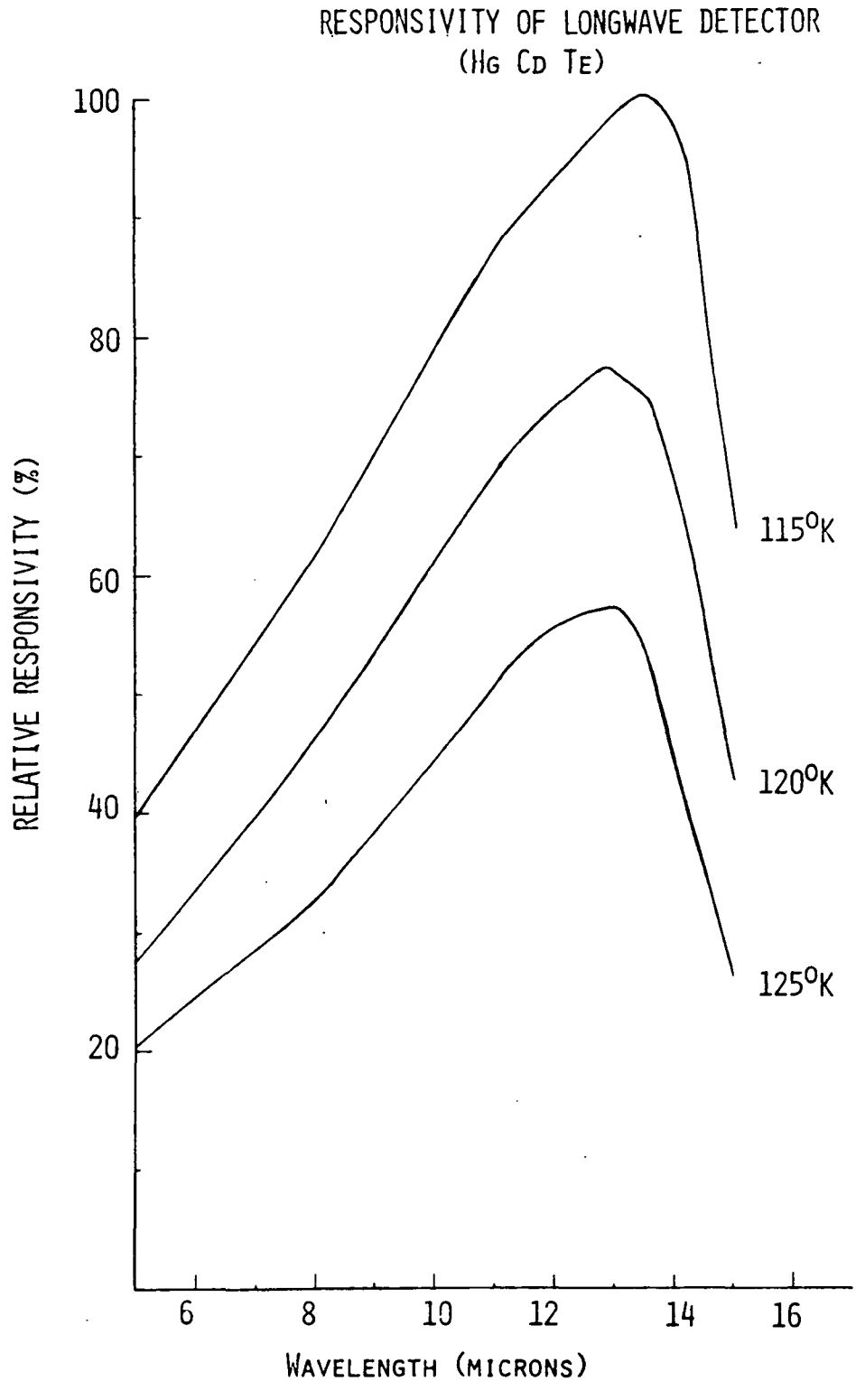


FIGURE 6.2-1 LONGWAVE RESPONSIVITY DEPENDENCE ON TEMPERATURE

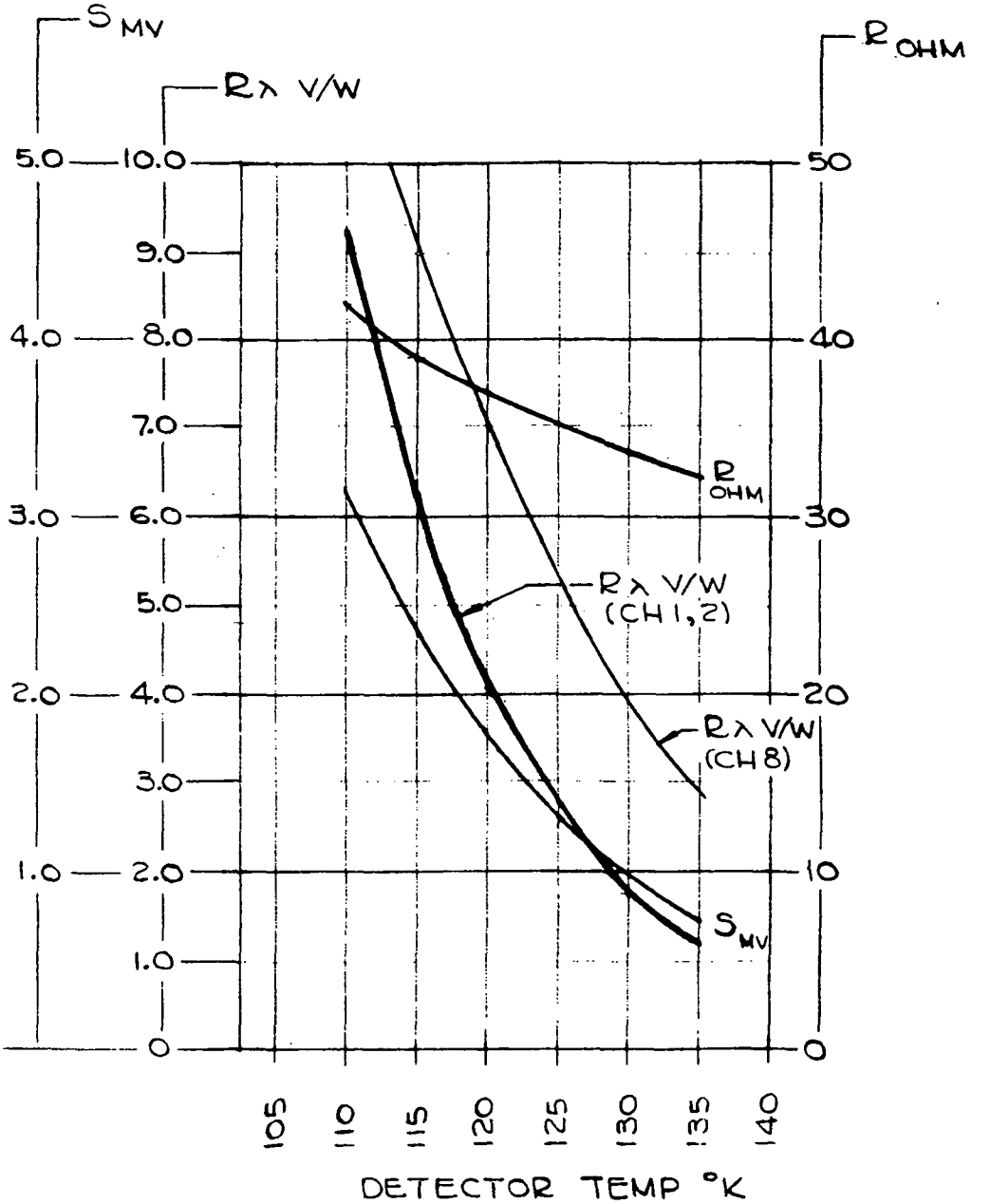


FIGURE 6.2-2 LONGWAVE DETECTOR CHARACTERISTICS

TABLE 6.2-3

Long Wave Detector Responsivity Variation With Temperature

CH #	110°K	115°K	120°K	125°K	130°K	135°K
BB	1.75	1.32	1.0	.72	.56	.40
1	2.35	1.76	1.0	.72	.46	.33
2	2.35	1.76	1.0	.72	.46	.33
3	2.47	1.84	1.0	.72	.49	.35
4	2.12	1.58	1.0	.72	.46	.33
5&6	1.80	1.35	1.0	.72	.52	.37
7	1.64	1.23	1.0	.72	.57	.41
8	1.65	1.24	1.0	.72	.56	.40
9	1.69	1.26	1.0	.72	.57	.41
10	1.73	1.29	1.0	.72	.58	.42

Figure 6.2-2 shows the resistance (R) of the detector and the signal (S) out of the detector* as a function of detector temperature. The detector bias current is held constant at 8 ma. The responsivity vs temperature of the detector at 15.0μm (Ch #1) and 11.1 μm (Ch #8) is shown in Figure 6.2-2. The detector bias current is held constant at 8 ma.

The data shown in Figure 6.2-2 is used to generate a family of curves for bias current and detector signal vs patch temeperature for four HIRS patch cooling capabilities.

The curves are plotted in Figure 6.2-3 and are based on the following assumptions:

1. With no detector bias heating the patch temperature (T_i) will be:

   $118.2^{\circ}K$ i = 1
   $115^{\circ}K$ i = 2
   $110^{\circ}K$ i = 3
   $105^{\circ}K$ i = 4

2. Detector bias heating will increase patch temperature $1.3^{\circ}K$/mw over the entire temperature range.

3. No temperature differential between detector and patch.

4. No control power applied to patch.

* Viewing a $500^{\circ}K$ blackbody and an output amplifier with a gain of 5000.

The bias current curves (T_i) were generated from the following equation:

$$I_i\ (T) = \sqrt{\frac{T - T_i}{1.3\ R_T}} \qquad \text{Eq. 6.2-1}$$

where T_i - zero bias patch temperature

T - patch operating temperature

R_T - detector resistance at T.

The detector signal curves (Si) were generated using the following equation:

$$S_i\ (T) = \frac{S(T)\quad I_{i(T)}}{8 \times 10^{-3}} \qquad \text{Eq. 6.2-2}$$

where $S(T)$ - detector signal at T with 8 ma bias shown in Figure 6.2-2.

$I_i(T)$ - detector bias current given in Equation 6.2-1.

The Si and Ii curves are plotted and are typical of HIRS channels 5-10 in Figure 6.2-3. These curves show that at low bias current the signal out of the detector increases with increasing bias current. Above an optimum current ($\approx$ 14 ma) heating of the patch due to bias current predominates and the signal decreases.

The two curves labeled load line show how signal will vary with different patch cooling capability with constant bias current of 11.4 ma and 14 ma. These curves show that reducing the bias current from 14 ma to 11.4 ma reduces the signal less than 4%.

A plot of detector responsivity at wave lengths corresponding to HIRS Channel 1 (15.0 μm) and Channel 2 (14.7 μm) is shown in Figure 6.2-2. This responsivity is at a detector bias of 8 ma. The current curves in Figure 6.2-3 and the responsivity curve in Figure 6.2-2 are combined, using Equation 6.2-2 to generate the curves shown in Figure 6.2-4. The assumptions listed earlier also apply to Figure 6.2-4. Load lines for a constant bias current of 11.4 ma and 14 ma. The optimum current in Channel 1 and 2 is about 11.4 ma.

Responsivity decreases about 5% at 14 ma. This shift in optimum current is due to the fact that the responsivity in Channels 1 and 2 changes more rapidly with temperature than in Channels 6 through 10.

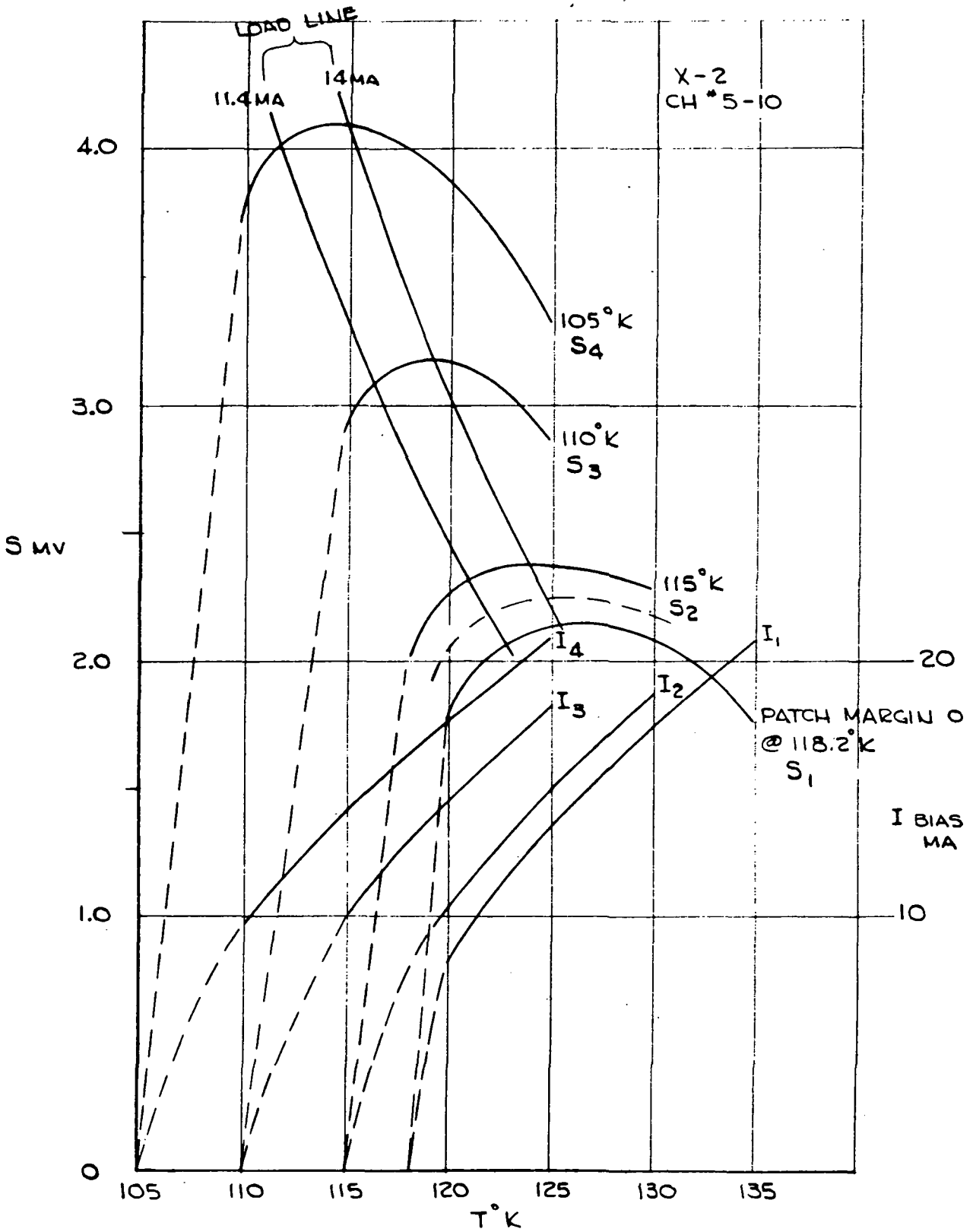


FIGURE 6.2-3 SIGNAL AND CURRENT VS PATCH TEMPERATURE SET BY DETECTOR BIAS HEATING FOR DIFFERENT PATCH MARGINS

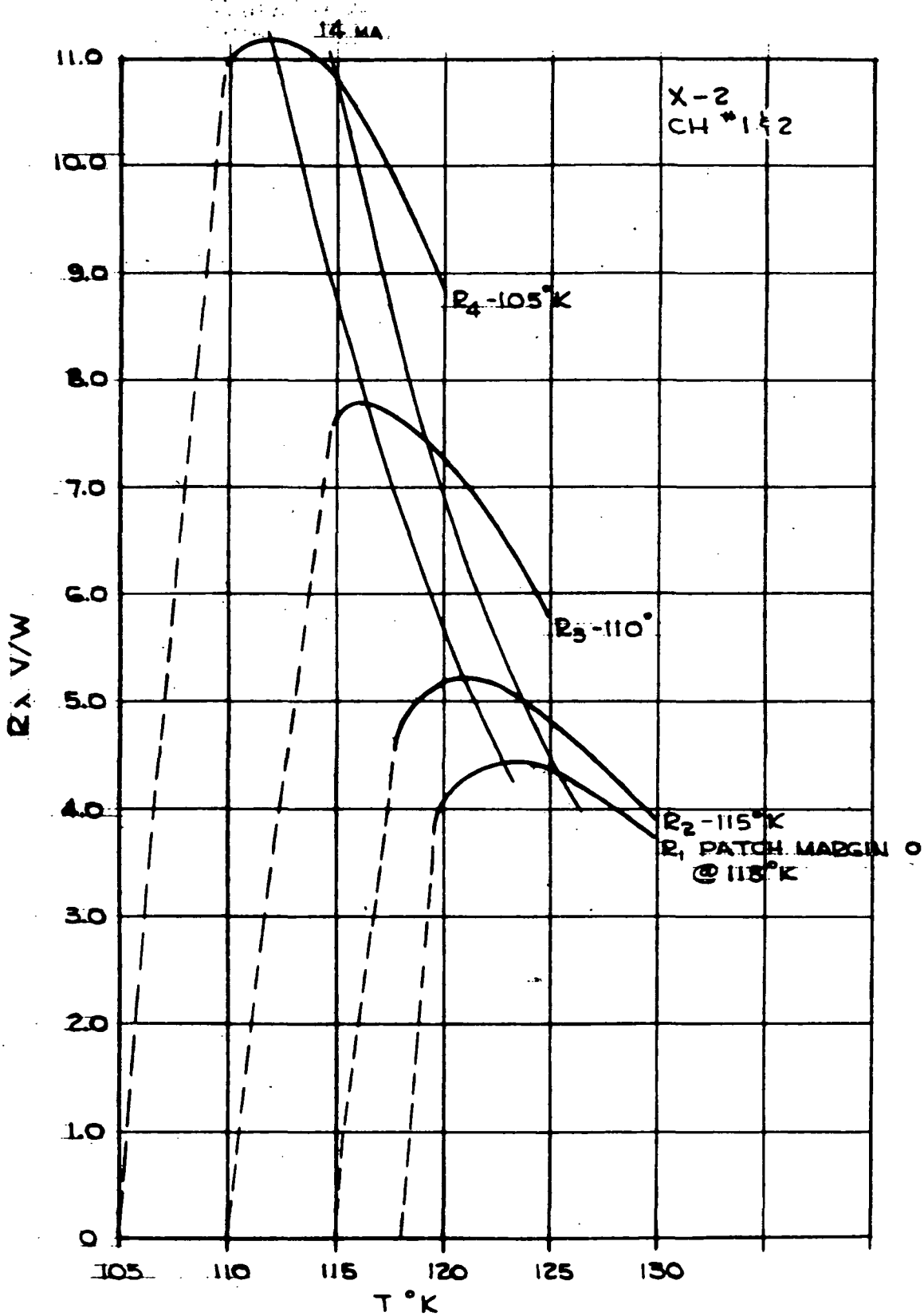


FIGURE 6.2-4 RESPONSIVITY VS PATCH TEMPERATURE FOR DIFFERENT PATCH MARGINS. PATCH TEMP SET BY DETECTOR BIAS HEATING

From these curves we can determine the improvement in signal output to be anticipated for a given cooler capacity and full time detector bias current. We have concluded that a bias current of approximately 11.4 ma will be optimum. As mentioned in the previous section, the patch temperature under zero input power was approximately 117.4°K. The curve of signal versus temperature is shown dotted for this condition. In the event that the cooling capacity increases in space, and that the bias may be turned on intermittently, the patch temperature might be as low as 112°K. The improvement from Figure 6.2-3 shows signals from Channels 5 through 10 increasing from 2.2 mv at 123K to about 3.9 mv at 112°K a 75% increase and up to 140% increase in Channels 1 and 2. With electronics power on for only short periods (10 minutes per orbit) this temperature might be achieved. For this reason, the lower patch control temperature was reduced from 120 to 112° to permit improvement of the data output.

6.3 Shortwave Detector

The shortwave detector is used to detect Channels 11 through 16 (3.7 to 4.6 microns). It consists of an indium antimonide photovoltaic detector with a peak responsivity at approximately 5.3 microns. The results of tests performed at the manufacturer, Cincinnati Electronics, are shown in Table 6.3-1. From these results the detector is not affected by temperature changes in the HIRS cooler operating temperature range. Above 130°K though the detector noise increases rapidly. Normally the detector responsivity should be proportional to $1/\lambda$ but because of effects from the antireflection coating the responsivity is relatively flat with wavelength. The quantum efficiency of the detector is greater than 90%, which is rather high for these detectors.

The predominant source of noise in the shortwave system is that produced from the background radiation falling on the detector. With the bare detector and aplanat this is a 300°K blackbody from 5.75 to 2 microns, the wavelength response of the detector. To decrease this noise, a cold shortwave length pass filter was placed on the cone of the cooler in front of the detector. At this position it was cooled to approximately 170°K and blocked all radiation above 4.9 microns as shown in Figure 6.3-1. The improvement in S/N or D^*_λ can be given by,

$$\text{Improvement} = \frac{(Q,\ 2\text{-}5.75\ @\ 300^\circ K)^{\frac{1}{2}}}{(Q,\ 2\text{-}4.9\ @\ 300^\circ K)^{\frac{1}{2}}}$$

Where Q is the photon flux falling on the detector. The improvement is shown in Figure 6.3-1.

TABLE 6.3-1

HIRS SHORTWAVE DETECTOR

DETECTIVITY AND RESPONSIVITY FOR SIX SPECTRAL POINTS

$D^*(\lambda,390,1) \times 10^{11}$ (cm $Hz^{\frac{1}{2}}$/Watt) @ $120^{\circ}K$

R_λ (Amp/Watt) Channel	Wavelength (μ)	R_λ	D*
11	4.57	3.6	1.10
12	4.53	3.6	1.10
13	4.46	3.6	1.10
14	4.41	3.6	1.10
15	4.24	3.5	1.08
16	3.70	3.4	1.04

DETECTIVITY AND RESPONSIVITY AT 4.53μ VERSUS TEMPERATURE

TEMPERATURE+ ($^{\circ}K$)	R_λ	D*
110	3.6	1.10
115	3.6	1.10
120	3.6	1.10
125	3.6	1.04
130	3.6	.94

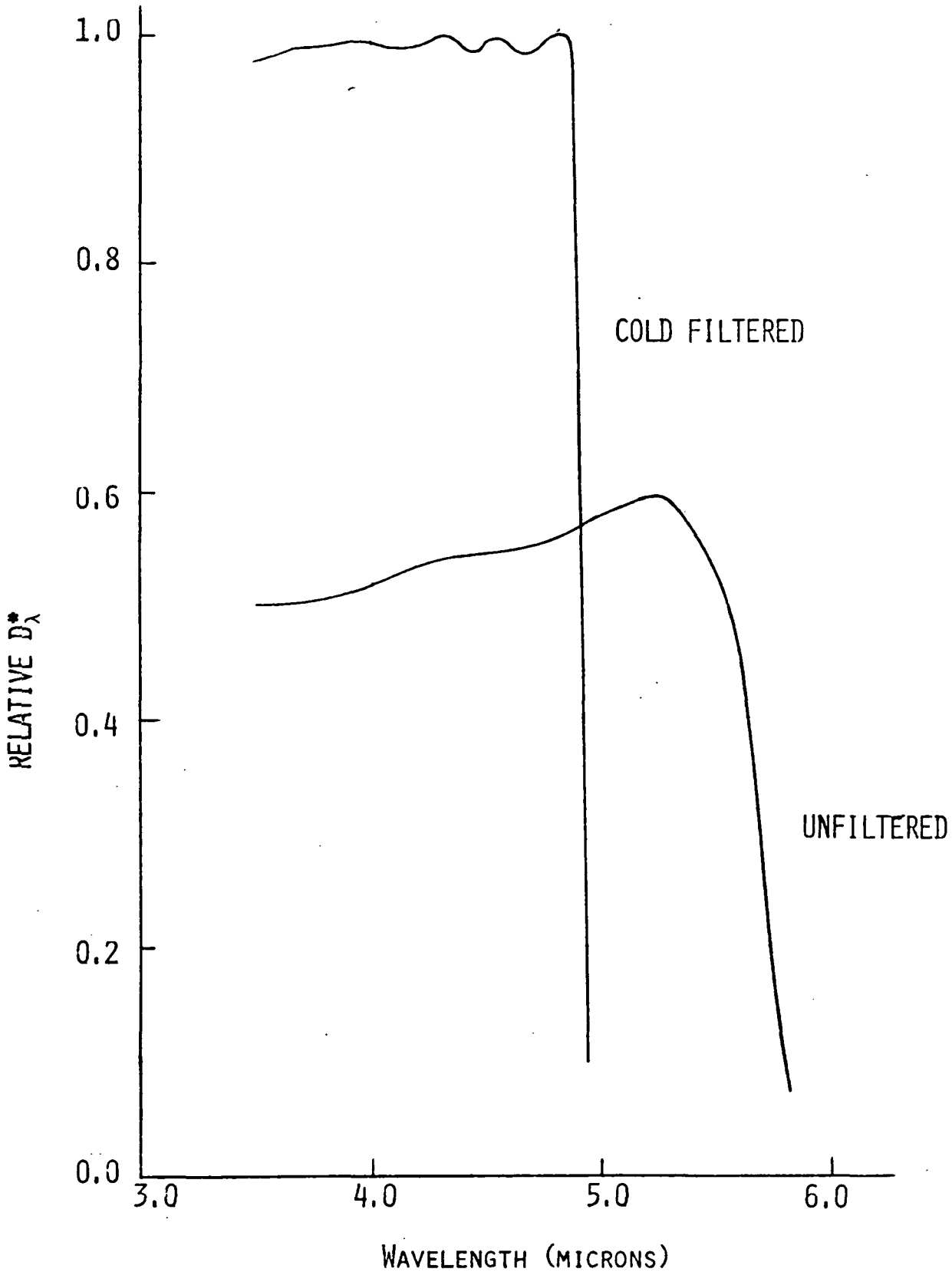


FIGURE 6.3-1 SHORTWAVE DETECTOR (InSb) IMPROVEMENT WITH COLD FILTERING FOV = 140°, 390 Hz

6.4 Visible Detector

The visible detector is a silicon photovoltaic detector manufactured by Electro-Nuclear Laboratories. The detector size is 10 mm and is used between 0.64 microns to 0.74 microns. Because it was desired to have the visible FOV match that of the LW and SW, an aperture with a 6.1 mm diameter hole was placed directly in front of the detector window, so as to reduce the visible FOV. The responsivity of the detector is 0.435 amps/watt at 0.67 microns. This gives approximately a quantum efficiency of 80%. Almost the entire noise appearing in the visible system comes from the A/D converter producing approximately half a count RMS noise value.

7.0 RADIANT COOLER

7.1 General

The purpose of the radiant cooler is to passively cool two IR detectors to a control temperature of 124°K. The basic mechanical sections that make up the radiant cooler are shown in Figure 7.1-1 and defined as follows:

Patch Assembly
Cone and Cone Bib Assembly
Housing
Sunshields
Earth Door and Drive Assembly

The cooler assembly is basically a two stage system. A housing assembly provides the mounting structure for the cone and patch and is partially isolated from the main frame of the instrument to permit operation near zero degrees centigrade. The cone, or first cooling stage is mounted on low thermally conductive synthane rods and surrounded with multi-layer insulating blankets to achieve a temperature near 165°K. The radiant patch is mounted to the cone again by low conductive rods and isolating blankets to achieve approximately 120°K orbital temperature.

7.2 Mechanical Assembly

The patch assembly consists of patch, patch shield and patch housing. Figure 7.2-1 is an assembly drawing illustrating the patch assembly. The patch contains the temperature sensor, control heaters, and two IR detectors. The purpose of the patch is to mount and cool the two IR detectors at 124°K for operation in space and to receive the IR signal which is focused on the detectors.

The surface finish of the patch consists of gold plating on all surfaces except the surface that views space. The surface that views space is high emissivity 3M black paint. The gold plating is to decouple the patch radiatively from the surrounding cone housing.

Surrounding the patch are two separate enclosures, the patch shield and patch housing. The patch shield prevents the patch from viewing the higher emissivity surface of the patch housing. The patch housing mounts to the cone end and supports the patch. The patch which is the coldest element (124°K) is structurally supported by two 0.124 inch diameter synthane tubes. Between the patch and patch shield is a mylar-silk insulation blanket and vibration damping bumpers. The bumpers are viton pads added to the patch shield to limit excursions of the patch in the y direction and prevent excessive rotation during vibration of the unit.

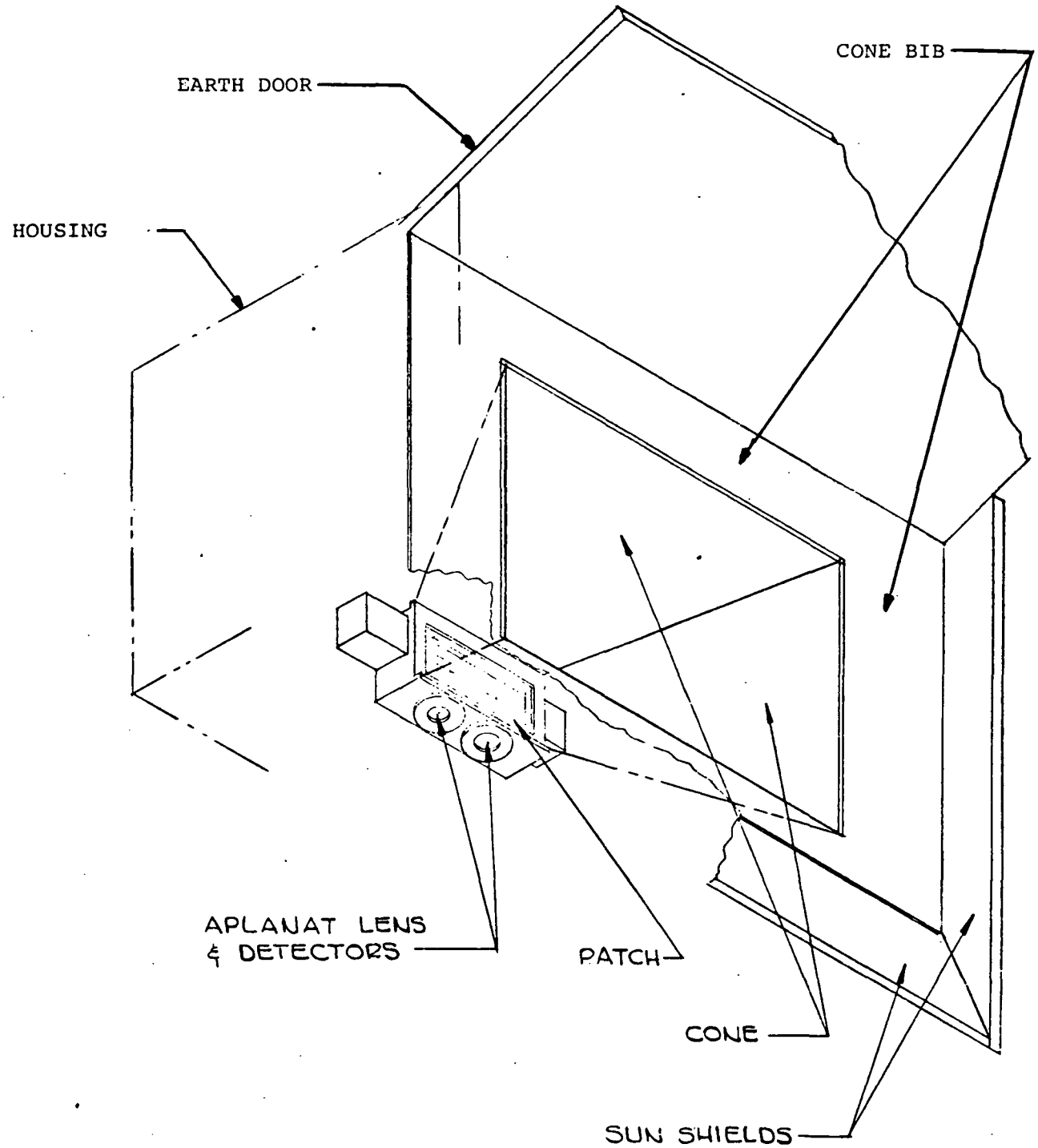


FIGURE 7.1-1 RADIANT COOLER

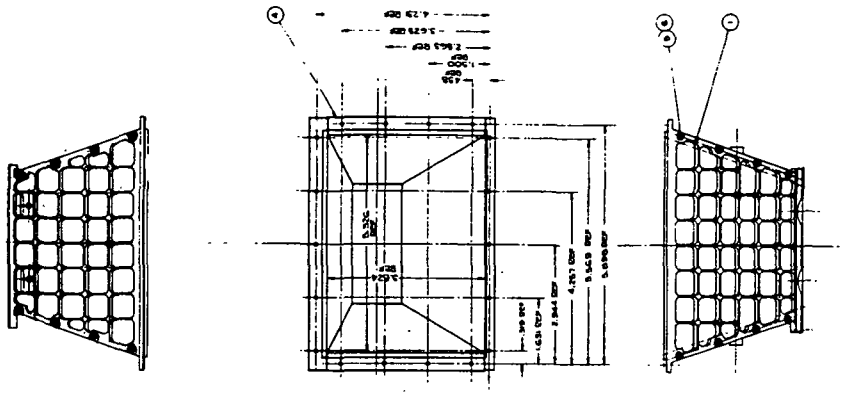


FIGURE 7.2-2 CONE ASSEMBLY

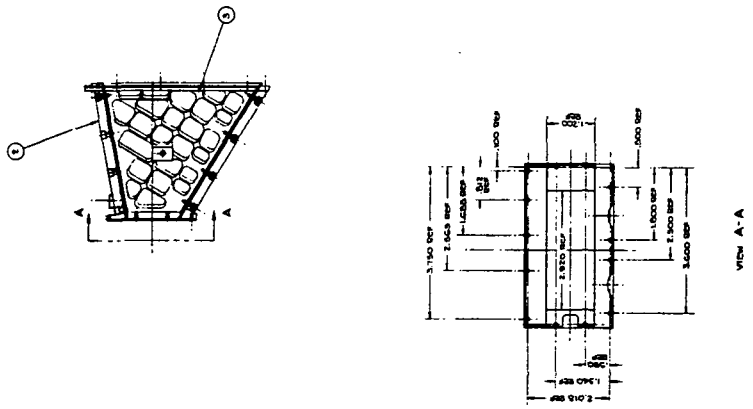


FIGURE 7.2-1 PATCH ASSEMBLY

The cone and cone bib view cold space and cool to 168°K. The cone is a trunecated rectangular pyramid that restricts the view of the patch to 28° toward the earth, 48.8° away from earth, and ±52° horizontal preventing input from spacecraft or earth for minimum spacecraft altitude of 925Km and sun angle of 12°. The reflective surfaces of the cone are highly polished nickel plating with vacuum deposited aluminum, providing no more than one cone wall reflection to cold space for rays leaving the patch in the horizontal plane and away from earth in the vertical plane. Figure 7.2-2 illustrates the cone assembly without the cone bib. The cone bib mounts to the cone mouth and radiates to cold space. The surface of the bib facing outer space is a low α/ε white paint. The external walls of the cone and the rear surface of the bib are covered with a multilayer mylar-silk insulation blanket. The blanket provides thermal isolation of the cone and bib assembly from the cooler housing.

The cone and cone bib assembly are supported by six 0.25 inch diameter synthane tubes to the cooler housing.

The temperature of the cone is monitored by a platinum sensor mounted on the external side of one of the cone walls. A 2.5 watt heater is mounted on the rear surface of the cone bib. The purpose of the heater is twofold: 1) for outgassing during preconditioning mode and 2) solar and earth heat load simulation during chamber testing. The heater is wired to a command relay through a test connector. During chamber tests the power level can be controlled.

The cooler housing completely encloses the cone and patch assemblies. The cooler housing acts as a radiating stage by cooling to 0°C, reducing radiant heat load to the cone and patch assembly. The cooler housing is a one piece housing machined as a vacuum shell to facilitate bench cooling of cone and patch assembly. Vacuum windows inserted for the bench operation are removed before installation on the final assembly for flight.

The temperature of the cooler housing is monitored by a single thermistor. The cooler housing has a ten watt heater to produce both preconditioning and environment heat loads. This heater is connected to the cone heat command relay through the test connector for controlled power testing.

The sunshields are machined aluminum with polished nickel plating and vacuum deposited aluminum. With 15° vertical inclined surfaces the sun at all B angles less than 15° is of little effect. An angle of 39.8° in the upper vertical direction prevents the cone top from seeing the earth. The external surface of the sunshields is covered with three pairs of mylar-silk insulation blanket.

The earth door consists of the same high reflective surface as sunshields on one side and painted with a low α/ε white paint on the earth side. The purpose of the earth door is twofold; 1) shield patch from viewing earth, and 2) when closed provide a means for heating radiant cooler for outgassing condition. The door is at -16.5° from horizontal when deployed. The door drive assembly consists of a stepper motor, polypropylene gear toothed drive belt, and cam assembly with two detent positions. The belt and cam positions are monitored by a potentiometer. Upon command the door can be opened for passive cooling or stored for protection or preconditioning modes.

The earth door has two five-watt heaters mounted to the rear surface. The heaters serve as environmental load simulation for chamber test but are not connected in flight configuration.

TABLE 7.2-1

Expected Environmental Heat Loads

	Heat In (Watts) Earth/Solar
Earth Door	8.8 W
Cooler Housing	7.3
Cone Bib	.25

Table 7.2-1 lists the simulated loads used in vacuum chamber test to represent space environment. The control temperature is at $124^{\circ}K$ such that when the patch tends to cool lower than $124^{\circ}K$, an automatic control circuit applies power proportionally to the patch heater controlling it to $124^{\circ}K$. The patch temperature sensitivity is $0.02^{\circ}K$ and patch temperature control is typically $\pm\ 0.05^{\circ}K$.

There are two control temperatures for space environment, $124^{\circ}K$ and $112^{\circ}K$. The second control temperature is provided for the additional cooling that could be gained in a space environment. For continuous operation this is expected to be approximately $122^{\circ}K$. From past experience with passive coolers it has been found that when the cooler is not in control the variation per orbit is less than $0.5^{\circ}K$. Also to get improved sensitivity in the LW channels it is expected that for some experiments the instrument will only be operated for approximately 15% of an orbit over a specific area of interest. With the bias to the LW detector off for most of the orbit it is expected that

the patch will cool to about 118°K. A typical plot of patch and cone temperature versus time during cool down for a chamber test is shown in Figure 7.2-3.

7.3 Contamination Prevention and Removal

The HIRS cooler and detector assembly has been designed to prevent contamination of optical, detector and cooler parts. The cooler housing drawing of Figure 7.3-1 shows the cooler housing, cone, patch and relay optic configuration. The detectors and aplanats are mounted on the cold patch at nominally 120°K. At the optical input through the cone there are band blocking filters, a coated sapphire window having cutoff at 5 microns for the shortwave detector and an Irtran 4 window with cutoff at 18 microns for the longwave detector. These blocking elements seal the patch area from contaminating gases coming from the warm optic input or cooler housing. Mounted on thermally isolating rings, these windows warm up from radiant input to a stabilization temperature above the supporting cone structure. Thermocouple measurements on these windows during test indicated a temperature rise of approximately 5° for the shortwave window and 15° for the longwave window. On the perimeter of the windows we have mounted gold plated rings extending approximately .12 inches toward the optical input. It is assumed that the warmer surface will collect water vapor molecules, since an eight degree temperature differential changes water vapor pressure from 3.8×10^{7} torr at 157K to 2.5×10^{6} torr at 165K. Condensation should not occur on the window.

Optical port input to the patch and detectors is through an opening in the cooler housing. The last optical element is mounted in a synthane block and will be at a temperature near 15° C. The cooler housing at 0°C acts as a trap for water vapor in the housing to optic interface area.

The detector and aplanat are mounted on the 120°K patch, isolated from the optical port input by the 165°K cone window and from gases coming in the cone opening by edge baffles at the patch to cone interface. A change in design of the patch assembly after the vibration test added multilayer insulation in the patch to cone spacing, making outgassing time very necessary. Thirteen days of orbital outgassing at a cone temperature of 26° C and patch temperature of 8°C should permit this area to be clean. Multilayer insulation is mounted in the cone to housing interfaces with the ends of the multilayer blocked from direct paths to optic elements and open to space through openings between the cone and housing. With the housing at 21°C this multilayer should be well outgassed during the thirteen day period.

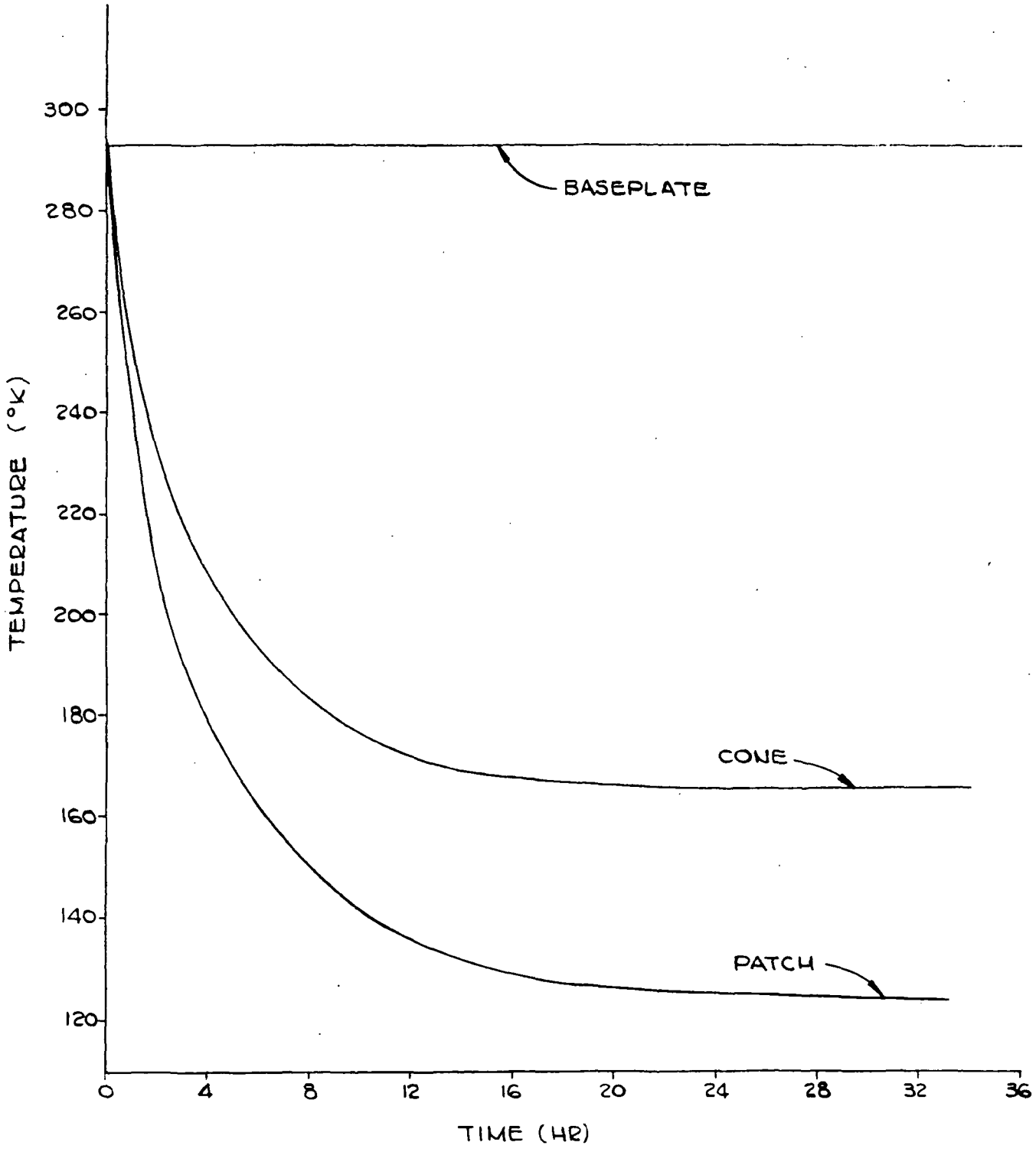


FIGURE 7.2-3 HIRS PATCH, CONE & BASEPLATE TEMPERATURE VERSUS TIME

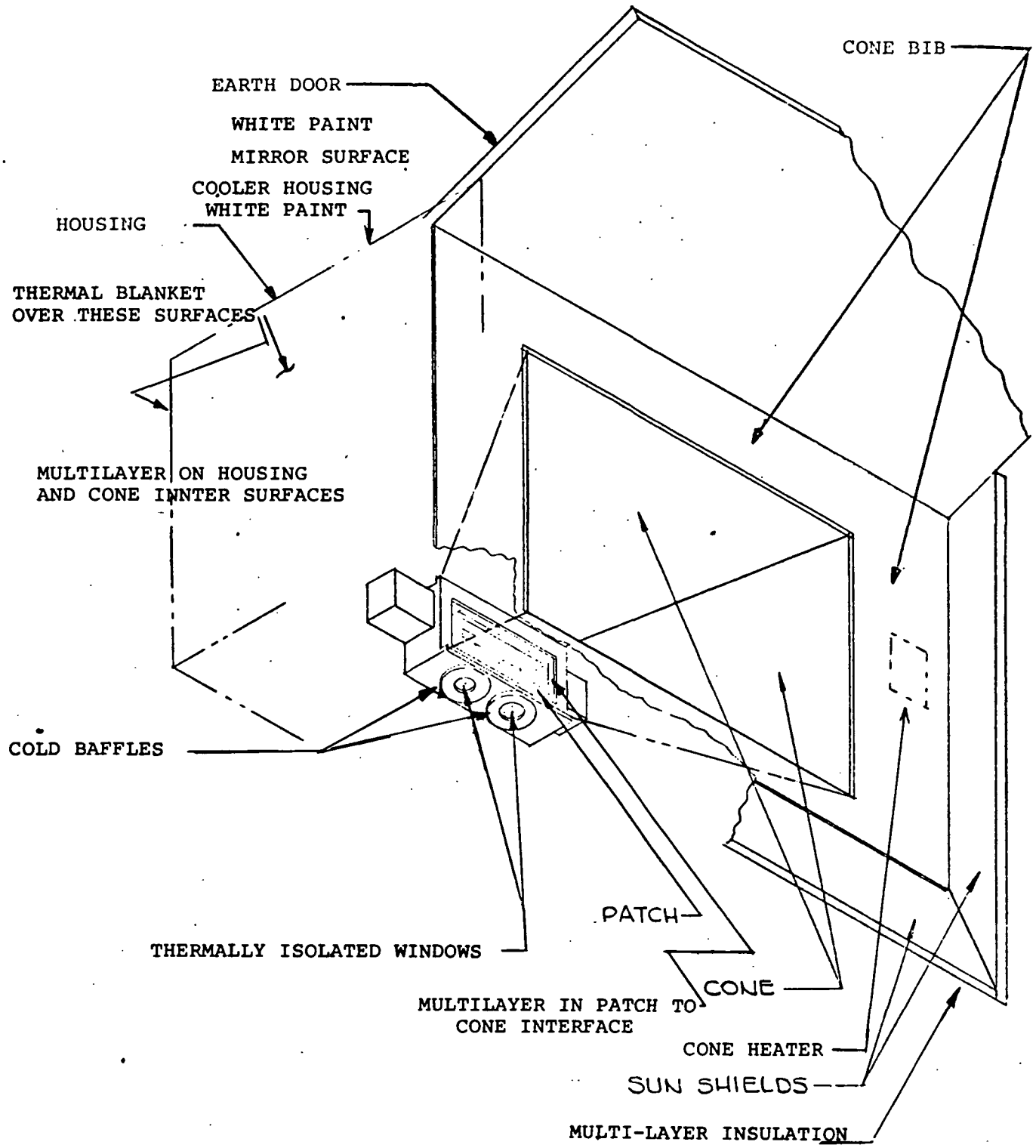


FIGURE 7.3-1 RADIANT COOLER THERMAL COMPONENTS

When the 2.5 watts of cone heat and 10 watts of housing heat are turned off and the cover door is opened, we anticipate rapid cooling to housing, cone, and patch temperatures of 4°C, 167K and 122°K.

Data from the system will be monitored to detect changes in optical input and cooling performance. If it is considered necessary to clean the system it is possible to command the door closed and the cone and housing heat on. Within 16 hours the cone and patch will be above 273°K. An outgassing period of 14 days is recommended to again clear the optic elements, patch, cone, and insulation of all deposited materials.

7.4 HIRS Cooler Performance Predictions

7.4.1 Cone Predictions

The predictions of performance of the HIRS cooler assume a sun angle of 12°. The thermal balance equation of the cone is:

$$\phi = \varepsilon_d A_d \sigma T_o^4 = \phi_e + \phi_s + \phi_o + \phi_h + \phi_k + \phi_i$$

where d = cone end, e = earth, 0 = optical port
s = direct sunlight, h = shield
k = conduction, i = insulation
$\sigma = 5.67 \times 10^{-8}$ W/m^2 °K^4

For a cone end emissivity of 0.85 and solar absorptivity of 0.20, the value of $\phi_e + \phi_s$ at a 12° sun angle was 0.296W. A list of thermal inputs is given below.

Source	Watts	%
Earth and Sun	0.2960	35
Optical port	0.2105	25
Shield	0.0708	9
Conduction	0.0505	6
Insulation	0.2061	25
	.8339	

With a cone area of $A_d = 222.5$ cm^2 and cone emissivity of $\varepsilon_d = 0.85$ the cone should have a temperature of approximately 167°K.

7.4.2 Patch Predictions

The thermal balance equation of the patch is:

$$\phi_p = \varepsilon_p \sigma A_p^4 = \phi_r + \phi_o + \phi_j + \phi_k + \phi_i$$

where p = patch, r = cone walls, o = optical port, j = joule heating, k = conduction, i = insulation

The joule heating comes from the LW detector bias (4.6 mW) and the control heat (0.5 mW). The list of thermal inputs is given below.

Source	Milliwatts	%
Cone Walls	2.75	10
Optical Ports	9.60	34
Joule Heat	5.10	18
Conduction	2.00	7
Insulation	8.77	31
	28.22 mw	

With a patch emissivity of $\varepsilon_p = 0.93$ and area $A_p = 22.6$ cm^2 the patch temperature should be $T_p = 124^{\circ}$K.

Comparing these figures with early estimates (mid-1972) the greatest increases are in optical port input and joule heating from longwave detector bias current.

8.0 ELECTRICAL SYSTEM

8.1 General

The electrical design of the HIRS instrument can be conveniently segmented into four broad categories related to each of the four input -24.5 VDC power busses from the spacecraft.

1) The Mirror Scan Motor Subsystem buss
2) The Filter/Chopper Motor Subsystem buss
3) The Electronics Subsystem buss
4) The unswitched Full-Time Telemetry buss

All of these busses are separate distribution systems with returns isolated within the instrument. In addition, the regulated output voltages of the Electronics DC to DC converter within the HIRS maintain a separate return or common called "Signal Ground" which is not connected to the Electronics "Power Ground." All power and signal returns in addition to the HIRS chassis ground is available on pairs of pins at each connector for optimizing the spacecraft grounding at the main regulator "unipoint ground."

The first of these, the Mirror Scan Motor buss powers only that circuitry which is involved with the power and logic control of the mirror drive mechanism which is described in detail in Section 3.0. The second, the Filter/Chopper Motor Buss not only provides a two-level amplitude and frequency controlled power source for the synchronous filter/chopper drive motor, but also input power for the following; the proportional heater controller of the filter/chopper housing assembly, the passive radiant cooler door mechanism and the heater power to the cooler housing and cone assemblies. The Electronics buss powers the DC to DC converter whose regulated outputs power all of the analog signal processing electronics and the digital electronics that not only control the analog circuits but formats the digitized data to a bi-phase serial bit stream (3,389.82 bits/sec) which is outputted to the High Data Rate Subsystem recorders. The Full-Time telemetry buss continuously powers a group of medium accuracy passive (thermistor) temperature monitor circuits and the cooler door position potentiometer. These analog telemetry points are shown on Table 2.1-1.

8.2 Timing and Synchronization

8.2.1 General

Although the filter chopper hysteresis synchronous drive motor has primary control over instrument timing and synchronization, all instrument timing, in the final analysis, is derived from the electronics subsystem 400 KHz gated astable multivibrator. This gated astable, which is normally driven by the extracted S/C 400 KHz clock, provides the input to the frequency divider that determines the rotational rate of the filter chopper motor. This motor drive subsystem is described in detail in Section 4.0. The motor is directly coupled to the filter wheel which rotates the visible and shortwave (SW) filters and the longwave (LW) filters through the optical path. The visible and the SW filters are arranged along the circumference of an outer radius of the wheel while the LW filters are arranged along a concentric inner radius of the wheel. The SW forty-two tooth chopper is directly attached to the filter wheel, while for the LW filters, a concentric counter-rotating sixteen tooth chopper is rotated at six times the angular velocity of the filter wheel.

The longwave and shortwave chopper rotation rates are monitored by LED/photodiode sensor circuits (a simplified circuit design is shown in Figure 8.2-1). The electrical reference frequencies thus derived are then phased properly to the chopped video to provide proper synchronous detection. The two reference signals are also electrically phase shifted by $\pi/2$ radians so that by suitable counting and decoding logic circuits for each, the video processing electronics described in Section 8.3 may be properly time correlated with the spectral filters as they pass through the optical path. This counting and decoding logic for both the LW and SW channels, is synchronized or initialized by a filter wheel sync signal, a "once around pulse" generated by another LED-photodiode sensor assembly which is positioned to detect but one narrow slot on the filter wheel. These synchronized counter/decoders are used to control the LW and SW data channels output signal electronic integrators.

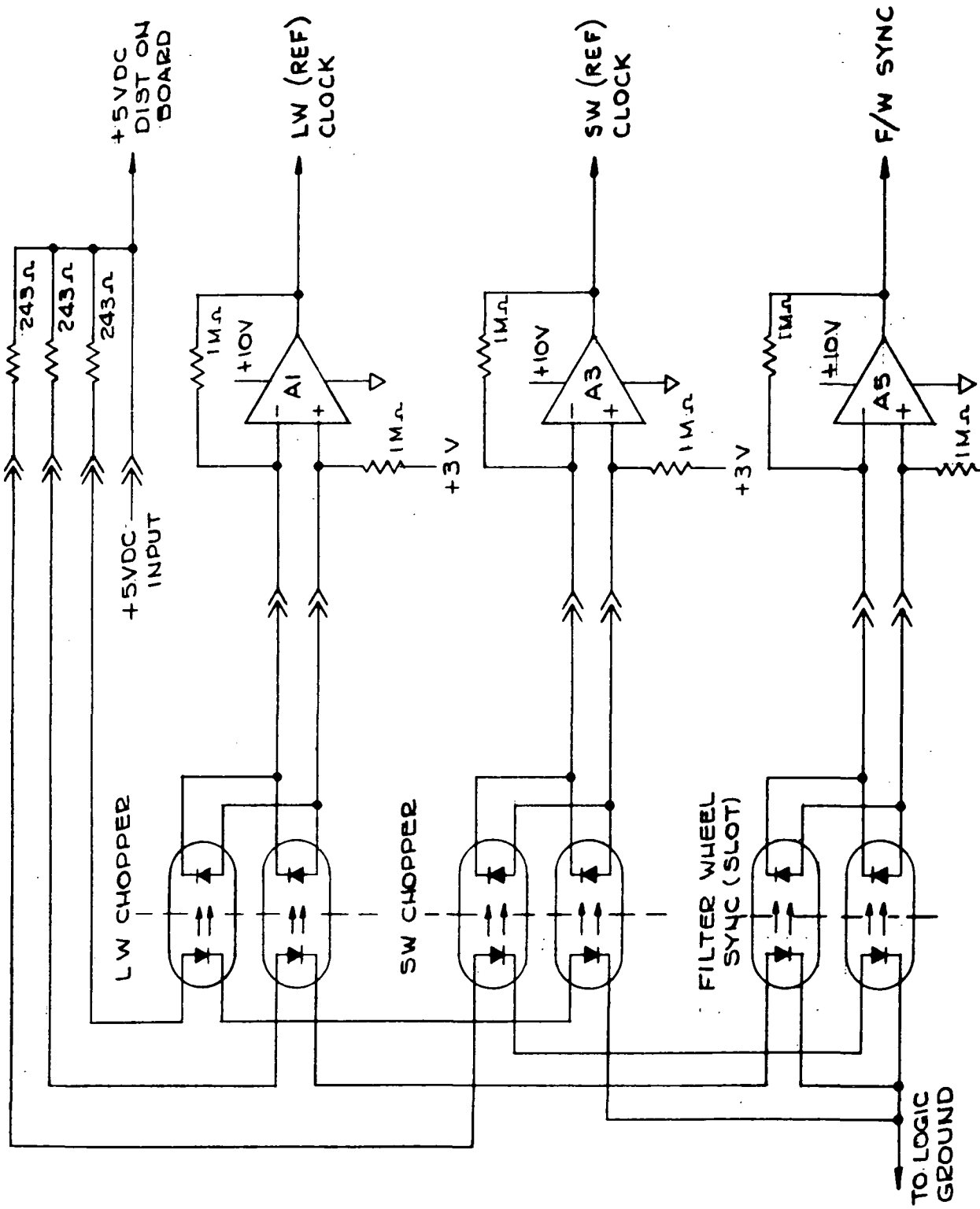


FIGURE 8.2-1 LED/PHOTODIODE SENSOR CIRCUITS

8.2.2 SW/LW Data Control

The counters for both SW and LW phase shifted references are shown on Schematic 8117742. Figures 8.2-2 and 8.2-3 show in simplified form the method used to phase shift the SW and LW references by $\pi/2$ radians. The SW counter consists of two-ripple clocked fully decoded octal counter circuits. (Octal rather than decimal counting and decoding resulted in a reduced board pin out which enabled both the SW and LW counters to be constructed upon the same assembly). A timing diagram of the SW counter portion of Schematic 8117742 is shown in Figure 8.2-5.

Integration period and reset period control latches and the necessary two-input octal number decoding NAND gates are shown on Schematic 8117799. The integration period is subsequently modified by two fixed period control one-shots shown on Schematic 8129428. Figure 8.2-4 shows this circuitry in simplified form. These selectively strobed one-shots modify the pulse train of line three of Figure 8.2-6 to that shown on line four. This modification resulted in greatly reduced SW channel sensitivity to motor assembly rotation rate variations or jitter and is described in detail in Paragrapn 8.3.1.3. Further modification of the basic integration control pulse train as shown in line five of Figure 8.2-6 was necessary. Circuitry shown on Schematic 8120708 gated out the first 3/4 cycle of each "three cycle" channel for the purpose of reducing SW data channel noise. The reason this was necessary is discussed in Paragraph 8.3.2.2.

The LW Counter consists of a frequency doubler and three ripple clocked octal counter-decoder elements also shown on Schematic 8117742.

The timing diagram is shown on Figure 8.2-7. This circuit implementation allowed simple three-input NAND decoding of any ½ reference cycle of the LW (out of 96 cycles per filter wheel revolution) to be decoded. The circuit showing the decoding necessary for setting and resetting of the LW data channel integration and reset control latches is shown on Schematic 8118491. This timing diagram is shown in Figure 8.2-8. It is very similar in structure to the SW system described earlier except that no modification to the integration control pulse train was necessary to reduce LW data channel noise. Referring to line three of Figure 8.2-8, it is seen that five different integration periods are necessary for the total of ten long wave channels. Except for Channel 10 to Channel 1, a 2½ reference cycle separation exists between filters. This is the reason the long wave counter-decoder contains a reference frequency doubler.

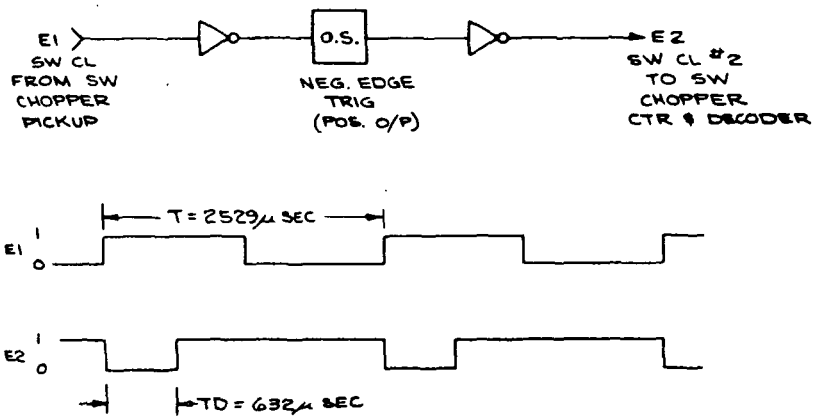


FIGURE 8.2-2 SW CLOCK 90° PHASE SHIFT CIRCUIT PART OF SCHEMATIC 8120428

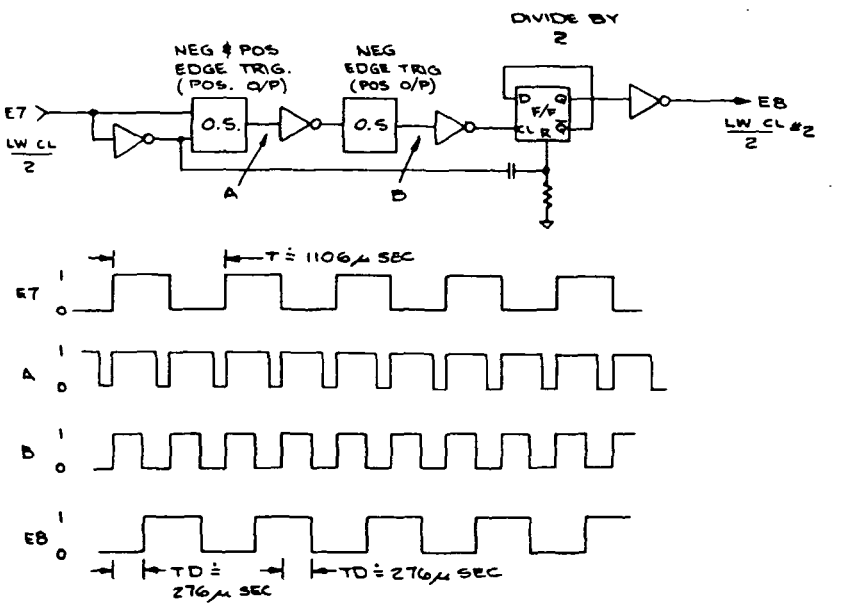
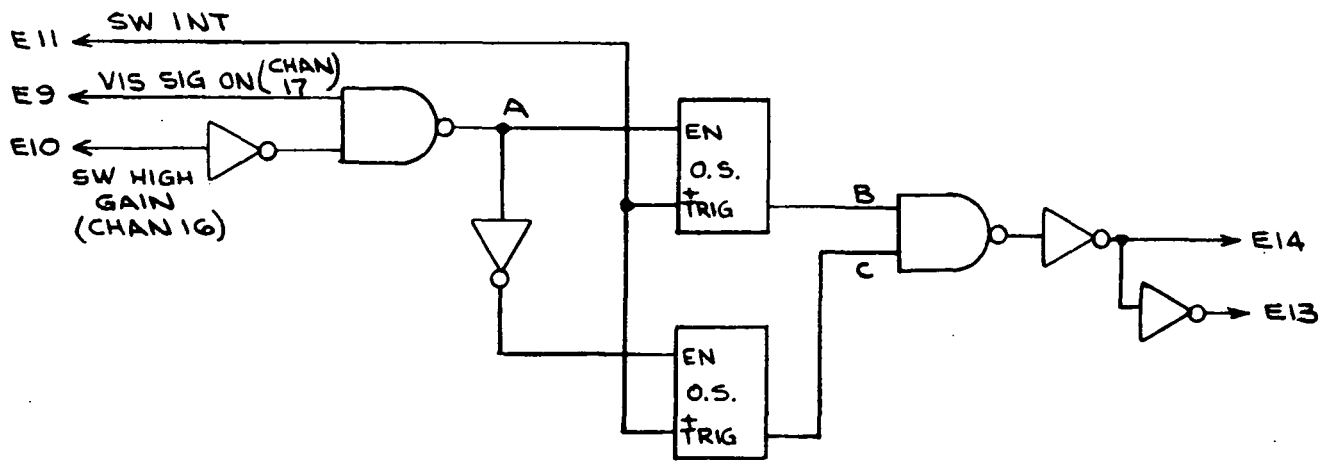


FIGURE 8.2-3 LW CLOCK 90° PHASE SHIFT CIRCUIT PART OF SCHEMATIC 8120428



POS EDGE TRIGGERED
ONE SHOT

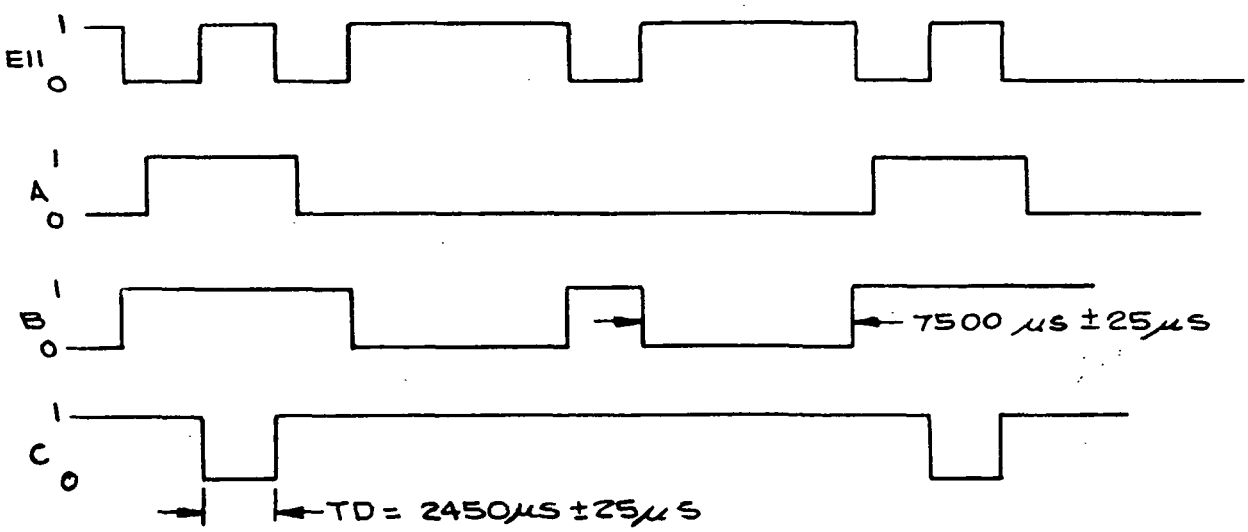


FIGURE 8.2-4 SW INT (FIXED DELAY) (SHORTWAVE INTEGRATION)
PART OF SCHEMATIC 8120428

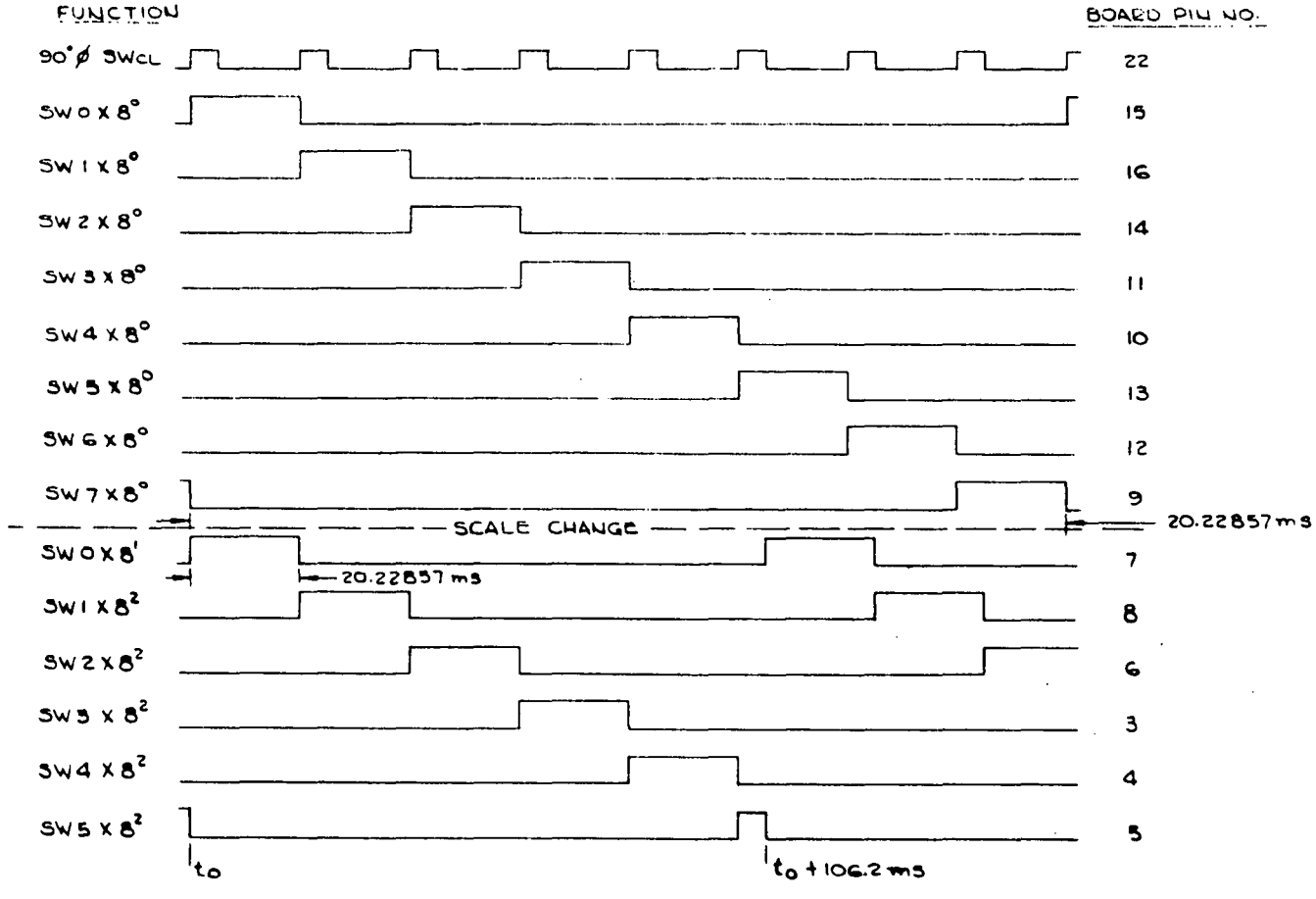


FIGURE 8.2-5 TIMING DIAGRAM FOR SW CHOPPER COUNTER (ONLY) PORTION OF SCHEMATIC 8117742

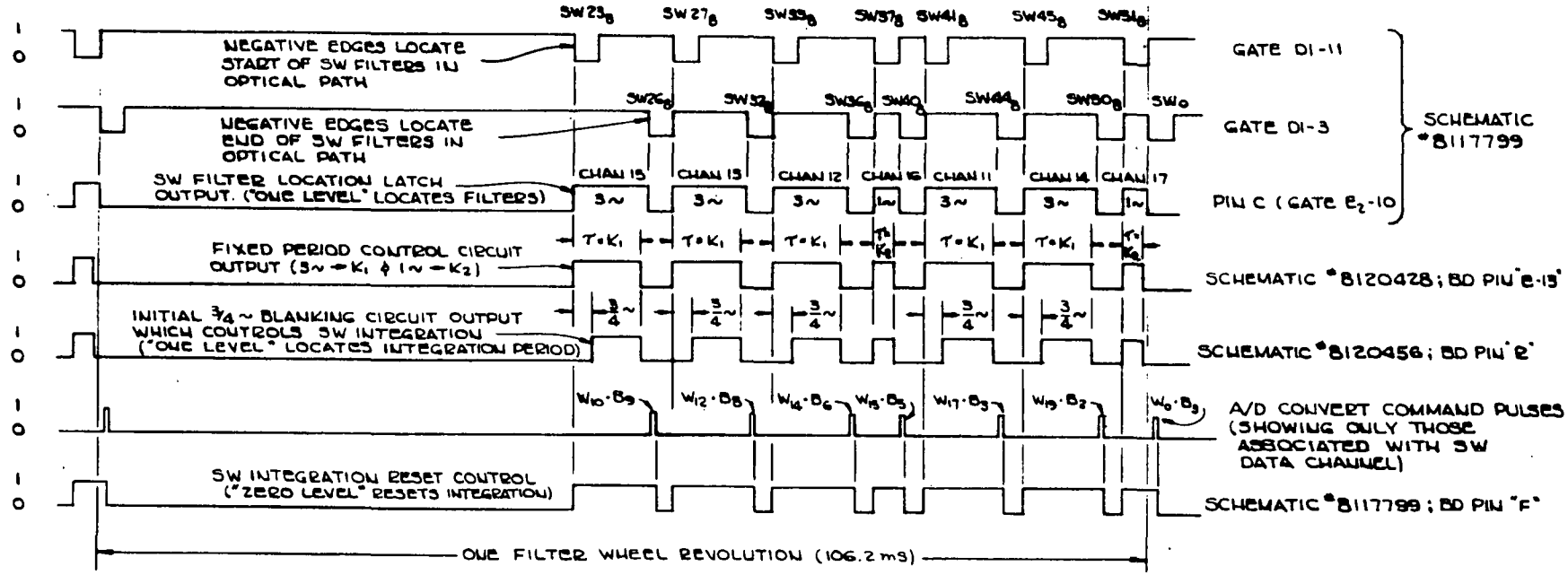


FIGURE 8.2-6 SW DATA CHANNEL INTEGRATOR CONTROL TIMING DIAGRAM

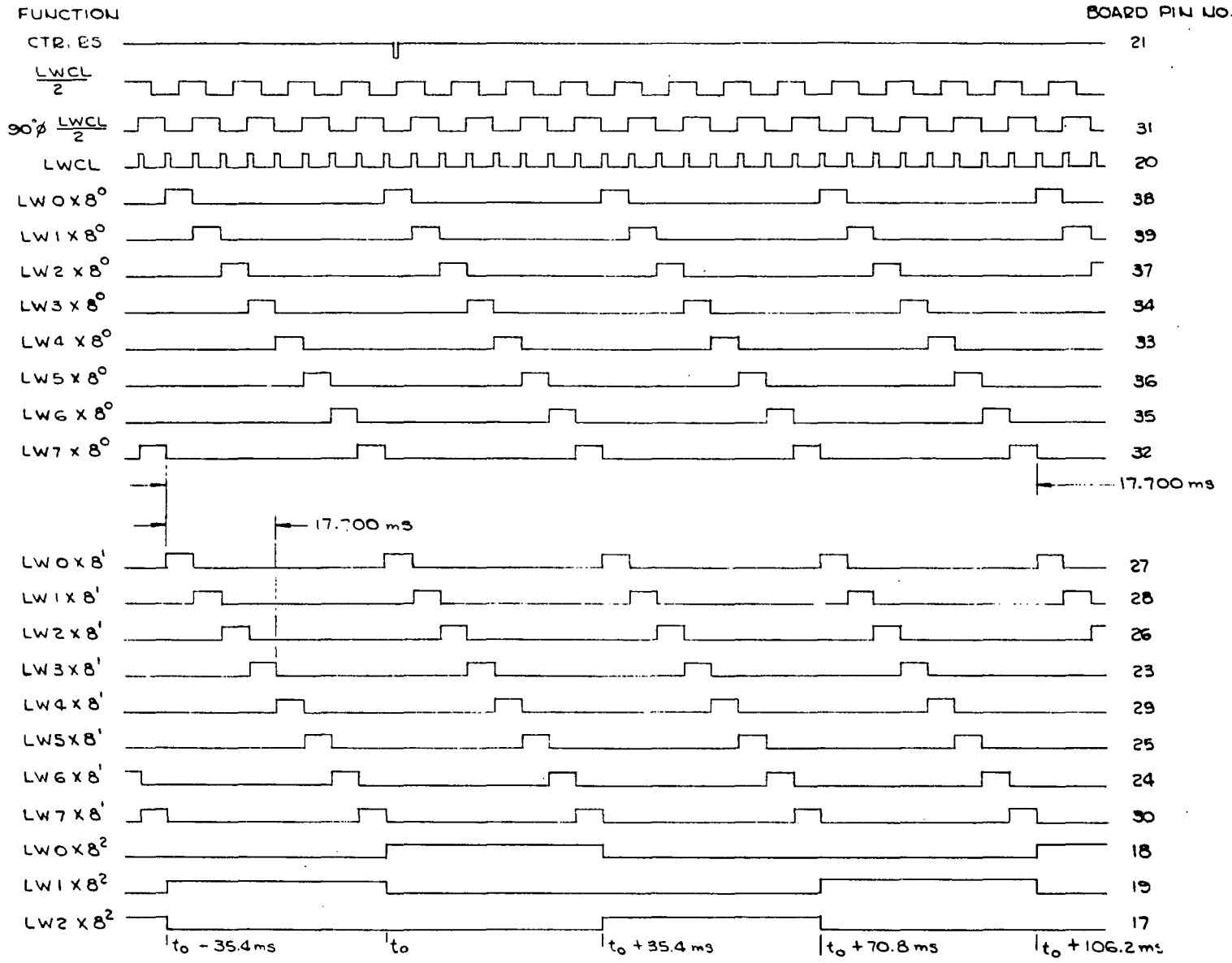


FIGURE 8.2-7 TIMING DIAGRAM FOR LW CHOPPER COUNTER (ONLY)
PORTION OF SCHEMATIC 8117742

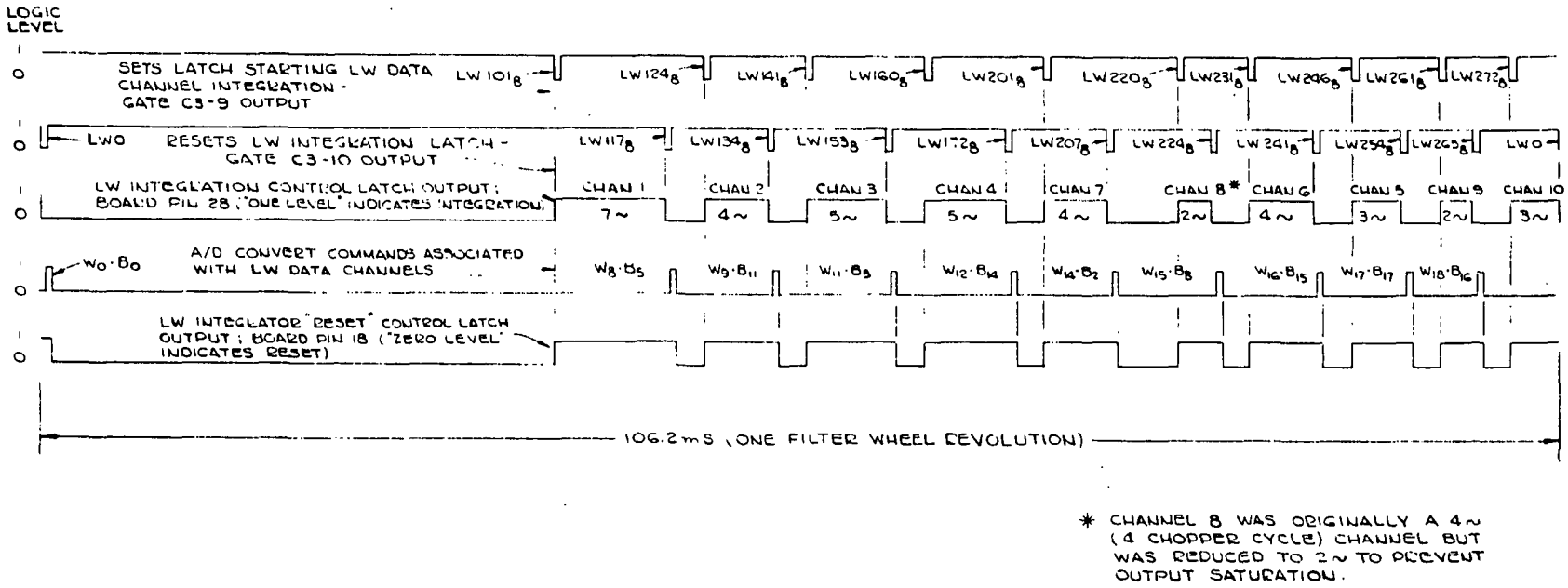


FIGURE 8.2-8 LW DATA CHANNEL INTEGRATOR CONTROL TIMING DIAGRAM (FROM SCHEMATIC 8118491)

8.2.3 Word-Bit Generation

In conjunction with these "derived" reference waveforms and the filter wheel sync pulse from the motor driven filter wheel and choppers, frequency division of the same 400 KHz input clock used to drive the motor to synchronous speed is also used to generate the "bit clock". This clock has a period of precisely 295 μsec which, because of the HIRS data format (of 20 words of 18 bits per word) results in 360 clock cycles for each filter wheel revolution. Through suitable counter-decoder circuits, this waveform not only clocks out the digital data but also is used to control both the start of each A/D conversion and analog multiplexer switching between the LW and SW data channels. The simplified circuit and timing diagram of the bit clock generator is shown in Figure 8.2-9. The circuit consists of an externally resetable (for the purpose of slaving this circuit to the filter wheel sync) symetrical divide-by-118 counter and a serial-in/serial-out shift register, clocked at 400KHz. This register thus has as its output, successive bit clocks which are time delayed by 1.25 μs for the purpose of providing sequential data clocking with the complete avoidance of race problems.

The simplified circuit diagram of the bit and word counter-decoder is shown in Figure 8.2-10. This permits complete bit and word "pointing" control and through use of additional two-input NAND gate circuits (as shown in Schematics 8117791 and 8117787) selective individual bits within the format are addressable.

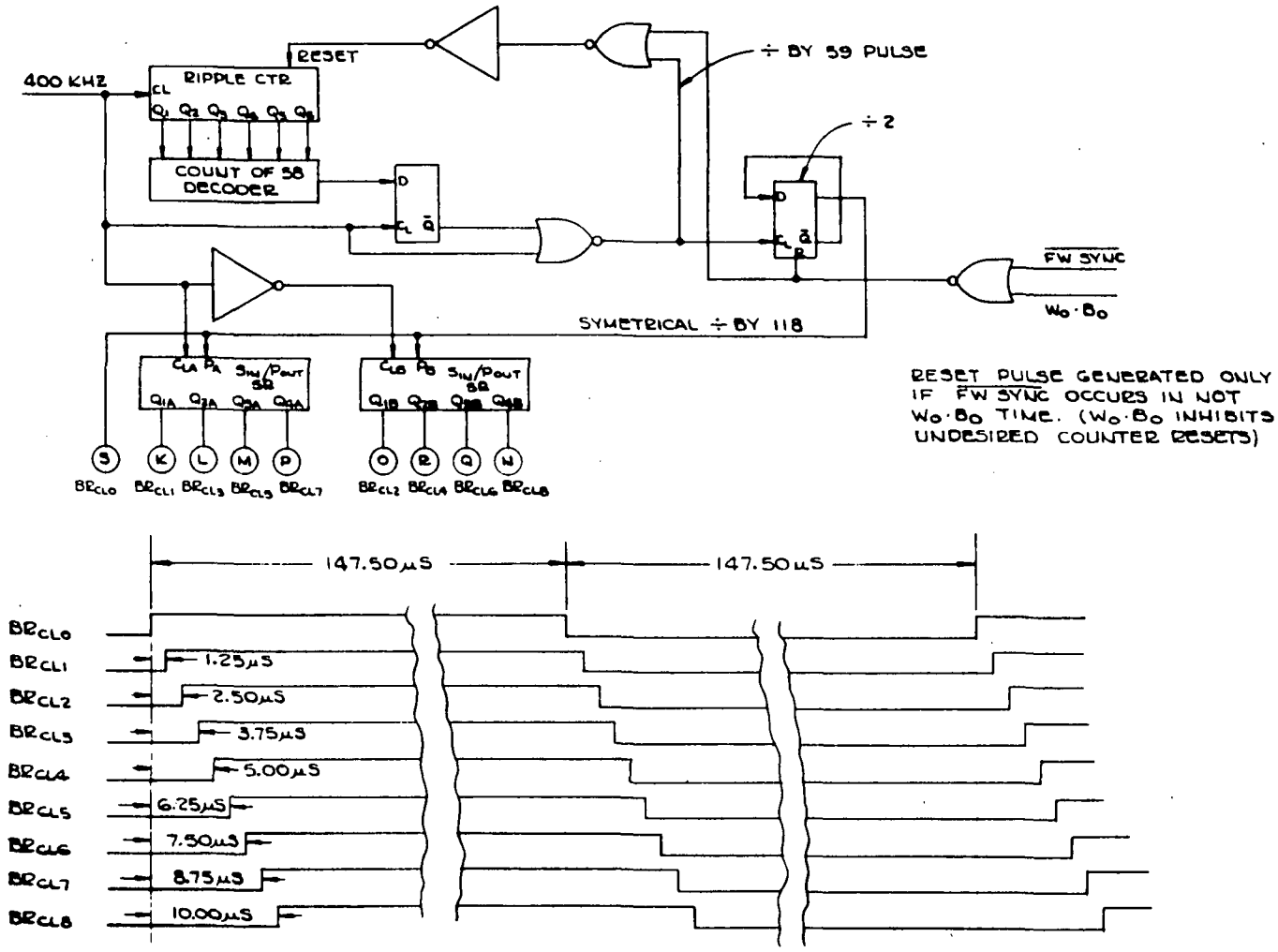
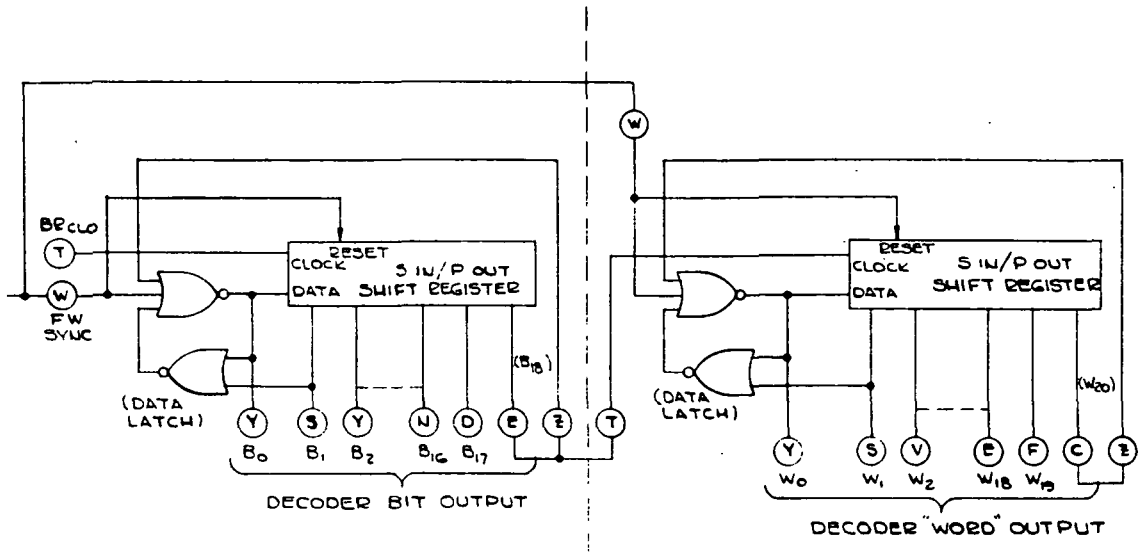


FIGURE 8.2-9 BIT CLOCK GENERATOR CIRCUIT & TIMING DIAGRAM (REF. SCHEMATIC 8118499)



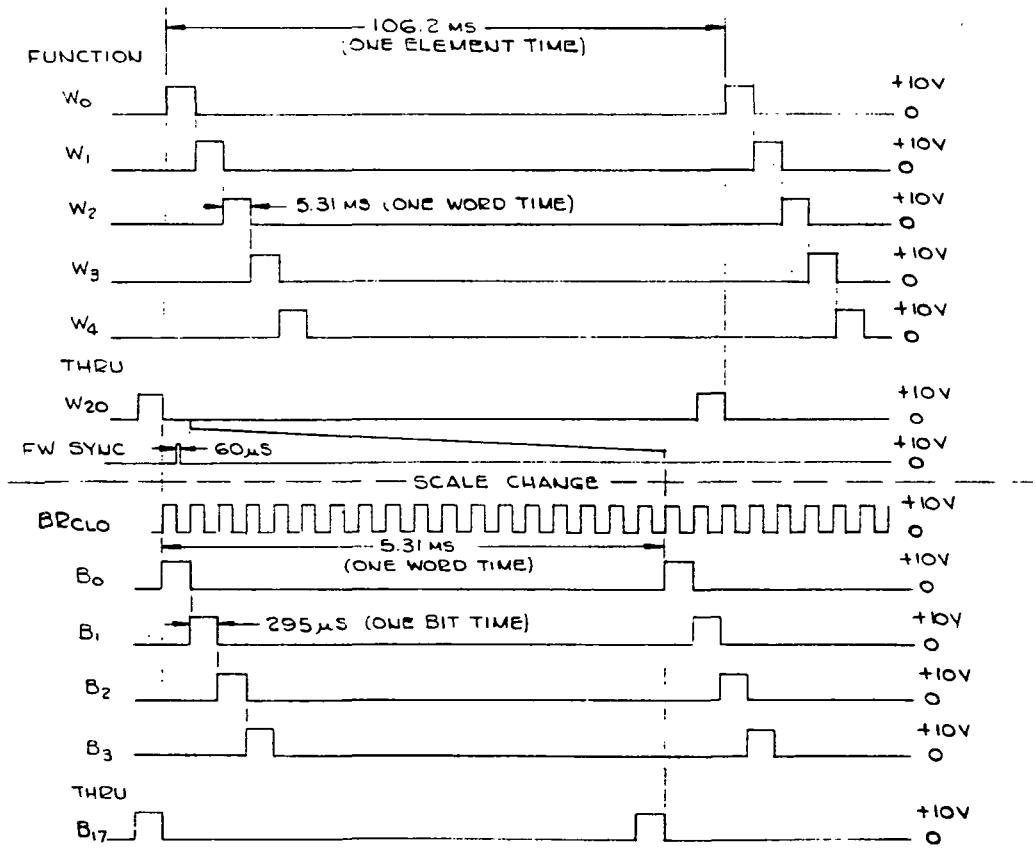


FIGURE 8.2-10 WORD BIT DECODING, PART OF 8117734 (2 BOARDS)

8.2.4 Element-Line Generation

The Scan Element/Scan Line Counters shown on Schematic 8117807 complete the logic necessary to format the data in synchronism with the scan mirror position.

8.2.4.1 Scan Element Counter

The scan element counter is implemented by means of a ripple clocked fully decoded internally reset octal counter. Two input NAND gating is then used to decode selected element numbers which control the four element mirror retrace/forward slewing and the unique data inserted in the format during this interval.

Logic gating upon the board resets the counter to element number zero following element number forty-five, for a total element count cycle of forty-six. This counter is the one counter in the system which is never externally reset. The filter wheel sync pulse advances the counter coincident with the nominal center of the first bit of the first word of a data element. Scan element number forty-two initiates mirror slewing and transfers the inputs of the video processing amplifiers from the detectors preamplifiers to the "positive" phased electronics calibration circuitry. Scan element number forty-three changes the electronics calibration input signal phasing to "negative." Scan element numbers forty-four and forty-five switch the analog channel multiplexer (Schematic 8118511) from the LW/SW Integrators to a nine channel temperature telemetry multiplexer (of Schematic 8118487). Figure 8.2-11 shows the timing diagram of the necessary element number decoding. The data format as it is changed in these last four elements of each line during slew is detailed in Paragraph 2.1.1.1 and Figure 2.1-3.

8.2.4.2 Scan Line Counter

The scan line counter counts the twenty-three lines (zero through twenty-two) contained in each grid. This counter is implemented very similar to the scan element counter except for the decoded counts and the external reset capability. The external reset is applied by the mirror scan system when initializing the mirror at the 300K target position (Encoder Position 84) thereby synchronizing the data format to the scan mirror subsystem. During the last four elements of Scan Line Number zero, the mirror slews to the 270K target position, in like manner slewing to the "Space" target position is during the last four elements of scan line number one, and slew to start of scan is during scan line two. Scan line numbers three through twenty-two are then utilized for earth scanning. At the end of line number twenty-two the mirror forward slews to the warm target rather than retracing to the start of scan. Figure 8.2-11 shows the timing diagram of the necessary line counter decoding.

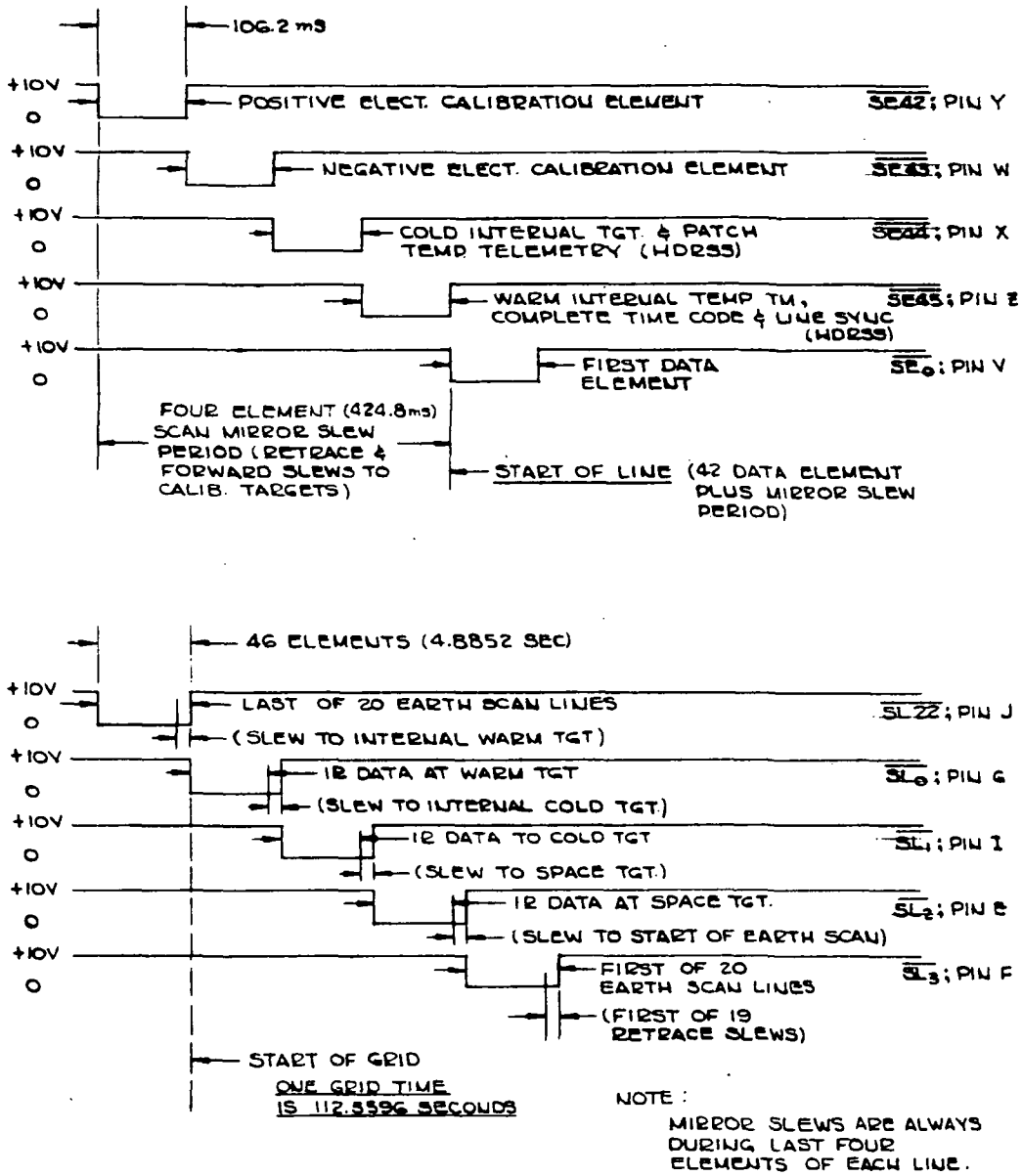


FIGURE 8.2-11 DECODED OUTPUTS OF SCAN ELEMENTS AND SCAN LINE COUNTERS (REF SCHEMATIC 8117807)

8.3 Video Processing System

8.3.1 Long Wave Channel

The long wave (LW) channel processes the chopped radiant signals in Channels 1-10. The LW detector is a Hg Cd Te photo-conductor with a resistance of approximately 40 ohms (including lead resistance). The detector bias current is about 11.4 ma. Signal processing consists of amplifying the signal, band limiting and detecting the amplitude of the signal using a synchronous demodulator/gated integrator.

8.3.1.1 Long Wave Linear Amplifier

A schematic of the LW linear amplifier board is shown in Figure 8.3-1. The input stage is a cascode amplifier with three parallel input transistors. Paralleling N transistors increases the ratio of output signal to amplifier noise by a factor equal to the $\sqrt{N}$. System performance will continue to improve with increasing N until the input impedance of the amplifier approaches the detector impedance or the amplifier noise becomes small relative to detector noise. The amplifier shown in Figure 8.3-1 has a measured spot noise figure of 2 db and a gain of 160 at 904 Hz.

Two post amplifier stages follow the input stage. Each stage consists of an LM 108AH operational amplifier with a nominal gain of 11. Between the two post amplifiers is a clamp circuit. The purpose of the clamp circuit is to eliminate the web signals and channel to channel baseline variations due to radiation offset. These must be eliminated to prevent overloading of the LW demodulator and to minimize noise due to jitter.

A typical LW detector output signal is shown in Figure 8.3-2.

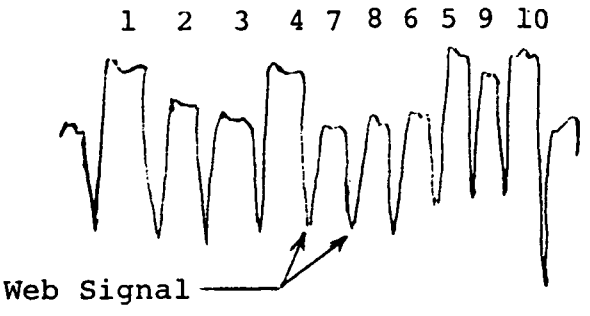


FIGURE 8.3-2 TYPICAL LW DETECTOR OUTPUT WITH ZERO DELTA RADIANCE

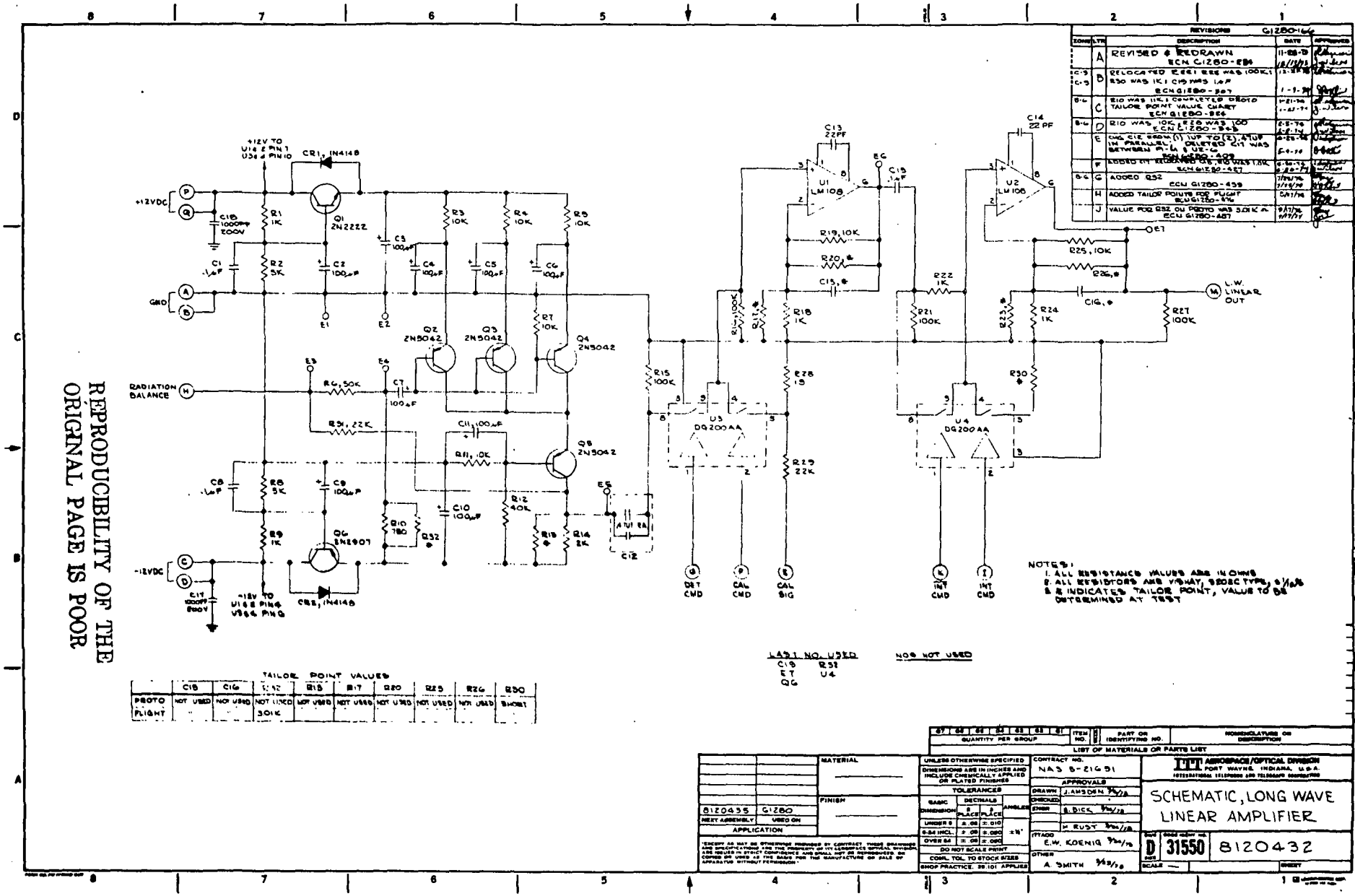


FIGURE 8.3-1 LONGWAVE LINEAR AMPLIFIER

The web signal comes from radiation from the metal support between the optical filters. The radiation offset, which is the variation in the baseline from channel to channel, is caused by differences in transmission through and emission from the optical filters.

A chopped electronic calibration signal is injected into the LW channel at the input of U_1 twice every scan line. Once with a positive amplitude and once with the same negative amplitude. These occur during scan elements 42 and 43, respectively. The magnitude of the calibration signals is incremented one level on each successive scan line. There are a total of 16 levels, starting at zero. These calibration signals are used to measure the gain, linearity and noise of the LW video processing system, except for the input amplifier. The 16 levels exceed the dynamic range of the radiant signals in all channels.

System noise entering the preamplifier via power leads is minimized by decoupling the $+V_{CC}$ (+9 volts) and $-V_{CC}$ (-9 volts) inputs to the preamplifier. This is accomplished by emitter follower regulators Q1 and Q6.

8.3.1.2 Long Wave Demodulator Integrator

A schematic of the LW demodulator integrator board is shown in Figure 8.3-3. The circuitry consists of an input amplifier U1 with a gain of 4, a bandpass filter U2, a synchronous detector U3 and a gated integrator U4.

The design equations and calculated parameters for the LW bandpass filter are shown in Figure 8.3-4. The measured normalized frequency response and phase response of the proto-flight bandpass filter are shown in Figure 8.3-5. The measured gain at 904 Hz was 1.95.

The switch between Pins 4 and 5 of U6 alternately grounds and ungrounds Pin 3 of U3 at a rate of 904 Hz. When Pin 3 is ungrounded the throughput gain of U3 is +1. When Pin 3 is grounded the throughput gain is -1. This synchronously demodulates the chopped input radiant signal. The output of U3 is a unipolar signal whose amplitude is proportional to the difference in radiance between the scene and the chopper wheel reference and whose sign indicates if the scene radiance is greater or less than the reference. Non-synchronous noise and offset voltages will be converted to bipolar AC signals.

The gated integrator integrates the demodulated signal during each channel. The peak value achieved in the gated integrator at the end of a channel is held while it is converted to a binary number in the A/D converter (See Section 8.4). After

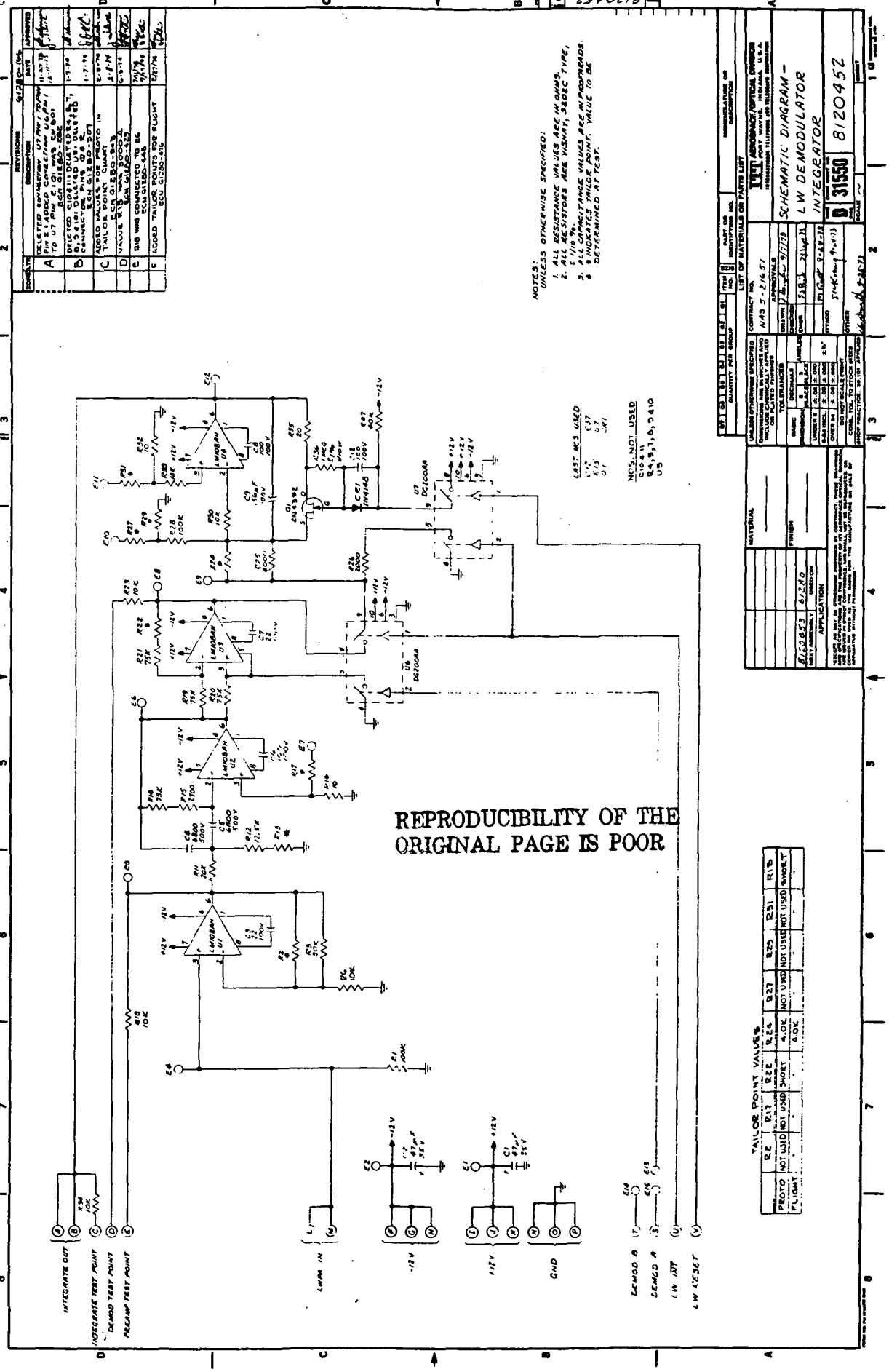
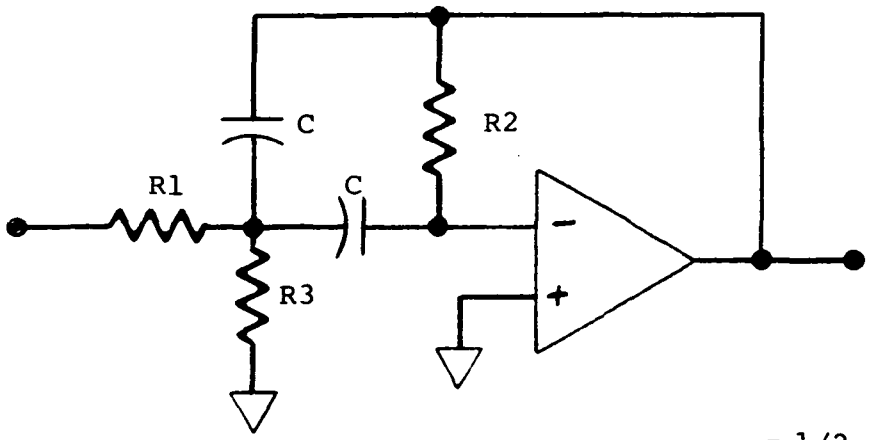


FIGURE 8.3-3 LW DEMODULATOR-INTEGRATOR



$$f_o = \frac{1}{2\pi C}\left[\frac{1}{R_2}\left(\frac{1}{R_1} + \frac{1}{R_3}\right)\right]^{1/2} = 904 \text{ Hz}$$

$$G = \frac{R_2}{2R_1} = 2$$

$$BW = \frac{1}{\pi C R_2} = 600 \text{ Hz}$$

FIGURE 8.3-4 LW BANDPASS FILTER

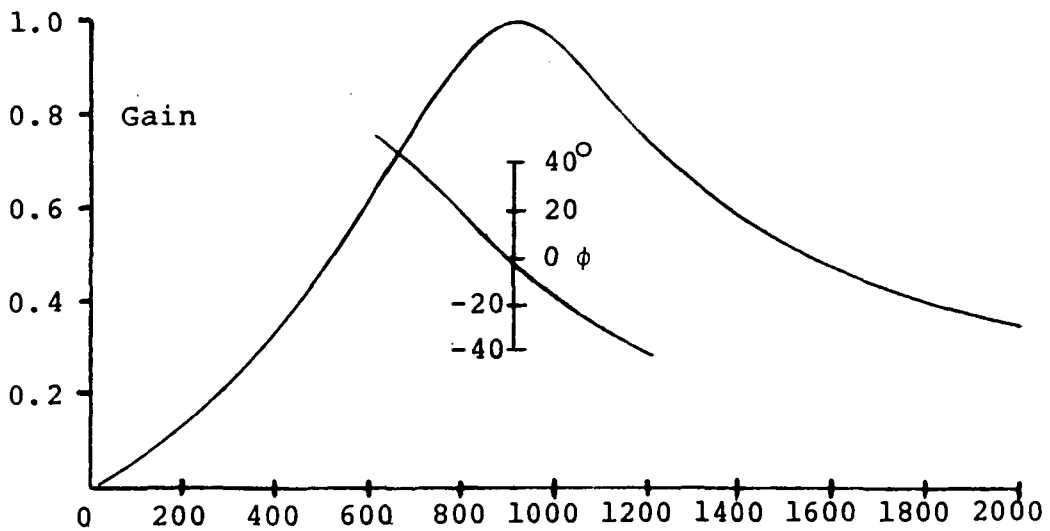


FIGURE 8.3-5 LW FREQUENCY-PHASE RESPONSE

conversion the gated integrator is reset to zero by Q1 and held there until the start of the next channel.

8.3.1.3 Long Wave Channel Performance

The over-all gain in each channel from the input from the detector to the output of the gated integrator is given in Table 8.3-1. These gains are for an input signal chopped at 904 Hz. The temperature coefficient of the gain is -0.20%/^{o}C.

The transfer function of the LW channel can be expressed as:

$$e_o = Ge_{in} \left[1 - Be_{in} \right]$$

Where

G = gain

B = distortion factor

Values for B for each channel in the protoflight unit are given in Table 8.3-1. At maximum input the factor Be_{in} is about 0.015.

The theoretical noise from the long wave detector is equivalent to the Johnson noise of a 50 ohm resistor at 300^{o}K. This noise is equal to 0.9 nanovolts per $\sqrt{Hz}$. The measured noise from the linear amplifier on the test bench was 1.15 nv/$\sqrt{Hz}$. With the amplifier in the system and the optical port blocked the noise was 1.42 nv/$\sqrt{Hz}$. A measurement at the output of the complete system including integration and data conversion resulted in an equivalent input background noise of 1.46 nv/$\sqrt{Hz}$. When radiant input from the detector was permitted into the detector, the noise increased to 1.57 nv/$\sqrt{Hz}$.

Memory in the bandpass filter causes a fraction of the signal from one channel to be present in the adjacent channel. Crosstalk was measured by injecting a large test signal in alternate channels and no signal in adjacent alternate channels. The change in the output of the integrator in the no signal channel versus a change in the amplitude of the test signal channel was defined as the crosstalk. The crosstalk, using the prototype demodulator integrator (PM-1) is 0.07%.

TABLE 8.3-1 HIRS PROTOFLIGHT LW AMPLIFIER CHARACTERISTICS

CHANNEL	1	2	3	4	5	6	7	8	9	10
GAIN X 10^5 (Volts/Volt p-p)	3.52	1.89	2.44	2.44	1.35	1.91	1.91	.81	.82	1.35
B x 10^2	4.61	6.17	4.98	5.89	7.11	5.61	5.61	9.67	7.55	7.05

CHARACTERISTICS AT BASEPLATE TEMP 20^{o}C

8.3.2 Short Wave-Visible Channel

The shortwave (SW) - visible (VIS) channel processes the chopped radiant signals in Channels 11-16 (SW) and Channel 17 (VIS). The SW detector is an InSb photon detector and the VIS detector is an Si photon detector. Signal processing consists of converting the SW and VIS detector current signals to voltage signals, amplifying these signals, time multiplexing the SW and VIS channels, band limiting and detecting the amplitude of the multiplexed signal using a synchronous demodulator/gated integrator.

8.3.2.1 Short Wave-Visible Linear Amplifier

A schematic of the SW-VIS linear amplifier is shown in Figure 8.3-6. The input stages of both the SW (U5) and VIS (U1) channels are current to voltage converter amplifiers. This circuit configuration provides relatively low input noise and allows accurate biasing of the detectors for optimum noise performance. Each input stage is followed by additional voltage amplification. The two channels are combined by time multiplexing into a composite channel at the output of the board.

A chopped electronic calibration signal is injected into the SW and VIS channels at the input of U7 and U3, respectively, twice every scan line. Once with a positive amplitude and once with the same negative amplitude. These occur during scan element 42 and 43, respectively. The magnitude of the calibration signal is incremented one level on each successive scan line. There are a total of 16 levels starting at zero. These calibration signals are used to measure the gain, linearity and noise of the SW/VIS video processing system, except for the input amplifiers. The 16 levels exceed the dynamic range of the radiant signals in all channels except Channel 16.

8.3.2.2 Short Wave-Visible Demodulator Integrator

A schematic of the SW/VIS demodulator integrator is shown in Figure 8.3-7. The circuitry consists of an input amplifier, U1, with a gain of 2, a gated bandpass filter, U2, a synchronous demodulator, U3, and a gated integrator, U4.

The design equations and calculated parameters for the SW/VIS gated bandpass filter are shown in Figure 8.3-8. The measured normalized frequency and phase response of the proto-flight bandpass filter are shown in Figure 8.3-9. The measured gain at 396 was 1.90.

Two switches are shown in Figure 8.3-8. Switch S1 is a clamp circuit. The purpose of the clamp circuit is to eliminate the web signals and channel to channel baseline variations

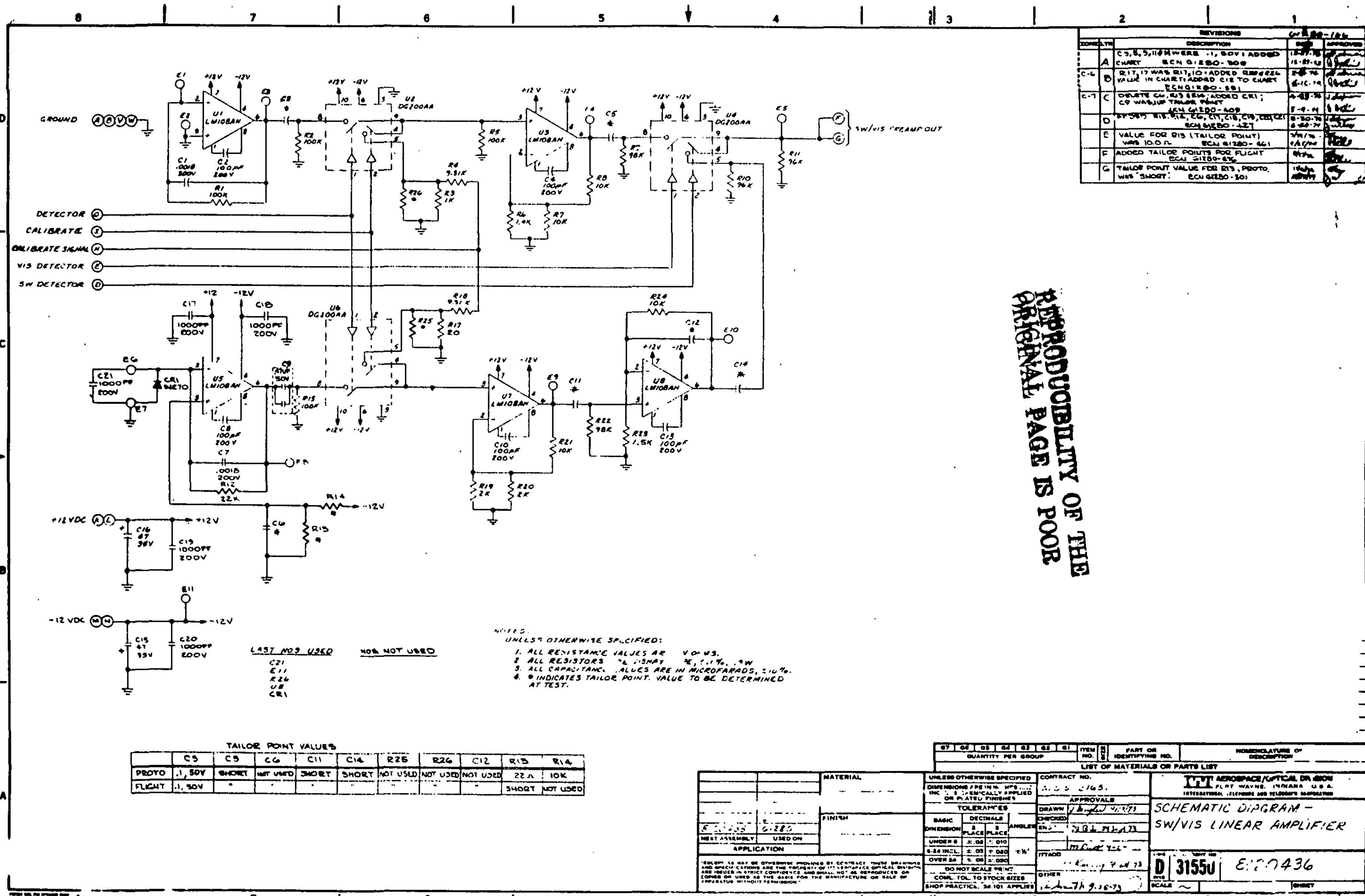


FIGURE 8.3-6 SW/VIS LINEAR AMPLIFIER

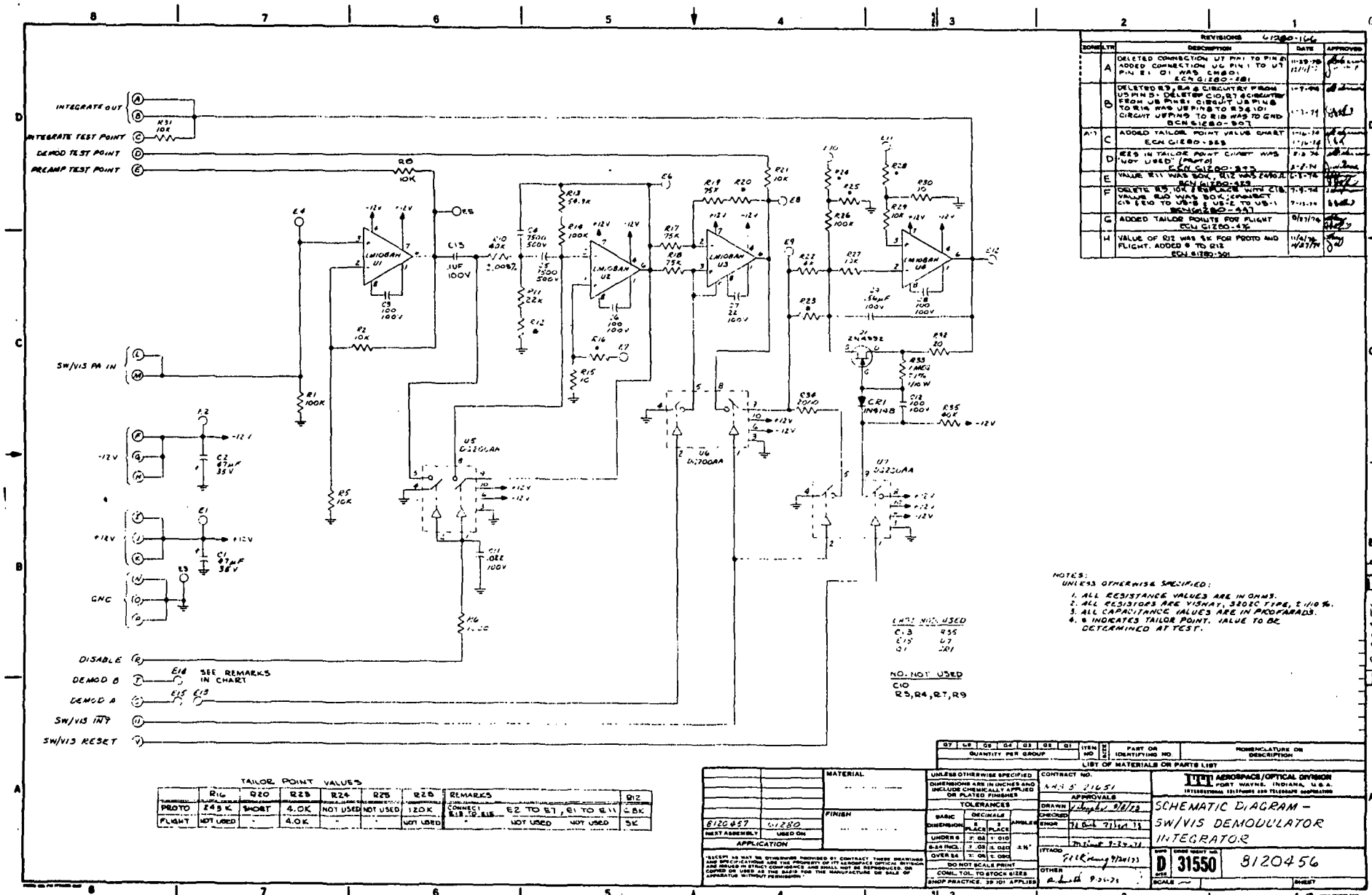
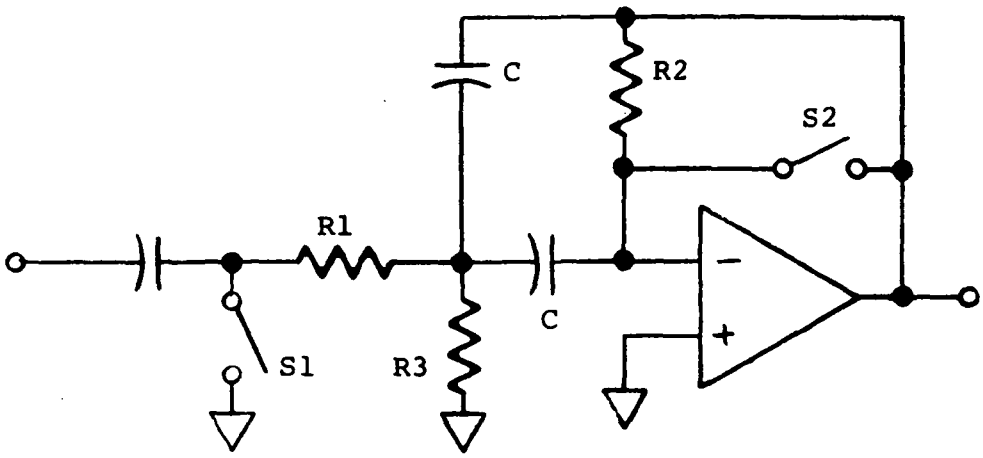


FIGURE 8.3-7 SW/VIS DEMODULATOR/INTEGRATOR



$$f_o = \frac{1}{2\pi C}\left[\frac{1}{R_1}\left(\frac{1}{R_1} + \frac{1}{R_3}\right)\right]^{1/2} = 425 \text{ Hz}$$

$$G = \frac{R_2}{2R_1} = 1.94$$

$$BW = \frac{1}{\pi C R_2} = 274 \text{ Hz}$$

FIGURE 8.3-8 SW/VIS BANDPASS FILTER

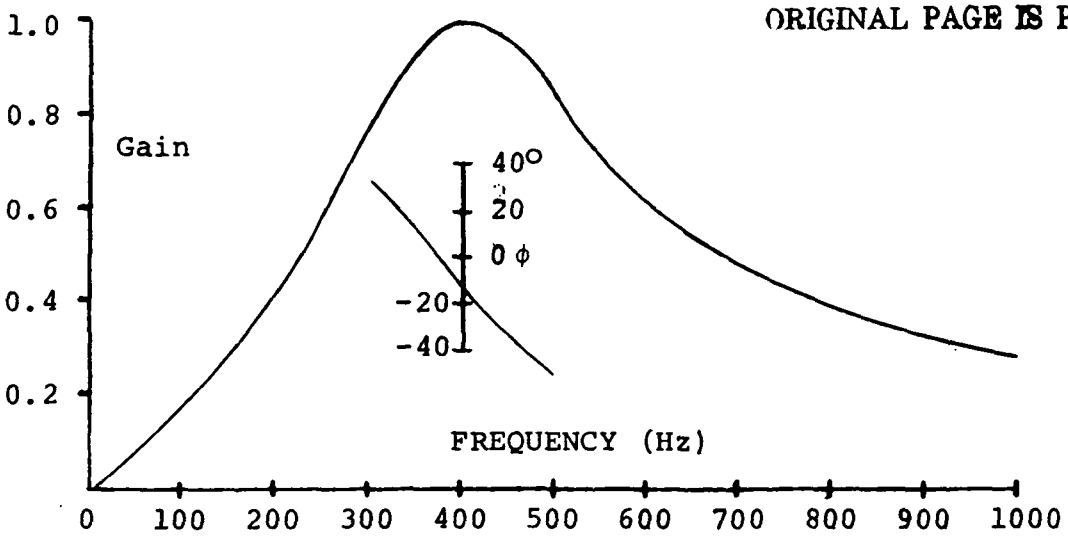


FIGURE 8.3-9 SW/VIS FREQUENCY-PHASE RESPONSE

due to radiation offset. A typical SW detector output signal is shown in Figure 8.3-10. The web signals come from radiation from the metal supports between the optical filters. The radiation offset, which is the variation in the baseline from channel to channel, is caused by differences in transmission through and emmission from the optical filters.

The second switch, S2, is used to discharge the energy stored in the bandpass filter at the end of each channel to prevent channel to channel crosstalk errors. The crosstalk without S2 is about 3%.

Closing S2 lowers the value of R2 (See Figure 8.3-8) to nearly zero. From the design equation it can be seen that this lowers the gain to nearly zero and raises the center frequency and bandwidth to high values. Hence, the filter will respond rapidly to the zero input established by S1. Thus the controls between channels is eliminated. Measured values in the protoflight unit are less than 0.02%.

The switch between Pins 4 and 5 of U6 alternately grounds and ungrounds Pin 3 of U3 at a rate of 396 Hz. When Pin 3 is ungrounded the throughput gain of U3 is +1. When Pin 3 is grounded the gain is -1. This synchronously demodulates the chopped input radiant signal. The output of U3 is a unipolar signal whose amplitude is proportional to the difference in radiance between the scene and the chopper wheel reference and whose sign indicates if the scene radiance is greater or less than the reference. Non-synchronous noise and offset voltages will be converted to AC signals.

The gated integrator integrates the demodulated signal during each channel. The peak value achieved in the gated integrator at the end of a channel is held while it is converted to a binary number in the A/D Converter (See Section 8.4). After conversion, the gated integrator is reset and held to zero by Q1 until the start of the next channel.

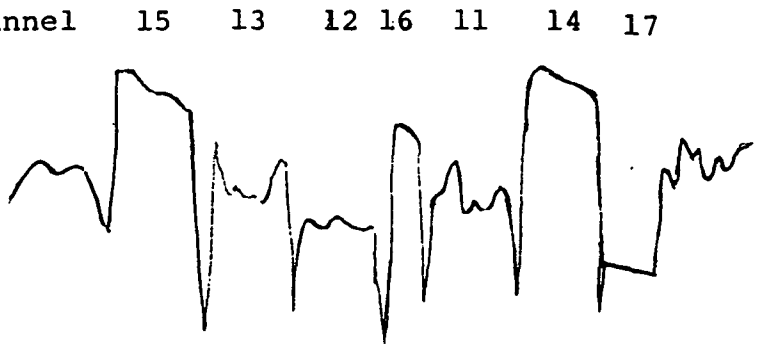


FIGURE 8.3-10 SHORTWAVE DETECTOR OUTPUT

8.3.2.3 Short Wave-Visible Channel Performance

The over-all gain in each channel from the detector input to the output of the gated integrator is given in Table 8.3-2. These gains are for an input signal chopped at 396 Hz. The temperature coefficient of gain is less than 0.05%/^{o}C. The measured non-linearity over the dynamic range of the input radiant signal in all channels is 0.1% or less.

TABLE 8.3-2

HIRS PROTOFLIGHT SW-VIS AMPLIFIER CHARACTERISTICS

Channel	Gain x 10^6 (Volt/Amp p-p)
11	10.5
12	10.5
13	10.5
14	10.5
15	10.5
16	1.7
17	.83

CHARACTERISTICS AT BASEPLATE TEMP 20^{o}C

Principal noise sources in the SW channels are detector shot noise, input amplifier noise, pickup noise, and noise resulting from short term changes in the SW chopper frequency (jitter). The calculated shot noise in the detector (at 40μa background current) is 3.6 pico-amperes. The measured equivalent noise current of the amplifier is 2 pico-amplifiers. The measured equivalent noise current from all sources except jitter was 6.2 pico-amperes. This includes the noise currents listed above and a degradation factor of 1.5 to account for pickup noise.

Noise contributed by jitter is related to the amplitude of the jitter and the amplitude of the signal in each SW channel. A scheme was devised which cancels most of the effect of the jitter. (See Q Report Jan-Mar 1974 for a detailed derivation of the cancellation technique). The efficacy of this scheme is illustrated in Table 8.3-3. A chopped constant amplitude test signal was injected into the SW demodulator/integrator and output of the HIRS was processed in a computer. The mean and standard deviation in each channel was computed using 42 samples.

TABLE 8.3-3

INTEGRATE PERIOD COMPENSATION RESULTS

A. Fixed integrate period; integral number of cycles

Mean			Standard Deviation		
M 11	=	3881	SD 11	=	15.729--
M 12	=	3877.36	SD 12	=	9.54277
M 13	=	3874.1	SD 13	=	17.4954
M 14	=	3872.48	SD 14	=	17.2135
M 15	=	3883.79	SD 15	=	12.8529
M 16	=	903.31	SD 16	=	4.55582
M 17	=	1585.5	SD 17	=	8.88202

B. Fixed integrate period; compensated

Mean			Standard Deviation		
M 11	=	3721.33	SD 11	=	.570266
M 12	=	3718.98	SD 12	=	.562577
M 13	=	3719.31	SD 13	=	.748595
M 14	=	3719.9	SD 14	=	.370202
M 15	=	3718.62	SD 15	=	.660834
M 16	=	555.286	SD 16	=	.507779
M 17	=	972	SD 17	=	.220863

The residual noise shown in Table 8.3-3B is primarily due to quantization noise in the A/D converter. Similar reduction in noise due to jitter was obtained with radiant inputs. However, some jitter noise occurs because of non-uniformity of the optical filters (e.g., see Figure 8.3-10 Channels 11 and 13).

8.4 Data Processing Electronics

8.4.1 General

The function of the data processing electronics is to time multiplex the analog data of both the LW and SW video processing electronic integrators (Section 8.3) and the precision internal temperature analog signals to an analog to digital (A/D) converter. This digitized data is then formatted with various housekeeping digital information consistent with the requirements of the HIRS bi-phase serial data output data format of Paragraph 2.1.1.1. The A/D conversion electronics consists of an input analog multiplexer, a unity gain absolute value analog circuit (also providing a digital "sign bit"), and a successive approximation A/D converter. The method of providing short term storage of this digitized data for proper word formatting and word parity insertion at the output serial data rate is then covered in this section along with NRZ (shift register data) to bi-phase data conversion. Paragraph 8.5 describes the manner in which spacecraft time code data is extracted from the pulse width modulated one-hundred pulse per second serial input to HIRS and its storage, updating and formatting within the HIRS.

8.4.2 Analog to Digital Conversion

8.4.2.1 General

This discussion is limited to that portion of the HIRS data handling electronics which provides for the converting to encoded digital information, those analog signals present on the three analog inputs to the Analog MUX/Absolute Value board (Sch. No. 8118511); the LW Analog Data on Pin 36, the SW Analog Data on Pin 33 and the Temp TM Analog Data on Pin 32. In addition the format of this digital data following A/D Conversion will be covered in detail.

The sectioning of this subsystem will be between the circuitry used for Analog Signal Absolute Value conversion, (see Figure 8.4-1) analog multiplexing and the combination of the A/D Converter DAC, its feedback decision comparator and the successive approximation control logic.

8.4.2.2 Absolute Value Conversion

The first step in processing these Analog signals is to convert all inputs to an absolute value because the A/D Converter can convert only positive voltages of approximately 0 to +6.4 volts. Therefore an absolute value circuit accepting ±6.4 volts can, with the aid of an input polarity comparator, extend the A/D Converters effective range from 12 to 13 bits (12 bits plus sign). Referring to Schematic 8118511 of the

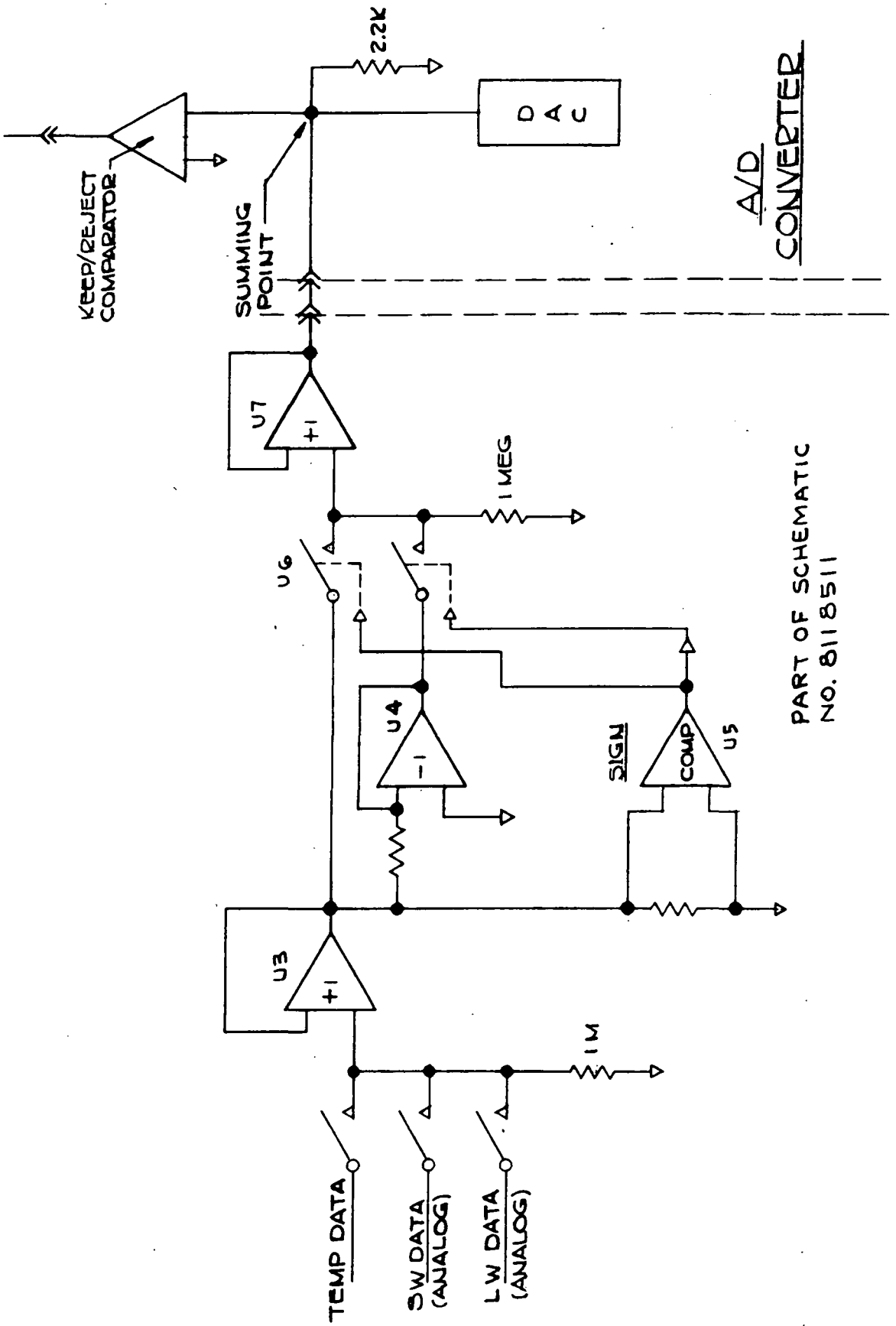


FIGURE 8.4-1 ANALOG MUX/ABSOLUTE VALUE

Analog MUX/Absolute Value Board, U1 and U2 can be considered an analog multiplexer whose output is connected to U3, a unit gain non-inverting buffer. Analog Switches U1 and U2 are controlled by and through Logic Element U9 such that simultaneous application of two or more of the analog inputs are never applied to U3.

The output of Buffer U3 is applied to each of the following: U5, a polarity comparator, U4, a unity gain inverting amplifier and to U6 which is a single pole, double throw analog switch. (The output of U4 goes to the other pole of the Switch U6). This analog switch, U9, is controlled by the digital circuits consisting of an input polarity comparator U5 and logic elements U8, U10 and U11. The purpose of these digital circuits is to position the switch common to the pole having a positive voltage (Note that a voltage of zero volts is not a positive or a negative voltage and results in an uncertain switch position). The function of flip-flop U11 and gating U8 and U10 is to provide storage of the polarity comparator output coincident with the start of A/D conversion, thereby preventing switch U6 from switching during the converter aperture time (that time required to complete the successive approximation sequence).

Following the start of A/D Conversion, the output of Switch U6 will then remain connected to the unity gain amplifier (either U3 or U4) whose output is positive. The switch output is then buffered by U7, a unity gain non-inverting amplifier. Amplifiers U3 and U7 are incorporated to make the analog switching impedances negligible and provide an output to the A/D Converter from a very low source impedance (an essential consideration when considering a total resolution of 13 digital bits.

8.4.2.3 A/D Conversion

The analog output of the Analog MUX/Absolute Value board on Pin 29 becomes the input to the A/D Converter (Schematic 8120489) on Pin X. The absolute value analog (positive) voltage is converted to a "positive" current by Resistor R9 and parallel 5K resistors in Element U3. This current is terminated to analog ground through Resistor R5. Resistor R5 also terminates the precisely binary weighted "negative" current outputs of the 12 bit DAC. The voltage appearing across R5 will therefore be positive, negative or zero depending upon whether the DAC withdraws less current, more current or an equal current out of this "summing node" than that contributed by the Absolute Analog Signal. It is therefore apparent that within the limits of input current from zero to the absolute value of DAC output full scale current, a balance at the input of Comparator U1 can be achieved to within ± ½ of the LSB (least significant bit) current output of the DAC.

Since the DAC can be made to act as negative "feedback" with the "current balance" comparator's input functioning as the summing junction, it becomes the function of the A/D Logic board (Schematic 8117771) to close the control loop between the decision comparator output and the input bit control lines of the DAC.

To accomplish this task, the A/D Logic board essentially provides textbook successive approximation converter control. For 12 bits, the feedback balance current available from the DAC is 2^{12} -1 (or the sum of 2^{0} thru 2^{11}) bits or decimal 4095. At the command to convert analog data, all bits are turned on except the MSB (most significant bit) which is the 2^{11} bit. The comparator will then decide if the DAC current output is greater or less than that required to provide a balance. If it is greater than that required, the 2^{11} bit will remain off and the 2^{10} bit will be turned on to allow the comparator to make a new decision. If the current was less than that required, the A/D logic will turn on the 2^{11} bit coincident with the turning on of the 2^{10} bit. The turning off of each bit in sequence from 2^{10} to 2^{0} continues at a rate of ten microseconds per bit to permit the transients introduced in the loop to settle, the comparator to make its decision, and to allow for circuit propagation delays.

When the comparator's decision to either turn on or leave off the 2^{0} bit is made, the conversion is complete.

Since serial data is the form of the HIRS data output, the converted data is used only in serial form. This serial data is stored in static "serial in - serial out" shift registers described in Paragraph 8.2.5. A shift clock for this data, occurring at the 100 KHz rate (with a clocking edge delayed 2.5 μseconds from valid data, is also one of the outputs of this board.

In addition to providing DAC control logic, serial output data and clock for this data, the A/D logic board provides the required formatting of these 12 bit converted data words. The HIRS output word is eighteen bits in length. All data words consist of four initial "zero" bits, then the "sign" or analog polarity bit followed by the twelve digitizing bits of the converter. Although these add up to only seventeen bits, the eighteenth bit or "word parity bit" is added by circuitry described in Paragraph 8.3.6. Therefore, rather than outputting only twelve data bits, the A/D Logic board formats these twelve converted data bits and the sign bit into seventeen bit words as described above.

8.4.2.4 A/D Converter Accuracy

The A/D Converter used on the PFM HIRS was found during board tests to have a maximum differential non-linearity

error of about +0.6 or +6/10 of the LSB. This is well within the requirement of ±½ LSB total error, particularly when any A/D converter can, at best, resolve analog signals to only one LSB. Figure 8.4-2 depicts and tabulates the linearity error. In addition, the converter was tested over its total dynamic range to verify the absence of "missing codes" and to demonstrate converter monitoricity. Figure 8.4-3 depicts the temperature dependent errors induced over a temperature range from 0°C to +50°C. The dominant factor was the converter gain change over temperature equivalent to -0.05 bits per °C at full scale between +25°C and +50°C. This is very nearly a -10 ppm temperature coefficient at full scale.

8.4.3 Digital Data Formatter

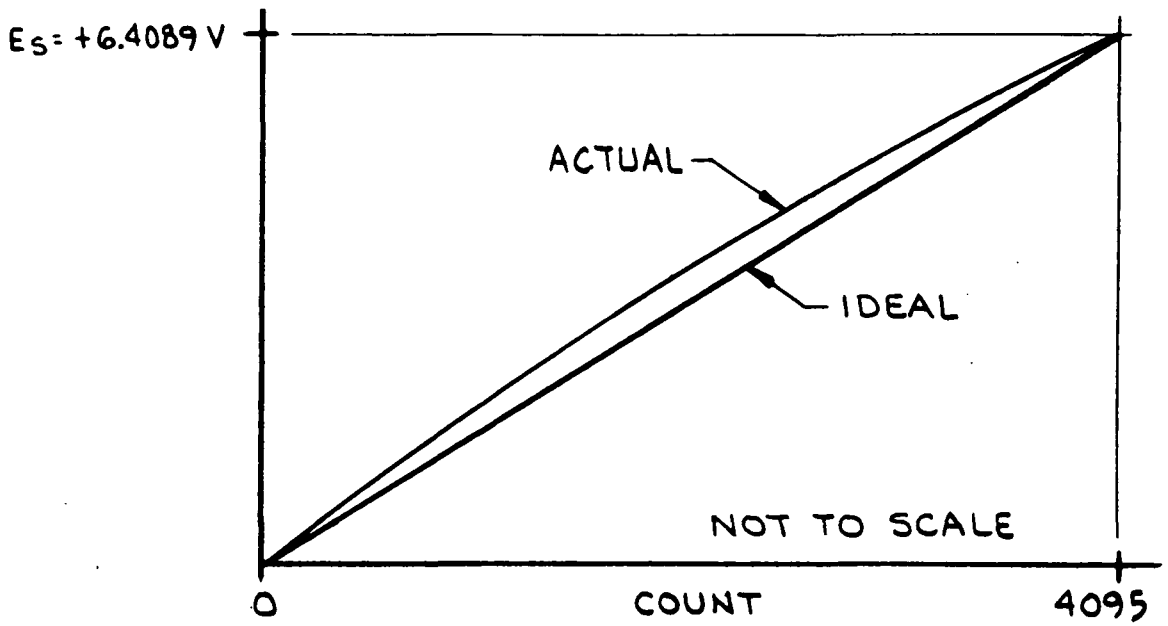
The thirteen bit successive approximation A/D converted digital data (twelve bits absolute value plus sign) is converted at 100 KHz clock rate at the end of integrating the spectral channel demodulator signals. These bursts of serial data must be stored at the 100 KHz data rate at the time of conversion, and held in memory until the proper time (as determined by the word pointer or "fully decoded word number counter") for shifting the data onto the main "Formatted Data Bus" at the instrument output bit rate of 360 bits/106.2 ms (3389 + bits/sec).

This short time digital data storage (and data rate conversion) could have been implemented with as few as six registers if time sharing of the registers had been attempted through use of complex input gating. However, the use of exceedingly low power complimentary MOS logic (exclusively) permitted the use of a total of seventeen, seventeen-bit serial-in/serial-out shift registers, each dedicated to temporarily storing a particular digital spectral channel word and/or digital temperature word. With this particular circuit design, the complexity of the register input control gating and the digital multiplexing of the register outputs was substantially reduced.

Figure 8.4-4 illustrates, in an unsimplified form, the circuit details of the converted digital data storage/formatter registers. All seventeen register data inputs are common and connected to the serial data output of the A/D converter. The clocking input of each register is from an AND/OR select gate which, in conjunction with two "pointers," the data conversion pointer ($W_N \cdot B_N$) and the Word Pointer (W_N), provides steering of the gated clock of the A/D converter to sequentially load data into a particular register and steering of the bit clock to sequentially shift out contents of a particular register on the data buss. Note that the bit clock steering signal (W_N) also controls the digital multiplexer switch which places

NOTE: THIS DATA INCLUDES LINEARITY ERROR OF HP3460B DVM

LINEARITY ERROR: MOST CONSERVATIVE METHOD (USING FULL SCALE AS CALIBRATION)



LARGEST LINEARITY ERRORS

COUNT	ERROR IN VOLTS	ERROR IN BITS	COUNT	ERROR IN VOLTS	ERROR IN BITS
32	+.0006 V	.383	512	+.0009V	.575
64	+.0007 V	.447	1024	+.0009 V	.575
128	+.0007 V	.447	2048	+.0006V	.383
256	+.00086V	.5495			

DIFFERENTIAL NON LINEARITY

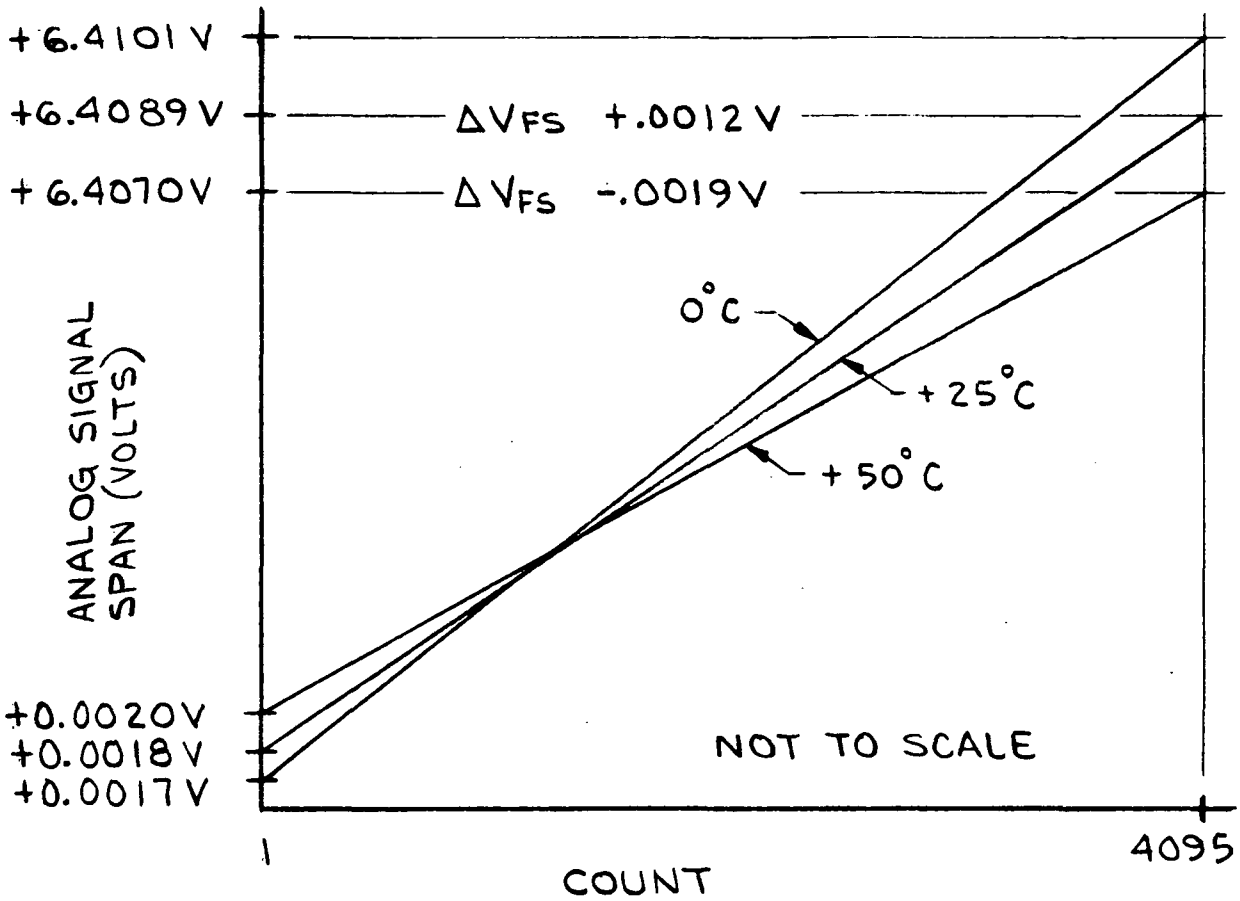
$$\Delta E_N = E_S\left(\frac{1}{2^n - 1}\right) = \frac{6.409V}{2^{12} - 1} = .001565V = \frac{\text{VOLTS}}{\text{BIT}}$$

LARGEST DIFFERENTIAL NON LINEARITY ERROR

$$E_{DL} = \frac{\Delta E - \Delta E_N}{\Delta E_N} = \frac{.0025 - .001565}{.001565} = .597$$

(WHERE ΔE IS ACTUAL MEASURED STEP VOLTAGE)

FIGURE 8.4-2 A/D CONVERTER ACCURACY



FULL SCALE TEMPERATURE COEFFICIENT IS APPROXIMATELY -10.0 PPM/°C.
THIS IS EQUIVALENT TO -0.05 BITS/°C (AT FULL SCALE) BETWEEN +25°C AND +50°C.

FIGURE 8.4-3 A/D CONVERTER - TEMPERATURE VS ACCURACY

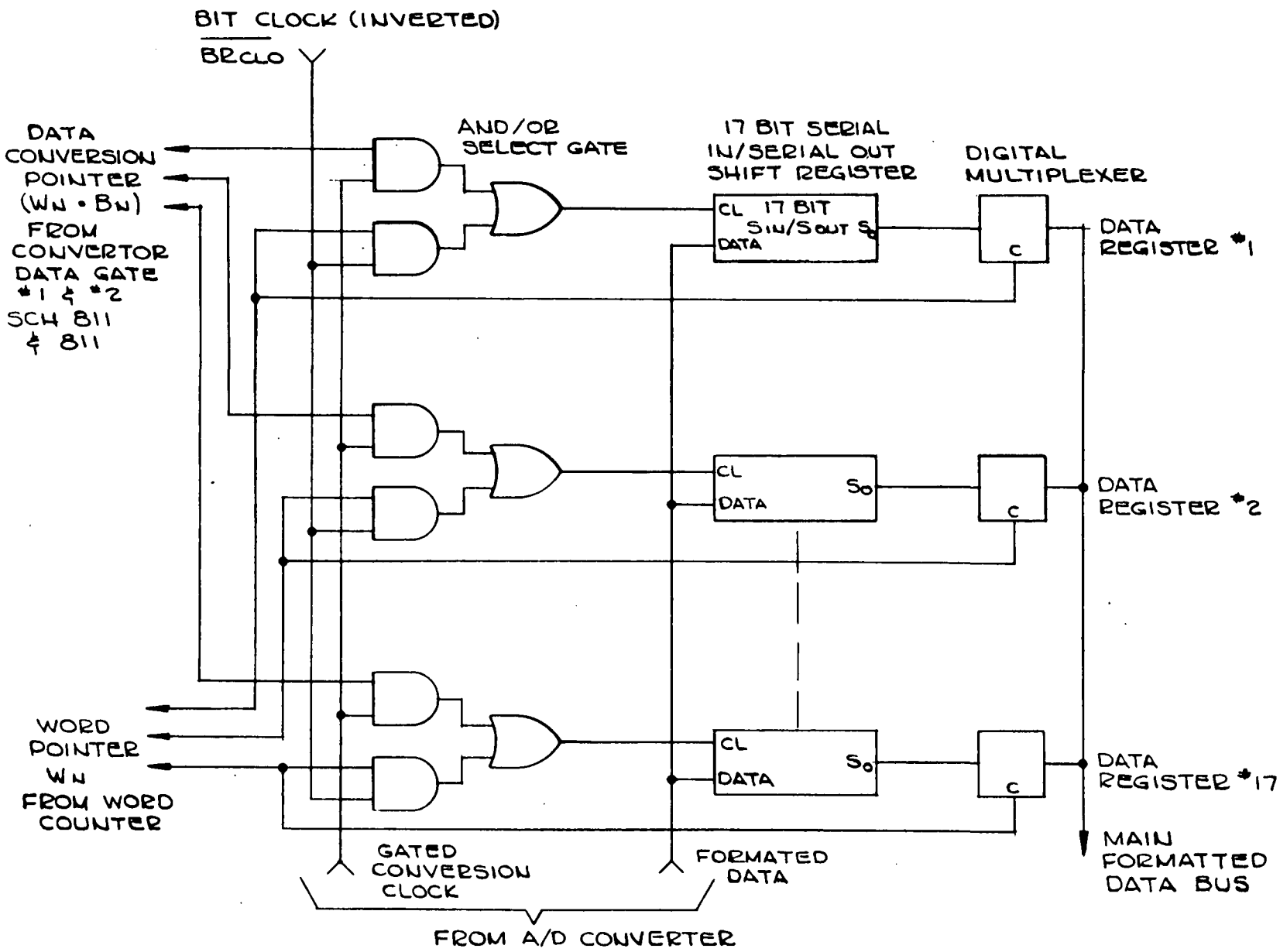


FIGURE 8.4-4 CONVERTED DIGITAL DATA STORAGE/FORMATTER REGISTER

the register being cleared (data shifted out) onto the main formatted data buss.

The seventeen bit serial data words on this buss are then no longer stored within the HIRS. The following section will describe how odd parity is added as the eighteenth bit of each word and how these NRZ WORDS (shift register outputs) on the buss are converted to bi-phase data (clock and data comfined) for outputting to the spacecraft high data rate recorder.

8.4.4 Parity Generation/Insertion--Serial NRZ to Bi-Phase Data Conversion

A simplified schematic of the digital circuitry necessary to determine "ODD" parity and insert this error detection bit into the otherwise unused last or 18th bit slot of each HIRS output digital word is shown in Figure 8.4-5. In addition, the method of converting the NRZ serial data to bi-phase instrument output is also shown. Figure 8.4-6 is a timing diagram for a typical data word input for the Parity generator circuit of Figure 8.4-5.

The NOR Gate output D2-3 clocks a divide by 2 flip-flop (with Q Output D1-1) at each zero level bit of the Formatted Data buss input (at Input D2-2). Following the start of the 17th bit the flip-flop output Q (D-1) will be at a logic zero level if the number of zero levels in the data were even or its corollary that the number of logic one levels were odd. D1-1 will be a logic one if the opposite is true (number of zeroes were odd or the number of ones were even). The data format was planned such that in each word of 18 bits, the number of ones is made odd by parity insertion. Therefore, D1-1 is the proper logic level to insert directly into the serial stream; however, this information must be stored for use in the last bit prior to updating D1-1 at the start of that last bit. The flip-flop with Q output D1-13 stores this parity information in the center of Bit 17. The input B_{17} (actually the pointer for Bit Number 18) then transfers the data path from Gate D3-10 to Gate D4-10 which injects parity data onto the buss in the 18th bit slot. Differentiating the leading edge of Signal B_o to obtain an approximately 1 μsec pulse provides the reset to initialize both flip-flops prior to examining the bits of a new seventeen bit word. The gate output D4-11 logic "OR's" the two paths described above (data/parity). Exclusive ORing of this Complete Serial Data (NRZ) with bit clock $BRCL_5$ converts the NRZ data to Bi-Phase data. A flip-flop with delayed clocking insures that no glitches appear on the output Bi-Phase data. A logic level converter follows this flip-flop to bring the output level from a range 0V to +10 VDC to 0V to +5.7 VDC to provide a proper interface between the flip-flop and the output buffers. The timing diagram on Figure 8.4-7 illustrates a typical conversion of an NRZ digital data word to bi-phase data.

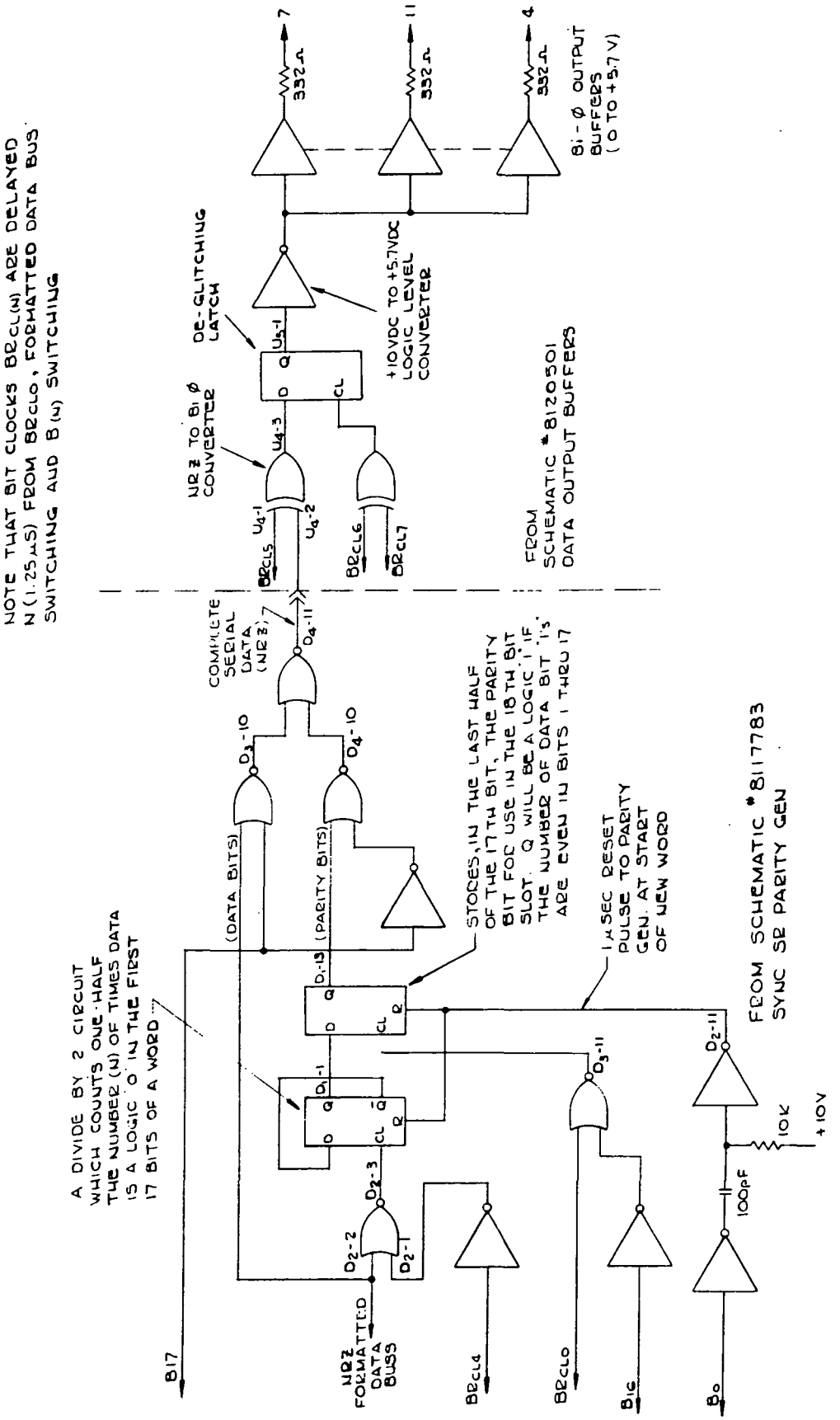


FIGURE 8.4-5 SIMPLIFIED SCHEMATIC OF PARITY GENERATION/NR2 TO BI-PHASE DATA CONVERSION

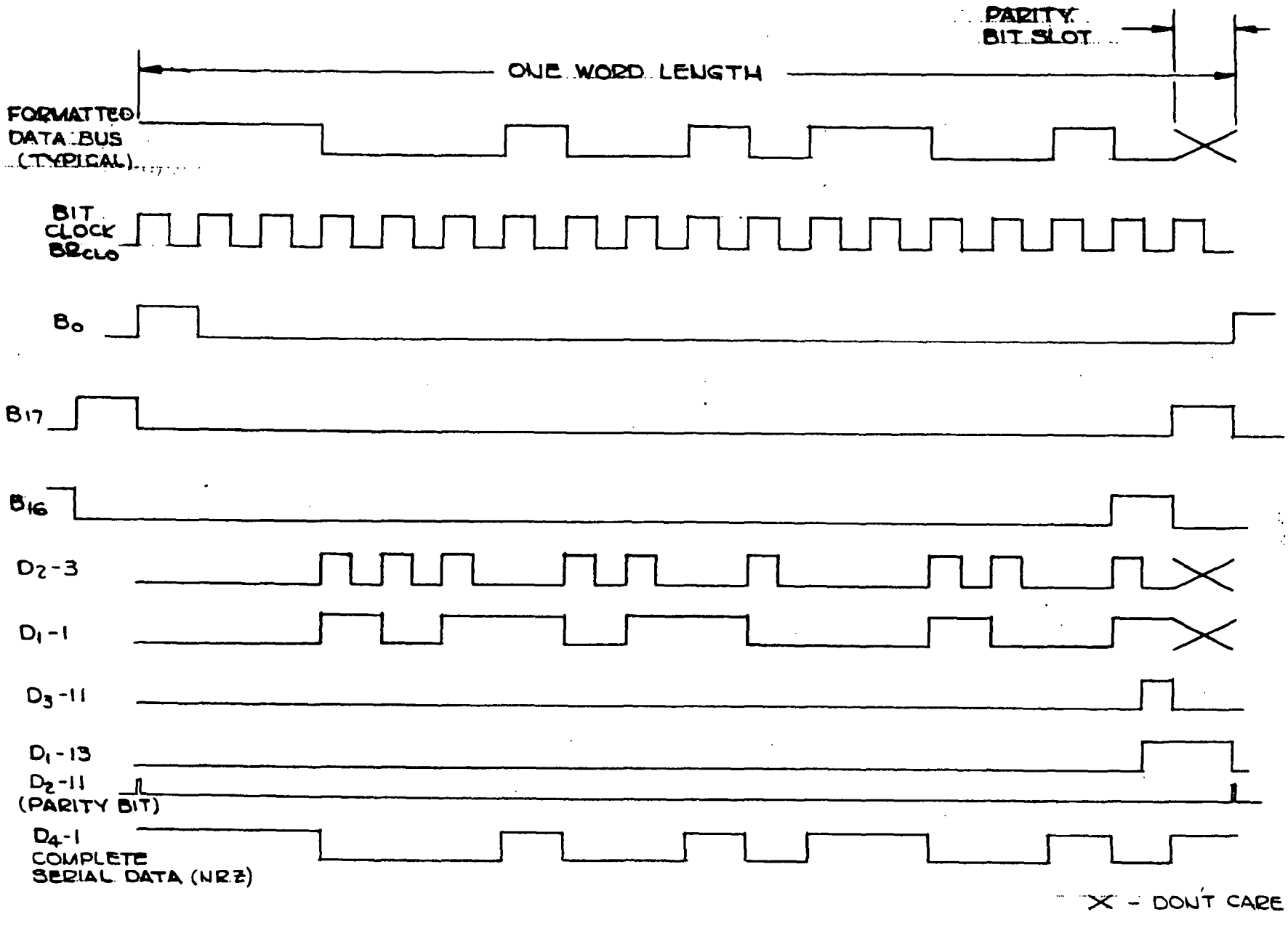


FIGURE 8.4-6 TYPICAL PARITY GENERATOR TIMING DIAGRAM

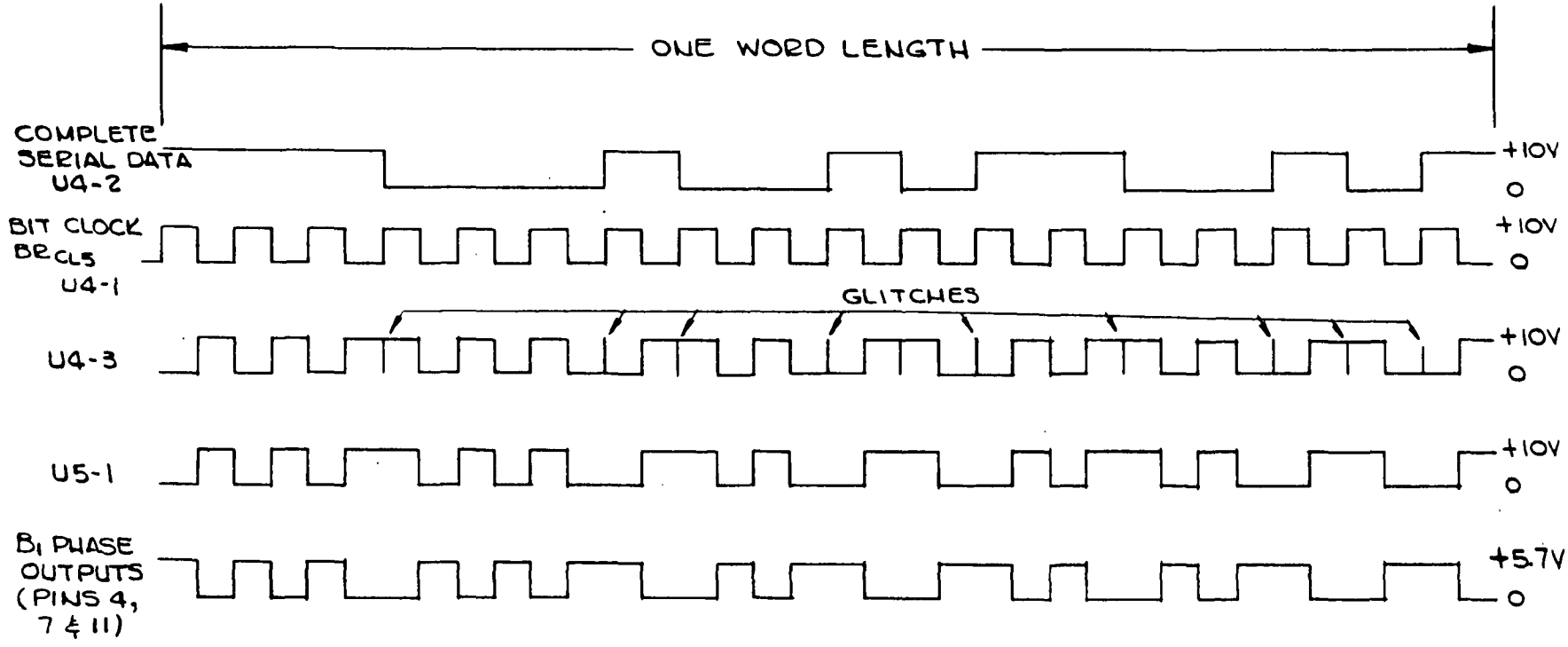


FIGURE 8.4-7 TYPICAL NRZ TO BI-PHASE CONVERSION
(REFER TO DATA OUTPUT BUFFERS PORTION OF FIG. 8.4-5)

8.4.5 Time Code Electronics

8.4.5.1 General

The Spacecraft Command and Clock Subsystem (CCS) provide the HIRS with a pulse width modulated (PWM) NASA 36 bit, 100 pulse per second (PPS) time of year signal designated the ME signal. A companion signal to the ME signal is the PWM strobe (MST). This signal is a gated series of 0.5 millisecond (MS) strobe pulses occurring 3.5 ms after the start of the PWM information and sync bits. By logic "anding" the ME signal with the MST signal, every other group of five ME bits are extracted while the five "fill zeros" separating the five useful bits (a sub-frame identification bit plus four binary coded decimal (BCD) data bits) are not.

The ME signal consists of a series of one hundred binary elements per one second frame. Each binary element or "index count interval" is a precise ten ms period and within that period a "logic 0" is +5.25 ±0.75 VDC (hereafter called +6V) for 2 ms and +0.2 $^{+0}_{-0.1}{}^{0.5}$ vdc (hereafter called OV) for 8 ms. For a "logic 1", the level will be +6V for 6 ms and OV for 4 ms.

In the series of 100 PWM bits, the first bit, eleventh bit, twenty-first bit and etc. through to the ninety-first bit are called the sub-frame identification bits (termed P_0, P_1, P_2 through P_9). Only the P_0 bit is a "logic 0" while P_1 through P_9 are "logic 1's". These P_N bits in the ME signal are always strobed by the first pulse in the group of gated five bits.

8.4.5.2 Circuit Design

8.4.5.2.1 Time Code Processor

It is the function of the Time Code Processor board (Sch. 8117738) in the HIRS to utilize both the ME and MST signals to produce a once per second pulse (ONE SEC MARK) coincident with the P_0 element and to strobe only those other elements (the four bits following the P_0 through P_9 sub-frame identification bits) which contain time of year data. (See Figure 8.4-8 and 8.4-9). This is accomplished by envelope detecting the MST such that only the P_0 element will be clocked into B_2 - 1 for use in resetting the decoded divide by 10 counter B_1. The decoded output "0" on B_1 - 3 then gates out all strobe pulses occurring coincident with a P_N element. All other strobe pulses gate time code data to board Pin M as well as being present at board Pin C, delayed by two inverter gates, for use in clocking the data into a serial-in/parallel-out register on the Time Code Shift Register Board (Sch. 8117730).

Another particular concern with regard to the ONE SEC MARK pulse is that it not only occurs during the P_0 sub-frame

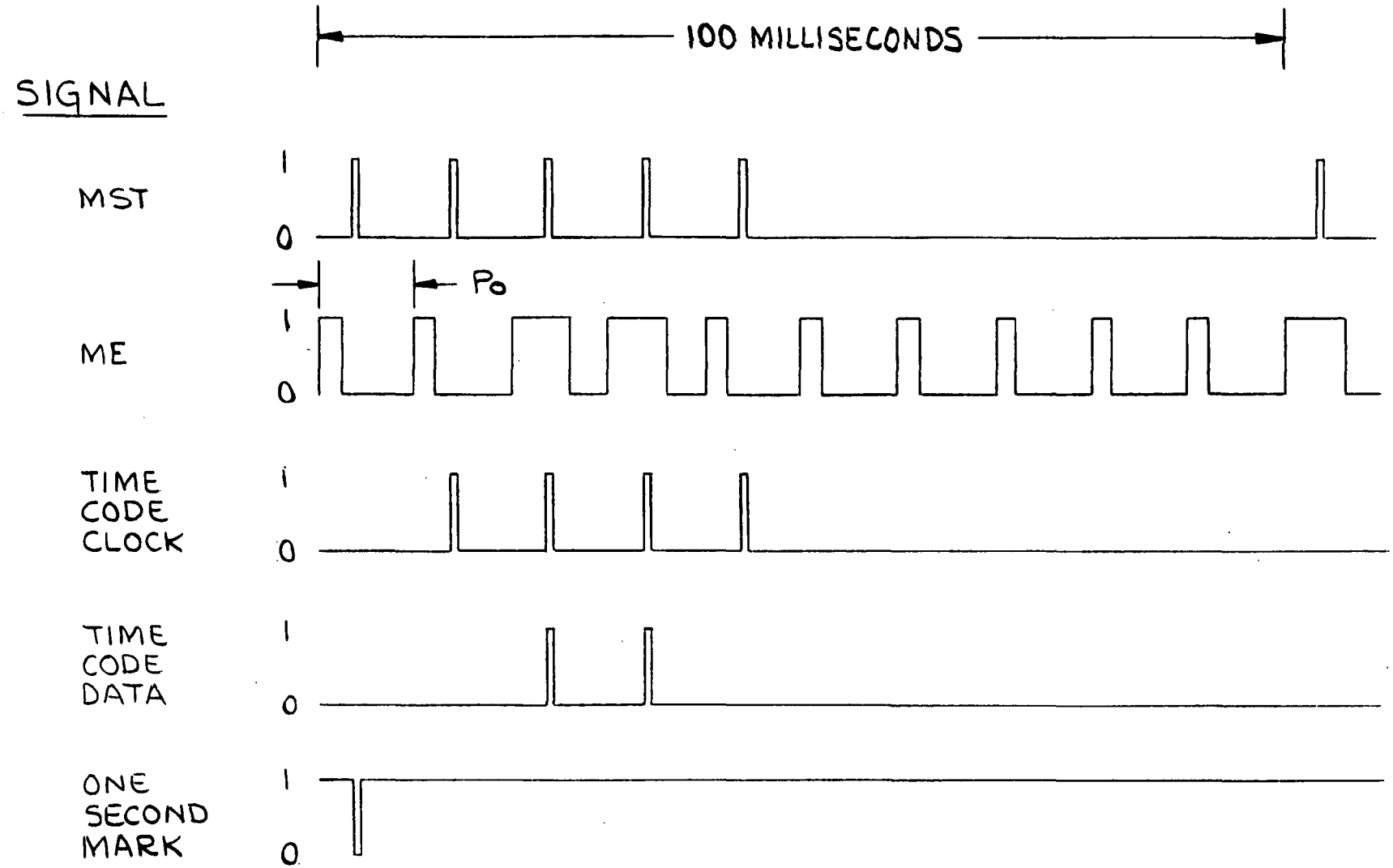


FIGURE 8.4-8 TYPICAL TIME CODE TIMING; P0 SUBFRAME

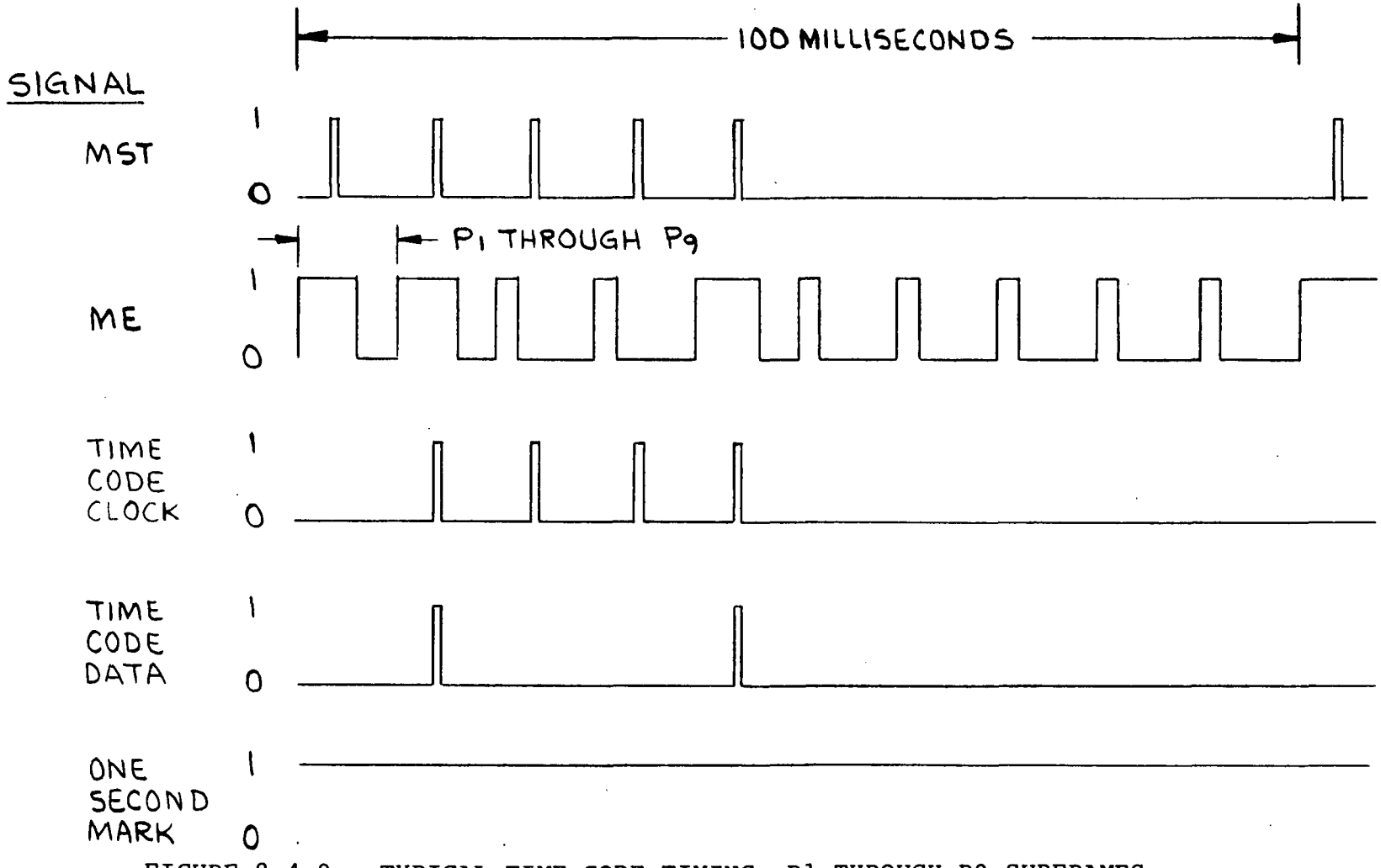


FIGURE 8.4-9 TYPICAL TIME CODE TIMING; P1 THROUGH P9 SUBFRAMES

identification bit, but also that it be gated out as a pulse synchronized to the logic "O" state of the bit clock. This is accomplished by sequencing the P_0 information into register B_2 - 13 coincident with the leading edge of the "anded" P_0 and MST strobe. On the next bit clock cycle, the leading edge of bit clock then stores B_2 - 13 into register C_2 - 1 and the trailing edge subsequentally stores C_2 - 1 into register C_2 - 13. The complement to C_2 - 13 at C_2 - 12 provides the leading edge of the ONE SEC MARK pulse, a zero level transition. The next leading edge of bit clock "Clears" the registers B_2 - 13, C_2 - 1 and C_2 - 13 which also returns the ONE SEC MARK to a logic "1". The purpose of synchronizing the ONE SEC MARK pulse to the "O" logic half of bit clock is to absolutely prevent updating the contents of the stored time code word coincident with an attempt to read out this stored word, and yet it insures that updated time code information is always placed in storage.

8.4.5.2.2 Time Code Storage

Referring to Figure 8.4-10, the block diagram of the Time Code Shift Register board, the 40 bit serial in-parallel out shift register is continually being updated with the time code information bits at the Time Code Clock rate. Once per second coincident with the "O" logic level of the ONE SEC MARK input, the contents of the register (less the last four bits to be shifted in) contains the 36 bit NASA time code word. The "ONE SEC MARK" pulse transfers the contents of the new time code word broadside into the 36 bit parallel in - parallel out holding register (whose outputs follow the inputs during this pulse interval). When the "O" level, 147.5 μs pulse is removed, the outputs retain the time code word as an input to the 54 bit formatting register shown directly below in Figure 8.4-10, until the next ONE SEC MARK pulse. At the point in the HIRS output data format defined as the start of the 16th through the end of the 18th word of the 46th or last element of each line of data, the parallel to serial control will, by going to a logic "O"; 1) cause the parallel loading of this 54 bit register to be inhibited, 2) transfers the digital multiplexer (on Sch. 8117783 - B_2 8 to 9 closes, B_2 11 to 10 closes and C_2 3 to 4 opens) such that only time code data from board pin 35 will be on the digital data buss,and 3) enables clocking of this 54 bit register for a period of exactly three words. The 36 bits of time code information are contained in bits 6 through 17 (a total of 12 bits) in each of the three output words. The order of the data is that "Hundreds Days" is contained in bits 6 through 9 of the first word shifted out down to "Units Seconds" in bits 14 through 17 of the third word shifted out.

The above sequence occurs at the line rate of 4.8852 seconds, which is not often enough to resolve time in seconds

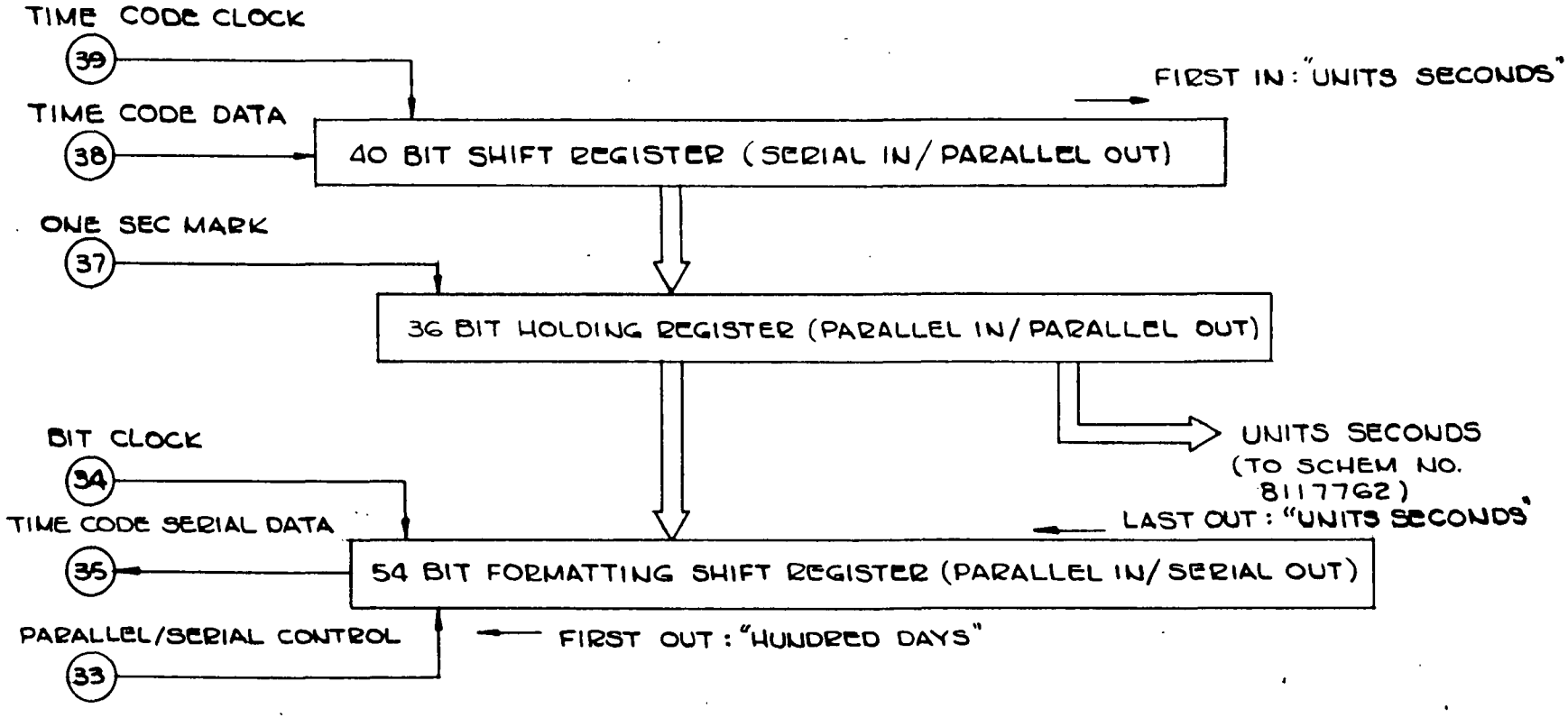


FIGURE 8.4-10 BLOCK DIAGRAM OF THE TIME CODE SHIFT REGISTER
(REF. SCHEMATIC NO. 8117730)

in the output data but is often enough for obtaining complete time information.

An additional output of the Time Code Shift Register board is the four BCD coded "Units Seconds" bits which are inserted (by the words ONE THRU FOUR SHIFT REGISTERS board - Schematic No. 8117762) in bits 1 through 4 of the third word of each output data element. Since each element time is 106.2 ms, the time resolution in the data format then becomes nearly one-tenth of a second.

8.5 Electronic Calibration

8.5.1 General

Electronic calibration of the SW, Visible and LW data channels (the entire signal path to the bi-phase output with the exception of each of the three preamplifier stages) is performed for one of a total of sixteen individual step levels, including a zero level step during each forty-six element scan line. The calibration steps are incremented at the start of each new scan line resulting in a complete sequence every sixteen lines. During the first and second elements of retrace, the calibration signal, by means of analog switching, replaces the detector preamplifier signals. In the first element of retrace, the phasing of the electronic calibration is such as to cause a positive count from the A/D Converter while in the second element of retrace, phasing of the electronic calibration is shifted π radians so as to result in a negative count from the A/D.

All internal instrument timing during the two calibration elements remains unchanged such as channel integration times and output format. This results in a total of ten plus and ten minus LW channel calibration points at a particular step level each line. In like manner the SW channel has six plus and six minus while the visible channel has but one plus and one minus.

8.5.2 Circuit Design

The Electronic Calibration board (Schematic 8118519) generates the calibration steps by chopping the output of a four-bit digital to analog converter (DAC) with both the LW and SW chopper references. Each series shunt chopper (composed of two analog switches) alternately connects the DAC output then analog ground (0 VDC) to the input of a precision unity gain buffer at the reference waveform rate. The logic which controls the electronic series-shunt chopper is a part of Schematic 8118487, the Temperature TM-Analog Sequencer/MUX band.

The DAC uses the same components as the twelve bit A/D converter described in Paragraph 8.4.2. Full twelve bit accuracy is used by the DAC for precise calibration step generation, although only four bits are used. The four-bit binary up counter whose output code determines the DAC output step reference level is included on the Electronic Calibration board. For achieving twelve bit accuracy from the basic DAC components, it is necessary to use a stable, nominally +6.2 VDC voltage source (an identical circuit to that described below is also used by the A/D Converter). The accuracy need not be better than 5%; however, the stability over temperature and line (+15 VDC reg buss) variations must be excellent. The nominal +6.2 VDC is converted to a precision 0.125 ma current source by

externally triming an internal 48.4K ohm reference current resistor within the DAC ladder network. The circuit which provides both the accurate 7.5 ma bias current to the temperature compensated reference diode (A 1N829 having a 5 ppm (0.0005%) per degree centigrade temperature coefficient) and excellent power-supply rejection is shown in Figure 8.5-1. The circuit analysis follows:

Because of the high open loop gain of the operational amplifier, V_X can be assumed equal to V_Z. V_Z can also be assumed to be nominally 6.2 VDC as the analysis would be the same for any V_Z within ±2.5% of nominal 6.2 VDC. V_1 is then calculated to be

$$\frac{R15 + R14}{R15} \quad (6.2V) \quad = 10.1263$$

The voltage across R12 and R19 in parallel must then be 3.9263V, resulting in a total current flow through R12 and R19 of 8.823 ma. Since precisely 7.5 ma is desired through the zener diode for obtaining a 5 ppm per degree centigrade temperature coefficient, 1.323 ma must be bled from the "V_Z" nodal point. As the primary purpose of the circuit is to supply 0.125 ma through R17, R18 and the 48.4K (nominal) resistor of the DAC (which is done by tailoring the resistor values of R17 and R18), a current of 1.198 ma remains to be shunted to ground. A current of 0.155 ma is shunted by the 40K ohm resistor on the telemetry reference amplifier board which uses the +6.2 VDC reference of the electronic calibration circuit as its stable reference source. Final tailoring is then accomplished by selecting a value for R4 and R5 so that precisely 1.043 ma is shunted to ground.

Turning our attention to the function of the operational amplifier in the circuit, and how its high open loop gain can be made to virtually eliminate input buss variations, we must assume a value for the +15VDC analog buss. Assuming +14.8VDC we can determine the current through R16:

$$i_{R16} = \frac{+14.8 - V_1}{392} = \frac{+14.8 - 10.1263}{392} = \frac{4.6737}{392} = 11.923 \text{ ma}$$

Since 8.823 ma plus 1.002 ma flows through R14 and R12 paralleled with R19 for a total of 9.825 ma, it is evident that to satisfy the axiom that the sum of the currents into a junction must equal the sum of the currents out of a junction, 2.098 ma must be flowing in R13. Therefore, $V_1 - \varepsilon_o$ must equal 5.6027 VDC.

$$- \varepsilon_o = 5.6027 - 10.1263$$

ε_o therefore equals +4.5236 VDC for the analysis shown. Recalculating for values of "+15 VDC" buss voltages of both +14.6 VDC and +15 VDC will show that ε_o will change if the variations are

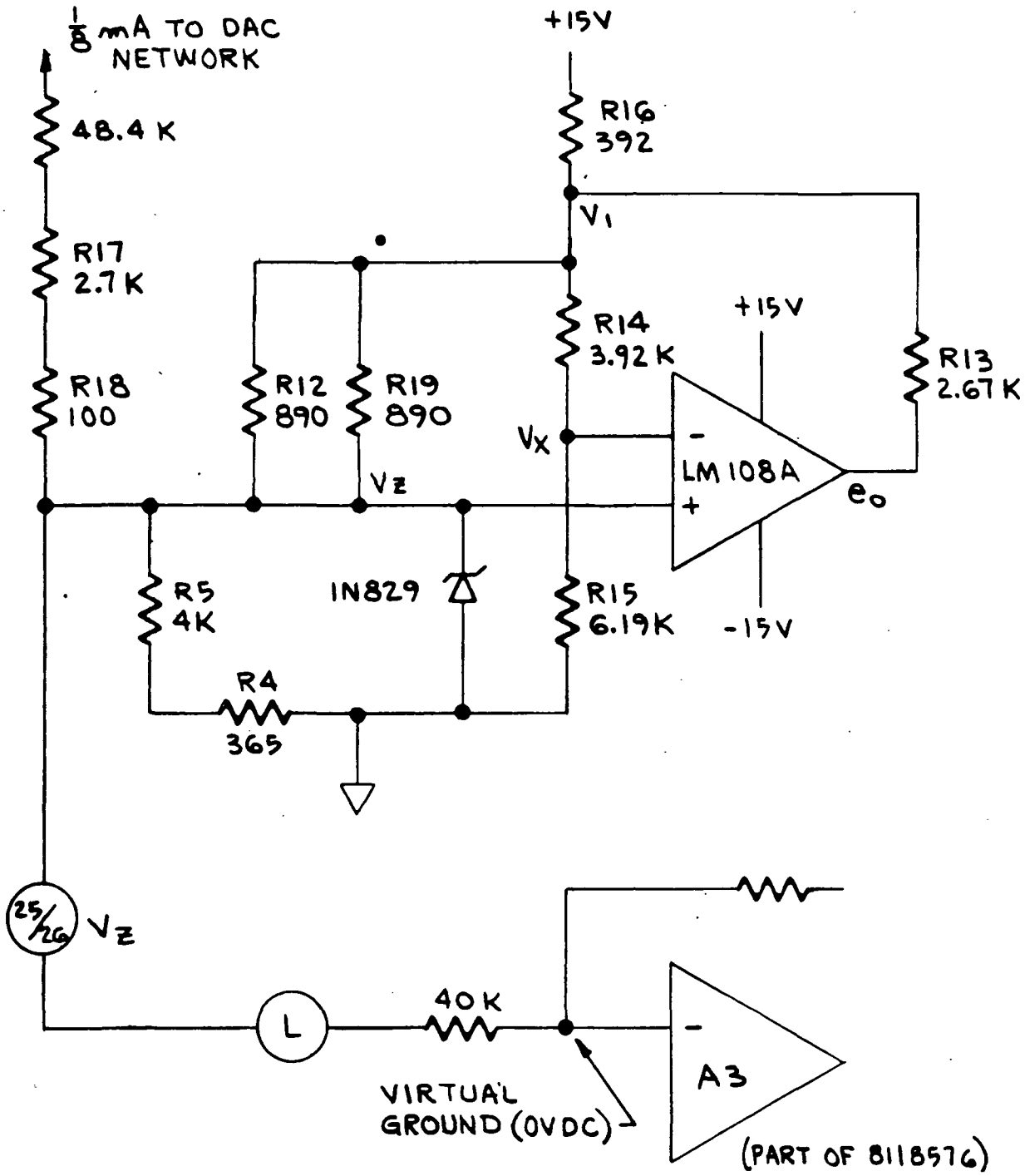


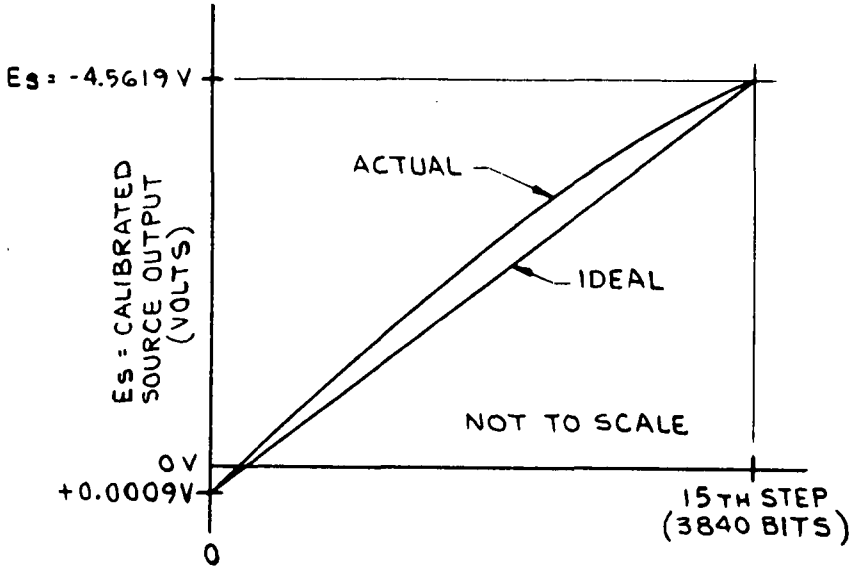
FIGURE 8.5-1 ELECTRONIC CALIBRATION REF. REGULATOR
(PART OF SCHEMATIC 8118519)

occurring well within the amplifiers pass band so as to maintain a constant voltage at V_1 thereby reducing the effect of line variations to a minimum.

8.5.3 Circuit Performance

The actual differential linearity error of the HIRS PFM electronics calibration voltage source was determined by test to be just slightly less than minus one-half a bit (see Figure 8.5-2) relative to full twelve bit accuracy on the four bits (2^{11} through 2^{8}) turned ON. Note that the technique of calibration (for determination of linearity error at full scale and zero) is not only straightforward, it always results in the most conservative linearity and relative accuracy measurement when compared with using the "best straight line" approach.

Figure 8.5-3 illustrates the fact that test data disclosed the fact that the circuit was affected by temperature primarily by a -5 ppm gain error per ^{o}C with virtually no change in offset or linearity error.



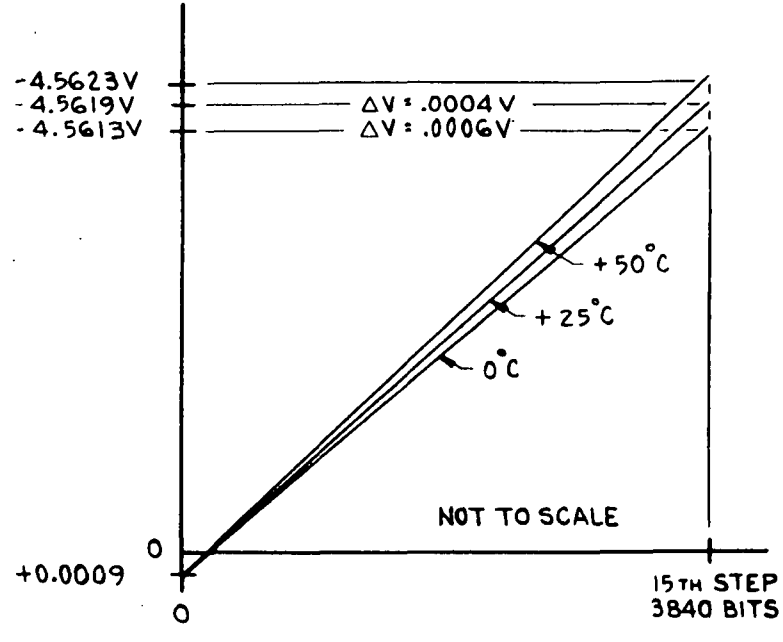
LARGEST DIFFERENTIAL LINEARITY ERROR OCCURS AT SIXTH STEP:

ERROR IN VOLTS IS -0.00058

ERROR IN BITS IS -0.488

$$\Delta E_N = E_S\left(\frac{1}{2^{11}+2^{10}+2^9+2^8}\right) = \frac{-4.5628}{3840} = \frac{-0.00119 \text{ VOLTS}}{\text{BIT}}$$

FIGURE 8.5-2 ELECTRONICS CALIBRATION SOURCE LINEARITY



CALIBRATION SOURCE FULL SCALE TEMPERATURE COEFFICIENT IS APPROXIMATELY 5 PPM/°C. THIS IS EQUIVALENT TO -0.02 BIT/°C AT FULL SCALE BETWEEN +50°C AND 0°C. (RELATIVE TO FULL TWELVE BIT CONVERTER ACCURACY)

FIGURE 8.5-3 ELECTRONICS CALIBRATION SOURCE ACCURACY VS TEMPERATURE

8.6 Command Status

8.6.1 General

Each command relay has an unswitched input buss voltage (either Electronics Pwr. Buss, F/C Pwr. Buss or Scan Pwr. Buss) wired to a common pole which will, in one of the two possible states of the relay, connect buss voltage to a resistor divider. The divider output is connected to the HIRS output interface for use with the S/C Digital "B" Telemetry subsystem which monitors the command relay status of each S/C instrument. Nine of the eleven command relay Digital "B" TM dividers within the HIRS also are connected to logic level conversion circuits which convert the negative voltage Digital "B" logic signal to a positive voltage logic level signal compatible with CMOS logic operated from a +10 VDC logic buss.

Two interface requirements on the Digital "B" TM outputs are; 1) that the Zo must be 50K ohms or less in the "OFF" condition and 1 Meg ohm or less in the ON condition and, 2) that the voltage out be -7.5 VDC ±2.5 VDC in the "ON" condition and -0.5 VDC ±0.5 VDC in the "OFF" condition.

8.6.2 Circuit Design

This first interface requirement is met by the fact (Referring to Figure 8.6-1) that Zo max in the "OFF" condition is (48.7KΩ)*(1.01) or 49.2KΩ. In the ON condition the Zo max drops to (48.7KΩ/100K)*(1.01) or 33.1KΩ. The Digital "B" output voltage range for the Electronics Pwr "ON" or F/C Motor Pwr "ON" relays (which do not have the logic level translation circuits) is:

$$V_{TM} = 0.3275\ E$$

This results in nominal digital B TM voltage of -8.02 volts with a nominal buss voltage of -24.5 VDC. A fifteen volt zener diode acts as a clamp to bound the output between +0.5 VDC and -15.0 VDC.

For those nine relays having the logic level conversion circuit shown in Figure 8.6-1, V_{TM} is found to be 0.3064 E because of the attenuating effect of R_4 (which appears in parallel with R_2). Since the inverting gain of the amplifier is -1.434, the amplifier output e = 0.439E. Therefore, for a nominal buss voltage of -24.5 VDC, e equals +10.76 VDC. Resistor R_8 (4.75KΩ) prevents the amplifier U1 from overdriving the CMOS input protection diode, even under a maximum input overvoltage condition of -37.5 VDC. At an input of -37.5 VDC, the input protection diode will conduct less than 1.4 ma (2 to 3 ma is considered by the GSFC Reliability Group to be the maximum permissible).

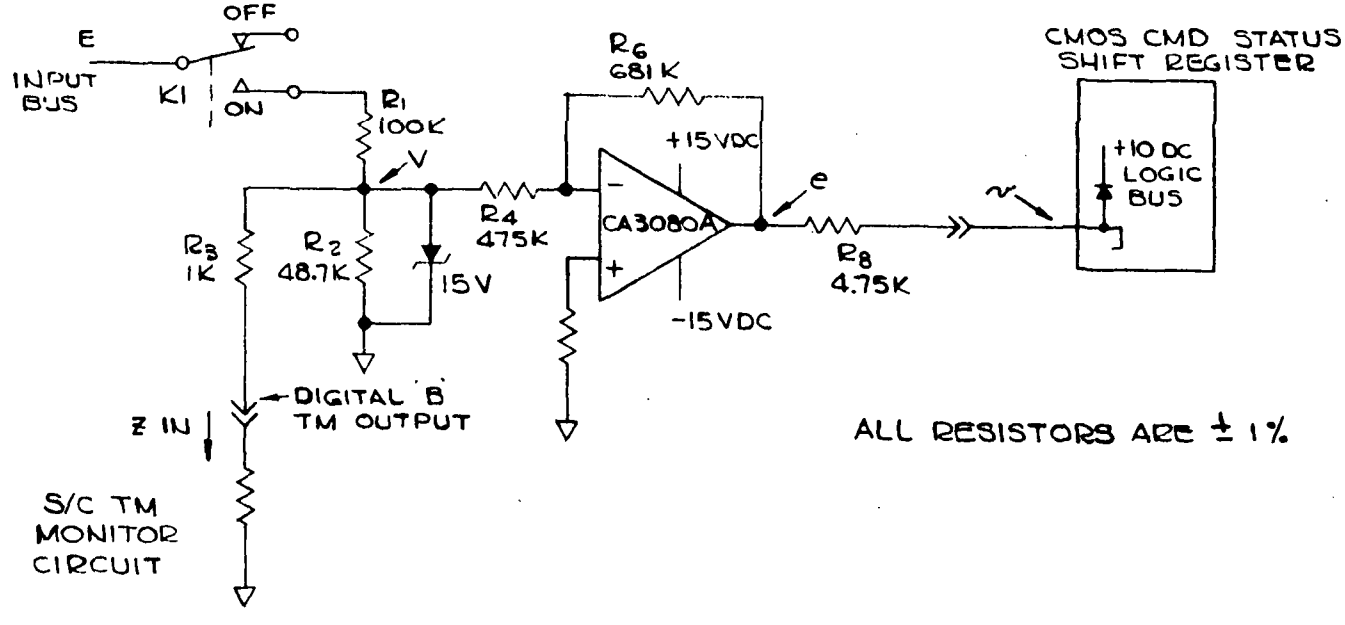


FIGURE 8.6-1 TYPICAL COMMAND STATUS LOGIC LEVEL CONVERTER CIRCUIT

8.7 Electronics Power Subsystem

8.7.1 General

This subsystem consists of two circuit board assemblies, the DC to DC converter (8118720) and the Voltage Regulator (8120427). Referring to Figure 8.7-1, the DC to DC Converter has, as its primary input, the -24.5 VDC Electronics Power Buss (switched) from the Electronics Power ON/OFF Command Relay. A secondary input is a 400KHz OV to +10 VDC square wave for synchronizing the converter to a submultiple (10KHz) of the S/C 400KHz clock. The primary outputs of the converter are separate buffered 0 to -12 VDC 10 KHz square waves for synchronizing the three switching regulators with the HIRS; 1) the Scan Motor Subsystem regulator, 2) the F/C Housing Heater regulator and, 3) the F/C Motor Power regulator. The regulated output voltage of the Voltage Regulators board (See Figure 8.7-2) power all of the signal processing and digital output data electronics.

8.7.2 DC to DC Converter

The DC to DC Converter is a driven converter which eliminates self starting problems. The -12 VDC linear regulator on the board turns on the 10KHz drive electronics that provides drive to the chopper transistor bases through transformer T1. Combining the base drive signal of T1 (through R_1 or R_2) with the differentiated edge of the complimentary drive signal through R_8 or R_9 results in the elimination of momentary current surges through Q1 and Q2 which occur if they are not switched in a break before make manner.

8.7.3 Voltage Regulators

The Voltage Regulators function to regulate the principal instrument analog and digital circuits operating voltages to within ±0.5% of their predetermined output under all expected combinations of converter input voltage, output load variations and operating temperature span. Five regulated DC outputs are derived from four unregulated inputs; 1) +15 VDC, 2) -15 VDC, 3) +5 VDC, 4) +10 VDC and, 5) +5.8 VDC. The + and - 15 VDC outputs are "fold-back current limited" regulators which will deliver up to approximately 200 ma to their load. If the load is increased the output voltage will drop off to zero and the short circuit current reduces to approximately 20 ma. This feature is for the protection of the analog circuitry as well as for the converter-regulator combination during the period of assembly and confidence/performance testing. The last three of these regulators are integrated regulators which are current limited as well as thermally protected and can survive output short circuits indefinitely, although the transformer of the DC to DC converter would be subjected to overheating if faults on these last three outputs were ever sustained.

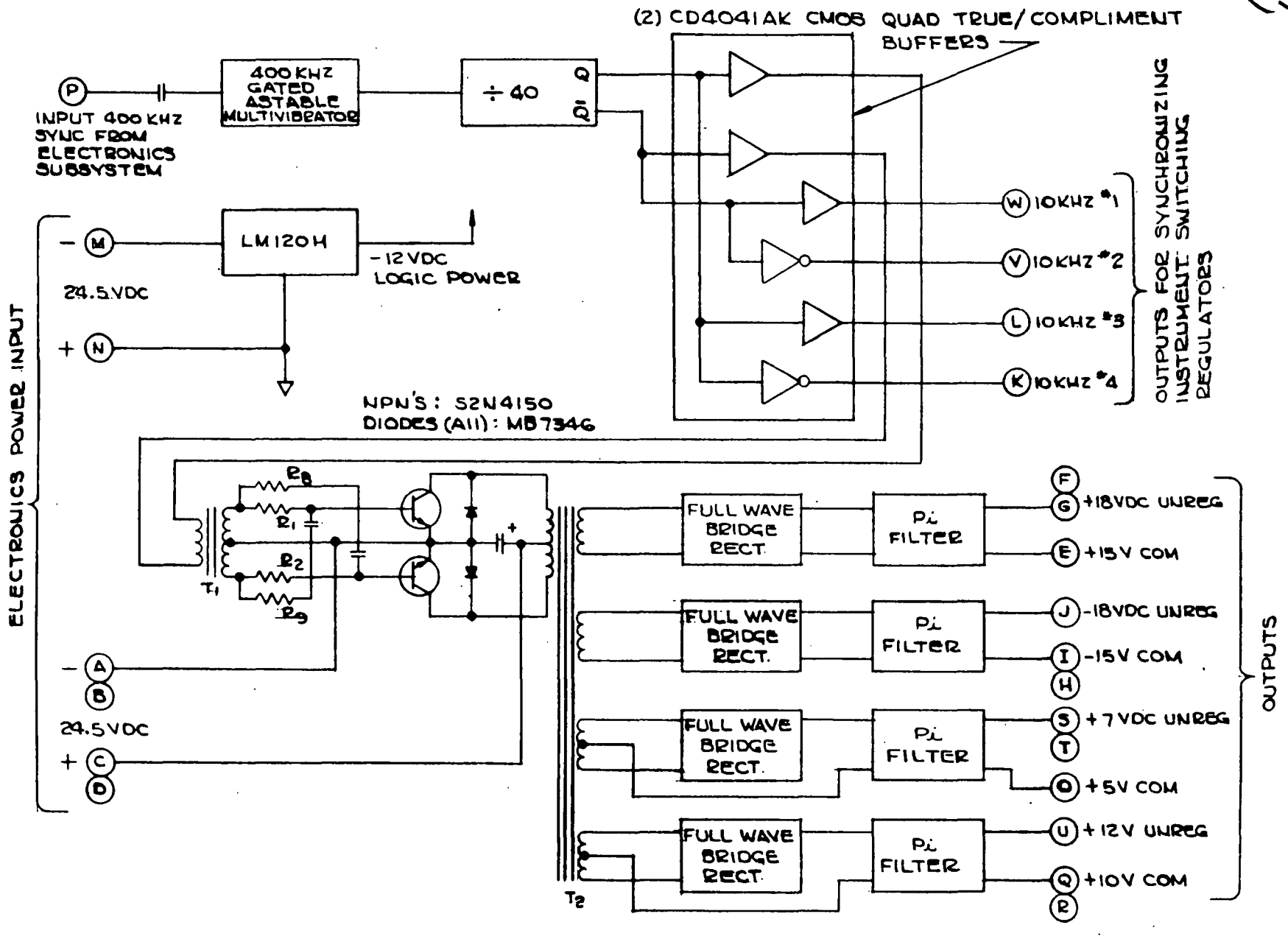


FIGURE 8.7-1 SIMPLIFIED SCHEMATIC OF DC TO DC CONVERTER
(REFERENCE SCHEMATIC NO. 8118717)

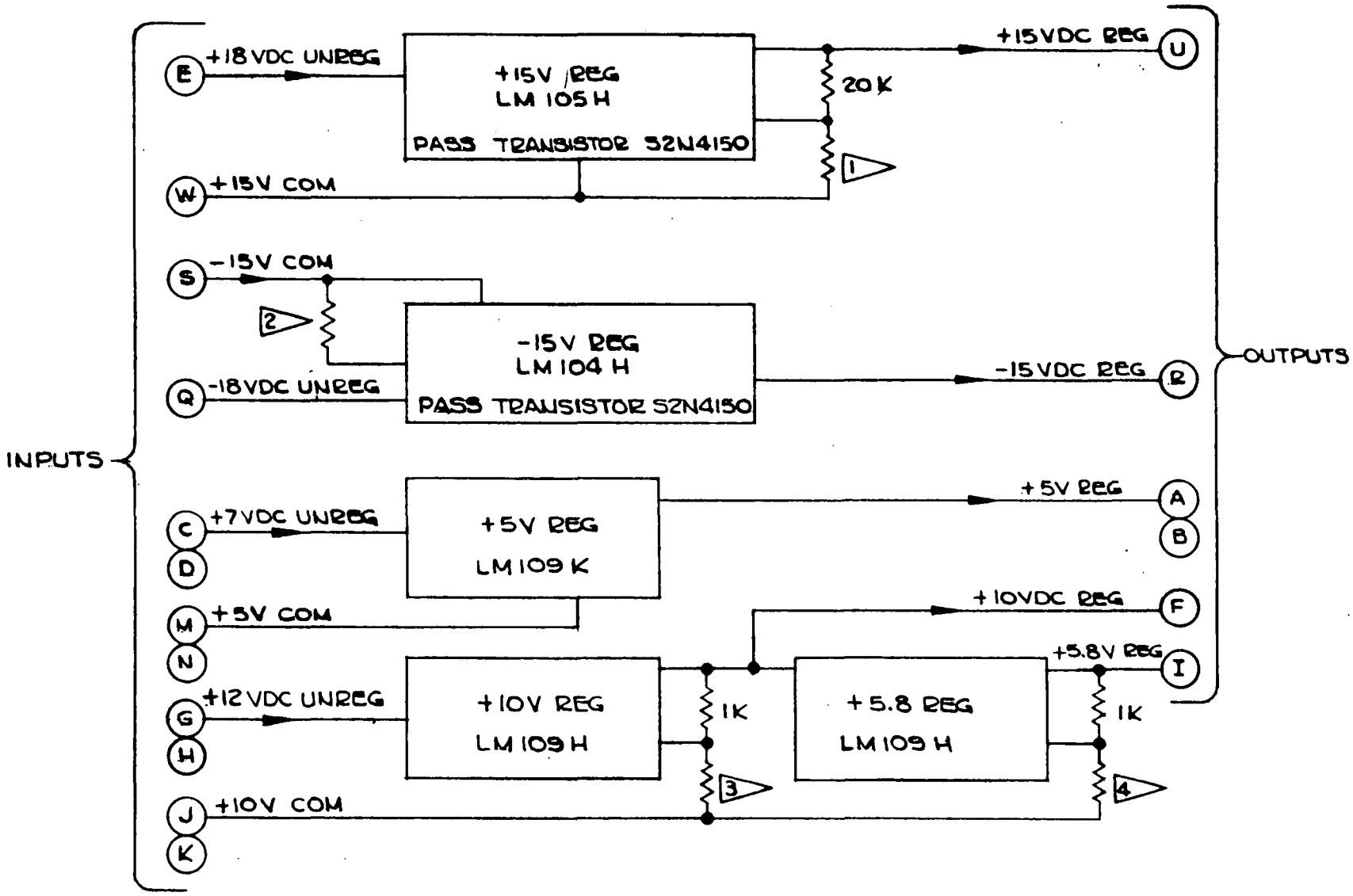


FIGURE 8.7-2 BLOCK DIAGRAM OF VOLTAGE REGULATORS
(REFERENCE SCHEMATIC NO. 8120424)

8.8 Telemetry

8.8.1 General

Telemetry outputs of the HIRS can be divided into three groups according to the output spacecraft subsystem which receives the telemetry data. These are the twenty-three output functions to the "Analog A" telemetry subsystem, the eleven command relay verification outputs to the "Digital B" telemetry subsystem and the various functions which are encoded digitally into fixed word-bit locations in the main instrument data format output to the "HDRSS" spacecraft recorders.

8.8.2 "Analog A" Telemetry

The analog telemetry consists of twenty-three functions calibrated so that the useful range is restricted to 0 VDC to -6.375 VDC. The spacecraft Versatile Information Processor (VIP) multiplexes these (and many other) analog signals (at a once per sixteen second rate) to a 10-bit A/D converter (useful to only 8 bits) for both real time transmission and recording on one of the HDRSS tracks. These telemetry points are tabulated in Table 2.1-1. Ten outputs of the total of twenty-three consist of full time telemetry monitoring of eight instrument temperatures (F/C and Scan Mirror, Baseplate, Primary and Secondary Telescope Mirrors, Cooler Housing and Electronics), the cooler cover door position and the telemetry buss input voltage. These continuous unswitched functions are discussed in detail in Paragraph 8.8.6.

Six additional temperatures are monitored by circuitry powered by the instrument Electronics ON/OFF command which are of considerably higher precision and stability; the four F/C Housing Temperature Monitor circuits, the Patch Temperature Monitor circuit and the Radiant Cone Temperature Monitor Circuit. These six telemetry circuits are covered in detail in Paragraph 8.8.5. Two outputs monitor the Scan Motor and F/C Motor currents at any time these subsystems are commanded ON. Of the five remaining, four monitor the magnitude to the internal analog and digital regulated buss voltages and one monitors the amount of power dissipated on the patch required to maintain temperature regulation. These five are also powered by the Electronics ON/OFF command.

All twenty-three of the above maintain an output impedance of less than 10K ohms and provide a bounding of the output signal range between +0.5 VDC and -15.0 VDC.

8.8.3 "Digital B" Telemetry

The eleven bi-stable magnetic latching command relays are continuously monitored as to the relay state or "last command

stored." These command relays are tabulated in Table 2.1-2. A complete discussion of the digital output characteristics is found in Paragraph 8.6, while the "Digital B" logic state for a given command state is tabulated in the Main Sensor Data dissipation of Paragraph 2.1.1.1. As shown in this paragraph, nine of the eleven relays are (in addition to being outputted to the Digital B telemetry) also monitored in the HDRSS output data, in bits three through eleven of the second word of each data element. The two not monitored by HDRSS are the Electronics ON/OFF and the F/C Motor Power ON/OFF, both of which are a "logic one" to the Digital B when commanded ON.

8.8.4 HDRSS Telemetry

While the Patch Temperature is the only Analog A, and the nine of eleven command relays of the Digital B (the two not included, Electronics and F/C Motor Power can be inferred as on in the presence of HDRSS) are the only telemetry functions actually duplicated by being in HDRSS, many other data bits can be properly classed as telemetry outputs. In fact, with the exception of the spectral data words (including fill zero bits and the sign bit) and the sync (element and line) words, all other bits in the data format can be properly called telemetry. While a complete discussion of this format is found in Paragraph 2.1.1.1, a synopsis of these information bits is included below.

1) All "Odd Parity Bits" which are in the eighteenth bit slot of each word. This bit verifies data transmission accuracy in that in each group of eighteen bit words, the sum of the "ones" in the data word must be an odd number.

2) All second and third words of each element. These words contain the two "Mode Bits" which identify from which of four basic radiometric sources (internal warm target, internal cold target, space (target) or earth scanning) the instrument is receiving its input, the nine command status bits, the six bit binary element number (0 through 45) bits, the BCD encoded units seconds partial time code, the four bit binary calibration level code and the eight bit complementary binary encoder position number.

3) All data bits during the last four elements of each line (mirror retrace or forward slew) with the exception of sync bits. During the first two elements of retrace electronics calibration data is inserted in lieu of spectral data which permits scale factor and linearity correction of the entire data handling electronics. During the last two elements of retrace, nine precision temperature

monitors are sampled, the four internal cold target sensors, the four internal warm target sensors and the patch-sensor circuits. In Words 16, 17 and 18 of the last element of each line, the NASA 36 bit full time code is inserted in the spectral data bit positions.

8.8.5 Precision Temperature Monitoring

8.8.5.1 General

These amplifiers are used to convert the resistance-temperature characteristics of calibrated platinum sensors to a voltage which in turn provides an accurate and stable measure of critical instrument temperatures. (Schematic 8118566 and 8118576). A total of fourteen platinum sensors are utilized for monitoring the temperature of five instrument structures:

1) The 300K internal warm blackbody (radiometric calibration) target (4 sensors).

2) The 270K internal cold blackbody (radiometric calibration) target (4 sensors).

3) The Filter Chopper Housing (4 sensors).

4) The Radiant Cooler Cone (1 sensor) structure.

5) The Radiant Cooler "Patch" structure upon which the long and shortwave detectors mount (1 sensor).

While the four sensors on each of the three above structures do provide redundancy in measuring temperatures, the primary reason for using four sensors is to determine thermal gradients across the structures.

The temperature span over which the sensor amplifiers must operate (in the analog telemetry compatible range of 0 volt to -6.375 VDC) are as follows:

Warm Target	273K to 333K
Cold Target	243K to 303K
F/C Housing	293K to 313K
Cone	133K to 323K
Patch	103K to 323K

Although neither the warm target or cold target sensors were required to remain within the 0 to -6.375 VDC range as they were not planned for Analog Telemetry use, compatibility with the VIP Analog TM was deemed more desirable than expanding the resolution of these channels by using the total ± 6.4 VDC dynamic range of the HIRS internal A/D converter.

Two major constraints in the design of these fourteen amplifiers was the availability of only four printed circuit boards, each with a useful area of 6.1 square inches, and the need to keep the total power required to a minimum.

8.8.5.2 Circuit Design

Two galvanometric bridge amplifier circuit configurations were examined; 1) the grounded-unbalanced bridge shown in Figure 8.8-1, and, 2) the grounded balanced supply bridge shown in Figure 8.8-2.

The circuit of Figure 8.8-1 is linear for $\alpha \ll 1$ which is the case when considering platinum sensors $\alpha \doteq 0.00392$ $(T-T_o)$ for T_o = 303K and T between 373K and 33K and $\alpha \doteq$ 0.00425 (T_1-T_o) for T_o = 120K and T between 105K and 135K.

For the circuit of Figure 8.8-1, five characterizing resistors are necessary in each circuit and it is necessary to choose an amplifier type which is insensitive to the potentially large common mode level.

The circuit of Figure 8.8-2 (the type used on HIRS), is also linear for $\alpha \ll 1$ and although an accurate tapped, stable power supply for the references +V and -V is required, it is the better of the two choices according to Philbrick Researches, Inc., "Application Manual for Computing Amplifiers for Modeling, Measuring, Manipulating and Much Else." (second edition dated June 1966). As shown in Figure 8.8-2, only two accurate characterizing resistors are needed per channel and common mode voltage problems are eliminated as well. In addition, implementing a $-V_{REF}$ supply is justifiable when using fourteen amplifier circuits.

The final circuit design used in HIRS uses three identical boards (Schematic 8118566), with only the characterizing resistors being different. Each contains four identical amplifier circuits. A fourth board contains two temperature monitor circuits and the two bipolar reference regulators (Schematic 8118576). A typical temperature monitor circuit is shown in Figure 8.8-3.

At the minimum temperature of the temperature span desired for the particular channel,

$$R_T + R_2 = R_1, \text{ therefore } e_o = \text{OVDC}$$

At the maximum temperature desired, R_4 is selected such that e_o = -6.375 VDC.

R_1, R_2 and R_4 are bulk metal film resistors with specified absolute accuracy of ±0.05% and a temperature coefficient of ± 1 ppm/°C between 273K and 333K. The highest closed loop

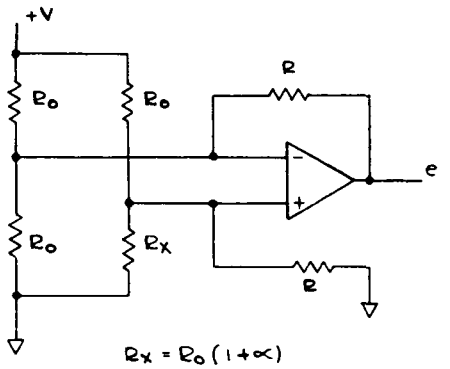


FIGURE 8.8-1 GROUNDED UNBALANCED BRIDGE

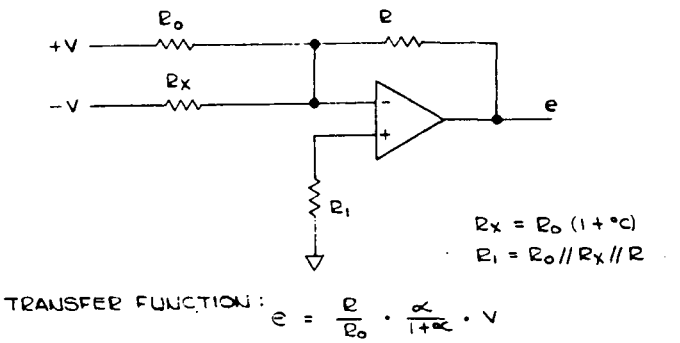


FIGURE 8.8-2 GROUNDED BALANCED SUPPLY BRIDGE

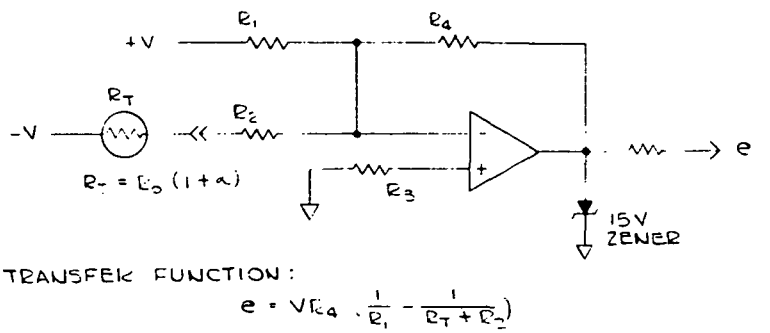


FIGURE 8.8-3 TYPICAL HIRS TM AMPLIFIER

gain of any amplifier is approximately 29 (for the four F/C housing sensor amplifiers) which combined with a worst case voltage offset drift of 5 $\mu V/^{o}C$ (for LM108A) and an operating temperature range of 50°C, results in a maximum change in offset voltage of 7.3 mv (typical drift in a LM108A is about one-fifth this amount). An idea of the significance of this drift is that a change of 7.5 mv represents 0.025K in measurement error. The maximum gain error due to the ± 1 ppm T.C. of R_1, R_2 and R_4 is insignificant in that over a 50°C change in temperature, this contribution is less than one-tenth that of the maximum amplifier drift error of 0.025K and then only at the upper temperature range of the channel temperature span.

The total current required from the plus and minus fifteen volt analog buss for all fourteen sensor amplifiers and the two reference voltage amplifiers is 16 ma resulting in a total power requirement of 480 mw.

8.8.6 Full Time Telemetry

8.8.6.1 General

A totally isolated -24.5 VDC unswitched distribution within the instrument is used to power eight medium precision (within 1°C error band) temperature monitoring circuits and the cooler door position by means of a position potentiometer. These nine analog functions are outputted to the spacecraft VIP "Analog Telemetry Subsystem" with one additional telemetered function, a linear scaling circuit whose output becomes a measure of the actual full time telemetry buss voltage. A listing of these temperatures is in Table 2.1-1.

8.8.6.2 Circuit Design

For simplicity and reliability, the temperature monitor circuits consist only of passive components, including a temperature sensitive thermistor selected from GSFC QA Div. Parts Branch PPL No. 11. The basic circuit is shown in Figure 8.8-4 below.

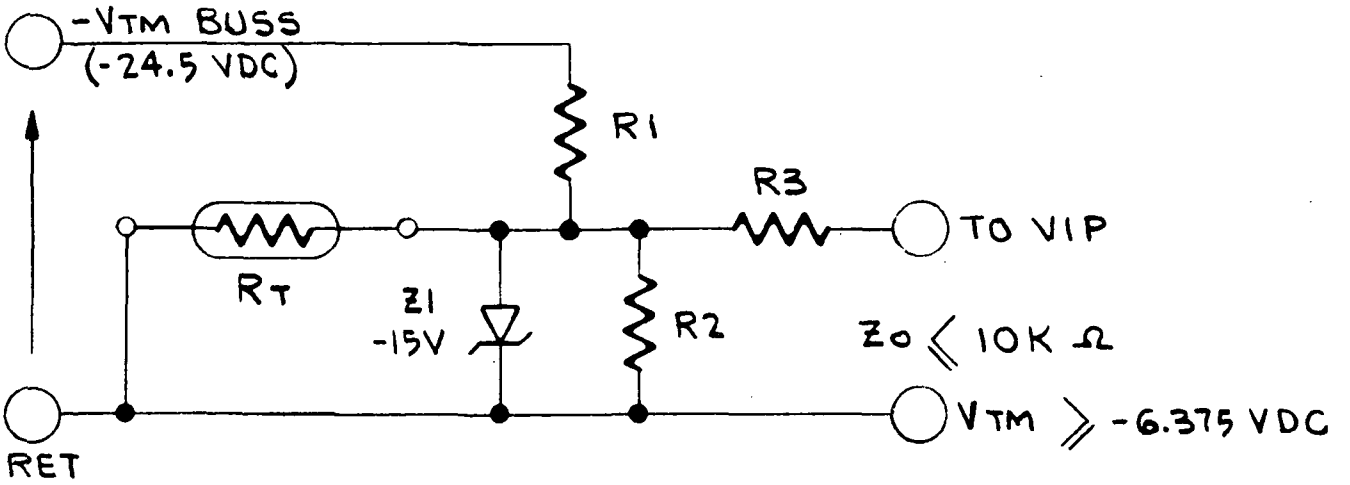


FIGURE 8.8-4 TEMPERATURE TELEMETRY CIRCUIT (TYPICAL OF EIGHT)

Despite the simplicity of the preceding circuit, the output to VIP must meet three basic design characteristics; 1) the output impedance must be less than 10K ohms over the useful temperature range of interest. As R_T increases resistance at lower temperatures, this T_{min} must be selected (resulting in an R_{Tmax}) along with R_1, R_2 and R_3 to meet this requirement, 2) the minimum voltage which can be converted by the VIP is -6.375 VDC (the maximum is 0 VDC); therefore, at T_{min} (when R_T is maximum) R_1 and R_2 must attenuate the -24.5 VDC Full Time TM buss to a minimum voltage of -6.375 VDC, and, 3) the circuit must limit the output excursion to a safe range for the VIP gate as well as protect the instrument from VIP gate failure.

To achieve number three above, R_3 was arbitrarily selected to be 1 K ohm and Z_1 was likewise selected to be a -15V zener. Meeting number one above, then required that:

(1) $$Z_{o\ max} - R_3 = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_T}} \leq 9K \text{ ohm}$$

(letting $R_2 \| R_T = R_X$ and $Z_{o\ max} = 9K$) simplifies the above equation to:

(2) $$\frac{R_1 R_X}{R_1 + R_X} = 9K$$

To meet the -6.375 VDC minimum output voltage requirement;

(3) $$\frac{-24.5\ VDC.R_x}{R_1 + R_x} = -6.375\ VDC$$

Solving R_x in terms of R_1 yields

(4) $$R_x = .35172\ R_1$$

Substituting (4) in (2) above yields a value of R_1 equal to 34.59K. Equation (4) then yields a value for R_x equal to 12.166K.

As PPL values for thermistors are in standard values at 25°C of 5K, 10K, 30K ohm and higher, the optimum value, considering the choice was 10K ohm.

The lower temperature limit (T_{min}) was selected (for seven of the eight circuits) to be -5°C, where the thermistor has a resistance of 37.31K. Solving for R_2 in Equation (1) (letting $Z_{o\ max}$ equal 10K ohms) yielded R_2 equal to 18.05K ohm.

The closest standard resistance value for R_1 was 34.8K ohm and for R_2 was 17.8K ohm. With these compenents, $Z_{o\ max}$ computes to be 9.95K ohm and $V_{o\ min}$ to -6.302 VDC.

The algorithms for converting the output voltage of these circuits to temperature can be found in Table 2.1-5.

In the case of the Cooler Housing Temperature Telemetry, T_{min} was required to be -20°C. In this particular case, only R_2 was changed in the circuit from 17.8K ohm to 13.7K ohm with the result that at -20°C, Z_o max was 9.75K ohm and V_o min was -6.154V. It should be noted that while these individual circuits were constructed with resistance tolerances of ± 1%

in locations R_1 and R_2, which could result in as much as ±2% error, open circuit voltage attenuation and 10K ohm simulated thermistor loading of the attenuator $\left(\frac{R_2}{R_1 + R_2}\right)$ on the Protoflight model circuit board revealed actually less than ± 0.5% total combined scaling and network impedance error.

The cooler door position potentiometer is a 10K ohm linear taper type, capable of continuous rotation having one end of its resistance connected to the TM-Buss Return while the other is connected to the -24.5 VDC TM Buss through a fixed 10K ohm scaling resistor. The wiper is positioned rotationally during assembly so that the closed door output is approximately -5.35 VDC and the open door output is -0.80 VDC. In a manner similar to Figure 8.8-4, the potentiometer output (the telemetry to VIP) is buffered by a 1K ohm resistor and clamped by a 15V zener.

To insure algorithm accuracy to each of the nine telemetry functions discussed above, a separate purely resistive -24.5V TM Buss attenuator (VTM = 0.2232 · -24.5 VDC TM Buss) is provided to the VIP for making scale factor corrections to each of the proceeding telemetry outputs.

8.9 Detector Patch Temperature Control

8.9.1 General

The radiant cooler patch upon which the LW and SW detectors mount is continuously subject to the operation of a two-temperature level, proportional temperature controller circuit when the system electronics is turned on. By spacecraft command, the control temperature may be 124K (HIGH) or 112K (LOW). No power is supplied to the two parallel heater resistors until the patch is at or below the control temperature set point.

8.9.2 Circuit Design

Referring to Figure 8.9-1 for the following discussion, the controller receives as its input a voltage (labeled V_A) whose magnitude is related to patch temperature by virtue of the temperature-resistance characteristic of the platinum sensor R_T. While the resistance/temperature (R-T) relationship is best defined by a 2nd order polynominal equation, virtually no error between 110K and 125K will result if a straight line approximation is used in which the temperature-resistance relationship is expressed as the linear equation;

$$(1) \quad T_{Kelvin} = \frac{R_T + 275.64}{8.55}$$

Equation (1) is computed by the point-slope method from the actual calibration data supplied with S/N 7225 platinum sensor which is used on the PFM patch.

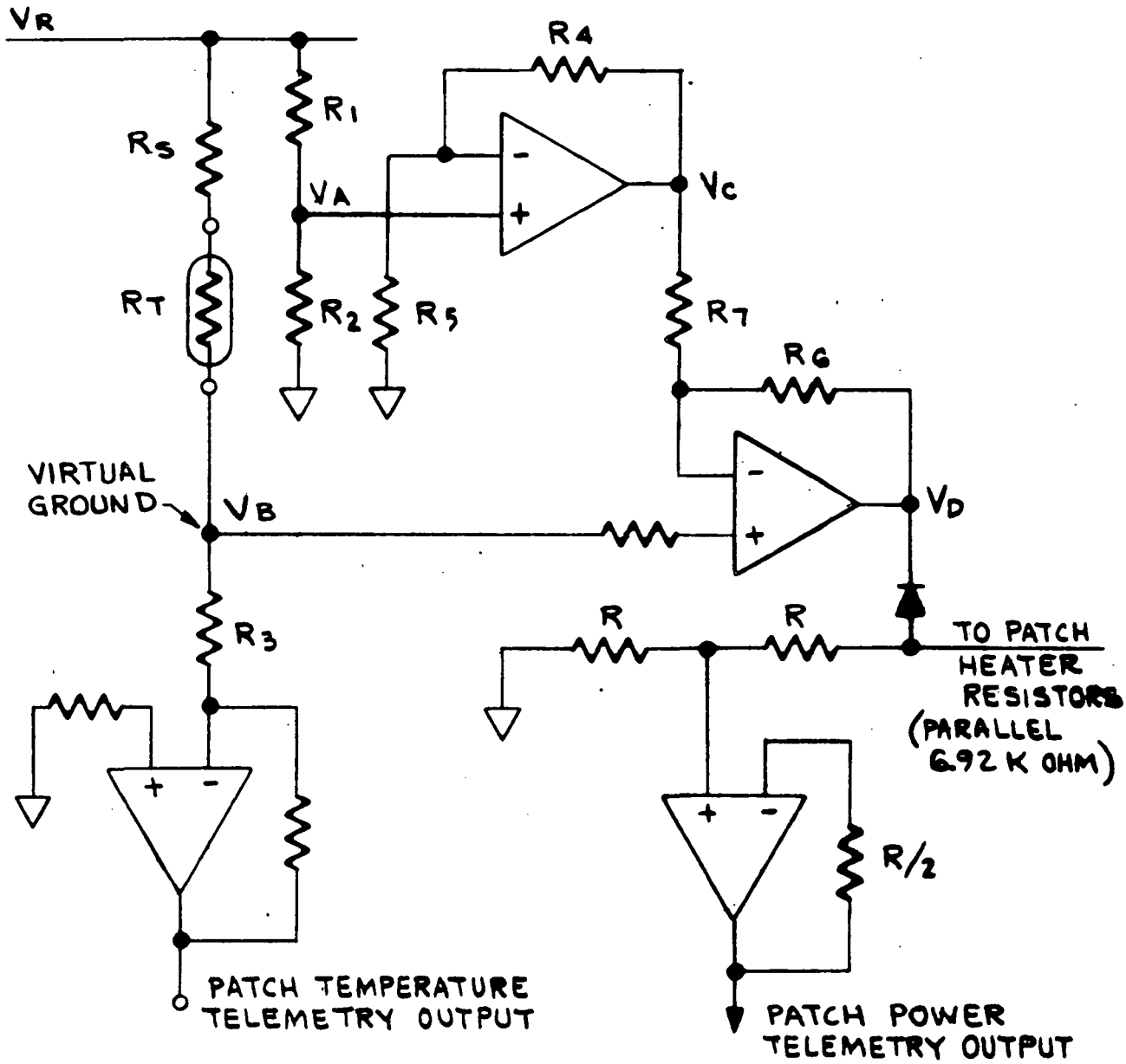
An analysis of the circuitry of Figure 8.9-1 follows:

$$(2) \quad V_A = \frac{V_R \ (R_2)}{R_1 + R_2}$$

$$(3) \quad V_B = \frac{V_R \ (R_3)}{R_3 + R_S + R_T}$$

$$(4) \quad V_C = \frac{V_A \ (R_4 + R_5)}{R_5}$$

$$(5) \quad V_D = (V_B - V_C) \left(\frac{R_6}{R_7} \right)$$



FOR HIRS PROTOFLIGHT MODEL:

R_1 = 5476 Ω	R_G = 22 MEG. Ω	* EFFECTIVE R_2 IN PATCH TEMP HIGH IS 1468.4 Ω
* R_2 = 1500 Ω	R_7 = 4000 Ω	
R_3 = 1315 Ω	R_S = 4.124 Ω	
R4 = 1000 Ω	V_R = 3.991 VDC	
R_5 = 1 MEG Ω		

FIGURE 8.9-1 PATCH TEMPERATURE CONTROL/PATCH POWER TELEMETRY CIRCUIT

Therefore,

$$(6) \quad V_D = V_R \left[\frac{R_3}{R_3 + R_S + R_T} - \left(\frac{R_2}{R_1 + R_2} \right) \left(\frac{R_4 + R_5}{R_5} \right) \right] \frac{R_6}{R_7}$$

R_1 is tailored so that at a temperature of 112K (as sensed by R_T on the patch), the term within the brackets in Equation (6) is equal to zero. This is to say;

$$(7) \quad \left(\frac{R_3}{R_3 + R_5 + R_T} \right) = \left(\frac{R_2}{R_1 + R_2} \right) \left(\frac{R_4 + R_5}{R_5} \right)$$

Plugging the actual HIRS PFM resistor values into Equation (7) results in a computed R_T equal to 676.63 ohms. Using this computed value of R_T in Equation (1) yields 111.38K From the calibration data of the sensor, the value of R_T at 112K is actually 681.96 ohms, which results in a computed error of 5.33 ohms (from Equation (7) a temperature error of 0.62°C). In fact, because of resistor tolerances used in the controller, a larger apparent error would not be surprising; however, the actual control set point was performed with the actual R_T value of approximately 682 ohms which eliminates actual set point error in the HIRS PFM.

8.9.3 Controller Closed Loop Thermal Gain

Evaluating Equation (6) for the slope of V_D versus R_T reveals that the equation of the function V = f(T) can be approximated quite accurately (between V = 0 and V = 13.2 VDC) by;

$$(8) \quad V = 6.6T - 739.2 \text{ where T is in Kelvin.}$$

Since the heater resistance is 3460 ohms, and power is expressed as V^2/R, heater power (in milliwatts) in terms of T becomes;

$$(9) \quad \text{Patch Pwr} = 12.5896T^2 - 2820.07\ T + 157924$$

Differentiating Equation (9) to determine the slope of power versus temperature ($\Delta P/\Delta T$) characterizes the circuit.

$$(10) \quad \frac{dP}{dT} = 25.1792T - 2820.07$$

Since the slope of temperature rise on the patch per milliwatt input was experimentally determined to be -1.1 mw/°C, the closed loop thermal gain A_{CL} is found by dividing Equation (10) by -1.1 mw/°C.

$$(11) \quad A_{CL} = 2563.7 - 22.89T$$

Therefore, while A_{CL} equals zero at 112K; at 111.5K, A_{CL} equals 11.465, at 111.0K, A_{CL} equals 22.9 and at 110K, A_{CL} equals 45.8.

The real significance of the closed loop thermal gain is the fact that at 111K, a change in the thermal input to the patch of 1.1 millwatts which would result in a decrease of 1 degree (if not controlled) will actually cause a temperature drop of only approximately $1/A_{CL}$ or (0.04) degrees.

8.9.4 Patch Power Telemetry

Patch Power Telemetry is implemented by adding a non-inverting buffer having a gain of one-half whose input is the voltage to the patch heater which consists of paralleled 6.92K ohm resistors. Therefore, patch power in milliwatts is equal to

$$\frac{\left(2\ V_{TM}\right)^2}{\frac{6.92}{2}}$$ which simplifies to;

(12) Patch Pwr = $1.16 \times 10^{-3}\ (V_{TM})^2$

Notice that Equation (9), that expresses patch power in terms of T in Kelvin, and (11) which expresses patch power in terms of V_{TM} can be combined, allowing V_{TM} to then become a method of measuring temperature (between 0V and -6.375 VDC) by means of the linear Equation

(13) $T_{\text{in Kelvin}} = 112 - .30303\ V_{TM}$

8.9.5 Patch High Temperature Control

Patch "High" temperature control is effected by commanding a bistable latching relay to shunt 69.6K ohm across Resistor R_2 in Figure 8.9-1, resulting in a change to the effective value of R_2 from 1500 ohms to 1468.4 ohms. Going back through the analysis performed in Paragraph 8.9-2 (Circuit Design) results in a control temperature set point of 124K with this value of R_2. The constant term of Equation (8) will change to 818.4 from 739.2 when in Patch Temp "HIGH". The terms of Equation (9) will change to:

Patch Power = $12.5896T^2 - 3122.22T + 193577.7$

The constant term of Equation (10) changes from 2820.07 to 3122.22, the constant term of Equation (11) changes from 2563.7 to 2838.38 and the constant term of Equation (13) changes from 112 to 124.

8.10 Cooler Cover Motor Control

8.10.1 General

The radiant cooler has a permanent magnet stepping motor driven cover or door which can be placed in the stored or closed position to block the patch view to space. This is for the purpose of outgassing the cooler assembly. The door can also be placed in the deployed or open position to permit the cool down of the detector patch. In this position the patch is unable to view any part of the door.

8.10.2 Circuit Design

The electrical control is commanded independent of all other instrument subsystems by use of two command relays. The Cooler Cover Deploy/Store relay determines which direction the motor will drive (when turned on) and the power command relay applies power to the phase control logic and to the motor. Figure 8.10-1 shows a simplified schematic of the entire subsystem; the control relays, the two phase control logic and pull-up switching transistors and the motor windings. Figure 8.10-2 shows the logic timing. Note the effect of switching the control polarity (Motor Direction Control) on A1-1&2 in the case of the control going from Logic "0" to Logic "1" and on A1-12 & 13 in the case of the control going from Logic "1" to Logic "0".

Each section of the CD4041A quad buffer supplies a minimum of 11.5 ma of base drive to its respective 2N5153 transistor. At nominal -24.5 VDC buss voltage each motor winding will have approximately 250 ma when the transistor pulls up the winding to ground. The min h_{fe} requirement for the 2N5153 is 22, while screening data for these transistor types procured for HIRS indicates h_{fe} ranges from 53.5 to 97.

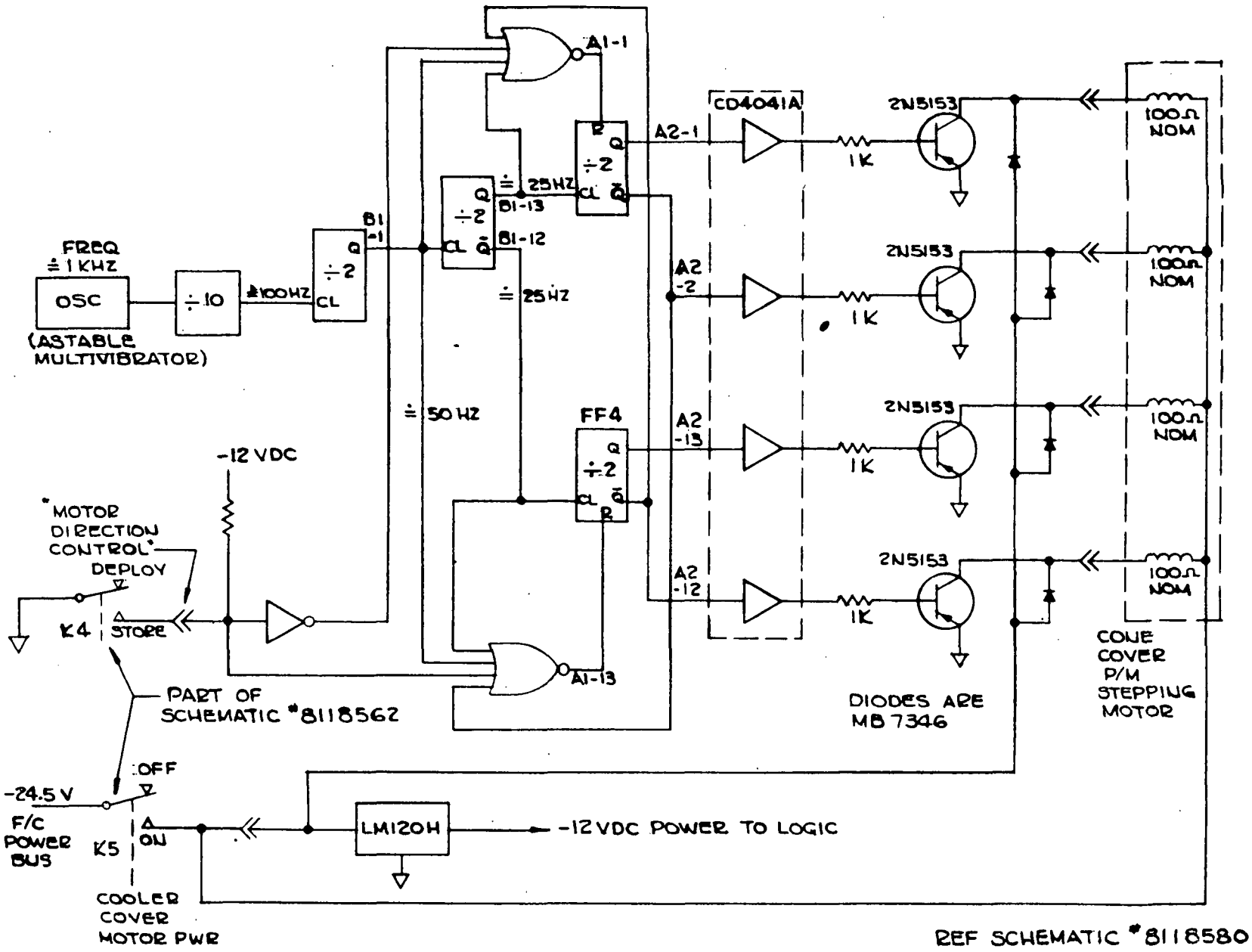


FIGURE 8.10-1 SIMPLIFIED COOLER COVER MOTOR CONTROL SCHEMATIC

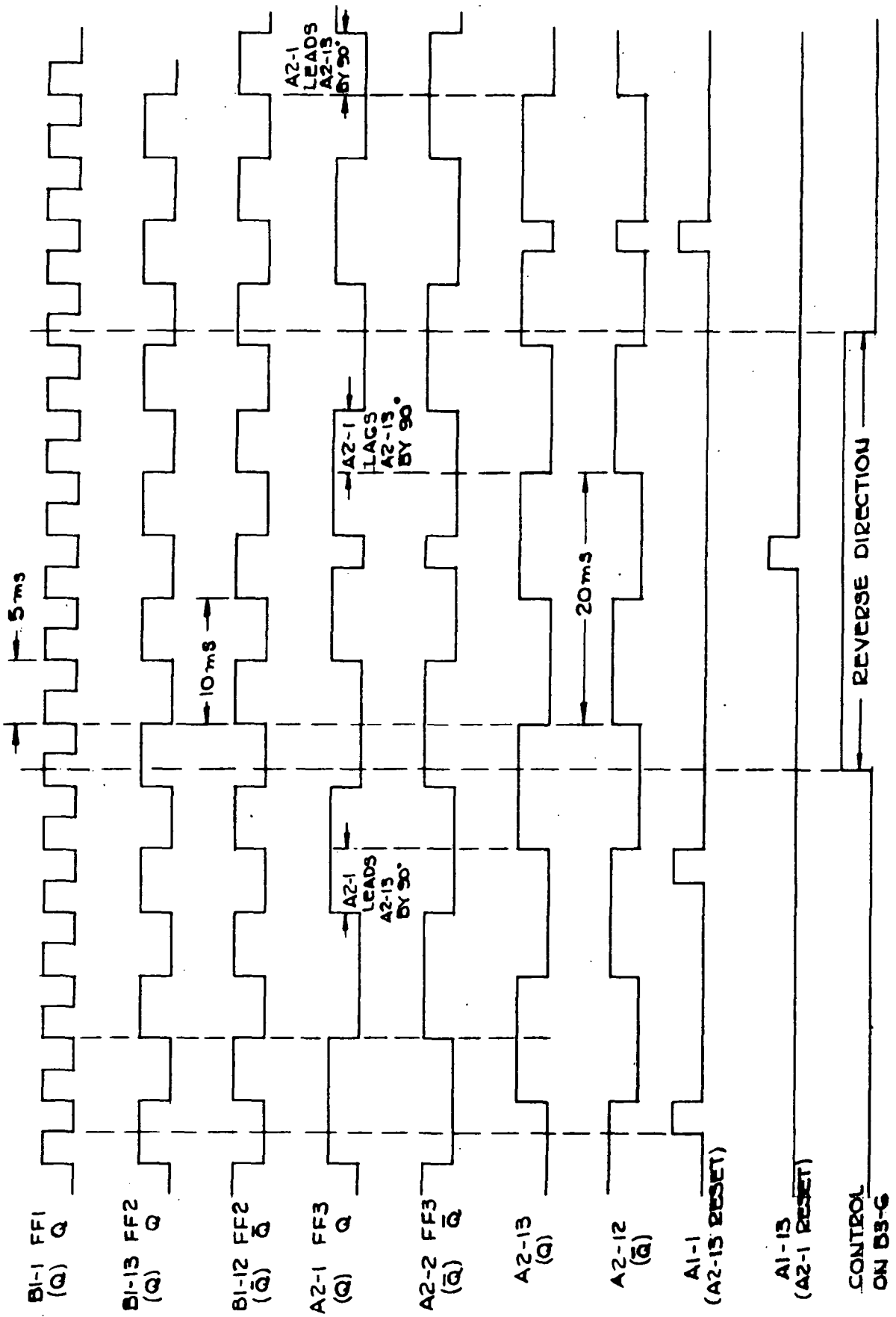


FIGURE 8.10-2 TWO PHASE STEP MOTOR LOGIC TIMING
(SHOWING DIRECTION REVERSING CONTROL LOGIC)

9.0 HIRS SYSTEM TEST EQUIPMENT

9.1 General

Test equipment for this program was defined to provide a means of exercising the HIRS unit in bench and chamber tests and to reduce data sufficiently for system analysis. Support from the larger computing facilities at NASA and GE were assumed for full system evaluation. At the system test level the equipment may be grouped into six major categories.

1. Bench Check Equipment (BCE)
2. Targets
3. Chamber and Instrumentation
4. Decompiler and Analog Recording
5. Data/Voice Line to GSFC
6. Mini-Computer

Early program needs defined the BCE, Targets and Chamber requirements. The other major categories resulted from the recognition of a need for more extensive local data analysis and a real time link to the NASA ground station data system. These components were added relatively late in the program but proved very effective in system performance tests.

Original requirements for HIRS system operation and routine testing were met with the design and construction of a Bench Checkout Equipment.

The requirement for real time recording and display of the HIRS serial digital data resulted in hardware design of a decompiler and pen recorder drive system. This system detects the HIRS data stream sync, selects and holds particular words of interest, and gates these selected words to a converter for analog output. The existence of the "Decompiler" for analog display led to consideration of the need for local arithmetic data reduction. The availability of an HP 2100 computer resulted in a HIRS system test equipment growth to include the computer for printing the radiometric data and calculating standard deviation of each channel output. Still another requirement existed; the transmission of the HIRS HDRSS data by telephone line to GSFC for analysis of data blocks over long periods of instrument testing. This was accomplished using GFE and leased interface equipment, working very satisfactorily and aiding early ground station preparedness. A final requirement evolved when the entire system functioned, with data being outputed but with the absence of telemetry for chamber and target temperature points. Following the telemetry addition to the 2100 inputs, the system was finalized and is shown in Figure 9.1-1. The following sections

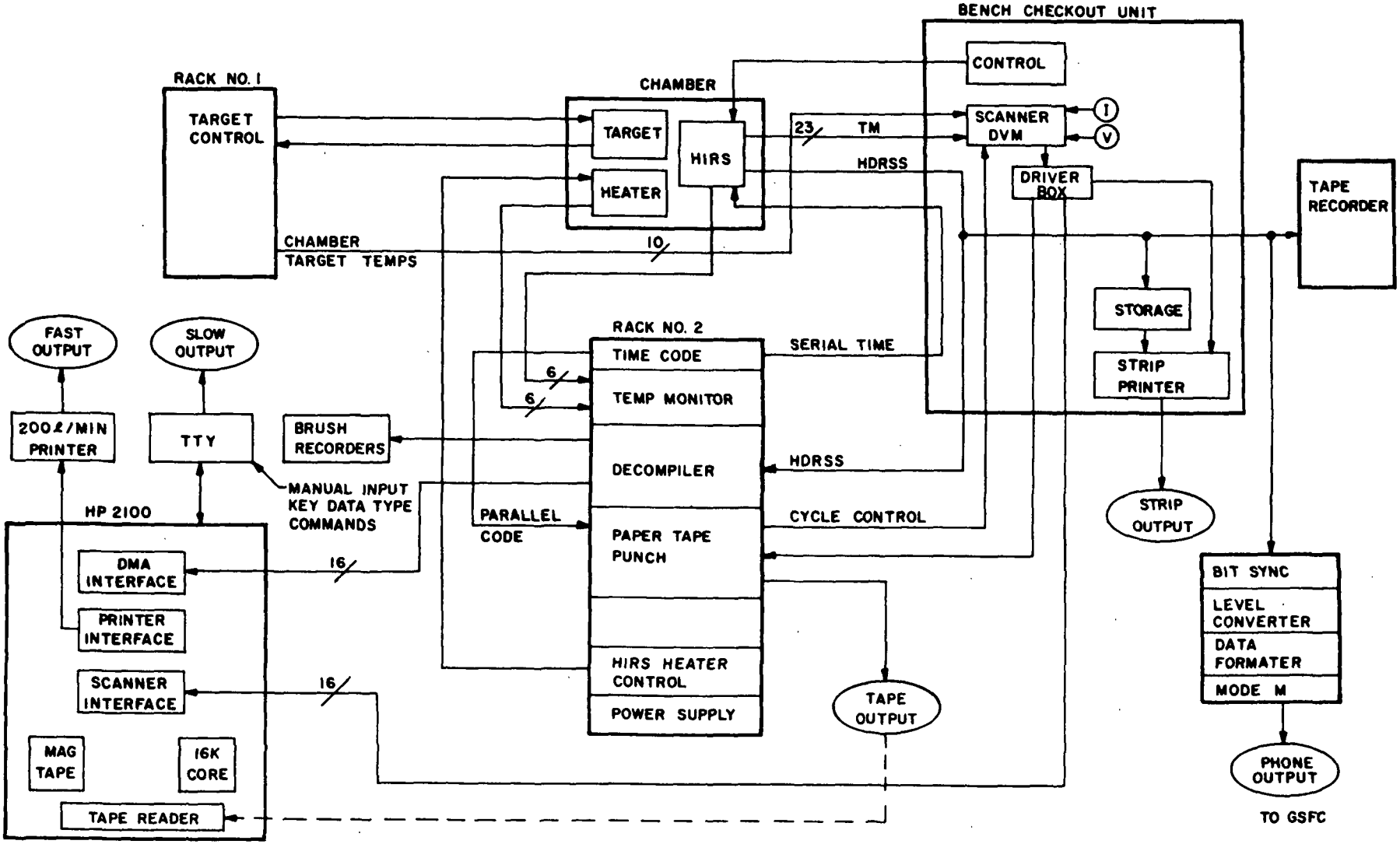


FIGURE 9.1-1 HIRS DATA HANDLING SYSTEM

will describe major parts of the total system. Table 9.1-1 lists the components of the HIRS Test Equipment. Figure 9.1-2 is a reduced copy of the ITT computer printout from one line scan of data.

9.2 Bench Check Equipment

9.2.1 General

The function of the bench check equipment (BCE) is to simulate all necessary spacecraft interfaces, exercise the instrument through its normal functions and provide data retrieval for further processing and evaluation.

A functional block diagram of the HIRS BCE is shown in Figure 9.2-1 (Drawing No. 8118710) and a photograph is shown in Figure 9.2-2. The BCE provides all required S/C interfaces for power, clock, commands, and time code inputs. The oscilloscope is for general diagnostic and monitoring capability. A selector switch allows the printer to accept either spectral data words or DVM-measured telemetry information. Digital "B" telemetry outputs will also be monitored continuously by indicator lights on the control panel. The data control subsystem retrieves the raw digital data from the HIRS instrument and displays the converted information in hard copy on a line printer. The 12 bit spectral, telemetry, and calibration data is decoded and printed as a four digit decimal number, while the remainder of the data is printed in straight binary as "ones" or zeros". A magnetic tape recording system is provided for recording all digital data in the original Bi-Ø-L format.

Primary S/C power is provided by a Hewlett Packard Model 6265B power supply located in the lower-right bay in the BCE. This power is supplied to the HIRS through a switch on the interface panel and is monitored by a current meter on this panel.

The HP Model 181A Storage Oscilloscope is used primarily as a monitor and diagnostic tool in the event of any troubleshooting.

A 40 channel Scanning Digital Voltmeter is incorporated to provide for automatic measurement of analog telemetry outputs from HIRS. This unit comprises the Hewlett Packard 3480B main frame with a 3485A Scanning plug-in unit.

The inputs to the scanner are wired directly to the VIP Analog TM Connector, J-4. The BCD outputs of the DVM are routed to the digital line printer when the mode relay in the Data Control Chassis is in the TM position.

A separate input to the DVM is available at the interface panel when the scanner is on Channel 40. Maximum input to this point is ±10 volts.

TABLE 9.1-1 LIST OF TEST EQUIPMENT

		Stock Number
I.	Bench Check Unit	
1.	HP Scope 181A	33220
2.	HP Dual Chan Amp 1801A	32807
3.	HP Time Base & Dca Gen 1821A	32808
4.	Datadyne Printer 722	33365
5.	HP DVM 3480B and Scan Unit 3485A	33356
6.	Lambda P.S. LA50-038M	11157
II.	Eppley Target Console	
1.	L&N Electromax III	33384
2.	Fenwall TC Con troller	33385
3.	HP Harrison PS 6433B	11369
4.	EG&G Thermoelectric Controller	--
5.	West Inst. JPT-2 (B/P Controller)	--
6.	Digitec DC Voltmeter	--
7.	Digitec Digital Printer 691	--
8.	Digitec Scanner	--
9.	Rosemount Bridges (2 chassis)	--
III.	Ext. Power Source for Heaters & Visible Tar (Chamber Test)	
1.	HP DCPS 6265B	33357
2.	Pwr Res. Decade Box 240-C	33163
3.	Weston Ammeter 931	31049
4.	Weston Ammeter 901	31543
5.	Weston Ammeter 430	661
6.	Sensitive Research Ammeter (University)	1503
7.	NJE PS QR-18-6	10858
IV.	Vacuum Chamber	
1.	Automatic Control Valve NAC 703	11254
2.	TC & Ultra Hi Vac Ion Gage Cont NRC763	11284
V.	HP Computer	
1.	Digital Tape Unit 7970B	33564
2.	2100A Computer 2100A	33564
3.	Tape Reader 2748B	33564
4.	Teletype 2752A	
VI.	Optics Test Support Equipment	
1.	Test Collimator	33403
2.	Nernst Glower P.S. 506	11438
3.	Kepco P.S. CK60-.5M	11314
4.	Nernst Glower	--
5.	Black Body PS (used with 3 above)	--

TABLE 9.1-1 LIST OF TEST EQUIPMENT - Page 2 of 2

		Stock Number
VII.	Visible Target (Bench Test)	
1.	Nobatron PS DCR 40-20A	11381
2.	Visible Calibration Source	--
VIII.	Unclassified	
1.	HP Mag. TApe Recorder	33404
2.	Datametrics T/C Gen Sp425	33541
3.	Brush Pen Recorder Mark 200	33509
4.	HP Timer/Counter 5326A	33226
5.	L&N Temp Potentiometer 8692	11120
6.	Fluke Dvm 8000A	33430
7.	Fluke Dvm 8000A	33429
8.	HP Digital Recorder 5050B	33244
9.	HP 5½ Digit Dvm 3460B	11252
10.	Centronics Printer 102A	--
11.	Weston Ammeter D.C. 10A F.S 931	31098
12.	Weston Ammeter DC 901	6749
13.	Nobatron PS DCR 40-20A	11382

**** TIME ****

ZONE	DAYS	HOURS	MINUTES	SECONDS
ZULU	187	21	14	16
LOCAL	187	16	14	16

**** MEAN AND STANDARD DEVIATION ****

CHAN	MEAN	STD. DEV.
1	-35.5	5.7436
2	338.357	3.43455
3	427.049	3.89212
4	805.214	3.30215
5	541	3.01217
6	768.738	3.69614
7	699.881	4.31222
8	777.262	2.48958
9	526.881	1.91531
10	744.952	2.80202
11	616	4.34489
12	1468.38	1.30575
13	1242.02	4.57719
14	1598.79	1.70417
15	1110.21	1.71842
16	812.548	1.96559
17	0	0

SD AVG CH 11-15 = 2.73008

**** SELECTED CHANNEL MATRIX ****

CHANNEL # = 1

-31	-31	-42	-45	-36	-35	-44	-30	-35	-27	-31	-37
-41	-35	-35	-35	-26	-40	-38	-41	-39	-38	-35	-29
-32	-28	-40	-34	-37	-42	-42	-31	-27	-29	-32	-41
-41	-41	-46	-35	-28	-23	3177	-3193	-2149	-1419		

CHANNEL # = 13

1243	1246	1247	1248	1238	1240	1234	1243
1240	1241	1241	1243	1241	1234	1246	1248
1229	1240	1247	1229	1247	1234	1243	1243
1243	1246	1235	1247	1235	1242	1243	1231
1240	1239	1248	1241	1246	1248	1243	1243
1250	1240	1773	-1775	-545	-391		

CHANNEL # = 0

**** HDRSS TELEMETRY ****

SENSOR	TEMPERATURE	
300 # 1	290.675	K
300 # 2	291.773	K
300 # 3	291.548	K
300 # 4	290.67	K
270 # 1	272.137	K
270 # 2	271.623	K
270 # 3	271.967	K
270 # 4	272.142	K
120 # T	120.284	K

CHAN	NOMENCLATURE	CONV. VALUE		TM VOLTS	LIMIT DEV.
01	SCAN MIRROR	5.89136	C	-5.489	0
02	PRI. TEL. MIRROR	18.3264	C	-4.409	0
03	SEC. TEL. MIRROR	9.66217	C	-5.146	0
04	F/C HSG. # 1	303.948	K	-3.169	0
05	F/C HSG. # 2	304.108	K	-3.214	.107544
06	F/C HSG. # 3	303.675	K	-3.092	0
07	F/C HSG. # 4	303.799	K	-3.127	0
08	F/C MOTOR TEMP.	28.6295	C	-3.599	0
09	RADIANT CODE	164.367	K	-1.53	0
10	RAD. COOLER HSG.	.996826	C	-5.171	.996826
11	BASEPLATE TEMP	20.0652	C	-4.258	0
12	ELECTRONICS	21.3872	C	-4.144	0
13	PATCH TEMP	120.185	K	-.053	0
14	PATCH POWER	119.201	UW	-.299	0
15	CONE COVER OPEN	*****		-.296	.404
16	+15 VDC ELEC.	14.9079	V	-2.146	0
17	-15 VDC ELEC	-14.979	V	-4.988	0
18	+10 VDC ELEC.	10.2314	V	-1.644	.131365

FIGURE 9.1-2 TYPICAL HDRSS OUTPUT

16	+15 VDC ELEC	14.9079	V	-2.146	0
17	-15 VDC ELEC.	-14.979	V	-4.983	0
18	+10 VDC ELEC.	10.2314	V	-1.644	.131365
19	+5 VDC ELEC.	5.30014	V	-2.416	.200135
20	-24.5 VDC TLM	-24.6982	V	-5.513	0
21	SCAN MOTOR TEMP.	22.837	C	-4.02	0
22	F/O MOTOR CUR.	333.828	MA	-1.686	0
23	SCAN MOTOR CUR.	0 A		0	-1.4
24	-24.5 VDC DCU	-24.7	V	-2.47	0
25	INSTRUMENT CUR.	2.474	A	-2.474	0
31	EPPLEY TARGET # 0	221.15	K	-5.20000E-02	*****
32	EPPLEY TARGET # 1	221.15	K	-5.20000E-02	*****
33	EPPLEY TARGET # 2	221.15	K	-5.20000E-02	*****
34	EPPLEY TARGET # 3	221.15	K	-5.20000E-02	*****
35	EPPLEY TARGET # 4	221.15	K	-5.20000E-02	*****
36	EPPLEY TARGET # 5	220.15	K	-5.30000E-02	*****
37	WALL TEMP. SP TGT.	82.15	K	-.191	*****
38	BASE TEMP. SP TGT.	95.15	K	-.178	*****
39	SHROUD TEMP	95.15	K	-.178	*****
40	RAD. COOLER TGT.	41.15	K	-.232	*****

**** CHANNEL ELECTRONIC CALIBRATION ****

CHAN CAL DATA-STEP # 9

CHANNEL	POS	NEG
1	3177	-3192
2	1710	-1715
3	2201	-2217
4	2198	-2203
5	1221	-1225
6	1714	-1726
7	1713	-1728
8	735	-737
9	741	-752
10	1222	-1224
11	1775	-1778
12	1775	-1976
13	1778	-1775
14	1777	-1774
15	1776	-1779
16	285	-281
17	1383	-1381

**** SCAN SUMMARY ****

ELEMENT #	ENCODER POS	ELEMENT #	ENCODER POS
0	84	21	84
1	84	22	84
2	84	23	84
3	84	24	84
4	84	25	84
5	84	26	84
6	84	27	84
7	84	28	84
8	84	29	84
9	84	30	84
10	84	31	84
11	84	32	84
12	84	33	84
13	84	34	84
14	84	35	84
15	84	36	84
16	84	37	84
17	84	38	84
18	84	39	84
19	84	40	84
20	84	41	84

**** COMMAND STATUS SUMMARY ****

1. SCAN MOTOR OFF
2. F/O MOTOR MODE NORMAL
3. CONE HEAT OFF
4. TARGET MODE ON
5. COOLER COVER DEPLOYED
6. COOLER COVER MOTOR OFF
7. PATCH TEMP HIGH
8. F/O HEATER ON
9. SCAN MODE ON

****

****

Figure 9.2-1 (Continued)

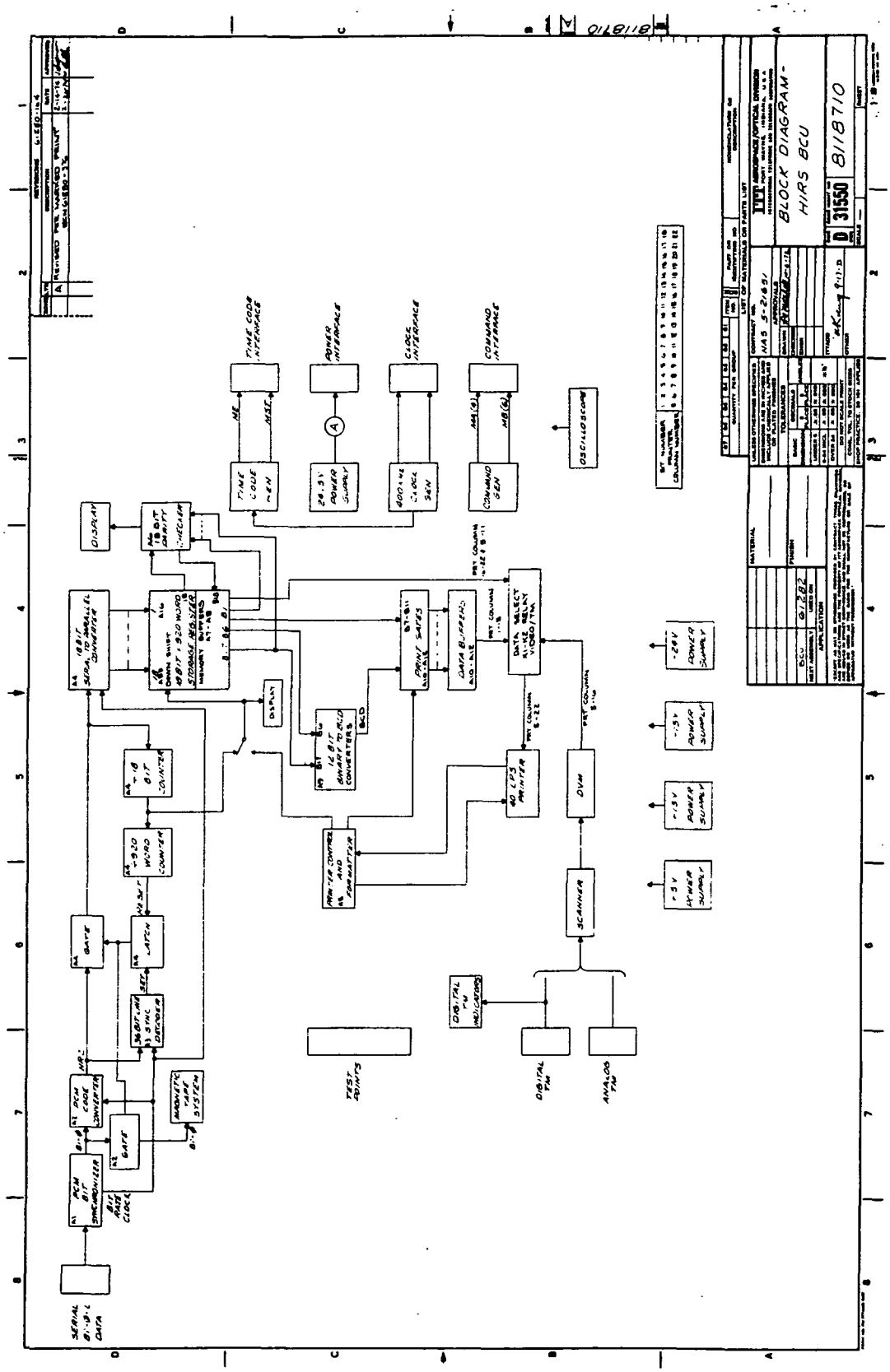


FIGURE 9.2-1 BLOCK DIAGRAM - HIRS BCU

FIGURE 9.2-2 HIRS BENCH CHECKOUT EQUIPMENT

A Datadyne Model 722 printer serves as the permanent hard copy readout for both TM from the DVM and HIRS data from the output data stream. This unit is an 18 column, 40 lines/ second, rotating drum printer.

The printer derives its inputs, both data and control, from the data control chassis. It also provides timing information to the input devices to properly feed data into its buffer registers.

9.2.2 BCU to HIRS Interface

The major BCE to instrument subsystems are the Command Generator, Digital BTM Indicators, 400 KHz Clock Generator, Time Code Simulator, and Instrument Power.

The Command Generator circuit simulates as nearly as possible the command interface from the S/C. The four MA and six MB lines to the HIRS are matrixed in the command switches on the front panel. Each switch is a 3 pole-double throw arrangement so that poles route the command pulses to the proper matrix lines and the third triggers the command generator itself. See Figure 9.2-3.

As a command switch is activated, a negative trigger is applied to a monostable which has a pulse width of about 50 msec. The trailing edge of this pulse then triggers another monostable which provides the actual command pulse. The purpose of the first monostable is to delay triggering the command pulse until all matrix switch contacts are closed and the proper command lines are ready to receive the pulse information.

Both phases of the second monostable are then routed through a complementary driver and the switch matrix to the HIRS system. Resistor values control the delay and command pulse widths respectively.

Direct confirmation of command execution is provided by the front panel Digital BTM Indicators which are controlled by the Digital B telemetry outputs from the HIRS.

Voltage controlled switches with input threshold levels at -2 volts dc are connected to the HIRS digital B output lines. The coils of relays are tied to the outputs of the switches so that as the TM voltage exceeds the threshold, the coil is energized and the relay contacts are switched. Hence, a "zero" digital BTM level switches 24 volts AC power to the appropriate indicator lamp through the normally closed relay contacts. If the TM output becomes a "one" or high level, the relay switches the power to the opposite indicator.

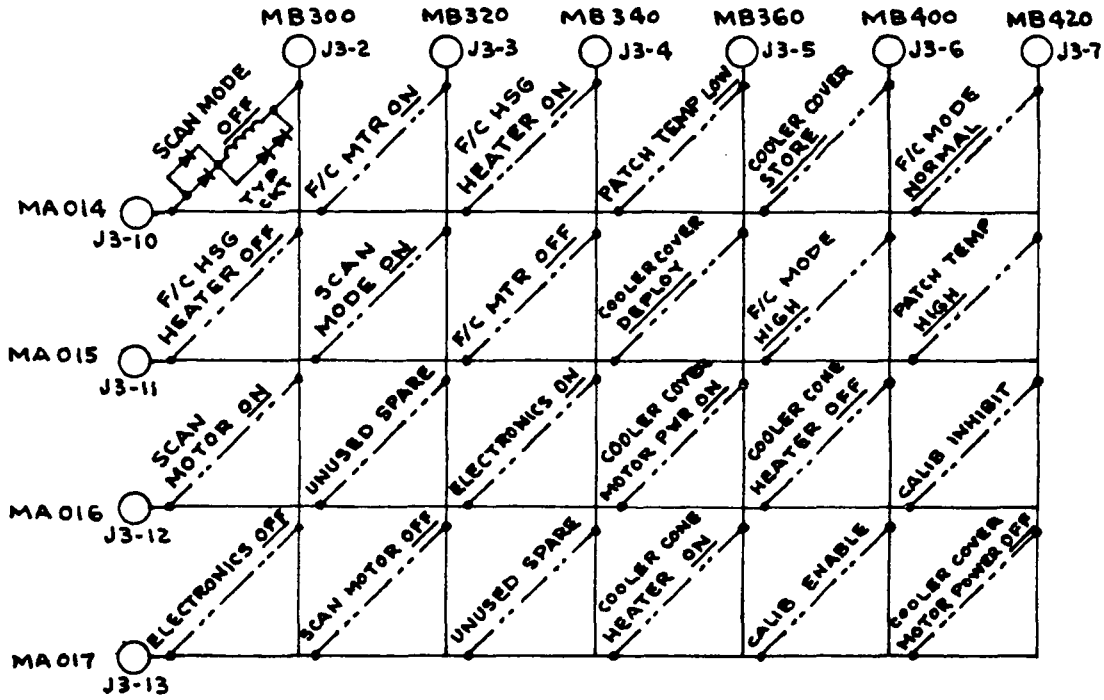


FIGURE 9.2-3 SCHEMATIC HIRS COMMAND MATRIX

The 400 KHz Clock Generator simulates the spacecraft clock input, providing a 400 KHz squarewave from a balanced line drive identical to that used in the S/C Clock subsystem. This driver circuit is fed from a 400 KHz crystal oscillator.

The Time Code Simulator board is designed to provide the standard NASA 36 bit pulse width modulated fixed time code for further processing in the HIRS data system. Also provided is the MST Strobe signal. Only strobes and a fixed pattern time were available.

An astable multivibrator generates the basic 24 KHz Clock signal which is further divided by Ripple Counters to 1 KHz, 100 Hz, 10 Hz, and 1 Hz respectively. The remaining logic decodes these frequencies into the proper time-width relationships for the time code (ME) and Strobe signals (MST). These are further buffered by interface circuits which are copies of the actual clock interface circuits provided on the S/C. This board became non-functional with the procurement of a model SP-425 Datametrics NASA 36 Time Code Generator. The SP-425 simulates the Nimbus Time Code and Strobe gates.

The -24.5 volts S/C buss is routed from the main power supply to the instrument through the Instrument Power Switch and a 3 ampere current meter for continuous monitoring and observing noise and transients on the buss.

Terminals are available on the front panel for monitoring the outputs of the HIRS test connector or for applying power to the various heaters within the instrument. These test points are numbered to correspond directly with the pin numbers on connector J7.

9.2.3 HIRS Data Control

The Data Control Panel, which actually comprises a complete system with some 30 printed circuit cards, has a number of functions which are listed below.

1. Retrieve the raw Bi-Ø-L serial bit stream from the instrument and further process to remove noise and extract the synchronous bit rate clock signal.

2. Serve as the interface for the magnetic tape recorder. The enhanced Bi-Ø data is fed to the recorder through a variable attenuator and can be either continuous or a single scan line of data.

3. Convert the serial Bi-Ø data to parallel NRZ, store a complete scan line, and print the data as digital numbers on 18 column tape.

4. Serve as the data and printer control interface between the HIRS analog TM outputs and the Scanning DVM and printer.

A brief description of each board in the system is given in this section. Refer to Figure 9.2.1.

The PCM Bit Synchronizer consists of a narrow band phase-locked loop and a coherently clocked integrate and dump data filter. Optimum bit detection is accomplished by utilizing the maximum pulse time interval for data integration. Data degraded by DC level unbalance and noise are reconstructed to stable, low noise data signals along with a Coherent Clock.

The PCM Code Converter, receives Bi-Ø data and clock from the PCM Bit Synchronizer, converts the data to NRZ and the clock to the NRZ bit rate. A 4009 CMOS buffer isolates the output of the clock. The NRZ data is reinserted into the converter and converted back to Bi-Ø-L for the tape recorder output. A control signal is switched into U2 to gate the recorder output for either full time data or a single line of data.

The function of the line 36 Bit Line Sync Decoder is to recognize the 36 bit line synchronization signal at the end of element 46 and initiate the BCE logic to process the data line immediately following.

Closing the Start Load switch sets the bistable latch which enables the clock transmission gate allowing the bit rate clock to advance the 36 stage serial in-parallel out shift register. This register is also reset with the Start Load switch. NRZ data is now clocked through the shift register until the line sync sequence code is recognized at the parallel outputs by the 36 bit comparator. This code is preset into the comparator by hand wiring inputs to logic 1 or 0. The proper code is:

0 1 1 1 0 1 0 1 1 1 1 0 1 0 1 1 1 1
0 0 1 1 0 0 1 1 0 1 0 0 0 0 0 0 0 0

Upon recognition, a pulse at the comparator output resets the bistable latch, stopping the clock, and enables the clock gate in the serial to parallel converter.

The Serial-to-Parallel Converter, on command from the line sync decoder, begins receiving input data into its 18 bit serial in-parallel out shift register. At the same time, two counters operate on the input bit rate clock signal. The word counter at the count of 18, provides a down-shift pulse to the main data registers such that each 18 bit word is read into the main register from the serial-to-parallel register.

A second counter is the element counter which, when the Read/Write switch is in the Read position, counts the shift pulses from the word counter and resets the input clock gate at the count of 46.

If the Read/Write switch is in the Write position, the counter input is derived from the printer shift pulses. In this mode, the counter is reset when the start Print switch is depressed, and inhibits the printer at the count of 46.

The Printer Control and Formatter circuit provides overall control of the printing sequence including formatting of the data into that shown in the example below.

One Scan Element

-ØØ24	1
-Ø7Ø2	1
-ØØØ3	1
-Ø768	1
+Ø714	1
+Ø668	1
+Ø768	1
-ØØ32	1
-Ø665	1
-ØØØ5	1
+Ø72Ø	1
-Ø7ØØ	1
+Ø672	1
+Ø651	1
+Ø671	1
+Ø691	1
-Ø7Ø2	1

Ø11ØØØØØØ111111111
ØØØØØ1ØØ1ØØØ1ØØØØ1
11111ØØ11Ø1Ø1ØØØØ1

The first three words are printed out in straight binary format, while the seventeen data words are routed through the binary-to-BCD Converter and are printed as four digit binary numbers.

The print sequence of one full data line is initiated by pressing the Start Print switch, which resets the two counters and triggers a monostable. The leading edge of the monostable output pulse results in a print command. Two microseconds after the print command is received, the printer has latched the data into its memory-buffer and is in the printing sequence. A second monostable is triggered providing a shift pulse for the data storage register to advance a new word into the printer memory-buffer. A pulse also commands the parity check circuit to examine the word being printed for proper parity and so indicate in bit 18.

The Parity Checker circuit is a standard 18 bit odd parity checker using exclusive or packages. A parity check is initiated by the trailing edge of a print command pulse, which triggers a monostable. The monostable provides a one millisecond delay to allow all inputs to settle before processing. If the number of "ones" at the input is even, indicating a parity error, the parity condition is printed in column 18 on the printer. A "one" indicates true parity, while a "zero" indicates a false parity, or bit error.

A hold output drives the front panel indicator light. This output only indicates a single error per data line. If the light comes on during a printout, it indicates only that an error has occurred and the data should be checked.

Memory Buffer boards contain high current non-inverting buffers to interface the CMOS output logic into the TTL printer logic.

The 12 bit Binary-to-BCD Converter operates on the 12 data bits of words 4 through 29 of each element. The 1-2-4-8 BCD outputs directly feed the printer columns 8-11 and print the digital number corresponding to the binary outputs in bits 6 through 17.

The Print Gates are actually single pole-double throw electronic transmission gates. It is these gates which perform the actual formatting under the control of the printer control circuits.

Column 7 is used for the polarity signal designation during spectral readout in words 4 through 20. In the first three words the "two" and "eight" inputs are grounded by the print gates while the "four" input is wired low. During spectral printout, the "two" and "eight" inputs are switched high. Since the printer code is 1010 for (-) and 1011 (+), the "one" input can indicate both polarities. The instrument code is "0" for (-) and "1" for (+).

Columns 8 through 11 use the print gates to switch printer inputs between BCD outputs in the case of spectral data, and to ground and a bit input in the other.

Since the data rate from the HIRS instrument is nearly five times the maximum printer rate, data Storage Register must be provided in the BCE. The storage register here is capable of 922 words even though only 920 are required. Eighteen storage boards are implemented.

Each of the boards provide data storage for 1 X 922 bits. The 4031, 4006 and 4014 CMOS packages are static shift register that together comprise 922 stages of storage.

Since the printer is utilized for printing both data and analog telemetry information, it is necessary to switch printer data and control signals between the Scanning DVM and the Data Control System. This is accomplished by two 48-pole double throw Data/Telemetry Relays. Control of these relays is by the Data/TM switch.

9.3 Data Decompiler

The HIRS Data Decompiler is an interface unit between the HIRS and a multi-track pen chart recorder. It selects proper bits from the HIRS output data stream, stores the selected bits and provides an analog signal output related to the binary number selected; the primary goal being the presentation of encoder position, element number, time code, and spectral channel signal information in real time.

9.3.1 Analog Recording

Basic HIRS output data is serial in time, recurring every 4.8852 seconds. During this cycle (46 scan element times), 16,560 bits are outputted. For simplicity these bits are grouped into 18 bits forming words one (1) through nine-hundred-twenty (920).

Basic HIRS output data occurs, therefore, in serial word form every 5.31×10^{-3} seconds and each data channel is updated every 20th word. One exception is in the 46th cycle (Scan Element Block 46) with the final two words. These two words serve as a 36 bit synchronization point in the data stream and are decoded using a circuit copied from one in the HIRS Bench Checkout Equipment (8117795). Two additional boards, 8119385 (Code Converter), and 8117813 (Serial-to-Parallel Converter), are used in the Decompiler. These three board assemblies provide the decompiler with a phase-lock-loop input, extracted clock, extracted signal, 18 bit sync pulses, and 36 bit sync pulses. Armed with these signals a WORDSELECTOR (Sch. 8120736) board was designed to generate word 1 through word 20 gating signals which are synchronized with the HDRSS data. These word gates are used to enable the HDRSS data into serial shift registers located on the WORD STORAGE AND D/A CONVERTER BOARDS (Schematic 8120739). Four words may be stored on one board and each word stored is applied to a D/A whose output is the analog of the digital word.

The stored words are updated every 20th word which cause outputs from the D/A which resemble noise, however, the proper DC level is maintained for a 95% duty cycle.

The present Decompiler configuration outputs: MODE, UNIT SECONDS, Element No., ENCODER Position and CHANNEL #17 are connected to five channels of a BRUSH ANALOG RECORDER. The

remaining analog channels of the Brush recorder display -24 VDC HIRS input, input current and HIRS F/C Sync. Figure 9.3-1 is a block diagram of the Decompiler.

9.4 Telephone Link

9.4.1 System Description

A request by NASA for a data phone link for the purpose of supplying a GSFC Computer with HIRS data was received after assembly of the Protoflight Unit in January 1974. Three data sets were considered; the 201, 203 and 208. The 208A set with dedicated line was installed primarily because of the availability of the units at both Fort Wayne and Greenbelt.

The 208A data set is a four wire set designed for transmission and reception of synchronous 4800 bps serial binary data on basic unconditional 3002-type 4 wire channels. The data set uses Phase Shift Keyed (PSK) modulation. The set is 16 inches wide, 4¾ inches high and 12" deep.

Since the data set sending rate is fixed at 4800 bps and the HIRS rate is 3898 bps a "bit stuffer" was required which provided filler bits. A Digital Data Formatter Encoder (bit stuffer) was located at GSFC along with a Dynamic Signal Conditioner (phase locked loop amplifier). These two units along with the 308A data set from General Telephone Electronics and a 4 wire phone line from ATT and handset made a quickly assembled and highly reliable data link to GSFC. Approximately 250 hours of HDRSS Data from various tests were sent to GSFC. Only one instance of equipment failure occurred, due to tornados in the area. Figure 9.4.1 indicates the general data path for the data link relative to the complete data system.

9.5 Computer Data Reduction

9.5.1 General

Originally HIRS data reduction was obtained through the BCE and manual calculations. The BCE is limited to acceptance and printout of one line of data once every two minutes. Data reduction and calculations required hours. Because of the volume of data and delay in determining instrument output results added capability was recognized as a necessity.

During the HIRS Review of April 9-10, 1974, a concern for the need of real time monitoring of HIRS TM Data was voiced. A monitoring system design using the HP2100 was immediately initiated. The existing TTY printer, a limiting item in the data reduction hardware, was replaced with a Centronics Model 120 (200 line/minute) printer. The HP2100 with 12K Core, was increased to 16K, and necessary cables were assembled. The TM

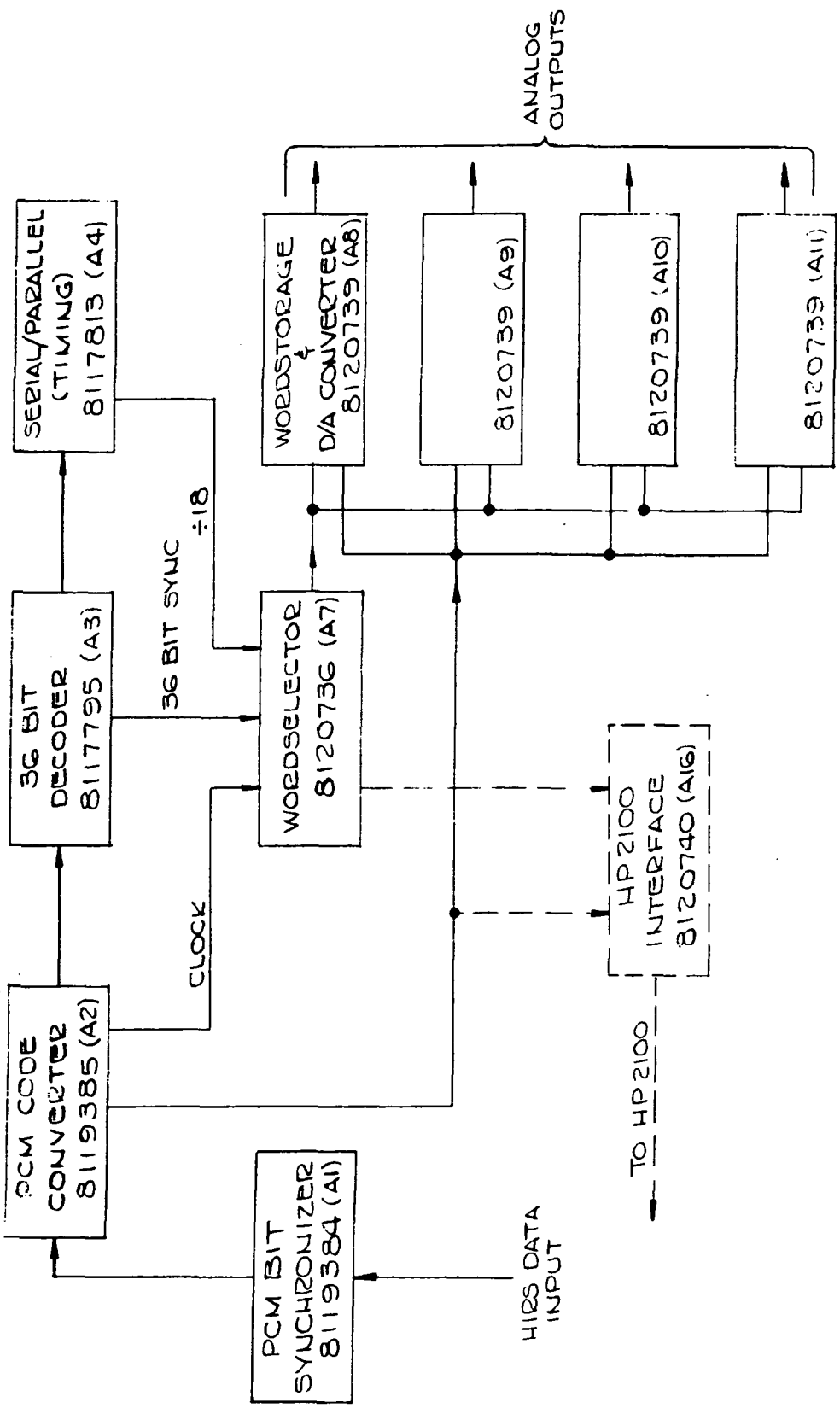


FIGURE 9.3-1 BLOCK DIAGRAM, HDRS DECOMPILER

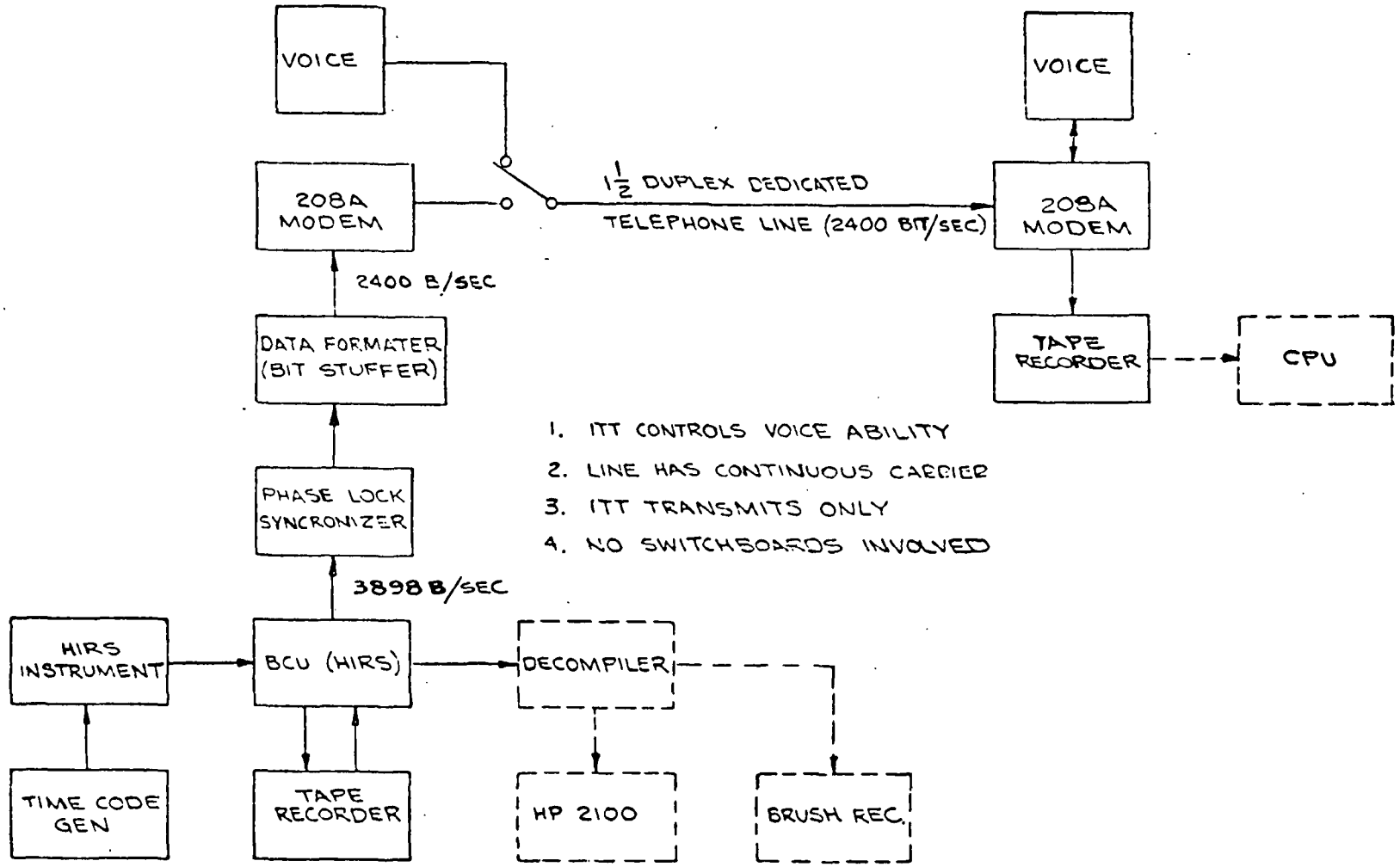


FIGURE 9.4-1 HDRS DATA PATHS

data from the scanning DVM was routed to the slow paper tape through the BCU, and the HP2100. A junction and driver box were added to facilitate the dual output.

All of this was integrated for the Protoflight pre-vibration T/V in June, with the exception that TM limits were not inputted. Limits were added after the T/V test.

Figure 9.5-1 is a block diagram of the basic real time TM monitor.

Figure 9.5-2 shows the HP2100 CPU System used for HIRS Data Reduction.

The Decompiler, already used to form words of the HIRS serial data stream, was modified to feed data words to the mini-computer. This was achieved by adding one logic card and a cable to the computer interface card. The computer was programmed to expect an array of data numbers of 17 x 46. Loading time was limited to the 4.88 second generating time of HIRS. Calculations using the array of $\bar{X}$ (mean) and Σ (standard deviation) required ten (10) seconds and print out required approximately fifteen (15) seconds.

9.5.2 The Working System

Under normal testing, analog TM and chamber temperatures are recorded by the paper tape punch. Initiate pulses originate in the tape punch at a rate selectable by front panel switches. Upon initiation, the DVM Scanner samples each TM and temperature transducer, and outputs the sampled level to the BCU slow printer, HP2100 and Paper Tape Punch. Data to the HP2100 is placed in memory, converted to proper units, compared to limits and outputted if out-of-limit or as a complete listing if desired. This cycle may be repeated at up to 4 cycles per minute. See the block diagram figure 9.5-1.

As HDRSS data is desired, operator commands via the TTY Keyboard stops the TM data acceptance and enables the HDRSS input acceptance. HDRSS data is gated to the HP2100 by a switch at the decompiler. The present input array is 19 x 46, 16 Bit words. After HDRSS printout operator commands return the HP2100 to TM monitoring.

At this writing, programs to the HP2100 are loaded by paper tape.

A typical HDRSS HP2100 output and the necessary constants for Analog TM conversion equations are included in Section 9.8 for the HIRS Protoflight model.

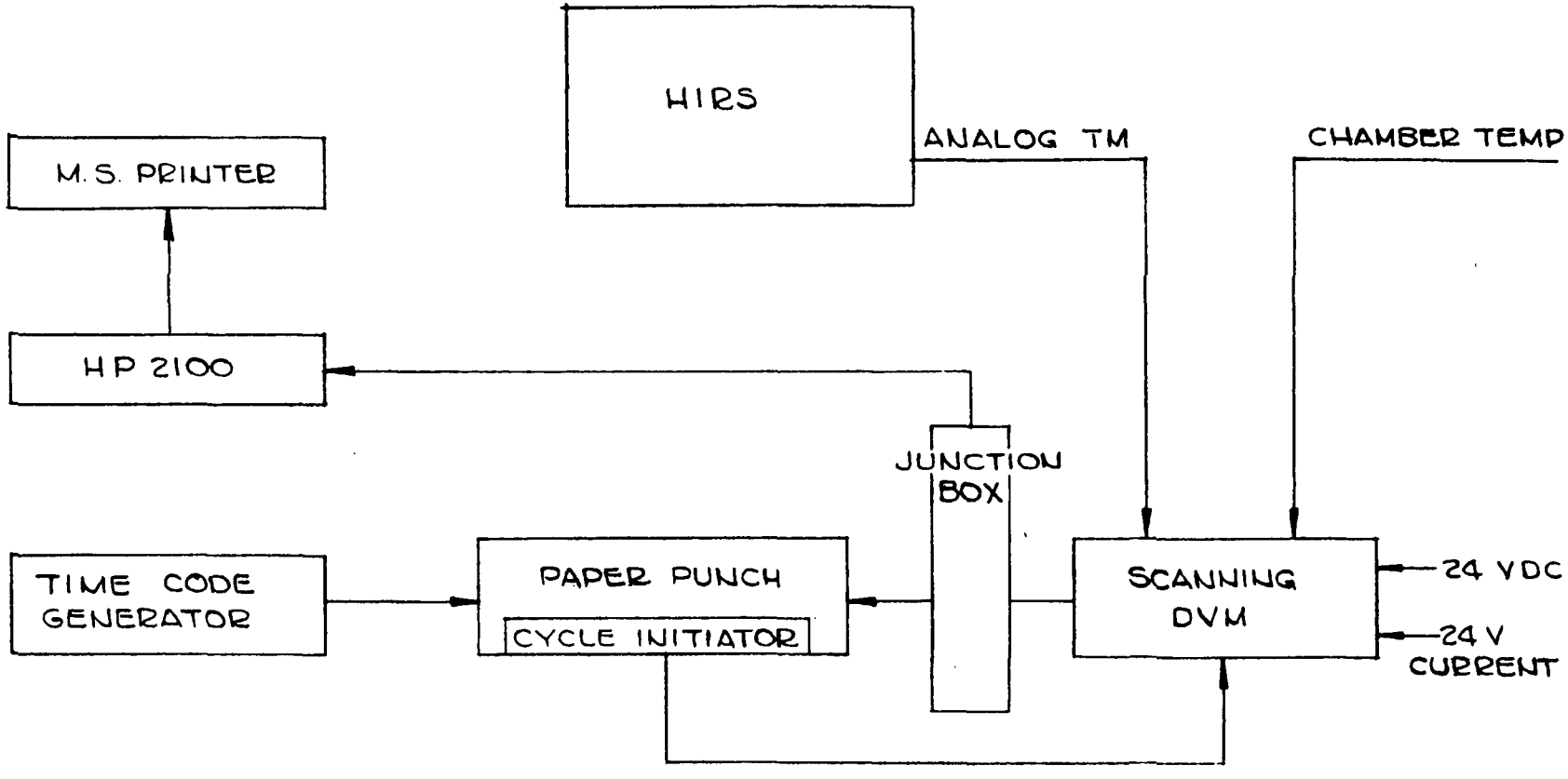


FIGURE 9.5-1 BASIC REAL TIME TM MONITOR

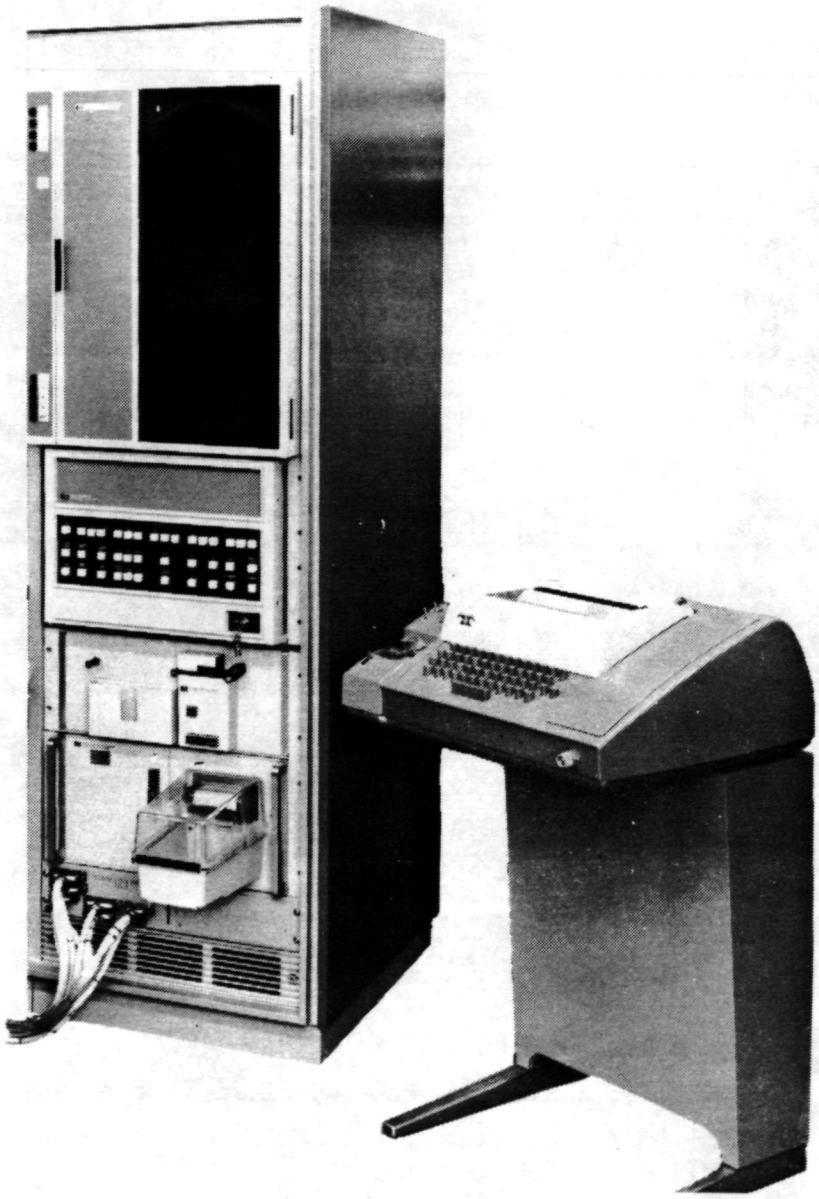


FIGURE 9.5-2 HP2100 COMPUTER

9.5.3 Alternate Output Sequences

It soon became apparent that periods of automatic TM checks were seldom required as expected. Constant observation by test personnel necessitated a slight change in CPU operation. This required only slight changes to the CPU program in the areas of CALL sequence. (CALL being subprograms outside of BASIC language.) Through a set of selectable options it was possible to operate in a more meaningful sequence for full time test personnel.

After outputting data the CPU returned to an "INPUT HIRS HDRSS DATA" condition. Pressing the start switch on the Decompiler permitted loading to memory one complete data block. After receipt of the HIRS HDRSS DATA the CPU responded with "INPUT ANALOG TM DATA." Pressing the initiate switch on the sampling DVM inputted all TM data. At this point the CPU returned to its internal program, outputted data as requested during the initial program option selection, and returned to a "INPUT HIRS HDRSS DATA" state.

This sequence, used in nearly all testing of both the Protoflight and Flight units permitted complete outputting of all data HDRSS, TM and all computations every eight minutes. Computations and TM data alone were available every three minutes, five minutes additional being due to the printout time required for all the HDRSS data numbers.

9.6 Chamber Instrumentation

9.6.1 General

Proper performance of the HIRS is based upon the instrument being operated in an outer space environment. This imposes the restriction that the radiant cooler must look at a cold target that simulates deep space. Calibration of the infrared channels must be performed under this condition and it is desirable to test the visible channel under actual operating conditions also.

In order to provide the proper environmental conditions for HIRS operation, a vacuum chamber instrumented with infrared, visible and space target is used. Figure 9.6-1 is a functional block diagram of the vacuum chamber instrumentation. The HIRS is mounted so that during scan it can look at the three targets depending upon the tests being performed. All target controllers, temperature monitors and power supplies are mounted in a separate rack near the vacuum chamber. Figures 9.6-2 and 9.6-3 are photographs of the chamber instrumentation.

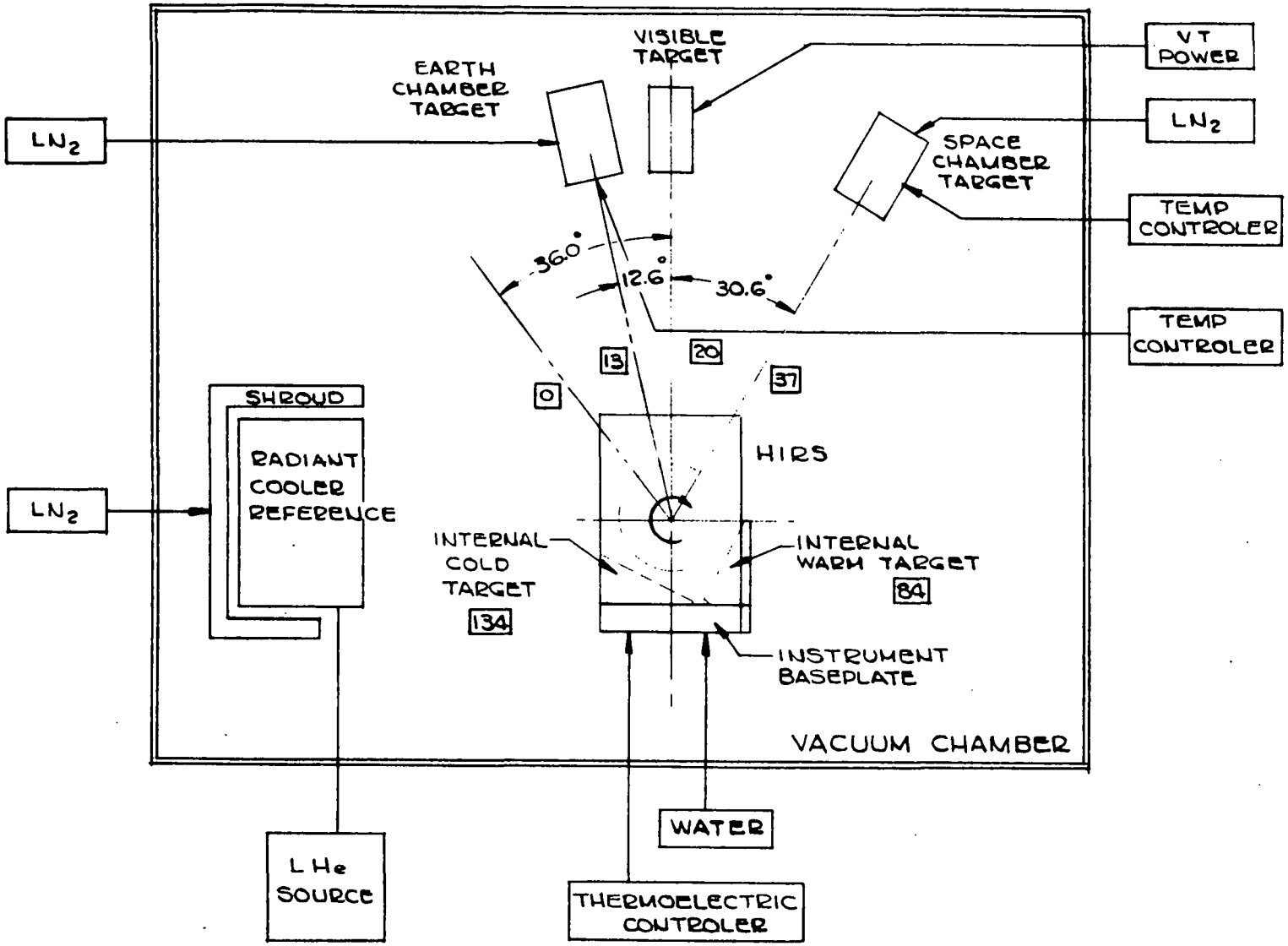


FIGURE 9.6-1 VACUUM CHAMBER INSTRUMENTATION

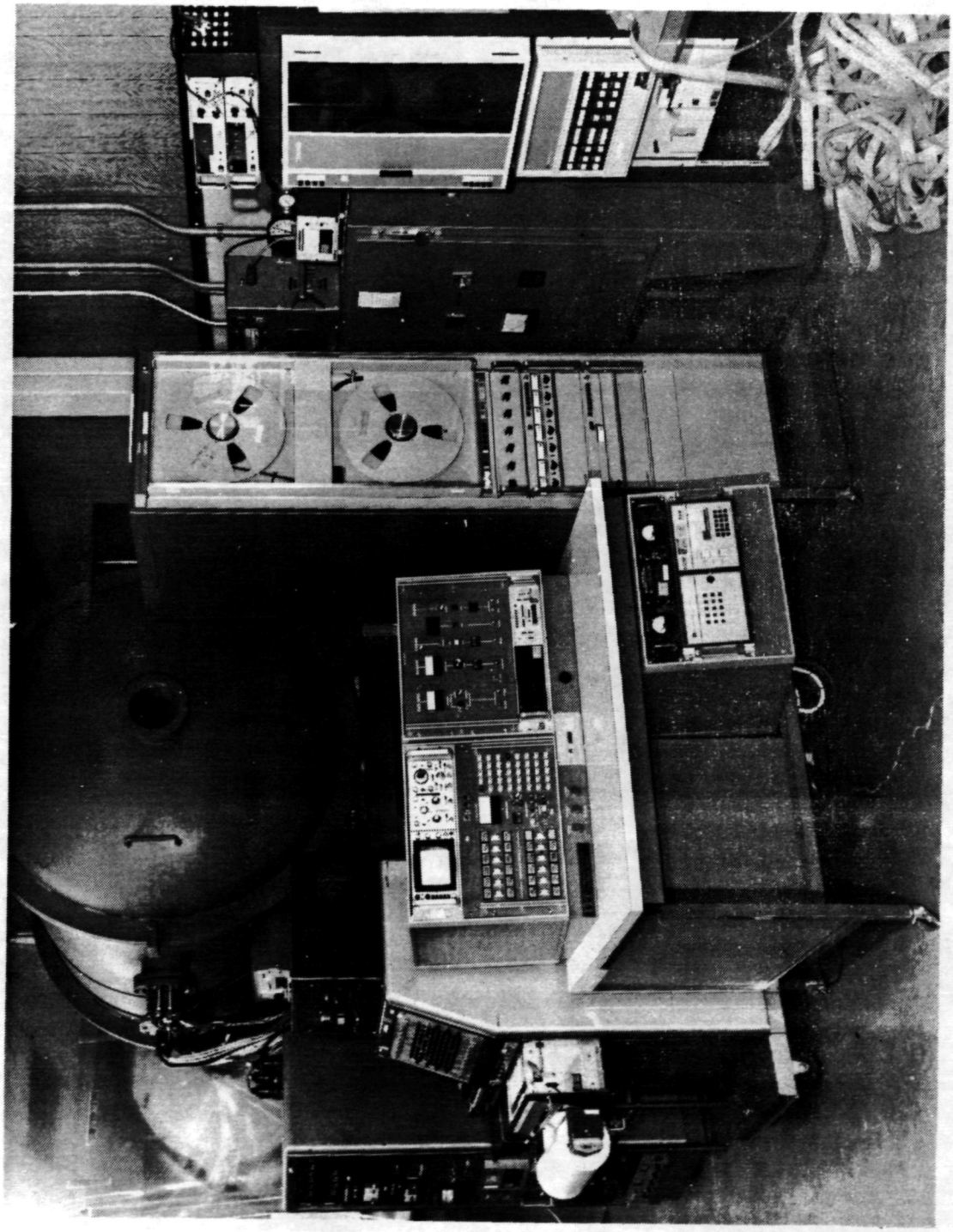


FIGURE 9.6-2 HIRS CHAMBER INSTRUMENTATION

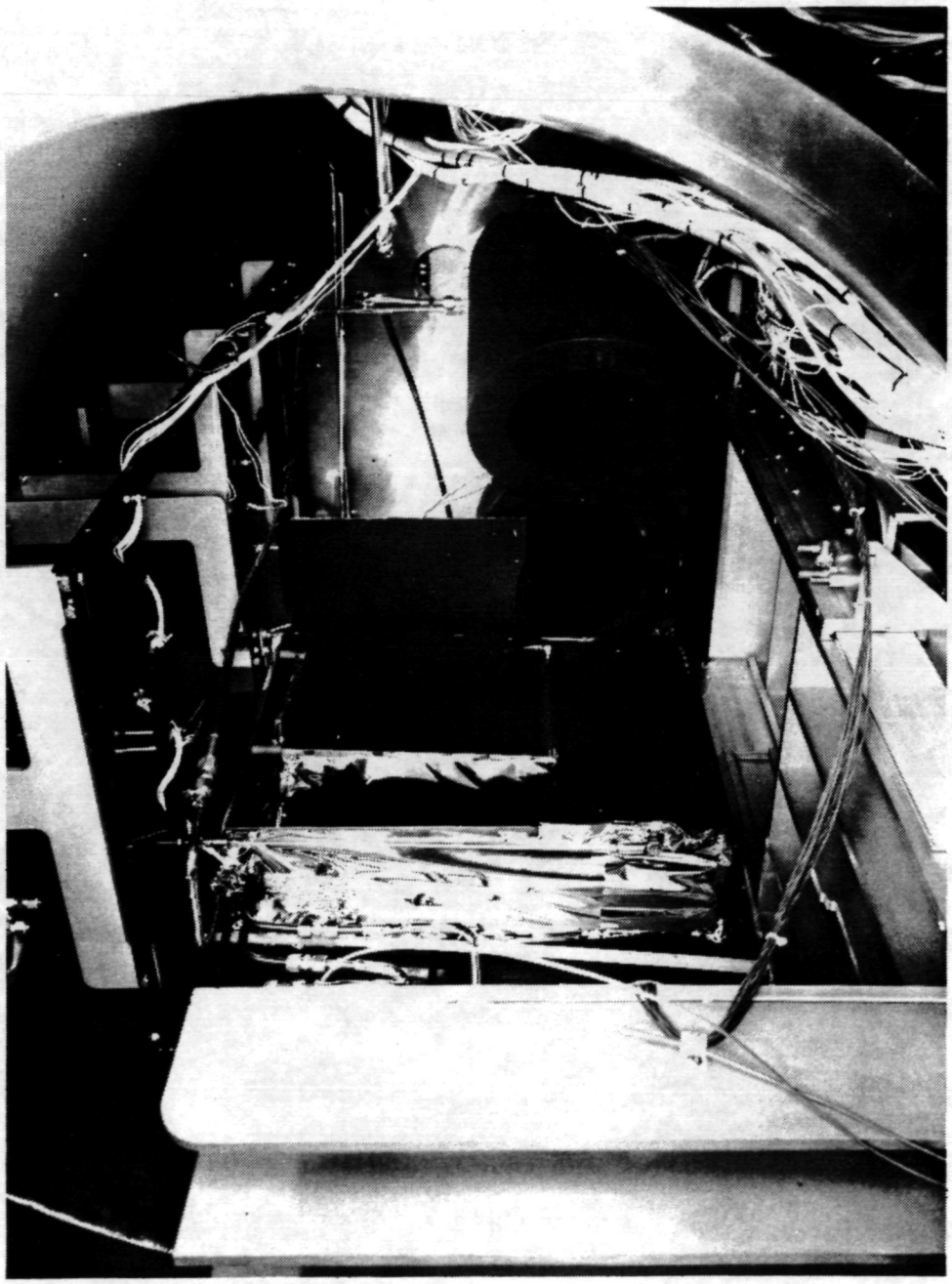


FIGURE 9.6-3 CHAMBER INTERNAL COMPONENTS

9.6.2 Baseplate Mounting

The instrument is mounted on a temperature controlled baseplate. This mount simulates the mechanical spacecraft interface and provides the thermal reference for the instrument during T/V testing. The operating temperature range of this plate simulates the expected thermal ranges predicted by the thermal math model.

Temperature control is achieved by circulating water through cooling coils attached to a copper plate. The water acts as a reference for thermo-electric heaters attached between the water plate and instrument mount. A proportional temperature controller applies the proper amount of power to the heaters for temperature control. Temperature sensors are mounted to the instrument plate to provide a reference for the controller, and for test monitoring of the mounting plate temps.

9.6.3 Vacuum Chamber

HIRS vacuum testing was performed in a NCR Equipment Corp. ultra high vacuum chamber having dimensions of 4 feet diameter by 6 feet in length. Both chamber ends have doors with windows. Rough pumping is provided by a Welch Model 1398 forepump having displacement capacity of 1400 liters per minute. High vacuum is provided by a 16" diffusion pump. Rough pumping time was approximately five (5) minutes and diffusion pump time approximately thirty (30) minutes. Pressure at sixty (60) minutes is normally 20×10^{-5} mmHg.

Within the chamber are mounted two targets, a radiant cooler target and shroud, and the visible target. External to the chamber is a helium cryogenerator and LN_2 supply. The radiant cooler is cooled by a $20^{\circ}K$ feed line from the cryogenerator. The spacetarget and radiant cooler shroud are cooled directly with the first stage gas of the cryogenerator at $80^{\circ}K$. Separate LN_2 lines supply the earth chamber target (ECT). The visible target is an incandescent lamp powered by a direct current voltage source. The LN_2 and Helium targets are generally stable within four hours.

9.7 Chamber Radiant Test Targets

Radiant inputs to the HIRS instrument are from two blackbody targets referred to as the Earth Chamber Target (ECT) and Space Chamber Target (SCT).

9.7.1 Earth Chamber Target

This low-temperature blackbody was designed in accordance with ITT Specification No. 8117846 and Drawing No. 8117847

to provide a large area infrared radiance source to be employed in the radiometric calibration of the infrared detectors in the HIRS system.

The ECT source, operating between 180K and 340K utilizes thermoelectric heat pumping to temperature control an octagonal cavity array radiator of 130 in^2 (8 inches across flats) with an emissivity greater than 0.998. Features of the blackbody include excellent stability and uniformity as well as rapid response to controlled temperature changes.

Essentially, the entire blackbody is contained within a cylindrical stainless steel shell 12 inches in diameter and 11 inches high attached to a stainless steel baseplate (See Figure 9.7-1). At one end is an eight inch diameter viewing aperture. All electrical and coolant connections are concentrated near the base of the unit. The entire exterior surface of the source is covered with 3M 101 C10 black velvet paint over an undercoat of Cat-A-Lac black.

The two main components (or subassemblies) are the source and baffle assemblies which are attached to the baseplate through standoffs and support straps. The temperature controlled baffle system is employed to reduce thermal loading on the cavity radiator.

The source assembly consists of the blackened, aluminum honeycomb array of cells, 1/4 inch wide by 1 inch deep, attached to a copper uniformity plate. Mounted in the plate are six platinum resistance temperature sensors. Also located near the center of the uniformity plate, in the under surface, are the control thermistors. Placed between the above plate and a copper heat sink plate are nine single-stage modules. An over-temperature cut-off switch is mounted to the heat sink plate. Below the heat sink is an auxiliary thermofoil heater (350 watts -110 VAC) which is separated from a liquid nitrogen cooled plate by a thermal impedance section made of Delrin. All exposed copper surfaces are gold plated to reduce radiative interchange with neighboring components.

The baffle system, temperature controlled by resistive heating and liquid nitrogen cooling, is made up of eight flat sections approximately 3 1/2 x 8 inches in size extending above the source array to form a cavity with octagonal cross section. Copper plates with blackened honeycomb cells 1/4 inch wide by 1/2 inch deep form a cavity wall with high emissivity. A thermofoil heater (100 watts each) (800W total) extends over the back surface of the cavity plate, and is separated from a cooling coil plate by a thermal impedance section similar to the primary target radiator. Liquid nitrogen is passed through tubing attached to the exterior cold plate. Several layers of

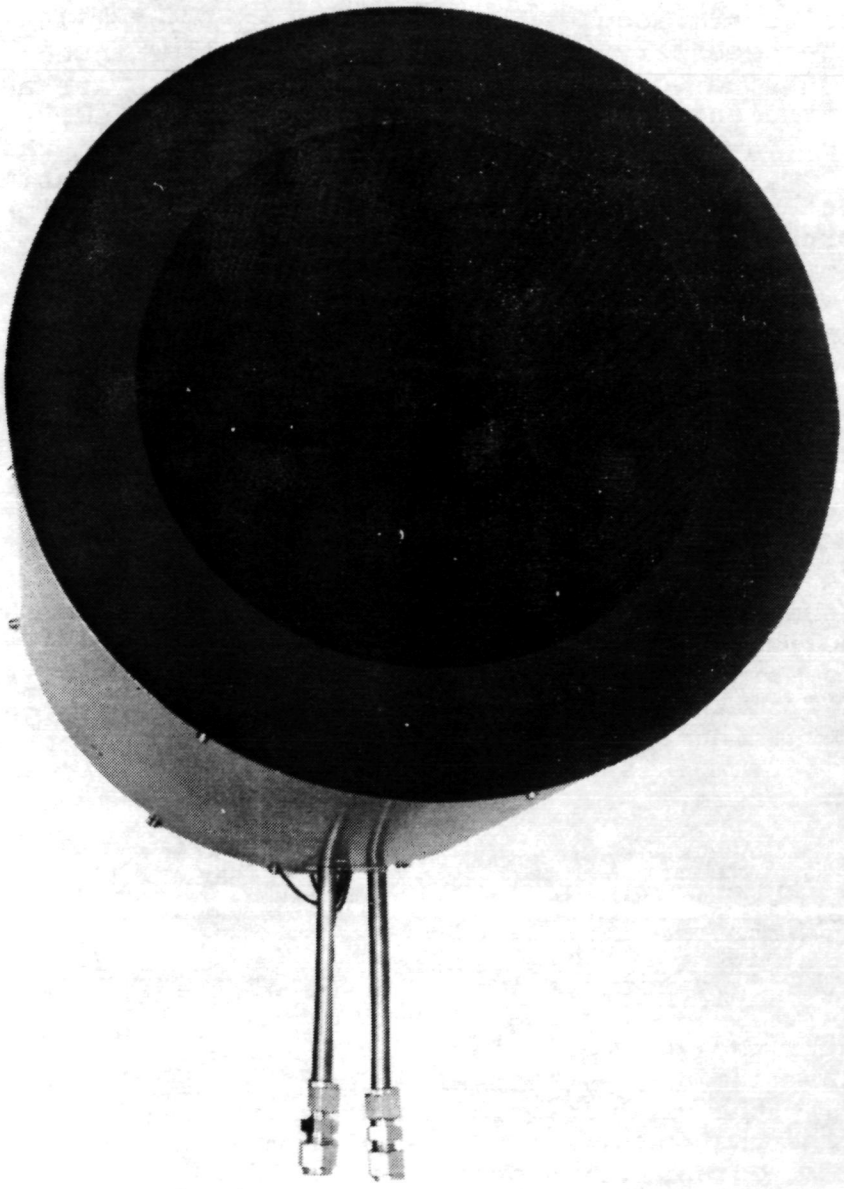


FIGURE 9.7-1 CHAMBER TEST TARGET

multilayer insulation fill the space between the outer shell and the baffle system. Three tapped mounting holes are provided on the exterior cylindrical surface.

Three electronic controllers are employed to obtain the required temperature control over the range of 180K to 340K. The thermoelectric module controller, EG&G Model 1116-26CF-R-DS, provides the necessary power to the modules. This controller has been modified so that two thermistor sensors are available for more efficient control over the operational temperature range. The Fenwal controller, model 524, stablizes the module heat sink temperature through the auxiliary heater utilizing a copper-constantan thermocouple located in the heat sink. A Leeds & Northrup Electromax Mark III, is operated from one of eight chromel-constantan differential thermocouples, to maintain the walls of the source at the same temperature as the target radiator.

The six calibrated PRT sensors are used to measure the target radiator temperature necessary for the blackbody radiation calculations.

9.7.2 Space Chamber Target

A second blackbody source with the identical configuration of the ECT is provided as a constant cold source. The SCT has cooling coils distributed over the baseplate and wall sections to maintain a single cold condition. First stage cold Helium gas from the cryogenerator is circulated through these coils, maintaining a temperature of 84 ^{o}K. Thermistor temperature sensors from this blackbody are sufficient to record the target temperature.

9.8 Data System Programs

9.8.1 System Objectives

The five principal objectives of the system are:

1) the decompilation of HIRS data,
2) the analysis of HIRS data,
3) the production of hardcopy results,
4) the operation of the system by non-computer oriented personnel, and
5) programming flexibility for ease in modification of the main program.

9.8.2 Data Description

The HIRS instrument data is composed of 23 analog channels and a Bi-Ø-L serial digital data stream of 920 18-bit

words with a period of 4.8852 seconds. The 920 word data stream is divided into 46 scan element blocks, 0 thru 45, each consisting of 20 words.

The data output format is described in Section 2.1. In the programming of the HDRSS data through the analysis program it was necessary to modify the designators on the word numbers such that Bits 1-18 become Scan Grid Word Numbers 17-0, and the nomenclature for Word Number 1-20 becomes Scan Element Word Numbers 20 N+1 - 20 N+20 where N is the scan element number. The use of BASIC language in the computer led to a simple operating and display procedure where the data output was easily recognized.

9.8.3 Computer Program Organization

The HIRS digital data is decompiled partially by hardware prior to its final decompilation by a software program. The analog data is first converted to digital data via hardware methods and then decompiled by a software program.

The analysis of HIRS data is accomplished by a software program with some additional analysis done manually by the engineering staff.

The hardcopy results are obtained via a medium speed line printer connected as a peripheral output device to a HP2100 mini computer.

The operation of the system by non-computer oriented personnel is faciliated through the use of a software program that interrogates the person desiring to use the system. The software program then configures the system according to the person's responses to the questions.

In addition, the program displays the operational status of the program at all times.

Programming flexibility is realized as a result of writing the principal analysis source program in BASIC language.

9.8.4 System Description

The principal parts of the HIRS data collection and analysis system, reference Figure 9.8-1, is a HP2100 computer system with 16K memory and an analysis program written in BASIC.

A supporting element is a FORTRAN IV program for the generation of the platinum sensors telemetry table.

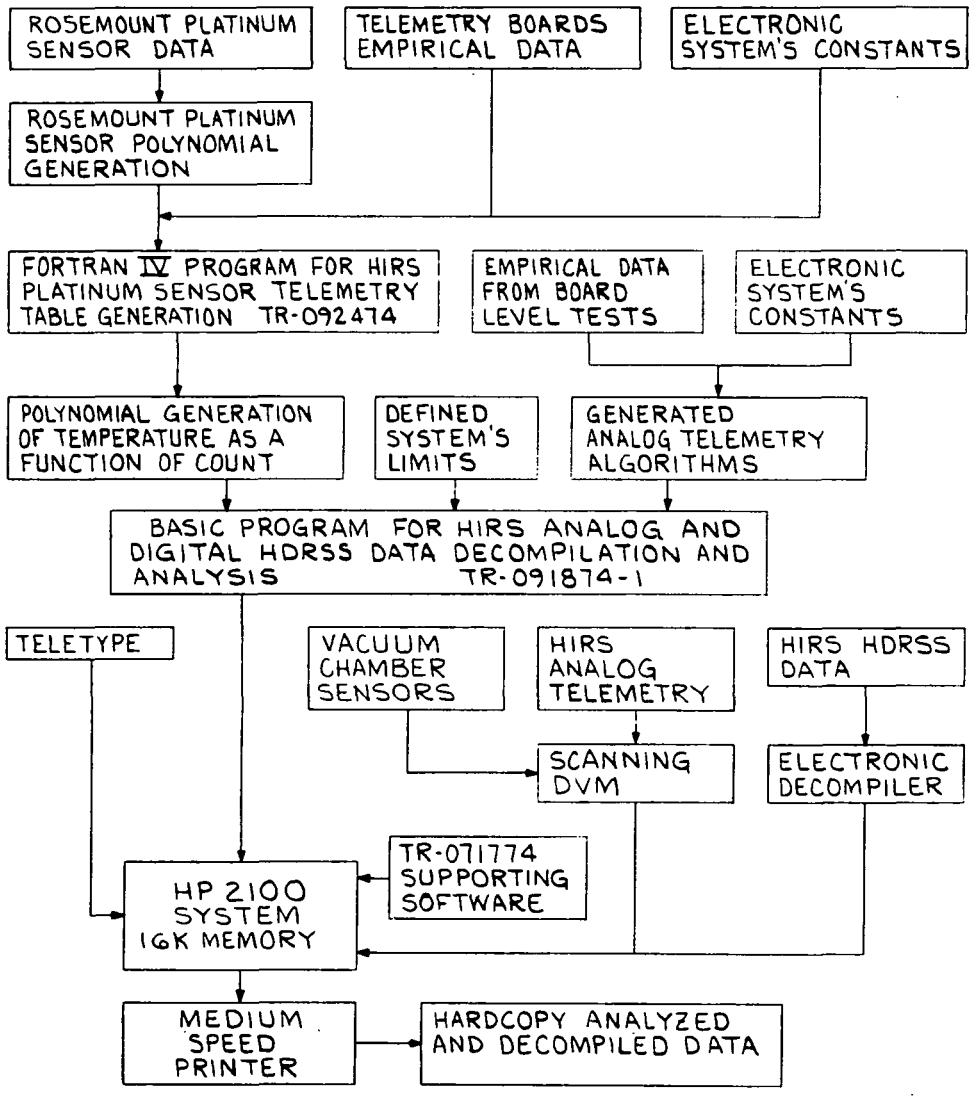


FIGURE 9.8-1 HIRS DATA COLLECTION AND ANALYSIS SYSTEM

Figure 9.8-5, HIRS Data Collection and Analysis System, depicts the relationships of both the software and the hardware needed to meet the objectives of the system. The system discussion will be divided into three parts; the HP2100 system, the Basic Program for HIRS Analog and Digital HDRSS Data Decompilation and Analysis, and the Fortran IV Program for HIRS Platinum Sensor Telemetry Table Generation. In addition, each supporting element will be described.

9.8.5 HP2100 System

The HP2100 system consists of a 16K memory main frame, optical tape reader, teletype punch unit, and a medium speed printer.

The HIRS HDRSS data is converted from Serial Bi-Ø-L data to Serial NRZ data by the electronic decompiler. In order to format the data for the HP2100, the Serial NRZ data is processed to obtain a 16 bit parallel word that contains scan element bits one through sixteen.

Scan line synchronization is accomplished by detecting the scan line sync code located in scan line words 919 and 920. A computer flag is generated at the end of each scan element word with the exception of the first word, scan element sync. The 16 bit parallel words are transferred to the computer if the computer program calls for the data and the operator closes the data switch on the electronic decompiler.

The HIRS analog telemetry is converted to four digit binary decimal numbers by a Hewlett Packard Scanning digital voltmeter. This data occupies scanner channels one through twenty-three. Channel twenty-four monitors the Bench Check Units -24.5 volt power buss. Channels thirty-one to forty are the temperature sensor inputs from the vacuum chamber.

scanner channel and telemetry assignments are as follows:

CHAN	NOMENCLATURE
01	SCAN MIRROR
02	PRI. TEL. MIRROR
03	SEC. TEL. MIRROR
04	F/C HSG. # 1
05	F/C HSG. # 2
06	F/C HSG. # 3
07	F/C HSG. # 4
08	F/C MOTOR TEMP.
09	RADIANT CONE
10	RAD. COOLER HSG.
11	BASEPLATE TEMP
12	ELECTRONICS
13	PATCH TEMP
14	PATCH POWER
15	CONE COVER OPEN
16	+15 VDC ELEC.
17	-15 VDC ELEC.
18	+10 VDC ELEC.
19	+5 VDC ELEC.
20	-24.5 VDC TLM
21	SCAN MOTOR TEMP.
22	F/C MOTOR CUR.
23	SCAN MOTOR CUR.
24	-24.5 VDC BCU
25	INSTRUMENT CUR.
31	EPPLEY TARGET # 0
32	EPPLEY TARGET # 1
33	EPPLEY TARGET # 2
34	EPPLEY TARGET # 3
35	EPPLEY TARGET # 4
36	EPPLEY TARGET # 5
37	WALL TEMP. SP. TGT.
38	BASE TEMP. SP. TGT.
39	SHROUD TEMP.
40	RAD. COOLER TGT.

The number of parallel bits sent to the computer is limited to sixteen bits. Thus the four BCD digits would occupy all sixteen bits. Since the data may be both plus and minus, there is a need for the sign bit to be included. Therefore, the sign was incorporated in the MSD of the BCD most significant unit. This effects the dynamic limits of the analog voltage transformation to ±7.999 volts. This constraint is outside of the systems operating voltage values.

The converted analog voltages are sent to the computer if the computer requests the information and the operator initiates the scan.

The programming for the HP2100 consists of two paper tapes. The first tape is the 16K Basic + Call HIRS configuration tape, TR-071774. It is a binary core image or object tape for the BASIC language and the special BASIC Call routines. The second tape is the BASIC Program for HIRS Analog and digital HDRSS Data Decompilation and Analysis, TR-091874-1. It is a source language tape.

The HP2100 loading procedure is as follows:

I. PRELIMINARY

1. System Power-up

   A. Position 2100A Computer Key Switch to "Power On" position.
   B. Position Teletype Line-Off-Local switch in "Line" position.
   C. Depress Tape Reader Power Switch. Light should be visible.
   D. Depress Printer On/Off and Select buttons.

2. Verify Adequate Supply of paper for TTY and Printer.

II. LOADING PROCEDURE

1. Tape Reader

   A. Depress Load Button.
   B. Place Configuration Tape in Tape Reader with arrows face down.

      Tape TR-071774

   C. DEPRESS READ.

2. 2100A Computer

   A. Depress the following front panel buttons.

a) HALT/CYCLE
b) S
c) CLEAR DISPLAY
d) P
e) CLEAR DISPLAY
f) 13, 12, 11, 10, 9, 8, 7, 6
$(37700)_8$
g) EXTERNAL PRESET
h) INTERNAL PRESET
i) LOADER ENABLE
j) RUN

B. Tape Loads

C. Depress the following front panel buttons.

a) P
b) CLEAR DISPLAY
c) 10, 4, 2, 1, 0
$(2027)_8$
d) INTERRUPT SYSTEM
e) RUN

D. Teletype (TTY) Responds "READY"

E. Remove tape from Optical Reader and rewind.

3. Basic Tape Load Procedure

A. Load Basic Tape #TR-091874-1 in Optical Reader.
B. Depress READ.
C. Type "SCR" followed by return on TTY.
D. TTY responds "READY".
E. Type "PTAPE" followed by return on TTY.
F. Tape Loads.
G. Type "RUN" followed by return on TTY.
H. Program Runs.

NOTE: To change from one Basic Program to another, perform Step #3.

At the start of the program the name and revision of the program is given along with a series of questions related to program format. When all the questions have been answered, the program executes according to the format as defined by the operator's responses to the questions. The computer will request analog and/or HIRS HDRSS data when its program requires it.

The processing status is also displayed on the teletype. An example of the teletype display follows.

```
READY
RUN
HDRSS+TM CONVERT**TR-081874-1
SELECT PROGRAM OPTIONS? 1-YES, 0-NO?1
   1. MEAN & SD?1
      -CHAN SELECT?0
   2. HDRSS TM CONVERT?0
   3. CHAN CAL DATA?0
   4. SCAN SUMMARY?0
   5. ANALOG TM CONVERT?0
   6. CHAN SPAN?11,16
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

INPUT HIRS HDRSS DATA!
DATA PROCESSING
```

9.9 Visible Calibration Target

The calibration target for the visible channel (Channel 17) consists of a 200W quartz-iodine tungsten filament lamp (G.E. Model 6.6A/T4Q/ICL-200-W) mounted in the center of a cylindrical cavity. The walls of the cavity are coated with $BaSO_4$ paint (Eastman white reflectance paint), and the opening is covered with an opal diffuser. The dimensions are approximately 23 cm long by 23 cm in diameter. In Table 9.9-1 the calibration values for the target are given as measured at GSFC. The values given are the spectral radiant emittance for different operating conditions and different wavelengths. At 0.700 microns the percent albedo is also given using 100% = 144 $mw/cm^2 \cdot u$.

Table 9.9-1, Spectral Radiant Emittance
($mW/cm^2 \cdot u$) for Visible Target Operating Conditions

Lamp Current	6.6A	6.0	5.5	5.0	4.5
Voltage	29.7V	25.1	21.4	18.0	14.8
Wavelength					
0.600μ	80.11	47.47	30.66	15.82	--
0.650	100.94	63.94	40.61	23.15	12.50
0.700	118.18	76.84	50.45	30.66	17.02
	(82.58%)	53.36	35.63	21.29	11.82
0.750	129.91	87.41	59.38	36.87	20.92
0.800	139.77	97.13	65.93	42.78	

The HIRS-PM was tested with the visible calibration unit. The output signal ($\overline{X}$) had the following change with albedo (A) change.

$\Delta\overline{X}/\Delta A$ = 12.14 counts/% albedo
$\overline{X}$ (A = 0) = 1.02 counts
RMS Visible Noise = .47 counts
Noise Equivalent Albedo = 0.038% albedo

There is no in-flight calibration target for the visible. It is planned that in-orbit calibration of the visible channel will be done using ground truth measurements.

10.0 SUMMARY OF ACCEPTANCE TEST RESULTS

10.1 General

Complete testing of the Protoflight was accomplished following procedures outlined in the Acceptance Test Plan for the Flight Model HIRS and in accordance with detailed individual test procedures. The test procedures were written using the provisions of GSFC Specification S-653-P-2A, dated July 1970, ITT Proposal 70-1061, dated October 1970.

A definite sequence of tests were planned. Due to anomalies, to be described in this report, that occurred during testing, some of the tests designed for one time use per system, were performed more than once.

The Protoflight unit passed its test series with no significant failures or problems.

Protoflight calibration data obtained during thermal vacuum testing is included in this test section.

Preliminary electrical tests and some thermal vacuum tests were accomplished on the flight unit. The flight unit performed satisfactorily but is not spacecraft flight worthy.

10.2 Test Procedures

The Acceptance Test Plan for the Protoflight HIRS was submitted in October 1973 and the Acceptance Test Plan for the Flight HIRS was submitted in June 1974. Between the time the protoflight and flight test plans were submitted, the units were modified by removing radiation balance circuitry in the pre-amplifier, and original test procedures were modified. Therefore, the test plan written for the flight unit better defines tests performed and criteria for acceptance on both protoflight and flight units.

Each test plan was followed up by a submission of detailed test procedures. Each procedure was written either to test a specific subassembly or for a specific environmental test of the complete instrument.

Following is a list of test documents and purpose of each used in instrument testing.

ITT-A/OD Document Number 433076 dated October 1, 1973

Acceptance Test Plan for the Protoflight High Resolution Infrared Radiation Sounder (HIRS)

Purpose: This document presents a test plan used for qualification of the High Resolution Infrared Radiation Sounder (HIRS) experiment, Protoflight Model, under the requirements of GSFC Specification S-653-P-2A and other applicable documents.

This plan acknowledges the specified requirements and presents a plan responsive to these requirements. The plan defines detailed test requirements, test criteria, and general test methods. This plan became the basis for preparation of detailed test procedures.

IRR-A/OD Document Number 433083 dated June 18, 1974

Acceptance Test Plan for the Flight Model High Resolution Infrared Radiation Sounder (HIRS) for Nimbus F
Purpose: Same as stated above for Protoflight

Test Procedure 8120617 - "Preliminary Electrical Tests for HIRS"

Purpose: These tests verified Bench Check Equipment (BCE) to HIRS interface. The BCE parameters were measured to verify similarity with those expected from the Spacecraft. The HIRS I/O parameters were measured to verify proper operation and specified loading will be presented to the spacecraft.

All HIRS commands and nodes were exercised.

The HIRS was subjected to worst case electrical conditions to prove specified operational limits.

Test Procedure 8120618 - "Complete (Ambient and Bench Cooler) Baseline Tests"

Purpose: This procedure describes tests that were performed to determine the status of the HIRS at specific times during acceptance testing. These tests were performed before, during and/or after any major mechanical alteration, shipment to and from a location, or environmental testing.

Test Procedure 8120619 - "Optical System Tests"

Purpose: This document details the methods, equipment and parameters required to fully measure the optical system performance according to the specification.

Similar tests were previously performed on the optics prior to delivery. These tests were performed on the assembled instrument to verify instantaneous field of view, channel registration and energy profile.

Test Procedure 8120620 -"Thermal Vacuum (T/V) Testing of the HIRS"

Purpose: These tests established the operational limits of the HIRS during simulated flight conditions over the specified temperature range. During these tests, temperature cycling, long term exposure to temperature extremes and final calibration of each IR channel was completed on the instrument.

Specification Deviation: Figure 10.2-1 shows the thermal vacuum cycle specified in GSFC Specification S-320-EN-1 dated November 1971, Environmental Test Specification for the ERTS (A and B) and Nimbus (E and F) Observatory Systems, Subsystems and Experiments.

Due to the complexity of the IR Calibration cycle, ITT proposed the cycle shown in Figure 10.2-2. The actual approved cycle performed on the Protoflight is shown in Figure 10.2-3.

Test Procedure 8120621 - "Pre-Acceptance Bench Cooler Tests of the HIRS Instrument"

Purpose: This procedure describes tests that were performed to determine the status of the HIRS after initial assembly completion.

Test Procedure 8120622 - "RFI Testing of the HIRS"

Purpose: This procedure describes in detail the test sequence performed for evaluation of the instrument during specified frequency radiation from an external source.

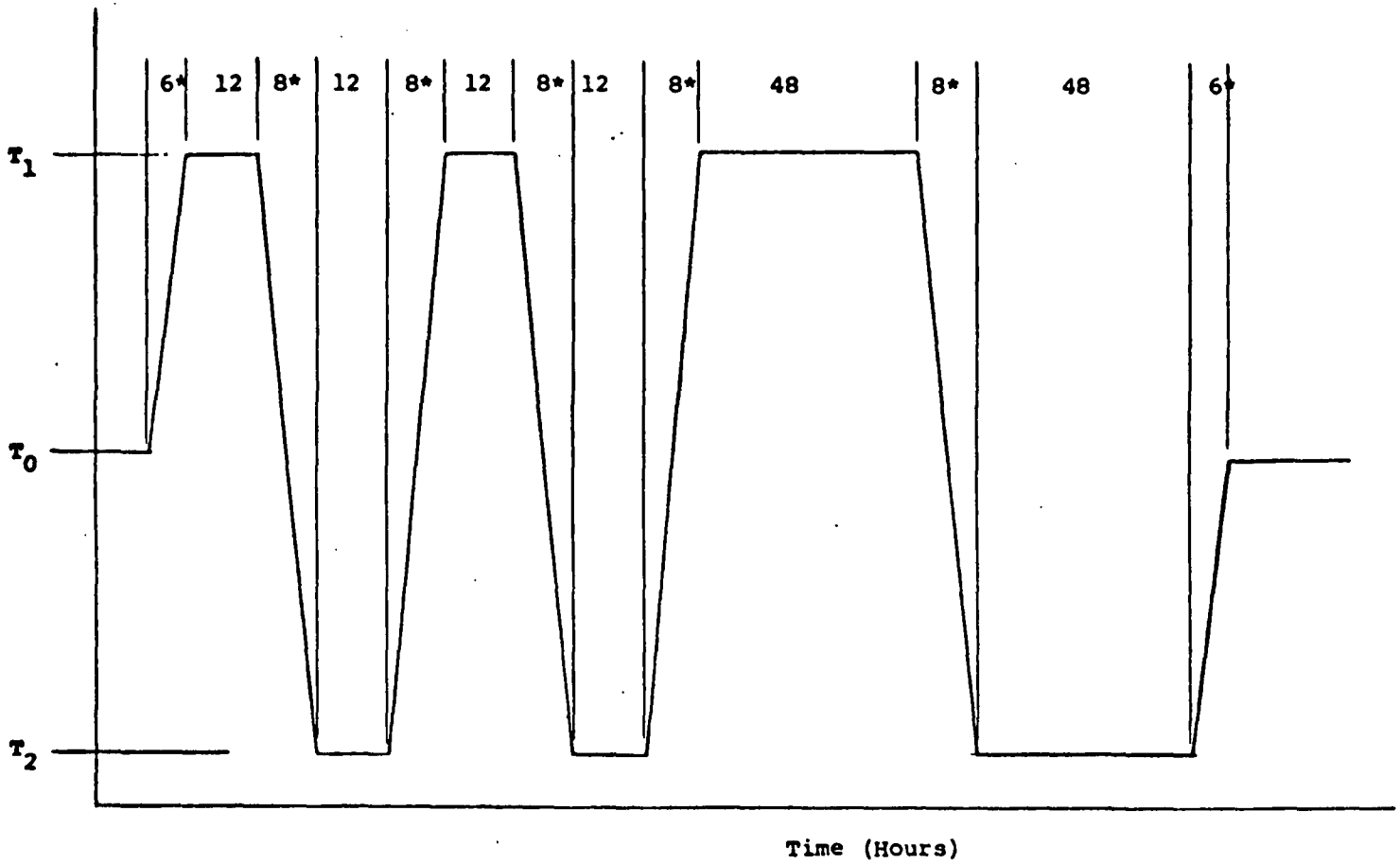
Deviation: The frequencies used for RFI were specified in Document Number X-450-68-415, "Numbus E and F Experiment Interface Requirements", and are as follows:

136.5 MHz	0.5 W
1702.5 MHz	1.0 W
1707.5 MHz	1.0 W
2253.0 MHz	1.0 W

The 1707.5 MHz frequency was omitted at the request of GSFC. None of the frequencies were to be modulated.

During actual testing, at the request of GSFC, the 136.5 MHz was 30 percent modulated with 400 Hz and 1000 Hz and the 2253 MHz was 100 percent modulated with a 1000 Hz square wave.

Initial testing was performed with the instrument located in a screen room. Final testing was conducted with the instrument



	Prototype	Flight
T_1	45°C	40°C
T_0	≈ 25°C	≈25°C
T_2	-5°C	0°C

*Transition times shall be accomplished in no greater than 8 and no less than 4 hours. The rate of change shall be based on the temperature extremes as specified.

FIGURE 10.2-1 SENSORY RING SUBSYSTEMS, THERMAL-VACUUM CYCLE

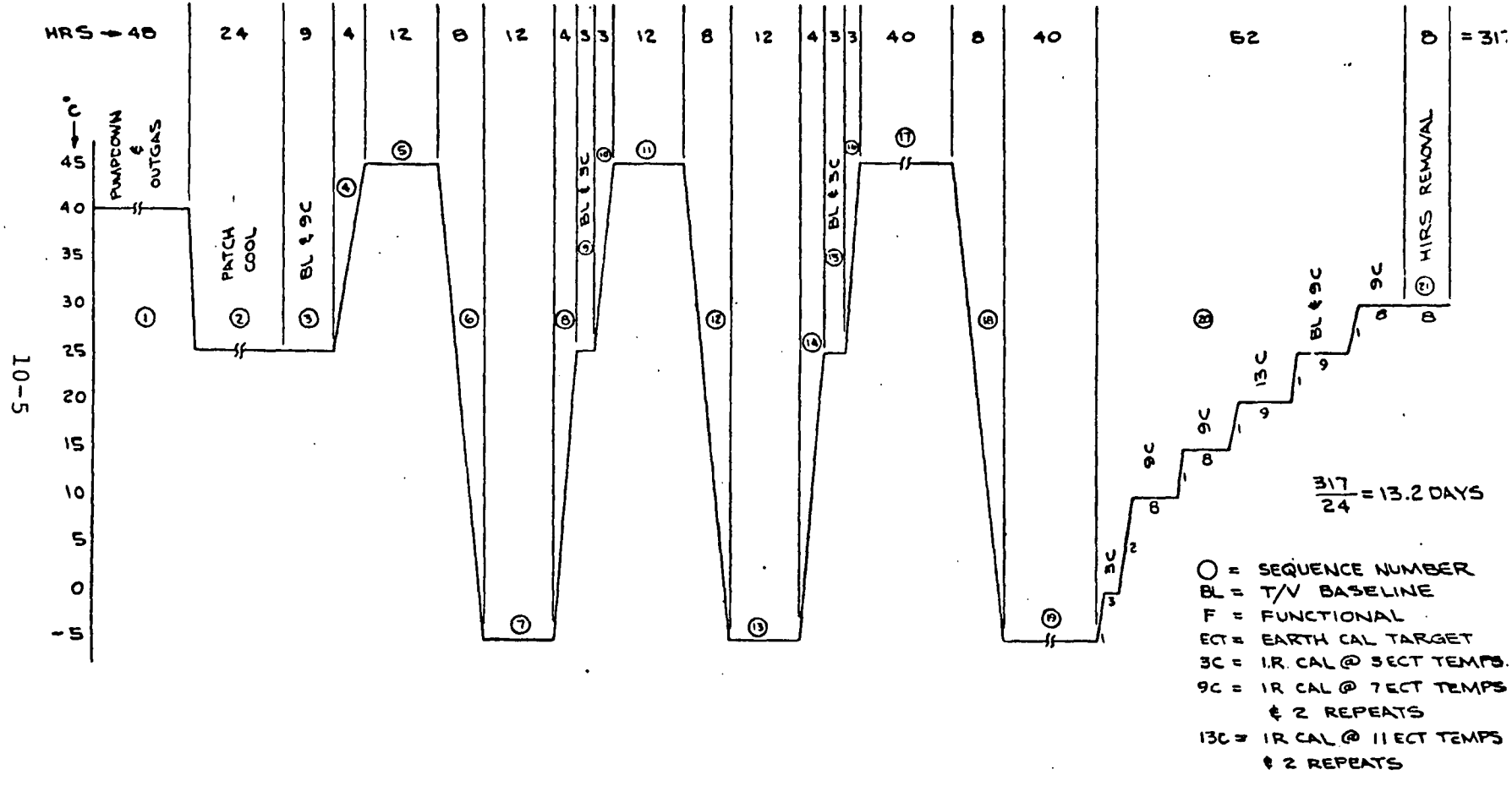
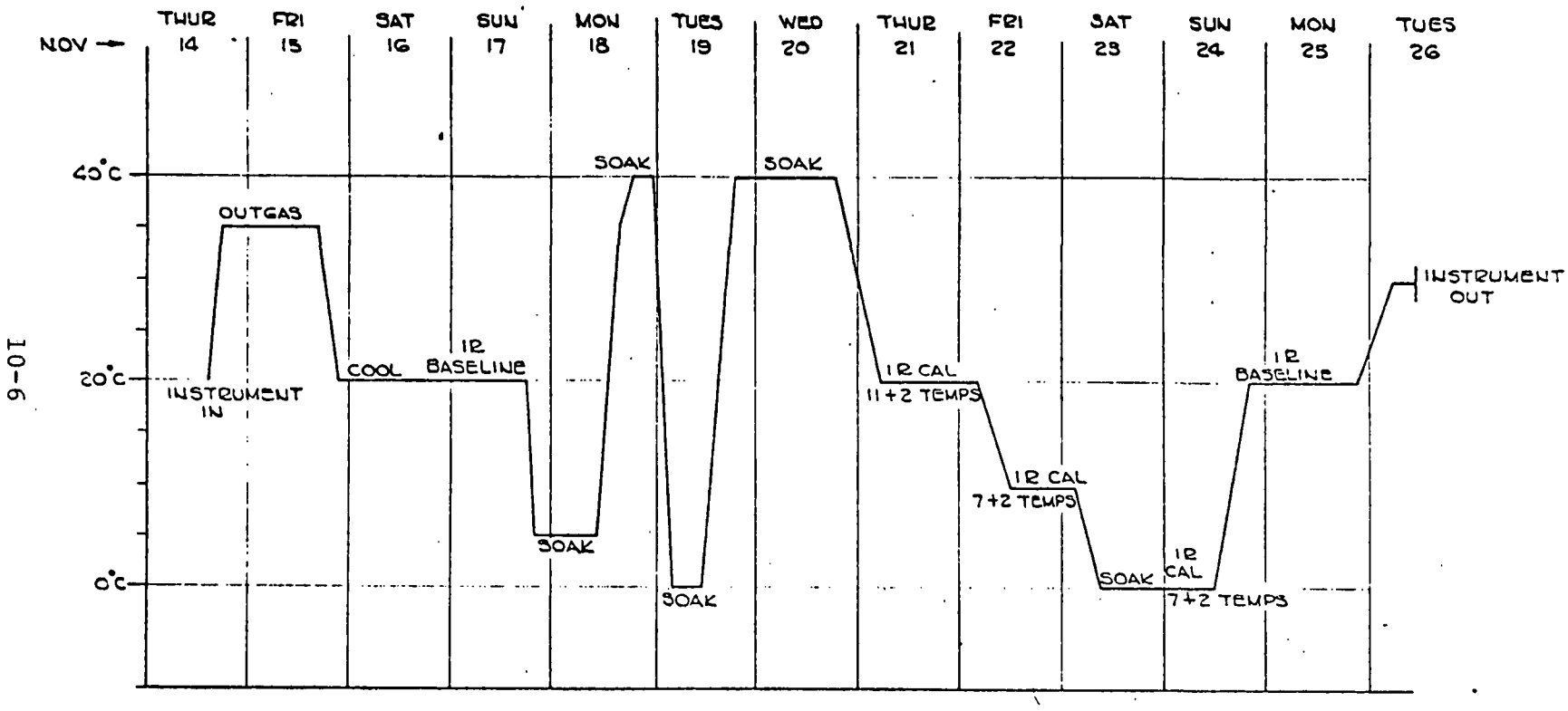


FIGURE 10.2-2 HIRS THERMAL-VACUUM (T/V) CYCLE FOR PROTOFLIGHT



10-6

FIGURE 10.2-3 HIRS PROTOFLIGHT POST VIBRATION THERMAL VACUUM TEST (FINAL IR CALIBRATION)

in an open area to reduce RFI reflections. The final test frequency was 136.5 MHz 30 percent modulated with 4000 Hz to present to the instrument a more realistic RFI environment introduced by the spacecraft transmitters.

Test Procedure 8120623 - "HIRS Vibration Testing"

Purpose: This document describes the procedures followed during vibration testing of the HIRS.

The HIRS Protoflight has been through vibration at GSFC three times. The first vibration was at specification levels. The second vibration was at lower levels for workmanship checks. The third vibration was X axis only at 3.3G, from 200 to 2000 Hz, for one minute.

The Flight Model has had no vibration tests.

Deviation: Tables 10.2-1 and 10.2-2 lists the vibration levels recommended by GSFC Environmental Specification S-320-EN-1, November 1971. The protoflight levels were to be applied at twice the specified sweep rate for sine and one half the duration specified for the random exposure. As a result of a review of the Mass Test Model vibration test by GSFC we were directed to use the levels shown in Tables 10.2-3 and 10.2-4. For the first vibration test, the sine levels shown in Table 10.2-5 were the ones used as directed by GSFC. During the first vibration test the Patch and Cone assemblies were damaged. Therefore, after repair, a second workmanship vibration was performed with the approved levels shown in Table 10.2-6 and Table 10.2-4 for random flight. Test durations were changed to 4 octaves/min on sine and 1 minute duration for random.

Test Procedure 8120624 - "HIRS Weight and C.G."

Purpose: Outlines procedure used in the measurement and recording of instrument weight and center of gravity.

Test Procedure 8120625 - "HIRS System Scan Mirror Tests"

Purpose: Describes procedure used to test the Mirror Scan system at the system level.

Test Procedure 8120626 - "Visible Calibration (HIRS)"

Purpose: This document defines the equipment and procedures used during the calibration of the HIRS visible channel #17.

TABLE 10.2-1 SPECIFIED PROTOFLIGHT VIBRATION LEVEL, SINUSOIDAL

Frequency Range (Hz)	Amplitude - "g" 0-to-Peak	
	Thrust	Transverse
5-23	8.0*	-
23-60	6.0	-
60-150	10.0	-
150-2000	5.0	-
5-200	-	6.0*
200-2000	-	5.0

*Exposure limited to 0.5" double amplitude.
Sweep Rate: 1 octave/minute

TABLE 10.2-2 SPECIFIED PROTOFLIGHT VIBRATION LEVEL, RANDOM

Frequency Range (hz)	Power Spectral Density (g^2/Hz)	g-RMS	Duration
20-2000	0.09	13.4	4 min/axis

These levels apply to all three axes.

TABLE 10.2-3 MODIFIED PROTOFLIGHT VIBRATION LEVELS, SINUSOIDAL

Frequency Range (Hz)	Amplitude - "g" 0-to-Peak			
	Proto-Flight Qualification		Flight Acceptance	
	Thrust	Transverse	Thrust	Transverse
5-25	7.0*	-	4.7	-
25-200	6.0	-	4.0	-
200-2000	5.0	-	3.3	-
5-200	-	3.0*	-	2.0*
200-2000	-	5.0	-	3.3

*Exposure limited to 0.5" double amplitude.
Sweep Rate: 2 octaves/minute

TABLE 10.2-4 MODIFIED VIBRATION LEVELS, RANDOM

	Frequency Range (Hz)	Power Spectral Density (g^2/Hz)	g-RMS	Duration
Proto Flight Qualification	20-2000	0.09	13.4	2 min/axis
Flight Acceptance	20-2000	0.04	8.9	2 min/axis

TABLE 10.2-5
FINAL VIBRATION TEST LEVELS, PROTOFLIGHT, SINUSOIDAL

Frequency Range (Hz)	Amplitude - "g" 0-to-peak		
	Proto-Flight Qualification		
	Thrust (Z axis)	Transverse	
		X axis	Y axis
5-25	7.0*		-
25-200	6.0		-
200-400	3.3		
400-2000	5.0		-
5-200	-	3.0*	
200-350	-	5.0	
350-500	-	3.3	
500-2000	-	5.0	
5-200	-	-	3.0*
200-475	-	-	3.3
475-2000	-	-	5.0

*Exposure limited to 0.5" double amplitude
Sweep Rate: 2 octaves/minute

TABLE 10.2-6 WORKMANSHIP PROTOFLIGHT VIBRATION TEST LEVELS

CORRECTED SINE VIBRATION LEVELS
HIRS - PROTOFLIGHT TEST 11/12/74

X-AXIS		Y-AXIS		+ Z-AXIS	
FREQUENCY (Hz)	AMPLITUDE "g" 0-to-Pk	FREQ (Hz)	AMPLITUDE "g" 0-to-Pk	FREQ (Hz)	AMPLITUDE "g" 0-to-Pk
5-8	.33 in.*	5-8	.33 in.*	5-9	.33 in.*
8-14	1.1	8-12	1.1	9-15	1.4
14-24	.8	12-18	.9	15-21	4.6
24-34	.04 in.*	18-26	.05 in.*	21-36	1.7
34-46	1.1	26-32	1.7	36-50	.035 in.*
46-56	1.3	32-46	1.1	50-56	3.1
56-70	.9	46-54	1.1	56-80	2.1
70-80	2.0	54-64	1.1	80-120	3.3
80-100	.9	64-76	1.7	120-200	1.7
100-200	.8	76-86	1.1	200-400	3.3
200-350	3.3	86-98	1.6	400-2000	3.3
350-500	3.3	98-200	1.1		
500-2000	3.3	200-2000	3.3		

*EXPOSURE LIMITED TO DISPLACEMENT IN INCHES DOUBLE AMPLITUDE

Test Procedure 8120627 - "Pre-Vibration Thermal Vacuum (T/V) Baseline Test of HIRS"

Purpose: These tests were used to determine the limits of the IR detectors and associated amplifier channels and to verify that each channel gain is properly set.

These tests confirmed the effectiveness of the HIRS Cooler in a simulated sun loading environment.

The IR tests conducted were used as a baseline to compare with identical tests performed after vibration.

10.3 Optical Test Results

10.3.1 Alignment Method and Results

In June 1974 the alignment of the HIRS-PM unit was completed and found to be satisfactory. Because the detectors were destroyed during vibration the alignment procedure had to be done with the new detectors. In the past the cooler was positioned for alignment of the SW and visible, then the LW field stop was moved to align the LW with the SW and visible. During this alignment it was found that the LW field stop (FS) had to be moved so far that the LW field of view (FOV) was reduced. In order to minimize the LW-FS movement the alignment procedure was changed somewhat. First, the aperture in front of the visible detector was repositioned to align it with the SW then the LW-FS was moved. Again, the LW-FOV reduced when LW alignment was attempted.

A check of the position of the center of the LW and SW beams as they enter the cooler showed that they were not properly aligned. The beam separation was found to be about 1.650 inches instead of 1.700 inches. At the time it was thought that this may be the cause of the alignment problem. After repositioning several folding mirrors the beams were correctly positioned. This did not help the alignment problem. Finally, it was decided to align the system for maximum FOV and sacrifice some alignment. The results of the alignment are shown in Figure 10.3-1. The largest misalignment between LW-SW represents about 5% of the effective FOV.

10.3.2 Field of View Test Results

The measured FOV as described above are shown in Figure 10.3-1. These are the calculated effective field of views.

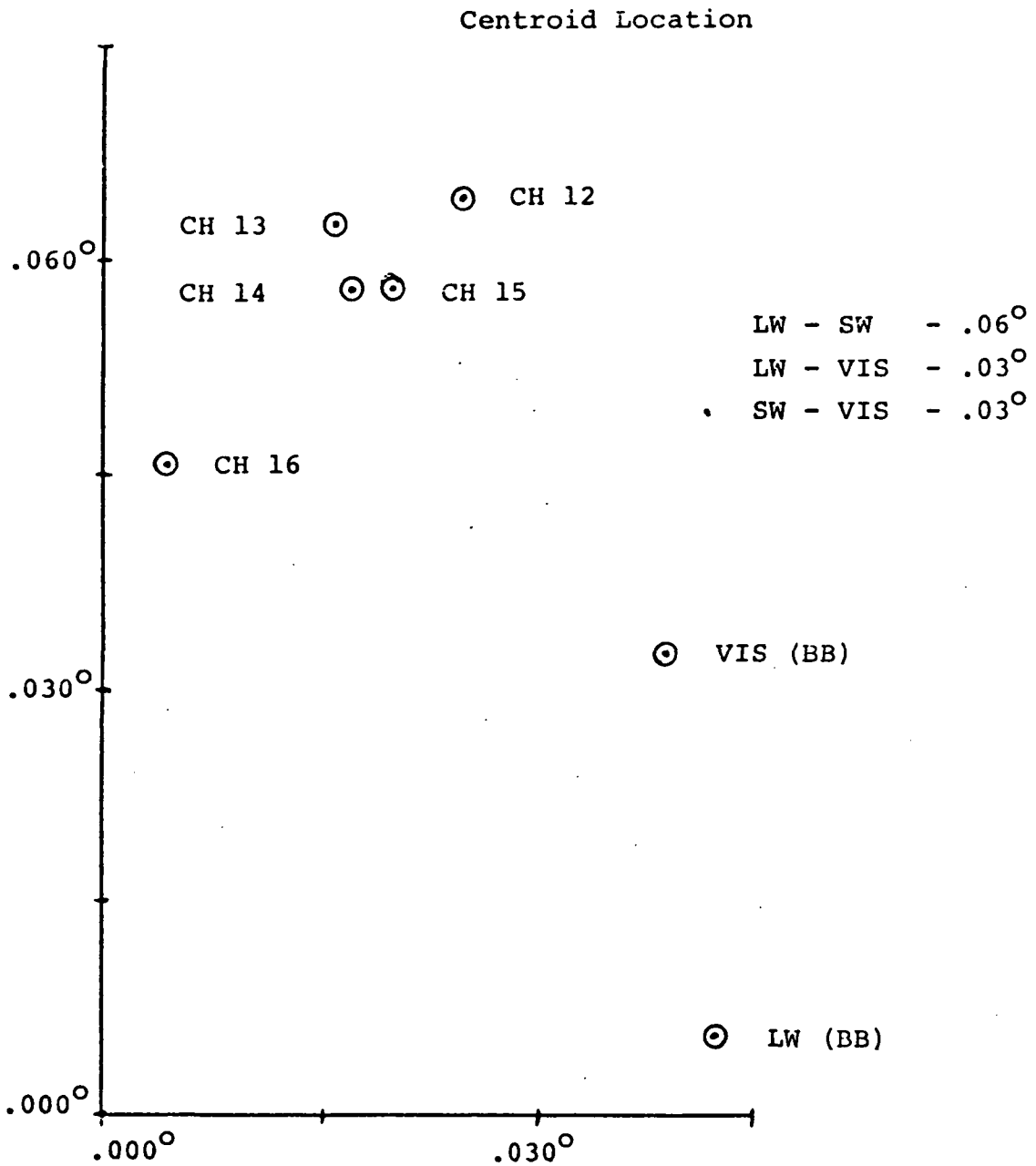


FIGURE 10.3-1 OPTICS FIELD OF VIEW

FIELD OF VIEW			
LW (BB)	1.17°	CH 15	1.24
CH 12	1.24	CH 16	1.25
CH 13	1.22	VIS (BB)	1.28
CH 14	1.24		

Test Procedure 8120619A, Completed 10-25-74

10.4 System Functional Tests

All functional tests have been completed. The Preliminary Electrical Tests (Test Procedure 8120620) were accomplished. Parts of these tests were repeated each time the instrument was reassembled.

10.4.1 Power Profile

Following are the finalized Profile Charts (Table 10.4-1) and Power Usage Table (Table 10.4-2).

10.4.2 Transients

The significant transients existing on the signal and power busses within the instrument are listed below.

One of the transients is listed as being out of specification and the remaining are noted either to be a matter of record or to be an assistance during data reduction.

10.4.2.1 Analog Telemetry (TM)

	Signal Peak-to-Peak	ATM Variation
1. F/C Motor Temp TM	80 Millivolts (noise spikes)	1°C
2. F/C Motor Current TM	1 volt (Sawtooth)	198 MA
3. Scan Motor Current TM	0.2 volt (Sawtooth)	80 MA

The F/C Motor Temp TMV transient is 60 millivolts over specification limit.

The F/C Motor Current TMV contains the a-c component listed above superimposed on a nominal d-c level. The a-c component is normal and is the result of the current switching into the stepping motor.

The Scan Motor Current TMV contains the normal a-c component listed above during normal scan only. The a-c component is the result of current switching of the stepping motor.

The TMV limits for data reduction should be set to include the F/C and Scan Motor variations noted above.

10.4.2.2 -24.5 Volt Power Buss Current Transients at Command Execution

As a matter of record, listed below are current transients greater than one ampere, existing as a result of a specific command execution.

TABLE 10.4-1 POWER PROFILE CHART

Current in Milliamps

	+15 VDC	-15 VDC	+5 VDC	+10 VDC	TM	-24.5		
						Norm	Min	Max
Analog Data Channels	25	25						
A/D Converter	58	53						
Clock				2				
Chopper Pickups			30					
Logic			55	15				
Telemetry	16	16			6			
F/C Housing						50		
F/C Motor						258		422
Scan Motor						365 (Avg)	240*	1680**
Total Current	99	94	85	17	6	673		
Sub Total Power(Watts)	1.485	1.41	.425	.17	.147	16.488		
Power X Reg Eff (Watts)	75%	75%	75%	75%	.147	No Reg 16.488		
Power X Conv. Eff (Watts)	70% 2.83	70% 2.69	70% .81	70% .324	.147	No Reg 16.488		

Total Power = 23.30 Watts
(Nominal)

* During step scan (43/46 of the time)
** During slew (4/46 of the time)

TABLE 10.4-2 POWER USAGE

Operating Modes	Source	Power	(Watts)
Min. Sat.	None	0	
Standby	Filter Wheel Htr.	1.23	7.88
	Electronics	6.65	
Launch	F/C Motor	6.32	12.94
	Scan Motor	6.62	
Preconditioning	F/C Motor	6.32	35.9
	Scan Motor	8.94	
	Electronics	6.65	
	Cooler Cone Htr.	2.77	
	Filter Wheel Htr.	1.23	
	Cooler Hsg. Htr.	10.0	
Operation	F/C Motor	6.32	23.1
	Scan Motor	8.94	
	Electronics	6.65	
	Filter Wheel Htr.	1.23	
All	Full Time Telemetry	.14*	

*Add to above for total system power.

All transients listed are within the limit set by system specification.

Command Executed	Transient (P-P) (Amps)
F/C Housing Heat ON	2
F/C Motor ON	2.3
Electronics ON	1.2
Scan Motor ON	2.1

10.4.3 Scan System Test

Requirements and results of Mirror Scan System tests are listed below.

Requirements:

Drive 6" scan mirror to 42 successive steps of 1.8^{o}, repeat 20 times, then drive to each of 3 calibration positions and to start of scan.

Timing:

Step to $1.8^{o} \pm .05^{o}$ in 32 milliseconds (MS). Reach final position ± 1% in 45 ms. Dwell at each step 74 ms. Retrace 76^{o} in 425 ms. Slew 90^{o} in 425 ms to each calibration point. Repeat continuously.

System Characteristics:

Step Position	1.8^{o}
Step Settling Time	40 ms
Slew Time	350 ms typical
Power, Step Period	8 watts
Slew	44 watts
Average	8.9 watts

Deviations from Spec:

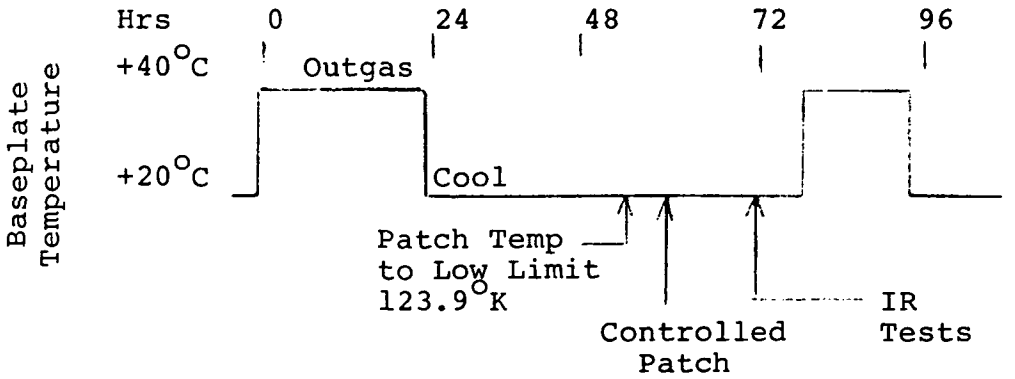
Start of scan (SEBO) is typically $+.18^{o}$ from nominal. All other scan positions on nominal.

10.5 Pre-Vibration Thermal Vacuum Test

To be assured that the integrity of the system would not be affected by full vibration testing, the HIRS was subjected to a Thermal Vacuum test. This T/V test was to be used as a baseline of system performance to be compared with similar T/V tests to be performed after vibration testing.

10.5.1 Test Sequence

The tests were performed on November 4 through November 9. The temperature cycle and major milestones are shown below.



10.5.2 Test Results

Final Temps with Simulated Sun Loads at Normal Power

Baseplate	-	+20°C
Cooler Housing	-	276°K
Cone	-	168.6°K
Patch	-	123.9°K
Patch Power	-	0.16 μW

Normal Sun Load Power

Cone	-	0.413W
Cooler Housing	-	7.3W
Cooler Door	-	8.79W

L.W. Detector Bias - 11.2 MA

IR Tests Conducted at three Earth Calibration Target (ECT) Temps.

222°K
278°K
322°K

NOTE: For this test, Patch Control Temp. was 122.8°. After test, control point was changed to 124.0°.

10.6 Vibration Test

A full three axis vibration test was performed at GSFC on November 12 using ITT-A/OD Test Procedure No. 8120623.

Due to the Encoder position anomaly that occurred during this vibration test, the instrument was again vibration tested on December 12 in the X axis only.

10.6.1 Test Sequence

Date: December 12

Sinusoidal and then Random Vibration performed in each axis.

Vibration Axes - X, Y and X (in this order)
Vibration Levels - Reversed Flight Levels

Date: December 12

Sinusoidal vibration in one axis

Vibration Axis: X only
Vibration Levels: 200-2000 @ 3.3G

10.6.2 Test Results

Before and after each axis of vibration a functional test was performed. This also included visible channel checks. No anomalies were noted immediately after any of the vibration tests.

10.6.3 Encoder Failure Review

Anomaly: Scan System Encoder Position data erratic (2^3 bit)

This anomaly was first discovered at the start of Post Vibration Thermal vacuum test and was noted on the Brush recorder. At this time, the instrument was in the worst case position to cause the problem to occur on every scan line.

Study of past history of the instrument functional operation uncovered the fact that the encoder anomaly first occurred after the X axis sine vibration test on November 12. The instrument was vibrated again in the X axis on December 12 to prove the integrity of the encoder on the remaining encoder position tracks.

After the vibration test, the 2^3 bit encoder track operation continued to be erratic. There were no additional malfunctions to the remaining encoder tracks.

10.7 Vacuum Chamber Tests

At completion of the three axes vibration tests, the instrument was subjected to the final Thermal Vacuum testing.

10.7.1 Test Sequence

The testing started on November 14 and ended on November 26 using ITT-A/OD Test Procedure No. 8120620, "Thermal Vacuum Testing of the HIRS." An extra cycle of warm and cold temperature exposure was added to compensate for the likelihood that this protoflight may not be subjected to soak tests at G.E.

Figure 10.2-2 and 10.2-3 show the proposed and modified general test plans, while Figure 10.7-1 is a detailed plot of the baseplate and radiant cooler housing temperatures throughout the test period.

10.7.2 Test Results, General

Final Temps with Simulated Sun Loads at Normal Power

Baseplate	-	$+20^{o}C$
Cooler Housing	-	$282^{o}K$
Cone	-	$170.2^{o}K$
Patch	-	$124.7^{o}K$

With Cooler Hsg. Heater power reduced 50% on normal Sun load conditions.

Baseplate	-	$+20^{o}C$
Cooler Housing	-	$276^{o}K$
Cone	-	$167.8^{o}K$
Patch	-	$123.9^{o}K$ (Controlled)
Long Wave Detector Bias	-	11.2 MA

Anomalies:

1. Encoder Position data erratic: 2^{3} bit of encoder erratic. Problem was noted shortly after reaching vacuum. F/C in sync. Permission was granted to continue T/V testing. This condition does not affect flight operation.

2. Scan System reinitializing improperly. Problem occurred at last $0^{o}C$ Baseplate Temperature Soak. The cause and solution of this problem is given in Section 10.9.

3. Loss of Sync occurred at a 2 per hour rate throughout the complete T/V test.

10.7.3 System Sensitivity

10.7.3.1 Time and Temperature Effects

The major effect of time on the unit was a degradation of the system response and is discussed in Section 10.12.2. A

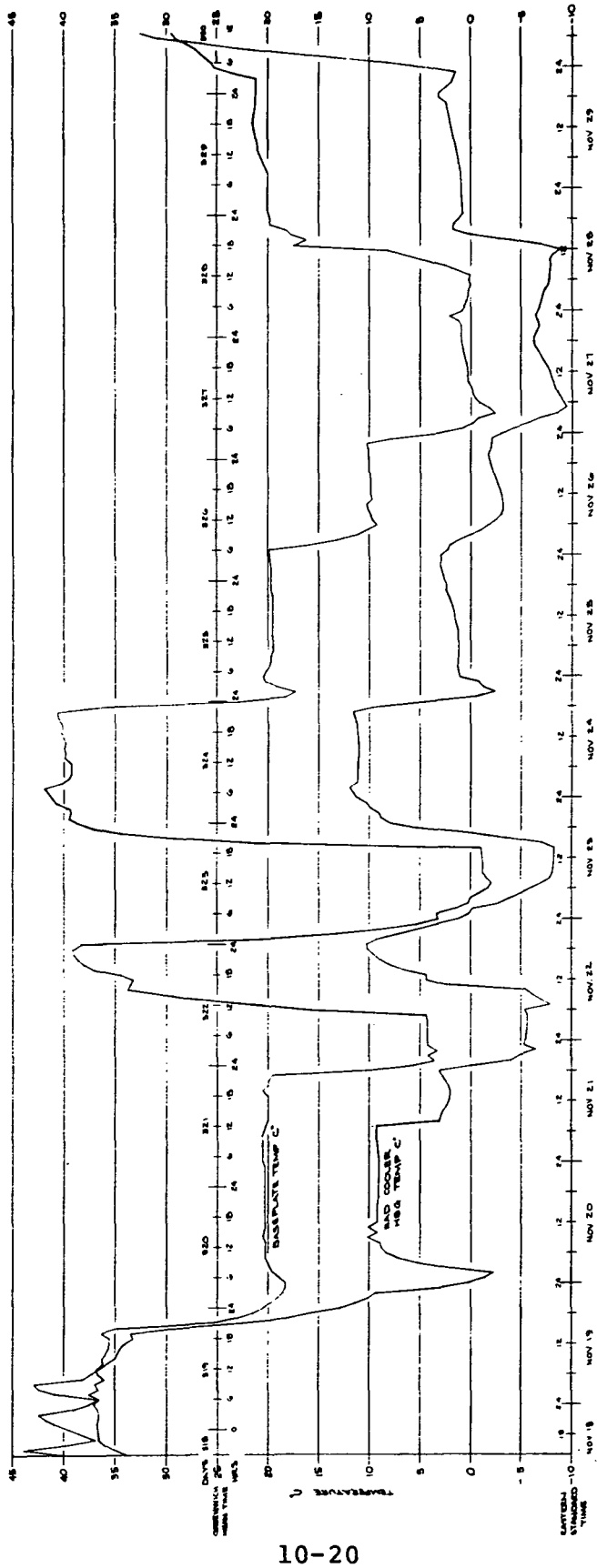


FIGURE 10.7-1 HIRS PROTOFLIGHT T/V TEMP CYCLES

check of the electronic calibration output showed no change over the time period of the T/V test. The standard deviation as shown in Table 10.7-1 shows no significant change during the test.

There is one major effect that occurred because of baseplate temperature changes. This effect assumes constant temperature for the detectors. The change in baseplate temperature has the effect of changing the background radiation that the detectors see. In the longwave the major effect is an increase response with cooler temperatures as can be seen in Table 10.7-2. The increase in responsivity mainly occurs because of an increase in resistance of the detector. The effect can also be seen in Table 10.7-3 which shows the space output for different baseplate temperatures.

10.7.3.2 NEΔN Performance

The sensitivity of the HIRS-PM unit was measured during the T/V test and is shown in Table 10.7-4. There are three modes of operation in which the unit is expected to operate. One is to have the patch regulated at 124^{o}K which would provide complete global coverage by the instrument. Another is to have the patch unregulated running at about 122^{o}K and also provide global coverage. This would produce NEΔN's for the longwave channels slightly lower than those shown for 124^{o}K. The last method which is expected to be used at the beginning of HIRS satellite operation is to operate during approximately 17% of the orbit and unregulated at about 118^{o}K or lower. The lower temperatures are much more advantageous since the longwave sensitivity increases with lower temperature.

10.7.3.3 Linearity

A preliminary check of the linearity was done by Dr. William Smith, NOAA, during the T/V test. These results showed that the HIRS-PM had a satisfactory linearity. All of the data from the T/V test will be checked in the future by NOAA. There was some problem with the ECT matching the IWT, ICT and SCT during the test, this is discussed in Section 10.12.3.

10.8 Visible Calibration

10.8.1 Test Method

To calibrate the HIRS-PM unit for Channel 17 (0.700μ) the Visible Calibration Target Assembly (VCTA) was used. The test was performed according to test procedure TP-8120626 in the laboratory with the room lights off. HIRS-PM was in its cradle with the scan mirror in nadir position and the VCTA above

TABLE 10.7-1 PROTOFLIGHT ACCEPTANCE TEST DATA SUMMARY

THERMAL VACUUM TEST STANDARD DEVIATION SUMMARY

CH	20°C Baseline	5°C Soak	40° Soak	0° Soak	40° Soak	20° Cal	10° Cal	0° Cal	20° Cal
1	4.8	6.0	6.4	7.0	5.6	5.0	5.2	8.2	4.5
2	4.8	3.1	2.7	3.3	2.9	2.7	3.0	4.2	2.7
3	3.8	3.5	3.9	5.8	3.6	3.4	3.7	3.7	3.0
4	3.8	3.2	3.5	3.7	3.4	3.4	3.5	3.7	3.3
5	4.7	3.3	4.0	4.4	3.7	4.2	3.6	2.8	3.1
6	3.35	3.4	4.0	3.6	3.2	3.3	3.3	5.3	3.4
7	3.3	3.7	4.6	3.9	4.1	4.7	3.8	3.5	2.9
8	2.7	2.4	2.7	3.8	2.1	2.5	2.6	4.0	1.9
9	2.3	2.2	2.0	3.2	3.2	2.4	2.55	3.0	3.2
10	3.35	3.6	2.9	4.2	2.5	2.5	2.4	6.8	3.0
11	5.6	5.8	3.7	4.2	3.6	4.0	3.9	3.5	3.7
12	1.5	1.4	2.3	1.7	2.4	1.4	1.5	1.5	2.0
13	2.65	3.0	2.1	2.8	2.3	2.2	2.5	2.1	2.1
14	1.5	1.3	1.9	1.3	2.2	1.45	1.3	1.3	1.3
15	1.7	1.6	2.0	1.8	2.0	1.7	1.7	1.8	1.7
16	1.6	2.8	1.5	1.7	1.6	1.3	2.0	2.1	1.1
17									
ECT	-51C	-51C	-51C	-51C	-51C	-51C	-51C	-51C	-51C
SCT	88K	94K	82K	82K	84K	86K	86K	84K	88K
ICT	254.3	243.9	266.8	240.1	267.1	254.3	247.9	240.9	255.1
IWT	291.0	275.0	310.7	268.9	310.0	291.3	281.3	271.3	292.5
No. Samples	504	504	504	504	504	504	504	504	504

TABLE 10.7-2 PROTOFLIGHT ACCEPTANCE TEST DATA SUMMARY

THERMAL VACUUM TEST RADIANT RESPONSE (COUNTS/w$\cdot$cm^2 $\cdot$ sr^1 $\cdot$ cm)

CH	20°C Baseline	5° Soak	40° Soak	0° Soak	40° Soak	20° Cal	10° Cal	0° Cal	20° Baseline	Exponent
1	8.429	8.945	7.651	9.267	6.291	8.056	9.029	8.867	8.272	+6
2	2.748	2.986	2.519	3.010	2.081	2.767	2.877	2.965	2.740	+7
3	4.420	4.748	4.086	4.800	3.370	4.407	4.572	4.706	4.343	+7
4	7.432	7.971	6.827	7.935	5.693	7.167	7.370	7.608	7.028	+7
5	4.613	4.957	4.300	4.938	3.592	4.407	4.570	4.709	4.374	+7
6	7.435	7.975	6.879	7.921	5.861	7.163	7.338	7.500	6.987	+7
7	7.832	8.413	7.179	8.329	6.124	7.400	7.533	7.682	7.173	+7
8	7.974	8.400	7.272	8.205	6.201	7.103	7.183	7.339	6.758	+7
9	8.758	9.375	8.329	9.371	7.367	8.743	8.945	9.178	8.719	+7
10	1.773	1.893	1.662	1.871	1.435	1.633	1.663	1.700	1.606	+8
11	4.251	4.295	4.016	4.216	3.801	3.804	3.811	3.836	3.764	+9
12	5.048	5.202	4.839	5.178	4.575	4.602	4.612	4.648	4.556	+9
13	4.436	4.558	4.248	4.555	4.011	4.058	4.061	4.090	3.876	+9
14	7.100	7.329	6.745	7.318	6.375	6.530	6.556	6.610	6.471	+9
15	5.933	6.101	5.740	6.121	5.478	5.535	5.549	5.574	5.548	+9
16	1.346	1.387	1.064	1.405	.670	1.223	1.226	1.239	1.292	+10
Patch	124.02	123.85	124.14	123.94	125.60	123.99	123.86	123.83	123.98	
F/C	303.9	303.7	313.9	303.7	317.3	304.9	303.7	303.7	30.9	

TABLE 10.7-3 PROTOFLIGHT ACCEPTANCE TEST DATA SUMMARY

THERMAL VACUUM TEST SYSTEM OUTPUT (COUNTS) VIEWING SPACE TARGET

Base Temp. / Test	20° Baseline	5° Soak	40° Soak	0° Soak	40° Soak	20° Cal	10° Cal	0° Cal	20° Cal
Ch 1	84.3	113.0	117.5	92.5	64.1	45.8	78.4	174.0	141.5
2	580.4	745	494.1	781.0	477.5	600.3	702.1	764.4	586.6
3	897.4	1083	788.1	1131.4	735.9	834.1	982.1	1139.4	867.7
4	1519.9	1825	1312.1	1849.6	1234.6	1423.5	1627.7	1853.4	1379.0
5	915.1	1124	841.1	1207.6	802.6	902.0	1044.2	1112.8	820.4
6	1408.1	1727	1331.8	1762.2	1199.3	1359.2	1539.9	1737.7	1352.8
7	1478.5	1735	1324.8	1744.6	1242.6	1359.8	1513.7	1711.2	1301.1
8	1287.6	1420	1154.8	1412.4	1130.2	1060.6	1178.1	1343.6	1024.0
9	805.3	934	810.6	929.3	782.3	731.1	849.6	1032.4	761.4
10	845.2	1052	928.4	1037.1	827.4	811.4	914.5	1017.9	839.1
11	1575.7	1541	1862.1	1414.8	2102.4	1425.2	1399.5	1370.8	1390.1
12	2600.8	2619	3055.0	2385.0	3394.5	2337.8	2341.1	2340.9	2277.3
13	2205.3	2224	2591.5	2024.0	2879.0	1986.4	1991.9	1993.6	1936.0
14	3018.7	3028	3550.0	2754.8	3951.3	2732.2	2732.5	2624.6	2666.8
15	1994.0	1991	2405.7	1804.4	2715.6	1827.7	1823.6	1813.0	1787.9
16	1433.0	1407	1493.0	1253.8	1485.4	1279.7	1264.1	1246.2	1255.9
17									
Patch	124.0K	123.8	124.1	123.9	125.5	123.9	123.86	123.82	123.91
Pri Tel	19.3C	6.4	35.5	1.62	37.1	18.9	11.3	2.88	20.11
Sec Tel	7.5C	-3.3	21.7	-7.88	22.8	7.5	1°	-6.88	8.75
F/C	303.9K	303.7	313.7	303.68	317.3	303.8	303.7	303.7	303.94
SCT	78K	78	78	78	78	78	78	78	78
Base	20.0C	4.1	39.1	-1.39	39.8	19.5	10.1C	+.15	20.95
ECT	-51C	-51	-51	-51	-51	-51	-51	-51	-51
No. Samples	42	42	42	42	42	42	42	42	42

TABLE 10.7-4

NEΔN MEASUREMENTS

(F/C - Hi - Power)

Channel	$\Delta N/\Delta X$ @ 118°K	NEΔN @ 118°K	$\Delta N/\Delta X$ @ 124°K	NEΔN @ 124°K
1	0.58	3.20	1.18	6.4
2	0.18	0.54	0.36	1.1
3	0.12	0.40	0.22	0.79
4	0.076	0.26	0.13	0.40
5	0.13	0.43	0.21	0.68
6	0.084	0.28	0.13	0.45
7	0.083	0.30	0.13	0.43
8	0.091	0.24	0.12	0.30
9	0.072	0.14	0.11	0.22
10	0.039	0.11	0.056	0.15
11	0.0024	0.010	0.0024	0.011
12	0.0022	0.003	0.0020	0.003
13	0.0025	0.005	0.0022	0.005
14	0.0015	0.002	0.0014	0.002
15	0.0018	0.003	0.0017	0.003
16	0.00082	0.001	0.00074	0.001

the scan mirror. Helium gas was used to hold the F/C in synchronization during the test. The BCU, computer and tape recorder were used to obtain data during the test. The test involved taking measurements at different albedo levels with some levels being repeated. Each measurement was the average of 42 samples.

10.8.2 Results

The results of the test are shown in Table 10.8-1. The albedo levels are those for the current and calibration voltage as determined by NASA. For each albedo level the current was set to the value determined by NASA, the current setting was within ±0.01 amperes. The test voltage levels are those obtained during the test along with the signal and standard deviation (σ) for 42 points. Some decrease in signal output is noted during the test, it has not been determined whether this was due to temperature effects on the output of the VCTA or a degradation of the VCTA. The source has been sent back to NASA for re-calibration. Below are listed the slope of the points and noise equivalent albedo.

$X/\Delta A$ = 12.14 counts/% albedo
NEA = 0.04% albedo

10.9 Scan System Modifications

10.9.1 Background

During V/T testing of the PFM unit at ITT-A/OD on November 24, 1974, toward the conclusion of the 0°C baseplate cold soak, the scan mirror drive subsystem developed an anomaly which was subsequently found to be an abrupt change in the motor slewing rate. This reduced velocity rate change affected all ramped slews, but resulted only in a failure of the motor to retrace or return the mirror to the start of scan position in the four data element times allotted (424.8 ms) for this operation. This failure of the mirror to return to the start of scan position during the retrace slew period "trips" a "scan mirror out-of-sync" detectors circuit, an internal logic function which concludes that the mirror position is totally unknown and must re-initiallize at the internal warm target position in a new attempt to organize the mirror scan pattern properly.

The failure was traced to a false logic transition on the "Carry Out" pin of a digital circuit, an up-down binary counter, which through a D/A converter, generates the triangular slow ramp voltage to a voltage controlled oscillator. This device, a CD4029AK (generic device), in location D5 of Assembly 8120423G1 (SN PM1), was replaced with a new part with the

TABLE 10.8-1

Visible Calibration

Albedo (%) @ 0.700μ	Current (amps)	Calibration voltage (volts)	Test Voltage (volts)	Signal (counts)	σ (counts)
82.58	6.6	29.7	29.66	944.64	.66
				992.10	.62
			29.68	983.02	.56
				982.36	.69
53.36	6.0	25.1	25.19	649.76	.43
				646.26	.45
35.03	5.5	21.4	21.35	410.00	.22
				409.86	.35
			21.29	405.14	.47
				403.86	.35
21.29	5.0	18.0	17.95	247.95	.22
				247.57	.50
11.82	4.5	14.8	14.64	132.60	.50
				132.45	.50
0.00	--	--	--	1.28	--

consequence being that the false logic transition now occurred continuously over the entire temperature range of +50°C to -40°C (determined by board test data) rather than occurring only at temperatures below 0°C.

Consulting the applications engineering department of the manufacturer disclosed that the device was known to have an "on chip" race condition which would often result in this type of problem. A complete solution to the problem fortunately existed if steps external to the counter were implemented to gate or filter out the sub-microsecond false transition. The decision was made, with the concurrence of NASA, to filter this false transition by means of a simple RC low pass filter (composed of a 100K ohm resistor and a 22 pf capacitor) as shown in Figure 10.9-1. This filter, with a time constant of 3μs, blocks all transitions occurring within this interval after counter clocking.

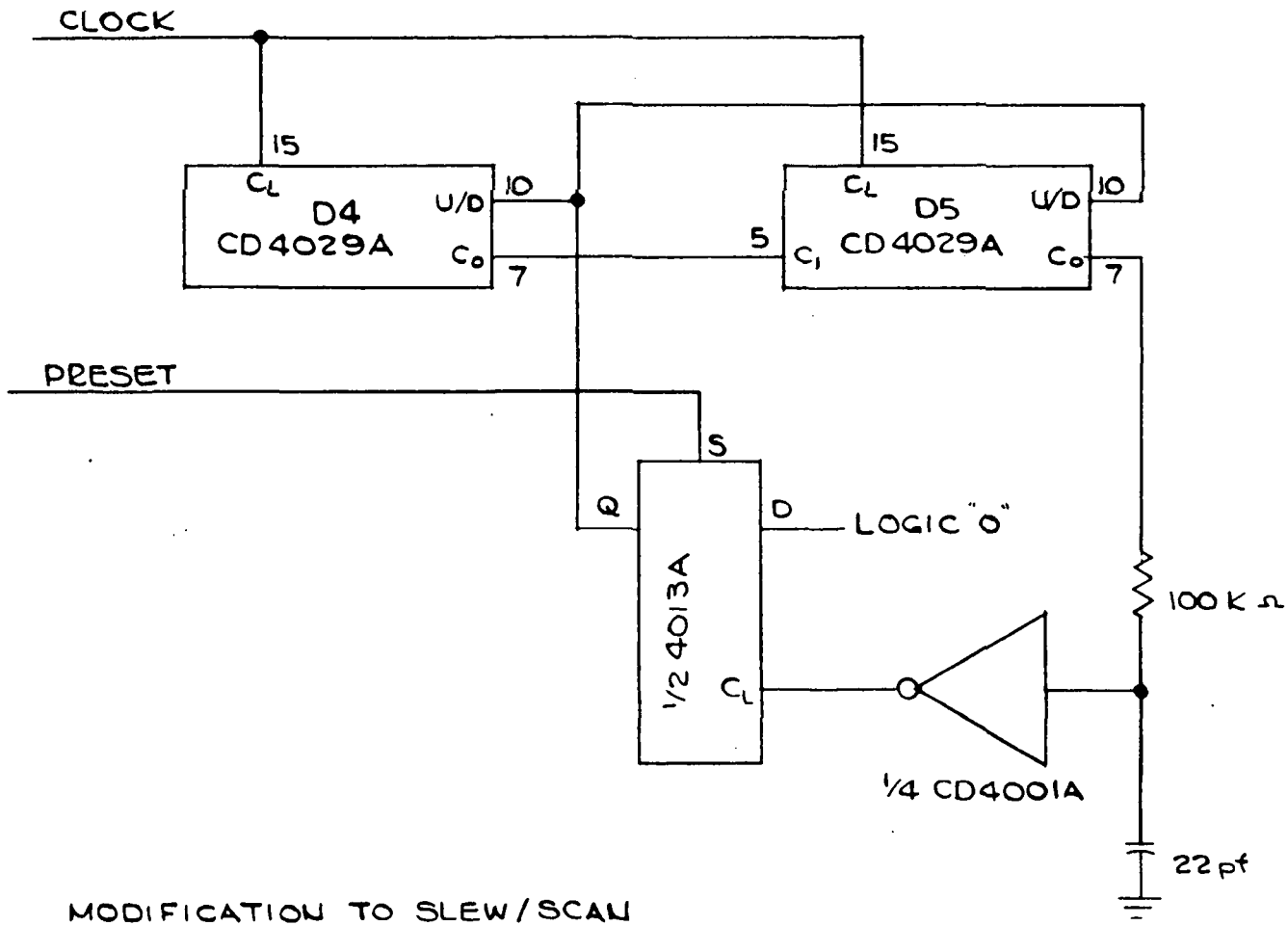
10.9.2 Chamber Tests

The modified board (per ECN No. 6128-506) was then individually tested in a temperature chamber while electrically connected, by means of a cable, to the HIRS PFM unit over a temperature range of +50°C to -40°C without detecting any malfunctions. The board was then directly inserted into the HIRS which was subsequently installed in the V/T chamber and tested at high vacuum at a baseplate temperature of -3.7°C and an electronics cavity temperature of -1.0°C. No scan system malfunctions were noted.

10.10 Telemetry Summary

A compilation of telemetry taken at each of the vacuum chamber temperature plateaus is given in Table 10.10-1. This information is useful within some bounds. It must be recognized that some deviation in telemetry is caused by various modes of operation used during the functional and system sensitivity tests. A deviation must be considered in more depth, as was done periodically during the test sequence. The telemetry outputs have been reviewed in depth, with the result that no signs of system losses or degradation are known to have occurred during the test.

Table 10.10-2 is a listing of the telemetry readings with ranges anticipated during nominal system operation at a baseplate temperature in the range of 14 to 18°C. These values have been used for monitoring of system performance at spacecraft integration level tests and found to be valid.



MODIFICATION TO SLEW/SCAN
CONTROL LOGIC #3
ASSEMBLY NO. 8120423 G1
SCHEMATIC NO. 8120420

MODIFICATION CONSISTED OF ADDING 100K Ω RESISTOR AND 22 pf CAPACITOR (ECN 61280-506)

FIGURE 10.9-1 SLEW RAMP UP/DOWN COUNTER

TABLE 10.10-1 PROTOFLIGHT ACCEPTANCE TEST DATA SUMMARY

	THERMAL VACUUM TEST TELEMETRY OUTPUT									
	20°C Baseline	5° Soak	40° Soak	0° Soak	40° Soak	20° Cal	10° Cal	0° Cal	20° Cal	Units
F/C HSG Temp	304.6	303.3	313.6	301.6	315.6	303.9	303.5	303.3	304.0	°K
Cone Temp	169.6	167.1	168.2	167.5	171.3	167.8	166.3	165.2	167.8	°K
Cooler HSG Temp	279.9	267.7	283.1	266.2	283.7	275.2	270.5	265.6	274.9	°K
Base Plate Temp	20.03	4.05	39.1	-1.1	40.2	19.7	10.0	0.3	20.8	°C
Patch Temp	124.45	123.76	134.0	123.76	125.51	124.01	123.83	123.80		°K
Patch Temp Low						119.21				°K
Patch Power	177.8	2037.2	1.3	4182.5	120.2	191.6	1704.6	2906		μω
+15V DC Elect.	14.77	14.77	14.78	14.77	14.78	14.78	14.77	14.77	14.88	Volts
-15V DC Elect.	-14.93	-14.93	-14.94	-14.93	-14.93	-14.93	-14.93	-14.93	-14.93	Volts
-10 DC Logic	10.06	10.06	10.04	10.05	10.04	10.06	10.07	10.05	10.07	Volts
+5V DC Logic	5.24	5.24	5.25	5.23	5.24	5.24	5.24	5.24	5.24	Volts
Deploy Cover	-.961	-.965	-.74	-.743	-.830	-.873	-.927	-.945	-.974	Volts
Store Cover	-5.29				-5.17				-5.32	Volts
Scan Motor Temp	22.4	4.6	42.3	-1.3	42.1	23.2	12.9	1.8	24.2	°C
Scan Motor Current	.637	.667	.617	.654	.622	.656	.656	.666	.641	Amp
F/C Motor Current	339.6	352.4	311.9	364.2	324.4	346.4	350.5	363.6	345.2	MA
F/C Motor Current		442.7 (High)		521.5				462.9		MA
Scan Mirror Temp	5.41	-7.30	19.4	-11.77	19.27	7.65	-1.26	-9.13	4.55	°C
Primary Tel. Temp	20.00	6.87	35.65	2.08	36.57	10.51	11.17	3.52	19.23	°C
Secondary Tel. Temp	9.00	-2.75	23.57	-7.48	23.06	9.37	0.72	-5.83	8.31	°C
Electronics Temp	21.90	6.67	39.48	1.41	40.1	21.41	12.04	2.92	20.22	°C
-24.5 VDC TLM	-24.47	-24.45	-24.60	-24.55	-24.55	-24.84	-24.86	-24.88	-24.86	Volts

ANALOG TELEMETRY LIMITS

TABLE 10.10-2

Analog TM Channel No.	Function Nomenclature	HIRS Protoflight Normal Operating Limits			
1.	Scan Mirror Temp.	$4^{\circ}C \pm 8^{\circ}C$			
2.	Pri. Tel. Mirror T.	$15^{\circ}C \pm 8^{\circ}C$			
3.	Sec.Tel. Mirror T.	$6^{\circ}C \pm 8^{\circ}C$			
4.	F/C Housing T. 1	$303.9^{\circ}K \pm 0.5^{\circ}K$			
5.	F/C Housing T. 2	$304.0^{\circ}K \pm 0.4^{\circ}K$			
6.	F/C Housing T. 3	$303.6^{\circ}K \pm 0.7^{\circ}K$			
7.	F/C Housing T. 4	$303.8^{\circ}K \pm 0.4^{\circ}K$			
8.	F/C Motor Temp.	$27^{\circ}C \pm 5^{\circ}C$			
9.	Radiant Cone T.	$168^{\circ}K \pm 6^{\circ}K$			
10.	Rad Cooler Hsg. T.	$227^{\circ}K \pm 8^{\circ}K$			
11.	Baseplate Temp.	$15^{\circ}C \pm 5^{\circ}C$			
12.	Electronics Temp.	$17^{\circ}C \pm 5^{\circ}C$			
13.	Patch Temp.	$123.6^{\circ}K \pm 0.4^{\circ}K$			
14.	Patch Power	6 Mw ±6Mw (0 Mw @ $124^{\circ}K$ Patch Temp) (Door			
15.	Cooler Cover Pos.	1.0V±0.3V Open)	5.0 ±0.35V (Door Closed)		
16.	+15VDC Elect.	+14.78V±0.07V			
17.	-15VDC Elect.	-14.93V±0.07V			
18.	+10VDC Logic	+10.07V±0.05V			
19.	+5VDC Logic	+5.26V ±0.04V			
20.	-24.5VDC TLM	Should follow spacecraft voltage			
21.	Scan Motor Temp.	$17^{\circ}C$ $+6^{\circ}C$			
22.	F/C Motor Cur.	320MA±100MA (NORMAL)	500MA±100MA (HIGH)		
23.	Scan Motor Cur.	690 MA ± 100MA (Normal)	1.65 Amps ±0.35A (During slew)		

10.11 Vibration Test

10.11.1 Purpose and Sequence

The HIRS Protoflight Assembly was hand carried to Goddard Space Flight Center (GSFC) on Monday, November 11, 1974. The purpose of the trip was qualification vibration of the HIRS assembly. The first day was spent setting up and checking out the HIRS using the following pieces of test equipment.

1. Bench Checkout Unit #2
2. Brush Recorder
3. Magnetic Tape Drive
4. Jitter Detection Circuit

The test equipment was used as per Test Procedure TP-8120623. The environmental testing followed Option B of the attached Test Plan.

The Test Plan was deviated in three specific ways:

1. Sine levels were slightly increased because original conversion from protoflight levels to flight levels was in error (see corrected sine levels, Table 10.11-1.)

2. Addition of 10 Hz fit check and low level survey were added for instrumentation and checkout.

3. Test durations in test plan were for protoflight levels, these were changed.

	Sine Sweep Rate (Octaves/Min)	Random Time Duration (Min)
Protoflight	2	2
Flight	4	1

The preceding changes in no way sacrificed test integrity.

The vibration testing did not start until Tuesday morning, November 12, 1974. The sequence of testing is tabulated in Table 10.11-2. The TP-8120623 was followed as noted with an additional 10 minutes of scanning recorded on magnetic tape. The mag tape was taken to the ground station for further processing.

10.11.2 Results

After Z-axis sine and random shake the instrument was mounted on cradle then turned cavity down and filter wheel synchronization and jitter were checked. The reason for cavity

TABLE 10.11-1 CORRECTED SINE VIBRATION LEVELS
HIRS - PROTOFLIGHT TEST 11/12/74

X-AXIS		Y-AXIS		+ Z-AXIS	
FREQUENCY (Hz)	AMPLITUDE "g" 0-to-Pk	FREQ (Hz)	AMPLITUDE "g" 0-to-Pk	FREQ (Hz)	AMPLITUDE "g" 0-to-Pk
5-8	.33 in.*	5-8	.33 in.*	5-9	.33 in.*
8-14	1.1	8-12	1.1	9-15	1.4
14-24	.8	12-18	.9	15-21	4.6
24-34	.04 in.*	18-26	.05 in.*	21-36	1.7
34-46	1.1	26-32	1.7	36-50	.035 in.*
46-56	1.3	32-46	1.1	50-56	3.1
56-70	.9	46-54	1.1	56-80	2.1
70-80	2.0	54-64	1.1	80-120	3.3
80-100	.9	64-76	1.7	120-200	1.7
100-200	.8	76-86	1.1	200-400	3.3
200-350	3.3	86-98	1.6	400-2000	3.3
350-500	3.3	98-200	1.1		
500-2000	3.3	200-2000	3.3		

*EXPOSURE LIMITED TO DISPLACEMENT IN INCHES DOUBLE AMPLITUDE

TABLE 10.11-2

SEQUENCE OF TESTING HIRS PROTOFLIGHT TEST

11/12/74

1. FUNCTIONAL TEST TP-816023 - PRIOR TO VIBRATION

2. Z-AXIS
   - FIT CHECK @ 10 HZ
   - LOW LEVEL SURVEY (5-2000 HZ)
   - QUALIFICATION SINE LEVELS
   - FUNCTIONAL - TP-816023
   - QUALIFICATION RANDOM LEVELS
   - FUNCTIONAL - TP-816023

3. Y-AXIS
   - FIT CHECK @ 10 HZ
   - LOW LEVEL SURVEY (5-2000 HZ)
   - QUALIFICATION SINE LEVELS
   - FUNCTIONAL - TP-816023
   - QUALIFICATION RANDOM LEVELS
   - FUNCTIONAL - TP-816023

4. X-AXIS
   - FIT CHECK @ 10 HZ
   - LOW LEVEL SURVEY (5-2000 HZ)
   - QUALIFICATION SINE LEVEL
   - FUNCTIONAL - TP-816023
   - QUALIFICATION RANDOM LEVELS
   - FUNCTIONAL - TP-816023

down test was to ensure no loose parts resulting from vibration. The cavity down test was performed again only at completion of vibration testing, prior to packing for shipping.

Time was spent after Z-axis testing investigating a change in longwave noise in Channels 1 and 2. The investigation was a precaution taken to ensure that no damage occurred to the system. It was discovered that the change in noise was strictly due to shifting in mean position and not noise spread. The cause for shift was due to the phase relationship between motor drive frequency and filter wheel angular position at sync. The testing continued.

The only other concern resulting from testing was change in jitter characteristics. The peak-to-peak jitter changed only slightly from 55 μsec to 40-44 μsec. The biggest change was due to a lowering of standard deviation of the jitter (i.e., there were fewer peaks than prior to vibration). The cause of change is not readily identifiable, but could exist in two areas: 1) change in double anti-backlash spacer-gear characteristics or; 2) loosening of bearing pre-load-nut (as existed from previous testing). The second cause can be eliminated because of two additional factors:

1) Cavity Down position did not cause stalling of the motor (no axial movement of either filter or longwave chopper).

2) If preload nut is loose the jitter should not get worse but remain at low level (further axis shake change characteristics but peak-to-peak was still higher than previous testing).

It is anticipated that the first reason is the cause of jitter changes. There is no direct way of verifying this cause other than continued operation of F/C drive motor. If the reason for jitter change is spacer-gear contact relationship, operation of F/C drive will cause jitter to settle to a stable characteristic.

After the HIRS unit was returned to ITT, Fort Wayne, it was noted the 2^3 natural binary code digit of the Scan motor shaft encoder was dropping out intermittently.

A close inspection of Brush record data taken following vibration runs disclosed the anomaly occurred during the X axis sine vibration. During the subsequent thermal-vacuum testing, the dropouts became more frequent. The problem was associated with the one track output alone, a non-critical data point, and the test continued.

10.11.3 Post Rework Vibration

Following the Scan system modification described in Section 10.9 the HIRS Protoflight Assembly was again taken to Goddard Space Flight Center (GSFC) on December 12, 1974. The purpose of the trip was to perform post rework confidence level vibration.

The HIRS spacecraft mount was mounted to the shaker slip table. The HIRS-PM was mounted to the spacecraft mount. A baseline test was performed per Par. 5 of TP-8120618, followed by an additional 10 minutes of scanning recorded on magnetic tape. The tape was taken to the ground station for further processing. Prior to vibration a visual inspection per Par. 4 of TP-8120618 was performed.

The test plan consisted of a 10 Hz, .5G fit check followed by an X-axis vibration from 200 to 2000 Hz at 3.3G. The HIRS was not instrumented.

The vibration was performed and completed just at departure time of the GSFC employees. The HIRS was left on the vibration table overnight.

Friday, December 13, 1974, the visual inspection per Par. 4, TP-8120618 was repeated with no discrepancies noted. The baseline test of Par. 5, TP-8120618 was repeated. No anomalies were noted. The HIRS was then placed on the cradle and rotated to cavity down position. Filter wheel snychronization and jitter were checked.

The J7 dummy connector (ITT Pt. No. 8120677) was installed and Cooler Power commanded ON. Proper operation was noted by a measured heater current of 512 ma.

No further anomalies were noted as a result of the vibration. The 2^3 natural binary code digit was still intermittent.

10.12 Delivery to G.E.

Following successful completion of post rework vibration tests at GSFC on December 13, 1974, the HIRS protoflight system (SN002) was deemed flight ready. The unit was packed in its instrument case, purged with dry nitrogen, and delivered to Bert Johnson, GSFC, for shipment to G.E. The HIRS protoflight system was delivered to G.E. on December 16, 1974.