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DEVELOPMENT AND FABRICATION OF IMPROVED SCHOTTKY POWER DIODES

by

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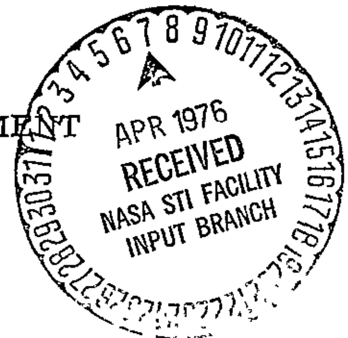

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16. Abstract

Reproducible methods for the fabrication of silicon Schottky diodes have been developed for tungsten, aluminum, conventional platinum silicide, and low temperature platinum silicide. Barrier heights and barrier lowering under reverse bias have been measured, permitting the accurate prediction of forward and reverse diode characteristics. Processing procedures have been developed that permit the fabrication of large area (~1 cm^2) mesa-geometry power Schottky diodes with forward and reverse characteristics that approach theoretical values. A theoretical analysis of the operation of bridge rectifier circuits has been performed, which indicates the ranges of frequency and voltage for which Schottky rectifiers are preferred to p-n junctions. Power Schottky rectifiers have been fabricated and tested for voltage ratings up to 140 volts.

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Section 1

INTRODUCTION AND SUMMARY

Schottky diodes have long been attractive for high power applications by virtue of their reduced power loss in forward conduction and their rapid recovery time compared with p-n junction rectifiers. These virtues are balanced by the disadvantages of greater reverse leakage current, lower reverse bias breakdown voltage, and far greater variability in electrical characteristics due to processing problems. Severe compromises must thus be made in balancing forward drop against reverse leakage current and voltage. The dominant material parameter determining both forward drop and reverse leakages is ϕ_b, the metal-silicon Schottky barrier height. Notwithstanding this, reliable data for the barrier heights of various metals against silicon, obtained from well characterized metal-silicon interfaces fabricated by a reproducible process, have not hitherto been available, with but a few exceptions. The basic data required to make the design compromises needed for optimum Schottky rectifier design have thus not been available. The reason for this is the same as for the variability in Si Schottky diode electrical characteristics – the great difficulty in removing the last fraction of a monolayer of native SiO_2 inevitably present upon a silicon surface and getting intimate, direct, contact between the barrier metal and the silicon.

A theoretical analysis of the efficiency of operation of p-n junction and Schottky rectifier bridges has been performed. This study indicates that for full bridge operation at low frequencies Schottky power rectifiers are preferred over p-n junctions for bridge ratings up to 100-200 volts. High frequency operation extends the voltage range where Schottkys are preferred.

Phase I of the present effort comprised the acquisition of the barrier data and processing parameters required to design the diode of the contract specifications. Phases II and III were concerned with the actual fabrication and testing of devices built applying the technology and following the design of Phase I.

Our efforts were focused upon the contract specification goals. In Phase II these were (a) reverse D.C. blocking capability of 200 volts, (b) 0.6 volt max forward drop at 25 amp forward D.C. current, (c) maximum reverse leakage of 50 ma at 100°C, and (d) 50 nsec reverse recovery time. The Phase III goals were (a) reverse D.C. blocking capability of 100 volts, (b) 0.6 volt max forward drop at 50 amp forward current, (c) max reverse leakage of 5 ma at 100°C, and (d) 50 nsec reverse recovery time.

We have developed reproducible methods for the fabrication of Schottky diodes for the metals tungsten, aluminum, conventional platinum-silicide and low temperature platinum-silicide. We have measured barrier heights

and barrier lowering for these materials, thereby allowing us to predict accurately the reverse junction leakage and the ideal forward characteristics for any specific diode design. We have, further, developed a processing procedure which results in high-yield fabrication of large area mesa geometry Schottky diodes with reverse breakdown capability that is upwards of 50% of theoretical values. We have, in brief, generated the baseline data – ideal material parameters; processing sequences; and knowledge of practical limits – that are required for the design fabrication and assembly of high power-high voltage Schottky diodes.

We have successfully applied the procedures developed by this program to the fabrication of finished power mesa Schottky diodes. Twenty-six diodes substantially meeting Phase II goals and thirty-one diodes substantially meeting Phase II goals were delivered to NASA Lewis.

Section 2

INTRODUCTORY TECHNICAL DISCUSSION

2.1 General Characteristics of Schottky Diodes

In order to provide a framework for discussion, it will be beneficial to consider some of the basic physics of metal-semiconductor contacts. Whenever a metal contacts silicon, a potential barrier is formed between the two. The situation for n-type Si is illustrated schematically in Figure 1. In the Schottky theory of barrier formation, [1, 2]

$$\phi_b = \phi_m - \chi_s , \qquad (1)$$

where ϕ_m is the metallic work function and χ_s is the electron affinity of the Si. A second model of barrier formation, due to Bardeen, [3] gives

$$\phi_b = \phi_g - \phi_o , \qquad (2)$$

where ϕ_g is the Si energy gap and ϕ_o is the energy of the highest filled surface state, measured with respect to the top of the valence band at the

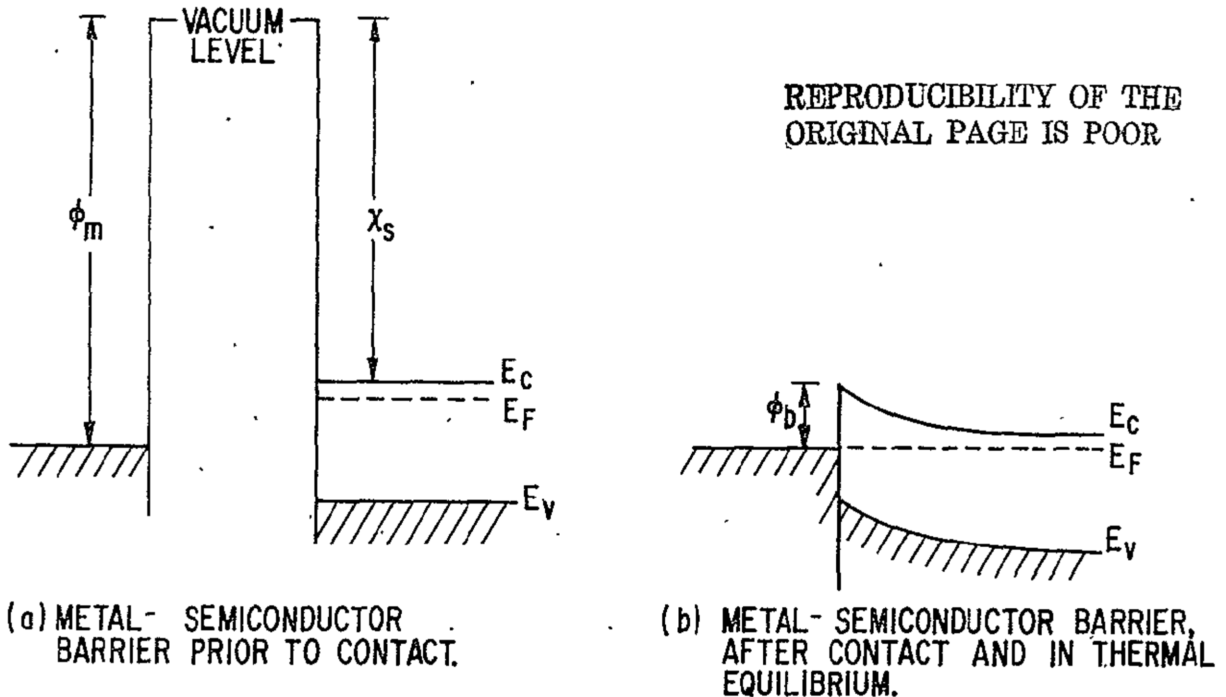

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Figure 1. Metal-semiconductor interface before and after contact formation

surface. Experimental data[4, 5] seem to indicate that the true barrier height lies somewhere between the values predicted by (1) and (2).

In general, the current-voltage characteristic of a Schottky diode is represented by

$$J = J_s \left[\exp\left(\frac{e(V-IR)}{nkT}\right) - 1\right] \tag{3}$$

where V is the applied voltage, I is the total current, R is the sum of all series resistances in the device, n is a "slope" factor which indicates a deviation from "ideality" in a given device, and J_s is the "saturated emission current" given by

$$J_s = A^* T^2 \exp\left[-\frac{e\phi_b}{kT}\right] \tag{4}$$

where A^* is the effective Richardson constant and ϕ_b is the barrier height. Equations (3) and (4) assume that thermionic emission over the barrier is the dominant transport mechanism and the deviation of n from unity is a measure of the departure from this assumption. It is seen from (3) that large values of n will be responsible for excessive voltage drops in the forward direction, as well as large values of R.

Although (3) and (4) accurately describe most forward characteristics, reverse leakages in excess of that predicted by (3), i.e., $J > J_s$ are frequently observed, particularly at high values of reverse bias. This effect is due to three separate sources. The first of these sources is the presence of a generation-recombination current. The second contribution to the "excess" reverse leakage is due to an image lowering of the barrier at high fields[6]. The value of ϕ_b used in (4) should be modified to $\phi_b - \Delta_b$ where $\Delta\phi_b$ is given by[7]

$$\Delta\phi_b = \left(\frac{q\mathcal{E}_m}{4\pi\epsilon_s}\right)^{1/2} + \alpha\mathcal{E}_m \tag{5}$$

where $\mathcal{E}_m$ is the maximum electric field existing at the metal-semiconductor interface, ϵ_s is the dielectric permittivity of the semiconductor, and α is an empirical parameter. Unfortunately, the $\alpha\mathcal{E}_m$ term in (5) is not always negligible and therefore it is not possible to calculate the barrier lowering accurately. Since the "excess" device leakage current depends exponentially on $\Delta\phi_b$, it becomes necessary to make a precise measurement of $\Delta\phi_b$ in order to specify the leakage current for a given device design. A third contribution to the "excess" reverse current may arise from surface leakage currents.

2.2 Experimental Determination of Schottky Diode Parameters

These preceding considerations show that the important parameters in Schottky diode design are ϕ_b, n and if high reverse voltages (V_r) are required, a knowledge of $\Delta\phi(V_r)$ is also required. Of these, n is most easily obtained. From (3) it is seen that n can be obtained from the slope of a log J vs (V-IR) plot for $eV > \sim 3nkT$. J_s can be obtained from the zero voltage intercept of the same plot, and can then be used to calculate ϕ_b, using (4). There may be some doubt as to the correct value of A* to be used,[8, 9] but the value of ϕ_b determined in this manner is not particularly sensitive to the value of A* used. A second method of determining ϕ_b is from a measurement of depletion capacitance vs reverse bias.[10] This method also yields the value of N_d (or N_a) the density of donors (acceptors) in the semiconductor. A final method of determining ϕ_b is by photoemission over the barrier.[11] With this method, the interface is illuminated through the Si, and the zero current intercept of the extrapolated photocurrent (into the Si) vs photon energy plot gives the barrier height. Illumination through the Si is possible because the barrier heights are less than the band gap of Si. It is desirable to measure ϕ_b by several methods on the same device. Any significant variation in the value determined by the independent measurements is an indication of a faulty measurement, or the presence of complicating factors (such as a nonintimate metal-Si contact) in the interface regions. Whatever the cause of these complicating factors, the result is to produce an essentially noncharacterizable device and thus all measurements made on such a device are to be distrusted.

Of the three parameters discussed, the measurement of $\Delta\phi_b(V_r)$ is by far the most difficult. It is possible to make photo-measurements as a function of reverse bias and thus obtain $\Delta\phi_b(V_r)$, but for large values of V_r, the presence of a large thermionic current over the barrier so dominates the photo current that even ac measurement techniques are often unreliable. The problem is further compounded if a measurement of $\Delta\phi_b(V_r)$ is attempted at elevated temperatures.

A second method of obtaining $\Delta\phi_b(V_r)$ is to measure the reverse leakage current as a function of reverse bias. The "excess" leakage current can then be used to obtain $\Delta\phi_b$ using Equation (4). Although this is a relatively quick and simple measurement it is somewhat unreliable since the implicit assumption is made that all the reverse leakage current is due to thermionic current over the barrier. The presence of other contributions to the reverse leakage current will lead to erroneously high values of $\Delta\phi_b(V_r)$.

A third method of determining $\Delta\phi_b(V_r)$ involves measurement of the reverse leakage current (I_r) at a fixed value of reverse bias as a function of junction (contact) temperature. The slope of a plot of log I_r vs 1/T will then give ϕ_b at the given value of reverse bias. A complete knowledge of $\Delta\phi_b(V_r)$ requires measurement of I_r as a function of temperature at a series of

reverse bias values. Care must be taken to insure that the junction temperature is measured accurately. Once again the assumption is made that all of the reverse current is due to thermionic current over the barrier. However, with this method the validity of that assumption can be checked, since the presence of other contributions to the reverse current will in general produce a nonlinear log I_r vs 1/T plot. This can then be used as an indication that a false value of $\Delta\phi_b$ has been measured.

2.3 Reverse Breakdown Considerations

Under reverse bias conditions, the Schottky barrier supports the external voltage in a way quite similar to a p-n junction under similar conditions. In the underlying silicon, a depletion region is formed from which essentially all mobile charge is removed leaving the ionized impurities to create a space-charge region. The resulting electric field supports the applied voltage. The numerical values of resistivity and thickness of depletion layer encountered in Schottky rectifier design are quite comparable to those found in p-n junction rectifiers. Figure 2 illustrates the design of such blocking layers.(11) Here we have plotted a family of curves showing the relationship between resistivity and depletion layer thickness for various choices of breakdown voltage.

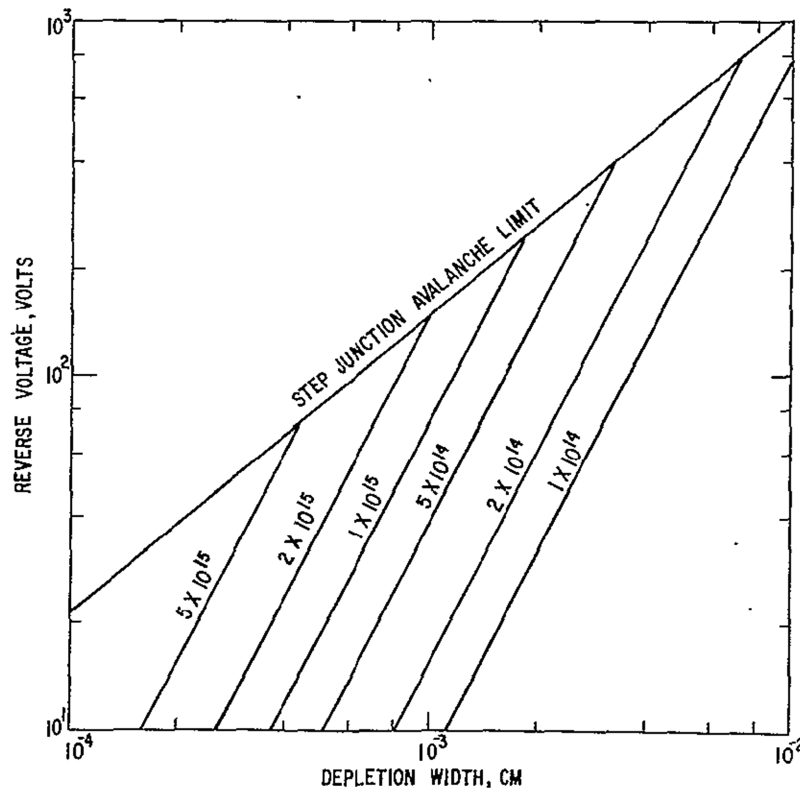

Figure 2. Voltage variation of depletion width and avalanche breakdown voltage for ideal planar step junction

Figure 2 applies for designs in which the depletion layer is considered to be plane parallel. If, however, the depletion layer takes the shape normally associated with a planar junction, then the curves of Figure 3 must be used.[12] Here we see that for a hemispherical approximation to a planar junction the curvature, because of the increased field intensity, causes the breakdown voltage for the junction to be lower than it would be otherwise. Theoretically, it is possible to make planar junctions of reasonable dimensions up to about 1000 volts breakdown. More frequently, one uses the planar technique for lower voltage applications.

The effect of junction or depletion layer curvature becomes increasingly significant as the radius of the curved portion becomes smaller, as Figure 3 illustrates. In Schottky barrier devices this difficulty becomes acute because the effective radius of the depletion layer near the edges of the Schottky metal layer becomes very small indeed. The electric field, therefore, is greatly enhanced and may exceed the avalanche field intensity of silicon (see Figure 4). This difficulty can be avoided by providing a diffused guard ring region under the periphery of the metal-semiconductor interface as is illustrated in Figure 5. In effect, a junction diode is placed in parallel with the Schottky diode. It does not contribute in any important way to forward conducting characteristics because the on-state voltage drop of the Schottky diode

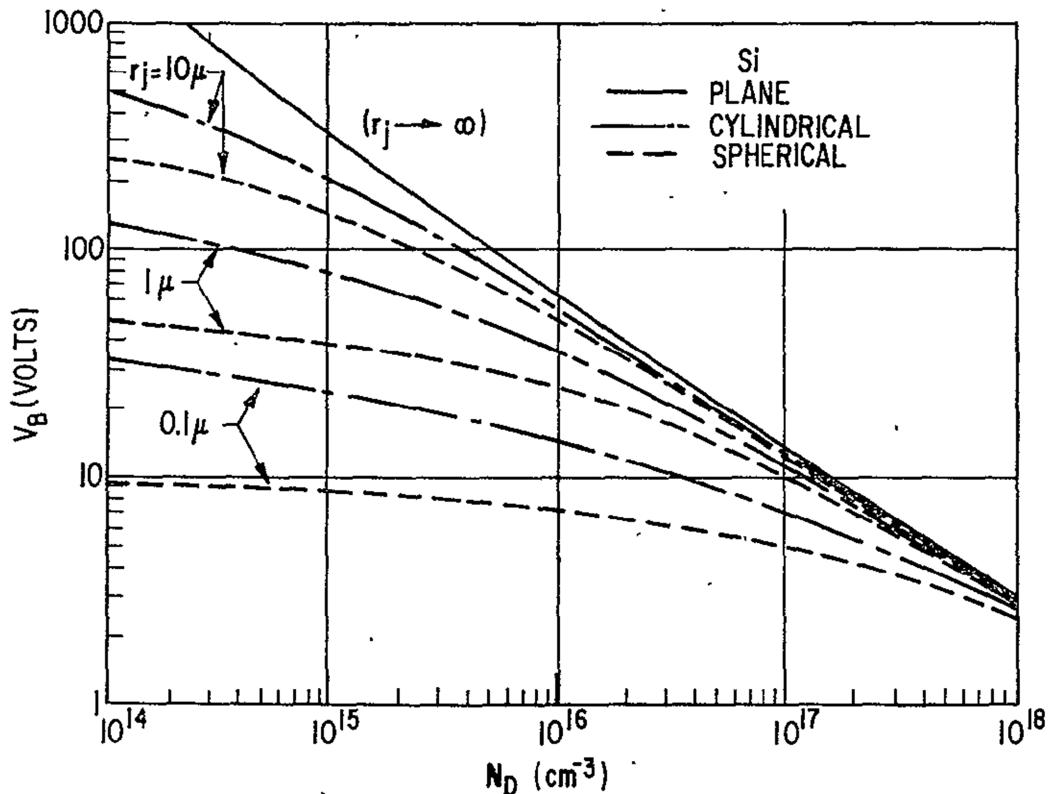

Figure 3. The effects of junction curvature upon avalanche breakdown voltage

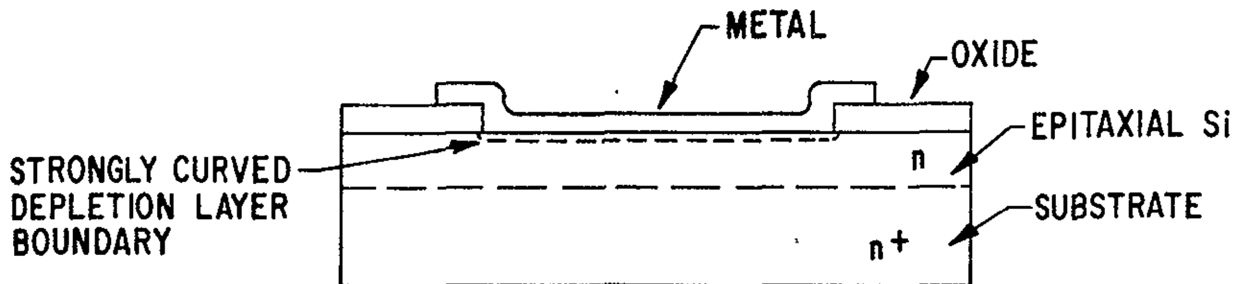

Figure 4. Idealized simple planar Schottky diode structure

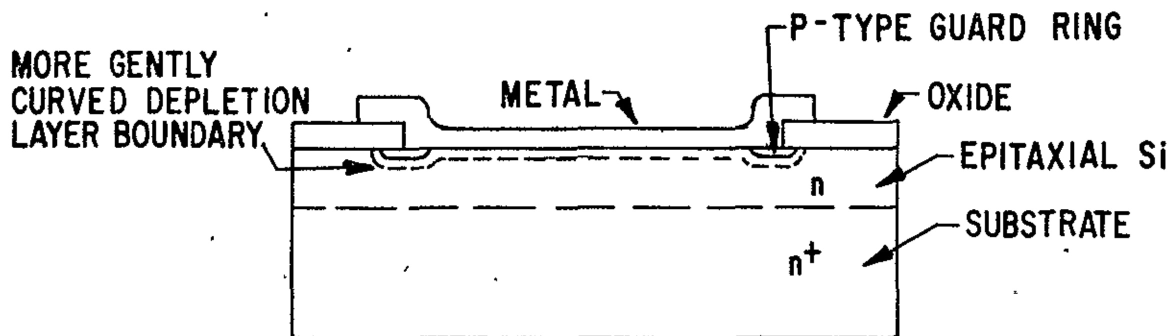

Figure 5. Schottky diode with p-n junction guard ring

is less than that of the junction diode. In the reverse direction, however, this diffused region acts to increase the radius of curvature of the depletion layer at the place where, without its presence, the radius would be very small. A significant reduction in electric field is thus accomplished and the reverse characteristics of the diodes so made are considerably improved.

A similar effect can be obtained by use of the MOS effect as illustrated in the device of Figure 6. Here the oxide surrounding the metal-semiconductor contact is made of an appropriate thickness so that under reverse bias conditions inversion of the surface of the silicon can occur and the depletion layer is thus extended laterally beyond the region of Schottky action. By properly shaping the oxide near the edge of the contact, this action can spread the depletion layer across the surface much more rapidly than it spreads vertically away from the surface and low surface electric field can be maintained. This technique is difficult to implement in practice, however, because the detailed shape of the oxide edge at the boundary of the Schottky metallization is crucial.

Still another approach to reducing the surface field [13] of the edge of the Schottky junction is illustrated in Figure 7. This technique applies principally to power Schottky devices where the dimensions of the device permit beveling of the edge of the pellet without requiring a large increase in the

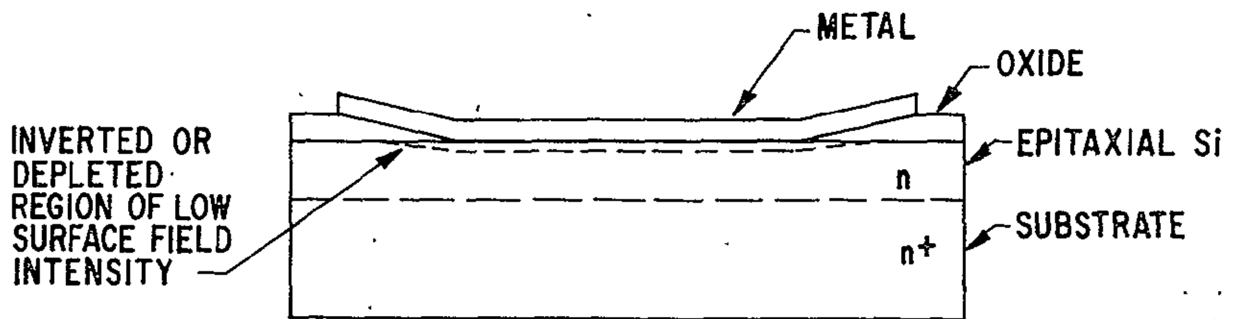

Figure 6. Schottky diode with beveled oxide to reduce field concentration

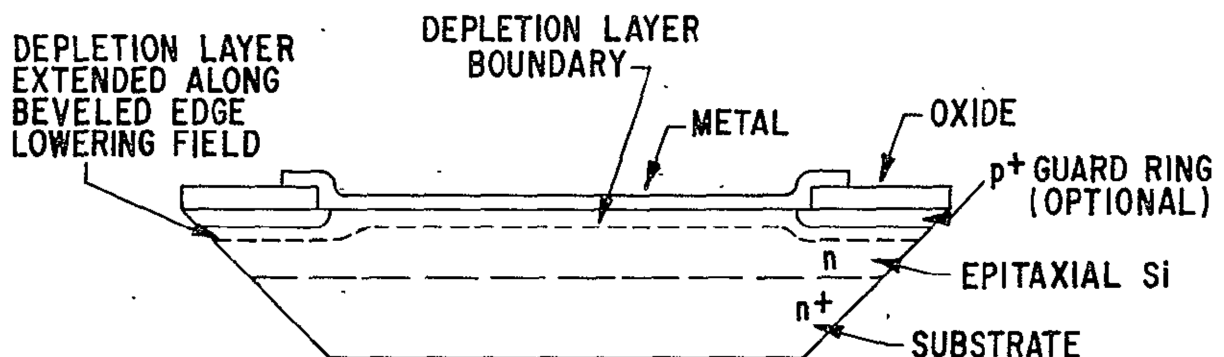

Figure 7. Schottky diode with both p+ guard ring and edge beveling

area of the silicon pellet. This technique is directly analogous to that used in many p-n junction diodes where reduced surface electric fields are provided by properly shaping the edge of the silicon pellet.

Yet another approach to reducing the surface field at the edge relies on forming the contact on a "mesa" as is shown in Figure 8. This method incorporates some of the features of the MOS technique and the beveling technique in a manner which offers great advantages in terms of device fabrication. The extension of the metallization over the oxide, combined with the "mesa" shape, results in the equipotentials in the Si being displaced away from metal-Si contact edge rather than "crowding" toward it as is the case illustrated in Figure 4. This results in a decrease rather than an enhancement of the electric field at the contact edge. It is true that the field is enhanced at the edge of the metallization, but this edge is over the oxide which is easily capable of supporting the increased electric field there. This technique has a further advantage over the guard ring approach in that it eliminates several process steps (cutting the guard ring in the oxide, diffusing the guard ring, and etching the Si to minimize the series drop as is discussed in Section 2.5.2).

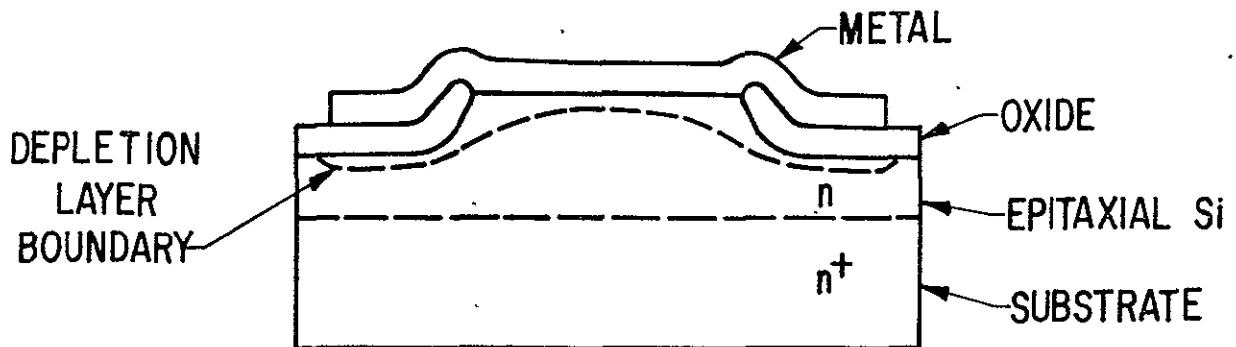

Figure 8. Mesa Schottky diode

All of the above techniques, whether singly, or in combination, can be employed to minimize the concentration of electric fields at the perimeter of the Schottky metal-semiconductor interface region and thus provide suitable low current reverse blocking characteristics. The influence of surface impurities is also much reduced in this way.

It was our opinion at the outset of the contract effort that the mesa geometry represented the best approach to meeting the contract goals. Most important, this approach affords a way to fabricate a power Schottky diode with the minimum possible series resistance. The reason for this is that the breakdown voltage observed with this structure is that for a planar device, since the field is reduced rather than enhanced at the contact edges. Thus the required Si resistivity for a given breakdown voltage is the minimum possible value, and is determined solely by the required breakdown voltage, and not by the radius of curvature of the guard ring junction. In addition, the fact that there is no deep guard ring diffusion implies that the required thickness of the epitaxial layer is just equal to the depletion width at breakdown, as given by the curves in Figure 2. This means that the minimum possible epitaxial thickness can be employed, without using the acid etching technique to reduce thickness described by Heymann and Petruzella.[14] Since the series resistance of a Shottky diode is proportional to the product of the epitaxial thickness and resistivity, the mesa geometry offers the theoretical minimum series resistance for a given breakdown voltage, and presents the designer with the opportunity to achieve the nearest approach possible to ideal forward characteristics.

2.4 Effect of Barrier Height on Schottky Diode Performance

Most carefully done metal depositions on good quality, clean Si with proper contact geometry result in n values [in (3)] between 1.0 and 1.1, and thus n is not of primary importance in determining device performance. Because of the exponential dependence of J_s on ϕ_b, ϕ_b is by far the most im-

portant factor in determining diode performance. This fact is evident from the results of Heymann and Petruzella,[14] who noted that with W-Si Schottky diodes ($\phi_b \approx 0.67$ eV), they could easily meet the required 25A at 0.5V forward condition (I > 30A at 0.5V was obtained) but failed to meet the 100 ma at 100V reverse leakage criterion at 100°C. They also noted that using conventional PtSi-Si Schottky diodes ($\phi_b \approx 0.85$ eV), they could easily meet the required reverse leakages at 100°C ($I_r < 0.4$ ma was obtained) but that with these devices they experienced difficulty meeting the forward requirements. From these observations it is clear that the ideal device would employ a barrier intermediate to that of W and conventional PtSi. This would allow one to "trade" some of the "excess" forward current capability for reverse leakage at 100°C.

In concluding their report, Heymann and Petruzella[14] suggest that the limitation of the conventional PtSi-Si guard ring structure has been reached. They state that:

> "A forward voltage drop of 0.5 V for a 100°C Schottky device with blocking capability of 100V or higher would always be a problem regardless of size due to the inherent high voltage of the barrier required. In the case of (conventional) platinum silicide, the barrier voltage is about 0.4 volt for a 100 volt device. When the voltage due to solders and contacts of about 0.1 volt is added, the desired limit of the forward voltage is reached without even considering the resistive drop in the silicon."

These considerations make it clear that a continuous range of ϕ_b values between W (0.67 eV) and conventional PtSi (0.85 eV) would be desirable in order to provide for the optimum Schottky design over a wide range of reverse voltages and temperatures. Obviously such a continuous range is not physically possible, but our research at GE Corporate Research and Development has provided a number of acceptable contact materials and deposition processes which span this desired range and provide us with a unique capability for Schottky diode design and fabrication. These materials and processes are discussed in Sections 2.5.4 and 2.6.

2.5 Effect of Silicon Properties on Schottky Diode Performance

2.5.1 Effect of Minority Carrier Lifetime

Certain material properties which affect the forward voltage characteristics of conventional junction rectifiers have much less significance when considering design of Schottky devices. The minority carrier lifetime, for example, which affects the forward conducting voltage drop of a p-n junction diode due to its influence on the diffusion length of minority carriers, has relatively little effect on the forward characteristics of a Schottky diode. Of course, in the reverse blocking condition, since recombination centers act

as charge generation sites, one would expect similar behavior for both devices; that is, low lifetime material would cause increased space-charge generation current and thus a higher leakage current under reverse bias. But in the forward bias condition, since the Schottky diode is a majority carrier device, recombination and lifetime considerations need not be considered.

2.5.2 Effect of Si Resistivity (doping density) and Carrier Mobility

To take the place of lifetime as a determining factor in the conducting voltage drop, one must take into account the series resistance of the silicon and other layers used in the device. Conductivity modulation plays an important role in p-n junction rectifiers in reducing the effective series resistance of the silicon layers present in the active areas of the device. In a Schottky diode, however, conductivity modulation plays practically no part. Therefore, a series resistance is encountered in the Schottky diode which may be a significant fraction of the total resistance of the active device. One cannot reduce the series resistance below a certain point, because this implies reducing the resistivity of the silicon under the barrier, and thus reducing the reverse breakdown capability of the device. On the other hand, if the resistivity of the silicon is higher than necessary, the series resistance will be unduly raised, and either the forward conducting drop will rise, or the area of the device would have to be increased to compensate.

One approach toward minimizing the series resistance of a power Shottky diode is that adopted by Heymann and Petruzella,[14] who used epitaxial material and then further thinned the high resistivity Si under the contact to provide a structure with minimum series resistance consistent with the required reverse breakdown specifications. Another approach is the mesa technique discussed in Section 2.3.

A second effect of Si resistivity on Schottky diode performance has already been discussed, in Section 2.3 (effect of ρ on the reverse breakdown). Two other possible effects of resistivity must also be considered. They are the effect of ρ on barrier height and the effect of ρ on the image lowering of the barrier under high reverse bias. A study has indicated that the barrier height in silicon is independent of doping density over the range 0.15 ohm-cm $< \rho <$ 20 ohm-cm. Since this range includes the resistivities normally employed in Schottky diode fabrication, we may conclude that ϕ_b is independent of ρ. The dependence of $\Delta\phi_b$ on ρ results from the dependence of $\mathcal{E}_m$ (Equation 5) on ρ, and is of the form [7] $\mathcal{E}_m \propto 1 \sqrt{N_d}$.

The carrier mobility does not exert a direct influence on Schottky diode performance. However, it must be remembered that the mobility is a function of doping density, and therefore the usual studies which involve a variation of resistivity also include a variation of mobility as a result.

2.5.3 Effect of Dislocation Density and Surface Defects

One effect of high dislocation density has already been discussed in Section 2.5.1. A second, more subtle, effect occurs when etch down processes are employed to minimize the series resistance. Preferential etching may occur at the site of a crystal defect, leading to a reduced epitaxial thickness at that point. A second effect of preferential etching is to create etch pits which give rise to high field points in reverse bias. Both of these effects can significantly reduce the reverse breakdown voltage of a given device. These considerations become more important for large area barriers.

2.5.4 Si Orientation Effects

One area of possible importance which has received little attention is the effect of Si orientation on device performance. The orientation of Si used to fabricate the barrier might be expected to influence three diode parameters, all of which have an influence on J_s, as given by Equation (4); these are A^*, $\Delta\phi_b(V_r)$, and ϕ_b itself. Effects of orientations on A^* have been shown[8] to be small for Si [A^* varies by less than 5 percent from <100>to<111>] and since device characteristics are only weakly influenced by the value of A^* this effect is unimportant. Possible effects of orientation on $\Delta\phi_b(V_r)$ would come through the $\alpha\mathcal{E}_m$ term in (5). This term arises from "the presence of a bound charge distribution near the metal-semiconductor interface"[7] and thus might be sensitive to the detailed atomic arrangement of the Si at the interface.

Such effects are not well understood, and require careful study, because of the profound effect barrier lowering has on reverse leakage currents. Equally important is the effect of orientation on ϕ_b, and the resultant effect on diode performance as discussed in Section 2.4.

Research previously done at GE Corporate Research and Development has indicated that an orientation effect on barrier height does exist and should prove valuable in the design of a wide range of Schottky devices. Our results for Al have been confirmed by Gutknecht and Strutt.[15] Preliminary data showing the barrier heights and orientation effects of the materials we have studied to date are shown in Figure 9. Figure 9 shows that use of the orientation effect enables us to choose the barrier material and Si orientation which results in the most nearly optimum diode design to meet the required specifications. In Figure 9 we have plotted two sets of data for PtSi, one labeled "conv." for PtSi contacts formed in a conventional manner, i.e., sputter-depositing 400Å of Pt onto Si, then heating the samples to 600°C for 20 minutes in a high purity argon atmosphere. The data labeled "low" refer to contacts formed by our low temperature process, described in Section 2.6.

The only barrier heights we have listed on Figure 9 are for those materials for which reliable processes for contact formation exist. We exclude from this list materials and processes which produce diodes with large n

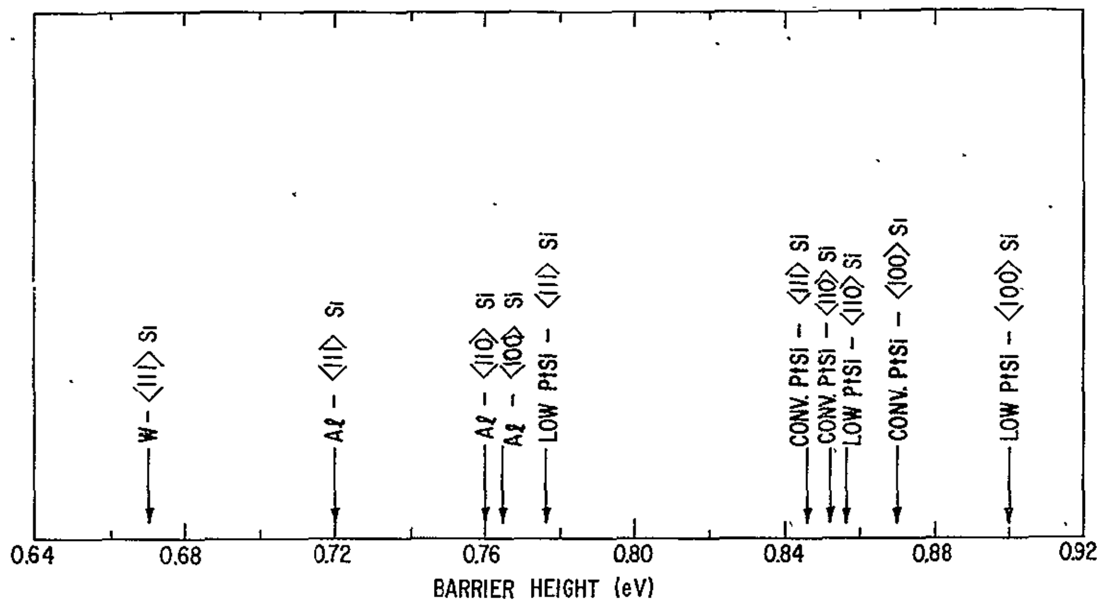

Figure 9. Barrier heights of W, Al, conventionally formed Pt-Si and "low temperature" Pt-Si for major n-Si crystallographic orientations

values, or result in a large variation of barrier heights from device to device. The principal cause of this variation is the presence of a thin "native" oxide on Si.

2.6 New Barrier Materials

A new technology which we feel provides a significant advantage is the "low temperature" PtSi-Si contact system which we have developed and which, when used in conjunction with the <111>Si orientation provides us with a material having a barrier height of 0.78 eV. Although we do not understand how this material is different from conventionally formed PtSi-Si contacts, we have shown that we can reproducibly form this new contact.

As discussed in Section 2.5.4 PtSi contacts are conventionally formed by sputter depositing Pt onto Si and then heating the wafer in an inert atmosphere to a temperature of approximately 600°C to allow the Pt to react with the Si. In our new process, we sputter deposit the Pt onto a heated Si wafer so that the reaction proceeds simultaneously with deposition. The normal thickness of the deposited Pt layer is 400Å.

Although this new material appears attractive because it offers a barrier height intermediate to that of W and conventional PtSi, two other important factors must be considered before we can accept it as a useful barrier material. The first question one must ask is how reproducibly can this material be formed, and the second is are the n values suitably low to yield high-quality Schottky diodes. Experimental data bearing on these two points will be presumed in Section 4.

Section 3

RECTIFICATION EFFICIENCY

3.1 General Considerations

Schottky barrier diodes possess two basic physical properties which distinguish their electrical characteristics from those of p-n junctions. First, they are majority carrier devices where the current is almost exclusively due to majority carrier flow; and second, ϕ_b, the diode barrier height, is smaller than the semiconductor band gap. Schottky barrier signal type diodes which take advantage of the inherent, high speed capability associated with the majority carrier nature of the device have been in use for many years in a wide variety of high speed applications. The second property, however, has been far less exploited. Schottky diodes which take explicit advantage of the reduced barrier height and thus reduced forward power dissipation, are not very common.

In this section we will investigate the rectification properties of Schottky diodes over a wide range of voltage ratings, power dissipation, and operating frequency. We will permit the barrier height to be variable in order to determine the optimum barrier height for each application. We will compare these results with those for corresponding p-n junction rectifiers in order to determine and specify, insofar as efficiency of power conversion is concerned, the range of frequency and voltage over which Schottky rectifiers and preferred to p-n junction rectifiers.

A normalized power loss, L, may be defined for any rectifier circuit by means of the equation

$$L = \frac{\text{POWER DISSIPATED}}{\text{POWER DELIVERED TO LOAD}} \quad (6)$$

For the case of the full bridge circuit with resistive load, Figure 10, L is given by

$$L \doteq \frac{2\left[V_F I_F + (V-V_F) I_R\right]}{(I_F - I_R)(V-2V_F)} \; ; \quad (7)$$

where V_F is the total rectifier forward drop including any resistance drops, I_F is the rectifier forward current at V_F, V is the bridge excitation voltage, and I_R is the reverse leakage current on the rectifier. For the case of the full wave half bridge circuit, Figure 10, L takes the value

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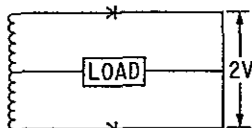
RECTIFICATION EFFICIENCY

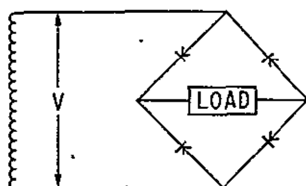
$$\text{NORMALIZED LOSS} = \frac{\text{POWER DISSIPATED}}{\text{POWER DELIVERED}}$$

HALF BRIDGE:



$$L = \frac{J_F V_F + J_R(2V - V_F)}{(J_F - J_R)(V - V_F)}$$

FULL BRIDGE:



$$L = \frac{2\left[J_F V_F + J_R(V - V_F)\right]}{(J_F - J_R)(V - 2V_F)}$$

Figure 10. Full wave full bridge and center tapped half bridge rectifier circuits

$$L = \frac{I_F V_F + I_R(2V - V_F)}{(I_F - I_R)(V - V_F)} \tag{8}$$

where I_F, V, and V_F are as defined in (7). Both I_F and I_R are linear in A, the diode area, so Equations (7) and (8) may be written in terms of J_F and J_R the current densities. In general,

$$V_F = V_j + I_F R \tag{9}$$

where V_j is the rectifier barrier forward bias and R is the diode series resistance.

Minority carrier injection in p-n junction rectifiers modulates the bulk conductivity and the series resistance comprises that of the bulk material shunted by the conductance of the injected plasma. Schottky diodes, however, have little or no conductivity modulation so the inherent, built-in value of series resistance takes the value

$$R = \frac{\rho \ell}{A} \tag{10}$$

where A is the diode area and ρ and ℓ are the resistivity and thickness of the silicon, respectively. They are chosen so as to minimize R while providing

enough total donor or acceptor atoms to support the depletion associated with the desired reverse breakdown voltage.(16) The thicknesses required for ratings up to several hundred volts are measured in microns. The appropriate practical structure is thus epitaxial.

3.2 Schottky Diode Losses

The diode equation gives a relationship between the junction bias and the Schottky diode forward current density. We have

$$J_F = J_R \left[\exp \frac{qV_j}{nkT} - 1 \right] \tag{11}$$

and

$$J_R = A^* T^2 \exp - \left(\frac{q\phi_b}{kT}\right) \tag{12}$$

where A^* is the Richardson constant, n is the so-called "ideality factor", ϕ_b is the Schottky barrier height, T is the absolute temperature and J_f and J_R are the forward and reverse current densities respectively. It has been shown previously(17) that Equations (11) and (12) accurately represent the actual diode characteristics of practical power devices over as many as 7 decades of current if (a) the n values are reasonable (less than approximately 1.1) and (b) the diode series resistance is taken into account. It is thus possible to calculate the normalized power loss for Schottky diodes designed to any given voltage rating comprising any desired barrier height.

We have carried out this calculation for both the half and full wave silicon Schottky rectifier bridges. The calculation covered the range of voltage designs up to 500 volts and included barrier heights up to 1 eV. In this calculation we have assumed that $n = 1$ and that the Richardson constant is $120 A/(cm\text{-}^{o}K)^2$. The effects of barrier lowering, under reverse bias $\Delta\phi_b$, have also been included. The material parameters ρ, ℓ and $\Delta\phi_b$ appropriate for several design voltages are listed in Table I.

TABLE I

MATERIAL PARAMETERS FOR SILICON SCHOTTKY DIODES

Reverse Capability V_R (volts)	Resistivity ρ(ohm-cm)	Epitaxial Thickness ℓ (micron)	Barrier(18) Lowering $\Delta\phi_b$ (eV)
10	.06	.26	.09
50	.44	2.1	.07
100	.93	4.8	.07
300	4.0	18.0	.06

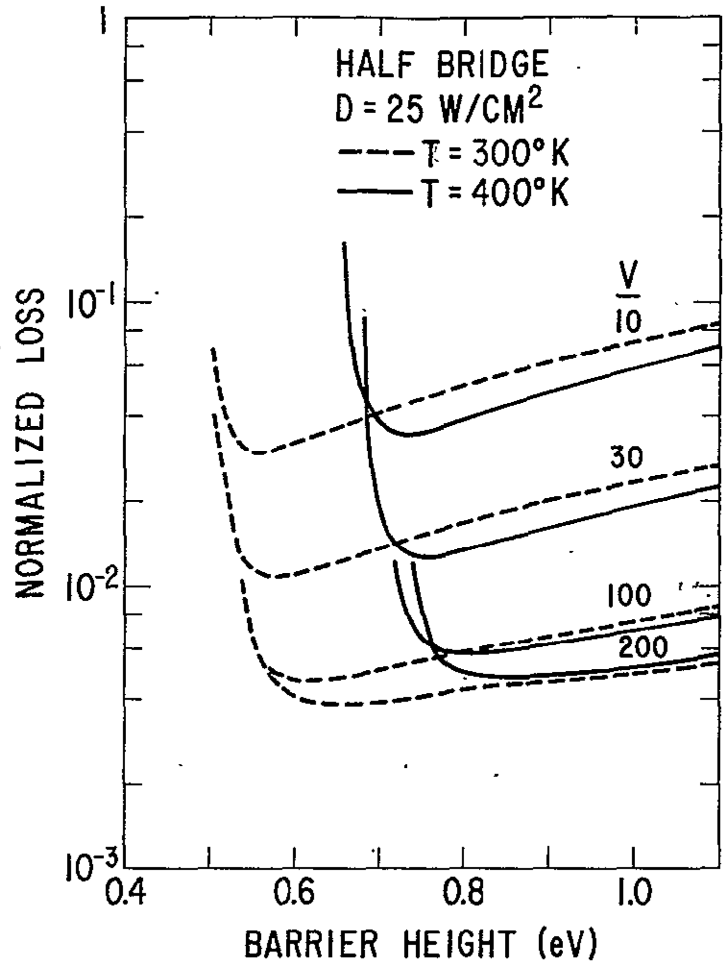


Figure 11. Normalized power loss for Schottky half bridge. Power dissipation per diode is 25 W/cm^2.

The calculation proceeds as follows: First the power dissipation per unit area of diode and the voltage rating are specified. The junction bias V_j in Equations (9) and (11) is varied for each value of $_b$ in order to determine the unique set of values for V_j, J_F, and J_R which will satisfy the dissipation criterion. L is then simply calculated from either Equation (7) or (8).

Typical results presented in the form of the variation of L with ϕ_b for fixed power dissipation and reverse voltage rating are shown in Figures 11, 12, 13, and 14. Figures 11 and 12 give half bridge results for dissipation densities of 25 and 100 W/cm^2 at both 300°K and 400°K for several voltage ratings and Figures 13 and 14 contain the corresponding results for the full bridge. The bridge excitation waveform used in the calculation is that of a square wave of amplitude V in order to simplify the calculation with a unique voltage value.

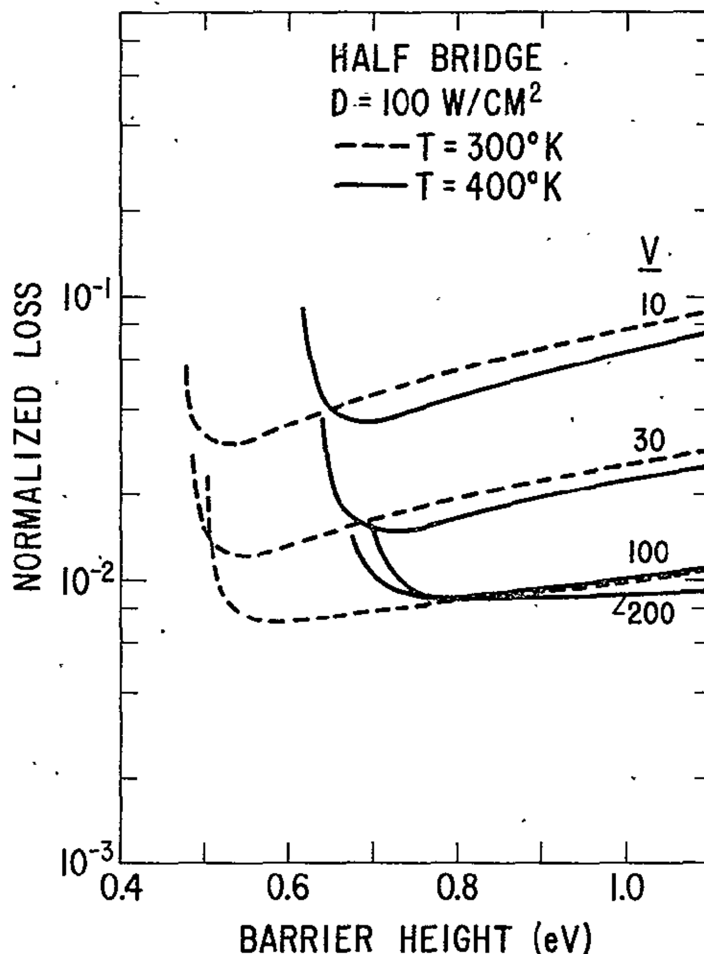


Figure 12. Normalized power loss for Schottky half bridge. Power dissipation per diode is 100 W/cm^2.

All the curves are qualitatively similar. Regardless of power dissipation, voltage rating, or temperature, the normalized power loss initially decreases rapidly as the Schottky barrier height increases, passes through a minimum and then shows a somewhat slower increase with ϕ_b. The reasons for this behavior are quite straightforward. At low barrier heights the reverse current, J_r, is large and the reverse losses, VJ_r, dominate. As ϕ_b increases, J_r falls rapidly permitting J_F and V_F to increase while maintaining constant dissipation. This increase in the forward loss, $J_F V_F$, coupled with the decrease in reverse loss makes for the minimum in L and is the cause for the slow rise in L beyond the minimum. The minimum is shifted to higher values of ϕ_b as the temperature increased due to the increase in diode leakage with temperature.

The results of Figures 11, 12, 13, and 14 show that there is an optimum barrier height for which the normalized power loss is a minimum; i.e., for which the Schottky diode is most efficient as a rectifier. Below this value

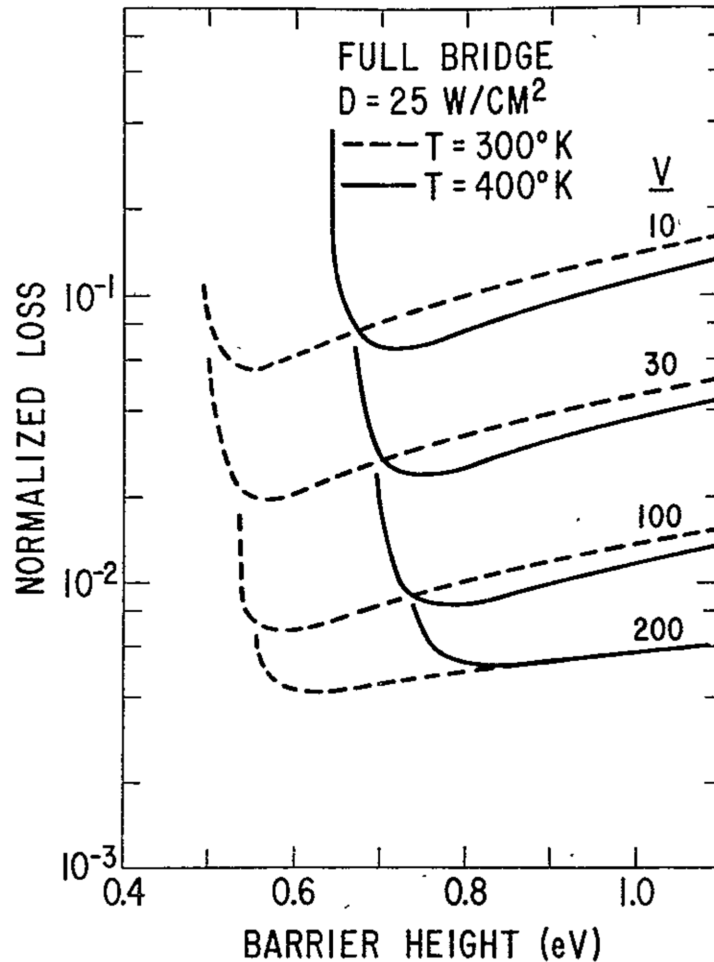


Figure 13. Normalized power loss for Schottky full bridge. Power dissipation per diode is 25 W/cm^2.

the reverse losses are excessive and above the forward losses dominate. At fixed junction temperatures this value is relatively insensitive to blocking capability or power dissipation. The optimum barrier height does, however, vary with junction temperature, shifting by about 0.15 volt from 300°K to 400°K.

An especially noteworthy feature of Figures 11-14 is the result that for designs below about 200 volts the 300°K and 400°K curves cross. The reason for this is that as the temperature increases, both the reverse current and the forward current at fixed forward bias increase. The reverse leakage adds directly to the losses, thereby increasing L and extending the range of barrier heights for which the reverse losses are important. The increase in forward current, on the other hand, increases the power handled, $I_F V$, more rapidly than it increases the forward loss, $I_F V_j$, leading to a reduction in L and more efficient rectification.

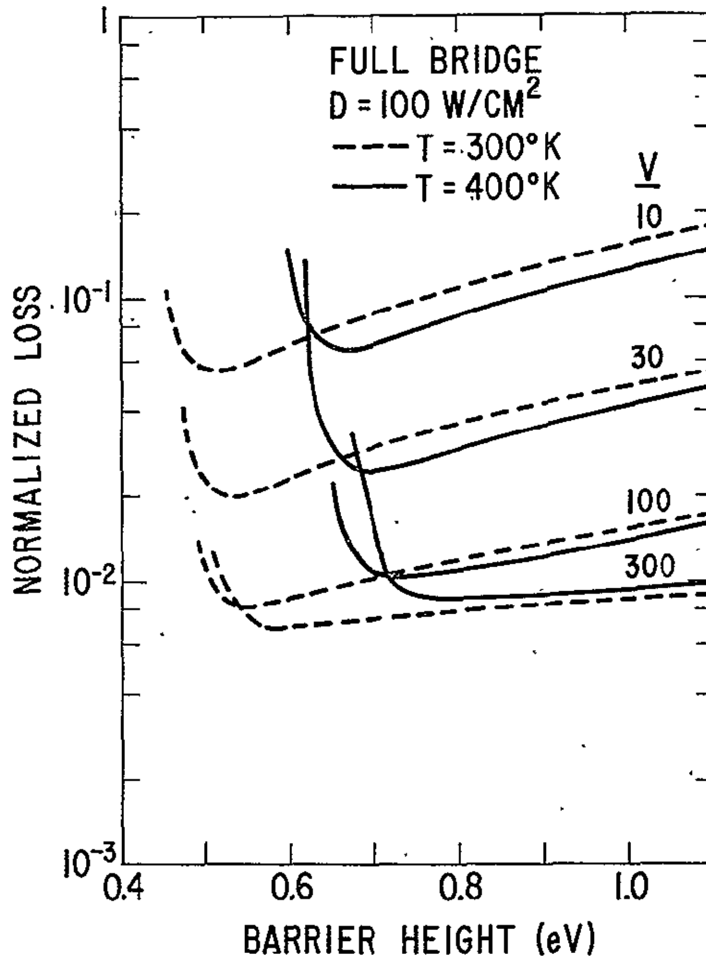


Figure 14. Normalized power loss for Schottky full bridge. Power dissipation per diode is 100 W/cm^2.

Schottky diodes whose barrier heights are to the left of the crossing will have lower losses when operated at room temperature than if run at 400°K. Diodes with higher barrier values, to the right of the crossing, will, on the other hand, run more efficiently at the higher temperature than at room temperature. In short, Schottky diodes with lower barrier heights have positive temperature coefficients of power dissipation, whereas diodes with higher barrier heights have negative coefficients.

These considerations provide the basis for the selection of Schottky barrier values for practical power diodes. A Schottky diode whose barrier height lies to the left of the crossing, even though it be at the minimum of L for 300°K for example, will be inherently thermally unstable. Any momentary increase in power dissipation will raise its temperature, rendering the device less efficient which, in turn, increases further the power dissipation. If this extra heat cannot be conducted away this process accelerates and thermal runaway results. Thermal stability requires that the diode not be

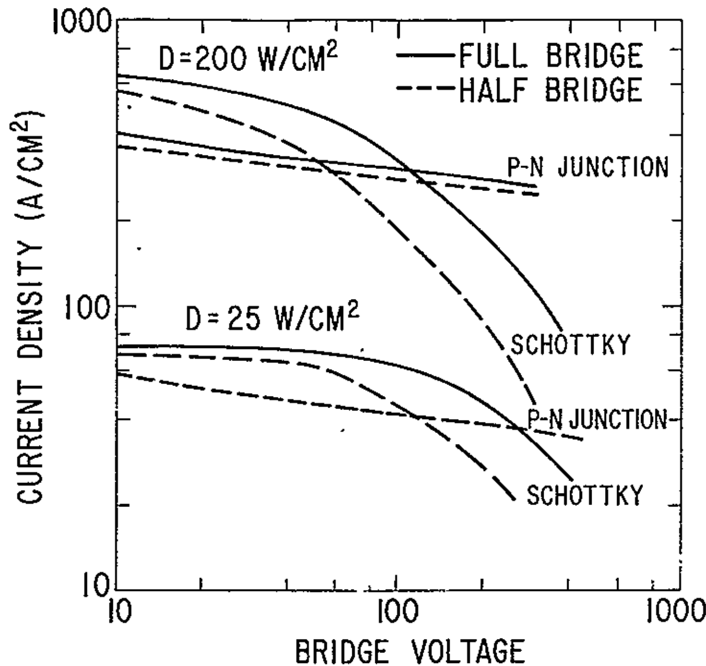


Figure 15. Current density for optimized Schottky diodes at 25 and 200 W/cm^2 dissipation

operated in a regime where reverse losses dominate the total power dissipation. The proper selection of barrier height which minimizes losses and leads to a thermally stable device is that value of ϕ_b which lies at the minimum of the L curve for the maximum allowable junction operating temperature. In this case, any perturbation which momentarily increases the junction temperature decreases the power dissipation thereby concurrently stabilizing the device operating point.

We see from Figures 11-14 that Schottky barrier heights below 0.7 eV are inappropriate for the fabrication of power rectifiers since they result in devices that are thermally unstable. Optimum barrier heights for highest rectification efficiency and stable operation to 125°C lie in the range 0.7-.85 eV depending upon the voltage rating. Device current densities for optimized devices are shown in Figure 15 at 25 and 200 W/cm^2 dissipation.

3.3 Low Frequency P-N Junction Losses

A similar calculation of normalized power loss can be made for p-n junctions. In this case, Equations (7) and (8) describing L remain the same, but we need a new expression relating diode current and voltage. The physical structure of the p-n junction designed to block a given voltage and exhibit minimum forward drop is quite similar to the equivalent Schottky structure

except that the Schottky barrier metal is replaced with a p+ silicon layer. The structure is a p+nn+ one where the n layer has thickness ℓ as above.

Here we make the assumption that the holes that are injected into the n regions modulate its conductivity sufficiently to reduce the voltage drop across this region below several millivolts. Benda and Spenke[19] have solved for the voltage drop across a conductivity modulated region. Their results in volts plotted as a function of reduced lifetime (to be defined below) or n layer thickness are shown in Figure 16.

L' is the ambipolar diffusion length. For L' greater than 2ℓ the drop across the n region at 400°K is less than 4 mv, which is negligible. Under this assumption, all of the current is due to recombination in the n region. The forward current density is given by the expression[20]

$$J_F = \frac{q\bar{p}\ell}{\tau} \qquad (13)$$

where $\bar{p}$ is the space averaged steady-state injected hole density in the n region and τ is the lifetime.

Excess electrons are injected into the n region from the n+ contact in order to maintain charge neutrality. Thus, in the n region

$$n = p = n_i \exp q V_j/2kT, \qquad (14)$$

where V_j is the total voltage from n+ to p+ contact and n_i is the intrinsic number. Equations (13) and (14) may be combined to give

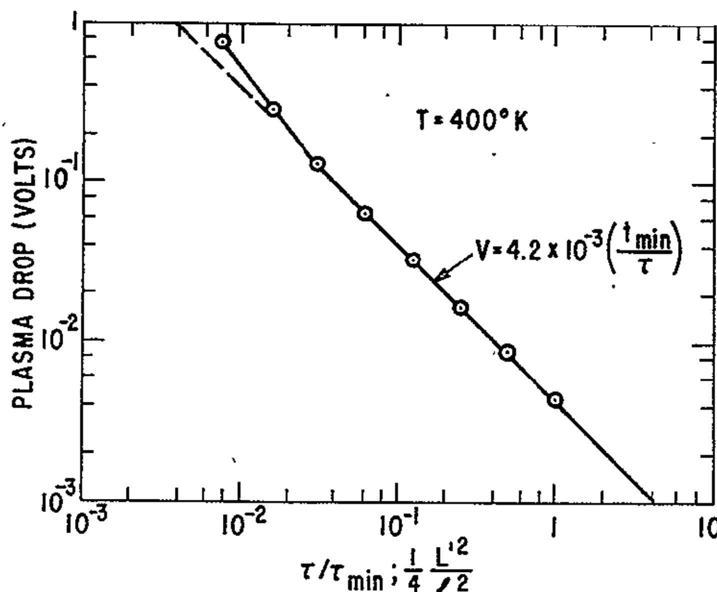


Figure 16. Voltage drop across conductivity modulated n layer

$$V_j = \frac{2kT}{q} \ln \left[\frac{J_F \tau}{q n_i}\right], \qquad (15)$$

a result first obtained by Hall[21] in 1952.

The minimum junction voltage at given current density and thus the minimum forward loss is obtained by minimizing the lifetime. There is, however, a minimum lifetime that is consistent with our assumption of strong conductivity modulation. In general,

$$\tau = \frac{L'^2}{D}, \qquad (16)$$

where D is the ambipolar diffusivity. Under our assumption that $L > 2\ell$, the minimum lifetime is

$$\tau_{min} = \frac{4\ell^2}{D}. \qquad (17)$$

The silicon band gap is greater than 1 eV even at 400°K, so, for blocking voltage less than 10^3 volts, the power dissipated due to reverse current is always smaller than the forward loss. Equations (15) and (17) thus define the minimum power that can be dissipated in the junction while still maintaining negligible ohmic drop across the n region. The normalized power loss may now be calculated from Equations (15), (17), and (10). Values of τ_{min} required to satisfy Equation 17 are given in Figure 17 for various voltages for diodes rated for both full and half bridge operation.

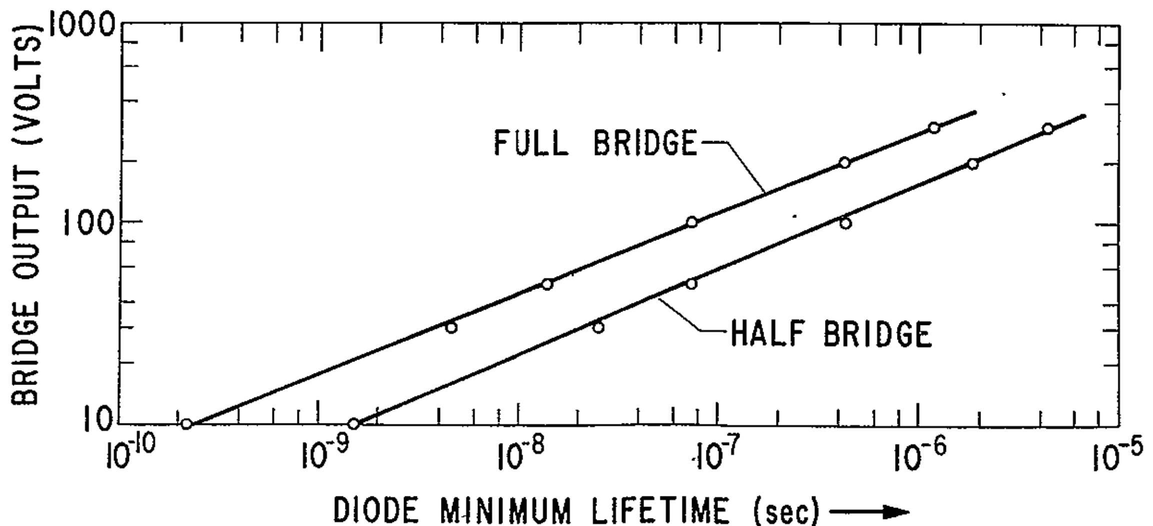


Figure 17. Lifetime required to reduce "ohmic" drop in p+ n n+ structures below 4 mv

The lifetime required for the 10 volt diodes are unattainably short. We have recalculated L for the 10 volt diode assuming a lifetime of 1 nsec.

3.4 Comparison of Schottky with P-N Junction Rectifiers

Values of L for both p-n junction and Schottky rectifier bridges are shown in Figures 18 and 19 for 25 and 200 watt/cm^2 junction dissipation. The junction temperature in all cases is 400°K.

The normalized power loss decreases with increasing bridge voltage due to the essentially linear increase in the denominator of Equation (7). At large power dissipation (high current density) and high voltage, ρ and ℓ increase causing large ohmic $J_F^2 \rho \ell$ losses in the Schottky devices and saturation in L. The normalized loss for the p-n junction devices, on the other hand, continues to decrease with increasing voltage due to the conductivity modulation.

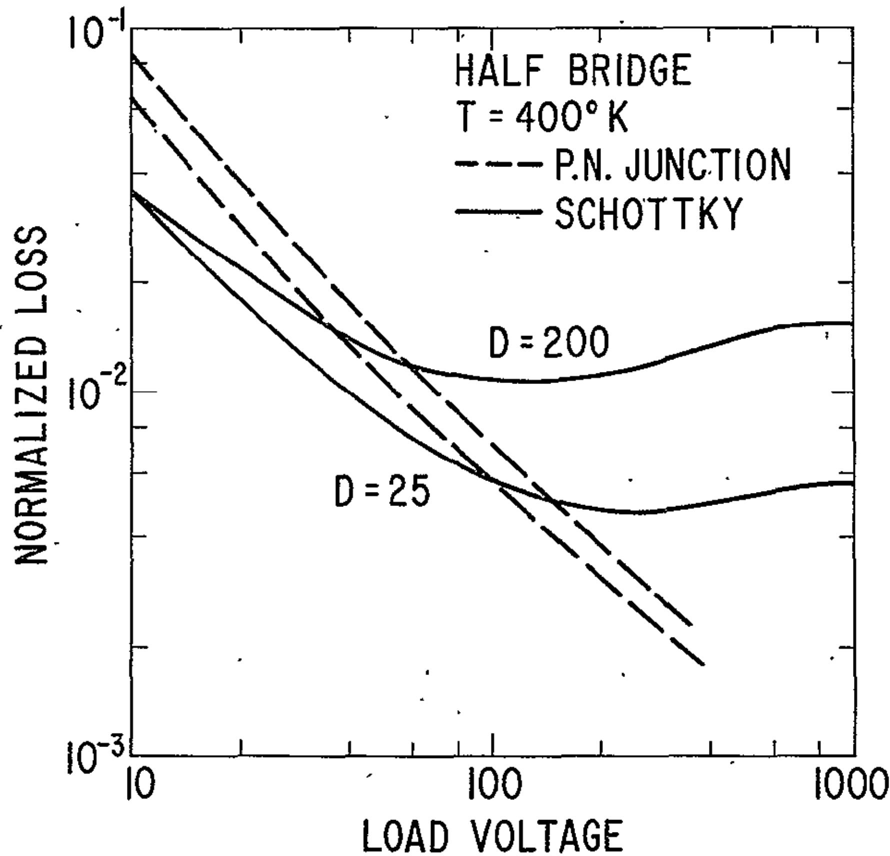


Figure 18. Comparison of the half bridge circuit losses for optimized Schottky barrier rectifiers with those of fully conductivity modulated p-n junctions. The upper and lower curves correspond to 200 W/cm^2 and 25 W/cm^2 dissipation respectively.

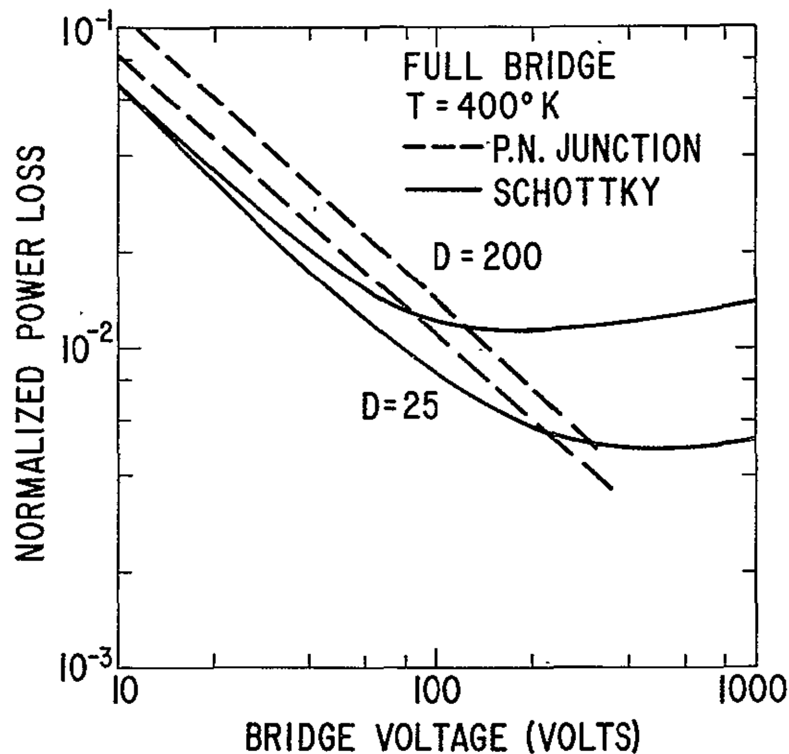


Figure 19. Comparison of the full bridge circuit losses for optimized Schottky barrier rectifiers with those of fully conductivity modulated p-n junctions. The upper and lower curves correspond to 200 W/cm^2 and 25 W/cm^2 respectively.

Nevertheless, the results of Figures 18 and 19 show that for a practical range of junction dissipation there is a range of voltage ratings for which the Schottky barrier is a more efficient rectifier than the p-n junction even at low frequencies. A direct comparison of normalized loss is given in Figure 20 for two voltage ratings, 10 and 50 volts, over a wide range of junction dissipation. The ratio of the useful power delivered to a load by a Schottky rectifier to that delivered by a junction device is presented in Figure 21 for the two cases of 25 and 200 watt/cm^2 rectifier dissipation. We see that the Schottky device is roughly 50 percent more efficient than the junction rectifier at low voltages. The crossover in efficiency depends upon the dissipation level and whether the devices are designed for half or full bridge service.

3.5 P-N Junction Switching Losses

Junction rectifiers have A-C losses as well as the D.C. losses discussed above. These losses are due to sweepout of the injected plasma when the diode is reverse biased. The rectifier takes a finite time to "turn off" and substantial currents flow during a portion of the reverse cycle. Figure 22 shows a simple rectifier circuit. The impressed voltage together with the

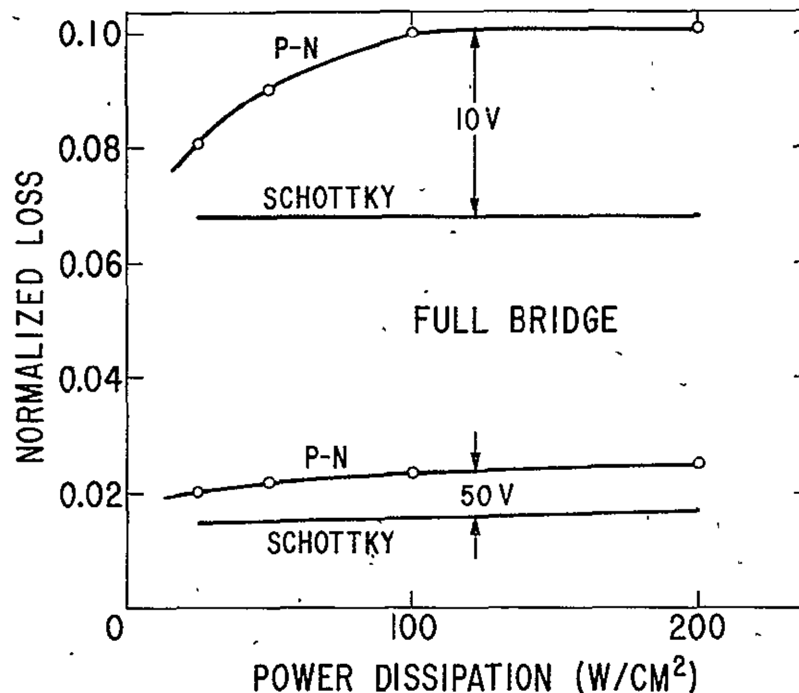


Figure 20. Normalized power loss for 10 and 50 volt rectifiers circuits as a function of junction dissipation

diode current and voltage waveforms are shown over the time interval required for the diode to re-establish its blocking capability. At time t_1 the impressed voltage changes sign. The junction diode, however, still conducts in the reverse direction due to the fact that the plasma which had been injected in the forward portion of the cycle is able to supply carriers to the external circuit. The electric field across the diode is reversed and carriers are extracted from the edges of the plasma adjacent to the highly doped n+ and p+ regions, thereby supplying the charge for the reversed current flow. The plasma concentration at these edges is fed by diffusion from the interior of the modulated region. As long as the plasma concentration at the edges of the n+ and p+ regions is finite the junction bias remains small with the rest of the voltage drop occurring elsewhere. In the case of Figure 22 the drop occurs across R_L which limits the current flow. At t_2 the plasma concentration at the edges of the n+ and/or p+ regions becomes zero and the junction voltage begins to rise. The current falls smoothly to the reverse leakage value, and at t_3 the junction has regained its blocking capability. The details of the turn off are quite varied depending critically upon the device lifetime and the specifics of the rectifying circuit. As an example the reverse current in the initial stage for the circuit of Figure 22 is constant and equal to the forward current V/R_L. For the rectifier circuits of Figure 10, by contrast, the reverse currents will have very large initial spikes with peak amplitudes many times the forward D.C. current since they are limited at the outset only by the residual inductance and resistance of the bridge arms.

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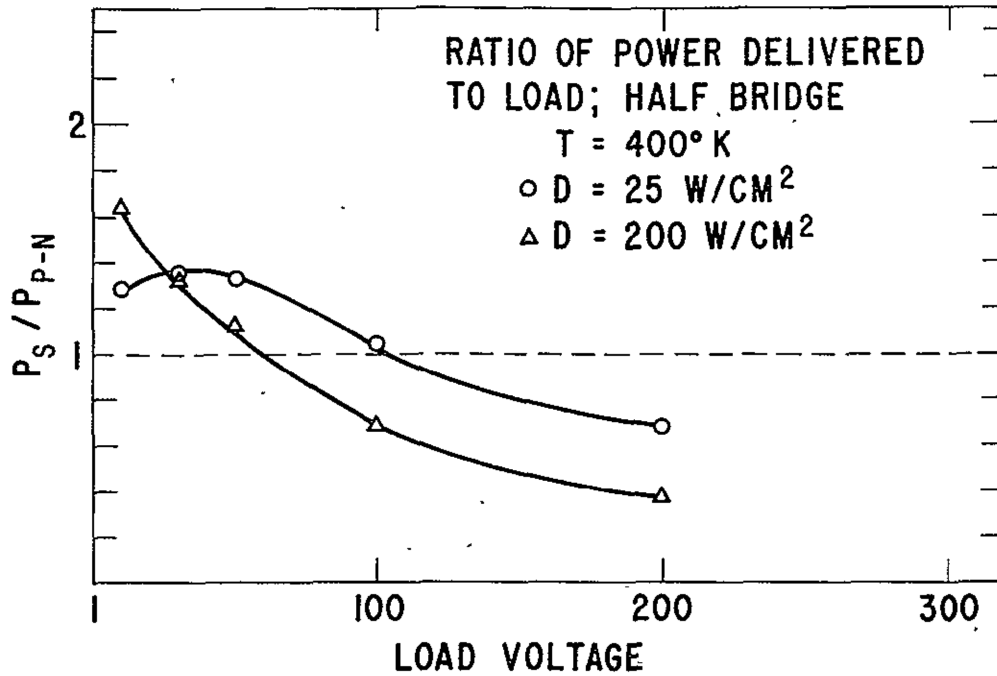
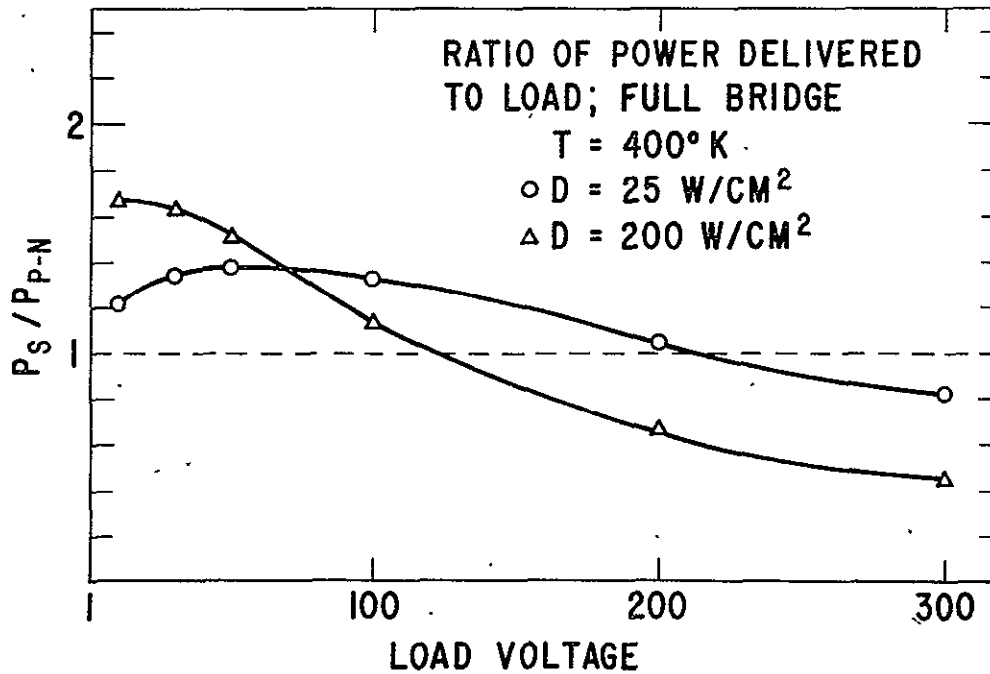


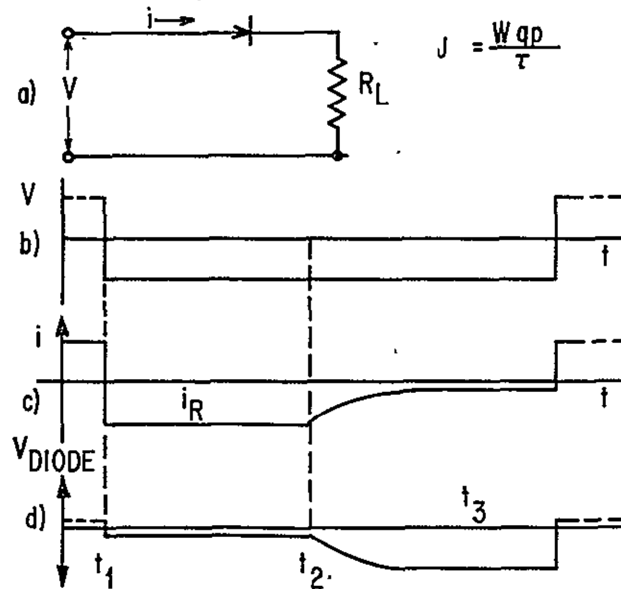
(a) Half bridge



(b) Full bridge

Figure 21. Ratio of the useful power delivered to the load by a Schottky rectifier bridge to that delivered by a junction rectifier bridge

SWITCHING PROCESSES



(a) Simple rectifier circuit (b) Impressed voltage
(c) Current through the load (d) Voltage appearing across the junction rectifier

Figure 22. Simple rectifier circuit

The energy lost per switching cycle, however, is remarkably insensitive to all these complexities. The instantaneous power dissipation appropriate to the process described above is given by

$$P(t) = i\,(t)\,V, \tag{18}$$

where i(t) is the instantaneous reverse current in the circuit and V is the total impressed voltage. The total voltage and not merely the diode drop is appropriate in Equation (18) since we are not making any distinction between dissipation in the diodes and that elsewhere in the circuit. The energy lost per cycle is thus

$$E = \int_{\text{cycle}} P(t)\,dt = V \int i(t)\,dt, \tag{19}$$

the integral being the total charge that is extracted from the conductivity modulated region during the reverse half cycle. This charge per cm^2 of diode is equal to the difference between the total injected charge, $\bar{p}\ell$, and the number of carriers that recombine in the diode before they can be swept out. The switching loss calculation is thus reduced to a determination of the internal diode recombination charge.

The internal recombination current density is

$$\frac{dp(x,t)}{dt} = \frac{p(x,t)}{\tau} \quad (20)$$

which may be directly integrated. When normalized to $\bar{p}$, the space average of the steady state plasma density under forward bias, we obtain

$$\frac{Q_{recombination}}{\bar{p}} = \beta = \int_{cycle} d\left(\frac{\tau}{t}\right) \int_0^{\ell} \frac{p(x,t)}{\bar{p}} dx. \quad (21)$$

We have performed the integration of Equation (21) over the range of lifetime from $10^{-3}\ \tau_{min}$ to τ_{min} for two values of initial reverse current, $I_R = I_F$ and $I_R = 10\ I_F$. Our starting point was Equation (36) of Benda and Spenke.[19] The decay with time of typical normalized plasma distributions are shown in Figures 23 and 24 for lifetimes of τ_{min} and $.0625\ \tau_{min}$ respectively. The double integration of Equation 21 was numerically performed from curves of this type. Examples of the time variation of the space integrals are shown in Figure 25 for the case $I_F = I_R$ for lifetimes spanning the range $10^{-3}\ \tau_{min}$ to τ_{min}. When time is normalized to the lifetime assumed all the decay curves are remarkably similar; the fraction, β, of the initially injected charge which recombines before being swept out varying only from approximately 0.3 to 0.4 over the 10^3 change in lifetime. A similar calculation for the case $I_R = 10\ I_F$ yields the result that β varies from .15 to .20 over the same lifetime range.

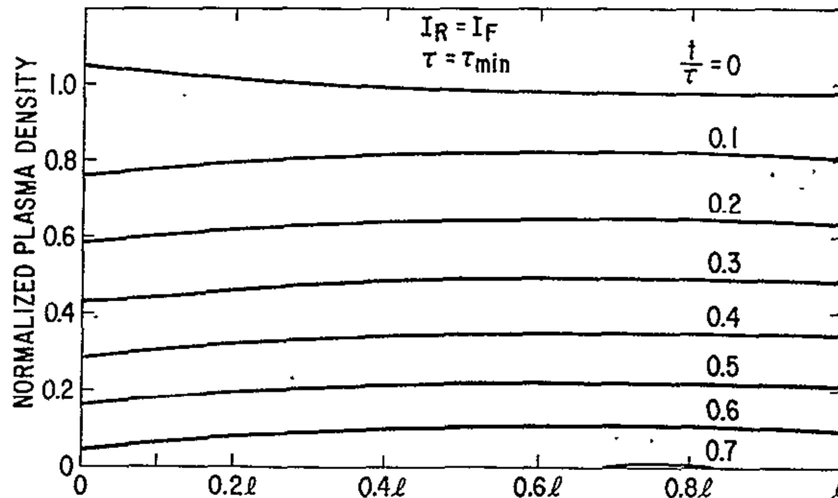


Figure 23. Time evolution of the injected plasma in the n region of the p+ n n+ junction rectifier for the case of long lifetime. The densities have all been normalized to the average forward value, $J_F\tau/q\ell$. The left-right asymmetry is due to the difference in the electron and hole mobilities.

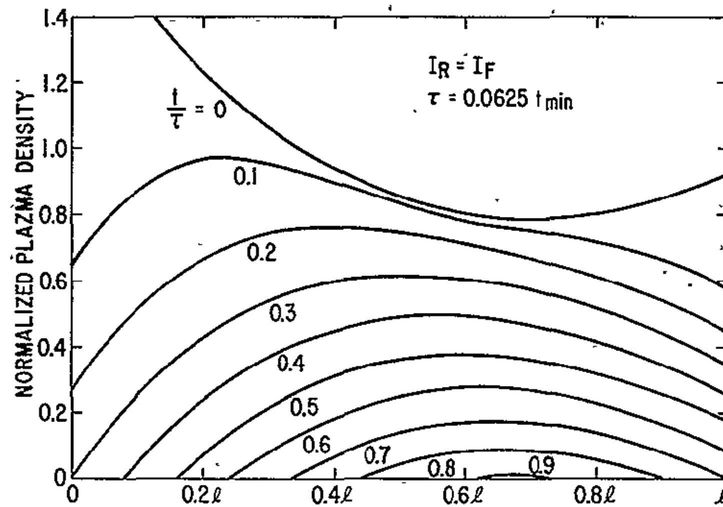


Figure 24. Time evolution of plasma density for short lifetime (τ = .0625 τ_{min}). The effects of recombination are much more evident in this case.

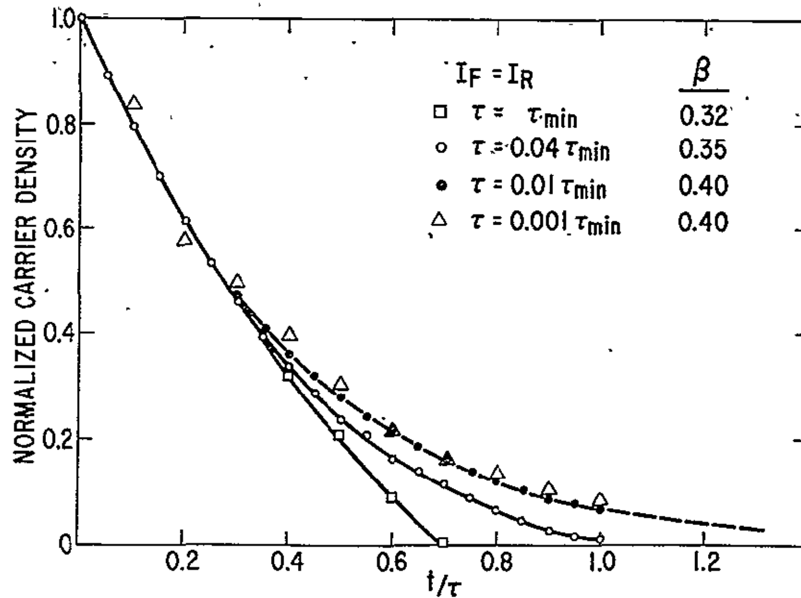


Figure 25. Decay of normalized total injected charge

Recalling from Equation (13) that $\bar{p}$ is given by $J_F \tau/\ell q$ the energy loss per cycle per cm^2 of junction area becomes

$$W = (1-\beta)\ VJ_F \tau, \tag{22}$$

where β varies from .15-.4 over an extremely wide range of reverse sweep-out currents and lifetimes. The total rectification losses must include these switching losses.

The total loss is thus given by

$$P_{AC} = V_j J_F + U_P + (1-\beta)V\ J_F\ f, \tag{23}$$

where the first term is the barrier loss, the second term is the ohmic component, and the third term is the switching loss. In the third term, f is the frequency of operation. The various terms in Equation (23) are shown in Figure 26 where we have assumed an average value of .3 for β. The first two are shown directly as voltage drops. The switching term calculated at 1 MHz has been divided by J_F and is presented as an equivalent voltage for diodes of several voltage ratings. The junction bias varies only very weakly with lifetime and falls in the range .3-.4 volt for all reasonable values of lifetime and current density. It increases slowly as τ increases. The ohmic losses, on the other hand, vary quite rapidly with τ. They become quite significant at a reduced lifetime value of 4×10^{-2} and completely dominate

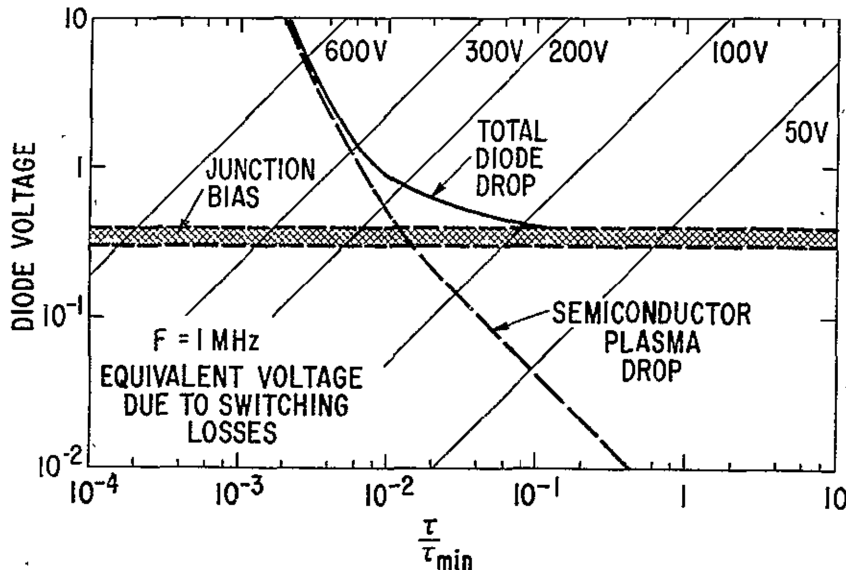


Figure 26. Various components to junction diode losses expressed as voltages. The switching losses are calculated at 10^6 Hz for diodes of various voltage ratings. One may obtain the "drop" appropriate to any other frequency, f, simply by multiplying the curves given by 10^{-6} f.

the d-c forward drop at $\tau/\tau_{min} = 10^{-3}$. It is clear from Figure 26 that the sum of these three terms has a minimum which depends upon frequency and diode voltage rating.

We have recalculated the bridge losses including switching losses for the circuits of Figure 10 for p-n junction rectifiers over the frequency range 10^2-10^6 Hz for rectifiers up to 2000 volt rating. The procedure followed was essentially the same as was followed for the D.C. case except that at each bridge output voltage (i.e., for each junction rating) the diode lifetime was varied at each frequency to determine the value of τ which minimized the total bridge losses.

A specific example is shown in Figure 27 for 200 volts. As τ increases from 10^{-9} sec the loss decreases independent of frequency due to the rapid decrease in ohmic losses. There is clearly an optimum lifetime which is frequency dependent beyond which the loss increases in a manner that is also frequency dependent. At low frequency the increase is due to the slow increase in junction bias and at high frequency the switching losses, linear in τ, dominate. By way of reference, τ_{min} at 200 volts is 4.7×10^{-7} sec. We see that it is advantageous to have τ a factor of 20 less than τ_{min} even at low frequencies.

The optimum p-n junction rectifier lifetimes determined in this way are shown in Figure 28 over the frequency range 10^2-10^6 Hz. Values obtained were essentially independent of junction dissipation in the range 25-200 watt/cm^2. The "low frequency" region extends out to 10^6 Hz for the 30 and 50 volt diodes, to 10^4 Hz and 10^3 Hz for the 100 and 200 volt diodes respectively, and to about 10^2 Hz for the 600 volt rectifier. The optimized 2000 volt device is dominated by switching losses even at 10^2 Hz.

It is worth emphasizing here that the lifetimes shown in Figure 28 are those for which the p-n junction rectifier have the lowest possible losses. Values of lifetime other than those shown will result in greater rectification loss. Decreased τ below the values shown will increase the ohmic loss as the $\tau^{-3/2}$ power and increasing τ increases the switching loss linearly with τ.

Values of normalized loss for p-n junction bridges are shown in Figures 29, 30, 31 and 32 as a function of frequency. As may be seen, the switching losses begin to make a substantial contribution to the losses at frequencies of 10^4 Hz above about 300 volt ratings. Schottky diode losses are frequency independent since there are no switching losses. For any given bridge output voltage one may, therefore, find a frequency of operation above which losses of a Schottky bridge will be less than those of the junction bridge. The locus of these points are shown in Figures 33 and 34. Below and to the right of each curve the preferred rectifier is a Schottky diode

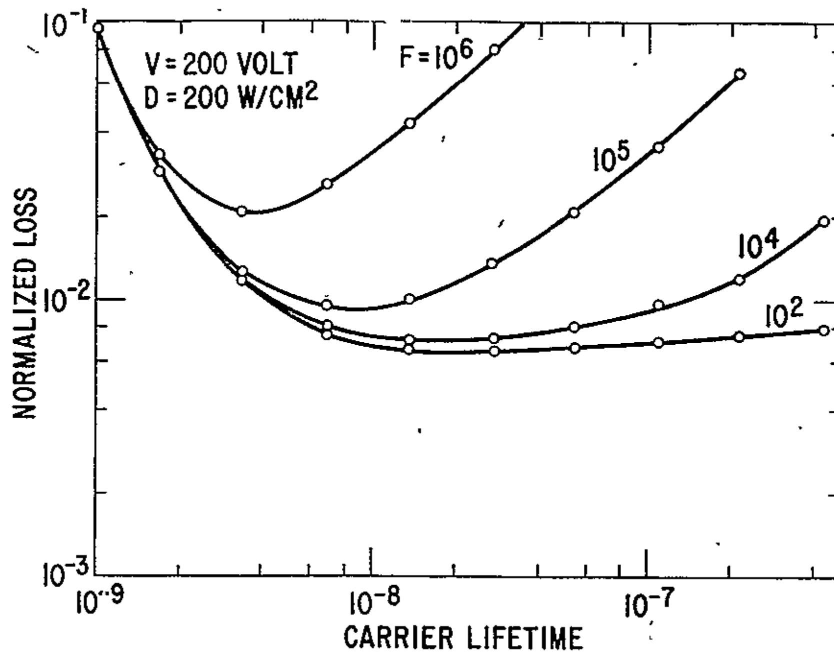


Figure 27. Variation in p-n junction full bridge loss vs. diode lifetime

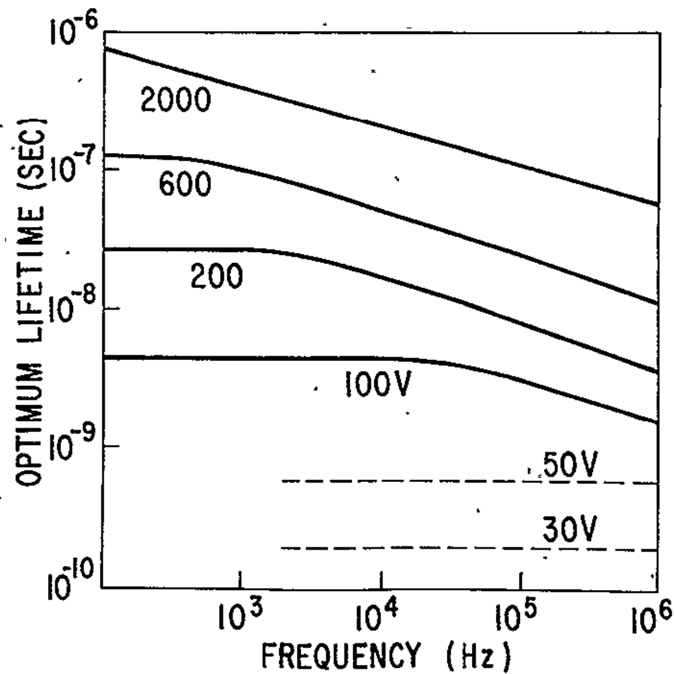


Figure 28. P-N junction rectifier lifetime which minimizes total power dissipation as a function of frequency for various voltage ratings

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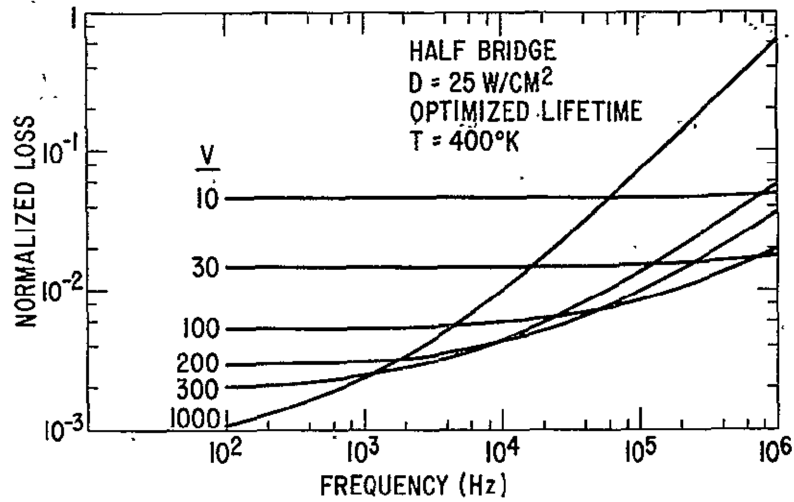

Figure 29. Frequency variation of bridge losses for p-n junction half bridge. Diodes operated at 25 W/cm^2 dissipation.

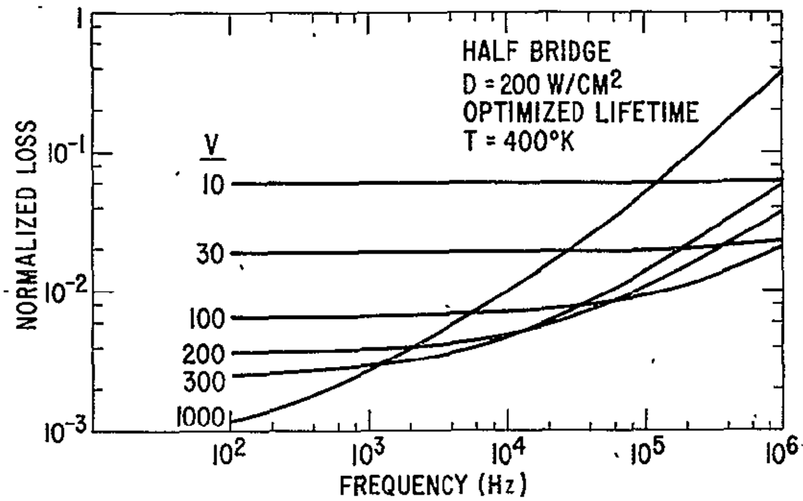

Figure 30. Frequency variation of bridge losses for p-n junction half bridge. Diodes operated at 200 W/cm^2 dissipation.

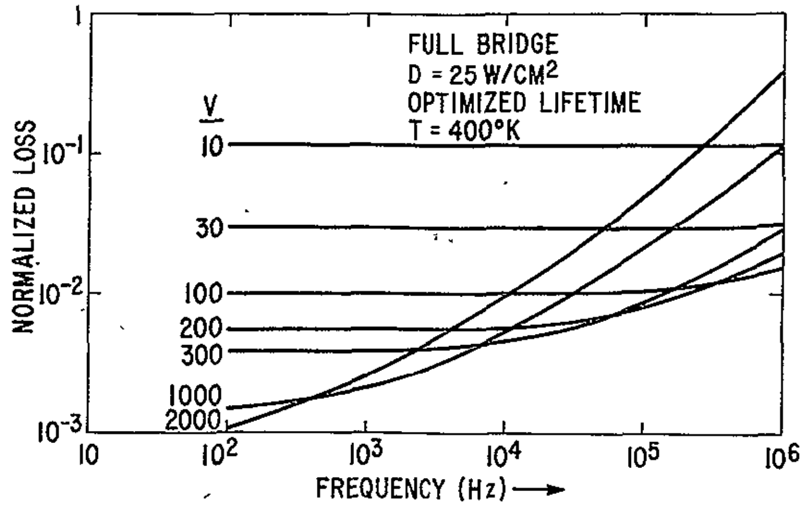

Figure 31. Frequency variation of bridge losses for p-n junction full bridge. Diodes operated at 25 W/cm^2 dissipation.

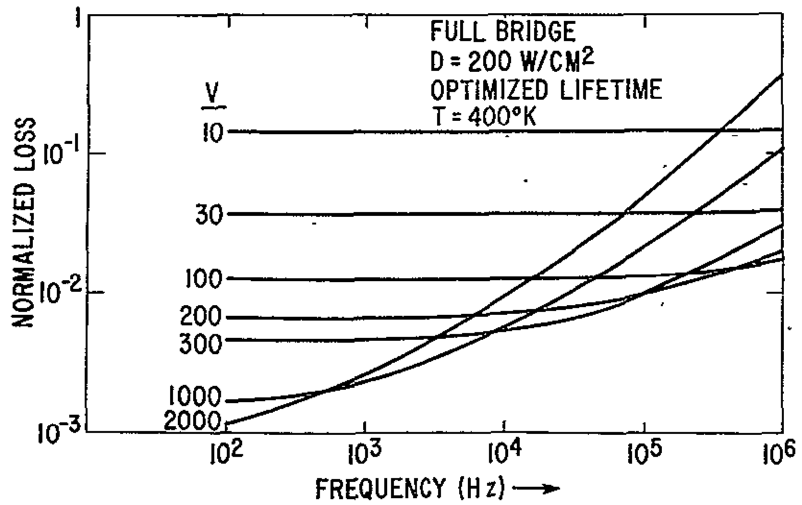

Figure 32. Frequency variation of bridge losses for p-n junction full bridge. Diodes operated at 200 W/cm^2 dissipation.

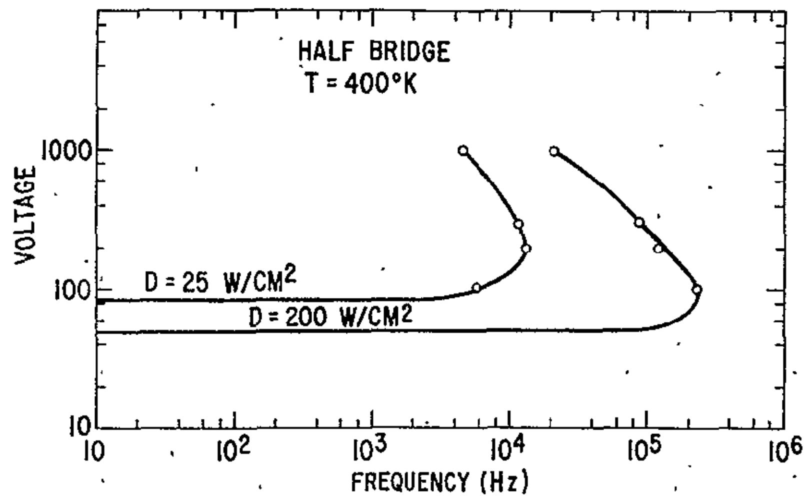

Figure 33. Preferred regions of operation for p-n junction and Schottky diode half bridge circuits

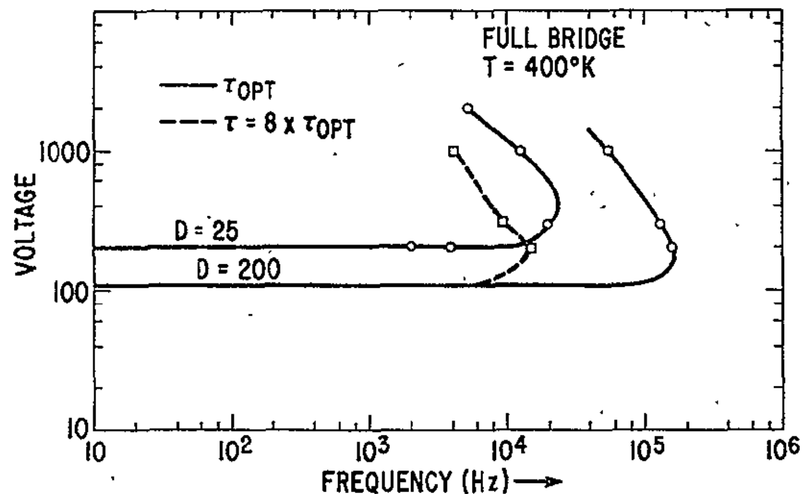

Figure 34. Preferred region of operation for p-n junction and Schottky diode full bridge circuits

while above and to the left the p-n junction minimizes losses. Junction rectifiers with other than optimum lifetimes will have the generally vertical sections of these curves shifted to the left. The case where the junction lifetime is greater than the optimum value by a factor of 8 is shown as the dotted curve of Figure 34.

Section 4

ACQUISITION OF BARRIER DATA

It was shown in Section 3 that a knowledge of barrier parameters is of prime importance in the design of power Schottky diode. Accordingly, one aspect of the program which received a great deal of attention in Phase I was the acquisition of barrier data. These efforts can be conveniently divided into two primary areas: first, the verification of the variation of Schottky barrier height with crystal orientation of the silicon substrate, for several potentially useful barrier materials; and, second, the determination of the magnitude of the barrier lowering under reverse bias for these barrier materials.

4.1 Barrier Height and Quality

As was discussed in Section 2.1, a knowledge of the barrier height, ϕ_b, is of prime importance in describing the performance of a Schottky diode. In addition to this information, a knowledge of the variation of ϕ_b across an area comparable to that of the proposed diode is important. This is especially true for large area, high current devices since those areas with low values of ϕ_b will tend to conduct the highest current density [in accord with Equations (3) and (4)] and this effect could conceivably result in device failure because of localized "burnout." Also of importance is the n value of the contact, since excessively large n values result in excessive forward voltage drops. This section deals with the measurement of these three parameters.

The most reliable (and simplest) method of determining the barrier height was found to be the extrapolation of log I vs. V plot to the origin as detailed in Section 2.2. This procedure also has the advantage that the n value can be determined from the slope of the curve. Typical results are shown in Figure 35 for small area (9.3×10^{-4} cm^2), low temperature PtSi-Si contacts to the three crystal faces investigated, <111>, <110>, and <100>. A computer least squares fitting procedure was employed to determine the n and ϕ_b values shown in the figure. The value of ϕ_b was also checked in a few cases by the reverse capacitance-voltage method, but the precision was found to be far less by this latter method. Measurements of the barrier height were made for Al, W, "conventionally" formed PtSi, and low temperature PtSi contacts to silicon. For the "conventionally" formed PtSi, a 600°C, 20-minute heat treatment in argon was employed to react the Pt and Si subsequent to deposition. The results of the barrier height and n value measurements are summarized in Table II.

4.2 Reproducibility

Table II also shows the results of a number of measurements which were made in order to determine the spread of ϕ_b values across a wafer. The

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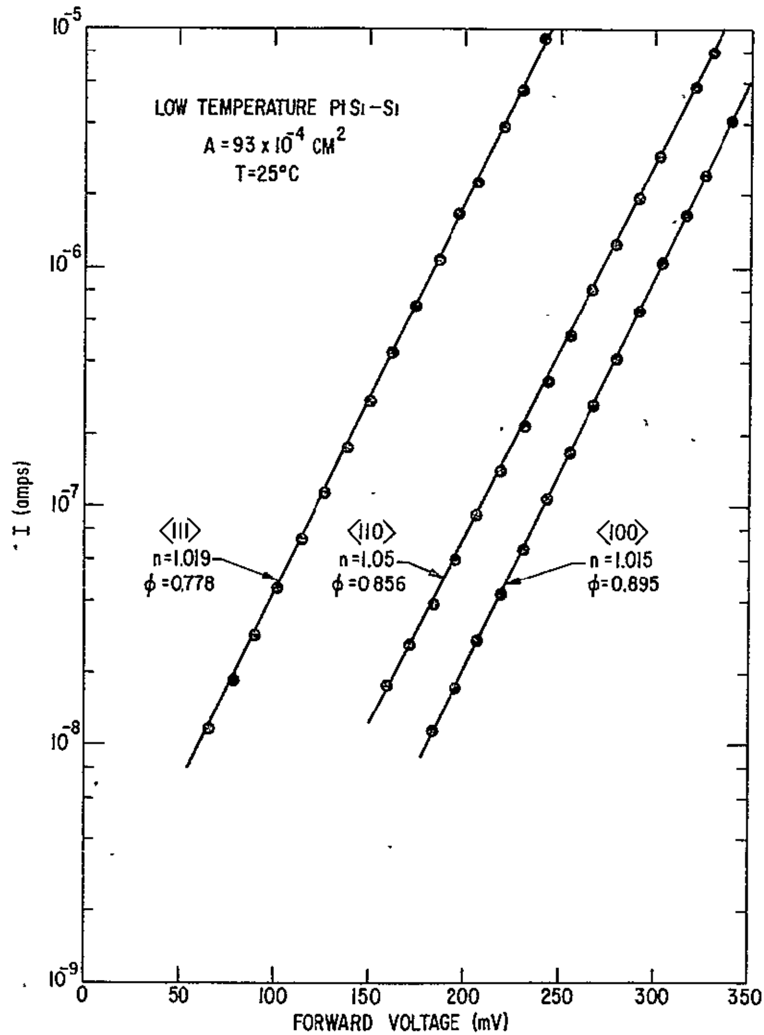

Figure 35. Forward bias current-voltage characteristics of "low temperature" Pt-Si on the three major crystallographic faces of silicon. The effects of crystal faces upon barrier height are evident.

spread was determined by fabricating a number of small ($A = 9 \times 10^{-4}\ cm^2$) Schottky contacts on 0.020-inch centers on a wafer. A constant current source was used to pass a fixed current ($I = 10^{-6}$ amp in this case) through each device and the forward drop across the diode was measured. In the ideal case ($n = 1$, $R = 0$), Equations (3) and (4) show that the variation in forward drop is just equal to the variation in ϕ_b across the wafer provided $V > \sim 3\ kT$. Since R is never zero, the value of I was selected to satisfy the two inequalities,

$$V > 3\ kT$$

$$V \gg IR.$$

TABLE II

BARRIER HEIGHTS, n VALUES, AND FORWARD DROP RANGE FOR SEVERAL CONTACT SYSTEMS

CONTACT MATERIAL	CRYSTAL ORIENTATION	ϕ (eV)	ΔV (volts)	NUMBER OF SAMPLES	TYPICAL n
Al	<100>	.760	±.014	231	1.04
Al	<111>	.732	±.012	530	1.02
Al	<111>	.708	±.008	601	1.04
Al	<110>	.760	±.008	105	1.05
W	<100>	.690	±.018	531	1.05
W	<111>	.688	±.012	623	1.02
W	<110>	.685	±.017	358	1.02
Conv. PtSi	<100>	.871	±.018	217	1.08
Conv. PtSi	<111>	.846	±.016	291	1.08
Conv. PtSi	<110>	.851	±.022	215	1.13
Low PtSi	<100>	.900	±.003*	10	1.02
Low PtSi	<111>	.780	±.002	1750	1.03
Low PtSi	<110>	.856	±.002*	20	1.05

* On account of the small number of samples of these orientations, the ΔV values represent the range of the entire lot, rather than 90% of the samples as for the other entries in the table.

Non-unity n values are still a problem, however, and so the variation in forward drop actually includes both variations in ϕ_b and variations in n and thus represents a "worst case" estimate of the variation in ϕ_b, assuming ϕ_b and n to be essentially independent. This latter assumption was found to be the case for all samples investigated, with the exception of the conventionally formed PtSi contacts where a correlation between high n and low ϕ_b values was observed.

The reason for using this procedure to determine the variation in ϕ_b was that in this case only a single measurement was required, whereas to determine ϕ_b from the I-V characteristic required at least 3 and preferably 10 measurements; thus the time required was greatly reduced. To insure that no systematic error crept into this procedure, however, ϕ_b and n were determed independently for 10 to 20 randomly selected diodes for each of the contact combinations listed in Table II. The ΔV values shown in Table II

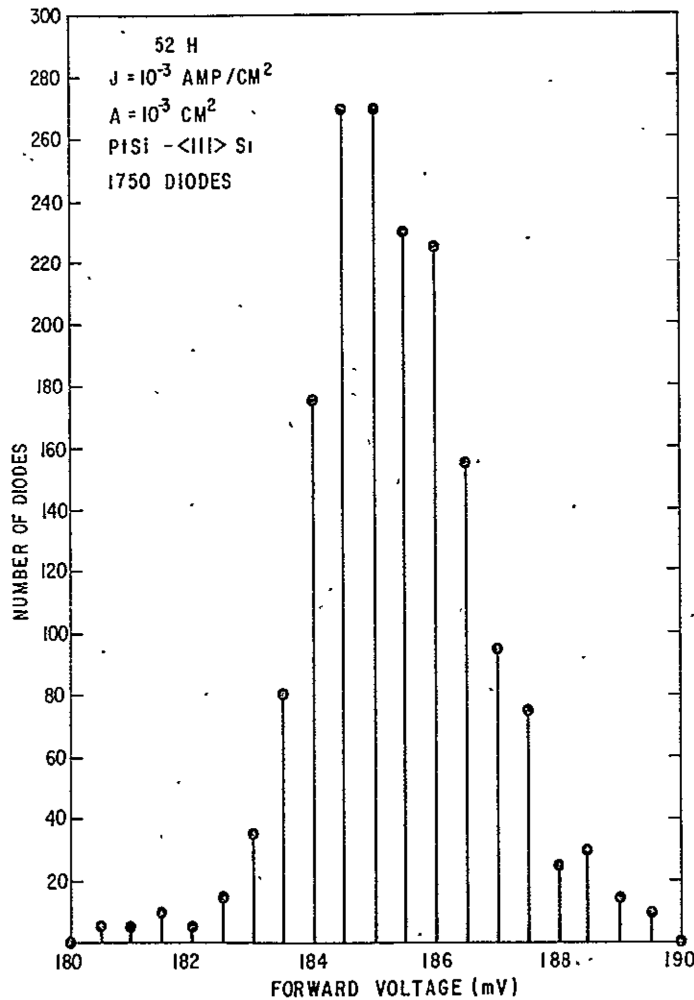

Figure 36. Histogram showing distribution of forward voltages corresponding to a current density of 10^{-3} A/cm^2 for all the diodes on a 1 1/4" wafer

represent the voltage range which included 90% of the samples investigated; the sample size is also listed. The only exceptions to this rule are for the low temperature PtSi contacts to <100> and <110> Si where only a small number of samples were measured and the ΔV values shown represent the range for the entire lot. Although only a small number of samples of low temperature PtSi to <100> or <110> Si were measured, the uniformity of this type of contact is clearly demonstrated by the <111> results where 1750 diodes were measured, representing the spread across an entire 1 1/4-inch diameter wafer. The actual distribution of measured forward voltage drop for the low temperature PtSi-<111> Si case is shown in Figure 36. There is no reason to expect that the variation of barrier height across other crystal faces will be significantly different than that across the <111> face.

It should be noted in Table II that there are two entries for Al - <111> Si contacts; these represent samples from different wafers, which were "sintered" in separate runs. The variation in barrier height from one sample to the other is most probably due to small differences in the actual sintering conditions, and this run to run variation is typical of what was observed in the Al measurements. The "sintering" procedure for the Al samples consisted of heating the sample at ~450°C for 1/2 hour in a reducing atmosphere.

4.3 Barrier Lowering

Equation (5) indicates that barrier lowering is a function of $\mathcal{E}_m$, the electric field at the metal-semiconductor interface. Unfortunately $\mathcal{E}_m$ is not directly measurable, but must be determined from the reverse voltage, V_r, and the net impurity concentration in the semiconductor. Thus a description of barrier lowering requires two essentially independent measurements, the first to determine $\mathcal{E}_m(V_r)$ and the second to determine $\Delta\phi_b(V_r)$. The procedure used in this study was to determine $N_d(X_D)$ and $X_D(V_r)$ by measuring the depletion capacitance of the Schottky barriers as a function of V_r. Here N_d is the net donor concentration at X_D, the depletion length when V_r is applied. $\mathcal{E}_m(V_r)$ can then be determined from

$$\mathcal{E}_m = \mathcal{E}_o + \frac{q}{\epsilon}\int_0^{X_D} N_d(X)dX , \tag{24}$$

where $\mathcal{E}_o$ is the "built-in" field due to the barrier. A typical $\mathcal{E}_m(V_r)$ curve obtained in this manner is shown in Figure 37, for an average net donor concentration of ~8×10^{14} cm^{-3}. Local variations in the net donor concentration, although visible in the $N_d(X)$ data, were too small to appreciably influence this curve and so it retains the parabolic shape ($\mathcal{E} \propto V^{1/2}$) characteristic of a constant value of N_d.

The determination of $\Delta\phi_b(V_r)$ was not as straightforward. A combination of the second and third methods of Section 2.2 for determining $\Delta\phi_b(V_r)$ was used to obtain accurate results.

Consider the equation

$$J_S = AT^2 \exp-(q\phi_b(V_r)/kT). \tag{25}$$

If $\phi_b(V_r)$ is to be determined by varying T (for a fixed V_r) and observing J_S, variations in ϕ_b as a function of T must also be considered. These variations are predominantly due to a variation of the Fermi level with temperature. The variation which is usually assumed is of the form

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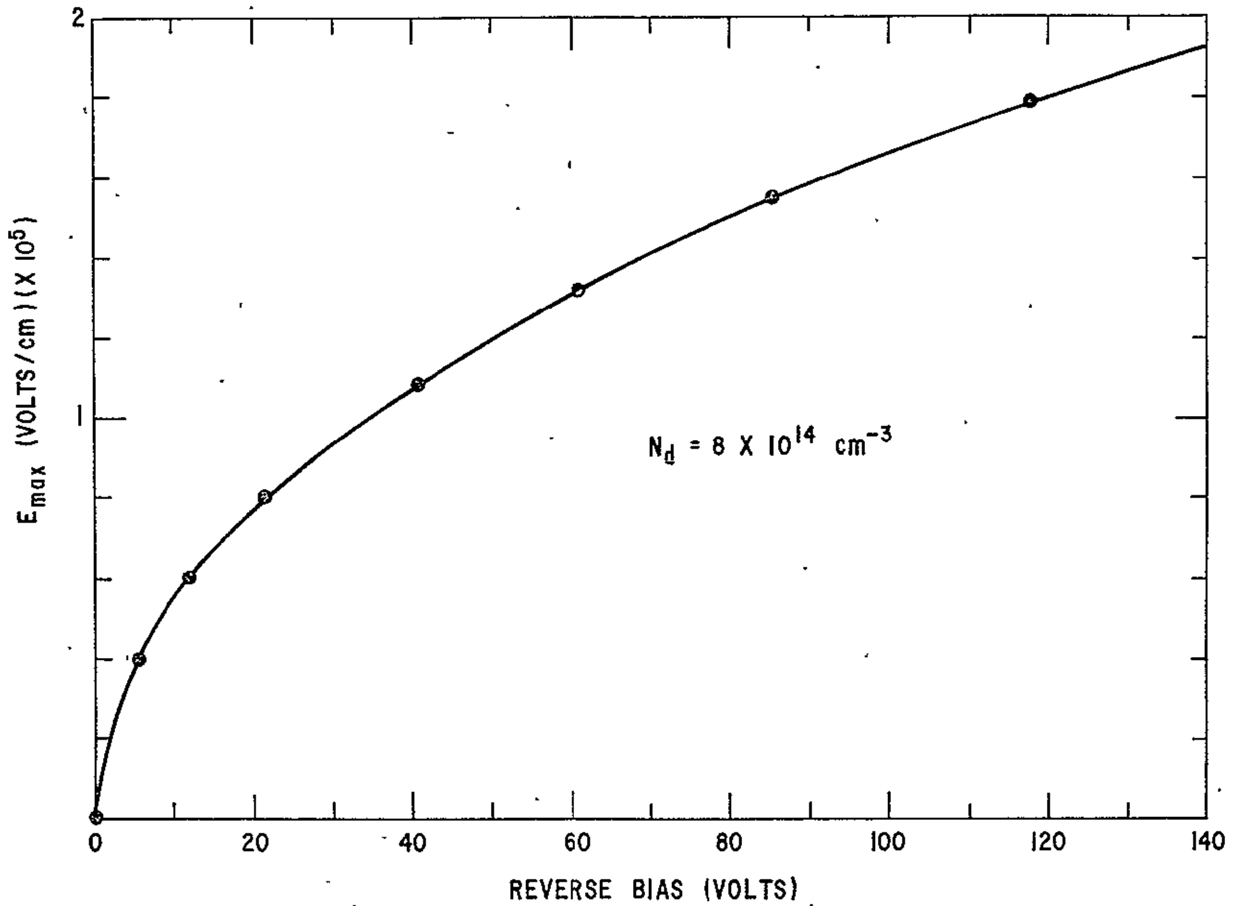

Figure 37. Variation of $\mathcal{E}_m$, the maximum electric field of a reverse biased Schottky diode, with reverse bias. The curve is obtained by stepwise integration of the capacity-voltage data.

$$\phi(V_r, T) = \phi_o(V_r) + \alpha(V_r)\, T, \qquad (26)$$

where

$$\alpha(V_r) = \left.\frac{\partial \phi}{\partial T}\right|_{T = o}$$

Substituting (25) into (26), one obtains

$$J_S = AT^2 \exp\left(-q(\phi_o + \alpha T)/kT\right) \qquad (27)$$

or

$$J_S = AT^2 \exp\left(\frac{-q\alpha}{k}\right) \exp\left(\frac{-q\phi_o}{kT}\right) \qquad (28)$$

Rearranging terms and defining

$$A_{eff} = A \exp\left(\frac{-q\alpha}{k}\right) \qquad (29)$$

one obtains

$$J_S/T^2 = A_{eff} \exp\left(\frac{-q\phi_o}{kT}\right) \qquad (30)$$

or, taking natural logarithms

$$\ln(J_S/T^2) = \ln(A_{eff}) - q\phi_o/kT. \qquad (31)$$

If we assume that all the reverse leakage is due to thermionic emission over the barrier, then the measured current, J_r, is exactly the saturation current, J_S;

$$J_S = J_r. \qquad (32)$$

If a plot is now made of $\ln(J_r/T^2)$ as a function of $1/T$ Equations (31) and (32) show a straight line with slope $-q\phi_o/k$ and intercept (at $1/T = 0$) of $\ln(A_{eff})$. This latter intercept may be used with Equation (29) to give α. Equation (26) may then be used with the value of ϕ_o determined from the slope to calculate ϕ at the given value of V_r and the temperature of interest. This is essentially method 3 of Section 2.2.

In practice, several problems arise when $\Delta\phi$ is determined in this manner. First of all, data are obtained over a relatively small temperature range, typically 25° to 160^oC (298° to 423^oK), corresponding to a $1/T$ range of $\sim 2.4 \times 10^{-3}$ to $\sim 3.4 \times 10^{-3}$. The intercept must thus be determined by extrapolating the curve over approximately 2.5 times the range over which data are available. Any error in this procedure greatly affects the measured value of α. A second problem encountered with this procedure is that it is desirable to measure $\Delta\phi$ with a precision of ± 0.005 eV or better. Our experience was that it was not possible to measure the slope of the curve nearly that precisely; thus the measurement of both ϕ_o and α are in doubt by amounts greater than can be tolerated.

For these reasons we adopted the following procedure. Rather than hold V_r fixed and vary temperature, we kept the temperature fixed and measured J_r as V_r varied. Data were still plotted as before, i.e., $\log J_r/T^2$ versus $1/T$, but now only to insure that a straight line fit did result. If a straight line was obtained, the assumption that all the current is due to thermionic emission over the barrier is probably valid. We then used Equation (25) to determine ϕ_b.

Reverse bias I-V data were taken at various fixed values of junction temperature. The temperature was kept fixed to better than 0.1°C throughout the course of measurement of each of the I-V characteristics. The "true" absolute junction temperature cannot, of course, be measured directly. There may well be differences between it and our measured thermocouple values due to calibration errors and the effects of heat flow. These types of discrepancy are quite difficult to identify in detail and correct for. It is far easier to hold a fixed temperature than to know its precise value. We estimate that our measured temperatures are correct to 0.5°C. Nevertheless, this uncertainty does not affect in any serious way a determination of $\Delta\phi_b(V_r)$ from Equation (25) when T is held fixed and V_r is varied.

This result is easily obtained from Equation (25). The barrier at no reverse bias is given by

$$\phi_b(0) = \frac{kT}{q} \ln \frac{J_S(0)}{AT^2} \tag{33}$$

and that at some value of reverse bias, V_r, is

$$\phi_b(V_r) = \frac{kT}{q} \ln \frac{J_S(V_r)}{AT^2} . \tag{34}$$

When the procedure just described is followed the two values of "true" junction temperature are the same even though they may deviate from the measured values. A simple subtraction gives us

$$\Delta\phi(V_r) = \phi_b(0) - \phi_b(V_r) = \frac{kT}{q} \left[\ln \frac{J_S(0)}{AT^2} - \ln \frac{J_S(V_r)}{AT^2} \right] \tag{35}$$

Any error in temperature, δT, now contributes, in linear fashion, a corresponding error in $\Delta\phi(V_r)$

$$\frac{\delta\Delta\phi}{\Delta\phi} = \frac{\delta T}{T} . \tag{36}$$

Thus, our 1 percent knowledge of temperature yields a 1 percent measurement of barrier lowering due to electric field. In this manner, the entire $\phi_b(\mathcal{E}_m)$ curve could be obtained.

A typical reverse current vs. voltage curve (with temperature as the parameter) is shown in Figure 38. The particular data shown are for a W-<111> Si contact ($A = 9.3 \times 10^{-4}$ cm^2, $N_d = 8 \times 10^{14}$ cm^{-3}). Figure 39 is a plot of log J_r/T^2 vs. $1/T$ for a field of 1×10^5 v/cm. For this sample, a

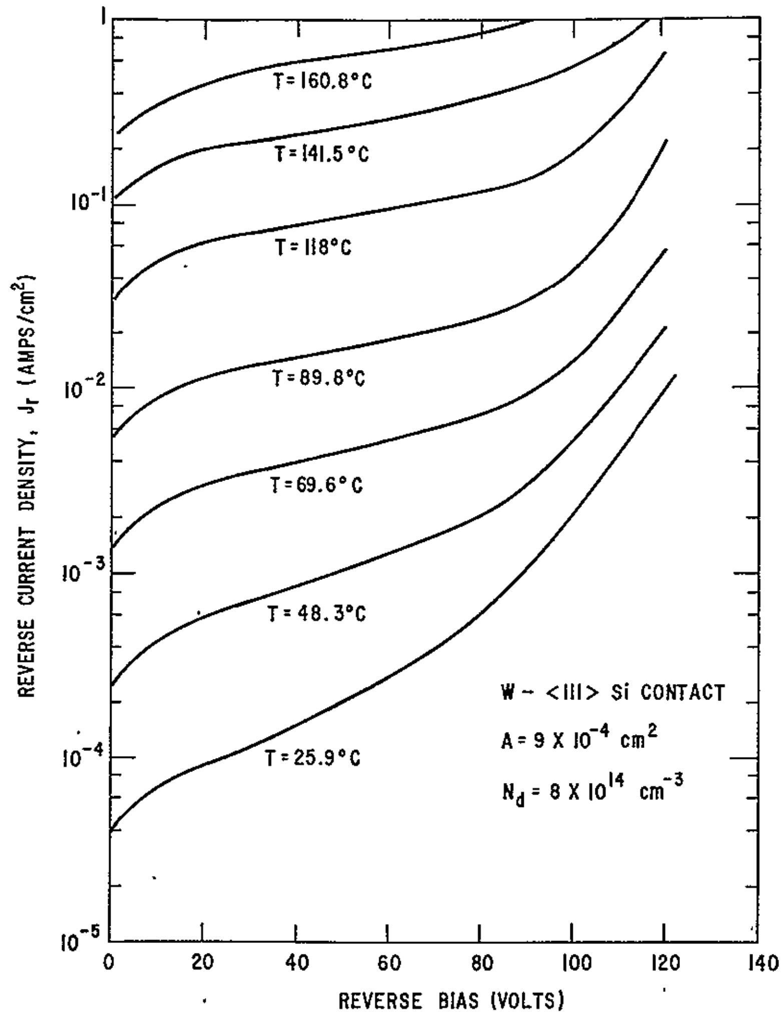

Figure 38. Typical set of data used to determine the effects of reverse bias upon barrier height

reverse bias of 34 volts was required to produce this field at the contact. It should be noted that in this case an excellent fit is obtained and one can be confident that the reverse current is predominantly due to thermionic current over the barrier. Such was not always the case, however, as is illustrated by the results shown in Figure 40. These results were obtained from a low temperature PtSi-<111>Si contact; the three curves were obtained at reverse biases of 10, 70, and 140 volts, corresponding to electric fields of 7×10^4, 1.6×10^5, and 2.2×10^5 v/cm, respectively. It should be noted that while the data for the two lower values of field give a good fit, the data for the highest field show a systematic deviation from a straight line, which is most evident at lower temperatures. It appears that an extra component of leakage current was present in this sample; thus data obtained from this sample for fields in excess of 1.6×10^5 volts/cm were suspect and were not used to generate the $\phi_b(\mathcal{E}_m)$ curves. Whenever a deviation from a straight line fit

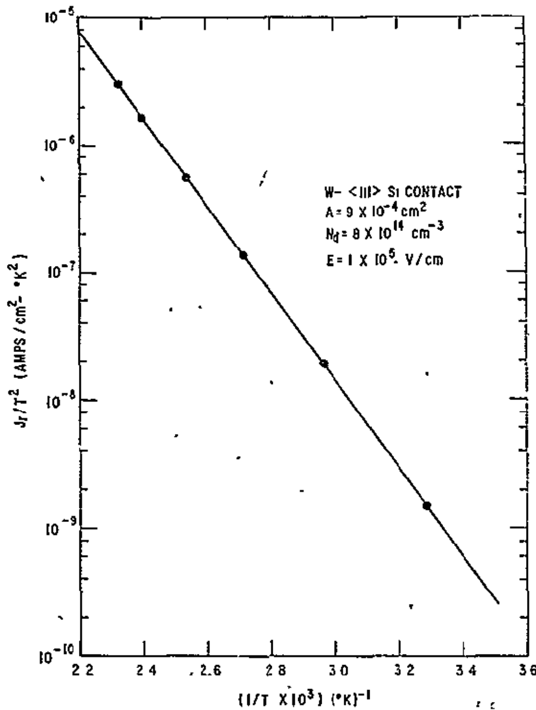

Figure 39. Typical plot of log (J_rT^2) vs. T^{-1} used to verify the assumption that the measured values of J_r, the reverse current, are indeed thermionic. The data for this curve are the same as those of Figure 38 at reverse bias corresponding to E_{max} = 1 x 10^5 volt/cm.

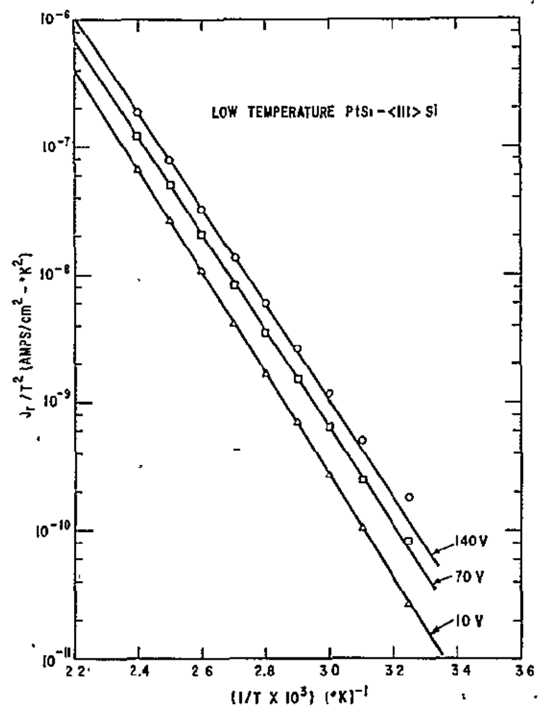

Figure 40. Variation of log (J_r/T^2) vs. T^{-1} for three different values of reverse bias ($\mathcal{E}_m$).

was observed, it was always in the manner shown in Figure 40, i.e., it was always an "excess" current, which was most evident at low temperatures and high fields.

The results of the barrier lowering measurements are presented in Figures 41 through 47, for W, Al, and low temperature PtSi contacts. In each case, the zero field barrier value is that which was obtained from the forward I-V characteristic of the diode; the fact that most of the curves join smoothly to this point is a further argument that the measurement procedure was valid. The curves are all similar; they show an upward curvature at low fields followed by a linear decrease in barrier height with electric field at the higher values of field, which is consistent with the prediction of Equation (5).

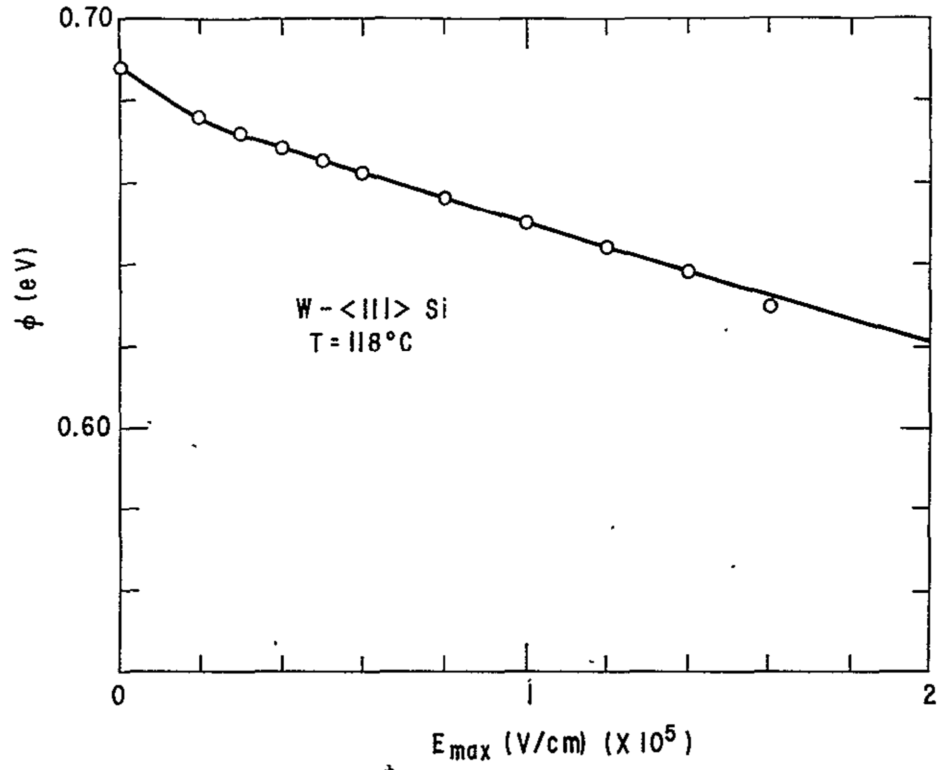

Figure 41. Reverse bias lowering of the tungsten barrier on <100> silicon at 110°C

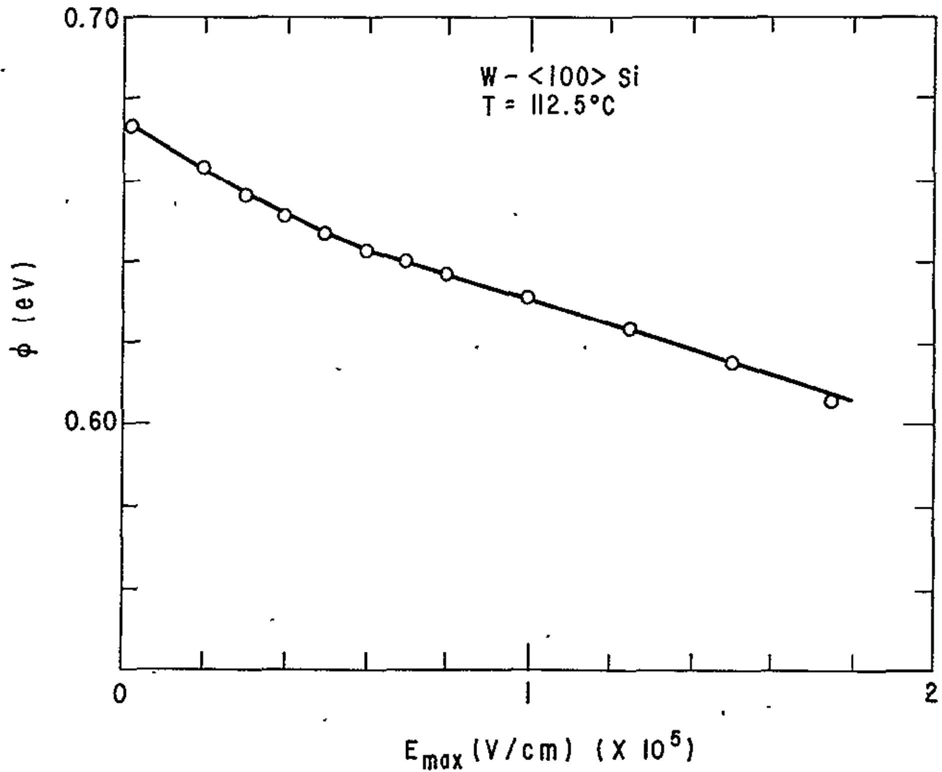

Figure 42. Reverse bias lowering of the tungsten barrier upon <111> Si at 120°C

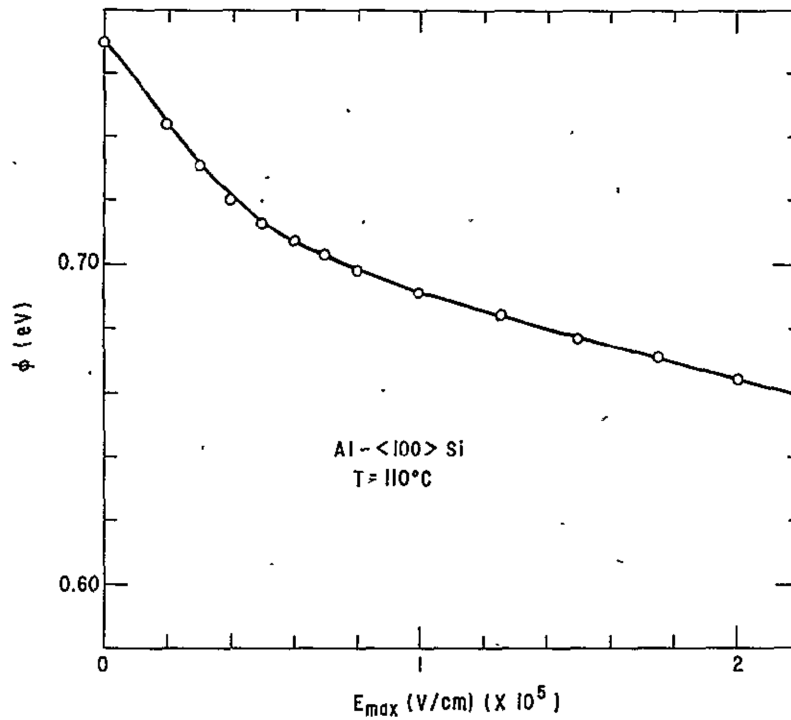

Figure 43. Reverse bias lowering of the aluminum barrier upon <100>Si at 110°C

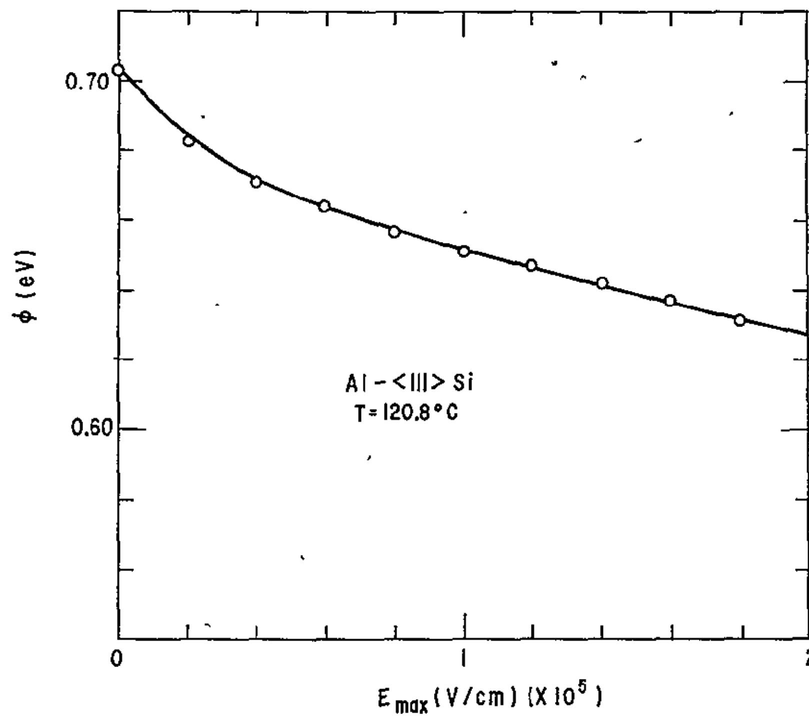

Figure 44. Reverse bias lowering of the Al barrier upon <111> Si at 120°C

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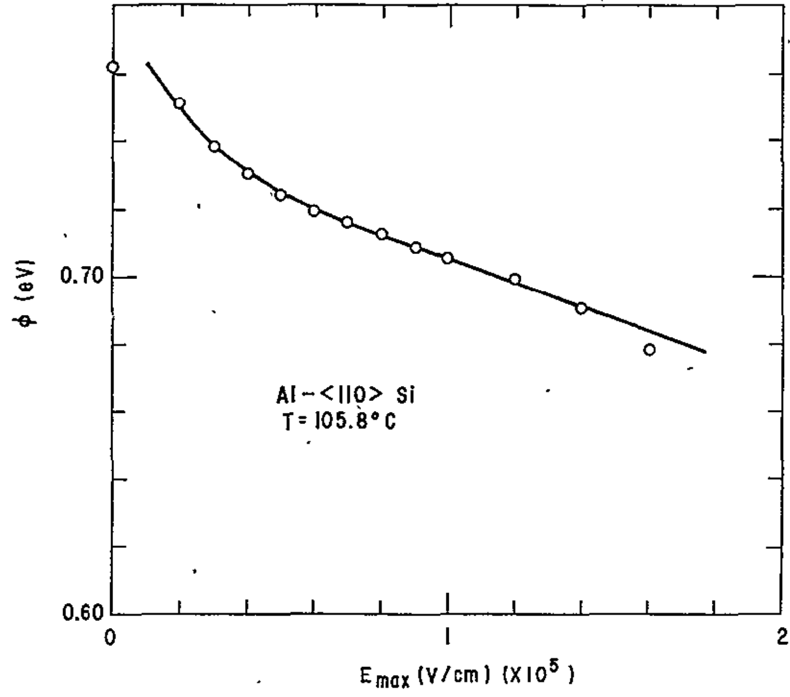

Figure 45. Reverse bias lowering of the aluminum barrier upon <110> Si at 110°C

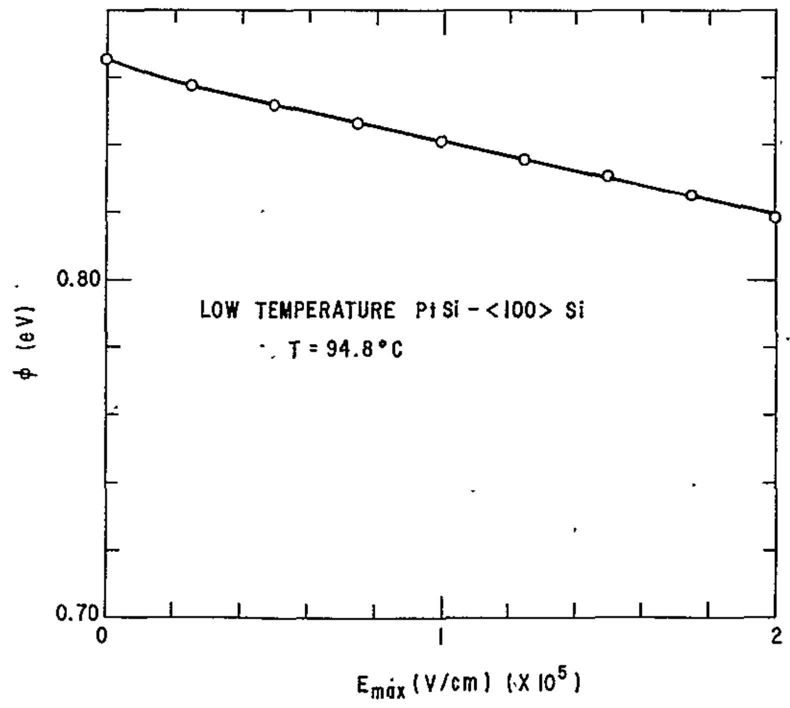

Figure 46. Reverse bias lowering of the low temperature Pt-Si barrier upon <100> Si at 95°C

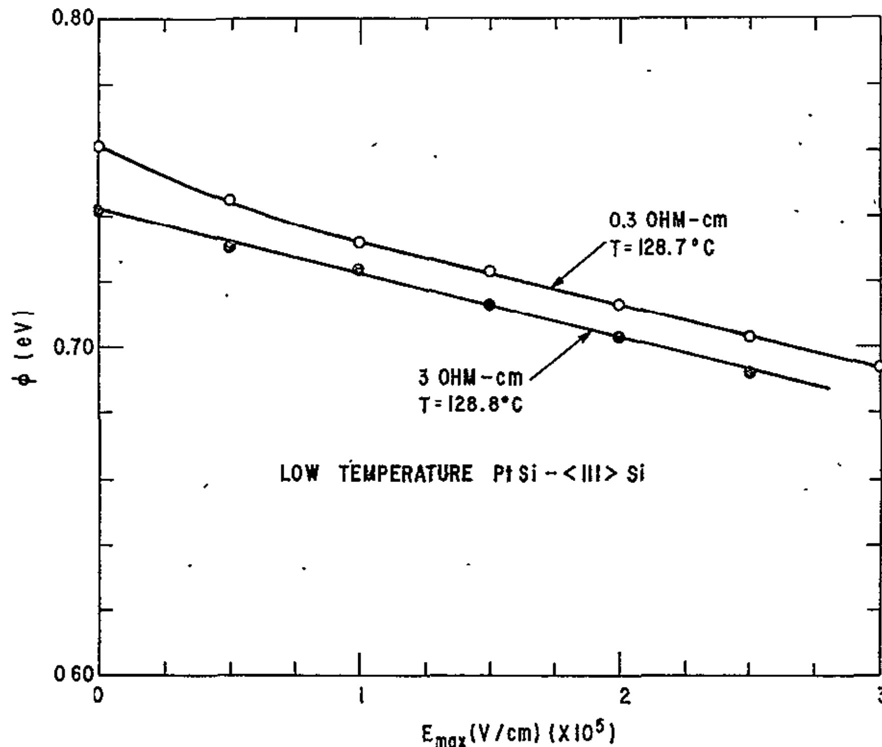

Figure 47. Reverse bias lowering of the low temperature Pt-Si barrier upon <111>Si at 130°C for two different resistivity substrates

Figure 47 shows the barrier lowering for low temperature PtSi - <111> Si contacts for two different Si resistivities, 0.3 and 3 ohm-cm. The fact that the curves are essentially parallel demonstrates that the barrier lowering does depend on field rather than applied voltage. For example, at a field of 3.0×10^5 volts/cm, the applied voltage in the 3 ohm-cm case is 125 volts while for the 0.3 ohm-cm device it is only 40 volts (the difference in the two curves arises principally from the difference in the zero field barrier height). Thus a single curve can be used for design purposes, and the barrier lowering at a given voltage can be determined from the voltage and Si resistivity. The curves given in Figures 41 through 47 were obtained at the temperatures shown, all near 100°C. Since most power rectifiers will operate at or near this temperature, the curves should provide the necessary information for estimating the reverse leakage current of any potential W, Al, or PtSi Schottky diode. The data shown in Figure 47 were used to estimate the reverse leakage for the large area diodes discussed in Section 5.

Section 5

DIODE DESIGN

5.1 Ideal Forward Specifications (Phase II Diode)

Let us first consider the forward specifications. All calculations in this section will be based on Equations (3), (4), and (5) of Section 2.1. A value of $A = 120$ amp/cm^2 will be used throughout and the barrier parameters used will be those of Table I. In Figure 48 we have plotted a number of diode voltage drop curves as a function of the diode area. The curve labeled "barrier drop" is the required barrier voltage to produce a current of 25 A at 25°C assuming a low temperature PtSi - <111> Si Schottky contact. In order to calculate the series resistance of the epitaxial Si layer, we assume the geometry to be that of a mesa structure. For this case we may use the curves of Figure 3 (plane junction curve) to determine the maximum donor concentration which will support 100V and 200V. The values are 5×10^{15} cm^{-3} and

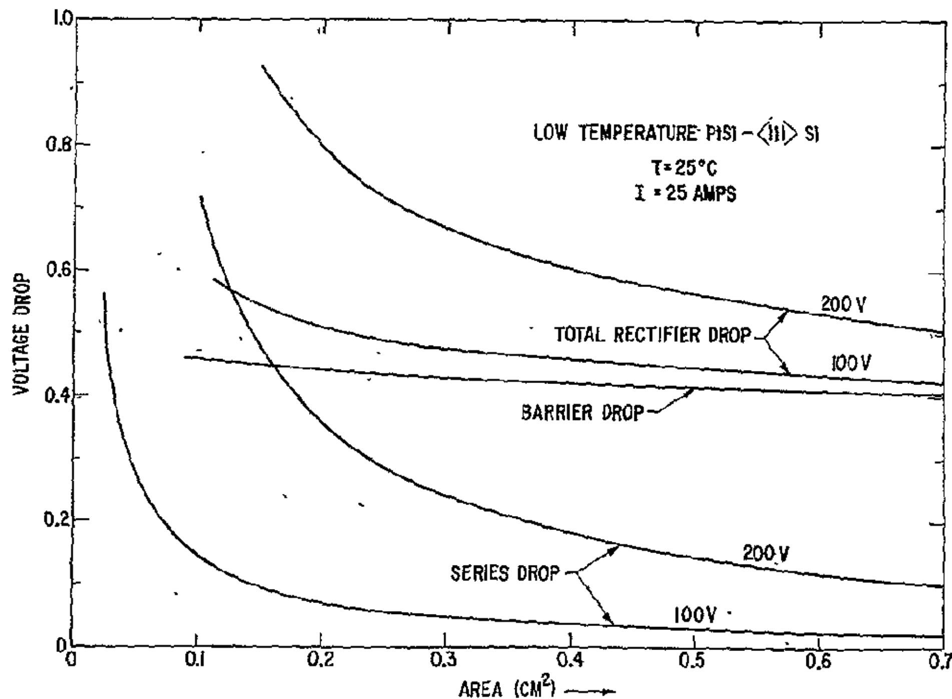

Figure 48. Ideal design curves for a 25 A mesa Schottky diode for both 100 and 200 volt breakdown. It is assumed that avalanche breakdown will occur at the theoretical maximum, the microplasma free bulk avalanche value.

2×10^{15} cm^{-3}, respectively, and the corresponding resistivities are 1.1 Ω-cm and 2.5 Ω-cm. The required epitaxial thickness for the mesa geometry is just equal to the depletion width; for the 100V device this is 5.1μ and for the 200V device the required thickness is 12μ. The corresponding volt-drop in the silicon is then given by $V = J\rho\ t$ where J is the required current density, ρ is the epitaxial resistivity, and t is the epitaxial thickness. These results are plotted in the curves labeled "series drop" for the two cases in question. The curves labeled "total rectifier drop" are the respective sums of the barrier drop and the series drop. If we ignore the contact losses, we see that the minimum area possible which will allow us to meet the new forward specification goals is 0.22 cm^2 for the 100V device and 0.4 cm^2 for the 200V device. If we assume that the packaging losses add 0.04 to 0.05 volt, the new minimum required area becomes 0.4 cm^2 for the 100V device and 0.55 cm^2 for the 200V device.

Similar total rectifier drop curves for other choices of contact material or crystal orientation are easily obtained from Figure 48. The parasitic series drop is independent of barrier since it depends only upon reverse blocking capability. The barrier drop, however, is linear in barrier height. Total rectifier drop for other barriers are thus obtained by merely shifting the <111> PtSi curve vertically by the appropriate amount.

5.2 Practical Forward Specifications (Phase III Diode)

It is not realistic to design on the basis that one will achieve the full theoretical maximum breakdown voltage for bulk material. In practice, realistically obtainable reverse breakdown values will be limited to some fraction, f, of the theoretical bulk value. Proper design procedure takes this into account. We present in Figure 49 a recalculation of the forward drops for the 100 volt 50 amp diode of the Phase III effort. Several curves are given for the total diode forward voltage at 50 A (including the ohmic drop) corresponding to values of f ranging from 0.5 to 1, the ideal case. As f decreases from 1 the series resistance increases, dominating the forward drop; even for the 100 volt device at practical current densities of 100 A/cm^2 for values of f less than 0.5.

The Phase III diode was designed assuming that we would be able to achieve $f = 0.8$. The diode area was chosen at 0.6 cm^2 giving the following forward characteristics: (a) barrier drop of 0.48 volt, (b) ohmic drop of 0.10 volt and power dissipation of 30 $watt/cm^2$.

5.3 Reverse Specifications

We now calculate reverse leakage currents at breakdown and 100°C to determine whether reverse goals are attainable with devices of area large enough to meet forward requirements.

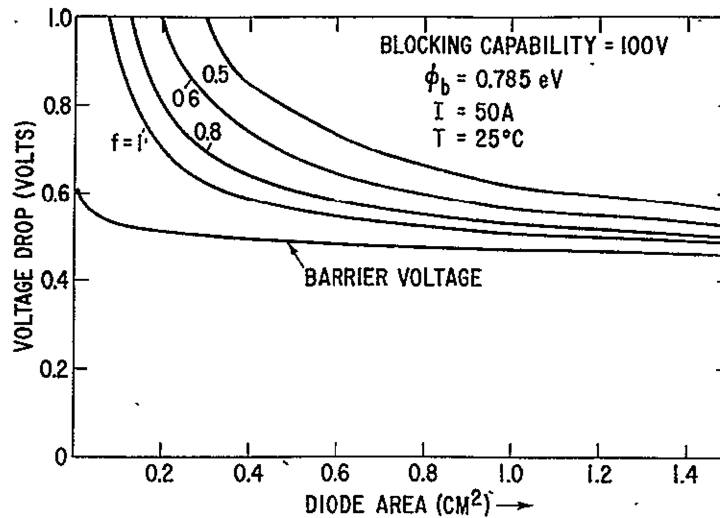

Figure 49. Practical design curves for a 50 A 100 volt, mesa Schottky diode. Values of f, the fraction of the theoretically maximum voltage that is achieved, down to 0.5 are shown.

Barrier heights at 100°C and $\mathcal{E}_m = 3 \times 10^5$ volts/cm are presented in Table III for Al, W, and low temperature PtSi. These values were obtained from the data of Section 3.3. Table III also gives the reverse leakage current density corresponding to thermionic emission at 100°C over these field lowered barriers. The field chosen, 3×10^5 v/cm, is the maximum field that can be sustained by silicon at $N_D \cong 10^{15}$. This value varies very slowly with doping and since $\Delta\phi_b$ depends only upon electric field and not voltage, the values of leakage current density listed in Table II are applicable to diodes of any voltage rating.

We see from Table III and Figure 48 that a low temperature Pt-Si barrier on <111> silicon is the most desirable choice for meeting the Phase II contract specifications for the 200 volt device. Selecting a junction area of 0.6 cm^2 ideally yields a forward drop of 0.52 volt and reverse leakage of 6.6 ma. A choice of tungsten as the barrier metal allows one to go to 0.25 cm^2 and still keep to 0.6 volt forward for the 200 volt device. This decrease in size, however, is not enough to reduce the reverse current to acceptable levels. The leakage for a tungsten diode made on <100> material is 85 ma and on <111> silicon it is 44 ma. Aluminum devices meeting the specifications are also ideally possible. We did not pursue this approach, however, as the aluminum-silicon interface is metallurgically unstable. There is a substantial literature on the migration of silicon onto the aluminum metallizations of integrated circuits. This problem is apt to be even more serious in power devices which are normally run at elevated temperatures. We thus selected low temperature Pt-Si on <111> Si as the barrier material and the mesa geometry as the device structure for Schottky diode fabrication.

TABLE III

BARRIER HEIGHT AND REVERSE THERMIONIC CURRENT AT 100°C AND JUNCTION FIELD OF 3 x 10^5 v/cm

Contact Material	Crystal Orientation	ϕ (volts)	$J_s \frac{ma}{cm^2}$
Al	<100>	0.636	42
Al	<111>	.602	120
Al	<110>	.636	42
W	<100>	.570	330
W	<111>	.591	175
Low temp Pt-Si	<100>	.798	0.27
Low temp Pt-Si	<111>	.680	11

The design of the Phase III diode took account of the assumption that the theoretical maximum in reverse breakdown voltage would not be reached. The value f = .8 corresponds to a barrier lowering of only 63 mv rather than the 95 mv for the ideal case. Accordingly, the design value for reverse leakage for the Phase III Pt-Si diode at 100°C was 2.1 ma.

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Section 6

WAFER PROCESSING

Conventional planar processing procedures are inadequate to fabricate high-voltage structures because of field crowding, as was discussed in the Introductory Technical Discussion. The basic structure chosen in order to meet the reverse voltage requirements was a mesa structure. Diode fabrication proceeded as follows:

6.1 Epitaxial Growth

N type silicon is grown epitaxially upon heavily doped n+ substrates. Resistivity ranges covered were 1 to 4 Ω-cm and thicknesses of growth varied from 10μ to 15μ. The specific design objectives for the 200 volt rectifier were 2.5Ω-cm resistivity and 12μ final thickness. Epitaxial silicon of 1.9 Ω-cm resistivity was grown 7 microns thick for the 100 volt rectifier.

6.2 Initial Oxidation

A 700Å thick layer of SiO_2 is next grown upon the epitaxial layer. This is necessary so as to prevent slip from occurring in the wafer when the wafer which is next coated with Si_3N_4 is subsequently heated to temperatures greater than 1000°C.

6.3 Si_3N_4 Deposition

The wafer is next coated with a Si_3N_4 layer 1300Å thick. This Si_3N_4 layer provides the masking material for later mesa diode definition.

6.4 SiO_2 Deposition

Six thousand angstroms of SiO_2 are next deposited in order to serve as a transfer mask material for patterning of the Si_3N_4. This is necessary since the usual photoresists will not stand up to the hot phosphoric acid etch necessary to pattern silicon nitride. This SiO_2 also serves as a protective coat for the silicon nitride layer preventing it from being attacked by the phosphorus-rich oxidizing atmosphere that we next use to getter impurities from the wafer.

6.5 Getter Cycle

At an early stage in our development program we learned that it was necessary to introduce an explicit gettering step in the device processing

sequence even though in principle it should not be required. In practice, epitaxial material, while varying widely, contains substantial amounts of deep-level impurity centers. These act as generation centers which, if not removed from the device structure, produce excessive leakage in reverse bias. Even worse is the interaction of these deep level impurities with crystalline defects and interfaces in the silicon. Heavy metal impurities may precipitate out upon vacancy clusters, dislocation lines, and stacking faults. This leads to geometric local electric field enhancement and thus to breakdown under reverse bias occurring at prematurely low voltage levels.

These problems are more serious in Schottky devices than in p-n junction devices. There are no boron-rich or phosphorus-rich silica glasses which are normally incidentally formed in the course of Schottky diode fabrication as is the case for p-n junction formation. These glasses are well known in the industry to be getters for metals such as Cu, Fe, and Au although detailed knowledge of gettering mechanisms is not available and scientific studies are only recently beginning to be made. Junction devices thus have the benefit of a measure of heavy metal gettering which occurs in an inadvertent, incidental way during the course of their fabrication. Notwithstanding this, it is often necessary to do a final explicit getter diffusion cycle, usually taking the form of a very heavy phosphorus surface diffusion.

The getter cycle used in our Schottky diode fabrication is similar to those used in junction device preparation. It was not possible in the course of this work to do a detailed study of gettering. Our approach, instead, was strictly a utilitarian one. We wanted only to find a cycle which worked and allowed us to fabricate Schottky diodes whose breakdown voltages approached bulk planar values and where generation current was not excessive. We developed a cycle which indeed worked not only upon the lot of epitaxial material used in its definition – but also upon selected other lots of epitaxial material obtained from at least two other sources. There was, however, some epitaxial material for which our cycle simply didn't work. We believe that the reasons for this failure are connected with inferior crystalline quality of this latter material.

The wafers next had the 700Å thermal oxide removed from the back surface and were put through our getter cycle. Wafers were preheated in nitrogen for 5 minutes. Next they were exposed to a vapor stream containing N_2, O_2, and $POCl_3$ for 30 minutes. The quantities used in diode formation were 1000 cc/min, 90 cc/min, and 3 cc/min, respectively, flowing through a tube 63 mm in diameter. At the end of the 30 min the $POCl_3$ was shut off while the N_2 and O_2 continued for 5 more minutes. O_2 was next shut off and the furnace was flushed with pure N_2 for 5 minutes longer after which the samples were removed. The furnace temperature was in all cases 1040°C.

This procedure grows an oxide glass approximately 1500Å thick upon silicon and gives a "predep" having sheet resistance of about 3 to 4 Ω/□ with

phosphorus depth as obtained from p-type test wafers of 1μ to 2μ. The glass as formed on polished surfaces is clear and there is no sign of attack of the original silicon surface.

We arrived at these specifics after a series of experiments performed upon polished p-type $1\,\Omega$-cm test wafers. The oxygen and $POCl_3$ concentrations were varied in order to determine the maximum phosphorus concentration which could be achieved in both glass and silicon without doing gross damage to the silicon surface. We were guided in this effort by the attitude that the more heavily doped was the phosphorus glass the more effective would it be in gettering heavy metals. Figure 50 shows the quantity ρx_j, the product of sheet resistance and junction depth, for various flow rates of carrier N_2 gas through liquid $POCl_3$ kept at both 0^oC and room temperature for two different oxygen concentrations. The surface concentration obviously saturates near the value of $6 \times 10^{-4}\,\Omega$-cm which corresponds to a surface concentration greater than 5×10^{20} phosphorus per cm^3. Throughout the entire range of Figure 50 there is no gross attack of the Si surface.

This "predep" cycle was followed by a long slow cooling in O_2 to approximately 250^oC, after which the wafers are quickly brought to room temperature. Figure 51 shows the time-temperature cycle.

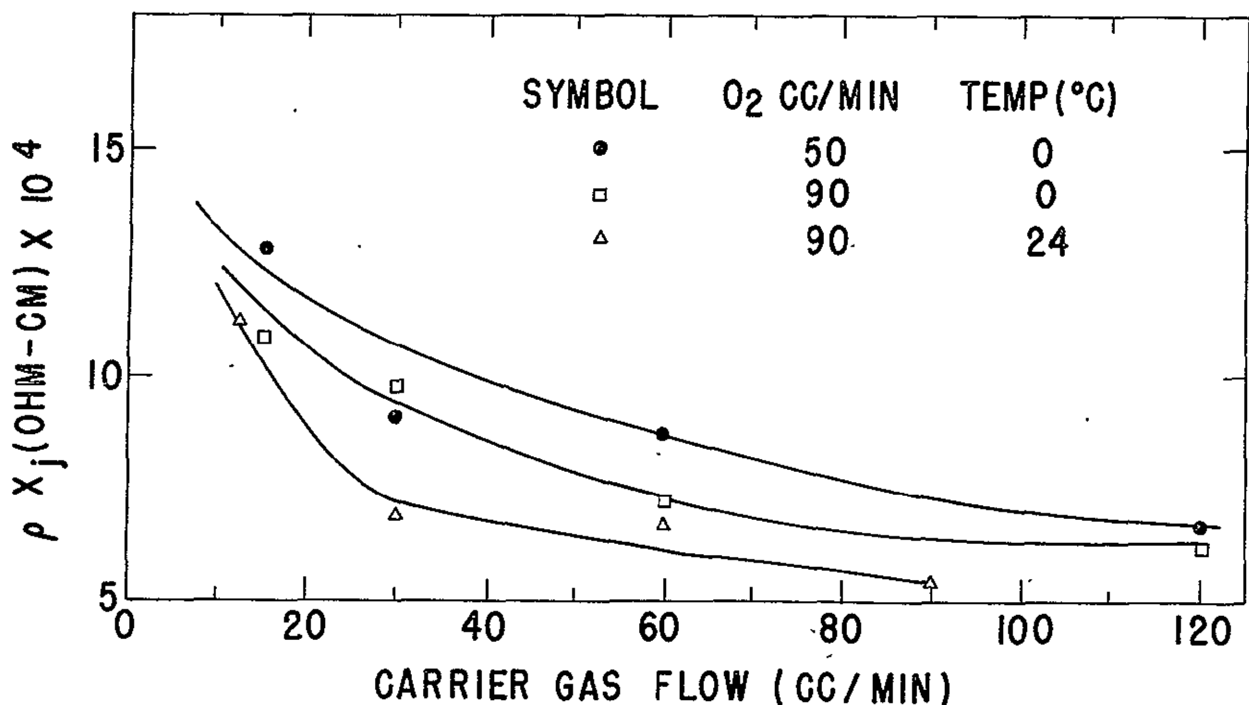

Figure 50. Product of junction depth and sheet resistance for several different gettering conditions

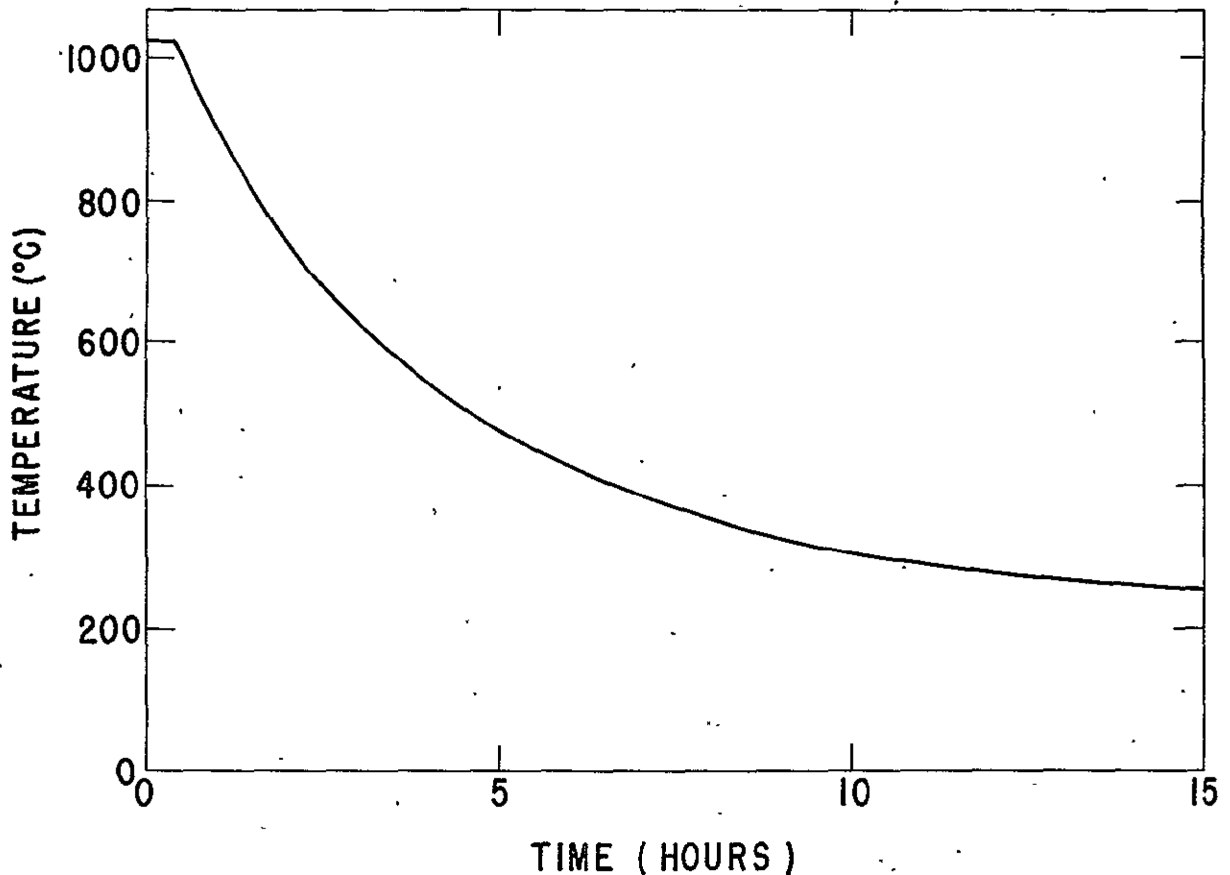

Figure 51. Temperature-time profile of slow cool cycle

6.6 Mesa Definition

The next step is to pattern the Si_3N_4 film using standard photolithographic techniques. Photoresist covers the wafer in those areas where the barrier is to be formed and which will eventually comprise the Schottky diode. The patterning oxide is etched in the usual buffered HF, the photoresist is removed by means of a hot (200°C) H_2SO_4 immersion, and the silicon nitride is etched away in hot (180°C) H_3PO_4. We found it desirable to remove the photoresist before the Si_3N_4 etch to maintain cleanliness. At this point, Si_3N_4 remains on the wafer in those areas which will end up as mesa Schottky diodes.

6.7 Mesa Formation

We investigated two methods of mesa formation; oxide etching and acid etching. In the former a 2μ layer of SiO_2 is grown upon the exposed Si areas by means of a high-temperature long steam oxidation. This layer is then removed by a buffered HF etch. The oxidation rate of Si_3N_4 is very slow as compared with that of Si and a layer of Si_3N_4 1500Å is adequate to prevent the Si underneath it from being oxidized. The thickness of Si removed is 40 per-

cent of the oxide thickness, so this procedure gives a mesa 8000Å high. The second method was simply to etch the Si_3N_4 patterned wafers in an acid bath containing HF and HNO_3 in the ratios 1:20. In this case too, the Si_3N_4 is essentially not attacked by the etch and protects the silicon lying beneath it. The unprotected Si, however, is attacked by this etch. This etch is slow (~2 μ/min) and not selective so a smooth surface is obtained. Etch times were chosen to etch down through the epitaxy.

We found no advantage to the oxide etch over the acid etch, and since it took longer and required thicker Si_3N_4 layers we dropped it after satisfying ourselves that the acid etch procedure worked.

6.8 Passivation

Following the mesa formation, a passivating oxide approximately 5000 Å thick is grown upon the mesa sides. This is done by means of a 3.5 hour wet oxidation at 1000°C followed by a 1 hour 1000°C argon anneal.

We performed a limited study of the effects of different oxidation and annealing conditions for the cases of arsenic and phosphorus doped epitaxy. Breakdown voltages were measured for a series of three arsenic doped and three phosphorus doped wafers. The mesa passivation was formed in one of three ways: (1) wet oxidation, (2) dry oxidation and argon anneal or (3) wet oxidation and argon anneal. The annealing and oxidations were all performed at 1000°C. The function of the anneal is to reduce the stored positive charge density in the oxide and at the Si-SiO_2 interface to the lowest possible value. The results obtained are shown in Figure 52 and are summarized in Table IV.

TABLE IV

PASSIVATION PROCESS VARIATIONS

Dopant	Wafer No.	Processing	No. of Diodes	Peak of Dist.	Width of Dist.
Arsenic	201-1	Wet oxidation	952	84	30
"	201-2	Wet oxidation + argon anneal	1002	12	Dribbles to 110 volts
"	201-4	Dry oxidation + argon anneal	982	96	20
Phos.	202-2	Wet oxidation	756	70	20
"	202-3	Wet oxidation + argon anneal	1088	114	20
"	202-4	Dry oxidation + argon anneal	974	78	40

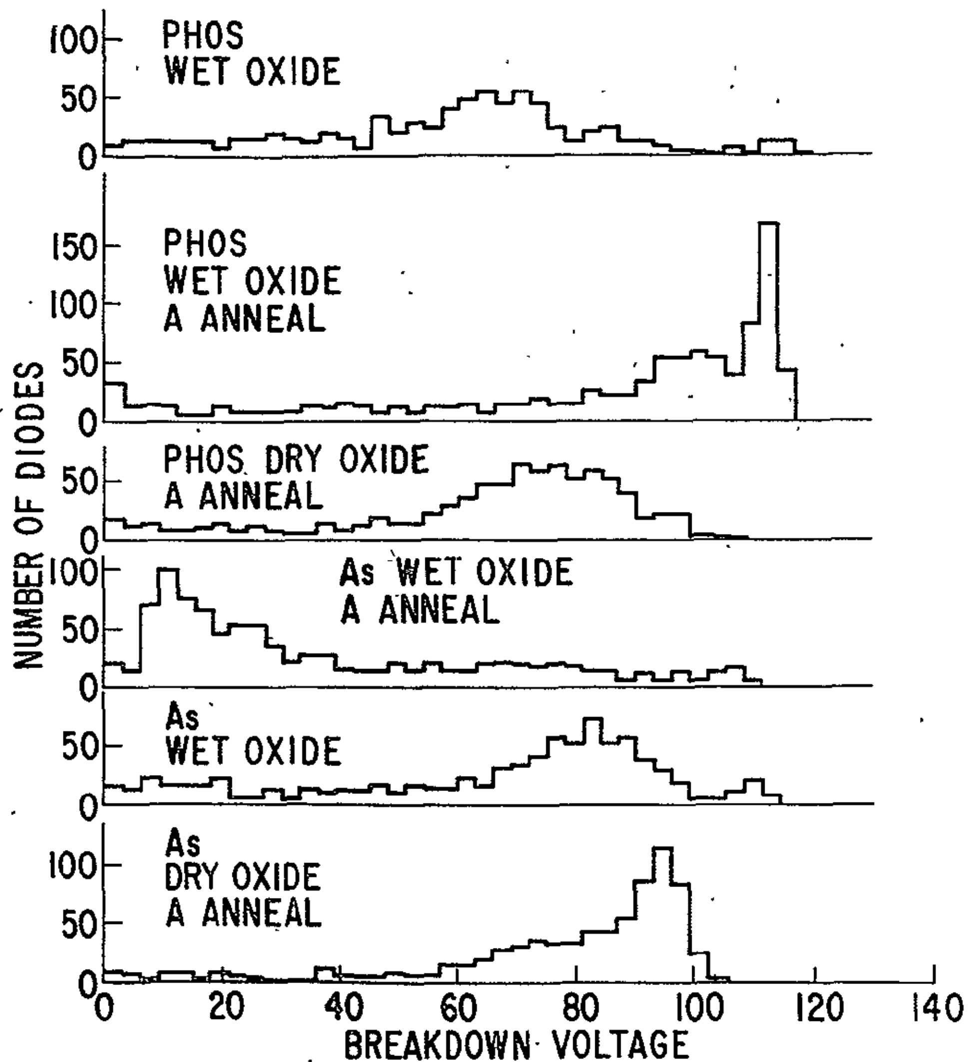

Figure 52. Histograms showing the distribution of reverse breakdown voltages for arsenic and phosphorus doped epitaxy for a variety of oxidation cycles

The area of these diodes was $10^{-2}cm^2$ and the breakdown was defined as the voltage that produced a reverse current of 100μ amp. The results indicate that phosphorus doped epitaxy gives more consistent results than arsenic and that wet oxidation followed by the argon anneal further minimizes reverse leakage. The bulk breakdown of the epitaxial material for these samples was 160 volts. The 110 volts achieved for the phosphorus samples that were argon annealed thus represents 68 percent of the theoretical maximum.

The generally better results for phosphorus than arsenic are probably due to the fact that phosphorus is a much faster diffusant than arsenic. "Pile up" at the surface due to rejection of dopant from the oxidizing silicon is less for phosphorus than for arsenic since the rejected phosphorus is able to dif-

fuse into the bulk silicon. Any increase in dopant at the mesa perimeter which occurs via this mechanism will lower the local breakdown voltage. In the one case where the As results most nearly approached those for phosphorus, the oxide was grown slowly in pure O_2 allowing maximum time for the arsenic to diffuse away from the surface. As a result of these experiments we settled on phosphorus as the n-dopant and the steam-argon oxidation cycle described above.

6.9 Mesa Strip

The wafer is now ready for barrier formation except for the fact that the barrier region is still covered by the original nitride and oxide layers. These are etched away by means of the usual hot phosphoric acid and buffered hydrofluoric acid etches.

We found that at this point it is advantageous to etch between 1μ and 2μ off the mesa top. This step was originally introduced at an earlier stage of process definition when the sequence was somewhat different. The getter cycle then followed mesa formation and passivating oxidation. With this procedure, every diode subsequently fabricated was a short. We found it necessary to deposit an additional SiO_2 layer, 6000Å thick, over the already formed mesa tops and edges in order to protect them from the $POCl_3$ environment of the getter furnace. Even with this additional protection, however, 5 percent to 10 percent of the diodes formed still showed large ohmic shunt leakage which saturated with increasing reverse bias.

These experiments were performed with diodes of 10^{-2} cm^2 area, whereas 25 or 50 amp diodes require approximately 0.5 cm^2 area. Assuming that the density of shorts is randomly distributed over the area of any wafer even a 95 percent yield of small diodes results in only 7 percent good large diodes.

An example of this behavior is shown in Figure 53. This diode shows reverse leakage current which, at the outset, increases linearly with applied voltage and which finally saturates at a level far higher than the thermionic value. This behavior may be understood by means of the model shown in Figure 54.

We believe that the protective 6000Å SiO_2 cover is not perfect and that some component of the phosphorus-rich gas mixture of the $POCl_3$ getter furnace penetrates it, attacks the Si_3N_4 on the mesa top, and dopes the silicon surface heavily n type. This very likely occurs at mesa edges, since this is the place where mechanical stresses arising from thermal expansion and geometry are greatest. When the mesa is subsequently stripped and the Schottky barrier formed, contact is also made to the heavily doped n+ region. This contact is a tunneling Schottky and is thus ohmic. Its conductance at low applied voltage is determined by the spreading resistance from the

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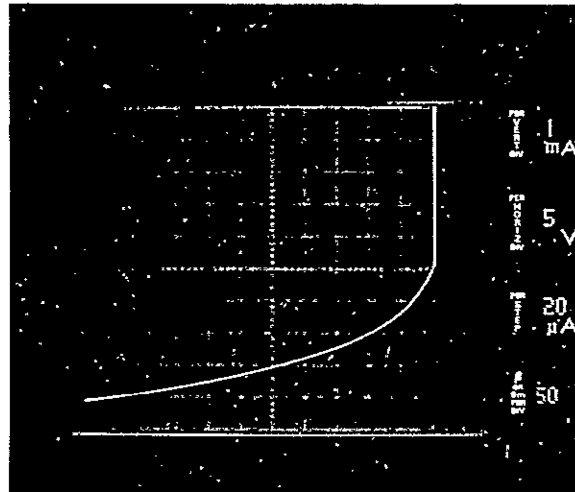

$$\rho = 2.5\ \Omega\text{-CM}$$

$$a = \frac{\rho}{2R} = 5\mu$$

Figure 53. Current-voltage characteristic of a diode exhibiting a getter-induced ohmic barrier shunt

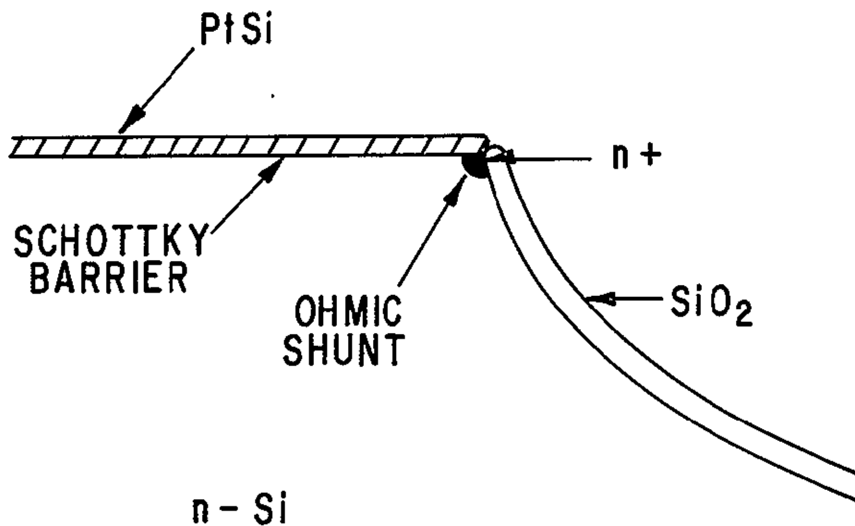

Figure 54. Idealized model of barrier shunt

heavily doped region. The current saturates due to the pinching off of the conductance path by the spreading depletion width of the proper Schottky region. The specifics of Figure 53 are consistent with this model. The shunt resistance calculated from the initial slope at $V = 0$ is $2.5 \times 10^3 \Omega$ which corresponds to the spreading resistance of a pinhole 5μ in diameter. It is noteworthy that the current saturates at about 50 volts which corresponds to the depletion width of the $2.5\ \Omega$-cm material.

This difficulty was completely eliminated for the 10^{-2} cm^2 area diodes by adding the step of etching 1μ to 2μ off the mesa tops after the getter cycle and before the barrier formation. This step etches away any heavily doped regions which may occur, thus removing the cause of the short. This etch step was found to be useful even in the absence of any n+ shunts. An example is shown in Figure 55 which compares reverse characteristics obtained from typical diodes from two halves of a single wafer. The upper trace, characteristic of diodes which have been gettered, slow cooled but not mesa etched, shows no leakage at low values of reverse bias but exhibits microplasma breakdown starting at 30 volts. The mesa etched devices, on the other hand, do not show any reverse current other than thermionic out to 160 volts where they break down via microplasmas. Evidently our getter cycle does not dissociate and remove all of the heavy metal complexes that are located near the original Si-SiO_2 interface. Etching away the Si near the interface clearly removes the impurities.

The effects of the getter cycle and mesa etching may be seen in statistical fashion by means of Figures 56, 57, and 58. Several otherwise identical wafers were processed in slightly different ways in an attempt to define the most nearly optimal procedure. The reverse bias corresponding to 1 ma leakage (10^{-1} amp/cm^2) was measured for each diode. The results are plotted in Figure 56. Samples 881 and 881E are two halves of a wafer that was gettered but not slow cooled. Sample 881E was mesa etched before barrier formation whereas 881 was not. It is clear that the mesa etching was useful in shifting the distribution to higher breakdown voltages. Samples 883E and 882E were both slow cooled and mesa etched differing only in that the phosphorous glass remained on 882E until after the Pt Si deposition, whereas 883 had its phosphorous glass removed before Pt-Si formation. The time of removal of the phosphorous glass doesn't seem to make any difference. A comparison of 882E or 883E with 881E, however, shows that slow cooling is beneficial. Figure 57 shows a similar distribution for $1.3\ \Omega$ material having lower bulk breakdown which was gettered, slow cooled, and mesa etched. These results are quite similar to those of 883E or 882E. Another comparison is shown in Figure 58. Sample 951 was ungettered but mesa etched, and 952 was gettered, slow cooled, and mesa etched. Again, the combination of gettering, slow cooling, and mesa etching gives the superior results.

The process was thus defined by means of experiments on diodes with 10^{-2} cm^2 area. The original sequence had the getter cycle appearing after

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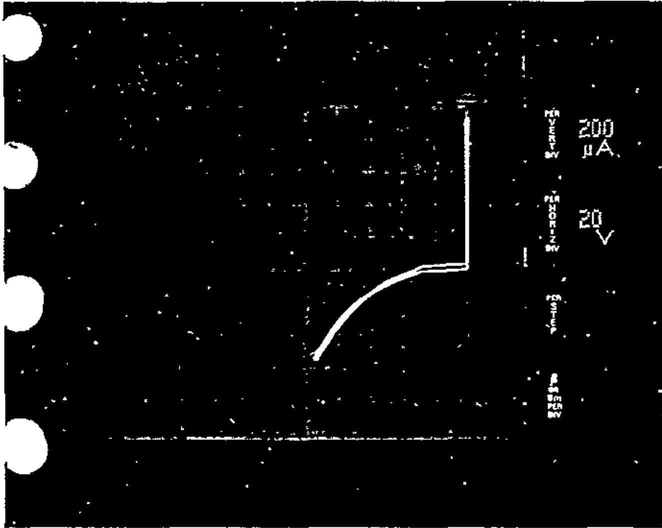
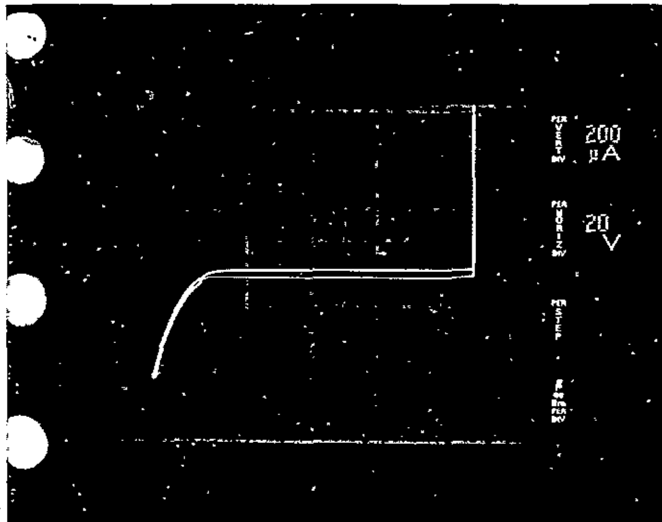


GETTERED
SLOW COOLED
NO MESA ETCH



GETTERED
SLOW COOLED
MESA ETCHED

Figure 55. Comparison of two diodes showing the effects of mesa etching

GENERAL ELECTRIC

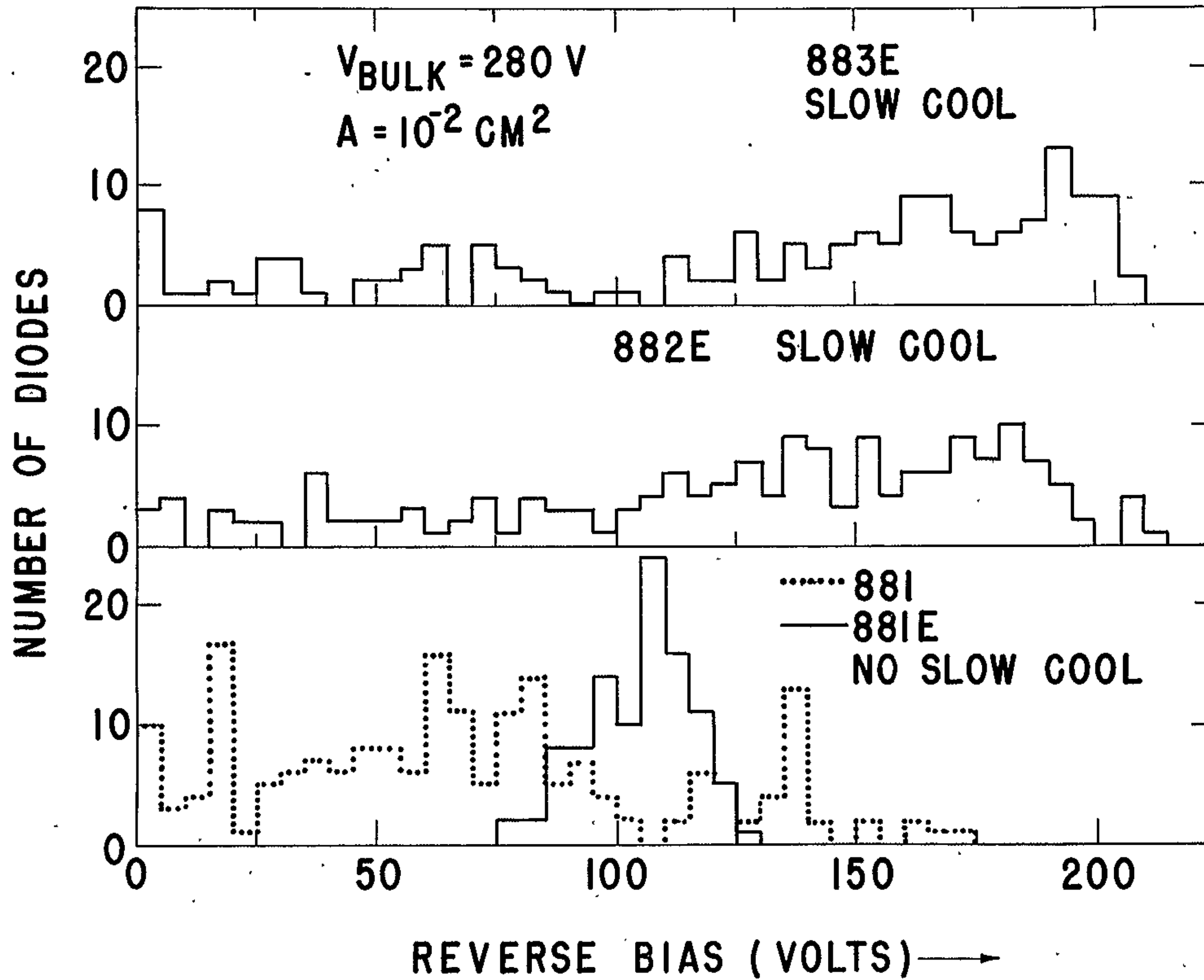


Figure 56. Histogram of breakdown voltage showing the effects of slow cooling and mesa etching

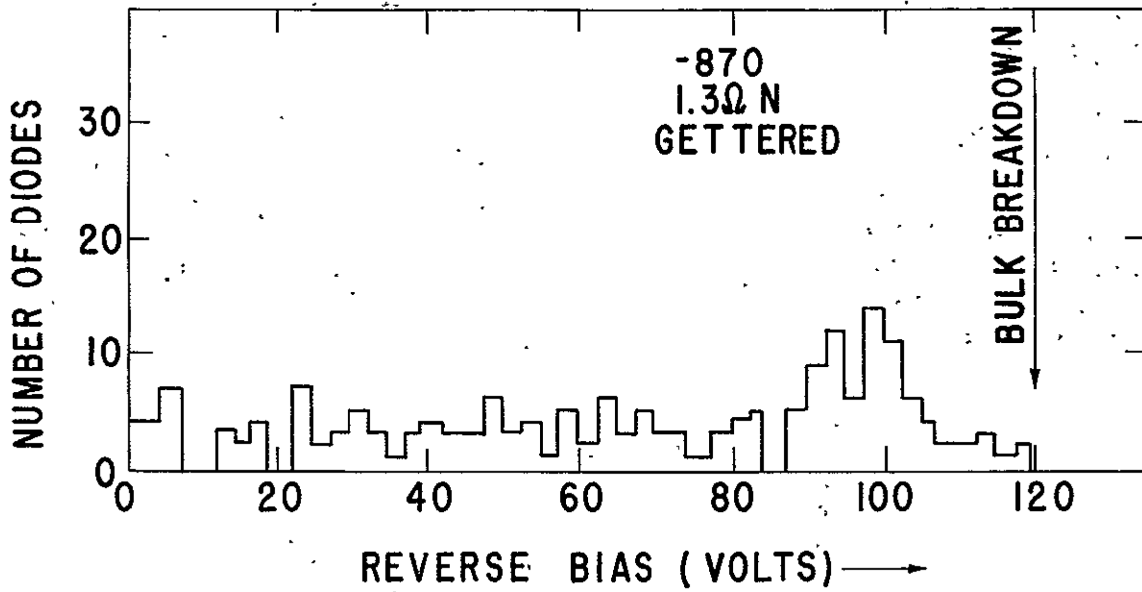


Figure 57. Distribution of breakdown voltages for 1.3Ω-cm material

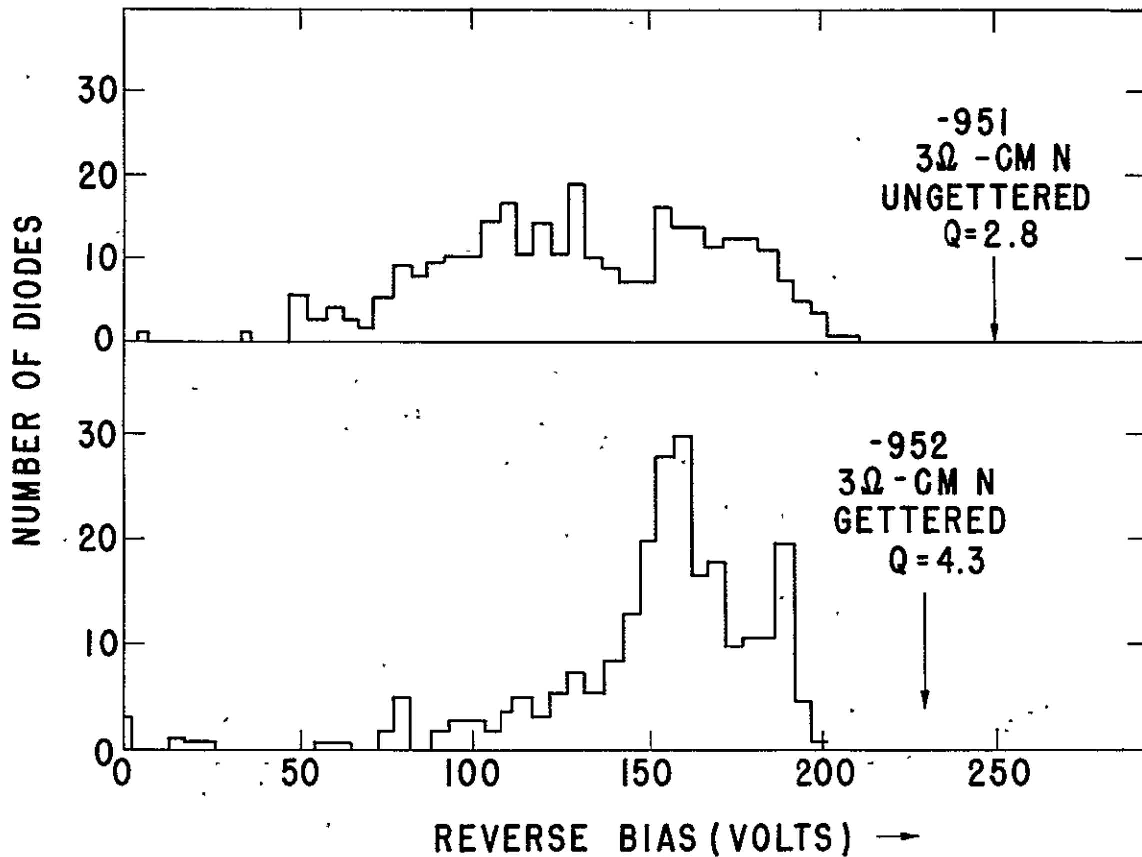
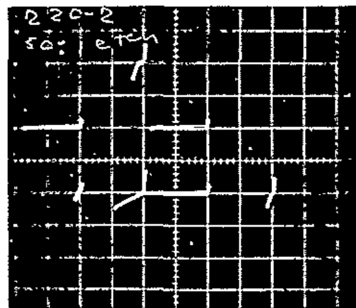


Figure 58. Histograms showing the effects of gettering upon the distribution of breakdown voltages

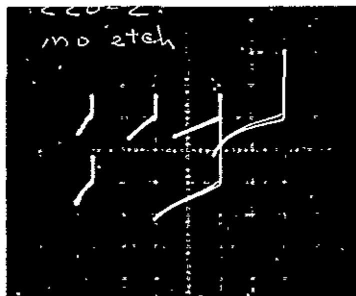
the passivating oxidation. In the course of fabricating the large .6 cm^2 size devices, however, we found that yields of large diodes and diode quality were greatly improved by gettering before mesa definition.

An example showing the effects of light mesa etching of large area diodes just prior to barrier formation is presented in Figure 59. Here we show the reverse I-V characteristics of two halves of a single wafer. One half has been lightly etched prior to Pt-Si barrier formation and the other is unetched. The leakage currents of the good diodes in the etched case are clearly far less than those of the unetched halves, corroborating the results obtained for small area devices.



2 ma/div
50V/div

a) MESA ETCHED



2 ma/div
50V/div

b) MESA UNETCHED

Figure 59. Comparison of the reverse leakage currents for two halves of a single wafer. One half was mesa etched prior to barrier formation and the second half was unetched. The diode area is 0.6 cm^2.

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6.10 Barrier Formation

The barrier is now formed by sputtering 600Å of Pt onto the wafer while keeping the wafer at an elevated temperature. The Pt reacts with the exposed silicon on the mesa tops and the barrier is formed in a way which automatically aligns the metal contact with the SiO_2 passivation. The Pt-Si Schottky metallization covers the entire mesa top, thus preventing edge breakdown.

6.11 Aqua Regia Etch

The unreacted platinum is removed by etching the wafer in hot (50°C) aqua regia; the platinum is dissolved while the Pt-Si is unaffected.

6.12 Final Metallization

The Schottky contact is now built up with successive depositions of 5000 Å of Mo, 1μ of Ni and 1μ of silver. These were chosen for the following reasons: Mo to seal and protect the thin barrier metal, Ni to serve as a solderable metal and also to act as a barrier to solder penetration, and silver to provide additional conductance and to prevent oxidation of the Ni surface. The Phase II diodes had their backs metallized with 1000 Å of Ti and 2μ of Au to allow eutectic bonding to tungsten backup plates. The Phase III diode backs were metallized with 1000 Å of Ti followed by 2μ of silver and 1μ of gold. This metallization was chosen to permit final soft solder assembly rather than eutectic bonding. The upper metallization is then patterned photolithographically. The etch used was HNO_3:H_2SO_4:H_2O in the ratios 1:1:3.

6.13 Cleave

Diodes are then separated by conventional cleaving.

6.14 Assembly

The Phase II rectifier assembly proceeded in two stages. The final 25 amp diodes have an active area of 0.6 cm^2 (0.307 in.)^2 the chip being (0.333 in.)^2. Completed, pretested chips were first eutectic bonded to 0.460 inch diameter tungsten backup plates at a bonding temperature of 500°C. The resulting subassembly is easy to handle and is thus easily checked for reverse characteristics at this stage. We considered this check to be a desirable one to do since this temperature is the highest one that the

completed diode sees in assembly. We anticipated that this cycle would result in significant losses, and wanted to discard bad diodes before final assembly. We were pleasantly surprised, however, with almost perfect yields through this step.

The completed tested subassembly is then mounted to its copper header and has its top lead applied. A completed assembly is shown schematically in Figure 60. A tungsten top piece $(0.280\text{ in.})^2$ is used to spread the current from the copper lead-in wire to the metallized Schottky barrier. The solders used were (a) Au-Sn eutectic to bond the tungsten backup plate to the copper stud, (b) high-lead soft solder to bond the top tungsten piece to the metallized Schottky diodes, and (c) either the soft solder or the Au-Sn to solder the copper lead to the top tungsten piece. The entire assembly of Figure 60 was soldered together in one step by heating it in hydrogen to a

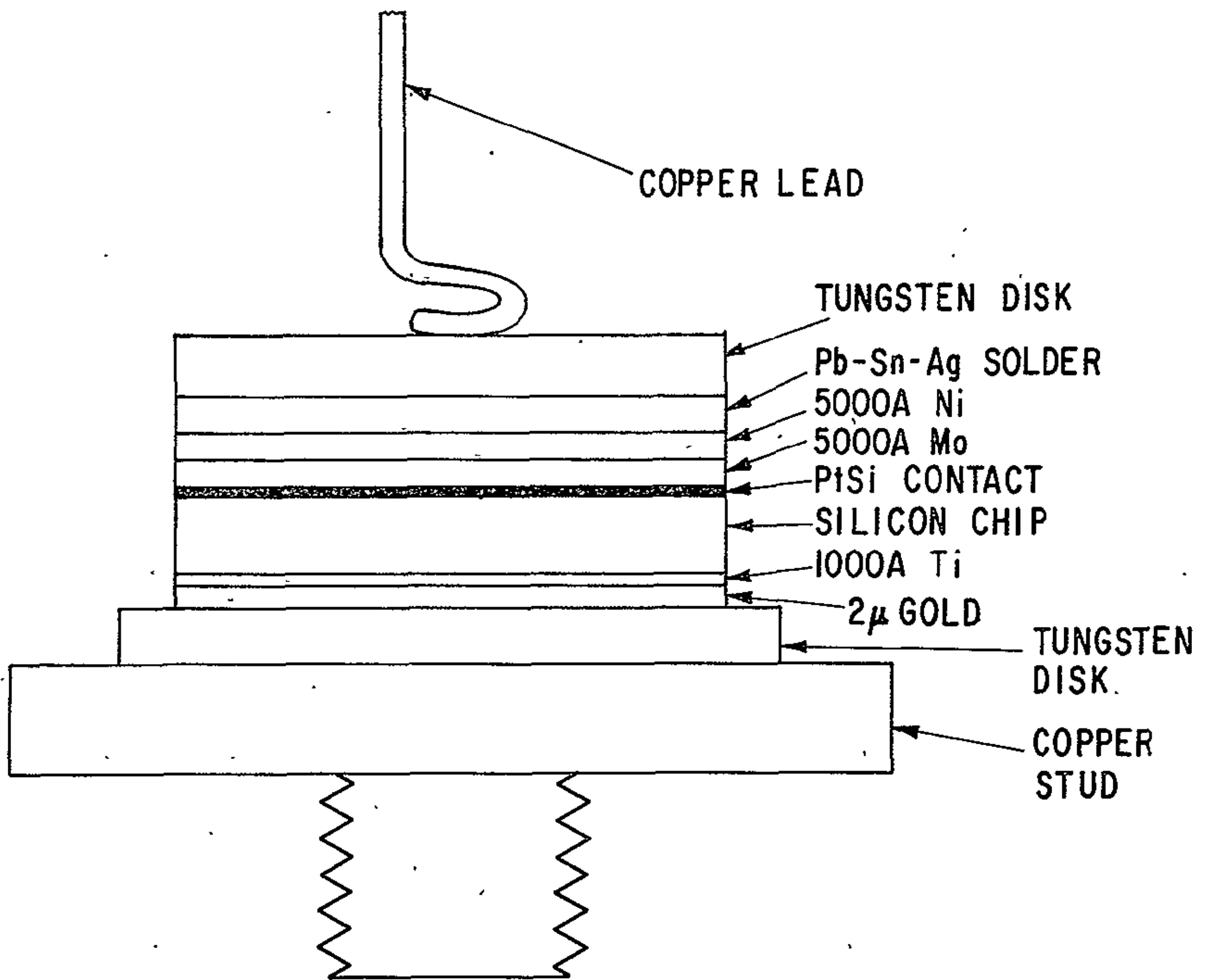


Figure 60. Schematic view of diode assembly

temperature of 350°C. The diode is now ready for standard hermetic sealing. We chose, instead, to encapsulate the mounted diode in silicone rubber, leaving the top Cu lead accessible for measurements. This was done in order to avoid any problems connected with possible contact resistance between the copper lead and the crimped stainless steel tube of the standard package.

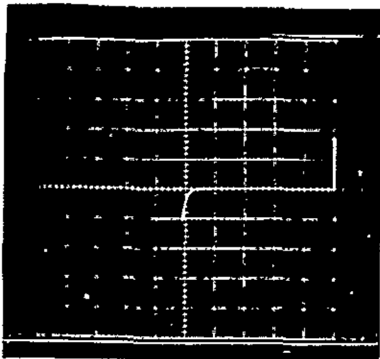
We found it possible to assemble large-area mesa Schottky diodes by means of the procedure described without degrading their reverse bias characteristics in any serious way. Figure 61 shows the reverse bias characteristics of two diodes in both initial chip form and after final assembly. Diode 6-1-5 shows no change in leakage current and no effects of assembly except for a slightly higher final breakdown voltage. This is likely due to the field shielding effect of the overlapping contact metallization. Diode 17-1(1, 3) also exhibits an increase of breakdown voltage in assembled form. It also shows a slight increase in leakage beyond 70 volts after assembly. As may be seen from the characteristic jogs in the I-V trace of Figure 61(d), this current is due to the onset of microplasma breakdown. We do not understand the reasons for the appearance of microplasmas after assembly, but it is not a common occurrence. In any event, this additional leakage current is not excessive and does not appear to be the factor determining the diode breakdown.

We experienced considerable difficulty with parasitic series resistance in forward bias with many of the large area Phase II diodes assembled in this manner. The details will be presented later in Section 7. Experiments were performed in order to identify the source of the "extra" series resistance and to develop processing and assembly procedures to eliminate it.

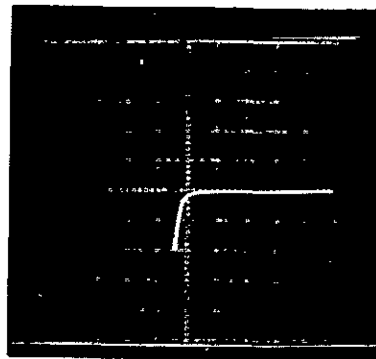
A series of samples was prepared from our usual epitaxial substrate ($\rho \simeq .01\Omega$-cm) material. No lightly doped Si was grown, as would normally be the case in actual Schottky diode fabrication, but the substrate processing and metallization were varied. Changes in sample resistance due to these variations could thus be studied without their being obscured by the relatively high resistance of an epitaxial layer. Additionally, in this effort we abandoned the eutectic bond chip mount down approach in favor of an all solder assembly. This was done in order to simplify the assembly procedure, to relax the flatness specification on the W backup plate required for uniform, full area, wetting to the Si chip, and to obviate contact resistance problems as will be discussed below.

The processing for the various samples, fabricated in all cases from .01Ω-cm antimony doped substrates was as follows:

OC7 - Wafer directly metallized with sputtered Ti (1000 Å), sputtered Ag (1.8μ), and sputtered Au (5000Å) on both top and bottom.

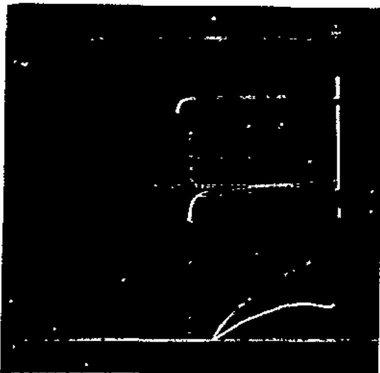


20 VOLT/DIV
A. 6-1-5 BEFORE ASSEMBLY

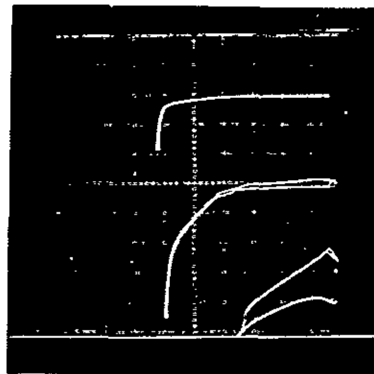


10 ma/DIV

20 VOLT/DIV
B. 6-1-5 AFTER ASSEMBLY



20 VOLT/DIV
C. 17-1 (1,3) BEFORE ASSEMBLY



10 ma/DIV

1 ma/DIV

0.1 ma/DIV

20 VOLT/DIV
D. 17-1 (1,3) AFTER ASSEMBLY

Figure 61. Comparison of diode reverse characteristics before and after final assembly

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OC8 - Wafer directly metallized with evaporated Ti (1000 Å), evaporated Ag (1.8 μ), and sputtered Au (5000Å) on both top and bottom.

OC9 - Wafer was subject to heavy phosphorus diffusion (N_s = 5×10^{20}) into both top and bottom and Ti, Ag, Au sputtered on both top and bottom.

OC10 - Wafer was phosphorus diffused both top and bottom as OC9 but metallization was evaporated Ti, evaporated Ag, and sputtered Au.

OC11 - Wafer was phosphorus diffused into top and bottom. The initial top metallization was "low temperature" Pt-Si formed in the usual manner directly upon the .01Ω-cm material. The top was then metallized with our usual sequence Mo, Ni, Ag with an additional 1000 Å of Au to prevent silver tarnishing. The bottom was metallized with evaporated Ti, Ag and sputtered Au.

OC12 - This wafer was processed exactly as wafer 11 except that the Mo layer was omitted.

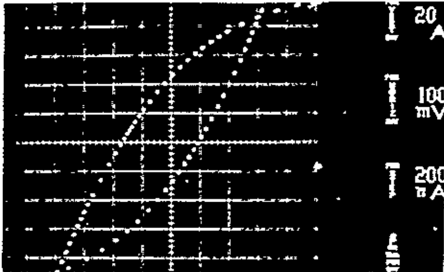
These wafers were cleaved into .333" chips and were solder assembled using two different solders, hard eutectic AuSn solder melting at 280°C, and a soft Sn-Pb-Ag solder melting at 180°C. In addition, a sample (OC7) was assembled for which the semiconductor chip was left out, the only resistance thus being that of the metal parts and the solder layers.

Representative results are shown in Figure 62. In every case where the substrate was metallized directly with no additional phosphorus diffusion, the sample current-voltage characteristics showed rectification and high (>5 milliohm) resistance independent of metallization procedure or the solder used.

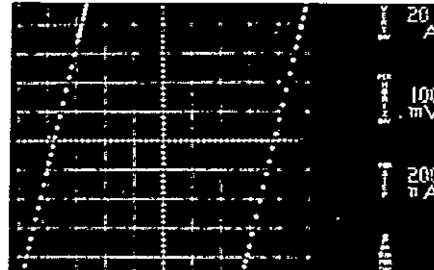
The reasons for this behavior is due to the relatively low doping (5×10^{18}) in the standard .01Ω-cm epitaxial substrate. This concentration is not high enough to allow much tunneling to occur and the relatively high Schottky barrier height to n-Si produces a high impedance contact. Samples which were phosphorus diffused to a surface concentration high enough to permit tunneling (5×10^{20}) on the other hand, showed low resistance characteristics (with exceptions to be discussed below) essentially independent of

METALLIZED SUBSTRATE

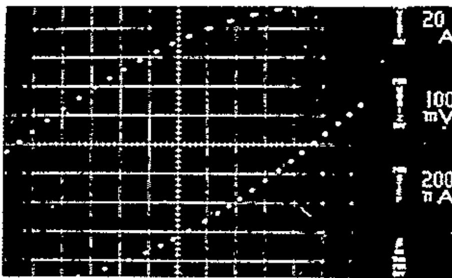
SUBSTRATE PHOSPHORUS DIFFUSED ($N_D = 5 \times 10^{20}$)



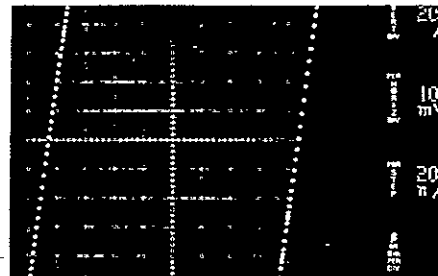
7-1



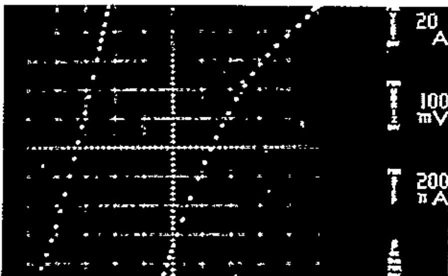
9-9



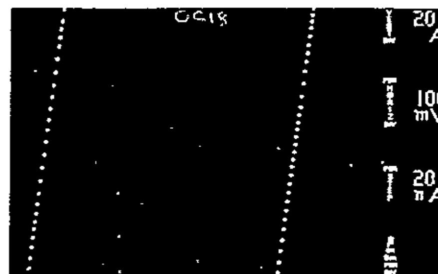
7-3



10-11



8-5



11-18

Figure 62. Current-voltage characteristics for representative samples from wafers OC7-OC11. Both polarities of current flow are shown.

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metallization procedures or the solder used in assembly. A complete summary of the results are given in Table V below. The first number identifies the wafer and the second the sample.

TABLE V

ASSEMBLY RESULTS

Sample	Solder	Assembly Temp	R_S (milliohm)
OC7-1	Au-Sn		15
7-2	Au-Sn		12
7-3	Pb-Sn-Ag	400	20
OC8-4	Pb-Sn-Ag	300	15
8-5	Pb-Sn-Ag	300	4
8-6	Au-Sn	360	7.5
OC7	No semiconductor		.1
OC9-8	Pb-Sn-Ag	240	1
9-9	Au-Sn	360	1
9-10	Au-Sn	360	1
OC10-11	Au-Sn	380	2
10-12	Au-Sn	350	.8
10-13	Au-Sn	350	.8
10-14	Pb-Sn-Ag	350	.67
OC9-15	Au-Sn	340	.75
9-16a	Au-Sn	340	.75
9-16b		(reheat 16a to 460)	1.33
OC11-17	Au-Sn	350	.625
11-18	Pb-Sn-Ag	280	.65
OC12-19	Au-Sn	350	2.5
12-20	Pb-Sn-Ag	350	.7
12-21	Au-Sn	350	4

The bulk resistance of the epitaxial substrate corresponding to these samples is 0.5 milliohm, which when added to the 0.1 milliohm result for the metal drops obtained from sample OC7, gives an ideal value of 0.6 x 10^{-3} ohm. The results from wafers OC9-OC11 which vary from .65 milliohm to 1 milliohm are thus very close to ideal.

The results from wafers 9 and 10 indicate that there is no advantage to evaporation over sputtering and that the differences between the hard AuSn

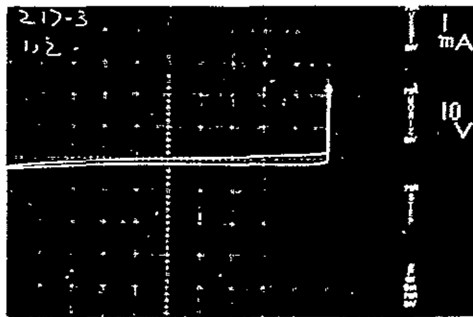
solder and the soft Pb-Sn-Ag solder are minimal. The results from wafer 11 which has the Schottky metallization and the top contact buildup shows that the presence of the Schottky barrier together with its associated metallization has not introduced any additional parasitic resistance. Wafer 12 gave erratic results due to the fact that, in the absence of the Mo layer, the Ni exerted enough stress on the Si through the Pt-Si film to detach itself in places. In the process it cleaved the silicon indicating excellent adherence between the various metal layers.

There is some indication from these results that it is undesirable to allow the assembly temperature to exceed the Au-Si eutectic temperature of 370°C. This may be seen in the higher resistance of sample OC10-11 as compared with either OC9-10 or OC10-12 and in the increase in the resistance of OC16 after reheat to 460°C. The reasons are connected with the specifics of the Au-Si eutectic alloy cycle. The solubility of phosphorus in Si at any reasonable alloy regrowth temperature is considerably less than the 10^{20}-10^{21} cm^{-3} that can be quenched in from a high temperature diffusion which is necessary, as we have seen, for good ohmic contact. If gold alloying is allowed to take place with the back of the Si chip during assembly the thin (1-2 micron) phosphorus diffused layer may be completely dissolved. Upon cooling the regrown silicon will reject the dopant to the solvent, depleting the surface of the high concentration needed for tunneling. This will lead to an increased contact resistance. The degree to which this takes place will depend upon such factors as (1) depth of the high concentration phosphorus diffusion, (2) the amount of gold solvent available, (3) the alloying temperature, and (4) the specific details of the thermal gradients and rates of cooling during the regrowth process.

We decided to bypass all of these problems in the assembly of the Phase III diodes by using an assembly procedure that maintained in an undisturbed state the high concentration phosphorus layer diffused into the diode back during the getter cycle. In brief, we used solder assembly at low temperatures rather than eutectic bonding.

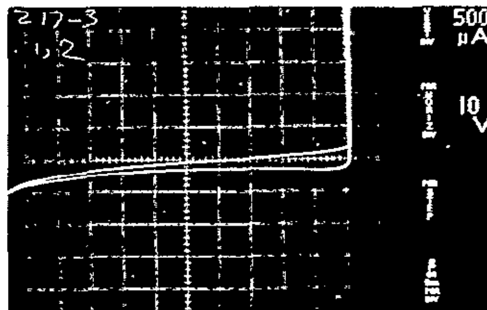
6.15 Capping

The final step in device fabrication is that of capping. We utilized a hermetic resistance weld seal and lead crimp. By contrast with our initial expectations the lead crimp introduced no additional resistance. The reverse characteristics of some diodes, however, were degraded somewhat by the ring seal step. The breakdown voltages were lowered by 10-15 volts. This problem was solved by coating the mesa periphery with a thin layer of a silicone rubber prior to capping. The difficulty was evidently caused by spattering of metal upon the exposed passivating oxide during the ring weld.



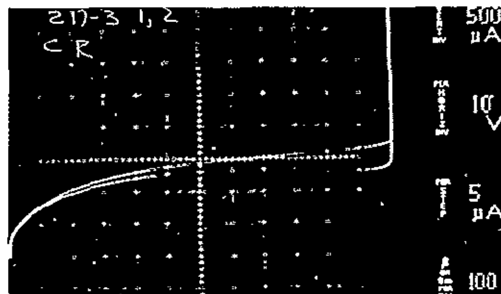
1ma/div
10 VOLT/div

A. PRIOR TO ASSEMBLY



0.5ma/DIV
10 VOLT/DIV

B. ASSEMBLED, NOT CAPPED



0.5ma/DIV
10V/DIV

C. ASSEMBLED AND CAPPED

Figure 63. Reverse I-V characteristics of a Phase III, 100 volt diode at various stages of its fabrication

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The reverse leakage characteristics of diode 217-3 1, 2 are shown at various stages in its history in Figure 63. The room temperature leakage in chip form prior to assembly is presented in A and the leakage just prior and following capping are shown in B and C respectively. It is clear that there is no substantial change in the leakage throughout the sequence.

Section 7

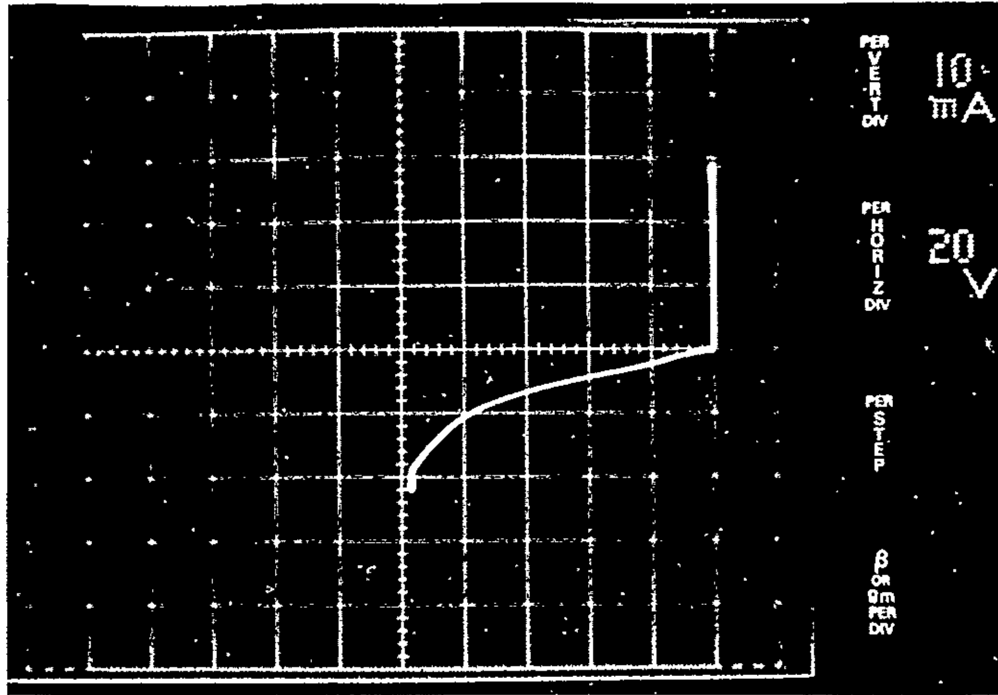
RESULTS OBTAINED ON LARGE AREA DIODES

7.1 Reverse Bias – Yield and Quality

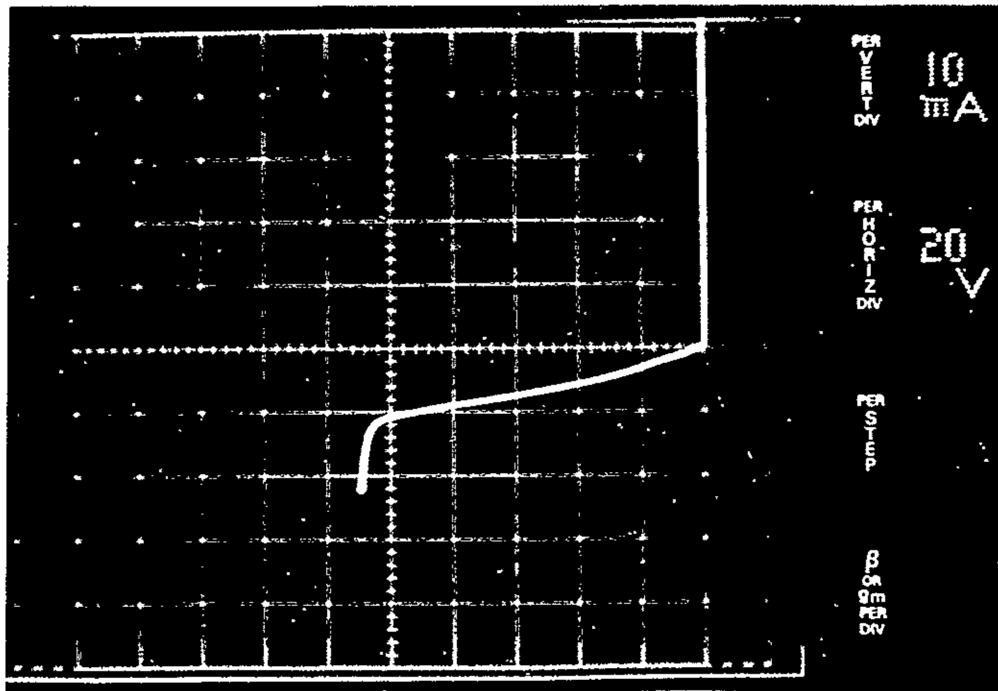
While barrier parameters were determined from experiments done upon diodes having area 10^{-3} cm^2 and wafer processing procedures were developed using diodes of 10^{-2} cm^2 area, the bulk of our actual wafer fabrication was done for diodes having 0.6 cm^2 area. This is the size appropriate for the 25 amp 200 volt and the 50 amp 100 volt diodes as have been described above. Epitaxial material varying in resistivity from 0.8 to 3.4Ω-cm was processed. Thirty-three lots of 3 to 6 wafers per lot have been processed in all. The major focus of effort in the fabrication of large diodes has been on the improvement of reverse characteristics in a manner consistent with providing low forward contact resistance.

The mesa process as initially developed with small (10^{-2} cm^2) diodes was not capable of producing high yields of high quality diodes. Initial yields were at best 1 to 4 diodes per wafer out of a possible 14 per 2-inch wafer, and the reverse characteristics of these diodes were typically soft as shown in Figure 64(a), or leaky from the outset as shown in Figure 64(b). An example of one such early wafer is shown in Figure 65. The I-V characteristics of each of the 14 diodes on the wafer is shown in the picture at the position corresponding to its actual location on the wafer. Most of the diodes break down at low voltages with only four having blocking capability greater than 50 volts. A room temperature reverse bias characteristic of one of these diodes is shown in Figure 64(b) where a nonthermionic component of current is seen even at low voltage. This extra current is not very temperature dependent, increasing, as may be seen in Figure 66, by no more than a factor of 2 at 107°C. While this type of leakage was thus not overly serious insofar as the 100°C reverse leakage specifications were concerned, we felt it desirable to eliminate it and achieve more nearly ideal room temperature reverse currents. Small adjustments were made in the processing sequence which had the eventual result of improving yield, uniformity, and diode quality. The final process sequence resulting was described above in Section 6.

Near the ends of each of the Phase II and Phase III efforts several lots were processed in a disciplined manner. Process variations were not allowed and material was put through in a sustained way in order to get some feeling for reproducibility and yield. A typical wafer from these last lots is shown in Figure 67(a) and the best wafer is shown in Figure 67(b). These wafers show that high-quality diodes can be fabricated even in this large diode size at yields greater than 70 percent.



a



b

Figure 64. Reverse characteristics illustrating soft characteristics and excess leakage at low voltage

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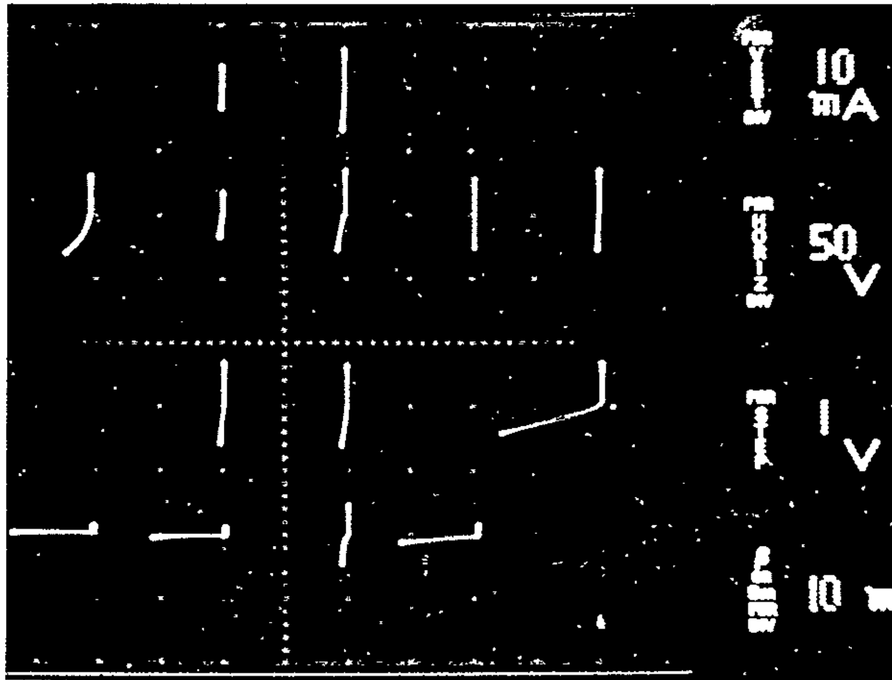

Figure 65. Spatial distribution of reverse diode characteristics for a wafer from one of the early lots

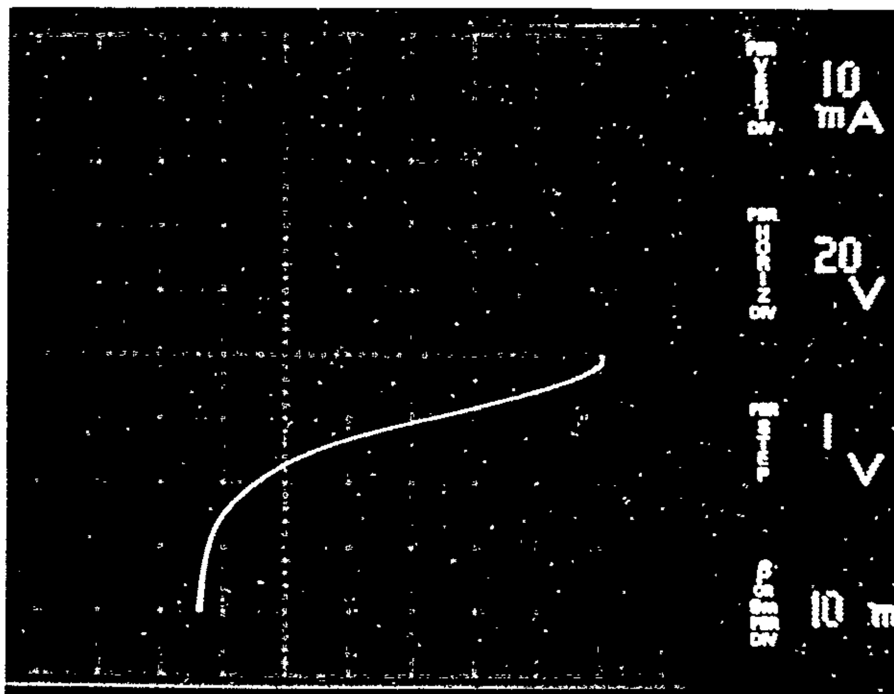

Figure 66. Reverse bias characteristic at 107°C for the leaky diode of Figure 34(b). The leakage current is essentially unchanged from its room temperature value.

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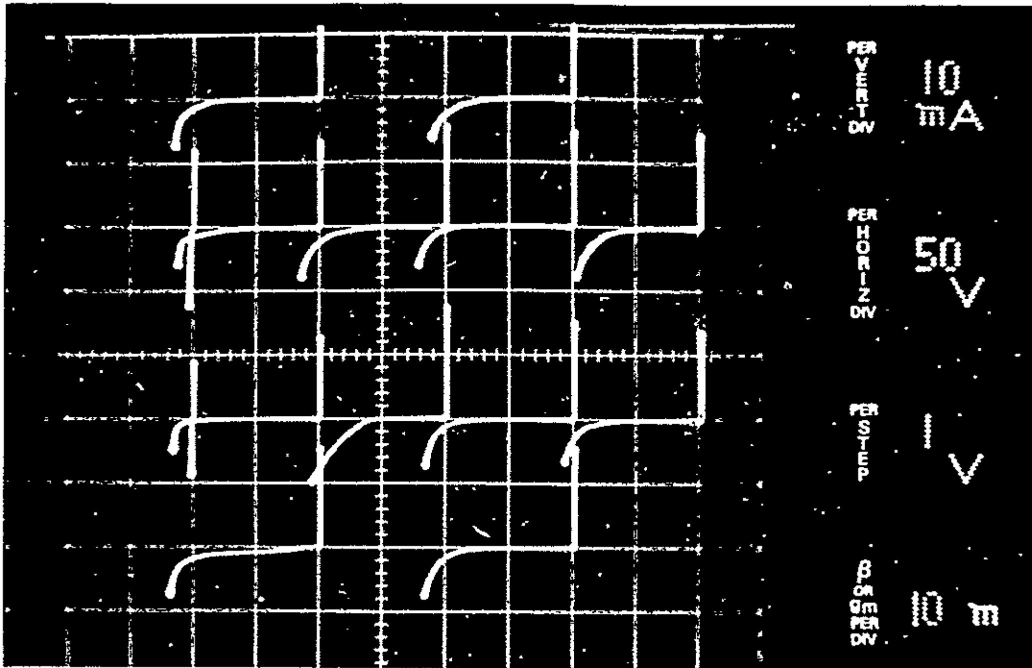
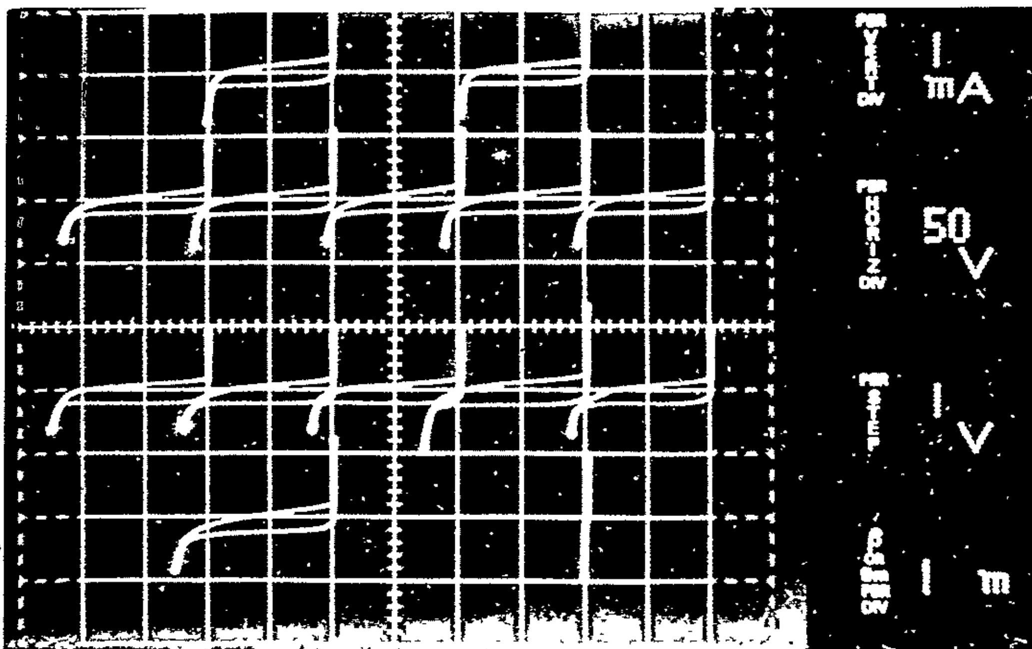


a



b

Figure 67. Wafer maps of reverse diode characteristics for a typical wafer and for the best wafer from the later lots

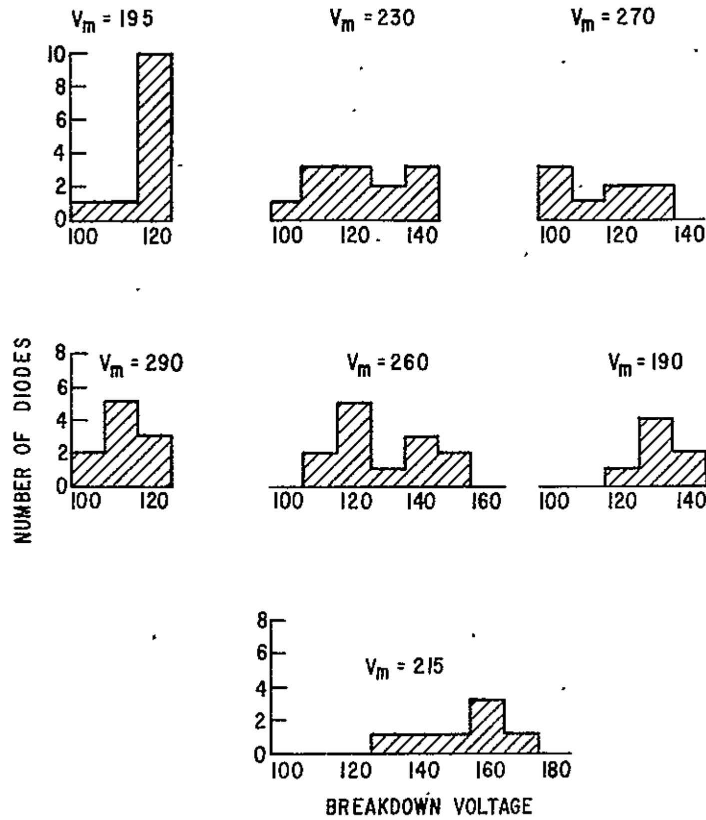
Figure 68 shows the distribution of breakdown voltages for all the wafers of these last lots. In no case was the yield of diodes having breakdown voltage above 100 volts less than 50 percent. For the best wafer the yield was 93 percent.

The measured breakdown voltage distributions for the large area diodes of the Phase II effort are shown in Figure 69 where a comparison is made between them and V_{max}, the theoretical maximum value. V_{max} is the microplasma free bulk avalanche breakdown voltage corresponding to the resistivity of each diode. These results scatter between the lines $V = 0.5\ V_{max}$ and $V = 0.7\ V_{max}$. Corresponding results for the 100 volt design of the Phase III work are shown in Figure 70. Breakdown voltages for these diodes cluster rather closely about values corresponding to 70 percent of the theoretical V_{max}. This then would seem to be the proper value for a practical design rather than value of $f = 0.8$ assumed in Section 5.2.

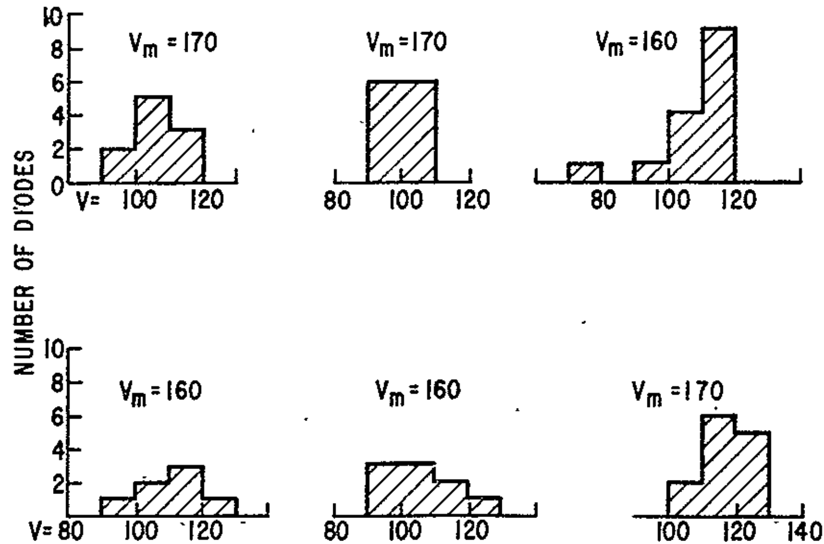
Many of the diodes exhibited "pushiness" in their room temperature reverse bias characteristics. That is, the device avalanche breakdown slowly moves out to higher values through the course of measurement, finally saturating after a minute or so at values 10 to 20 volts higher than at the outset. This is a well-known phenomenon in reverse biased passivated p-n junctions. It is characteristic of diodes where for one reason or another, avalanche multiplication takes place at the silicon surface where the p-n junction intersects the SiO_2 passivation. As the multiplication process continues, electrons from the avalanching region are accelerated towards the passivating oxide, tunnel into it, and are trapped. These trapped electrons act to reduce the local electric field, thereby allowing greater applied bias to be applied before the avalanche occurs.

We conclude that our "pushy" mesa Schottky diodes likewise have their highest electric field region at the intersection of the Schottky barrier with the passivating oxide. When avalanche breakdown occurs it takes place right there at the periphery of the mesa top. We do not know the reason for this field enhancement at the diode periphery. It may, however, be due to residua heavy metal complexes that are ungettered and that have not been removed by the light mesa etch just prior to barrier formation.

We made careful measurements of the capacity-voltage characteristics of small area (10^{-2} cm^2) test Schottky diodes located on the same wafers as were processed in the fabrication of the 50 A 100 volt diodes. We used these data primarily to obtain the basic material parameters, resistivity and epitaxial thickness needed to calculate the forward resistance of these diodes. Typical results obtained by straightforward differentiation of the experimental C(V) vs. V data are shown in Figure 71. Once available, these curves may be directly integrated to yield experimentally determined values for E_{max}, the electric field at the metal-Si interface of the Schottky barrier. Values of E_{max} corresponding to the wafers of Figure 71 are shown in Figure 72.



(a) Towards the end of Phase II



(b) Towards the end of Phase III

Figure 68. Distribution of breakdown voltages for wafers processed in a disciplined manner

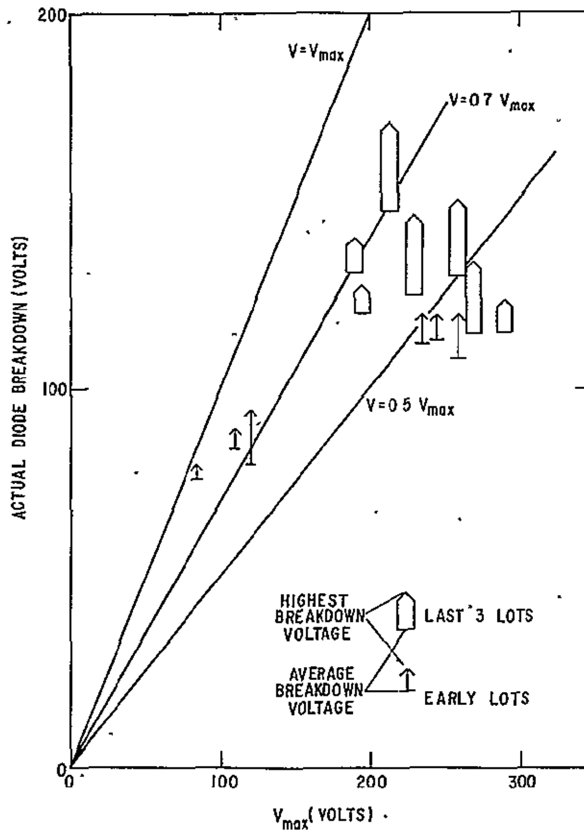


Figure 69. Comparison of actual measured diode breakdown voltages with theoretical maxima for Phase II diodes

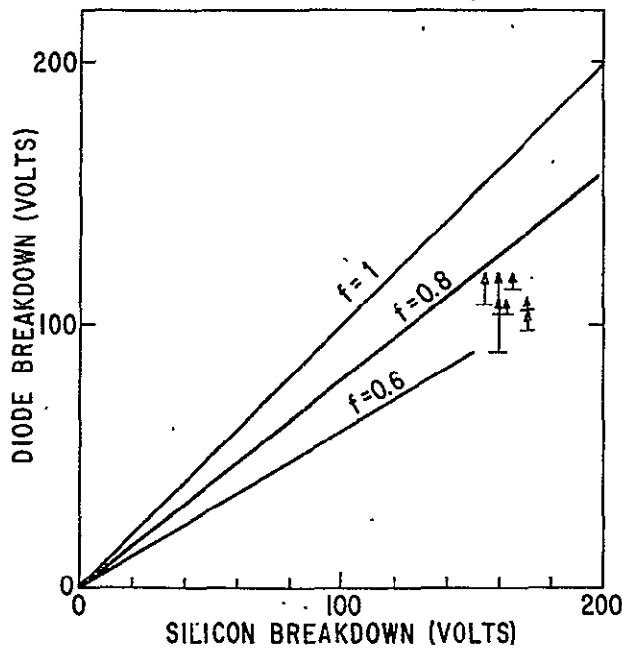


Figure 70. Comparison of measured breakdown voltages with the theoretical maxima for Phase III diodes

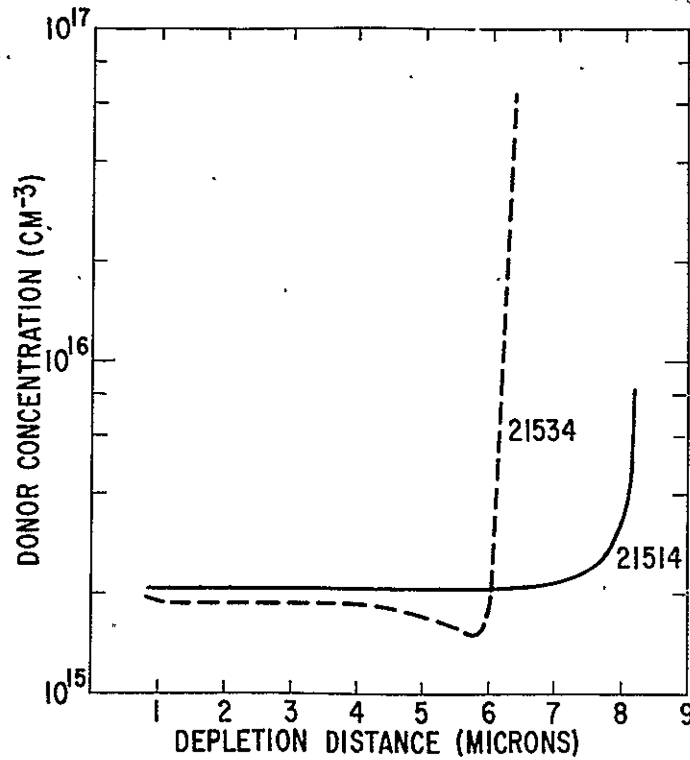


Figure 71. Carrier concentration vs. distance into the epitaxial region obtained from differentiation of capacity-voltage data

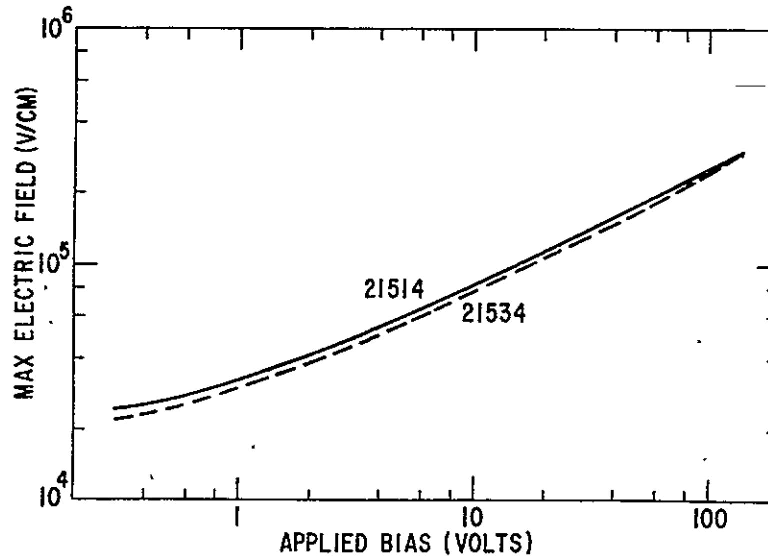


Figure 72. Variation of E_m, the electric field at the metal-semiconductor interface, with reverse bias

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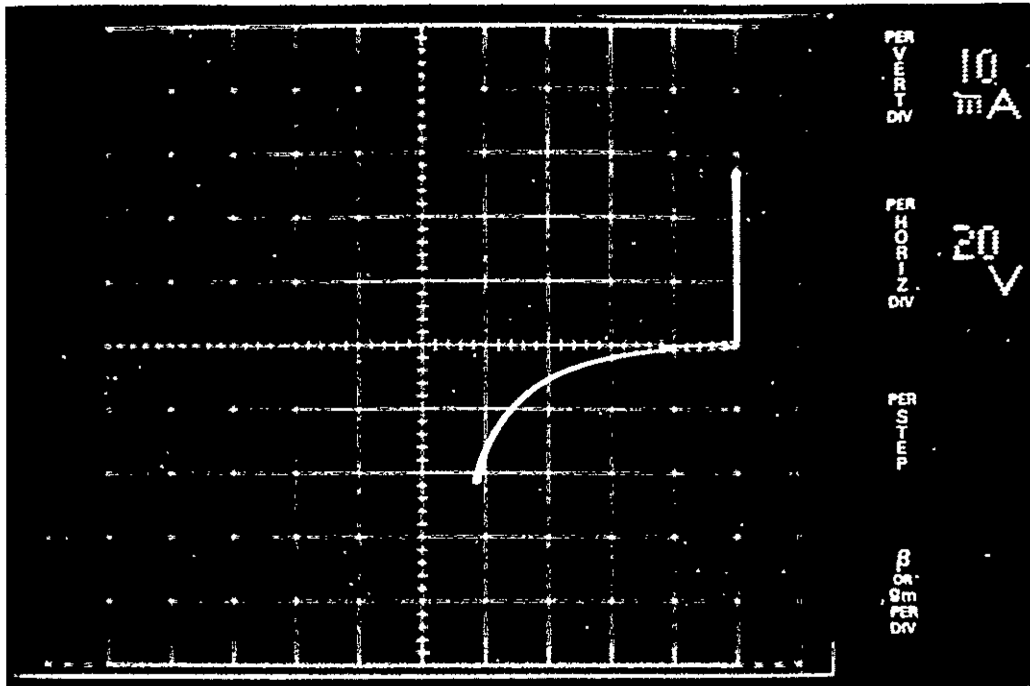
As may be seen, the electric field corresponding to the 100 volt reverse breakdown typical of the 50 amp devices obtained from these wafers is a respectable 2.6×10^5 V/cm. Electric field values at breakdown for all of the 50 amp diodes fabricated fell between 2.4×10^5 V/cm and 2.8×10^5 V/cm. This is to be compared with the critical breakdown field of 3.15×10^5 V/cm for Si at 2×10^{15} impurity concentration.

The reverse characteristics of two diodes are shown in Figures 73 and 74. Figure 73 is typical of the results obtained in our early lots, and Figure 74 is typical of the later results. Results are shown for both room temperature and for 125°C. The diode of Figure 73 shows very low leakage at room temperature and an ideal characteristic at 125°C out to approximately 100 volts reverse bias. The reverse current begins at 1 ma near V = 0 and increases to 11 ma at 100 volts. These values are completely accounted for by calculating the thermionic emission current over the Schottky barrier. The low voltage value of 1 ma corresponds to thermionic current over a barrier of 0.79 eV as determined by forward current measurements made on test diodes on the same wafer. The reverse thermionic current increases to 7 ma at 80 volts reverse bias due to 55 mv of barrier lowering associated with the barrier field of 1.8×10^5 v/cm at 80 volts. Above 80 volts, additional nonideal current appears and the diode finally breaks down at 120 volts. Thermionic barrier current is also seen in Figure 73 (b). It is the same magnitude as that in Figure 74, except here it is added to the nonideal leakage component which appears to be unchanged from room temperature. All of the good diodes from the last three lots as well as many of the early diodes exhibited theoretical saturation current out to electric fields of approximately 2×10^5 v/cm for temperatures above 100°C.

In the course of our fabrication of large diodes we processed epitaxial material produced in many separate runs obtained from three entirely different sources. It is not possible for us to come to any precise conclusions about the correlation between epitaxial quality and reverse breakdown. Nevertheless, some comments are in order. As was stated above, we were unable to get reasonable yields from material supplied by one of our sources while getting good results from other suppliers' wafers processed in the same way. We conclude from this that there is some minimum level of epitaxial crystalline quality and purity required for the successful fabrication of mesa Schottky diodes. There was no explicit specification on the crystalline quality of the other two suppliers' material. This leads us to the belief that ordinary, production run material of reasonable quality is adequate for high yield fabrication, and ultrahigh quality is unnecessary.

A specific example buttressing this belief is given in Figure 75 where photomicrographs of several different regions of diode (1, 2) of wafer 17-1 are shown. At least three different kinds of crystalline defect are present in this diode as well as a process-induced defect. Dislocations occurring near and at the mesa edge may be seen in Figure 75(c); dislocation lines are



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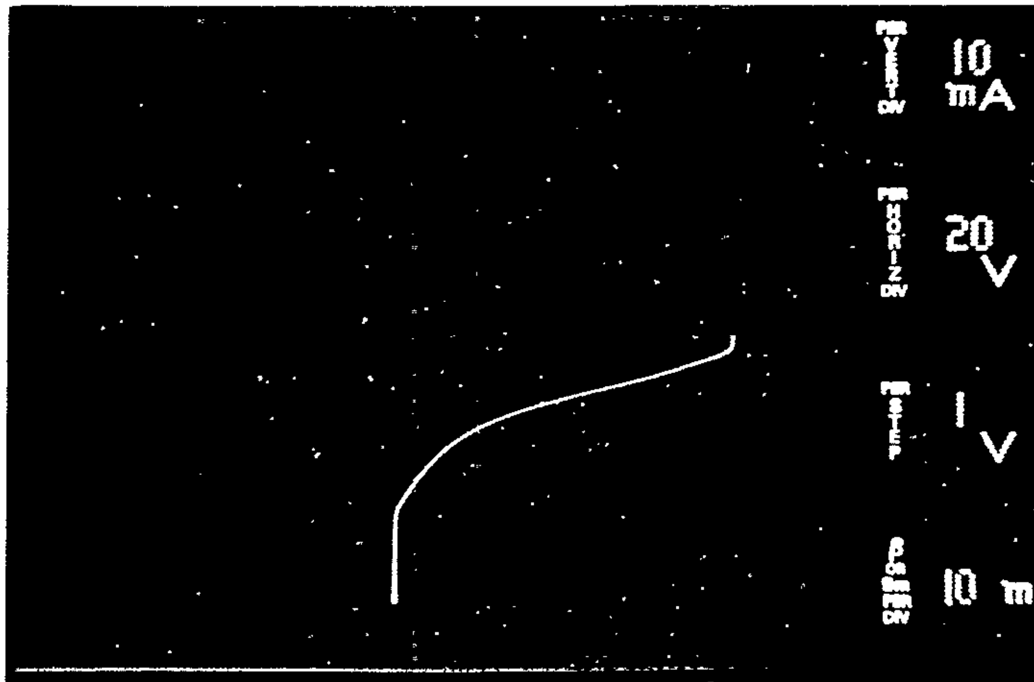

b

Figure 73. Comparison of room temperature leakage of a leaky diode with that at 125°C

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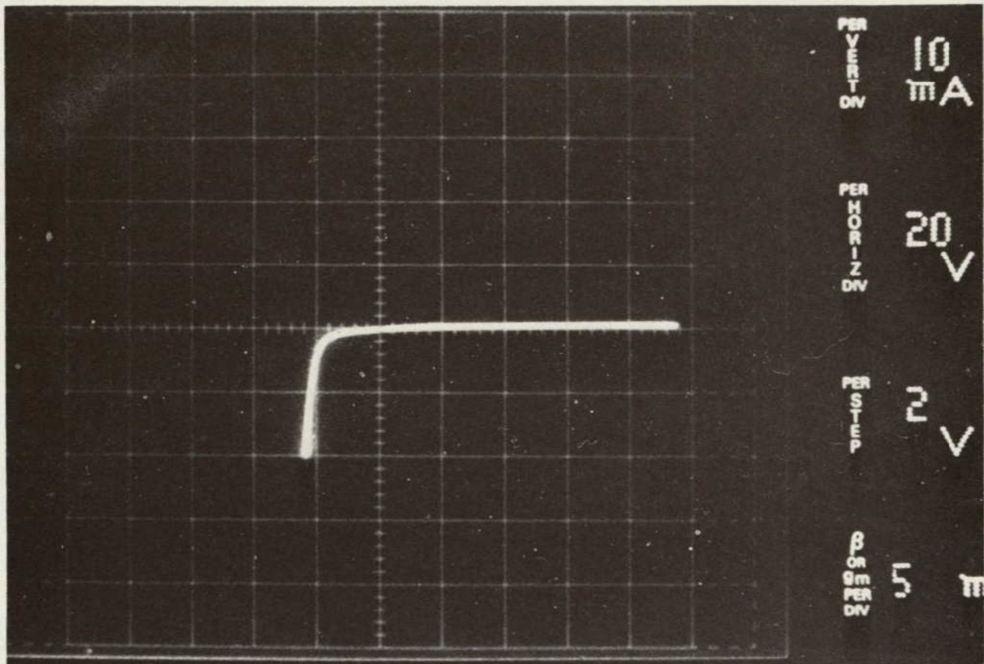

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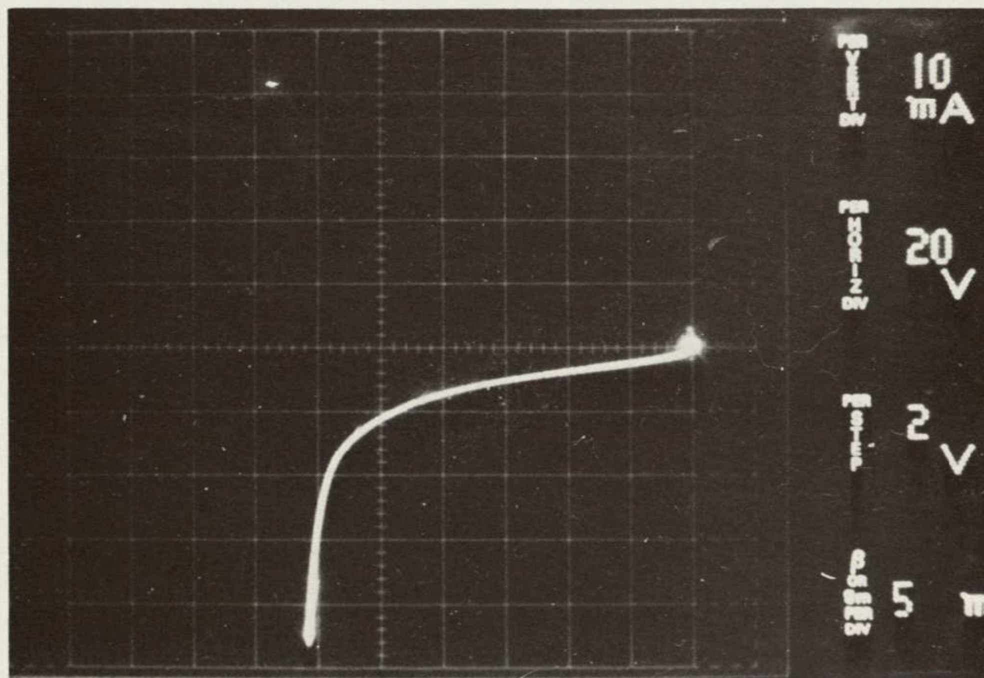


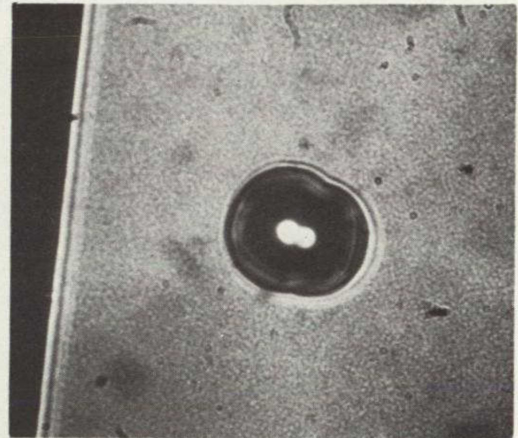
b

Figure 74. Room temperature and 125°C reverse characteristics for a nearly ideal diode

WAFER 17-1
(700X)

DIODE 1,2

a) FINE GROWTH DEFECT



b) PINHOLE IN Si_3N_4

c) DISLOCATIONS

d) EXTENDED DISLOCATION NETWORK

Figure 75. Photomicrographs of various crystalline defects that do not contribute leakage current

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visible in Figure 75(d); and unidentified fine scale growth defect is shown in Figure 75(a); and a hole in the mesa caused by a pinhole in the Si_3N_4 layer is evident in Figure 75(b). Notwithstanding all these defects, this diode is the best diode of wafer 17-1, exhibiting voltage breakdown greater than 130 volts. This may be seen in Figure 76(a). Needless to say, there are defects that will result in shorted diodes. Each of the diodes of wafer 17-1 that exhibit low voltage breakdown; (4, 1), (4, 2), and (5, 3), has a gross defect associated with it. Diode (5, 3) has had a corner chipped off [Figure 76(b)], diode (4, 1) has an epitaxial growth hillock [Figure 76(c)], and (4, 2) shows an assembly of micron-sized defects which may be impurity precipitates localized in a well-defined area [Figure 76(d)].

7.2 Forward Characteristics

Detailed forward I-V characteristics for three assembled diodes are given in Figures 77 and 78. Diode 2-15-3, shown in Figure 77, was fabricated on 1 Ω-cm epitaxial material 10μ thick. The current increases at room temperature exponentially with applied voltage from 10μ amp to 1 amp forward at the rate of 64 mv per decade. This leads to an "n" value in the expression

$$I = I_s \exp \frac{qv}{nkT}$$

of 1.08. Above 1 amp the current increases less rapidly than exponentially due to the series resistance of the diode. The measured value of series resistance, R_S, obtained from the data of Figure 77 is 2.4×10^{-3} ohm. The value of the semiconductor bulk series resistance calculated from the measured resistivity and epitaxial thickness is 1.8×10^{-3} ohms. This Schottky rectifier is thus near ideal in its forward characteristics; having an "n" value close to unity, and exhibiting a series resistance very close to the bulk value. This diode has current handling capability greater than 100 amp since its epitaxial voltage drop is so small.

Diode 6-1-4, shown in Figure 78, was made on 2.9Ω-cm epitaxial material 12μ thick. The "n" value in this case is 1.07, and the measured ohmic series resistance is 6×10^{-3} ohms. This value, once again, corresponds very closely to the value of 5.8×10^{-3} ohms calculated from the resistivity and thickness of the epitaxy. A comparison of this diode with 2-15-3 shows how much more serious the parasitic epitaxial voltage drop is for this higher resistivity. Also shown in Figure 78 is the I-V characteristic of diode 17-1-(1, 3). This diode is quite similar in construction to 6-1-4. The epitaxy here is 3.2 ohm-cm 11.3μ thick, giving a diode epitaxial resistance of 6×10^{-3} ohms. The forward characteristic of this diode, however, is far from ideal. Current rises exponentially with applied voltage at the reasonable rate of 63.8 mv per decade for an "n" of 1.06. The measured series resistance in this case, however, is 25 milliohms.

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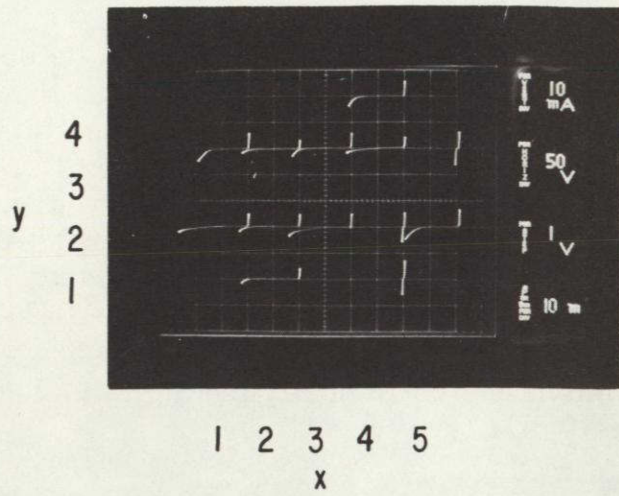
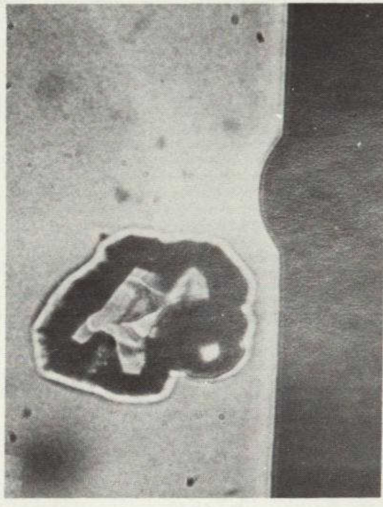


a) WAFER 17-1

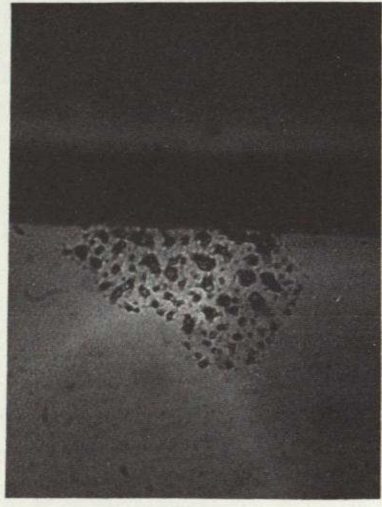
b) DIODE 5,3
CHIPPED
DIODE

(700X)



c) DIODE 4,1
GROWTH
HILLOCK

(700 X)



d) DIODE 4,2
EXTENDED
DEFECT
PRECIPITATES ?

(700X)

Figure 76. Wafer map of reverse diode characteristics for wafer 17-1 and photomicrographs of gross defects in shorted diodes

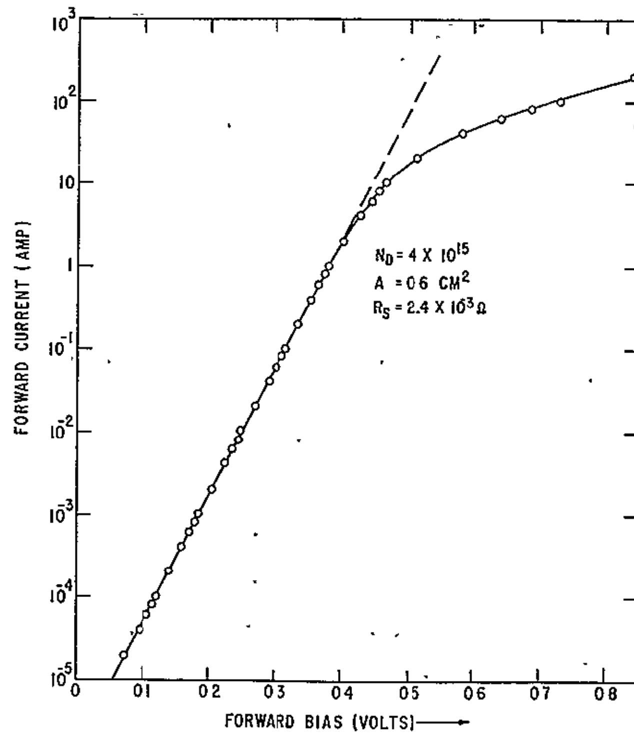


Figure 77. Forward bias I-V characteristics for relatively heavily doped diode 2-15-3

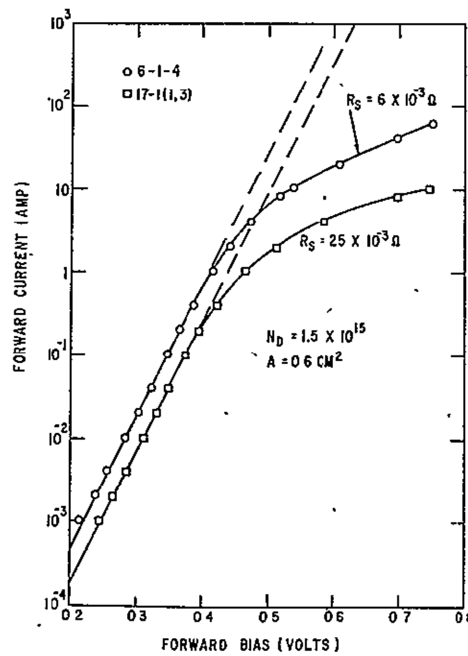


Figure 78. Forward I-V characteristics of two diodes demonstrating the effects of extra series resistance

There is clearly extra resistance in this rectifier over and above that of the epitaxial silicon which introduces very large parasitic voltage drops at high currents. At 10 amp, for example, the series drop for this rectifier is 250 mv, more than four times the proper value.

This additional resistance showed up on many, but not all, of the assembled Phase II diodes. Independent measurements of the epitaxial thickness and resistivity were made on test elements from most of the wafers that yielded finished, assembled diodes. Table VI lists these values and the epitaxial resistance, R_{epi}, derived from them together with the experimental values of R_s, the diode series resistance. As may be seen, the measured resistance for these diodes ran, on occasion, more than twice the values expected. The source of this difficulty and its erratic nature was identified by the series of experiments described in Section 6.14 above. The parasitic resistance was due to insufficient dopant at the back chip contact to permit tunneling to take place.

This problem was solved by the change to the all-solder assembly procedure described in Section 6.14 and by the care we took to maintain the dopant concentration at the wafer back at a value greater than 10^{20} cm^{-3}. Figure 79 is a histogram of the measured resistances of the approximately sixty, 50 ampere, Phase III diodes assembled in this way. The resistance

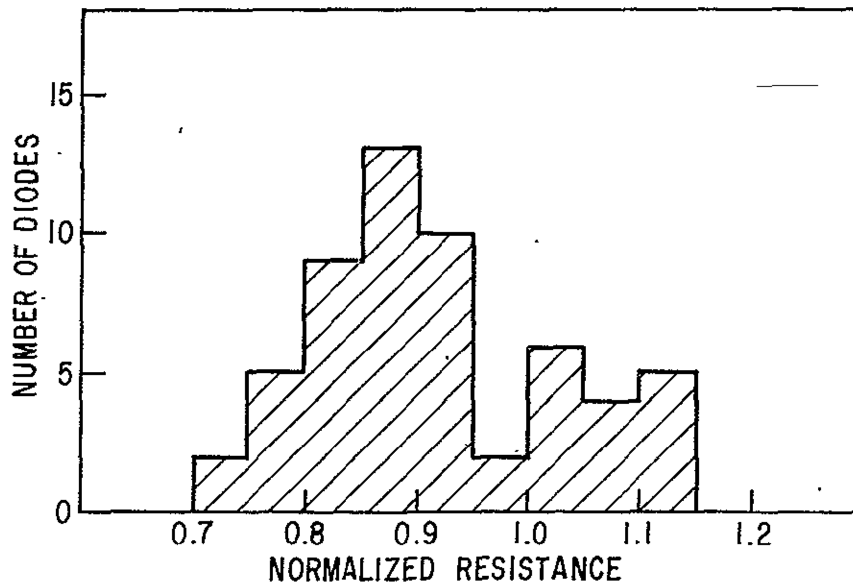


Figure 79. Distribution of normalized resistance for finally assembled Phase III diodes

TABLE VI

RESISTANCE OF MOUNTED DIODES

Diode No.	Measured Resistance (milliohm)	ρ (ohm-cm)	t (microns)	R_{epi} (milliohm)
1-34-2	2	0.77	11.5	1.5
1-34-3	2			
2-15-3	2.4	1	11	1.8
6-1-1	10	2.9	12	5.8
6-1-2	6			
6-1-3	6			
6-1-4	6			
6-1-6	7			
6-2-1	10	2.9	12	5.8
6-2-2	10			
6-3-2	8	2.9	11	5.3
6-3-3	8			
6-3-4	8			
6-3-6	7			
6-5-4	10	2.9	12	5.8
7-1-3	15	3.0	13	6.5
7-1-5	15			
7-4-1	13	3.0	13	6.5
7-4-2	9			
7-4-4	7			
7-4-6	9			
7-4-8	7			
7-5-1	9	3.0	13	6.5
7-5-2	7			
17-1(1,2)	16	3.2	11.3	6
17-1(1,3)	25			6
17-4(2,2)	15	3.4	11.5	6.5

was measured at 50 ampere forward current and was normalized to the value calculated from the measured epitaxial thickness and doping concentration. The results from the seven wafers represented here fall within 20 percent of the expected values. The resistances measured for diodes originating from

any single wafer were even more consistent, typically varying by no more than 5 percent.

The forward I-V characteristics of the 50 A Phase III diodes were very close to ideal. The measured values of current and bias followed the ideal thermionic expression,

$$I = I_s \left[\exp\left(\frac{qV}{nkT}\right) - 1\right]$$

to within the precision of measurement (1 percent in current and 2 mv in voltage) over the five decades of current from several microamps to several hundred milliamps where series resistance can be neglected. The values of n obtained are all quite close to 1.0. Their distribution is shown in Figure 80

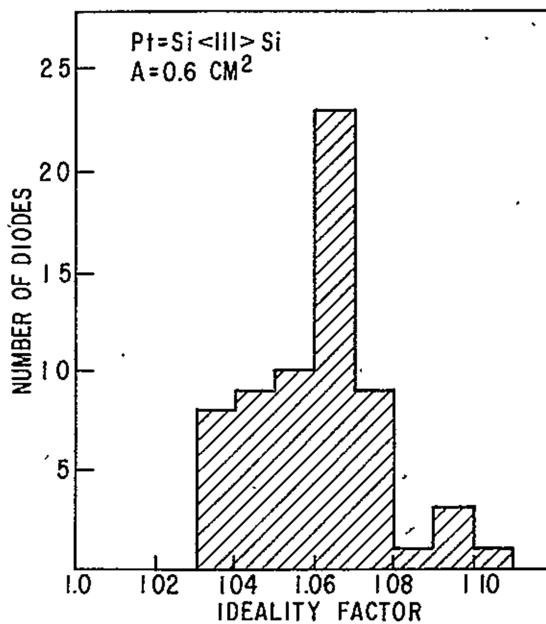


Figure 80. Distribution of "n"

7.3 Test Results

Each of the diodes delivered was characterized in both forward and reverse directions. The results for the Phase II diodes are presented in tabulated form in Table VII. Data presented are: (1) detailed current-voltage characteristics out to 40 amp forward; (2) measured value of diode series resistance; (3) calculated value of epitaxial resistance for those wafers

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TABLE VII

ELECTRICAL CHARACTERISTICS OF PHASE II DELIVERED DIODES

V (mv) (1) I (amp)	1-34-2	1-34-3	1-35-2	6-1-1	6-1-2	6-1-3	6-1-4	6-1-6	6-2-1	6-2-2	6-3-2	6-3-3	6-3-4
$1x10^{-3}$	225	236	214	221	170		215		229	231	215	221	234
2	247	256	238	247	210	214	236	164	248	248	249	247	253
4	266	274	257	268	242	244	257	218	266	266	279	271	273
$1x10^{-2}$	291	302	282	296	276	279	283	261	290	291	314	303	298
2	312	321	304	317	300	299	303	286	310	311	338	325	318
4	331	339	325	337	323	319	323	310	329	330	358	346	338
$1x10^{-1}$	355	364	347	363	348	345	347	338	354	355	386	373	363
2	374	383	367	384	368	364	367	357	373	374	407	394	382
4	399	402	387	405	389	384	387	378	394	395	429	415	404
$1x10^{0}$	421	429	416	437	419	414	416	408	424	426	459	445	434
2	442	450	440	467	450	440	442	435	450	453	486	471	459
4	465	474	468	510	475	472	474	467	484	488	522	506	494
8	495	504	503	572	522	519	519	514	535	540	565	553	542
10	507	512	522	600	539	537	538	534	554	561	584	571	560
20	549	552	584	710	638	610	610	607	635	643	649	642	634
40	615	614	674	865	694	695	697	694	730	740	724	724	718
(2) R_S (mΩ)	2	2	6	10	6	6	6	7	10	10	8	8	8
(3) R_{epi} (mΩ)	1.5	1.5		5.8	5.8	5.8	5.8	-5.8	5.8	5.8	5.3	5.3	5.3
(4) V (50 ma) 23°CM	76	66	86	112	110	115	105	104	95	110	117	108	102
(5) V (50) ~100°C						112		108		110	110	125	120
(6) V_{ext} (25 amp)	518	510	497	497	507	503	499	490	502	503	538	527	515
V_m	85	85		245							235		
f	.89	.78		.46	.45	.47	.43	.44			.50	.53	.51

V (mv) I (amp)	6-3-6	6-5-4	7-1-3	7-1-5	7-3-1	7-3-2	7-4-1	7-4-2	7-4-4	7-4-6	7-4-8	7-5-1	7-5-2
$1x10^{-3}$	222	226	212	203	149	217	206					206	227
2	244	244	230	224	202	248	238			221		230	249
4	266	262	249	242	228	272	263	231	254	256		254	269
$1x10^{-2}$	295	286	274	267	276	305	293	276	292	294		281	296
2	316	306	293	286	304	327	323	306	318	319	251	304	318
4	336	325	314	306	329	349	337	333	340	342	318	324	337
$1x10^{-2}$	362	350	339	334	360	376	364	362	368	369	351	350	362
2	381	370	359	354	384	399	385	384	389	390	376	370	388
4	403	391	381	377	414	425	408	407	412	414	400	392	403
1	433	424	407	414	446	466	443	440	443	445	433	424	434
2	458	463	448	448	514	512	476	469	469	474	460	454	460
4	491	491	493	496	592	576	525	508	506	514	494	492	495
8	538	548	542	570	708	675	596	561	554	566	542	550	546
10	556	570	593	602	750	717	628	584	574	589	562	575	566
20	628	660	718	725	907	858	742	670	650	680	638	676	648
40	708	762	895	870	1.080	1.022	884	778	739	785	724	814	743
R_S (mΩ)	7	10	15	15	30	22	13	9	7	9	7	9	7
R_{epi} (mΩ)	5 3	5.8	6.5	6.5			6.5	6.5	6.5	6.5	6.5	6.5	6.5
V (50 ma) 23°CM	120A	100	100	140	112	130	115	110	122	115		108	120
V (50) ·100°C	120A	104	105	105	110	125	108	106	108	110	110	110	120
V_{ext} (25A) mv	513	498	486	485	527	544	526	526	531	531	520	507	520
V_m							260				260		
f	.51						.44	.42	.47	.44	.42	.42	.46

measured: (4) the reverse bias at which the current is 50 ma at room temperature; (5) the reverse bias at which the current is 50 ma at temperatures greater than 100°C measured prior to final assembly; (6) the barrier drop at 25 amp forward obtained by subtracting the ohmic drop from the measured diode bias at 25 amp; (7) V_{max}, the theoretically maximum breakdown voltage, and (8) f, the ratio of V (50 ma) to V_{max}.

The results for the 50 A Phase III diodes are presented in tabulated form in Table VIII. The data presented here include: (1) the measured Schottky barrier height before and after capping; (2) n, the ideality factor; (3) measured ohmic resistance at 50 amp; (4) calculated ohmic resistance; (5) thermal impedance; (6) the detailed I-V characteristic from 10^{-5} amp to 50 amp; (7) V_m, the theoretical bulk breakdown value; and the measured values of reverse bias corresponding to 6 ma reverse leakage for the diodes; (8) in chip form; (9) after assembly; (10) after capping; (11) after capping and at 100°C.

The capping step had essentially no effect upon the diode forward characteristics. The barrier heights before and after capping of the diodes delivered are given in Table VIII and those of all the diodes assembled are shown in Figure 81. In almost all cases the change in ϕ came to less than 5 millivolts. The capping had no effect at all upon either the ideality factor or the series resistance.

We measured the thermal impedance (from barrier to stud) of some of the Phase III diodes. The results are given in Table VIII and Figure 82. Values obtained clustered about 0.2 (°C-cm^2/watt), less than twice the impedance expected from the tungsten backup plate. We thus conclude that our assembly procedure is a good one.

The distribution of barrier heights obtained with finished diodes is shown in Figure 83. Values appear to be uniformly spread over a 50 mv range. We have identified the source of this variability as non-uniform heating of wafers in the course of barrier formation or metallization. This may be seen explicitly in Figure 84 where diode barrier heights are plotted vs. position as one goes from left to right across the wafer. Higher barrier heights are associated with the left side of the wafer which is always hotter in our vacuum system due to radiative heating from the filament generating the plasma discharge. The barrier heights range upwards to the 0.85 appropriate to conventional platinum silicide. More uniform temperatures will tighten the distribution to 10 mv.

GENERAL ELECTRIC

TABLE VIII

ELECTRICAL CHARACTERISTICS OF PHASE III DELIVERED DIODES

Diode No.		Barrier Height (millivolt)		Ideality Factor	Measured Resistance at 50A (milliohms)	Calculated Resistance (milliohms)	Thermal Impedance (degrees-cm² / watt)	Foward Bias (mr) For Current in Amperes Shown Below										Reverse Bias for 6 ma (volts)				
								10^{-5}	10^{-4}	10^{-3}	10^{-2}	10^{-1}	1	10	20	40	50	Vm	Chip Form	Assembled	Capped T=25°C	Capped T=100°C
214-1	4,3	794		1.04	4.0	3.8		098	158	220	280	337	412	529	602	700	740	160	110	120	100	105
214-6	1,3		793	1.10				103	165	232	297	363	442	568	625	710	730	155	98	105	105	110
	3,3	790	794	1.03	4.1	3.7	.19	98	157	219	280	343	410	522	590	690	710					107
215-1	3,2	792	800	1.06	4.2	4.0		101	165	228	290	347	422	538	610	710	740	160	100	100	105	100
	4,4	794	792	1.03	4.0		.22	096	156	218	278	341	409	516	582	680	710		85	100	88	112
	5,2	797	804	1.04	4.0			100	162	226	288	352	422	540	608	710	730		98	110	110	105
	5,3	793	804	1.05	4.1			110	170	233	295	358	428	544	612	700	730		100	100	100	102
215-2	2,1	828	841	1.06	3.8	4.4		150	213	274	338	401	469	581	645	730	750	165	120	105	105	120
	2,2	842	843	1.06	3.8			152	214	276	340	397	473	587	650	730	760		110	110	100	103
	3,2	827	827	1.06	4.0		.18	134	196	259	323	386	457	575	644	720	760		110	115	105	110
	3,3	812	814	1.05	4.2			120	181	243	305	368	438	554	624	710	730		110	120	120	>120
	4,1	826	836	1.06	3.6			145	207	269	333	397	466	579	642	720	760		120	120	110	>110
	4,3	804	807	1.04	4.0			111	171	233	295	357	426	537	605	700	730		110	110	120	>120
	5,2	813	811	1.06	3.7		.18	118	179	242	305	369	439	555	624	710	740		100	110	105	110
215-3	1,3		842	1.05	2.7	3.3		149	211	272	334	396	462	558	605	670	690	170	105	110	105	116
	2,3		836	1.06	2.5			146	208	270	335	398	467	568	618	674	694		115	100	110	106
	2,4		838	1.06	2.5			147	210	272	336	399	464	560	612	670	694		100	100	100	>100
	3,2		825	1.09	2.4			137	200	267	332	396	466	565	615	672	693		110	100	105	110
	4,3		813	1.06	2.9			121	182	245	308	371	440	541	596	664	685		115	115	100	115
	4,4	833	835	1.05	2.7		.24	142	204	266	330	394	462	568	622	690	720		105	115	110	>110
	5,2		808	1.07	2.9			116	178	242	305	369	438	536	590	660	683		100	100	100	105
215-4	1,2		821	1.06	2.9	3.4		129	190	253	316	379	447	545	596	660	690	170	90	100	95	100
	2,1		816	1.09	2.6			125	191	255	319	383	452	548	595	660	680		95	95	95	102
	2,3		817	1.09	2.9			118	181	246	312	376	447	545	605	670	700		105	105	110	>110
	3,2	814	810	1.06	3.1			120	180	243	304	367	436	536	589	660	680		105	105	95	99
	5,3		820	1.06	3.0			129	190	253	317	380	449	549	602	670	700		100	105	105	110
217-3	1,2	845	842	1.07	3.1	3.6	.24	152	216	278	342	406	475	584	638	705	730	160	110	110	110	120
	1,3	844	840	1.07	3.2		.20	149	213	275	338	402	471	579	636	700	730		105	110	115	110
	3,5	834	830	1.06	3.1		.21	137	199	262	325	389	457	558	612	690	710		95	95	95	102
	4,3		845	1.06	3.3		.37	153	211	278	343	406	475	580	635	705	730		105	110	110	115
	4,4		845	1.06			.25	154	217	278	343	406	475	580	640	705	730		100	100	100	105

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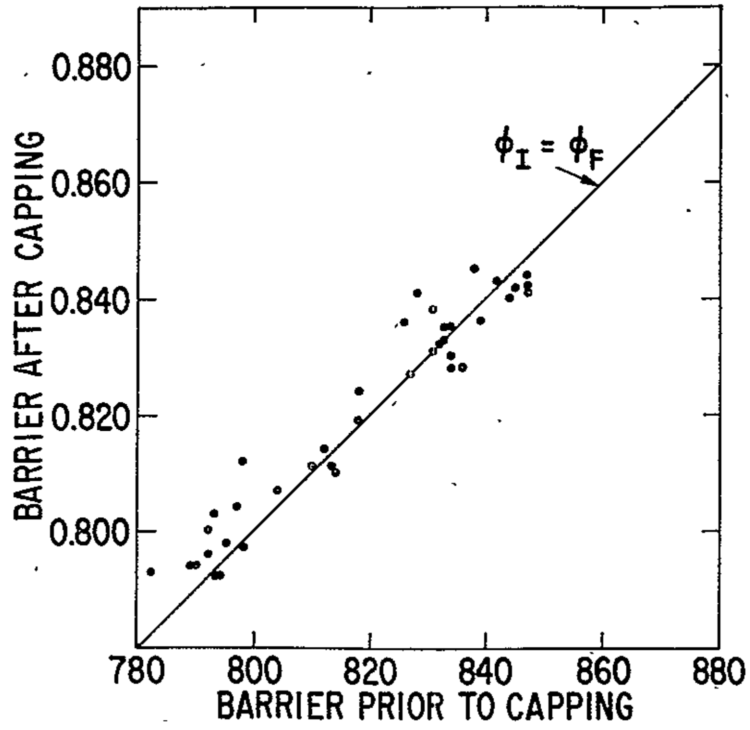

Figure 81. Barrier heights for assembled diodes before and after capping

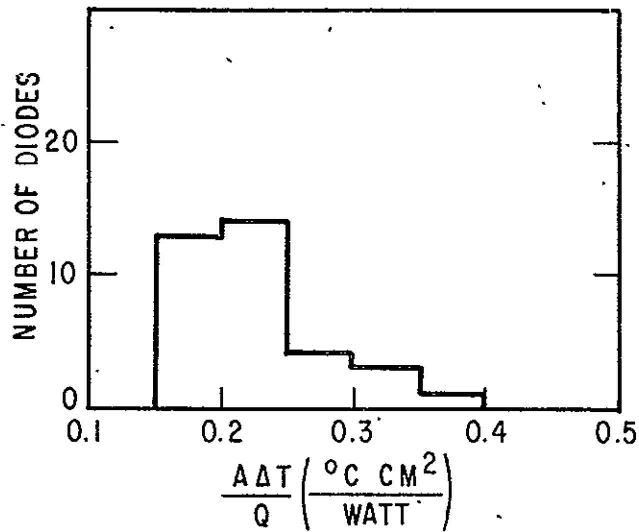

Figure 82. Thermal impedance for finished Phase III diodes

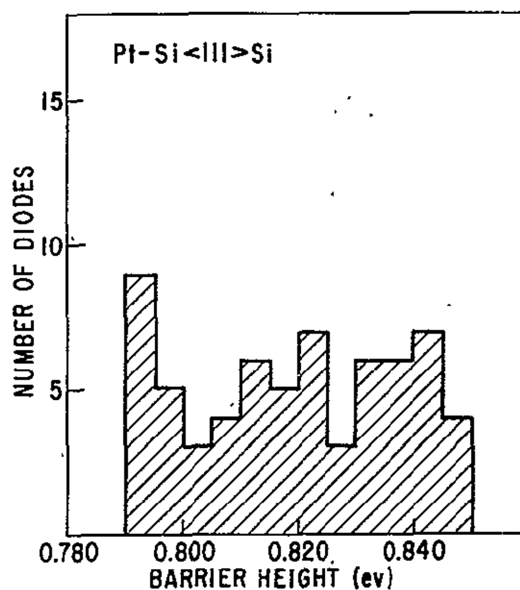

Figure 83. Distribution of barrier heights obtained with 0.6 cm^2 diodes

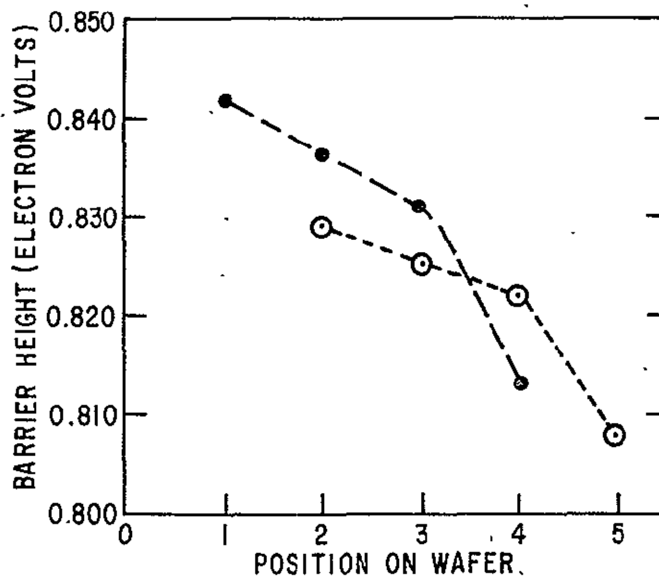

Figure 84. Variation of barrier height across the wafer

Section 8

REVERSE RECOVERY TIME

It is extremely difficult to measure short recovery times at large current values. We therefore did not measure the reverse recovery times of the final large rectifiers. We did, however, measure recovery times for several smaller (10^{-2} cm^2) mesa Schottky rectifiers that were processed in exactly the same manner as were the large diodes. These measurements were made at current density equal to or greater than the 42 amp/cm^2 corresponding to the rated 25 amp of the large diodes. A typical result is shown in Figure 85. The circuit used for the measurement is also shown. The diode header used was not properly matched to 50Ω, so severe reflections are seen. Nevertheless, there is a small difference between the zero reverse bias and the 10 volt reverse bias current waveforms.

The -10 volt curve lies below the zero bias curve after the forward current pulse ends indicating a small amount of charge being swept out by the -10 volt reverse bias. There is thus some small amount of minority carrier insertion. This reverse recovery current is, however, gone within 20 to 30 nsec.

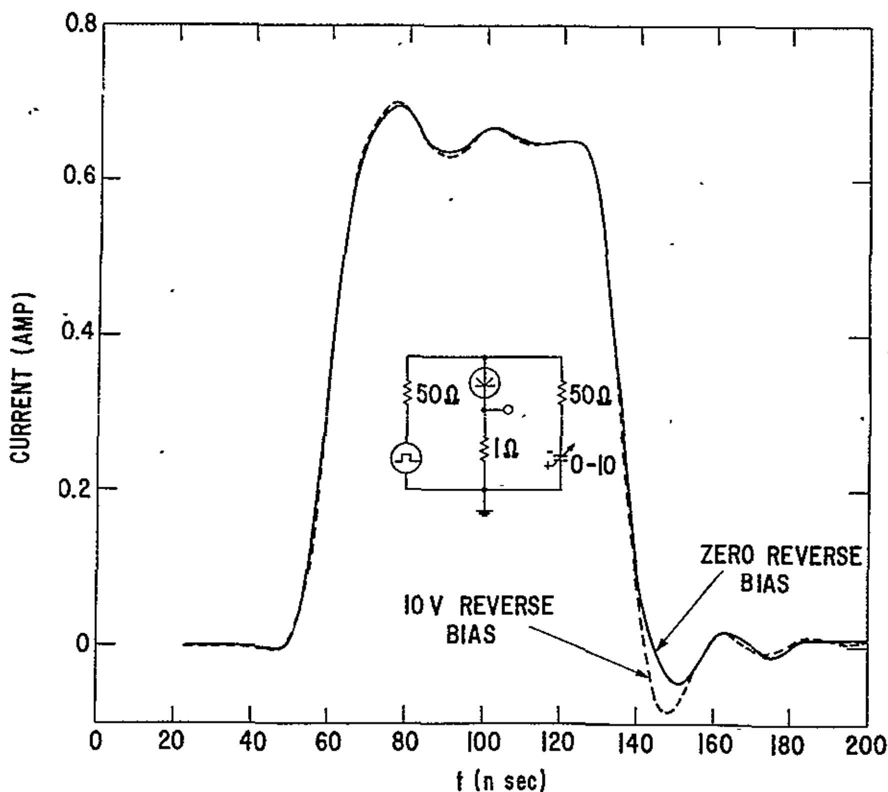

Figure 85. Reverse recovery after 60 A/cm^2 forward pulse

Section 9

SUMMARY AND CONCLUSIONS

Our progress in Schottky diode development to date may be summarized as follows:

9.1 Barrier Fabrication

We have developed manufacturable, reproducible methods for fabricating Schottky diodes and for the metals W, Al, low temperature Pt-Si and conventional Pt-Si.

9.2 Barrier Height Measurements

Barrier heights for the above metals have been determined for the major crystallographic directions of n-silicon.

9.3 Barrier Lowering

Barrier lowering under reverse bias for W, Al, and low temperature Pt-Si has been measured allowing us to accurately predict reverse junction leakage for any specific diode design.

9.4 Processing

We have developed a processing sequence which results in the fabrication, at high yields, of large area ($0.6\ cm^2$), high-quality, mesa geometry Schottky diodes exhibiting only thermionic leakage current. This process has worked successfully on several different lots of epitaxial material obtained from several sources.

9.5 Practical Breakdown Values

Test data for large area mesa diodes show that under practical processing conditions avalanche breakdown occurs at reverse voltages that are between 50 and 80 percent of the theoretical values. The value of 70 percent represents a practical design limit.

9.6 Effects of Assembly on Reverse Characteristics

We have demonstrated the feasibility of an assembly procedure which does not degrade the reverse characteristics of near ideal Schottky pellets of large area.

9.7 Diode Resistance

We have demonstrated that it is feasible and practical to assemble power Schottky diodes exhibiting ohmic resistance within a few percent of the theoretical epitaxial value.

9.8 Effects of Assembly on Forward Characteristics

We have developed an assembly procedure which reproducibly yields low resistance contacts to large area Schottky pellets.

9.9 Applications Areas

A theoretical study has been performed which broadly indicates the range of voltage and frequency for which Schottky power rectifiers are more efficient than junction devices.

Section 10

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