MDC E1208

ACCELERATED TEST TECHNIQUES FOR MICROCIRCUITS

Evaluation of High Temperature (473°K — 573°K) Accelerated Life Test Techniques as Effective Microcircuit Screening Methods

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24 January 1975

Final Technical Report for Period July 1973 — December 1974

Prepared for

Goddard Space Flight Center
Greenbelt, Maryland 20771

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
4. Title and Subtitle ACCELERATED TEST TECHNIQUES FOR MICROCIRCUITS - Evaluation of High Temperature (473°K - 573°K) Accelerated Life Test Techniques as Effective Microcircuit Screening Methods		5. Report Date 6. Performing Organization Code
7. Author(s) G. M. Johnson		8. Performing Organization Report No. MDCE 1208
9. Performing Organization Name and Address McDonnell Douglas Astronautics Company-East P.O. Box 516 St. Louis, Missouri 63166		10. Work Unit No. 11. Contract or Grant No. NAS5-22233
12. Sponsoring Agency Name and Address GODDARD SPACE FLIGHT CENTER GREENBELT, MARYLAND 20771 W. KAGDIS, TECHNICAL MONITOR		13. Type of Report and Period Covered Final Technical Report January 1975 14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

The application of high temperature accelerated test techniques was shown to be an effective method of microcircuit defect screening. Comprehensive microcircuit evaluations and a series of high temperature (473°K to 573°K) life tests demonstrated that a freak or early failure population of surface contaminated devices could be completely screened in thirty two hours of test at an ambient temperature of 523°K. Equivalent screening at 398°K, as prescribed by current Military and NASA specifications, would have required in excess of 1500 hours of test. All testing was accomplished with a Texas Instruments' 54L10, low power triple-3 input NAND gate manufactured with a Titanium-Tungsten (Ti-W), Gold (Au) metallization system. A number of design and/or manufacturing anomalies were also noted with the Ti-W, Au metallization system. Further study of the exact nature and cause(s) of these anomalies is recommended prior to the use of microcircuits with Ti-W, Au metallization in long life/high reliability applications.

17. Key Words (Selected by Author(s))	18. Distribution Statement
RELIABILITY MICROCIRCUITS ACCELERATED LIFE TESTING	

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
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PREFACE

The primary objective of the work described herein was to evaluate the merits of a proposed, more cost effective method of microcircuit screening. The screening method evaluated incorporated high temperature (473°K to 573°K) accelerated life test techniques. A Texas Instruments' 54L10, low power, triple-3 input NAND gate, manufactured with a Titanium-Tungsten (Ti-W), Gold (Au) metallization system was utilized as the test vehicle. Program objectives were achieved through detailed initial device evaluations which led to the selection of a life test circuit suitable for safe microcircuit operation at junction temperatures up to 556°K, and a series of 4000 hour high temperature life tests. Five life tests of devices at junction temperatures between 477°K and 556°K were conducted to determine device failure distributions, life acceleration factors and the relative effectiveness of high temperature burn-in versus MIL-M-38510, Class B burn-in and NASA 85M03766, Class SM burn-in. Results of the life tests indicated that a short (32 hour) burn-in at an ambient temperature above 473°K is more effective for screening of surface related failure mechanisms than either the M38510 or NASA 85M03766 burn-in methods. Numerous design and/or manufacturing anomalies that are unique to the Ti-W, Au metallization system were also detected. Due to the nature and extent of these anomalies, further study of the observed failure mechanism(s) and cause(s) is recommended prior to use of microcircuits with Ti-W, Au metallization in long life/high reliability applications.

The work described in this report was performed by the Parts Evaluation Laboratory section of the McDonnell Douglas Astronautics Company - East (MDAC-E) Engineering Reliability Department during the period between July 1973 and December 1974. The basic work was performed for the National Aeronautics and Space Administration, Goddard Space Flight Center under Contract Number NAS5-22233. The NASA Technical Monitor is Mr. W. Kagdis. Supplementary data reduction and failure analysis activities described in the report, especially the study of gold penetration failures, were not charged to this contract.

Significant technical contributions were made by Messrs. Robert Clay, Chester Densmore, Bruce Kirk, Ed Sisul, Morton Stitch and Robert Watson of the MDAC-E Engineering Reliability Department.

The author would also like to thank Mr. Joseph Brauer, Dr. Robert Thomas, Mr. Jack Bart and Mr. Clyde Lane of the USAF Rome Air Development Center for their assistance on this program.

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1.0 INTRODUCTION

Accelerated testing of microcircuits in the 473°K to 573°K temperature range has been proposed as a more effective method of microcircuit screening than the currently specified methods in MIL-M-38510 and NASA specification 85M03766. To evaluate the effectiveness of High Temperature Operating Tests (HTOT) as a microcircuit screening method, a series of 4000 hour high temperature life tests was performed with Texas Instruments' 54L10 low power, TTL, NAND Gates manufactured with a Ti-W, Au, Ti-W metallization system. Specific objectives of the life test program were to obtain:

a) a high temperature screening method for the 54L10 microcircuit,

b) comparative life data on 54L10 microcircuits screened to:
   - o NASA/MSFC 85M03766, Class SM requirements
   - o MIL-M-38510, Class B requirements, and
   - o modified M38510, Class B requirements where the 398°K burn-in is replaced with a high temperature (473°K to 573°K) burn-in,

c) the failure distribution and failure accelerating factors associated with 54L10 microcircuits

d) failure mechanism information that is unique to the Ti-W, Au, Ti-W metallization system

2.0 PROGRAM DESCRIPTION

The Accelerated Test Techniques for Microcircuits Program consisted of six interrelated test phases as depicted in Figure 1. Major test objectives were achieved from the series of 4000 hour high temperature life tests conducted during Phases C and E. However, the evaluations and tests performed during Phase B to establish nondestructive electrical and thermal life test conditions were a necessary prerequisite to the Phase C and E testing.

To evaluate the effects of different processing/screening requirements, devices were procured from Texas Instruments during Phase A to the following specification requirements:

PART NO.	SPECIFICATION
SN54L10T	Commercial Product
SNM54L10T	M38510/20-03, Class B, less burn-in
SNC54L10T	M38510/20-03, Class B
SM54L10F1	NASA 85M03766, Class SM

The allocation of devices, by part number, to each of the tests conducted during the program, and the interrelationships of the various tests are shown in Figure 2. The primary purpose of each test is listed in Table 1.

All devices were initially tested at 298°K prior to performing any other tests or evaluations. Devices intended for the Phase E, Screening Comparison Test, were also electrically tested at 398°K and 218°K. Prior to performing the Phase C and E life tests, preliminary studies were performed in Phase B to obtain baseline

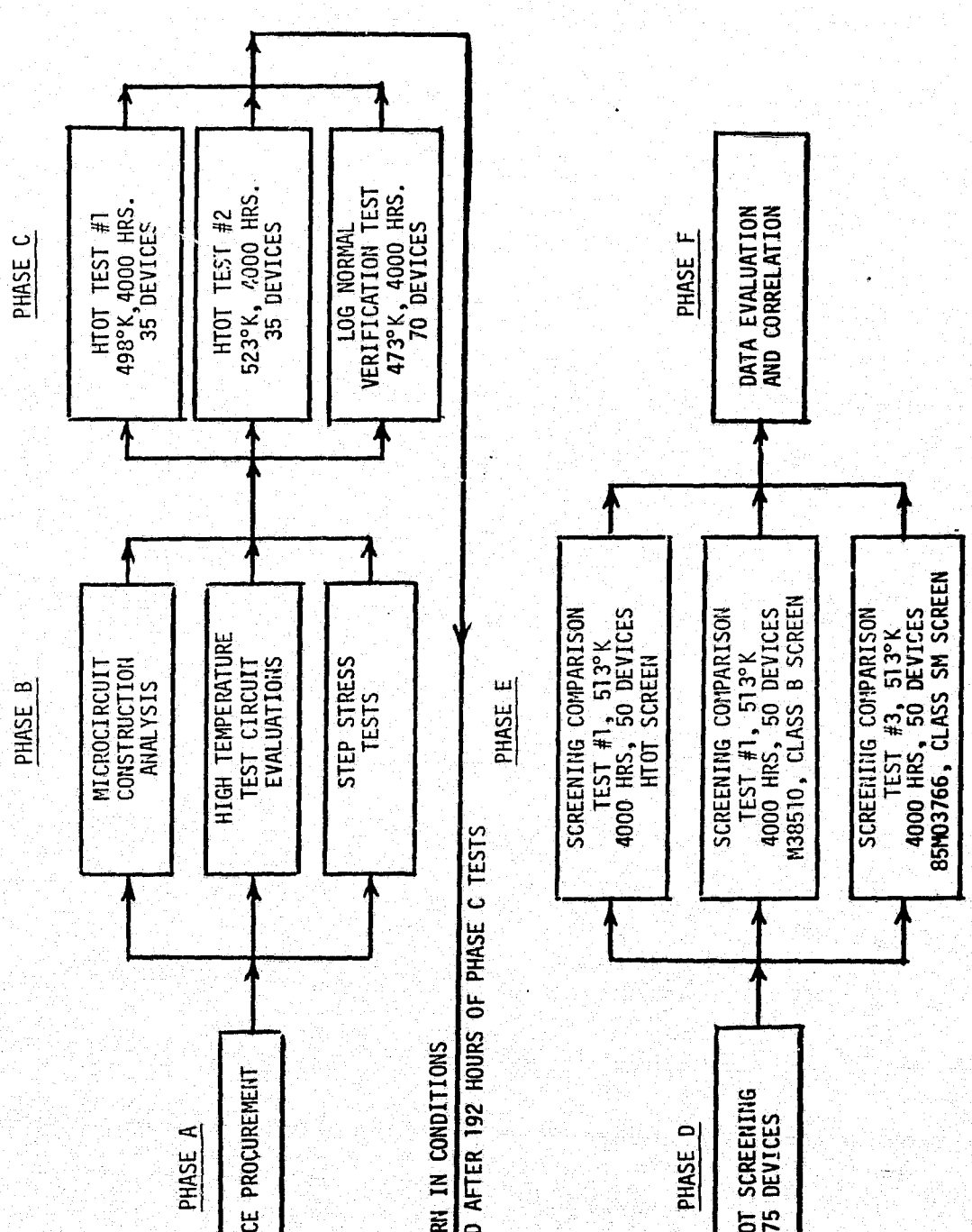


FIGURE 1. PROGRAM WORK FLOW

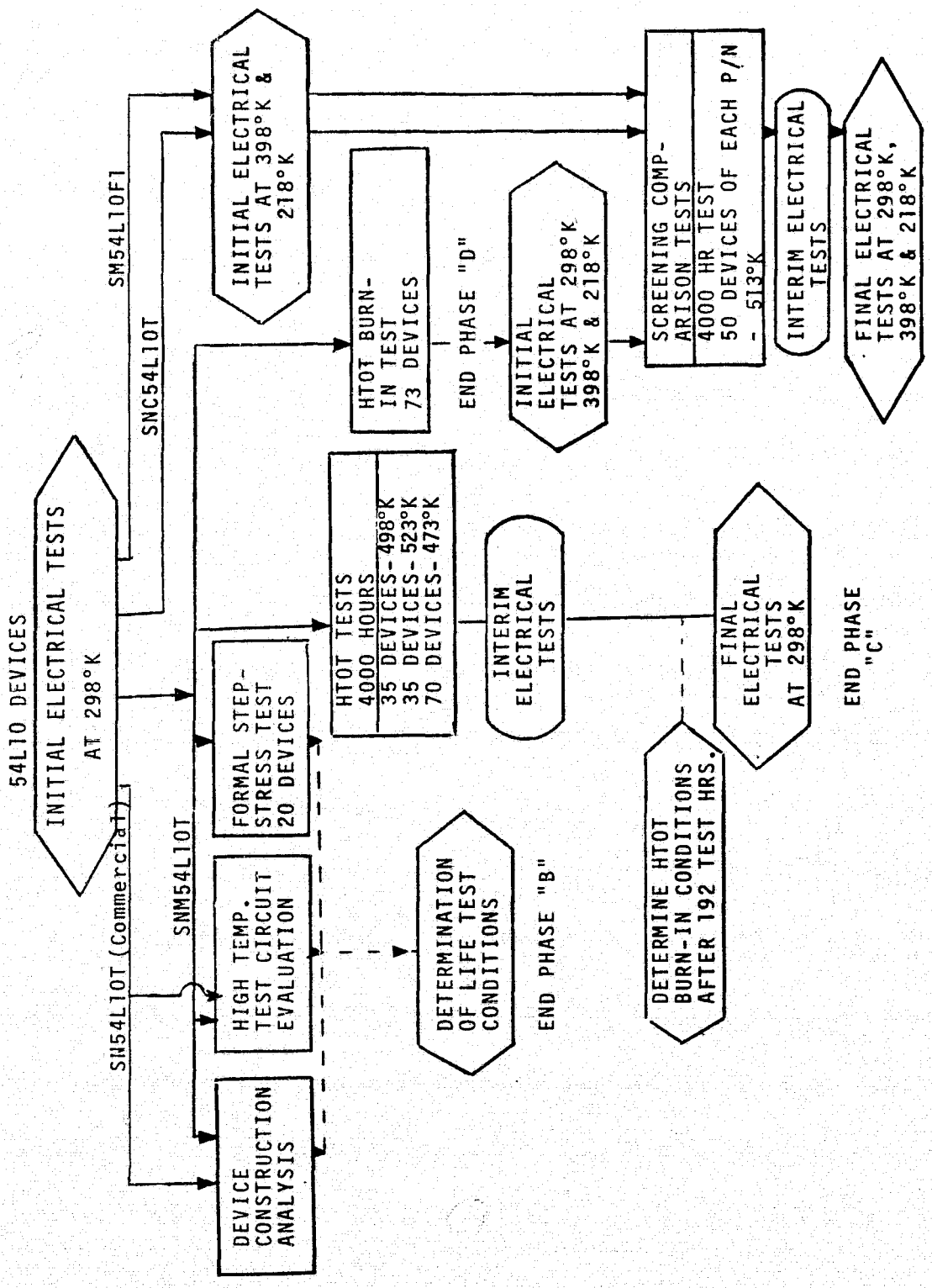


FIGURE 2. TEST PROGRAM OVERVIEW

TEST PHASE	TEST IDENTIFICATION	PRIMARY PURPOSE
B, C, D, E	Initial Electrical Tests	Provide baseline parameter information on delivered devices.
B, C, D, E	Interim/Final Electrical Tests	Verify operating condition of devices on test
B	Device Construction Analysis	Provide baseline information for high temperature test circuit evaluation and device failure analysis.
B	High Temperature Test Circuit Evaluation	Establish a high temperature life test circuit that is nondestructive to devices under test. Also provide information for device thermal characterization.
B	Formal Step-Stress	Provide data for determination of HTOT and Screening Comparison Test temperatures.
C	HTOT Tests Subgroups #1 and #2	Provide data points for computing device acceleration factors.
	Subgroup #3	Provide sufficient data to evaluate assumption that the distribution of device failure times is log normal.
D	HTOT Burn-In Test	Provide HTOT burned-in devices for the Screening Comparison Test.
E	Screening Comparison Test	Evaluation of the effectiveness of HTOT screening vs. M38510, Class B screening, vs. 85M03766, Class SM screening.

TABLE 1. PRIMARY PURPOSE OF TESTS

information on device construction, thermal characteristics, and to establish a nondestructive life test circuit. A formal step-stress test with twenty of the SNM54L10T devices was also performed as a final check of the circuit selected and to provide information necessary to select the Phase C life test temperatures. Based on the results of the step stress test, Phase C life test temperatures of 473°K, 498°K and 523°K were selected, and the Phase C, HTOT tests commenced. These tests consisted of two subgroups of 35 devices at ambient temperatures of 498°K and 523°K. A third subgroup of 70 devices was also tested at 473°K. Each subgroup was tested for 4000 hours. Interim Electrical Tests at 298°K were performed periodically on the devices in each subgroup after cool down with bias applied.

Upon completion of 192 test hours, the available data was analyzed to select an appropriate burn-in time and temperature for the Phase D HTOT Burn-in Test. Seventy three SNM54L10T devices were burned-in for thirty two hours at an ambient temperature of 498°K to obtain 50 good devices (Subgroup E1) for the Phase E Screening Comparison Test. The other Phase E subgroups consisted of 50 SNC54L10T devices (Subgroup E2) and 50 SM54L10F1 devices (Subgroup E3). Each subgroup was tested at an ambient temperature of 513°K for 4000 hours.

2.1 Device Electrical Tests

Device Electrical Tests were comprised of a combination of selected sets of M38510, Group A tests and 85M03766-010 tests. The sets of tests are categorized as Initial, Interim and Final. Initial tests were performed prior to placing devices in test subgroups and consisted of the DC parameter measurements shown in Table 2. The Interim tests shown in Table 3 were performed on a scheduled basis during the 4000 hour life tests to verify device operating condition. All Interim Tests were performed at 298°K after cool down under bias at the following intervals:

TEST GROUP	INTERIM ELECTRICAL TEST SCHEDULE
HTOT #1, HTOT #2 and Screening Comparison Tests	4, 8, 16, 32, 64, 128, 256, 512, 1000, and 2500 hours
Log Normal Verification Test	4, 8, 16, 32, 48, 64, 96, 128, 192, 256,384, 512 768, 1000, 1500, 2000, and 3000 hours

At the conclusion of Step-Stress Tests and Life Tests, surviving devices were subjected to the Final Electrical Test which consisted of the same electrical parameter tests as the Initial Electrical Test.

A device was considered to be failed if any of its electrical parameters exceed the limits specified in Tables 2 or 3.

3.0 PROGRAM RESULTS

3.1 Phase B - Device Evaluations

The series of device evaluations and tests performed in preparation for the series of 4000 hour HTOT and Screening Comparison Tests is shown in Figure 3. Most of the device evaluations were performed with commercial grade and M38510, Class B, less burn-in, devices. Since construction details and electrical performance of

SYMBOL	PIN UNDER TEST	TERMINAL CONDITIONS (NOTES 1 & 2)	LIMITS MIN.	LIMITS MAX.	UNITS
VOL	3	VIH1-1,2,14;VCCL-4;IOL-3;GND-11		0.3	V_{DC}
VOL	5	VIH1-6,7,8;VCCL-4;IOL-5;GND-11		0.3	V_{DC}
VOL	13	VIH1-9,10,12;VCCL-4;IOL-13;GND-11		0.3	V_{DC}
VOH	3	VIL1-1,VCCL-2,4,14;IOH-3;GND-11	2.4		V_{DC}
VOH	3	VIL1-2;VCCL-1,4,14;IOH-3;GND-11	2.4		V_{DC}
VOH	3	VIL1-14;VCCL-1,2,4;IOH-3;GND-11	2.4		V_{DC}
VOH	5	VIL1-6;VCCL-4,7,8;IOH-5;GND-11	2.4		V_{DC}
VOH	5	VIL1-7;VCCL-4,6,8;IOH-5;GND-11	2.4		V_{DC}
VOH	5	VIL1-8;VCCL-4,6,7;IOH-5;GND-11	2.4		V_{DC}
VOH	13	VIL1-9;VCCL-4,10,12;IOH-13;GND-11	2.4		V_{DC}
VOH	13	VIL1-10;VCCL-4,9,12;IOH-13;GND-11	2.4		V_{DC}
VOH	13	VIL1-12;VCCL-4,9,10;IOH-13;GND-11	2.4		V_{DC}
VOO	3	VIL2-1;VCCL-2,14;VCC-4;GND-11	3.2		V_{DC}
VOO	5	VIL2-6;VCCL-7,8;VCC-4;GND-11	3.2		V_{DC}
VOO	13	VIL2-9;VCCL-10,12;VCC-4;GND-11	3.2		V_{DC}
IOS	3	VCCH-4;GND-1,2,3,11,14	-3	-15	mA
IOS	5	VCCH-4;GND-5,6,7,8,11	-3	-15	mA
IOS	13	VCCH-4;GND-9,10,11,12,13	-3	-15	mA
IIH1	1	VIH2-1,VCCH-4;GND-2,11,14,6,7,8,9,10,12		0.01	mA
IIH2	1	VCCH-1,4;GND-2,11,14,6,7,8,9,10,12		0.1	mA
IIH1	2	VIH2-2;VCCH-4;GND-1,11,14,6,7,8,9,10,12		0.01	mA
IIH2	2	VCCH-2,4;GND-1,11,14,6,7,8,9,10,12		0.1	mA
IIH1	14	VIH2-14;VCCH-4;GND-1,2,11,6,7,8,9,10,12		0.01	mA
IIH2	14	VCCH-4,14;GND-1,2,11,6,7,8,9,10,12		0.1	mA
IIH1	6	VIH2-6;VCCH-4;GND-7,8,11,1,2,14,9,10,12		0.01	mA
IIH2	6	VCCH-4,6;GND-7,8,11,1,2,14,9,10,12		0.1	mA
IIH1	7	VIH2-7;VCCH-4;GND-6,8,11,1,2,14,9,10,12		0.01	mA
IIH2	7	VCCH-4,7;GND-6,8,11,1,2,14,9,10,12		0.1	mA
IIH1	8	VIH2-8;VCCH-4;GND-6,7,11,1,2,14,9,10,12		0.01	mA
IIH2	8	VCCH-4,8;GND-6,7,11,1,2,14,9,10,12		0.1	mA
IIH1	9	VIH2-9;VCCH-4;GND-10,11,12,1,2,14,6,7,8		0.01	mA
IIH2	9	VCCH-4,9;GND-10,11,12,1,2,14,6,7,8		0.1	mA
IIH1	10	VIH2-10;VCCH-4;GND-9,11,12,1,2,14,6,7,8		0.01	mA
IIH2	10	VCCH-4,10;GND-9,11,12,1,2,14,6,7,8		0.1	mA
IIH1	12	VIH2-12;VCCH-4;GND-9,10,11,1,2,14,6,7,8		0.01	mA
IIH2	12	VCCH-4,12;GND-9,10,11,1,2,14,6,7,8		0.1	mA
IIL	1	VIL2-1;VCCL-2,14;VCCH-4;GND-11		-0.18	mA
IIL	2	VIL2-2;VCCL-1,14;VCCH-4;GND-11		-0.18	mA
IIL	14	VIL2-14;VCCL-1,2;VCCH-4;GND-11		-0.18	mA
IIL	6	VIL2-6;VCCL-7,8;VCCH-4;GND-11	-0.18	-0.18	mA
IIL	7	VIL2-7;VCCL-6,8;VCCH-4;GND-11		-0.18	mA
IIL	8	VIL2-8;VCCL-6,7;VCCH-4;GND-11		-0.18	mA
IIL	9	VIL2-9;VCCL-10,12;VCCH-4;GND-11		-0.18	mA
IIL	10	VIL2-10;VCCL-9,12;VCCH-4;GND-11		-0.18	mA
IIL	12	VIL2-12;VCCL-9,10;VCCH-4;GND-11		-0.18	mA
IPD	4	VCC-1,2,6,7,8,9,10,12,14;VCCH-4;GND-11		1.53	mA
IMAX	4	VCCH-4;GND-1,2,6,7,8,9,10,11,12,14		0.6	mA

NOTES:

1. ALL UNUSED INPUTS MUST BE CONNECTED TO LOGIC "1" VOLTAGE
2. SYMBOLS

IOL	2.0mA	VCCH	$5.5V_{DC}$	VIH2	$2.4V_{DC}$
IOH	-0.1mA	VCCL	$4.5V_{DC}$	VIL1	$0.7V_{DC}$
VCC	$5.0V_{DC}$	VIH1	2.0VDC	VIL2	$0.3V_{DC}$

TABLE 2. INITIAL AND FINAL ELECTRICAL MEASUREMENTS

SYMBOL	PIN UNDER TEST	TERMINAL CONDITIONS (NOTES 1 & 2)	LIMITS MIN.	LIMITS MAX.	UNITS
VOL	3	VIH1-1,2,14;VCCL-4;IOL-3;GND-11 [1]		0.3	V_{DC}
VOL	5	VIH1-6,7,8;VCCL-4;IOL-5;GND-11 [1]		0.3	V_{DC}
VOL	13	VIH1-9,10,12;VCCL-4;IOL-13;GND-11 [1]		0.3	V_{DC}
VOH	3	VIL1-1;VCCL-2,4,14;IOH-3;GND-11 [1]	2.4		V_{DC}
VOH	5	VUK1-6;VCCL-4,7,8;IOH-5;GND-11 [1]	2.4		V_{DC}
VOH	13	VIL1-9;VCCL-4,10,12;IOH-13;GND-11 [1]	2.4		V_{DC}
IOS	3	VCCH-4;GND-1,2,3,11,14	-3	-15	mA
IOS	5	VCCH-4;GND-5,6,7,8,11	-3	-15	mA
IOS	13	VCCH-4;GND-9,10,11,12,13	-3	-15	mA
IIH1	1	VIH2-1;VCCH-4;GND-2,11,14,6,7,8,9,10,12		0.01	mA
IIH1	2	VIH2-2;VCCH-4;GND-1,11-14,6,7,8,9,10,12		0.01	mA
IIH1	14	VIH2-14;VCCH-4;GND-1,2,11,6,7,8,9,10,12		0.01	mA
IIH1	6	VIH2-6;VCCH-4;GND-7,8,11,1,2,14,9,10,12		0.01	mA
IIH1	7	VIH2-7;VCCH-4;GND-6,8,11,1,2,14,9,10,12		0.01	mA
IIH1	8	VIH2-8;VCCH-4;GND-6,7,11,1,2,14,9,10,12		0.01	mA
IIH1	9	VIH2-9;VCCH-4;GND-10,11,12,1,2,14,6,7,8		0.01	mA
IIH1	10	VIH2-10;VCCH-4;GND-9,11,12,1,2,14,6,7,8		0.01	mA
IIH1	12	VIH2-12;VCCH-4;GND-9,10,11,1,2,14,6,7,8		0.01	mA
IIL	1	VIL2-1;VCCL-2,14;VCCH-4;GND-11 [1]		-0.18	mA
IIL	2	VIL2-2;VCCL-1,14;VCCH-4;GND-11 [1]		-0.18	mA
IIL	14	VIL2-14;VCCL-1,2;VCCH-4;GND-11 [1]		-0.18	mA
IIL	6	VIL2-6;VCCL-7,8;VCCH-4;GND-11		-0.18	mA
IIL	7	VIL2-7;VCCL-6,8;VCCH-4;GND-11 [1]		-0.18	mA
IIL	8	VIL2-8;VCCL-6,7;VCCH-4;GND-11 [1]		-0.18	mA
IIL	9	VIL2-9;VCCL-10,12;VCCH-4;GND-11 [1]		-0.18	mA
IIL	10	VIL2-10;VCCL-9.12;VCCH-4;GND-11 [1]		-0.18	mA
IIL	12	VIL2-12;VCCL-9,10;VCCH-4;GND-11 [1]		-0.18	mA
IPD	4	VCC-1,2,6,7,8,9,10,12,14;VCCH-4;GND-11		1.53	mA
IMAX	4	VCCH-4;GND-1,2,6,7,8,9,10,11,12,14		0.6	mA

NOTES:

1. ALL UNUSED INPUT MUST BE CONNECTED TO LOGIC "1" VOLTAGE

2. SYMBOLS

IOL	2.0mA	VCCH	$5.5V_{DC}$	VIH2	$2.4V_{DC}$
IOH	-0.1mA	VCCL	$4.5V_{DC}$	VIL1	$0.1V_{DC}$
VCC	$5.0V_{DC}$	VIH1	$2.0V_{DC}$	VIL2	$0.3V_{DC}$

TABLE 3. INTERIM ELECTRICAL MEASUREMENTS

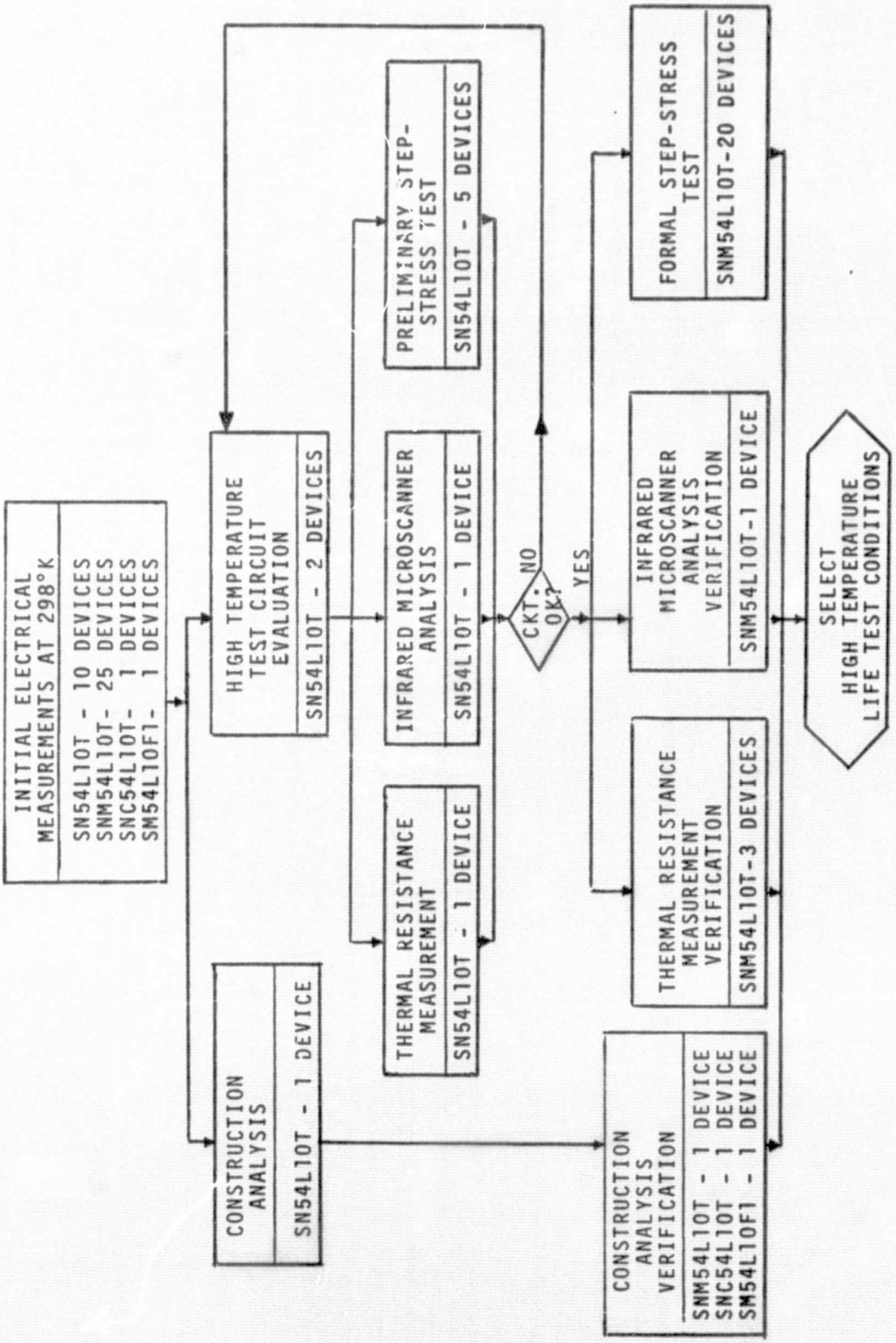


FIGURE 3. PHASE "B" TESTING

all devices should be identical, only those analyses were performed that were necessary to verify that the M38510, Class B and 85M03766, Class SM, devices were the same as the M38510, Class B, less burn-in, devices.

3.1.1 Microcircuit Construction Analysis - A detailed examination of both the external and internal features of the microcircuit was performed to detect design and construction details that could affect the life test results, and to facilitate subsequent failure analysis activities. Significant device construction features, including the Ti-W, Au, Ti-W metallization system, are shown in Figures 4 and 5. The complete construction analysis is contained in Appendix A. No construction features or anomalies were noted that would have a significant impact upon the evaluation of life test results.

3.1.2 High Temperature Test Circuit Evaluation - The initial selection of electrical bias conditions resulted from an evaluation of device performance in various candidate bias circuits at temperatures between 473°K and 533°K. Candidate bias circuits were evaluated in accordance with the following criteria:

a) Maximum rated voltage is maintained across the device over the temperature range.

b) Total device current is minimized over the temperature range.

c) A consistent set of internal device voltage conditions is maintained over the temperature range, i.e., device state does not change.

d) The maximum number of microcircuit junctions are reverse biased, and

e) The number of biasing resistors and power supplies is minimal.

The actual testing of microcircuits in the candidate circuits was performed in a test set-up similar to the one shown in Figure 6. Two devices were placed in a candidate circuit, and total device current and output voltage measurements were made at 298°K, 473°K, and several other temperatures between 473°K and 533°K. Forty-five minutes was allowed for the devices to reach thermal equilibrium before making the electrical measurements.

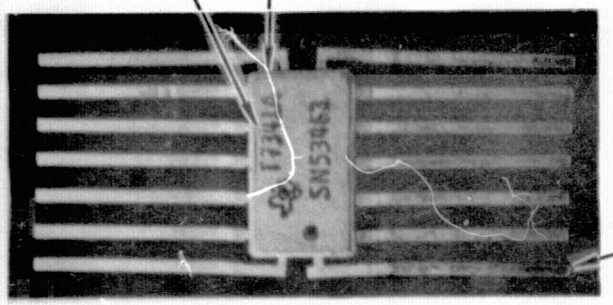
3.1.2.1 Candidate Circuit Evaluation Results - Three candidate circuits (A, B & C) were selected for evaluation. All circuits were operated with open circuit outputs and a 100 ohm current limiting resistor in the power supply (Vcc) line. The inputs of each gate were connected as follows:

Circuit A - two inputs connected to the Vcc terminal and one input grounded.

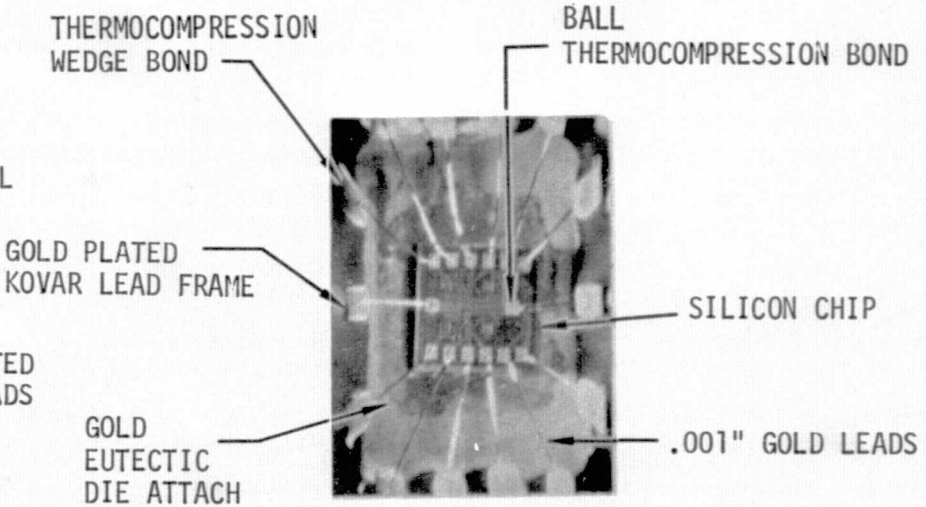
Circuit B - all inputs connected to the Vcc terminal.

Circuit C - all inputs grounded.

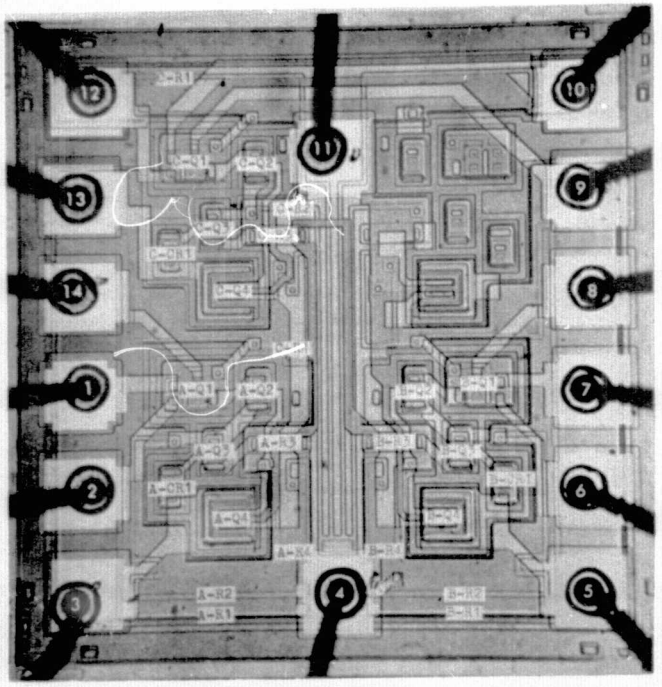
The results of testing commercial SN54L10T devices in the three candidate circuits at temperatures between 298°K and 513°K are shown in Figure 7. Circuits A and C exhibited a change from the high state to the low state between 473°K and 513°K, thereby, making them undesirable as life test circuits. Devices in Circuit B exhibited a stable low output voltage state through the temperature range. Device current was increasing rapidly above 493°K in Circuit B, but was less than the



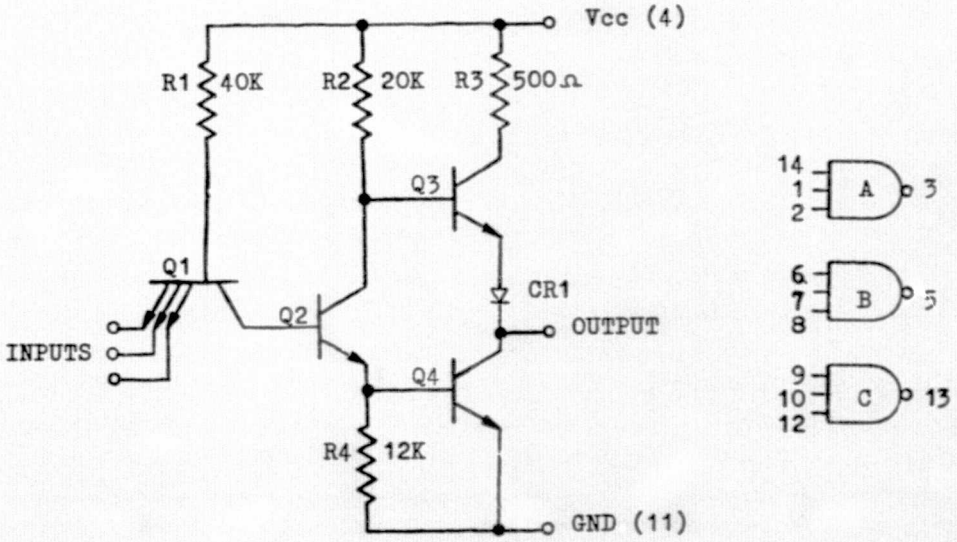
A. EXTERNAL CONSTRUCTION



B. INTERNAL CONSTRUCTION



C. DIE TOPOGRAPHY



D. FUNCTIONAL SCHEMATIC

FIGURE 4 - SN54L10T MICROCIRCUIT, TEXAS INSTRUMENTS

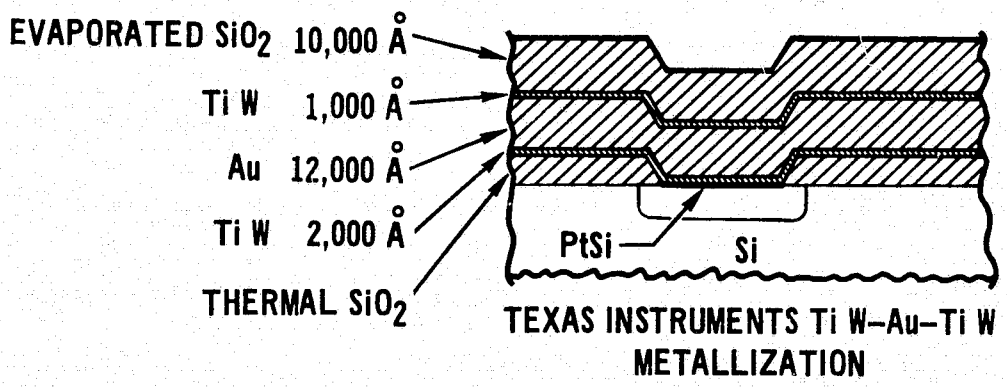


FIGURE 5. CROSS SECTION OF METALLIZATION

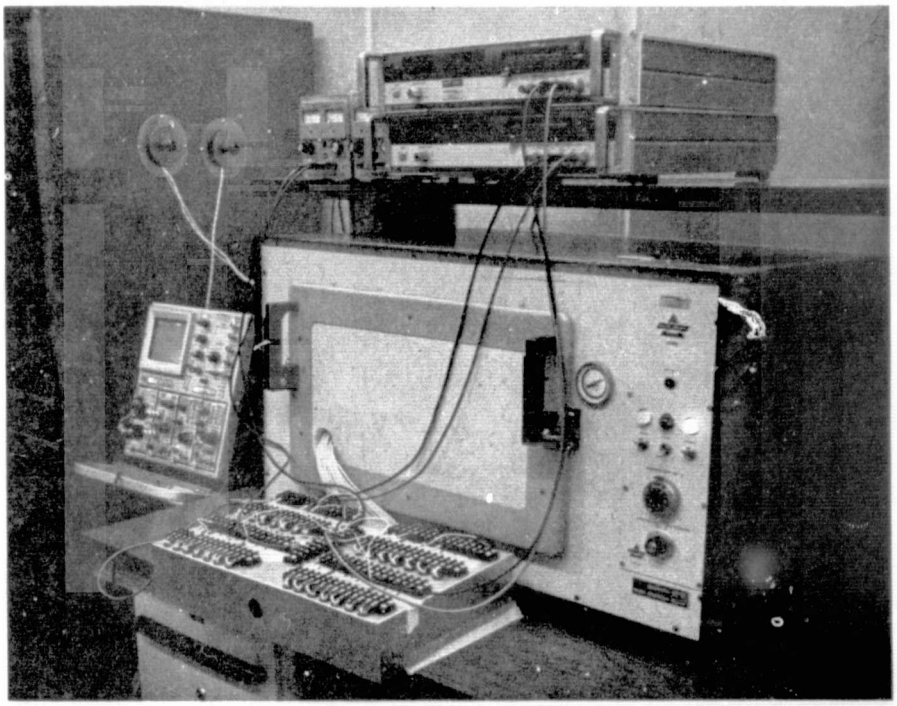


FIGURE 6. TYPICAL BIAS CIRCUIT EVALUATION SET-UP

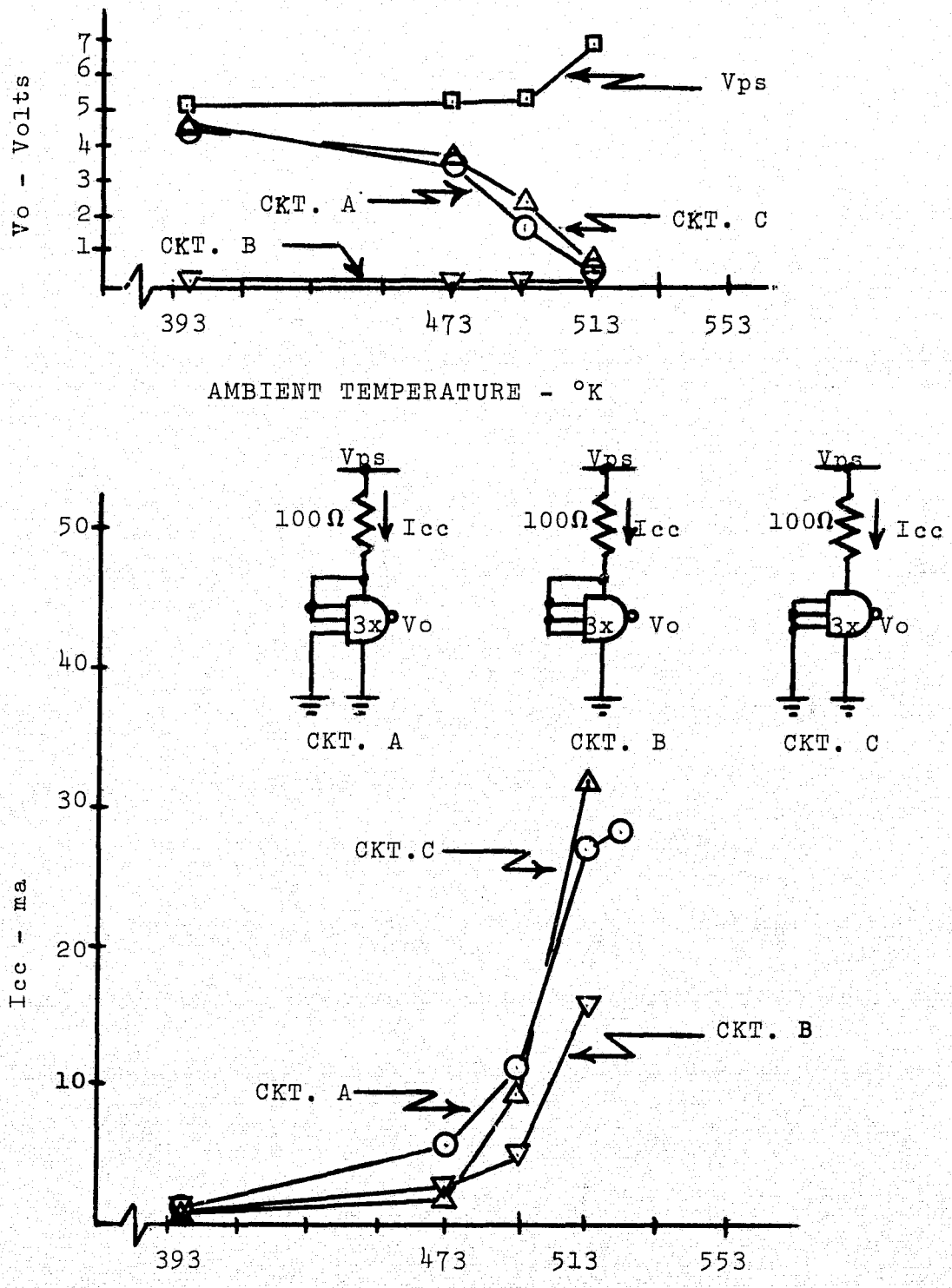


FIGURE 7, 54L10 CANDIDATE CIRCUITS A, B & C

device current in either Circuit A or C at the same temperature. The number of reverse biased junctions in Circuit B is also greater than in the other two circuits. Thus, Circuit B, with one modification, was tentatively selected as the test circuit for subsequent life testing.

The modification of Circuit B consisted of reducing the value of the current limiting resistor from 100 ohms to 50 ohms. Variations in device voltage are reduced with the modified circuit as a result of the reduced voltage drop across the current limiting resistor. The performance of commercial devices in the modified Circuit B when operated in the ovens intended for life testing is shown in Figure 8. Device current is higher than previously observed in the evaluation of Circuit B, but this is attributed to the use of ovens which circulate air at half the velocity of the air circulation in the oven used for the prior Circuit B evaluation. Device heat losses due to the reduction in forced air convection cooling are therefore less, and junction temperatures are higher as a result of internal device heating. Device current is also extremely sensitive to device voltage at ambient temperature above 503°K. This sensitivity is clearly seen in the family of Vcc - Icc curves shown in Figure 9. It is also evident from Figure 9 that maximum rated voltage can not be maintained across the device above 503°K. Thus, life test temperatures must be maintained below 503°K if the 5.5 VDC maximum recommended operating voltage is to be maintained across the device. Ambient temperatures up to 533°K could be utilized with 3.5 VDC maintained across devices. The 70 to 80 ma of device current at 533°K with 3.5 VDC across the device is excessive for an aluminum metallization system due to the rapid acceleration of electromigration failures. However, electromigration failures were not expected to be a problem with the Ti-W, Au, Ti-W metallization system, since the rate of electromigration of gold is several orders of magnitude lower than aluminum [1]. Thus, on the basis of device performance, ambient temperatures up to 533°K with an applied voltage of 3.5 VDC could be utilized as life test conditions. If the applied voltage is to be maintained at 5.5 VDC, ambient temperatures must be limited to 503°K. The decision to operate devices at the higher test temperatures with less than maximum rated voltage is discussed subsequent to the presentation of device thermal characteristics and step stress test results.

3.1.3 Thermal Characterization - Having established a tentative bias circuit design, an evaluation of device thermal characteristics was performed to determine the microcircuit junction temperatures that could be expected at the life test conditions. Infrared (IR) microscanning techniques were employed to study microcircuit chip temperatures and thermal gradients across the chip surface. Bias conditions established by the selected life test circuit were applied to the device during these studies. The devices were operated in specially constructed "micro-ovens" at temperatures above 493°K during the course of making IR measurements. However, the device mounting method and ambient air velocity existing in the actual life test chamber could not be duplicated with the "micro-ovens". Consequently, thermal resistance values were derived from MIL-STD-883 type electrical measurements made with the devices mounted in the normal manner in the life test chamber. Measurements were made at ambient temperatures above 473°K with the bias conditions established by the selected life test circuit.

3.1.3.1 Infrared Evaluation - Infrared evaluations of the surface temperature of one (1) SNM54L10 chip were performed using the Barnes RM-50 Infrared Microscanner and a specially constructed "micro-oven". The test set-up used for the infrared evaluation is shown in Figure 10. Thermal maps of the chip surface were constructed

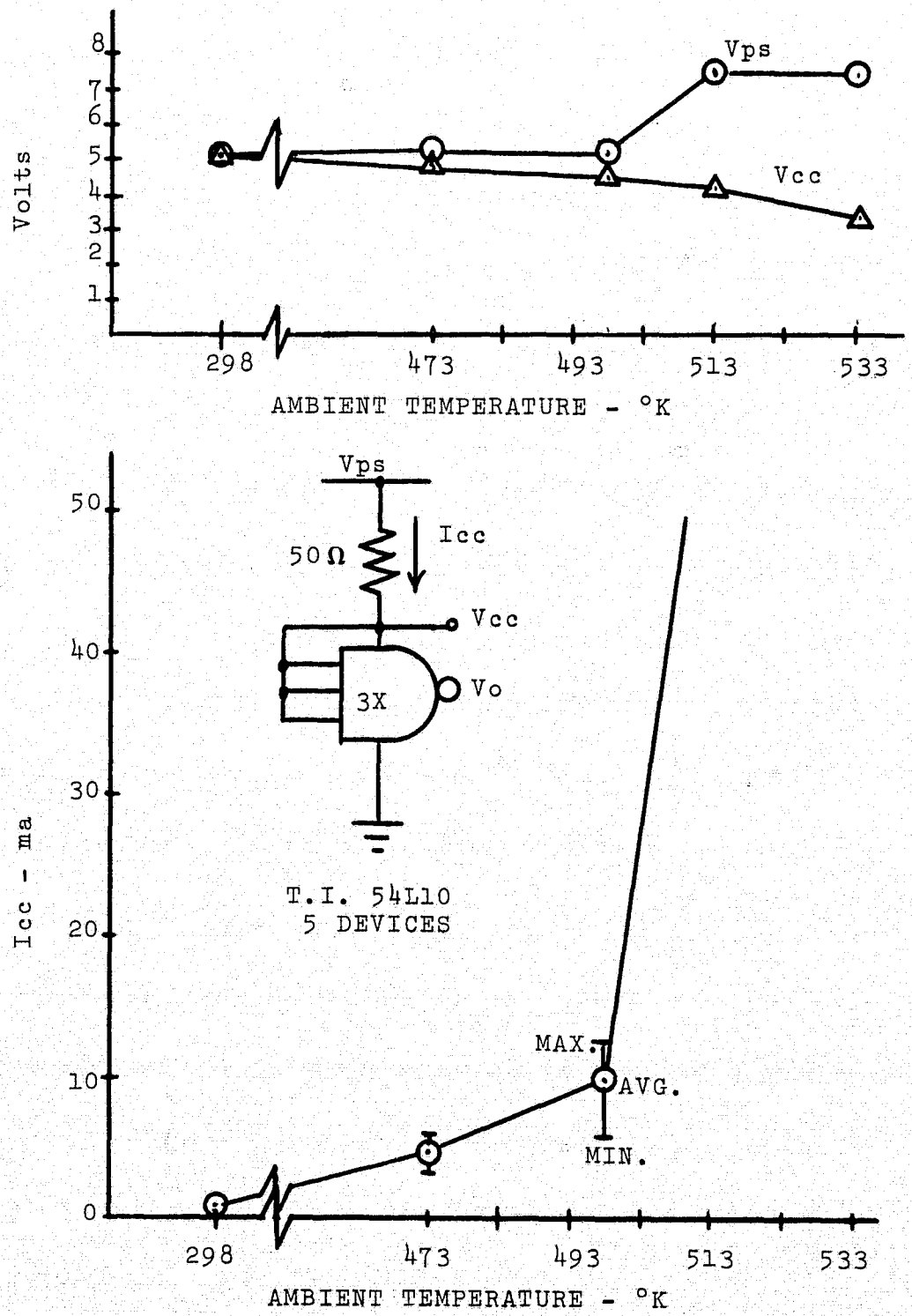


FIGURE 8 , 54L10 PERFORMANCE DURING STEP STRESS

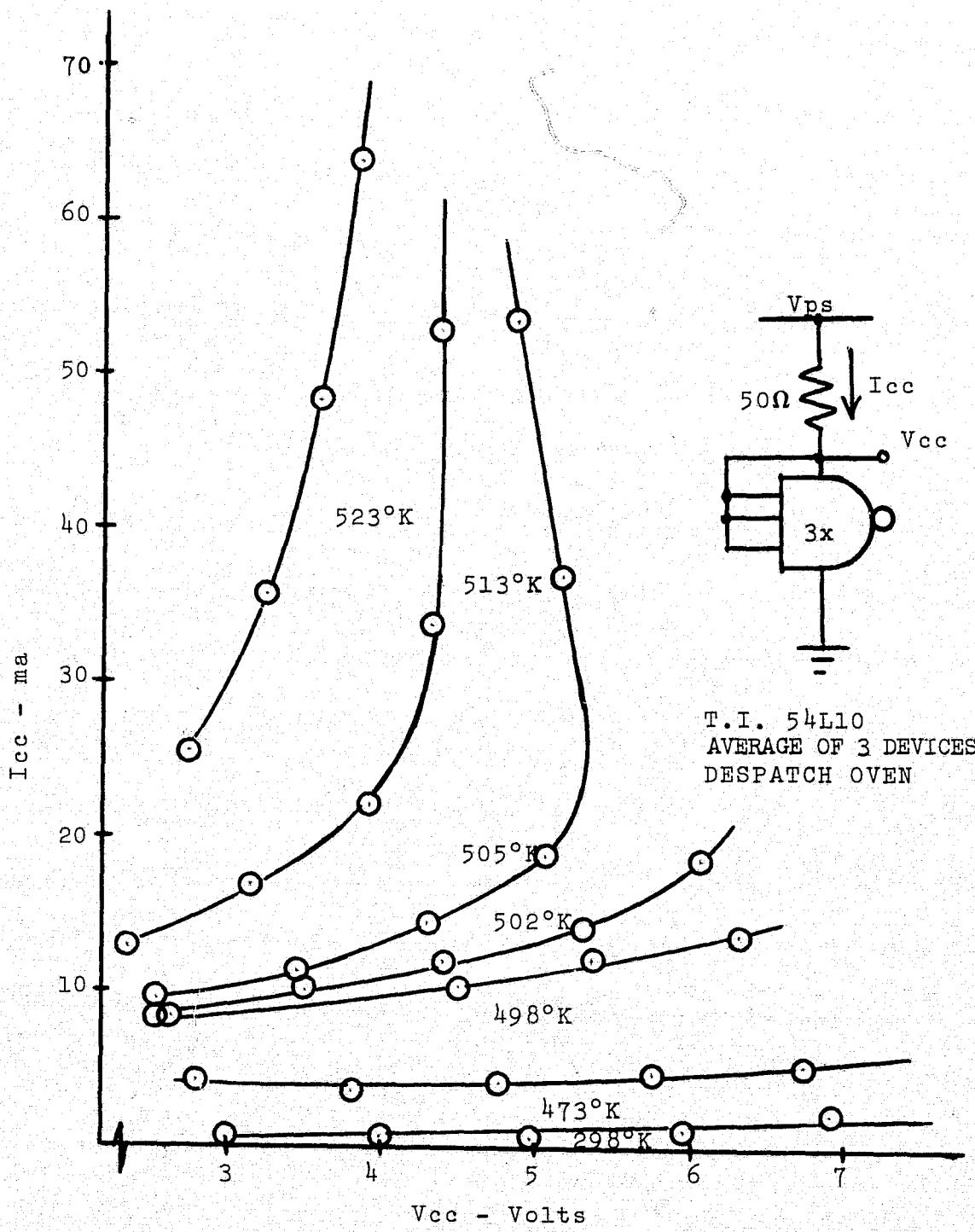


FIGURE 9 , Vcc-Icc CHARACTERISTIC, 54L10

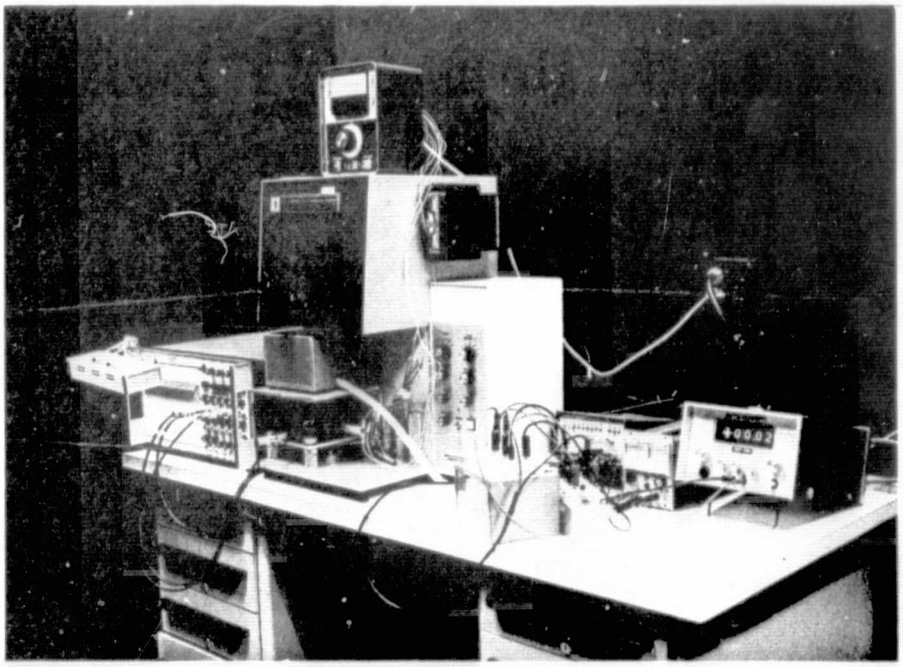


FIGURE 10. TYPICAL INFRARED MICROSCANNER SET-UP

from data taken while the microcircuit was operated in the "micro-oven" at temperatures between 473°K and 533°K. These maps are presented in Figures 11 through 15. Note that the surface temperature is fairly uniform. The maximum temperature difference between any two points on the chip surface is only 5°K. Thus, no junction within the device should be more prone to failure then any others.

3.1.3.2 Thermal Resistance Measurements - Device thermal resistance was established from a sample of three SNM54L10T microcircuits. The sample devices were tested at ambient temperatures of 473°K, 513°K and 523°K while operated in the selected life test circuit. The thermal resistance between junction and ambient (θ_{JA}) was calculated from the test data using a method similar to MIL-STD-883, Method 1012, Test Condition C, as follows:

$$\theta_{JA} = \frac{T_J - T_A}{P_J} \qquad (1)$$

where:

T_J = device junction temperature,
T_A = Ambient temperature in the vicinity of the device, and
P_J = the power being dissipated in the device.

For the above equation, T_A and T_J were obtained by measuring the forward voltage of a substrate diode in the device under test and calculating T_A and T_J as follows:

$$T_A = A + B\,(V_{F_0}) + C\,(V_{F_0})^2 \qquad (2)$$

and,

$$T_J = A + B\,(V_{F_P}) + C\,(V_{F_P})^2 \qquad (3)$$

Where:

V_{F_0} = Forward voltage of unpowered devices under test, and

V_{FP} = Forward voltage of powered devices under test.

The coefficients A, B and C were obtained as a result of a linear regression analysis of the oven ambient temperature (T_0), and the unpowered forward voltage of the device under test (V_{F0}). The oven temperature (T_0) was measured with a small thermocouple in the vicinity of the part and the reference junction in an ice bath at 0°C. Calculating both T_A and T_J from a second order polynominal in V_F compensates for the nonlinearity in the $T_J = F(Vp)$ function observed for $T_J > 448°K$ and removes small errors in the temperature/voltage function that would exist if T_A were derived from the thermocouple directly.

The electrical and environmental conditions during the time forward voltage measurements were being performed was almost identical to the anticipated life test conditions. The only difference during thermal resistance testing is that the device is operated in a pulsed mode with the Thermal Resistance Tester shown in Figure 16. A summary of test results (averaged for three devices) is presented in Table 4.

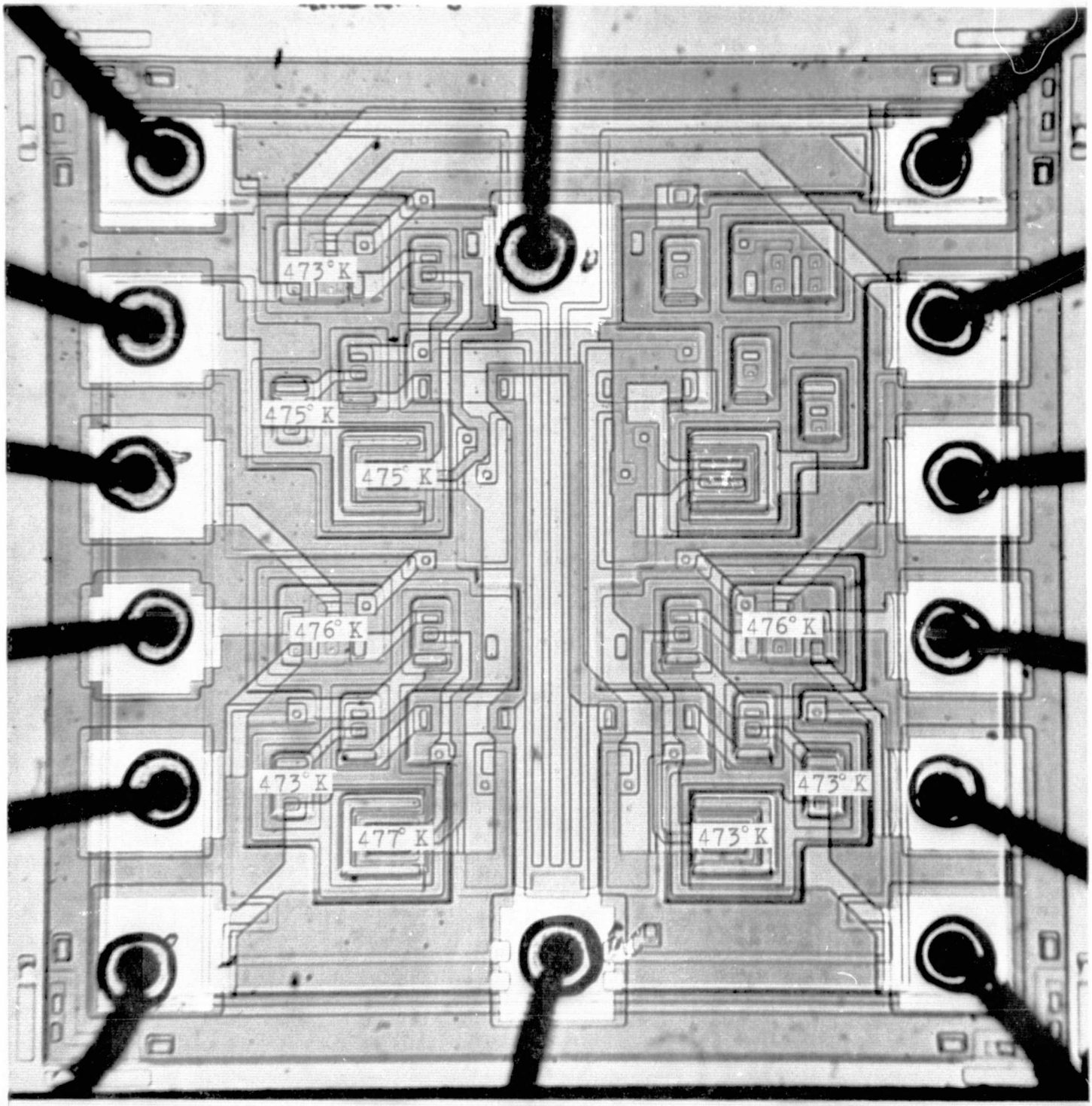


FIGURE 11. THERMAL MAP AT 473°K

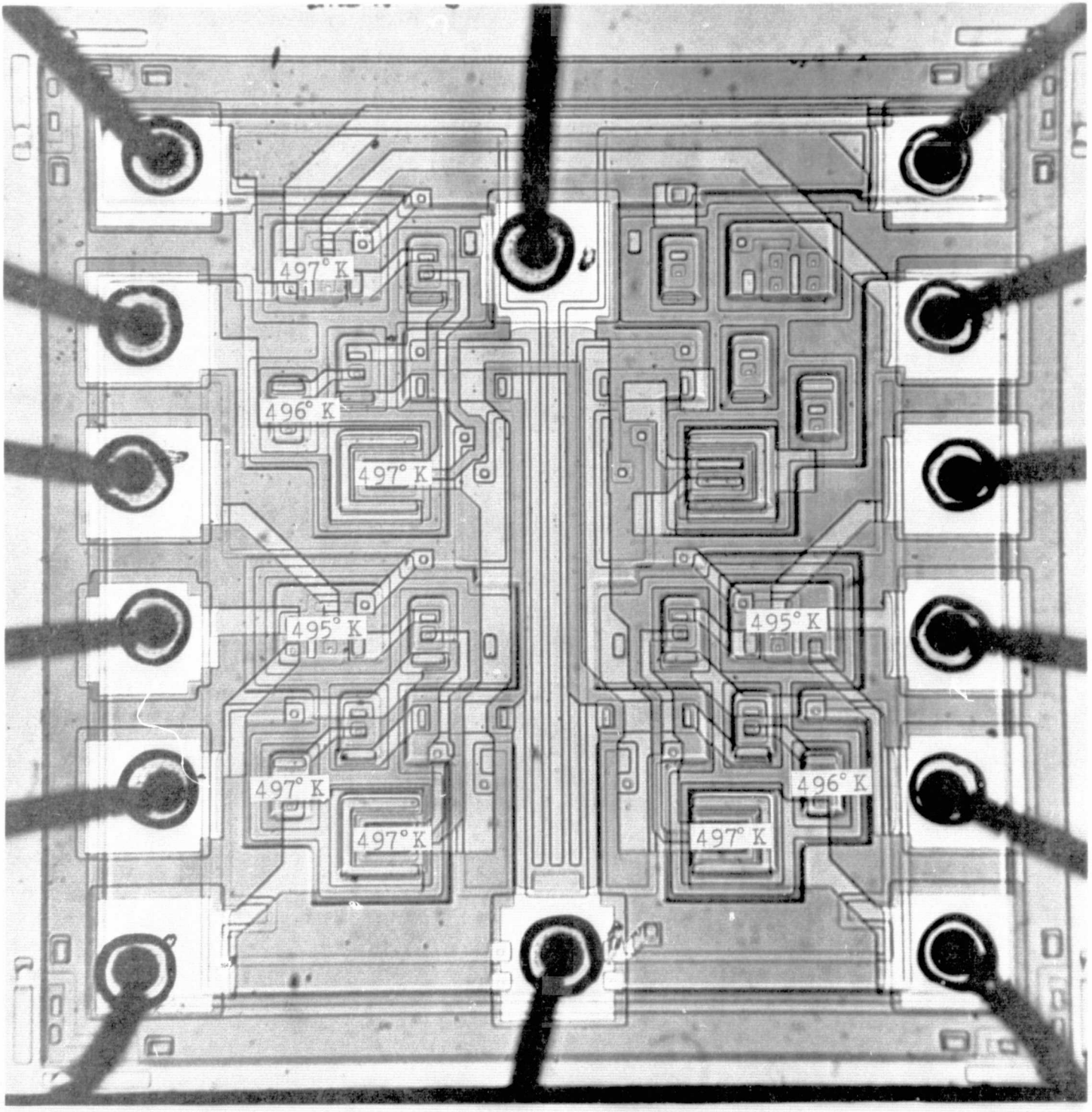


FIGURE 12. THERMAL MAP AT 492°K

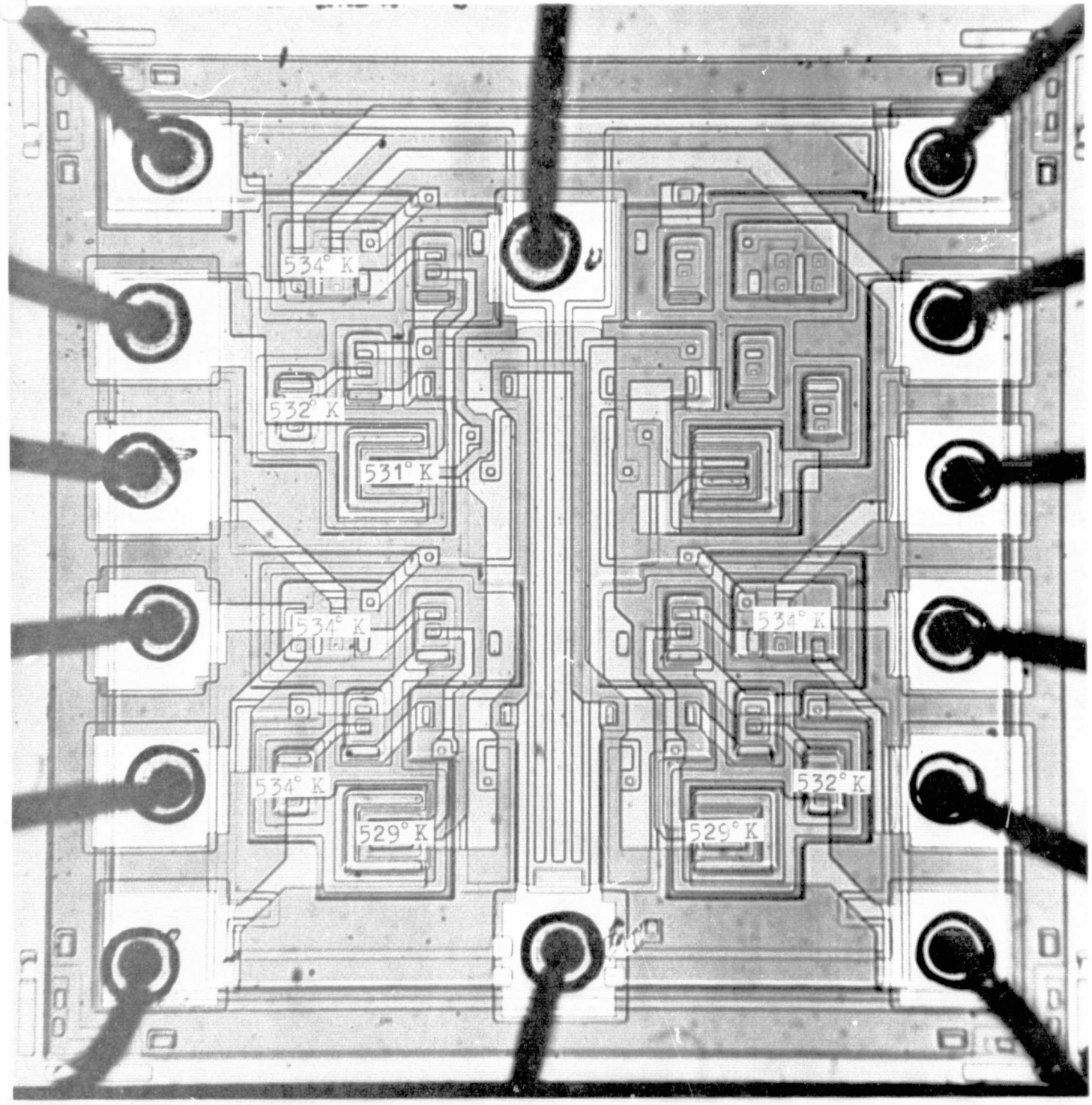


FIGURE 13. THERMAL MAP AT 513°K

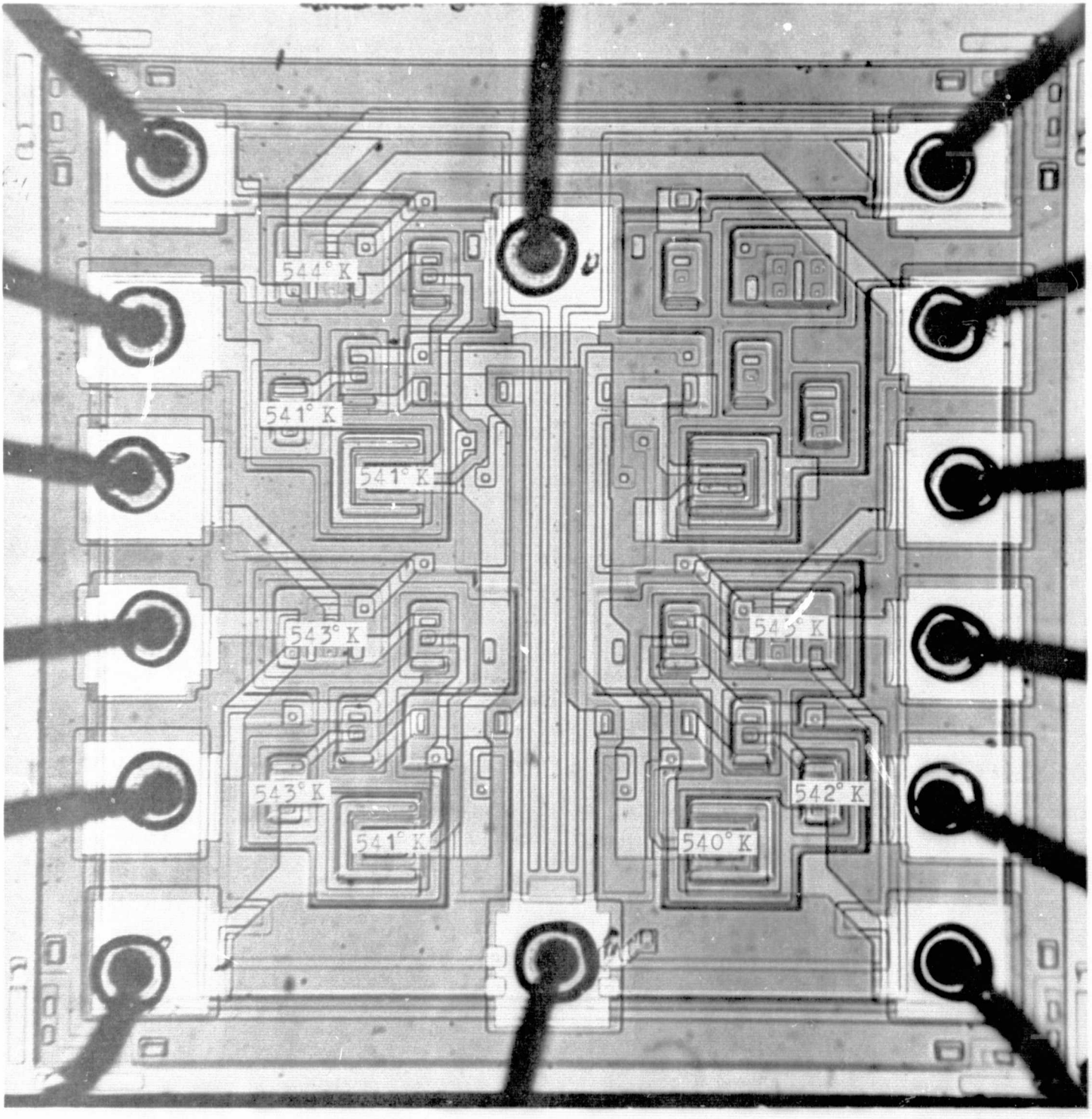


FIGURE 14. THERMAL MAP AT 522°K

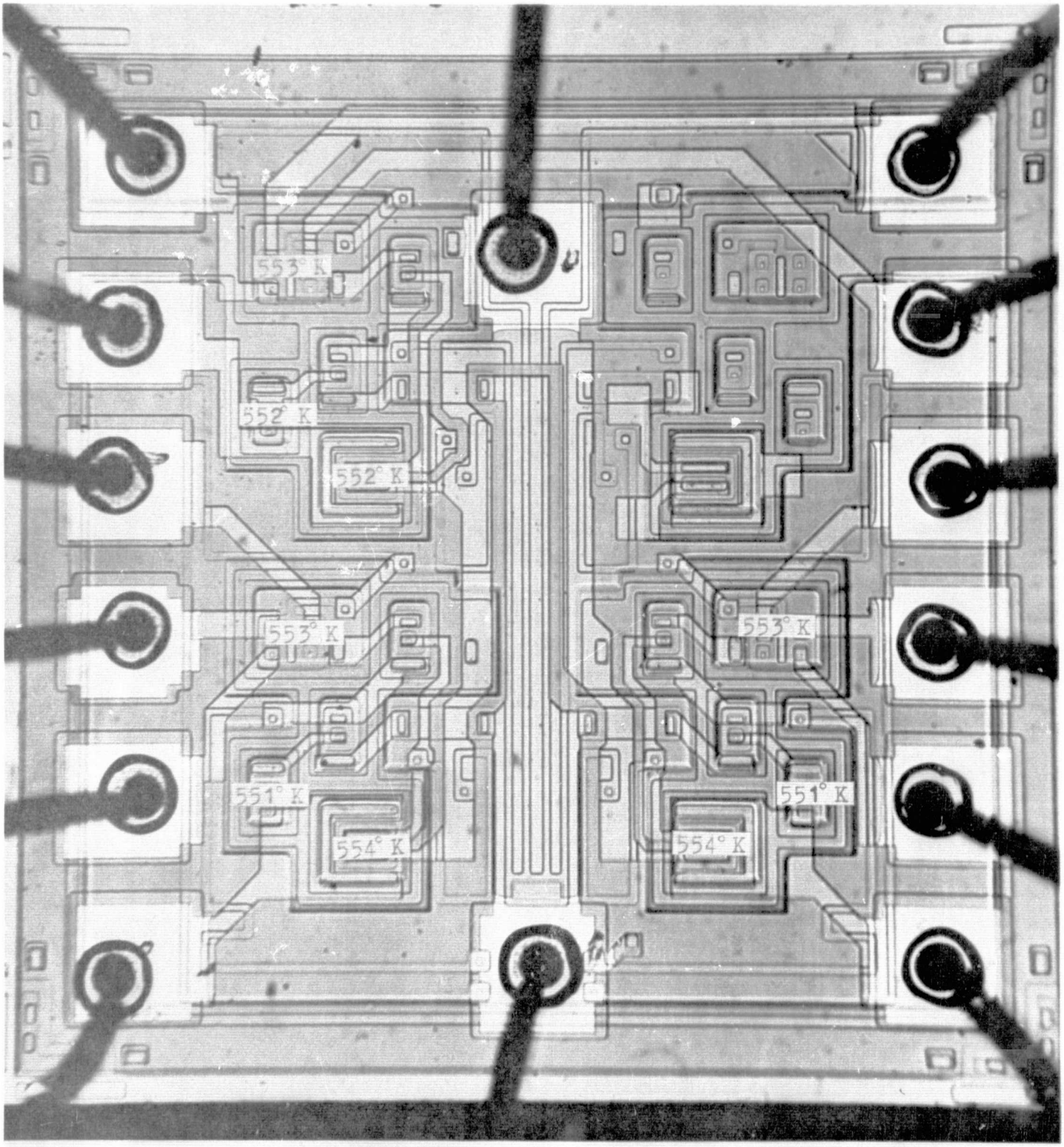
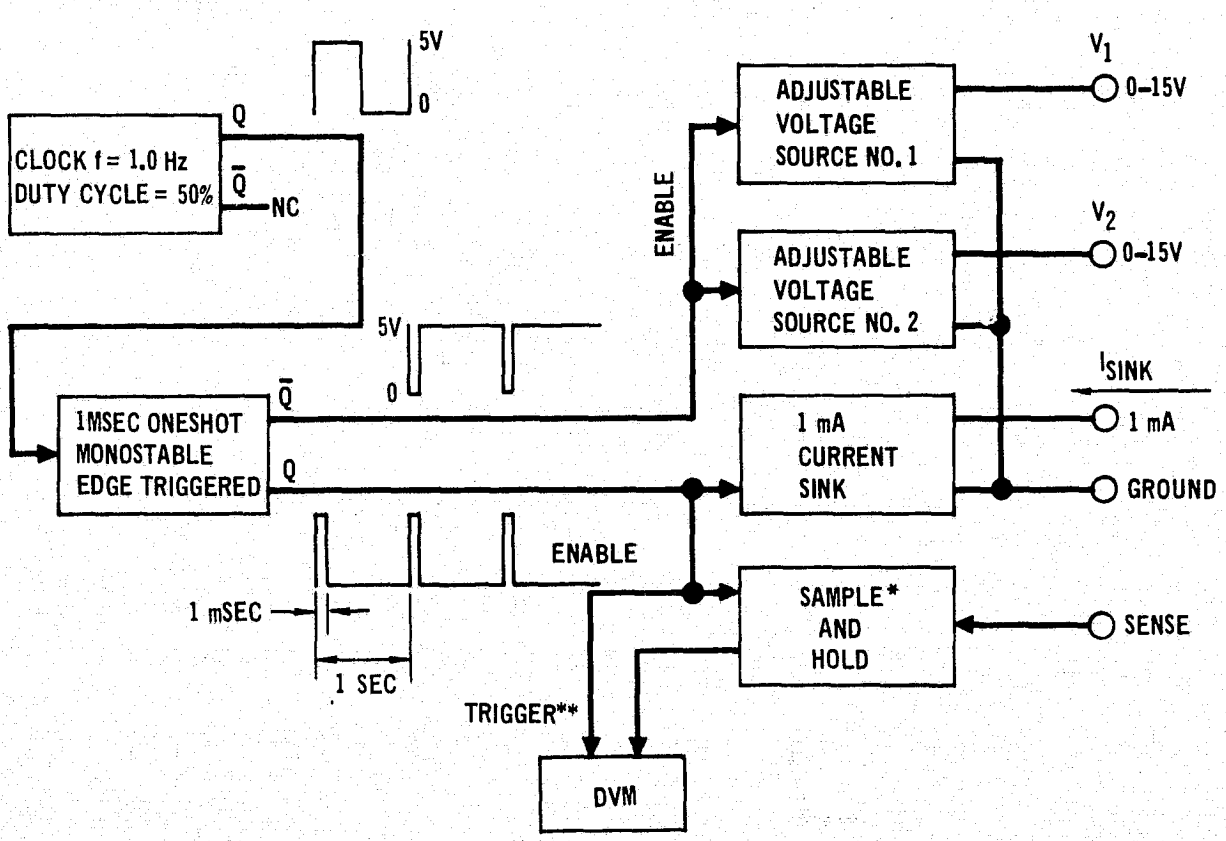


FIGURE 15. THERMAL MAP AT 533°K



*NOTE: S&H HAS A 100μS APERTURE TRIGGERED AT BEGINNING OF MEASUREMENT CYCLE.
**NOTE: DVM IS TRIGGERED AT END OF MEASUREMENT CYCLE.

FIGURE 16. THERMAL RESISTANCE TESTER

TABLE 4. SUMMARY OF THERMAL RESISTANCE MEASUREMENTS

AMBIENT TEMPERATURE T_A (°K)	POWER SUPPLY VOLTAGE V_{PS} (VOLTS)	DEVICE VOLTAGE V_{CC} (VOLTS)	DEVICE CURRENT I_{CC} (mA)	POWER DISSIPATION P_d (mW)	JUNCTION TEMPERATURE T_J (°K)	THERMAL RESISTANCE θ_{JA} (°K/W)
473	5.33	5.03	5.7	29.8	484	275
493	5.51	4.83	13.7	66.3	507	210
513	7.49	3.98	70.2	285.0	564	179
523	7.49	3.75	72.5	272.0	573	191

3.1.4 Step-Stress Tests - Both Preliminary and Formal Step-Stress Tests were performed with devices in the selected life test circuit. Figure 17 shows the testing sequence used during the step stress tests. The Preliminary Step-Stress Test was performed with five (5) commercial samples to evaluate the effects of longer exposure to temperatures above 473°K than were experienced during the bias circuit evaluation tests. No failures were observed during this test. A Formal Step-Stress test was performed with twenty SNM54L10T devices from the lot intended for life testing to select the HTOT life test temperatures. A summary of the Formal Step Stress Test is shown in Figure 18. Fifteen device failures were detected during the post 473°K step electrical tests. All fifteen failed devices exhibited out of tolerance V_{OL} readings due to a channel in the N-epitaxial collector region between the base of the input transistor and the substrate. Two additional device failures were noted during the post 513°K step electrical tests, but subsequent retest of these devices did not verify the failed condition.

A complete failure analysis summary is contained in Appendix B.

3.1.5 Selection of Life Test Conditions - Evaluation of the results from step stress tests, circuit evaluation tests and device thermal studies led to the selection of test conditions shown in Table 5. These tests and studies indicated that ambient temperatures up to 523°K are nondestructive provided the device voltage is maintained below 3.5 VDC. The step stress tests also indicated that thermal stresses above 473°K are necessary to obtain sufficient failure distribution data for non-contaminated devices within the 4000 hour test period. From the results of the Formal Step Stress Test, it would appear that 75% of the devices designated for life testing are contaminated and will fail within the first sixteen hours of test at 473°K. However, since four different lot numbers were identified in the shipment of SNM54L10 devices, it was suspected that most of the parts subjected to the Formal Step Stress Test were from a single lot of contaminated devices. A special high temperature test of ten devices selected at random from the total shipment of devices, tended to verify that only one lot was contaminated. Only two devices failed after 30 hours of test at 473°K and no further failures were noted after an additional 32 hours of test at 523°K. Unfortunately, device traceability to a specific lot number was not maintained, and it could not be determined if the two failed devices from the special test and the devices from the Formal Step Stress Test were from the same lot. Nevertheless, it was felt that an excessive number of device failures would not be experienced in any Phase C test subgroup, provided devices for each were selected at random from the total device shipment.

Thus, ambient temperatures of 473°K, 498°K and 523°K were selected for the Phase C life tests to provide the maximum safe accelerating stress. It was recognized that devices from the contaminated lot would fail quite early in the life tests, but that the selected stresses are necessary to obtain the failure distribution of devices from non-contaminated lots. Selection of the test conditions for the Burn-In and Screening Comparison Tests in the previously mentioned Table 5 were based on Phase C test results.

3.2 Phase C - High Temperature Operating Tests (HTOT)

Three 4000 hour high temperature life tests were conducted with SNM54L10T devices to: a) evaluate the assumption of a log normal failure distribution, b) determine the device life-temperature acceleration factor(s), and c) select the

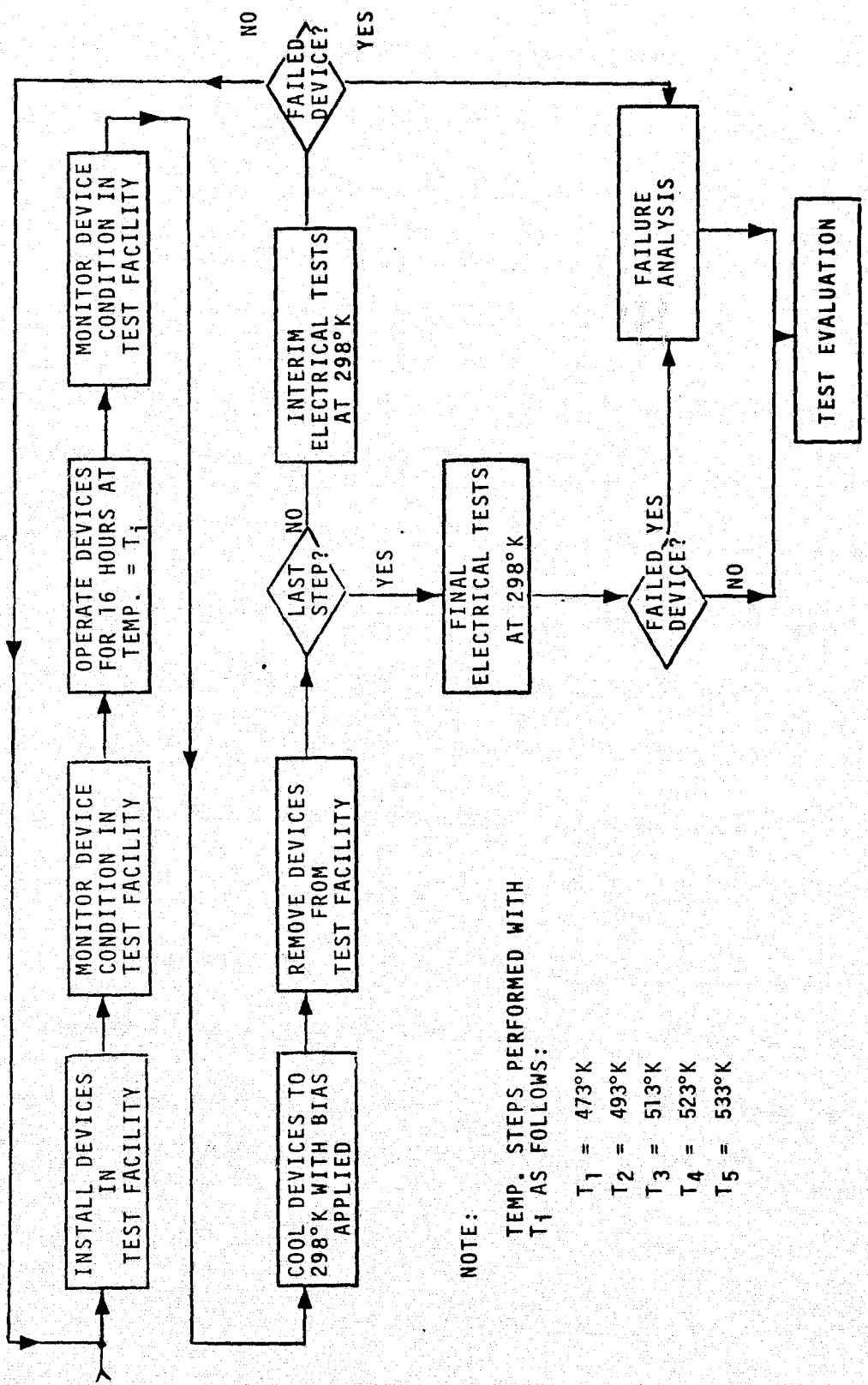
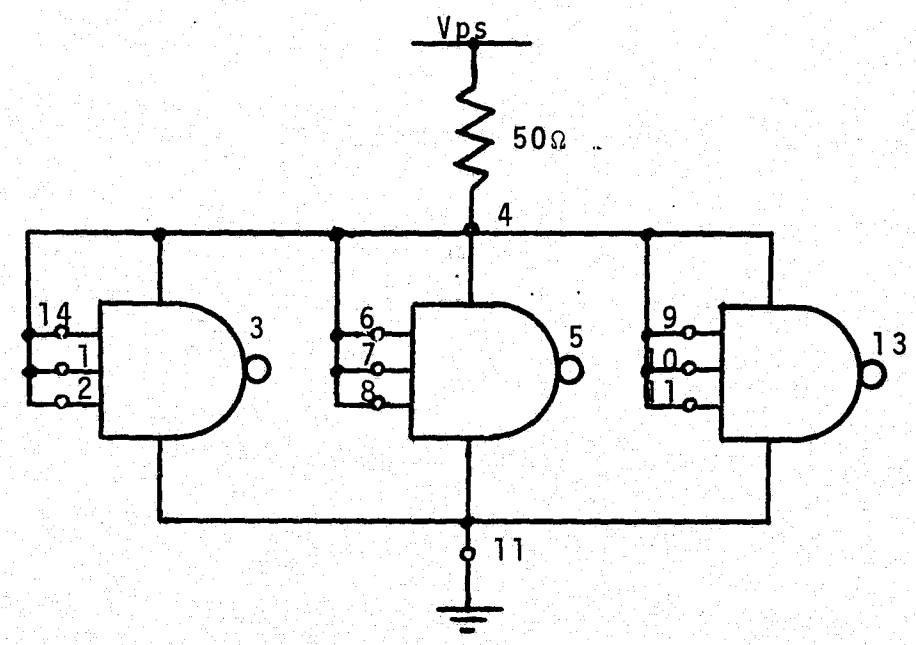


FIGURE 17. STEP-STRESS TESTING SEQUENCE



BIAS CIRCUIT

TEST CONDITIONS & RESULTS

NO. OF DEVICES ON TEST	TEST TIME AT T_A	AMBIENT TEMP. °K	JUNCTION TEMP. °K	AVG. V_{cc} VDC	AVG. PWR. DISSIPATION MW	NO. OF DEVICE FAILURES
20	16	473	481	4.7	28	15*
5	16	493	506	5.1	61	0
5	16	513	563	4.2	277	2**
3	16	523	576	3.8	281	0
3	16	533	592	3.5	280	0

* ALL DEVICES FAILED VOL, 4 OF THE 15 ALSO FAILED I_{IH}

** DEVICE FAILURES NOT VERIFIED

FIGURE 18, 54L10 STEP STRESS TEST SUMMARY

TABLE 5. SUMMARY OF LIFE TEST CONDITIONS

TEST GROUP	AMBIENT TEMP. T_A (°K)	JUNCTION TEMP. T_J (°K)	POWER SUPPLY VOLTAGE V_{PS} (VOLTS)	DEVICE VOLTAGE V_{CC} (VOLTS)	DEVICE CURRENT I_{CC} (mA)	POWER DISSIPATION P_d (mW)
HTOT #1	498	505	4.0	3.5	10	35
HTOT #2	523	556	7.0	3.5	50	175
HTOT #3	473	477	3.7	3.5	4	14
BURN-IN	498	505	4.0	3.5	10	35
SCREENING COMPARISON TESTS #1, #2 & #3	513	539	4.5	3.5	20	70

time and temperature for the Phase D burn-in test. The life tests consisted of two subgroups of 35 devices each at ambient temperature of 498°K (HTOT #1) and 523°K (HTOT #2) plus a third subgroup of 70 devices at 473°K (HTOT #3). Applied electrical stresses were as previously stated in Table 5. All life testing was conducted in the test facility shown in Figure 19. The cumulative numbers of device failures observed at each electrical measurement time, and categorized by failure mode are shown in Table 6. Three distinct failure modes were observed during the test. Analysis of failed devices (Appendix B) indicated that out of the total of 140 devices tested only one device in subgroup HTOT #3 failed catastrophically. This occurred at 96 hours as a result of an internal lead shorting to the case. All other device failures were the result of surface instabilities or penetration of the gold metallization into emitter junctions via microcracks in the Ti-W barrier metal. A total of 42 devices or 30% of the 140 devices tested failed due to surface instability. All of the surface instability failures occurred early in the program (32 hours or less) which correlates with the earlier assumption of a single lot of contaminated devices. Since no additional surface related failures were noted after 32 hours of test at the lowest ambient temperature of 473°K, it was decided that 32 hours at the higher 498°K test temperature would be a sound Phase D burn-in test.

A plot of the cumulative percentage failures versus time, excluding the one device that failed due to an internal lead to case short, is shown in Figure 20. Although there were insufficient data points to perform a meaningful goodness of fit test to evaluate the underlying failure distribution, the assumption of a log normal distribution appears reasonable for both the surface related failures and the failures due to gold penetration.

Based on the assumption that the overall failure distribution of each test group may be represented by two log normal distributions, one with a short median life (freak distribution) and one with a long median life (main distribution), the overall cumulative percentage of device failures was represented as follows:

$$P(t)_T = K_f\, P(t)_f + (1-K_f)\, P(t)_m \qquad (1)$$

where:

$P(t)_T$ = total cumulative percentage of device failures at time t

$P(t)_f$ = cumulative percentage of failures at time t expected from the freak population of devices having a log normal failure distribution with median life θ_f and standard deviation σ_f

$P(t)_m$ = cumulative percentage of failures at time t expected from the main population of devices having a log normal failure distribution with median life θ_m and standard deviation σ_m

K_f = estimated percentage of device failures in the overall test group that are from the freak population.

Using the average time between electrical measurements as the best estimate of the actual failure time, and an iterative technique that minimized the average deviation between the percentage of failures computed from equation (1) and the observed cumulative failure percentage, values of θ_f, σ_f, θ_m and σ_m for each HTOT subgroup were computed. The results of these computations are summarized in Table 7.

Detailed failure analysis coupled with data analysis revealed that the freak population failures were predominantly surface related and that the main population failures were exclusively gold penetration.

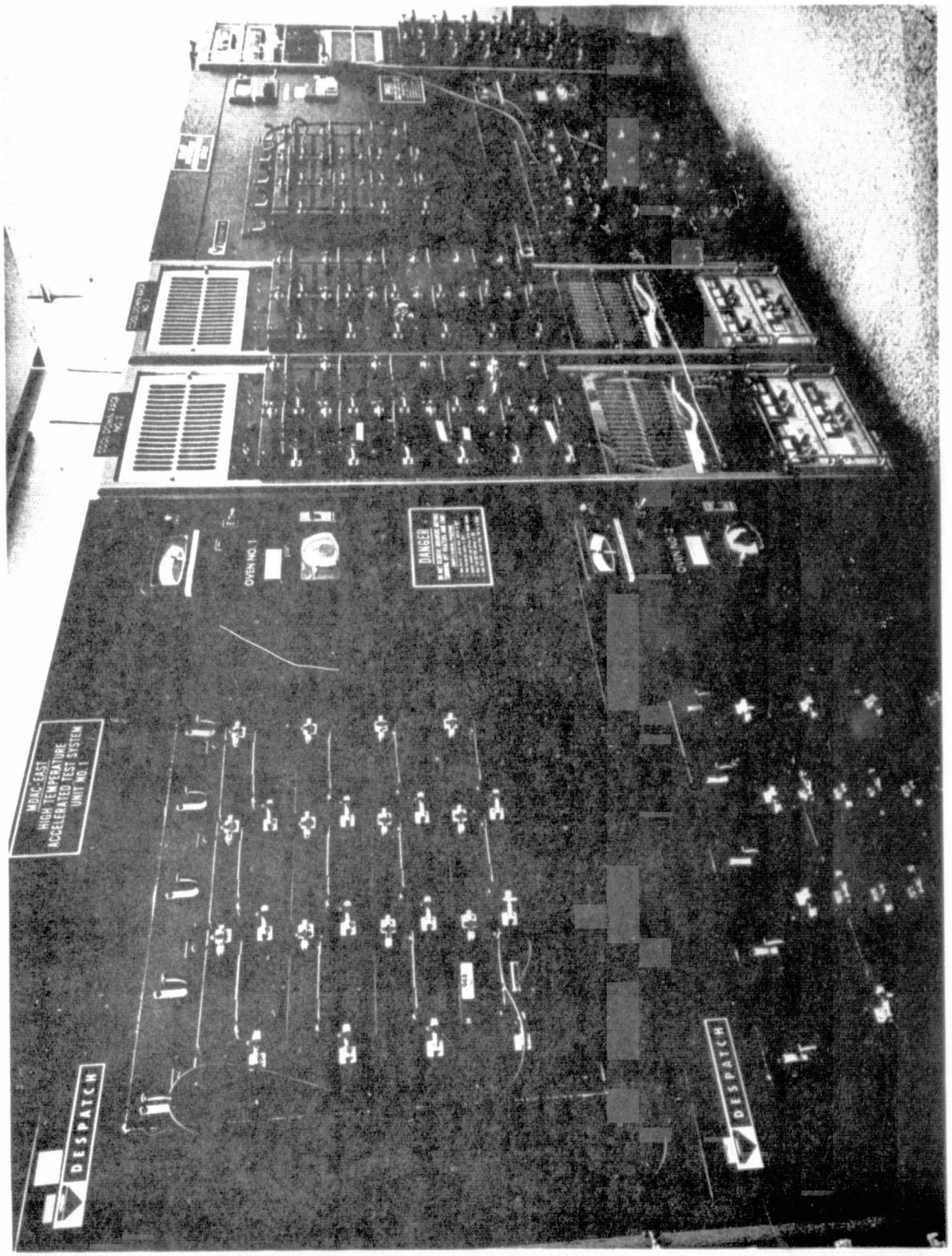


FIGURE 19. HIGH TEMPERATURE OPERATING TEST SYSTEM

TABLE 6. HTOT FAILURE SUMMARY

TEST GROUP & PART NO.	QTY.	T_A °K	T_J °K	FAILURE MODE	CUMULATIVE NO./% FAILURES AT HOURS OF TEST																	
					4	8	16	32	48	64	96	128	192	256	384	512	768	1000	1500	2000	2500	3000	4000
HTOT #2 SNM54L10T	35	523	556	A	15	16	16	16	-	16	-	16	-	16	-	16	-	16	-	-	16	-	16
				B	0	0	0	0		0		0		0		6		12			13		13
				TOTAL	16	16	16	16		16		16		16		22		28			29		29
				%	42.9	45.7	45.7	45.7		45.7		45.7		45.7		62.9		80.0			82.9		82.9
HTOT #1 SNM54L10T	35	498	505	A	1	6	7	7		7		7		7		7		7			7		7
				%	2.9	17.1	20.0	20.0		20.0		20.0		20.0		20.0		20.0			20.0		20.0
HTOT #3 SNM54L10T	70	473	477	A	0	4	11	19	19	19	19	19	19	19	19	19	19	19	19	19		19	19
				C	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1		1	1
				TOTAL	0	4	11	19	19	19	20	20	20	20	20	20	20	20	20	20		20	20
				%	0.0	5.7	15.7	27.1	27.1	27.1	28.6	28.6	28.6	28.6	28.6	28.6	28.6	28.6	28.6	28.6		28.6	28.6

FAILURE MODE DEFINITIONS

A - SURFACE INSTABILITY

B - GOLD PENETRATION

C - INTERNAL LEAD TO CASE SHORT

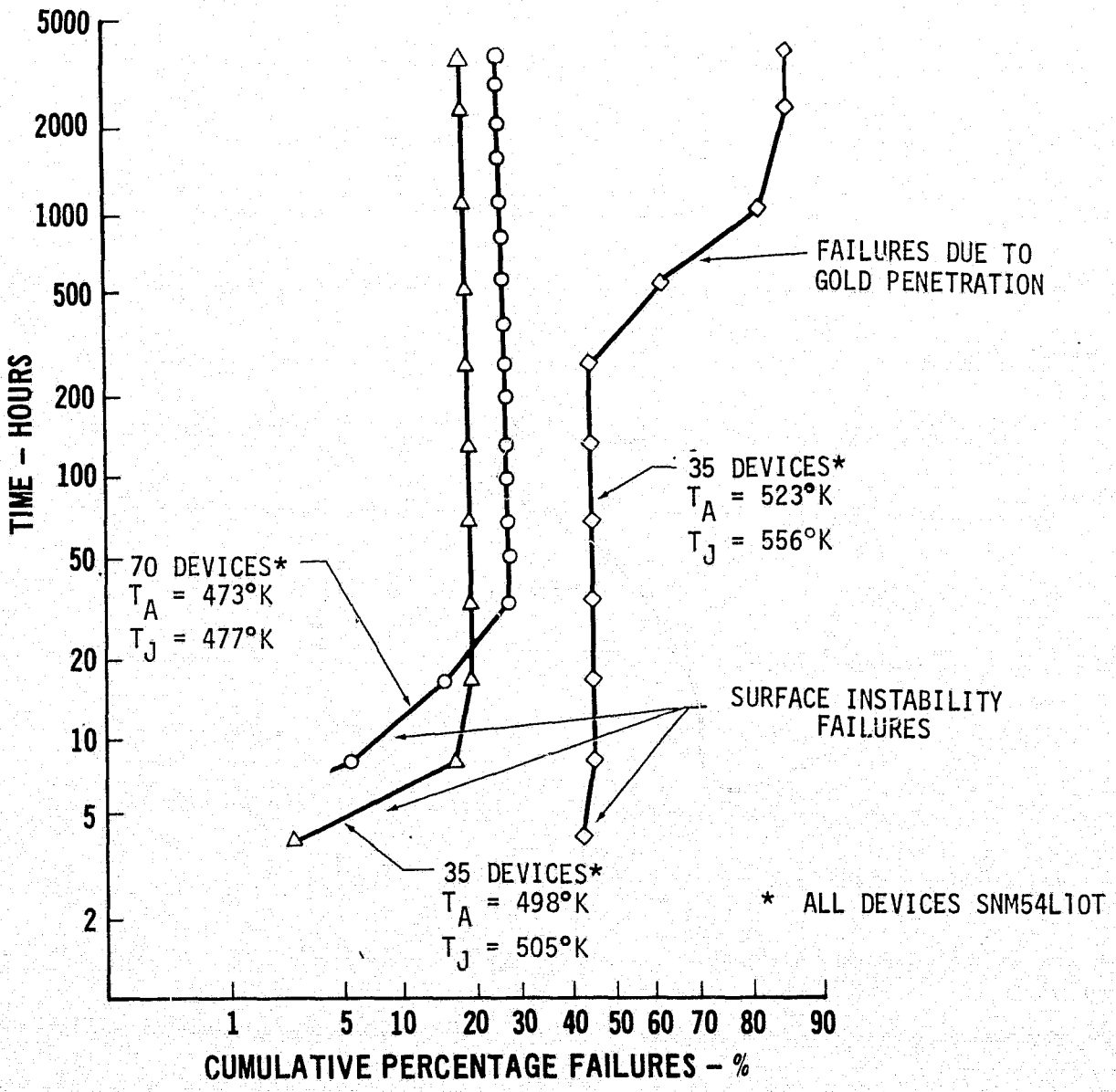


FIGURE 20. HTOT LIFE TEST RESULTS

Since no devices in HTOT Groups #1 and #3 failed due to gold penetration in 4000 hours of test, an estimate of the main distribution median life could not be made for these subgroups.

TABLE 7. SUMMARY OF HTOT FAILURE DISTRIBUTION PARAMETERS

TEST GROUP	T_J	K_f	θ_f	σ_f	θ_m	σ_m
HTOT #2	556°K	45.7%	0.7 HRS.	0.8	970 HRS.	1.4
HTOT #1	505°K	20.0%	4.0 HRS.	0.8	-	-
HTOT #3	477°K	27.1%	11.5 HRS.	0.8	-	-

Device life-temperature acceleration associated with the surface instability failures or freak distribution was evaluated using an Arrhenius reaction rate model as described by Peck [2]. The Arrhenius model related device median life to junction temperature as follows:

$$\theta = A \exp [E_A/K_B T] \quad (2)$$

where:

θ = device median life or time to 50% failure
A = an empirical constant
E_A = apparent activation energy (electron volts)
K_B = Boltzman's constant (electron volts/°K)
T = junction temperature (°K)

The application of regression analysis techniques to the median life data previously computed for the freak population observed in each HTOT subgroup resulted in an apparent activation energy of 0.83 electron volts, and a value for A of -17.8. A graphical representation of these results is shown in Figure 21. Arrhenius model parameters for the main population could not be evaluated due to the lack of gold penetration failures in HTOT Groups #1 and #3.

3.3 Phase D - High Temperature Burn-In Test

The Phase D, 32 hour burn-in of 73 SNM54L10T devices at an ambient temperature of 498°K was performed to provide 50 HTOT burned-in devices for the Phase E Screening Comparison Test. The bias circuit configuration, test procedures and facilities used for the burn-in test were identical to those described for the Phase C life tests. Results of the burn-in test are shown in Table 8.

TABLE 8. BURN-IN TEST RESULTS

TEST HOURS	CUMULATIVE FAILURES	
	NUMBER	PERCENT
4	4	5.5
8	5	6.8
16	8	11.0
32	8	11.0

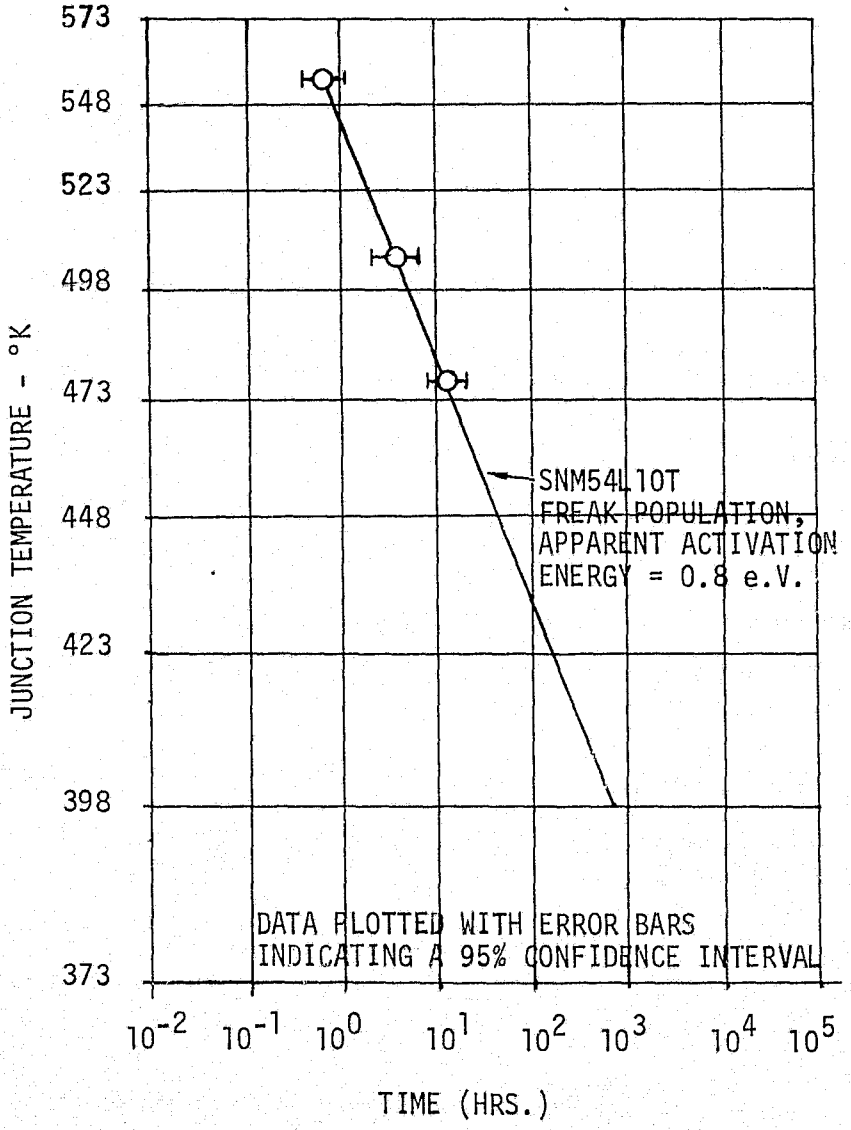


FIGURE 21. ARRHENIUS PLOT OF HTOT FREAK POPULATION

All devices failed due to surface instability as described in Appendix B. An additional six failures were detected in the post burn-in electrical tests at 398°K. All six of these failed devices exhibited I_{max} values that exceeded the specification limit as a result of surface instability.

Although the total percentage of failures (11%) in the burn-in test differs from the percentage of failures (20%) at 32 hours in the comparable HTOT #1 life test, the point in time that failures ceased to occur is identical in both tests. No additional failures were noted in either the HTOT #1 test or the burn-in test after 16 hours. Thus, the duration of the burn-in test appeared to be adequate to eliminate all of the contaminated devices or freak population in the test group.

3.4 Phase E - Screening Comparison Test

High temperature life tests were conducted for 4000 hours with 50 SNM54L10T devices previously burned-in for 32 hours at 498°K (HTOT burn-in), 50 devices previously burned-in for 168 hours at 125°C (M38510, Class B) and 50 devices previously burned-in for 240 hours at 125°C (85M03766, Class SM). The purpose of these tests was to evaluate the relative effectiveness of the three screening methods. The life test circuit, test procedures and facilities were identical to those described for the Phase C life tests. However, an ambient test temperature of 513°K was arbitrarily selected to provide failure data at a temperature different than any of the Phase C life test temperatures. The cumulative numbers of device failures observed at each electrical measurement time, and categorized by failure mode are shown in Table 9. As previously observed in the HTOT #2 test at 523°K, two distinct failure mechanisms were observed; surface instability and gold penetration into emitter junctions. The total number of devices that failed as a result of each mehcanism is shown in Table 10 to aid in comparing the effectiveness of the three screening techniques.

TABLE 10. FAILURE MECHANISM SUMMARY

DEVICE TYPE	NUMBER OF FAILURES		
	SURFACE INSTABILITY	GOLD PENETRATION	TOTAL
M38510, Class B plus HTOT burn-in	1	21	22
M38510, Class B	3	2	5
85M03766, Class SM	1	9	10

Since burn-in is primarily effective in detecting surface related failures, it is not unexpected that the 85M03766, Class SM screened devices experienced fewer surface related failures than the M38510, Class B screened devices. Class SM devices are burned-in at 125°C for 240 hours, whereas Class B devices are burned in at 125°C for only 168 hours. However, the one surface related failure of an HTOT burned-in device at 32 hours was unexpected, since no surface related failures had occurred in the Phase C life tests after 16 hours of test at 498°K. Consequently, a test error or faulty test fixture was suspected. Examination of the failed device electrical

TABLE 9. SCREENING COMPARISON TEST SUMMARY

TEST GROUP & PART NO.	QTY.	T_A °K	T_J °K	FAILURE MODE	CUMULATIVE NO./% FAILURES AT HOURS OF TEST										
					4	8	16	32	64	128	256	512	1000	2500	4000
SCREEN, COMP. #1 SNM54L10T, PLUS HTOT BURN-IN - CELL 5	50	513	539	A B TOTAL %	0 0 0 0.0	0 0 0 0.0	0 0 0 0.0	1 0 1 2.0	1 0 1 2.0	1 1 2 4.0	1 1 2 4.0	1 1 2 4.0	1 6 7 14.0	1 16 17 34.0	1 21 22 44.0
SCREEN, COMP. #2 SMC54L10T, M38510 CLASS B - CELL 6	50	513	539	A B TOTAL %	1 0 1 2.0	3 0 3 6.0	3 0 3 6.0	3 0 3 6.0	3 0 3 6.0	3 0 3 6.0	3 0 3 6.0	3 1 4 8.0	3 1 4 8.0	3 1 4 8.0	3 2 5 10.0
SCREEN COMP. #3 SM54L10F1 - 85M03766, CLASS SM - CELL 7	50	513	539	A B TOTAL %	0 0 0 0.0	0 0 0 0.0	1 0 1 2.0	1 1 2 4.0	1 1 2 4.0	1 3 4 8.0	1 3 4 8.0	1 3 4 8.0	1 5 6 12.0	1 8 9 18.0	1 9 10 20.0

FAILURE MODE DEFINITIONS:

A - SURFACE INSTABILITY

B - GOLD PENETRATION

parameter values throughout the burn-in test showed a progressive degradation of Input High Current (I_{IH}) up to the 16 hour readout. At the next readout (32 hours) I_{IH} had recovered to approximately its initial value. This recovery is indicative of a surface related failure annealing as the result of an unpowered high temperature bake. Inspection of the test records showed that test sockets had to be changed for this device at the 32 hour readout due to an open solder joint. Therefore, since this particular device was installed in a test socket with an open solder joint during the burn-in period between the 16 and 32 hour readouts, it is concluded that the one surface related failure of an HTOT burned-in device is not a legitimate Screening Comparison Test failure.

To evaluate the potential effect of the various burn-in times and temperatures upon failures due to gold penetration, the time-temperature relationship of the gold penetration mechanism was examined. Using the techniques previously described and the failure data from both the Phase C and Phase E tests of SNM54L10T devices, resulted in the Arrhenius acceleration model shown in Figure 22. The Arrhenius acceleration model previously derived for the surface instability mechanism (freak population) is also shown for comparison. Note that the differing burn-in conditions would result in a marked difference in the percentages of freak devices detected, even at 125°C, due to the low activation energy (0.8 ev). However, the effect of the different burn-in conditions upon the number of gold penetration failures (main population) is negligible due to the higher activation energy (2.0 ev). The equivalent burn-in times for the gold penetration mechanism at the Phase E test temperature for each of the three burn-in conditions differ by less than one hour. Thus, the different burn-in conditions should not have affected the percentage of gold penetration failures observed in each cell of the Screening Comparison Test.

Gold penetration into the silicon can occur when the barrier metal, Ti-W in this case, is compromised. Proper controls on both the coverage and thickness of the barrier metal is critical for obtaining long life high reliability gold metalized devices. It is suggested that the gold penetration failures were caused by either voids due to etching problems and/or microcracking of the barrier metal due to either design or processes weaknesses. In addition, a hypothesis for the different number of failures experienced by each test group is based on the distribution of device data codes in the various test cells, and an assumption that more comprehensive process controls were added or a device process or design change was made somewhere within the range of date codes tested. The following is a list of device types, date codes and the number of gold penetration failures traced to each date code.

DEVICE TYPE	DATE CODE	NO. DEVICES	FAILURES NUMBER	FAILURES PERCENT
85M03766, Class Sm	7305	13	9	69
	7348	37	0	0
M38510, Class B	7346	50	2	4
M38510, Class B plus HTOT burn-in	7341 / 7345	50	21	42

Note that almost 70% of the devices date coded 7305 failed and that no devices with date code 7348 failed. Only four percent of the devices with a 7346 date code failed. Forty two percent of the devices with date codes 7341 or 7345 failed, but no records were kept to determine the percentage of failures within each date code.

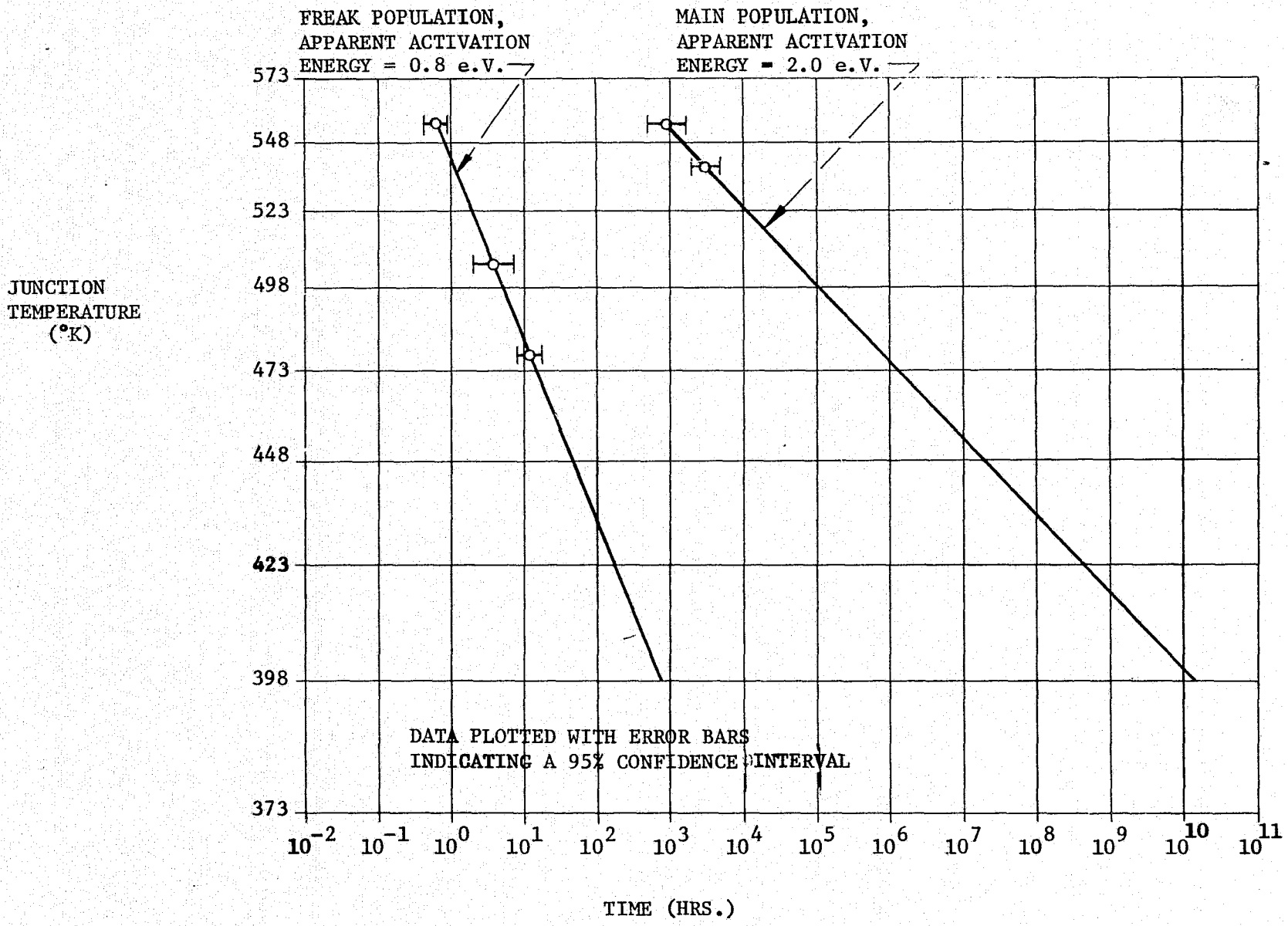


FIGURE 22. ARRHENIUS PLOT, FREAK AND MAIN POPULATIONS OF SNM54L10T DEVICES

4.0 CORRELATIONS AND CONCLUSIONS

Accelerated testing of microcircuits at temperatures between 473°K and 573°K has been shown to be an effective method of screening microcircuits for surface related failure mechanisms. Accelerated tests of 54L10 microcircuits consistently showed that a contaminated portion (freak population) of microcircuits could be screened from the total population of devices in thirty two hours of test at ambient temperatures above 473°K. Equivalent screening at 398°K would require in excess of 1500 hours of test. The relationship of screening time and temperature required to remove all of the freak population is illustrated by the isometric graph of device failure frequency shown in Figure 23. Since it was assumed that the main population of devices would fail due to gold penetration into emitter junctions via microcracks in the Ti-W barrier metal, screening for this failure mechanism is not practical. The gold penetration mechanism is apparently due to a device design and/or manufacturing deficiency and should be corrected by the manufacturer. However, as shown in the previous Figure 23, the gold penetration mechanism may not be a serious reliability hazard at temperatures below 398°K due to the high activation energy (2.0 ev) of this mechanism. The presence of microcracks in the Ti-W barrier metal and subsequent penetration of gold does restrict the maximum allowable burn-in temperature. As may be seen from the previously mentioned Figure 23, ten hours of screening at 556°K will eliminate the freak population, but will also result in a significantly increased probability of failure due to gold penetration at the maximum normal use temperature of 398°K. Seventy-two hours of operation at a junction temperature of 505°K will eliminate 99.9% of the freak population with 90% confidence, and does not result in a significantly increased probability of failure due to gold penetration at normal use temperatures. Thus, 72 hours of operation at an ambient temperature of 498°K (505°K junction temperature) is included in the recommended accelerated burn-in specification presented in Appendix C. The calculated maximum failure rate [2] during the first 100,000 hours of operation at 398°K for devices burned-in at the recommended conditions is 2.2×10^{-14} failures per hour. For comparison, Table 11 shows calculated failure rates for non-burned-in devices subjected to typical 398°K burn-ins. Note the marked improvement in device failure rate resulting from complete removal of freak devices during the HTOT burn-in.

TABLE 11. EFFECT OF BURN-IN ON DEVICE FAILURE RATE

BURN-IN CONDITION	MAXIMUM FAILURE RATE IN FIRST 100,000 HOURS OF OPERATION (FAILURES/HR.)	
	T_J = 398°K	T_J = 323°K
HTOT 72 HOURS AT T_A = 498°K	2.2×10^{-14}	6.7×10^{-17}
NASA 85M03766, CLASS SM 240 HOURS AT T_A = 398°K	4.1×10^{-4}	1.5×10^{-6}
MIL-M-38510, CLASS B 168 HOURS AT T_A = 398°K	4.4×10^{-4}	1.5×10^{-6}
NO BURN-IN	4.6×10^{-4}	1.5×10^{-6}

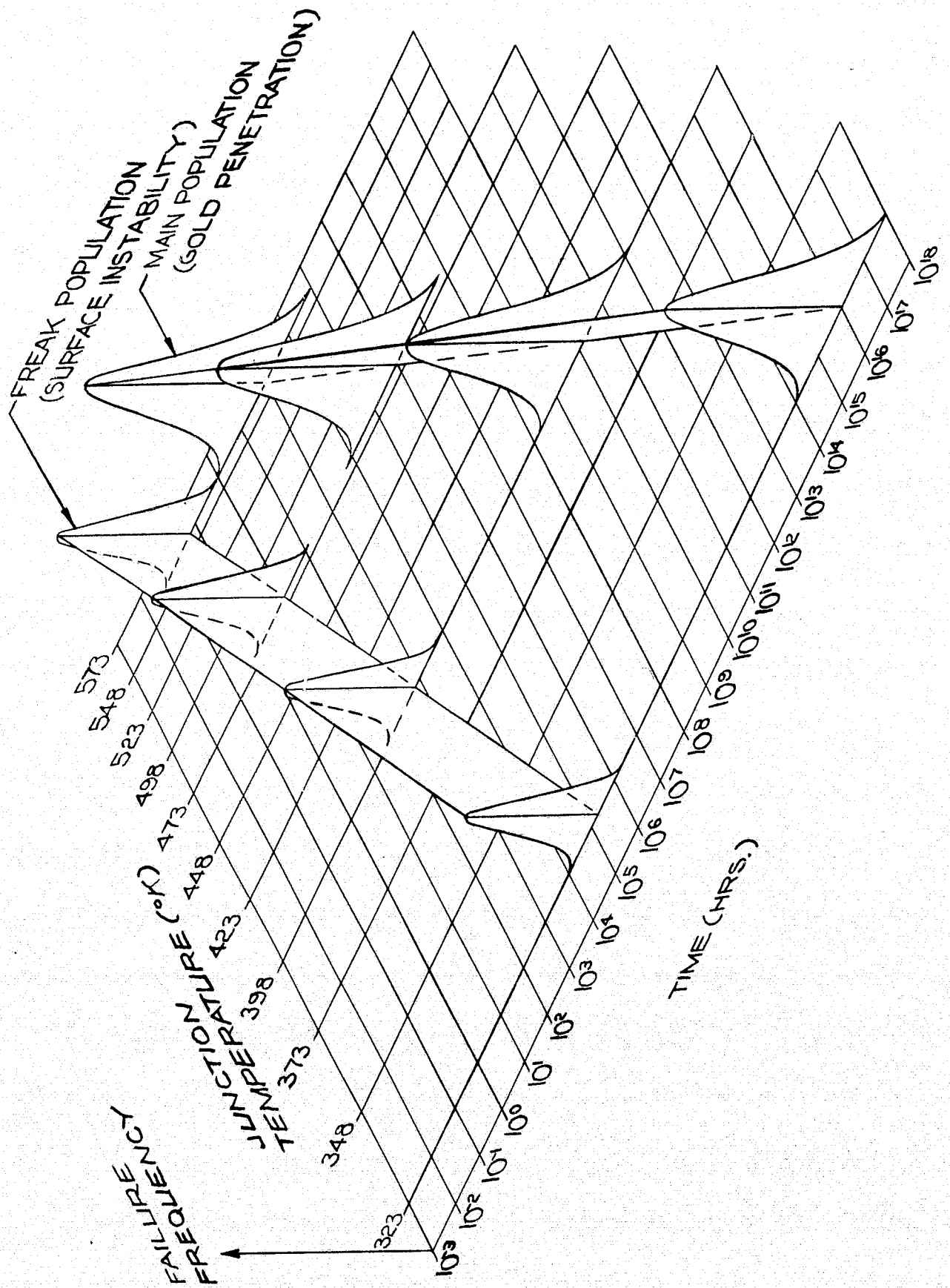


FIGURE 23. ISOMETRIC GRAPH OF SNM54L10
FAILURE DISTRIBUTIONS

Except for the screening time restriction at temperatures approaching 573°K, there was no evidence of detrimental effects due to device operation at junction temperatures of 556°K. Internal examination of devices surviving 4000 hours of test indicated some evidence of gold electromigration and cracked quartz glassivation, primarily at junction temperature above 539°K. However, no device failures were attributed to either of these phenomenon. Further discussion of these phenomena along with a discussion of discontinuities and voids noted in both Ti-W metallization layers is presented in Appendix B.

Due to the number and types of design and/or processing anomalies noted with the Ti-W, Au, Ti-W metallization system, further study of this metallization system is recommended prior to its use in long life/high reliability applications.

5.0 REFERENCES

[1] D. S. Peck, "The Design and Evaluation of Reliable Plastic - Encapsulated Semiconductor Devices", 8th Annual Proceedings, Reliability Physics, pp 81 - 93, 1970.

[2] D. S. Peck, "The Analysis of Data from Accelerated Stress Tests", 9th Annual Proceedings, Reliability Physics, pp 68 - 83, 1971.

[3] P. Staecker, "K_a - Band IMPATT Diode Reliability," 1973 IEDM Technical Digest, pp 493 - 496.

[4] D. G. Ford, "Safe Fatigue Lifes: The Theory and Practice of Various Estimators and Confidence Bounds", Report ARL/SM 344, Australian Defence Scientific Service, Aeronautical Research Laboratories, April, 1973.

[5] Mary Gibbons Natrella, "Experimental Statistics", National Bureau of Standards Handbook 91, pp 2-13 - 2-14, 1 August, 1963.

[6] D. B. Owen, "Factors for One-Sided Tolerance Limits and for Variables Sampling Plans", Sandia Corporation Monograph SCR-607, March, 1963.

5.1 Referenced Military/NASA Documents

MIL-M-38510 - Military Specification, Microcircuits, general specification for.

NASA/MSFC 85M03766 - Microcircuit, Monolithic Silicon, Transistor-Transistor Logic (TTL) Family of Devices, Specification Control Drawing for.

MIL-STD-883 - Military Standard, Test Methods and Procedures for Microelectronics.

APPENDIX A

MICROCIRCUIT CONSTRUCTION ANALYSIS

1. IDENTIFICATION
   a. Part Name: Triple 3-Input Positive Nand Gate
   b. Part Number: SN54L10T
   c. Date Code: 7341 Serial No.: 52
   d. Package Type: Flat Pack Texas Instruments
2. PACKAGE CONDITION
   a. Cracks, Chips, etc.: No cracks or chips
   b. Adequate Packaging: Flat Pack carrier
3. PACKAGE CONSTRUCTION
   a. Material & Dimensions: .258 X .151, Gold Plated Kovar lid and case.
   b. Lid Seal: Solder seal
   c. Lead Type, Material and Plating: Gold plated Kovar; entire lead from case to tip is gold plated.
4. INTERNAL VISUAL EXAMINATION
   a. Contamination: None
   b. Metallization: Three Layers: Top-TiW (except bond pads), Middle-Au, Bottom-TiW
   c. Pad Size: All pads are approximately the same size; .005 sq.
   d. Surface Protection: Glassivation.
   e. Chip Mount: Gold eutectic scrub in.
   f. Lead Frame: Gold plated Kovar.
   g. Wire: .00098 Gold.
   h. Bond at Chip: Ball Thermocompression bond approximately .0026" dia.
   i. Bond at Post: Thermocompression wedge bond approximately .0023" X .0023".
   j. Chip Dimension: .049" X .049
   k. General Condition: Good.

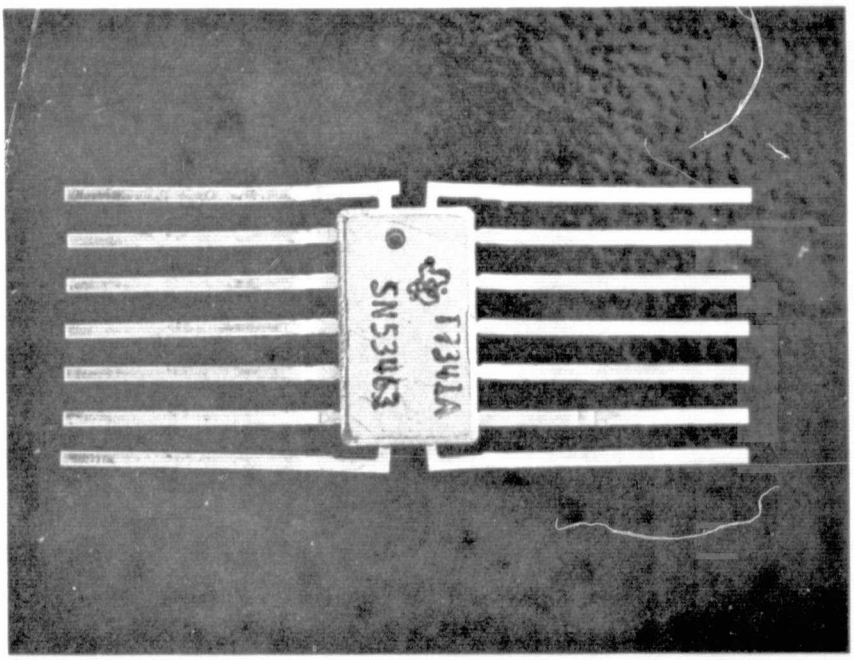


FIGURE A1. PACKAGE PHOTO

SCHEMATIC IMPLEMENTATION

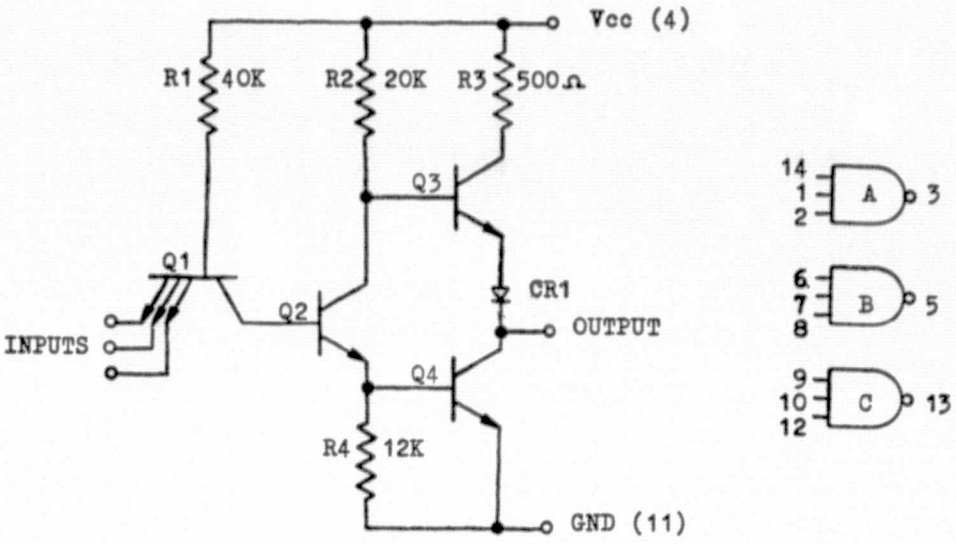


FIGURE A2. SCHEMATIC DIAGRAM

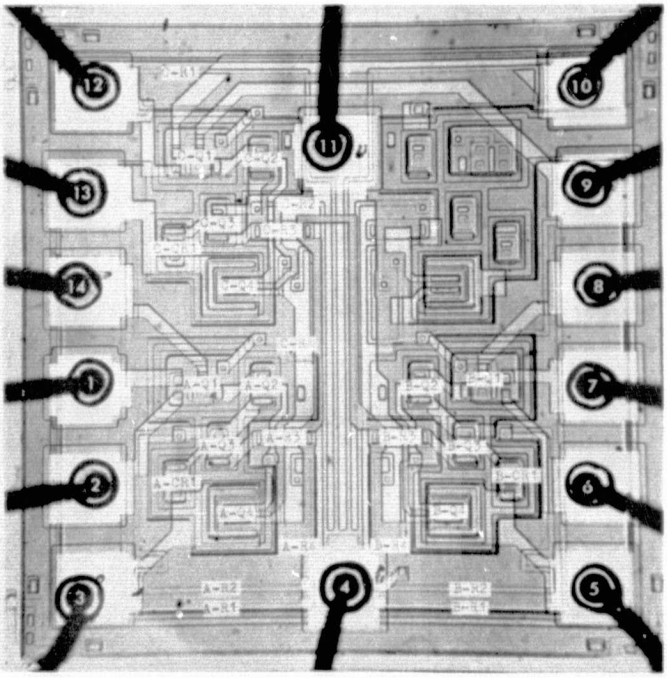


FIGURE A3. CHIP LAYOUT

PHOTOMICROGRAPH

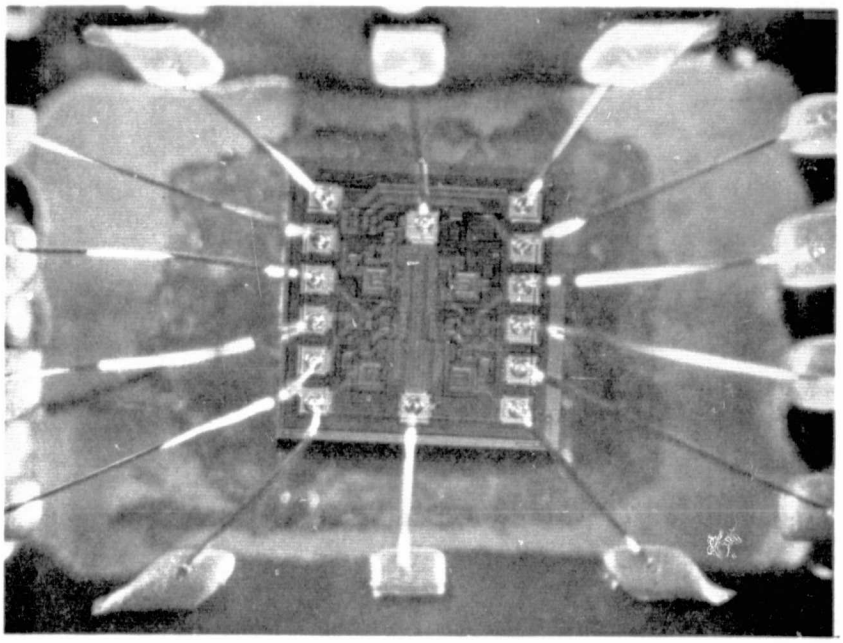


FIGURE A4. DEVICE TOPOGRAPHY

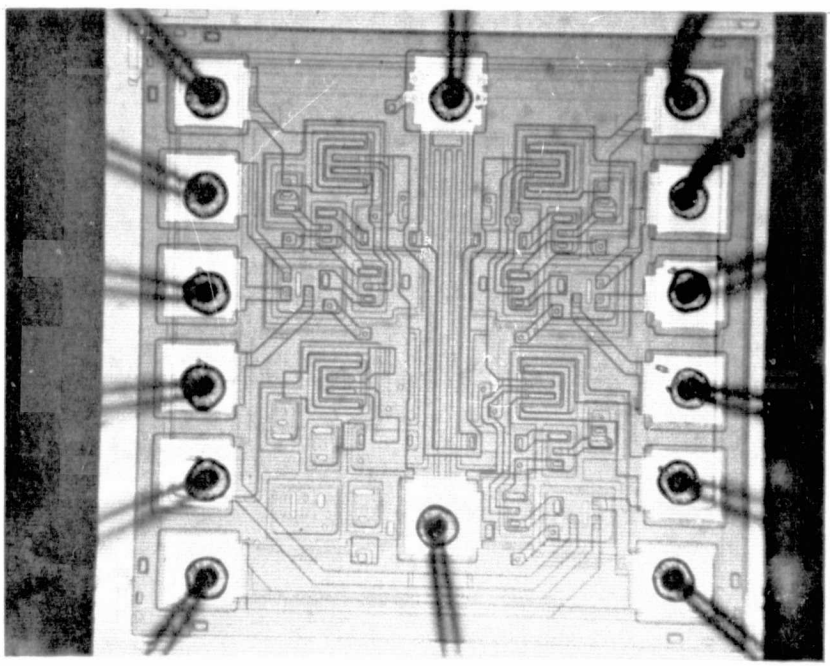


FIGURE A5. CHIP TOPOGRAPHY

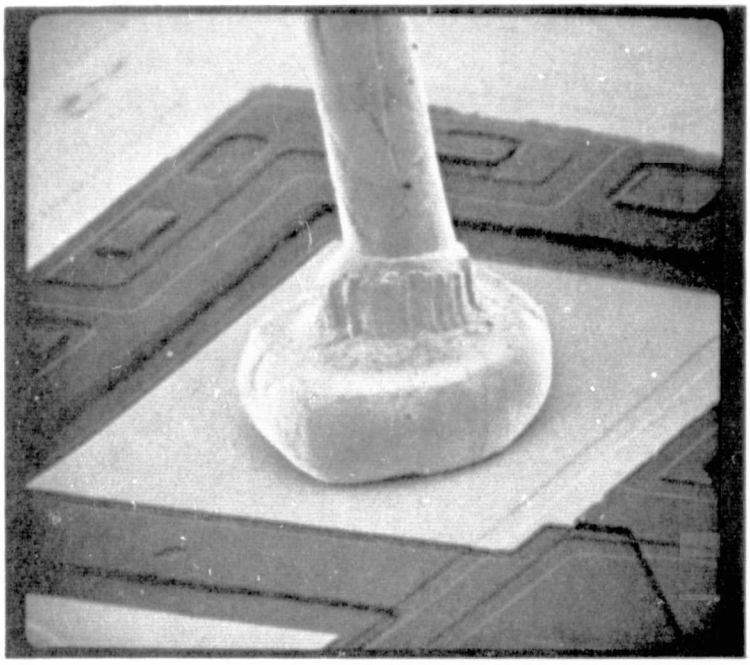


FIGURE A6. WIRE BOND AT DIE

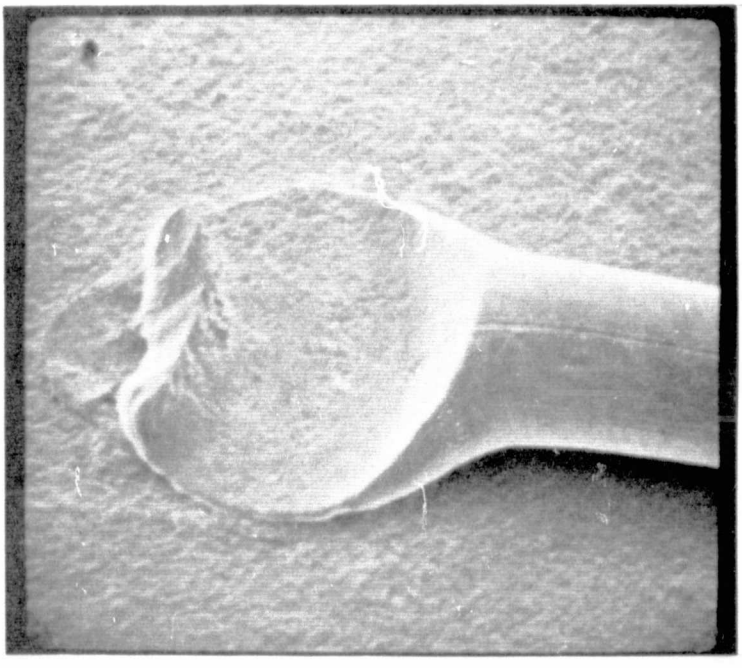


FIGURE A7. WIRE BOND AT LEAD FRAME

APPENDIX B

FAILURE ANALYSIS AND POST TEST OBSERVATIONS

1.0 GENERAL

All 54L10 microcircuits that failed an Interim or Final Electrical Test during Formal Step Stress Test, HTOT Life Tests, Burn-In or Screening Comparison Tests were analyzed to determine the particular failure mechanism. The general analysis procedure was as follows:

a) Complete electrical retest to verify the failed condition.

b) Curve tracer tests to further isolate and identify the nature of the failure.

c) Die level tests, via microprobes, of a representative sample of devices with similar failure symptoms to isolate the failure to a specific junction(s).

d) Unpowered high temperature bakes as a final verification of a surface instability mechanism.

e) Delidding and routine microscopic examination of all failures to confirm the failure catagorizations.

A total of 116 failed devices were analyzed and categorized into three distinct failure mechanisms. Surface instability was the mechanism responsible for 70 device failures and penetration of the gold metallization into emitter junctions was responsible for 45 device failures. One device failed due to an internal lead to case short. The details of the analyses leading to the determination of failure mechanisms are presented in this Appendix.

Also presented is a brief discussion of the general condition of devices surviving 4000 hours of high temperature testing. Parameter symbols, circuit symbols, device pin numbers and life test subgroup identifications referred to in the discussion are as previously defined.

2.0 ANALYSIS OF FAILED DEVICES

2.1 Surface Instability Failures

All devices that failed due to surface instability exhibited out of tolerance values for one or more of the following parameters: V_{OL}, I_{IH1}, I_{PD}, or I_{MAX}. The V_{OL} failures were generally confined to the pin 3 and the pin 5 outputs. The I_{IH1} failures were confined to two of the three inputs of each gate, pins 1 and 2, pins 6 and 7, and pins 10 and 12. All failed parameters would recover upon subjecting the parts to an unpowered bake, which is indicative of a surface instability mechanism. Also, it was discovered that if a failed part were returned to test (without baking), it would recover by the next test period. Fine and gross leak tests established that the devices were hermetic. Die level curve tracer tests of a representative sample of eight devices established the mechanism responsible for each failed parameter. V_{OL} failures were caused by excessive leakage current from the base of the input transistor, Q1, to ground. This leakage current prevented Q2 and Q4 from conducting. Thus, the output was always latched high. The discrepant transistors exhibited a channeled characteristic from base to substrate as shown in Figure B1. The channel was attributed to inversion of the n-epitaxial collector

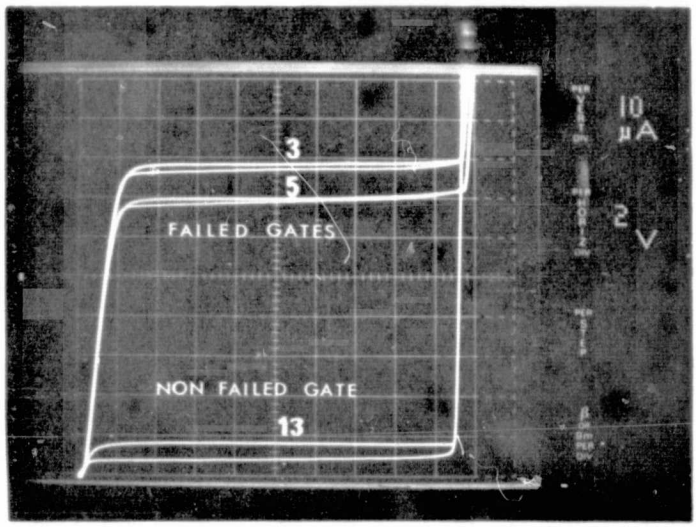


FIGURE B1. I-V CHARACTERISTIC FROM THE BASE OF THE Q1 TRANSISTORS (+) TO THE SUBSTRATE (-).

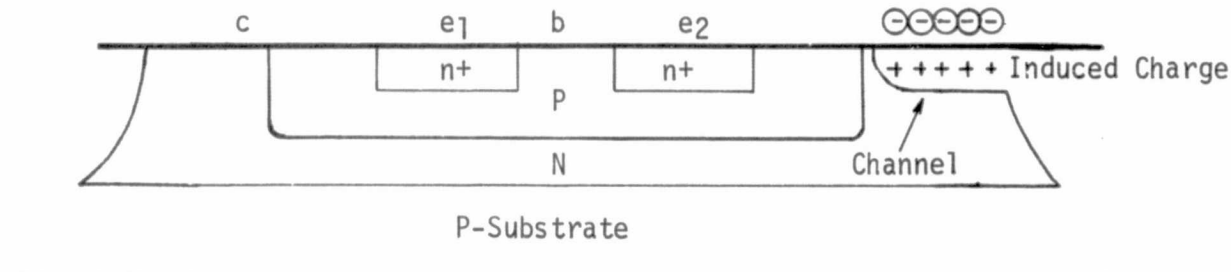


FIGURE B2. DIFFUSION PROFILE OF Q1 SHOWING INDUCED CHANNEL

region, as shown in Figure B2, due to the accumulation of a net negative charge in or over a passivation layer above the collector.

I_{IH1} failures were caused by an increase in the lateral parasitic (NPN) gain between the Q1 input emitter diffusions. This increased gain was attributed to inversion of the p-type base region around the emitters as shown in Figure B3. The inversion is due to the accumulation of a net positive charge in or over a passivation layer above the base. The inverted regions reduced the lateral base widths causing the inter-emitter gain to increase.

I_{PD} and I_{MAX} failures were caused by excessive leakage from the base of Q1 to ground and by excessive leakage from the p-type resistor diffusions to ground. The resistor to ground leakage was caused by inversion of the n-epitaxial resistor isolation tub due to the accumulation of a net negative charge.

Although the majority of devices exhibited only one type of parameter failure, it was established that a net negative charge and a net positive charge had accumulated over the collector and the base, respectively, of the Q1 transistors of each failed device.

On the basis of failure symptoms, curve tracer tests and the effects of stabilization bakes, it was concluded that seventy devices failed due to inversion of the p-type base of Q1 and/or inversion of an n-epitaxial region. A net negative charge had accumulated over the collector and a net positive charge has accumulated over the base of the Q1 input transistors of each device. The charge accumulation could be explained in terms of a common mechanism and cause by charge separation due to the fringing field of the junctions. The emitter-base junctions and the collector substrate junction of Q1 were reverse biased during the high temperature testing. Any mobile contaminant ions above the junctions would be separated by the action of temperature and field, positive ions gathering over the negatively biased base, negative ions gathering over the positively biased collector.

2.2 Failures Due to Gold Penetration

Device failures attributed to gold penetration into emitter junctions via microcracks in the Ti-W barrier metal exhibited out of tolerance values for one or more of the following parameters: V_{OL}, V_{OH}, V_{OO}, I_{IH1}, I_{IH2}, I_{IL}, I_{PD}, or I_{MAX}. The failures were not confined to any particular gates or pins. Some devices failed only one parameter, while other devices failed every parameter. The failed parameters did not recover after subjecting the parts to an unpowered bake, indicating a non-surface-related failure mechanism. In addition fine and gross leak tests of failed devices indicated no loss of hermeticity.

Internal examination of devices after delidding did not show any obvious cause for the failures. Consequently a special study was conducted to determine the nature of the failure mechanism. The results of this study, which led to the conclusion that the failure mechanism is gold penetration into emitter junctions, is contained in Appendix D.

2.3 Package Lead-To-Case Short Failure

One device exhibited excessive pin 6 input leakage after 96 hours at an ambient temperature of 473°K due to a 1.6K ohm short between pin 6 and pin 11 (ground). The

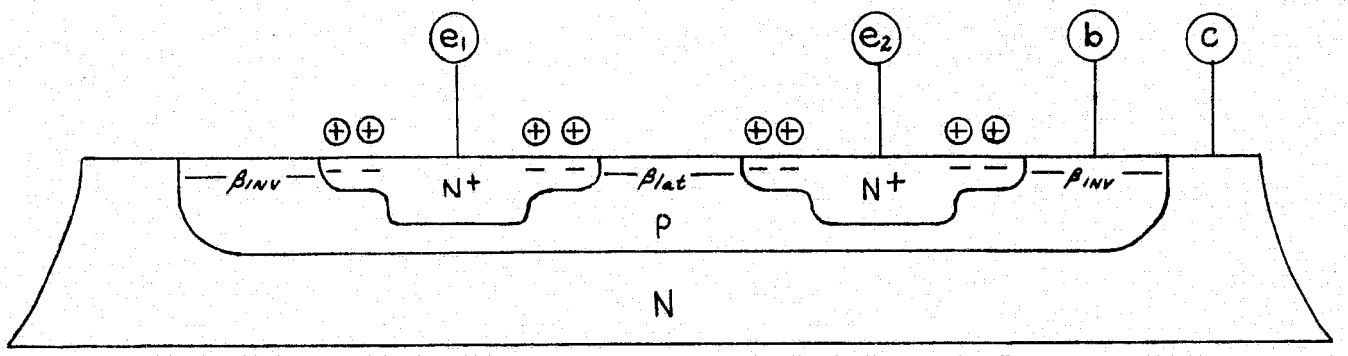


FIGURE B3. DIFFUSION PROFILE OF Q1
SHOWING INVERTED BASE REGIONS

short was caused by contact between the pin 6 package lead and the bottom of the case which is electrically tied to ground. The pin 6 lead had been misaligned or accidently bent downward during assembly as shown in Figure B4. The point of contact is beneath the meniscus of the glass seal.

3.0 POST TEST OBSERVATIONS

In addition to the conditions previously described as the mechanisms resulting in device failure, the following other anomalous conditions were noted:

a) Gold Electromigration - All of the 2500 hour and 4000 hour failures, 50% of the 1000 hour failures, and a few 512 hour failures had developed gold-colored whisker and flake growth at the emitter contact of the Q4 transistors as illustrated in Figure B5. These emitters were forward biased during the test, which indicates the growth is due to gold electromigration. Examination of twenty four 4000 hour survivors (5 or more from each test temperature) established that the electromigration was confined exclusively to the high temperature (513 and 523°K) tests. There were no device failures due to gold electromigration.

b) Cracked Quartz Glassivation - All 4000 hour, 513°K or 523°K failures (and survivors) examined contained cracks in the deposited quartz glassivation as illustrated in Figure B6. Examination of 4000 hour, 473°K and 498°K survivors disclosed that some 498°K devices contained cracks in the quartz, but the 473°K devices did not. These findings indicate that the cracks developed during the high temperature testing. However, flawless glassivation is not expected to craze at the life test stress levels. Thus, the glassivation of these devices was probably inherently weak or deficient.

c) Voiding In the Upper Ti-W Layer - Many devices contained voids in the top Ti-W metallization layer. The most severe case is shown in Figure B7. The voiding was probably caused by a manufacturing etching anomaly.

d) Discontinuities In The Lower Ti-W Barrier Layer - Anomalies in the lower Ti-W layer were first observed as dimples or holes in the glassivation where stripes passed over the oxide steps associated with p-type diffusions as shown in Figure B8. Removal of the glass revealed tunnels or caves in the stripes as shown in Figure B9. Removal of the top Ti-W layer and the gold layer disclosed that the bottom Ti-W layer was discontinuous at the oxide step as shown in Figure B10. The discontinuities were confined almost exclusively to the surface instability failure which suggests that the contaminant ions may have originated from residues trapped in the tunnels.

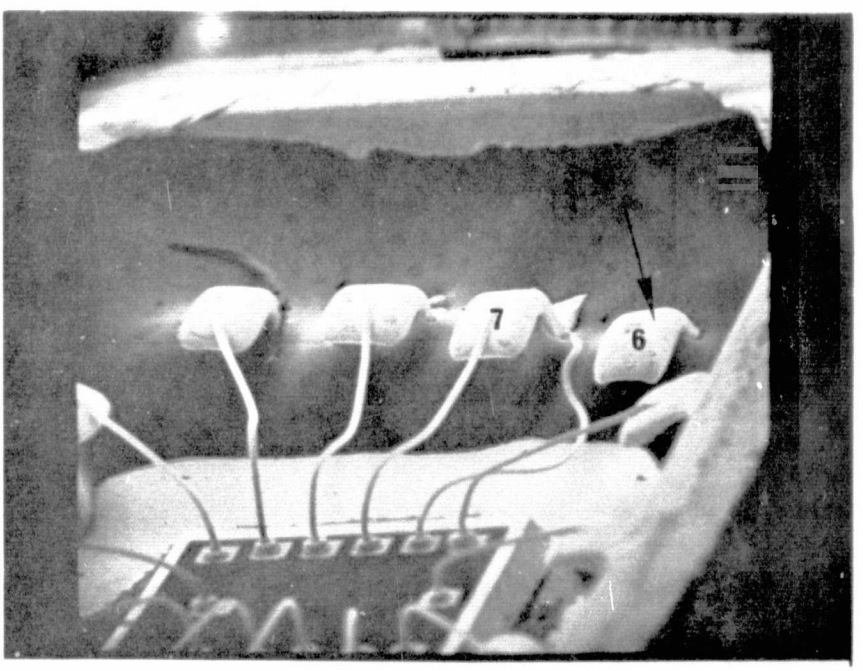


FIGURE B4. SEM PHOTO SHOWING PIN 6
SHORT - 25X

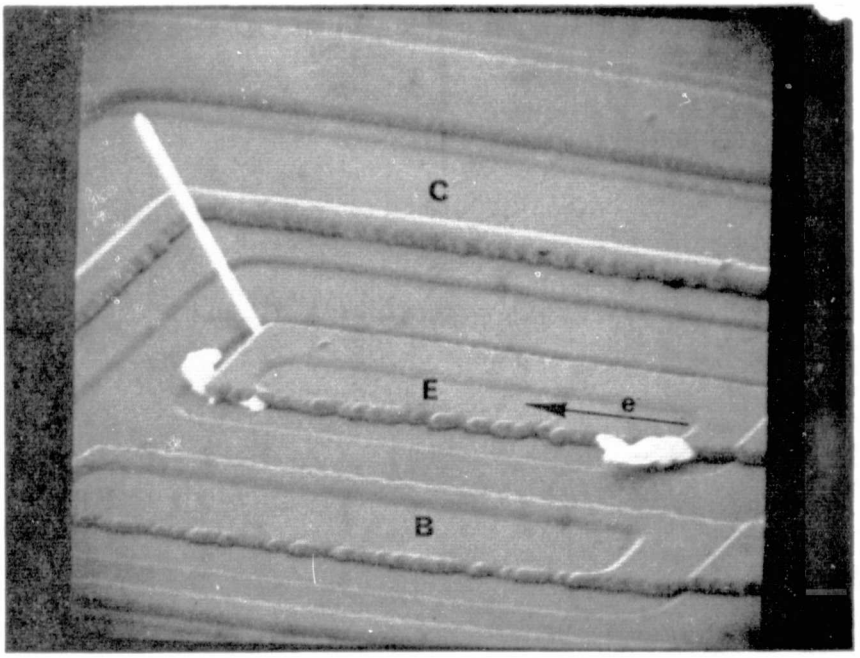


FIGURE B5. SEM PHOTO OF GOLD WHISKER AND FLAKE GROWTH PROTRUDING THROUGH THE GLASSIVATION AT A Q4 EMITTER - 2500X

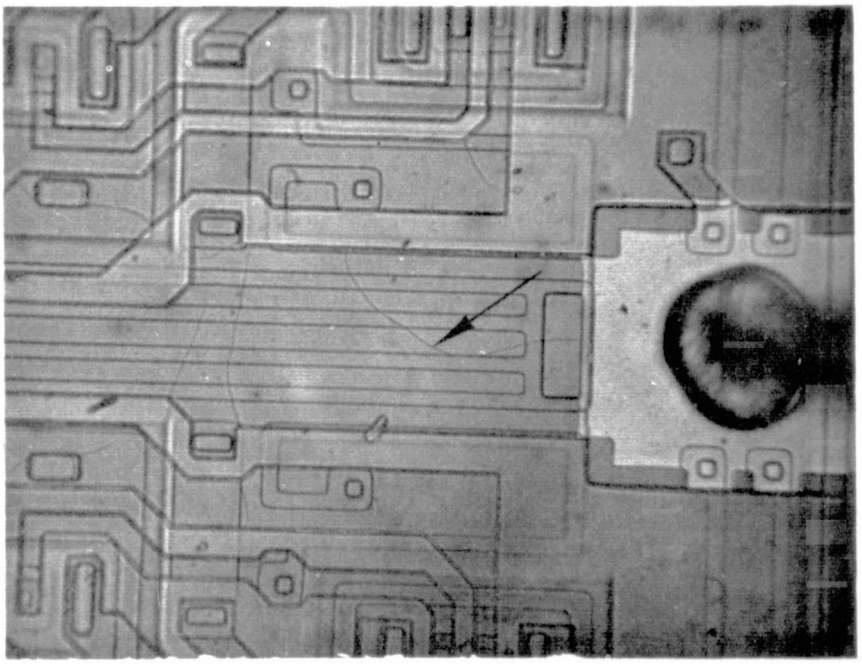


FIGURE B6. PHOTOMICROGRAPH SHOWING CRACKED GLASSIVATION - 250X

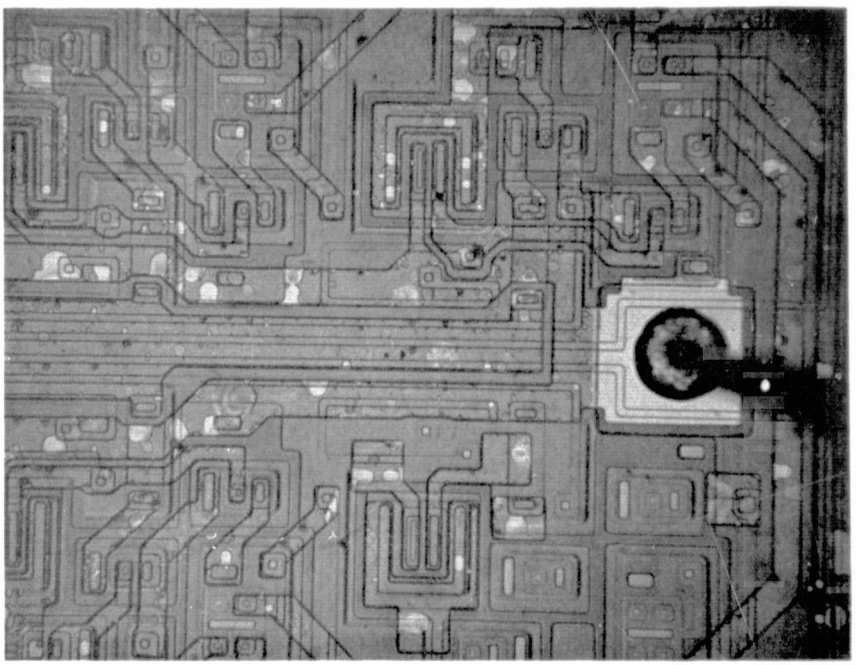


FIGURE B7. PHOTOMICROGRAPH OF VOIDING IN THE TOP Ti-W LAYER (WORST CASE) - 130X

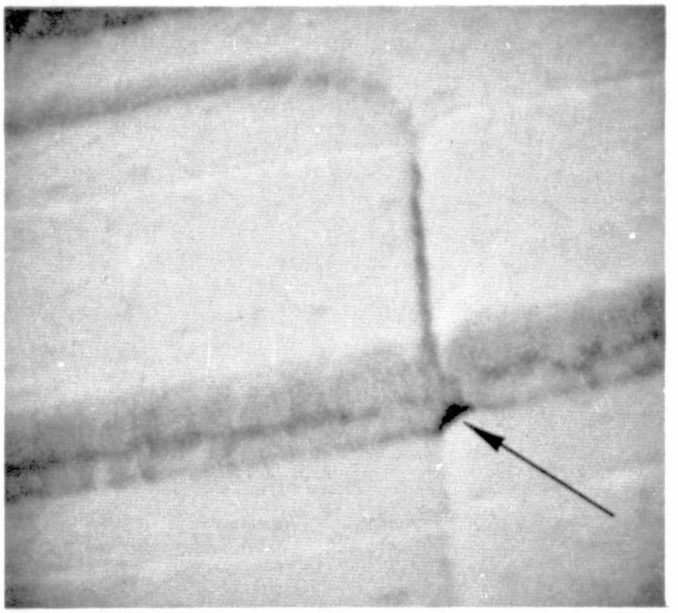


FIGURE B8. SEM PHOTO OF GLASSIVATION DIMPLE AT AN OXIDE STEP - 5000X

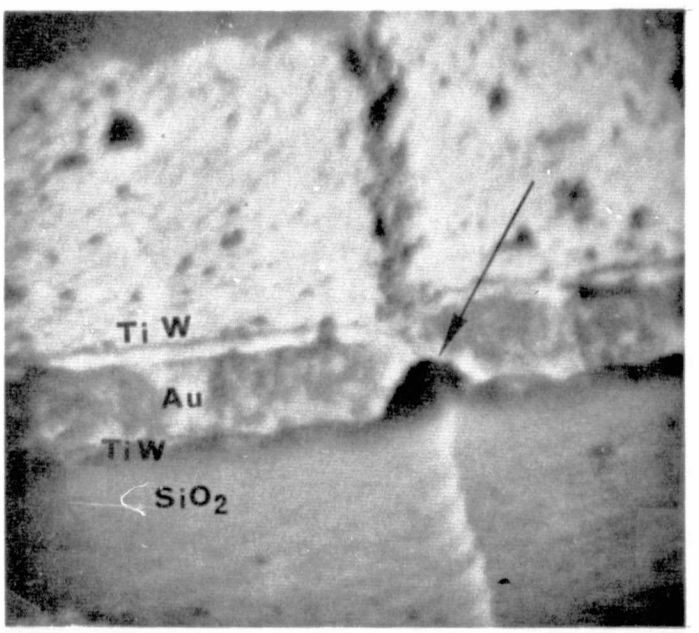


FIGURE B9. SEM PHOTO OF STRIPE AFTER QUARTZ REMOVAL SHOWING TUNNEL. -7000X

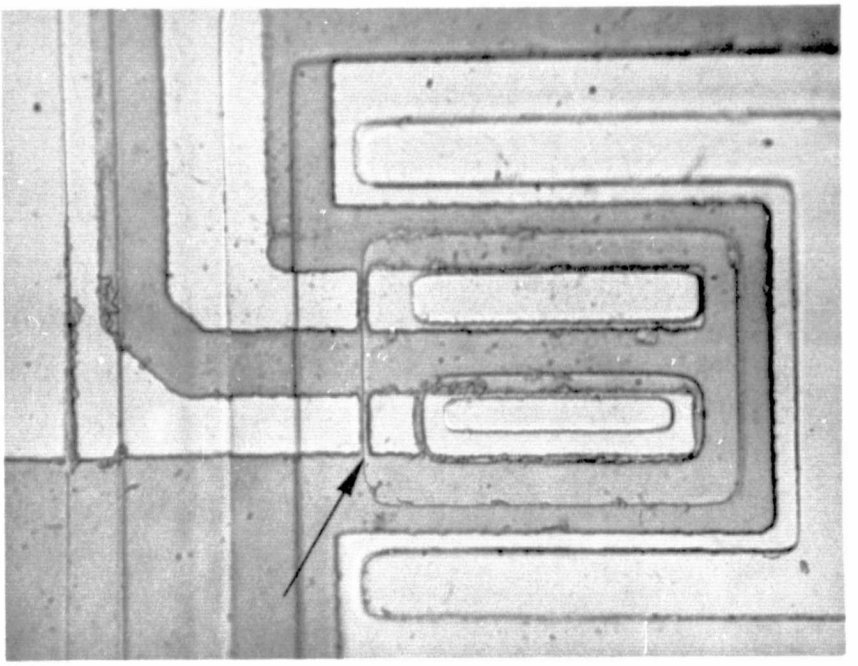


FIGURE B10. PHOTOMICROGRAPH SHOWING DISCONTINUITY IN LOWER Ti-W LAYER - 785X.

APPENDIX C

ACCELERATED BURN-IN TEST SPECIFICATION

GENERAL

An accelerated burn-in specification for a family of 54L type microcircuits manufactured with a Ti-W, Au metallization system is presented herein. The specification is based on the results of tests and evaluations performed on 54L10 microcircuits manufactured by Texas Instruments. Although it is believed that this specification is generally applicable to other devices within the 54L family and other manufactures, long term life characterization tests of other device types are recommended prior to applying this specification to the overall family of 54L devices. Additional life characterization tests should also be conducted if design or processes changes are made. The burn-in temperature specified is the maximum safe temperature that should be utilized to avoid the possibility of unduly accelerating the failure times of main population devices. The specified 72 hour burn-in time is based on the application of tolerance limit statistics [5, 6] to a log normal distribution [4], and provides removal of at least 99.9% of the freak population with 90% confidence.

ACCELERATED BURN-IN TEST

1.0 PURPOSE

The accelerated burn-in test is performed for the purpose of screening or eliminating marginal devices, those with inherent defects or defects resulting from manufacturing aberrations which are evidenced as time and stress dependent failures. In the absence of burn-in, these defective devices would be expected to result in infant mortality or early lifetime failures under use conditions. Therefore, it is the intent of this screen to stress microcircuits at high stress operating conditions to reveal time and stress dependent failure modes in a minimum amount of test time.

2.0 APPARATUS

Suitable sockets or other mounting means shall be provided to make firm electrical contact to the terminals of devices under test in the specified circuit configuration. The mounting means shall be so designed that they will not remove internally-dissipated heat from the device by conduction, other than that removed through the device terminals and the necessary electrical contacts, which shall be maintained at or above the specified ambient temperature. The apparatus shall provide for maintaining the specified biases at the terminal of the device under test and, when specified, monitoring of the input excitation. Power supplies and current-setting resistors shall be capable of maintaining the specified operating conditions, as minima, throughout the testing period with normal variations in their source voltages, ambient temperatures, etc. The test equipment shall preferably be so arranged that only natural-convection cooling of the devices occurs. When test conditions result in significant power dissipation, the test apparatus shall be arranged so as to result in the approximate average power dissipation for each device whether devices are tested individually or in a group. The test circuits need not compensate for normal variations in individual device characteristics but shall be arranged so that the existence of failed or abnormal (i.e., open, short, etc.) devices in a group does not negate the effect of the test for other devices in the group.

3.0 PROCEDURE

The microelectronic device shall be operated in a suitable bias circuit for 72 hours minimum at an ambient temperature of 498°K minimum. Since microcircuits will generally not operate at 498°K as specified in their applicable procurement document, it is necessary that special attention be given to the choice of bias circuits and conditions. Preliminary tests and evaluations shall be performed to assure that important circuit areas are adequately biased, without damaging over-stress of other areas of the circuit. To properly select the accelerated test conditions, an adequate sample of devices shall be exposed to the intended high temperature while measuring voltage(s) and current(s) at each device terminal to assure that the applied electrical stresses do not induce damage. The applied voltage at any or all terminal(s) shall be equal to the maximum rated voltage at 398°K. If necessary, with the specific approval of the procuring activity, the applied voltage at any or all terminal(s) may be reduced to not less than 50% of the specified value(s) when it is demonstrated that excessive current flow or power dissipation would result from operation at the specified voltage(s). The selected bias circuit shall be approved by the procuring activity prior to performing the burn-in test with deliverable microcircuits.

3.1 Measurements

Pre burn-in measurements, when specified, shall be conducted prior to applying burn-in test conditions. Unless otherwise specified, post burn-in measurements shall be completed within 8 hours after removal of the devices from the specified burn-in test condition and shall include all 25°C DC parameter measurements, and all parameters for which delta limits have been specified as interim (post burn-in) electrical measurements. Delta limit acceptance when applicable shall be based on this measurement within 8 hours. Devices shall be cooled to room temperature prior to the removal of bias. All specified 25°C electrical measurements shall be completed prior to any reheating of the devices.

3.1.1 Test Monitoring - The test setup shall be monitored at least initially and at the conclusion of the test to establish that all devices are being stressed as required for the specific test condition. Each device does not have to be checked but sampling techniques may be used. Where failures occur which result in removal of the required test stresses for any period of the required duration, the test shall be continued to assure actual exposure for the total minimum specified duration.

APPENDIX D

SPECIAL STUDY OF FAILURES DUE TO GOLD PENETRATION

1.0 GENERAL

The results of an in depth study of 54L10 devices failing due to gold penetration into emitter junctions is presented in this Appendix. Since the magnitude of this effort far exceeded the scope of the contractually specified failure analysis activity, it was not charged to NASA Contract NAS 5-22233.

2.0 FAILURE SYMPTOMS

A total of 51 devices from life tests at ambient temperatures of 513°K and 523°K exhibited out of tolerance values for one or more of the following parameters: V_{OL}, V_{OH}, V_{OO}, I_{IH1}, I_{IH2}, I_{IL}, I_{PD}, or I_{MAX}. The failures were not confined to any particular gates or pins. Some devices failed only one parameter, while other devices failed every parameter. The failed parameters did not recover after subjecting the parts to an unpowered bake, indicating a non-surface- related failure mechanism. In addition fine and gross leak tests of failed devices indicated no loss of hermeticity.

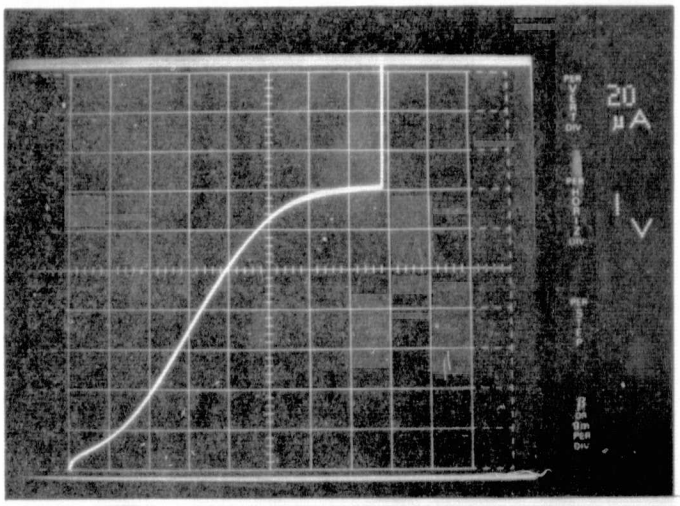
3.0 ANALYSIS RESULTS

Die level probing of a representative sample of six devices indicated degradation of one or more emitter-base junction in each device. Both the forward and reverse characteristics of the junctions were degraded. The degree of degradation ranged from saturating leakage to virtual short-circuits as shown in Figure D1. This degradation had two effects:

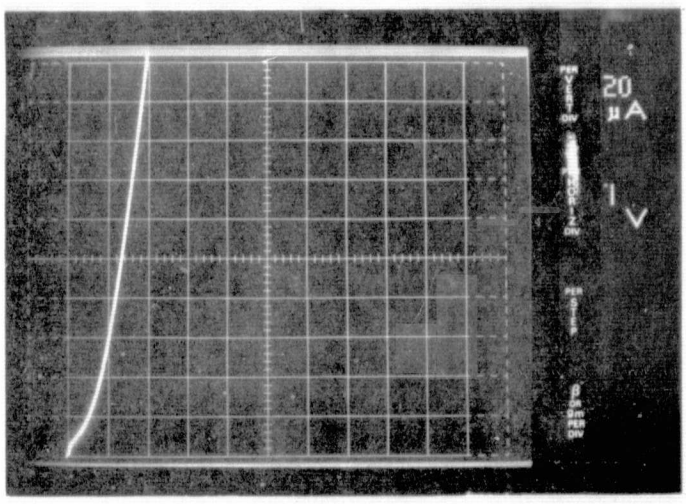
a) Loss of dc gain - Due to the poor emitter-base forward characteristics, the affected transistors exhibited almost no gain and consequently would not turn-on. Loss of gain in transistors Q2 or Q4 resulted in V_{OL} failure. Loss of gain in transistor Q3 resulted in V_{OH} and V_{OO} failure.

b) Excessive I_{EBO} - Due to the poor reverse emitter-base characteristics, the affected transistors exhibited excessive emitter leakage. Excessive emitter leakage(s) in Q1 resulted in high device input current(s) which resulted in I_{IH1}, I_{IH2}, I_{IL}, and occasionally, V_{OL} failure.

The failure mechanism appeared to be independent of current density. Both forward and reverse biased emitters were affected. Furthermore, die level probings disclosed instances where the e-b junction of the metallized Q4 transistor of the unused (fourth) gate was electrically degraded. No sign of damage was found during microscopic examinations of defective transistors after delidding, after glassivation removal, or after metallization removal. After removal of the thermal oxide (using HF acid), the defective emitters always appeared darkened. Sirtl etching of the exposed silicon disclosed that the n+ emitter diffusions had deteriorated as shown in Figures D2 through D5. Figures D2 and D3 show electrically degraded emitters and for comparison normal emitters after Sirtl etch. The n+ doped emitter material around the ohmic contact of the degraded emitters has been almost completely etched away. This degree of etching indicates a change in the composition of the emitter material, probably due to silicon dissolution and metal penetration. Figure D4 shows a degraded emitter in a device that failed after only 16 hours at an ambient temperature of 513°K, and did not contain the degree of damage usually obsereved. Note that in this instance the metal penetration occurred only in one small site directly beneath the contact as indicated by the single deep etch pit.

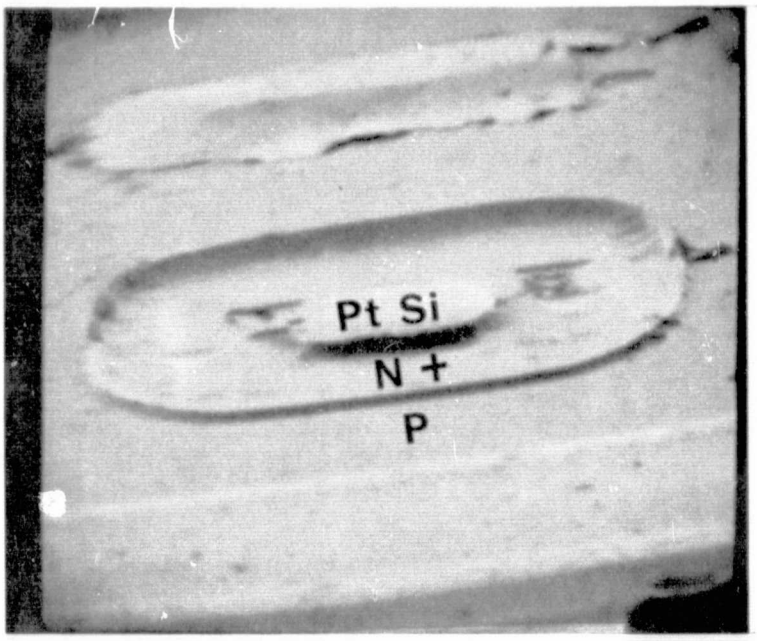


a) SLIGHT DEGRADATION

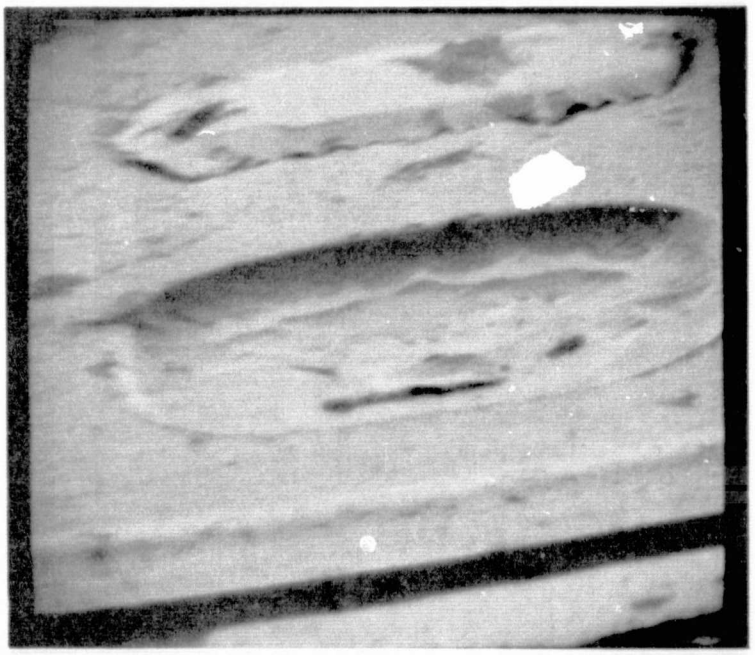


b) EXTREME DEGRADATION

FIGURE D1. REVERSE I-V CHARACTERISTICS OF DEGRADED EMITTER-BASE JUNCTIONS

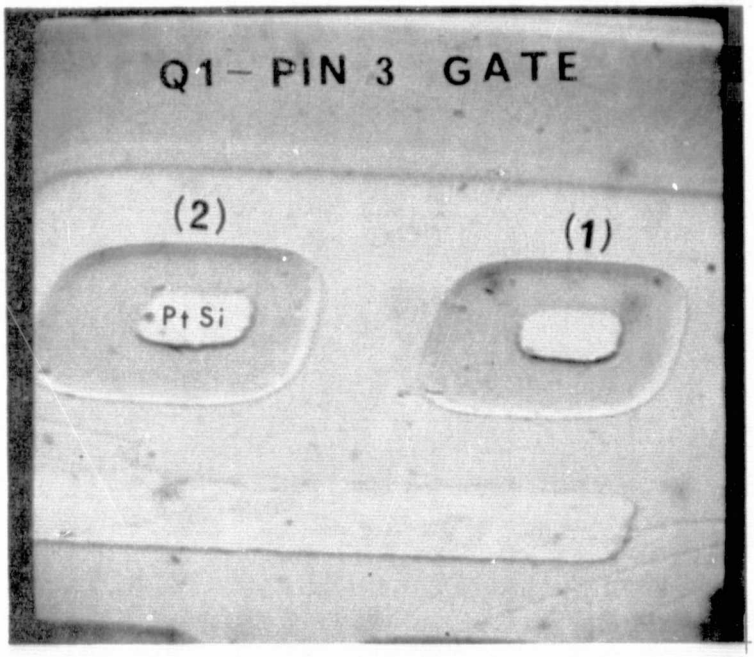


a) NORMAL EMITTER

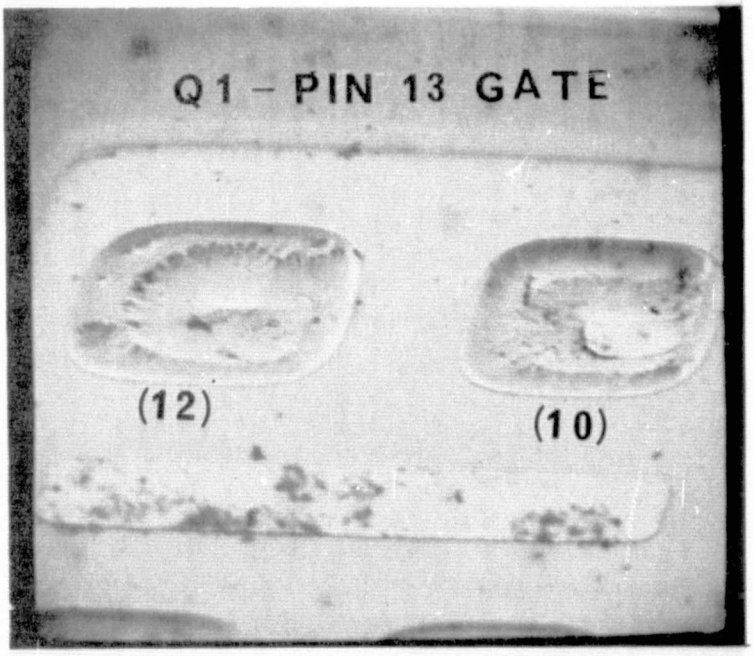


b) DEGRADED EMITTER

FIGURE D2. SEM PHOTOS OF EMITTER CONTACT AREAS AFTER 10 SECOND SILICON ETCH - 3000X



a) NORMAL EMITTERS



b) DEGRADED EMITTERS

FIGURE D3. SEM PHOTOS OF EMITTER CONTACT AREAS AFTER 5 SECOND SILICON ETCH - 1500X

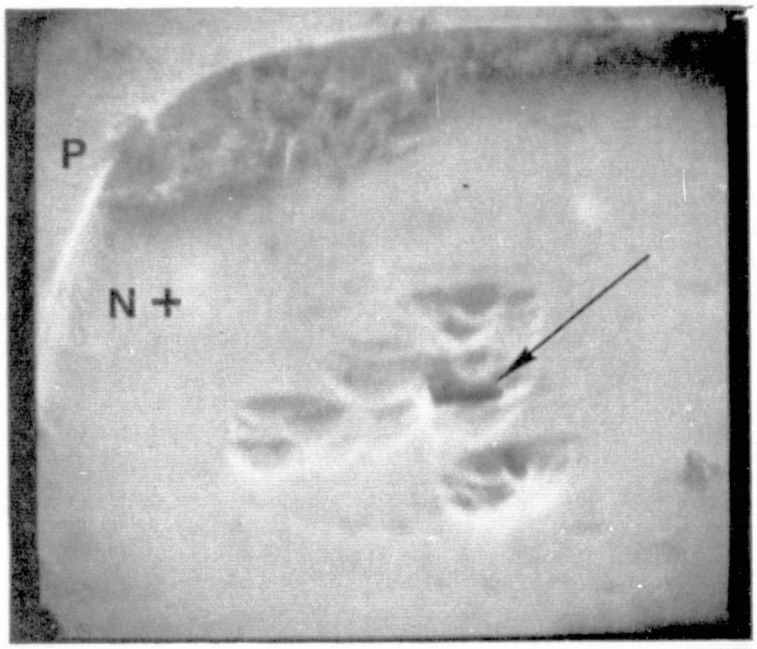


FIGURE D4. SEM PHOTO OF DEGRADED EMITTER WITH SINGLE POINT OF PENETRATION - 5000X

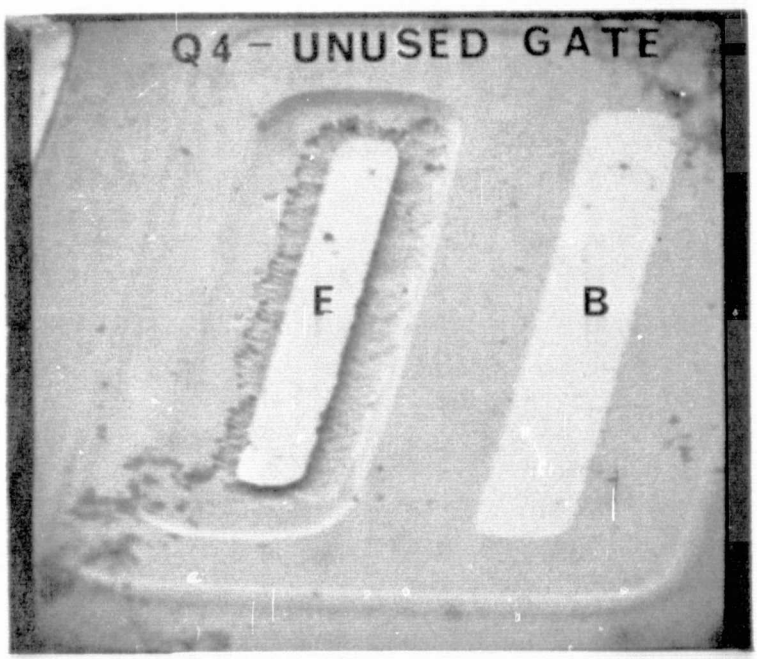


FIGURE D5. SEM PHOTO OF UNBIASED EMITTER - 1000X

Figure D5 shows the condition of one of the unconnected Q4 transistors that contained a degraded emitter. The condition of all the emitters examined indicates that the degradation was caused by metal penetrating the horizontal portion of the shallow diffused junction directly beneath the contact as illustrated in Figure D6. A similar problem had been observed during reliability studies of K_A - band IMPATT diodes [3], and was attributed to gold metallization penetration of the barrier metal and subsequent degradation of the junction.

High magnification optical and SEM examinations of the 54L10 microcircuits revealed discontinuities in the barrier metal, but none at contact windows. However, close examinations of failed transistors after removal of the barrier metal and the thermal SiO_2 revealed gold alloy triangles in the silicon at the collector and base ohmic contacts as shown in Figure D7. The migration occurred along entire sides of contact steps which suggests a barrier metal step coverage problem.

4.0 CONCLUSION

On the basis of the detailed analysis of a representative sample of devices, and failure symptoms, curve tracer tests, etc. of the remaining devices, it is concluded that 45 devices failed due to degradation of one or more emitter-base junction as a result of metal penetration. It is believed that gold migrated through barrier metal defects at the emitter contacts and penetrated the shallow diffused emitter junctions.

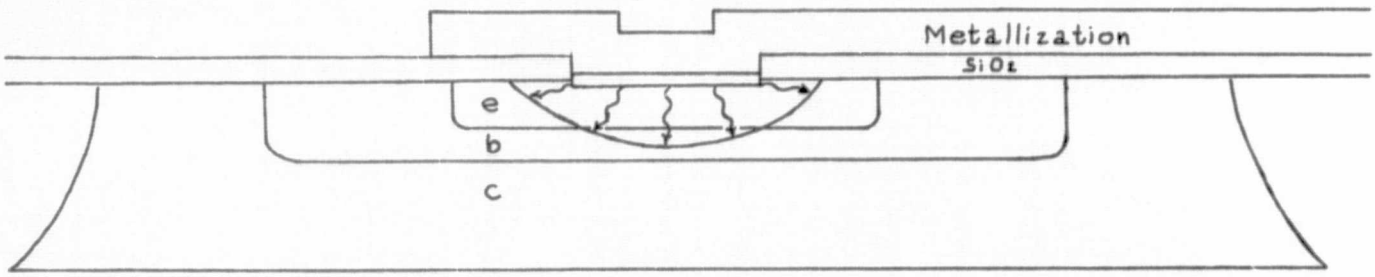


FIGURE D6. DIFFUSION PROFILE SHOWING SUSPECTED PATH OF METAL PENETRATION THROUGH THE EMITTER.

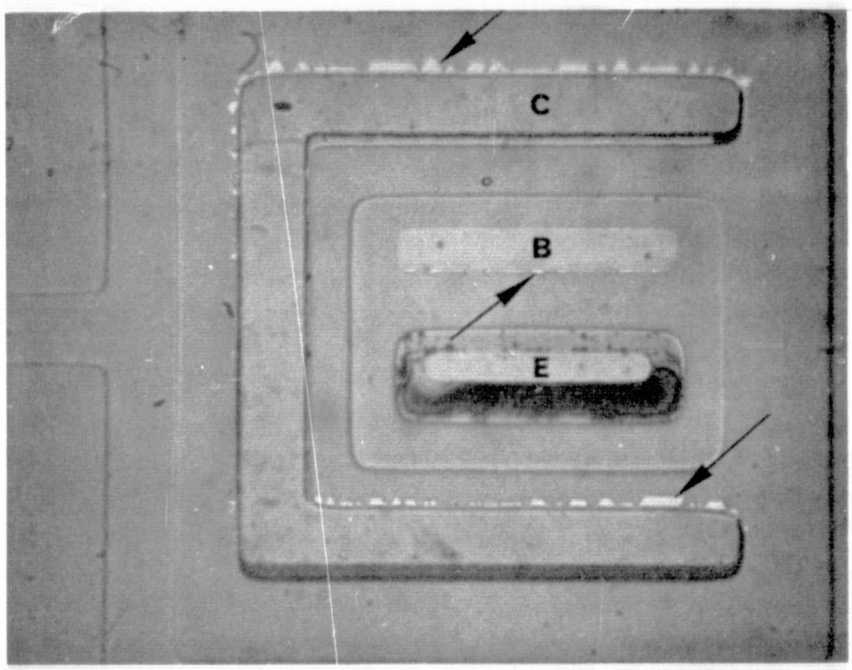


FIGURE D7. PHOTOMICROGRAPH OF GOLD ALLOY TRIANGLES IN Q4 AFTER OXIDE REMOVAL - 780X