(NASA-CR-144052) DATA MANAGEMENT SYSTEM CIU AND DIU. APPENDIX A: CIU AND DIU SCHEMATICS Final Technical Report (SCI Systems, Inc., Huntsville, Ala.) 317 p HC $9.75 CSCL 09B G3/60

N76-21915

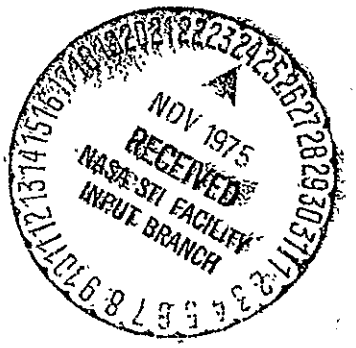
Unclas 19951

COPY 1 OF 13

DATA MANAGEMENT SYSTEM
CIU AND DIU
FINAL TECHNICAL REPORT

PREPARED FOR
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GEORGE C. MARSHALL SPACE FLIGHT CENTER
UNDER CONTRACT
NAS8-29155

PREPARED BY
SCI SYSTEMS, INC
OCTOBER, 1975



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I INTRODUCTION

The information contained in this document constitutes the Final Technical Report for NASA-MSFC contract NAS8-29155.

Information contained in topic II - SYSTEM DESCRIPTION, describes the Computer Interface Unit (CIU) and the Data Interface Unit (DIU) of the Data Management System (DMS) as to it's functional location, purpose and function. This topic describes the CIU and DIU at the unit level illustrating their interface thru the Data Bus (DBUS) and to other DMS units.

Information contained in topic III is pertinent to the Computer Interface Unit while topic IV is related to the Data Interface Unit. These topics provide a description of the unit function and characterisitics. All unit level interfaces are defined as to function and characteristics. The controls, indicators, test points and connectors are listed and function, location and application are described for each. The mechanical configuration is defined and illustrated to provide card and component location for modification or repair purposes. Unique disassembly and assembly requirements are outlined where applicable. A unit internal functional block diagram level description is provided. This description is at a level that an engineer skilled in the electronic disiplines of the hardware could use this as a guide for employing the unit schematics, drawings, listings and procedures to make repairs or modifications.

II SYSTEM DESCRIPTION

Reference drawing "CIU/DIU Interface Block Diagram" for the following description. The CIU is the element of the DMS that controlls all DBUS signal flow. The CIU and DBUS interface sequentially all DIU's to the IOP thru commands from the IOP to the CIU. The CIU interfaces data from the DIU's via the DBUS, data from the IOP and time information to the DMS Recorders via the DECU thru the CIU's Serial Outputs. An illustration of this information flow is illustrated in the drawing "CIU Information Flow". Also illustrated in this flow diagram is a path from the IOP input to the CIU and the CIU's output to the IOP. This is a self test feature between the IOP and CIU. Also illustrated is DBUS input to output flow for the DIU to DIU transfer. In controlling DBUS information flow, the CIU generates the timing and synchronization required, formats all SUPV-DBUS words and controls the transfer sequencing of messages on the DBUS. Upon a control byte from the IOP the CIU selects the Serial Output/s (4 ea) to be active and channels Time and IOP messages or DBUS messages to the output. The CIU performs error checking between the CIU/IOP interface and the CIU/DIU interface. Errors are stored in the CIU, the IOP is notified and upon IOP request the error information is sent to the IOP.

The DIU operates to distribute, translate and to some extent analyze data between the DBUS and the DMS User Subsystems. All data flow on the DBUS is in serial digital form. Data flow to and from the Subsystems may be analog, bi-level digital or serial digital. The DIU must, therefore translate between serial digital and analog or serial digital and bi-level digital and visa versa. Normal distribution for the DIU is to Write (Output CIU ⟶ USER) Analog (AO), Discrete (Bi-level — DO) and Record (Serial Digital — RO) information and to Read (Input USER⟶CIU) Analog (AI), Discrete (Bi-level — DI) and Record (Serial Digital — RI) information. To decrease traffic on the DBUS the DIU contains certain analysis functions.

Three of these functions consist of reading only the DI changes since the last request (Read DI Changes), eliminate the servicing (scanning) of certain DI's (Write DI Monitor Control) and respond only with AI information that exceeds a certain delta limit (Read AI Exceeding Delta). Deltas are established by the IOP via the CIU and DBUS thru the command, Write AI Deltas. To evaluate DIU operation the commanded DO's can be returned by the command-Read DO Status, the Monitor Control information is returned by the command-Read DI Monitor Control, and the Delta limits returned by the command-Read AI Deltas. There are three other commands by which the CIU communicates with the DIU's via the DBUS. One is the DIU to DIU Transfer. This command along with the previously discussed data transfer commands, allows data to flow from one DIU (sending) to another DIU (receiving). In this mode transmission is via the DBUS with the CIU acting as the controlling element and as a switching junction for the information routing. The DBUS is a pair of transmission lines with one referred to as the Supervisory Bus (SUPV) and the other the Reply Bus (RPLY). The SUPV bus carries all communications (data, control, timing and synchronization) from the CIU to the DIU's. The RPLY bus is used for the DIU's reply of identification, data and status to the CIU. In the DIU to DIU transfer the DIU takes the data from the RPLY bus of the sending DIU and appropriately retransmits the data on the SUPV bus to the receiving DIU. In this transaction the CIU also monitors the transfer for proper operation and can also supply the sending DIU's data to the IOP or to the Serial Outputs for recording purposes. Another command supplied by the CIU to a DIU is the Reset command, which initializes the DIU. The final command is the Read Error Status, which ask that the DIU supply the CIU the Saved Error Status from its previous transmission as well as the Current Error Status. All these communication/information transfer operations are illustrated in the drawing "CIU/DIU Bus Word Sequencing."

The DBUS, SUPV and RPLY lines, employ a serial digital coded signal operating at a rate of 2 MBPS. The communications link is differential employing transformer coupling. The serial code is Bi-phase L-Manchester Type II. The bus employs 2 twisted shielded pair cables of 78 ohm impedance extending to 500 ft. in length. Each DIU responds to a unique 5 bit binary coded address. The CIU employs an Address (A) word to command the specifc DIU. This word contains, in addition to a Word Sync bit, Bus Code Prefix bit pair and Parity bit which are common for all standard words, the 5 bit DIU Address, 5 bit OP Code (function command) and 6 bit Channel (User Subsystem Signal Line) Address. Data can be transmitted as a single word or multiple words of varying number as defined by the Word Count (WC) word. The Data (D) word employs a common configuration for both the SUPV and RPLY busses, which is the standard coding bits with two 8 bit bytes to contain the data to be transmitted. When actual information transfer is not in progress on the SUPV bus, the CIU sends continuous Blank (B) words to maintain system timing and synchronization. This is a logic 1 in the Word Sync position and all other bits logic 0's. Thus the Bus Code Prefix (BCP) for the B word is 00. The A word always uses the 11 BCP. The WC word normally uses the 11 BCP unless it is the last word (End of Message) in the CIU SUPV transmission. In this case the WC-EOM employs 01 for the BCP. The D word also uses 01 for the EOM and 10 for all other D words. The only non standard DBUS word is the DIU Sync Word (SW) reply to a CIU command over the RPLY bus. This is a 12 bit word containing a 6 bit fixed sync code of 111101, a 5 bit DIU wired address and parity bit for the unique 5 bit code. The last word in a DIU reply is the Error Status (ES) word. The ES uses a 11 for the BCP and contains 16 bits of error status along with the first bit (word sync) and last bit (parity). The RPLY bus, or rather DIU response, utilizes similar B and D words to those of the SUPV bus (CIU generated). The only difference is that the RPLY bus does not require B words between messages. The B word on this bus is only used internal to a message to fill

word gaps to maintain message continuity. All these words are illustrated in the drawing "CIU/DIU Bus Word Sequencing" and message content and formating of these words is illustrated for each command and both busses.

The CIU Time Input and Serial Outputs employ a serial digital interface that is similar to the DBUS. These signals are communicated via a 200 ft. maximum cable length with only a single transmitter/receiver interface. The Time Code Word (TW) are transmitted in groups of three, once each millisecond, with B words between. The BCP code for TW #1 is 11 and contains Day information in Byte 1 with Hours in Byte 2. TW #2 employs a BCP of 10 and contains Minutes and Seconds respectively in the bytes. TW #3 uses 01 as the BCP and contains milliseconds which require both bytes for coding. The time information is 2 BCD digits per byte. Each of the 4 Serial Outputs contains a Time and Data line. Word formats are maintained per the input. The 4 channels are selectively accessed by the IOP to the CIU thru 4 unique control bits. A 5th control bit sets up a special output mode where by data is only sent when an error is detected. A special IOP to CIU command, employing OP Code 00100, allows IOP data to be sent on the Serial Output/s that has/have been selected.

The CIU/IOP interface is a Standard IBM System/360 and System/370 interface with the Bus Extension Feature. This is a parallel interface employing an action/reaction command sequencing technique, with "sign on" and "sign off" identification. One IOP may service multiple CIU's. The CIU's are sequentially chained to the bus and each employs a unique 3 bit binary address code for response. A third interface of similar configuration interfaces the CIU to a CIU Text Fixture. This interface or the IOP interface is selectively activated by a CIU manual control. The CIU/IOP bus word employs separate input/outputs, each consisting of 2-8 bit bytes with each byte also having a parity bit. Transfer is parallel digital of standard IBM signal characteristics.

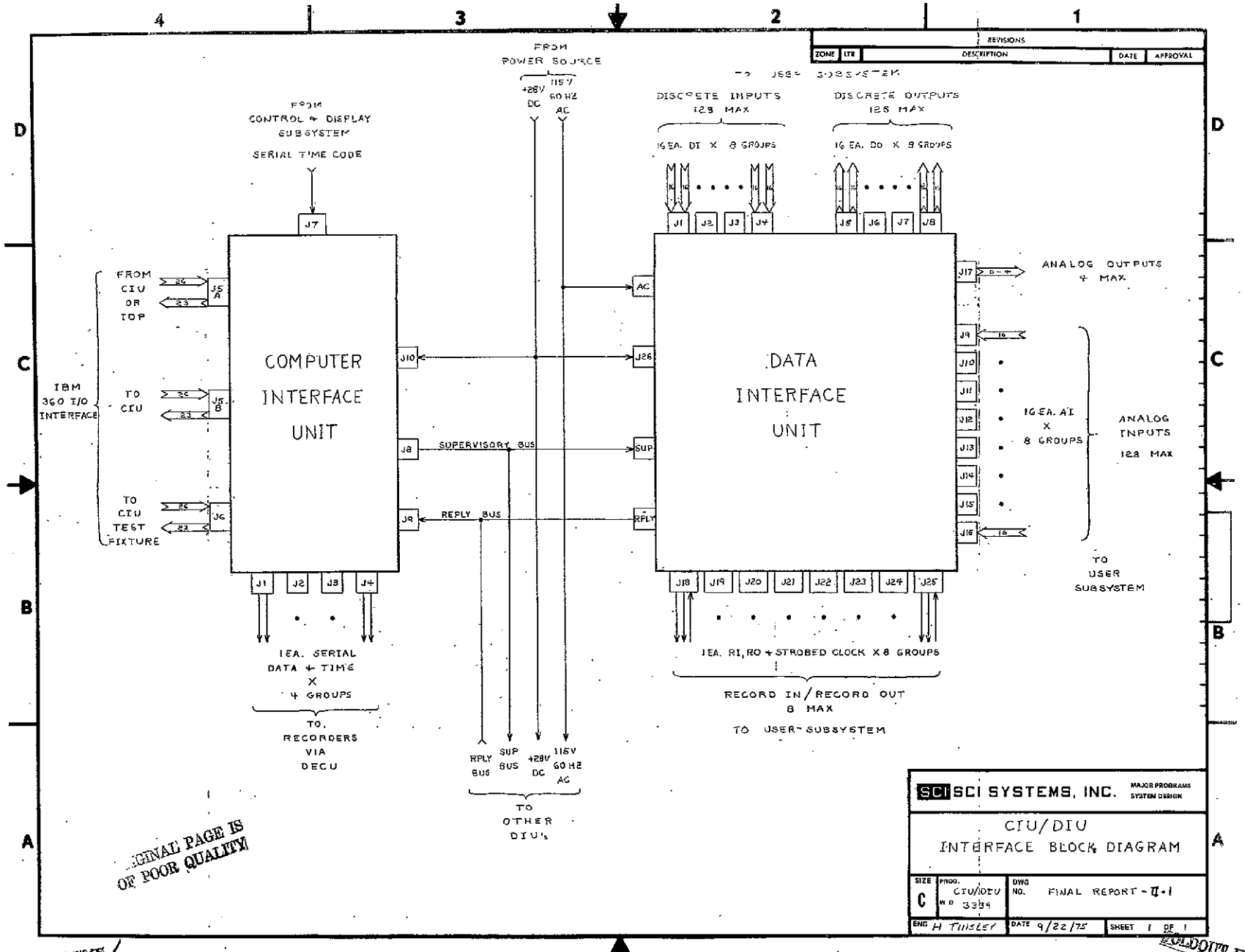
A special command OP Code of 00101 allows IOP commanded self test of the CIU. The CIU responds to all IOP transactions with a 4 bit status byte containing a Unit Check bit (a consolidated error indicator), Device End bit, Channel End bit and Busy bit. The CIU stores and transmits to the IOP upon request 3 error status words. They are: IOP to CIU Transfer Errors, DBUS to CIU Reply Errors and the DIU's Error Status Word.

The CIU front panel houses a power ON/OFF control-display. The time code is displayed in decimal and has an associated Time Error indicator. The 3-bit CIU address code is selected by an octal coded control. A control and bit display allows the operator to select for analysis any of the three Error Words. Also displayed are: Message Sync, Reply Sync and Unit Check. A selector is provided to operate the CIU from its internal clock or an external clock source, the selector for IOP/TEST FIXTURE as previously described, and a RESET control. Additionally test points are provided for critical signals. A special service test switch and all connectors are housed on the rear panel. The CIU is powered from an external 28 volt source and contains a converter to isolate and produce regulated secondary voltages.

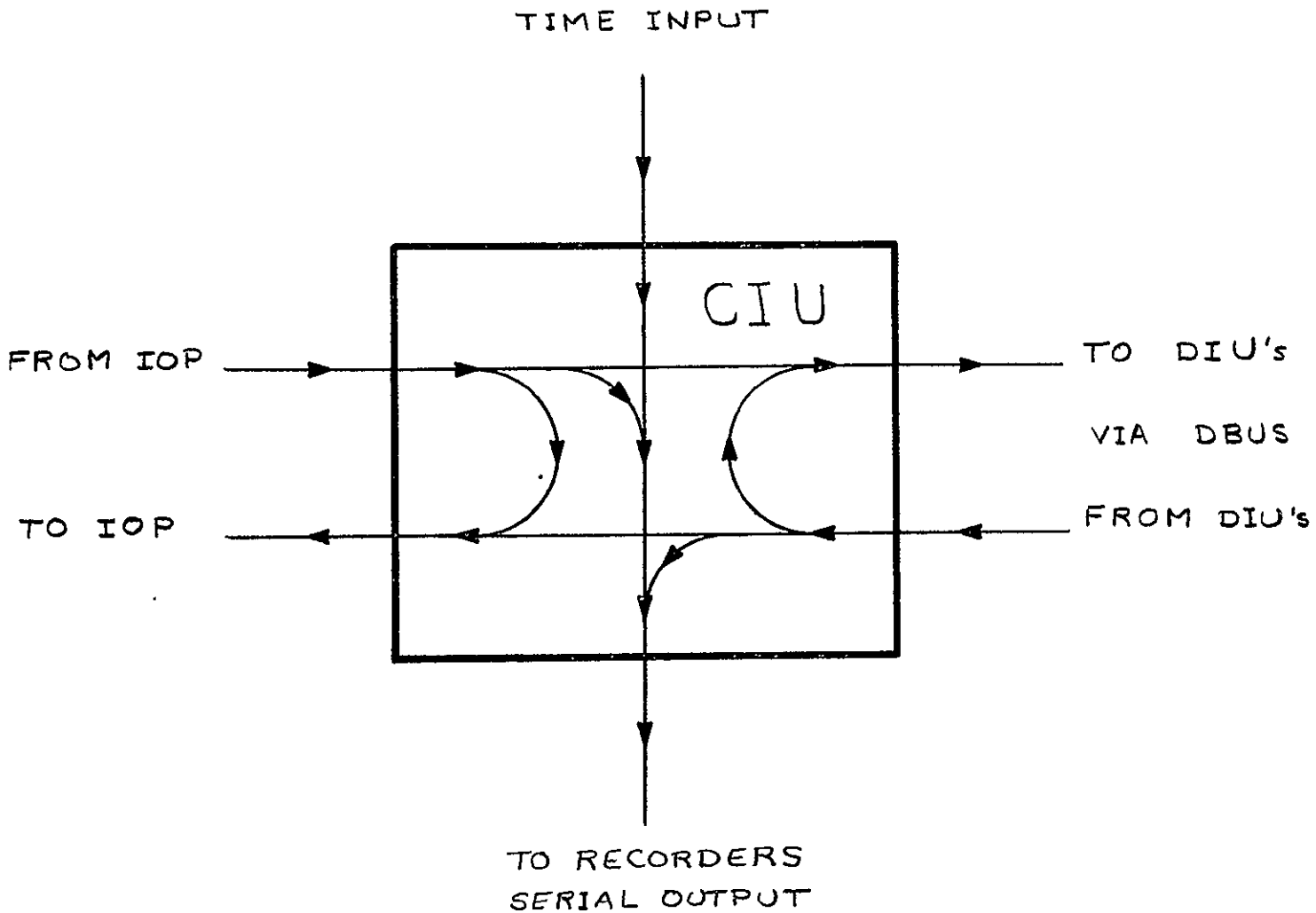
The DIU responds to the CIU commands via the DBUS as previously described. It interfaces to the User Subsystems the Analog, Discrete (Bi-Level Digital) and Record (Serial Digital) inputs and outputs. The AI's provided are a maximum of 128 in groups of 16 each. A 0 to +5 volt signal is digitized to 8 bits with accuracy to $\pm$ the LSB. The AO's have similar characteristics, but a maximum of 4 is provided. The DI's and DO's provided are a maximum of 128 for each in groups of 16 bits. The DI's can be High Level (0-32V) or Low Level (0-5V), selected by a jumper on the internal circuit card. The source voltage for the DO's is supplied by the User Subsystem and can range from 2.5 to 32 volts. Output is continuous levels between up-dates. Each of the 8 RI/RO channels consist of a serial digital data input and output

that has characteristics similar to the other serial digital busses. Cable length is limited to 50 ft. and there is a single transmitter/receiver for each line. The RO line contains continuous B words between messages to maintain subsystem timing and sync. Also each RI/RO contains a third signal that is a 4 MHz clock. The clock is gated ON during the RI/RO message transfer. It also employs a differential, coupled, twisted shielded pair line.

The DIU employs +28 volts for a converter that isolates and produces regulated secondary voltages. A 115V, 60 Hz, AC input is required to operate cooling fans. A control-indicator is located on the front panel to turn ON/OFF the power. The DIU front panel houses displays, controls and test points. The indicators are a bit word display with selector control, modularity and RI/RO clock displays with a modularity selector and four bit displays of: Word Sync, Word Sync Error, Error Detect and Address Detect. Two other selectors are provided and they are: Group Select and DIU Address Select. Appropriate test points are provided for critical signals. The rear panel houses the 29 interface connectors.



CIU INFORMATION FLOW



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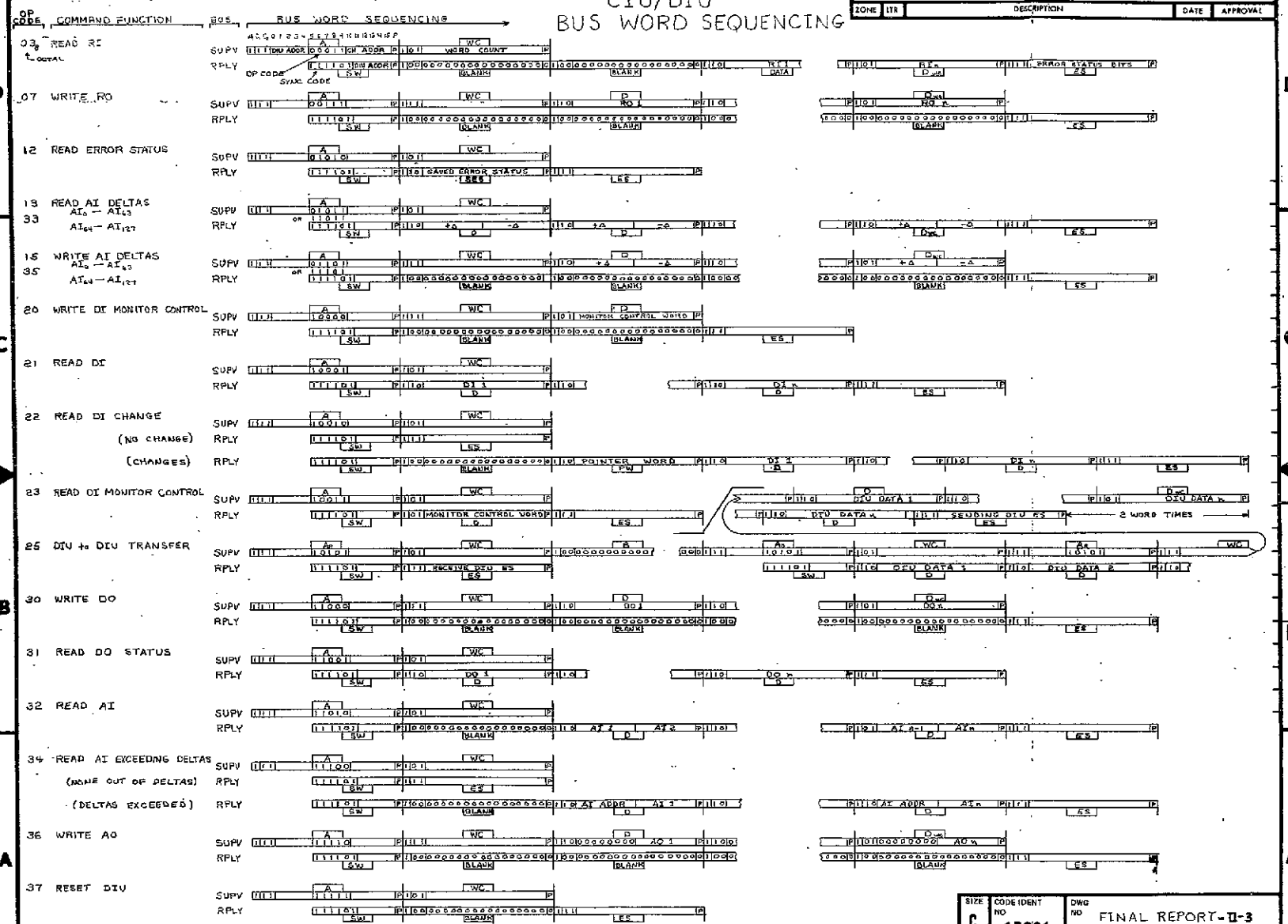
A	17981	FINAL REPORT-II-2
SCALE —	UNIT WT. —	SHEET 1 OF 1

CIU/DIU BUS WORD SEQUENCING

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVAL



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C	17981	FINAL REPORT-II-3

SCALE — +1 | UNIT WT. — | SHEET 1 OF 1

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SECTION III

COMPUTER INTERFACE UNIT
(CIU)

3.0 COMPUTER INTERFACE UNIT

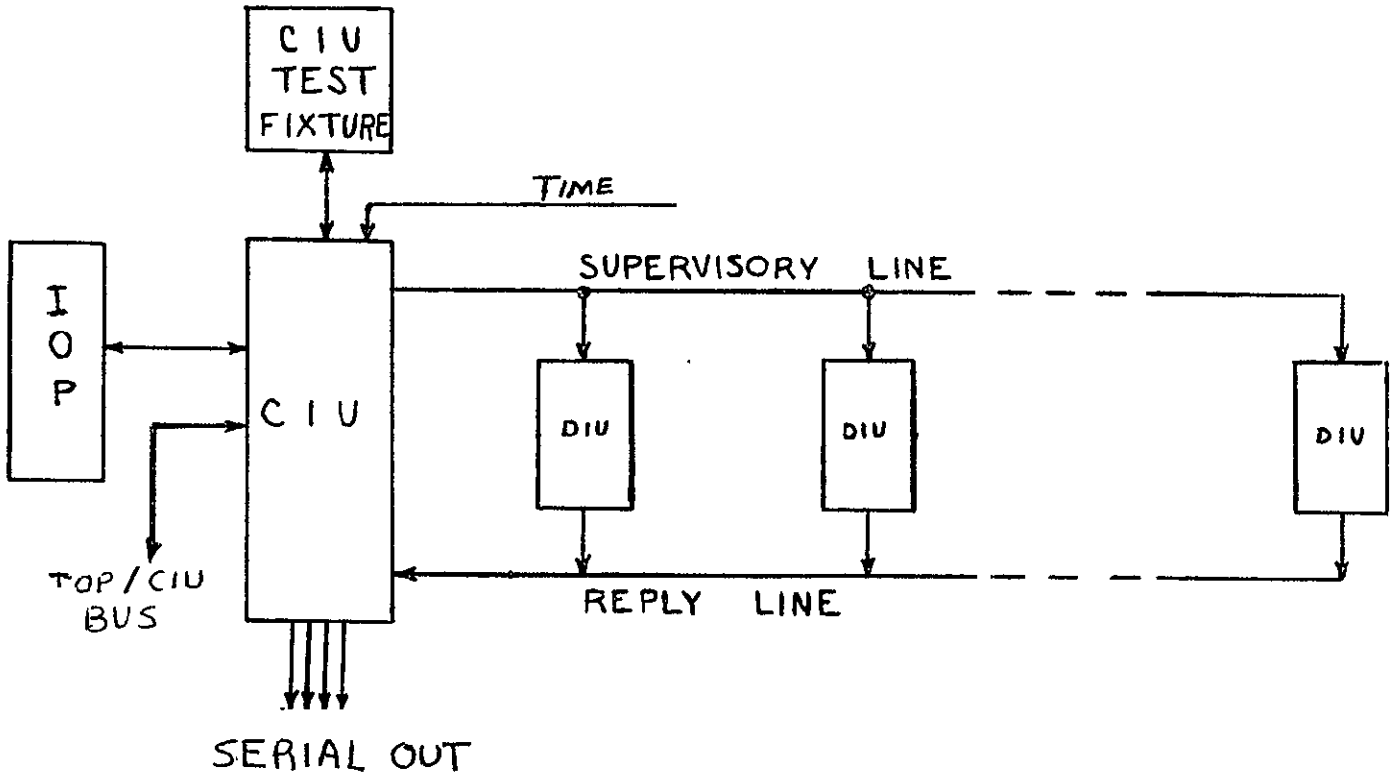
3.1 FUNCTIONAL DESCRIPTION

The Computer Interface Unit (CIU) is the element of the Data Management System (DMS) that formats all data bus traffic. The CIU interface to the IOP may share a common bus with up to seven other CIU's. A typical data bus system is shown in Figure 3.1-1. The CIU interfaces with the IOP, the CIU Test Set, the system Time source, and up to 32 DIU's on a full duplex data bus (Supervisory bus and Reply bus).

The functional characteristics of the CIU are highlighted below:

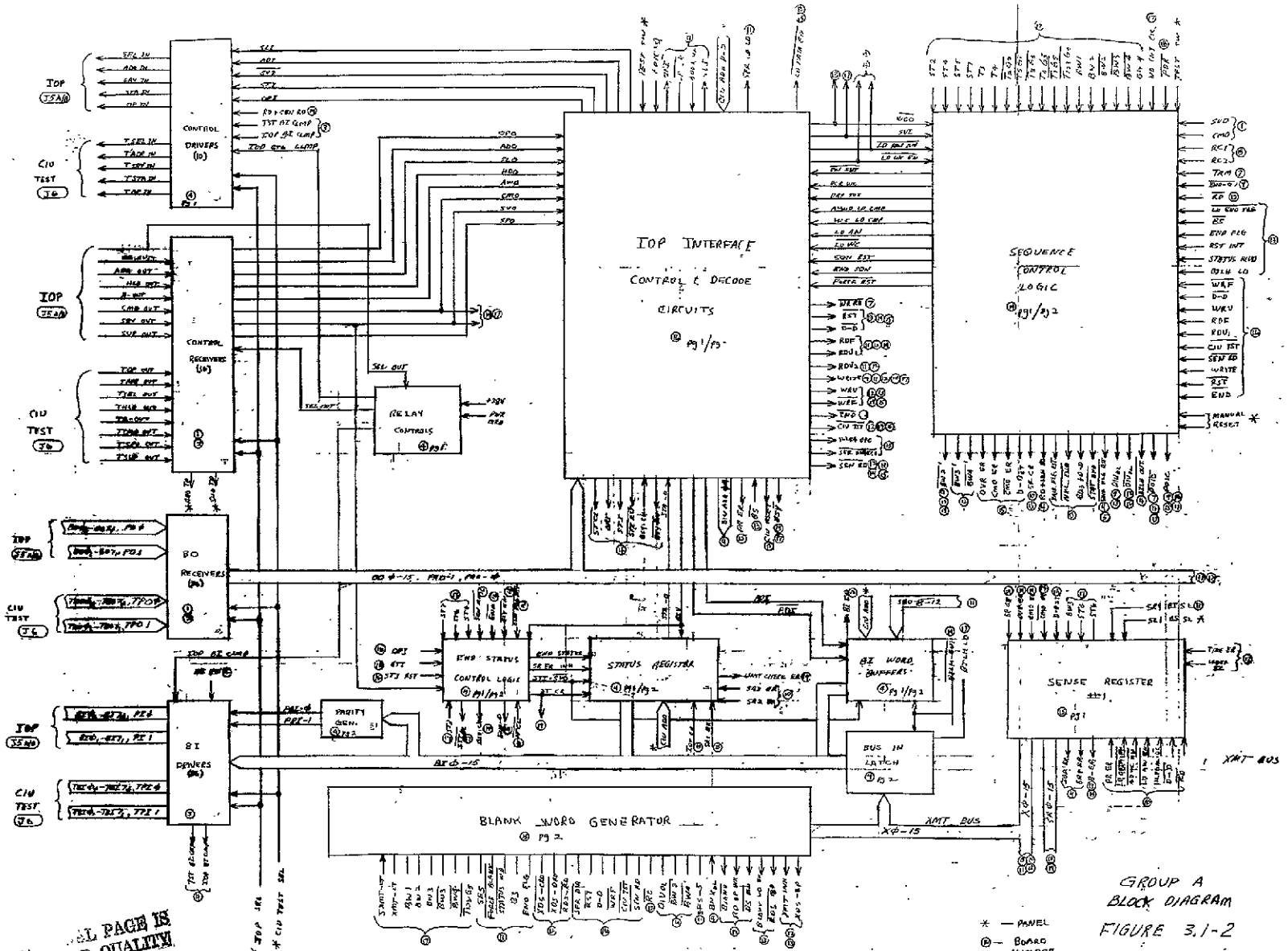
- Generate timing and sync for the data bus.
- Format all data bus words.
- Control the transfer of messages on the bus.
- Check for data bus subsystem errors (Parity, etc.) and interface errors from IOP to the CIU.
- Store CIU and Digital Interface Unit (DIU) detected error indications for each data bus message.
- Provide the capability for computer controlled self test.
- Provide IOP-CIU interface functionally similar to the standard IBM system 360 INPUT/OUTPUT interface.
- Control the transfer and present the received data to the IOP, for DIU to DIU transfers.
- Generate word sync, two control bits and odd parity for each bus word to be transmitted on the Supervisory bus.
- Provide time outputs for time taging recorded bus data.
- Provide serial data outputs.
- Provide indicator lights and test points for critical CIU functions.

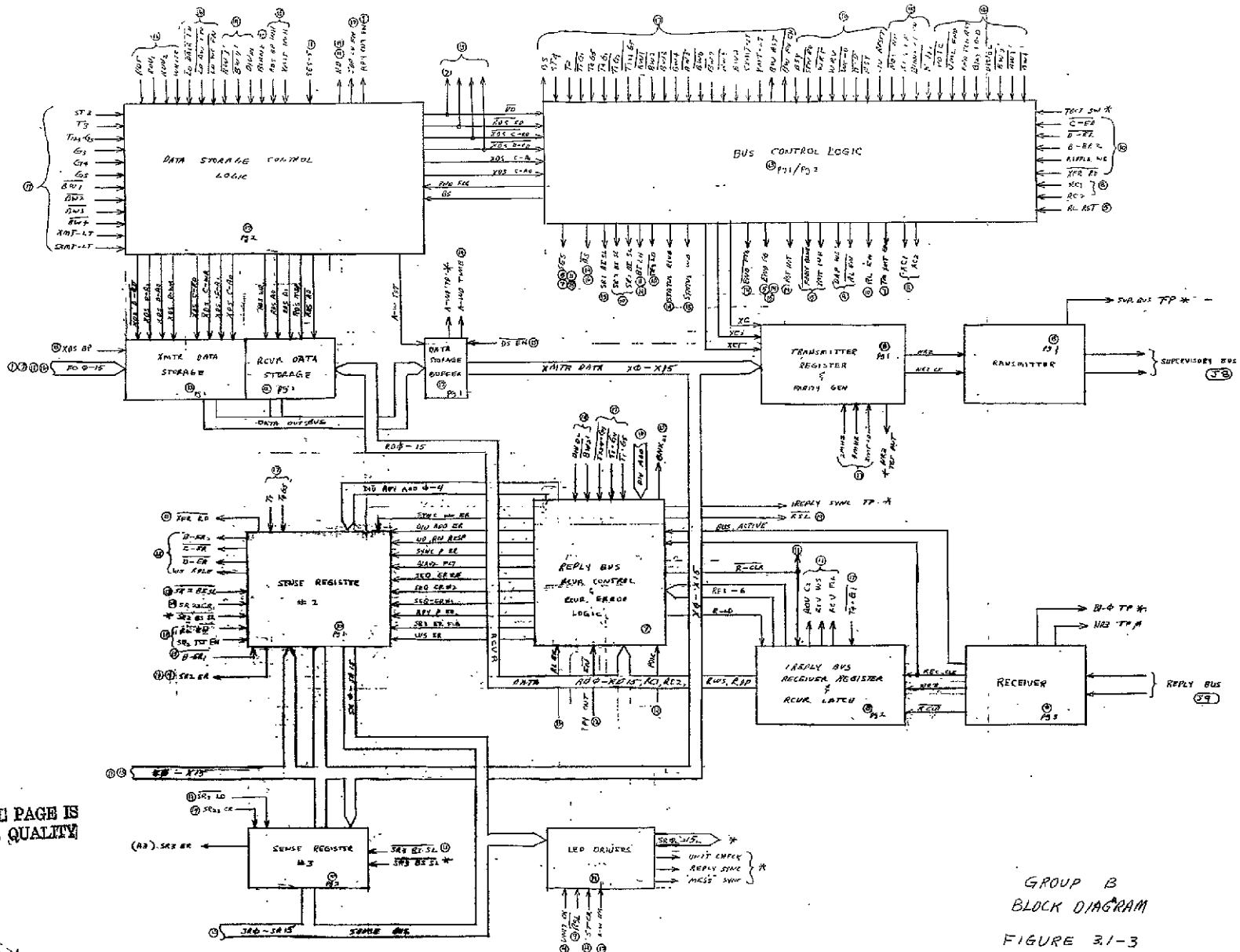
The CIU functional block diagram is divided into three groups. Group A Block Diagram is shown in Figure 3.1-2. Group A is primarily devoted to



DMS-CIU
INTERFACE DIAGRAM

FIGURE 3.1-1





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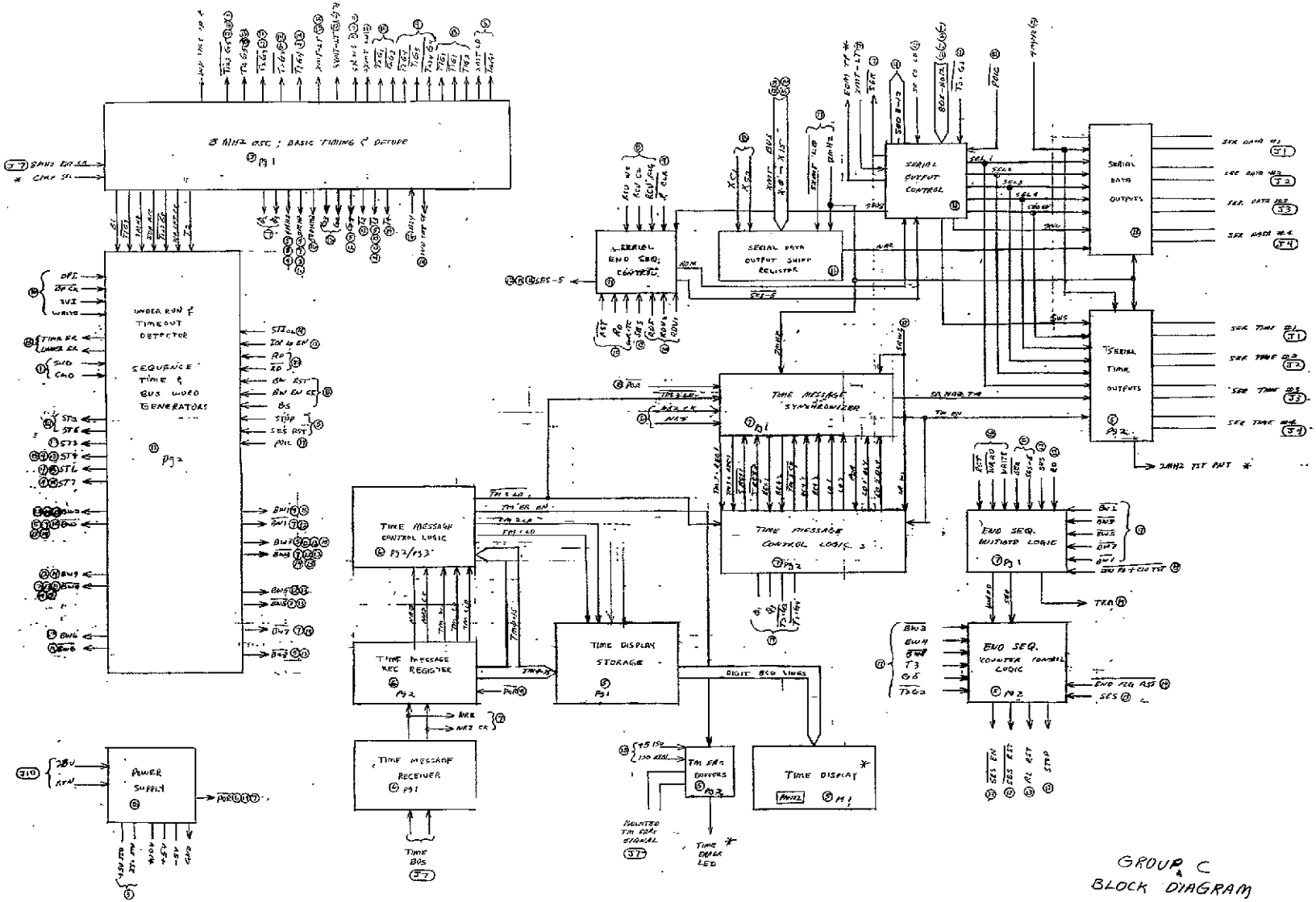
GROUP B
BLOCK DIAGRAM

FIGURE 3.1-3

FOLDOUT FRAME 1

FOLDOUT FRAME 1



GROUP C
BLOCK DIAGRAM
FIGURE 3.1-4

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FOLDOUT FRAME

FOLDOUT FRAME

servicing the IOP interface. Group B Block Diagram is shown in Figure 3.1-3. Group B is primarily devoted to control of the DIU interface. Group C Block Diagram is shown in Figure 3.1-4. Group C is primarily devoted to the CIU timing, Serial Output interface, and CIU Time message interface.

The Block Diagrams of Figure 3.1-2, 3.1-3, and 3.1-4 are referenced to the circuit board location and to the schematic page. All signal inputs show the source of the signal by the Board number. All signal outputs also show the Board number destination of the signal. Signals originating from a function block are referenced as arrows pointing outward from the block while signal inputs are arrows pointing into the block.

The three Block Diagrams show the bus architecture of the CIU. Internal organization of the CIU results in the following buses:

- Bus Out - B0Ø - B015 Routes data from IOP to CIU decode and storage elements.
- Bus In - BIØ - BI15 Routes data from CIU storage to IOP.
- Transmitter Bus - XØ - X15 Routes data from CIU storage to Supervisory and Serial Output transmitter. Routes data from CIU storage to Sense Register 1 & 2. Routes data from Sense Register 1, 2 & 3 to IOP via Bus In.
- Sense Register Bus - SRØ - SR15 Routes data from Sense Registers 1, 2, & 3 to CIU front panel LED drivers.
- Receiver Data Bus - RDØ - RD15, RC1, RC2, RWS and RDP Routes data from Reply receiver (DIU data) to CIU data storage and CIU error monitor logic.
- Data Out Bus - Internal data storage bus which ties transmitter data memory and receiver data memory to the Transmitter bus through the Data Storage Buffer.
- Time Bus - TMØ - TM15 Routes data from Time Receiver to Time Display storage.

3.2 INTERFACE SIGNALS

The CIU has four functional interface areas: 1) IOP, 2) DIU, 3) Serial Outputs and 4) Time Input. The following sections describe each interface area in detail.

3.2.1 IOP Interface

The IOP-CIU interface shown in Figure 3.2-1 consists of control lines, also referred to as "tag" lines, and data line. Signals originating from the IOP are designated as "OUT" lines, while signals originating in the CIU are designated "IN" lines.

BUS OUT/BUS IN

The data buses between the IOP and CIU are composed of two bytes. Each byte is a set of nine lines consisting of eight data lines and one parity. Information on the buses is arranged so that bit position 7 and 15 of the bus is the low-order bit within a byte. The highest-order bit within a byte is bit position 0 or 8. Byte 2 carries the least significant data of the bus word, address, and status information.

When a word transmitted over the interface consists of less than sixteen information bits, the bits are placed in the highest-numbered continguous bit positions of the bus. Any unused lines of the bus present logical zeros to the receiving end. The parity bit of any byte appears in the parity postion (P). Each half-word byte has odd parity.

A summary of the Byte and Bit positions for the IOP/CIU interface is shown on the following page.

Byte 1

0 1 2 3 4 5 6 7	P_1
BUS IN/OUT #1	
UNUSED	
UNUSED	

Byte 2

8 9 10 11 12 13 14 15	P_0
BUS IN/OUT #0	
CIU SERIAL OUT CONTROL / CIU ADDRESS	
0 0 0 / STATUS / 0	

OPERATIONAL OUT

This is an IOP control line used to enable the CIU interface. This line will rise to a logical one state when the IOP is communicating with CIU. During the "reset" sequence this line shall fall to a logical zero until Operational IN drops after which Operational Out will rise again to a logical one state.

OPERATIONAL IN

This line will be raised to a logical one level each time the CIU has logically connected to the IOP. The CIU will hold this line at a logical one level until an entire message sequence has been completed or until reset by the IOP.

ADDRESS OUT

This is a tag line used to alert the CIU that its address has been placed on Bus Out for decoding. The rise of this line is delayed long enough to insure that the address has been gated to Bus Out. Address Out will rise only when the Select Out/Hold Out, and the Select In and Operational In lines are at a logical zero level. Once both Address Out and Select Out are up, Address Out will stay up until either Select In or Operational In rise. Address Out cannot be up concurrently with any other outbound tag line.

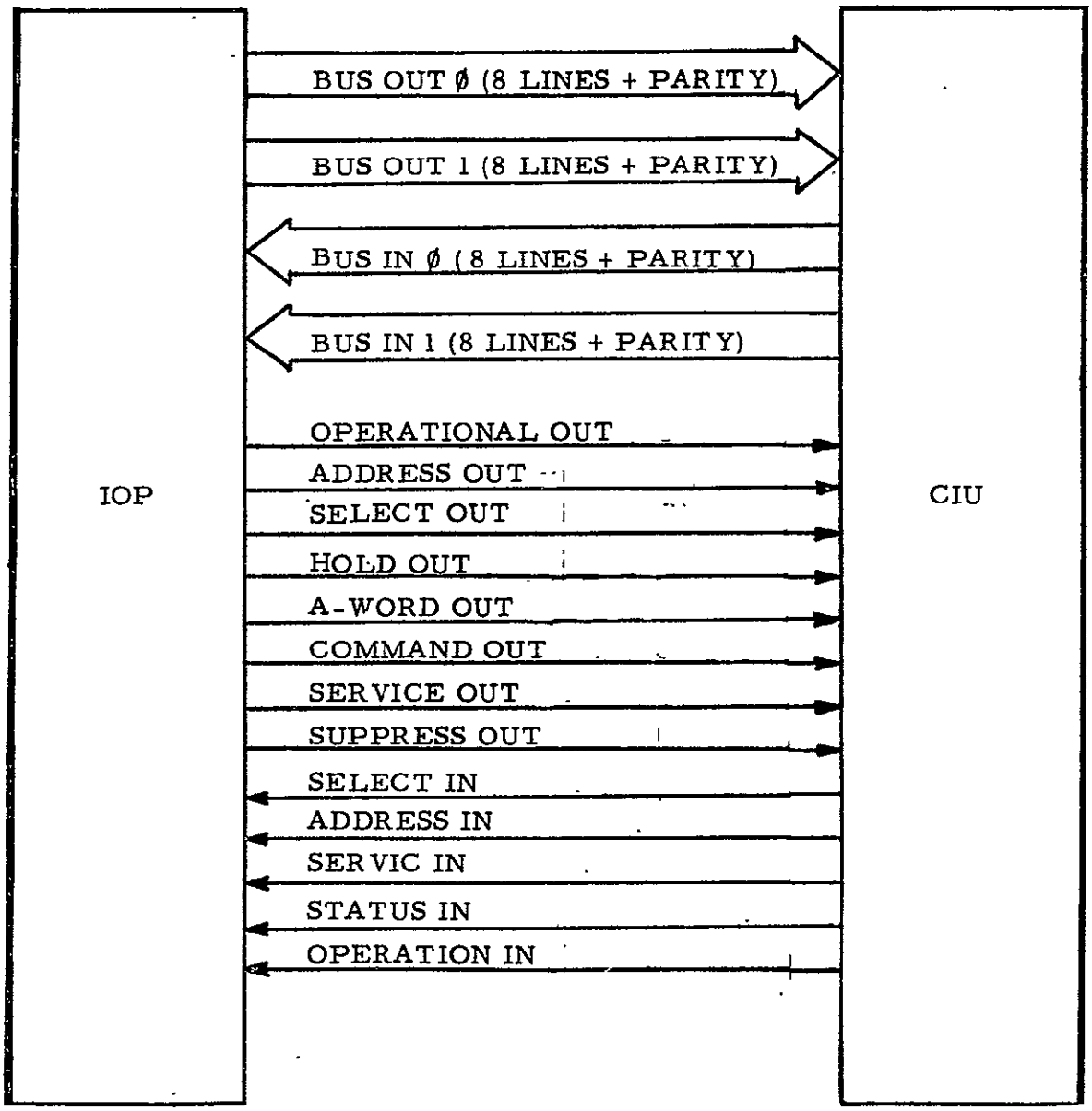


Figure 3.2-1

IOP-CIU INTERFACE

SELECT OUT/HOLD OUT

These are control lines used to interlock the CIU. These lines will rise after the rise of Address Out. The IOP shall hold these lines up until the rise of Select In, or Status In in the end sequence. Once these lines have fallen, they will remain in a logic zero state for a minimum of 4.0 usec.

The Select Out line is the one line that is propagated from one CIU to the next so that, together with Select In, it forms a loop.

When the first CIU in the chain recognizes that Address Out, Select Out and Hold Out are high it checks the address on the Bus Out lines. If the address is the one assigned to that CIU, it responds with Operational In, holding this line high until termination. If the address is incorrect or has a parity error the CIU will propagate the Select Out signal to the next, CIU. If the last CIU in the chain does not recognize its address or detects a parity error, it will return the Select In Signal and hold it high until the IOP initiates a disconnect. Once a CIU propagates Select Out, it cannot raise its Operational In or respond with a CIU-busy sequence until the next rise of the incoming Select Out. Each CIU must assure the propagation and continuity of the Select Out Signal. When a CIU is off-line or powered down it will pass the Select Out to the next CIU.

SELECT IN

This line is raised to a logical one level whenever the CIU fails to recognize its address as supplied by the IOP. This line will be raised instead of the Operational In tag line.

When the address is correct, the CIU keeps the Select In at a logical zero level.

ADDRESS IN

This line will be raised by the CIU in response to Address Out dropping. It will signify that the CIU Bus In has recognized that its address is correct, and has placed its address on the Bus In lines. If the return address agrees with the one sent and does not have a parity error the IOP shall raise A word out in response to Address In.

The Address In tag is dropped when the CIU accepts the A word.

A WORD OUT

This line will be raised to indicate that the 16 bit A-Word is on the Bus Out lines. It shall be delayed until the lines are stable. The A-Word Out tag line will be dropped in response to Address In dropping.

COMMAND OUT

Command Out is raised in response to Address in falling, this tag line is used to signal the CIU that the word count is on the Bus Out lines. This line will fall whenever Status In is raised. The rise of Status In in response to Command Out indicates the CIU has received the WC-Word.

The Command Out is also raised to a logical one in response to Service In when the IOP initiates an Ending Sequence. Command Out then falls when Service In falls.

STATUS IN

Status In is raised by the CIU when it has placed a status byte on Bus In. The IOP responds to an up level on this line by raising the Service Out tag line to a logical one level.

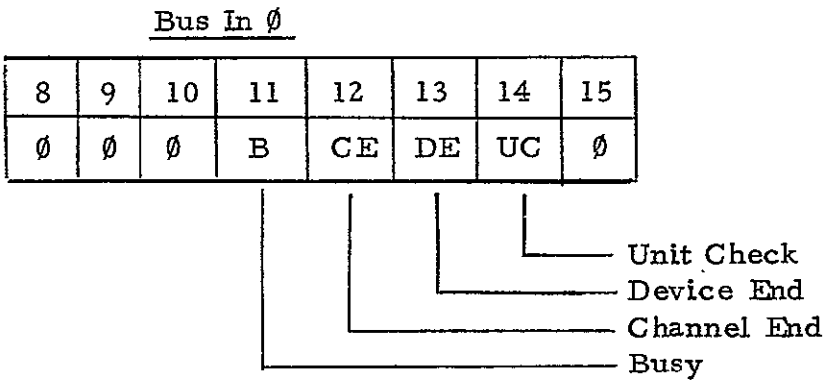
The following conditions are detected by the CIU and transferred to the IOP as the CIU Status Byte.

Busy indicates that the CIU is in use.

Channel End in conjunction with device end indicates that the CIU/Data Bus has completed an operation.

Device End in conjunction with channel end indicates that the CIU/Data bus has completed an operation. Channel end and device end are electrically tied together.

Unit Check indicates that the CIU or DIU has detected an error condition that can be detailed by additional information available to the IOP from the three Sense Registers.



SERVICE OUT

This line is used by the IOP to indicate to the CIU that it is ready to transmit or receive data. Service Out is raised to a logical one state in response to a logical one level on the Service In or Status In tag lines. When the IOP is transmitting data to the CIU, the rise of Service Out is delayed long enough

to insure that the data byte has been gated to Bus Out. When receiving data from the CIU the IOP will raise Service Out after it has gated the contents of Bus In into an internal register. Service Out will rise each time in response to Status In and will fall whenever Status In falls.

SERVICE IN

This line is raised by the CIU to indicate that it is ready to either transmit or receive a byte of data.

Writing is the transfer of data from the IOP to the CIU. After the CIU recognizes Service Out dropping in the initial selection sequenced it will raise Service In indicating it is ready to receive data. When the IOP has data on the Bus Out lines it will raise Service Out. The CIU will indicate it has accepted the data by dropping Service In. This will allow Service Out to drop. When the CIU is ready to accept the next data word it will again raise Service In and the sequence will be repeated.

Reading is the transfer of data from CIU to the IOP. After the CIU recognizes Service Out dropping in the initial selection it will raise Service In after data has been placed on the Bus In lines. The IOP will respond to Service In by accepting the data. If the parity is good the IOP will raise Service Out which will cause the CIU to drop Service In. The dropping of Service In will allow Service Out to drop. When the next data word is available at the CIU it will again raise Service In and the sequence will be repeated.

The IOP can end the sequence by raising Command Out in response to Service In.

SUPPRESS OUT

This line is used by the IOP to perform the chaining operation. When chaining has been indicated, Suppress Out will rise in response to a logical one on the Status In tag line during the ending sequence for the command which has indicated chaining. To insure chaining, Suppress Out must precede the rise of Service Out by a minimum of 250 nanoseconds. In both sequences Suppress Out will remain up until Operation In rises again.

3.2.2 CIU Test Set Interface

The Test Set interface is nearly identical to the IOP interface. The only differences are 1) the Test Set receivers are terminated internally on the PC board and 2) the Test Set interface lines can not be chained to another CIU. Selection of the operational interface is by the IOP/TEST FIXTURE switch on the CIU front panel.

3.2.3 DIU Interface

The CIU can interface with a maximum of 32 DIU's through a full duplex Data Bus. The bus operates at 2 MHz bit rate with word lengths of 20 bits/word. The two bus lines are designated "Supervisory" bus and "Reply" bus.

The Supervisory bus is a continuous biphase L (Manchester Type II) signal originating in the CIU. The Reply bus is a gated biphase L (Manchester Type II) signal generated by the commanded DIU. Word structures of both Supervisory and Reply bus formats is given in Figure 3.2-2. The Supervisory bus has six word structures--A word, WC word, WC word/EOM, Data word, Data word/EOM and Blank word. The Reply bus has five different word structures -- Sync word, Error Status word, Data word, Last Data word and Blank word.

	Word Sync	Bus Code Prefix	Information Bits			Parity
	W_S	C_1 C_2	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15			P
	SUPERVISORY BUS					
A Word	1	1 1	DIU Address	Op Code	Channel Address	P
WC Word	1	1 1	Word Count			
WC Word (End of Message)	1	0 1	Word Count			P
Data Word	1	1 0	Byte #1	Byte #2		P
Data Word (End of Message)	1	0 1	Byte #1	Byte #2		P
Blank	1	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			0
	Reply Bus					
Sync Word	No Signal		1 1 1 1 0 1	Wired DIU Address		P *
Error Status Word	1	1 1	Error Status Bits			
Data Word	1	1 0	Byte #1	Byte #2		P
	1	0 1	Byte #1	Byte #2		P
Blank	1	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			0

*Parity on Wired DIU Address Only

DIU-CIU BUS FORMATS

Figure 3.2-2

A data bus word is twenty bits (20) in length. The first bit is word sync (WS) and shall always be a 1 unless deliberately set to a 0 by the CIU to cause a word sync error. The second and third bits are Bus Code Prefix Bits (C_1 C_2) and are used to define types of bus words. The next sixteen bits are information (Data) bits. The last bit of each word is the odd parity bit to make the number of ones in the twenty bit word odd, except for the Reply Sync word in which case odd parity is generated only on the five DIU address bits.

A-WORD

The A-word contains all command information for the addressed DIU and is always the first word of a message.

C_1, C_2: A 11 code in the first message word defines the A-word.

0 - 4: The DIU address field, defines which of the possible 32 DIU's is to receive the message.

5 - 9: The Operation Code field defines the command to be executed by the DIU.

10 - 15: The channel address field defines the starting INPUT/OUTPUT channel to be acted upon.

WC-WORD

The WC-word contains all count information for the addressed DIU and sub-system, and is always the second word of every message.

C_1, C_2: A 11 code in the second message word defines a WC-word with more words to follow. A 01 code defines the WC-word as the last word of the message.

Bits 0 - 15: The word count field defines the number of words to be transferred during a bus operation. A word count of zero defines an unlimited number of words for that particular sequence.

DATA WORD

Each Data word contains two 8-bit bytes of data. A data word may have either of two prefix codes. A 10 code a Data word. A 01 code identifies the Data word as last Data word in the message. The data field is defined as Byte #1 the most significant half of the data.

BLANK WORD

The Blank word contains only sync information and is used to maintain message continuity. Blank words are allowed to exist within a message after the WC-word and the Sync Word. Over six continuous blank words within a message is an error which is flaged in the error monitor circuity of the CIU DIU.

C_1, C_2: A 00 code defines a Blank word.

0 - P: Zeros for clocking.

SYNC WORD

The Sync word is transmitted by the addressed DIU as soon as it detects its A-word address on the supervisory line.

WS - 4: No signal

5 - 10: Reply message sync pattern 111101.

11 - 15: Hard wired address of the replying DIU.

P: Odd parity for the 5-bit address field only.

ERROR STATUS WORD

The Error Status word contains information concerning errors detected by the DIU and subsystem. The Error Status word is always the last word transmitted by the responding DIU and shall terminate a reply.

C_1, C_2: A 11 prefix code on the reply line signifies an error status word.

0 - 15: Error bits.

3.2.4 Time Message Interface

The CIU has an input to receive three time words from the Control and Display System. The three time words are transmitted as a 2 MHZ biphase signal once every millisecond. Blank words are transmitted between time words to maintain a continuous biphase signal. The time words data bus format is shown below:

	W_s	C_1	C_2	Byte 1 Byte 2	Parity
Time 1	1	1	1	Days - Hours	P
Time 2	1	1	0	Hours - Minutes - Seconds	P
Time 3	1	0	1	Milliseconds	P

The time words will be coded in BCD and arranged as shown below:

Data Field																
Word	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Time 1	Days X 10^2				Days X 10^1				Days X 10^0				Hrs X 10^1		Hrs X 10^0	
	8	4	2	1	8	4	2	1	8	4	2	1	2	1	8	4
Time 2	Hrs X 10^0		Min X 10^1			Min X 10^0			Sec X 10^1				Sec X 10^0			
	2	1	4	2	1	8	4	2	1	4	2	1	8	4	2	1
Time 3	Not Used				MS X 10^2				MS X 10^1				MS X 10^0			
					8	4	2	1	8	4	2	1	8	4	2	1

The CIU checks the three time words for parity and sync errors and provides a dc isolated discrete output to the control and display system to indicate detected errors. A +5 volt output indicates no errors and a 0 volt output indicates that parity or sync errors are being detected. Time word errors are also indicated on the CIU front panel with a light.

The CIU displays Days, Hours, Minutes, and Seconds on the front panel in the decimal format shown.

Days		HRS		Min		SEC
99	:	23		59	:	59

3.2.5 Serial Outputs

The CIU has four serial output channels to allow external access to any bus transmission. The output channels are individually selectable by the IOP. The CIU add word sent by the IOP during an initial selection sequence is used to select the output(s). Four bits are used to select any of the four outs. A fifth bit (Bit 8) is used to conditionally enable the selected serial channels. In a read operation the fifth bit enables the serial channel if data returns on the reply line or if an error is detected. In a write operation the fifth bit enables the serial channel only when an error is detected. In the write operation only the A-word, WC word and the three Sense Register words are transmitted on the Serial Out Channels. The format of the control bits for the Serial Output are given below:

CIU Serial Output Selection Word (CIU Address Out)

BUS OUT

8	9	10	11	12	13	14	15
Only if Data or Error	Select Out #4	Select Out #3	Select Out #2	Select Out #1	CIU Address		

Each of the Serial Output channels has two bus outputs -- Serial Data and Serial Time. Both bus outputs are continuous biphase L (Manchester Type II) signals at a 2 MHZ bit rate. Blank words are maintained on all outputs during non-transmission time irregardless of control enable bits. The Serial Output words use the same twenty bit format as the Supervisory bus. In addition to transmitting data, the Serial Output data bus transmits the Sense Register words after the last data word whenever this Unit Check bit has been set. The formats of both the DATA and TIME Output bus lines are shown below.

CIU SERIAL OUTPUT CHANNEL

DATA OUTPUT					TIME OUTPUT				
Ws	C_1	C_2	Byte 1 Byte 2	Parity	Ws	C_1	C_2	Byte 1 Byte 2	Parity
1	0	0	Blanks Blanks	0	1	0	0	Blanks Blanks	0
1	1	1	A-Word	P	1	1	1	Time #1	P
1	1	1	WC-Word	P	1	1	0	Time #2	P
1	1	0	Data	P	1	0	1	Time #3	P
1	1	0	Data	P	1	0	0	Blanks	0
1	0	1	Last Data Word	P				Blanks	
1	1	1	CIU Sense Reg # 1	P				Blanks	
1	1	0	CIU Sense Reg # 2	P				Blanks	
1	0	1	CIU Sense Reg # 3	P				Blanks	
1	0	0	Blanks	0				Blanks	

*** Send only if error(s) (Unit Check Bit Set) a blank word must follow Last Data Word if no error.**

3.3 INTERFACE SEQUENCES

The CIU interface sequences are grouped into three basic areas - 1) IOP interface 2) DIU interface and 3) Serial interface.

3.3.1 IOP - CIU Sequences

The IOP CIU interface sequences are listed below:

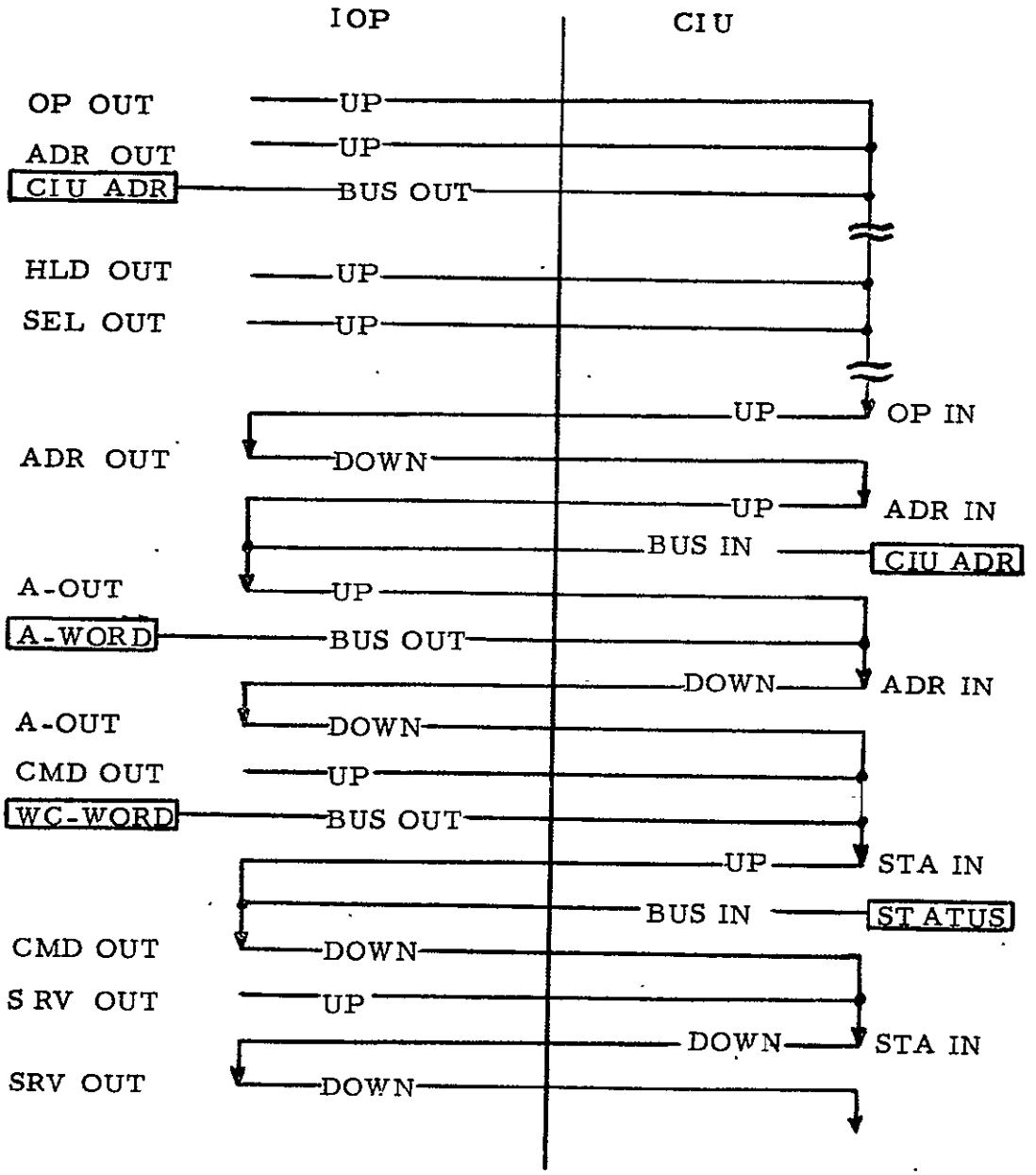
- Initial Selection Sequence
- Busy Sequence
- Read Sequence
- Write Sequence
- CIU Self-Test Sequence
- Ending Sequence
- Immediate End Sequence
- CIU Reset Sequence
- Interface Disconnect Sequence

The sequence action can be grouped into two general functions - 1) Action to initialize or test the CIU and 2) Action to transfer data through the CIU. A brief description of sequence operation is given in the following paragraphs.

INITIAL SELECTION SEQUENCE

The Initial Selection Sequence is initiated by the IOP each time it communicates with the CIU. This sequence is utilized to connect the CIU to the IOP and provide status data to the IOP indicating the readiness of the CIU to execute the command operation (Figure 3.3-1).

The Initial Selection Sequence requires the following steps:



INITIAL SELECTION SEQUENCE

FIGURE 3.3-1

1. The IOP raises OP OUT and ADR OUT tags, and simultaneously, places the CIU Address on the BUS OUT.

2. The IOP raises SEL OUT and HLD OUT.

3. The CIU checks for correct parity and address code. After validation of a correct address the CIU raises the OP IN tag.

4. The IOP drops ADR OUT tag.

5. The CIU raises the ADR IN tag, and, simultaneously, places the I/O address code on BUS IN.

6. The IOP places an A-word on the BUS OUT and raises A-word Out.

7. The CIU receives, processes the A-word, and drops the ADR IN tag line.

8. The IOP drops A-word Out tag.

9. The IOP places a bus word count on the BUS OUT and raises CMD OUT.

10. The CIU receives and processes the bus word count, places a status word on BUS IN and raises STA IN.

11. The IOP drops CMD OUT and raises SRV OUT.

12. The CIU drops STA IN.

13. The IOP drops SRV OUT. At this time, the initial selection sequence ends; the commands have been decoded and checked for validity, and the OP IN tag remains up to allow further exchanges with the IOP. In this condition, CIU interface control proceeds with a service cycle sequence if the decoded command entails data transfers; it proceeds with an ending sequence if no data transfers are involved.

BUSY SEQUENCE

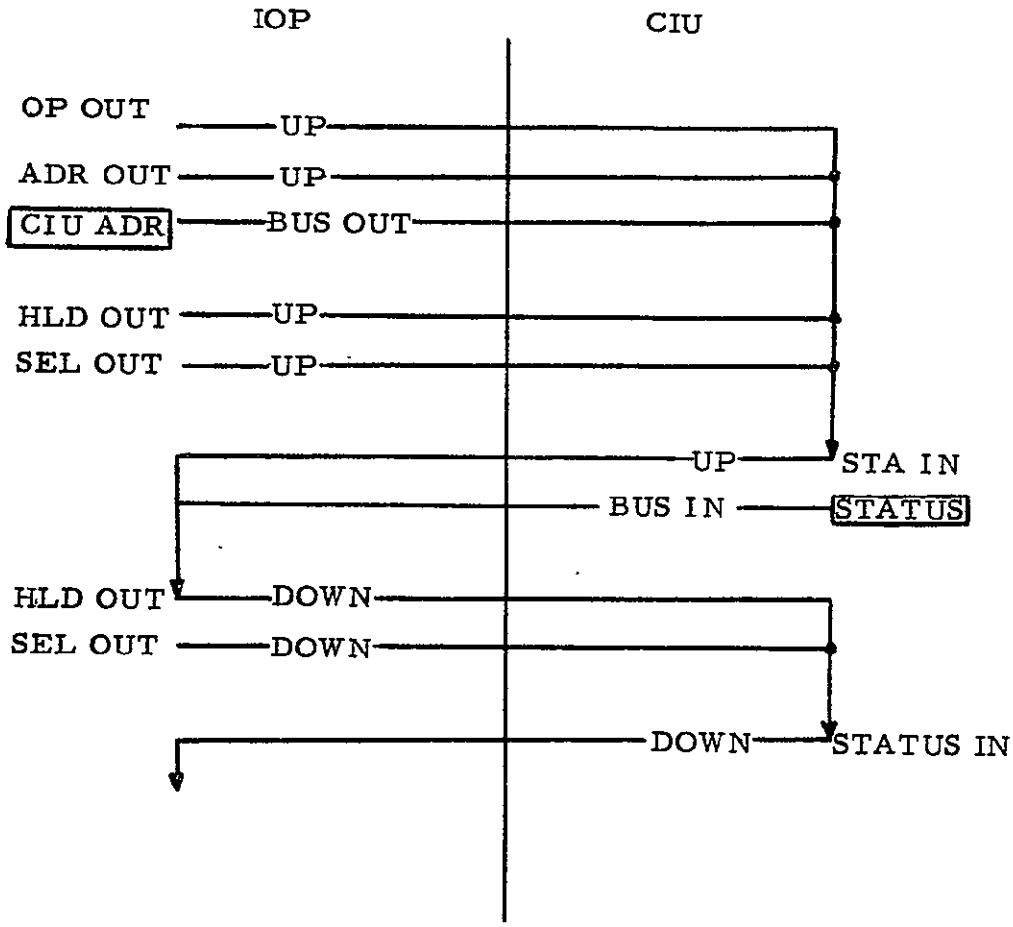
If the IOP tries to perform an Initial Selection Sequence with a busy CIU, the previous sequences shall be abbreviated. The CIU shall raise Status In with appropriate status information on Bus In instead of Operational In. The A-word and word count shall not be transferred from the IOP to the CIU. The Busy Sequence is diagrammed in Figure 3.3-2. The Busy Sequence requires the following steps:

1. The IOP raises OP OUT and ADR OUT tag, and simultaneously, places the CIU Address on the BUS OUT.
2. The IOP raises SEL OUT and HLD OUT.
3. The CIU checks for correct parity and address codes. After validation of a correct address the CIU raises the STA IN tag, and simultaneously places the Status word on the BUS IN.
4. The IOP drops the SEL OUT and HLD OUT tag.
5. The CIU drops the STA IN tag.

There are two basic service sequences whereby data is transferred through the CIU. The two service sequences are Read Sequence and Write Sequence.

READ SEQUENCE

The Read Sequence is the method of transferring data from the DIU's through the CIU to the IOP. This sequence is differentiated into fixed word length operations and variable word length operations. The fixed word length sequence contains as many service cycles as required by the command. Sequence end is determined by CIU interface control when, instead of SRV IN, it places the status word on Bus In and raises STA IN. The status word contains the channel end and device end bits which indicate an ending sequence.



BUSY SEQUENCE

FIGURE 3.3-2

The variable length sequence is similar to the one above except the IOP initiated the ending. For each service cycle. the CIU puts data on Bus In and raises SRV IN. The IOP accepts the data by raising SRV OUT. This sequence prevails until the IOP reaches its predetermined count. The next time SRV IN is raised, the IOP responds by raising CMD Out with an all zero data word on Bus Out 0 and 1. The ending sequence then follows.

A diagram of the Read Sequence is shown in Figure 3.3-3.

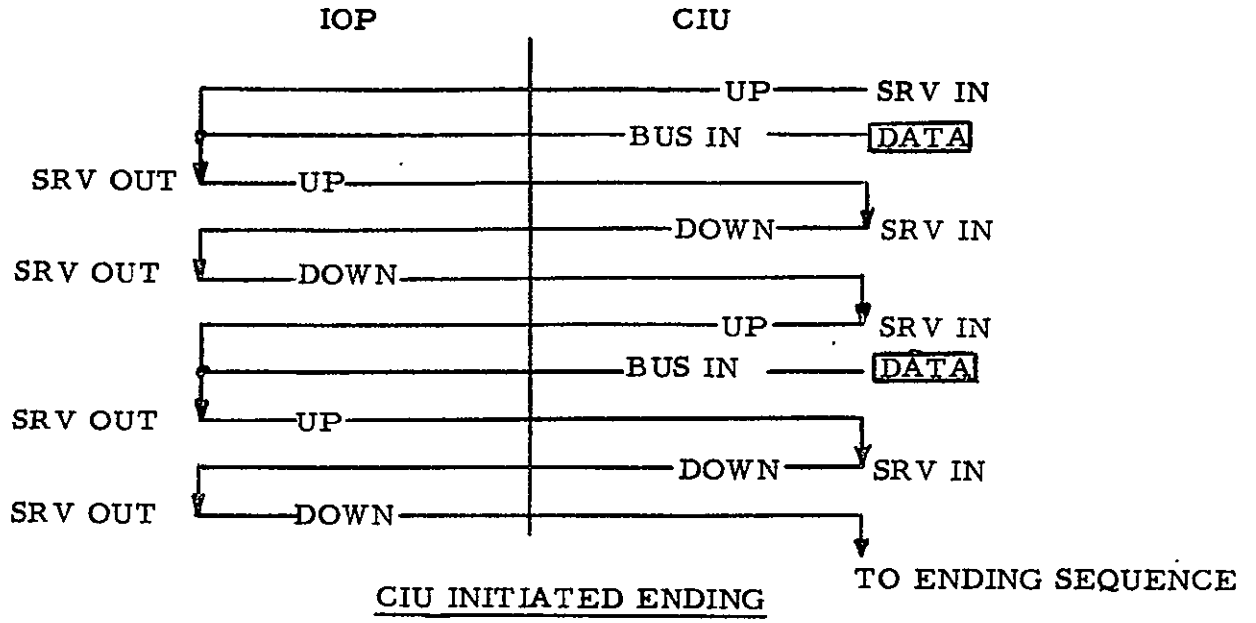
WRITE SEQUENCE

The Write Sequence is the method of transferring data from the IOP through the CIU to the DIU or Serial Outputs. This sequence , like the Read Sequence, is differentiated into fixed word length operations and variable word length operations.

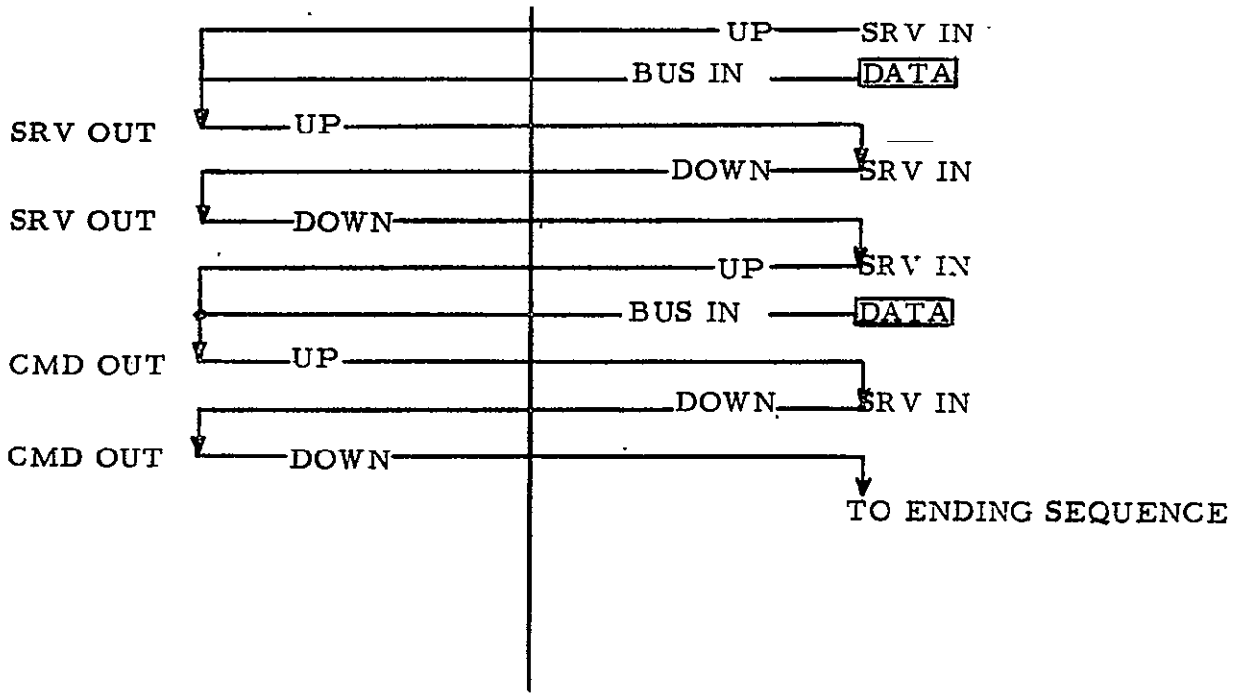
When the initial selection is complete, the CIU raises SRV In to request a bus word from the IOP. The IOP in turn places a bus word of data on Bus Out and raises SRV Out. Next, SRV In drops, then SRV Out drops to complete the first service cycle. Other service cycles in the sequence follow the same procedure.

The fixed word length sequence contains as many service cycles as required by the command. When the last bus word associated with the command is received, the CIU places the status word containing Channel End and Device End on BUS In and raises STA In instead of SRV In.

The variable length write sequence is similar to the one above. For each SRV In, the IOP follows with data on Bus Out and SRV Out up. This sequence continues until the IOP reaches the predetermined word count, at which time it responds



CIU INITIATED ENDING



IOP INITIATED ENDING

READ SEQUENCES

FIGURE 3.3-3

to SRV In by raising CMD Out. The presence of SRV In and CMD Out coincidentally raised initiates the ending sequence.

The two Write Sequences are diagrammed in Figure 3.3-4.

When the CIU detects an error during a service sequence, it will end the operation by placing a status word on Bus In and raising the Status In tag line in place of SRV In. If the Data Bus is active at the time the error is detected the CIU will wait until the Data Bus operation is completed or force a DIU termination before presenting status to the IOP.

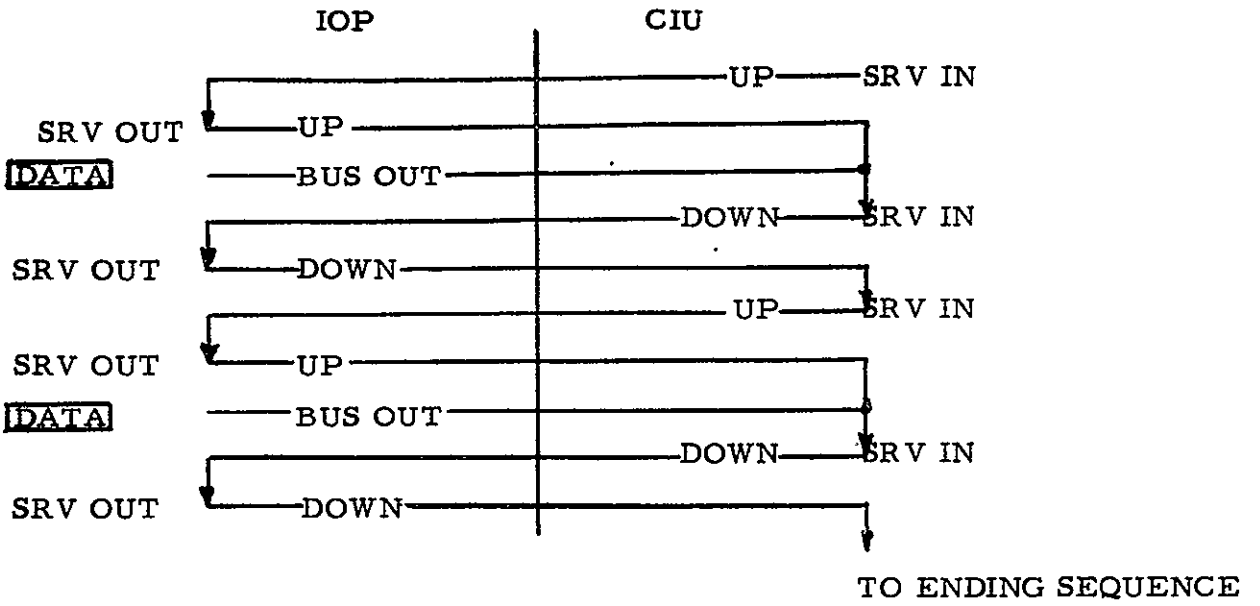
When the IOP detects an error during the Service sequence, it will end the transfer by raising CMD Out in place of SRV Out. When the Data Bus activity is completed the CIU will respond by placing its status on Bus In and raising the Status In tag line. Either of the above types of terminations will lead into a normal Ending Sequence as described below.

ENDING SEQUENCE

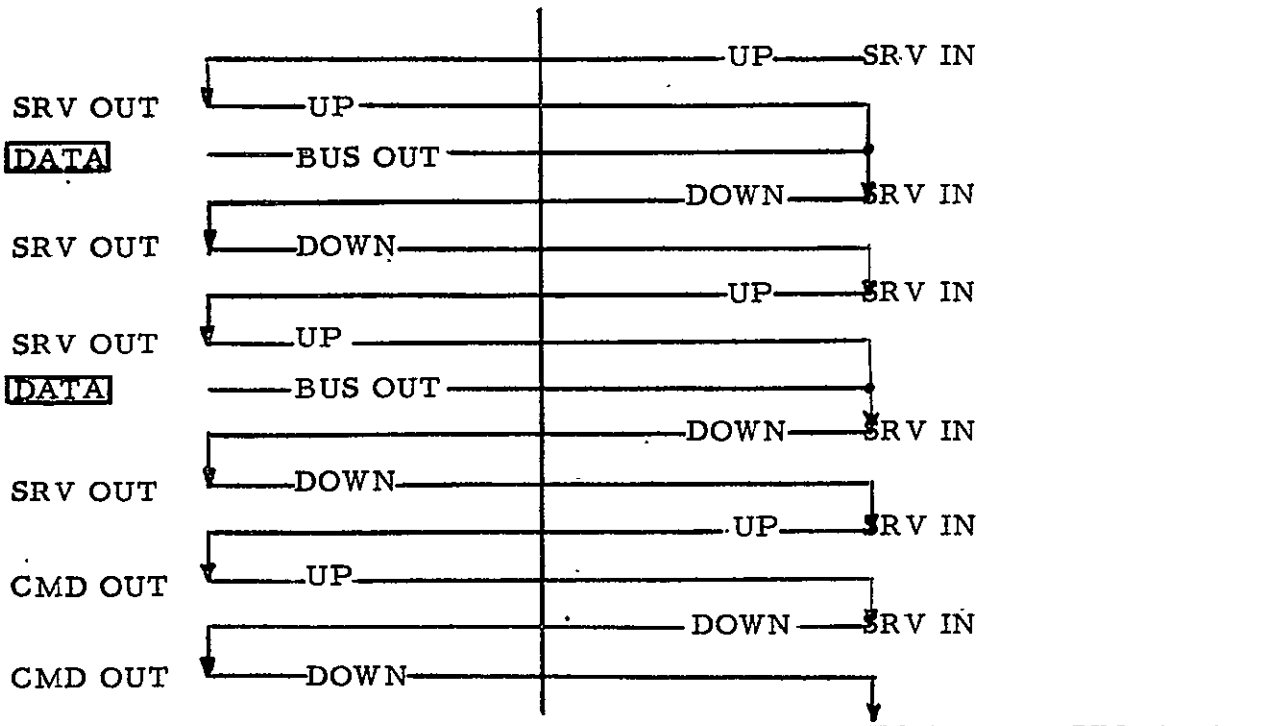
The Ending Sequence completes a command process. When processing a command requiring data transfer, the Read or Write sequence is normally followed by an Ending Sequence. The Ending Sequence has two objectives: to transfer a "sign-off" status word which contains channel end and device end; and to drop Op In, which allows the IOP to start the initial selection for a new command. This sequence can be initiated by either the IOP or the CIU as described above. The Ending Sequence diagram is shown in Figure 3.3-5.

CIU SELF-TEST SEQUENCES

Two IOP commands are used to perform a self test of the CIU. The commands are SENSE WRITE, OP Code 00101 and SENSE READ, OP Code 00110. These



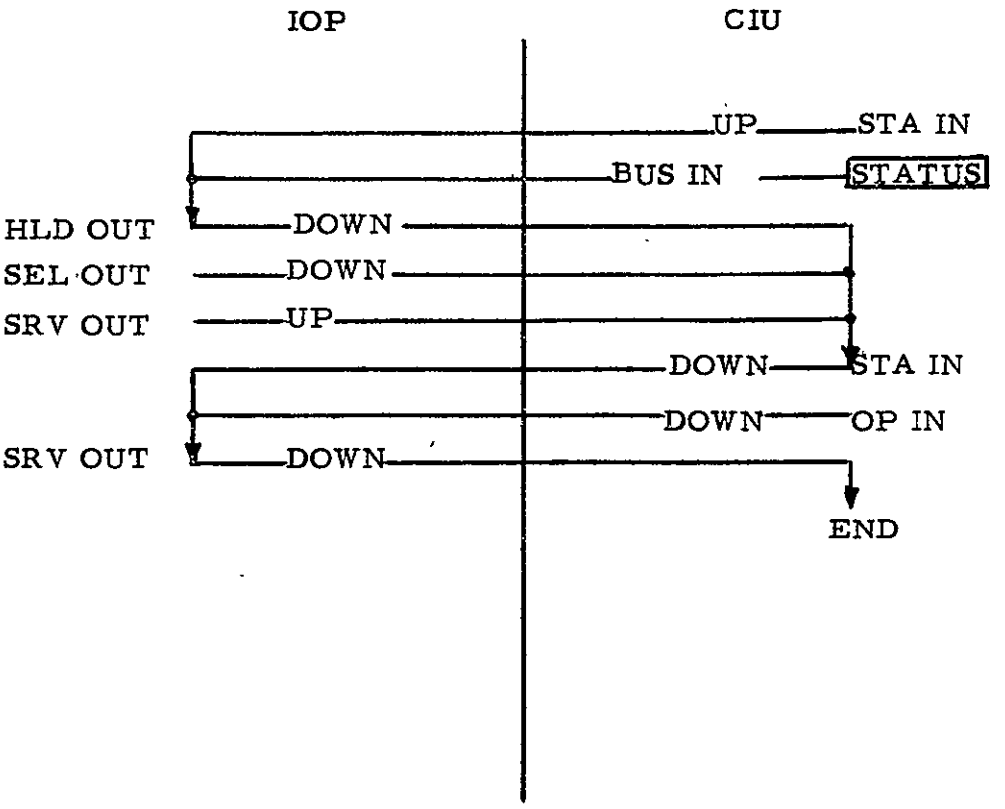
CIU INITIATED ENDING



IOP INITIATED ENDING

WRITE SEQUENCES

FIGURE 3.3-4



ENDING SEQUENCE

FIGURE 3.3.-5

commands are special conditions of the normal service sequences of READ and WRITE. Diagrams of both sequences are shown in Figure 3.3-6. Both sequences are initiated with normal Initial Selection Sequence and both are terminated by an Ending Sequence.

The SENSE WRITE Sequence allows the IOP to load a sixteen bit data word into Sense Registers 2 and 3.

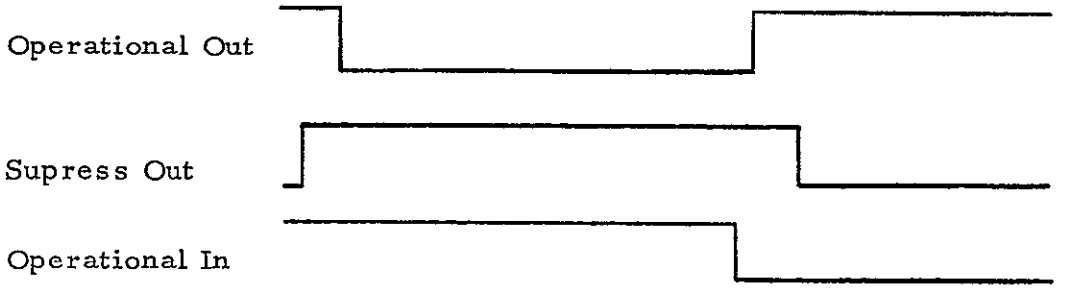
The SENSE READ Sequence allows the IOP to read the contents of Sense Registers 1, 2 and 3. The loop back action of the two commands permits the IOP to verify the interface circuitry. Another purpose of the self-test commands is to verify the CIU response to error conditions represented by the bits set in the Sense Registers.

IMMEDIATE END SEQUENCE

Another special purpose operation is the Immediate End Sequence, OP Code 00000. This command is used to test the condition of the CIU status register without modifying the contents of the sense and status registers. The sequence for this command is shown in Figure 3.3-7. The sequence is generated by combining an Initial Selection Sequence with an Ending Sequence.

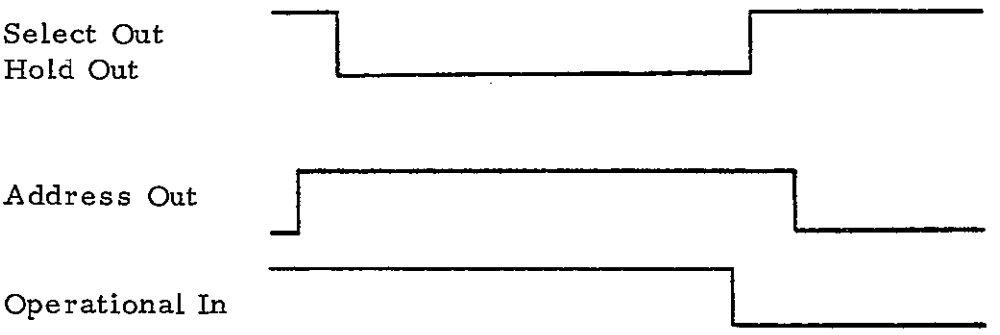
CIU RESET SEQUENCE

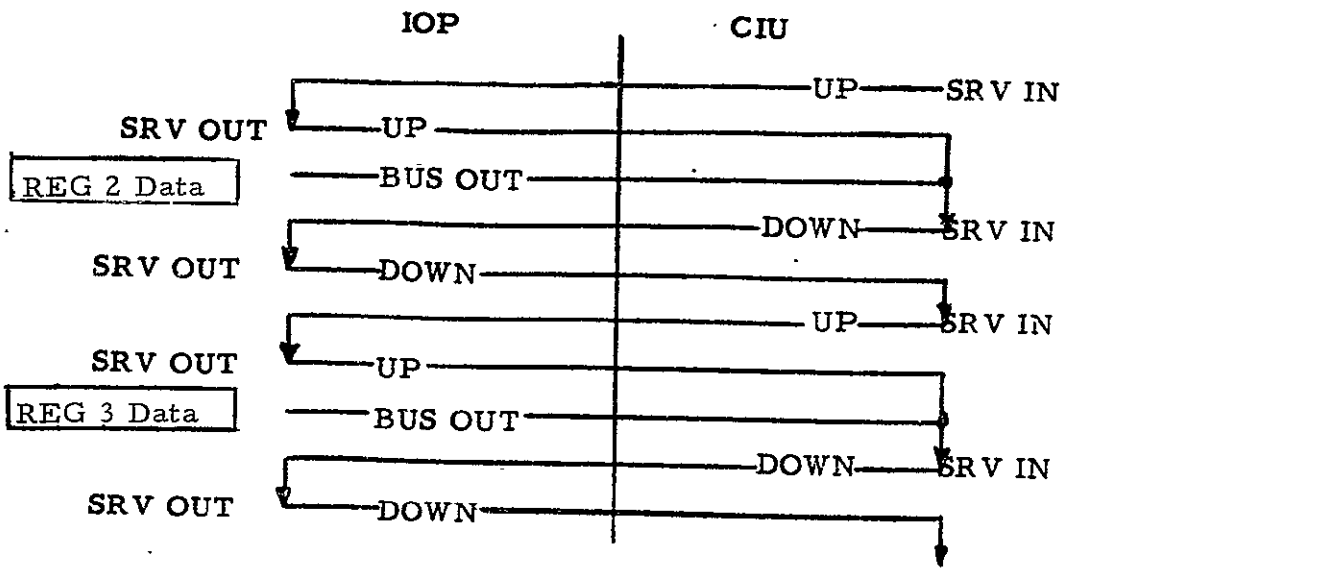
There are two CIU reset methods that are initiated by the IOP. The Master Reset sequence will reset all CIU's connected to the IOP interface. The Selective Reset will only reset the CIU which has an active interface with the IOP (a CIU which has OP In high). The Master Reset is performed by the IOP dropping OP Out. The Selective Reset is performed by the IOP raising SUP Out before dropping OP Out. The Selective Reset sequence is shown below:



INTERFACE DISCONNECT SEQUENCE

The last IOP-CIU sequence is the Interface Disconnect which is used to terminate the current CIU operation. The IOP will initiate a disconnect for a logically connected CIU by raising ADD Out and dropping SEL OUT/HLD OUT. The CIU responds to the Interface Disconnect Sequence by removing all signals from the IOP Interface and resetting the DIU's. The sequence is shown below:

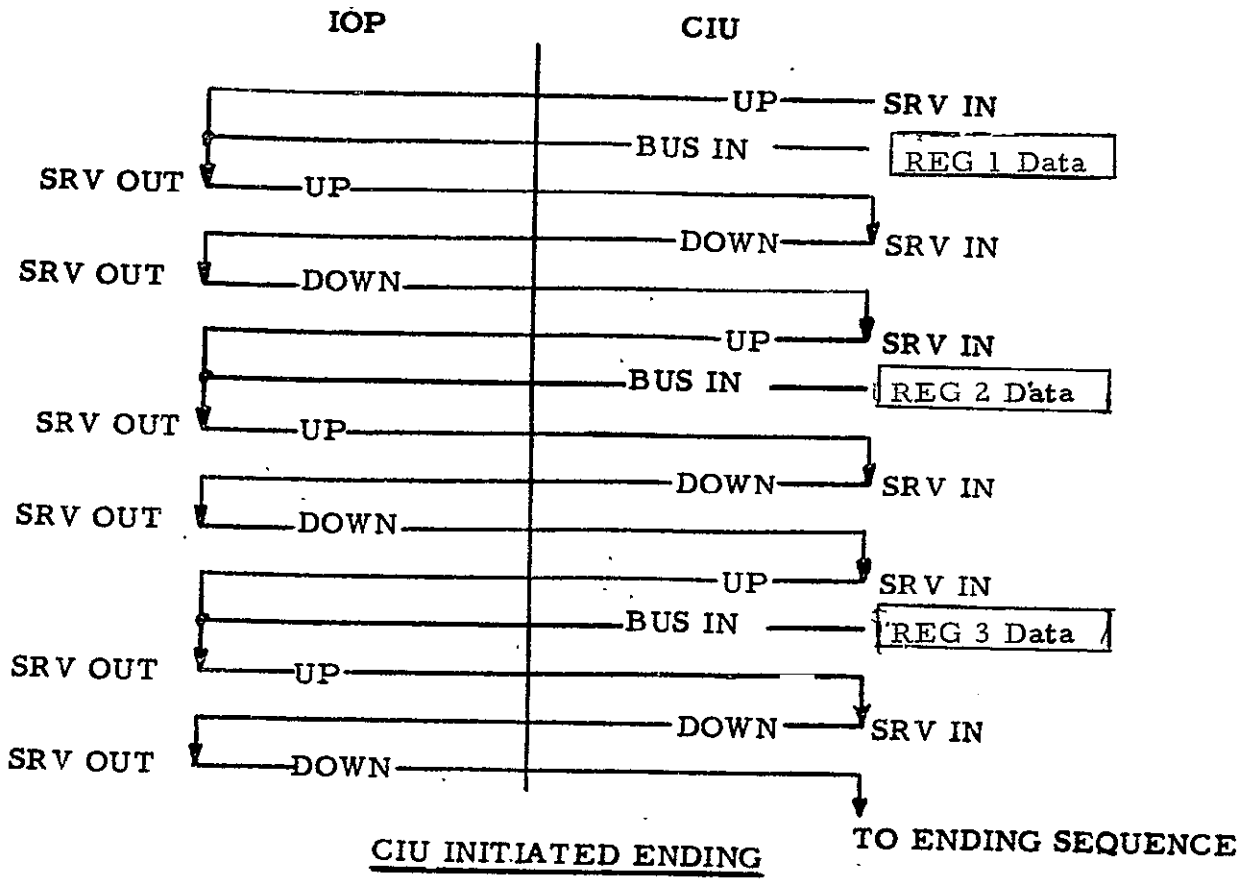




CIU INITIATED ENDING

SENSE WRITE SEQUENCE

OP CODE 00101

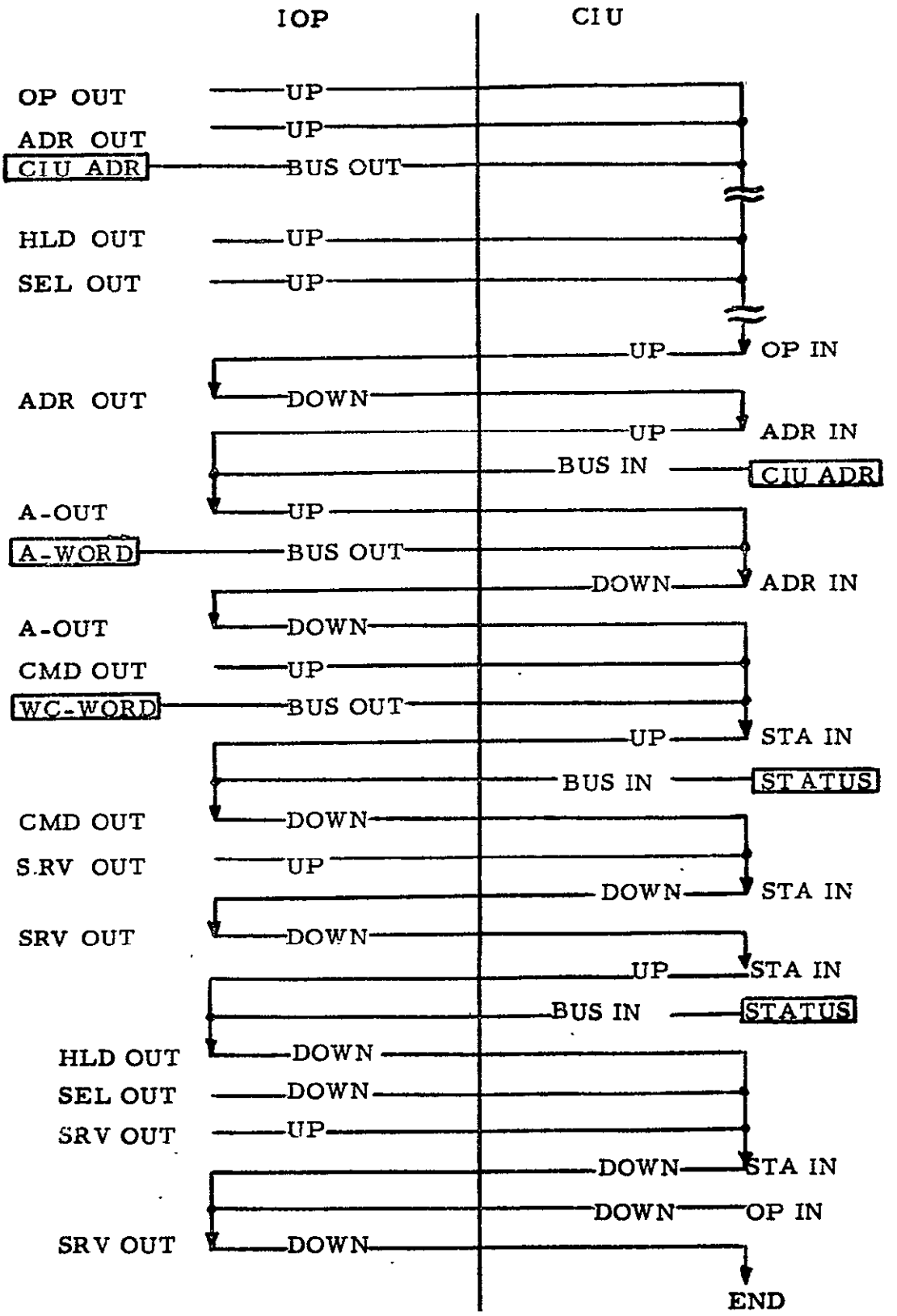


CIU INITIATED ENDING

SENSE READ SEQUENCE

OP CODE 00110

FIGURE 3.3-6



IMMEDIATE END SEQUENCE
OP CODE 00000

FIGURE 3.3-7

3.3.2 DIU-CIU Sequences

The DIU-CIU Sequences are specified by the OP Code field in the A-word. The Sequences can be grouped into the following types:

- Write
- Read
- Reset
- DIU - DIU Transfer

The CIU does not start a message transmission until the A and WC words are received correctly from the IOP. The CIU message then starts with the next available bus word slot. For each bus word the CIU adds the Word Sync-WS, the prefix code C1 and C2 and the proper parity bit. The CIU in all cases checks the replied sync word for the proper DIU address. If the address compares correctly the message is continued. In the case of an incorrect comparison the CIU forces incorrect parity on the WC-word and terminates the operation.

WRITE SEQUENCES

The Write Sequences consist of both fixed word length and variable word length transmission. The WRITE OP Codes are listed below:

FIXED WORD LENGTH

- Write DI Monitor Control - 10000 OP Code

The CIU transmits the A-word, WC word and Data word (Monitor Control Word) on the Supervisory Bus. The A-word and the WC word are combined with a 11 Prefix Code. The D-word is prefixed with a 01 code to define end of message. The DIU replies with a sync word, two Blank words and the Error Status word.

VARIABLE WORD LENGTH

- Write AO - 11110 OP Code
- Write AI Delta - 01101 and 11101 OP Codes
- Write RO - 00111 OP Code *
- Write DO - 11000 OP Code

The CIU starts its message with the A-word and the WC word prefixed with a 11 code and all but the last D-word prefixed with a 10 code. The WC-word defines the number of D-words. The CIU uses the word count to detect the last D-word and prefix it with a 01 code to define end of message. The DIU replies with a sync word and sufficient Blank words to continue the reply until the end message is detected on the supervisory line, and then terminates the transmission with the Error Status word.

* The Write RO reply contains two extra Blank words to permit the DIU additional time to develop the Error Status word.

The DIU-CIU sequence of operation for the Write Commands is shown in Figure 3.3-8.

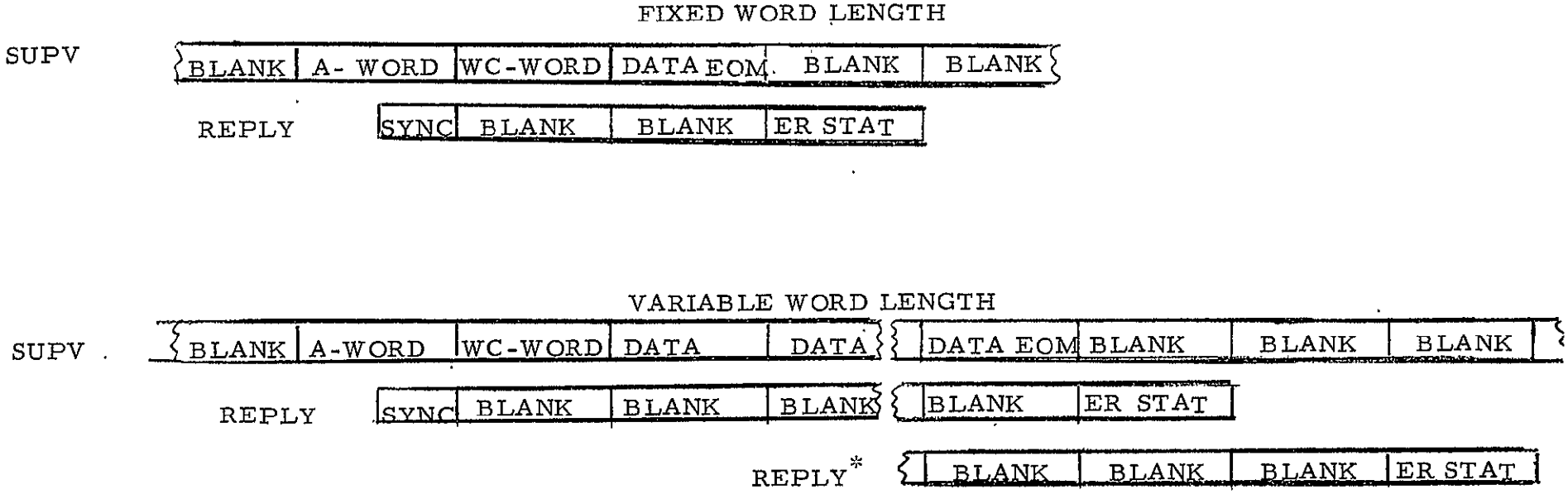
READ SEQUENCES

The Read Sequences consist of both fixed word length and variable word length transmissions. The READ OP Codes are listed below:

FIXED WORD LENGTH

- Read DI Monitor Control - 10011 OP Code
- Read Error Status - 01010

The CIU transmits the A-word and the WC word on the Supervisory Bus. The



* REPLY TO WRITE RO COMMAND

DIU - CIU WRITE SEQUENCE OPERATIONS

FIGURE 3.3-8

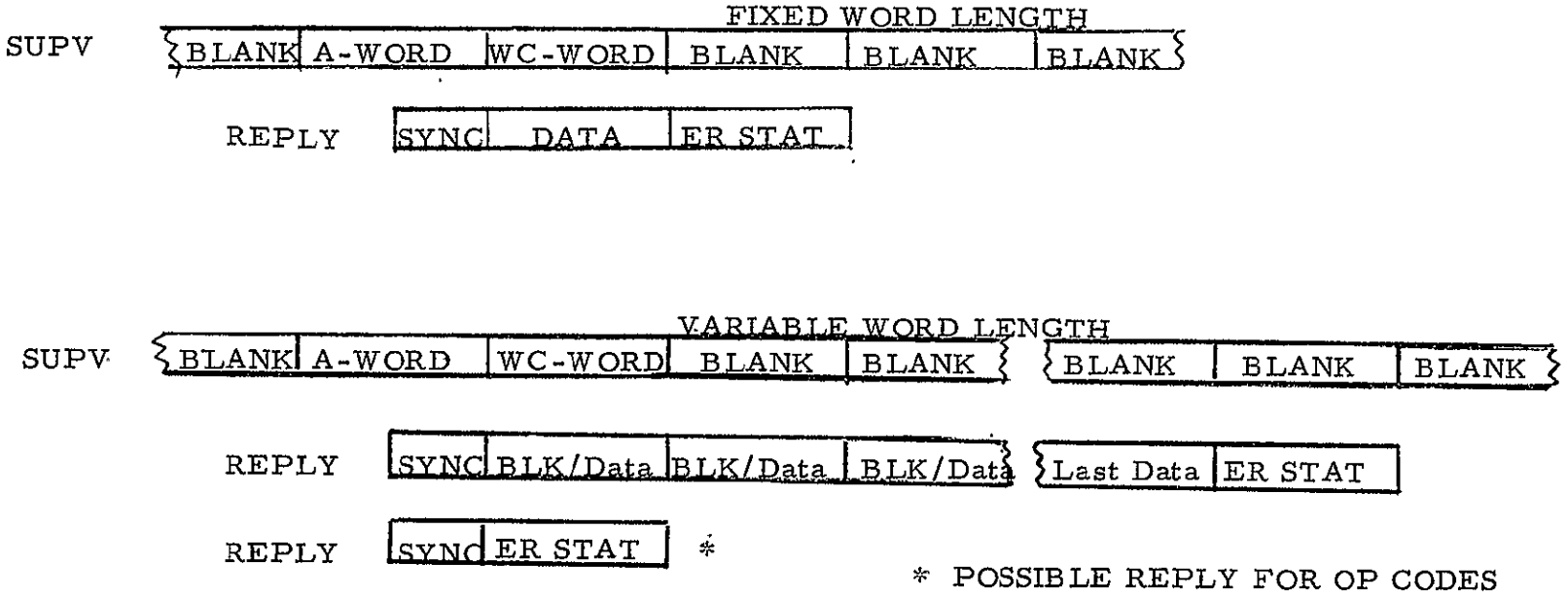
A-word is prefixed with a 11 code. The WC-word is prefixed with the end of message (EOM) code 01. The DIU replies with the Sync word, one Data word and the Error Status word.

VARIABLE WORD LENGTH

- Read DI - 10001 OP Code
- Read AI - 11010 OP Code
- Read RI - 00011 OP Code
- Read DO Status - 11001 OP Code
- Read AI Deltas - 01011 & 11011 OP Code
- Read DI Changes - 10010 OP Code
- Read AI Exceeding Deltas - 11100 OP Code

The CIU transmits the A-word and the WC word on the Supervisory Bus. The A-word is prefixed with a 11 code. The WC-word is prefixed with the end of message code 01. The DIU replies with a Sync word and either Blank or Data words. The number of Data words is determined by the WC-word code for all variable length Read Sequences except for the Read DI Changes and Read AI Exceeding Deltas commands. These two commands allow the DIU to reply with only the Data words necessary to identify the changes and exceeding limits of the two DIU interface areas. If there are no perturbations for these commands, the DIU responds with sync followed by the Error Status word. In all Read Sequences the DIU may terminate the reply with the Error Status word.

The DIU-CIU sequences of operation for the Read commands is shown in Figure 3.3-9.



* POSSIBLE REPLY FOR OP CODES

- o 10010
- o 11100

DIU-CIU READ SEQUENCE OPERATIONS

FIGURE 3.3-9

RESET SEQUENCE

The Reset Sequence is a fixed sequence transmission initiated with a 11111 OP Code. The CIU transmits an A-word and a WC-word to the DIU. The WC-word has the last word prefix 01.

The DIU replies with a Sync word, one Blank word and the Error Status word. The reset operational sequence is shown in Figure 3.3-10.

DIU - DIU SEQUENCE

The DIU to DIU transfer instruction is identified by OP Code 10101. The IOP initiates the Operation by sending the CIU an A-word (DIU to DIU OP Code), WC-word and a D-word. The CIU stores the D-word to be used later as the A-word (A_R) for the receiving DIU. As illustrated in Figure 3.3-10 the CIU sends out the A (A_R DIU-DIU) and WC words to the receiving DIU to set it up for the DIU to DIU transfer. The DIU replies with its error status word. The IOP then initiates a read operation by sending the CIU an A (As) and WC word for the sending DIU. The CIU sends the A and WC word for the sending DIU followed by the stored A-word (A_R) and the WC word for the receiving DIU. The D-words received from the sending DIU are sent out on the supervisory line by the CIU to the receiving DIU. The sending DIU completes its reply with its Error Status word. The CIU sends out the Last Data word and completes the operation. The receiving DIU does not reply.

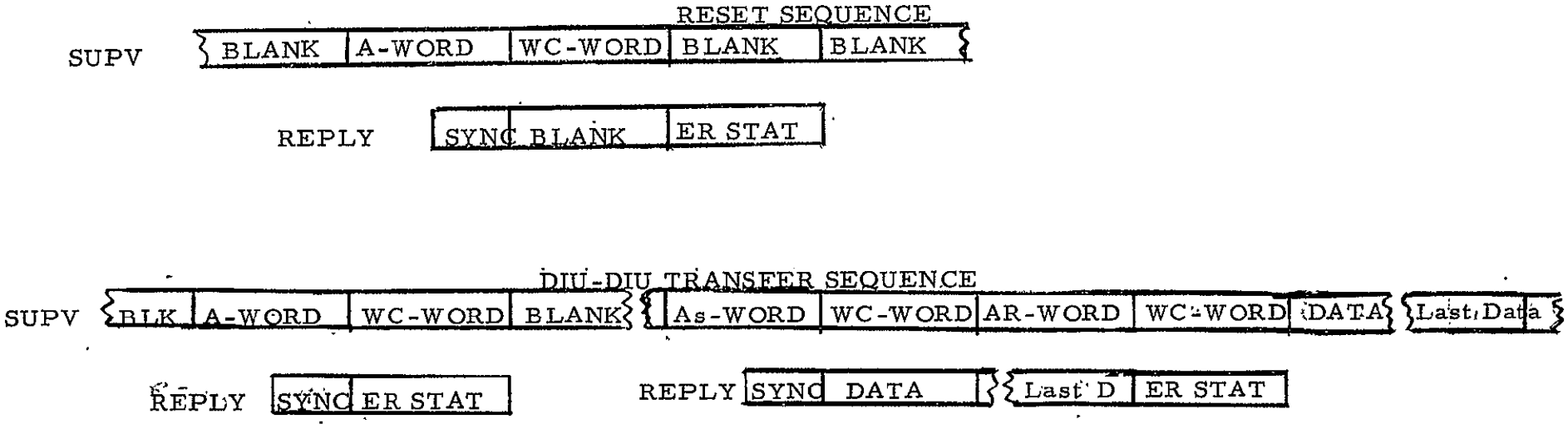

RESET SEQUENCE
SUPV
BLANK
A-WORD
WC-WORD
BLANK
BLANK
REPLY
SYNC
BLANK
ER STAT
DIU-DIU TRANSFER SEQUENCE
SUPV
BLK
A-WORD
WC-WORD
BLANK
As-WORD
WC-WORD
AR-WORD
WC-WORD
DATA
Last Data
REPLY
SYNC
ER STAT
REPLY
SYNC
DATA
Last D
ER STAT

FIGURE 3.3-10

3.3.3 Serial Output Sequences

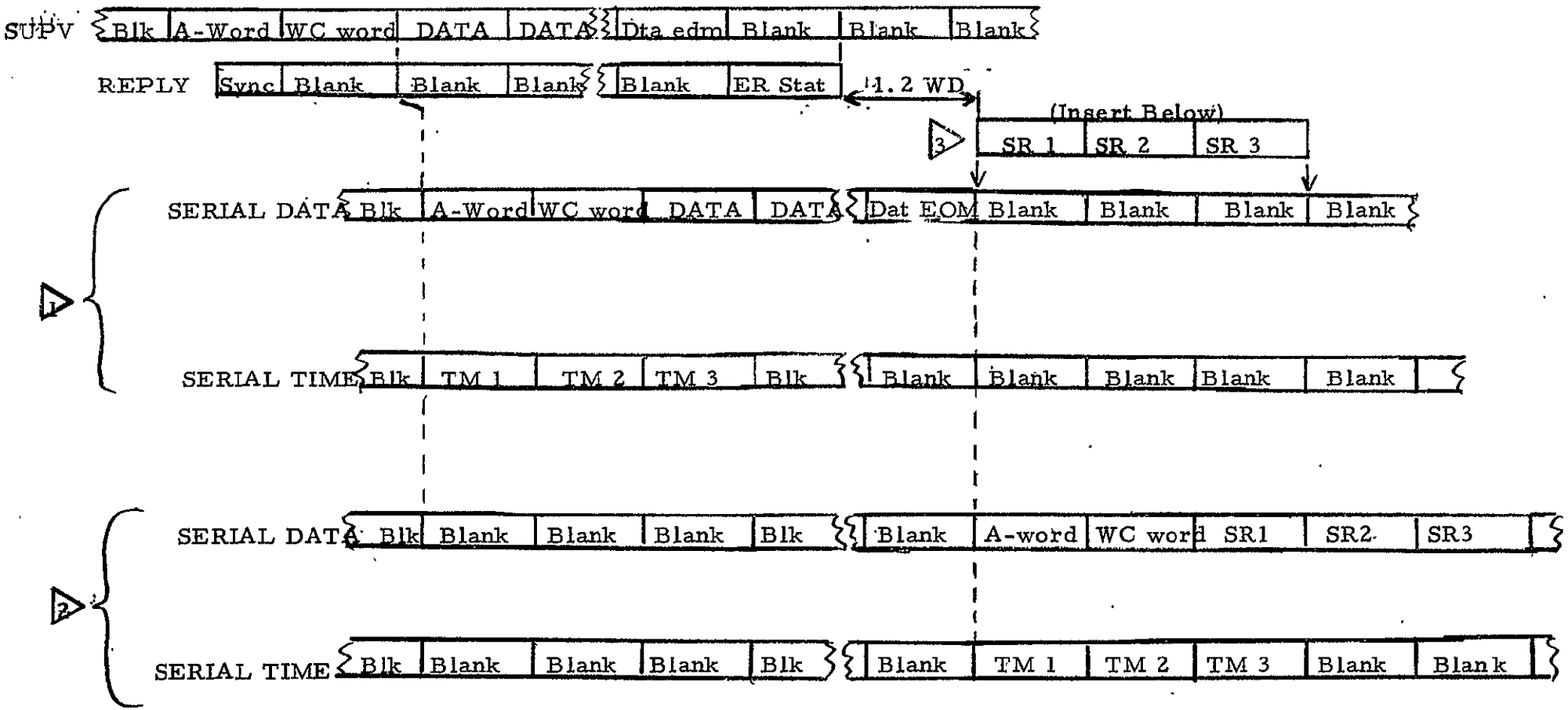
The Serial Output Sequences are basically the same as the DIU interface operations. The Serial Output signal contains the information content of both Supervisory Bus and Reply Bus signals. The CIU Sense Registers are also made available to the Serial Outputs along with a separate "Time" signal output. The Serial Output Sequences are divided into three basic operations.

- Write
- Read
- DIU-DIU Transfer

The CIU normally delays the start of a Serial Output sequence in excess of two bus word times from the start of the DIU interface sequence. There are three exceptions to this delayed operation: 1) DIU-DIU transfer in which the second message is transmitted during the same word time on both Serial Out Bus and Supervisory Bus; 2) A Write operation in which the fifth bit of the serial control code field has been set; and 3) the Serial Direct instruction (OP Code 00100) in which the Supervisory Bus is inactive with data only being transmitted on the Serial Out Bus. In the Serial Direct sequence data is transferred from the IOP to the Serial Output in the same manner of a variable length Write sequence.

SERIAL WRITE

The Serial Write operational sequences are shown in Figure 3.3-10. The Supervisory Bus and Reply Bus signals are shown as reference for the Serial Data and Serial Time Signals. For condition #1 (serial control bit not set) the Serial Data signal takes the identical form of the Supervisory Bus. At the transmission of the last Data word, the CIU will either transmit Blank words or insert the contents of the three Sense Registers on the bus. The Sense



1 SERIAL CONTROL BIT 8 NOT SET

2 SERIAL CONTROL BIT 8 SET & UNIT CHECK BIT SET

3 INSERTED WHEN UNIT CHECK BIT SET

SERIAL WRITE SEQUENCE
FIGURE 3.3-10

Register words are inserted if the CIU unit check bit is set, indicating an error condition in one or more of the Sense Registers. The CIU also transmits the three time words with Time Word 1 transmitted synchronous with the A-word.

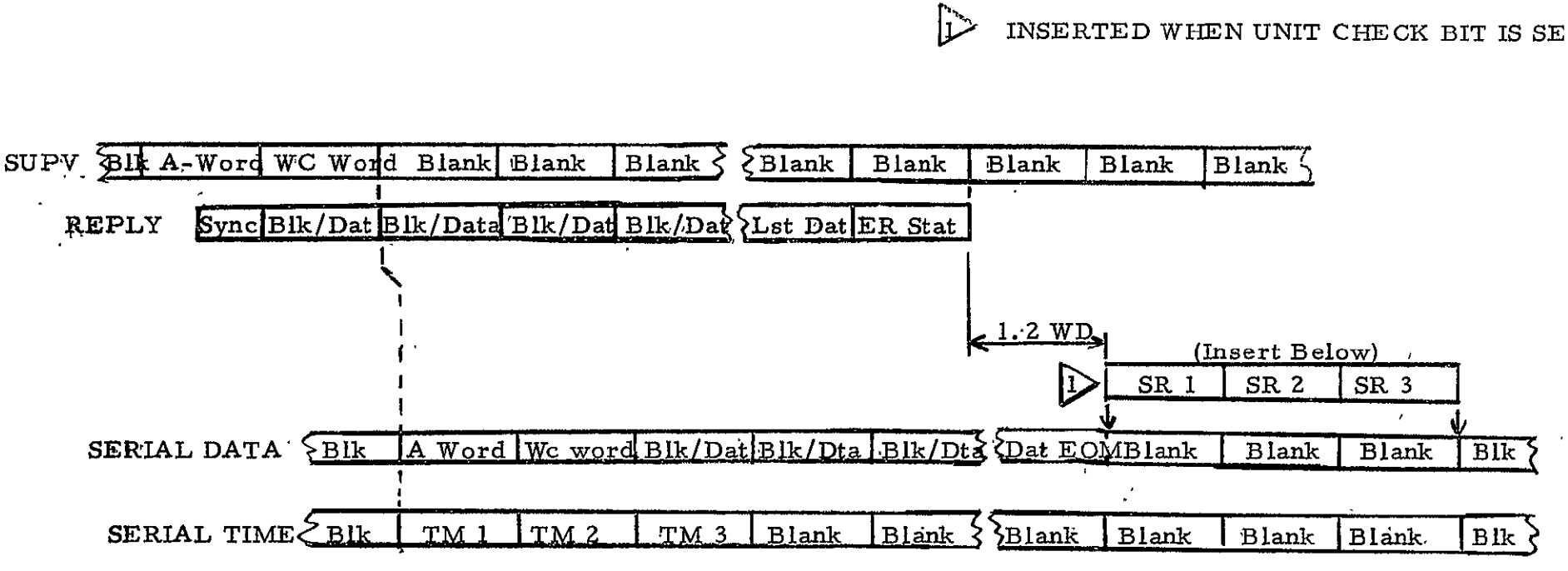
In condition #2 where the Serial Control bit 8 is set, the CIU will inhibit all Serial Bus transmissions unless the Unit check bit is set. When the Unit check bit has been set, the CIU will transmit the A-word and WC word followed by the three Sense Register words. The three Time words are also placed on the Time Bus.

SERIAL READ

The Serial Read operational sequence is shown in Figure 3.3-11. The Serial Data signal combines the A-word and WC-word of the Supervisory bus with the Blank/Data words of the Reply bus. The WC word of the Serial Data message is modified to have the 11 prefix code instead of 01 prefix code of the Supervisory bus WC word. Like the Serial Write sequence the Serial Data signal is followed by the three Sense Register words if the Unit check bit is set.

The three Time words are sent out on the Serial Time bus synchronous with the transmission of the A-word.

The Serial Data and Serial Time signals are not changed by the state of serial control bit 8 except for the two read sequences - Read DI changes and Read AI Exceeding Deltas. These two sequences may not result in reply data in which case the CIU will output only Blank words on the Serial Data and Serial Time buses.

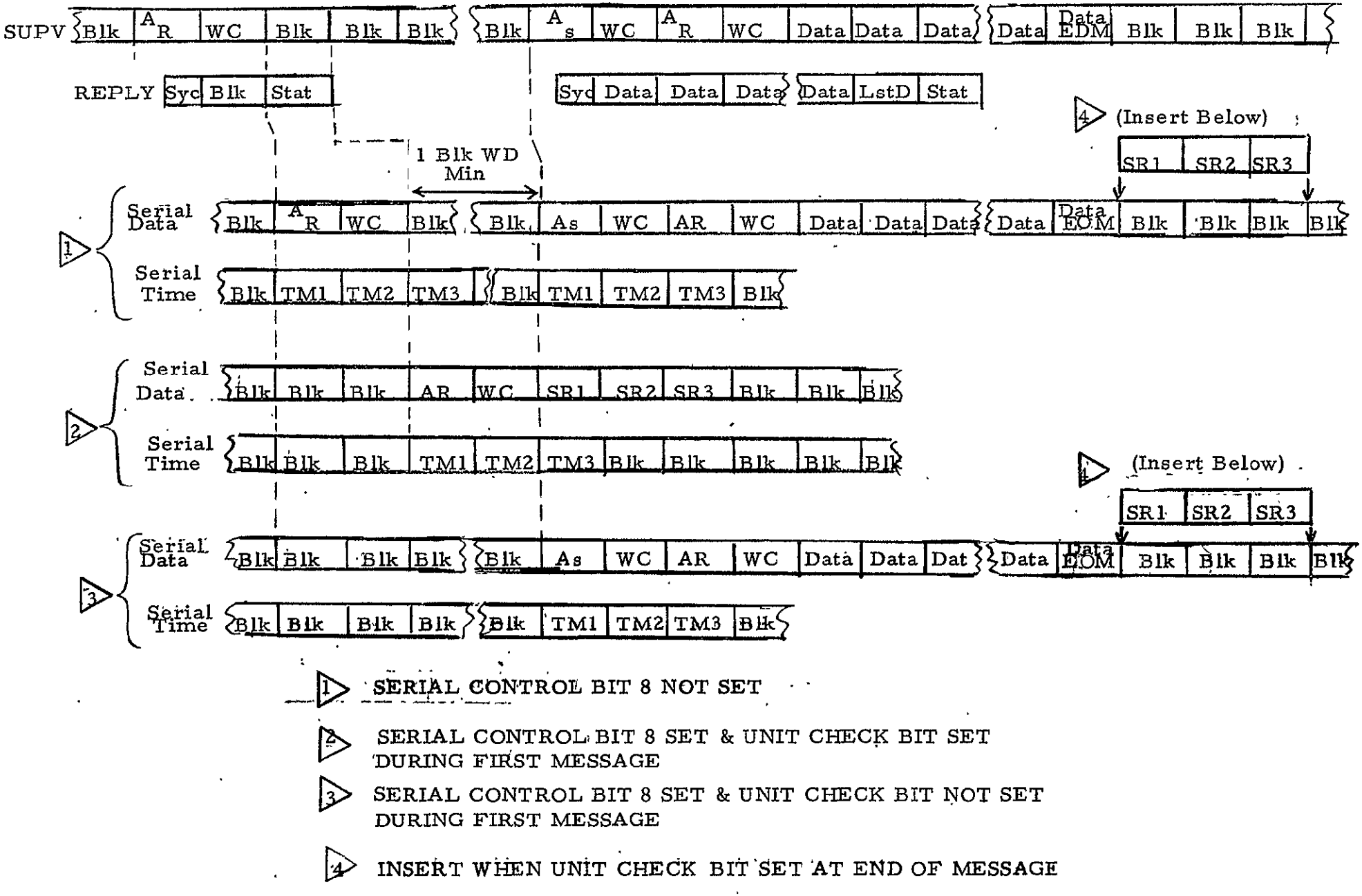


SERIAL READ SEQUENCE

FIGURE 3.3-11

SERIAL DIU- DIU TRANSFER

The Serial DIU-DIU Transfer sequences are shown in Figure 3.3-12. Three different sequence conditions are shown. In condition 1 serial control bit 8 is not set. The CIU outputs the composite signal of both Supervisory and Reply buses. If the Unit check bit is set at the end of the data message, the CIU terminates the message with the three Sense Register words. In condition 2 with serial control bit set during the first message, the CIU will output only the AR-word, WC-word and the three Sense Register words. Although not shown in Figure 3.3-12, the Supervisory bus will transmit Blank words instead of the second message (AR, WC, As, WC, etc.). In condition 3 with serial control bit 8 set, the CIU will transmit Blank words instead of the first message (AR WC) but will transmit the second message identical to the Supervisory bus.



1 SERIAL CONTROL BIT 8 NOT SET

2 SERIAL CONTROL BIT 8 SET & UNIT CHECK BIT SET DURING FIRST MESSAGE

3 SERIAL CONTROL BIT 8 SET & UNIT CHECK BIT NOT SET DURING FIRST MESSAGE

4 INSERT WHEN UNIT CHECK BIT SET AT END OF MESSAGE

SERIAL DIU-DIU TRANSFER SEQUENCE

FIGURE 3.3-12

3.4 CIU ERROR MONITORING

The CIU monitors for error conditions on both the CIU-IOP interface and CIU-DIU interface. There are three registers in the CIU to store errors. These registers are Sense Register #1 -- CIU-IOP error storage, Sense Register #2 -- CIU-DIU error storage and Sense Register #3 -- DIU Error Status reply word storage.

3.4.1 Sense Register #1 Errors

Bit 0 - A-Word Parity Error during Initial Selection Sequence.

Bit 1 - WC-Word parity error during Initial Selection sequence.

Bit 2 - Illegal Op code in A word op code field.

Bit 3 - Inactivity error of CIU-IOP interface during Initial Selection sequence. The CIU requires completion of the Initial Selection sequence within 160 microseconds of raising OP In tag.

Bit 4 - Data word parity error on IOP to CIU data transfer.

Bit 5 - Under run error on CIU-IOP interface. The CIU requires the IOP to provide data within 7 microsecond after raising SVI tag in a Write mode service cycle.

Bit 6 - Over run error on CIU-IOP interface. The CIU requires the IOP to accept data within 7 microsecond after raising SVI tag in a Read mode service cycle.

Bit 7 - (Not used).

Bit 8 - Word count error initiated when IOP terminates the operational sequence by raising CMD Out tag prior to the CIU word counter reaching the last word state.

Bit 9 - The DIU-DIU Transfer error flag caused by 1) improper first message sequence in which the IOP does not provide one Data Word and 2) improper second message sequence in which the IOP request a Write operation rather than a Read operation.

Bits 10-15 - (Not Used)

3.4.2 Sense Register #2 Errors

Bit 0 - No DIU response on the Reply bus to a command on the Supervisory bus.

Bit 1 - Message sync error generated when the CIU cannot recognize the sync pattern in the first six bits of the DIU reply.

Bit 2 - Sync word parity error set when the parity bit of the sync word is incorrect.

Bit 3 - DIU address error set when the five DIU address bits in the sync word do not compare to the DIU address transmitted in the A-word.

Bit 4 - Word sync error generated when the WS bit of a DIU reply word is a logical 0.

Bit 5 - Reply parity error detected on DIU data, Blank or Status reply words. This error condition is not monitored during a DIU-DIU Transfer operation.

Bit 6 - Blank word error set when DIU replies with more than six consecutive Blank words during a Read operational sequence.

Bit 7 - Reply sequence error #1; set when last word on DIU reply bus is not Error Status word.

Bit 8 - Reply sequence error #2; set when DIU Error Status word received by CIU but DIU reply did not stop.

Bit 9 - Sense Register #3 flag; set by CIU whenever the contents of Sense Register #3 are invalid due to the following conditions:

1) No Error Status word in DIU reply message.
2) More than one Error Status Word in DIU reply message.
3) Incorrect parity received for the Error Status word.

Bit 10 - Reply sequence error #4; set when the DIU does not terminate reply message after CIU has dropped Word Sync bit on the Supervisory bus. This sequence error is not monitored during a DIU-DIU Transfer operation.

Bits 11 - 15 - Used to stored the five DIU address bits received in the Sync word of the DIU reply.

3.4.3 Sense Register #3 Errors

The bits in Sense Register #3 contain the Error Status bits of the DIU reply message.

3.4.4 CIU Error Response

The detection of errors on the CIU-IOP Interface and the CIU-DIU Interface initiate three basic actions within the CIU sequence control logic.

CIU Action #1 - Accept the A-word and WC-word, set Unit Check bit, and perform ending sequence.

The CIU initiates Action #1 whenever bits 0, 1, 2, 3 or 9 of Sense Register #1 or bit 7 of Sense Register #2 is set.

CIU Action #2 - Transmit a logical 0 bit for word sync for one bus word the transmit Blank Words on Supervisory bus, set Unit Check bit, and perform ending sequence.

The CIU initiates Action #2 whenever bits 4, 5, 6 or 8 of Sense Register #1 8, or 10 of Sense Register #2 is set.

CIU Action #3 - Transmit incorrect parity in the WC-word then transmit Blank words on Supervisory bus, set Unit Check bit and perform ending sequence.

The CIU initiates Action #3 when ever bits 0, 1, 2 or 3 of Sense Register #2 is set.

3.5 CIU CIRCUITS DESCRIPTION

The circuitry in the CIU is contained on nineteen boards. Schematic diagrams of each board is presented in Appendix A of this report. As a further aid in correlation of schematic and system function, the block diagrams of Section 3.1 are cross referenced to the board location. A brief description of the circuitry on each board is given in the following sections.

3.5.1 Boards 1 and 2

Boards 1 and 2 contain the receiver circuitry to interface with the IOP and Test Set "Tag Out" and "Bus Out" lines. The schematic of Boards 1 and 2 shows the division of the receivers between the two boards, and is referenced to Block Diagram Figure 3.1-2.

A detailed schematic of the receiver circuit is shown at the bottom of Boards 1 and 2 drawing. The receiver is a descrete design having a PNP input stage and a NPN output. The input impedance for the IOP receiver is approximately 8K ohm. The Test Set receivers have a 91 ohm input impedance to allow correct termination of the interface bus. The receivers have a nominal input threshold of 1.25 volts. The receiver NPN outputs are selected by the $\overline{\text{IOP EN}}$ or the $\overline{\text{CIU TEST EN}}$ signals. The EN signals ground the NPN emitters thereby allowing the output stage to saturate. The IOP/TEST FIXTURE switch on the front panel selects one of the two groups of the receivers.

The IOP and Test Set receivers are "OR'ed" through logic gates to develop the tag signal and bus out signals listed below.

OPO - operational out
ADO - address out
SLO - select out

HDO - hold out

AWO - A word out

CMO - command out

SVO - service out

SPO - suppress out

B0Ø thru B07 - Bus Out #1. B0Ø thru B07

B08 thru Bo15 - Bus Out #0
B0Ø thru B07

3.5.2 Board 3

Board 3 contains the Bus In drivers for both the IOP and CIU Test Set. The schematic of Board 3 is referenced to Block Diagram Figure 3.1-2. The CIU internal Bus In lines are double buffered through TTL inverters before outputting to the CIU-IOP or CIU-Test Set interfaces. The second TTL stage is an open-collector TTL inverter. The discrete Bus In line drivers are NPN emitter followers. A detailed schematic of the drivers is shown at the bottom of BOARD 3 drawing. Base drive of 2 ma for the NPN transistor is provided by the IN5305 constant current diode. Short circuit protection is obtained with the 20 ohm resistor. The driver output is capable of providing 60 ma at 3.2 v to meet the interface signal requirement. In addition to the base current clamp of the BI CLMP signals, the voltage lines to the constant current diodes (BI EN) are strobed to reduce power dissipation.

3.5.3 Board 4

Board 4 contains the CIU Status Register and the end status control logic, the Bus In word buffers, word latch, and parity generator, the tag line drivers for both IOP and CIU Test Set interfaces, and the relay controls. The Board 4 circuitry is shown with two pages of schematics and is referenced to Block Diagram Figure 3.1-2.

Page 1 of Board 4 schematic shows the "tag" In drivers. The drivers provide the control signals for the IOP and CIU Test Set interfaces. The drivers are identical to the Bus In drivers described for Board 3.

The end status control logic is shown on the lower left half of Board 4, page 1. This logic provides the END STATUS signal which sets the Device End and Channel End bits in the CIU Status register on Board 4, page 2. The end status control logic also provides the BSY CK used to trigger the Busy flip-flop on Board 16. Another control signal, $\overline{\text{END-O}}$, is used to initiate an ending sequence for OP code 00000. SR ER INH prevents Sense Register error status from setting the Status Register Unit Check bit during Sense Read, (Op Code 00110) and Immediate Ending (Op Code 00000) operations.

The relay controls shown on page 1 bypass SEL OUT through the CIU and clamps the Bus In and Control In drivers during power off conditions.

Page 2 of Board 4 schematics contains the Status Register and CIU address word buffer on the right half. The Status word and CIU address word are put on the BI lines through tri-state devices. The bottom left half of page 2 has the tri-state buffers used to insert 0's for all unused bit locations in the above two words. The left half of page 2 also contains the BI latch composed of 4 each four bit tri-state devices. Data to the IOP is first loaded into these BI latch circuits before enabled to the BI drivers. The parity bits for each eight bit byte of the BI word is generated in the two parity trees (MC14531AL) at the top left of page 2.

3.5.4 Board 5

Board 5 contains the time display storage registers, the time error isolated buffer, the four serial time transmitters and the end sequence counter control logic. Board 5 is referenced to Block Diagram 3.1-4 and is schematically shown on two pages.

Page 1 of Board 5 contains the storage registers for Time Word 1 and Time Word 2. The registers are developed with 4 bit CMOS latches. A common input bus from the Serial Time reciever is used to transfer data into the Time registers with TM 1LD and TM 2LD signals. The data output to the front panel decode and display boards is illustrated.

The right half of page 2 contains the four serial time transmitters. Each serial time transmitter is paired with a serial data transmitter of Board 11 to form a Serial Output channel. The five control bits SEL 1 thru SEL 4 and SRO EN select which transmitters are enabled. Serial NRZ time words are shifted into Board 5 from Board 7. The TM EN signal is a 3 word (30 μS) pulse synchronous with the serial data A word, WC word and first successive bus word. The conversion from a 2 M Bit NRZ format to 2 M Bit Bi-phase format is achieved with the exclusive OR gates and clocked D flip-flops.

The Serial Time Error buffer is shown in the middle portion page 2. This buffer has an isolated +5 v power input and an optical coupler signal input. The buffer outputs a +5 volt pulse to indicate an error condition. The output pulse width is approximately 10 μ sec. The Time Error front panel LED is driven from a TTL one shot (74 L121) to indicate an error condition.

The circuitry at the left portion of page 2 is the end sequence counter control logic. The $\overline{\text{SES RST}}$ signal forces the Bus Word Counter to reset when a serial error sequence (SES) has been recognized. The SES is active to allow the extra ending sequence time to insert the three Sense Registers words in the Serial Data Output. The STOP signal provides a Bus Word Counter count inhibit and is generated at BW8 time or at the completion of an ending sequence ($\overline{\text{END FLG RST}}$). The $\overline{\text{SES EN}}$ allows the SES flip-flop to be set if SER (serial output required) is true. Timing functions (BW, T and G) provide appropriate sequence action.

3.5.5 Board 6

Board 6 contains the Time input receiver and receiver control logic. Board 6 is referenced to Block Diagram 3.1-4 and schematically shown on three pages.

Page 1 of Board 6 contains the Time receiver front end. The Bi-phase signal is transformer coupled, rolled off through a three pole low pass filter, and detected by the high speed differential comparator (LM360). The comparator output is integrated by five different integrators. The two integrators located in the top middle of page 1 are the 3/4 bit negative pulse and 3/4 bit positive pulse integrators. The NPN outputs of these integrators provide the 1 to 0 and 0 to 1 bit transitions for the bi-phase signal. Three other integrators are used to provide BUS ACTIVE and 1/4 bit positive and 1/4 bit negative pulses. The 1/4 bit integrators drive the clock RS latch which is exclusively OR'ed with the NRZ TIME DATA to generate the NRZ TIME CLK.

Page 2 of Board 6 contains the receiver input register at the top portion and the word sync and error detect logic in the lower portion. As serial Time data is converted to NRZ it is shifted into the 22 stage register. The parallel outputs of the register are then loaded into the time word latches on Board 5. The sync detect circuitry is a 21 input AND function generated with the NOR and NAND gates at the lower left section of page 2. The time error detection logic checks for correct WS bit and correct parity bit in each time input word.

Page 3 of Board 6 shows the logic required to generate the TM load pulses for the three time words. TM 1LD and TM 2LD are used on Board 5 to parallel load Time words 1 and 2 into the display storage registers $\overline{\text{TM 3 LD}}$ is used by the time message synchronizer on Board 7 to indicate the receipt of the third time word.

3.5.6 Board 7

Board 7 contains the Time message synchronizer and control logic and the end sequence initiate logic. Board 7 is referenced to Block Diagram 3.1-4 and shown schematically on two pages.

Page 1 of Board 7 contains the end sequence initiate logic and the Time message synchronizer.

The end sequence initiate control logic is shown on the upper right portion of Page 1. The logic generates the terminate (TRM) signal which is used on Board 14 to cause ending sequence between the CIU and IOP. The functions used to generate TRM are mode (Op codes), time (BW) and the Serial Output states (SES and SER).

The remaining circuitry on Page 1 is the Time message synchronizer. The synchronizer is developed around a dual 64 bit CMOS shift register (U10). Each shift register has three operational states -- load, recycle, and inactive The load state allows the Time NRZ to be shifted into one of the two 64 bit shift registers. The recycle state allows the content of the shift register to output as the serial NRZ time (SR NRZ TIME) signal and also to fold back to the shift register input to be reloaded. By the action of LD1, LD2, RCY 1 and RCY 2 signals one of the shift registers always contains the three Time words to output to the Serial time transmitter on Board 5, while the other register is loading in the next Time words. Receipt of the Time words is indicated from the Time receiver by the $\overline{\text{TM 3 LD}}$ function. A three word TM EN signal is generated by the shift register (U12) to enable the Time message to be transmitted.

Page 2 of Board 7 contains the control logic for manipulating the two 64 bit shift registers. There are two interactive flag latches (U22 and U25) which

develop four flag conditions for each 64 bit shift registers. The flag conditions are load (1Ω), full (2Ω), recycle (3Ω) and load delay (4Ω).

3.5.7 Board 8

Board 8 contains the bi-phase transmitter for the Supervisory bus and the bi-phase receiver for the Reply bus. Board 8 is referenced to Block Diagram 3.1-3 and is shown schematically on three pages.

Page 1 of Board 8 contains the Supervisory bus transmitter. CIU data is loaded into the transmitter shift register from the XØ thru X15 bus lines by the function $\overline{\text{XMT LOAD}}$. The word prefix code is loaded from Board 13 through the XC_1 and XC_2 lines. Even parity is generated for the eighteen bits by the cascaded parity trees (U5 and U10) and also loaded into the transmitter shift register. The serialized shift register output is converted from NRZ to bi-phase by the exclusive OR (A7) and a D flip-flop. A transmitter complement signal XC is used to complement the word sync bit or the word count word parity bit in response to the CIU error monitor circuits. The bi-phase Supervisory signal is driven onto the bus through a transformer coupled discrete driver.

Page 2 of Board 8 contains the Reply bus receiver input register and receiver data storage register. NRZ DATA and REC CLK are derived from the bi-phase Reply bus data and used to serially load the input register. When the register is full the R-LD signal is generated by the receiver control logic on Page 3 of Board 8 to parallel dump the received data into the receiver data storage register. The outputs of the register RDØ - RD15, RC_1, RC_2, and R WS and R DP are available to both the received data storage memory on Board 12 and to the DIU error detection logic on Board 9.

The Reply bus receiver is shown on Page 3. The receiver is identical to the receiver for the Time input described in Section 3.5.5.

3.5.8 Board 9

Board 9 contains the error monitor logic for the Reply bus. The circuitry provides the error inputs to Sense Register #2 described in Section 3.4.2. Board 9 is referenced to the Block Diagram of Figure 3.1-3.

No DIU response error is detected by the gate U5-8 (with U5 the device number; -8 the output pin number).

Message sync error is detected by the exclusive OR comparator U14 and U15, and gates U11 and U2-9.

Sync word parity error is detected by gate U30-6.

DIU address error is detected by the exclusive OR comparator U13 and U14, and gates U17 and U2-6.

Word sync error is detected by gate U30-9 at the bottom of Board 9 schematic.

Reply parity error is detected by flip-flop U25-6 and U26-9 and by the gates U30-10 and U4-8.

Blank word error is detected by the up-down counter U3, flip-flop U1-8 and gates U7-9 and U16-13.

Reply sequence error #1 is detected by flip-flop U26-6, and gates U7-6 and U29-10.

Reply sequence error #2 is detected by gates U7-6 and U2-10.

Sense Register #3 flag is set with the action of flip-flop U21-6, U25-6, U26-9, gates U30-10, U4-8, U7-6 and U9-12.

Reply sequence error #4 is detected by the shift register U17 and gates U29-6.

The DIU reply address bits are buffered by gates U5 and U9.

3.5.9 Board 10

Board 10 contains Sense Registers #2 and #3. Board 10 is referenced to Block Diagram Figure 3.1-3 and is shown schematically on two pages.

Sense Register #2 is shown on Page 1. The storage elements are the four bit R-S latches U9 thru U12. The inputs to the latches are multiplexed throug four wide 2 to 1 devices(U5 thru U8). Either the DIU reply errors from Board 9 or the transmit bus XØ thru X15 are inserted into storage. The XØ-X15 functions are used to load the sense write word associated with Op code 00101. The input signal SR_2 TST EN selects the XØ-X15 inputs. The multiplexers are enabled by both SR_2 TST EN and RL EN, the latter signal being receiver logic enable.

The transfer ready ($\overline{\text{XFR RD}}$) signal is generated on Board 10 to indicate the reply word does not have incorrect parity or word sync.

There are several outputs derived from the error bits. The $\overline{\text{RIPPLE WS}}$ is the pulse output which enables the CIU logic to drop WS on the Supervisory bus message each time an error is detected. Other error states held in the S-R latches are decoded to activate the particular CIU error responses

described in Section 3.4.4. The B-ER result in CIU error response action #2; C-ER and D-ER cause CIU action #3.

The stored error bits of Sense Register #2 are enabled to the Sense Register Bus (SRØ thru SR15) by the $\overline{\text{SR 2 BS SL}}$. The SRØ thru SR15 signal drive LED indicator lights on the front panel of the CIU. The Sense Register #2 bits are also enabled to the transmit bus XØ thru X15 by $\overline{\text{SR2 BI SL}}$ to permit transfer to the IOP and to the Serial Output transmitters. The buffers for these two interfaces are tri-state CMOS devices U13, U14, U15, U27, U28 and U30.

Page 2 of Board 10 contains Sense Register #3. The register storage elements are 6 bit clocked D type flip-flops (U21, U22, U23). Sense Register #3 is loaded with either the DIU Error Status word from the Reply receiver or with the IOP word associated with the sense write instruction Op Code 00101. Both inputs are transferred into the Sense Register through the transmit bus (XØ thru X15).

The outputs of Sense Register #3 are routed to the same bus lines as previously described for Sense Register #2.

3.5.10 Board 11

Board 11 contains the Serial Data Outputs, the serial output control logic, serial data shift register and the serial end sequence control logic. Board 11 is referenced to Block Diagram, Figure 3.1-4 and is shown schematically on one page.

The four serial output data transmitters are shown on the right half of Board 11 schematic. The transmitters are identical to the serial time transmitters on Board 5 and to the Superviosry bus transmitter on Board 8. A detailed schematic of discrete design is shown as an insert.

The data word is loaded from the transmit bus XØ thru X15 along with the prefix code XC_1 and XC_2. Even parity is generated for the eighteen bits by the cascaded parity trees U13 and U14. The shift register U5-5, U9, U10 and U11 is clocked with a buffered 2 MHz signal and loaded by the $\overline{\text{SXMT LOAD}}$ signal.

The Serial Output control bits (BO 8 thru BO10)are temporarily stored in a 6 bit D clocked latch U29 by the SER CD LD signal. Bit 8 (BO8) is combined with the operational states of the CIU to establish the Serial Output enable functions (SRO EN). The SRO EN function is loaded into the channel select latch (U16) from the gate U32-6. SRO EN along with the select lines SEL 1 thru SEL 4 control the selection of the Serial Output transmitters for both data and time signals.

The function serial error sequence SES is modified by the conditions input to gate U4-8 to develop the SES-5 signal. SES-5 is used to output the A-word, word count word and three Sense Register words described in the section on Serial Output sequences, Section 3.3.3.

The stored serial control bits SB08 thru SBO12 are routed to Board 4 to combined with the CIU address bits in the address response word to the IOP.

The last area on Board 9 is the circuitry which develops the function data reply latch (D-RPY LH). This signal indicates that the first word after the DIU sync reply word is either a data word of a Blank word. The D-RPY LH signal is used to develop the SRO EN and SES-5 functions.

3.5.11 Board 12

Board 12 contains the transmitter data storage, the receiver data storage, data storage buffer and data storage control logic. Board 12 is referenced to Block Diagram, Figure 3.1-3, and is shown schematically on two pages.

Page 1 of Board 9 contains the transmitter data storage. The receiver data storage and the data storage buffer.

The transmitter data storage is divided into the data word storage and the control word storage. Devices U6 and U9 are the data word storage. Each device is a 4 word by 8 bit CMOS static memory. The control words - A word, WC word and AR word - are stored in U3 and U7. Both sections are loaded through the BØ thru B015 bus lines. Memory write signal XDS C-WR, XDS D-WR, memory read signals $\overline{\text{XDS C-RD}}$, $\overline{\text{XDS D-RD}}$, memory address lines XDS C-A1, XDS C-A0, XDS D-A1, XDS D-A0 and memory bypass signal XDS BP are generated by the data storage control logic on Page 2, Board 12.

The Reply receiver data is stored in memory devices U1 and U4. The data RDØ thru RD15 is loaded from the register on Board 8. The receiver data memory is controlled by functions identical to the transmitter storage functions.

One feature of the CMOS memory devices is the by pass control which allows the input data to be transferred directly to the memory output. The XDS BP command is used to route the two Sense Register word associated with Op Code 00101, from the Bus out (BOØ - BO15) to the transmitter bus (XØ - X15). The RDS BP command is used to transfer data from the Reply receiver (RDØ - RD15) bus to the transmitter bus (XØ - X15) into the BI latch.

The memory address codes are fixed only for the control words; A-word - loc. 11, WC-word - loc. 10, and A_R-word - loc. 01. Location 00 is not used in the XDS-control storage (U3, U7). The XDS-data storage and RDS storage utilizes a relative addressing scheme. The data is loaded into an arbritary location. However, the load address is maintained in a shift register. The shift register is shifted at the CIU word rate (10 μs) to provide the necessary address delay operation for the Supervisory and Serial Output sequences. Then the delayed address is obtained from the shift register to allow data to be read from storage.

The outputs of the memory devices are tri-state and are tied together to form a 16 wide memory data bus. The memory data bus is buffered onto the transmitter bus through the CMOS tri-state devices U2, U5 and U26. This buffering was necessary due to the poor drive capability of the memory devices.

Page 2 of Board 12 contains the storage control logic. This logic develops the memory device control function previously described. The address shift register which generates the relative A0 & A1 addresses is the six bit D latch U14. Its first two stages are connected as a 2 bit Johnson counter, the other four stages are connected as a two bit wide, two stage shift register. The register is clocked at the CIU word rate and is timed relative to the operating mode.

The decode gates which generate the memory control signals are straight forward. They utilize mode inputs, distinct bus word times (BW and BW' functions) and the transmitter load time functions (XMT-LT and SXMT-LT). The XMT-LT and SXMT-LT functions are successive 2.5 us pulses during which the transmitter bus is made available to the Supervisory transmitter (XMT-LT) or to the Serial Output data transmitters (SXMT-LT). The other functional inputs are $\overline{\text{LD AW EN}}$, $\overline{\text{LD WC EN}}$, $\overline{\text{LD DATA EN}}$, $\overline{\text{DIU}}_{\text{DL}}$, END FLG, SES-5 and $\overline{\text{BLANK}}$.

The $\overline{\text{LD XX EN}}$ functions are developed on Board 16 to enable loading the respective A-word, WC-word and Data word from the IOP. $\overline{\text{DIU}_{DL}}$ is enabled for the second message time of the DIU-DIU transfer operation. END FLG is raised to terminate the Supervisory and Serial Output bus operations. The $\overline{\text{BLANK}}$ input line is developed by the blank word generator on Board 15 whenever Blank words are put on the Supervisory and Serial Out bus lines. The SES-5 signal was described in Section 3.5.10.

3.5.12 Board 13

Board 13 contains the CIU bus control logic. Board 13 is referenced to Block Diagram Figure 3.1-3 and is shown schematically on two pages.

Page 1 of Board 13 is divided into two general areas. The top portion of Page 1 contains the control flags bus sequence (BS), serial error sequence (SES) and end flag (END FLG).

The BS flag is the basic logic enable signal for all bus and self test operations. It is raised for all legal op codes except the immediate end OP code 00000. BS is clocked at T4 G5 time and controlled by the BSY signal from Board 16.

The SES flag is set during the END FLG enable time to initial the transmission of the three Sense Registers on the Serial Output. SES is modified by SES-5 to transmit the A-word and WC-word in addition to the three Sense Registers as required during a Write operation with serial control bit 8 set. The SES flip-flop is clocked at SXMT-LT when enabled by the error function input to U30-4 and U32-6.

The END FLG is set at the end of all BS operations except for the first message ending of a DIU-DIU transfer operation. The END FLG is enabled by three different signal sources: 1) normal ending ($\overline{\text{NRM END}}$) 2) status

ending $\overline{\text{STAT END}}$ and 3) forced ending ($\overline{\text{FORCE BLANK}}$). The $\overline{\text{NML END}}$ signal is developed on Board 14. The $\overline{\text{NML END}}$ indicates the CIU has reached the predefined time to terminate the BS operation, either by zero count in the word counter, by performing a fixed number of CIU-IOP operations or by receipt of a CMO signal from the IOP.

The $\overline{\text{STAT END}}$ signal is also developed on Board 14. This signal indicates the reception of the Error Status is detected on the Reply bus and the CIU terminates all BS operations. Two Read op codes utilize this ending method as a "normal" termination method -- Read DI changes, op code 10010 and Read AI Exceeding Deltas, op code 11100. Reception of the Error Status word prematurely is an error condition indication from the DIU to terminate the bus sequence.

The $\overline{\text{FORCE BLANK}}$ is developed on Page 2 of Board 13 whenever the Supervisory bus operation is terminated due to error detection by the CIU. The $\overline{\text{FORCE BLANK}}$ signal initiates the END FLG operation while forcing the Supervisory bus and Serial Output bus transmitters to transmit Blank words.

The BS flag and END FLG signals are also used to control the bus word counter on Board 17. The $\overline{\text{BW EN CK}}$ causes the bus word counter to begin counting thereby generating BW1 thru BW8 word times. The bus word counter is started at the beginning of both BS and END FLG signals. The END FLG also provides a bus word counter reset (BW RST) signal to force the counter to either BW8 or BW1 states when initiating a counter restart.

The circuitry on the lower portion of Page 1 contains the logic to control the threeSense Registers. The Sense Register select ($\overline{\text{SR}_x \text{ BI SL}}$) signal

enables reading the contents of the Sense Register onto the transmitter bus (XØ - X15) to be routed to either the IOP via the Bus In or to the Serial Output transmitters. Loading of the Bus In Latch is enabled by the BILH LD signal.

Two signals are also generated on Page 1 to allow Sense Registers 2 and 3 to be loaded. The SR_2 TST EN allows the IOP to load Sense Register 2 during the Sense Write (op code 00101) sequence. $\overline{\text{SR3 LD}}$ allows the loading of Sense Register 3 by the IOP during the above sequence, and by the DIU Error Status reply.

Page 2 of Board 13 contains the bus prefix generator on the left half and the error response logic on the right half. The receiver logic enable (RL EN) latch is also contained in the left half section.

The prefix generator (XC_1 and XC_2) signals are decoded by the gate array using the various CIU mode signals together with the data storage enable signals and bus word time decodes. The decoding is straight forward in that U19-11 output gives the 11 prefix, U19-3 output the 10 prefix, U2-6 output the 01 prefix and BLANK WD EN forces the 00 prefix.

The error response logic on the right half of Page 2 has the drop word sync (DRP WS) signal, the $\overline{\text{FORCE BLANK}}$ signal and the transmitter complement (XC) signal. The DRP WS enabled by three methods: 1) a CIU reset operation, 2) the $\overline{\text{RIPPLE WS}}$ signal and 3) the appropriate error status of Sense Registers 1 and 2. The last two methods are related in that the $\overline{\text{RIPPLE WS}}$ also sets error bits in Sense Register 2. The purpose of having $\overline{\text{RIPPLE WS}}$ is that repetitive errors during the same bus operation will cause the CIU to drop word sync at each error occurence at a maximum rate of every other word time.

The $\overline{\text{FORCE BLANK}}$ signal causes the Supervisory bus and Serial Output buses to transmit Blank words. The XC signal causes either the WC-word parity bit or the WS bit to be complemented in the Supervisory bus transmitter.

3.5.13 Board 14

Board 14 contains the CIU sequence control logic. Board 14 is referenced to Block Diagram Figure 3.1-2 and is shown schematically on two pages.

Page 1 of Board 14 contains the control logic for the CIU-IOP service cycles and the ending sequence initiate logic. Also on Page 1 are the error detectors for overrun error and $\overline{\text{CMO}}$ error.

The service cycle functions developed on Page 1 are enable Service In ($\overline{\text{EN SVI}}$), drop Service In (DRP SVI), enable BI latch output ($\overline{\text{BILH OUT}}$), and decrement word counter (DCR WC).

Functions associated with loading the A-word and WC-word from the IOP are LD A-WD, $\overline{\text{LD WC}}$, A-WD LD CMP, and WC-LD CMP. The first two signals are generated to do the load operation while the last two signals (— LD CMP) indicate completion of the load operation and allow continuation of the sequence.

Initiation of the END FLG and subsequent ending sequence is through logic circuits at the lower section of Page 1. The END FLG is enabled by $\overline{\text{NML END}}$; U20-1 or $\overline{\text{STAT END}}$; U3-12. The various CIU modes and timing function are decoded to generate these two signals. Also associated with the END FLG is the initiation of the CIU-IOP ending sequence. The function END SQN; U31-3 raises the Status In tag line to perform the ending sequence. With the exception of the DIU-DIU Transfer Op Code 10101 and the Immediate End Op Code 00000, the terminate (TRM) signal is used to enable END SQN. The DIU-DIU Transfer uses BW4 time while the Immediate End operation uses $\overline{\text{END-0}}$ generated on

Board 4. The sequence reset SQN RST is generated from U25-6 to reset the Busy flip-flop on Board 16 along with CMO, SVI and STATUS RCVD latches of U15 on Page 1.

Two error functions are generated for Sense Register 1. The overflow error (OVR ER) indicates that the Bus In latch has not been loaded into the IOP before it must be updated by the next BILH LD function. The Command Out error $\overline{\text{CMO ER}}$ indicates the CIU word counter does not have a word count of zero ($\overline{\text{WCO}}$)when the IOP terminates the CIU operating sequence.

Page 2 of Board 4 contains the CIU reset circuits, the Sense Register clear function and the special function bus word generator. The $\overline{\text{FORCE RST}}$ signal is generated by either the Power Supply power on reset ($\overline{\text{POR}}$) or by depressing the manual reset switch on the CIU front panel. The Sense Register clear (SR CR) resets all the Sense Registers, either as a result of $\overline{\text{FORCE RESET}}$ or as a result of loading a new A-word into the CIU. Sense Register clear is inhibited while operationg in the Sense Read mode (Op code 0110). The special function bus word generator developes bus word time $\overline{\text{BW2}}'$, $\overline{\text{BW3}}'$ and $\overline{\text{BW4}}'$. These bus word times correspond to the regular bus word times $\overline{\text{BW2}}$, $\overline{\text{BW3}}$ and $\overline{\text{BW4}}$ without the END FLG being set. In short bus transactions the bus word counter may be reset by the END FLG prior to reaching BW2 count. The special bus word generator provides the prime functions to circumvent this problem.

3.5.14 Board 15

Board 15 contains Sense Register #1 and the Blank Word generator. Board 15 is referred to Block Diagram, Figure 3.1-2 and is shown schematically on two pages.

Page 1 contains the Sense Register along with some error detection logic. Sense Register 1 is built with four 4 bit RS latches. The latch outputs are buffered onto both the Sense Register bus (SRØ - SR15) and the transmitter bus (XØ - X15) by tri-state buffers. The error detection shown on Page 1 is simple logic gating. The outputs of several error functions are also combined to create the IOP ER signal. When doing a Sense Read, (Op Code 00110) or Immediate End (Op Code 00000) operation the error states held by the Sense Registers are inhibited from setting the Unit Check bit in the CIU Status latch on Board 4. However, the IOP interface is monitored for errors through the IOP ER function. If any error function which inputs to IOP ER is detected, the Unit Check bit is set regardless of operating mode.

Page 2 of Board 15 contains the blank word generator. The blank word generator operates in conjunction with the data storage section of Board 12 to provide information to transmitter bus (XØ - X15). The $\overline{\text{BLANK}}$ function from U4-6 is used on Board 12 to inhibit reading the memory whenever Blank words are impressed on the transmitter bus through the tri-state buffers U9, U10, U15 and U30. The BLANK WD EN signal forces the prefix generator on Board 13 to output the 00 word prefix.

3.5.15 Board 16

Board 16 contains the IOP interface control circuits along with IOP message decodeand error checking logic. Board 16 is referenced to Block Diagram Figure 3.1-2 and is shown schematically on two pages.

Page 1 of Board 16 contains the A-word storage and decode logic, the CIU word counter and CIU word parity and address monitors. The word count from the IOP is loaded into the 16 stage down counter located at the top of Page 1. The counter is implemented with CMOS 4 bit devices U13, U14, U15 and U16.

The counter is loaded by $\overline{\text{LDWC}}$ and decremented by DCR WC, both from the sequence control logic on Board 14. After being loaded the counter is tested for all zeros counted by the WC LD CMP signal clocking U29. If the word counter has not been loaded with all zeros, the output function $\overline{\text{WCO}}$ will be enabled.

The CIU operating mode is decoded from the A-word Op Code field bits B05 thru B09. Bits B06 thru B09 are loaded into internal latched contained in the 4 line to 16 line decoders U2 and U4. Bit B05 is loaded along with the DIU address into the 6 stage latch U5. The outputs of the 4 line to 16 line decoders are combined for several Op Codes to form general modes of operation such as WRITE, READ VARIABLE 1 and 2 (RDV 1 & RDV2) and READ FIXED (RDF).

Parity checks on the two 8 bit bytes of the Bus Out interface are performed by U9 and U10 parity trees. The CIU address bits are compared to the front panel thumbwheel setting in the comparator U11.

Page 2 of Board 16 contains the IOP interface control functions - Operational In (OPI), Address In (ADI), Select In (SLI), Status In (STI) and Service In (SVI). Also on page 2 is the Busy flag latch U30-5 which controls the BS flag on Board 13 and the Busy bit of the CIU Status Word on Board 4.

3.5.16 Board 17

Board 17 contains the 16MHz oscillator along with various counters to form the CIU clock system. Board 17 is referenced to Block Diagram Figure 3.1-4 and is shown schematically on two pages.

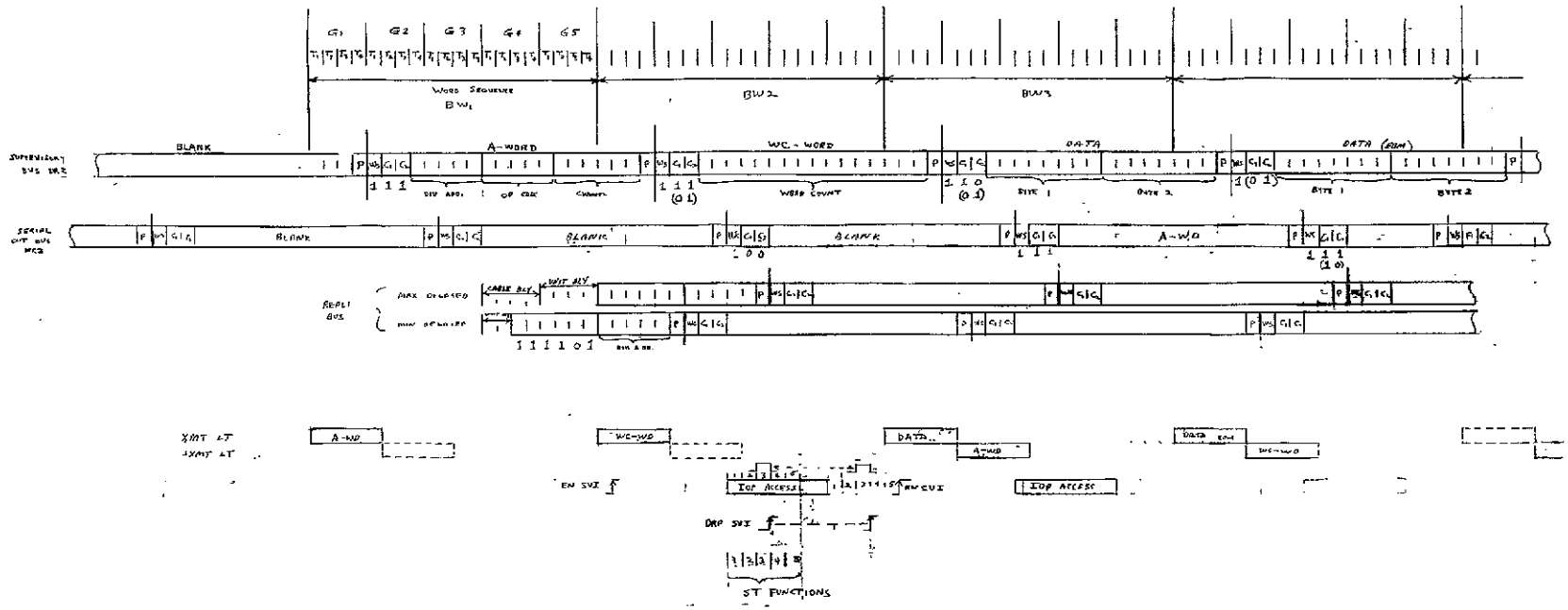
Page 1 of Board 17 contains the 16MHz oscillator, the phase counter, tag counter and group counter along with the CIU time decode gates. The phase counter

U9 outputs four phase clocks Ø1, Ø2, Ø3 and Ø4. The tag counter U10 outputs four tag clocks T1, T2, T3 and T4. The group counter outputs five group times G1, G2, G3, G4 and G5. The relationship of the three counters is shown in the general timing diagram Figure 3.5-1. Each phase clock is a 125 ns pulse occurring at a 2MHz rate. Each tag clock is a 500 ns pulse occurring at a 500 KHz rate. Each group clock is a 2 µs pulse occurring at a 100 KHz rate.

An external clock input is provided on J7 connector to accept an 8 MHz ext. clock. Selection of the CIU operating clock is by means of the front panel switch.

Page 2 of Board 17 contains the bus word counter, the sequence time counter and the error detection logic for the timeout error and the under run error.

The bus word counter is a divide by eight synchronous, presetable counter developed with U8, U12 and U6. The count sequence for the three stages is identified at the top of Page 2. The count decode is performed with a 3 line to 8 line decoder U29. The bus word counter is started at the beginning of the BS and END FLG signals and is controlled by the $\overline{\text{BW EN CK}}$ function. The counter will normally begin its count from the BW8 state and will count through, unless reset, to the BW8 state. In short CIU sequences the bus word counter may be preset by the END FLG control.BW RST signal. The BW RST signal will preset the counter to BW8 state for all but the Read modes. When operating in the Read modes the BW RST signal presets the bus word counter to BW1 state. A second reset function $\overline{\text{SES RST}}$ presets the bus word counter to the BW3 state. The STOP function along with BW8 state resets the counter clock enable flip-flop U6 to inhibit further bus word counting.



ORIGINAL PAGE IS
OF POOR QUALITY

BASIC TIMING
FUNCTIONS

FIGURE 3.5-1

FOLDOUT FRAME

FOLDOUT FRAME 2

The sequence time counter is implemented with an eight state shift register U2 configured along with U3 to form a one shot burst of ST clock functions. The ST functions are 500 ns sequential pulses which are triggered by the IOP-CIU data transfer tags. The clocks are enabled by AWO, CMO, STI dly SVO•SVI and CMO•SVI. During the initial selection sequence the ST ring counter is reset at ST8 time. Once the BS flag is raised, however, the ST counter is reset at ST 5 time. The function of the ST counter is to provide sequential time states to simplify the logic implementation of the IOP-CIU interface transfer.

The time out error detector (TIME ER) is a 4 stage counter clocked at a 10KHz (G1) rate. The counter is enabled whenever OPI is raised. The counter must be inhibited by the completion of the initial selection sequence (SVO response to STI) within the 160 us maximum count state.

The underrun error detector U18-10 is set during each Write service cycle. It must be reset by the IOP's SVO response during the allowable IOP access time (7 μs from SVI).

3.5.17 Board 18

Board 18 contains the CIU power supply, Board 18 is referenced to Block Diagram Figure 3.1-4 and is shown schematically on one page.

The CIU power supply consists of a switching regulator followed by a DC-DC converter. Input and output filtering is provided to keep power supply noise within acceptable limits for the logic families used in the CIU. The switching regulator is developed with low power integrated comparators (LM339) and discrete components. The power switch of the regulator is the NPN transistor Q3 (2N5487). The regulator LC filter L2 and C5 converts the pulse width

modulated signal to a 20VDC level input to the DC-DC converter. The 20 V regulated output is an approximate value as the regulator uses the 5V logic output as the regulated point. The feed back from the 5V logic output is through the optical coupler U32. R27 is the select resistor to trim the 5V level. A temperature compensated reference diode CR17 (1N823) provides a 6.2V reference to the regulator. The switching regulator output is protected against an overvoltage output by the comparator U15-13. Power supply current is monitored through the 0.1 ohm resistor R21 by comparator U15-14. Current overload is set to turn off the regulator at approximately 2 amps. The overvoltage detector turns off the DC-DC converter when the regulated converter input exceeds 23V.

The DC-DC converter is a two transformer design. The converter runs at approximately 17 KHz. The frequency is set by the drive transformer T2. T2 has a square loop magnetic tape core which is selected to operate the DC-DC converter without saturating the main transformer (T1) core. Full wave rectification is used on the secondary windings along with LC pi filters, except for the 5V isolated output. The isolated output is not referenced to any CIU ground and is used solely to power the isolated Time Error buffer on Bd. 5.

The CIU power supply also provides the power on reset ($\overline{\text{POR}}$) signal to initializ the CIU upon application of the 28V input. The $\overline{\text{POR}}$ signal remains low for approximately 100 millisecond after applying 28V to the input.

The input current at 28V is approximately 700 milliamps with all front panel LED turned on.

3.5.18 Board 19

Board 19 contains the LED drivers for all CIU front panel indicators except

the Time Error indicator. Board 19 is referenced to Block Diagram 3.1-3 and is shown schematically on one page. The LED drivers for the sixteen Sense Register bus line (SRØ-SR15) and the three interface indicators - Message Sync, Reply Sync, and Unit Check - are shown on Board 19 schematic.

3.6 MECHANICAL DESCRIPTION

The Computer Interface Unit consist of 19 each double-sided logic cards mounted in an ARK-12 series adjustable card cage. The CIU housing is approximately 19" x 19" x 12".

The CIU front panel shown in Figure 3.6-1 consist of functional displays, test points, and select switches. The decimal time displays are located on the rear of the panel. These displays plug-in and are interchangeable. The Sense Register displays consist of sixteen discrete LED's used to display register words 1 thru 3 as selected by the Sense Reg Select switch.

The time error light indicates either word sync error or parity error in the Time Input message. The Unit check error light is used to indicate any error condition detected by the CIU error monitor circuitry. The Message Sync light is used to indicate the transmission of an A-Wd on the Supervisory Bus. The Reply Sync light indicates that the CIU has received a reply sync word from DIU.

The CIU ADD switch is a BCD thumbwheel switch used to select addresses 0 thru 7. The EXT CLK switch may be used to select an external 8 MHz system clock. The reset switch is a momentary push-button used for internal resetting of the CIU. The power switch is used to apply +28 VDC to the CIU power supply.

An external GND test point is provided and is tied to the CIU system ground. There are thirteen discrete test points located on the front panel which can be used to monitor logic functions. The test point functions are summarized on the following page.

- The Clk test point provides a 2 meghz clock.
- The Word Sync test point provides a signal at the system word rate.
- The A-WD test point provides a pulse that is synchrones with each A-WD present on Supervisory bus.
- The End of Message is a signal used to indicate the last word sent out on Supervisory bus.
- The signal ADD Out is used to indicate that a CIU address word is present.
- The signal SER IN (Service In) is present for each data word that is exchanged between CIU and IOP.
- The signal SER OUT (Service Out) is present at the end of initial selection sequence for each data word exhanged between the CIU and IOP and at the end of one completed operation.
- The signal Status In is used to indicate CIU status during initial selection sequence and status at the end of a completed operation.
- The signal Reply Sync indicates that the CIU has received a sync word from the DIU.
- The test point marked SUP BUS can be used to monitor Bi-phase data sent out on the Supervisory bus.
- The Reply Bus test point monitors data received rom the DIU.
- The SUP and REPLY NRZ test points monitor data after its conversion to NRZ.

The CIU rear panel shown in Figure 3.6-2 contains all function connectors required for operation. The following is a brief description of connector function. Connectors J1 thru J4 are Serial data and time output connectors. The connectors J5A-1 thru -3 are required for direct interface to the IOP for operation. The connectors J5B-1 thru -3 are parallel wired to J5A-1 thru -3 to provide daisy chaining of CIU's. The connectors J6-1 thru -3 are provided for the CIU Test Set interface. The connector J7 is the Serial

C 12

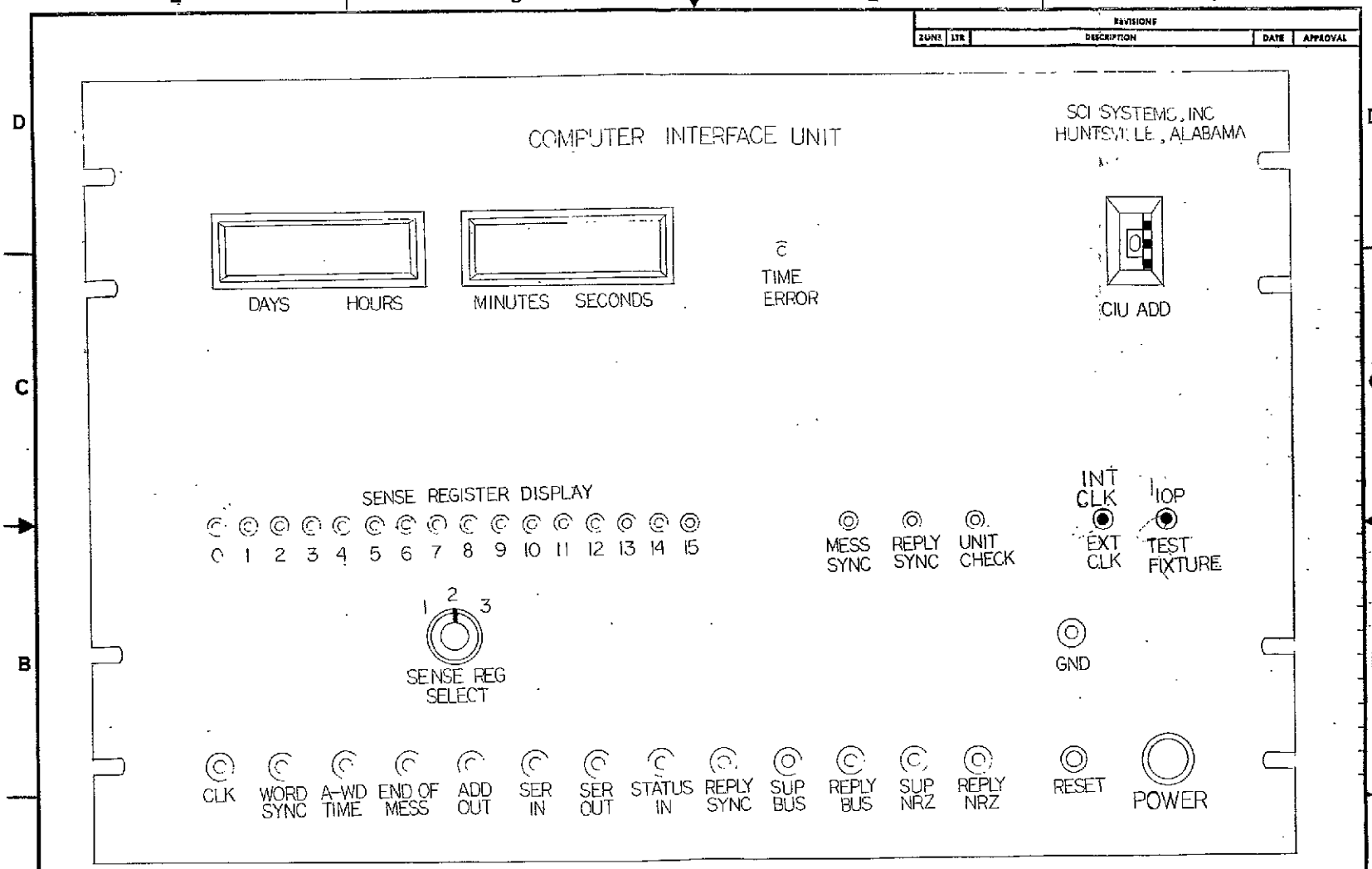


FIGURE 3.6-1

CIU FRONT PANEL

SIZE	CODE IDENT NO.	DWG NO.
C	17981	
SCALE	UNIT WT.	SHEET / OF /

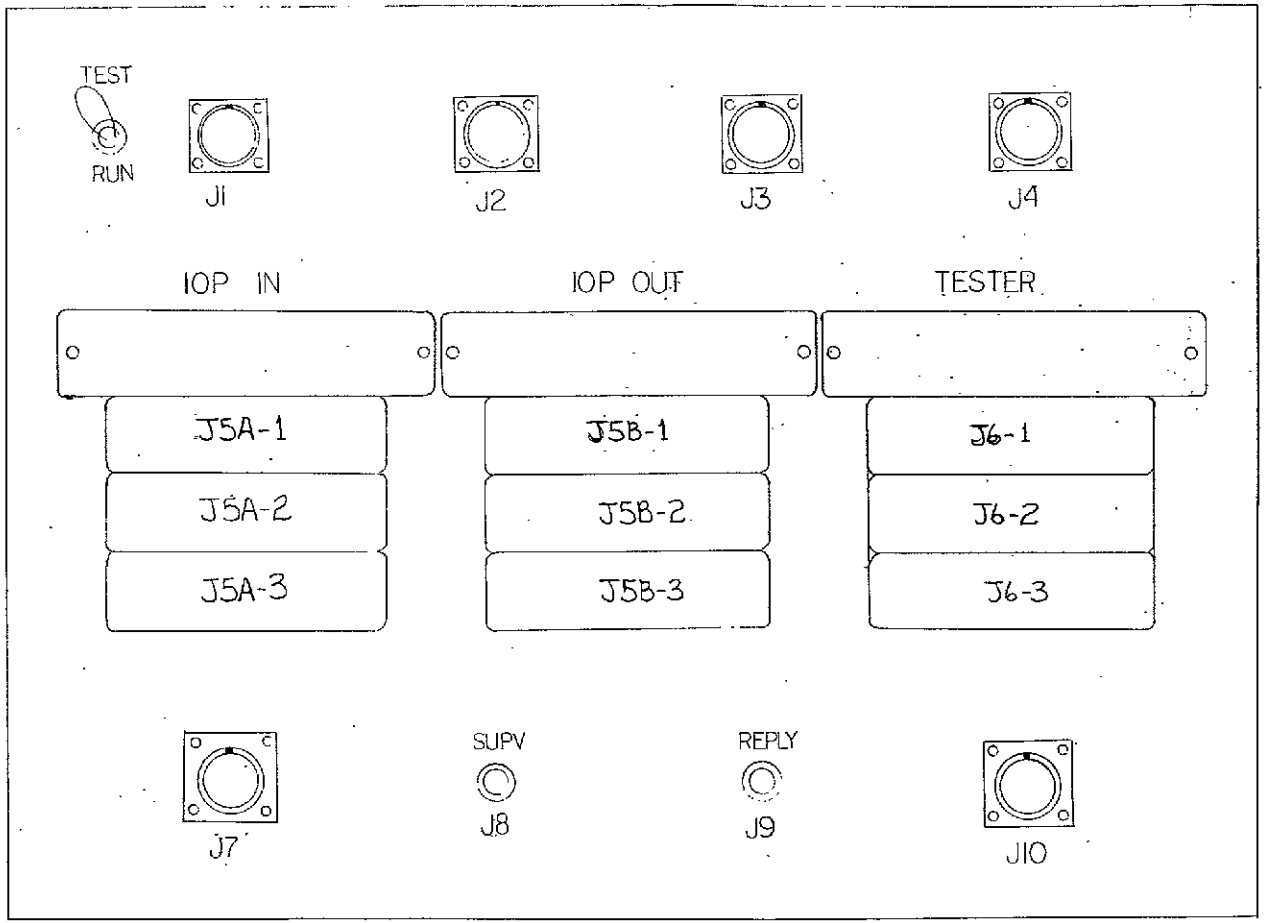


FIGURE 3.6-2

CIU REAR PANEL

SIZE	CODE IDENT NO.	DWG NO.
C	17981	

SCALE | UNIT WT. | SHEET OF

time and Ext clock input connector. Connector J8 is used to output Supervisory bus data. Connector J9 is used to receive data from all DIU's on the Reply Bus. Connector J10 is provided to input +28 VDC to the CIU. Also located on the rear panel is a Test/Run Switch. This switch when used in run position provides normal CIU operation. It can be used in test position for troubleshooting of CIU to provide continuous operation without a DIU connected to the bus.

The following pages contain the pin function lists for all rear panel connectors.

FUNCTION	Ref. Des.	Part Number/Value: PTOOCE-12-10S(SR)
		J1
SER DATA 1 +	A	B D 1 1 B 1 2 T P
SER DATA 1 -	B	B D 1 1 B 1 3
CHASSIS GND	C	
SER TIME 1 +	D	B D 5 B 3 T P
SER TIME 1 -	E	B D 5 B 5
N/C	F	
N/C	G	
N/C	H	
N/C	J	
N/C	K	

J1 - PTOOCE-12-10S(SR)

SERIAL OUTPUT 1

CODE IDENT. NO.	DWG. SIZE	
17981	A	CIU EXT J1
		SHEET 1 of 1

FUNCTION	Ref. Des.	Part Number/Value: PTOOCE-12-10S(SR)
	J2	
SER DATA 2 +	A	BD 11 B 14 TP
SER DATA 2 -	B	BD 11 B 15
CHASSIS GND	C	
SER TIME 2 +	D	BD 5 B 7 TP
SER TIME 2 -	E	BD 5 B 9
N/C	F	
N/C	G	
N/C	H	
N/C	J	
N/C	K	

J2 - PTOOCE-12-10S(SR)

SERIAL OUTPUT 2

CODE IDENT. NO 17981	DWG. SIZE A	CIU EXT J2
		SHEET 1 of 1

FUNCTION	Ref. Des.	Part Number/Value: PTOOCE-12-10S(SR)
	J3	
SER DATA 3 +	A	BD 11 B 16 → TP
SER DATA 3 -	B	BD 11 B 17 →
CHASSIS GND	C	
SER TIME 3 +	D	BD 5 B 11 → TP
SER TIME 3 -	E	BD 5 B 13 →
N/C	F	
N/C	G	
N/C	H	
N/C	J	
N/C	K	

J3 - PTOOCE-12-10S(SR)

SERIAL OUTPUT 3

CODE IDENT. NO. 17981	DRG. SIZE A	CIU EXT J3
		SHEET 1 of 1

FUNCTION	Ref. Des.	Part Number/Value: PTOOCE-12-10S(SR)
	J3	
SER DATA 3 +	A	BD 11 B 16 TP
SER DATA 3 -	B	BD 11 B 17
CHASSIS GND	C	
SER TIME 3 +	D	BD 5 B 11 TP
SER TIME 3 -	E	BD 5 B 13
N/C	F	
N/C	G	
N/C	H	
N/C	J	
N/C	K	

J3 - PTOOCE-12-10S(SR)

SERIAL OUTPUT 3

CODE IDENT. NO.	DWG. SIZE	
17981	A	CIU EXT J3
		SHEET 1 of 1

FUNCTION	Ref. Des.	Part Number/Value: PTOOCE-12-10S(SR)
		J4
SER DATA 4 +	A	BD 11 B 18 TP
SER DATA 4 -	B	BD 11 B 19
CHASSIS GND	C	
SER TIME 4 +	D	BD 5 B 15 TP
SER TIME 4 -	E	BD 5 B 17
N/C	F	
N/C	G	
N/C	H	
N/C	J	
N/C	K	

J4 - PTOOCE-12-10S(SR)

SERIAL OUTPUT 4

CODE IDENT. NO	DWG. SIZE	CIU EXT J4
17961	A	SHEET 1 of 1

NOTE:
1. ALL RTN's CONNECT TO CIU SYSTEM GND
2. X = SAME PIN

FUNCTION	Ref. Des.	Part Number/Value	Section	Pin No.	Not Used In CIU	J5B-1 SAME PIN
PO$_\phi$ RTN			B	2		X
PO$_\phi$			B	3		X
BO1$_\phi$ RTN			B	4		X
BO1$_\phi$			B	5		X
N/C			B	6		
BO3$_\phi$ RTN			B	7		X
BO3$_\phi$			B	8		X
BO5$_\phi$ RTN			B	9		X
BO5$_\phi$			B	10		X
N/C			B	11		
BO7$_\phi$			B	12		X
BO7$_\phi$ RTN			B	13		X
PI$_\phi$ RTN			G	2		X
PI$_\phi$			G	3		X
BI1$_\phi$ RTN			G	4		X
BI1$_\phi$			G	5		X
CIU SYSTEM GND			G	6		X B D. 1 A 3
BI3$_\phi$ RTN			G	7		X
BI3$_\phi$			G	8		X
BI5$_\phi$ RTN			G	9		X
BI5$_\phi$			G	10		X
N/C			G	11		
BI7$_\phi$			G	12		X
BI7$_\phi$ RTN			G	13		X

J5A-1 -(Block) IBM 5353868(B)
(Pin) IBM 5362901

IOP - IN (-1)

CODE IDENT. NO. 17981	DRG SIZE A	CIU EXT J5A-1
		SHEET 1 of 2

FUNCTION	Ref. Des.	Part Number/Value	Section	Pin No.	Not Used In CIU		J5B-1 SAME PIN
N/C			D	2			
N/C			D	3			
BO Φ$_\phi$			D	4			X
BO Φ$_\phi$ RTN			D	5			X
BO 2$_\phi$			D	6			X
BO 2$_\phi$ RTN			D	7			X
BO 4$_\phi$ RTN			D	8			X
BO 4$_\phi$			D	9			X
BO 6$_\phi$ RTN			D	10			X
BO 6$_\phi$			D	11			X
J5B-1 D12			D	12	*		X
J5B-1 D13			D	13	*		X
N/C			J	2			
N/C			J	3			
BI Φ$_\phi$			J	4			X
BI Φ$_\phi$ RTN			J	5			X
BI 2$_\phi$			J	6			X
BI 2$_\phi$ RTN			J	7			X
BI 4$_\phi$ RTN			J	8			X
BI 4$_\phi$			J	9			X
BI 6$_\phi$ RTN			J	10			X
BI 6$_\phi$			J	11			X
J5B-1 J12			J	12	*		X
J5B-1 J13			J	13	*		X

J5A-1 - (Block) IBM 5353868(B)
(Pin) IBM 5362301

IOP-IN (-1)

CODE IDENT. NO. 17981	DWG. SIZE A	CIU EXT J5A-1
		SHEET 2 of 2

FUNCTION	Ref. Des.	Part Number/Value	Section	Pin No.	Not Used In CIU	J5P-2 SAME
OP IN RTN			B	2		X
OP IN			B	3		X
ADR IN RTN			B	4		X
ADR IN			B	5		X
N/C			B	6		
SEL IN RTN			B	7		X
SEL IN			B	8		X
ADR OUT RTN			B	9		X
ADR OUT			B	10		X
N/C			B	11		
SUP OUT			B	12		X
SUP OUT RTN			B	13		X
J5B-2 G2			G	2	*	X
J5B-2 G3			G	3	*	X
J5B-2 G4			G	4	*	X
J5B-2 G5			G	5	*	X
J5B-2 G6			G	6	*	X B D 1 A 4
J5B-2 G7			G	7	*	X
J5B-2 G8			G	8	*	X
J5B-2 G9			G	9	*	X
J5B-2 G10			G	10	*	X
N/C			G	11		
HLD OUT			G	12		X
HLD OUT RTN			G	13		X

J5A-2 - (Block) IBM 5353868 (B)
(Pin) IBM 5362301

IOP - IN (-2)

CODE IDENT. NO.	DEG. SIZE	CIU EXT J5A-2
17961	A	SHEET 1 of 2

FUNCTION	Ref. Des.	Part Number/Value	Section	Pin No.	Not Used In CIU		J5B-2 SAME PIN																							
N/C			D	2																										
N/C			D	3																										
STA IN			D	4			X																							
STA IN RTN			D	5			X																							
SRV IN			D	6			X																							
SRV IN RTN			D	7			X																							
SEL OUT RTN			D	8			X																							
SEL OUT			D	9			X																							
CMD OUT RTN			D	10			X																							
CMD OUT			D	11			X																							
SPV OUT RTN			D	12			X																							
SPV OUT			D	13			X																							
A OUT			J	1			X																							
A OUT RTN			J	2			X																							
J5B-2 J4			J	4	*		X																							
J5B-2 J5			J	5	*		X																							
J5B-2 J6			J	6	*		X																							
J5B-2 J7			J	7	*		X																							
J5B-2 J8			J	8	*		X																							
J5B-2 J9			J	9	*		X																							
J5B-2 J10			J	10	*		X																							
J5B-2 J11			J	11	*		X																							
OP OUT RTN			J	12			X																							
OP OUT			J	13			X																							

J5A-2-(Block) IBM 5353868 (B)
(Pin) IBM 5362301

IOP - IN (-2)

CODE IDENT. NO.	DWG SIZE	CIU EXT J5A-2
17981	A	SHEET 2 of 2

FUNCTION	Ref. Des.	Part Number/Value	Section	Pin No.	Not Used In CIU		J5B-3 SAME PIN																		
PO, RTN			B	2			X																		
PO,			B	3			X																		
BO1, RTN			B	4			X																		
BO1,			B	5			X																		
N/C			B	6																					
BO3, RTN			B	7			X																		
BO3,			B	8			X																		
BO5, RTN			B	9			X																		
BO5,			B	10			X																		
N/C			B																						
EO7,			B				X																		
EO7, RTN			B				X																		
PI, RTN			G	2			X																		
PI,			G	3			X																		
BI1, RTN			G	4			X																		
BI1,			G	5			X																		
CIU SYSTEM GND			G	6			X	B	D		1		A	H	E										
BI3, RTN			G	7			X																		
BI3,			G	8			X																		
BI5, RTN			G	9			X																		
BI5,			G	10			X																		
N/C			G																						
BI7,			G	12			X																		
BI7, RTN			G	13			X																		

J5A-3 -(Block) IBM 5353868 (B)
(Pin) IBM 5362301

IOP-IN (-3)

CODE IDENT. NO.	DWG. SIZE	CIU EXT J5A-3
17921	A	SHEET 1 of 2

FUNCTION	Ref. Des.	Part Number/Value	Section	Pin No.	Not Used In CIU		J5B-3 SAME PIN
J5B-3 D2			D	2	*		X
J5B-3 D3			D	3	*		X
BO0,			D	4			X
BO1, RTN			D	5			X
BO2,			D	6			X
BO2, RTN			D	7			X
BO4, RTN			D	8			X
BO4,			D	9			X
BO6, RTN			D	10			X
BO6,			D	11			X
J5B-3 D12			D	12	*		X
J5B-3 D13			D	13	*		X
J5B-3 J2			J	2	*		X
J5B-3 J3			J	3	*		X
BI0,			J	4			X
BI0, RTN			J	5			X
BI2,			J	6			X
BI2, RTN			J	7			X
BI4, RTN			J	8			X
BI4,			J	9			X
BI6, RTN			J	10			X
BI6,			J	11			X
J5B-3 J12			J	12	*		X
J5B-3 J13			J	13	*		X

J5A-3- (Block) IBM 5353868 (B)
(Pin) IBM 536230!

IOP - IN (-3)

CODE IDENT NO 17231

DEC SIZE A

CIU EXT J5A-3

SHEET 2 of 2

NOTE:
ALL RTN's CONNECT TO CIU SYSTEM GND.

FUNCTION	Ref. Des.	Part Number/Value	Section	Pin No.	Not Used In CIU	J5A-1 PIN																		
PO$_\phi$ RTN			B	2			X			B	D		2		B	E	5	)	T	P				
PO$_\phi$			B	3			X			B	D		2		B	2	4	)						
BO1$_\phi$ RTN			B	4			X			B	D		2		A	2	7	)	T	P				
BO1$_\phi$			B	5			X			B	D		2		A	2	9	)						
N/C			B	6																				
BO3$_\phi$ RTN			B	7			X			B	D		2		A	3	8	)	T	P				
BO3$_\phi$			B	8			X			B	D		2		A	3	0	)						
BO5$_\phi$ RTN			B	9			X			B	D		2		A	3	7	)	T	P				
BO5$_\phi$			B	10			X			B	D		2		A	3	1	)						
N/C			B	11																				
BO7$_\phi$			B	12			X			B	D		2		A	3	4	)	T	P				
BO7$_\phi$ RTN			B	13			X			B	D		2		A	2	8	)						
PI$_\phi$ RTN			G	2			X			B	D		3		B	E	4	)	T	P				
PI$_\phi$			G	3			X			B	D		3		B	E	2	)						
BI1$_\phi$ RTN			G	4			X			B	D		3		A	3	8	)	T	P				
BI1$_\phi$			G	5			X			B	D		3		A	3	4	)						
CIU SYSTEM GND			G	6			X	B	D		1		A		4	6								
BI3$_\phi$ RTN			G	7			X			B	D		3		A	E	8	)	T	P				
BI3$_\phi$			G	8			X			B	D		3		A	E	2	)						
BI5$_\phi$ RTN			G	9			X			B	D		3		A	E	8	)	T	P				
BI5$_\phi$			G	10			X			B	D		3		A	E	4	)						
N/C			G	11																				
BI7$_\phi$			G	12			X			B	D		3		B	3	6	)	T	P				
BI7$_\phi$ RTN			G	13			X			B	D		3		B	3	8	)						

ORIGINAL PAGE IS OF POOR QUALITY

J5B-1 -(Block) IBM 5353867 (A)
(Pin) IBM 5362301

IOP - OUT (-1)

CODE IDENT NO 17931	DEG. SIZE A	CIU EXT J5B-1
		SHEET 1 of 2

FUNCTION	Part Number/Value / Ref. Des.	Section	Pin No.	Not Used In CIU		J5A-1 Same Pin												
N/C		D	2															
N/C		D	3															
BO0Φ		D	4			/		B	D		2		A	5	}	T	P	
BO1Φ RTN		D	5			/		B	D		2		A	3	)			
BO2Φ		D	6					B	D		2		A	6	}	T	P	
BO2Φ RTN		D	7			·		B	D		2		A	4	)			
BO4Φ RTN		D	8			·		B	D		2		A	3	}	T	P	
BO4Φ		D	9			/		B	D		2		A	7	)			
BO6Φ RTN		D	10					B	D		2		A	4	}	T	P	
BO6Φ		D	[illegible]			·		B	D		2		A	8	)			
J5A-1 D12		D	[illegible]	*		·												
J5A-1 D13		D	[illegible]	*		·												
N/C		J	[illegible]															
N/C		J	[illegible]															
BIΦΦ		J	[illegible]			/		B	D		3		A	3	3	}	T	P
BIΦΦ RTN		J	5			·		B	D		3		A	3	7	)		
BI2Φ		J	6			·		B	D		3		A	5	1	}	T	P
BI2Φ RTN		J	7					B	D		3		A	5	3	)		
BI4Φ RTN		J	8			·		B	D		3		B	1	9	}	T	P
BI4Φ		J	9					B	D		3		B	1	7	)		
BI6Φ RTN		J	[illegible]			·		B	D		3		B	3	7	}	T	P
BI6Φ		J	11			·		B	D		3		B	3	5	)		
J5A-1 J12		J	[illegible]	*														
J5A-1 J13		J	[illegible]	*														

ORIGINAL PAGE IS OF POOR QUALITY

J5B-1 - (Block) IBM 5353867 (A)
(Pin) IBM 5362301

IOP - OUT (-1)

CODE IDENT NO.	DWG SIZE	CIU EXT J5B-1
[illegible]	A	SHEET 2 of 2

FUNCTION	Ref. Des.	Part Number/Value	Section	Pin No.	Not Used In CIU	J5A-2 SAME PIN																		
OP IN RTN			B	2		X		B	D		4		A	2	0	)	T	P						
OP IN			B	3		X		B	D		4		A	1	B	)								
ADR IN RTN			B	4		X		B	D		4		A		9	)	T	P						
ADR IN			B	5		X		B	D		4		A	1	2	)								
N/C			B	6																				
SEL IN RTN			B	7		/		B	D		4		A		9		T	P						
SEL IN			B	8		X																		
ADR OUT RTN			B	9		/		B	D		2		B	2	5	)	T	P						
ADR OUT			B	10		X		B	D		2		B	2	2	)								
N/C			B	11																				
SUP OUT			B	12		X		B	D		1		B	3	2	)	T	P						
SUP OUT RTN			B	13		X		B	D		1		B	3	3	)								
J5A-2 G2			G	2	*	X																		
J5A-2 G3			G	3	*	X																		
J5A-2 G4			G	4	*	X																		
J5A-2 G5			G	5	*	X																		
J5A-2 G6			G	6	*	X		B	D		2		A		3									
J5A-2 G7			G	7	*	X																		
J5A-2 G8			G	8	*	X																		
J5A-2 G9			G	9	*	X																		
J5A-2 G10			G	10	*	X																		
N/C			G	11																				
HLD OUT			G	12		X		B	D		2		B	3	1	)	T	P						
HLD OUT RTN			G	13		X		B	D		2		B	3	3	)								

J5B-2 -(Block) IBM 5353867 (A)
(Pin) IBM 5362901

IOP - OUT (-2)

CODE IDENT NO 17801

DWG. SIZE A

CIU EXT J5B-2

SHEET 1 of 2

FUNCTION	Ref. Des.	Part Number/Value	Section	Pin No.	Not Used In CIU	J5A-2 SAME PIN															
N/C			E	C																	
N/C			E	G																	
STA IN			E	4		X		B	D		4		A	1	6	⟩	T	P			
STA IN RTN			E	5		X		B	D		4		A	1	1	⟩					
SRV IN			E	6		X		B	D		4		A	1	4	⟩	T	P			
SRV IN RTN			E	7		X		B	D		4		A	1	1	⟩					
SEL OUT RTN			E	8		X		B	D		4		A	3	4	⟩	T	P			
SEL OUT			E	9		"		B	D		4		A	1	0	⟩					
CMD OUT RTN			E	10		X		B	D		1		B	3	3	⟩	T	P			
CMD OUT			E			X		B	D		1		B	3	0	⟩					
SRV OUT PTN			E	12		X		B	D		1		C	2	3	⟩	T	P			
SRV OUT			E	13		X		B	D		1		B	3	1	⟩					
A OUT			J	2		X		E	D		2		B	3	2	⟩	T	P			
A OUT RTN			J	3		X		5	D		2		B	3	3	⟩					
J5A-2 J4			J	4	*	X															
J5A-2 J5			J	5	*	X															
J5A-2 J6			J	6	*	X															
J5A-2 J7			J	7	*	X															
J5A-2 J8			J	8	*	X															
J5A-2 J9			J	9	*	X															
J5A-2 J10			J	10	*	X															
J5A-2 J11			J	11	*	X															
OP OUT RTN			J	12		X		B	D		2		B	4	6	⟩	T	P			
OP OUT			J	13		X		B	D		2		B	4	7	⟩					

J5B-2 - (Block) IBM 5353867 (A)
(Pin) IBM 5362301

IOP - OUT (-2)

CODE IDENT. NO. 17761	DEG. SIZE A	CIU EXT J5B-2
		SHEET 2 of 2

FUNCTION	Ref. Des.	Part Number/Value	Section	Pin No.	Not Used In CIU	J5A-3 SAME PIN																				
P0, RTN			B	2		X		B	D		1		B	2	8	}	T	P								
P0,			B	3		X		B	D		1		B	2	9	)										
P01, RTN			B	4		X		B	D		1		A	2	7	}	T	P								
B01,			B	5		X		B	D		1		-	2	9	)										
N/C			B	6																						
B03, RTN			B	7		X		B	D		1		A	2	3	}	T	P								
B03,			B	8		X		B	D		1		A	3	0	)										
B05, RTN			B	9		X		B	D		1		A	2	7	}	T	P								
B05,			B	10		X		B	D		1		A	3	1	)										
N/C			B	11																						
B07,			B	12		X		B	D		1		A	3	2	}	T	P								
B07, RTN			B	13		X		B	D		1		A	2	8	)										
PI, RTN			G	2		X		B	D		3		B	5	2	}	T	P								
PI,			G	3		X		B	D		3		B	5	1	)										
BI1, RTN			G	4		X		B	D		3		A	2	4	}	T	P								
BI1,			G	5		X		B	D		3		A	1	8	)										
CIU SYSTEM GND			G	6		X		B	D		2		A		4											
BI3, RTN			G	7		X		B	D		3		A	3	6	}	T	P								
BI3,			G	8		X		B	D		3		A	3	0	)										
BI5, RTN			G	9		X		B	D		3		A	4	4	}	T	P								
BI5,			G	10		X		B	D		3		A	4	8	)										
N/C			G	11																						
BI7,			G	12		X		B	D		3		A	2	2	}	T	P								
BI7, RTN			G	13		X		B	D		3		A	2	6	)										

J5B-3 -(Block) IBM 5353867(A)
(Pin) IBM 5362301

IOP - OUT (-3)

CODE IDENT. NO.	DEG. SIZE	CIU EXT J5B-3
17961	A	SHEET 1 of 2

FUNCTION	Ref. Des.	Part Number/Value	Section	Pin No.	Not Used In CIU	J5A-3 SAME PIN																		
J5A-3 D2			D	E	*	X																		
J5A-3 D3			D	G	*	X																		
BOΦ,			D	H		X		B	D		1		A	5	}	T	P						
BOΦ, RTN			D	5		X		B	D		1		A	3	}									
BO2,			D	6		X		B	D		1		A	6	}	T	P						
BO2, RTN			D	7		X		B	D		1		A	4	}									
BO4, RTN			D	8		X		B	D		1		A	3	}	T	P						
BO4,			D	9		X		B	D		1		A	7	}									
BO6, RTN			D	10		X		B	D		1		A	4	}	T	P						
BO6,			D	11		X		B	D		1		A	8	}									
J5A-3 D12			D	12	*	X																		
J5A-3 D13			D	J	*	X																		
J5A-3 J2			J	E	*	X																		
J5A-3 J3			J	G	*	X																		
BIΦ,			J	H		X		B	D		3		A	1	7	}	T	P						
BIΦ, RTN			J	5		X		B	D		3		A	2	3	}								
BI2,			J	6		X		B	D		3		A	2	9	}	T	P						
BI2, RTN			J	7		X		B	D		3		A	3	5	}								
BI4, RTN			J	8		X		B	D		3		A	4	3	}	T	P						
BI4,			J	9		X		B	D		3		A	4	7	}								
BI6, RTN			J	10		X		B	D		3		A	2	5	}	T	P						
BI6,			J	K		X		B	D		3		A	2	1	}								
J5A-3 J12			K	L	*	X																		
J5A-3 J13			K	M	*	X																		

J5B-3-(Block) IBM 5353867 (A)
(Pin) IBM 5362301

IOP-OUT (-3)

CODE IDENT NO.	DEC. SIZE	CIU EXT J5B-3
17961	A	SHEET 2 of 2

NOTE:
ALL RTN's CONNECT TO CIU SYSTEM GND.

FUNCTION	Ref. Des.	Part Number/Value	Section	Pin No.	Not Used In CIU									
TPOφ RTN			B	2		B	D	2	B	2	7	}	T	P
TPOφ			B	3		B	D	2	B	2	8	)		
TBO1φ RTN			B	4		B	D	2	A	4	5	}	T	P
TBO1φ			B	5		B	D	2	A	4	7	)		
N/C			B	6										
TBO3φ RTN			B	7		B	D	2	A	4	6	}	T	P
TBO3φ			B	8		B	D	2	A	4	8	)		
TBO5φ RTN			B	9		B	D	2	A	4	5	}	T	P
TBO5φ			B	10		B	D	2	A	4	9	)		
N/C			B	11										
TBO7φ			B	12		B	D	2	A	5	0	}	T	P
TBO7φ RTN			B	13		B	D	2	A	4	6	)		
TPIφ RTN			G	2		B	D	3	B	5	4	}	T	P
TPIφ			G	3		B	D	3	B	5	0	)		
TBI1φ RTN			G	4		B	D	3	A	3	8	}	T	P
TBI1φ			G	5		B	D	3	A	3	2	)		
CIU SYSTEM GND			G	6		B	D	2	A	4	5			
TBI3φ RTN			G	7		B	D	3	A	5	4	}	T	P
TBI3φ			G	8		B	D	3	A	5	0	)		
TBI5φ RTN			G	9		B	D	3	B	2	0	}	T	F
TBI5φ			G	10		B	D	3	B	1	6	)		
N/C			G	11										
TBI7φ			G	12		B	D	3	B	3	4	}	T	P
TBI7φ RTN			G	13		B	D	3	B	3	6	)		

J6-1 -(Block) IBM 5353868(B)
(Pin) IBM 5362301

TEST IOP (-1)

CODE IDENT. NO. 17981 | DWG. SIZE A | CIU EXT J6-1 | SHEET 1 of 2

FUNCTION	Ref. Des.	Part Number/Value	Section	Pin No.	Not Used In CIU								
N/C			D	2									
N/C			D	3									
TBOΦφ			D	4		B	D	2	A	9		T	P
TBOΦφ RTN			D	5		B	D	2	A	1	3		
TBO2φ			D	6		B	D	2	A	1	0	T	P
TBO2φ RTN			D	7		B	D	2	A	1	4		
TBO4φ RTN			D	8		B	D	2	A	1	3	T	P
TBO4φ			D	9		B	D	2	A	1	1		
TBO6φ RTN			D	10		B	D	2	A	1	4	T	P
TBO6φ			D	11		B	D	2	A	1	2		
N/C			D	12									
N/C			D	13									
N/C			J	2									
N/C			J	3									
TBIΦφ			J	4		B	D	3	A	3	1	T	P
TBIΦφ RTN			J	5		B	D	3	A	3	7		
TBI2φ			J	6		B	D	3	A	4	9	T	P
TBI2φ RTN			J	7		B	D	3	A	5	3		
TBI4φ RTN			J	8		B	D	3	B	1	9	T	P
TBI4φ			J	9		B	D	3	B	1	5		
TBI6φ RTN			J	10		B	D	3	B	3	7	T	P
TBI6φ			J	11		B	D	3	B	3	3		
N/C			J	12									
N/C			J	13									

J6-1 - (Block) IBM 5353868 (B)
(Pin) IBM 5362301

TEST IOP (-1)

CODE IDENT. NO. 17981 | DWG SIZE A | CIU EXT J6-1

SHEET 2 of 2

FUNCTION	Ref. Des. / Part Number/Value	Section	Pin No.	Not Used In CIU										
TOP IN RTN		B	2		B	D	4		A	2	4	T	P	
TOP IN		B	3		B	D	4		A	2	3			
TADR IN RTN		B	4		B	D	4		A	1	3	T	P	
TADR IN		B	5		B	D	4		A	1	7			
N/C		B	6											
TSEL IN RTN		B	7		B	D	4		A	1	3	T	P	
TSEL IN		B	8		B	D	4		A	1	5			
TADR OUT RTN		B	9		B	D	2		B	3	3	T	P	
TADR OUT		B	10		B	D	2		B	3	0			
N/C		B	11											
TSUP OUT		B	12		B	D	1		B	5	0	T	P	
TSUP OUT RTN		B	13		B	D	1		B	5	1			
N/C		G	2											
N/C		G	3											
N/C		G	4											
N/C		G	5											
CIU SYSTEM GNL		G	6		B	D	2		A	4	6			
N/C		G	7											
N/C		G	8											
N/C		G	9											
N/C		G	10											
N/C		G	11											
THLD OUT		G	12		B	D	2		B	4	9	T	P	
THLD OUT RTN		G	13		B	D	2		B	4	5			

J6-2 -(Block) IBM 5353868(8)
(Pin) IBM 5362301

TEST IOP (-2)

CODE IDENT. NO. 17961 | DWG. SIZE A | CIU EXT J6-2 | SHEET 1 of 2

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FUNCTION	Part Number/Value / Ref. Des.	Section	Pin No.	Not Used in CIU												
N/C		D	2													
N/C		D	3													
TSTA IN		D	4			B	D		4		A	2	1	}	T	P
TSTA IN RTN		D	5			B	D		4		A	2	2			
TSRV IN		D	6			B	D		4		A	1	9	}	T	P
TSRV IN RTN		D	7			B	D		4		A	2	0			
TSEL OUT RTN		D	8			B	D		2		B	2	5	}	T	P
TSEL OUT		D	9			B	D		2		B	2	3			
TCMD OUT RTN		D	10			B	D		1		B	5	1	}	T	P
TCMD OUT		D	11			B	D		1		B	4	8			
TSPV OUT RTN		D	12			B	D		1		B	5	1	}	T	P
TSRV OUT		D	13			B	D		1		B	4	9			
TA OUT		J	2			B	D		2		B	5	0	}	T	P
TA OUT RTN		J	3			B	D		2		B	4	6			
N/C		J	4													
N/C		J	5													
N/C		J	6													
N/C		J	7													
N/C		J	8													
N/C		J	9													
N/C		J	10													
N/C		J	11													
TOP OUT RTN		J	12			B	D		2		B	4	6	}	T	P
TOP OUT		J	13			B	D		2		B	4	8			

J6-2 – (Block) IBM 5353868(B)
(Pin) IBM 5362301

TEST IOP (-2)

CODE IDENT. NO 17981	DEG. SIZE A	CIU EXT J6-2 / SHEET 2 of 2

FUNCTION	Ref. Des.	Part Number/Value	Section	Pin No.	Not Used In CIU																							
TPO, RTN			B	2			B	D		1		B	4	5	}	T	P											
TPO,			E	3			B	D		1		B	4	7	}													
TBO1, RTN			E	4			B	D		1		A	4	5	}	T	P											
TBO1,			E	5			B	D		1		A	4	7	}													
N/C			B	6																								
TBO3, RTN			B	7			B	D		1		A	4	6	}	T	P											
TBO3,			E	8			B	D		1		A	4	8	}													
TBO5, RTN			E	9			B	D		1		A	4	5	}	T	P											
TBO5,			E	10			B	D		1		A	4	9	}													
N/C			E	11																								
TBO7,			E	12			B	D		1		A	5	0	}	T	P											
TBO7, RTN			E	13			B	D		1		A	4	6	}													
TPI, RTN			G	2			B	D		3		B	5	3	}	T	P											
TPI,			G	3			B	D		3		B	4	9	}													
TBI, RTN			G	4			B	D		3		A	2	4	}	T	P											
TBI,			G	5			B	D		3		A	1	6	}													
CIU SYSTEM GND			G	6			B	D		2		B	4	5														
TBI3, RTN			G	7			B	D		3		A	3	6	}	T	P											
TBI3,			G	8			B	D		3		A	2	8	}													
TBI5, RTN			G	9			B	D		3		A	4	4	}	T	P											
TBI5,			G	10			B	D		3		A	4	6	}													
N/C			G	11																								
TBI7,			G	12			B	D		3		A	2	0	}	T	P											
TBI7, RTN			G	13			B	D		3		A	2	6	}													

J6-3 -(Block) IBM 5353868(B)
(Pin) IBM 5362301

TEST IOP (-3)

CODE IDENT. NO.	DEG. SIZE	CIU EXT J6-3
17961	A	SHEET 1 of 2

FUNCTION	Ref. Des. / Part Number/Value	Section	Pin No.	Not Used In CIU												
N/C		D	2													
N/C		D	3													
TBOΦ,		D	4			B	D		1		A	9		}	T	P
TBOΦ, RTN		D	5			B	D		1		A	1	3			
TBO2,		D	6			B	D		1		A	1	0	}	T	P
TBO2, RTN		D	7			B	D		1		A	1	4			
TBO4, RTN		D	8			B	D		1		A	1	3	}	T	P
TBO4,		D	9			B	D		1		A	1	1			
TBO6, RTN		D	10			B	D		1		A	1	4	}	T	P
TBO6,		D	11			B	D		1		A	1	2			
N/C		D	12													
N/C		D	13													
N/C		J	2													
N/C		J	3													
TBIΦ,		J	4			B	D		3		A	1	5	}	T	P
TBIΦ, RTN		J	5			B	D		3		A	2	3			
TBI2,		J	6			B	D		3		A	2	7	}	÷	P
TBI2, RTN		J	7			B	D		3		A	3	5			
TBI4, RTN		J	8			B	D		3		A	4	3	}	T	P
TBI4,		J	9			B	D		3		A	4	5			
TBI6, RTN		J	10			B	D		3		A	2	5	}	T	P
TBI6,		J	11			B	D		3		A	1	9			
N/C		J	12													
N/C		J	13													

J6-3 - (Block) IBM 5353868(B)
(Pin) IBM 5362301

TEST IOP (-3)

CODE IDENT. NO. 17931	DWG. SIZE A	CIU EXT J6-3 / SHEET 2 of 2

FUNCTION	Ref. Des.	Part Number/Value: PTOOCE-12-10SX(SR)
		J7
TIME IN +	A	BD 6 B4 } TP
TIME IN -	B	BD 6 B6 }
CHASSIS GND	C	
TIME ERROR +	D	BD 5 B27 } TP
TIME ERROR -	E	BD 5 B29 }
N/C	F	
N/C	G	
CHASSIS GND	H	
8MHZ CK +	J	BD 17 A8 } TP
8MHZ CK -	K	BD 17 A10 }

J7 - PTOOCE-12-10SX (SR)

TIME

CODE IDENT. NO.	DWG. SIZE	CIU EXT J7
17961	A	SHEET 1 of 1

FUNCTION	Ref. Des. J8 — Part Number/Value TEI-14949-BJ79								
SUP BIØ +	CENTER PIN	B	D	8	A	2	4		
SUP BIØ −	ISOLATED RING	B	D	8	A	2	6	T	W L
CHASSIS GND	CONNECTOR HOUSING							72-2	

J8 - TEI - 14949 - BJ79

SUPERVISORY BUS

CODE IDENT. NO. 17981	DWG. SIZE A	CIU EXT J8
		SHEET 1 of 1

FUNCTION	Ref. Des. / Part Number/Value: J9 TEI-14949-BJ79								
RPLY BIϕ +	CENTER PIN	B	D	8	B	4	T	W	C
RPLY BIϕ −	ISOLATED RING	B	D	8	B	6		72	2
CHASSIS GND	CONNECTOR HOUSING								

J9- TEI-14949-BJ79

REPLY BUS

CODE IDENT. NO. 17981

DWG. SIZE A

CIU EXT J9

SHEET 1 of 1

FUNCTION	Ref. Des.	Part Number/Value: PTOOCE-14-5S(SR)
		J10
+28 VDC +	A	SW2-1
+28 VDC (RTN) -	B	SW2-4
N/C	C	
N/C	D	
CHASSIS GND	E	

18 AWG

J10 - PTOOCE-14-5S (SR)

POWER

CODE IDENT. NO.	DWG. SIZE	
17981	A	CIU EXT J10
		SHEET 1 of 1

SECTION IV

DATA INTERFACE UNIT

TABLE OF CONTENTS

1.0 DIU FUNCTIONAL CHARACTERISTICS

The Data Interface Unit (DIU) supplies the input/output interfaces between the Computer Interface Unit (CIU) and the user subsystems of the Data Management System. The DIU receives serial command messages from the CIU on the Supervisory Bus, and transmits reply data and error status information to the CIU on a separate Reply Bus. Up to 32 DIU's may be interfaced with each CIU. The five-bit unit address for each DIU is controlled by a front-panel thumbwheel switch. The block diagram for the DIU interfaces is shown in Figure 1.0-1.

Data Bus Operation

Each command message from the CIU contains an Address word (A-WD), a Word Count Word (WC-WD), followed by the number of Data Words (D-WD) specified by the WC-WD for write commands, or blank words for read commands. The responding DIU replies with a 12-bit sync word, followed by blank words or D-Words, and an Error Status Word (ES-WD). The Data Bus word formats are shown in Figure 1.0-2, and the ES-WD bit assignments in Figure 1.0-3.

The five-bit OP Code Field is decoded by the addressed DIU for execution if no errors are detected in the message. The OP Code functions are as follows:

OP CODE	COMMAND FUNCTION
03_8	Read RI
07	Write RO
12	Read Error Status
13	Read AI Deltas (AI_0 - AI_{63})
15	Write AI Deltas (AI_0 - AI_{63})
20	Write DI Monitor Contol

(Continued)

OP CODE	COMMAND FUNCTION
21	Read DI
22	Read DI Changes
23	Read DI Monitor Control
25	DIU to DIU Transfer
30	Write DO
31	Read DO Status
32	Read AI
33	Read AI Deltas (AI_{64} - AI_{127})
34	Read AI Exceeding Delta
35	Write AI Deltas (AI_{64} - AI_{127})
36	Write AO
37	Reset DIU

The six-bit channel address field is used to select RI/RO channels, and as a starting address for DI, DO, AI, and AO address sequences. For the latter case, if the word count exceeds the number of channels or groups remaining after the starting address, the DIU address counters will wrap around to the first address implemented and continue until the word count is satisfied.

The addressed DIU tests the Supervisory Bus message for the error conditions shown in Figure 1.0-3. With the exception of D-word parity errors on Write RO commands, detection of an error condition will cause the DIU to terminate execution of the instruction, set the appropriate bit in the Error Status word, transmit the Error Status word to the CIU to complete the reply, and stop the RI/RO clock where applicable. For Write RO D-word parity errors, the DIU will transmit the incorrect data to the subsystem.

Discrete Input Functions

The DIU will interface up to 128 Discrete Inputs, arranged in 8 groups of 16 DI's. Associated with the DI interface modules is control logic for testing DI's for changes. This logic contains a 128-bit memory (DI Status Table) for comparison data, a 16-bit control register (DI monitor control) to enable/disable the compare function by byte, and a change history/change status register to flag changes by group. When power is applied to the DIU, the Status Table is set to all zero's, and the Monitor Control register cleared to all zero's (enable). A scan of all DI groups implemented is initiated and changes are flagged by setting the appropriate bit in the Change History register. The Change Status register and the Status Table are updated only during a Read DI Changes instruction. The scan function is inhibited during the execution of Read DI, Write DI Monitor Control, and Read DI Monitor Control instructions.

Discrete Output Functions

The DIU has the capability of outputting up to 128 DO's, in increments of 16 DO's per group. Each DO module contains a storage register for maintaining the status of the DO's between Write DO instructions, and a read register for monitoring the DO's by the Read DO Status instruction. When power is applied to the DIU, all DO's implemented are turned off until the first valid Write DO instruction is received.

Record In/Record Out Functions

The DIU contains up to 8 RI/RO interfaces. Data transfers are controlled over three twisted shielded pair cable. The RO line outputs continuous bi-phase data as received from the Supervisory Bus. The WC word prefix and parity bits are modified before transmission. The clock line ouputs a gated 4 MHz clock to control all data transfers. For Read RI instructions,

the DIU inserts a blank word into the reply to the CIU while receiving the serial RI data. Twelve bit times are allowed after the clock line is activated for the subsystem to respond. If no errors are detected, the word count is decremented by detection of D word prefixes on the RI line until the word count is satisfied.

Analog Output Functions

The DIU contains up to 4 AO modules. The AO's share a common, isolated return, and supply a 0-5 volt output level. The AO digital-to-analog converters are offset by 60 millivolts to accommodate the specified code for 0 volts. The AO's are set to 0 volts when power is applied to the DIU.

Analog Input Functions

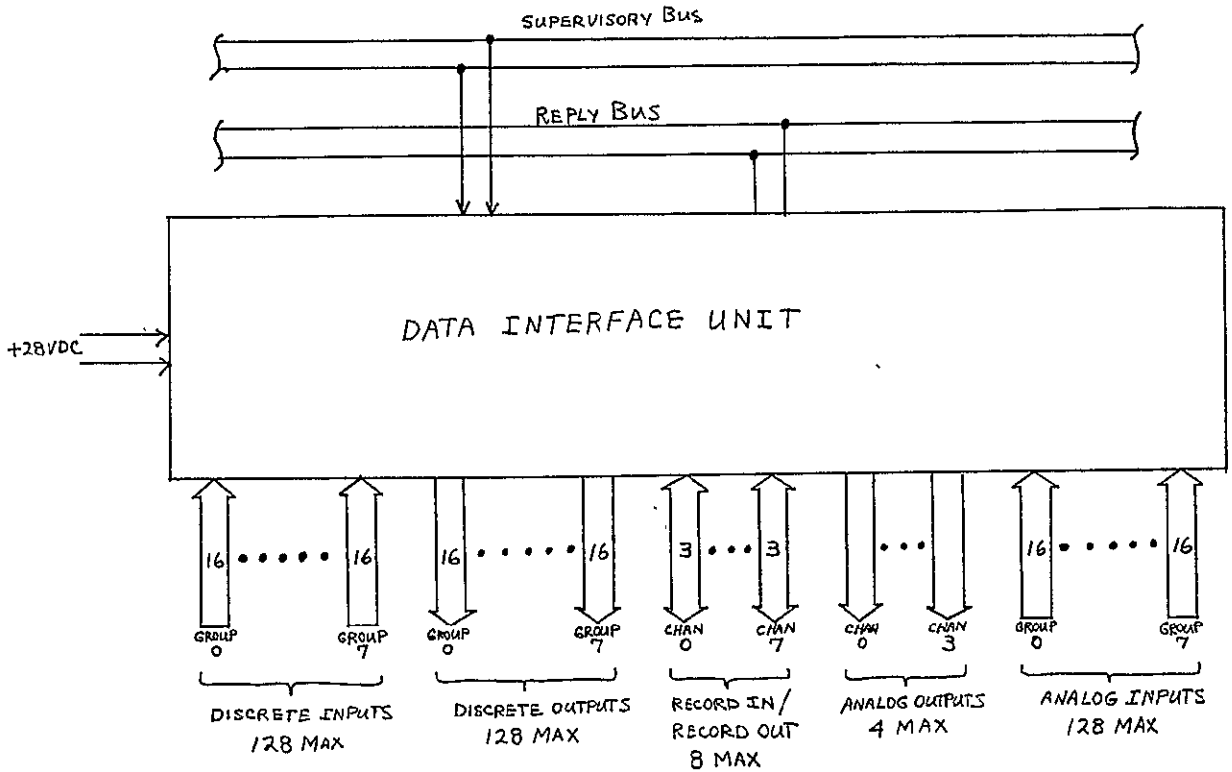
The DIU will accept up to 128 Analog Inputs, in increments of 16 channels. Each input module contains a 16 channel differential multiplexer with overvoltage protection for $\pm$ 32 volts. The DIU utilizes two differential amplifiers and sample-and-hold circuits to compensate for multiplexer settling time. The differential amplifiers contain an automatic calibration loop to compensate for offset drift.

The sample-and-hold outputs are routed to a common analog-to-digital converter. The converter operates at a 2 MHz bit rate and supplies data to the DIU transmitter for Read AI instructions, and to the AI Delta logic for processing.

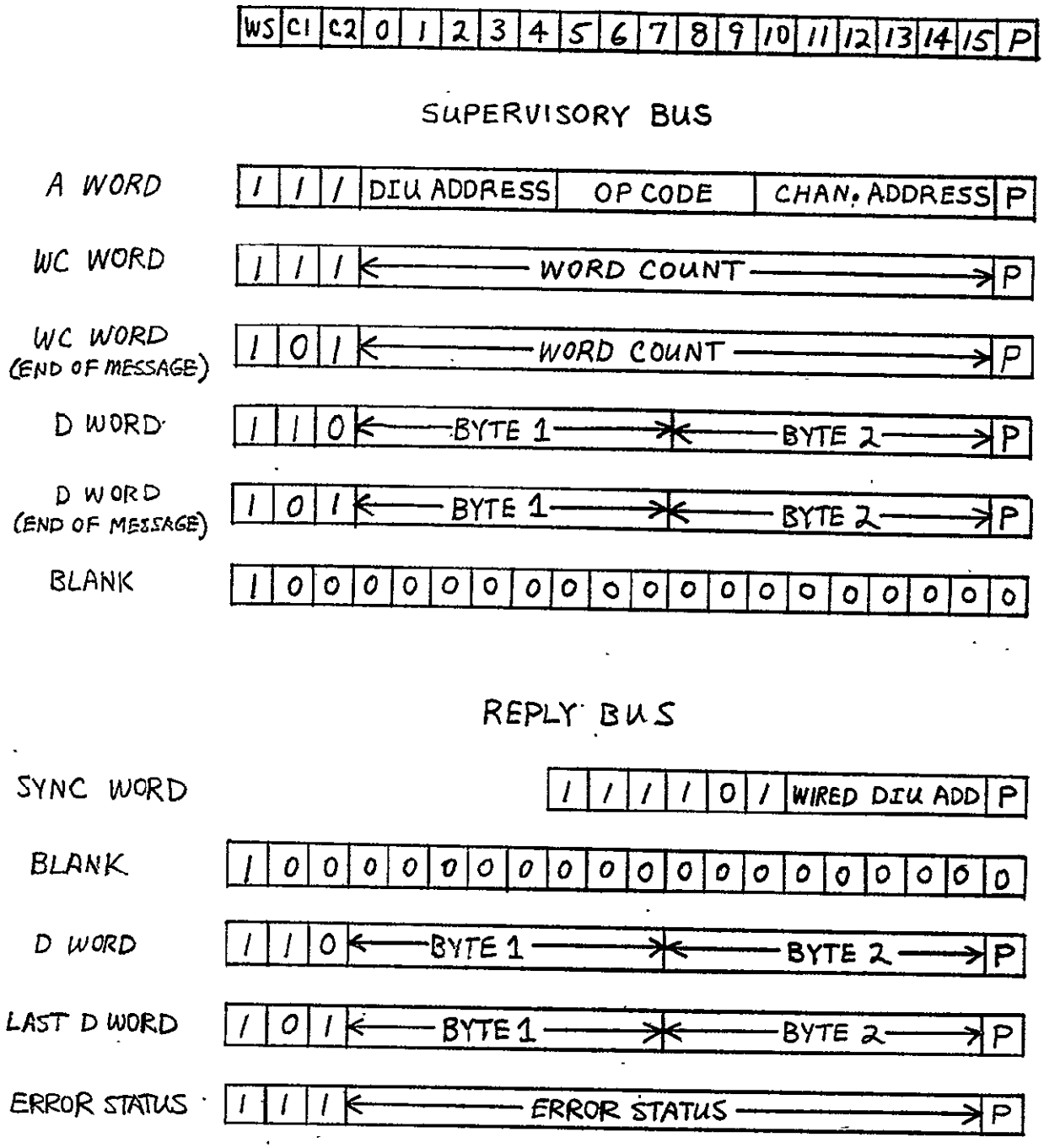
The AI logic contains a semiconductor memory for storing plus and minus deltas for each AI channel, a reference AI value, and a flag bit to indicate exceeding delta conditions for each channel. When power is applied to the DIU, the plus and minus delta values are set to maximum, and the flag bits

reset. A scan of all AI channels implemented is initiated, and each encoded value is tested for an exceeding delta condition. Delta values are loaded and verified by the Write AI Delta and Read AI Delta instructions. As each channel is encoded during the scan operation, its value is subtracted from the reference value stored in memory. Depending on the sign of the subtractor output, a plus or minus delta value is read from memory and compared to the subcontractor output. If an exceeding delta condition is detected, a flag bit for the channel is set, and the current AI value is written in memory for the reference value for succeeding tests.

When a Read AI Exceeding Delta instruction is received, the DIU scans the flag portion of memory, and replies with the current reference value and address for those channels that exceeded delta values. The flag bit for each channel is reset, and scanning of AI channels is resumed. Loading of new delta values also resets the flag bit for each channel specified in the instruction.

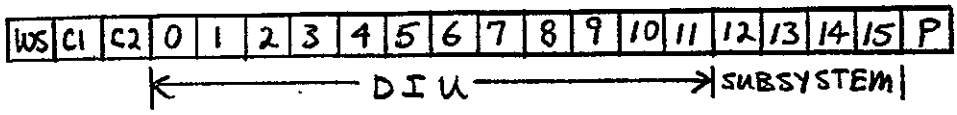


BLOCK DIAGRAM
DIU INTERFACES
FIGURE 1.0-1



DATA BUS WORD FORMATS

FIGURE 1.0-2



0 DIU to DIU Flag

1 Word Sync Error

2 A Word Parity Error

3 Illegal OP Code

4 WC Word Parity Error

5 WC Word Sequence Error

6 D Word Parity Error

7 More than 5 consecutive blank words during data on Sup Bus

8 Word Count Error

9 More than 5 consecutive blank words from Subsystem on RI line

10 No response from Subsystem on RI line

11 Parity Error on RI Error Status Word from Subsystem

12 Word Count Error on RO line

13 Sync Error

14 Parity Error

15 Read Status Register

} From Subsystem

ERROR STATUS WORD
FIGURE 1.0-3

2.0 DIU ELECTRICAL CHARACTERISTICS

POWER INPUT

Input voltage +28 VDC nominal

Normal operation from +22 to +32 VDC

Reverse voltage protection

D. C. isolation between input line and DIU ground

SUPERVISORY BUS

Continuous Manchester Type II Bi-Phase-L data, 2 MHz bit rate

78 ohm input impedance

D. C. isolation between Supervisory Bus and DIU ground

REPLY BUS

Gated Manchester Type II Bi-Phase-L data, 2 MHz bit rate

78 ohm output impedance

Short-circuit protection

Drive capability for 500 ft. of 78 ohm twisted shielded pair cable

D. C. isolation between Reply Bus and DIU ground

DISCRETE INPUTS

Up to 128 Discrete Inputs, in 8 groups of 16 Discrete Inputs

D. C. isolation between each group and DIU ground

Overvoltage protection for $\pm$ 32 volts on each input

2 msec filter on each input

Input Levels:

High Level:

Open: 0

0-6 volts: 0

10-32 volts: 1

Input Impedance: 39K ohms to ground

Low Level:

Open: 0

0-1.3 volts: 0

2.5 - 5 volts: 1

Input Impedance: 39K ohms to ground

Sink-to-ground:

Open: 0

0-1.3 volts: 1

2.5 - 5 volts: 0

Input Impedance: 51K ohms to +5 volts

DISCRETE OUTPUTS

Up to 128 Discrete Outputs, in 8 groups of 16 Discrete Outputs

D. C. isolation between each group and DIU ground

Short circuit protection on each output

External source voltage from +5 to +32 VDC

Output current capability of 50 ma. maximum

Diode suppression for inductive loads

Discrete outputs turned off during power on initialization

RECORD IN/RECORD OUT

Up to 8 RI/RO channels

Each channel contains a continuous data out line (RO), asychronous data in line (RI), and a gated 4 MHz control line (Clock)

Signal lines are transformer isolated, 78 ohm, twisted shielded pairs

Drive capability for up to 50 ft of 78 ohm cable

ANALOG OUTPUTS

Up to 4 Analog Output Channels

Common return for AO channels D. C. isolated from DIU ground

Short circuit protection

Output levels from 0 to +5 volts

0 volt code: 00000011

+5 volt code: 11111100

0.4 percent accuracy from digital input to analog output

Drive capability for 2K ohms to ground

Strap capability for monitoring AO's on AI channels 2-5.

Analog Outputs turned off (0 volts) during power on initialization

ANALOG INPUTS

Up to 128 Analog Input channels, in 8 groups of 16 Analog Inputs

Input impedance 10 Megohms minimum, shunted by 50 picofarads maximum

Input voltage range from 0 to +5 volts

0 volt code: 00000011

+5 volt code: 11111100

Overvoltage protection for $\pm$ 32 volts on each input

Adjacent channel isolation of 100 Megohms minimum, shunted by 5 picofarads maximum

Common mode rejection of 60 db minimum for 5.0 volts RMS, from DC to 400 Hz.

End-to-end three sigma error of $\pm$ 1 LSB maximum

AI channels have 8 bit resolution, with an encoding rate of 2 MBPS

High and low calibration inputs, with strap capabilities on AI channels 0 and 1

High level output code: 10101010

Low level output code: 01010101

3.0 DIU MECHANICAL CONFIGURATION

The DIU is packaged in a standard 19 inch pull out drawer. All input-output connectors are mounted on the rear panel. The functions for each connector are listed in Figure 3.0-1.

The front panel contains control switches, displays, and test points as follows:

Control Switches

POWER: Switches + 28 VDC primary power to the DIU power supply.

DIU ADDRESS: Two-digit octal thumbwheel to select DIU unit address, 00_8 - 37_8.

WORD SELECT: Selects A-Word, Error Status Word, Discrete Inputs, or Discrete Outputs for the Word Display.

GROUP SELECT: Selects 1 of 8 DI or DO groups for the Word Display.

MODULARITY SELECT: Selects AI's, RI/RO, DI's, or DO's for the Modularity Display.

Displays

WORD DISPLAY: 16 lamp display for functions selected by the Word Select and Group Select switches.

MODULARITY: 8 lamp display to indicate unit configuration for module types selected by the Modularity Select Switch.

RI/RO CLOCK: 8 lamp display to indicate activation of 1 of 8 RI/RO clocks. Lamp drivers are pulsed to provide visibility during transient conditions.

WORD SYNC: Indicates presence of WS bit on Supervisory Bus. Pulsed lamp driver.

WORD SYNC ERROR: Indicates WS = 0 on Supervisory Bus. Lamp driver is pulsed and turns off WORD SYNC display.

ERROR DETECT: Pulsed indication of error condition during addressed message on Supervisory Bus.

ADDRESS DETECT: Pulsed indication of DIU Address detection.

Test Points

WORD SYNC: Positive pulse coincident with WS-bit of DIU internal timing.

SUP BUS: Bi-phase data from DIU Supervisory Bus Receiver.

SUP NRZ: NRZ data from DIU Supervisory Bus Receiver.

A-WORD TIME: Negative pulse from mid-point of the C2-bit to the end of the parity bit of A-words on the Supervisory Bus.

ADD DET: Negative 125 nsec. pulse during B4 bit of addressed A-words.

DI SCAN SYNC: Negative pulse coincident with C2 bit. Pulse indicates addressing of DI Group O each word time during DI scan operations.

AI SCAN SYNC: Negative 250 nsec pulse coincident with second half of the WS-bit. Pulse indicates addressing of AI Channel 0 during AI scan operation. The pulse occurs every 64 word times with a full complement of AI modules.

REPLY BUS: Bi-phase data from DIU Reply Bus Transmitter.

REPLY NRZ: NRZ data from DIU Reply Bus Transmitter.

CLOCK: 2 MHz square-wave clock, positive during first half of each bit time.

The DIU electronics are packaged on single-connector and double-connector printed-circuit boards. Card location is shown in Figure 3.0-2. Before removing or inserting any of the boards, the power to the DIU and any attached subsystems or test fixtures should be removed.

DIU REAR PANEL CONNECTORS

J1 DISCRETE INPUT, GROUP 0,1
J2 DISCRETE INPUT, GROUP 2,3
J3 DISCRETE INPUT, GROUP 4,5
J4 DISCRETE INPUT, GROUP 6,7
J5 DISCRETE OUTPUT, GROUP 0,1
J6 DISCRETE OUTPUT, GROUP 2,3
J7 DISCRETE OUTPUT, GROUP 4,5
J8 DISCRETE OUTPUT, GROUP 6,7
J9 ANALOG INPUT, CHANNEL 0-15
J10 ANALOG INPUT, CHANNEL 16-31
J11 ANALOG INPUT, CHANNEL 32-47
J12 ANALOG INPUT, CHANNEL 48-63
J13 ANALOG INPUT, CHANNEL 64-79
J14 ANALOG INPUT, CHANNEL 80-95
J15 ANALOG INPUT, CHANNEL 96-111
J16 ANALOG INPUT, CHANNEL 112-127
J17 ANALOG OUTPUT, CHANNEL 0-3
J18 RECORD IN/RECORD OUT, CHANNEL 0
J19 RECORD IN/RECORD OUT, CHANNEL 1
J20 RECORD IN/RECORD OUT, CHANNEL 2
J21 RECORD IN/RECORD OUT, CHANNEL 3
J22 RECORD IN/RECORD OUT, CHANNEL 4
J23 RECORD IN/RECORD OUT, CHANNEL 5
J24 RECORD IN/RECORD OUT, CHANNEL 6
J25 RECORD IN/RECORD OUT, CHANNEL 7
J26 +28 VDC PRIMARY POWER
J27 SUPERVISORY BUS
J28 REPLY BUS
J29 115 VAC

Figure 3.0-1

FRONT PANEL

S1	AI Mux 0	3339-002		DA1	DI Module 0	3339-006	DB1
S2	AI Mux 1	3339-002		DA2	DI Module 1	3339-006	DB2
S3	AI Mux 2	3339-002		DA3	DI Module 2	3339-006	DB3
S4	AI Mux 3	3339-002		DA4	DI Module 3	3339-006	DB4
S5	Sample/Hold	3339-011		DA5	DI Module 4	3339-006	DB5
S6	ADC	3339-009		DA6	DI Module 5	3339-018	DB6
S7	AI Mux 4	3339-002		DA7	DI Module 6	3339-006	DB7
S8	AI Mux 5	3339-002		DA8	DI Module 7	3339-018	DB8
S9	AI Mux 6	3339-002					
S10	AI Mux 7	3339-002		DA10	DO Module 0	3339-004	DB10
S11	Guard Amp/Group Select	3339-068		DA11	DO Module 1	3339-004	DB11
S12	AI Mux Address Control	3339-054		DA12	DO Module 2	3339-004	DB12
S13	AI Mem Address Control	3339-056		DA13	DO Module 3	3339-004	DB13
S14	AI Memory	3339-052		DA14	DO Module 4	3339-004	DB14
S15	AI Mem Data Interface	3339-058		DA15	DO Module 5	3339-004	DB15
S16	AI Mem Sequence Control	3339-062		DA16	DO Module 6	3339-004	DB16
S17	AI Mem Function Select	3339-060		DA17	DO Module 7	3339-004	DB17
				DA18	DO Mux Control	3339-066	DB18
S19	AO Module 0,1	3339-020		DA19	DI Mux Control #1	3339-064	DB19
S20	AO Module 2,3	3339-020		DA20	DI Mux Control #2	3339-074	DB20
S21	AO Control	3339-072					
S26	Reply Bus Transmitter	3339-026		DA26	Front Panel Display Logic	3339-076	DB26
S27	Transmit Logic	3339-030		DA27	RI/RO Interface Logic	3339-070	DB27
S28	Receive Logic #1	3339-042		DA28	RI Transmitters	3339-016	DB28
S29	Receive Logic #2	3339-040		DA29	Supervisory Bus & RI/RO Receivers	3339-014	DB29
S30	Receive Logic #3	3339-032		DA30	Timing 1	3339-050	DB30
S31	Receive Logic #4	3339-036					
S32	Reply Sequencer 1	3339-028					
S33	Reply Sequencer 2	3339-034		DA33	Power Supply Converter	3339-024	DB33
S34	Error Status Registers	3339-048					
S35	Error Status 1	3339-046					
S36	Error Status 2	3339-038		DA36	Power Supply Regulator	3339-022	DB36
S37	Timing 2	3339-044					

REAR PANEL

DIU CARD PLACEMENT
FIGURE 3.0-2

J1 DI GROUPS Ø & 1

Pin	Function	Group	Pin	Function	Group
A	DIØ	Ø	a	DI6	1
B	DI1	Ø	b	DI7	1
C	DI2	Ø	c	DI8	1
D	DI3	Ø	d	DI9	1
E	DI4	Ø	e	DI10	1
F	DI5	Ø	f	DI11	1
G	DI6	Ø	g	DI12	1
H	DI7	Ø	h	DI13	1
J	DI8	Ø	i	DI14	1
K	DI9	Ø	j	DI15	1
L	DI10	Ø	k	Isolated Return	1
M	DI11	Ø	m	Chassis Gnd.	
N	DI12	Ø	n	Spare	
P	DI13	Ø	p	Spare	
R	DI14	Ø	q	Spare	
S	DI15	Ø	r	Spare	
T	Isolated Return	Ø	s	DIU Common 1	
U	DIØ	1	t	DIU Common 2	
V	DI1	1			
W	DI2	1			
X	DI3	1			
Y	DI4	1			
Z	DI5	1			

J2 DI GROUPS 2 & 3

Pin	Function	Group	Pin	Function	Group
A	DIØ	2	a	DI6	3
B	DI1	2	b	DI7	3
C	DI2	2	c	DI8	3
D	DI3	2	d	DI9	3
E	DI4	2	e	DI10	3
F	DI5	2	f	DI11	3
G	DI6	2	g	DI12	3
G	DI7	2	h	DI13	3
J	DI8	2	i	DI14	3
K	DI9	2	j	DI15	3
L	DI10	2	k	Isolated Return	3
M	DI11	2	m	Chassis Gnd.	
N	DI12	2	n	Spare	
P	DI13	2	p	Spare	
R	DI14	2	q	Spare	
S	DI15	2	r	Spare	
T	Isolated Return	2	s	DIU Common 1	
U	DIØ	3	t	DIU Common 2	
V	DI1	3			
W	DI2	3			
X	DI3	3			
Y	DI4	3			
Z	DI5	3			

J3 DI GROUPS 4 & 5

Pin	Function	Group	Pin	Function	Group
A	DIØ	4	a	DI6	5
B	DI1	4	b	DI7	5
C	DI2	4	c	DI8	5
D	DI3	4	d	DI9	5
E	DI4	4	e	DI10	5
F	DI5	4	f	DI11	5
G	DI6	4	g	DI12	5
H	DI7	4	h	DI13	5
J	DI8	4	i	DI14	5
K	DI9	4	j	DI15	5
L	DI10	4	k	Isolated Return	5
M	DI11	4	m	Chassis Gnd	
N	DI12	4	n	Spare	
P	DI13	4	p	Spare	
R	DI14	4	q	Spare	
S	DI15	4	r	Spare	
T	Isolated Return	4	s	DIU Common 1	
U	DIØ	5	t	DIU Common 2	
V	DI1	5			
W	DI2	5			
X	DI3	5			
Y	DI4	5			
Z	DI5	5			

J4 DI GROUPS 6 & 7

Pin	Function	Group	Pin	Function	Group
A	DIØ	6	a	DI6	7
B	DI1	6	b	DI7	7
C	DI2	6	c	DI8	7
D	DI3	6	d	DI9	7
E	DI4	6	e	DI10	7
F	DI5	6	f	DI11	7
G	DI6	6	g	DI12	7
H	DI7	6	h	DI13	7
J	DI8	6	i	DI14	7
K	DI9	6	j	DI15	7
L	DI10	6	k	Isolated Return	7
M	DI11	6	m	Chasis Gnd	
N	DI12	6	n	Spare	
P	DI13	6	p	Spare	
R	DI14	6	q	Spare	
S	DI15	6	r	Spare	
T	Isolated Return	6	s	DI Common 1	
U	DIØ	7	t	DI Common 2	
V	DI1	7			
W	DI2	7			
X	DI3	7			
Y	DI4	7			
Z	DI5	7			

J5 DO GROUPS Ø & 1

Pin	Function	Group	Pin	Function	Group
A	DOØ	Ø	a	DO4	1
B	DO1	Ø	b	DO5	1
C	DO2	Ø	c	DO6	1
D	DO3	Ø	d	DO7	1
E	DO4	Ø	e	DO8	1
F	DO5	Ø	f	DO9	1
G	DO6	Ø	g	DO10	1
H	DO7	Ø	h	DO11	1
J	DO8	Ø	i	DO12	1
K	DO9	Ø	j	DO13	1
L	DO10	Ø	k	DO14	1
M	DO11	Ø	m	DO15	1
N	DO12	Ø	n	V Supp.	1
P	DO13	Ø	p	V Supp.	1
R	DO14	Ø	q	Isolated Return	1
S	DO15	Ø	r	Chassis Gnd	
T	V Supp.	Ø	s	DIU Common 1	
U	V Supp.	Ø	t	DIU Common 2	
V	Isolated Return	Ø			
W	DOØ	1			
X	DO1	1			
Y	DO2	1			
Z	DO3	1			

J6 DO GROUPS 2 & 3

Pin	Function	Group	Pin	Function	Group
A	DOØ	2	a	DO4	3
B	DO1	2	b	DO5	3
C	DO2	2	c	DO6	3
D	DO3	2	d	DO7	3
E	DO4	2	e	DO8	3
F	DO5	2	f	DO9	3
G	DO6	2	g	DO10	3
H	DO7	2	h	DO11	3
J	DO8	2	i	DO12	3
K	DO9	2	j	DO13	3
L	DO10	2	k	DO14	3
M	DO11	2	m	DO15	3
N	DO12	2	n	V Supp.	3
P	DO13	2	p	V Supp.	3
R	DO14	2	q	Isolated Return	3
S	DO15	2	r	Chassis Gnd	
T	V Supp.	2	s	DIU Common 1	
U	V Supp.	2	t	DIU Common 2	
V	Isolated Return	2			
W	DOØ	3			
X	DO1	3			
Y	DO2	3			
Z	DO3	3			

J7 DO GROUPS 4 & 5

Pin	Function	Group	Pin	Function	Group
A	DOØ	4	a	DO4	5
B	DO1	4	b	DO5	5
C	DO2	4	c	DO6	5
D	DO3	4	d	DO7	5
E	DO4	4	e	DO8	5
F	DO5	4	f	DO9	5
G	DO6	4	g	DO10	5
H	DO7	4	h	DO11	5
J	DO8	4	i	DO12	5
K	DO9	4	j	DO13	5
L	DO10	4	k	DO14	5
M	DO11	4	m	DO15	5
N	DO12	4	n	V Supp.	5
P	DO13	4	p	V Supp.	5
R	DO14	4	q	Isolated Return	5
S	DO15	4	r	Chassis Gnd	
T	V Supp.	4	s	DIU Common 1	
U	V Supp.	4	t	DIU Common 2	
V	Isolated Return	4			
W	DOØ	5			
X	DO1	5			
Y	DO2	5			
Z	DO3	5			

J8 DO GROUPS 6 & 7

Pin	Function	Group	Pin	Function	Group
A	DOØ	6	a	DO4	7
B	DO1	6	b	DO5	7
C	DO2	6	c	DO6	7
D	DO3	6	d	DO7	7
E	DO4	6	e	DO8	7
F	DO5	6	f	DO9	7
G	DO6	6	g	DO10	7
H	DO7	6	h	DO11	7
J	DO8	6	i	DO12	7
K	DO9	6	j	DO13	7
L	DO10	6	k	DO14	7
M	DO11	6	m	DO15	7
N	DO12	6	n	V Supp.	7
P	DO13	6	p	V Supp.	7
R	DO14	6	q	Isolated Return	7
S	DO15	6	r	Chassis Gnd	
Y	V Supp.	6	s	DIU Common 1	
U	V Supp.	6	t	DIU Common 2	
V	Isolated Return	6			
W	DOØ	7			
X	DO1	7			
Y	DO2	7			
Z	DO3	7			

J9 AI GROUP 0

Pin	Function
A	AI0 +
B	AI0 -
C	AI1 +
D	AI1 -
E	AI2 +
F	AI2 -
G	AI3 +
H	AI3 -
J	AI4 +
K	AI4 -
L	AI5 +
M	AI5 -
N	AI6 +
P	AI6 -
R	AI7 +
S	AI7 -
T	AI8 +
U	AI8 -
V	AI9 +
W	AI9 -
X	AI10 +
Y	AI10 -
Z	AI11 +
a	AI11 -
b	AI12 +
c	AI12 -
d	AI13 +
e	AI13 -
f	AI14 +
g	AI14 -
h	AI15 +
i	AI15 -
j	Common Shield
k	Chassis Gnd.
l	Spare
m	Spare
n	Spare
p	Spare
q	Spare
r	Spare
s	DIU Common 1
t	DIU Common 2

J10 AI GROUP 1

Pin	Function
A	AI16 +
B	AI16 -
C	AI17 +
D	AI17 -
E	AI18 +
F	AI18 -
G	AI19 +
H	AI19 -
J	AI20 +
K	AI20 -
L	AI21 +
M	AI21 -
N	AI22 +
P	AI22 -
R	AI23 +
S	AI23 -
T	AI24 +
U	AI24 -
V	AI25 +
W	AI25 -
X	AI26 +
Y	AI26 -
Z	AI27 +
a	AI27 -
b	AI28 +
c	AI28 -
d	AI29 +
e	AI29 -
f	AI30 +
g	AI30 -
h	AI31 +
i	AI31 -
j	Common Shield
k	Chassis Gnd.
l	Spare
m	Spare
n	Spare
p	Spare
q	Spare
r	Spare
s	DIU Common 1
t	DIU Common 2

J11 AI GROUP 2

Pin	Function
A	AI32 +
B	AI32 -
C	AI33 +
D	AI33 -
E	AI34 +
F	AI34 -
G	AI35 +
H	AI35 -
J	AI36 +
K	AI36 -
L	AI37 +
M	AI37 -
N	AI38 +
P	AI38 -
R	AI39 +
S	AI39 -
T	AI40 +
U	AI40 -
V	AI41 +
W	AI41 -
X	AI42 +
Y	AI42 -
Z	AI43 +
a	AI43 -
b	AI44 +
c	AI44 -
d	AI45 +
e	AI45 -
f	AI46 +
g	AI46 -
h	AI47 +
i	AI47 -
j	Common Shield
k	Chassis Gnd.
l	Spare
m	Spare
n	Spare
p	Spare
q	Spare
r	Spare
s	DIU Common 1
t	DIU Common 2

J12 AI GROUP 3

Pin	Function
A	AI48 +
B	AI48 -
C	AI49 +
D	AI49 -
E	AI50 +
F	AI50 -
G	AI51 +
H	AI51 -
J	AI52 +
K	AI52 -
L	AI53 +
M	AI53 -
N	AI54 +
P	AI54 -
R	AI55 +
S	AI55 -
T	AI56 +
U	AI56 -
V	AI57 +
W	AI57 -
X	AI58 +
Y	AI58 -
Z	AI59 +
a	AI59 -
b	AI60 +
c	AI60 -
d	AI61 +
e	AI61 -
f	AI62 +
g	AI62 -
h	AI63 +
i	AI63 -
j	Common Shield
k	Chassis Gnd.
l	Spare
m	Spare
n	Spare
p	Spare
q	Spare
r	Spare
s	DIU Common 1
t	DIU Common 2

J13 AI GROUP 4

Pin	Function
A	AI64 +
B	AI64 -
C	AI65 +
D	AI65 -
E	AI66 +
F	AI66 -
G	AI67 +
H	AI67 -
J	AI68 +
K	AI68 -
L	AI69 +
M	AI69 -
N	AI70 +
P	AI70 -
R	AI71 +
S	AI71 -
T	AI72 +
U	AI72 -
V	AI73 +
W	AI73 -
X	AI74 +
Y	AI74 -
Z	AI75 +
a	AI75 -
b	AI76 +
c	AI76 -
d	AI77 +
e	AI77 -
f	AI78 +
g	AI78 -
h	AI79 +
i	AI79 -
j	Common Shield
k	Chassis Gnd.
l	Spare
m	Spare
n	Spare
p	Spare
q	Spare
r	Spare
s	DIU Common 1
t	DIU Common 2

J14 AI GROUP 5

Pin	Function
A	AI80 +
B	AI80 -
C	AI81 +
D	AI81 -
E	AI82 +
F	AI82 -
G	AI83 +
H	AI83 -
J	AI84 +
K	AI84 -
L	AI85 +
M	AI85 -
N	AI86 +
P	AI86 -
R	AI87 +
S	AI87 -
T	AI88 +
U	AI88 -
V	AI89 +
W	AI89 -
X	AI90 +
Y	AI90 -
Z	AI91 +
a	AI91 -
b	AI92 +
c	AI92 -
d	AI93 +
e	AI93 -
f	AI94 +
g	AI94 -
h	AI95 +
i	AI95 -
j	Common Shield
k	Chassis Gnd.
l	Spare
m	Spare
n	Spare
p	Spare
q	Spare
r	Spare
s	DIU Common 1
t	DIU Common 2

J15 AI GROUP 6

Pin	Function
A	AI96 +
B	AI96 -
C	AI97 +
D	AI97 -
E	AI98 +
F	AI98 -
G	AI99 +
H	AI99 -
J	AI100 +
K	AI100 -
L	AI101 +
M	AI101 -
N	AI102 +
P	AI102 -
R	AI103 +
S	AI103 -
T	AI104 +
U	AI104 -
V	AI105 +
W	AI105 -
X	AI106 +
Y	AI106 -
Z	AI107 +
a	AI107 -
b	AI108 +
c	AI108 -
d	AI109 +
e	AI109 -
f	AI110 +
g	AI110 -
h	AI111 +
i	AI111 -
j	Common Shield
k	Chassis Gnd.
l	Spare
m	Spare
n	Spare
p	Spare
q	Spare
r	Spare
s	DIU Common 1
t	DIU Common 2

J16 AI GROUP 7

Pin	Function
A	AI112 +
B	AI112 -
C	AI113 +
D	AI113 -
E	AI114 +
F	AI114 -
G	AI115 +
H	AI115 -
H	AI116 +
K	AI116 -
L	AI117 +
M	AI117 -
N	AI118 +
P	AI118 -
R	AI119 +
S	AI119 -
T	AI120 +
U	AI120 -
V	AI121 +
W	AI121 -
X	AI122 +
Y	AI122 -
Z	AI123 +
a	AI123 -
b	AI124 +
c	AI124 -
d	AI125 +
e	AI125 -
f	AI126 +
g	AI126 -
h	AI127 +
i	AI127 -
j	Common Shield
k	Chassis Gnd.
l	Spare
m	Spare
n	Spare
p	Spare
q	Spare
r	Spare
s	DIU Common 1
t	DIU Common 2

J17 AO'S

Pin	Function
A	AOØ +
B	AOØ -
C	AO1 +
D	AO1 -
E	AO2 +
F	AO2 -
G	AO3 +
H	AO3 -
J	Common Shield
K	Chassis Gnd.

J18 RI/RO 0

Pin	Function
A	RODØ +
B	RODØ -
C	RIØ +
D	RIØ -
E	Chassis Gnd.
F	ROCØ +
G	ROCØ -
H	RODØ Shield
J	RI Ø Shield
K	ROC Ø Shield

J19 RI/RO 1

Pin	Function
A	ROD1 +
B	ROD1 -
C	RI1 +
D	RI1 -
E	Chassis Gnd.
F	ROC1 +
G	ROC1 -
H	ROD1 Shield
J	RI1 Shield
K	ROC1 Shield

J20 RI/RO 2

Pin	Function
A	ROD2 +
B	ROD2 -
C	RI2 +
D	RI2 -
E	Chassis Gnd.
F	ROC2 +
G	ROC2 -
H	ROD2 Shield
J	RI2 Shield
K	ROC2 Shield

J21 RI/RO 3

Pin	Function
A	ROD3 +
B	ROD3 -
C	RI3 +
D	RI3 -
E	Chassis Gnd.
F	ROC3 +
G	ROC3 -
H	ROD3 Shield
J	RI3 Shield
K	ROC3 Shield

J22 RI/RO 4

Pin	Function
A	ROD4 +
B	ROD4 -
C	RI4 +
D	RI4 -
E	Chassis Gnd.
F	ROC4 +
G	ROC4 -
H	ROD4 Shield
J	RI4 Shield
K	ROC4 Shield

J23 RI/RO 5

Pin	Function
A	ROD5 +
B	ROD5 -
C	RI5 +
D	RI5 -
E	Chassis Gnd.
F	ROC5 +
G	ROC5 -
H	ROD5 Shield
J	RI5 Shield
K	ROC5 Shield

J24 RI/RO 6

Pin	Function
A	ROD6 +
B	ROD6 -
C	RI6 +
D	RI6 -
E	Chassis Gnd.
F	ROC6 +
G	ROC6 -
H	ROD6 Shield
J	RI6 Shield
K	ROC6 Shield

J25 RI/RO 7

Pin	Function
A	ROD7 +
B	ROD7 -
C	RI7 +
D	RI7 -
E	Chassis Gnd.
F	ROC7 +
G	ROC7 -
H	ROD7 Shield
J	RI7 Shield
K	ROC7 Shield

J26 POWER

Pin	Function
A	+28 VDC
B	+28 VDC (RTN) -
C	Spare
D	Spare
E	Chassis Gnd.

J27 SUPERVISORY BUS

Pin	Function
Center Pin	Sup BIØ +
Isolated Ring	Sup BIØ -
Conn. Housing (Shield)	Chassis Gnd.

J28 REPLY BUS

Pin	Function
Center Pin	Reply BIØ +
Isolated Ring	Reply BIØ -
Conn. Housing (Shield)	Chassis Gnd.

4.0 DIU FUNCTIONAL DESCRIPTION

The data flow diagram for the DIU is shown in Figure 4.0-1. The logic and circuits for each of the major sections shown will be described in the following paragraphs. A block diagram for each printed-circuit board will be described as a guide to the unit schematics and drawings.

4.1 DIU POWER SUPPLY (3339022 and 3339024)

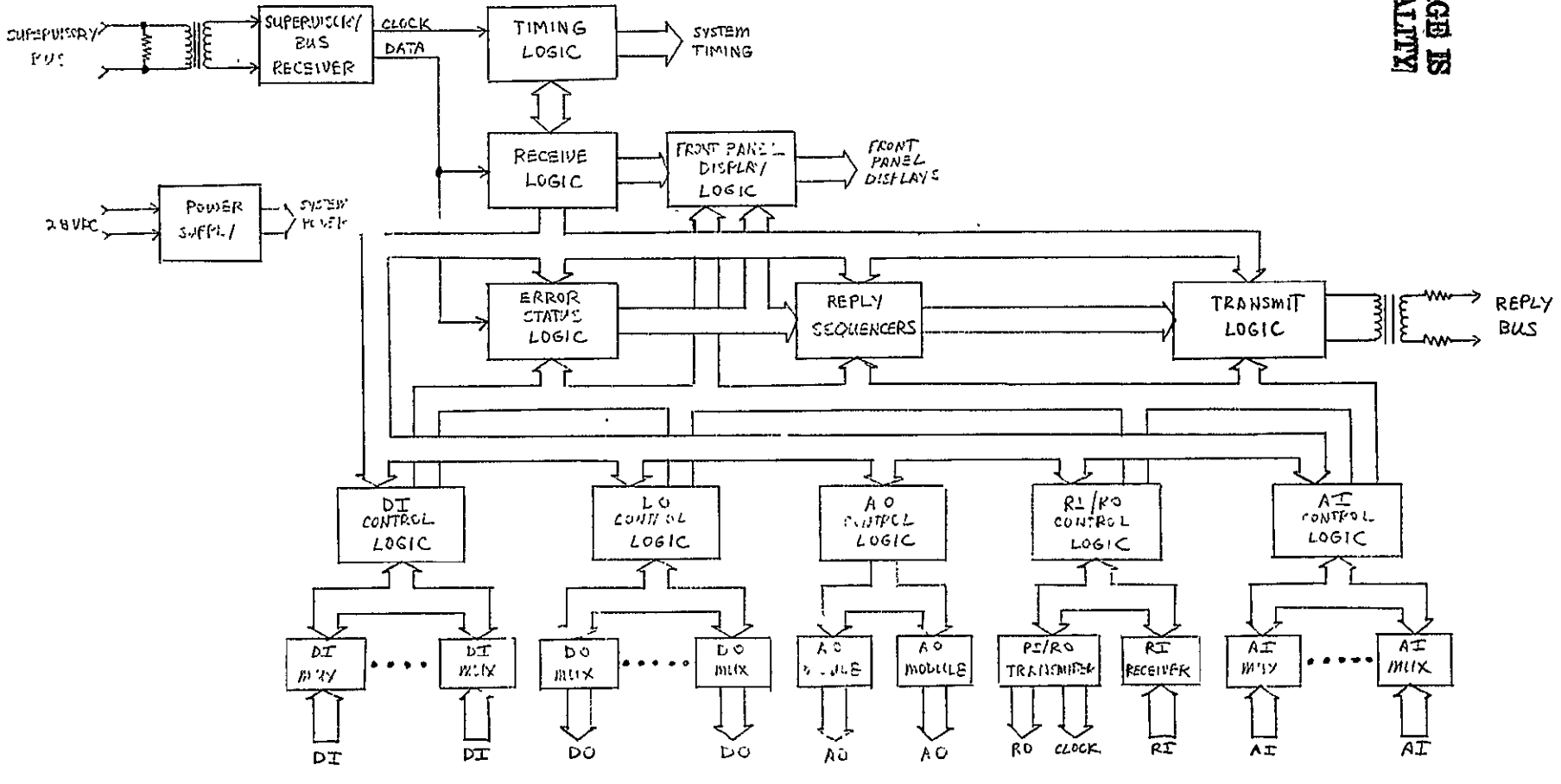
The power supply for the DIU is shown in simplified form in Figure 4.1-1. Basically the design consists of a dc-dc converter driven from a switching regulator to generate the system voltages. Protection against the application of reverse polarity voltage is provided by the input diode. The EMI filter reduces the current surges inherent in the dc-dc converter and the switching regulator, and suppresses noise on the input lines below interferring levels.

Regulation of system voltages is achieved by the switching regulator. The regulator and the dc-dc converter are synchronized to the DIU timing to force the converter switching transients to occur between encode cycles of the AI analog-to-digital converter. The external sync detector allows an internal oscillator to generate power supply timing when power is first applied to the system.

The +20 VDC output of the regulator is monitored for overvoltage and excess current conditions to protect both the DIU circuitry and the input power bus. A power-on-reset circuit detects low voltage conditions to generate an initialization pulse when power is first applied to the system and for power drop-out conditions.

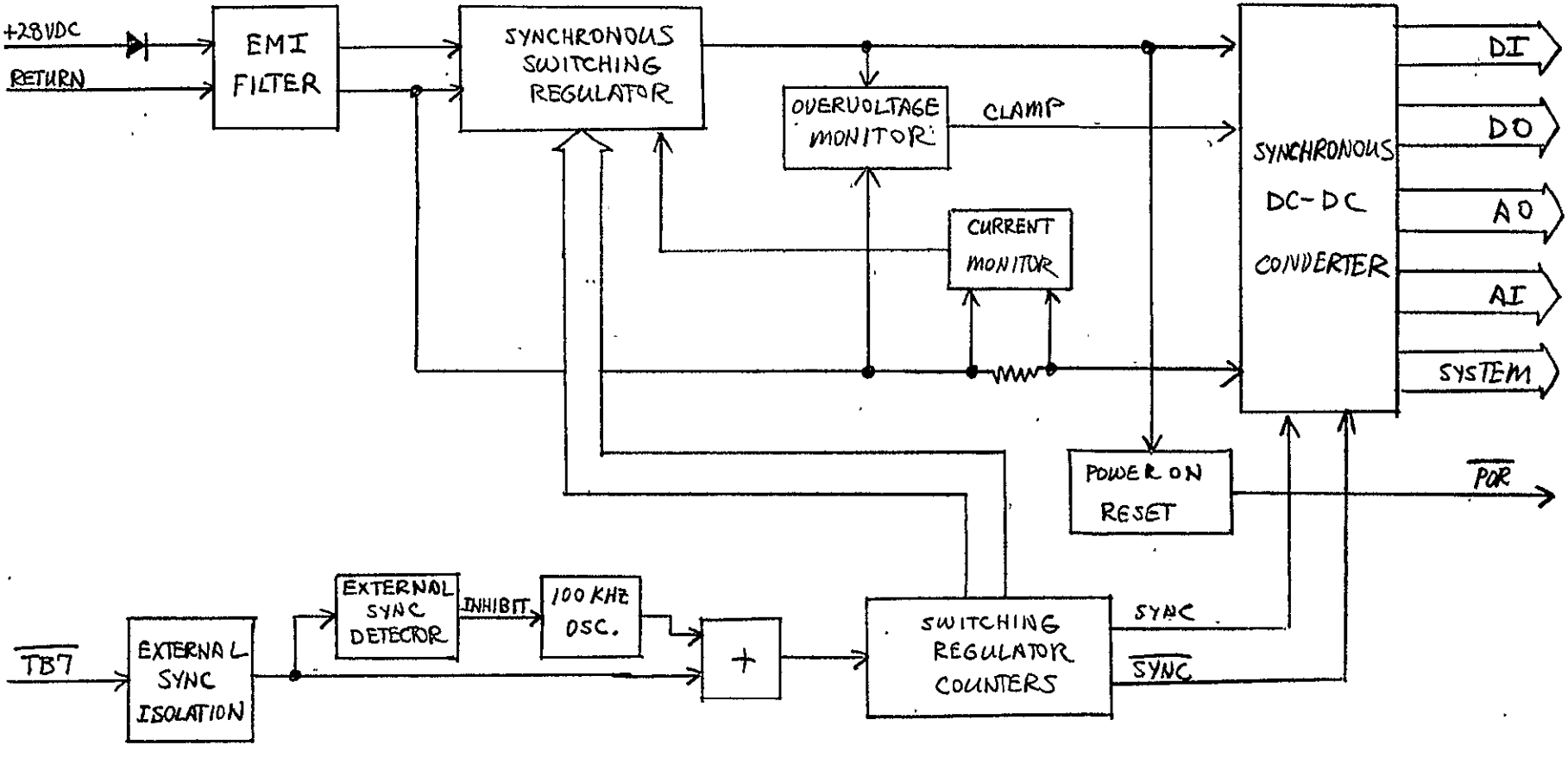
Secondary voltages for the DIU circuitry are obtained by full wave rectification and filtering. Isolated output voltages are supplied for the DI, DO,

and AO logic. A floating supply output is provided for the AI multiplexer circuitry. This winding is driven by the sampled analog input to reduce multiplexer settling time.



DIU BLOCK DIAGRAM

FIGURE 4.0-1



DIU POWER SUPPLY

FIGURE 4.1-1

4.2 SUPERVISORY BUS RECEIVER (3339014)

The DIU bus receiver accepts continuous bi-phase data from the supervisory bus and performs bi-phase to NRZ conversion using pulse integration techniques. The block diagram is shown in Figure 4.2-1.

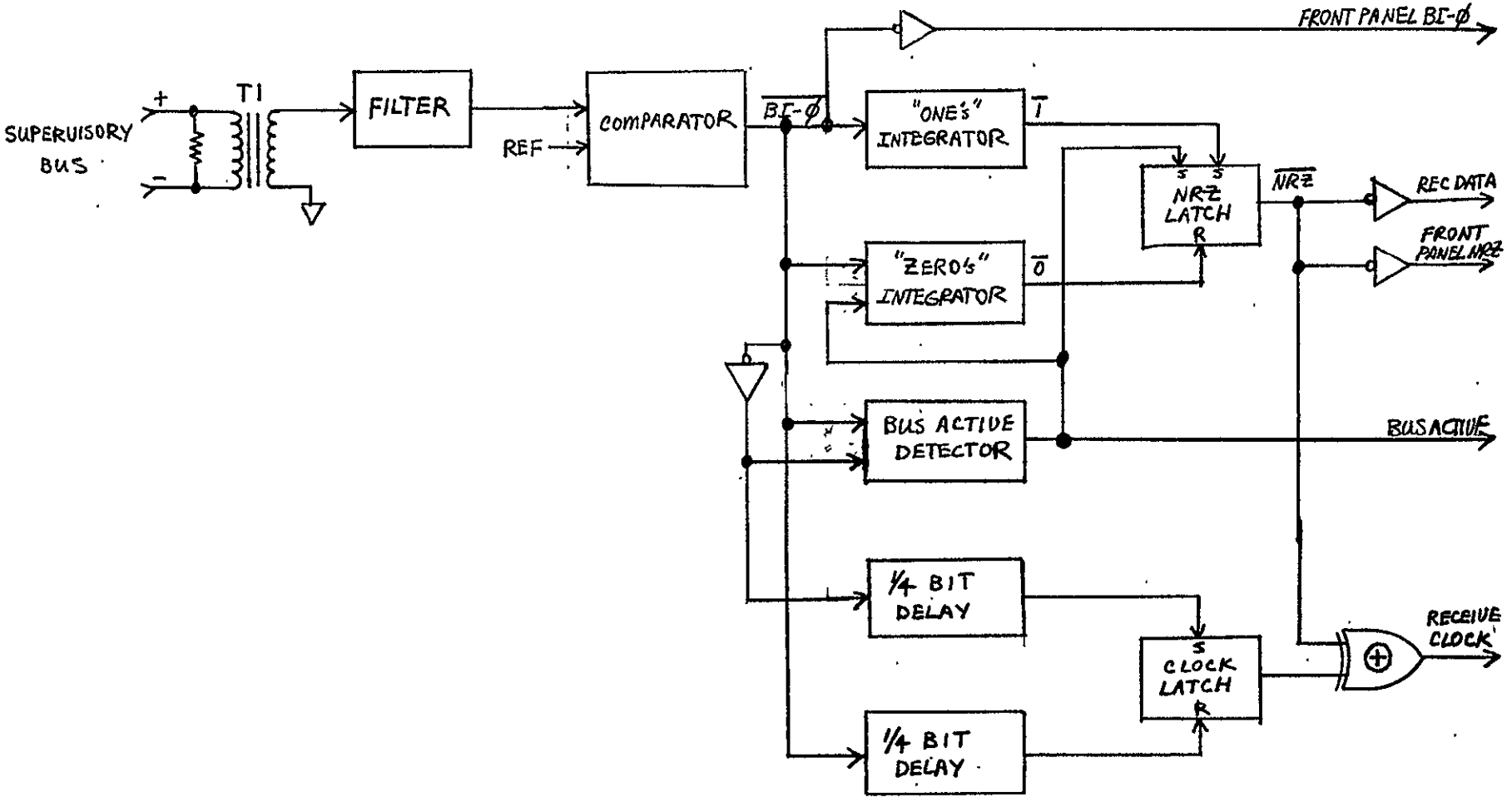
The front end of the receiver consists of an isolation transformer and a rasied-cosine input filter. The provides 6 db attenuation at twice the bit rate, and is optimized for minimum intersymbol interference for bi-phase data.

The filter output is supplied to a voltage comparator, which is biased at approximately 250 mv. Voltage feedback is included to provide approximately 5 mv. of hysteresis at the comparator reference input. The hysteresis prevents oscillation at the comparator output due to slow rise times at the filter output.

The comparator output is buffered for a front panel test point, and also supplied to two integrators, a bus-active detector, and the clock generator delay circuits.

The outputs of the "One's" integrator and "Zero's" integrator supply set and reset signals to the NRZ latch. The Bus Active detector sets the NRZ latch to a "One's" condition and discharges the "Zero's" integrator when the Supervisory bus is inactive.

The comparator output is also supplied to two 1/4 bit delay circuits to synchronize the clock and data outputs. The outputs of the Clock latch and the NRZ latch are Exclusive OR'ed to generate the Receive clock. The NRZ latch is buffered for a front panel test point and the Receive Data signal.



DIU BUS RECEIVER

FIGURE 4.2-1

4.3 TIMING LOGIC

The Timing Logic circuitry is contained on two printed circuit boards and provides the clock synchronization with the Supervisory Bus and the system timing signals for instruction execution.

Timing 1 Logic (3339050)

Clock synchronization is implemented with the phase-locked-loop shown in Figure 4.3-1. The Receive clock and the internal 2 MHz clock are supplied to a phase comparator. This circuit generates an error signal proportional to the phase difference in the two clocks. The low-pass filter controls the fundamental loop characteristics such as capture range, loop bandwidth, capture time, and transient response. The filter output drives a voltage-controlled oscillator to generate the system 8 MHz clock. An external capacitor provides a free-running frequency of approximately 8 MHz during the absence of data on the Supervisory bus.

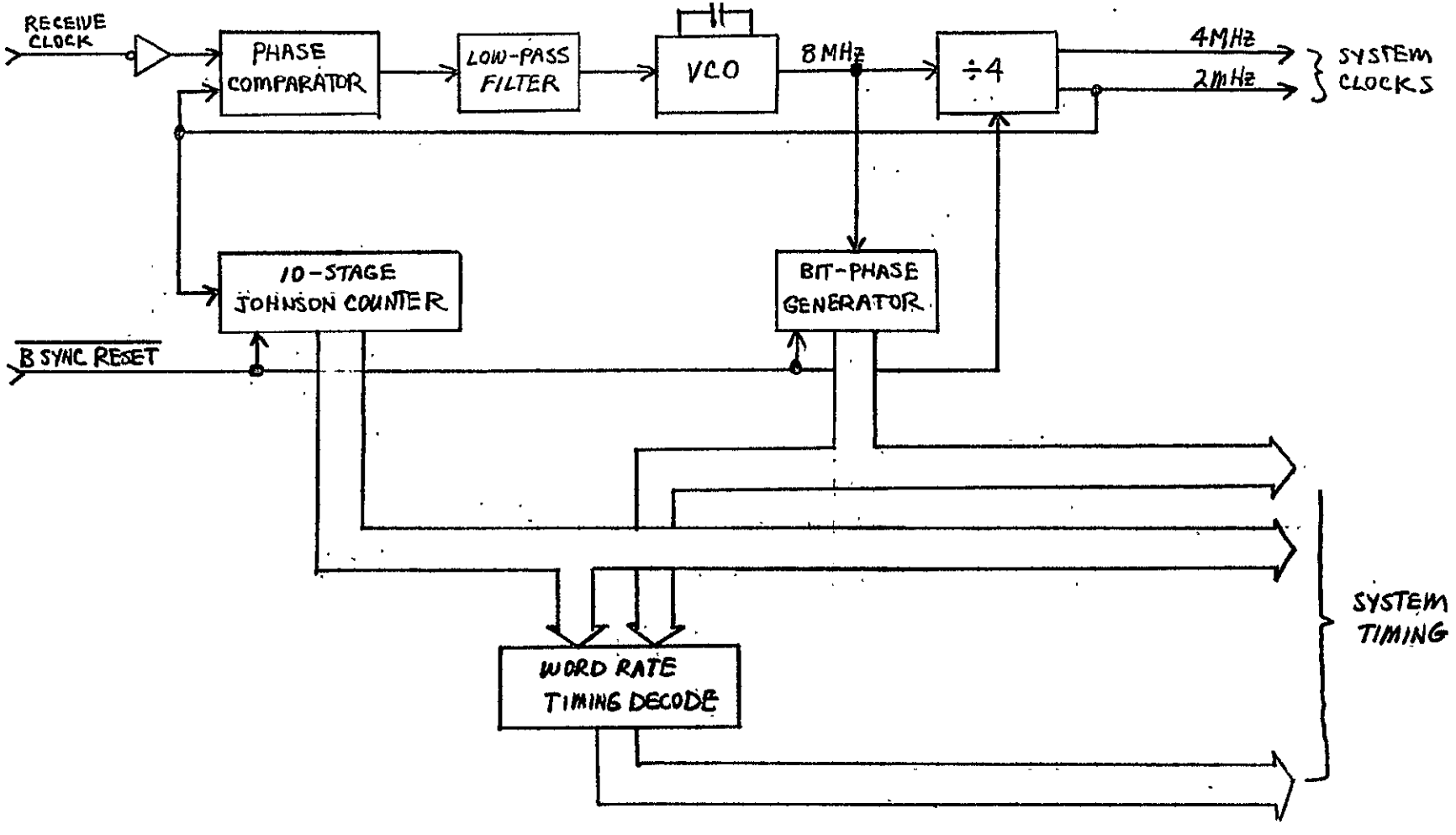
A 10-stage Johnson counter and the Bit-phase generator provide the timing signals for the system timing decode signals. The timing relationships are shown in Figure 4.3-2. Word synchronization is provided by the Blank Word Reset signal from the Receive Logic.

Timing 2 Logic (3339044)

The Timing 2 Logic provides additional decoding of the Timing 1 Logic outputs and an instruction execution signal for the DIU input/output logic. The block diagram is shown in Figure 4.3-3.

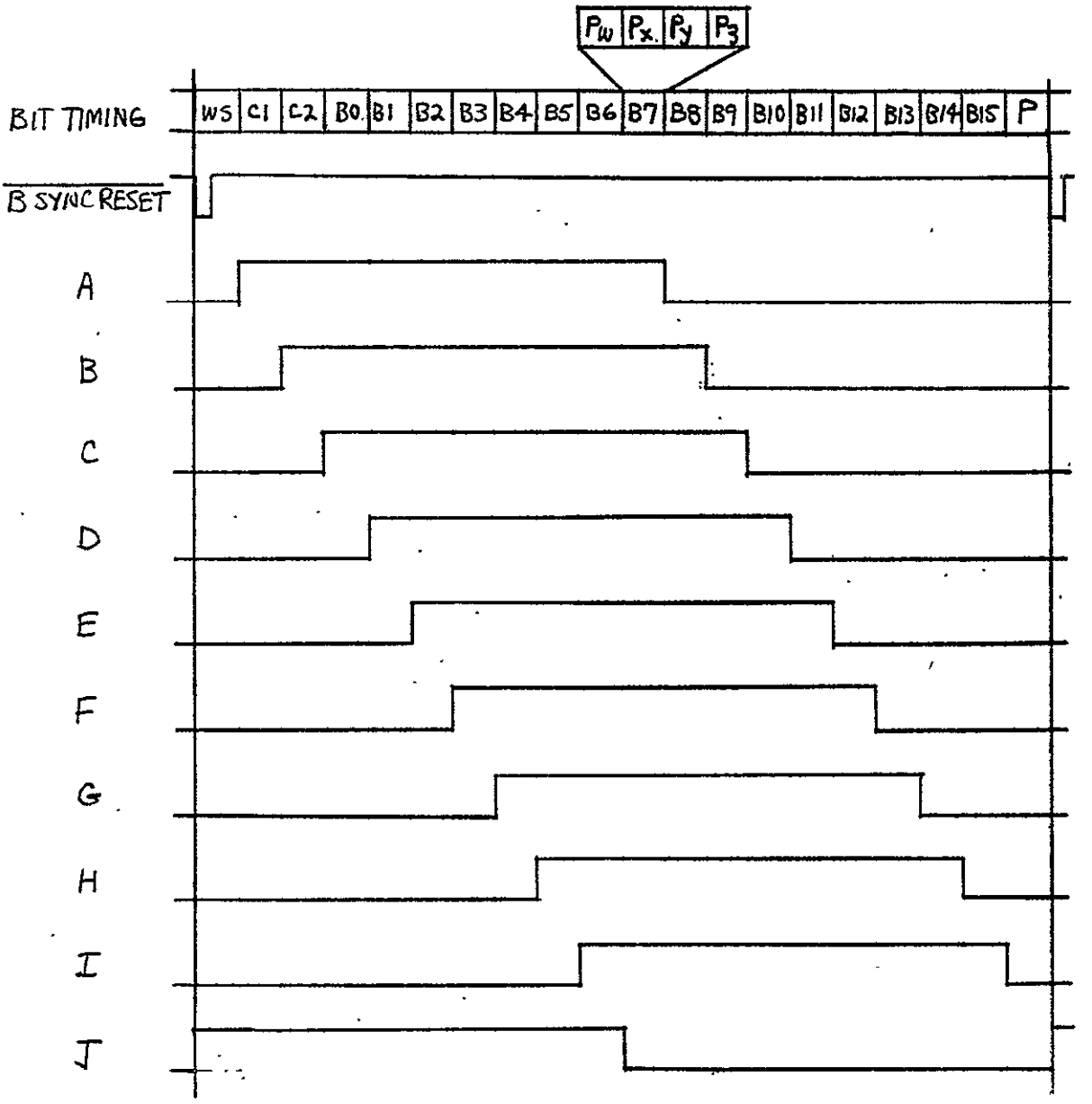
Two gated shift clocks are generated as shown in Figure 4.3-4 for data control during read and write instructions. The enable signal for the write clock is used by the transmit logic to insert the parity, word sync, and bus prefix into the DIU reply.

The OP Code Enable signal is initiated at the end of the A word for read OP codes, at the end of the WC word for Read DI changes and Reset OP codes to allow for checking WC word parity, and at the end of the first D word for write OP Codes to check D word parity. The Channel Address Load pulse is generated at the beginning of OPCEN to load the instruction channel address where applicable, and at the end of OPCEN to restore the AI scan address after AI type instructions.



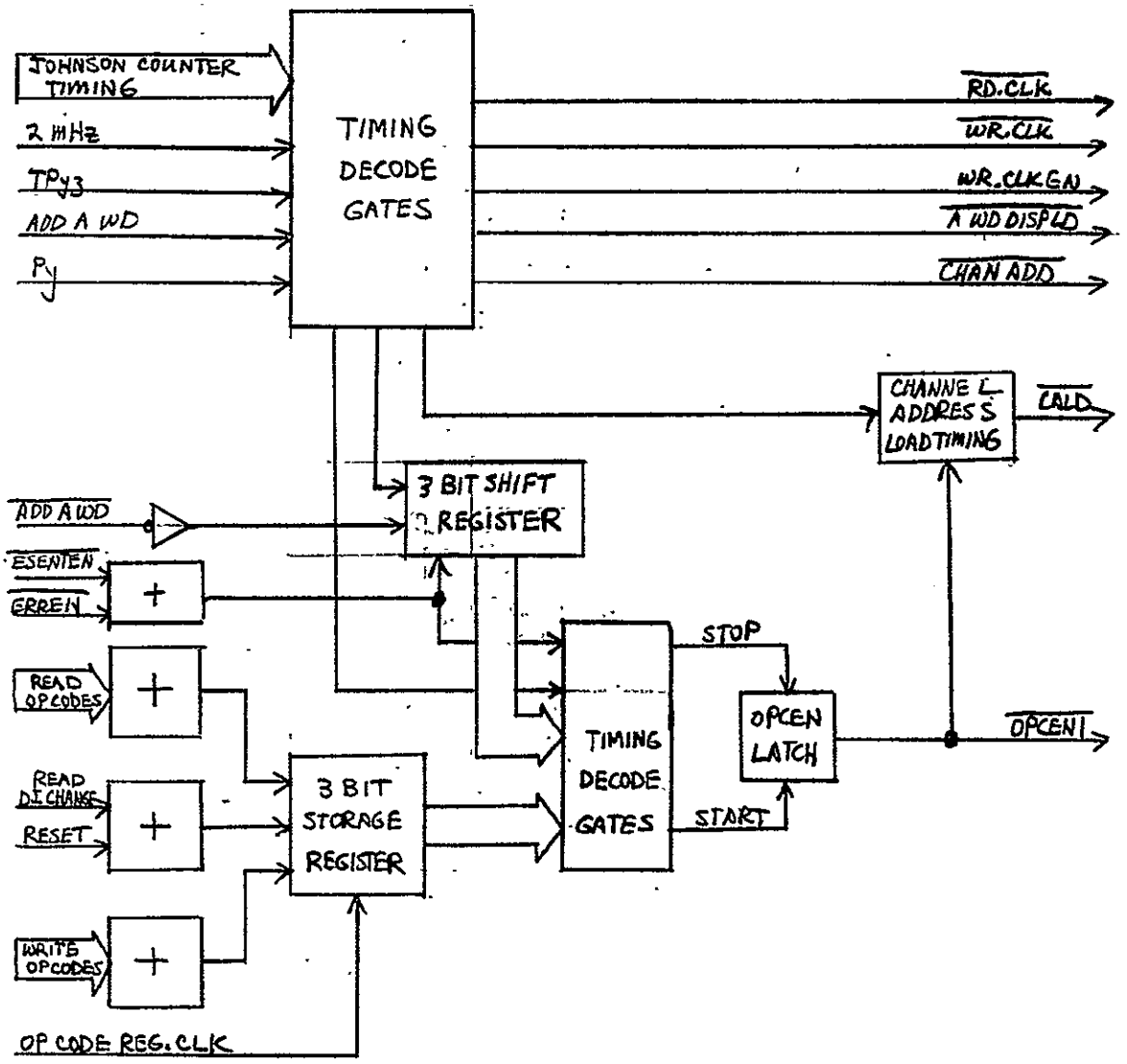
TIMING 1 LOGIC

FIGURE 4.3-1



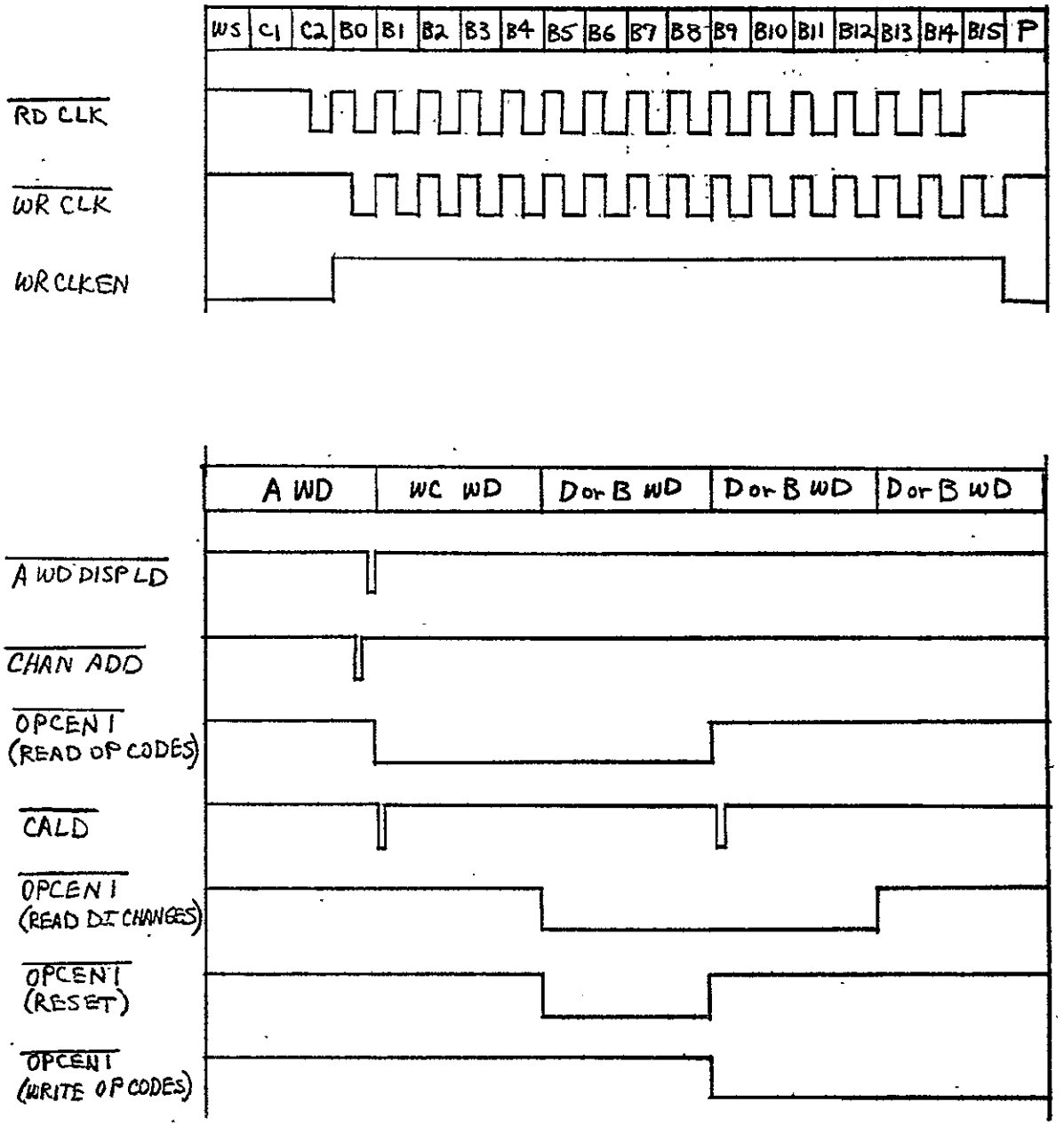
JOHNSON COUNTER TIMING

FIGURE 4.3-2



TIMING 2 LOGIC

FIGURE 4.3-3



TIMING 2 OUTPUTS

FIGURE 4.3-4

4.4 RECEIVE LOGIC

The Receive Logic is contained on four printed-circuit boards and performs the instruction recognition and processing logic for the DIU. Functions included in this logic are as follows:

- o Power-on initilization timing
- o A word, WC word recognition
- o Unit address recognition
- o Instruction decode and storage
- o Channel address storage
- o Word Counter
- o Bus prefix decode
- o Bus word synchronization

Receive Logic 1 (3339042)

The block diagram for Receive Logic 1 is shown in Figure 4.4-1. The OP code register clock is generated at the beginning and end of each instruction sequence. The timing relationships of this signal and other receive logic signals are shown in Figure 4.4-5. This drawing illustrates an instruction sequence for the Read DI instruction.

A six bit storage register is provided for storage of the channel address bits from the received A word. The register clock is generated in the Timing 2 logic.

The word counter load and clock pulses are generated for those instructions which utilize the word count data to determine the number of words in the DIU reply. The word counter data is loaded during the x-phase of the WC-word parity bit. For read instructions that require reply data immediately following

the sync word, the word counter is decremented during the z-phase of the parity bit of the WC-word and all subsequent words until a word count of 1 is detected. For the Read AI instruction, a blank word is inserted in the reply before the first D word, and the word counter clock during the WC word is inhibited. The word counter is decremented for write instructions by gating the clock with detection of D words on the supervisory bus. For Read RI codes, the clock is gated with detection of D word prefixes on the RI line.

Initilization of the DIU logic during power-up conditions is controlled by the Power On Initiate (POIN) signal. This sequence is required to be at least 64 word times long to initialize the AI delta memory. The sequence is started by the POR output from the power supply and ended by decrementing the word counter at the system word rate until the W/8 bit changes. The Transmit Inhibit 2 output is used to disable the DIU transmitter during the initialization sequence.

The POIN signal is OR'ed with the OP code enable output from the Timing 2 logic to form the system enable signal (OPCEN), and OR'ed with blank word detect and A word detect to generate the Sequence 1 Clear and Sequence 2 clear signals.

Receive Logic 2 (3339040)

The block diagram for Receive Logic 2 is shown in Figure 4.4-2. Serial data from the DIU Bus Receiver is shifted into a 21 bit serial-to-parallel receive register by the system 2 MHz clock. The last stage of the register supplies delayed serial data to the system for write instructions. Included on this board are a 16 bit parallel-to-serial front panel display register, the 16 bit word counter, and the blank word sync decoder. The sync decoder detects a 1 (ws bit) followed by 19 0's and another 1 (ws bit), and is used to maintain word synchronization with the supervisory bus.

The bus word logic examines the pulsed outputs from the word prefix decoder and sets two latches to provide levels indicating blank words and D words in the data received on the supervisory bus.

Receive Logic 3 (3339032)

The block diagram for Receive Logic 3 is shown in Figure 4.4-3. Data from the RI register and the receive register are decoded to provide pulsed word prefix outputs. The D word RI latch is set to provide levels for enabling word counter clocks during Read RI instructions.

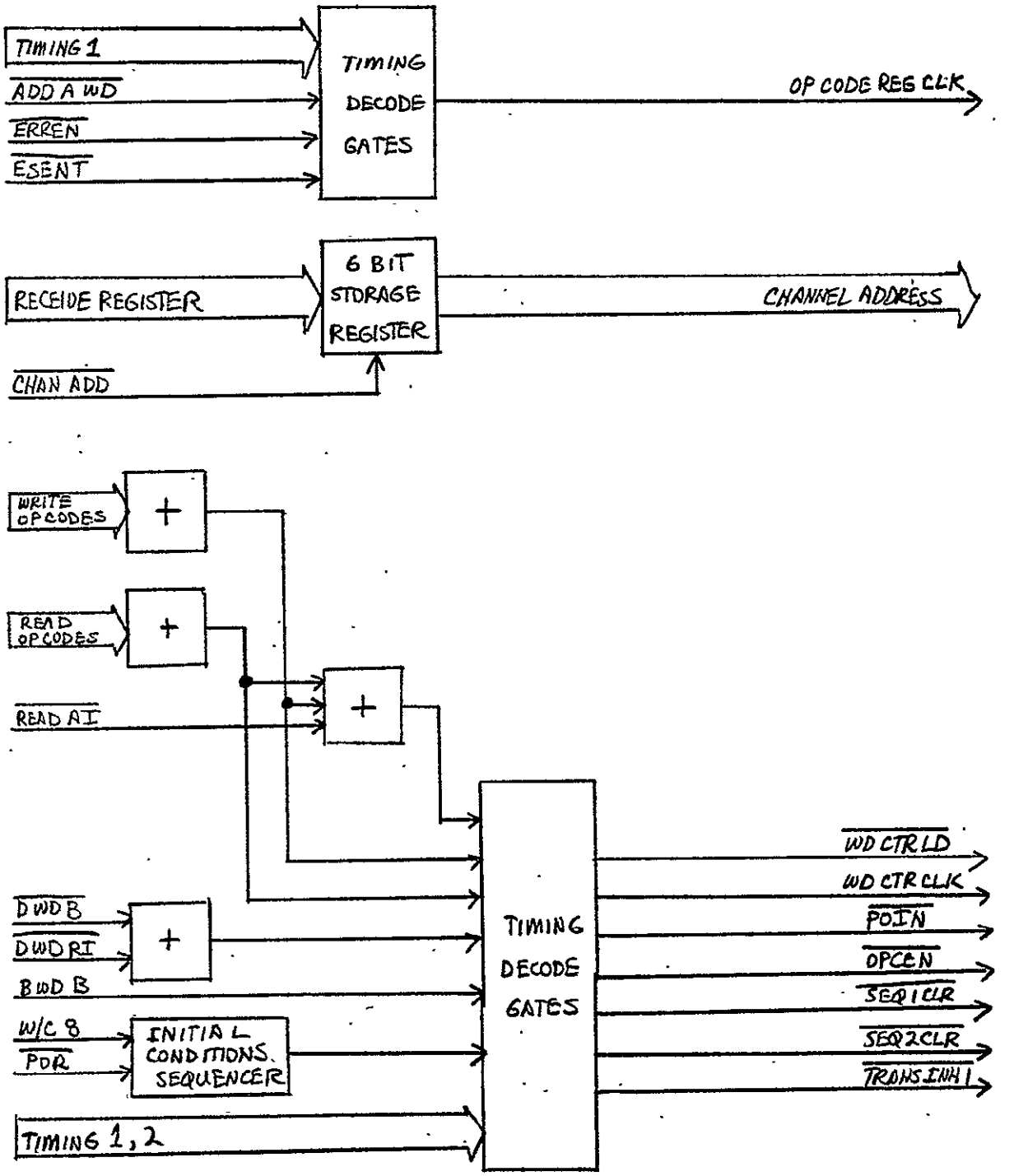
Buffered outputs from the front panel DIU address thumbwheel are compared to data from the receive register to provide a pulsed address compare output (ADD COMP) and a stored address compare level (SADD COMP) for the duration of a message.

Outputs from the word counter are decoded to detect a word count of 1 to indicate an end-of-message condition (DEOM). The one-shot outputs a 60 nsec. reset pulse for word synchronization.

Receive Logic 4 (3339036)

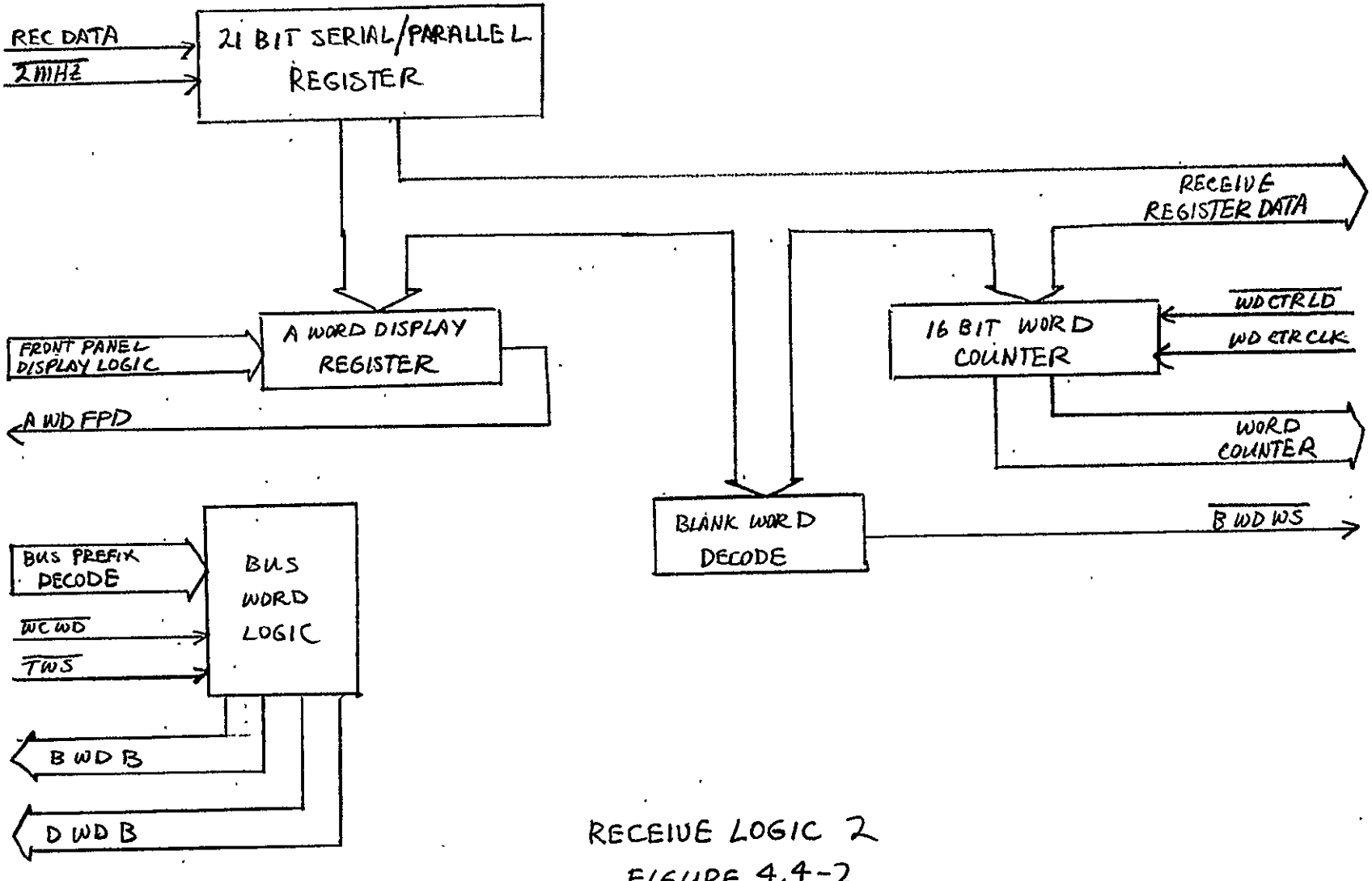
The block diagram for Receive Logic 4 is shown in Figure 4.4-4. Five data bits from the receive register are decoded to provide pulsed outputs for the 32 possible OP codes. Fourteen of these outputs are OR'ed to generate an illegal OP code signal (IOC). The remaining 18 valid OP code pulses are supplied as outputs and also stored in the OP code register.

The message sequence logic detects the presence of an A word prefix logic and generates levels one word in length for A word detect and WC word detect.



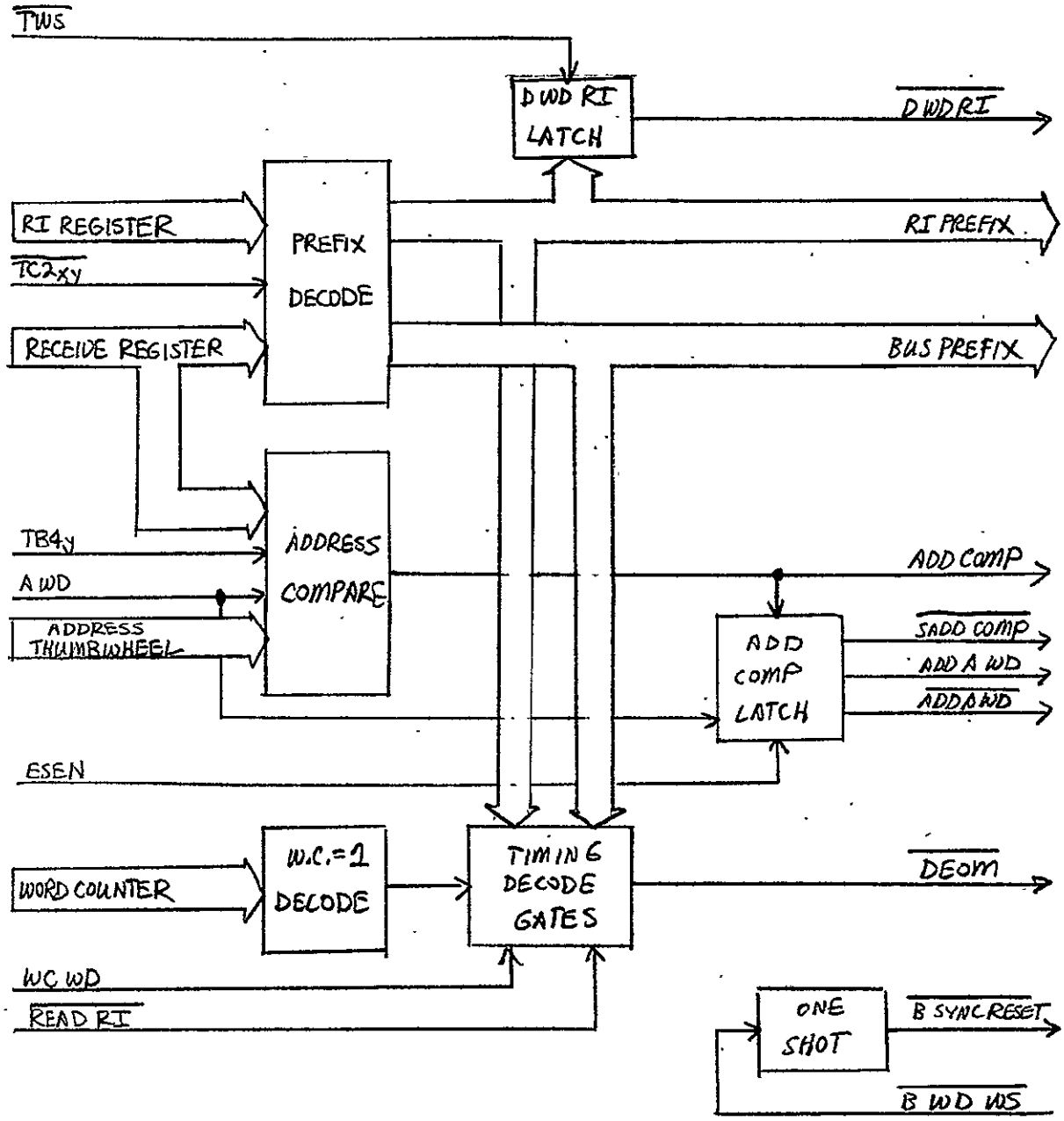
RECEIVE LOGIC 1

FIGURE 4.4-1

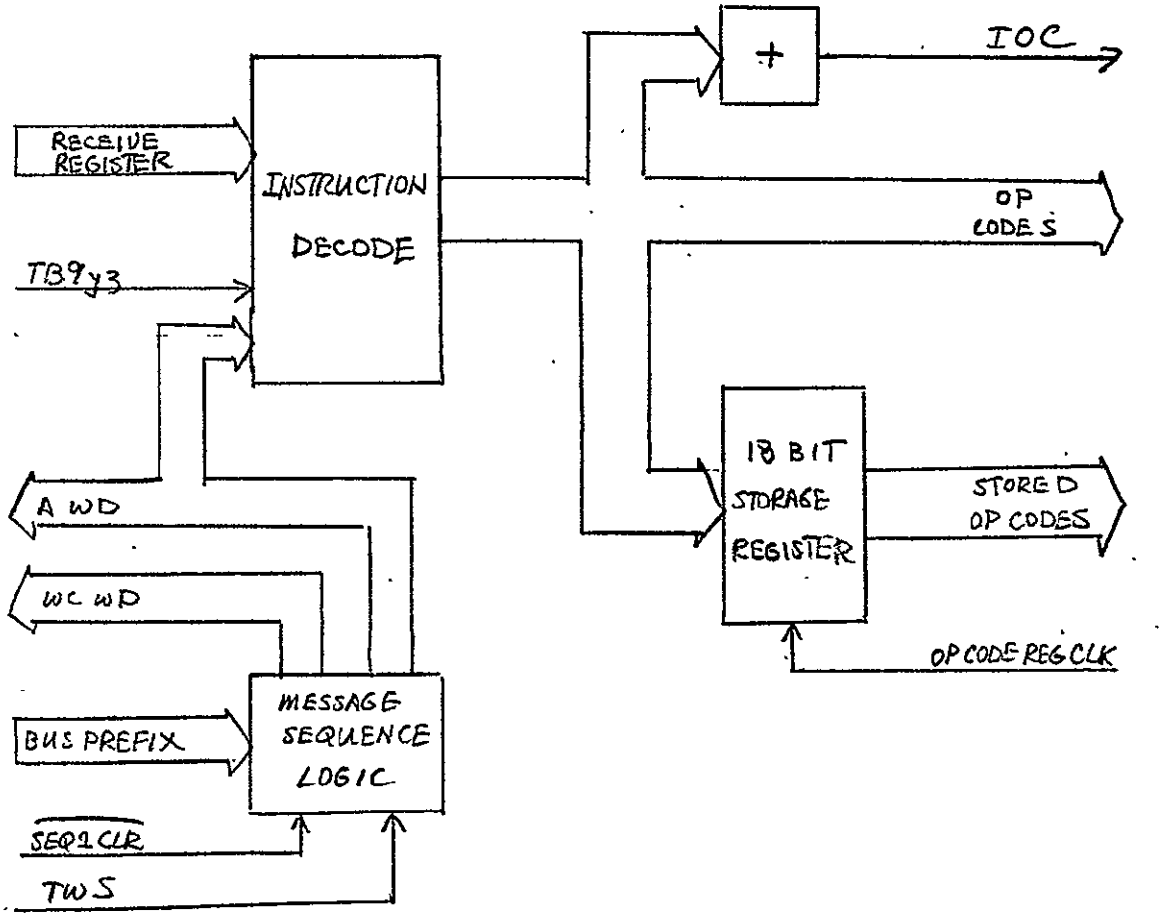


RECEIVE LOGIC 2

FIGURE 4.4-2

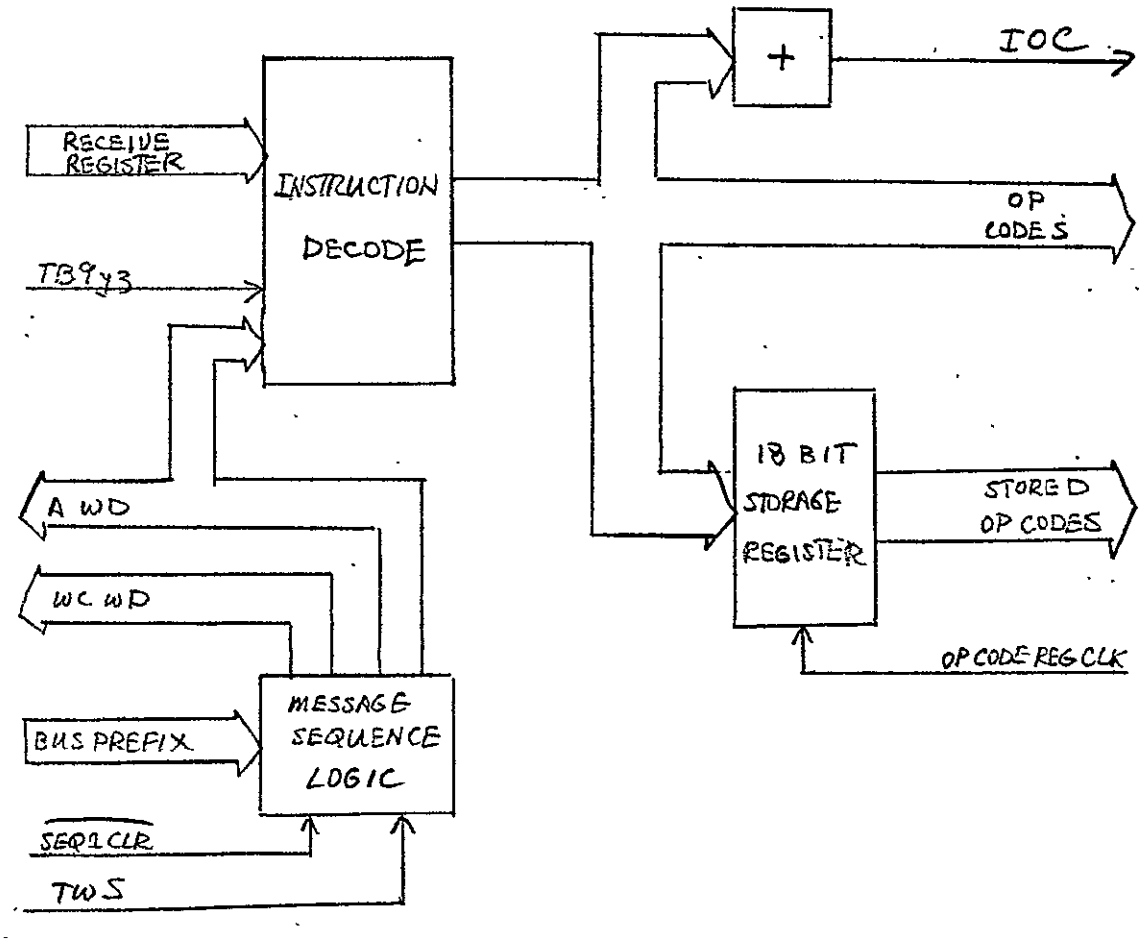


RECEIVE LOGIC 3
FIGURE 4.4-3



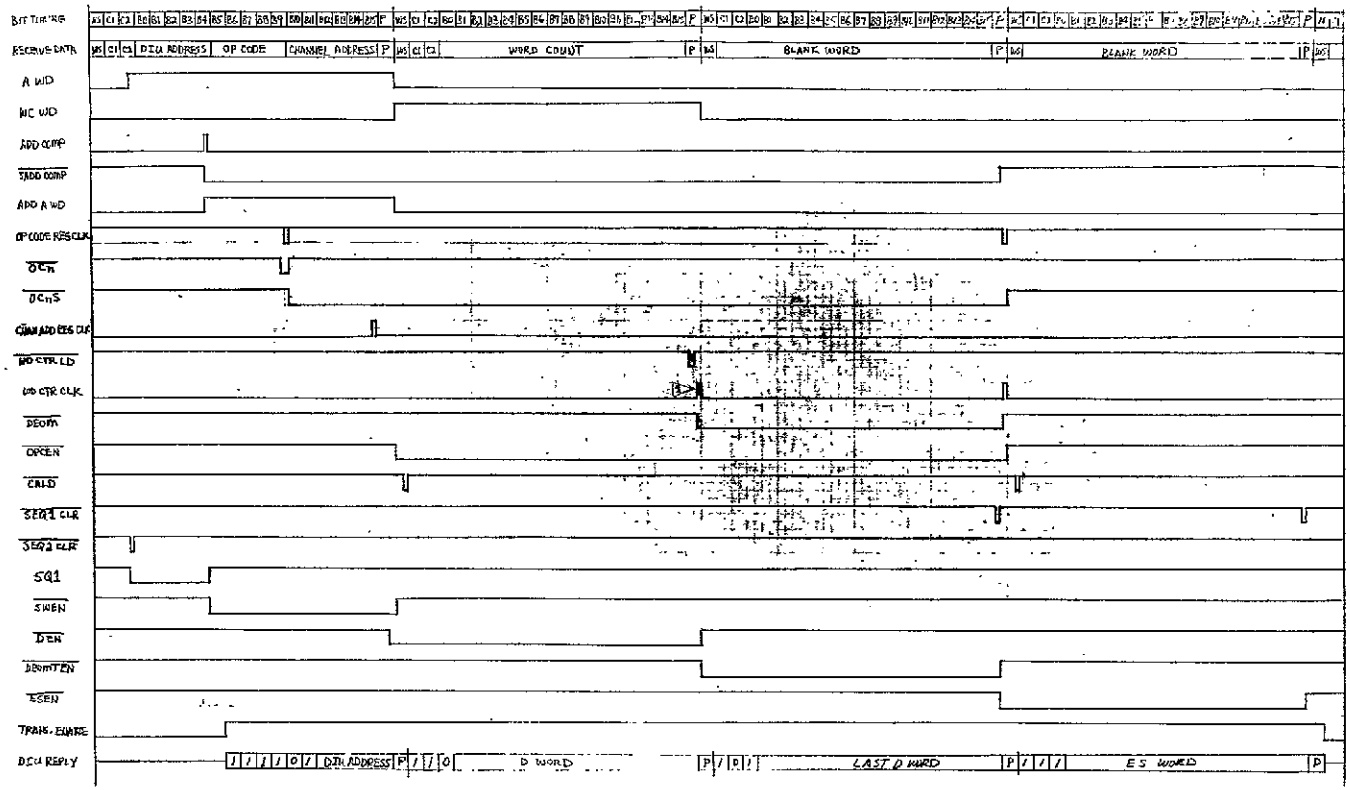
RECEIVE LOGIC 4

FIGURE 4.4-4



RECEIVE LOGIC 4

FIGURE 4.4-4



TIMING DIAGRAM
READ DI INSTRUCTION
FIGURE 4.4-5

4.5 ERROR STATUS LOGIC

The DIU performs 8 message validity tests on each addressed message received on the supervisory bus. Three additional validity tests are made on data received from a subsystem on the RI line. Detection of an error condition from these tests results in the DIU terminating execution of the instruction and inserting the Error Status word as the next word in the reply. For D word parity error on Write RO insturction, the DIU will complete the instruction and set the appropriate flag bit in the Error Status word. An additional register is used to save the error status conditions for each message. The Read Error Status instruction reply will contain the error status word from the previous message as data. The error status logic is contained on three printed-circuit boards.

Error Status 1 (3339046)

The block diagram for the Error Status 1 logic is shown in Figure 4.5-1. The RI blank word counter is preset to a count of 6 by detection of D words on the RI line and during the WC word and the next following word to allow reception of the serial RI data. The counter is decremented by the decoded RI blank word pulse during a Read RI instruction and when a count of zero is detected, a data level and clock pulse are sent to the Error Status Registers.

The error detect latch supplies the instruction termination signal (ERREN) to the Reply Sequencers. D word parity errors during Write RO instructions are inhibited from setting the latch, but are indicated on the front panel display. Errors detected by the Error Status 2 logic (ERR RESET 1) are OR'ed with the error detect logic shown to set the error latch. Errors detected on this board are as follows:

- Word count word errors
- Greater than 5 blank words on RI line

- o No response on RI line

Control signals for the Error Status Registers are as follows:

- o Error status register load (ESLD)
- o Saved error status register load (SES LD)
- o Error status holding register clear (ESH CLR)
- o Buffer read clocks for the error status registers (ESCD & ESDCP)

The ES WD display register supplies serial error status data to the front panel display logic.

Error Status 2 (3339038)

The block diagram for Error Status 2 logic is shown in Figure 4.5-2. The error detect logic supplies data levels and clock pulses to the Error Status Registers for the following error conditions:

- o Word sync error
- o A word parity
- o Illegal op code
- o WC word parity
- o WC word sequence error
- o D word parity
- o RI error status parity

With the exception of the D word parity errors, the detected error signals are OR'ed with the two RI error conditions detected in the Error Status 1 logic to form the error reset 1 signal (ER RESET 1)

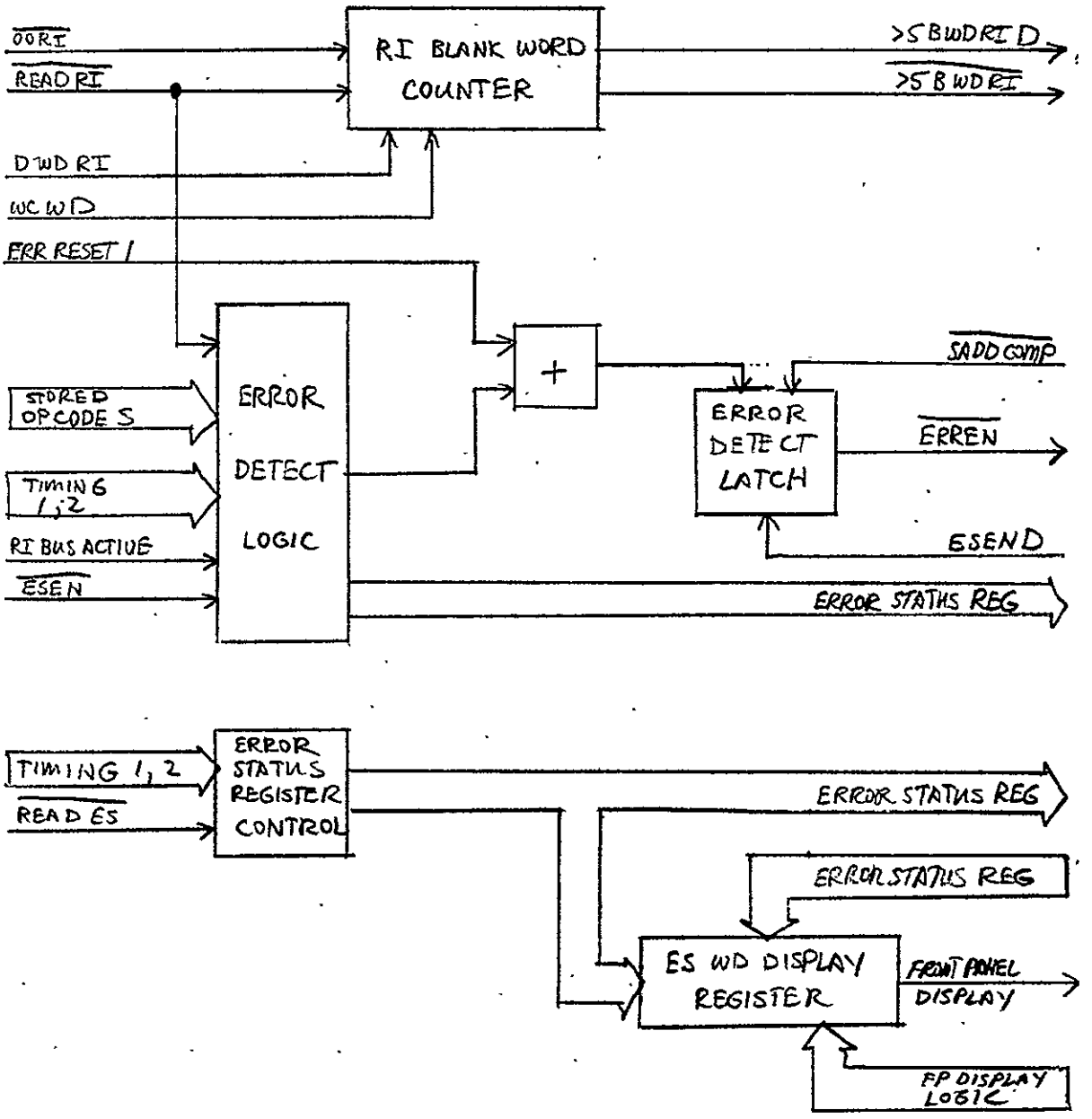
Supervisory bus parity errors are detected by resetting a flip-flop during the y-phase of each parity bit, and counting 1's in the following word. The RI error status word is tested for three one's in the WS, C1, and C2 bits, and parity is computed for information bits BO through B4.

Blank words on the supervisory bus are counted by presetting a counter to a value of 6 during the WC word and bus D words. The counter is decremented by the decoded blank word prefix until a count of zero is reached. The counter clock is inhibited for read instruction by resetting a latch with the 01 WC word prefix.

The DIU/DIU transfer flag is set by clocking the decoded OP code through a Z stage shift register by the addressed A word pulse. The first state inhibits the DIU reply for the next addressed message. The outputs of both register stages are OR'ed to form the DIU/DIU flag bit (DIUT FLAG). The register is reset to the normal condition by an A WD parity error in the DIU/DIU instruction, the RESET instruction, or the end-of-message pulse (DEOM) from the data transfer instruction.

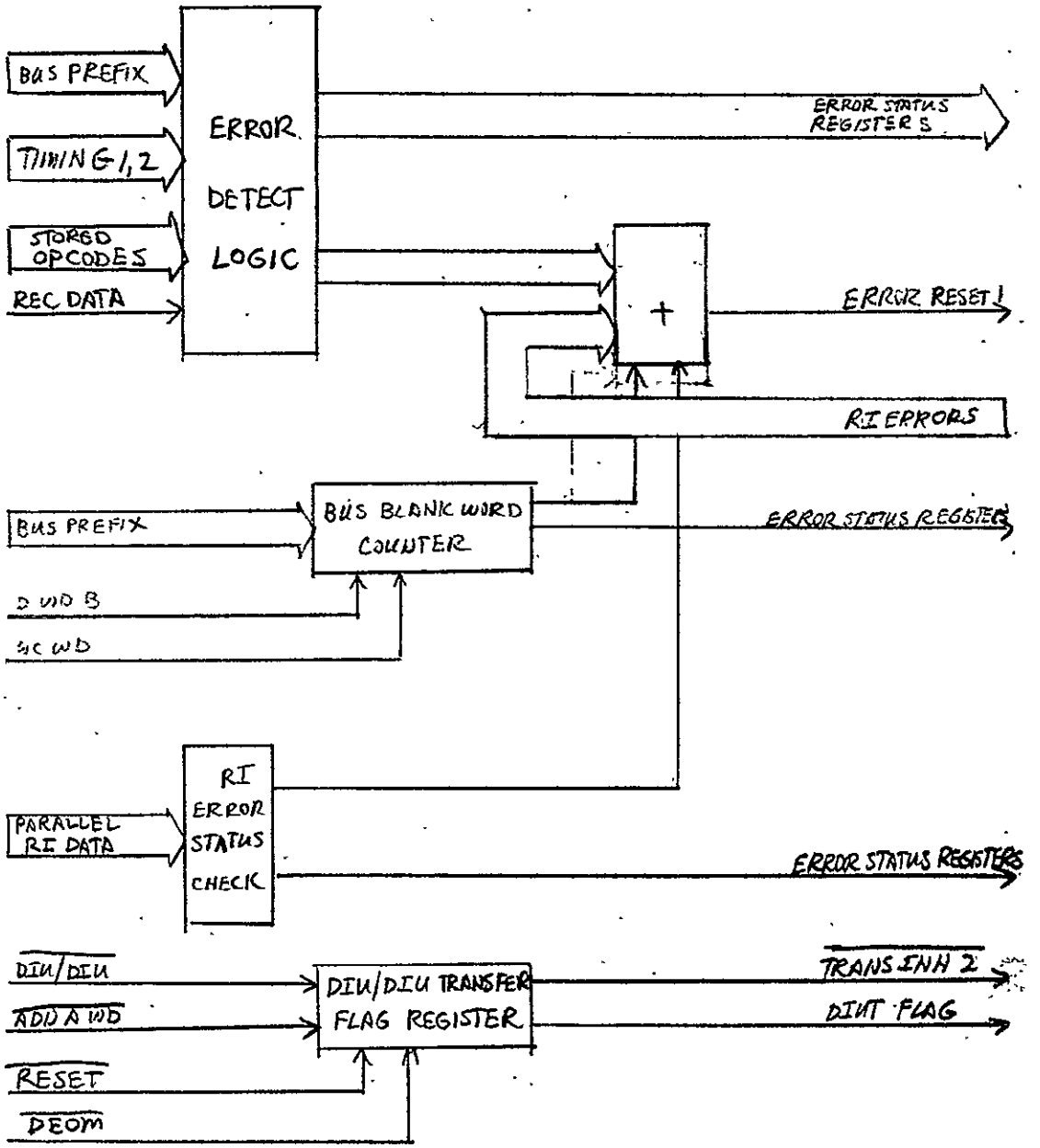
Error Status Registers (3339048)

The block diagram for the Error Status Registers is shown in Figure 4.5-3. The holding register for 10 bits of the error status word is located on this board. The DIU/DIU transfer flag and the RI error status parity error bit are implemented on the error status logic board. Subsystem error status bits are received from the RI/RO logic. Two 16-bit parallel-to-serial registers supply the error status word and stored error status word to the transmit logic. The error status data is buffered by two flip-flops to synchronize the data with the DIU transmitter timing.



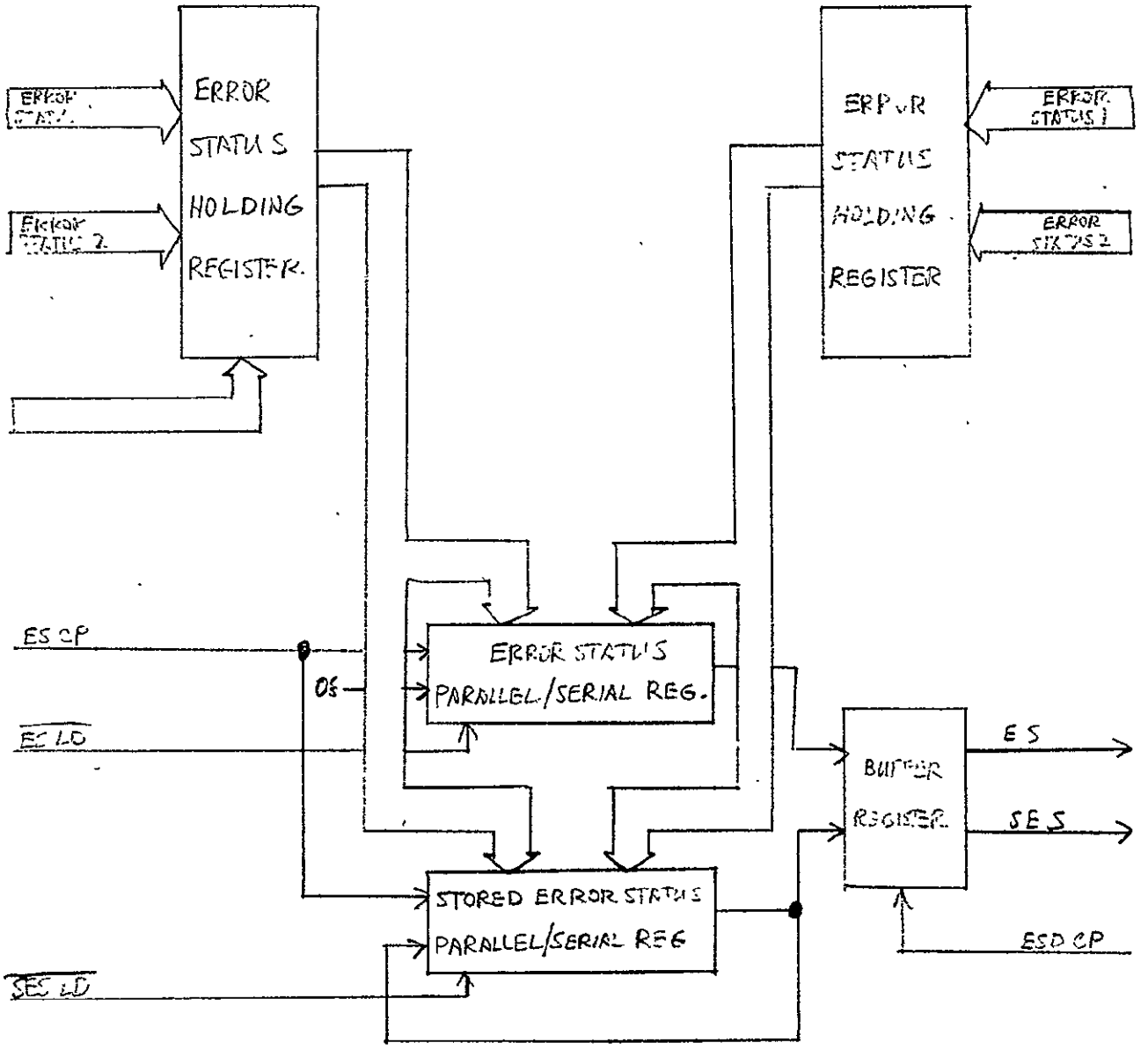
ERROR STATUS 1

FIGURE 4.5-1



ERROR STATUS 2

FIGURE 4.5-2



ERROR STATUS REGISTERS

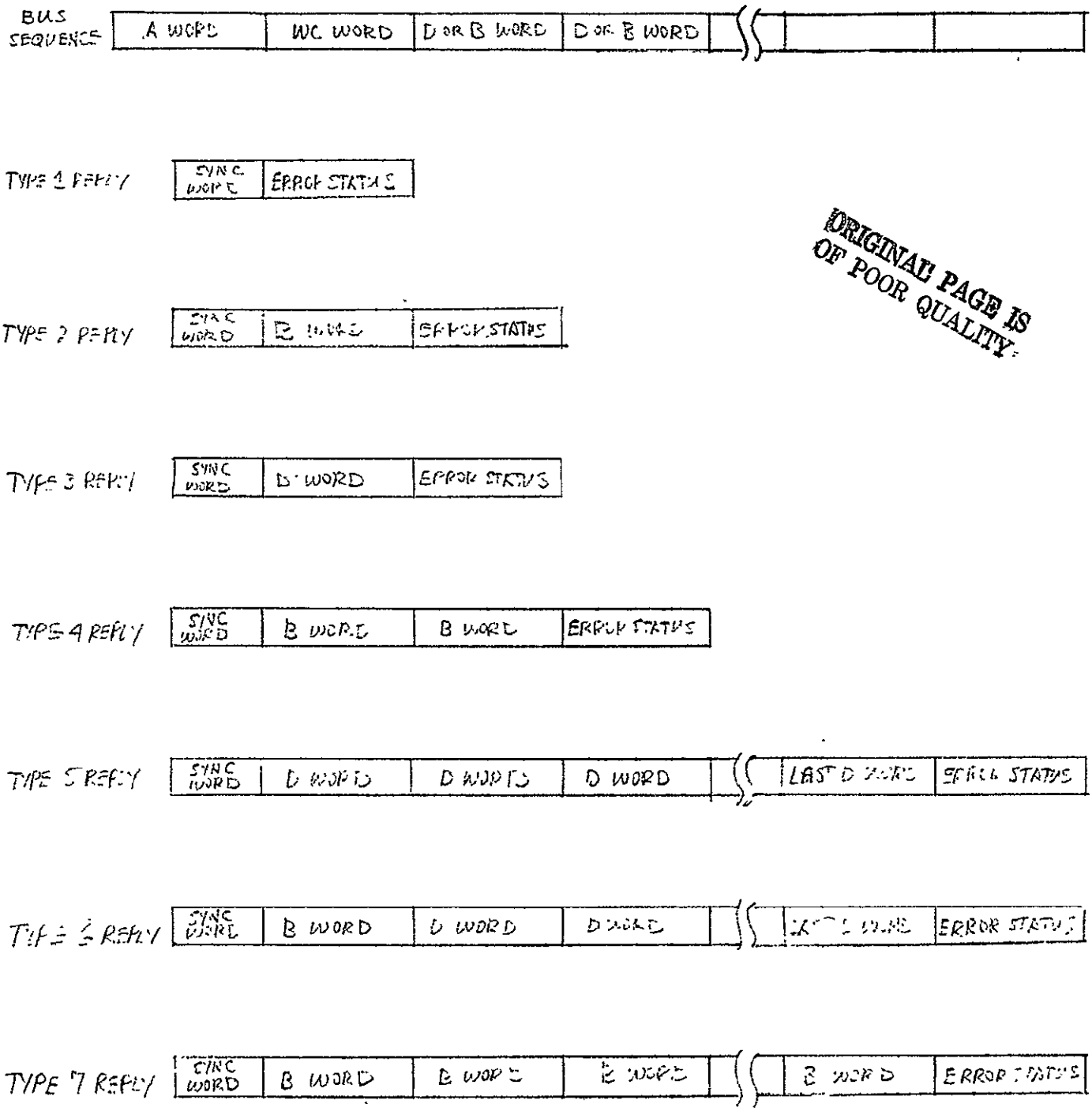
FIGURE 4.5-3

4.6 REPLY SEQUENCERS (3339028 & 3339034)

The reply sequence logic is contained on two printed-circuit boards and supplies timing signals to the DIU transmitter and the receive logic for the OP code register clock and terminating the OP code enable and stored address compare signals. Seven types of reply sequences are generated as shown in Figure 4.6-1. The instructions for each type of sequence are as follows:

Type 1:	DIU to DIU Transfer Read DI Changes (No Changes) Read AI's Exceeding Deltas (None Exceeded)
Type 2:	Reset
Type 3:	Read Error Status Read DI Monitor Control
Type 4:	Write DI Monitor Control
Type 5:	Read AI Deltas Read DI's Read DO Status
Type 6:	Read DI Changes (With Changes) Read AI Exceeding Deltas (When Exceeded) Read AI's Read RI
Type 7:	Write DO's Write AO's Write AI Deltas Write RO

The error enable signal (ERREN) from the error status logic forces the reply sequencers to terminate the current operation and insert the error status word into the DIU reply.



REPLY SEQUENCER

FIGURE 4.6-1

4.7 TRANSMIT LOGIC

The DIU transmit logic is contained on two printed circuit boards. Included in this section are the sync word generator, reply data multiplexer, and the reply transmitter interface.

Transmit Logic (3339030)

The block diagram for the Transmit Logic is shown in Figure 4.7-1. The sync word register receives buffered data from the front panel address thumbwheel and the hardwired sync code (111101). The parity outputs of the two address thumbwheels are combined to form the parity bit for the unit address. The sync word register is held in the load condition until the Sync Word Enable (SWEN) signal is received from the Reply Sequencers.

The Read Data Select gates are used to multiplex reply data from the DI, AI, DO, RI, and Error Status logic. Multiplexing of the various types of reply data from each section is implemented in the logic for that section.

Word prefixes and parity bits are inserted in the reply by the prefix/parity select gates. RI data and reply blank words inhibit the prefix/parity function. Parity for other data is generated by resetting a flip-flop during the WS bit and counting the number of zeroes in the reply data with the 16 bit write clock. Word prefixes are generated by a four-line to two-line encoder with enable signals from the reply sequencers.

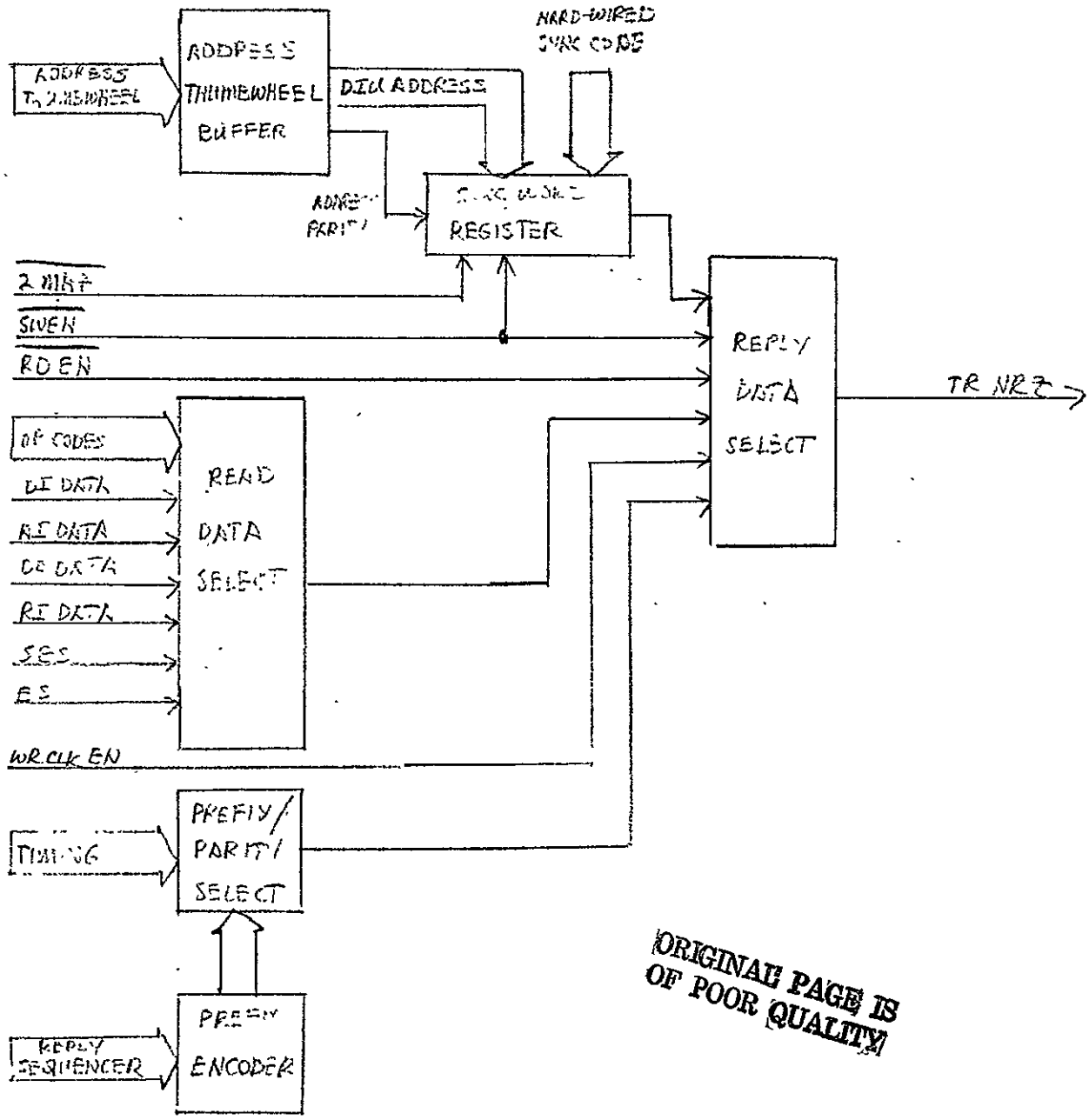
DIU Transmitter (3339026)

The block diagram for the DIU Transmitter is shown in Figure 4.7-2. Reply NRZ data from the transmit logic is converted to Bi-phase data by combining the NRZ data with the 2 MHz system clock in an Exclusive -OR gate. Encoding glitches are removed by clocking the Bi-phase data through a flip-flop with the 4 MHz system clock.

The transmit enable sequencer generates an enable signal to the transmitter that is synchronous with the delayed Bi-phase data. The Transmit Inhibit 1 signal inhibits DIU replies during the power-on initialization sequence. The Transmit Inhibit 2 signal inhibits the next reply after the DIU receives a valid DIU-to-DIU transfer instruction.

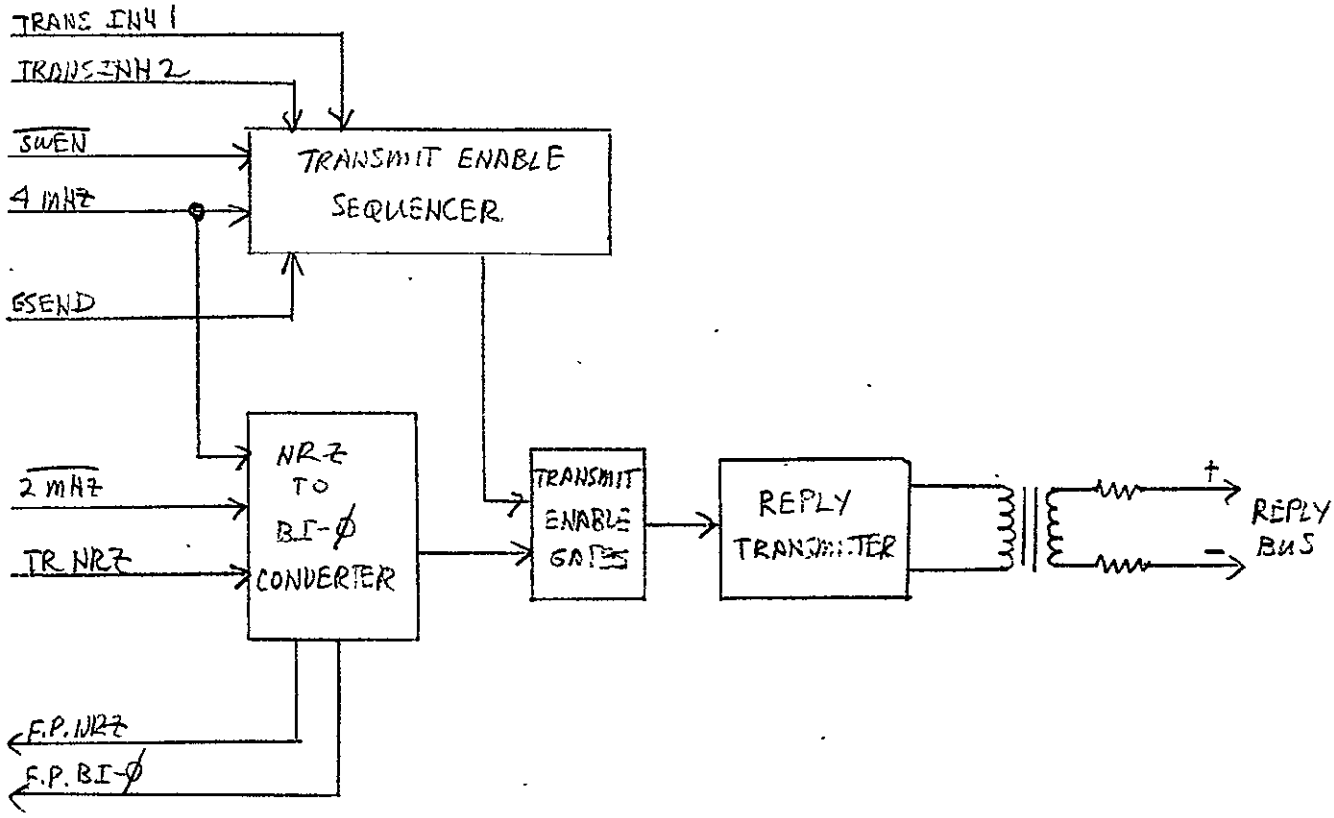
Front-panel test points are provided for the reply NRZ and Bi-phase data. The NRZ data is delayed through a flip-flop to synchronize the data with the reply Bi-phase.

The reply transmitter is implemented with a push-pull pair of transistors with Baker clamp diodes to prevent saturation, and a center-tapped output transformer. At the end of each reply, both transmitter transistors are turned on for a period of 1/2 bit to reduce ringing on the reply bus.



TRANSMIT LOGIC

FIGURE 4.7-1



DIU TRANSMITTER

FIGURE 4.7-2

4.8 DISCRETE INPUTS

The DIU circuitry for interfacing the Discrete Inputs consists of two control boards, DI Mux Control #1 and #2, and up to 8 DI multiplexer boards. The multiplexer boards are classified as DI #1 and #2 modules. The #1 module interfaces high-level and low-level inputs, with a jumper wire provided for selecting the corresponding input threshold. The #2 modules interface with the DI Sink inputs.

DI Mux Control #1 (3339064)

The block diagram for the DI Mux Control #1 is shown in Figure 4.8-1. DI group addresses for Read DI instructions and the DI scan operation are controlled by the DI address counter. The mux group encoder receives inputs from a grounded pin on each multiplexer module and outputs a binary number equivalent to the highest-order group implemented. When a compare is detected, the address counter is reset to group 0.

The three MSB's of the address counter are decoded by the group select mux to provide enable signals to the tri-state output gates on the selected DI multiplexer. The 16-bit DI outputs are buffered by Schmitt-trigger gates and loaded into a 16-bit register. For the Read DI instruction, the data is then shifted serially to the data multiplexer on the DI Mux Control #2 board. For the scan operation, the register is operated in the parallel mode and loaded at a rate of one group per microsecond. For the Read DI changes instruction, the address select multiplexer selects the address counter for the change status scan, and then is switched to the DI change addresses generated on the DI Mux Control #2 board.

The memory address register provides a delayed address for the DI scan function. The LSB of the address is used as a byte select bit for the 16-bit DI data. The selected byte is compared to the data outputs from the DI

Status Table memory and a compare signal (DICOM) is output to the DI Mux Control #2 board. The Status Table memory is set to all 0's during the power-on initiate sequence, and then is updated only during the Read DI changes instruction. Reply DI data for this instruction is loaded into the DI Change Data register for transmission.

DI Mux Control #2 (3339074)

The block diagram for DI Mux Control #2 is shown in Figure 4.8-2. Stored OP codes from the Receive Logic are encoded into a 3-bit binary code by the DI OP Code encoder. The Read DI Changes sequencer utilizes three inputs of the encoder to provide the reply sequence of Change Histroy and Change Status for the DI Pointer Word, followed by the DI Change data.

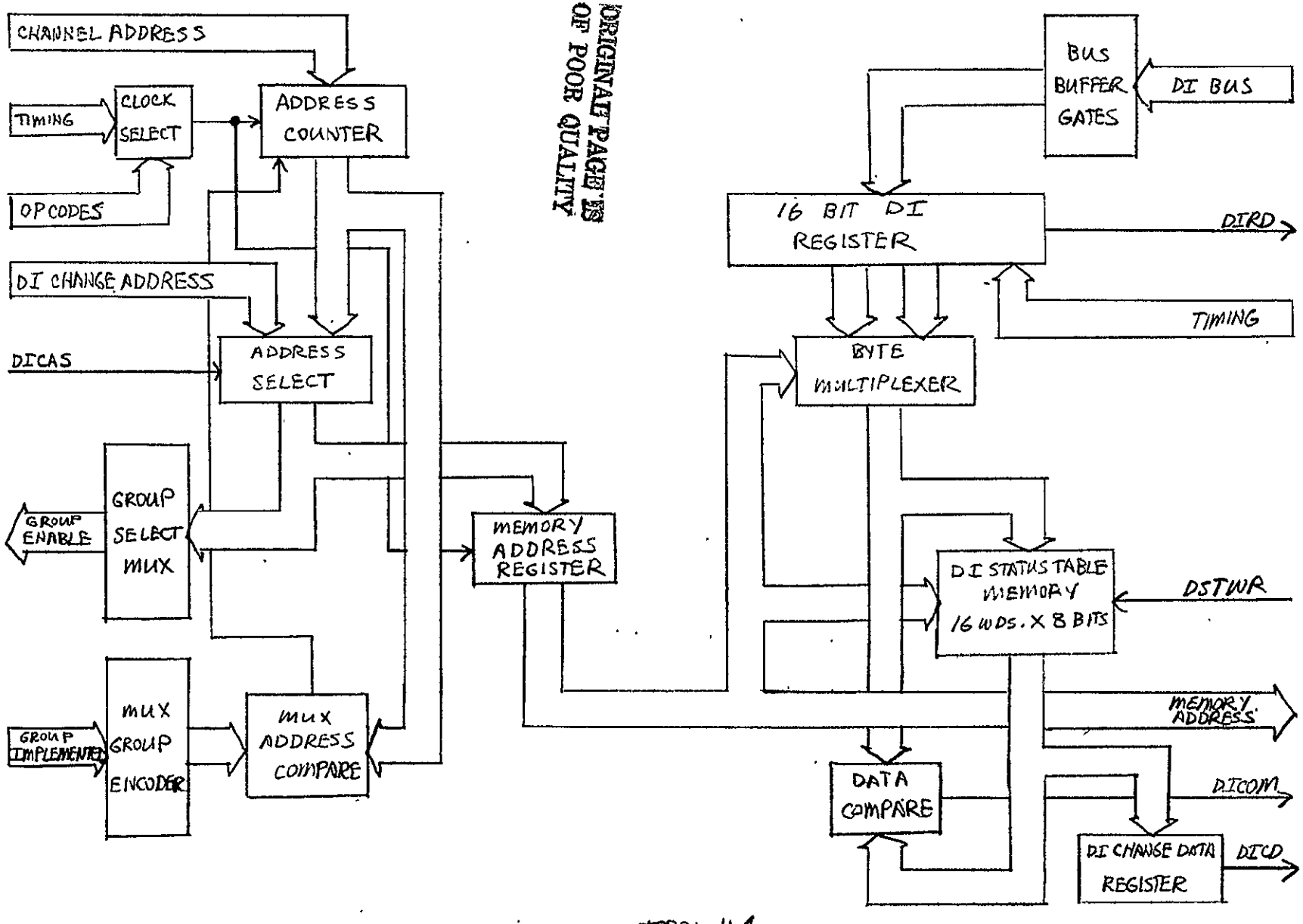
The encoder outputs are routed to the DI timing mux to provide register and counter clocks for the DI OP codes and the DI scan operation, and to the DI data multiplexer for read and write instructions. The data multiplexer receives inputs from the Change History register, Change Status Mux, and the DI Change Data register (DICD) for the Read DI Changes instruction. The output of the DI monitor control register and the delayed supervisory Bus data (NRZ data) are selected for the Read and Write DI Monitor Control instructions. Serial data from the DI register (DIRD) is selected for the Read DI's instruction. Output data for read instructions is buffered by a flip-flop for synchronization with the reply data, and output to the Transmit logic.

The memory address bits from the DI Mux Control #1 board are used to select masking bits from the DI Monitor Control register. The selected masking bit is gated with the DI compare signal (DICOM) and is routed to the DI change decoder. The decoder receives the 3 MSB's of the memory address and provides clock signals to the DI Pointer Word register. The outputs of this

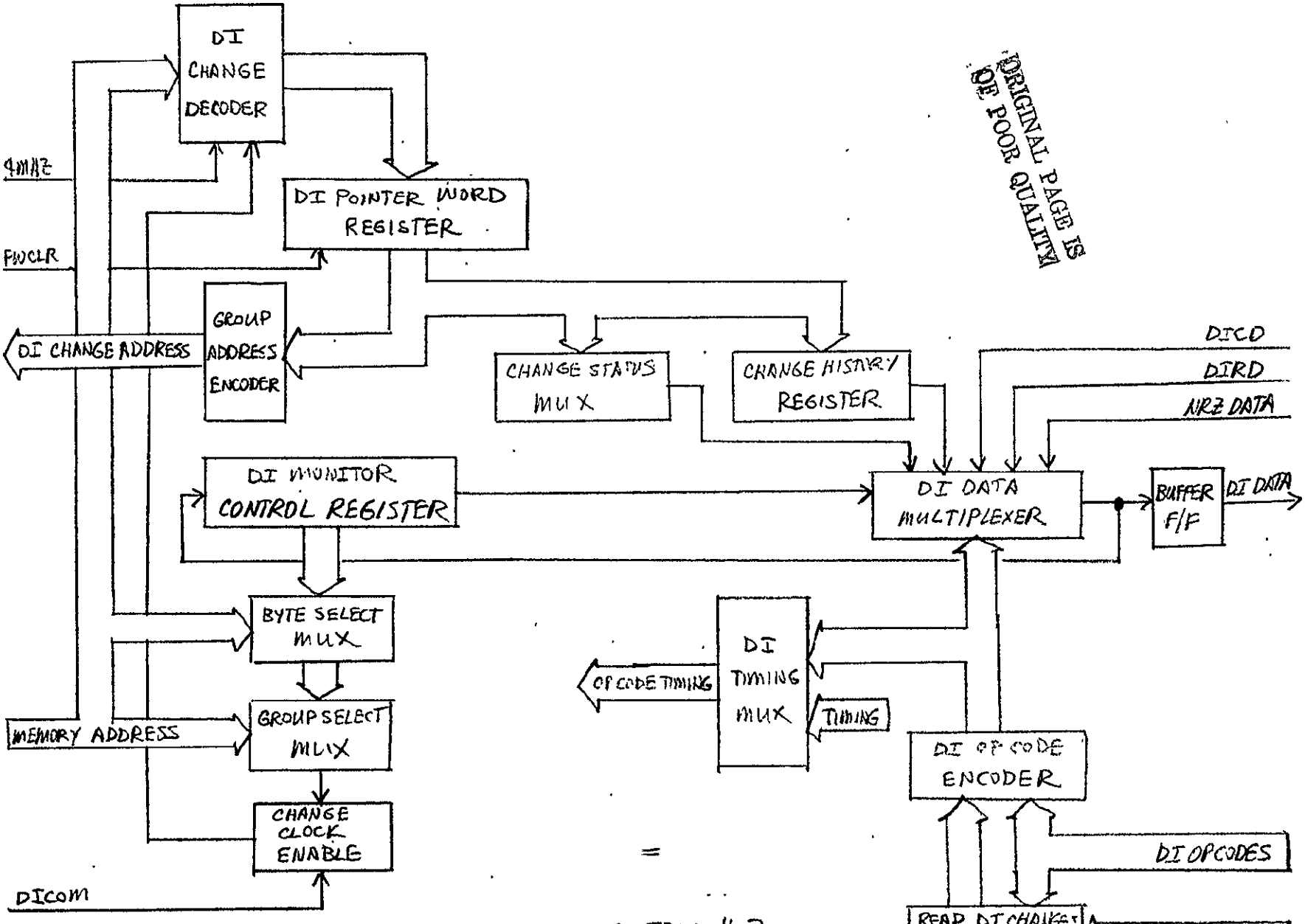
register are encoded into a DI change address and routed to the Change History register and the Change Status Mux. When a valid Read DI Changes instruction is received, the Pointer Word register is loaded into the Change History register for transmission, the Pointer Word register is cleared by the PWCLR signal, and then updated by the Change Status scan. The Change Status bits are multiplexed by a three-bit counter and an eight-to-one line multiplexer for transmission.

Discrete Input Modules (3339006 & 3339018)

Discrete Inputs are interfaced by a two millisecond filter for rejection of contact bounce, a level comparator, and photo-isolator circuit. The input diode and a zener diode at the comparator input provide protection against overvoltage fault conditions. The level comparators utilize hysteresis to prevent oscillations due to the slow rise-time of the filter output, and drive the LED input of the photo-isolator. The isolator outputs are routed to the tri-state bus gates controlled by the DI address counter, and a 16-bit parallel-to-serial register for the front panel display.



DI MUX CONTROL #1
FIGURE 4.8-1



DI MUX CONTROL # 2
FIGURE 4.8-2

4.9 DISCRETE OUTPUTS

The Discrete Output circuitry is contained on the DO Mux Control board, and up to 8 Discrete Output modules. The DO Mux Control logic provides the interface for the Write DO and Read DO status instructions. Registers for the front panel DO display are implemented on the DO modules.

Discrete Output Mux Control (3339066)

The block diagram for the Discrete Output Mux Control logic is shown in Figure 4.9-1. Delayed serial data from the Receive Logic (NRZ Data) is shifted into the DO Serial/Parallel register by the gated write clock. Channel addresses are loaded into the DO address counter by the channel address load signal (CALD) at the beginning of the instruction execution sequence, and the counter is then incremented at the DIU word rate.

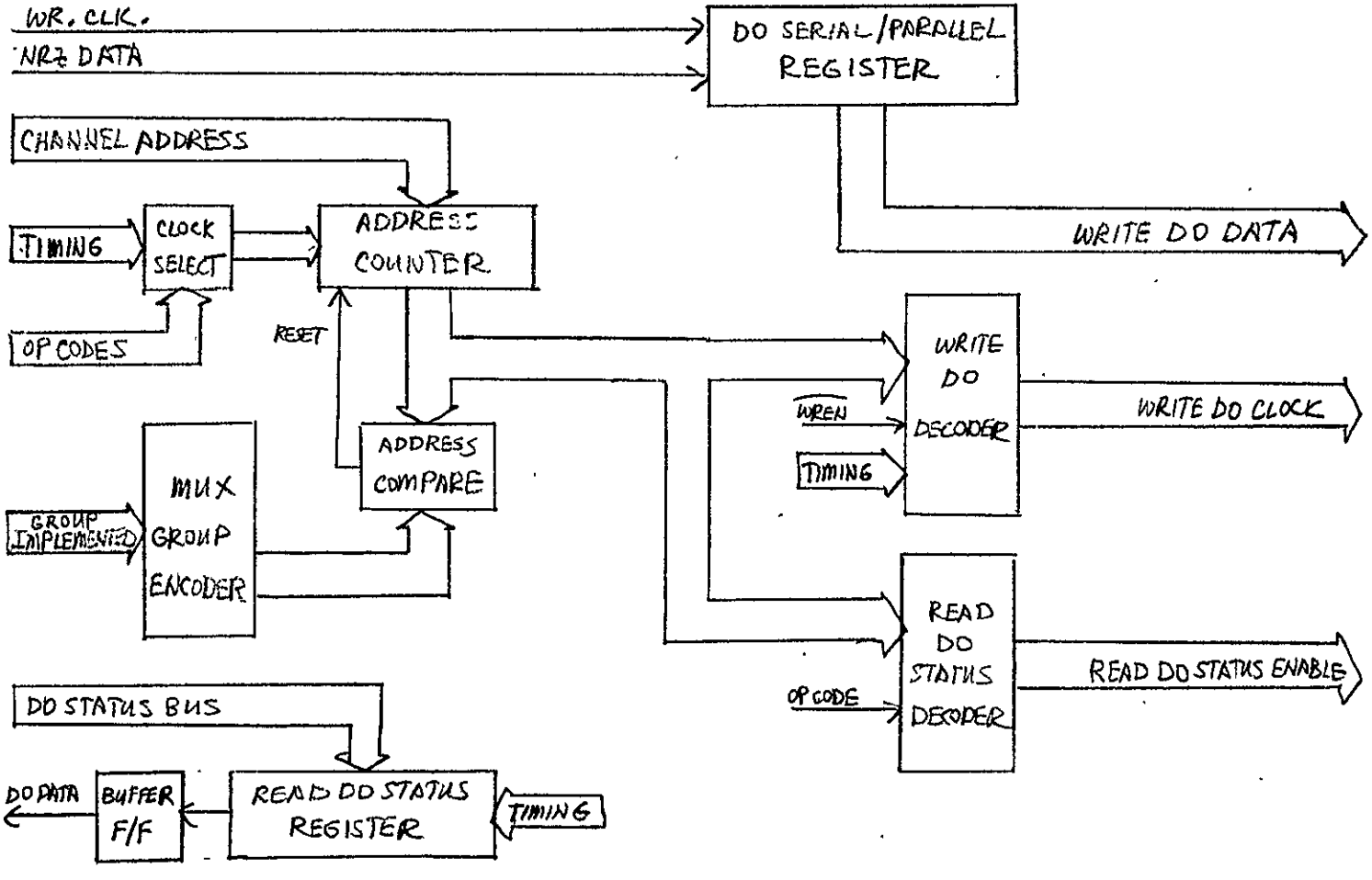
The Mux Group Encoder receives inputs from a ground pin on each DO module, and outputs a binary number equal to the highest-order group implemented to the address comparator. When an address compare is detected, the address counter is reset to group 0. The address counter outputs are decoded to provide clock signals for the DO data holding registers on the DO module boards. The Write Enable (WREN) input inhibits the clock signals and the address counter clock when blank words are present on the Supervisory bus.

The Read DO Status decoder provides enable signals to the tri-state DO status gates on the DO modules. The 16-bit output from the enabled module is loaded into the Read DO Status register, and shifted through a buffer flip-flop by the gated Read Clock signal to the Transmit logic.

Discrete Output Module (3339004)

The Discrete Output module contain a holding register for maintaining the DO data between instructions, tri-state buffer gates for the Read DO status instruction, a front panel display register, and photo-isolator circuits to drive the DO interface circuits. The holding register is cleared by the Power-On Reset signal (POR) to turn off the Discrete Outputs when power is applied to the DIU.

The photo-isolator outputs are applied to voltage comparators with a 1.22 volt reference input. A diode from the photo-isolator output to the Discrete output clamps the comparator in the off state for short-circuit fault condition. The supply voltage for the comparators is gated by a threshold detect filter circuit connected to the external supply voltage from the subsystem to inhibit the Discrete Outputs when external power is first applied from the subsystem. The comparator output drives a PNP Darlington transistor switch to supply the Discrete Output levels. A clamp diode to the DO return line provides protection against unsuppressed inductive loads.



DISCRETE OUTPUT MUX CONTROL

FIGURE 4.9-1

4.10 ANALOG OUTPUTS

The Analog output circuitry is contained on the AO control board and two AO Module boards. The AO Control board provides the interface for the write AO instruction and the initialization function for setting the AO's to zero volts when power is applied to the DIU. Each AO module board contains the circuitry for two Analog outputs, with jumpers for the address wrap-around function and the monitor output to the Analog Input multiplexers.

AO Control Logic (3339072)

The block diagram for the AO Control logic is shown in Figure 4.10-1. Isolation between the DIU ground and the common AO return is provided by transformer coupling to the AO Data Register and the holding registers on the AO modules.

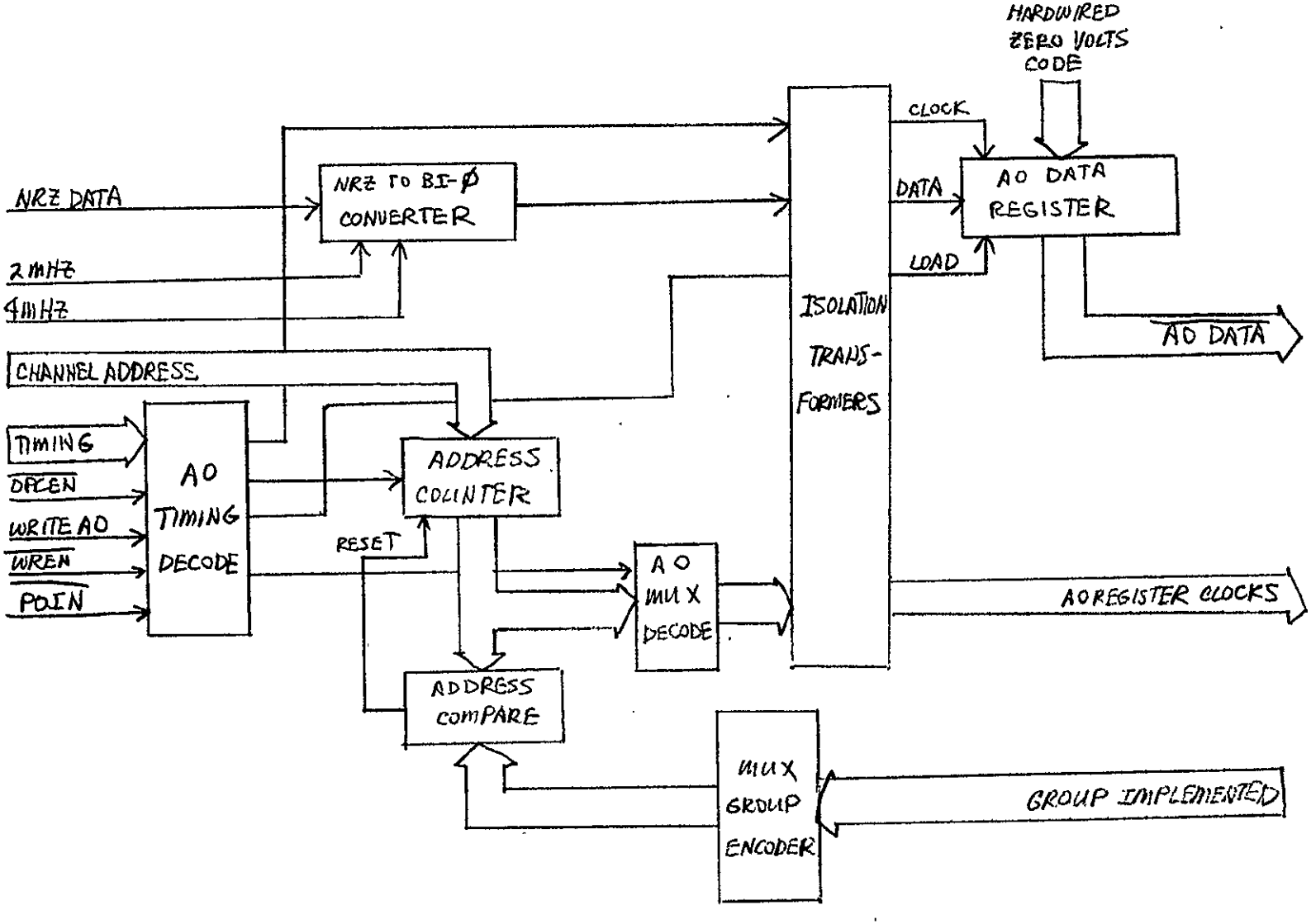
Serial NRZ data from the Receive Logic is converted to Bi-phase data to prevent transformer saturation and shifted into the AO Data register. The channel address for the Write AO instruction is loaded into the address counter and incremented at the DIU word rate. The address wrap-around function is implemented in the same manner as discussed for the DI's and DO's. The channel address bits are decoded to provide load clocks for the AO Module holding register. The power-on initialization function is implemented by operating the AO Data register in the parallel mode, and loading a hard-wired code for zero volts output during the initialization sequence. The address counter is incremented during this time to provide clocks for all AO modules.

Analog Output Module (3339020)

The circuitry for each Analog Output consists of a holding register for Write AO data, a digital-to-analog converter (DAC), and and output amplifier.

Complemented data from the AO Data register is supplied to the holding register to meet the interface requirements for the DAC. The offset input of the DAC is biased with a 1.22 volt reference zener and a selected input resister to provide 0 volts output for an input code of 00000011. The DAC gain is adjusted by select resistors to provide an output of 5.000 volts for an input code of 11111100.

The current output of the DAC is converted to a voltage output by the output amplifier. Clamp diodes at the DAC output provide protection for the DAC internal circuitry during power transients. The output amplifier is internally protected against short-circuit fault conditions. A series output resistor and feedback capacitor provide amplifier stability for capacitive loads. The monitor output to the Analog Input multiplexer is protected against over-voltage conditions on the AI's by a series resistor and clamp diodes to the supply voltage lines for the output amplifier.



AO CONTROL
FIGURE 4.10-1

4.11 RECORD IN/RECORD OUT

The Record In/Record Out circuitry provides the interface for read and write messages with up to eight external subsystems. The interface logic and RO transmitters are contained on two printed-circuit boards. The RI receiver is located on the same board as the Supervisory Bus receiver. The receivers are identical with the addition of 8 input transformers and an input multiplexer on the RI receiver.

RI/RO Interface Logic (3339070)

The block diagrams for the RI/RO Interface logic is shown in Figure 4.11-1. Supervisory Bus NRZ data from the Receive Logic is converted to Bi-phase data for transmission on the RO data outputs. The WC word prefix bits are modified for Read RI and Write $\overline{RO}$ instructions by the WC Word prefix logic. Since this function modifies the parity bit for the WC Word, the parity bit is complemented during the WC word.

The NRZ data from the RI receiver is synchronized with the DIU timing by alternately shifting the data into two 20-bit serial-to-parallel registers. Register selection is controlled by alternating the RI clock from the receiver between the two registers. The select logic is initiated by the bus active signal from the RI receiver and an RI/RO OP code signal (ROPC) from the RO Transmitter board. The output of a 20-bit ring counter is used to toggle a flip-flop for clock and data selection.

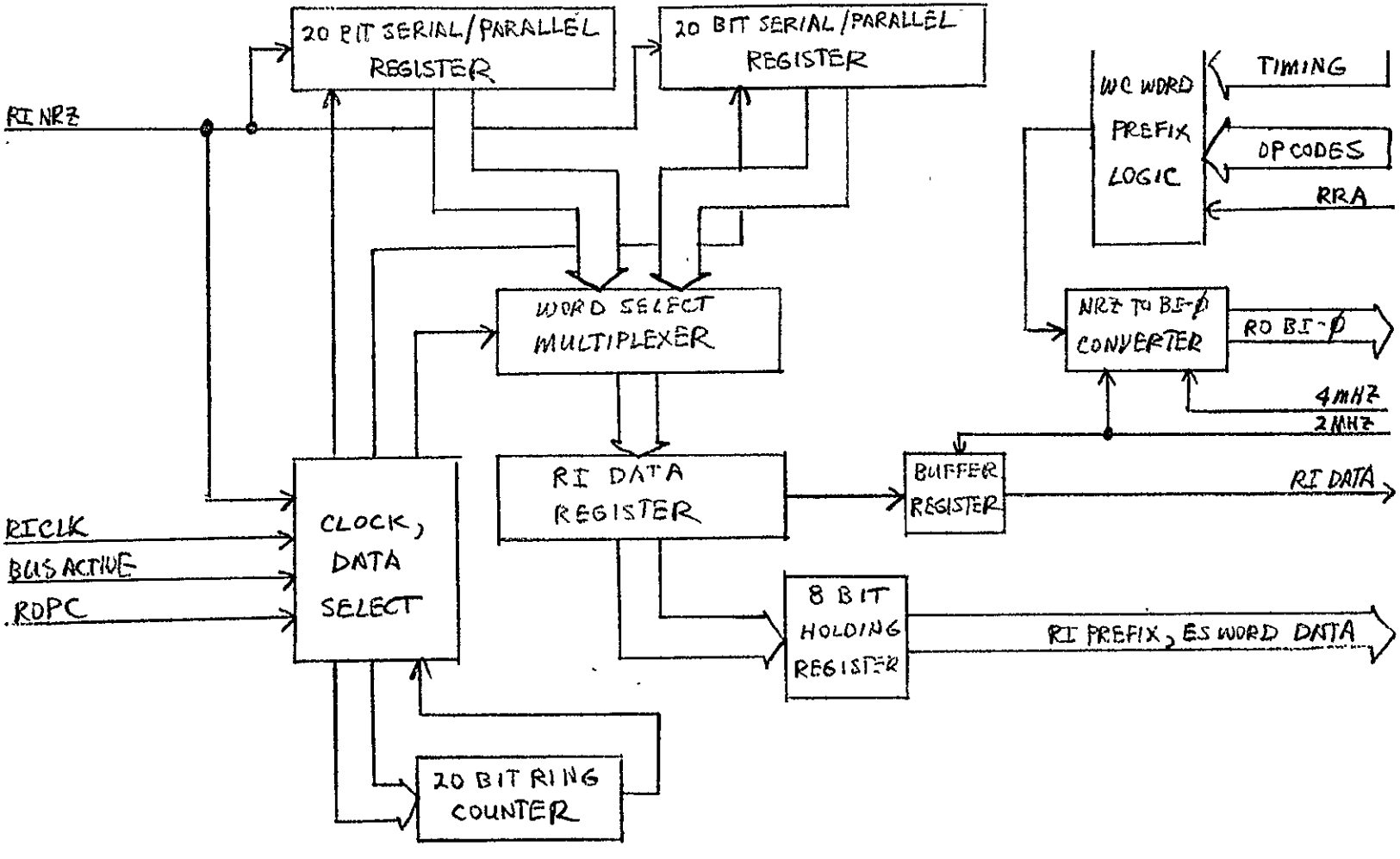
The selected data is loaded into the RI Data register for shifting to the Transmit logic. Eight parallel outputs from the register are loaded into a holding register for word prefix identification and Error Status word parity tests.

RI/RO Transmitter (3339016)

The RI/RO Transmitter board provides the channel address and OP code storage functions and the clock and data transmitter circuits. A four-bit register is utilized to store the 3-bit channel address and an enable signal (ROPC) resulting from OR'ing the Read RI and Write RO OP codes. The register is loaded by the Channel Address load pulse (CALD) and cleared by the Power-on-reset (POR) signal and the Reset instruction.

The stored channel address bits are output to the RI receiver multiplexer for channel selection, and supplied to two data decoders to select the corresponding RO clock line for activation. The data inputs are driven by buffered 4 MHz clocks from the RI/RO Interface logic.

The RO transmitters are discrete-component designs utilizing a push-pull pair of NPN transistors to drive a center-tapped output transformer. Diode Baker clamps are used on each transistor to prevent saturation. A current-limiting resistor in series with the supply lead to the center-top of each transformer provides short-circuit protection for the RO outputs.



RI/RO INTERFACE LOGIC

FIGURE 4.11-1

4.12 ANALOG INPUTS

The Analog Input circuitry provides the interface for up to 128 AI channels, analog-to-digital conversion, and delta checking for all channels. Associated with the delta checking function is a 400 word by 8 bit memory for storing programmable delta values, a reference AI value, and an exceeding delta flag for each channel. During the power-on initialization sequence, the delta values are loaded with maximum values (all Ones), the reference value are loaded with all zeros, and the exceeding delta flags are set to the none exceeded condition.

AI Mux Address Control (3339054)

The block diagram for the AI Mux Address Control logic is shown in Figure 4.12-1. Channel addresses from the Receive logic are utilized for the Read AI and Read and Write AI Delta instructions. Since the Read AI instruction is referenced to two channels, and the Delta instructions are referenced to a single channel, the clock/address select multiplexer performs an address shifting function for the channel address bits. The address MSB for the Delta instructions (RWAO) is derived from stored OP codes on the AI Memory Function Select board.

When the DIU is not being addressed for an AI instruction, the AI address counter scans through all the AI channels implemented to test for exceeding delta conditions. To allow for multiplexer settling time, the AI channels are each addressed for one word time by supplying odd and even numbered channel addresses (A Mux and B Mux addresses). When the scan operation is interrupted for an AI instruction, the scan address is stored in a register to allow resuming the scan at the same address when the instruction sequence is completed. The address wrap-around function for AI addresses is implemented in the same manner as discussed for the DI's (Section 4.8). The

memory address select multiplexer performs the same address shifting function as the channel address select multiplexer.

AI Memory Address Control (3339056)

The block diagram for the AI Memory Address Control logic is shown in Figure 4.12-2. The logic in this section performs the address select functic for the Read AI's Exceeding Delta instruction, and for reading and writing in the exceeding delta flag portion of memory.

An eight bit register is used to store an exceeding delta flag for each of the AI groups implemented. The three MSB's of the memory address are decod to supply clocks to the register during the scan operation, and during Read AI Exceeding Deltas and Write AI Deltas instructions when the exceeding delta flags from memory indicate that all channels in a group have been rese

The outputs from the Group Delta Flag register are encoded into a three-bit binary code to form the three MSB's of the channel address for the Read AI Exceeding Delta instruction. A similar encoder on the AI Memory board generates the remaining address bits.

AI Memory Function Select (3339060)

The block diagram for the AI Memory Function Select logic is shown in Figure 4.12-3. Stored OP codes from the Receive Logic are encoded into a three-bit binary number to access instruction sequences in the AI memory control PROM, and for reply data and instruction timing for AI scan and instruction sequences.

The three MSB's of the PROM address (PRA3-PRA5) and the PROM enable signal (PRE2) are stored in a register. The PROM enable signal is shifted

through an additional input to the register to disable the AI memory for one word time following AI instruction while the AI channels for the scan operation are being encoded. The write enable signal (WREN) inhibits the AI memory for blank words on the Supervisory bus during the Write AI Deltas instruction.

Reply data for AI instructions is selected from the analog-to-digital converter output (ADCD) for Read AI's, the AI memory output data register (MOD) for Read AI Deltas, and the exceeding delta address register for the Read AI Exceeding Deltas instruction.

AI Memory Sequence Control (3339062)

The block diagram for the AI Memory Sequence Control logic is shown in Figure 4.12-4. This board contains the control PROMs for generating AI memory sequences and AI logic signals for the AI scan operation and AI instructions. The PROM output signals and timing for the AI logic are shown in Figure 4.12-5.

Three address bits from the AI Memory Function Select board select the control PROM sequence. The sequence counter steps the PROM address LSB's through the eight steps of each sequence. The AI Memory Sequence Initiate pulse (AMSIN) starts the PROM sequence at the bit time required for each instruction and the AI scan operation.

The PROM outputs are gated with timing and control signals to supply AI memory and logic timing. The sign bit from the subtractor (SUBC4) on the AI Memory Data Interface board is stored in a flip-flop to control the access of plus or minus deltas during AI scans.

AI Memory Data Interface (3339058)

The block diagram for the AI Memory Data Interface logic is shown in Figure 4.12-6. Parallel data from the ADC is stored in a holding register for delta checking during AI scans. The reset input to the register and the data complement gates are used for writing 1's and O's into the AI memory.

During AI scans, the reference AI value from memory is stored in the memory output data register. The current AI value from the ADC is complemented, and the two values are input to an eight-bit to subtract the data values. Exclusive -OR gates at the adder output are controlled by the adder sign bit output to generate an absolute-value result from the subtraction. The plus or minus delta value is read from memory and compared to the subtractor output to test for exceeding delta conditions. The memory output data register is used as a **parallel**-to serial register for the Read AI Deltas and Read AI Exceeding Deltas instructions.

Eight chip-enable signals for the AI memory are generated by decoding three address bits from the AI Memory Address control logic. The memory timing requires stable address and data inputs before the chip-enable inputs are activated. The AI Memory Enable timing pulse (AMEN) supplies these timing requirements. The eight chip-enable outputs are activated simultaneously for reading and writing in the AI delta and AI reference portions of memory. When the exceeding delta flags are accessed, the decoder activates only one of the chip-enable outputs.

AI Memory (3339052)

The AI memory is implemented with CMOS 512 bit devices powered by a +10 volt supply voltage. Open-collector interface gates for all input signals perform the voltage translation from the 5 volt TTL AI logic levels. Memory data

outputs are interfaced with CMOS-to-TTL buffer gates. The data outputs are encoded into a three-bit binary value to generate address bits for the Read AI Exceeding Deltas instruction. The EDFGS output from the decoder provides a signals to indicate the presence of an exceeding delta flag in the eight channels accessed. The AI memory organization is shown in Figure 4.12-7.

AI Multiplexer (3339002)

The AI multiplexer modules are implemented with two integrated-circuit 8-channel differential multiplexer devices. Overvoltage protection for ± 32 volt input fault conditions is provided by the devices. Channel interaction due to an overvoltage on one input is eliminated by diode-clamping the multiplexer outputs to a voltage that is 1.2 volts less than the supply voltage. To improve multiplexex settling time, the supply voltages are derived from a floating output from the DIU power supply. The returns for these outputs are driven by the common-mode output from the AI differential amplifiers.

Guard Amplifier & Group Select (3339068)

The circuitry on this board provides the two AI reference voltages, the amplifiers for driving the floating AI supply voltages, and the AI multiplexer select decoders.

The reference voltages are generated by a temperature-compensated zener diode biased by an operational amplifier operated in non-inverting mode. The circuit gain is controlled by select resistors to provide a +10 volt output. Two resistive dividers are used to generate the High Cal output of 3.340 volts and the Low Cal output of 1.640 volts. The reference voltages are wired to AI channels 0 and 1. Jumpers are provided on the board to allow the option of using these inputs for external channels.

Group Select Mux & Sample/Hold Amplifiers (3339011)

The circuitry on this board provides the AI group multiplexers, input buffer and differential amplifiers, and the sample-and-hold amplifiers for the A Mux and B Mux analog inputs.

The differential outputs of the AI multiplexers are selected by the group address bits from the AI mux control logic to supply inputs to the buffer amplifiers. The buffer amplifiers are implemented with FET-input operational amplifiers to minimize loading on the input signals. A resistive divider between the buffer amplifier outputs provides the common mode output voltage for driving the AI guard voltage amplifiers. Since this type of amplifier has inherently high offset voltage and offset drift, a calibration loop is used to minimize these errors. A multiplexer at the buffer amplifier inputs is alternately switched between the input signal and ground. A comparator at the differential amplifier output provides an error signal to a flip-flop which is clocked at the end of the ground-sample period. The flip-flop output charges a capacitor at the input of a two-transistor differential amplifier. The amplifier outputs are connected to the bias control inputs of the buffer amplifiers to supply the offset correction voltage.

The sample-and-hold amplifier charges a holding capacitor during the sample period, and supplies a stable output voltage to the ADC during the hold period. An additional capacitor in the amplifier feedback loop minimizes the effects of charge transfer during switching transients.

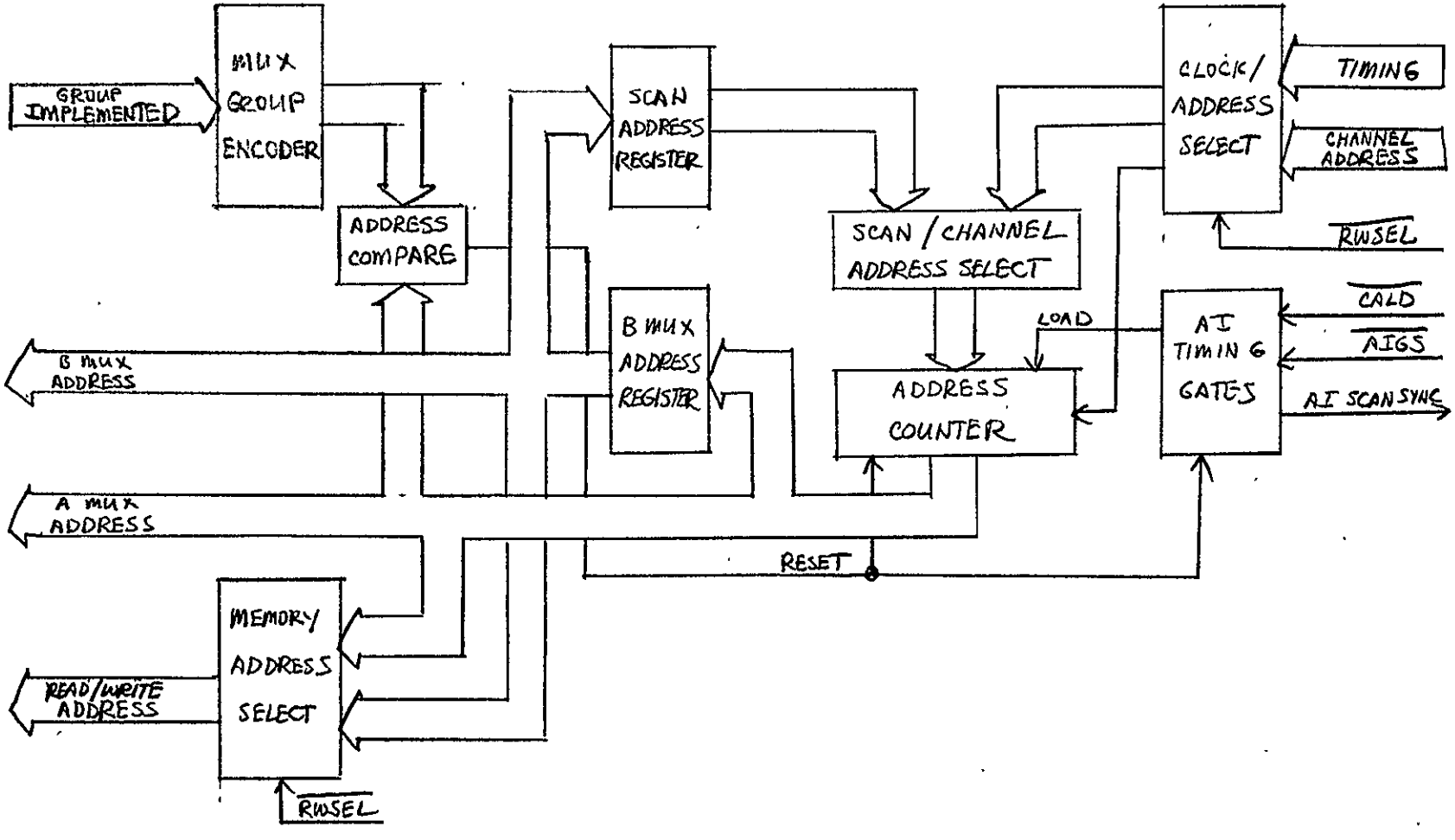
DIU ADC (3339009)

The DIU ADC is implemented with a successive-approximation analog-to-digital converter which provides two encode cycles during each 10 microsecond word time. Timing for the converter is provided by a divide-by-ten counter

which is clocked by the 2 MHz system clock. Word synchronization is provided by resetting the counter during the WS bit of each word.

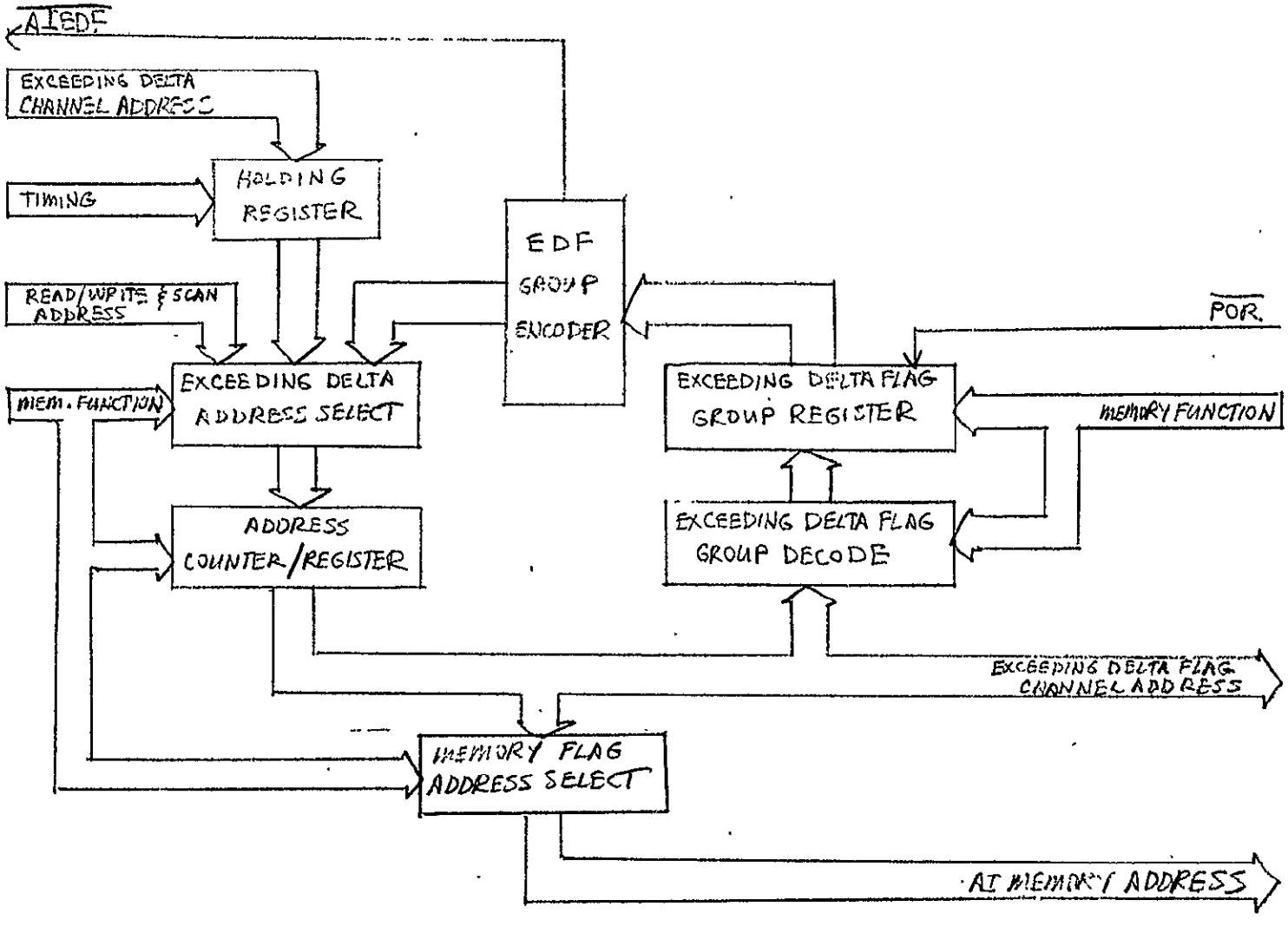
The counter outputs are decoded and supplied as clock signals to eight-bit successive approximation register (SAR). The SAR outputs drive an eight-bit digital-to-analog converter to supply a precision reference voltage for comparison with the AI signal, and are routed to the ADC output register for loading at the end of the encode cycle.

At the beginning of each encode cycle, the SAR is set to the half-scale value (10000000) to provide the initial reference voltage from the DAC. The voltage comparisons are made by driving the DAC feedback resistor with the AI voltage and comparing the DAC output with a fixed reference value. This value is adjusted by select resistors to provide the 60 mv. offset necessary to encode zero volts with a data value of 00000011. The DAC output and fixed offset voltage are buffered by a high-impedance differential amplifier to minimize loading. The amplifier outputs are supplied to a voltage comparator to generate data inputs to the SAR.



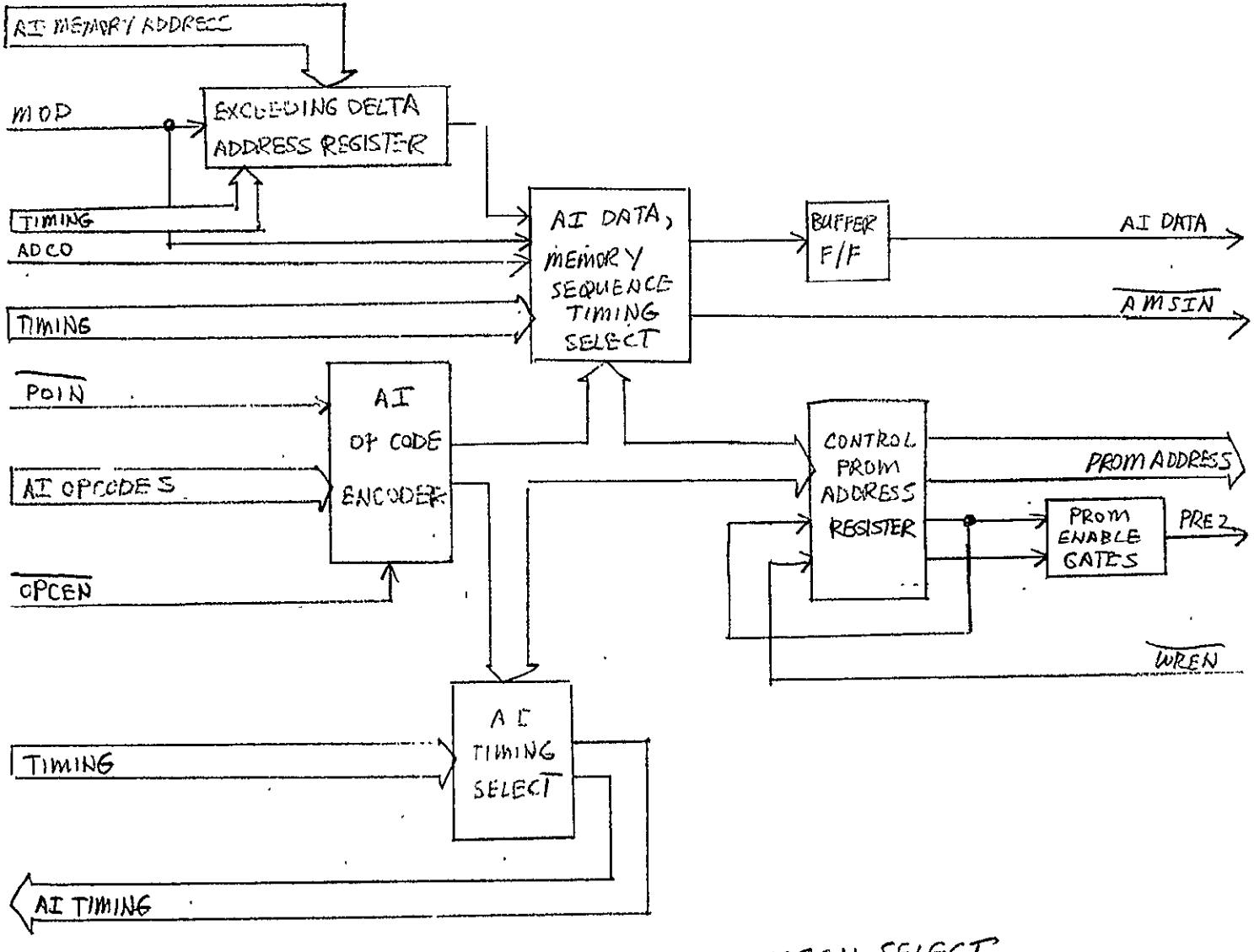
AI MUX ADDRESS CONTROL

FIGURE 4.12-1



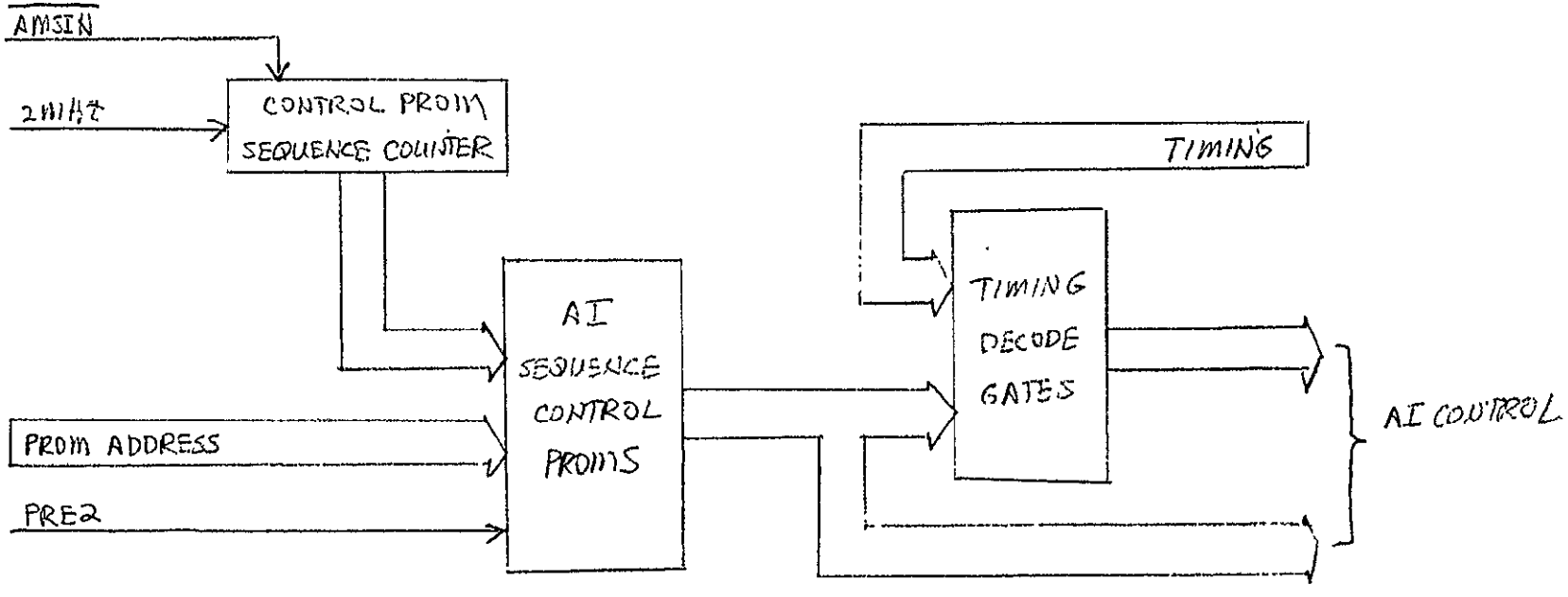
AI MEMORY ADDRESS CONTROL.

FIGURE 4.12-2



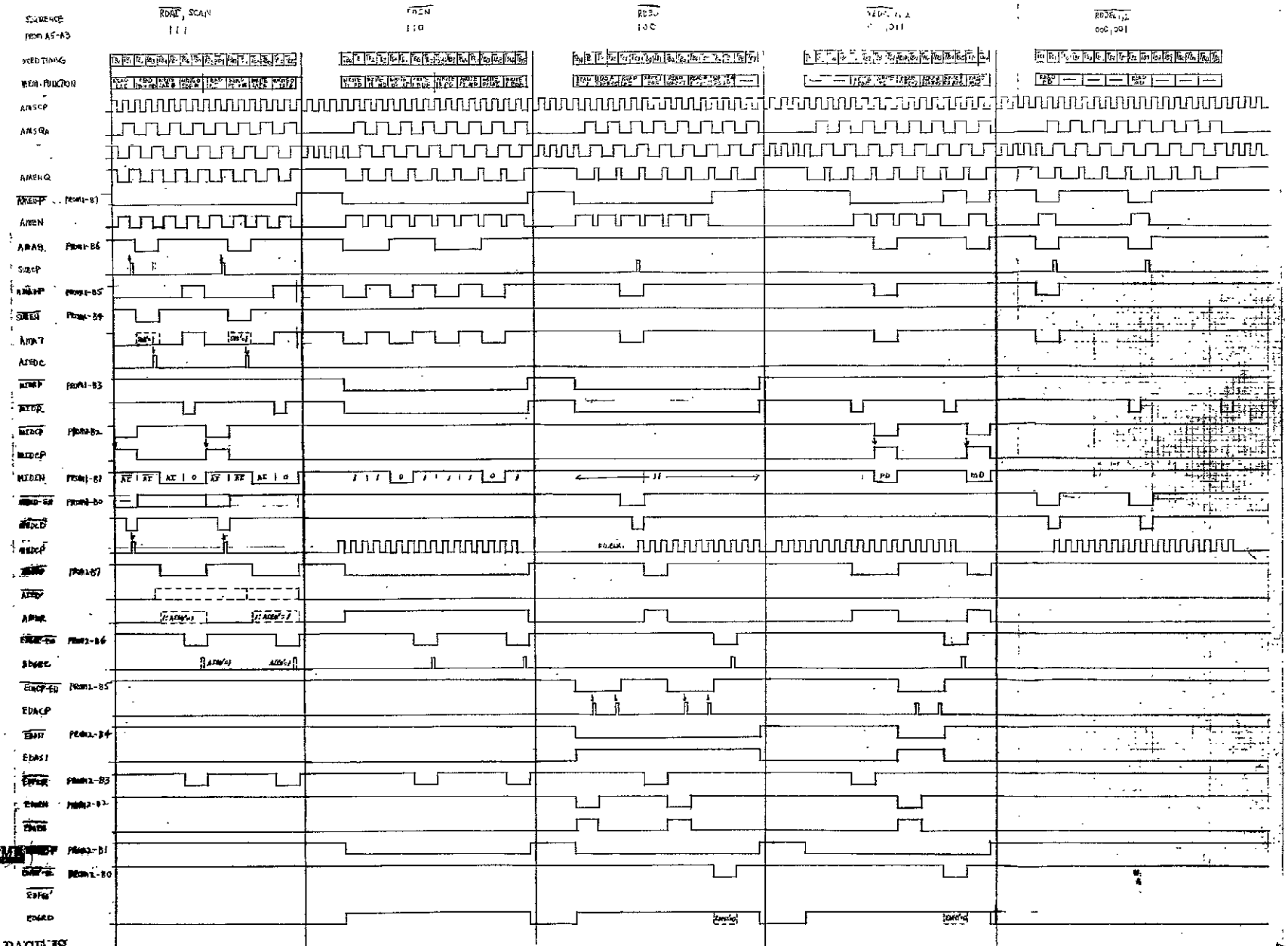
AI MEMORY FUNCTION SELECT

FIGURE 4.12-3



AI MEMORY SEQUENCE CONTROL

FIGURE 4.12-4



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AI MEMORY SEQUENCE TIMING
FIGURE 4.12-5

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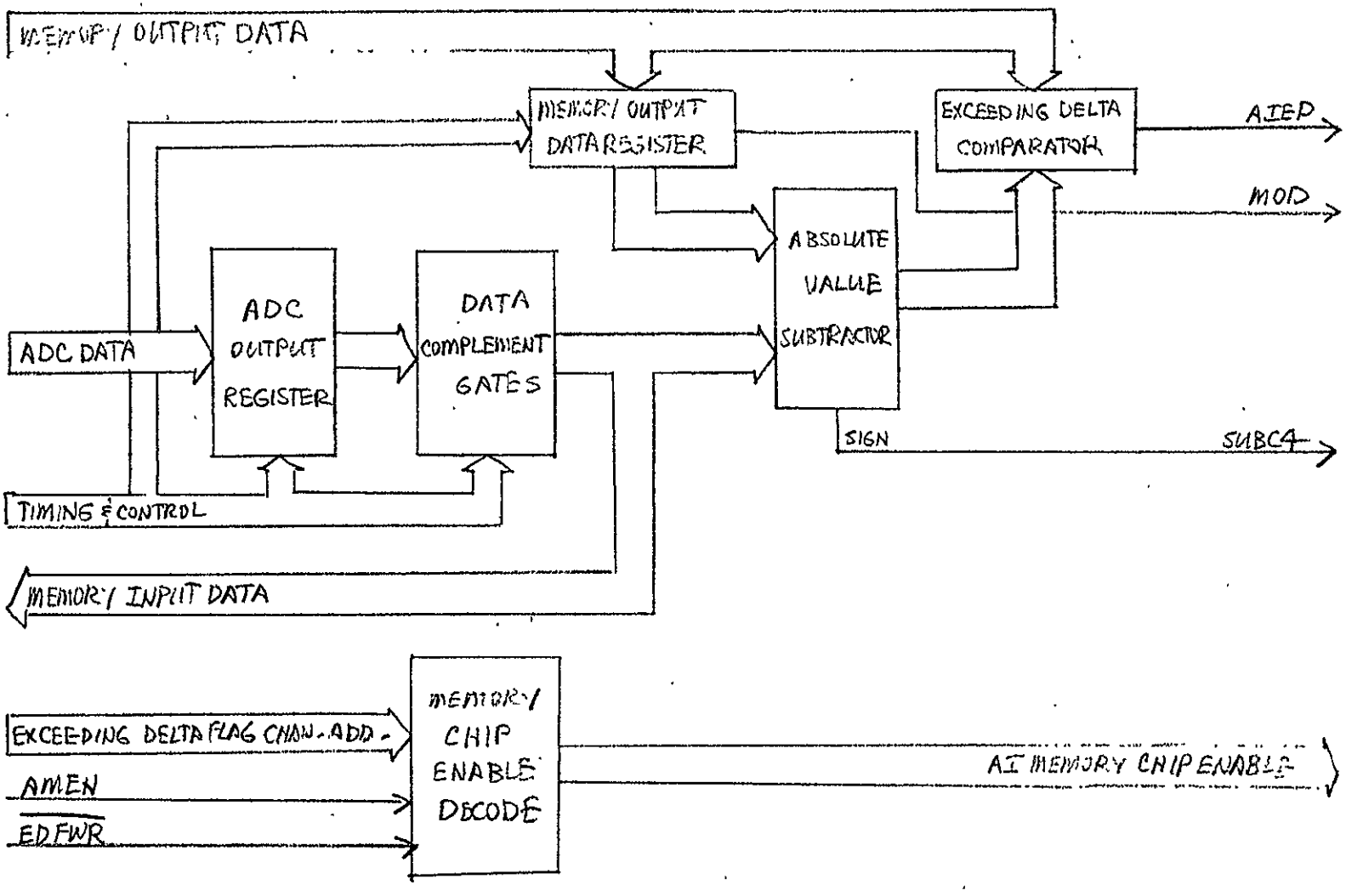
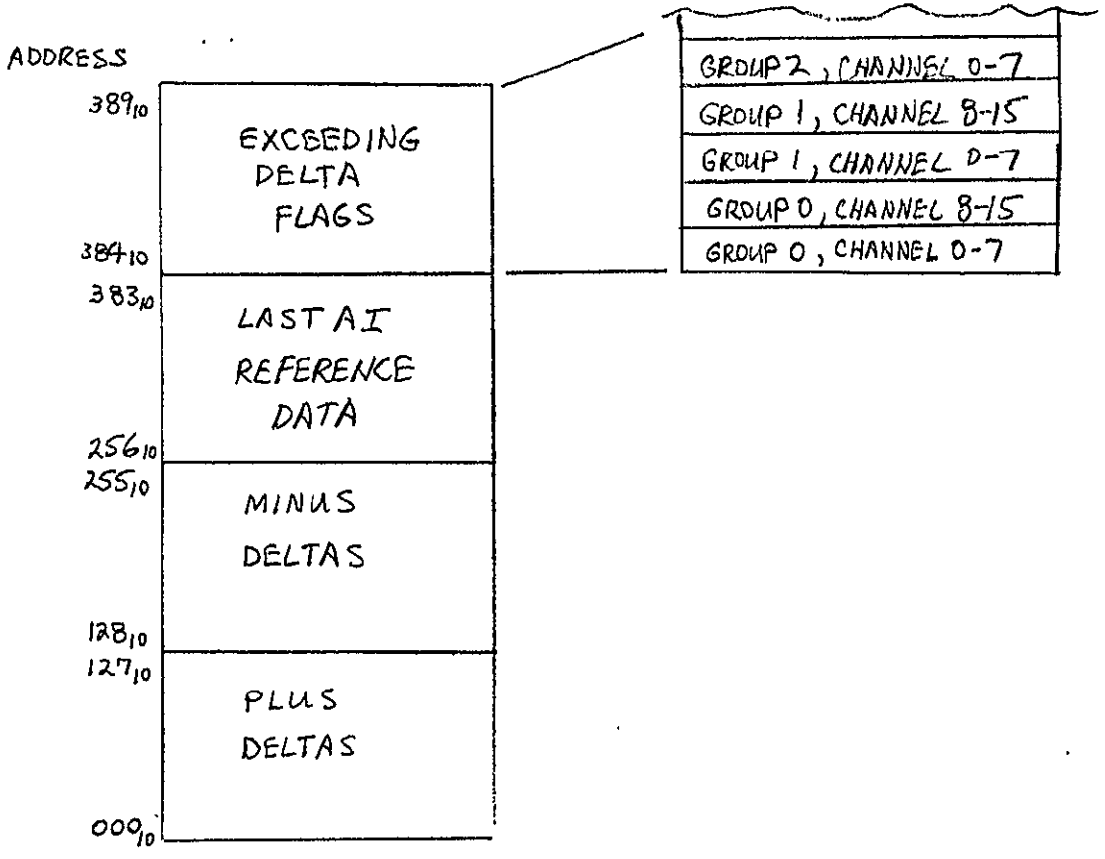


AI MEMORY DATA INTERFACE

FIGURE 4.12-6



AI MEMORY ORGANIZATION

FIGURE 4.12-7

4.13 FRONT PANEL DISPLAY (3339076)

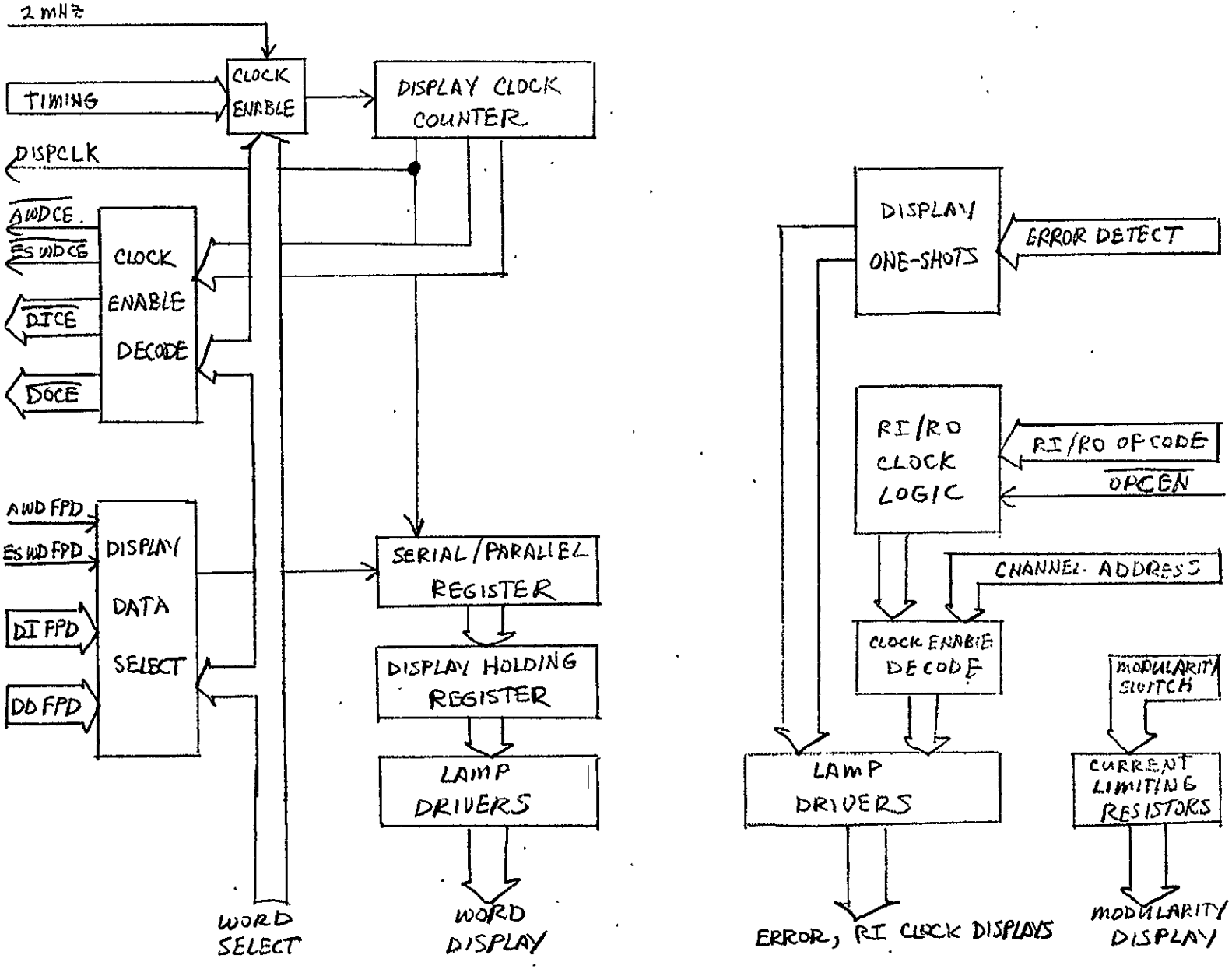
The block diagram for the Front Panel Display logic is shown in Figure 4.13-1. The circuitry in this section provides the data selection, clock generation, and display interfaces for the front panel word, error, and RI/RO clock displays.

The DIU data registers for A word, ES word, DI, and DO displays are implemented with CMOS logic to minimize power consumption. A 500 KHz gated display clock is supplied to all display registers, with register selection controlled by clock enable signals (A WD CE, etc.). The display clock counter generates a gated 16 bit clock signal when timing pulses from the DIU logic indicate the selected display register has been updated. For the DI and DO registers, a load pulse is output to read the selected data.

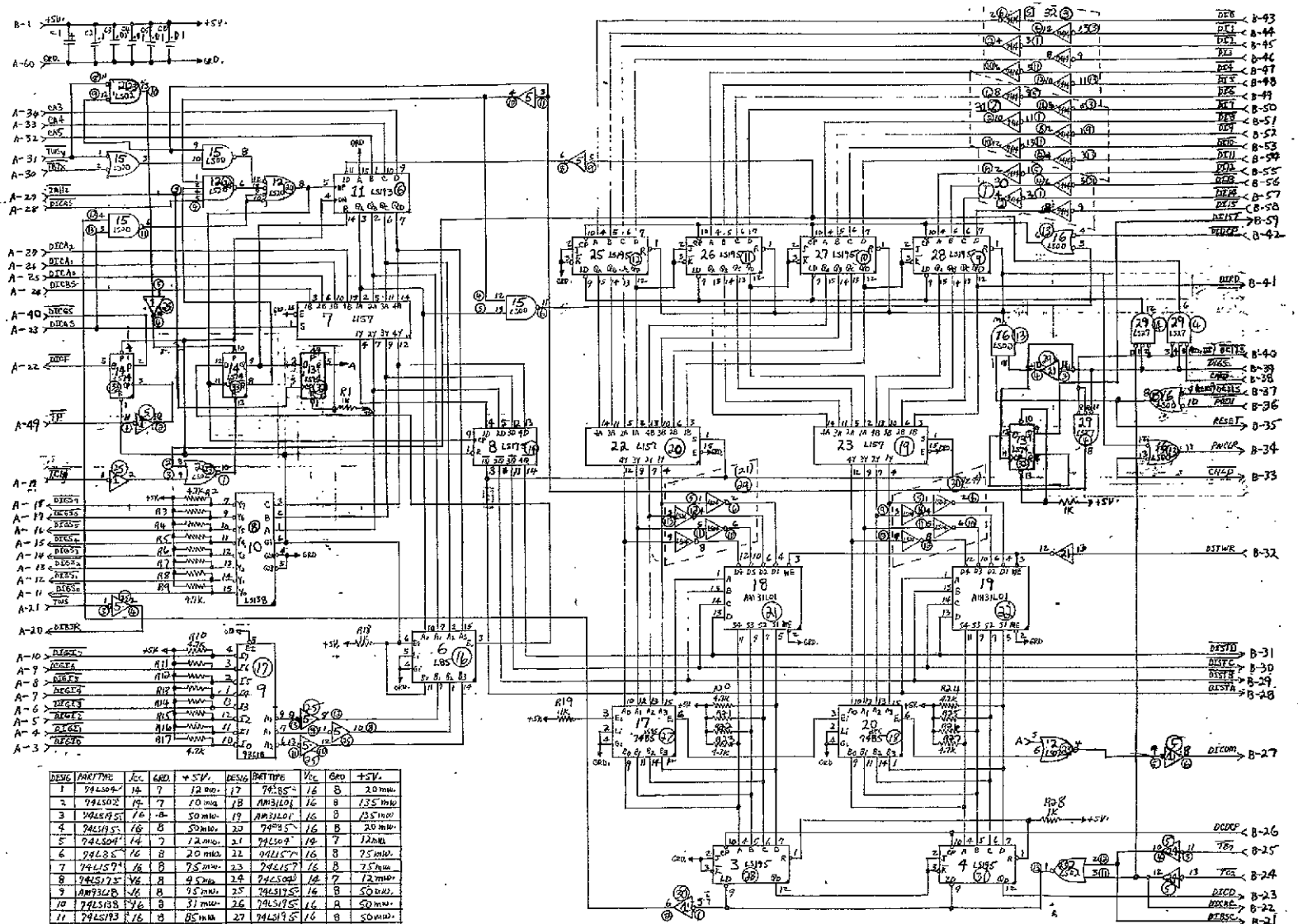
The serial display data is selected by levels from the front panel controls and shifted into a 16-bit serial-to-parallel register. At the end of the gated display shift clock, the data is loaded into a holding register to update the front panel word display.

Four signals are received from the Receive logic and Error Status logic to drive the Address Detect, Error Detect, Word Sync Error, and Word Sync Detect displays. These signals are interfaced through one-shots to provide a visible display for transient conditions.

The RI/RO clock display is interfaced by storing and decoding the channel address bits for RI/RO OP codes, and pulsing the decoder with a one-shot for visibility. The modularity display receives the "group implemented" ground lines from the DIU modules through an eight-pole rotary switch to indicate the DIU configuration for AI, RI/RO, DI and DO modules.



FRONT PANEL DISPLAY LOGIC
FIGURE 4.13-1



DESIG	PART TYPE	Icc	GRD	+5V.	DESIG	PART TYPE	Icc	GRD	+5V.
1	74LS04	14	7	12 ma.	17	74185	16	8	20 ma.
2	74LS02	14	7	10 ma.	18	AM3101	16	8	135 ma.
3	74LS195	16	8	50 ma.	19	AM3101	16	8	135 ma.
4	74LS195	16	8	50 ma.	20	74185	16	8	20 ma.
5	74LS04	14	7	12 ma.	21	74LS04	14	7	12 ma.
6	74L85	16	8	20 ma.	22	74LS157	16	8	75 ma.
7	74LS157	16	8	75 ma.	23	74LS157	16	8	75 ma.
8	74LS173	16	8	45 ma.	24	74LS00	14	7	12 ma.
9	AM93L18	16	8	95 ma.	25	74LS175	16	8	50 ma.
10	74LS138	16	8	31 ma.	26	74LS175	16	8	50 ma.
11	74LS193	16	8	85 ma.	27	74LS175	16	8	50 ma.
12	74LS20	14	7	9 ma.	28	74LS175	16	8	50 ma.
13	74LS74	14	7	20 ma.	29	74LS27	14	7	14 ma.
14	74LS74	14	7	20 ma.	30	7414	14	7	150 ma.
15	74LS00	14	7	8 ma.	31	7414	14	7	150 ma.
16	74LS00	14	7	8 ma.	32	7414	14	7	150 ma.
					BOARD, SYSTEM TOTAL				

DI MUX CONT. #1. D19
P.B. 3339 064

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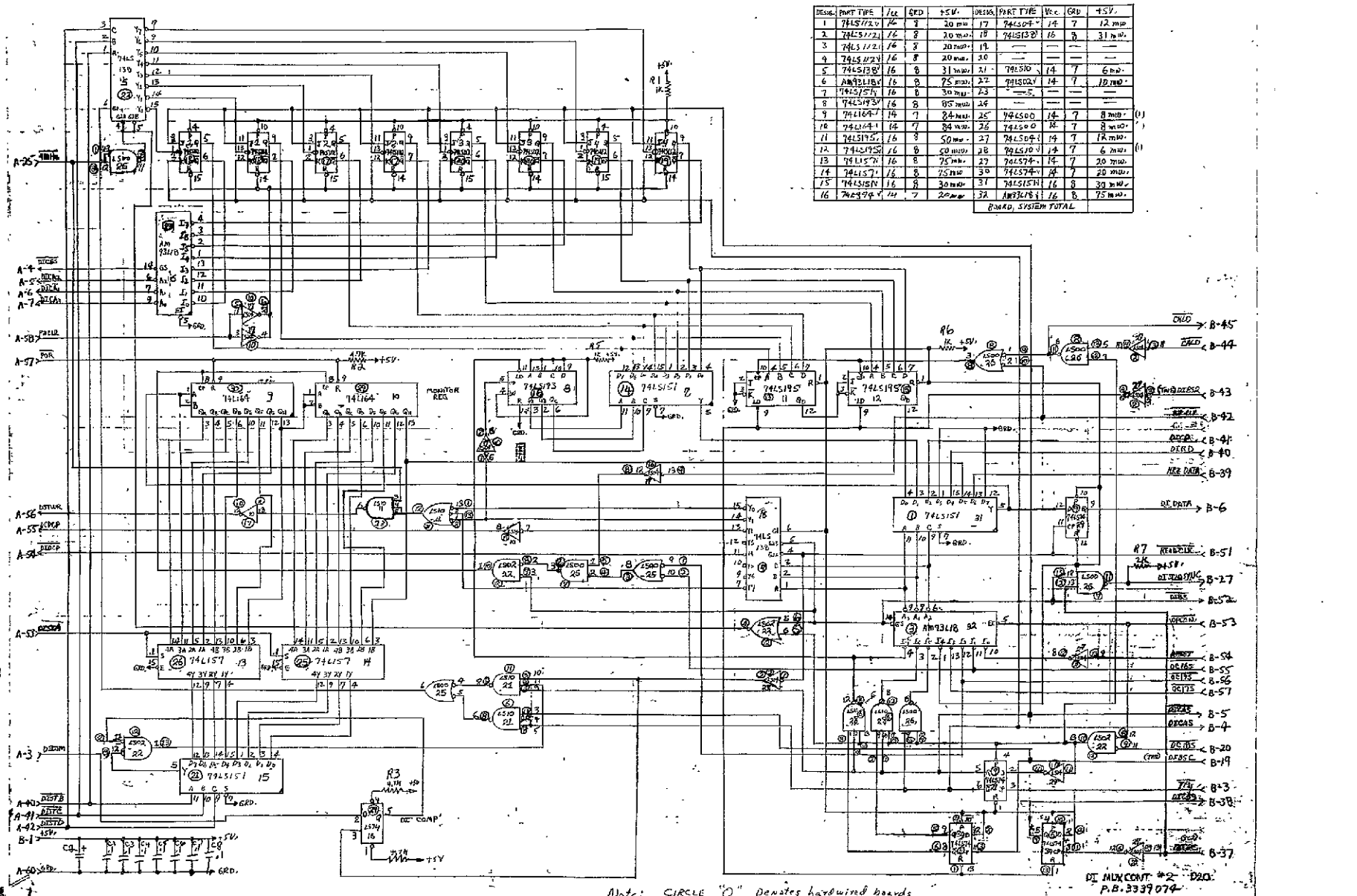

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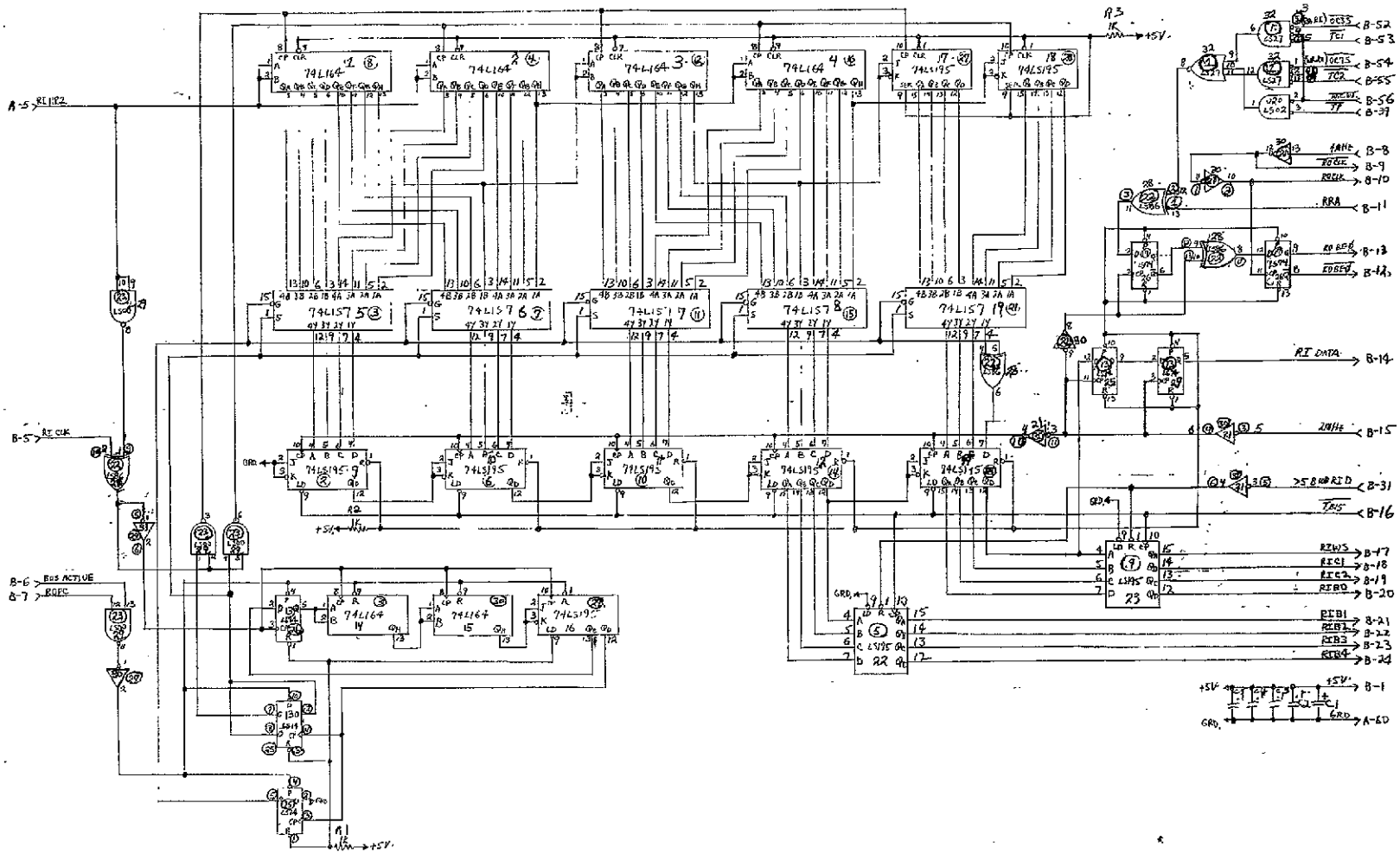
RI/RO INTERFACE LOGIC
D27
P.B. 3339070
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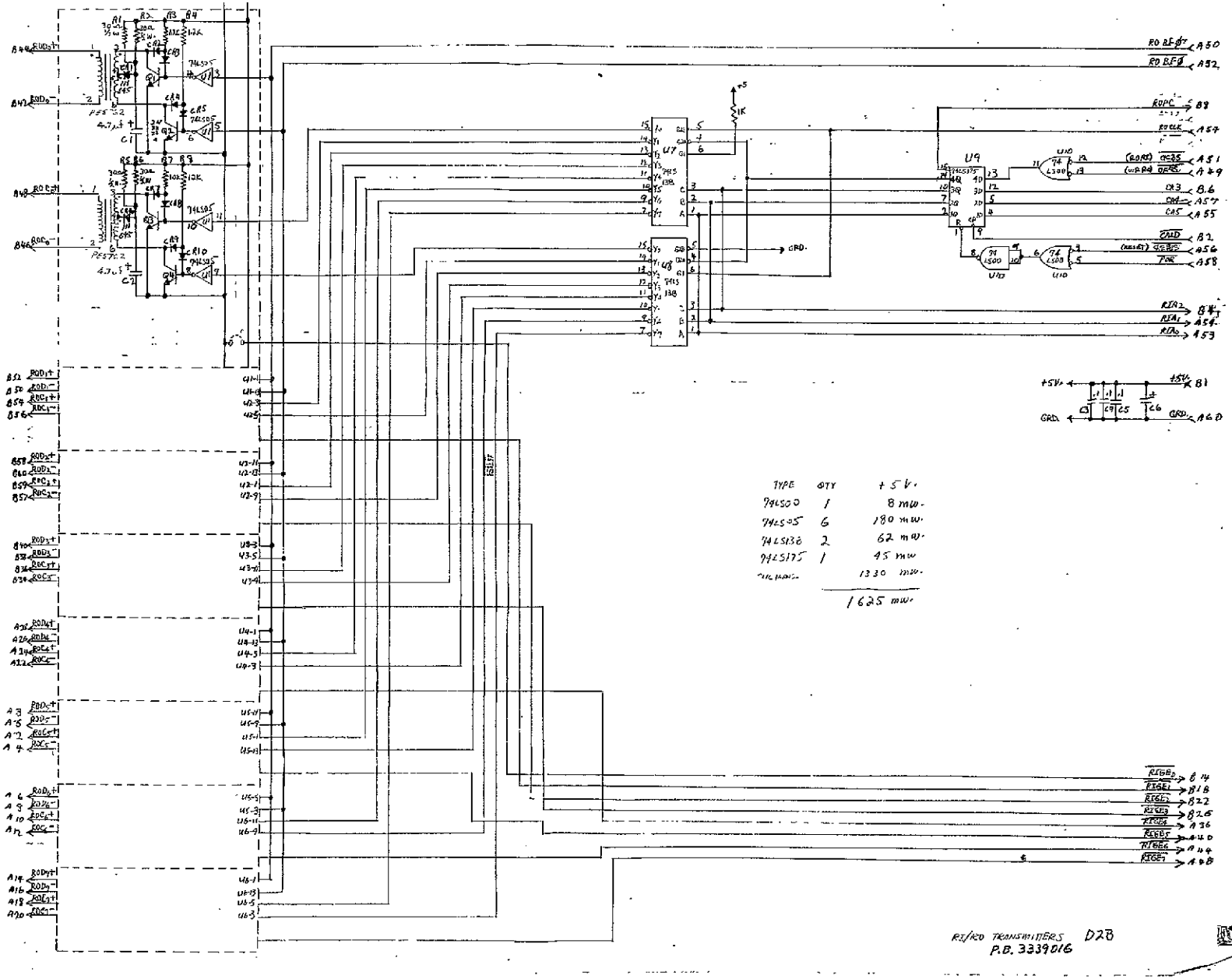
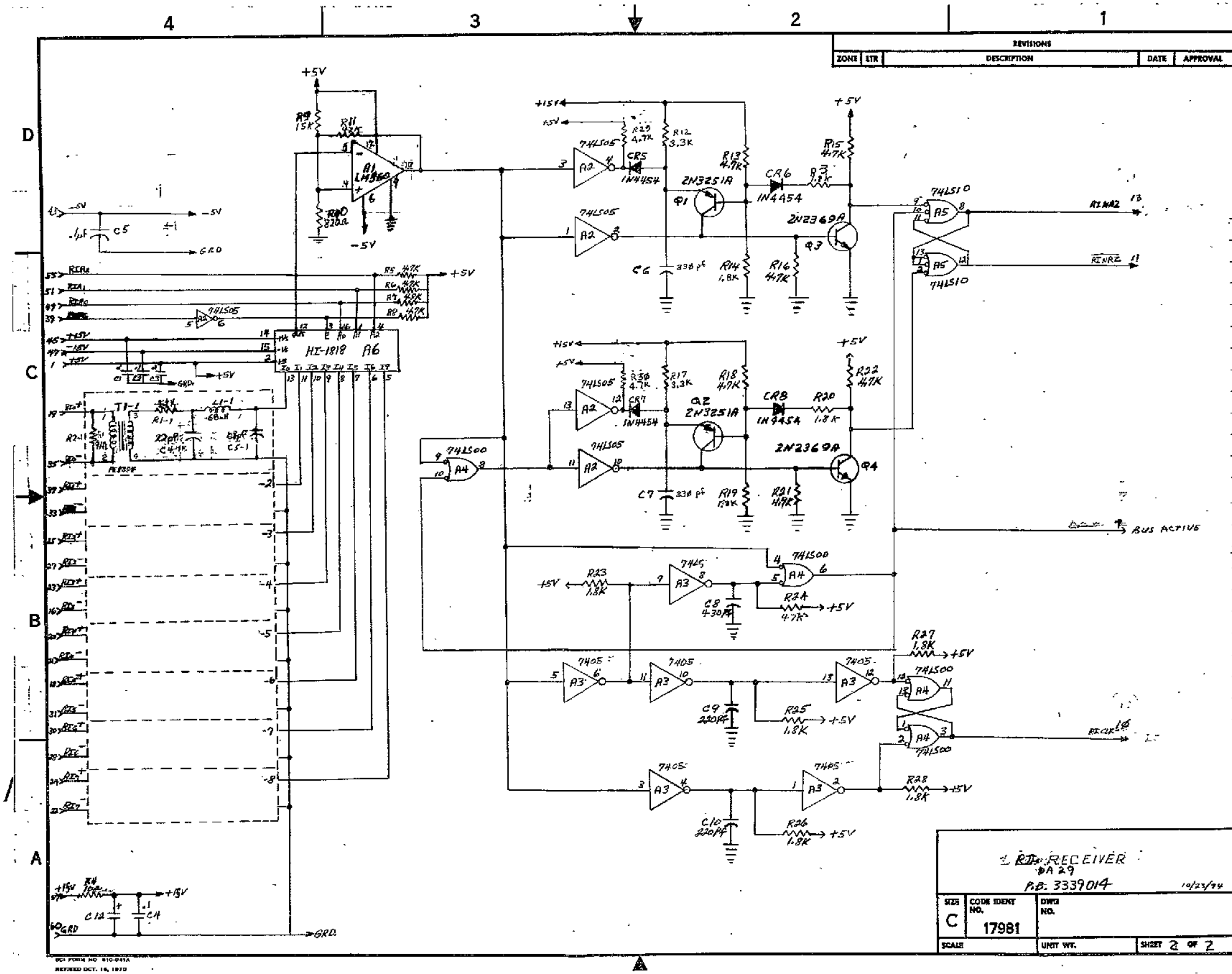
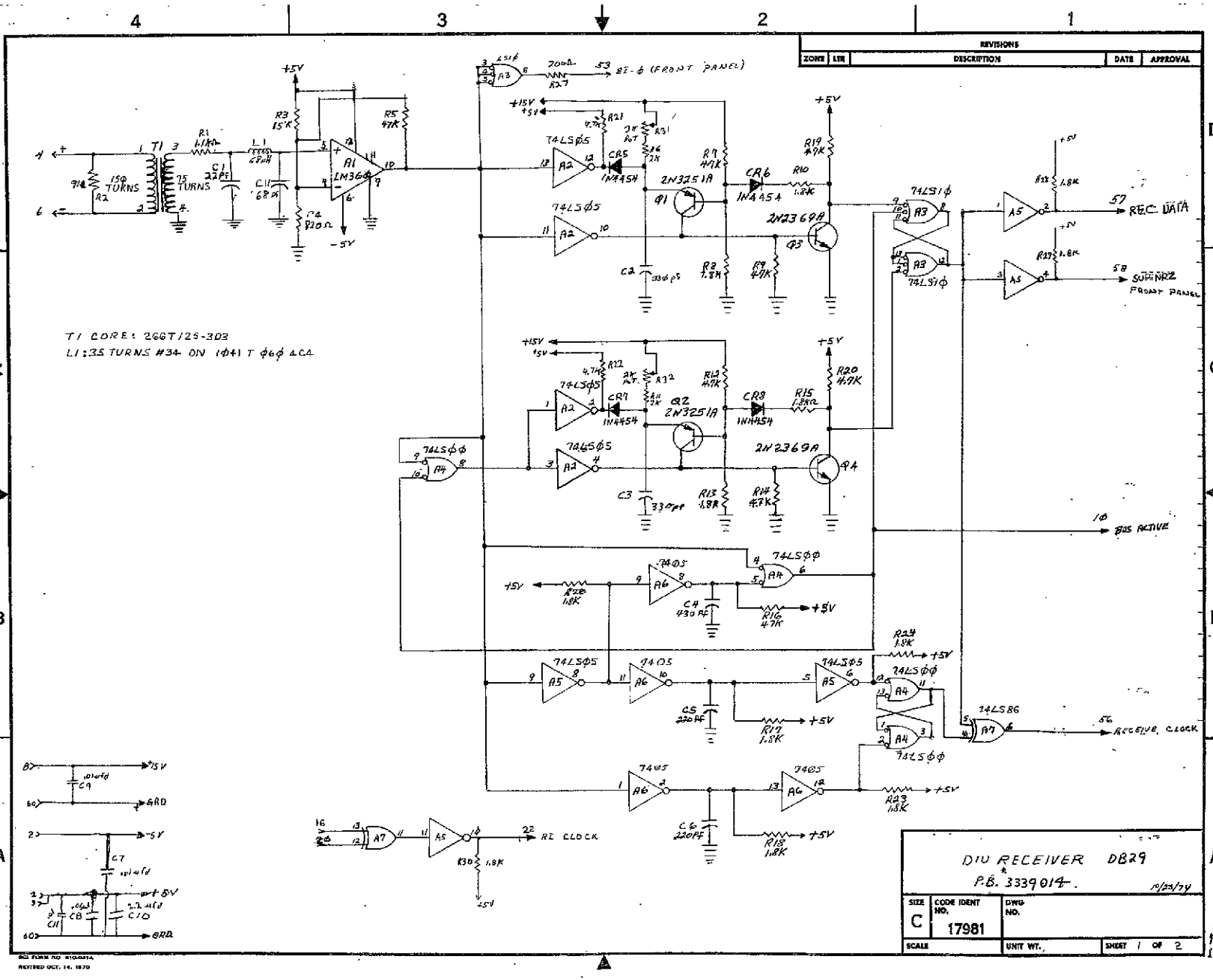
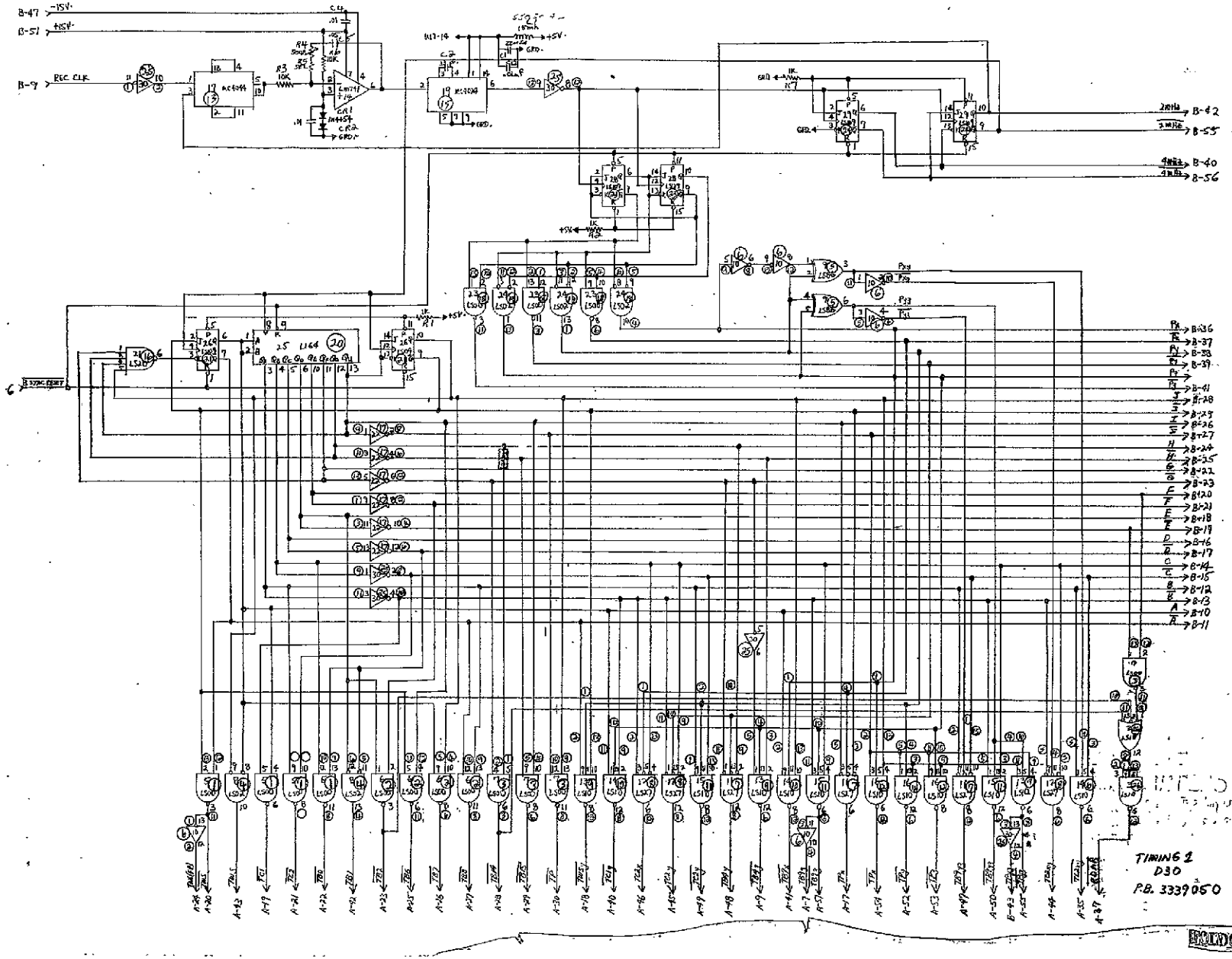


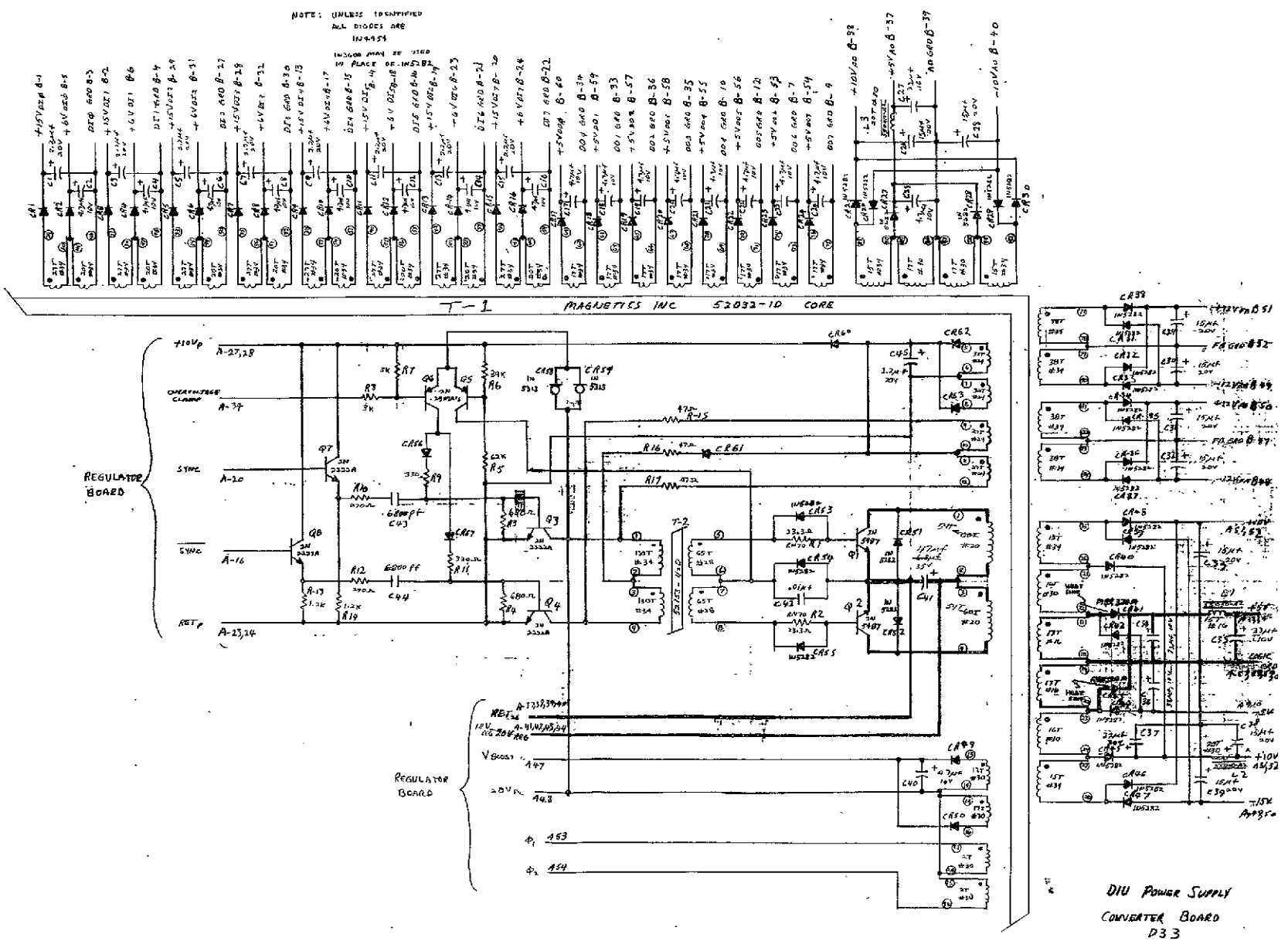
TYPE	QTY	+5V.
74LS00	1	8 mw.
74LS05	6	180 mw.
74LS138	2	62 mw.
74LS175	1	45 mw
		1330 mw.
		1625 mw.

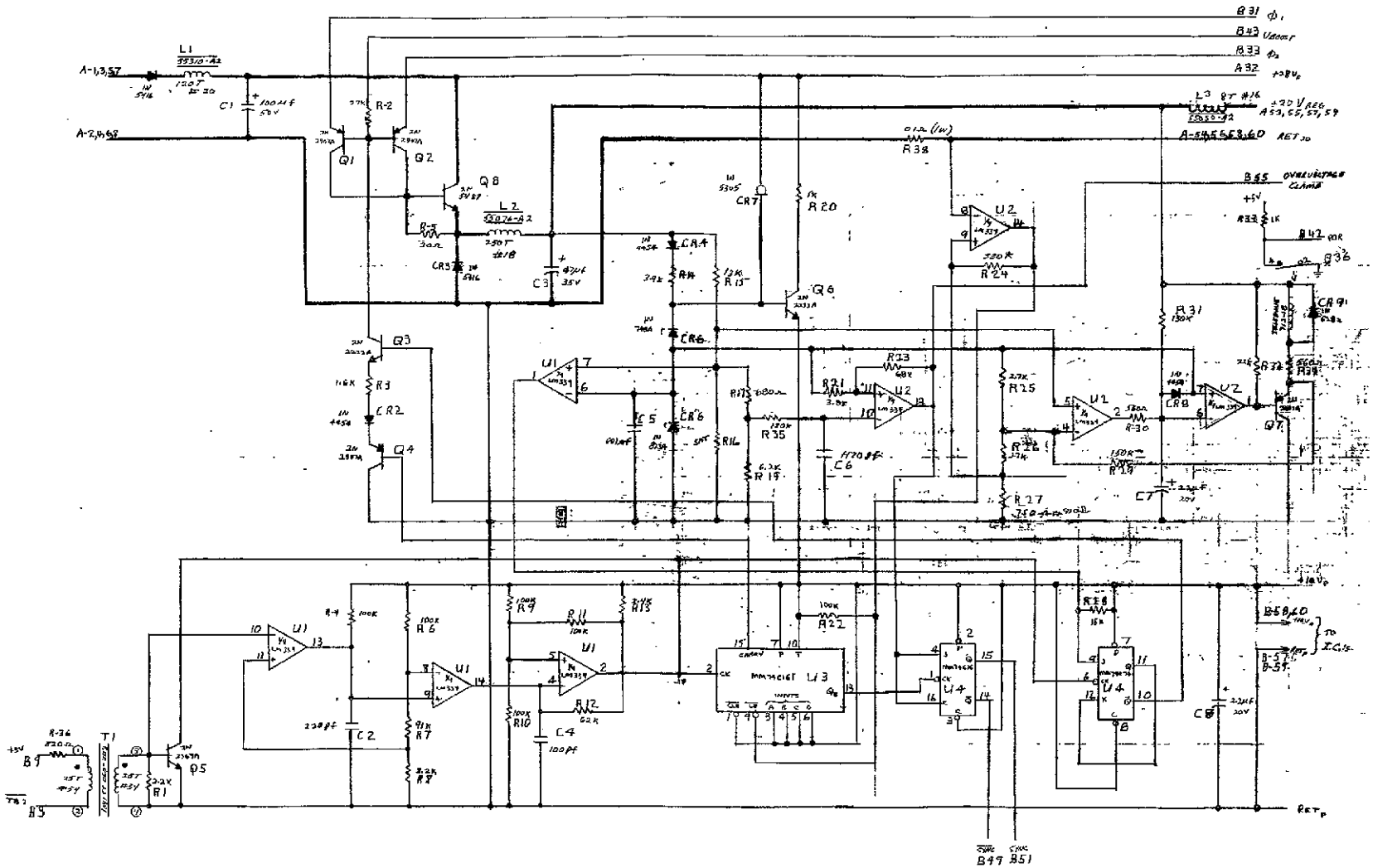
RF/RCD TRANSMITTERS D28
P.B. 3339016











DIU POWER SUPPLY
REGULATOR BOARD
* D36
RB. 3339022

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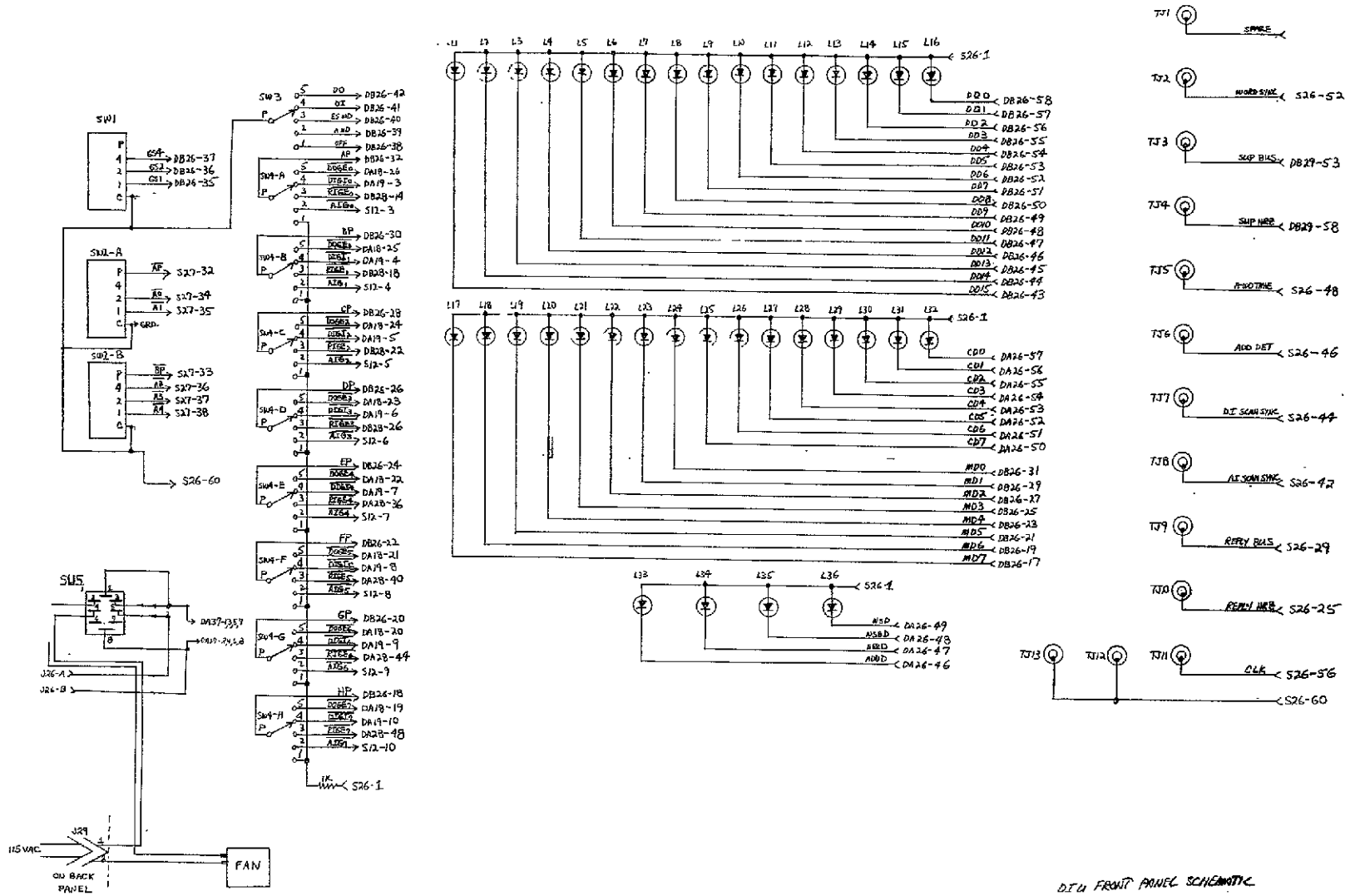
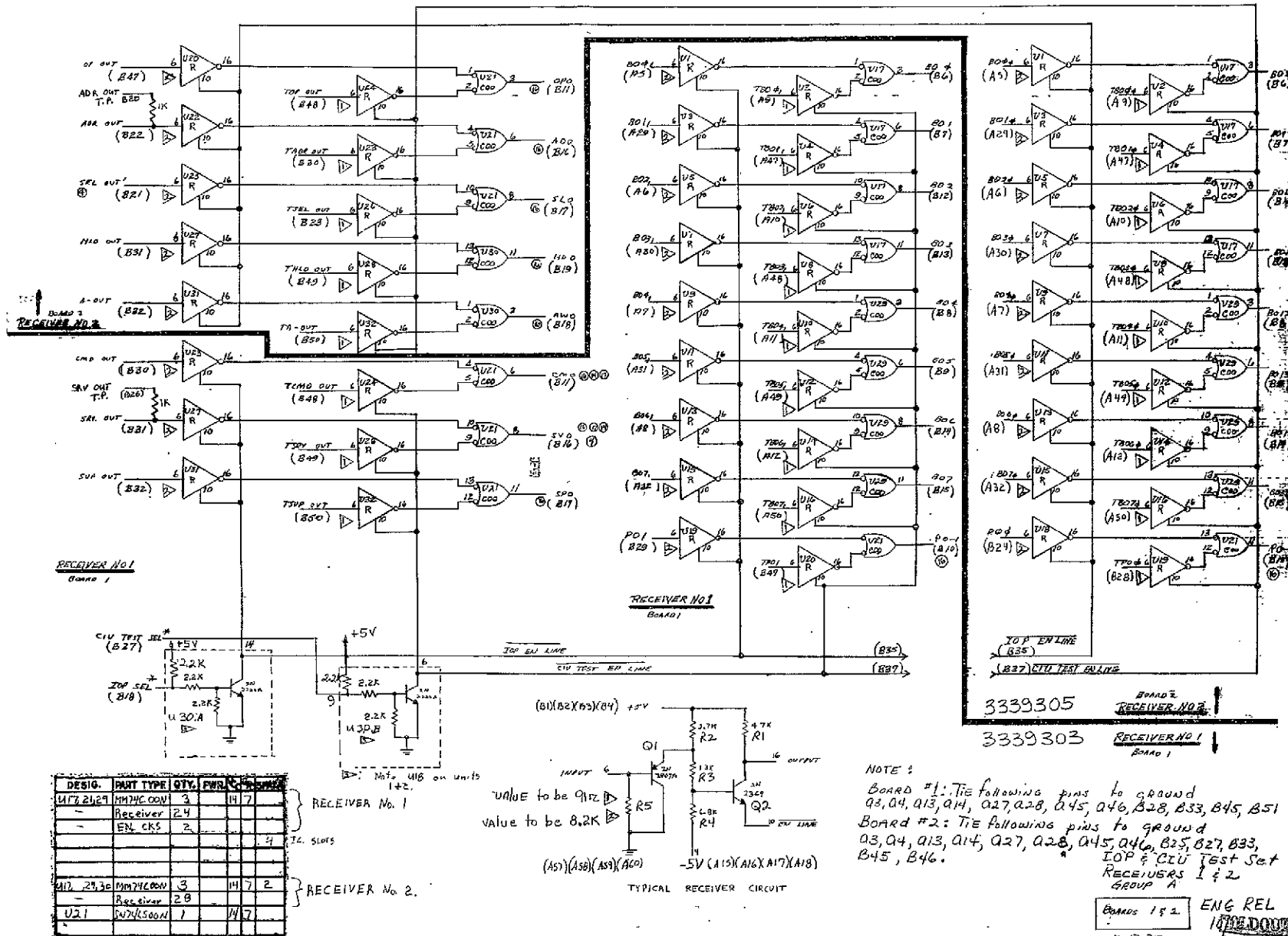


D.F.U FRONT PANEL SCHEMATIC



DESIG.	PART TYPE	QTY.	PWR.			
U17, 21, 27	MM74C 00N	3		14	7	
—	Receiver	24				
—	EN. CKS	2				4
U19, 23, 30	MM74C 00N	3		14	7	2
—	Receiver	28				
U21	SN74LS00N	1		14	7	

RECEIVER No. 1

IC. SLOTS

RECEIVER No. 2.

NOTE:
Board #1: Tie following pins to ground
Q3, Q4, Q13, Q14, Q27, Q28, Q45, Q46, B28, B33, B45, B51.
Board #2: Tie following pins to ground
Q3, Q4, Q13, Q14, Q27, Q28, Q45, Q46, B25, B27, B33, B45, B46.

IOP & CTU Test Set
Receivers 1 & 2
Group A

Boards 1 & 2

ENG REL

4-17-75

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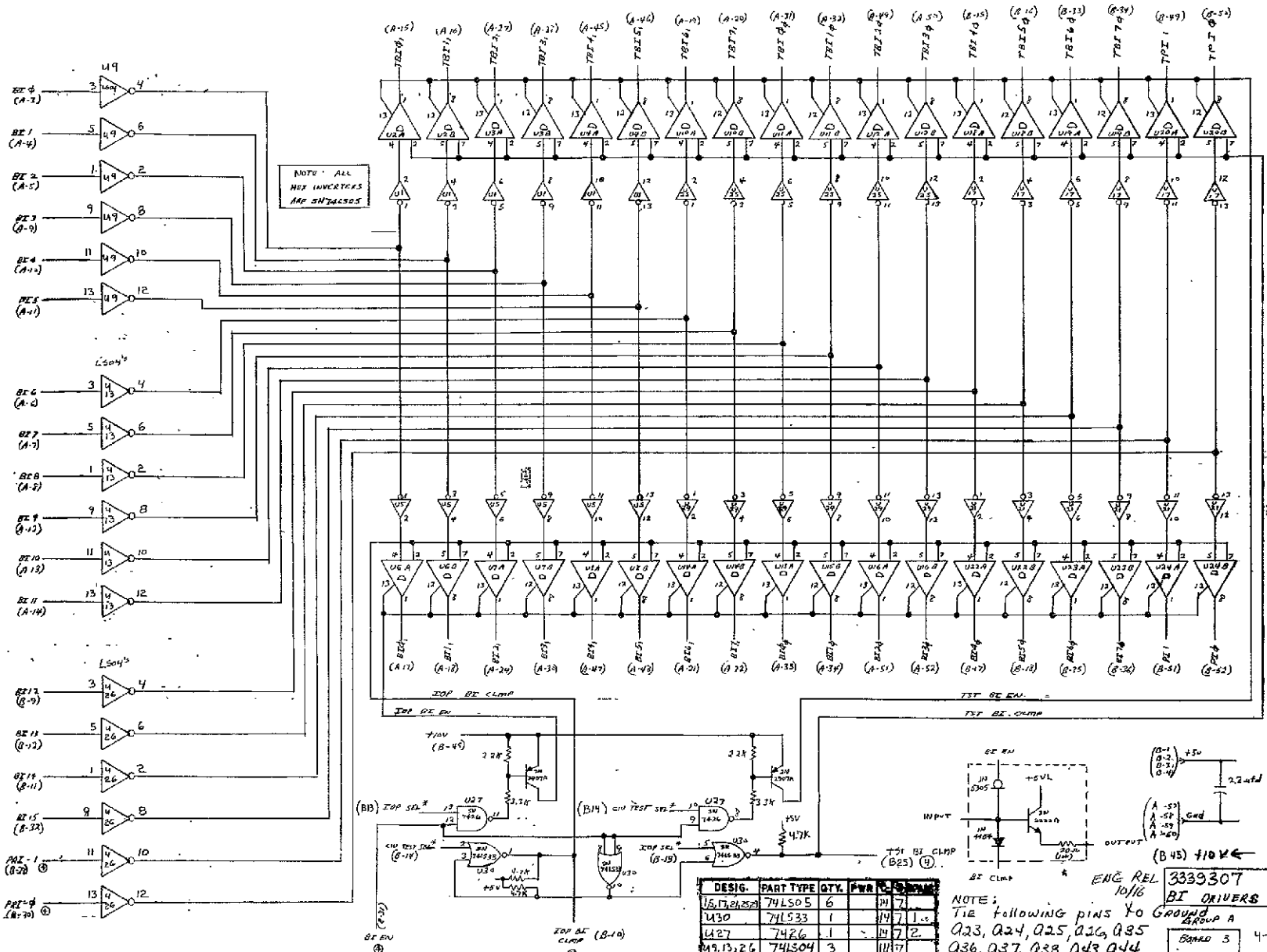

DESIG.	PART TYPE	QTY.	PWR	GND
15,17,21,23	74LS05	6	14	7
U30	74LS33	1	14	7
U27	7426	1	14	7
U9,13,26	74LS04	3	14	7
TYPICAL	DRIVER CK.	36		
	EN CKS.	2		

NOTE:
Tie following pins to Ground Group A
Q23, Q24, Q25, Q26, Q35
Q36, Q37, Q38, Q43, Q44
Q53, Q54, B19, B20, B37, B38, B53, B54

ENG REL 10/16 3339307
BI DRIVERS
BOARD 3
4-17-75

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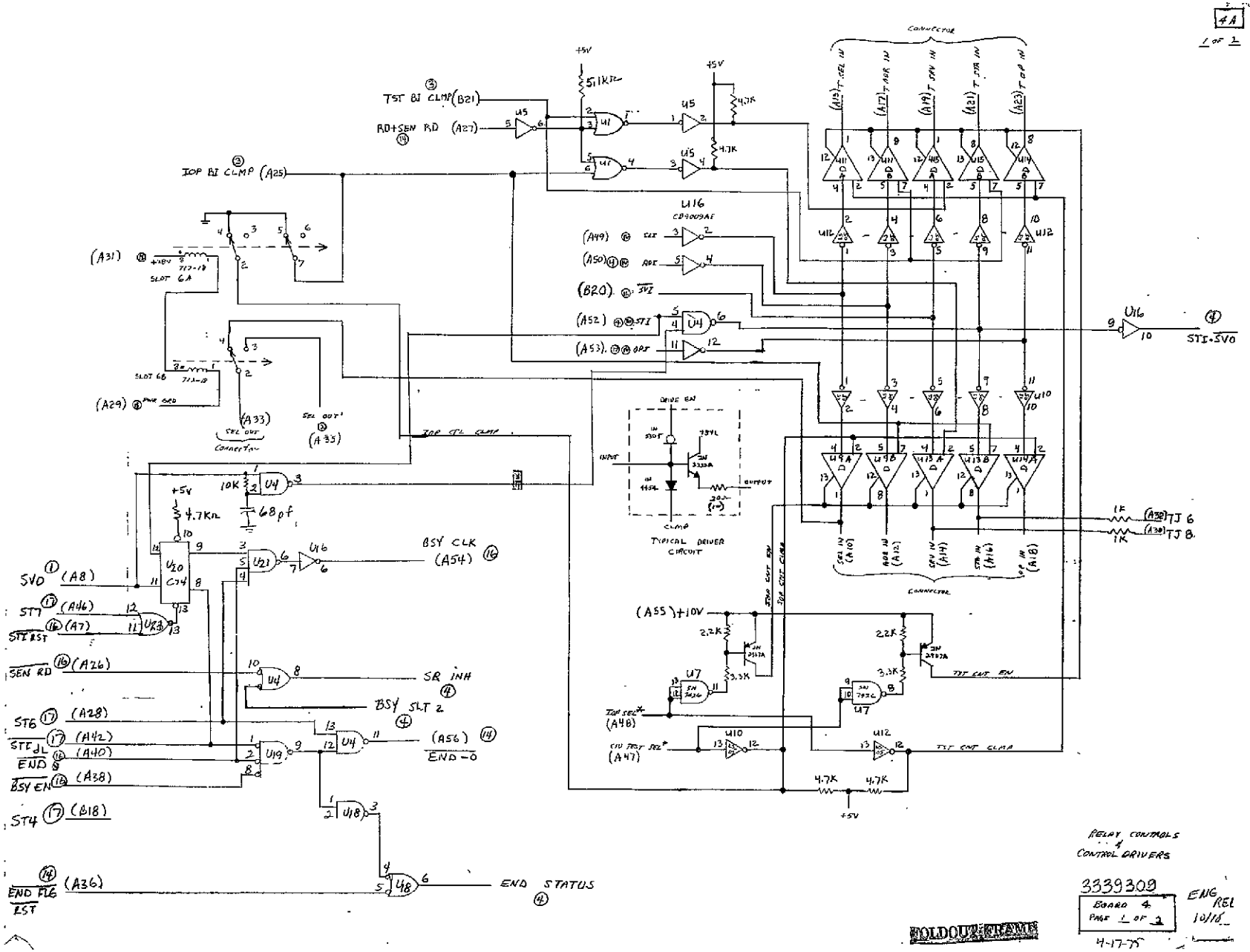
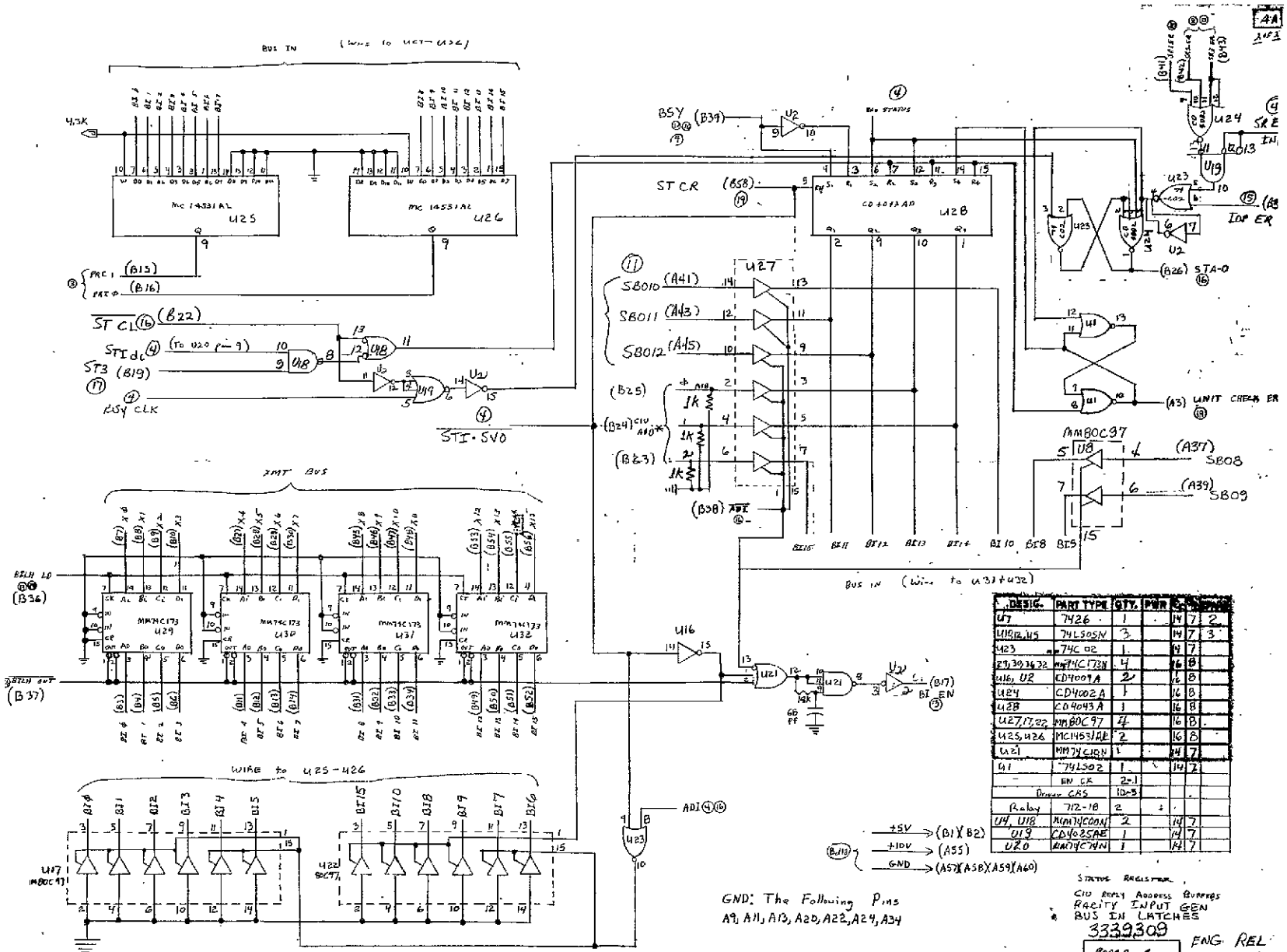
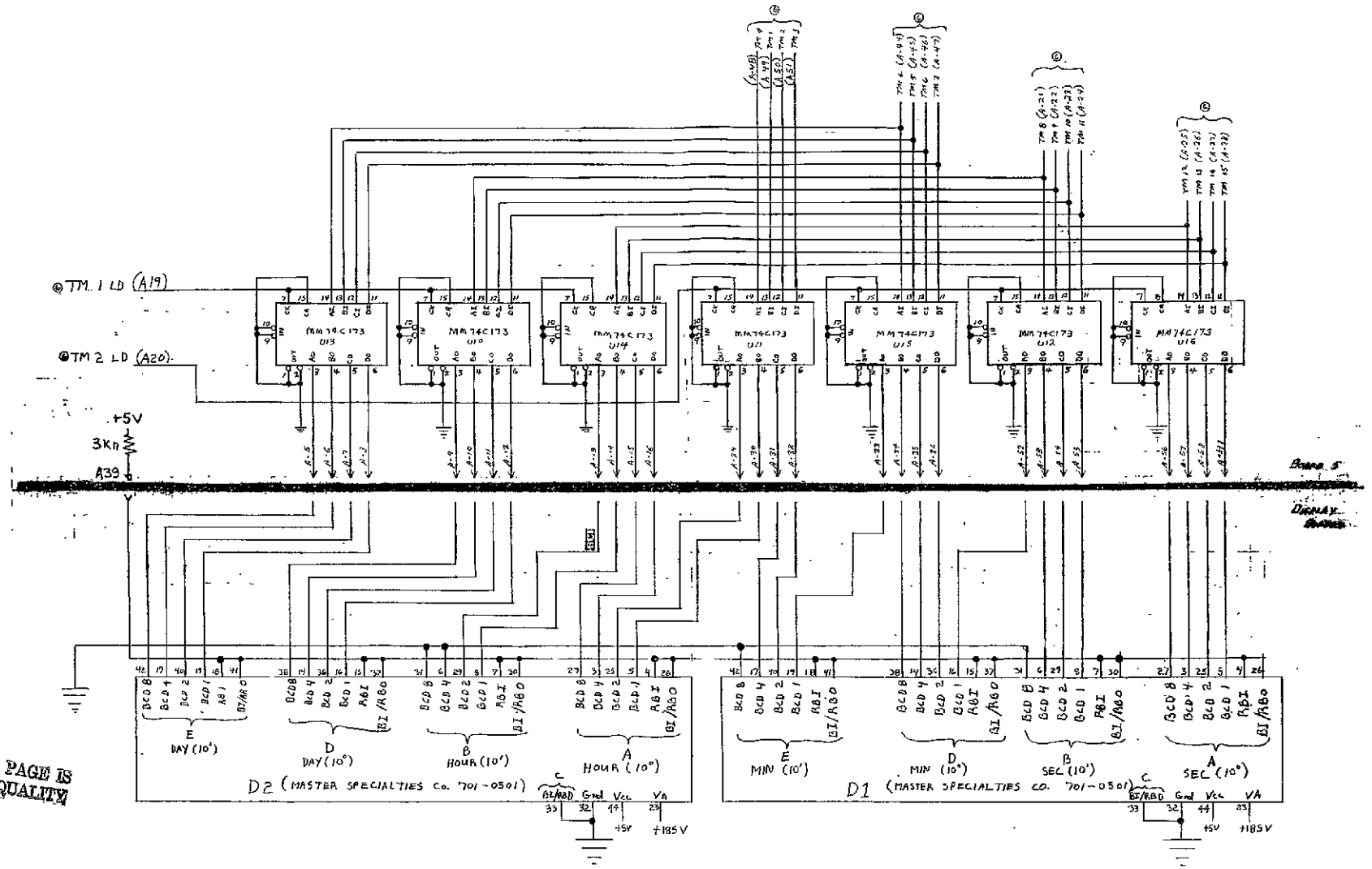

TST BI CLMP (B21)
RD+SEN RD (A27)
IOP BI CLMP (A25)
U16
CD4009AE
(A49)
(A50)
(B20)
(A52)
(A53)
(A31)
SLOT 6A
SLOT 6B
(A29)
(A33)
SEL OUT CONNECTOR
(A35)
SEL OUT
IOP CTL CLAMP
+5V
10K
4.7KΩ
68pf
U20
C34
U21
U16
BSY CLK (A54)
SV0 (A8)
ST7 (A46)
STF RST (A7)
SEN RD (A26)
SR INH
BSY SLT 2
ST6 (A28)
STF_DL (A42)
END (A40)
BSY EN (A38)
(A56)
END -0
ST4 (B18)
END FLG EST (A36)
END STATUS
DRIVE EN
INPUT
OUTPUT
CLAMP
TYPICAL DRIVER CIRCUIT
CONNECTOR
SEL IN (A10)
ADR IN (A12)
CTL IN (A14)
STR IN (A16)
IOP IN (A18)
(A55) +10V
2.2K
3.3K
U7
IOP SEL* (A48)
CTL TEST SEL* (A47)
TST CNT EN
TST CNT CLMP
4.7K
U16
STI·SV0
1K
(A32) TJ 6
(A30) TJ 8
RELAY CONTROLS & CONTROL DRIVERS
3339309
BOARD 4
PAGE 1 OF 2
ENG REL 10/15
4-17-75
1 OF 1



DESIG.	PART TYPE	QTY.	PWR			
U7	7426	1		14	7	2
U18,12,45	74LS05N	3		14	7	3
U23	74C 02	1		14	7	
29,30,31,32	MM74C173N	4		16	8	
U16, U2	CD4009A	2		16	8	
U24	CD4002A	1		16	8	
U28	CD4093A	1		16	8	
U27,17,22,	AM8DC97	4		16	8	
U25,U26	MC1453/AE	2		16	8	
U21	MM74C10N	1		14	7	
U1	74LS02	1		14	2	
	EN CK	2-1				
	Driver CKS	10-5				
Baby	712-18	2	±			
U4, U18	MM74C00N	2		14	7	
U19	CD4023AE	1		14	7	
U20	MM74C74N	1		14	7	



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FOLDOUT FRAME 1

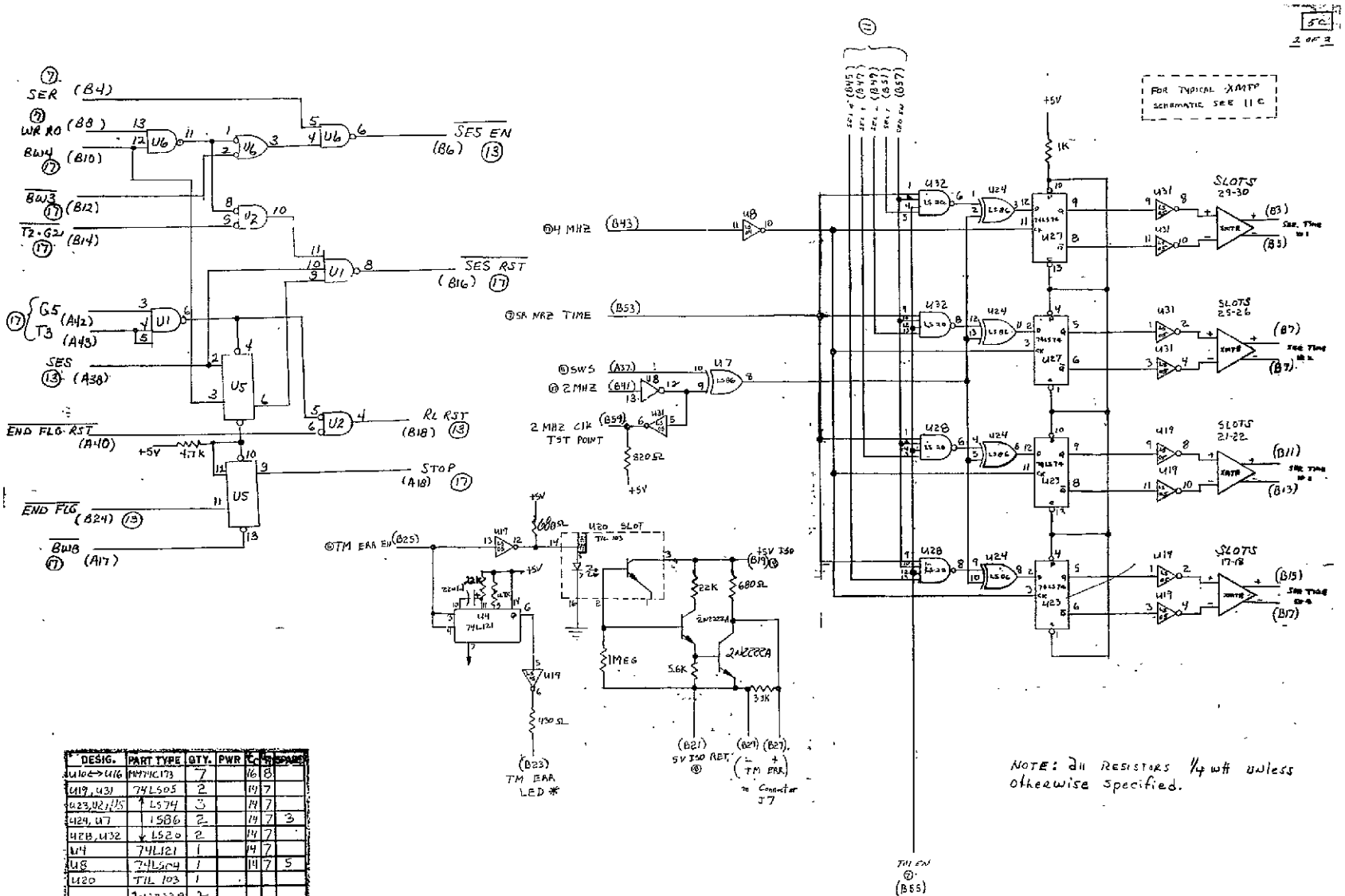
* Time Display Storage, Decode, Display Multiplexer & Digit Drivers

3339311

Board 5
Page 1 of 2
4-18-75

ENG REL 10/16

FOLDOUT FRAME 1



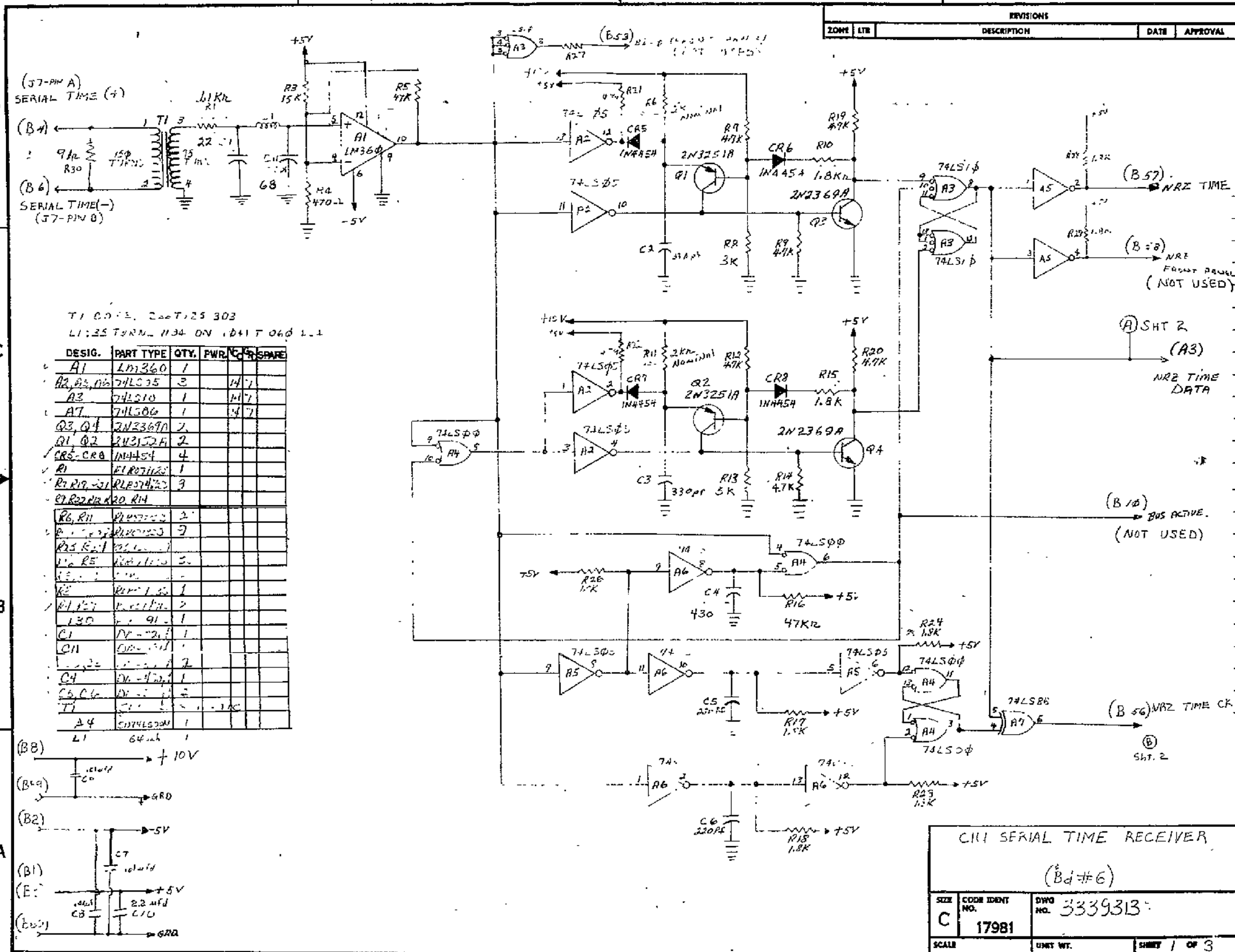
DESIG.	PART TYPE	QTY.	PWR			SPARE
U10↔U16	MMMC173	7		16	8	
U19, U31	74LS05	2		14	7	
U23, U21, U25	LS74	3		14	7	
U24, U7	LS86	2		14	7	3
U28, U32	LS20	2		14	7	
U4	74L121	1		14	7	
U8	74LS04	1		14	7	5
U20	TIL 103	1				
	2N2222A	2				
U1	SN74LS10	1		14	7	
U6	SN74LS00	1		14	7	
U2	SN74LS02	1		14	7	

SERIAL TIME OUTPUTS

* 3339311

BOARD 5
PAGE 2 OF 3

ENG REL
4-25-75



T1 CORE. [illegible] 303
L1: 35 TURNS #34 ON [illegible] 060 [illegible]

DESIG.	PART TYPE	QTY.	PWR.	Vcc	GND	SPARE
A1	LM360	1				
A2, A5, A6	74LS05	3		14	7	
A3	74LS10	1		14	7	
A7	74LS86	1		14	7	
Q3, Q4	2N2369A	2				
Q1, Q2	2N3251A	2				
CR5-CR8	1N4454	4				
R1	[illegible]	1				
R7, R12, R21	[illegible]	3				
R9, R22, R13, R20, R14						
R6, R11	[illegible]	2				
[illegible]	[illegible]	7				
R25, R[illegible]	[illegible]					
[illegible], R5	[illegible]	3				
[illegible]	[illegible]					
R[illegible]	[illegible]	1				
R[illegible]	[illegible]	2				
[illegible]30	[illegible] 91	1				
C1	[illegible]	1				
C11	[illegible]	1				
[illegible]	[illegible]	2				
C4	[illegible]	1				
C5, C6	[illegible]	2				
T1	[illegible]	[illegible]				
A4	74LS00	1				
L1	64 uh	1				

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FOLDOUT FRAME

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVAL

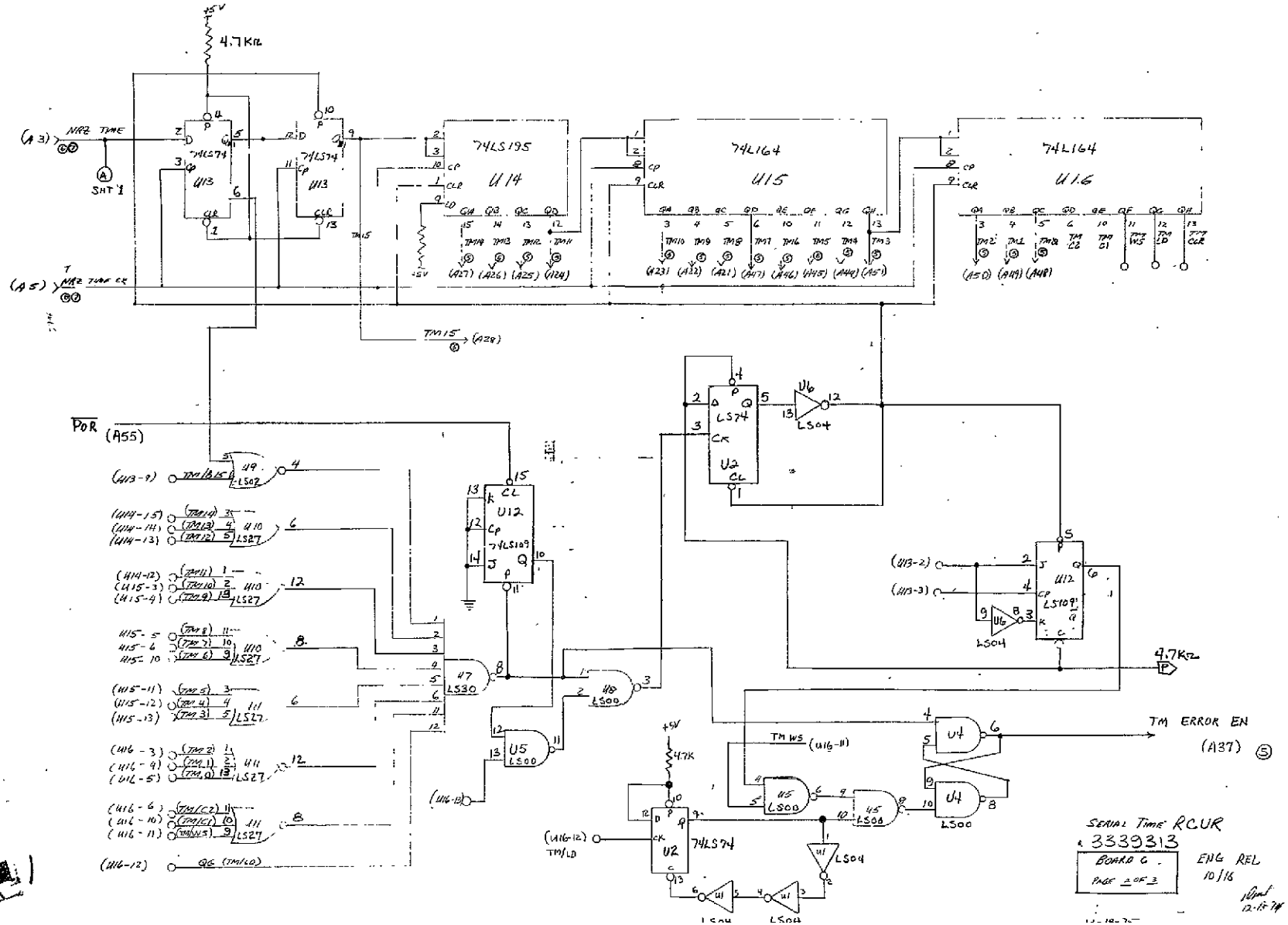
CTI SERIAL TIME RECEIVER

(Bd #6)

SIZE	CODE IDENT NO.	DWG NO.
C	17981	3339313

SCALE | UNIT WT. | SHEET 1 OF 3

FOLDOUT FRAME



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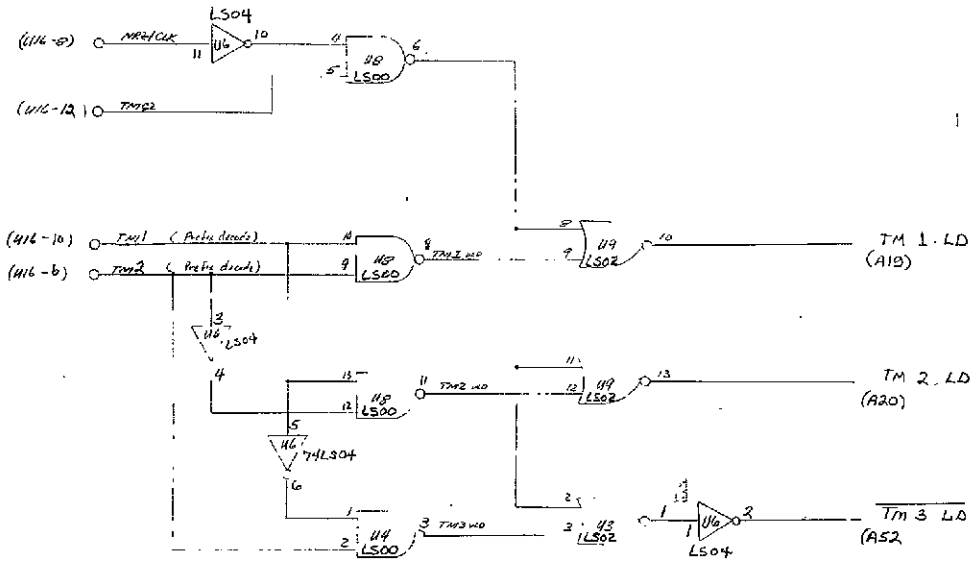

Parts For
Sheets 2 & 3 ONLY

DESIG.	PART TYPE	QTY.	PWR	PIN	PIN	SPARE
U6 1	74LS04	2		14	7	
U10, U11	74LS27	2		14	7	
3,9	74LS02	2		14	7	
4,5,8,	LS00	3		14	7	
U7	LS30	1		14	7	
13 2	LS74	2		14	7	
U14	LS145	1		16	8	
U15, U16	74	2		14	7	
U12	74LS109	1		16	8	1

+5V → (A1)(A2)
GND → (A59)(A60)

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SERIAL TIME REV
3339313
BOARD C
PAGE 3 OF 3
ENG REL
10/16
12-26-79
4-18-77

FOLDOUT FRAME

FOLDOUT FRAME

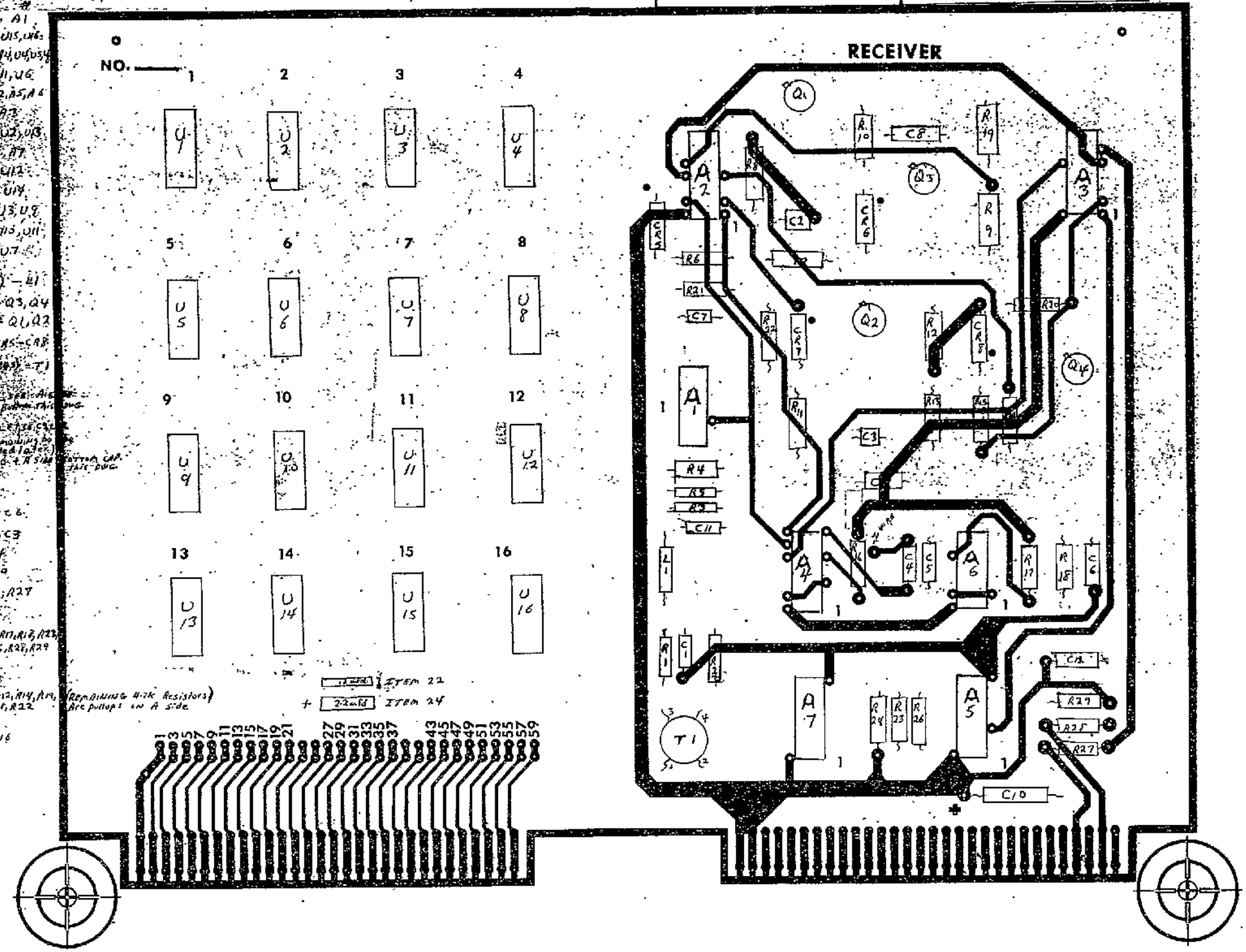
SCALE-2/1

SCI	SCALE 2/1	PART NO. [redacted]
UNIT NAME: RECEIVER		LAYER NO. COMPONENT SIDE
SYSTEM		TAPED BY/DATE: [illegible] 19 SEPT 74
		CHECKED BY/DATE:

3339313-2

ENG REL 10/11

ITEM #		DESIGN #
(2)	LM360	A1
(3)	74L164N	U15, U16
(4)	74LS00N	A4, U4, U5
(5)	74LS04N	U1, U6
(6)	74LS05N	A2, A5, A6
(7)	74LS10N	A3
(8)	74LS74N	U2, U13
(9)	74LS86N	A7
(10)	74LS109N	U12
(11)	74LS195N	U14
(12)	74LS02N	U3, U8
(13)	74LS27N	U10, U11
(14)	74LS30N	U7
(16)	1537-68 (68μH)	L1
(17)	2N2369A	Q3, Q4
(18)	2N3251A	Q1, Q2
(19)	1N4454	CR5 - CR8
(20)	T1 (783239-385)	T1
(22)	UK25104 (.1μf)	SEE: A15 [illegible] Bottom this DWG.
(23)	UK25103 (.01μf)	[illegible] (Remaining to be loaded later.)
(24)	2.2 μf	C10 + R side Bottom cap. this DWG.
(25)	22 pf	C1
(26)	68 pf	C11
(27)	220 pf	C5, C6
(28)	330 pf	C2, C3
(29)	430 pf	C4
(30)	91Ω	R30
(31)	470Ω	R4, R27
(32)	1.1K	R1
(33)	1.8K	R10, R15, R17, R18, R23, R24, R26, R28, R29
(34)	2K	R6, R11
(35)	3K	R8, R13
(36)	4.7K	R7, R9, R12, R14, R19, R20, R21, R22 (Remaining 4.7K Resistors are pullups on A side)
(37)	15K	R3
(38)	47K	R5, R16



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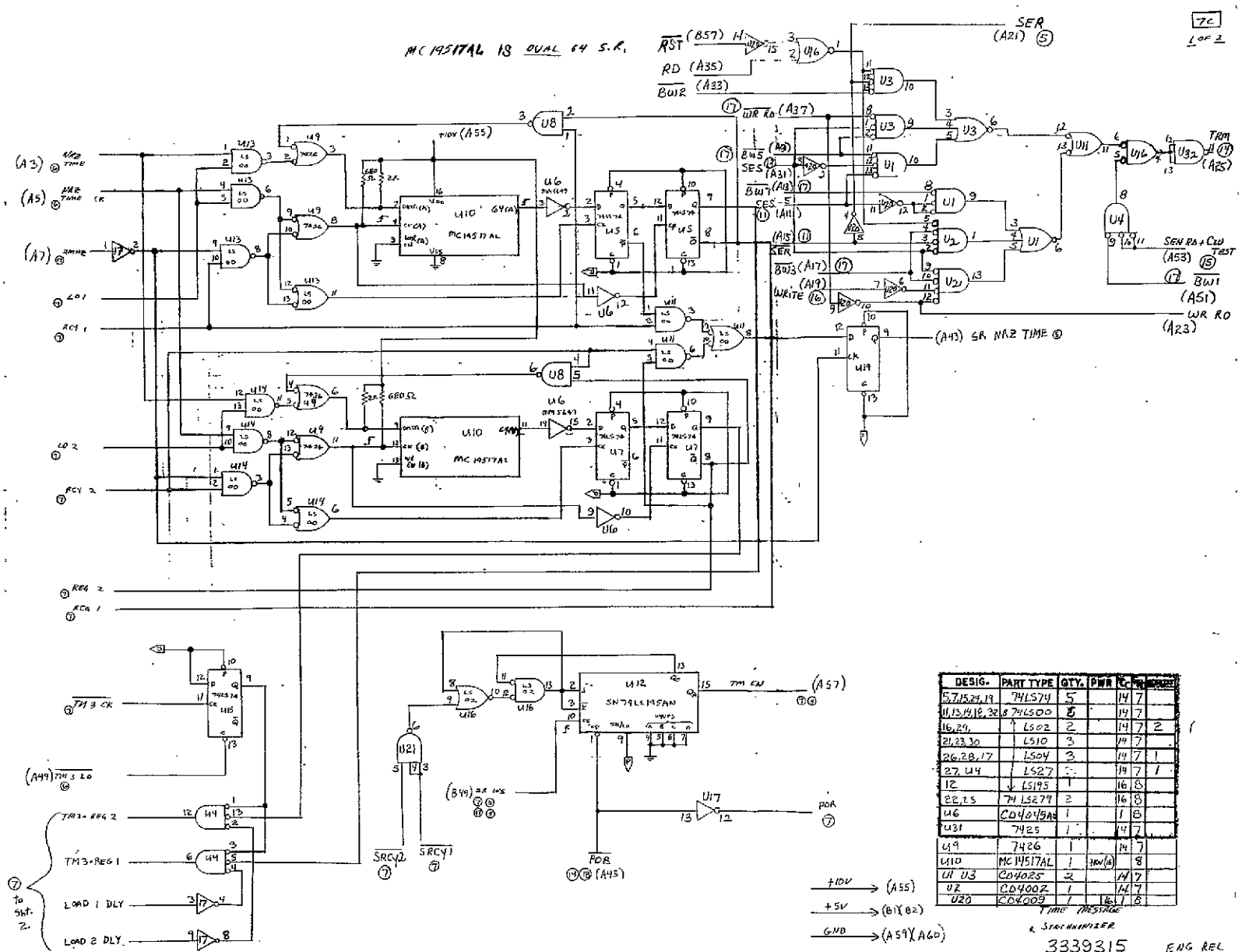
FOLDOUT FRAME

FOLDOUT FRAME 2



DESIG.	PART TYPE	QTY.	PWR	PIN	SOCKET
5,7,15,24,19	74LS74	5		14	7
11,13,14,16,32	74LS00	5		14	7
16,29,	LS02	2		14	7
21,23,30	LS10	3		14	7
26,28,17	LS04	3		14	7
27, U4	LS27	3		14	7
12	LS195	1		16	8
22,25	74LS279	2		16	8
U6	CD4049AE	1		16	8
U31	7425	1		14	7
U9	7426	1		14	7
U10	MC14517AL	1	+10V(16)		8
U1 U3	CD4025	2		14	7
U2	CD4002	1		14	7
U20	CD4009	1		16	8

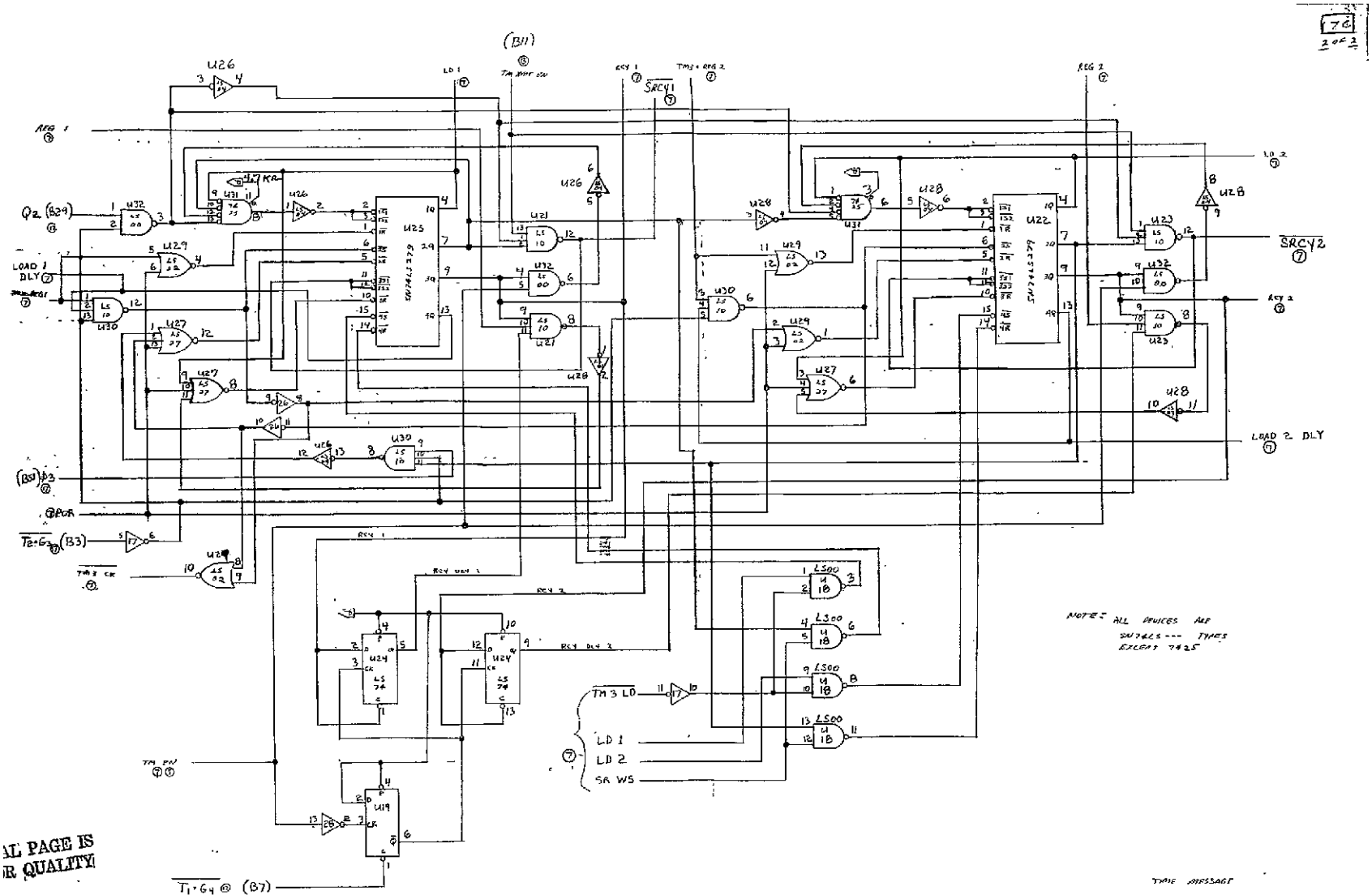
TIME MESSAGE & SYNCHRONIZER

3339315

BOARD 7
PAGE 1 OF 2

ENG REL 10/8

4-2375



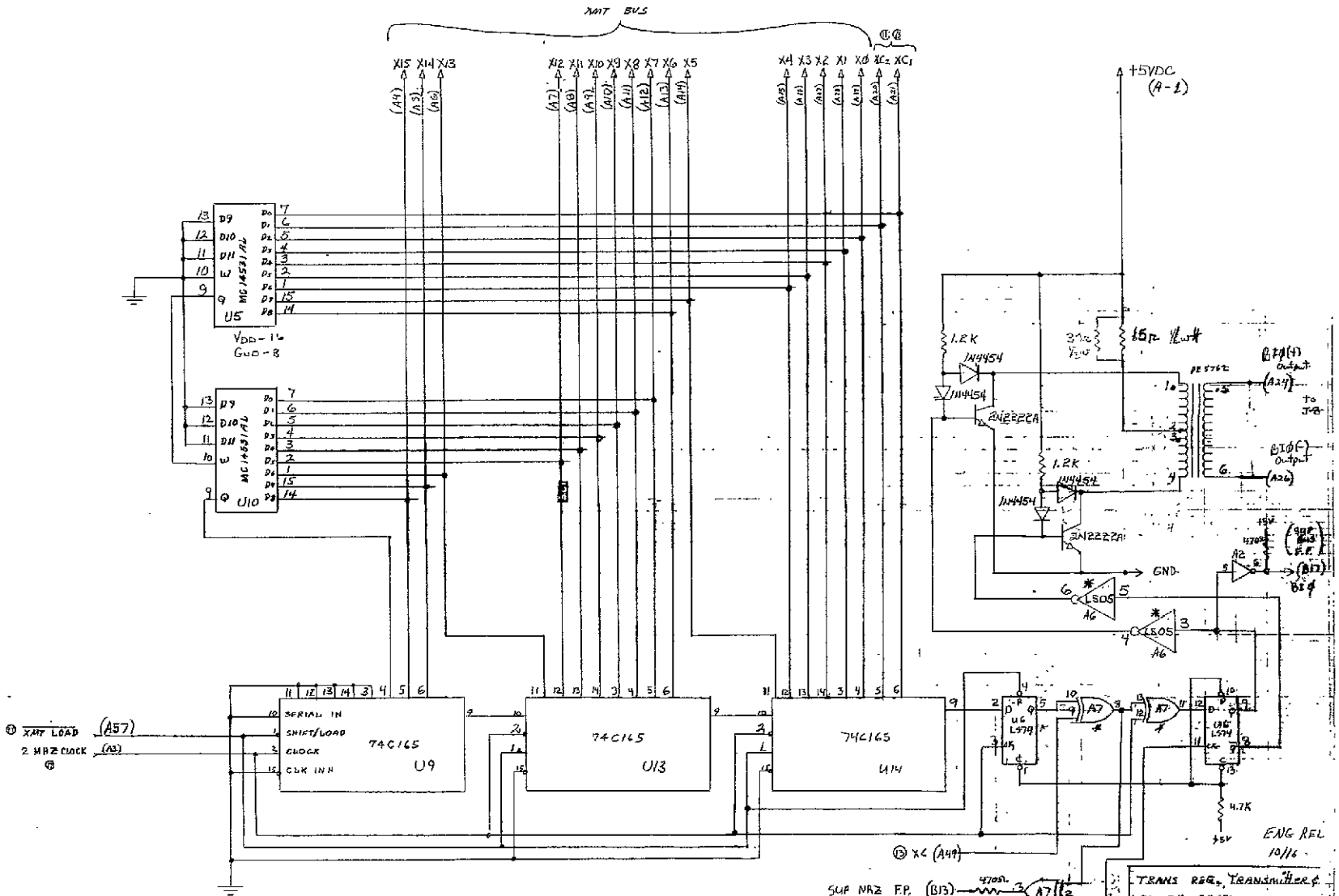
THIS MESSAGE
CONTROL LOGIC

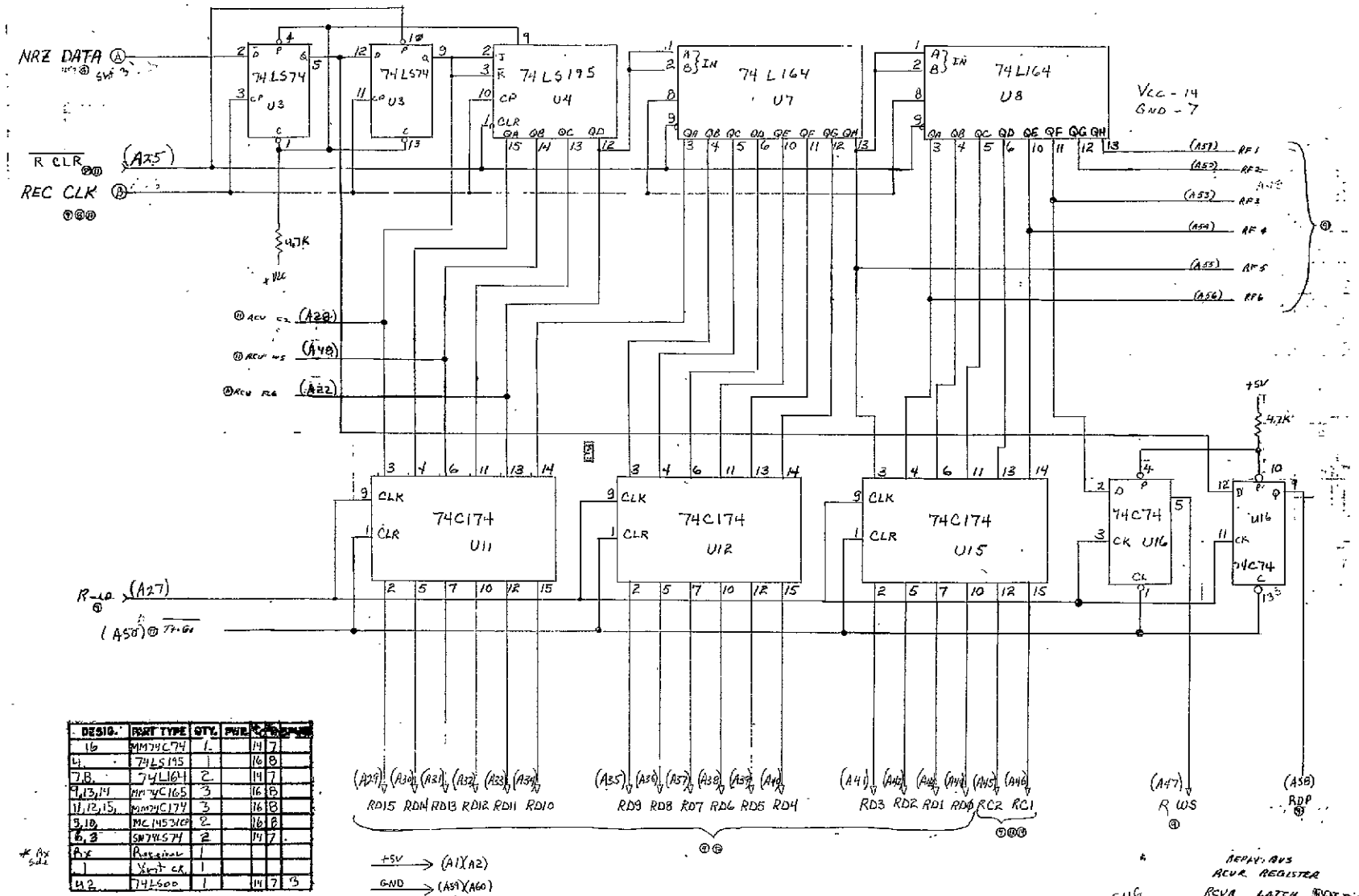
3339315

BOARD 7
PAGE 2 OF 2

ENG REL 10/16

4-23-75





DESIG.	PART TYPE	QTY.	PWR.		
16	MM74C74	1		14	7
4	74LS195	1		16	8
7,8	74L164	2		14	7
9,13,14	MM74C165	3		16	8
11,12,15	MM74C174	3		16	8
5,10	MC14538CP	2		16	8
6,3	SN74S74	2		14	7
Rx	Resistor	1			
1	Xtal ck	1			
U2	74LS00	1		14	7

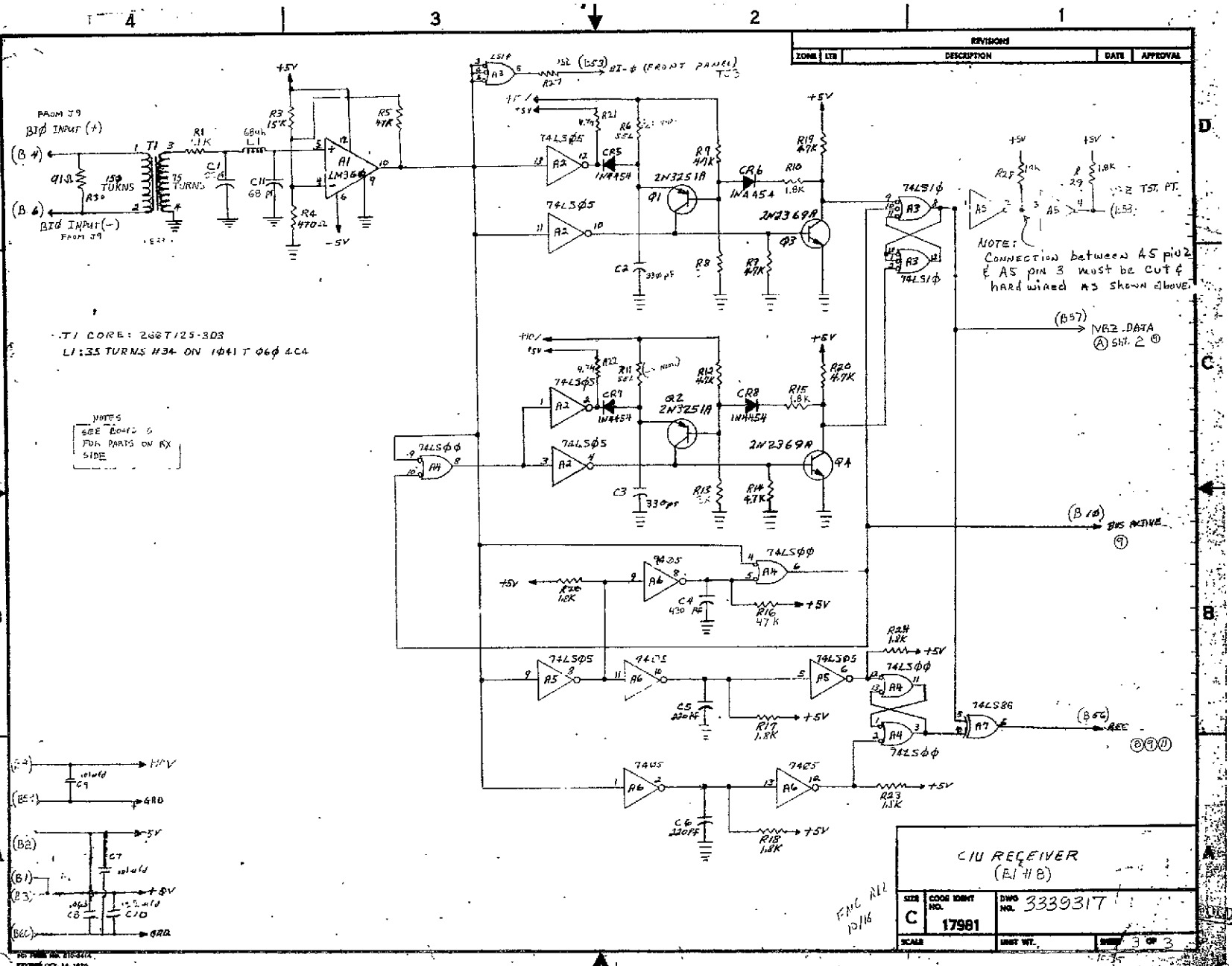
REPLAY BUS RCVR REGISTER
RCVR LATCH
3339317
BOARD B.
PAGE 2 OF 3

ENG REL 10/16

4-18-75

FOLDOUT FRAME

FOLDOUT FRAME



SCALE-2/

SCI | SCALE 2/1

SYSTEM NAME RECEIVER

SYSTEM

3339317-2

PART NO 3339018-1

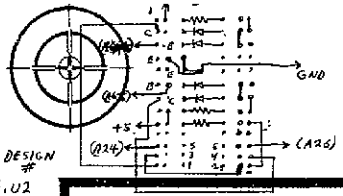
LAYER NO COMPONENT SIDE

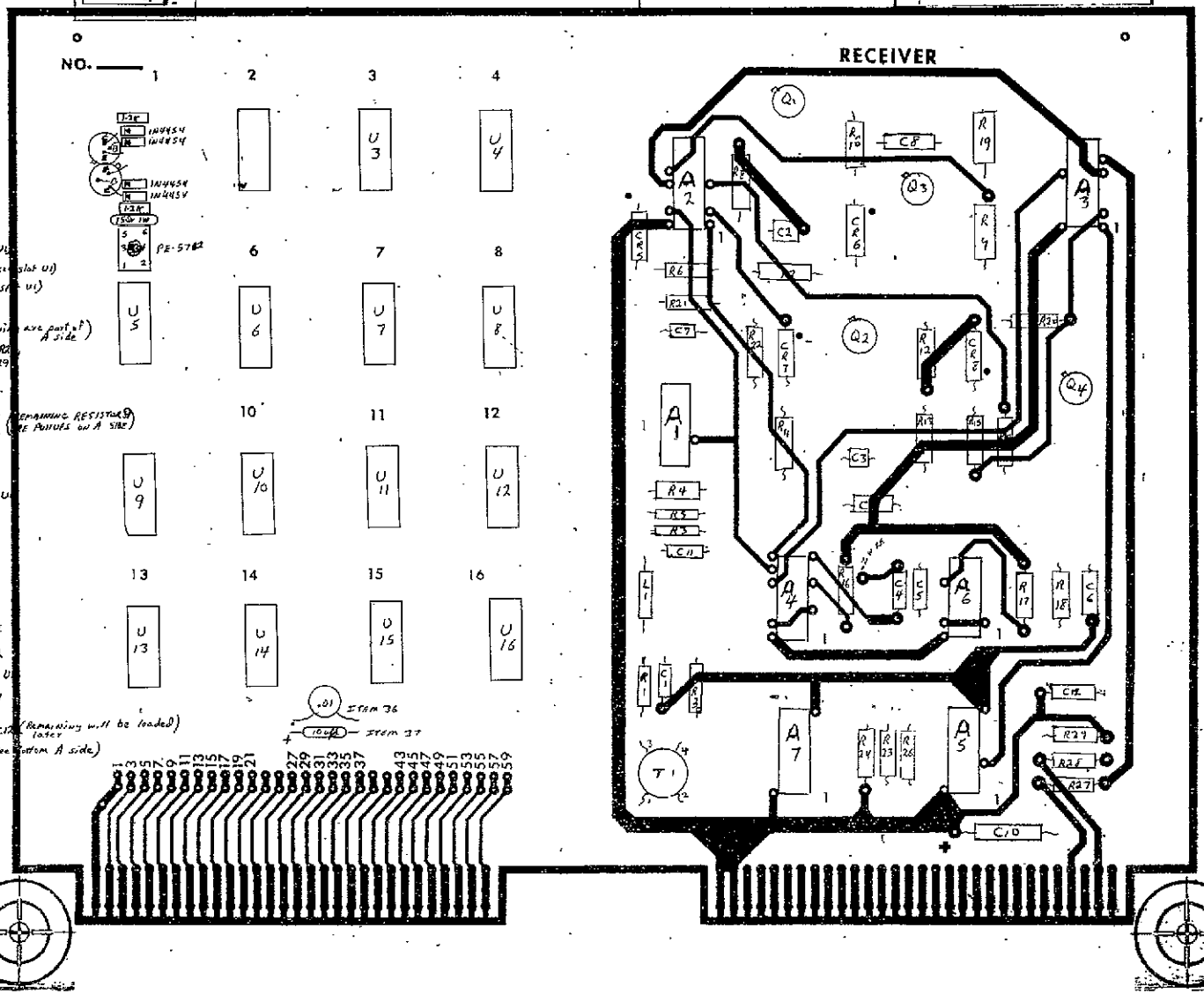
TAPED BY DATE Gilbert 19 SEPT 74

CHECKED BY/DATE

ENG REL 2/16

ITEM #	DESIGN #
2	74LS00N - A4, U2
3	74LS05N - A2, A5, A6
4	74LS10N - A3
5	74LS74N - U3, U6
6	74LS86N - A7
7	74LS175N - U4
8	74LI64N - U7, U8
9	74C165N - U9, U13, U14
10	74C174N - U11, U12, U15
11	MC14553CP - U5, U10
12	74C74N - U16
13	LM360N - A1
14	2N2222A - (See slot U1)
15	1N4454 - CR5 - CR8 (Also see slot U1)
16	1.2KΩ - R1 (Also see slot U1)
17	91Ω - R30
18	470Ω - R4, R27 (Remaining are part of A side)
19	1.PKΩ - R13, R15, R17, R19, R20, R24, R24, R23, R29
20	2KΩ - R6, R11
21	3KΩ - R8, R13
22	4.7KΩ - R7, R9, R12, R14, R16, R18, R22, R21, R22 (REMAINING RESISTORS ARE POTTED ON A SIDE)
23	15KΩ - R3
24	47KΩ - R5, R16
25	15Ω, 1W - See slot U1
26	22pF. - C1
27	68pF. - C11
28	330pF. - C2, C3
29	430pF - C4
30	220pF. - C5, C6
31	2N2369A - Q3, Q4
32	2N3251A - Q1, Q2
33	PE-5762 - See Slot U1
34	Ass'y 3339345 - T1
36	.01 mfd - C7, C8, C9, C12 (Remaining will be loaded later)
37	10 mfd - C10 (Also see bottom A side)
39	1537-28uh - L1





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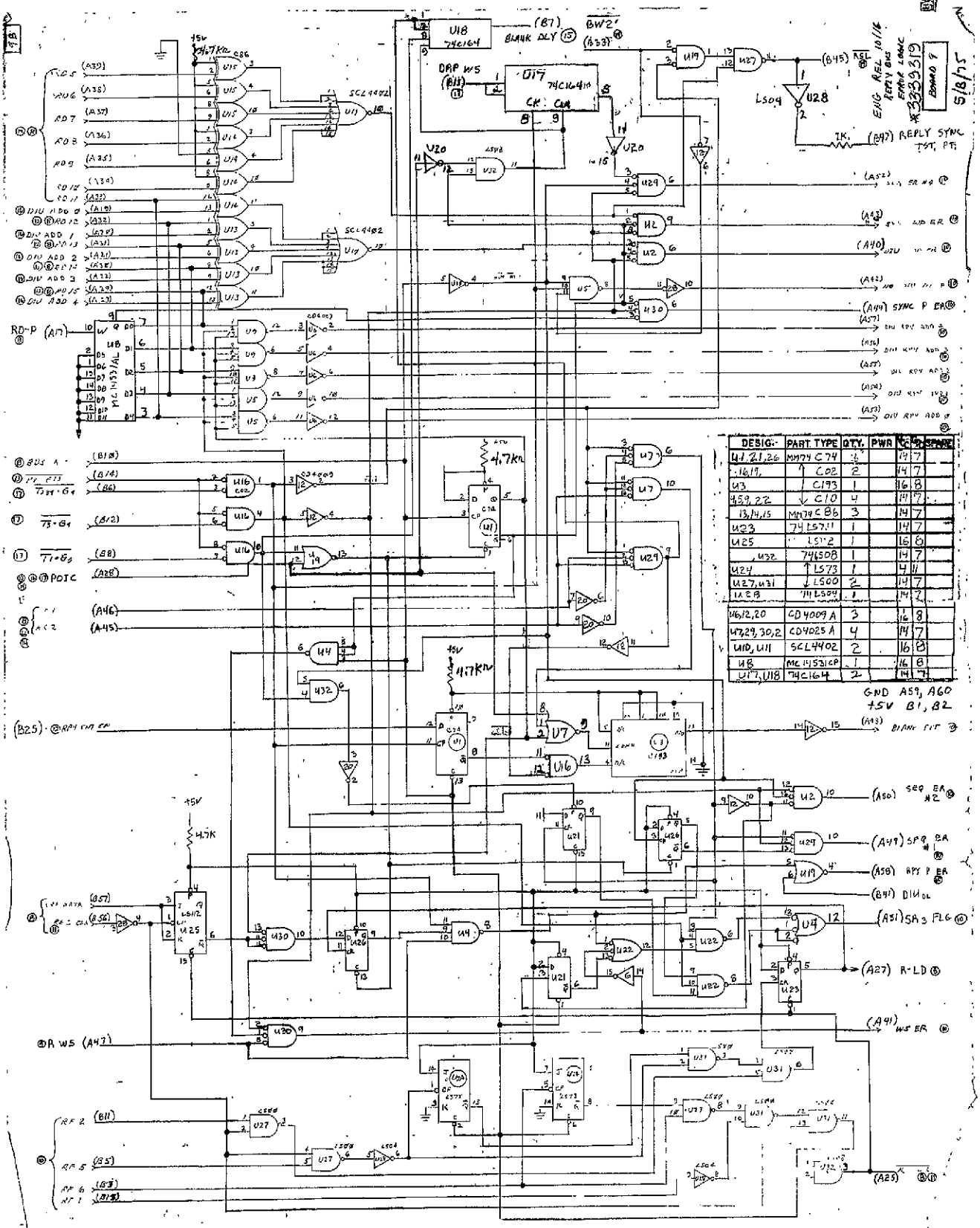
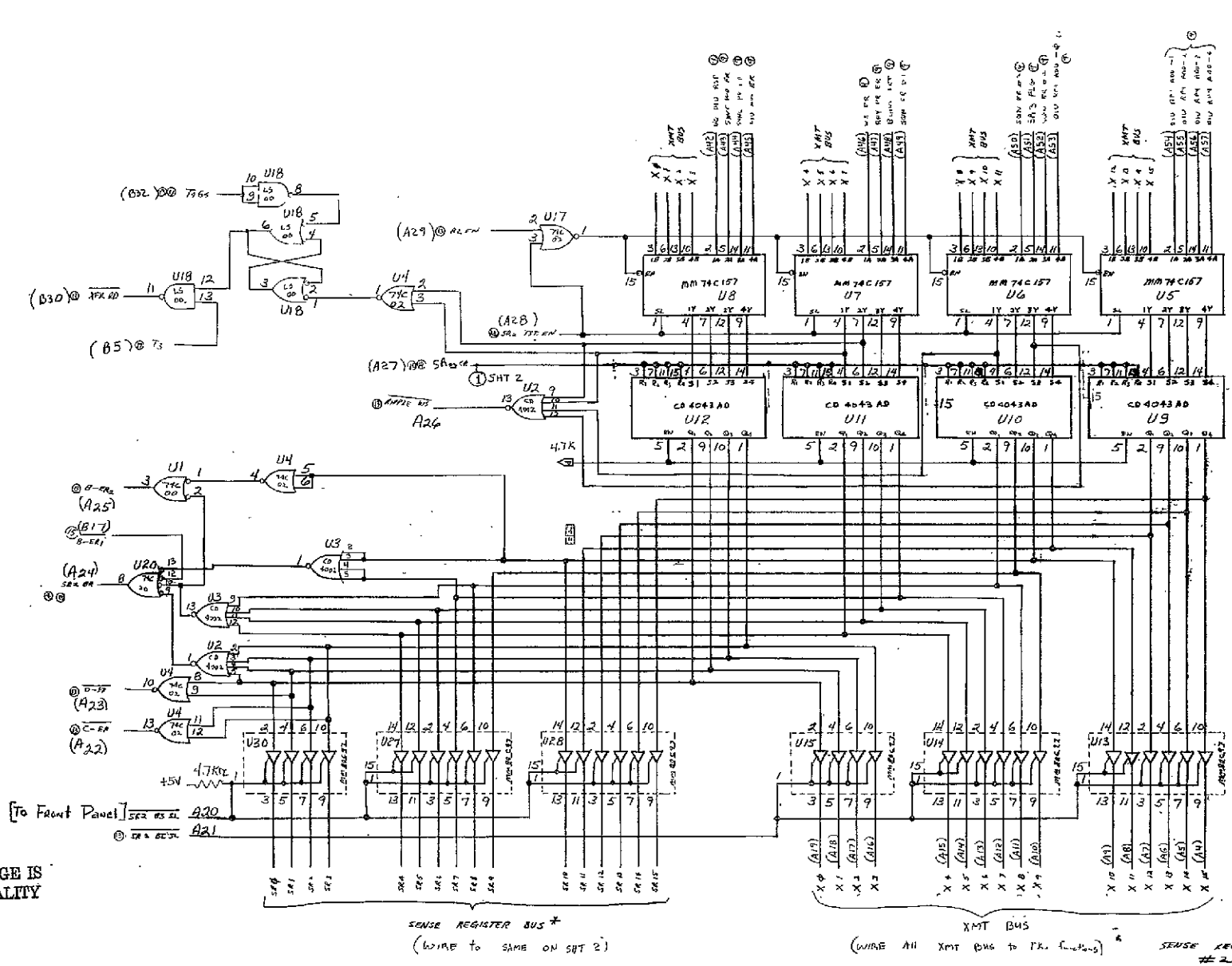
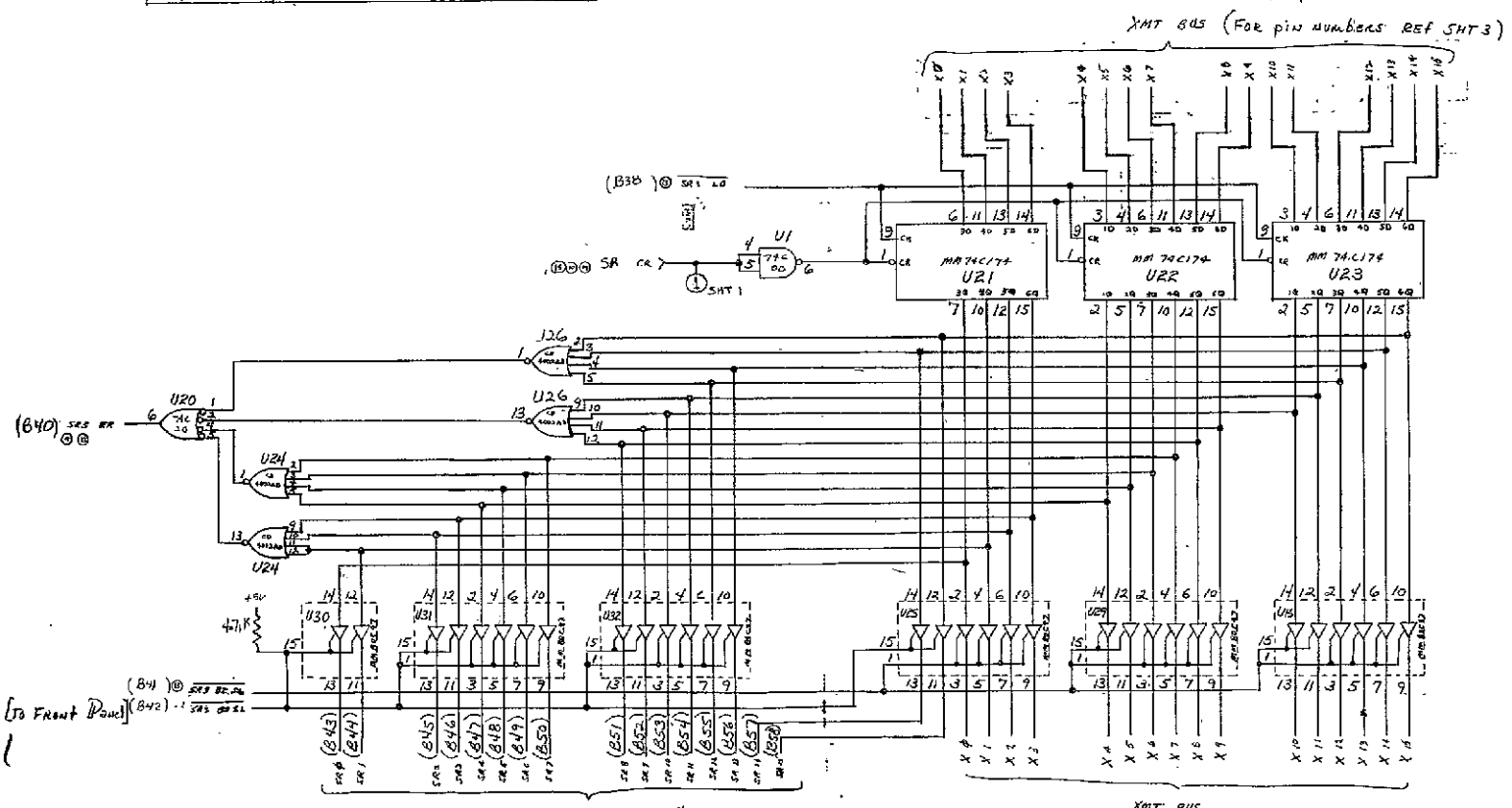


DESIG.	PART TYPE	QTY.	PWR	GND	SPARE
U1,21,26	MM74C74	3		14	7
16,19,	C02	2		14	7
U3	C193	1		16	8
459,22	C10	4		14	7
13,14,15	MM74C86	3		14	7
U23	74LS74	1		14	7
U25	LS112	1		16	6
U32	74LS08	1		14	7
U24	LS73	1		4	11
U27,U31	LS00	2		14	7
U28	74LS04	1		14	7
U6,12,20	CD4009A	3		16	8
U7,29,30,2	CD4025A	4		14	7
U10, U11	SCL4402	2		16	8
U8	MC14531CP	1		16	8
U17,U18	74C164	2		14	7

GND A59, A60
+5V B1, B2

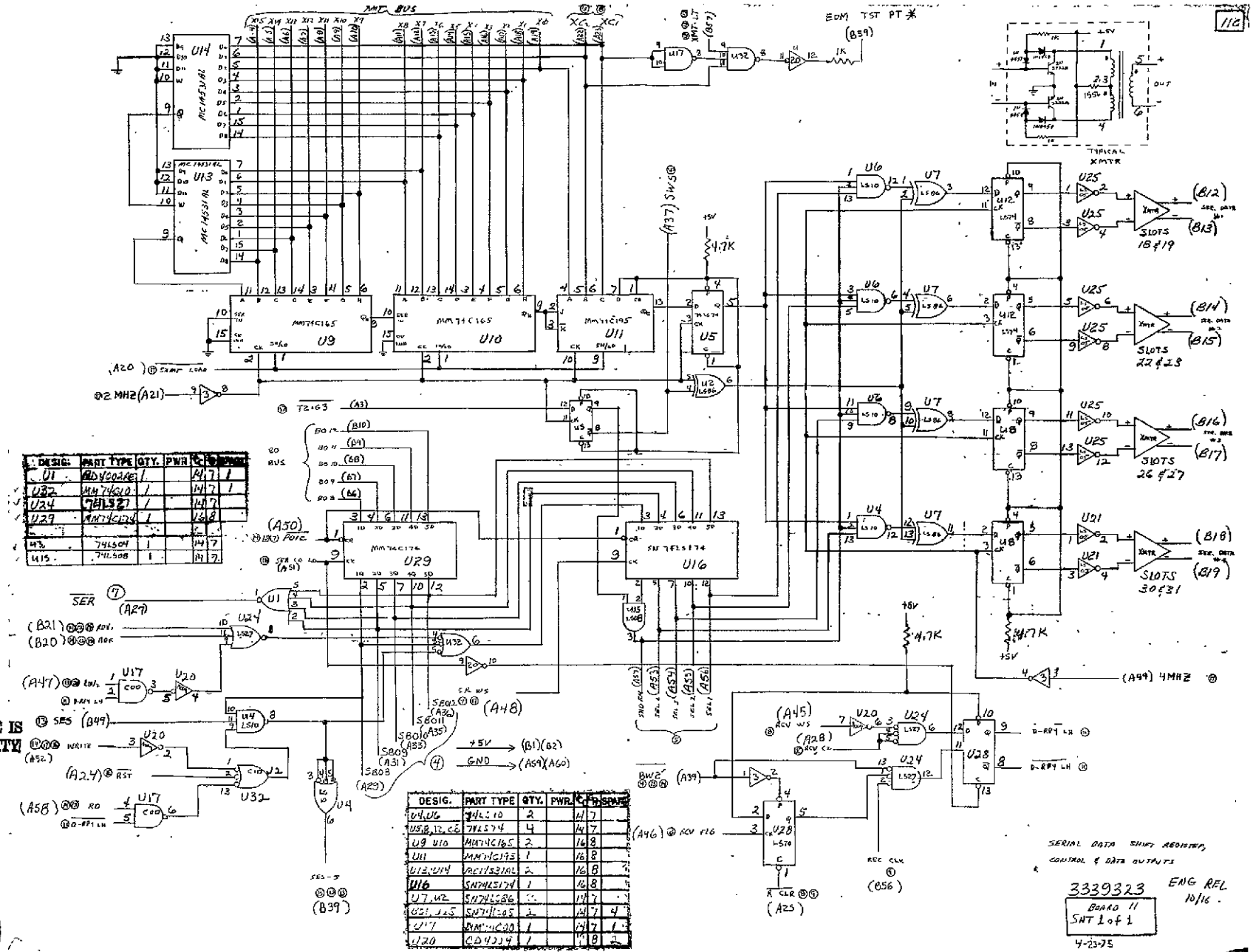


QTY	REF DES	PART NO.	SPARES	VCC PIN	GND PIN
1	U1,	74C00	1	14	7
2	U4, U17	74C02	3	14	7
1	U20	74C20		14	7
11	U27-U32, U13-U16, U25	80C97		16	8
4	U5-U8	74C157		16	8
4	U2, U3, U24, U26	CD4002		14	7
4	U9-U12	CD4043		16	8
1	U18	74LS00		14	7



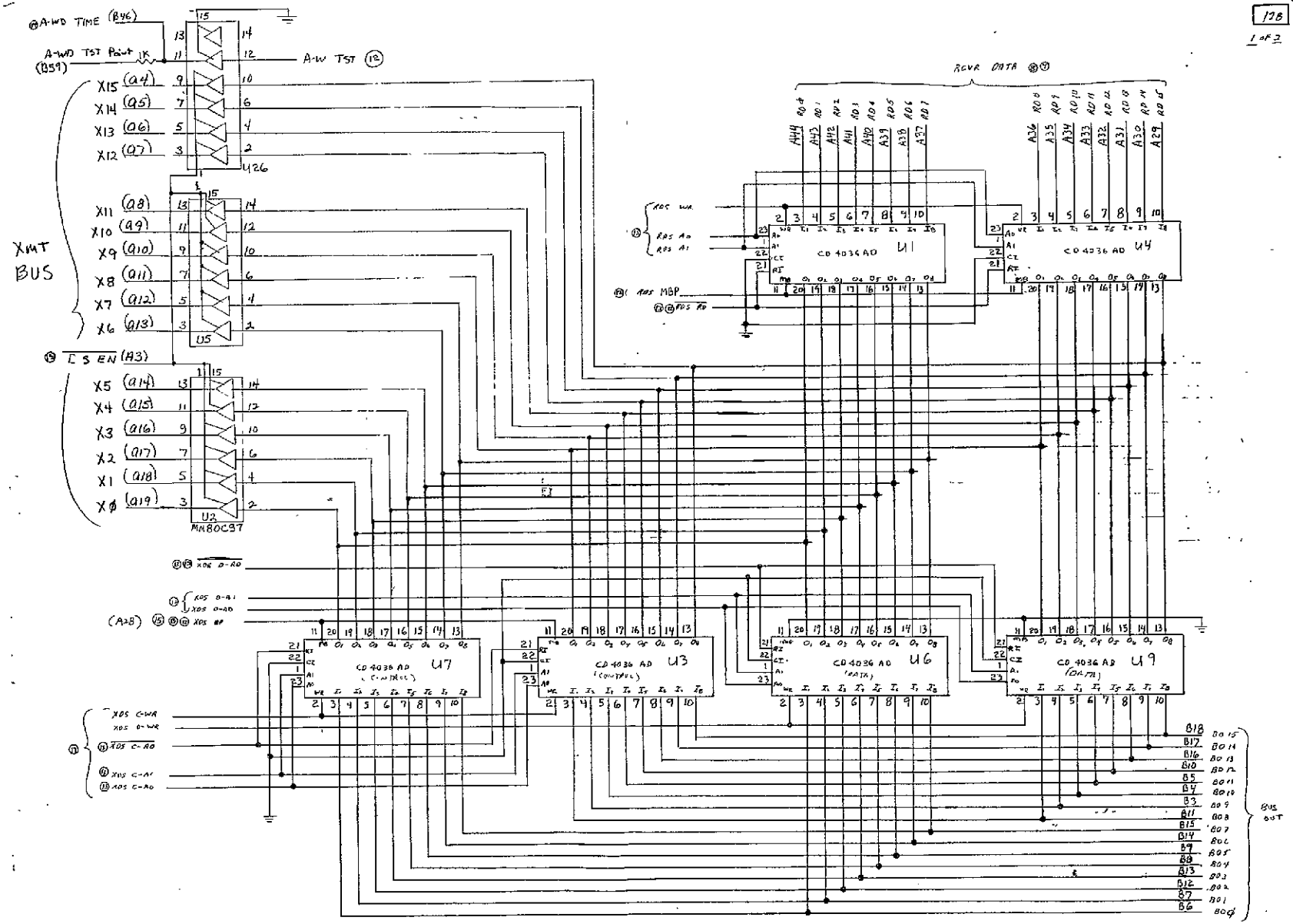
SENSE REGISTER #3
3339321
BOARD 10
PAGE 2 OF 2
4-18-75
ENG REL
10/16

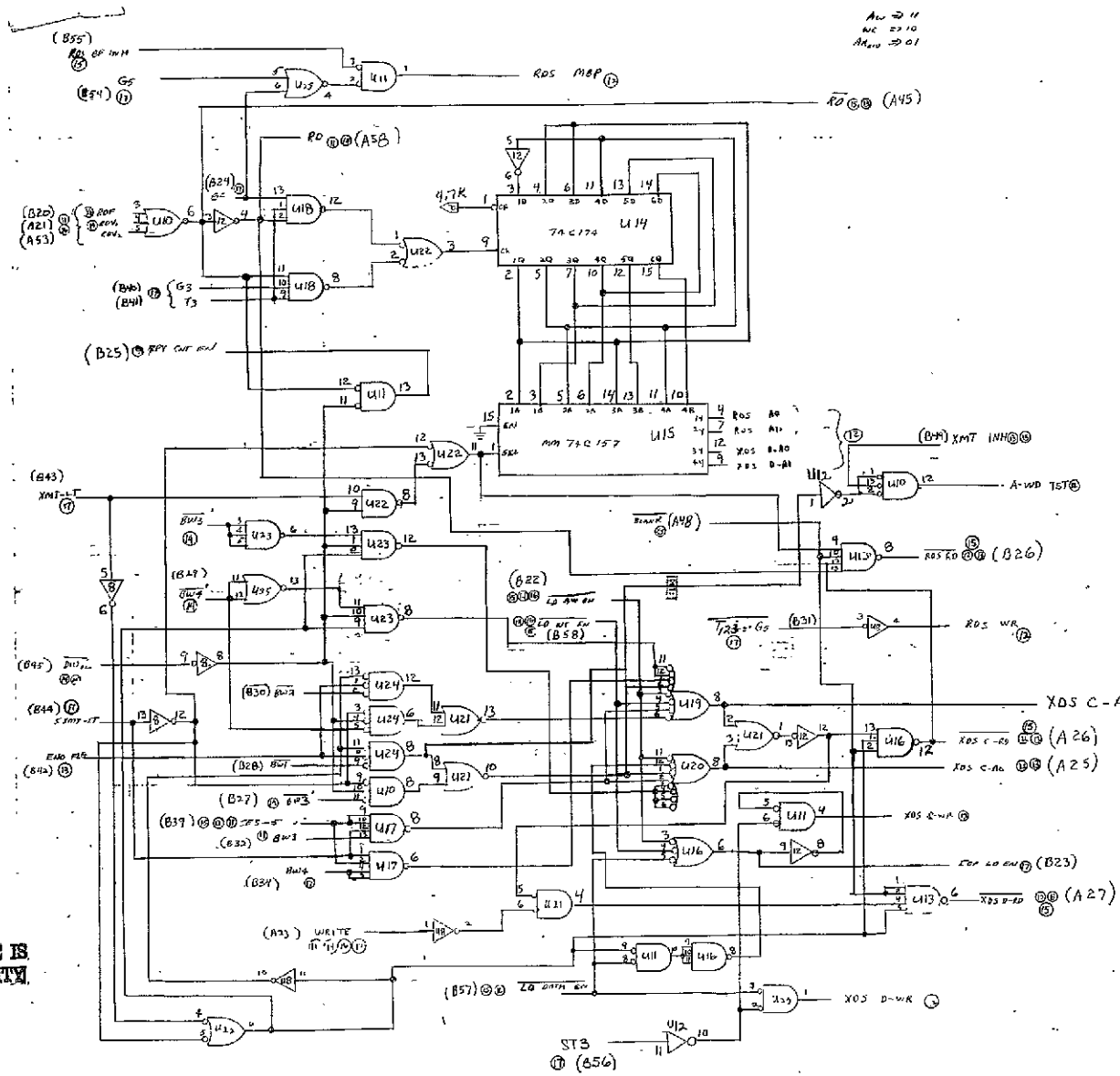
C14



DESIG.	PART TYPE	QTY.	PWR.	GND	SPARE
U1	74LS04	1		14	7	1
U32	MM74C10	1		14	7	1
U24	74LS27	1		14	7	
U29	MM74C174	1		16	8	
U3,	74LS04	1		14	7	
U15	74LS08	1		14	7	

DESIG.	PART TYPE	QTY.	PWR.	GND	SPARE
U4,U6	74LS10	2		14	7	
U5,12,16	74LS74	4		14	7	
U9 U10	MM74C165	2		16	8	
U11	MM74C195	1		16	8	
U12,U14	MC14552B	2		16	8	
U16	SN74LS174	1		16	8	
U7,U2	SN74LS86	2		14	7	
U21, 25	SN74LS05	2		14	7	4
U17	MM74C00	1		14	7	1
U20	CD4011	1		14	8	2


A-WD TIME (B46)
A-WD TST Point (B59)
A-W TST (12)
XMT BUS
X15 (Q4)
X14 (Q5)
X13 (Q6)
X12 (Q7)
X11 (Q8)
X10 (Q9)
X9 (Q10)
X8 (Q11)
X7 (Q12)
X6 (Q13)
X5 (Q14)
X4 (Q15)
X3 (Q16)
X2 (Q17)
X1 (Q18)
X0 (Q19)
U26
U5
U2
MN80C97
CS EN (A3)
RCVR DATA
CD4036AD U1
CD4036AD U4
CD4036AD U7 (CONTROL)
CD4036AD U3 (CONTROL)
CD4036AD U6 (DATA)
CD4036AD U9 (DATA)
BUS OUT
DATA STORAGE
*3339325
BOARD 12
PAGE 1 OF 3
ENG REL
10/16
FOLDOUT FRAME
FOLDOUT FRAME



DESIG.	PART TYPE	QTY.	PWR.			
U3,6,7,9	CD4036A	6		24	12	
U10, U24	74LS27	2		14	7	
U11,21,25	02	3		14	7	
U12, U8	04	2		14	7	1
U13,17	20	2		14	7	
U16,18,23	10	3		14	7	
U19, U20	30	2		14	7	
U22	74LS00	1		14	7	
U15	MM74C157	1		16	8	
U14	MM74C174	1		16	8	
U2, U5, U26	MM80C97	3		16	8	2

NOTE: To Locate I.C #U26 drill patern in middle of bd and hand-wire.

+5V B1, B2
GND A59, A60

NOTE: ALL DEVICES ARE 74LS-- UNLESS MARKED OTHERWISE

DATA STORAGE CONTROL LOGIC
#3339325 ENG REL
BOARD 12 PAGE 2 OF 2 10/16

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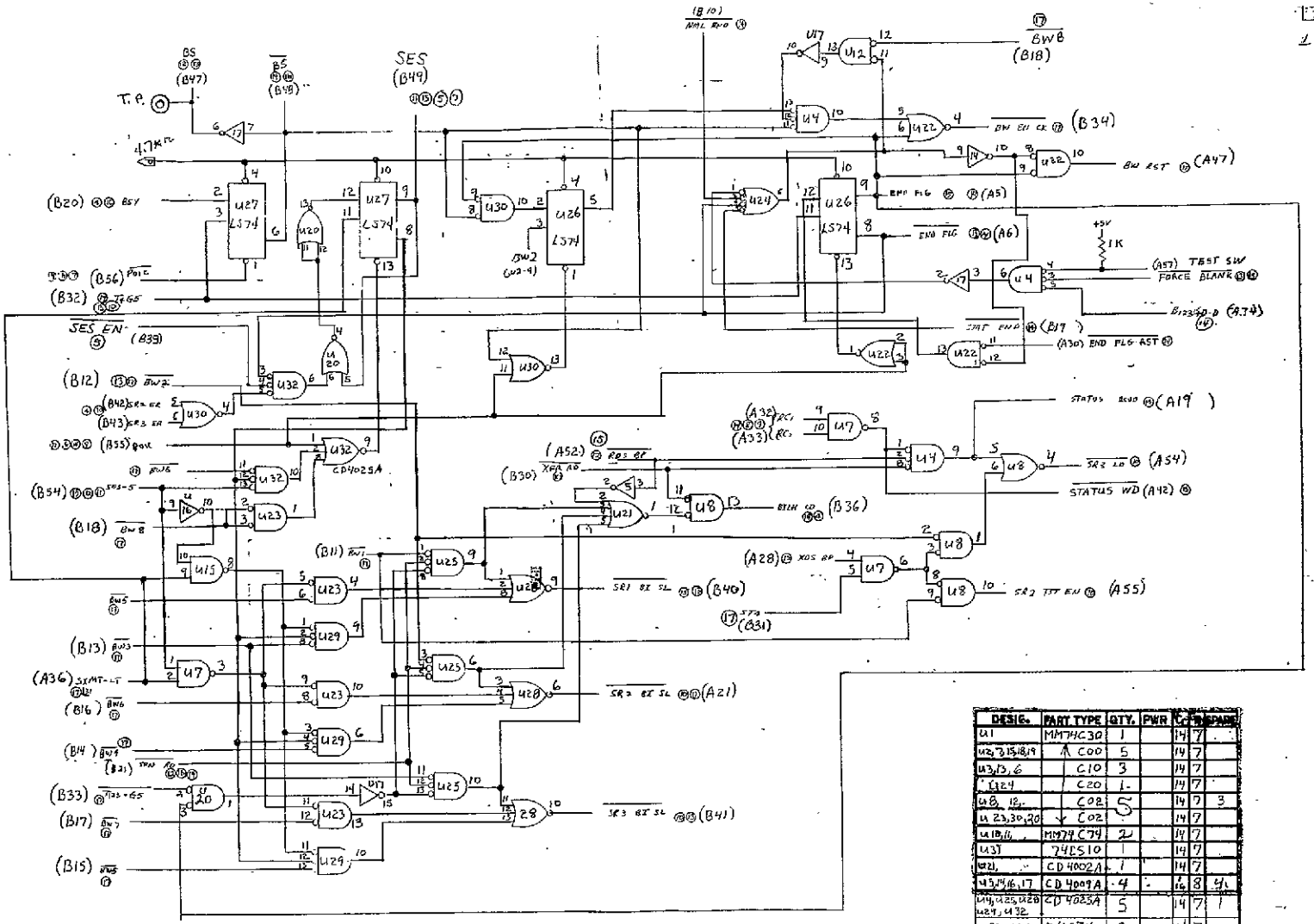

DESIG.	PART TYPE	QTY.	PWR	PIN	SPARE
U1	MM74HC30	1		14	7	
U2,3,15,18,19	C00	5		14	7	
U3,13,6	C10	3		14	7	
U24	C20	1		14	7	
U8, 12,	C02	5		14	7	3
U 23,30,20	C02			14	7	
U10,11	MM74C74	2		14	7	
U31	74LS10	1		14	7	
U21,	CD 4002A	1		14	7	
U5,14,16,17	CD 4009A	4		16	8	4
U4, U25, U28 U29, U32	CD 4025A	5		14	7	1
U27, U26	74LS74	2		14	7	
Test Point	SKT-102-PC	1	—	—	—	—
U9, U22	74LS02	2		14	7	

BUS CONTROL LOGIC
* 3339327
BOARD 13
PAGE 1 OF 1

4-21-75
ENG REL
10116

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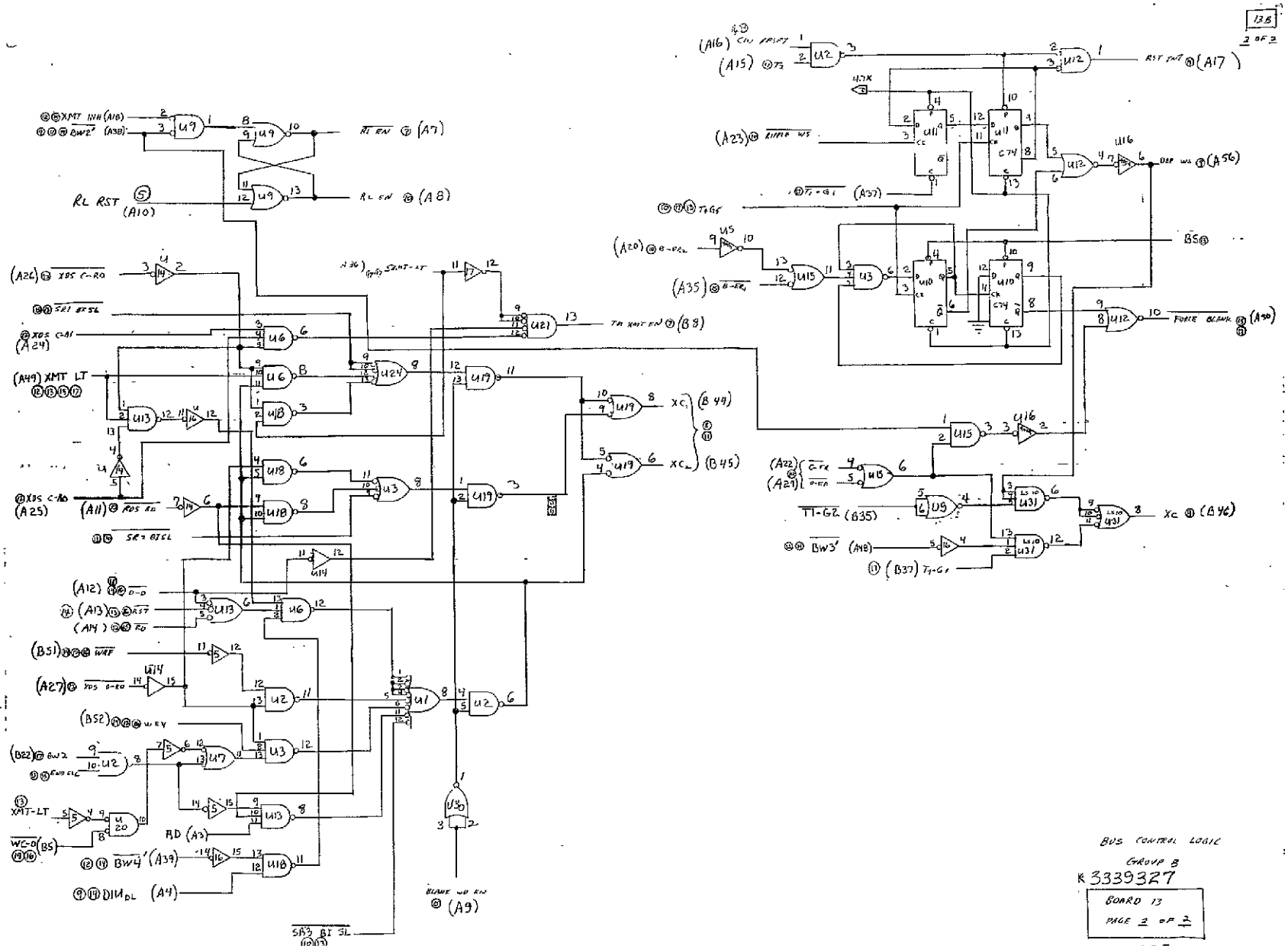
FOLDOUT FRAME

FOLDOUT FRAME


RL RST
(A10)
RL EN
(A8)
XMT LT
XMT-LT
RD (A3)
DIN DL (A4)
BLANK WD EN
(A9)
TM XMIT EN
(B8)
XC
(B49)
(B45)
FORCE BLANK
(A30)
BS
RST XMT
(A17)
DSP WS
(A56)
Xc
(B46)
T1-G2 (B35)
T1-G1 (B37)
BUS CONTROL LOGIC
GROUP B
K 3339327
BOARD 13
PAGE 2 OF 2
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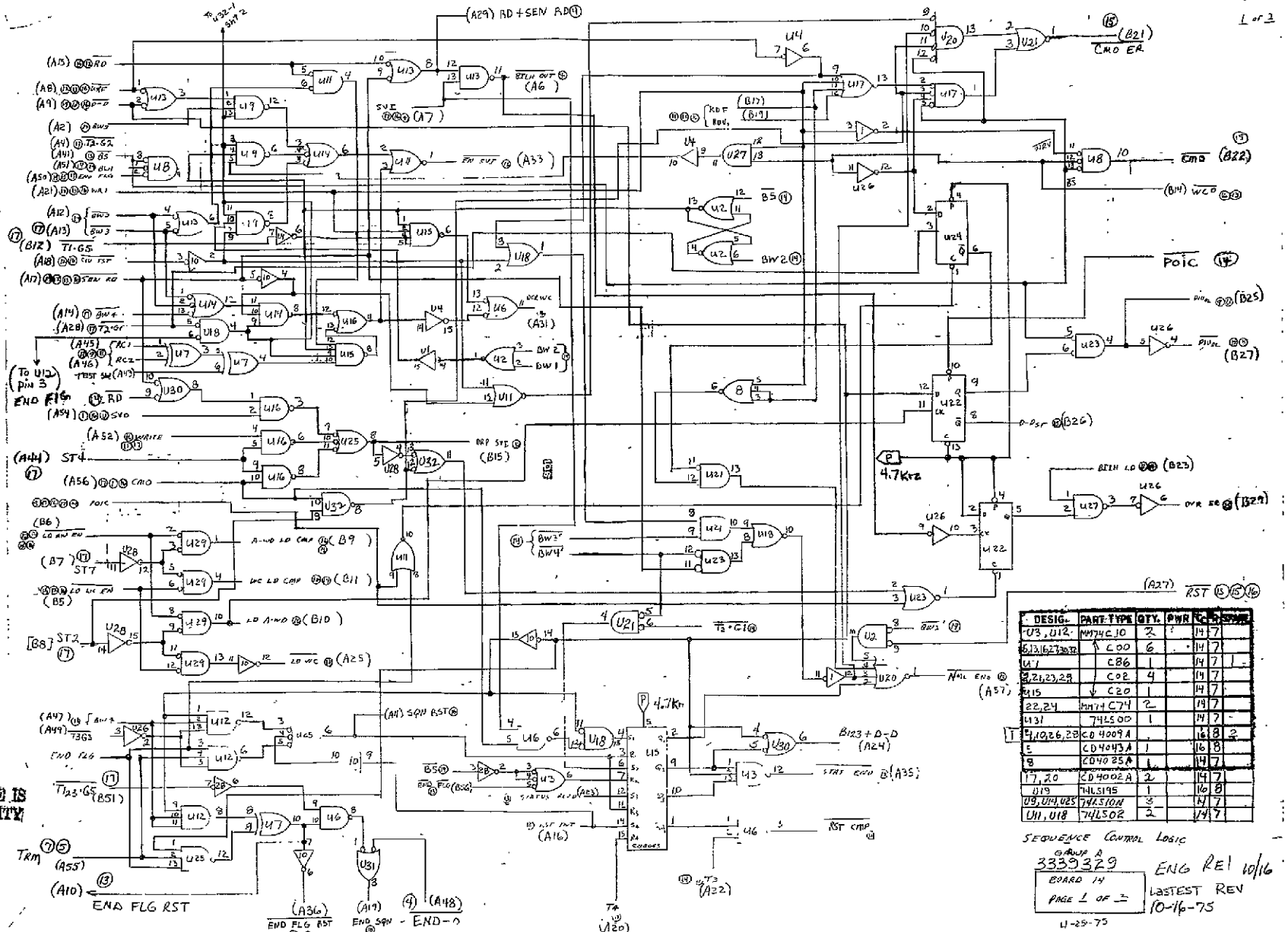
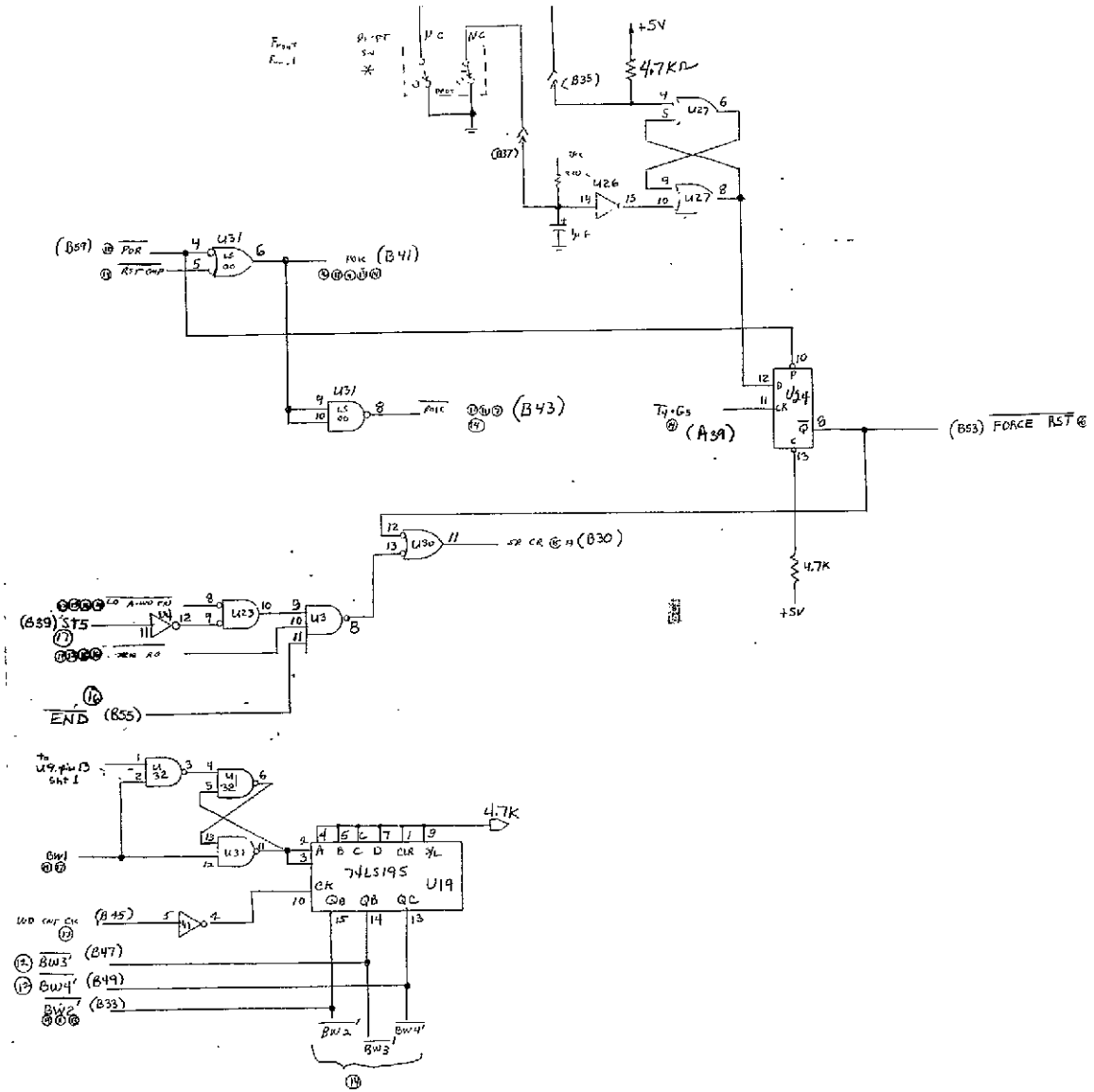
ENG REL
10/16
FOLDOUT FRAME
FOLDOUT FRAME



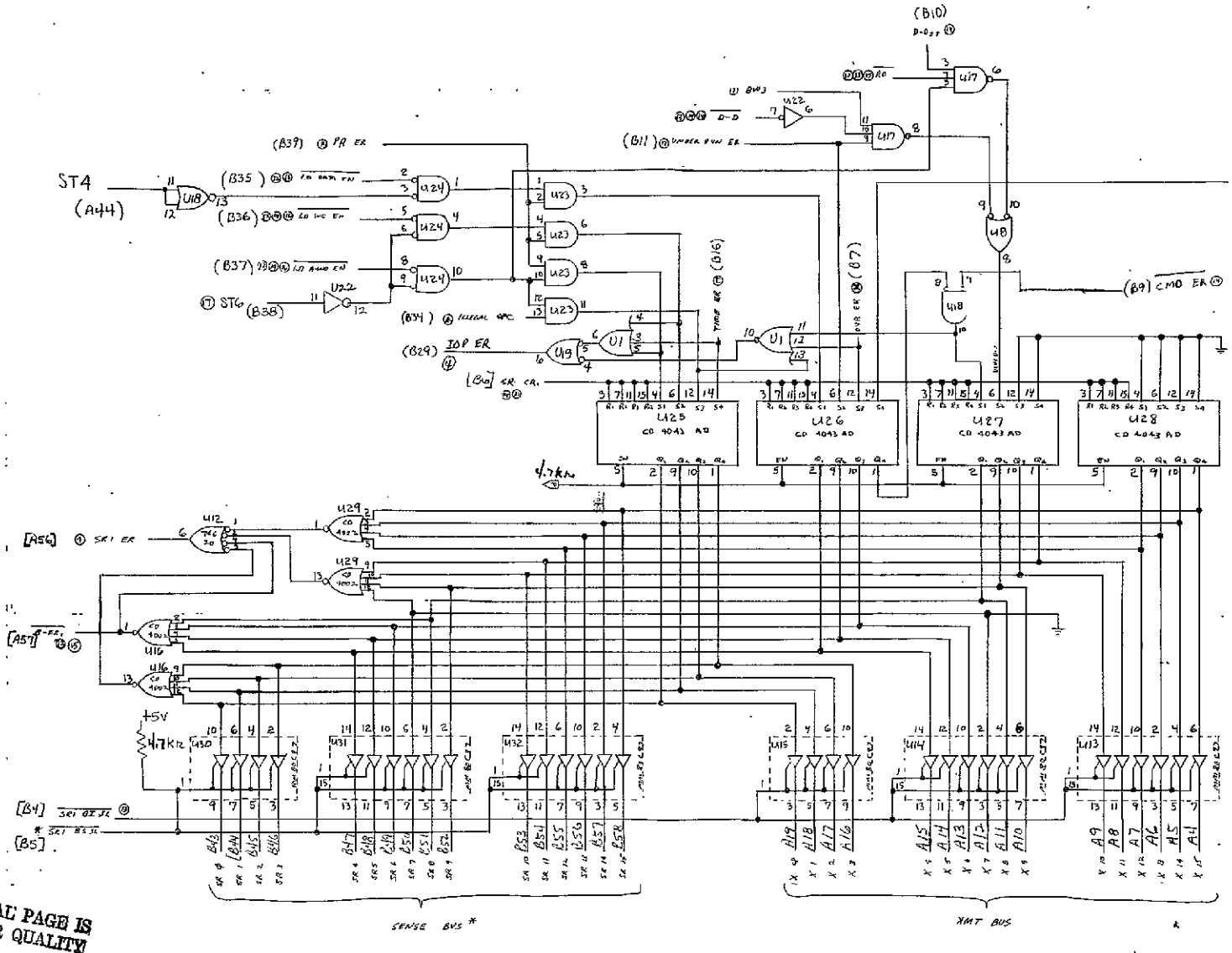
DESIG.	PART TYPE	QTY.	PWR		
U3, U12	MM74C10	2		14	7
5,13,6273033	C00	6		14	7
U1	C86	1		14	7
9,21,23,29	C02	4		14	7
U15	C20	1		14	7
22,24	MM74C74	2		14	7
U31	74LS00	1		14	7
4,1026,28	CD 4009A			16	8
5	CD4043A	1		16	8
8	CD4025A	1		14	7
17, 20	CD4002A	2		14	7
U19	74LS195	1		16	8
U9, U14, U25	74LS10N	3		14	7
U11, U18	74LS02	2		14	7

SEQUENCE CONTROL LOGIC
GROUP A
3339329
BOARD 14
PAGE 1 OF 2
ENG REL 10/16
LASTEST REV 10-16-75
11-25-75
5-14-75



+5V → (B1)(B2)
GND → (A59)(A60)

SEQUENCE CONTROL LOGIC
3339329
BOARD 14
PAGE 2 OF 2
ENG REL 10/16
4-22-75



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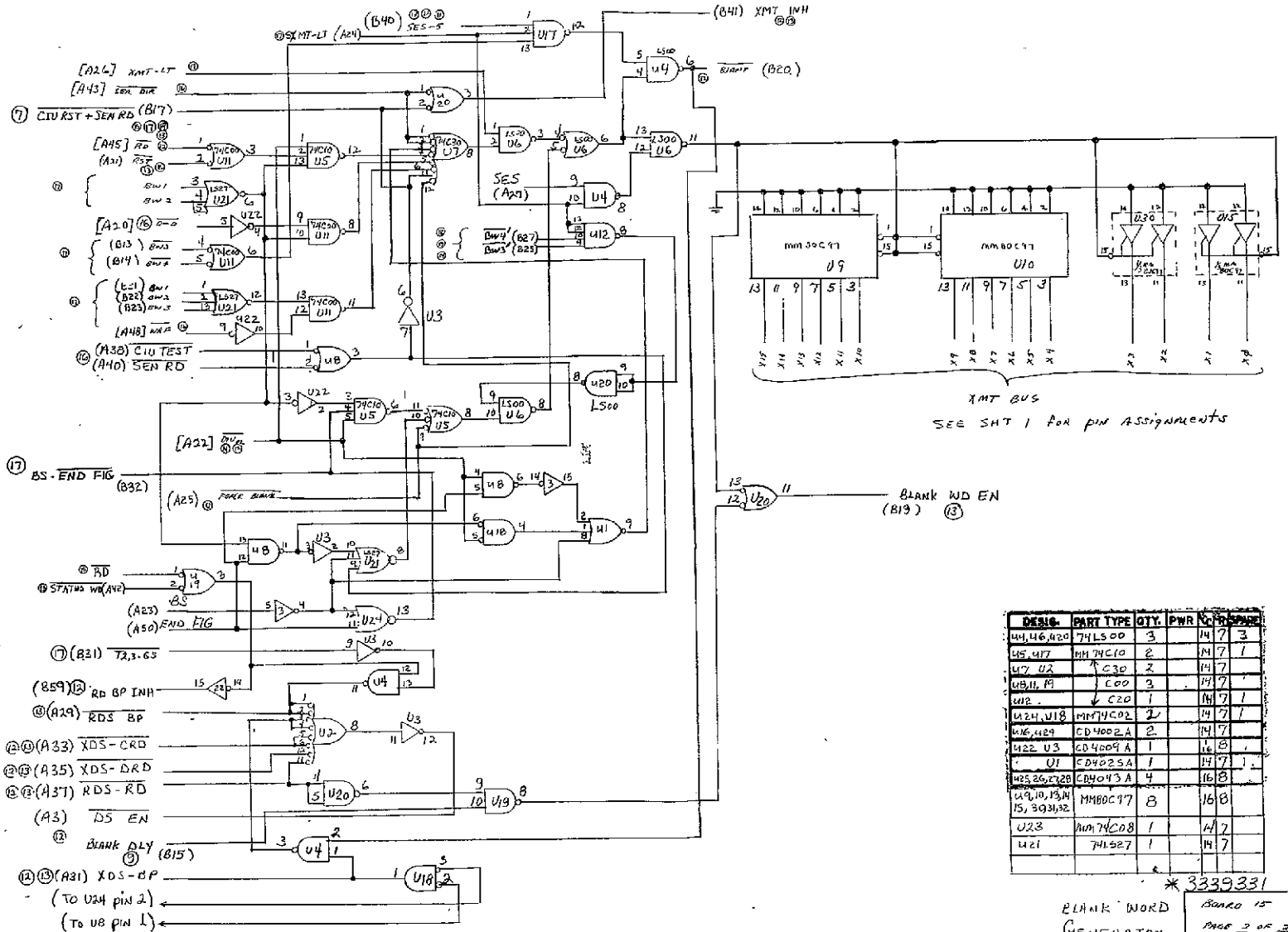
SENSE REGISTER
#1
GROUP A

ENG REL * 3339331
10/16 4-25-7

BOARD 15
PAGE 1 OF 3

FOLDOUT FRAME

FOLDOUT FRAME



DESIG.	PART TYPE	QTY.	PWR			
U4,U6,U20	74LS00	3		14	7	3
U5, U17	MM74C10	2		14	7	1
U7 U2	C30	2		14	7	
U8,11, 19	C00	3		14	7	
U12	C20	1		14	7	1
U24, U18	MM74C02	2		14	7	1
U16, U29	CD4002A	2		14	7	
U22 U3	CD4009A	1		16	8	
U1	CD4023A	1		14	7	1
U25,26,27,28	CD4043A	4		16	8	
U9,10,13,14 15, 3031,32	MM80C97	8		16	8	
U23	MM74C08	1		14	7	
U21	74LS27	1		14	7	

* 3339331

BLANK WORD GENERATOR Group B

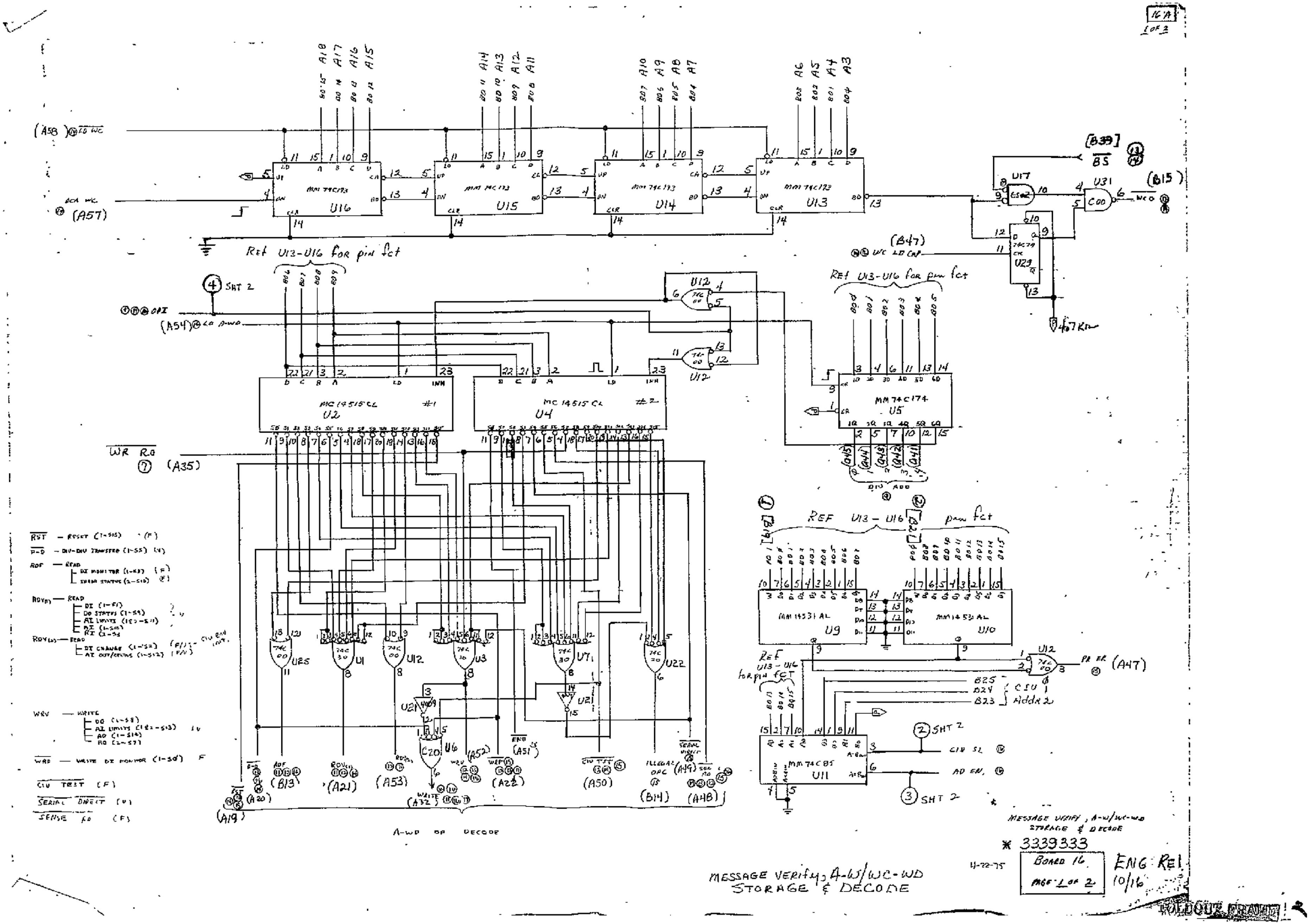
BOARD 15 PAGE 2 OF 3

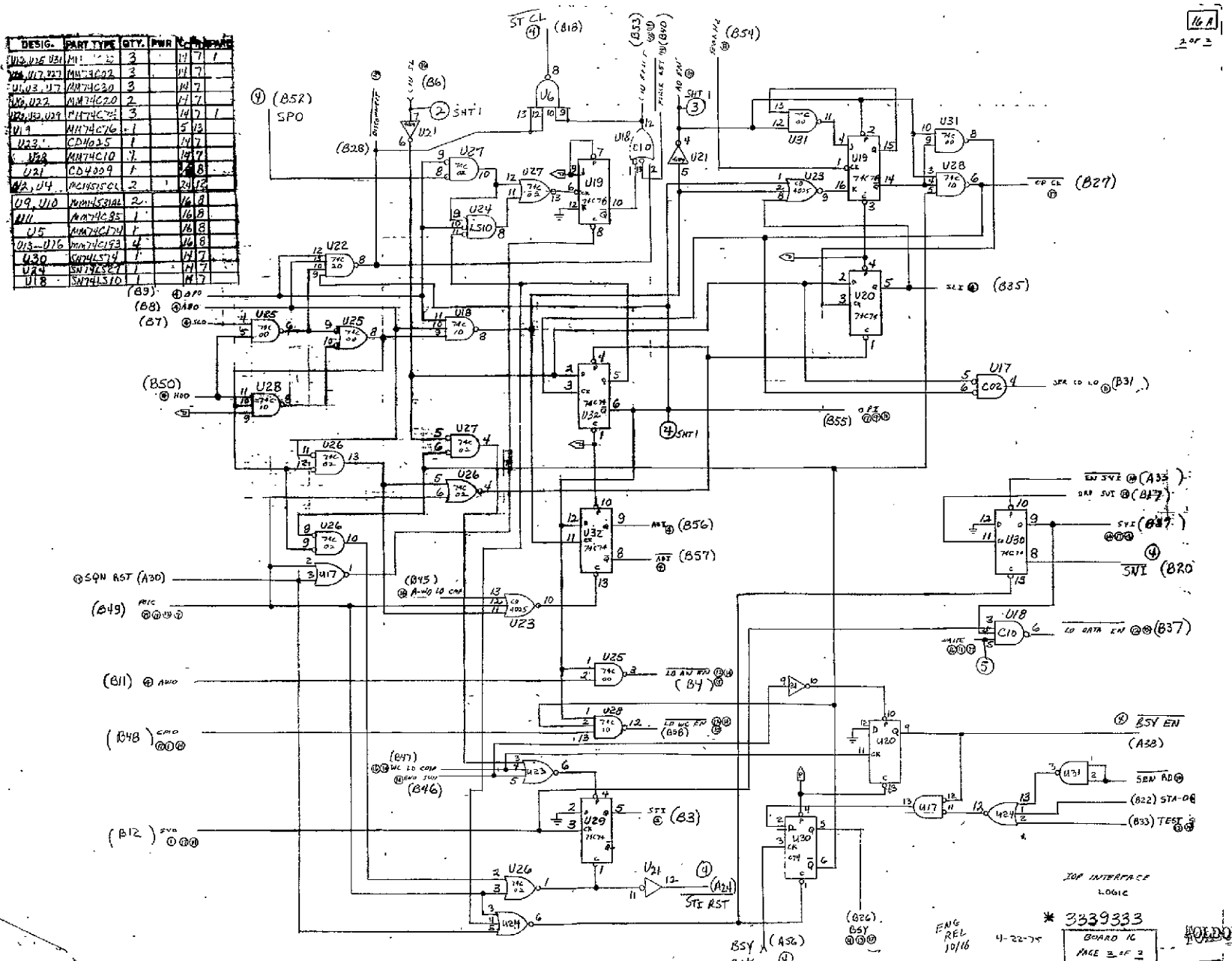
4-22-75 5-14-75

ENG REL 10/16

FOLDOUT FRAME

FOLDOUT FRAME


16A
1 of 2
MM 74C193 U16
MM 74C193 U15
MM 74C193 U14
MM 74C193 U13
Ref U13-U16 for pin fct
MC 14515 CL U2 #1
MC 14515 CL U4 #2
MM 74C174 U5
MM 14531 AL U9
MM 14531 AL U10
MM 74C85 U11
WR RQ
RST — RESET
ROF — READ
ROV — READ
WRV — WRITE
WRP — WRITE DI MONITOR
C/U TEST
SERIAL DIRECT
SENSE RQ
A-WD OP DECODE
PR ER (A47)
C/U SL
AD EN
MESSAGE VERIFY, A-W/WC-WD STORAGE & DECODE
* 3339333
4-22-75
BOARD 16
PAGE 1 OF 2
ENG REL
10/16
FOLDOUT FRAME


16A
2 OF 3
DESIG. | PART TYPE | QTY. | PWR | GND
U12,U26 U31 | MH74C02 | 3 | 14 | 7
U17,U27 | MH74C02 | 3 | 14 | 7
U1,U3,U7 | MH74C20 | 3 | 14 | 7
U6,U22 | MH74C20 | 2 | 14 | 7
U25,U28,U29 | MH74C32 | 3 | 14 | 7
U19 | MH74C76 | 1 | 5 | 13
U23 | CD4025 | 1 | 14 | 7
U18 | MH74C10 | 1 | 14 | 7
U21 | CD4009 | 1 | 16 | 8
U2,U4 | MC14515CL | 2 | 24 | 12
U9,U10 | MM54S381A | 2 | 16 | 8
U11 | MM74C85 | 1 | 16 | 8
U5 | MM74C174 | 1 | 16 | 8
U13–U16 | MM74C193 | 4 | 16 | 8
U30 | SN74LS74 | 1 | 14 | 7
U24 | SN74LS27 | 1 | 14 | 7
U18 | SN74LS10 | 1 | 14 | 7
ST CL (B18)
(B53)
(B54)
(B6)
(B52) SPO
(B28)
(B27)
(B35)
(B31)
(B50)
(B55)
(B56)
(B57)
(B45)
(B49)
(B11)
(B48)
(B47)
(B46)
(B12)
(B3)
(A24)
(A36)
(A33)
(B17)
(B37)
(B20)
(B4)
(A38)
(B22)
(B33)
(B26)
SQN RST (A30)
BSY CLK
STI RST
SVI
SEN RD
TEST
TOP INTERFACE LOGIC
* 3339333
BOARD 1C
PAGE 3 OF 3
ENG REL 10/16
4-22-75
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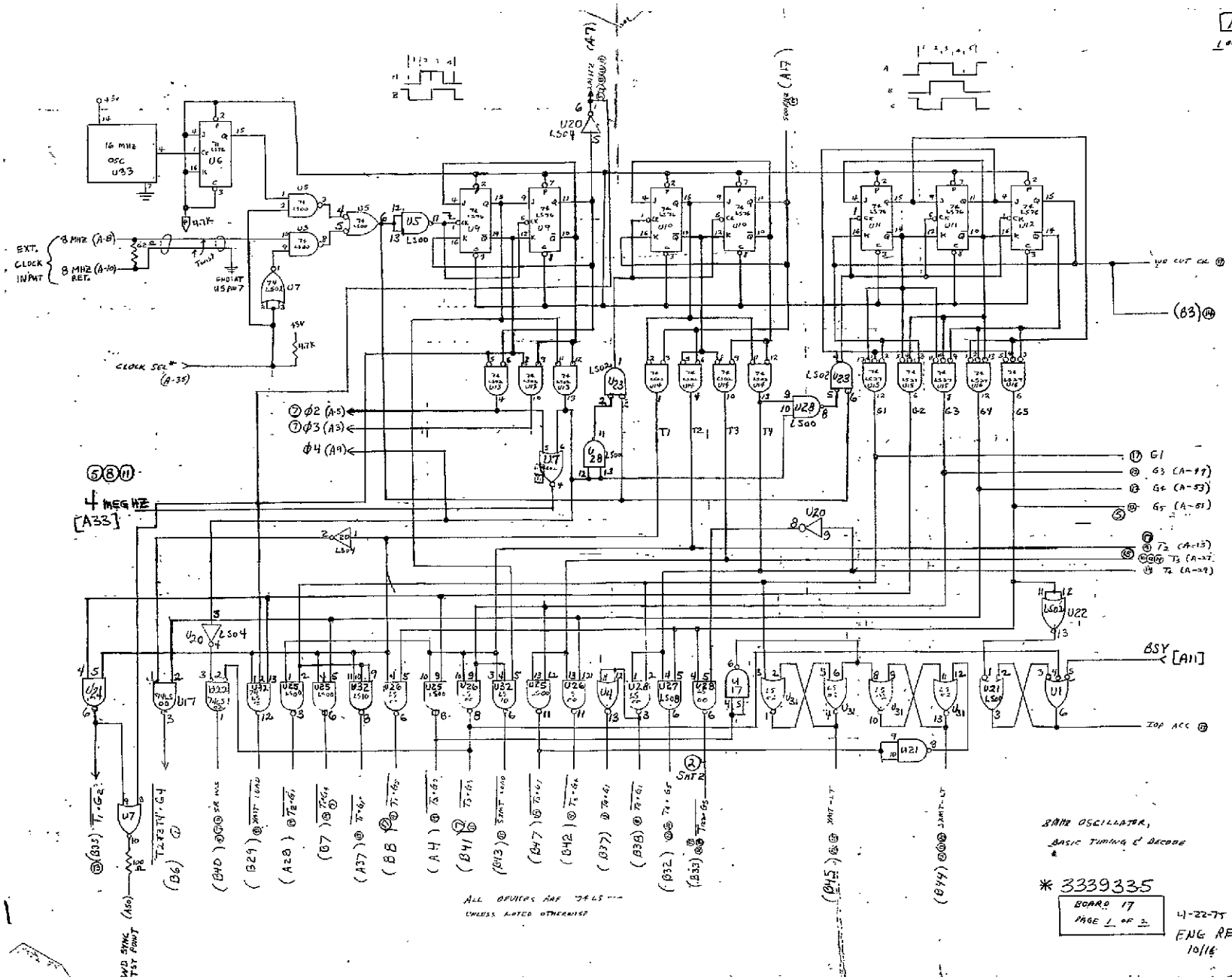
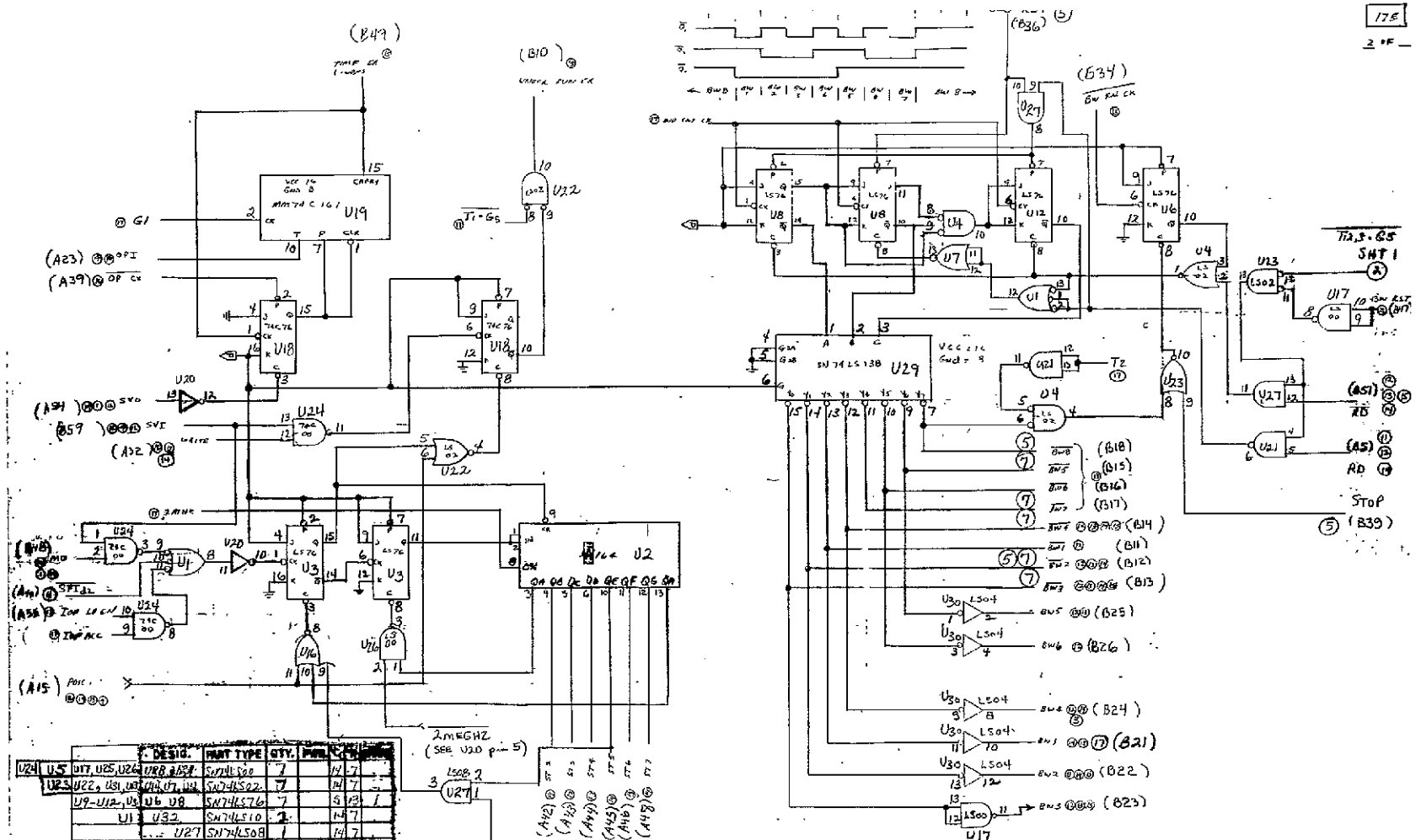
FOLDOUT FRAME


16 MHz OSC U33
EXT. CLOCK INPUT
8 MHz (A-8)
8 MHz RET. (A-10)
CLOCK SEL* (A-35)
4 MEG HZ [A33]
BSY [A11]
IOP ACC
8 MHz OSCILLATOR, BASIC TIMING & DECODE
* 3339335
BOARD 17 PAGE 1 of 3
4-22-77 ENG REL 10/16
ALL DEVICES ARE 74LS UNLESS NOTED OTHERWISE
FOLDOUT FRAME



	DESIG.	PART TYPE	QTY.	PIN		
U24	U5 U17, U25, U26	U18, U19	SN74LS00	7	14	7
U23	U22, U31, U32	U14, U7, U11	SN74LS02	7	14	7
U9-U12, U5	U6 U8		SN74LS76	7	5	13
U1	U32		SN74LS10	2	14	7
	U27		SN74LS08	1	14	7
	U29		SN74LS138	1	16	8
(or) 74164	U2		SN 164	1	14	7
U20	U30		SN74LS04	2	14	7
	U15, U16		SN74LS27	3	14	7
	U18		MM74C76	1	5	13
	U19		MM74C161	1	16	8
	U33		CD2280	1		

ENG REL 10/16

4-22-75

* 3339335

BOARD 17

PAGE 2 OF 2

FOLDOUT FRAME 2

FOLDOUT FRAME 1

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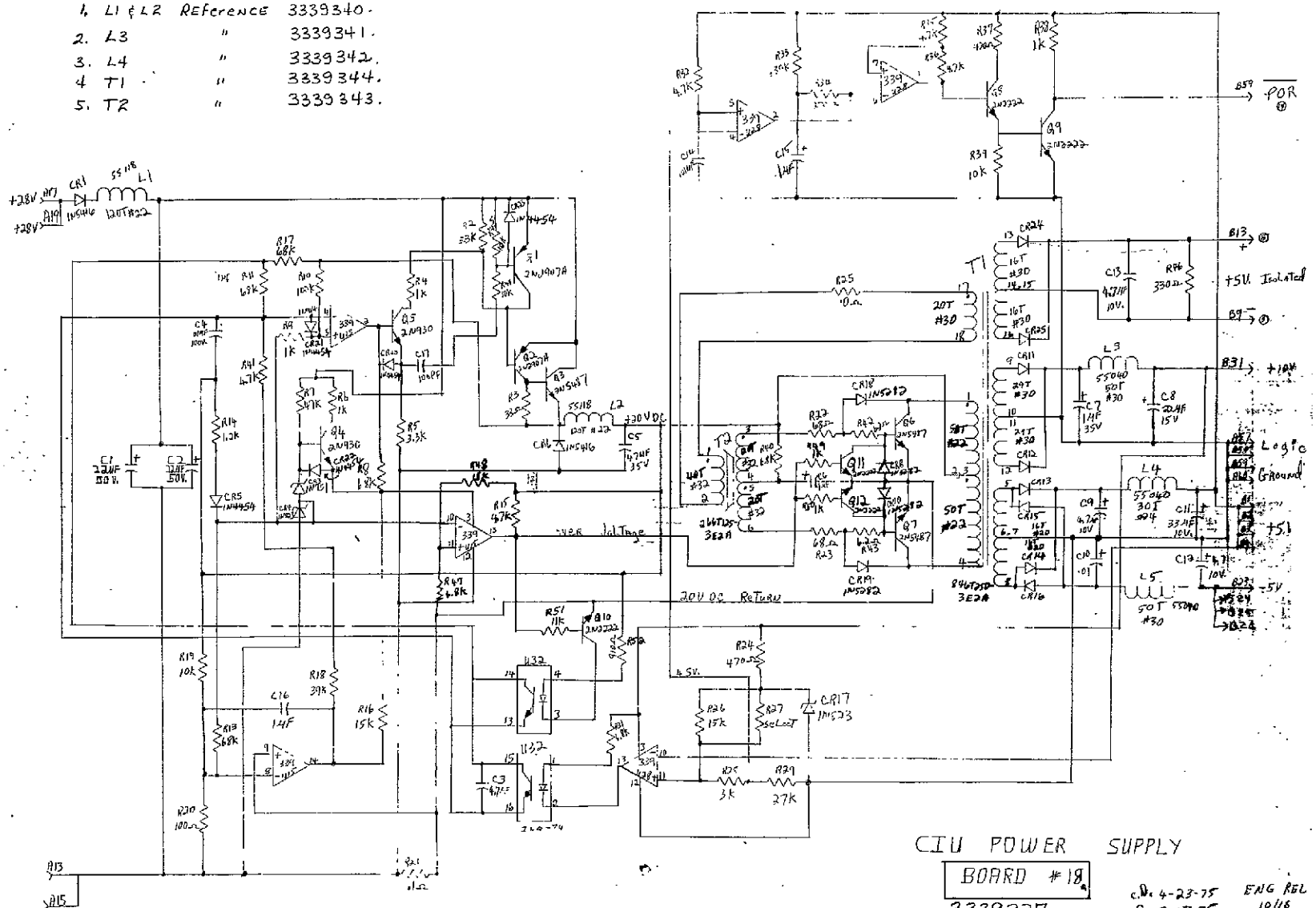
1. L1 & L2 Reference 3339340.
2. L3 " 3339341.
3. L4 " 3339342.
4. T1 " 3339344.
5. T2 " 3339343.



CIU POWER SUPPLY

BOARD #18

3339337

C.N. 4-23-75
C.B 5-13-75

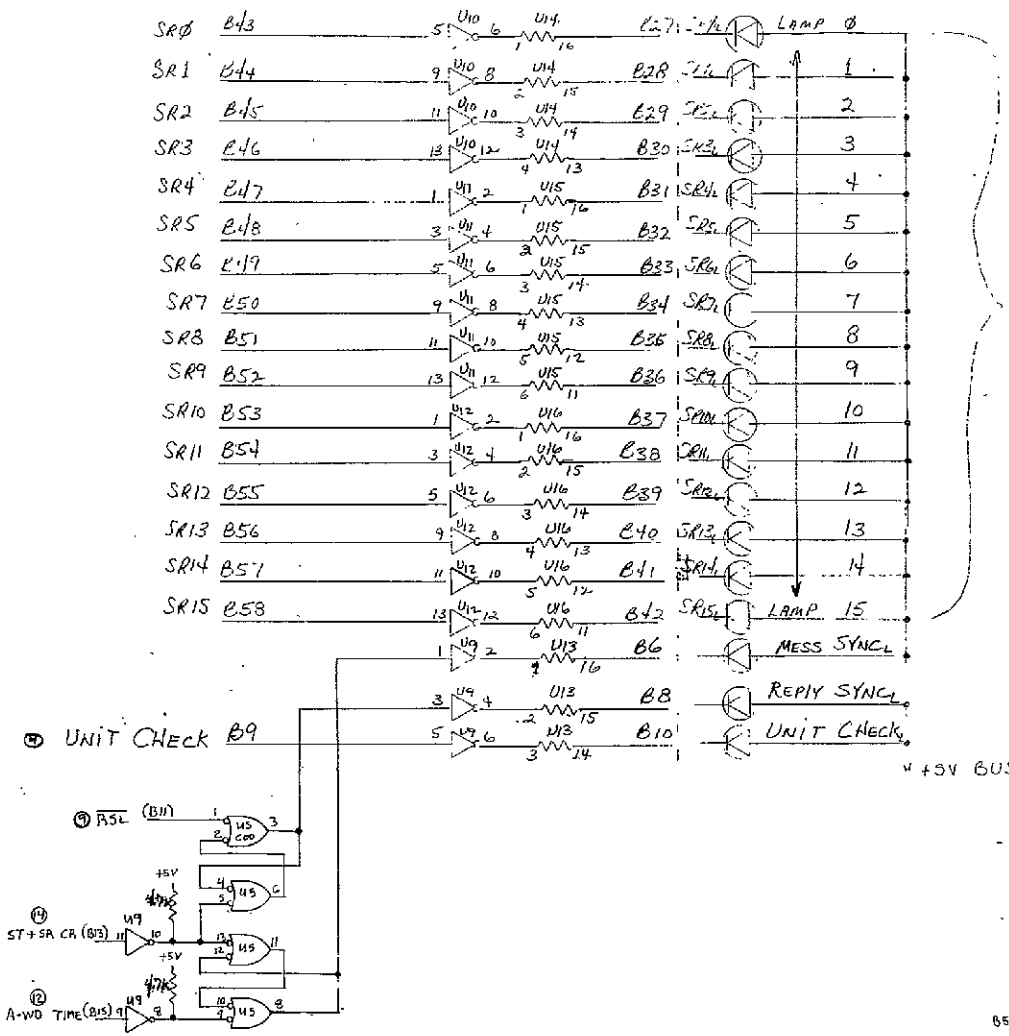
ENG REL 10/16

NOTE: W.O. 3949 { U-28 Change To U26 / U-32 Change To U30 } C.N. 5-30-75

FOLDOUT FRAME 1

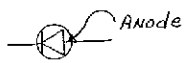
FOLDOUT FRAME 2

C.I.U.
FRONT PANEL



LED DISPLAY FOR REFERENCE ONLY
MV5023 (MONSANTO)

SENSE REGISTER DISPLAY



LAMP DISPLAY FOR REFRENCE ONLY

NOTE: U13 RESISTORS to be 430Ω, ¼WATT.

1. U9 thru U12 SN74LS05 4 each
2. U5 MM74C00 1 each
3. PC802B 1 each
4. 4.7KΩ RCR07G472J 5 each

B1, B2 → +5V
15mF 10V .01 uF
B59, B60 → GND

C.I.U.
BOARD 19
SHT 1 OF 1
LAMP DRIVERS
3339339
ENG REL
10/16

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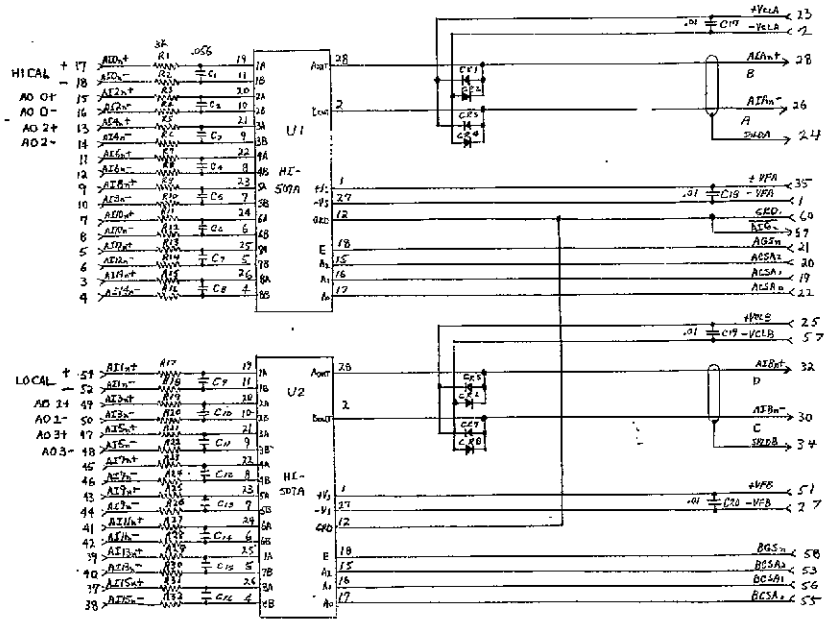


	TYPE	QTY	$+I_S$ (mA)	$-I_S$ (mA)	$+V_F$	$-V_F$	TOTAL
BIAS	HI-507A	2	1 mA	.04 mA	15mW	.6 mW	15.6 mW
LOGIC	HI-507A	16	2 mA	-32 mA	120 mW	4.8 mW	124.8 mW
	MUX	64					
	2N6	160					
	R10J	256					

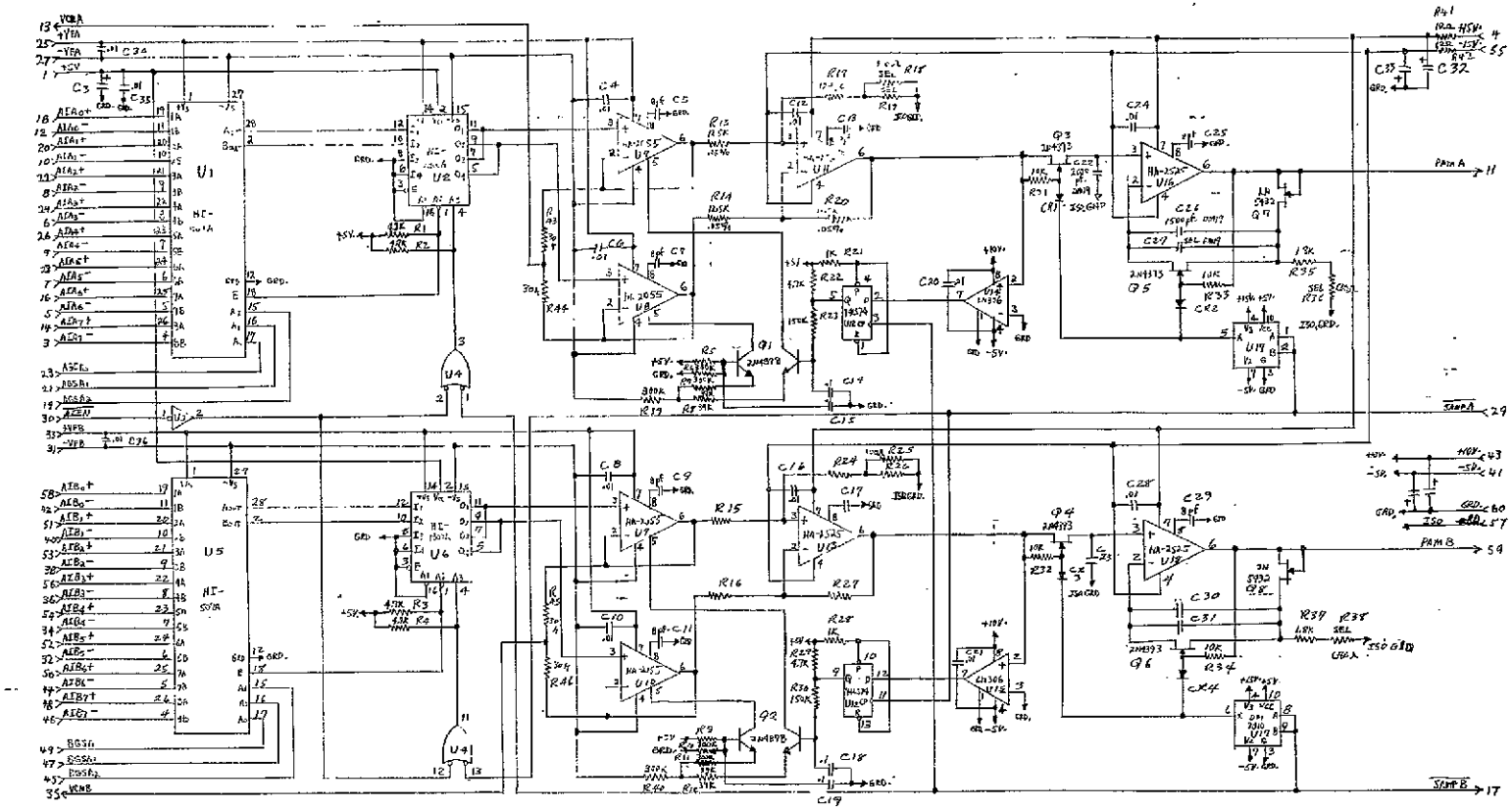
$-V_{FA}$	$-V_{FA}$	$+V_{FB}$	$-V_{FB}$
60 mW	3 mW	60 mW	3 mW

AI MUX MODULE

P.B. 3339002

51-54

57-510



TYPE	QTY	+5V.	+15V	-15V.	+VFA	-VFA	+VFB	-VFB	+10V.	-5V.
HI-507A	2	—	—	—	15 ma.	15 ma.	1 ma.	15ma.		
HI-508A	2	20ma.	—	—	15 ma.	30 ma.	15ma.	30ma.		
HA-2055	4	—	—	—	18 ma.	18 ma.	15 ma.	18 ma.		
HA-2525	4	—	24ma.	24ma.	—	—			110ma.	15 ma.
LM 306	2									5ma.
LM 1340	1	5 ma.								
74LS00	1	8 ma.								
74LS74	1	12 ma.								
RLO7	34									
CKO6	15									
CS13	3									
CIOA	8									
5102	8									

AFTER MUX

95ma. 240ma. 240ma. 210ma. 245ma. 210ma. 245ma. 110ma. 25ma.

GP, SEL, MUX, SAMPLD/HOLD

55

P.B. 3339011

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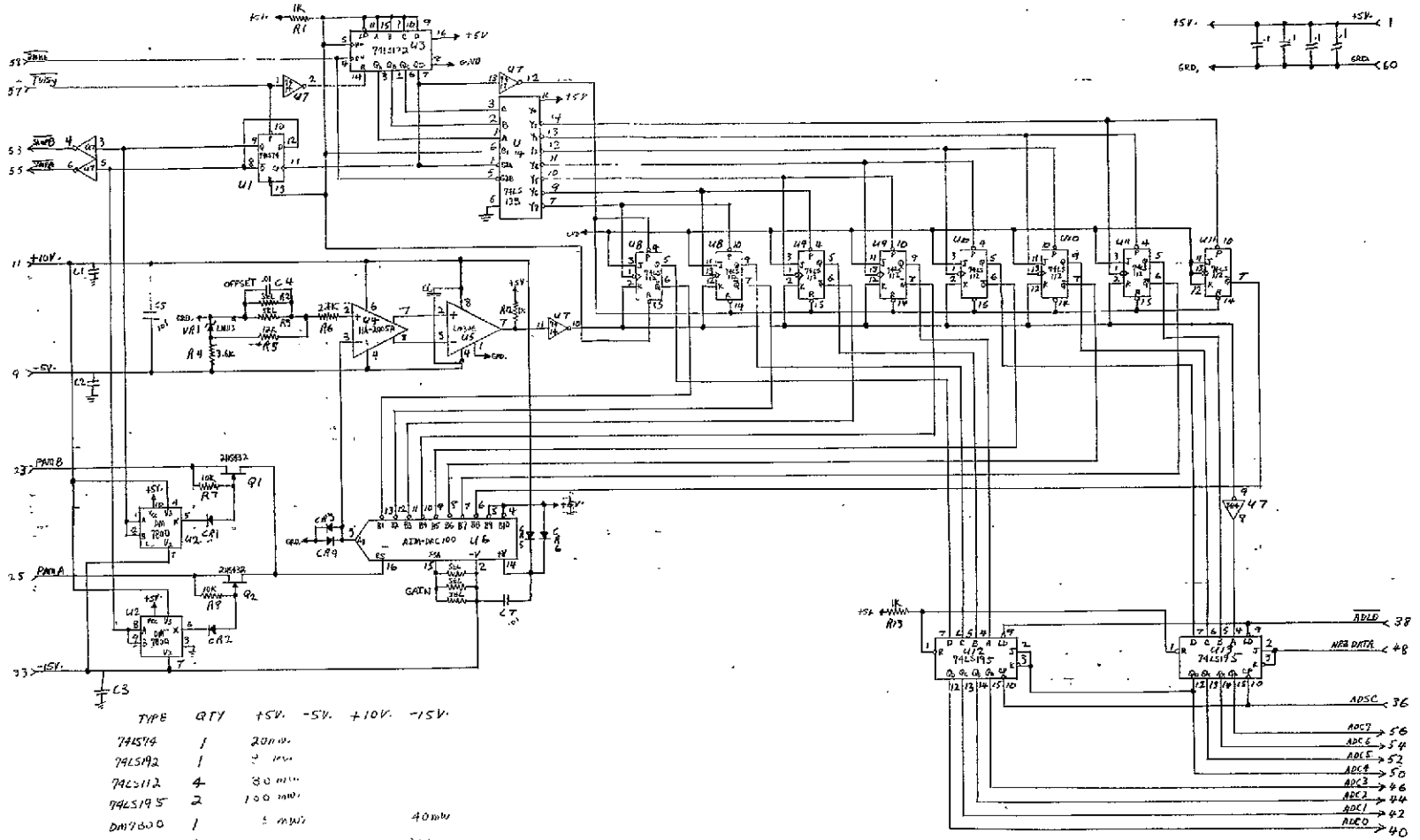
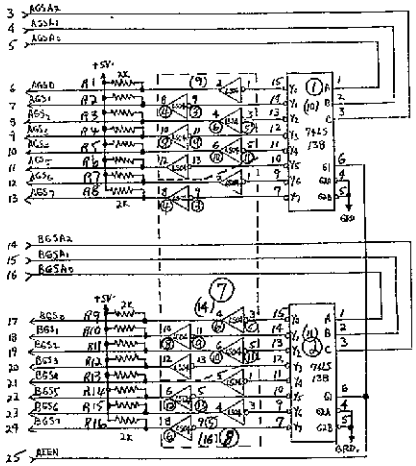
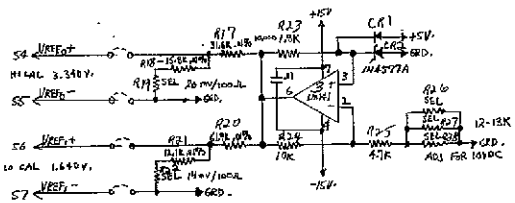
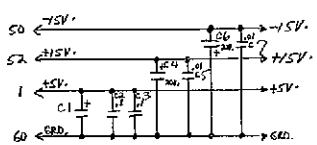


TYPE	QTY	+5V.	-5V.	+10V.	-15V.
74S74	1	20mw.			
74LS192	1	2 mw.			
74LS112	4	80 mw.			
74LS195	2	100 mw.			
DM7800	1	5 mw.			40mw
AEM-DAC 100	1			130mw.	130mw.
HA-2005A	1		15mw.		15mw.
LM1306	1		8mw.		55mw.
7914	1	150 mw.			
74LS138	1	31 mw.			
LM113	1		5mw.		
IN4454	4				
RL07	12				
CR06	6				
		471mw.	20mw.	270mw	190mw.

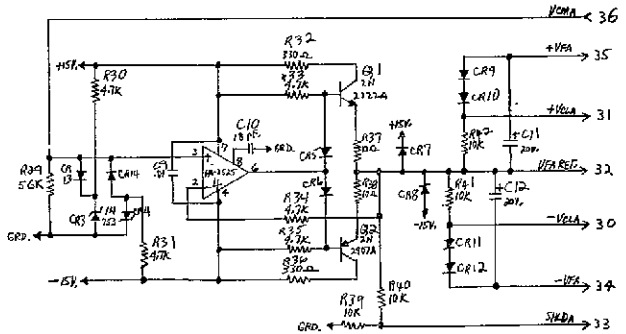


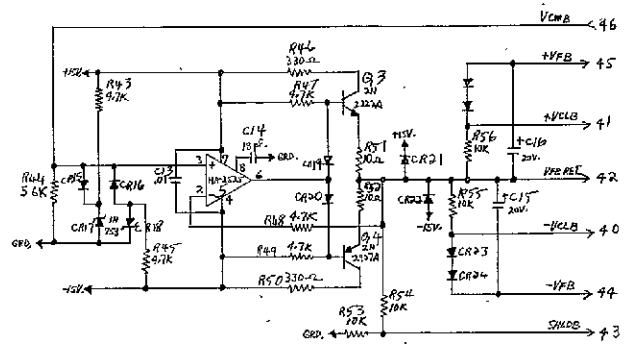




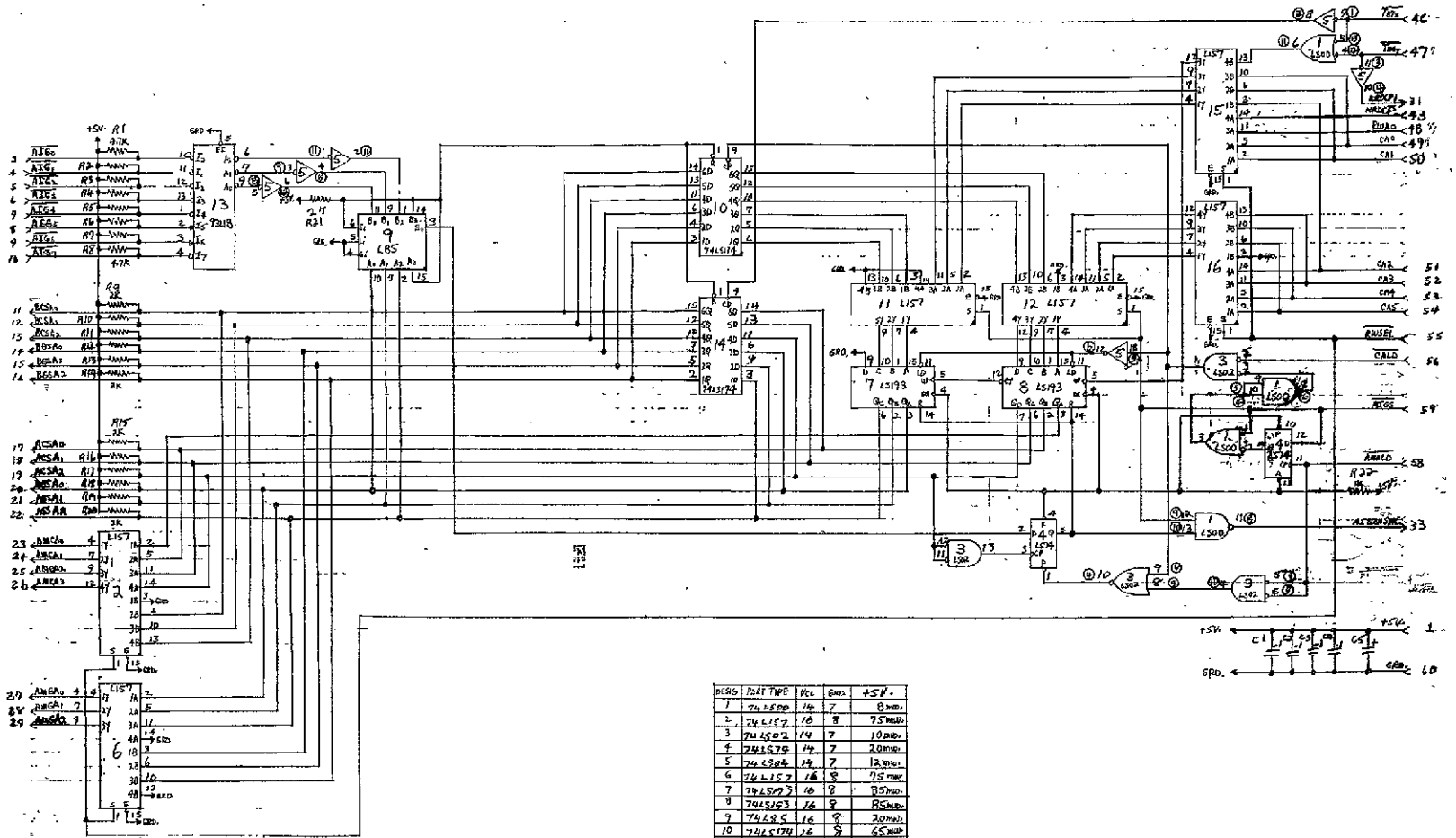
DIODES: 1N4454

3 THEN MUX



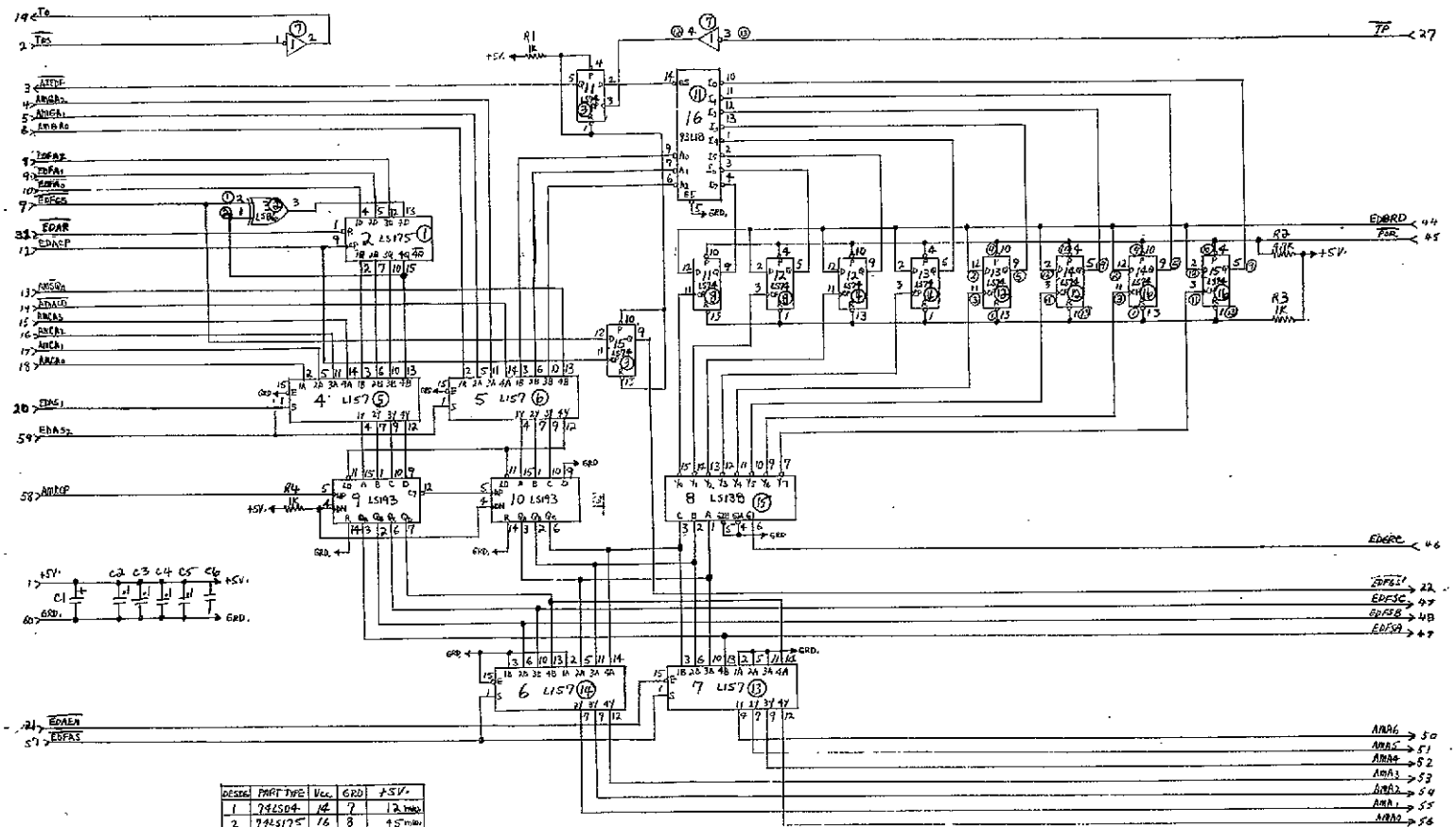


GUARD AMP. & GROUP SELECT
SIL.
P.B. 3339068



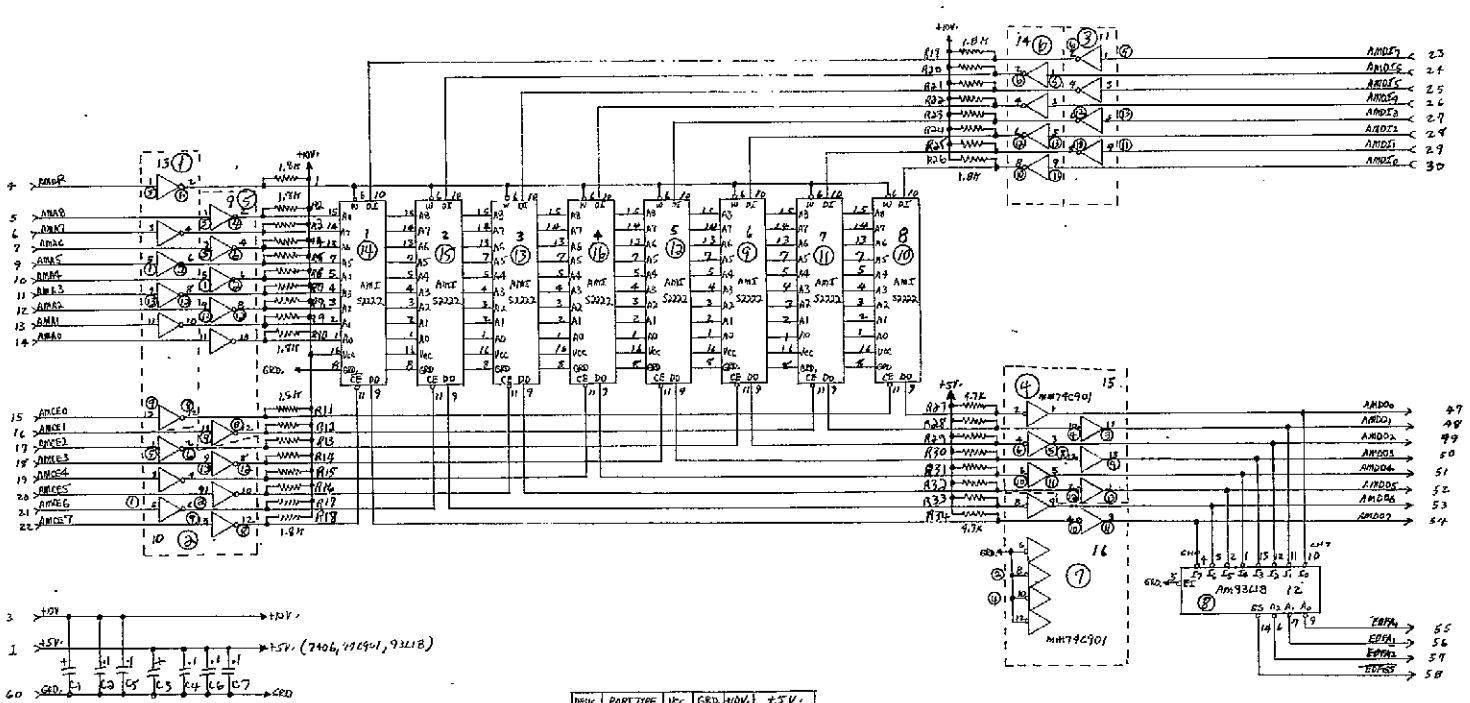
DESIG	PART TYPE	Vcc	GND	+5V
1	74LS00	14	7	8 mA
2	74LS157	16	8	75 mA
3	74LS02	14	7	10 mA
4	74LS78	14	7	20 mA
5	74LS86	14	7	13 mA
6	74LS157	16	8	75 mA
7	74LS193	16	8	85 mA
8	74LS193	16	8	85 mA
9	74LS85	16	8	30 mA
10	74LS174	16	8	65 mA
11	74LS157	16	8	75 mA
12	74LS157	16	8	75 mA
13	AM9348	16	8	75 mA
14	74LS174	16	8	65 mA
15	74LS157	16	8	75 mA
16	74LS157	16	8	75 mA
BOARD TOTAL				870 mA

A.E. MUX ADDRESS CONTROL
A 512
P.B. 3339054



DESIG	PART TYPE	VCC	GRD	+5V.
1	74LS04	14	7	12 mA.
2	74LS175	16	8	45 mA.
3	74LS86	14	7	30 mA.
4	74LS157	16	8	75 mA.
5	74LS157	16	8	75 mA.
6	74LS157	16	8	75 mA.
7	74LS157	16	8	75 mA.
8	74LS138	16	8	31 mA.
9	74LS193	16	8	85 mA.
10	74LS193	16	8	85 mA.
11	74LS74	14	7	20 mA.
12	74LS74	14	7	20 mA.
13	74LS74	14	7	20 mA.
14	74LS74	14	7	20 mA.
15	74LS74	14	7	20 mA.
16	AM93L18	16	8	75 mA.
BOARD TOTAL				763 mA.

AI MEM. ADDRESS CONTROL
SIX
P.B. 3339056



REF.	PART TYPE	VCC	GRD.	HDV.	+5V.
1	52222		8	16	1 MW.
2	52222		8	16	1 MW.
3	52222		8	16	1 MW.
4	52222		8	16	1 MW.
5	52222		8	16	1 MW.
6	52222		8	16	1 MW.
7	52222		8	16	1 MW.
8	52222		8	16	1 MW.
9	7406	14	7		156 MW.
10	7406	14	7		156 MW.
11	7406	14	7		156 MW.
12	AM93418	16	8		75 MW.
13	7406	14	7		156 MW.
14	7406	14	7		156 MW.
15	AM79C901	14	7		2 MW.
16	AM79C901	14	7		2 MW.
BOARD TOTAL					867 MW.

REF.	
AM48911 AM471	EAF
10	LAE
01	MA
00	PA

AI MEMORY
5/4
P.B. 3339052

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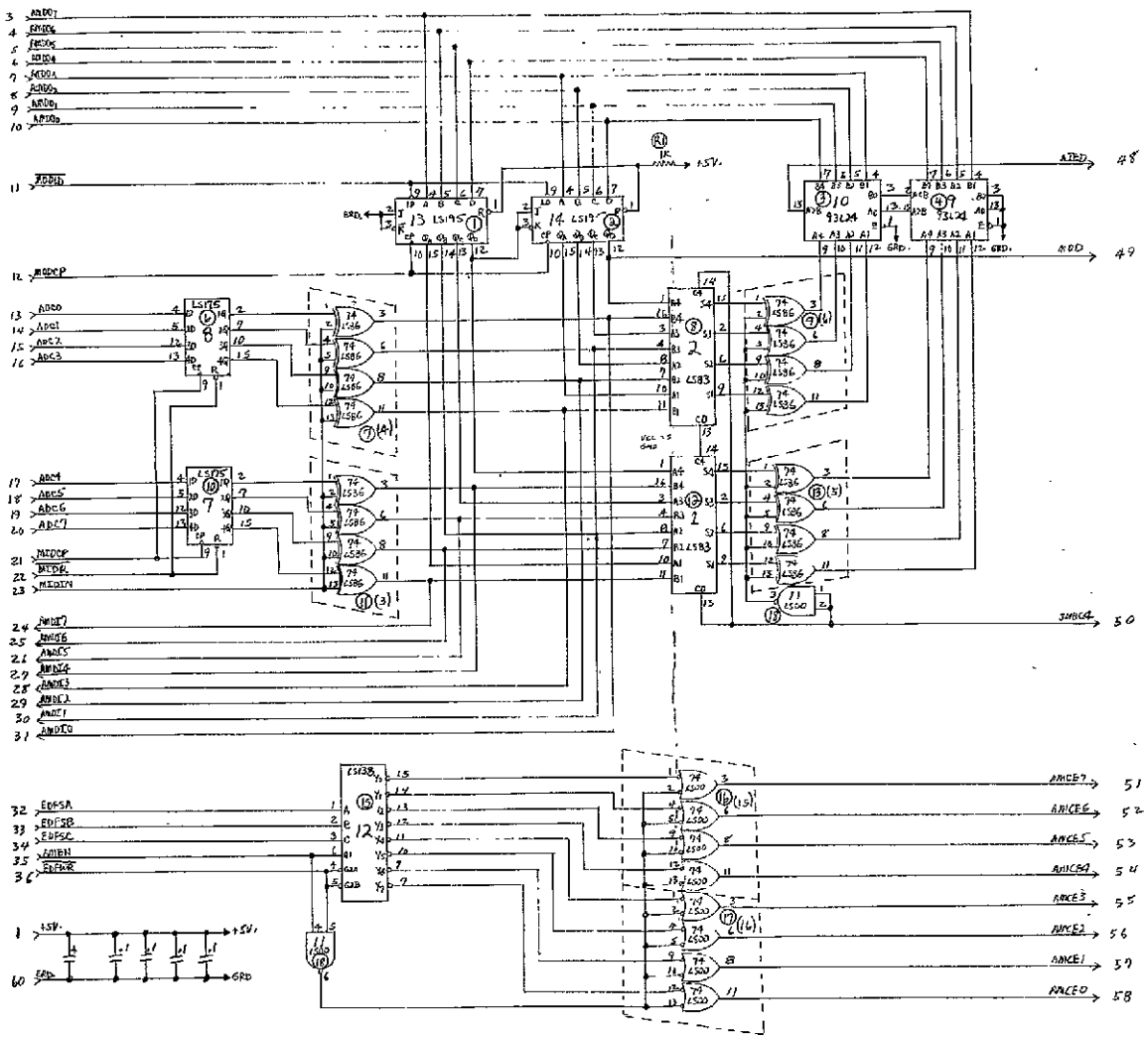
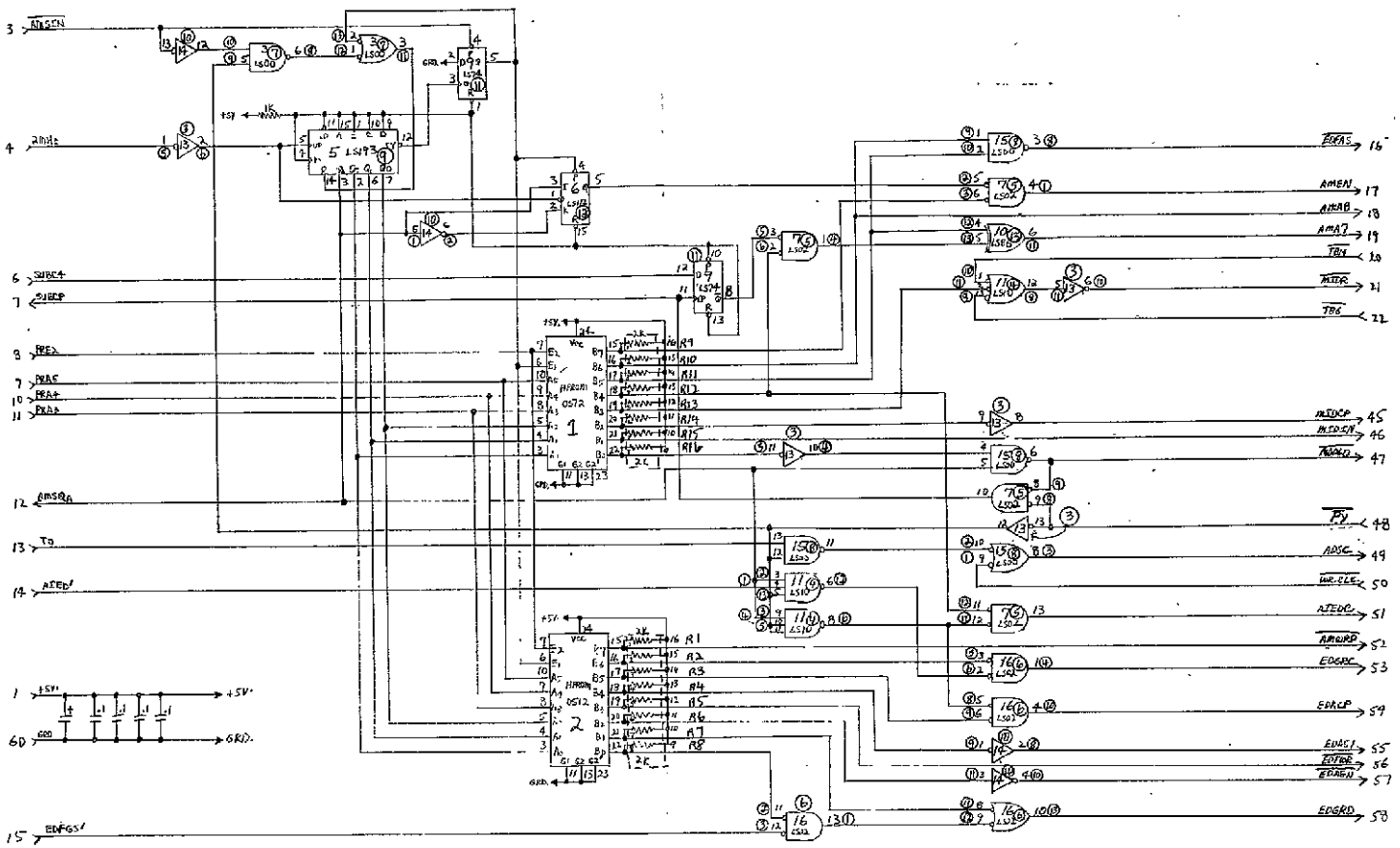


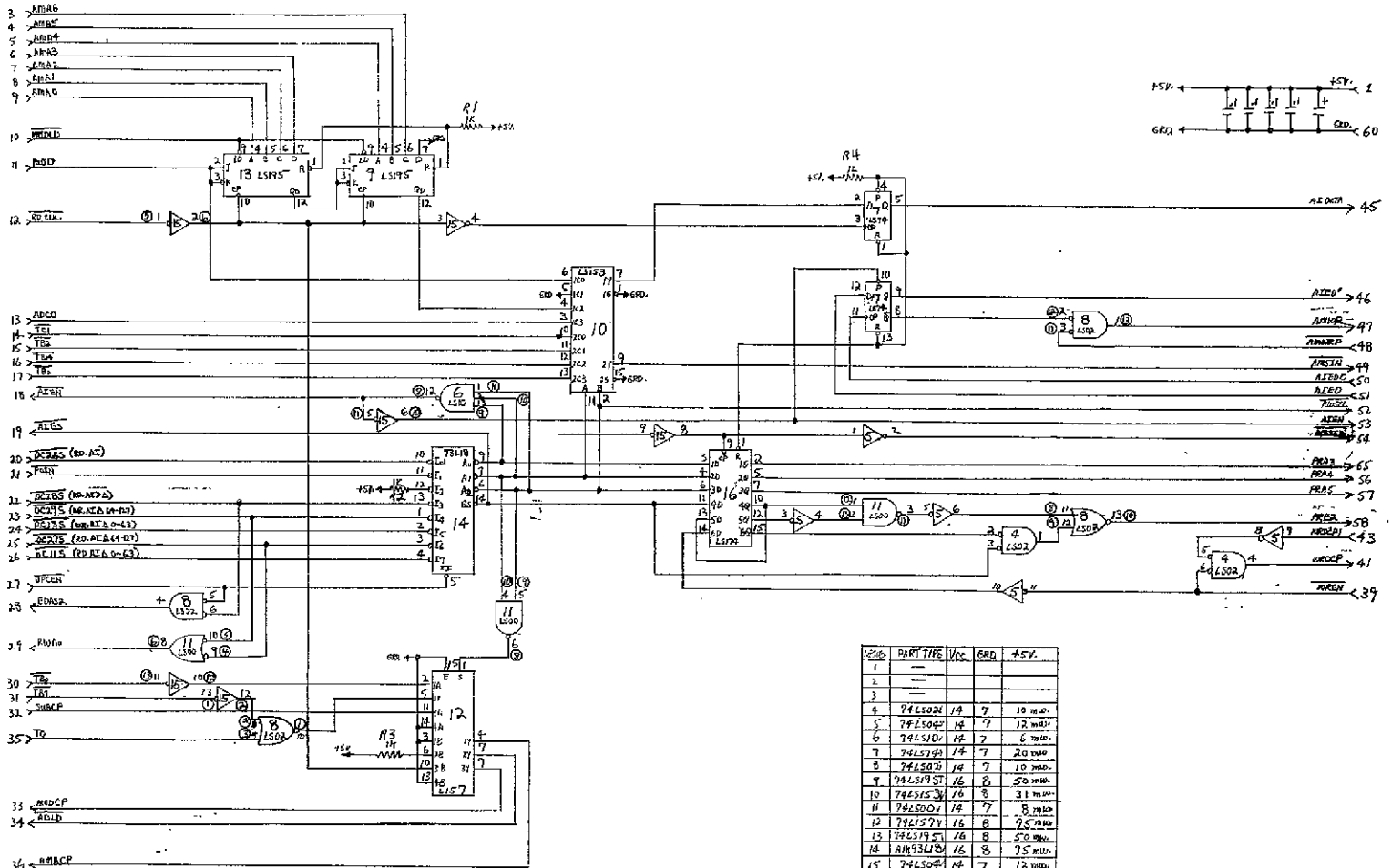
DESIG.	PART TYPE	V_{cc}	GRD.	+5V.
1	74LS83	5	12	19 max.
2	74LS83	5	12	19 max.
3	74LS86	14	7	30 max.
4	74LS86	14	7	30 max.
5	74LS86	14	7	30 max.
6	74LS86	14	7	30 max.
7	74LS175	16	8	45 max.
8	74LS175	16	8	45 max.
9	Am93L24	16	8	52 max.
10	Am93L24	16	8	52 max.
11	74LS00	14	7	8 max.
12	74LS138	16	8	31 max.
13	74LS195	16	8	50 max.
14	74LS195	16	8	50 max.
15	74LS00	14	7	8 max.
16	74LS00	14	7	8 max.
BOARD TOTAL				507 max.

AI MEM. DATA INTERFACE
515
P.B. 3339058



DESIG	PART TYPE	Vcc	GND	+5V.
1	HFE10-0512	24	11/12/23	400 mW.
2	HFE10-0512	24	11/12/23	400 mW.
3	74LS00			8 mW.
4	—			
5	74LS193	16	8	85 mW.
6	74LS112	16	8	20 mW.
7	74LS02	14	7	10 mW.
8	—			
9	74LS74	14	7	30 mW.
10	74LS86	14	7	30 mW.
11	74LS10	14	7	6 mW.
12	—			
13	74LS04	14	7	12 mW.
14	74LS04	14	7	12 mW.
15	74LS00	14	7	8 mW.
16	74LS02	14	7	10 mW.
BOARD TOTAL				1021 mW.

A.E. MEM. SEQUENCE CONTROL
SIG
P.B. 3339 D62



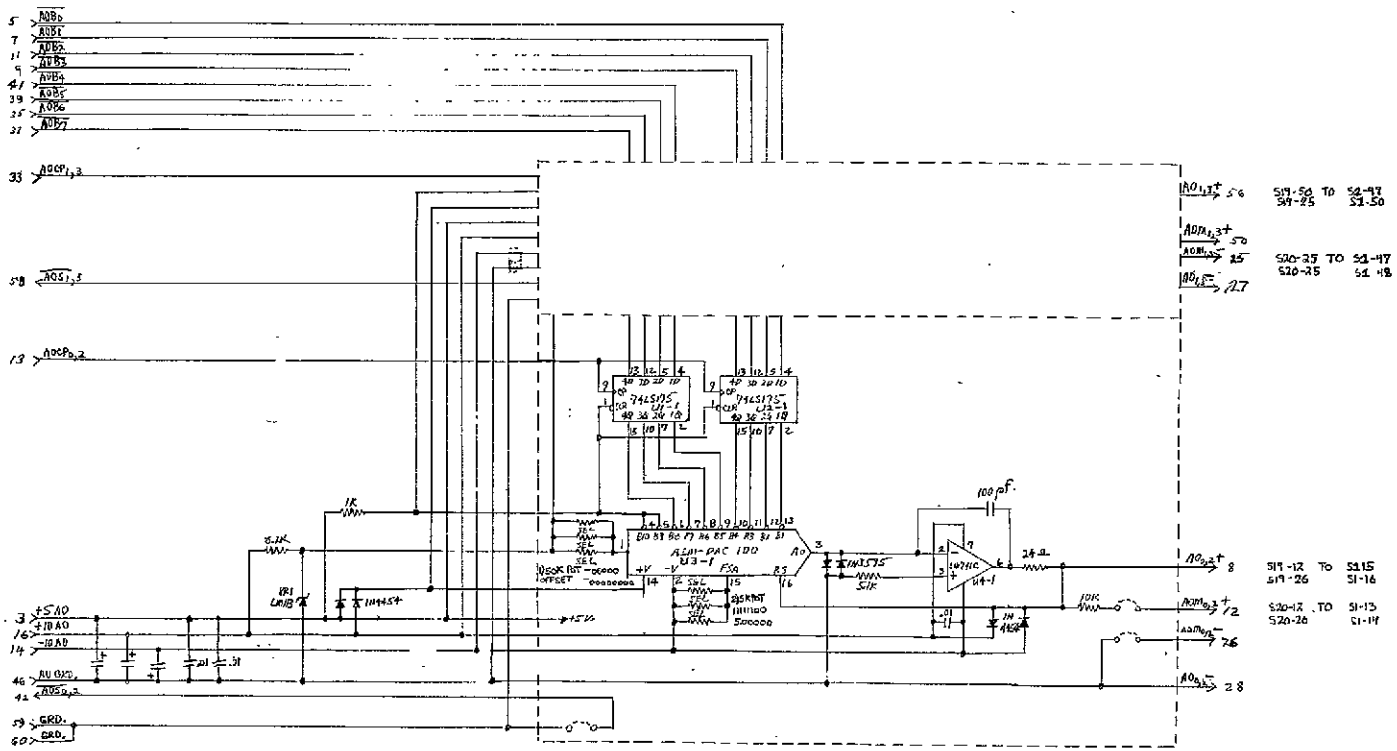
ITEM	PART TYPE	Vcc	GRD	+5V.
1	—			
2	—			
3	—			
4	74LS02N	14	7	10 MW.
5	74LS04P	14	7	12 MW.
6	74LS10J	14	7	6 MW.
7	74LS74A	14	7	20 MW.
8	74LS08J	14	7	10 MW.
9	74LS19ST	16	8	50 MW.
10	74LS153J	16	8	31 MW.
11	74LS00N	14	7	8 MW.
12	74LS157Y	16	8	75 MW.
13	74LS195J	16	8	50 MW.
14	AM93L18	16	8	75 MW.
15	74LS04N	14	7	12 MW.
16	74LS174	16	8	65 MW.
BOARD TOTAL				424 MW.

FOLDOUT FRAME 1

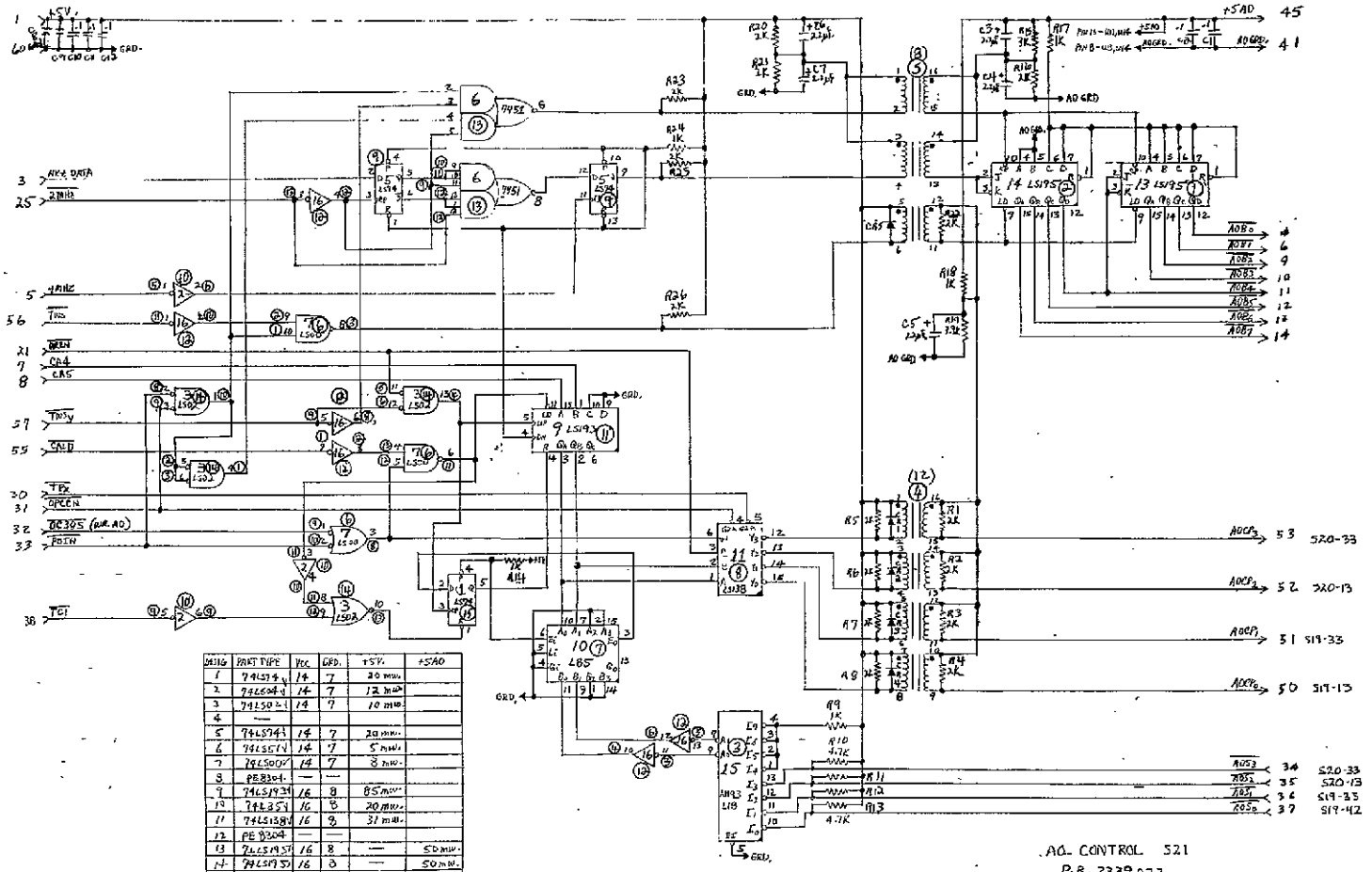
FOLDOUT FRAME 2

AI MEM FUNCTION SEL.
S17
P.B. 3339060

DESIG	PART TYPE	Vcc	GRD	+5AD	+10AD	-10AD
U1-1	74LS175	16	8	45 mw	—	—
U1-2	"	16	8	45 mw	—	—
U2-1	"	16	8	45 mw	—	—
U2-2	74LS175	16	8	45 mw	—	—
U3-1	ADH-PAC 100	—	—	—	70 mw	70 mw
U3-2	ADH-PAC 100	—	—	—	70 mw	70 mw
U4-1	LM318C	—	—	—	17 mw	17 mw
U4-2	LM318C	—	—	—	17 mw	17 mw
VR1	LM113	—	—	—	10 mw	—
BOARD TOTAL				180 mw	186 mw	174 mw
SYSTEM TOTAL				360 mw	368 mw	348 mw

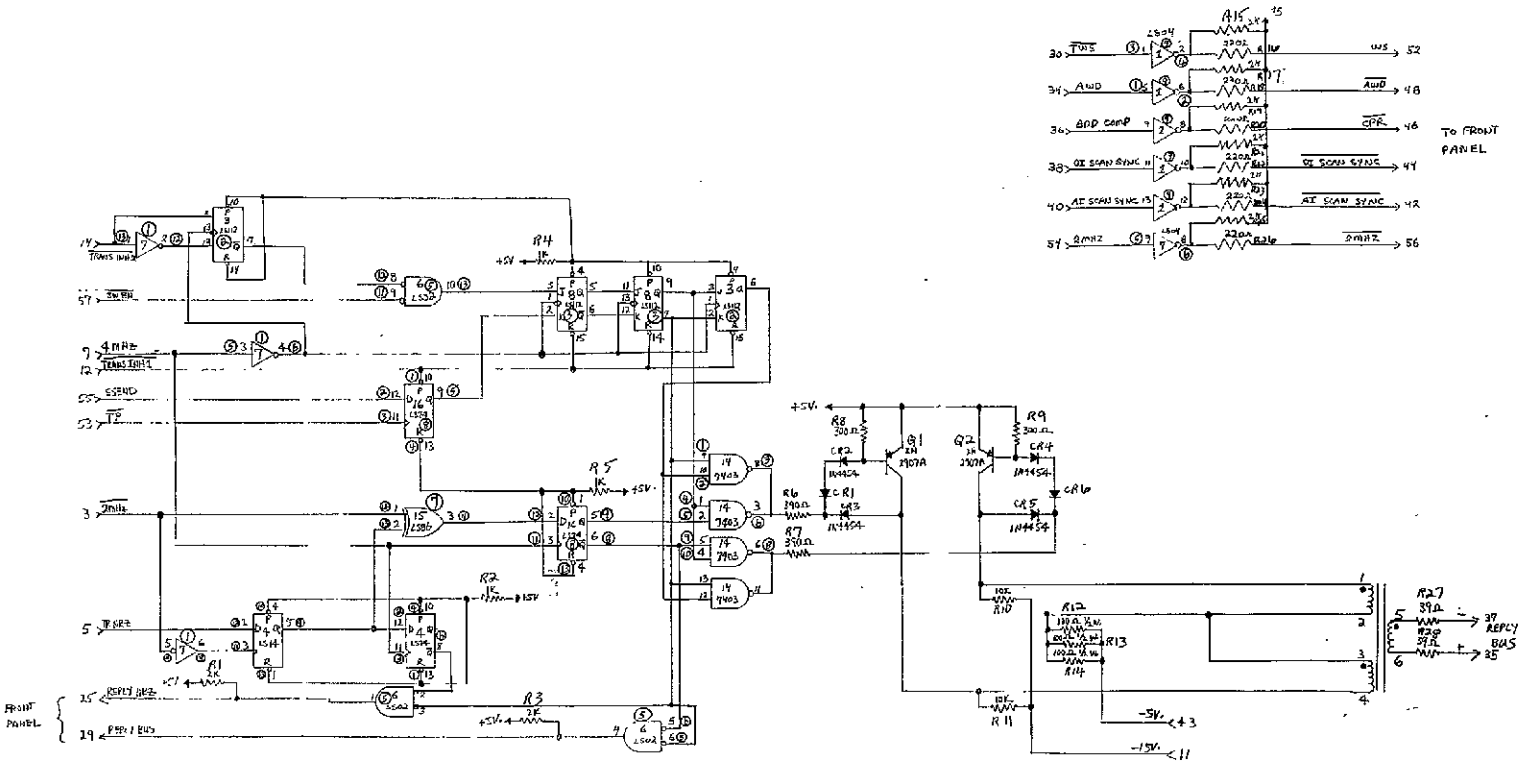


ANALOG OUTPUT MODULE
519, 520
AB. 3339020



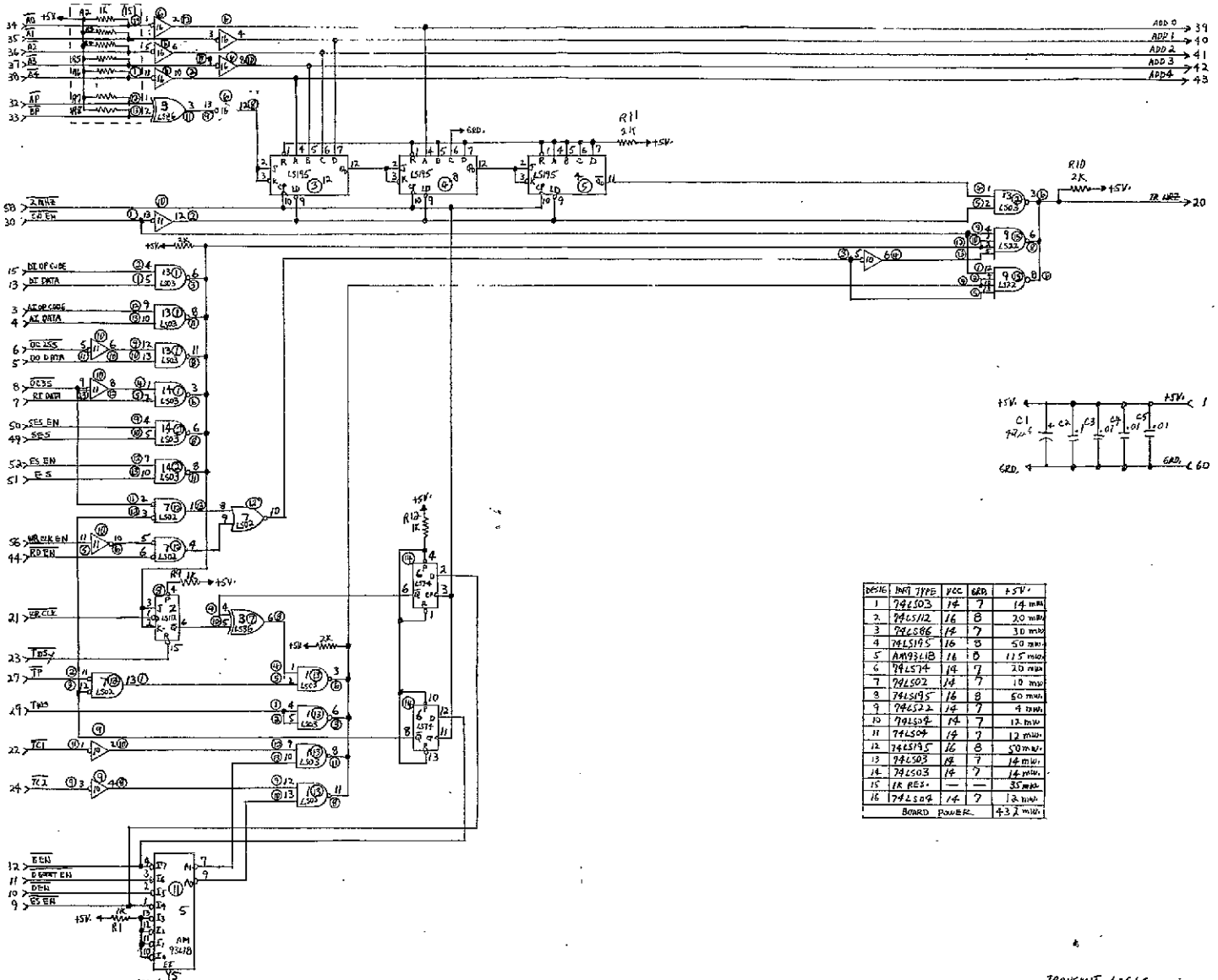
DESIG	PART TYPE	Vcc	GRD.	+5V.	+5AD
1	74LS14	14	7	30 mw.	
2	74LS04	14	7	12 mw.	
3	74LS02	14	7	10 mw.	
4	—				
5	74LS04	14	7	30 mw.	
6	74LS51	14	7	5 mw.	
7	74LS00	14	7	8 mw.	
8	PE8304	—	—		
9	74LS194	16	8	85 mw.	
10	74LS51	16	8	20 mw.	
11	74LS138	16	8	31 mw.	
12	PE 8304	—	—		
13	74LS195	16	8	—	50 mw.
14	74LS93	16	8	—	50 mw.
15	AM9218	16	8	95 mw.	
16	74LS04	14	7	13 mw.	
BOARD, SYSTEM TOTAL				498 mw.	100 mw.

AD CONTROL 521
P.B. 3339072



DESIG	PART TYPE	DOC	GRD	+5V
1	[illegible]	[illegible]	7	
2	—	—	—	—
3	—	—	—	—
4	74LS74	14	7	20 mA
5				
6	74LS02	14	7	10 mA
7	74LS36	14	7	12 mA
8	74LS32	16	8	20 mA
9				
10				
11				
12				
13				
14	7403	14	7	40 mA
15	74LS86	14	7	30 mA
16	74LS74	14	7	20 mA
	LOGIC POWER			15.2 mA

DIU TRANSMITTER
526
P.B. 3339026

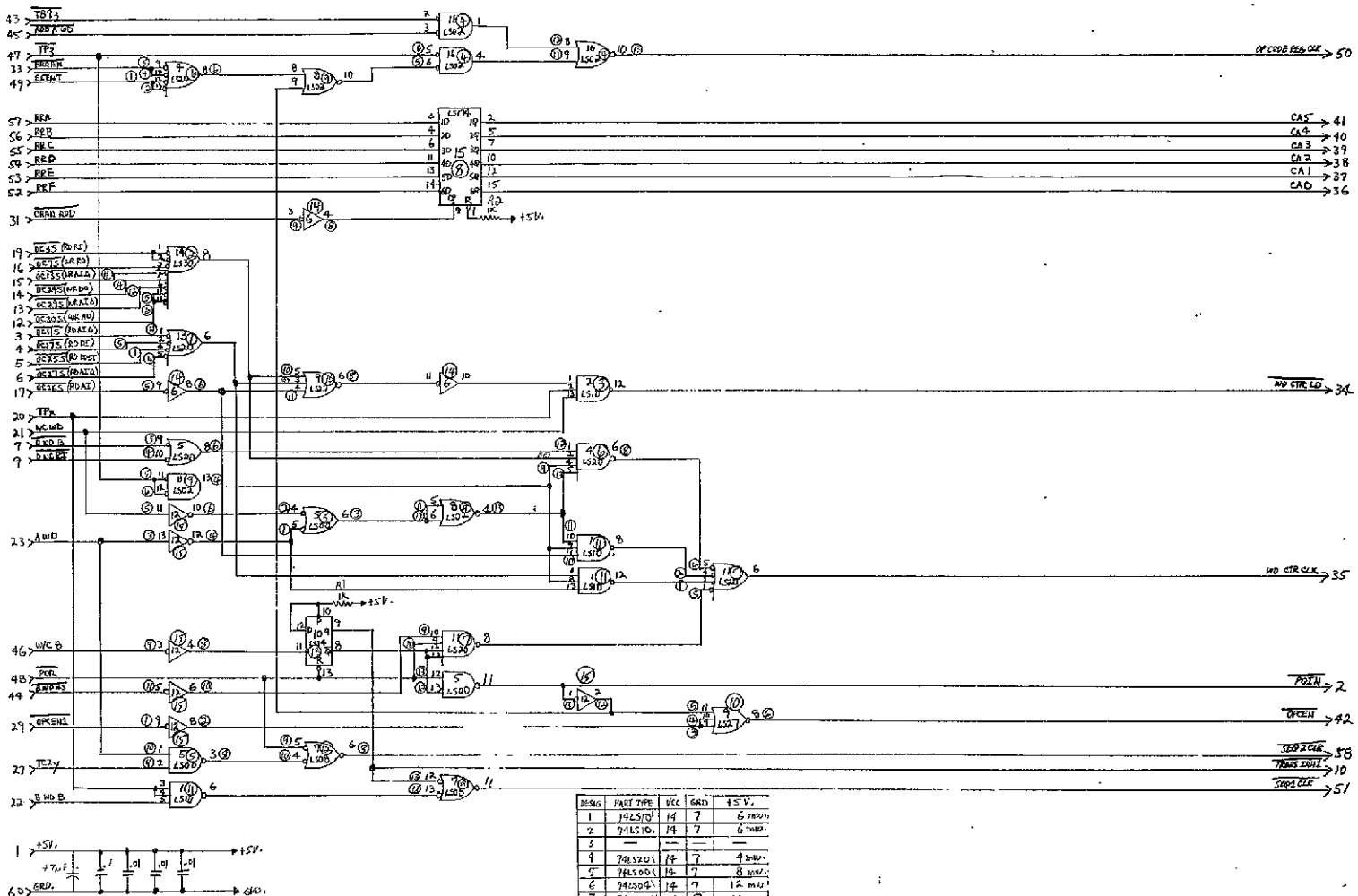


DESIG	INT. TYPE	VCC	GRD.	+5V.
1	74LS03	14	7	14 mA
2	74LS112	16	8	20 mA
3	74LS86	14	7	30 mA
4	74LS195	16	8	50 mA
5	AM9341B	16	8	115 mA
6	74LS74	14	7	20 mA
7	74LS02	14	7	10 mA
8	74LS195	16	8	50 mA
9	74LS22	14	7	4 mA
10	74LS04	14	7	12 mA
11	74LS04	14	7	12 mA
12	74LS195	16	8	50 mA
13	74LS03	14	7	14 mA
14	74LS03	14	7	14 mA
15	IR REC.	—	—	35 mA
16	74LS04	14	7	12 mA
BOARD POWER				432 mA

TRANSMIT LOGIC

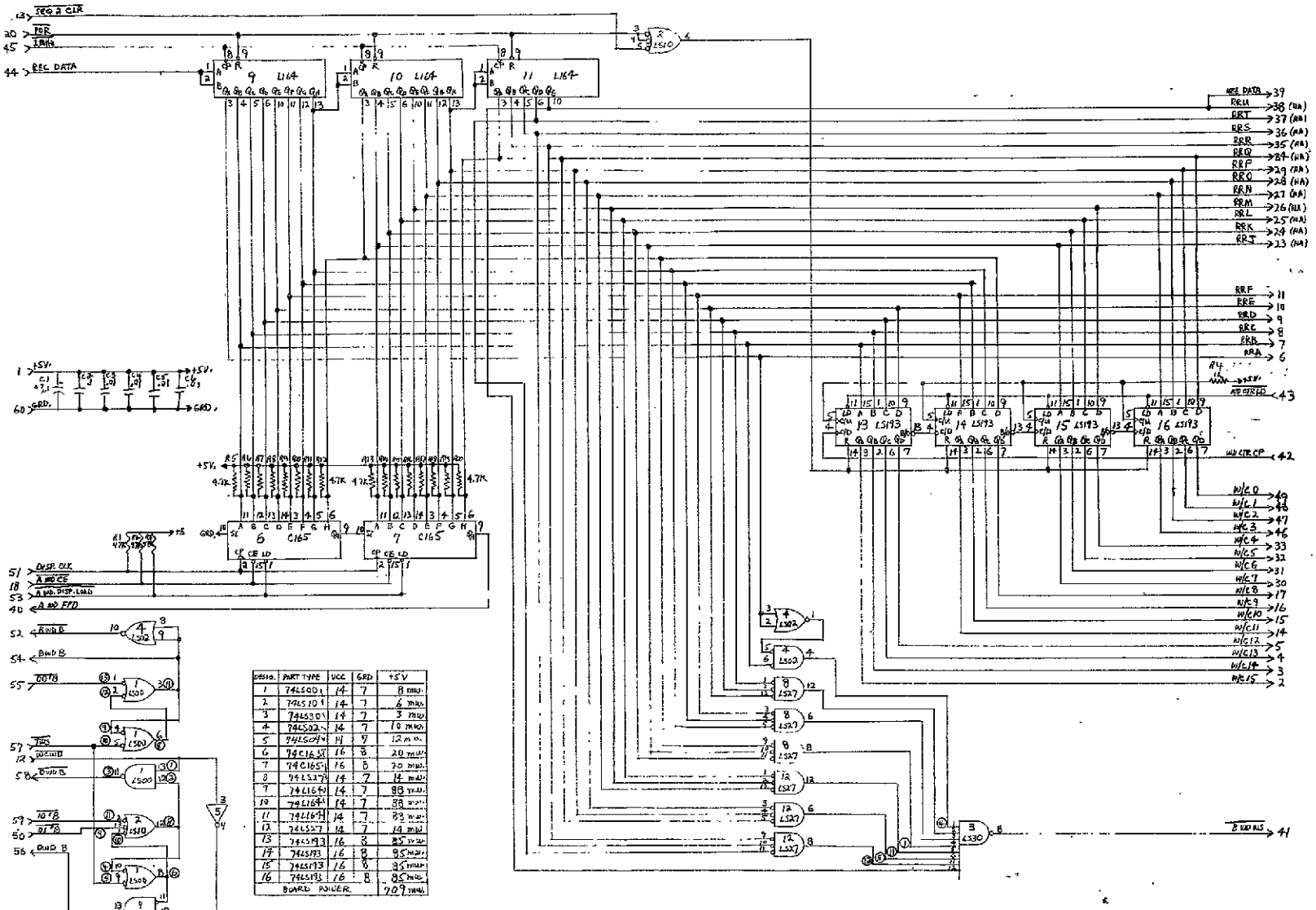
527

P.B. 3339030



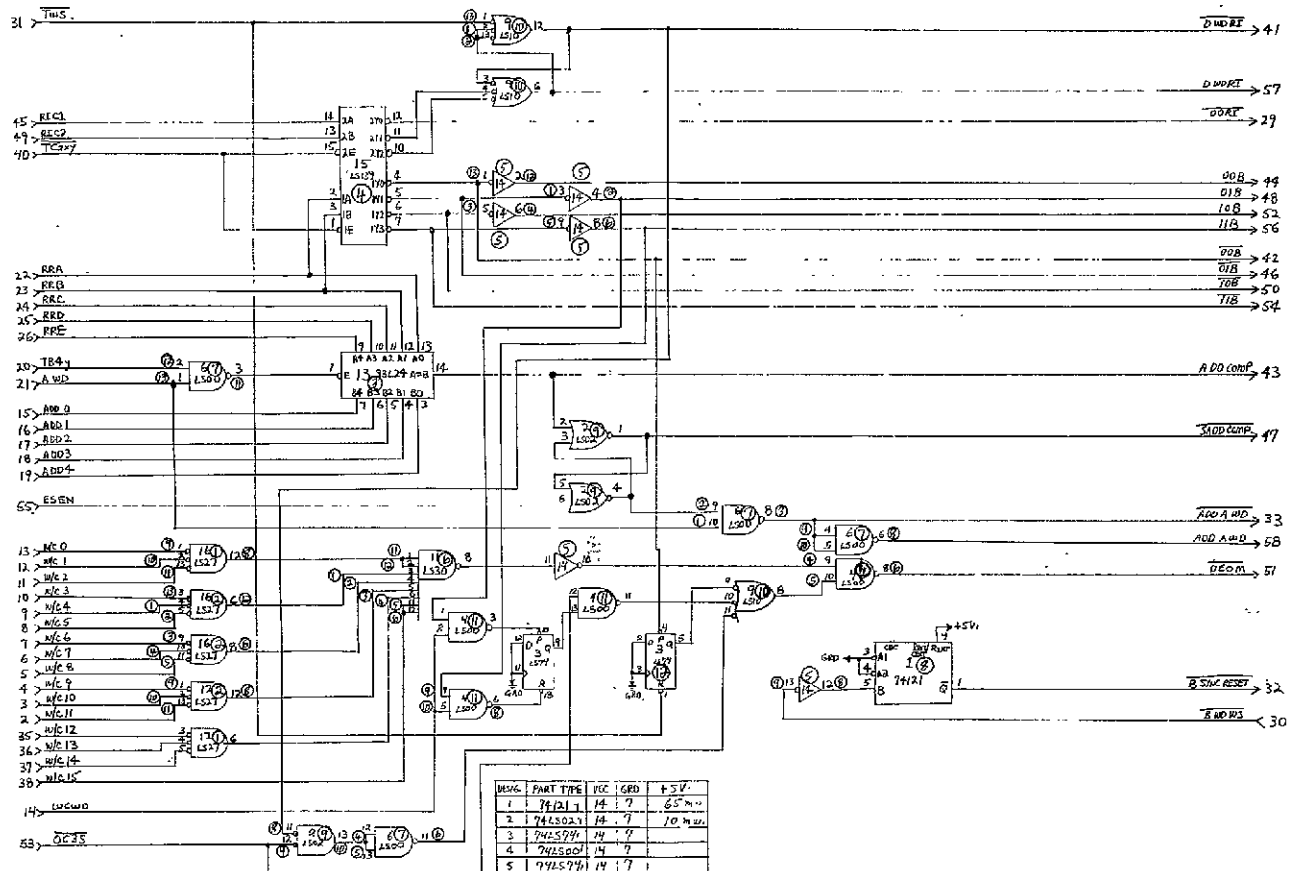
DESIG	PART TYPE	VCC	GRD	+5V.
1	74LS20	14	7	6 mA
2	74LS10	14	7	6 mA
3	—	—	—	—
4	74LS201	14	7	4 mA
5	74LS00	14	7	8 mA
6	74LS04	14	7	12 mA
7	74LS05	14	7	14 mA
8	74LS02	14	7	14 mA
9	74LS27	14	7	14 mA
10	74LS74	14	7	20 mA
11	74LS32	14	7	4 mA
12	74LS08	14	7	12 mA
13	74LS30	14	7	4 mA
14	74LS10	14	7	3 mA
15	74LS174	16	8	68 mA
16	74LS20	14	7	14 mA
BOARD POWER				201 mA

RECEIVE LOGIC 1
528
P.B. 3339042



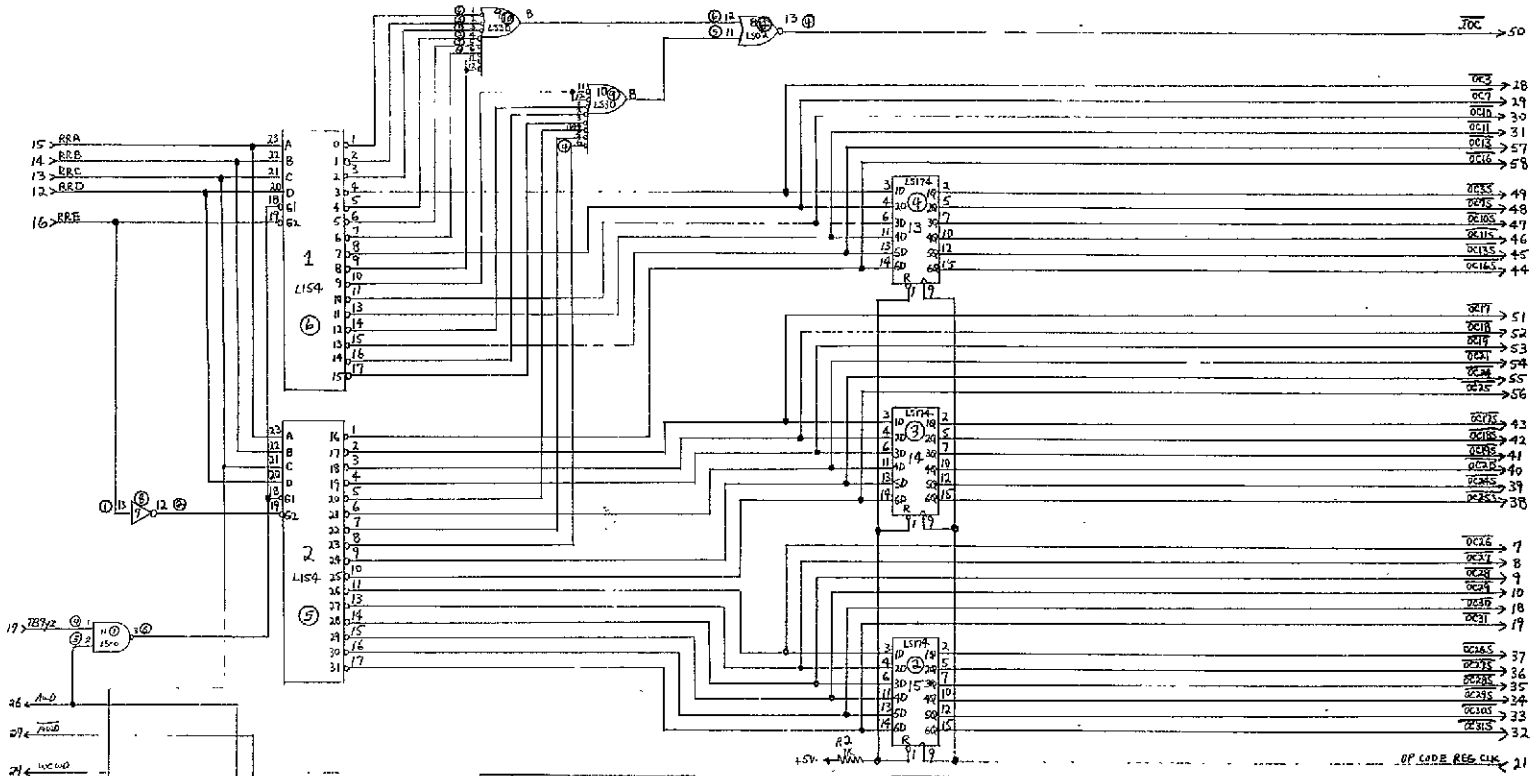
DESIG.	PART TYPE	VCC	GRD	+5V
1	74LS00	14	7	8 MA.
2	74LS10	14	7	6 MA.
3	74LS30	14	7	3 MA.
4	74LS02	14	7	10 MA.
5	74LS04	14	7	12 MA.
6	74C165	16	8	20 MA.
7	74C165	16	8	20 MA.
8	74LS27	14	7	14 MA.
9	74LI64	14	7	88 MA.
10	74LI64	14	7	88 MA.
11	74LI64	14	7	88 MA.
12	74LS27	14	7	14 MA.
13	74LS193	16	8	85 MA.
14	74LS193	16	8	85 MA.
15	74LS193	16	8	85 MA.
16	74LS193	16	8	85 MA.
BOARD POWER				709 MA.

RECEIVE LOGIC 2
529
P.B. 3339040



MFG.	PART TYPE	VCC	GRD	+5V.
1	74121	14	7	65 mw.
2	74LS02	14	7	10 mw.
3	74LS74	14	7	
4	74LS00	14	7	
5	74LS74	14	7	
6	74LS00	14	7	8 mw.
7	—	—	—	—
8	—	—	—	—
9	74LS10	14	7	6 mw.
10	—	—	—	—
11	74LS30	14	7	3 mw.
12	74LS27	14	7	19 mw
13	AM93L24	16	8	52 mw
14	74LS04	14	7	12 mw.
15	74LS139	16	8	34 mw
16	74LS27	14	7	19 mw.
BOARD POWER				219 mw.

RECEIVE LOGIC 3
S30
P.B. 3339032



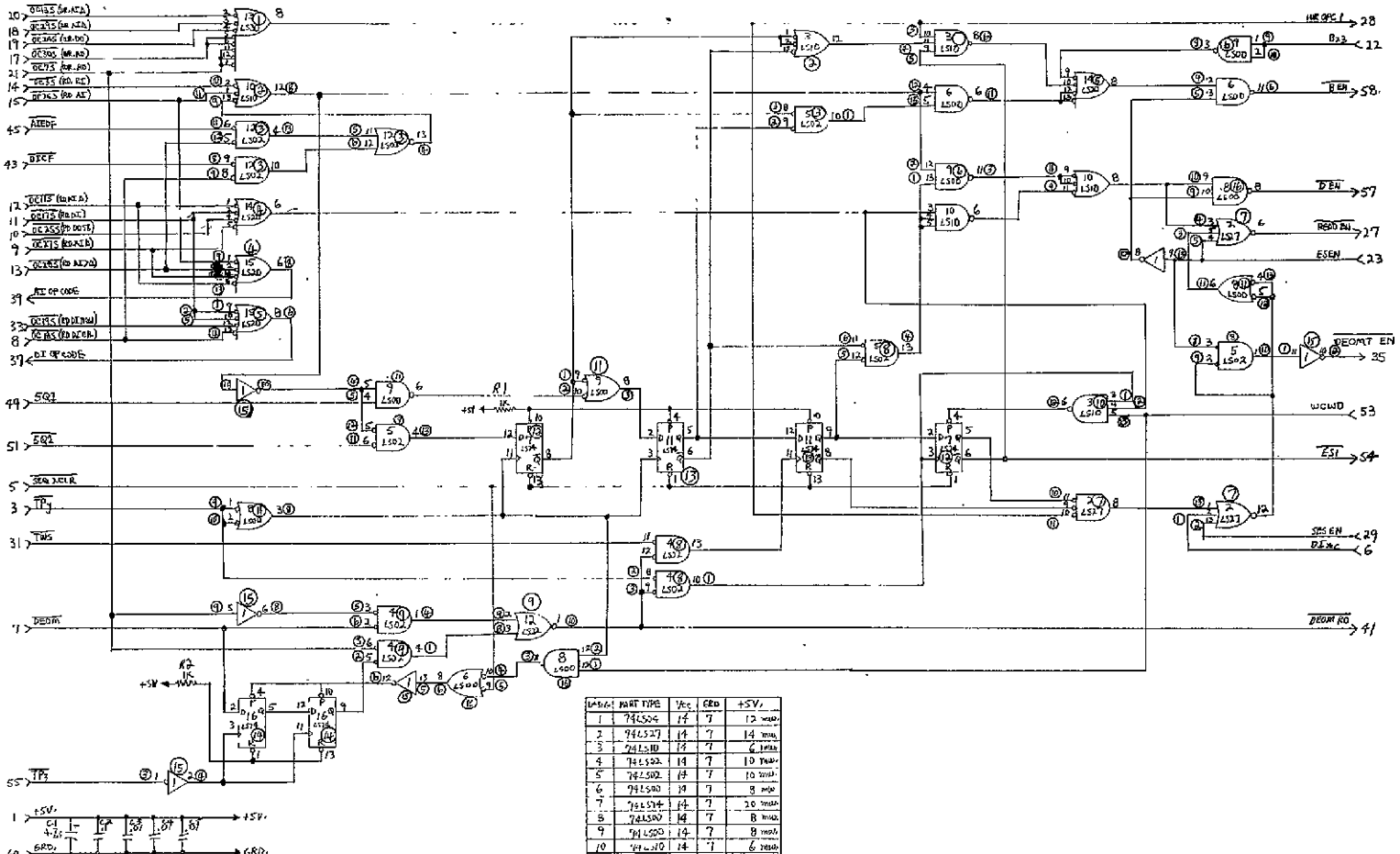
DESIG	PART TYPE	VCC	GND	+5V.
1	74LS154	24	12	85 mw.
1	74LS154	24	12	85 mw.
3	—	—	—	—
4	—	—	—	—
5	—	—	—	—
6	—	—	—	—
7	74LS04	14	7	12 mw.
8	74LS02	14	7	10 mw.
9	74LS30	14	7	3 mw.
10	74LS30	14	7	5 mw.
11	74LS00	14	7	8 mw.
12	74LS174	14	7	20 mw.
13	74LS174	16	8	66 mw.
14	74LS174	16	8	66 mw.
15	74LS174	16	8	66 mw.
16	74LS74	14	7	20 mw.
BOARD POWER				494 mw.

OP CODE	FUNCTION	OP CODE	FUNCTION
0	IOC	16	WRITE DI NON CAN.
1	IOC	17	READ DI
2	IOC	18	READ DI CHANNEL
3	READ KEY	19	READ DI NON CAN.
4	IOC	20	IOC
5	IOC	21	DCU/DCX TRANSFER
6	IOC	22	IOC
7	WRITE RO	23	IOC
8	IOC	24	WRITE DO
9	IOC	25	READ DO STATUS
10	READ ERROR STATUS	26	READ A1
11	READ A1 AS (0-63)	27	READ A1 AS (64-127)
12	IOC	28	READ A1 > A
13	WRITE A1 AS (0-63)	29	WRITE A1 AS (64-127)
14	IOC	30	WRITE A0
15	IOC	31	RESET

RECEIVE LOGIC 4
531
P.B. 3339036

FOLDOUT FRAME 1

FOLDOUT FRAME 2



LABEL	PART TYPE	Vcc	GRD	+5V.
1	74LS04	14	7	12 mA
2	74LS27	14	7	14 mA
3	74LS10	14	7	6 mA
4	74LS32	14	7	10 mA
5	74LS02	14	7	10 mA
6	74LS00	14	7	8 mA
7	74LS14	14	7	20 mA
8	74LS08	14	7	8 mA
9	74LS00	14	7	8 mA
10	74LS10	14	7	6 mA
11	74LS04	14	7	20 mA
12	74LS02	14	7	10 mA
13	74LS30	14	7	3 mA
14	74LS20	14	7	4 mA
15	74LS20	14	7	4 mA
16	74LS74	14	7	30 mA
BOARD POWER				163 mA

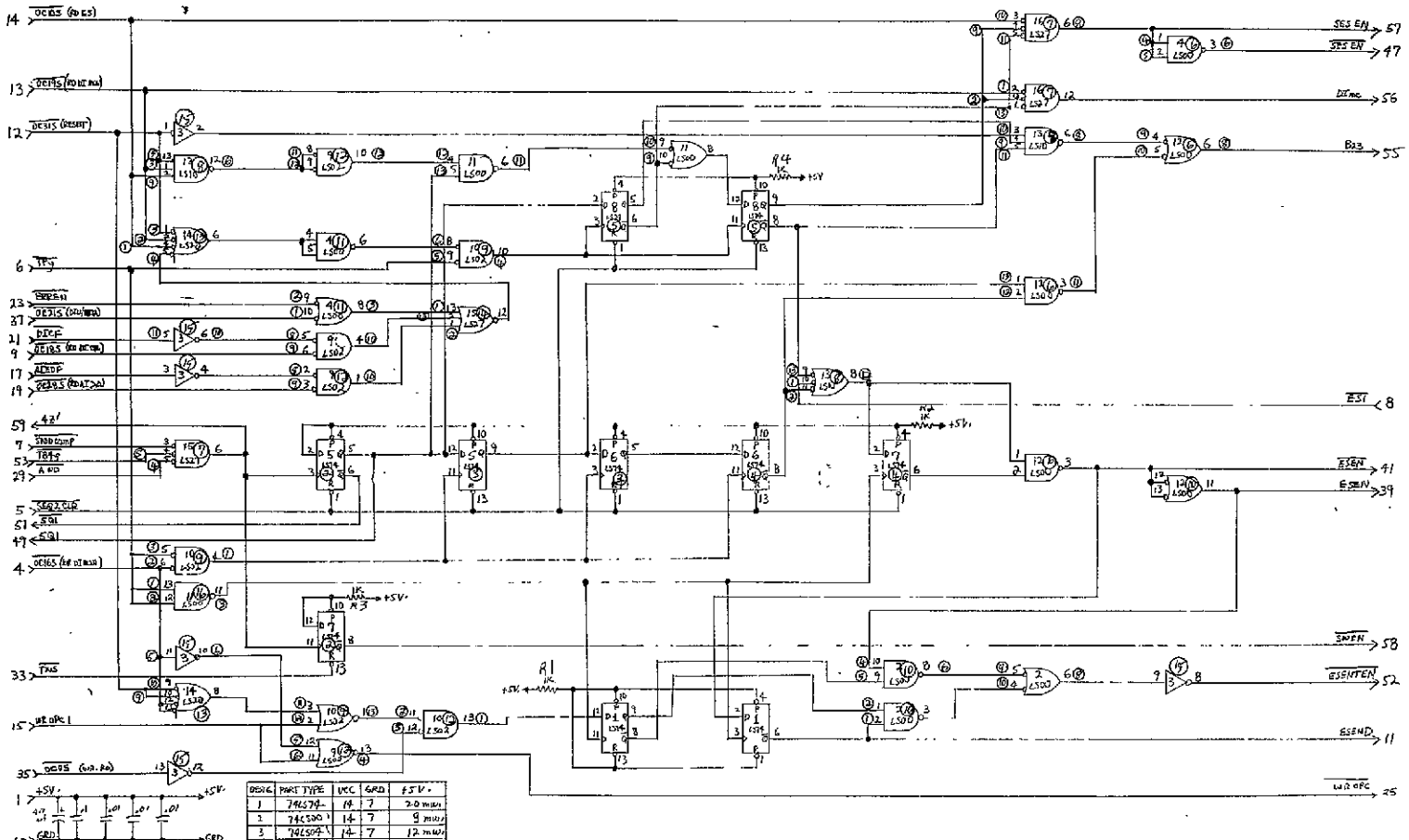
REPLY SEQUENCER 1

532

P.B. 3339028

FOLDOUT FRAME

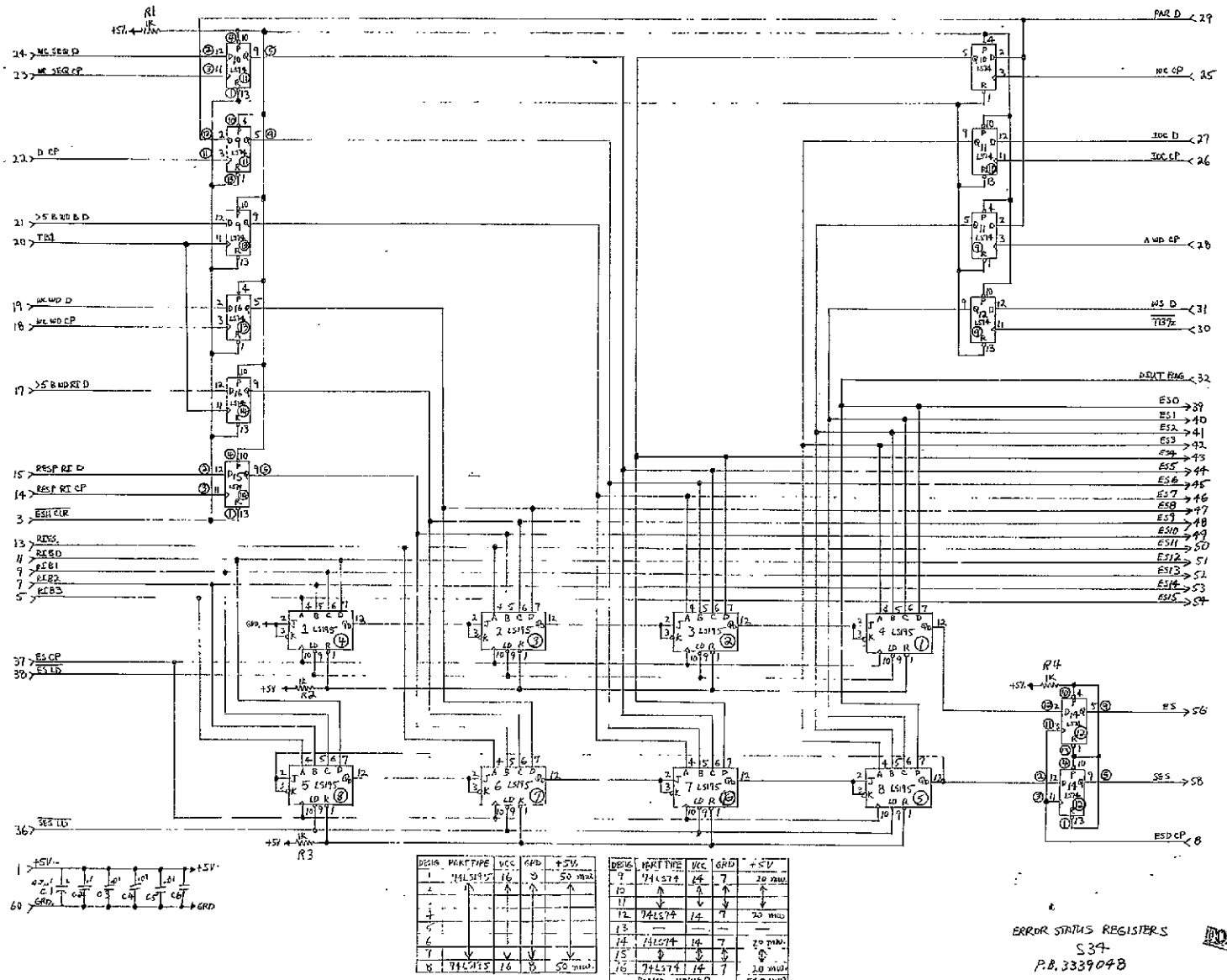
FOLDOUT FRAME 2



DESIG	PART TYPE	VCC	GRD	+5V.
1	74LS74	14	7	20 mA
2	74LS00	14	7	9 mA
3	74LS04	14	7	12 mA
4	74LS00	14	7	9 mA
5	74LS74	14	7	20 mA
6	74LS74	14	7	20 mA
7	74LS74	14	7	20 mA
8	74LS74	14	7	20 mA
9	74LS02	14	7	10 mA
10	74LS02	14	7	10 mA
11	74LS00	14	7	8 mA
12	74LS00	14	7	8 mA
13	74LS10	14	7	6 mA
14	74LS20	14	7	4 mA
15	74LS27	14	7	19 mA
16	74LS27	14	7	14 mA
	BOARD POWER			203 mA

KEPLY SEQUENCER 2
533
P.B. 3339034

FOLDOUT FRAME 2

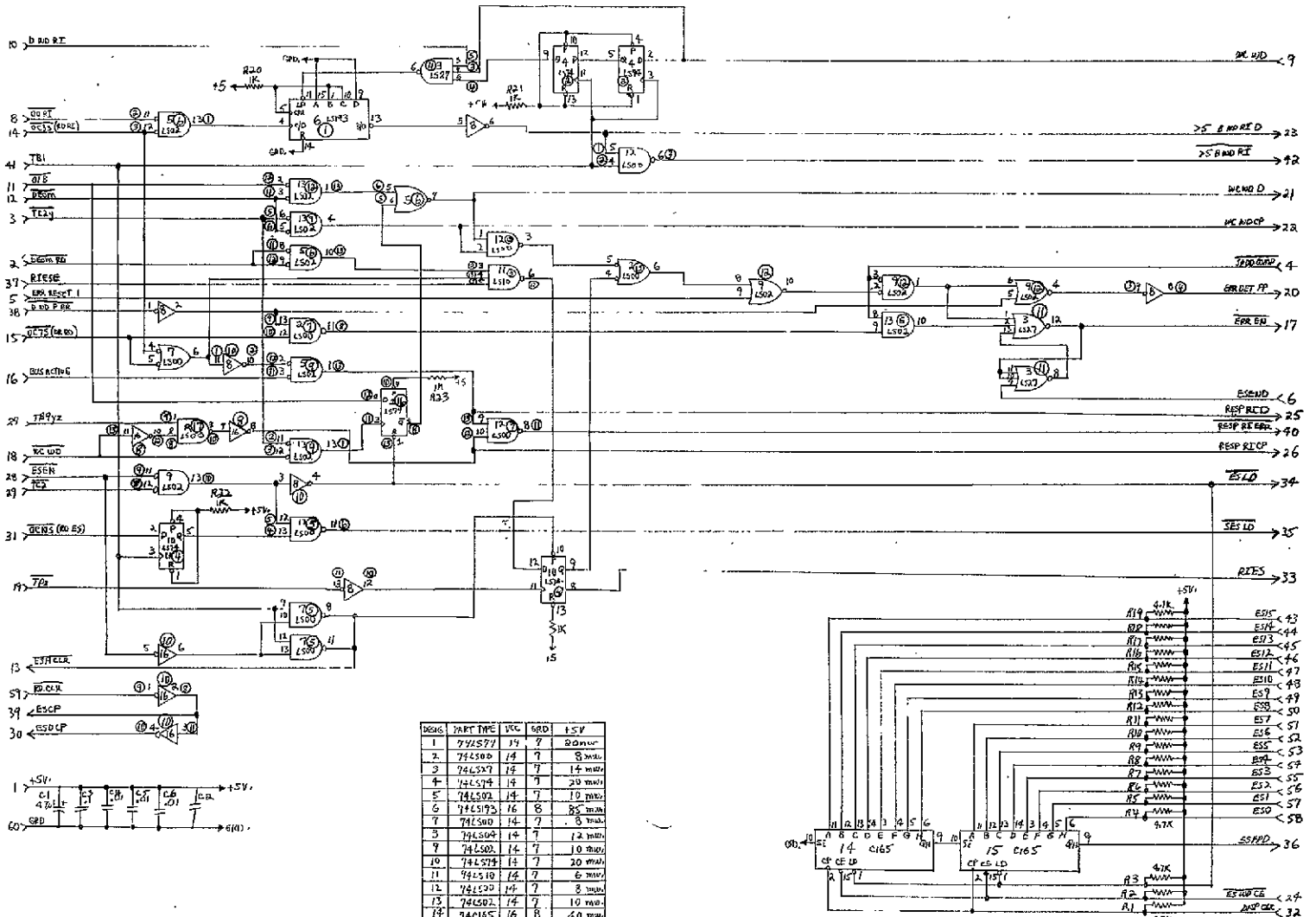


ERROR STATUS REGISTERS
S34
P.B. 3339048

FOLDOUT FRAME

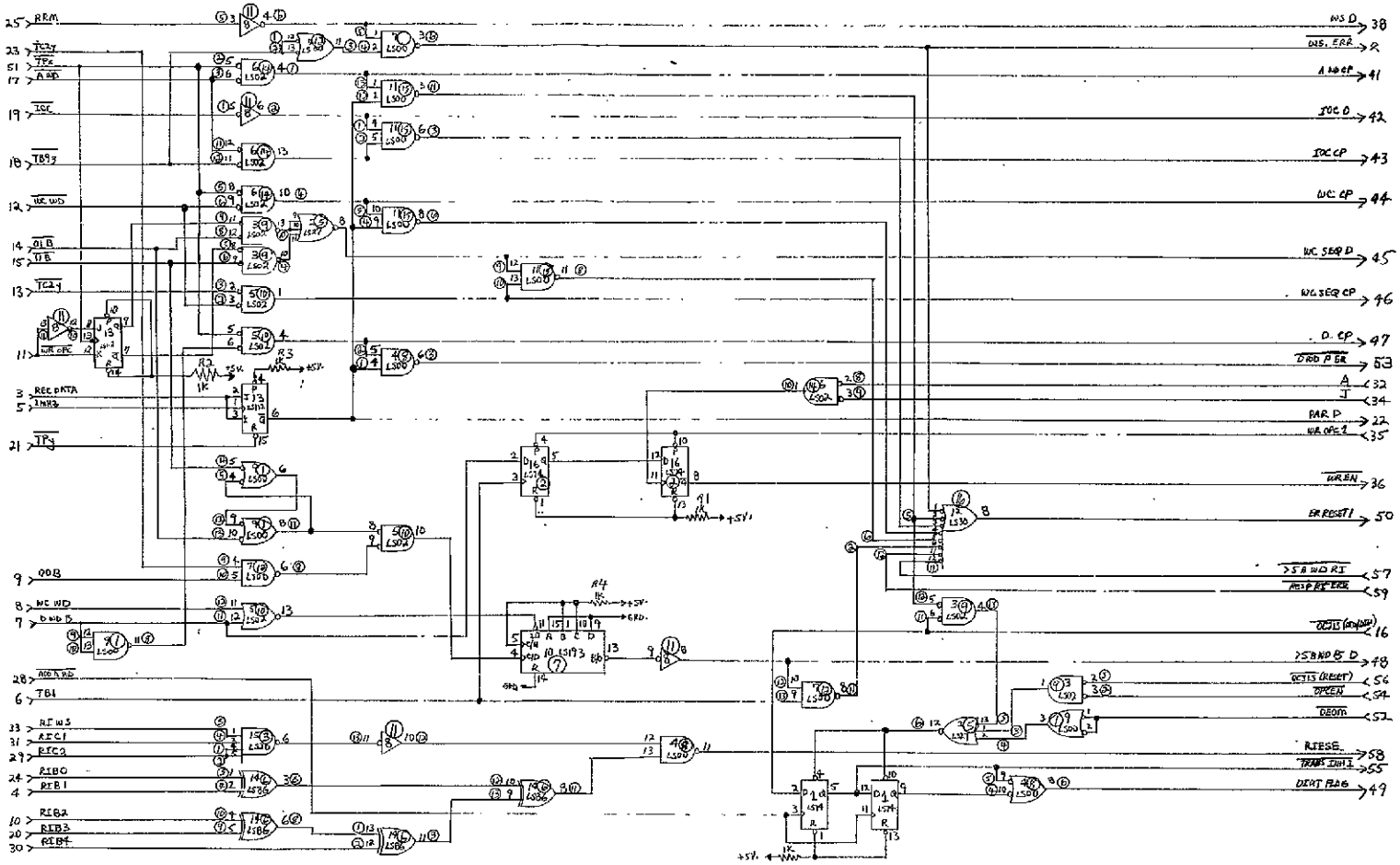
FOLDOUT FRAME

2



DESIG	PART TYPE	VCC	GRD	+5V
1	74LS377	14	7	20mw
2	74LS00	14	7	8 mw
3	74LS27	14	7	14 mw
4	74LS74	14	7	30 mw
5	74LS02	14	7	10 mw
6	74LS193	16	8	85 mw
7	74LS00	14	7	8 mw
8	74LS09	14	7	12 mw
9	74LS02	14	7	10 mw
10	74LS74	14	7	30 mw
11	74LS10	14	7	6 mw
12	74LS30	14	7	8 mw
13	74LS02	14	7	10 mw
14	74C165	16	8	40 mw
15	74C165	16	8	40 mw
16	74LS04	14	7	12 mw
BOARD POWER				393 mw

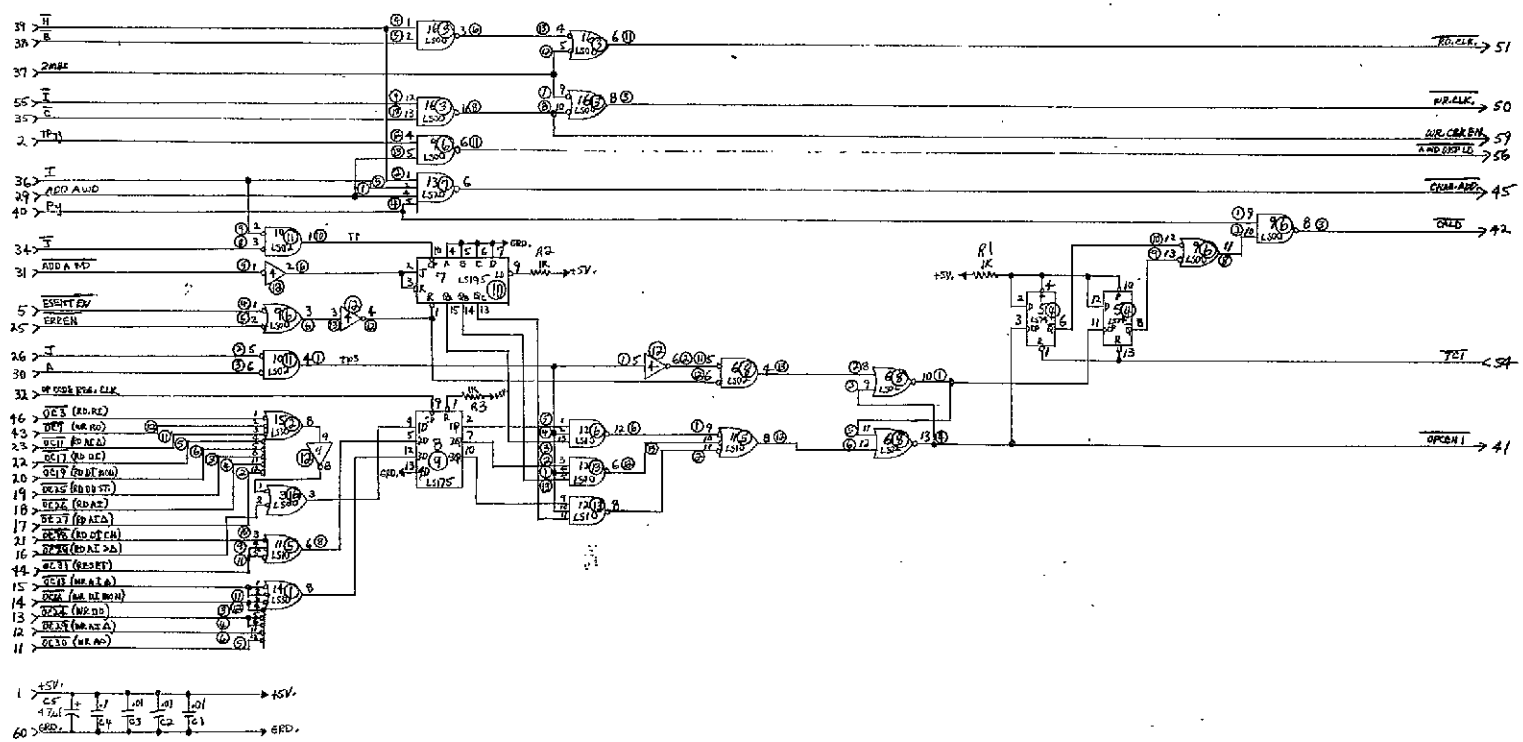
ERROR STATUS 1L
535
P.B. 3339046



DESIG	PART TYPE	VCC	GRD	+5V
1	74LS74	14	7	20 mw.
2	74LS27	14	7	14 mw.
3	74LS02	14	7	10 mw.
4	74LS00	14	7	8 mw.
5	74LS02	14	7	10 mw.
6	74LS02	14	7	10 mw.
7	74LS00	14	7	8 mw.
8	74LS04	14	7	12 mw.

DESIG	PART TYPE	VCC	GRD	+5V
9	74LS00	14	7	8 mw.
10	74LS193	16	8	85 mw.
11	74LS00	14	7	8 mw.
12	74LS30	14	7	3 mw.
13	74LS112	16	8	20 mw.
14	74LS86	14	7	30 mw.
15	74LS20	14	7	4 mw.
16	74LS74	14	7	20 mw.
BOARD POWER				270 mw.

ERROR STATUS 2
536
P.B. 3339038



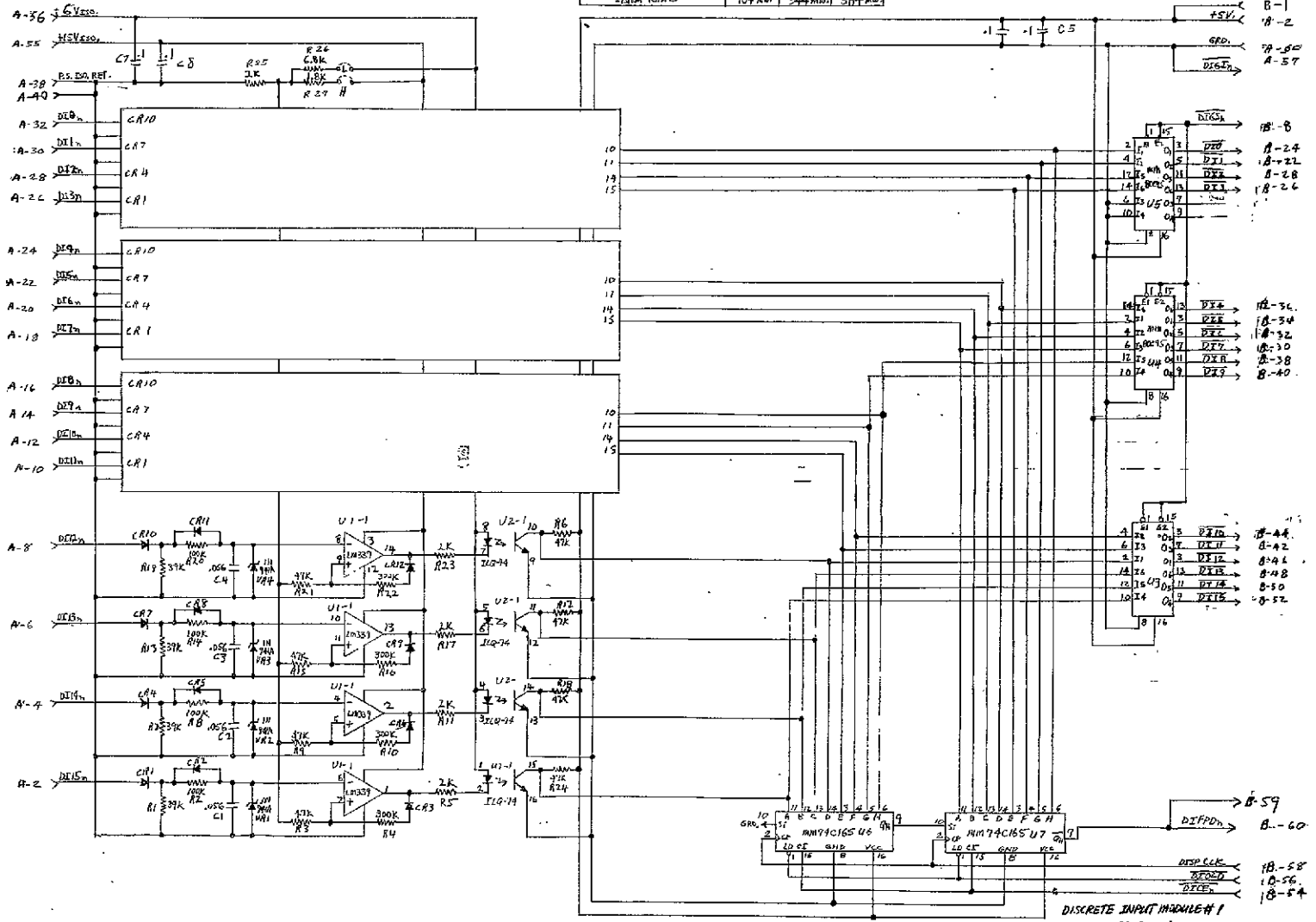
DESIG	PART TYPE	VCC	GRD	+5V
1	—	—	—	—
2	—	—	—	—
3	—	—	—	—
4	74LS04	14	7	12 mw.
5	74LS74	14	7	20 mw.
6	74LS02	14	7	10 mw.
7	74LS195	16	8	50 mw.
8	74LS175	16	8	45 mw.
9	74LS00	14	7	8 mw.
10	74LS02	14	7	10 mw.
11	74LS10	14	7	6 mw.
12	74LS10	14	7	6 mw.
13	74LS20	14	7	4 mw.
14	74L330	14	7	3 mw.
15	74L330	14	7	3 mw.
16	74LS00	14	7	8 mw.
BOARD POWER				18.5 mw.

TIMING 2
537
P.B. 3339 044

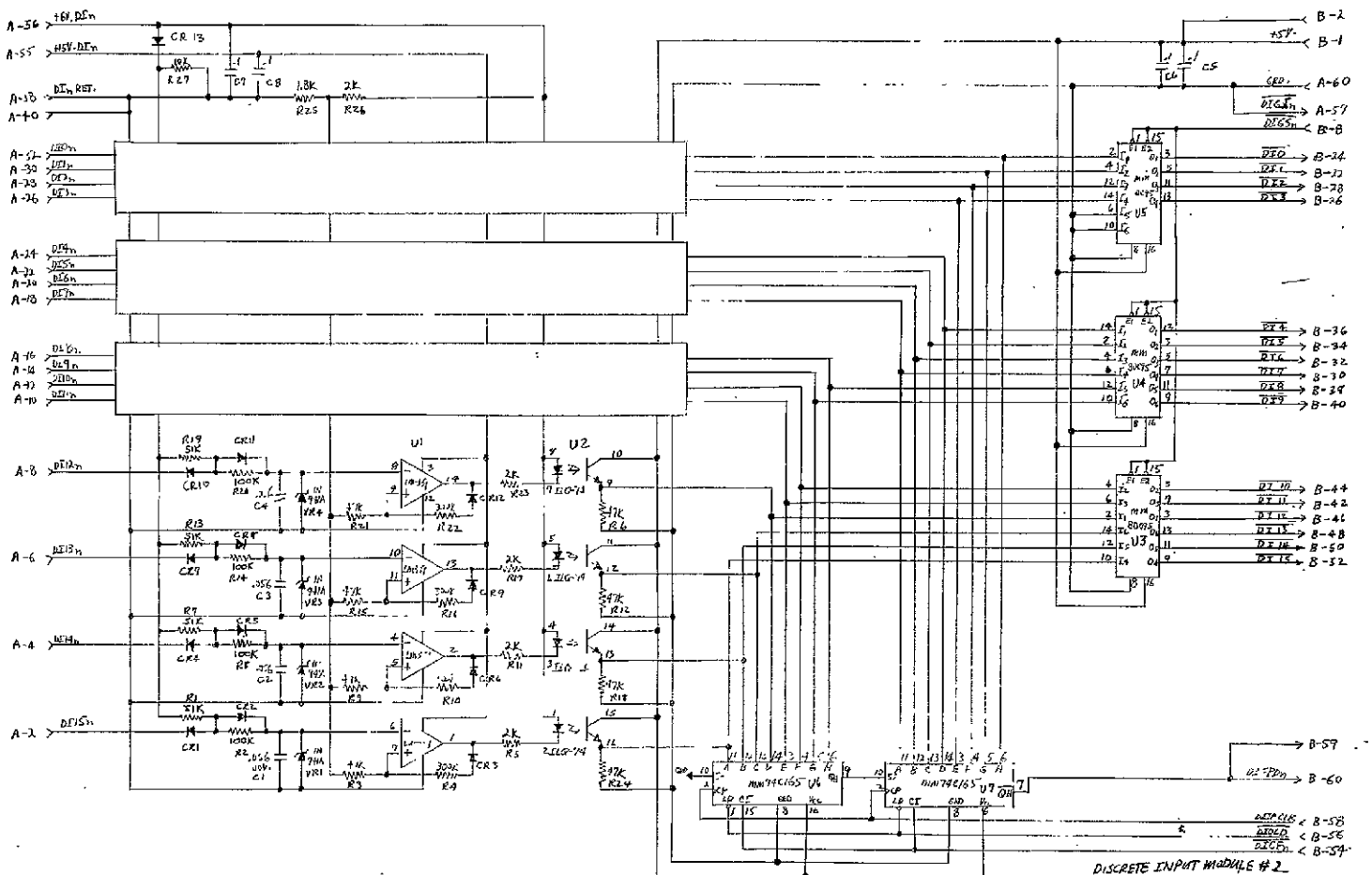
FOLDOUT FRAME 1

FOLDOUT FRAME 2

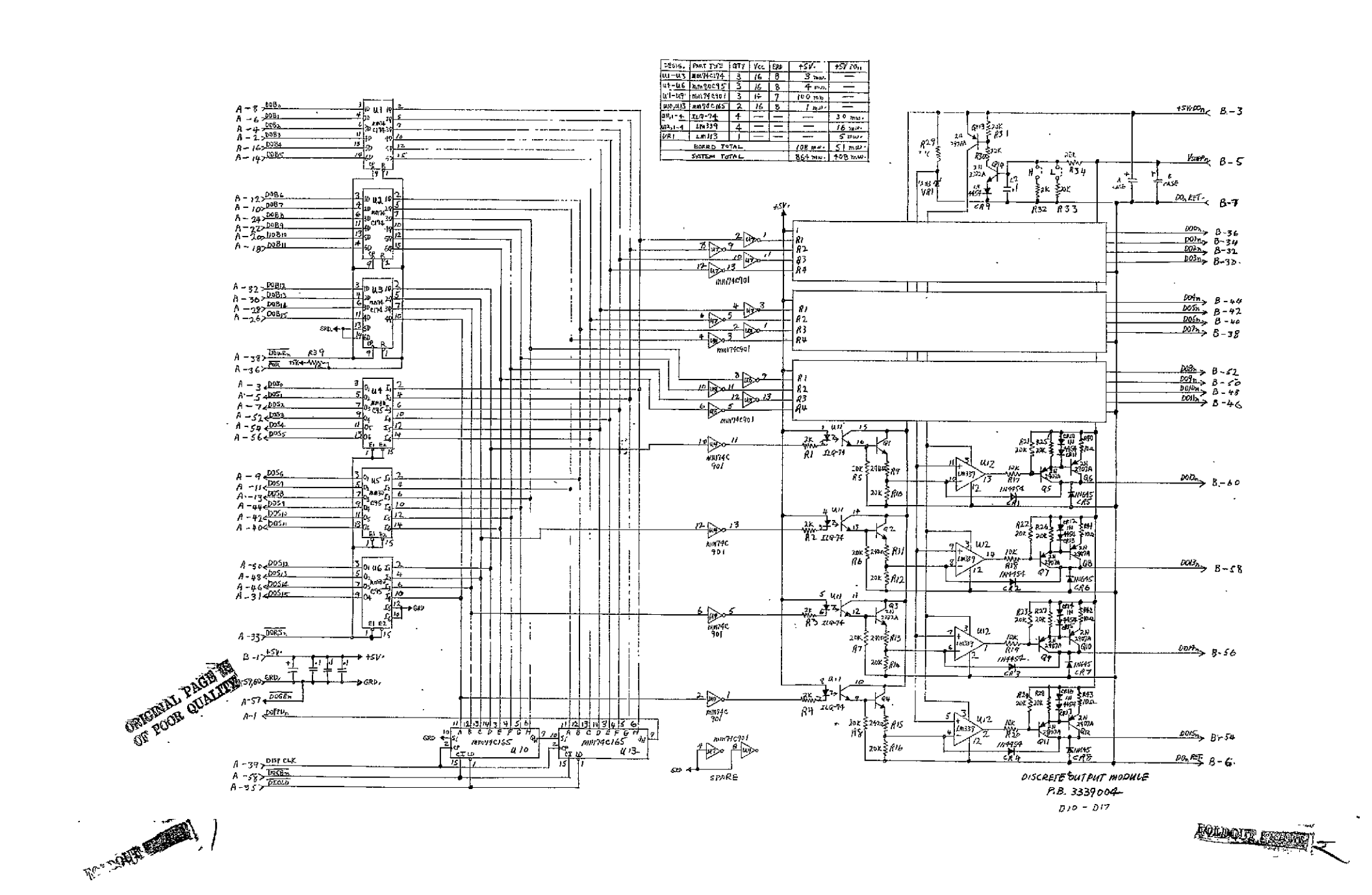
DESIG.	PART TYPE	Vcc	GRD.	+5V.	+6V. OUT	+5V. OUT
U1, 1-4	LM339	—	—	—	—	48 MAX.
U2, 1-4	ILQ-74	—	—	8 MAX.	43 MAX.	—
U3-U5	MM74C165	16	8	4 MAX.	—	—
U6, U7	MM74C165	16	8	1 MAX.	—	—
BOARD TOTAL				13 MAX.	43 MAX.	48 MAX.
SYSTEM TOTAL				104 MAX.	344 MAX.	384 MAX.



DESIG.	PART TYPE	Vcc	GRD	+5V.	+6V. DIn	+15V DIn
U1-4	LM 339	—	—	—	—	48 mw.
U2-4	ZLG-74	—	—	8 mw.	43 mw.	—
U3-U5	DM8095	16	8	4 mw.	—	—
U6, U7	MM74C165	16	8	1 mw.	—	—
BOARD TOTAL				13 mw.	43 mw.	48 mw.
SYSTEM TOTAL				104 mw.	344 mw.	384 mw.



DISCRETE INPUT MODULE #2
P.B. 3339018
Location D1-D8 (2 each


DISCRETE OUTPUT MODULE
P.B. 3339004
D10 - D17
SPARE
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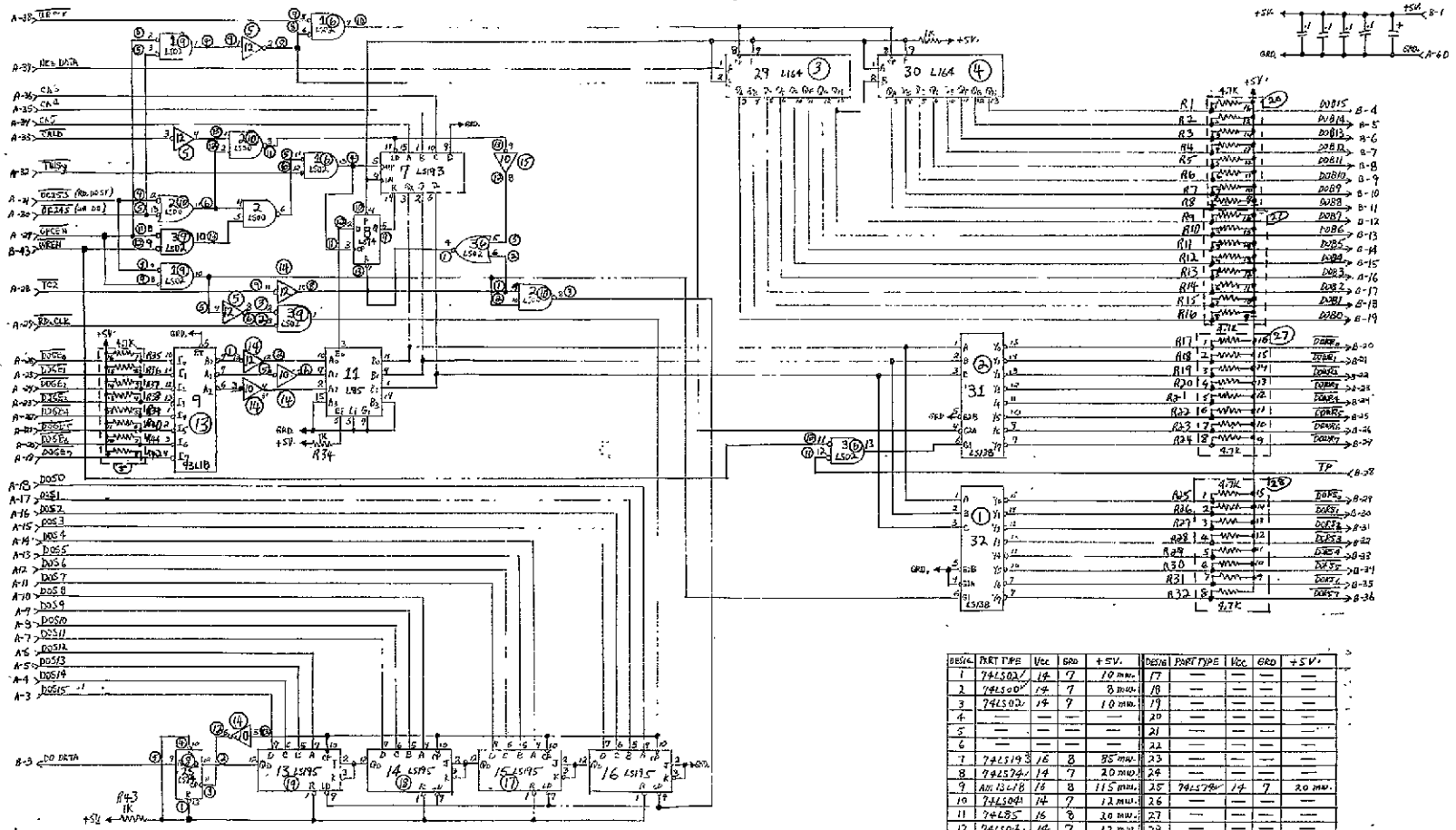
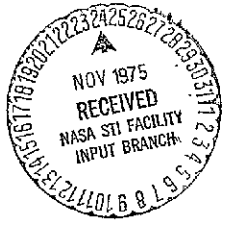


DESIG	PART TYPE	Vcc	GRD	+5V.	DESIG	PART TYPE	Vcc	GRD	+5V.
1	74LS02	14	7	10 ma.	17	—	—	—	—
2	74LS00	14	7	8 ma.	18	—	—	—	—
3	74LS02	14	7	10 ma.	19	—	—	—	—
4	—	—	—	—	20	—	—	—	—
5	—	—	—	—	21	—	—	—	—
6	—	—	—	—	22	—	—	—	—
7	74LS193	16	8	85 ma.	23	—	—	—	—
8	74LS74	14	7	20 ma.	24	—	—	—	—
9	AM 13L18	16	8	115 ma.	25	74LS74A	14	7	20 ma.
10	74LS04	14	7	12 ma.	26	—	—	—	—
11	74L85	16	8	30 ma.	27	—	—	—	—
12	74LS04	14	7	12 ma.	28	—	—	—	—
13	74LS195	16	8	50 ma.	29	74L164	14	7	124 ma.
14	74LS195	16	8	50 ma.	30	74L164	14	7	124 ma.
15	74LS195	16	8	50 ma.	31	74LS138	16	8	31 ma.
16	74LS195	16	8	50 ma.	32	74LS138	16	8	31 ma.
					BOARD, SYSTEM TOTAL				822 ma.

DISCRETE OUTPUT MUX CONTROL
DIB
P.B. 3339066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INPUT BRANCH

DATA MANAGEMENT SYSTEM
CIU AND DIU
FINAL TECHNICAL REPORT

APPENDIX A
CIU AND DIU SCHEMATICS

PREPARED FOR
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GEORGE C. MARSHALL SPACE FLIGHT CENTER
UNDER CONTRACT
NAS8-29155

PREPARED BY
SCI SYSTEMS, INC.
OCTOBER, 1975