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FINAL REPORT

Development of InSb Charge-Coupled Infrared Imaging Device – Linear Imager

Contract No. NAS1-13937

For - National Aeronautics and Space Administration
Langley Research Center
Hampton, Virginia

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1 April 1976

Prepared by James D. Phillips
James D. Phillips
Project Manager

Approved by
R. E. Eck, Head
Research Section
Components Laboratory

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Section 1

INTRODUCTION

The development of indium antimonide (InSb) Charge-Coupled Infrared Imaging Devices (CCIRIDs) by Santa Barbara Research Center has proceeded under NASA contract for approximately three years. By using charge transfer techniques for infrared imaging, processing of the desired signal can be achieved in real time on the focal plane with the attendant advantages of reductions in sensor power and weight requirements. Since the applications of these CCIRID structures include remote sensing of the earth from spacecraft as well as outer planet exploration, these features of the new devices are significant.

The feasibility of the concept[1] was demonstrated under NASA Contract NASl-12087. During this contract, InSb MIS devices were fabricated and tested to establish the requisite processing parameters for an InSb charge-coupled device. The success of this effort enabled the design of a 4-bit CCD mask set (8580) complete with other test structures for process control. Dimensional and multilayer requirements of charge-coupled structures were demonstrated for the InSb process by fabrication trials with the 8580 mask set.

Development of InSb CCD fabrication techniques[2] continued under NASA contract NASl-13163. The success of this effort was marked by the important milestone of achieving charge transfer in the 8580 InSb CCD. A transfer efficiency of 0.90, which was low due to the extreme gate lengths of the 8580, was measured and led to the design of a new mask set (the 8582 set) with reduced gate lengths.

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[1] "Charge-Coupled Infrared Imaging Device (CCIRID) Feasibility Study," Final Report NASA CR-132383, Contract No. NASl-12087, December 1973.

[2] "Development of InSb CCD for Infrared Imager Applications," Final Report NASA CR-132694, Contract No. NASl-13163, May 1975.

The investigations detailed by this report were performed under contract NAS1-13937. In this program, the 2-bit CCD structure of the 8582 mask set was successfully operated. The gate lengths of this structure as well as the 9-bit CCIRID imager of the 8582 were reduced to 1.0 mil from the 2.0 mil values of the 8580 chip. As a result of this change, improvements in transfer efficiencies to $\alpha = 0.99$ were predicted for storage well depths of 2 volts. The observed efficiency of $\alpha \cong 0.975$ agrees well with this prediction. Since the predicted value for a 1-volt well depth (approximately the observed value) is $\alpha \simeq 0.983$, the agreement with prediction is even stronger.

Successful operation of the 9-bit 8582 imager was not achieved during this contract period. As a result, a prime objective of the program effort has not been fulfilled. The origins of this failure have been traced to design flaws in the 8582 mask set and to some features of the processing sequence used to fabricate the CCIRID structures. Despite the failure to achieve complete functional operation of the imager, some optical sensitivity has been observed. The observed optical response is fully controlled by the transfer gate of the 9-bit imager indicating successful charge transfer from the photosensors into the CCD registers. This indication is not conclusive, however, and full details are given in Section 2. Section 2 also discusses in detail the 8582 fabrication effort during this program, the test results for the 2- and 9-bit devices, and a proposed chip format for the next generation CCIRID.

In Section 3, the development of a 4ϕ computer model to predict performance and optimum CCIRID parameter values is described. This model is applicable to surface and buried channel CCD structures with the various CCD parameters — such as gate insulator thickness, dielectric strength of the insulator, and substrate doping — being completely variable. Typical results obtained from the model are given.

The transfer inefficiency requirements for the CCD registers of the CCIRID are described in Section 4 as a function of the number of sensors in the array. As the performance of the CCIRID as an imager is critically dependent on the modulation transfer function (MTF) of the device, this function is discussed in some detail with emphasis on the image degradation caused by the finite separation of the sensors, diffusion effects within the InSb substrate, and particularly on the effects of a finite transfer inefficiency. The results as they pertain to existing devices and to projected devices using current fabrication procedures are also discussed.

Finally, Section 5 presents the conclusions to be drawn from the investigations of this contract.

Section 2

FABRICATION AND TESTING

Two prime tasks of this contract involved the fabrication, with attendant process development and testing, of the CCIRID structures. In this section, the results of these activities are discussed in detail, treating fabrication first. Following this discussion, the results obtained for the 2-bit InSb CCD and the 9-bit CCIRID are presented. Finally, the design of the next generation of CCIRIDs is considered.

CCIRID FABRICATION

The fabrication of a prototype CCIRID was carried out with photomask set 8582, designed during the previous contract. This set yields a die containing a 9-bit, 4ϕ CCIRID with 25-μm (≈ 1.0-mil) gate lengths and four photosensitive regions for infrared detection as well as a 2-bit, 4ϕ CCD of similar gate lengths. For additional discussion on this design, reference is made to the final report[2] of the prior contract.

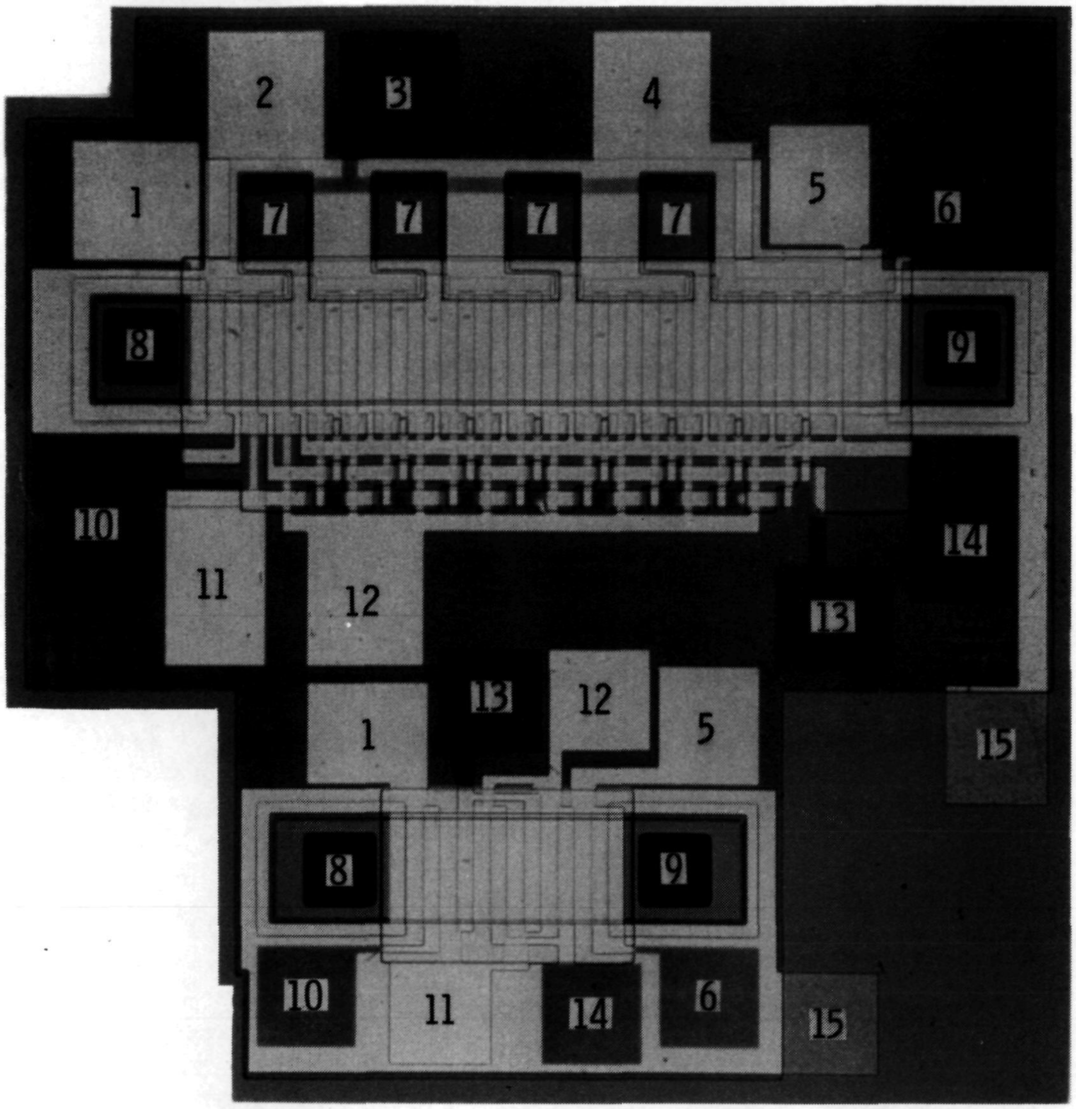
To date, forty wafers have been processed using the 8582 masks. The functional device yield from these runs has been low, and much of the effort during this period has focused on the reasons for the failures. As a means of identifying functional dice, the device dice are subjected to dc test. The phrase "dc test" denotes here a test sequence wherein a bias V_B is applied between, for example, the device substrate and channel stop metallization. If the device does not short under this test, performed at room temperature, then the test proceeds to a check of gate (buried or surface metal) to substrate, gate to channel stop, etc. The bias levels are typically 5 volts for all tests except channel stop to substrate in which a 1-volt bias is used.

From an analysis of the data obtained in this fashion, three principal modes for failure were identified. These were: 1) shorts between the channel stop metal and the substrate, 2) shorts between the buried and surface metals, and 3) input/output problems (e.g., lifting of gate insulator) associated with the mesa diodes.

The existence of shorts involving the channel stop metallization was traced to the overall size of this metal on the 8582 die. This die contains a 2-bit InSb CCD as well as the principal 9-bit CCIRID and, in the original mask design, the channel stop metal was made common to both devices. As a result of this connection, a large area existed over which the channel stop was separated from the substrate by only a thin (≃0.15-µm) insulator. The probability of a short due to insulator defects was then evidently increased due to this large area. In addition, the use of a common channel stop on the two CCDs resulted in failure of both devices even if there was only one defect on the entire die.

The solution to this problem was to significantly reduce the size of the channel stop metallization, and this was done by a mask redesign. The new channel stop pattern (illustrated in Figure 2-1) incorporates: 1) a separation of the metallization for the 2- and 9-bit devices, and 2) a reduction of the overall channel stop area. At the same time, an error involving the buried and surface metals was recognized on the 2-bit CCD. This error was also corrected during the 8582 mask redesign.

In considering the failures associated with the mesa diode structures, it becomes clear that these are related to the height (≃1.0 µm) of the mesa over the remainder of the InSb wafer. The mesa edge is essentially vertical so that coverage of the mesa edge by a 0.15-µm insulator becomes difficult. If there are adherence problems in the insulator, they will be most pronounced over these diodes and, indeed, some wafers have failed to complete processing due to "lifting" of the insulator on the mesa edges. To solve this problem, processing changes which will result in a smaller mesa height are being investigated in a related Company-funded study. The size of the decrease in the mesa height is limited by the diffusion depth of the diode junction. Best estimates indicate this depth to be approximately 0.3 µm from which a minimum mesa height of 0.5 µm is projected. This decrease should be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1 - INPUT SURFACE GATE (ϕ_{is})
2 - TRANSFER GATE (ϕ_T)
3 - PHOTOGATE (ϕ_p)
4 - ISOLATED ϕ_3 GATE (ϕ_{3i})
5 - OUTPUT SURFACE GATE (ϕ_{os})
6 - OUTPUT BURIED GATE (ϕ_{ob})
7 - SENSOR
8 - V_{INDC}
9 - OUTPUT DIODE
10 - INPUT BURIED GATE (ϕ_{ib})
11 - ϕ_1 CLOCK LINE
12 - ϕ_3 CLOCK LINE
13 - ϕ_2 CLOCK LINE
14 - ϕ_4 CLOCK LINE
15 - CHANNEL STOP (V_{CS})

Figure 2-1. Revised Channel Stop Metal Pattern on 8582 CCIRID Chip Together with Pad Identifications

sufficient to provide a significant drop in dc test failures of 8582 devices due to the mesa edge coverage.

Finally, the emergence of gate-to-gate shorts as a mode for dc failure is not entirely unexpected since such shorts have plagued CCD development from its inception — in silicon as well as InSb technology. The probable causes for these failures include: 1) defects in insulator separating gates, 2) existence of metal spikes in buried metal, and 3) critical points in device design. The term "critical points" here refers to regions in the device where there are multistep coverage requirements. An example is the entry port area where charge from the infrared sensitive photocells is introduced into the CCD registers. At these points, the probability of metal cracking or deficient insulator coverage is increased, and the chance for shorts also increased. Similarly, the existence of insulator defects, such as "pin holes," will increase incidence of gate-to-gate shorts. At the present time, however, the existence of metal spikes, which have been observed in SEM examination, seems the most likely cause for the shorts.

These spikes arise in the delineation step for the buried metal gate level, and occur at the edges of the gates in the processing of the 8582 device. Since the field strength is greatest at these points, it is believed that the spikes lead to preferential breakdown of the insulator in the regions covering these metal towers. Several approaches to minimize the impact of such structures were studied, and steps to reduce their height have been implemented. Recent runs have demonstrated that these corrections were sufficient to eliminate gate-to-gate shorts as a dominant failure mode.

The success of these studies is exemplified by the fact that the first run to be processed, which incorporated the mask changes and the steps to reduce gate-to-gate shorts, produced sixteen 9-bit devices and twenty 2-bit devices to pass the dc portion of the test. These successes were the result of forty-seven 2-bit and thirty-five 9-bit dice tested, which projects to 42% and 45% dc yields, respectively. The runs fabricated to completion since this first success have shown similar dc yields. The CCIRID process sequence is still not optimized, however, as is clear from 1) the small yield of ac functional units from the die passing the dc test, and 2) the incidence of poor adherence between some of the thin-film interfaces of the CCIRID multilevel structure. As regards the latter problem, the most notable layers to exhibit lack of adhesion are those for the channel stop and the buried metal insulator. A majority of the 8582 runs processed during this contract were stopped by the lifting of one of these layers, and thus impacted the production/test schedule of completed CCIRID dice.

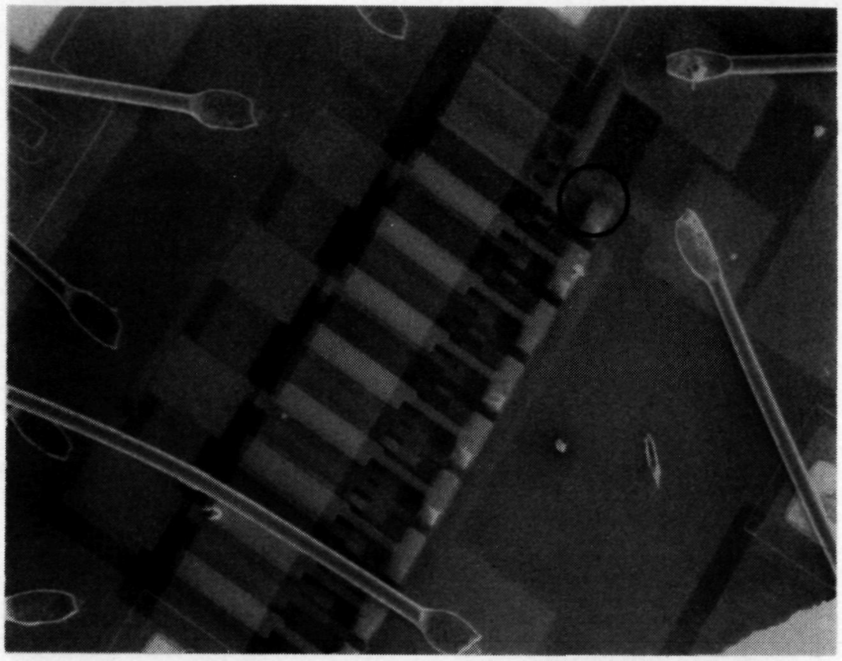
The lifting of a particular layer destroys, or at least degrades, device performance by causing breakage or tearing of overlying films (e.g., clock lines), thus preventing normal device operation. On the 8582 chip, three general regions of the 9-bit device have been identified where lifting and/or breakage phenomena occur. Foremost among these are the edges of the mesa diodes. As observed above, the height of these edges makes coverage by a thin film difficult even if the film adherence is good. If the adherence is weak, however, the lifting of the layer will begin at those points of greatest stress and, for the 8582 chip, one such point is the mesa edge. The process experience gained during this contract has confirmed that these edges do serve as the source of layer lifting in about 70% of the cases. With this large effect, the studies to reduce the height of the mesa diodes assume added significance.

A second region where layer adherence is a problem are those points where the transfer gate crosses the photosensitive infrared sensors. In about 50% of the cases, the portion of this gate which actually touches the sensor is observed to lift from the die. The remainder of the gate remains intact, however, so that the ability of this line to function as designed remains unimpaired. This lifting problem, which is due entirely to the topography of the photosensor sites for the 8582 design, is therefore not as severe as that associated with the mesas.

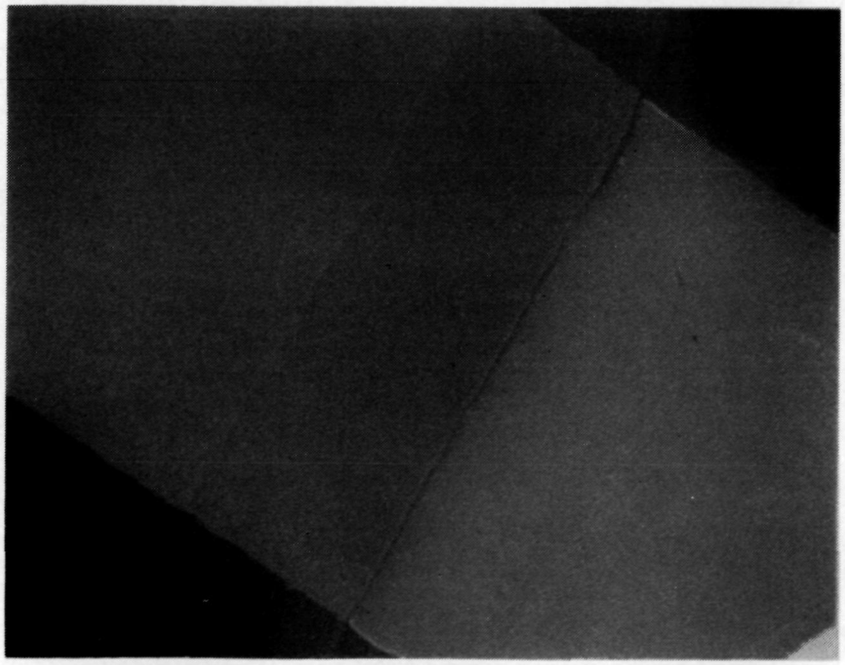
The final problem area noted on the 9-bit structure is the step(s) formed by the buried metal insulator. At these steps, the clock lines (ϕ_1, ϕ_3) show a tendency to crack or break at about 10% of the steps to be covered. A similar situation exists for the surface metal jumper of the ϕ_2 clock line. These breaks have prevented full operation of the 9-bit CCIRID thus far. To understand the nature of the problem, voltage contrast studies of the device were carried out. This method utilizes a scanning electron microscope to image the device while one or more gates are under bias. If a line is electrically continuous, then the contrast of the line is considerably brighter than the surrounding, unbiased levels. The success of this approach is illustrated in Figure 2-2(a) where the result of a -16-volt bias, applied to the ϕ_1 clock line relative to the InSb substrate, is shown. Note that only one ϕ_1 line is not bright in the channel. The source of the discontinuity is indicated by the inset of the figure, and it is apparent from Figure 2-2(b) that the problem is a break in the metal at the buried metal insulator step. Breaks similar to this one were observed also on the ϕ_2 and ϕ_3 clock lines. Since each device examined by this technique exhibited at least one such break, this insulator step qualifies as the principal source of defective 9-bit structures.

However, one possibility, other than the BMI step, for the observed breaks does exist, and that is thermal shock. Thus, the InSb CCIRIDs must be cooled (to ≃ 80°K) to operate properly, and the breakage phenomenon could result from the thermal stress induced by the rapid changes in temperature during the cooling cycle. To investigate this possibility, a CCIRID which had passed the dc test sequence — but had not been subjected to the thermal cycling procedure — was tested via the voltage contrast technique. The breaks at the BMI steps were again observed, however, with the overall appearance being virtually identical with that shown in Figure 2-2 for thermally cycled devices. As a result, it is concluded that the BMI step, not thermal cycling, is the reason for the lack of functional 8582 CCIRIDs.

To amend this defect, several options are available. The first involves an adjustment of the thicknesses for the buried metal insulator, the surface metal and, to a lesser extent, the channel stop insulator. By this approach, the reduction in height of the insulator step could lead to better coverage,



(a) ϕ_1 Clock Line Biased at -16V Relative to InSb Substrate; All Other Gates Connected to Substrate. Magnification 70×.



(b) Intensification of Inset in (a) to Magnification of 5000×.

Figure 2-2. Scanning Electron Micrograph in Voltage Contrast Mode of 8582 9-Bit Imager

i.e., less breakage of the lines. That this technique is not sufficient was demonstrated by biasing (-16 volts relative to substrate) the input surface gate (ϕ_{is}) of the 9-bit device. Figure 2-3 shows the result of this operation. The continuity of the gate is clear, yet this surface metal gate must cover the step of the mesa diode edge. The height of this step is approximately 0.75 μm compared with the 0.3-μm step of the buried metal insulator. It is then apparent that the overall step height is not the sole problem.

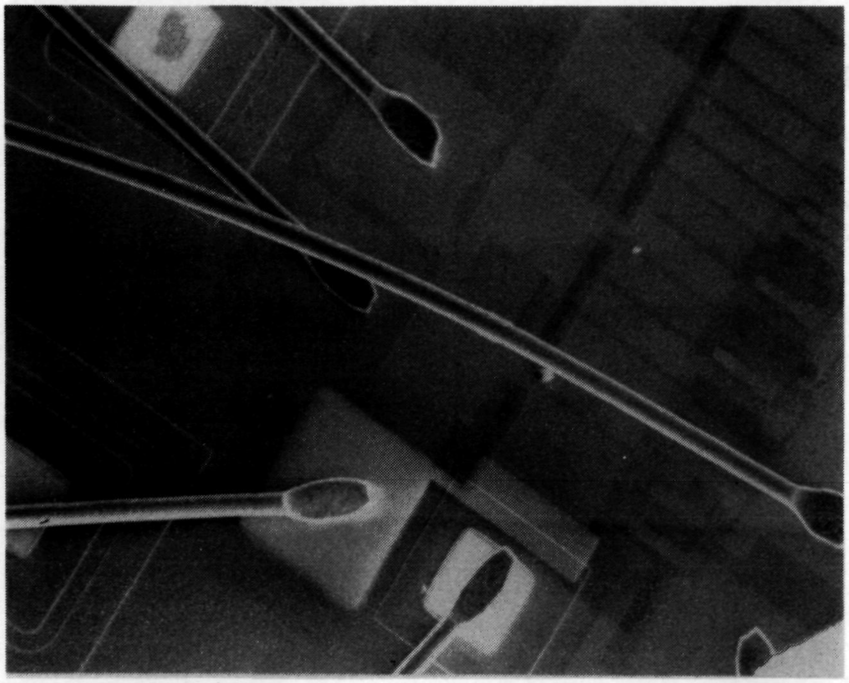


Figure 2-3. Scanning Electron Micrograph, with SEM in Voltage Contrast Mode, of Input Surface Gate (ϕ_{is}) of 9-Bit 8582 Linear Imager. (ϕ_{is} biased at -16V relative to InSb substrate; all other gates grounded to substrate.)

An assessment of these results in conjunction with the complete fabrication sequence of the 8582 indicates that the principal difficulty is not the step height but the delineation of the insulator itself. This process is accomplished by the well-known technique of reverse photolithography which can potentially introduce a microscopic "tearing" of the layer edges as it is defined. The problem of breakage is thus not due to failure of the surface metal to cover a step, but instead to the tearing of the insulator away from the underlying layer. This action can create a ragged insulator edge to which the surface metal can bond only with difficulty. The voltage contrast studies reveal that the bond is adequate in most cases but, at about one step out of ten, the thin surface metal strip exhibits "microcracks" at the buried metal insulator steps.

To solve this problem, a redesign of the 8582 buried metal insulator (BMI) mask will be required. Note from Figure 2-2(a) that the ϕ_1 "bus" bar is continuous throughout its length. This observation is significant since the bus bar is a buried metal strip to which the ϕ_1 surface metal is mated. The uniform success of this contact provides the mechanism for the revision of the insulator mask. It is only necessary to extend the insulator over the entire chip so that a common BMI will exist for both the 9-bit and 2-bit devices. At those points where contact is required, an opening or "window" through the BMI is easily provided. This change in the BMI will provide not only acceptable yields for the 9-bit device but will also give a thicker field oxide to support the various clock lines/pads of the structure. As a consequence, the successful application of floating clock detection of the CCIRID output becomes feasible.

This revision will then ensure viable 9-bit CCIRIDs using current processing procedures. For long term development of a CCIRID process, however, it is desirable to eliminate any recurrence of microcracks at critical steps in the multilevel structure.

To accomplish this goal, an internally funded effort is now in progress to remove all steps in the fabrication sequence which are defined by the techniques of reverse photolithography. This improved process will then be applied to both the revised 8582 structure and to the next generation CCIRID to be designed during the next contract. Until such time that this development is complete, the revised BMI mask will enable successful processing of the 8582 9-bit CCIRID with the extant fabrication procedure.

CCD PERFORMANCE: 2-BIT AND 9-BIT DEVICES

Despite the fabrication problems discussed above, completely functional 2-bit devices from the 8582 chip have been achieved and operated. The performance of these devices will be described in the following paragraphs in conjunction with comments on the measurement techniques used in operating the structures. In addition to this success, some optical response has been observed for the 9-bit CCIRID on the 8582 chip. Although the device was not completely ac functional, the observation that light sensitivity was controlled by the transfer gate (ϕ_T) bias is encouraging and a milestone for future CCIRID measurements. The details of this sensitivity will likewise be described below.

A completely functional device is characterized by the fact that the device output exhibits the proper delay — in time — relative to the input point. For the ideal 2-bit structure with electrical input, this definition means that the output should appear two clock periods after the input pulse. This behavior was achieved for the 8582 2-bit structures (Figure 2-1 defines the pads for the 2- and 9-bit devices) by operating them as 4-phase (4ϕ) devices with a discrete gated charge integrator for the detection of the output charge. For convenience, the system clocks (ϕ_1, ϕ_2, ϕ_3, ϕ_4) were operated at a frequency of 10 kHz with variable rise and fall times used on the (ϕ_1, ϕ_3) clocks. Device operation with these capabilities on the (ϕ_2, ϕ_4) clocks was prevented due to a vendor delay in the delivery of two additional pulse generators. The timing relationship of all clocks used for the devices is shown in Figure 2-4. The bias levels of the available generators allowed a 20-volt swing on the clock magnitudes in conjunction with a 10-volt offset capability. To achieve the simplest operating mode for the device, the output surface gate (ϕ_{OS}) of the device was connected to the ϕ_1 clock line. The performance herein described is thus that for a 2-1/4-bit device rather than a 2-bit structure. As a result, the number of transfers for a charge packet through the device is N = 9 compared with 8 transfers for the 4ϕ, 2-bit structure.

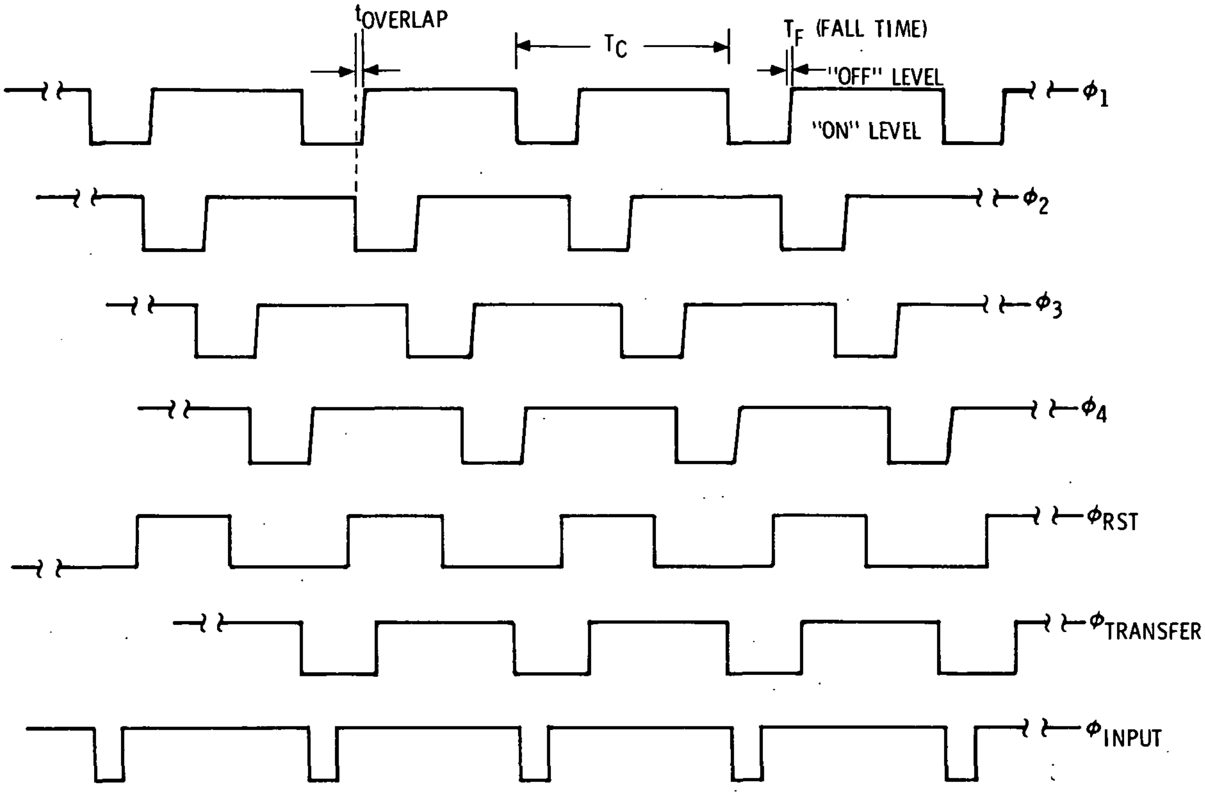


Figure 2-4. Typical Clock Waveforms for 4ϕ 8582 2-Bit and 9-Bit Charge-Coupled Devices

For the electrical input of charge into the CCD register, the method illustrated by Figure 2-5 was used. Two dc power supplies established the bias levels for the input diode (V_{INDC}) and the input buried gate (V_{IB}). A pulse generator was then used to apply the signal waveform (ϕ_{SIG}) to the input surface gate. The different bias levels (V_{INDC}, V_{IB}, ϕ_{SIG}, ϕ_1) yield surface potentials which, when properly set, are related as in the figure. No charge is input when ϕ_{SIG} is off (ϕ_{S1}) provided that

$$|\phi_{S1}| < |\phi_{SD}|$$

where ϕ_{SD} is the bias of the input diode. When ϕ_{SIG} is pulsed to "ON" position, then the surface potential under ϕ_{SIG} changes to ϕ_{S2} where

$$|\phi_{S2}| > |\phi_{SD}|$$

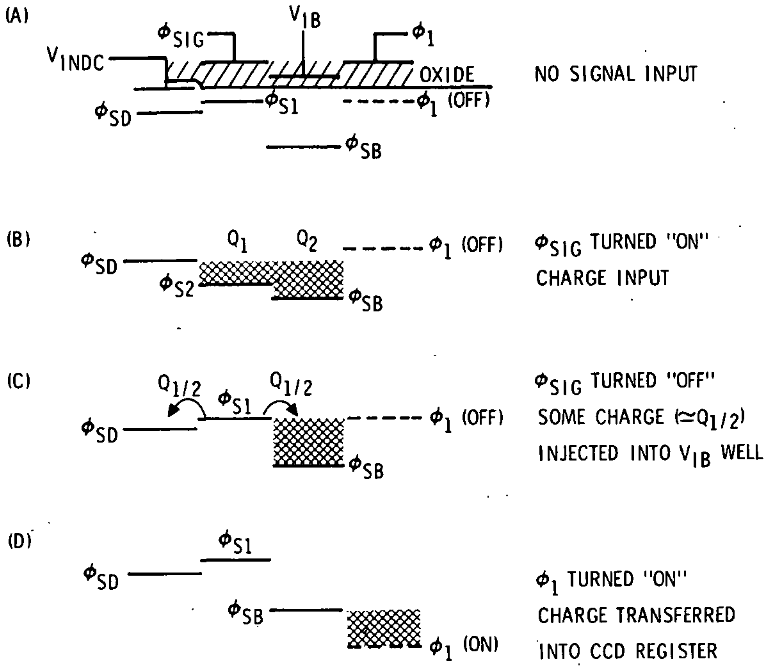

(A)
V_{IB}
ϕ_{SIG}
ϕ_1
V_{INDC}
OXIDE
NO SIGNAL INPUT
ϕ_{SD}
ϕ_{S1}
ϕ_1 (OFF)
ϕ_{SB}
(B)
Q_1
Q_2
ϕ_1 (OFF)
ϕ_{SIG} TURNED "ON"
CHARGE INPUT
ϕ_{SD}
ϕ_{S2}
ϕ_{SB}
(C)
$Q_{1/2}$
ϕ_{S1}
$Q_{1/2}$
ϕ_{SIG} TURNED "OFF"
ϕ_{SD}
ϕ_1 (OFF)
SOME CHARGE ($\simeq Q_{1/2}$)
INJECTED INTO V_{IB} WELL
ϕ_{SB}
(D)
ϕ_{S1}
ϕ_{SD}
ϕ_1 TURNED "ON"
ϕ_{SB}
CHARGE TRANSFERRED
ϕ_1 (ON)
INTO CCD REGISTER

Figure 2-5. Input of Charge Into 8582 CCD Register

Since V_{IB} is such that

$$|\phi_{SB}| > |\phi_{S2}|$$

it follows that charge will be injected from the diode until the surface potentials under the surface and buried gates are equivalent to ϕ_{SD}. Identifying C_s and C_B as the capacitances/unit area for the surface and buried gates respectively, the magnitude of this charge is given by

$$Q_{input} = C_s (\phi_{S2} - \phi_{SD}) + C_B (\phi_{SB} - \phi_{SD}) = Q_s + Q_B$$

As ϕ_{SIG} pulses back to V_1, a portion ($\simeq$50%) of Q_s is reinjected into the diode while the remainder spills over into the V_{IB} well. This action then gives the net input charge by this technique as

$$Q_{net} \simeq Q_B + Q_s/2 \tag{2-1}$$

The disadvantages of this approach are obvious in that 1) the spill over of Q_s introduces uncertainty into the value of Q_{net}, and 2) Q_{net} is only weakly dependent on the surface potential (ϕ_{S2}) resulting from the input gate. This latter feature makes the scheme unattractive for analog applications but, for the introduction of a fixed amount of charge, the technique is more than adequate.

A superior approach, similar to that proposed by Tompsett,[3] is the "fill-and-spill" technique. In this method, the input diode and the input buried gate are clocked while the surface gate is held at a dc bias. The proper control of these bias levels enables a low noise charge packet to be introduced into the CCD register. Since the size of the packet is directly proportional to the well depth created by the signal pulse, this technique is ideally suited for analog applications as well as digital. The application of the fill-and-spill technique is now planned as the routine mode for electrical input on future devices. But the added complexity of the extra clock made the approach less attractive for initial testing of the InSb CCD structures than the technique described above. Subsequent to the successful operation of the 2-bit devices, it was then decided that the fabrication and operation of the 9-bit CCIRID was of greater import than trying out this alternate input scheme. No results for the fill-and-spill approach, therefore, are presented at this time.

The input scheme used was nevertheless more than sufficient for successful operation of the 2-bit CCD structure. The signal output with proper 2-bit delay for one of these devices is shown in Figure 2-6(a) and (b) for one and six input pulses, respectively. The typical operating bias levels for this operation — in volts relative to InSb substrate — were:

ϕ_1: -5 to -11; ϕ_2: -2.8 to -6.6; ϕ_3: - 8.3 to -12.3; ϕ_4: -2.9 to -5.6
ϕ_{input}: -4.5 to -10.5; ϕ_{OB} = -6.0; ϕ_{IB} = -5.0; V_{INDC} = -1.0; V_{CS} = -0.9
Fall times ϕ_1, ϕ_3 clocks: 20 μsec

where all symbols are identified in Figure 2-1. In the case of the single input pulse, the initial and succeeding pulses are here designated as A, B, C . . . with A being the main pulse while B, C . . . are the trailing signals.

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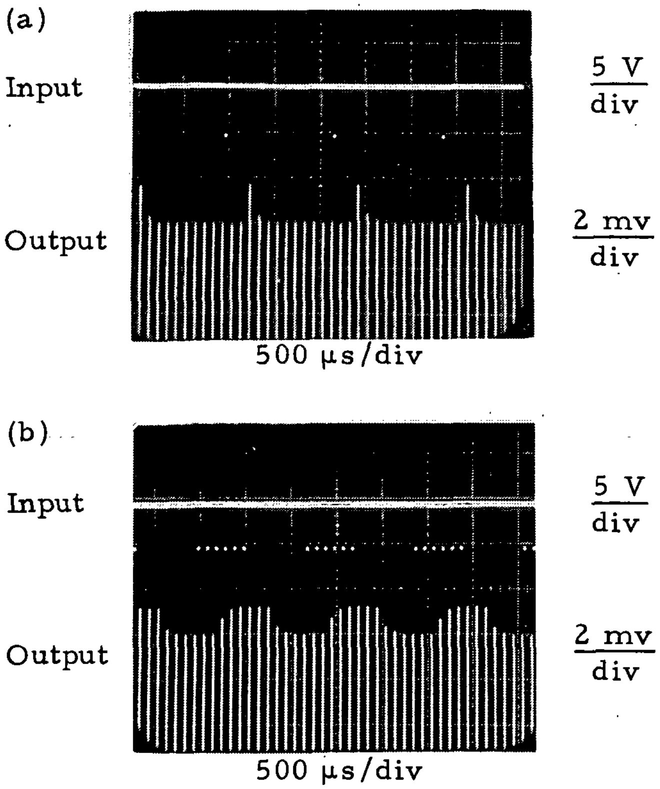
[3] M. F. Tompsett, "Surface Potential Equilibrium Method of Setting Charge in Charge-Coupled Devices," IEEE Trans. Electron. Devices, V. ED-22, p 305 (1975).

Their existence is due entirely to the transfer inefficiency (ϵ) of the CCD. It may be shown that ϵ is related directly to the values of A and B through the relation

$$N\epsilon = B/A \tag{2-2}$$

where N is the number of transfers for a charge packet through the device. As observed previously, the value N = 9 is appropriate for the 8582 structure as operated here.



f_c = 10 kHz
4ϕ Clocking
ϕ_{INS} Input
T = 77°K
0° FOV

Figure 2-6. InSb CCD Output Waveform, 2-Bit, 4ϕ CCD

To obtain the values of A and B, the output pulse magnitudes were measured, under a microscope, to the nearest one-hundredth of an inch with the measurement uncertainty being one-half of this value. The principal values obtained in this manner were as follows:

	First Pulse	Second Pulse	Third Pulse
A	20.0 ± 0.5	19.5 ± 0.5	20.0 ± 0.5
B	4.0 ± 0.5	3.5 ± 0.5	4.0 ± 0.5

from which the averages

$$A_{avg} \quad 19.8333 \pm 0.5$$
$$B_{avg} \quad 3.8333 \pm 0.5$$

are obtained. Using equation (2-2), these values then yield

$$\epsilon \simeq 0.0214$$

or, for the transfer efficiency ($\alpha = 1 - \epsilon$),

$$\alpha \simeq 0.9785 \qquad (2\text{-}3)$$

This value is to be compared with the predicted value of $\alpha = 0.99$ which appears in Figure 2-7. The analysis leading to the data in this figure was discussed extensively in the final report[2] of the prior contract, and it need not be repeated here. It is important to note, however, that the well depth parameter ΔV in the figure was assumed to be 2 volts for the predicted efficiency. In the present case, however, the data indicate that $V = 1$ volt is the more appropriate value. If the computations leading to the figure are repeated for this smaller size for ΔV, then the predicted value for α drops to 0.983, which agrees even more closely with the measured value quoted above. This agreement is important since it lends considerable support to the reliability of the other predictions listed in the figure.

The efficiency for the case of multiple input pulses is more difficult to obtain than for the single input case. For this type of input, the first charge packet into the device may suffer considerable loss to traps (e.g., interface states) as it transfers through the CCD register. The next packet will suffer less loss and subsequent packets still less until a steady-state output pulse is attained. At this point, all remaining packets in the pulse string will undergo the same loss to the device. After the final packet has emerged from the device, then the trailing packets begin to appear. These packets are composed

GATE LENGTH (μm)	WELL DEPTH (volts)	INTERFACE STATE LOSS	EFFICIENCY (α)
50	0.5	9.36×10^{-2}	0.90
25	2.0	9.64×10^{-3}	0.990
13	2.0	2.51×10^{-3}	0.997
7.5	2.0	9.11×10^{-4}	0.999
$f_C = 5$ kHz; $\tau_S = 5 \times 10^{-6}$ sec; NO FRINGE FIELD; 4Φ CLOCK MODE (a)			

Figure 2-7. Calculated Transfer Efficiency Versus Gate Length for InSb CCD

of the charge lost by those packets (the leading pulses) which precede the steady-state pulse train. The transfer inefficiency for the device with this multiple input structure is then obtained either from these leading pulses or the trailing pulses in conjunction with the steady-state pulse magnitude. The details of the required analysis may be found in the previous[2] final report. It is sufficient here to recall that these techniques require the measurement of all the leading pulse magnitudes and/or all of the trailing pulse magnitudes. The large number of the requisite measurements evidently increases the probability of error being introduced into the calculation. In addition, it is sometimes difficult to distinguish a leading pulse from a steady-state pulse. These factors each contribute to an added uncertainty in multiple pulse measurements not found in the single pulse technique. Nevertheless, the values obtained by these methods generally agree closely ($\alpha \simeq 0.965$) with the single pulse results.

In summary, the 2-bit, 1-mil gate length CCDs analyzed during this contract exhibited transfer efficiencies in close agreement with the values predicted on the basis of previous work. The measured value of $\alpha = 0.975$ for the device is a significant improvement over the values obtained for the 2-mil (8580) gate-length device. With these results, the design and fabrication of 0.5-mil gate-length structures is expected to provide transfer efficiencies of approximately 0.999 during the next contract period.

The operation of completely functional 9-bit CCIRIDs has not been achieved as of this writing. The reasons for this failure have already been discussed with the principal mechanism being the breaking of the surface metal clock lines at the buried metal insulator step. However, a milestone has been achieved with the observation of optical sensitivity in the CCIRID which was controlled by the transfer gate (ϕ_T) pulse.

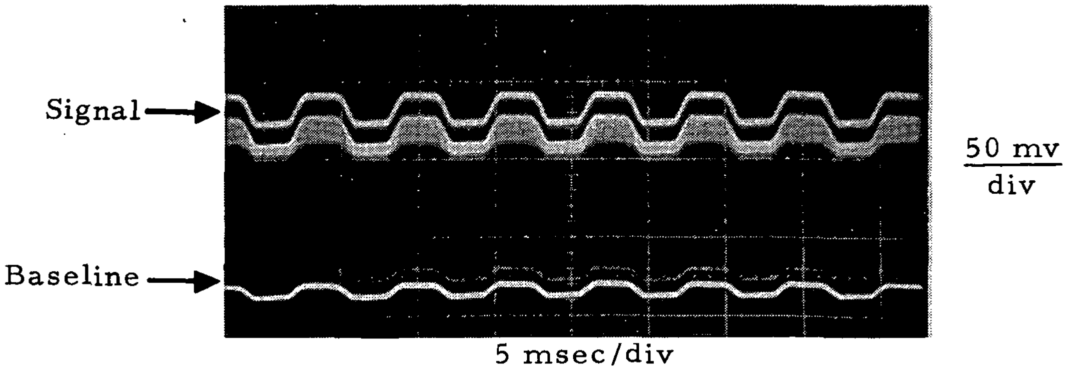
Optical measurements of the CCIRID are carried out in a variable background dewar with the requisite cooled field-of-view (FOV) restrictions. Provisions are also available for using cooled neutral and/or spectral density filters during device response measurements. These features ensure that the optical data obtained are accurate and reliable. Inside the dewar, a mounting fixture for the InSb CCIRID has been designed. This fixture contains space for the installation of monolithic silicon chips alongside the InSb device. These chips possess fully integrated source-follower and reset circuits for the detection of CCD output charge. Since the capacitance of these circuits is much less than that achievable with the discrete MOSFET circuits used with the 2-bit structures, the voltage swing for a given charge packet will be larger than those observed for the discrete circuits. This mounting scheme also allows, with only minor modifications, a conversion to floating clock detection rather than floating diffusion detection. The distinction of these is discussed in Section 4. For now it is sufficient to note that the floating clock technique appears to offer sensitivity and reliability advantages over the floating diffusion approach.

Using this dewar and fixture assembly, some optical sensitivity of the 9-bit CCIRID has been observed. To achieve this sensitivity, the device was cooled to 77°K, and then exposed to chopped (300-Hz) blackbody (T = 500°K) radiation. The bias levels for the InSb and silicon devices were set as

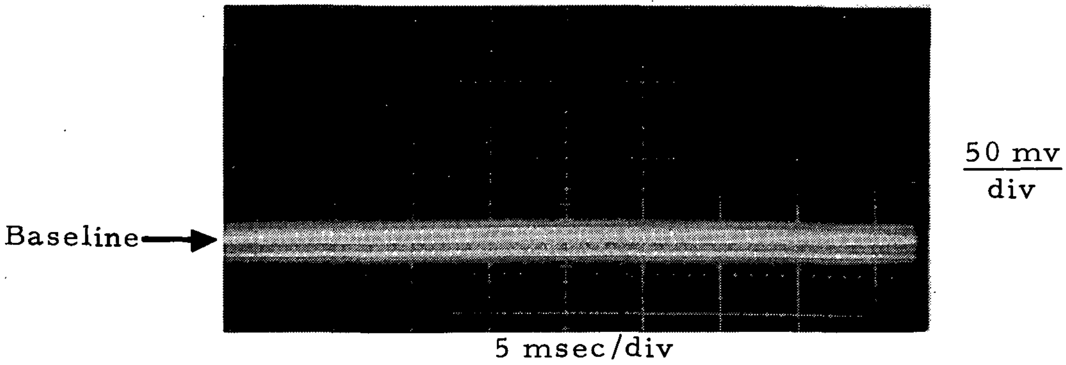
InSb (volts)		Silicon (volts)	
V_{INDC} = 0.0;	Substrate = 0.0;	Substrate	+5.0
V_{CS} = 0.5;	ϕ_{OB} = 0.0;	V_{DD}	-1.0
ϕ_{IB} = 0.0;	ϕ_P = 5.0;	V_{SS}	+10.0
ϕ_T = 0 → -3;	ϕ_1, ϕ_3 = -5 → -11;	ϕ_{RST}	+0 → +5.0
ϕ_2, ϕ_4 = -1 → -4			

The results of these operating values are shown in Figure 2-8(a) and (b). In part (a), the output signal representative of the chopped blackbody is clearly indicated. For part (b) of the figure, the peak to peak swing of ϕ_T was reduced to 0 volts. This action prevents creation of a channel from the photosensors to the CCD readout registers. No charge can, therefore, be transferred from the sensors and the output charge vanishes. The realization of this predicted behavior is clearly seen in Figure 2-8(b) where the signal of (a) is totally eliminated. Actual control by the ϕ_T gate was indicated by the fact that the transition from (a) to (b) exhibited a sharp cutoff when the ϕ_T amplitude decreased to a 0 to -1 volt swing.

This success can be considered only marginal, however, since the sensitivity to the photogate bias (ϕ_P) was very slight while the effect of the output buried gate (ϕ_{OB}) bias was even less. Similarly, the output waveform was insensitive to the CCD register clocks (ϕ_1, ϕ_2, ϕ_3, ϕ_4) to such an extent that the device output could not be eliminated by varying these clock amplitudes. And finally, the end of the test sequence for the device was marked by the apparent shorting of ϕ_T to the InSb substrate. It may be that a high resistance connection existed between these two elements throughout the test. If this were so, then some of the observed sensitivity may have been due to the ϕ_T waveform being applied — through a resistance — to substrate. Each of these observations, then, dampens somewhat the enthusiasm for the observed optical sensitivity. The shape of the observed output waveform, however, is strongly suggestive of true detection of the chopped blackbody radiation. This fact, together with the undeniable control of the output by ϕ_T, is strong evidence that correct, albeit partial, operation of the CCIRID photosensor/transfer gate structure has been observed.



(a) Transfer Gate Turned "On"



(b) Transfer Gate Turned "Off"

Figure 2-8. Response of 8582 9-Bit Linear Imager to Chopped (300-Hz) Blackbody (500°K) Radiation

The results are extremely encouraging then for future tests of the 8582 CCIRID to be performed at the beginning of the next contract. At this time, the 8582 fabrication runs will also benefit considerably from the revised mask of the buried metal insulator level. This revision should eliminate almost entirely the metal breakage problem and result in completely viable 9-bit CCIRIDs. The sensitivity discussed above certainly indicates the ability of the transfer gate to shift photogenerated charged into the CCD register. The results of the new runs should confirm this indication and allow accurate measurements of the device D* and quantum efficiency.

DEVICE DESIGN

The confirmation of improvement in transfer efficiency with a reduction in gate length has now occurred. Although complete operation of the 9-bit imager still remains, this gate length effect emphasizes the need for an improved CCIRID design incorporating shorter gate lengths (0. 5 mil) as well as other improvements to enhance device operation. Notable among these latter features is the reduction in size of the input and particularly the output diode. This type of change will greatly increase the voltage swing on the diode for a given charge packet. In the discussion below, a proposed chip for the next generation InSb CCIRIDs is thus given; a proposal which includes those improvements deemed necessary and/or desirable.

The basic assumption is that each CCD on the chip will be a 4ϕ device with a gate length of 0. 5 mil and hence a bit length of 2 mils. To allow for the option of using a floating clock scheme for charge detection as well as the conventional gated charge integrating mode with a floating diffusion, there will be two output gates in analogy with the present 8582 design. Similarly, there will be two input gates so that the "fill-and-spill" input scheme is possible. These four gates effectively introduce an additional bit into the devices so that an M-bit CCD has a length of

$$2\ (M + 1)\ \text{mil}$$

where 2 mils/bit is assumed. For the input, output diodes, an area of approximately

$$2 \times 2\ (\text{mil})^2$$

is assumed, a factor of 17 smaller than the area of the present diodes on the 8582 die. For sensor size, it is assumed to be approximately

$$2 \times 2\ (\text{mil})^2$$

as well, while the channel width of the CCD is approximately 8 mils.

If these assumptions for size are combined with allowances for pad and line spacing, then device sizes can be obtained for different structures. In particular, it is considered feasible to include, on a single chip: 1) a 20-element linear imager with 0.5-mil gates and 1-bit/sensor; 2) a 2-element linear imager with 0.5-mil gates and 2-bits/sensor; 3) a 4-element time delay and integration (TDI) array with 0.5-mil gates; 4) a 4-element linear imager with 7.5-μm gates and 1-bit/sensor; 5) a composite of amplifiers for gated charge integration and/or floating clock "on-chip" charge detection; and 6) test structures for characterization of device parameters. This comprehensive package of devices is desirable, but it does require a considerable increase in chip area.

An indication of this is given in Figure 2-9 where one possible layout of this chip is given. Note that the overall chip size is 110 × 120 $(\text{mil})^2$ as compared with 80 × 80 $(\text{mil})^2$ for the 8582 design. For the wafer areas available for InSb, this increase in area will yield a corresponding decrease in total die per wafer from approximately 80 to 40. It follows from this that processing yields will have to improve for a reasonable number of functional die to be achieved. A careful design of the various devices, taking cognizance of fabrication capabilities, should enable this requirement to be satisfied.

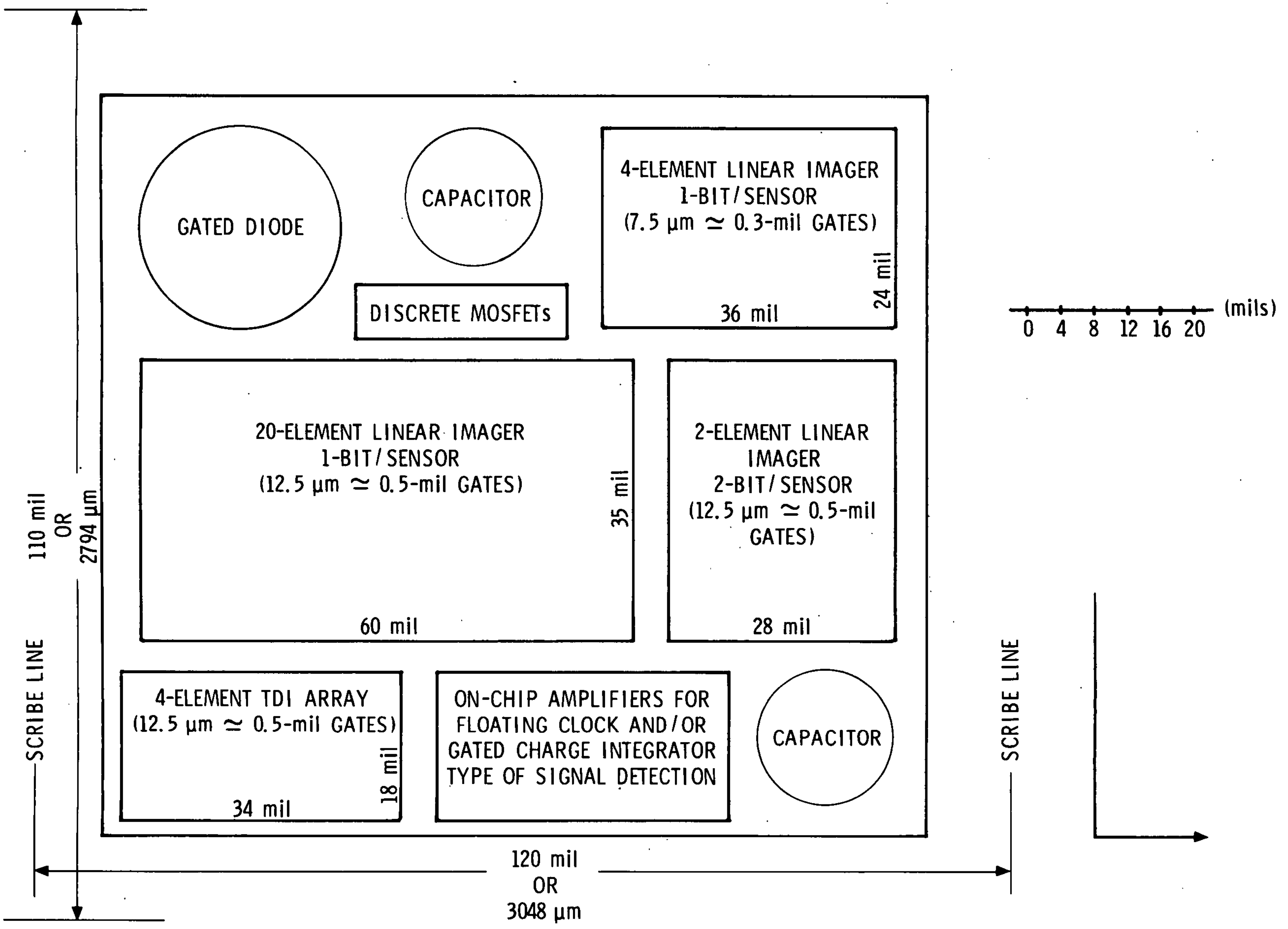

GATED DIODE
CAPACITOR
DISCRETE MOSFETs
4-ELEMENT LINEAR IMAGER
1-BIT/SENSOR
(7.5 μm ≃ 0.3-mil GATES)
24 mil
36 mil
(mils)
0 4 8 12 16 20
20-ELEMENT LINEAR IMAGER
1-BIT/SENSOR
(12.5 μm ≃ 0.5-mil GATES)
35 mil
60 mil
2-ELEMENT LINEAR
IMAGER
2-BIT/SENSOR
(12.5 μm ≃ 0.5-mil
GATES)
28 mil
110 mil
OR
2794 μm
SCRIBE LINE
4-ELEMENT TDI ARRAY
(12.5 μm ≃ 0.5-mil GATES)
18 mil
34 mil
ON-CHIP AMPLIFIERS FOR
FLOATING CLOCK AND/OR
GATED CHARGE INTEGRATOR
TYPE OF SIGNAL DETECTION
CAPACITOR
SCRIBE LINE
120 mil
OR
3048 μm

Figure 2-9. Schematic of Proposed Chip for InSb CCD for Use in Infrared Imager Development

Section 3

DEVELOPMENT OF CCD COMPUTER MODEL

A computer model for a 4ϕ, overlapping gate CCD was developed during this contract. The purpose of the development was to provide a viable means for identifying critical parameters and their values for optimum design characteristics for a CCD. The choice of a 4ϕ CCD for modeling was dictated by the fact that the current device designs for InSb CCIRIDs are 4ϕ devices. The choice is not a limitation, however, since conversion of the 4ϕ to a 3ϕ or 2ϕ system is straightforward.

DESCRIPTION OF MODEL

The existence of this model provides the capability of full design optimization for future InSb CCIRID structures. The model reduces the 4ϕ CCD to a unit cell composed of the four basic gates (V1, V2, V3, V4) which comprise the "bit length" of the structure. By considering the cell as shown in Figure 3-1, it may be seen that the center of a surface gate (V1) is used as the symmetry point for the structure. If a series of N cells such as these are matched at the gate centers, then a 4ϕ CCD of N bits is obtained. Hence, a general treatment for a CCD is obtained from the behavior for a single unit cell. Note that a specification of definite depletion regions in the figure implies that the depletion approximation[4] is used in this model.

This model treats the CCD under static conditions. There is thus no explicit time dependence of the system clocks or of charge density present in this analysis. The model does provide, however, the two-dimensional potential profiles for the device structure from which the charge storage capacity, fringe field coupling strengths, and optimum design parameters values can be obtained. As an example, the results of the model for different gate insulator thicknesses can be used to choose the value for this parameter which will ensure maximum fringe field coupling.

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[4] J. McKenna and N. L. Schryer, "The Potential in a CCD With No Mobile Minority Carriers," BSTJ 52, p 1765 (1973).

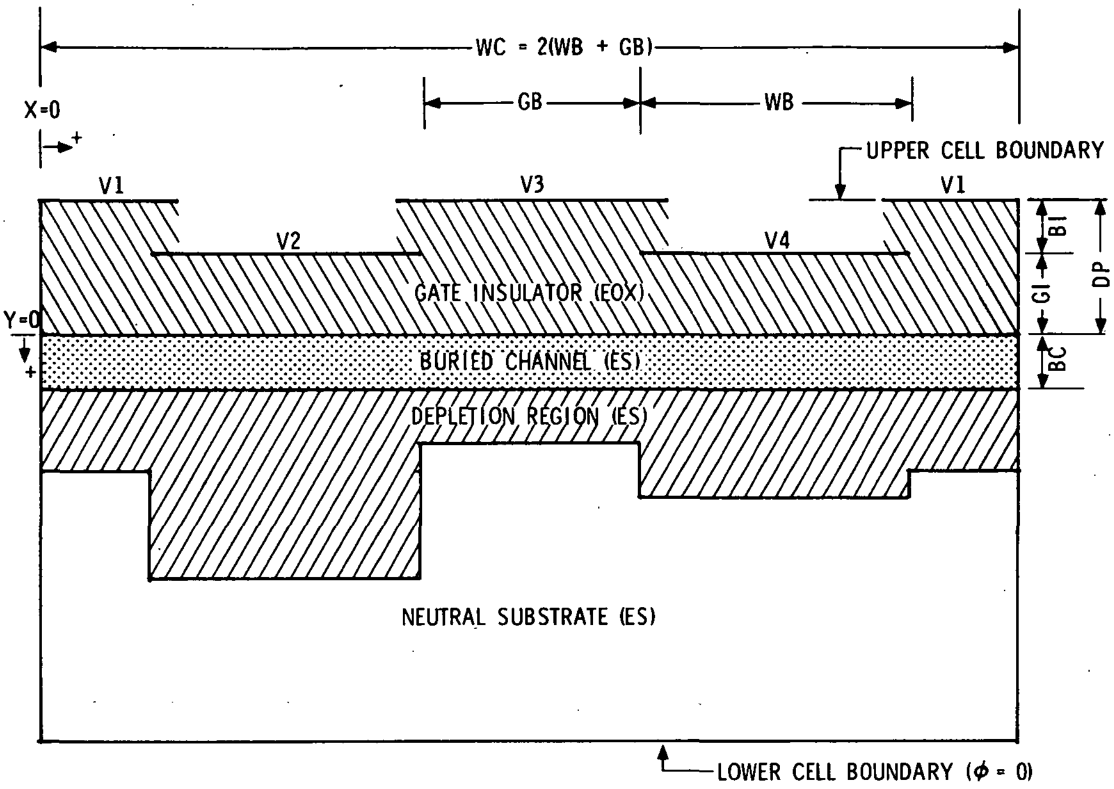

WC = 2(WB + GB)
GB
WB
X=0
+
UPPER CELL BOUNDARY
V1
V3
V1
V2
V4
BI
GI
DP
BC
Y=0
+
GATE INSULATOR (EOX)
BURIED CHANNEL (ES)
DEPLETION REGION (ES)
NEUTRAL SUBSTRATE (ES)
LOWER CELL BOUNDARY (ϕ = 0)

Figure 3-1. Unit Cell for 4ϕ Computer Model

The model considers as parameters the quantities shown in Table 3-1. The quantities listed in parenthesis in this table indicate the units required for the parameters as input for the model. These requirements must be observed since the program converts all data to units of volts, centimeters, and seconds. As a result, the computed results yield potentials and electric field strengths directly in units of volts and volts/cm.

The basic content of the model is the application of Poisson's equation:

$$\nabla^2 \phi = -\rho/\epsilon \qquad (3-1)$$

to the unit cell of Figure 3-1. Here ϕ (X, Y) is the potential function for points on and inside the boundary of the cell. The parameter ρ (X, Y) is the charge density while ϵ (X, Y) is the permittivity at the point (X, Y). To solve equation (3-1), the unit cell is broken into a mesh of points with a typical point labeled by a pair of integers (i, j). The equation is then solved at these points by utilizing a five-point finite difference approximation to the Laplacian operator (∇^2) in the above.

Table 3-1. Parameters Used in 4ϕ Computer Model

Symbol	Parameter
V1, V2, V3, V4	Gate Voltages (volts)
GI	Insulator Thickness for Buried Gates (μm)
DP	Insulator Thickness for Surface Gates (μm)
WB	Width of Buried Gates (μm)
GB	Gap Between Buried Gates (μm)
BC	Channel Depth for Buried Channel Device (μm)
N_{SUB}	Substrate Doping Density (× 10^{13} cm^{-3})
N_{SS}	Fixed Interface Charge Density (× 10^{10} cm^{-2})
NC	Charge Density for Buried Channel (× 10^{12} cm^{-2})
ES, EOX	Permittivities of Substrate (InSb) and Gate Insulator

In this approximation, equation (3-1) takes the form:

$$\overbrace{\left[\frac{h_i \phi_{i+1,j} + h_{i+1}\phi_{i-1,j}}{h_i h_{i+1}(h_i + h_i + 1)}\right]}^{\phi_H} + \overbrace{\left[\frac{V_{j-1} e_1 \phi_{i,j+1} + V_j e_2 \phi_{i,j-1}}{V_j - 1\ V_j(V_j - 1 + V_j)}\right]}^{\phi_V}$$

$$- \underbrace{\left[\frac{\phi_{i,j}}{h_i h_{i+1} V_j V_{j-1}(h_i h_{i+1} + V_j V_{j-1})}\right]}_{HR} = \frac{-\rho_{i,j}}{\epsilon_{i,j}} \qquad (3\text{-}2)$$

which can be solved for $\phi_{i,j}$ to yield

$$\phi_{i,j} = HR \left[\phi_H + \phi_V + \frac{\rho_{i,j}}{\epsilon_{i,j}}\right] \tag{3-3}$$

In these expressions, the notation is

(i, j) = location on X, Y mesh
$\phi_{i,j}$ = value of potential ϕ at i, j
H_i = $X_{i+1} - X_i$, $V_j = Y_{j+1} - Y_j$
X_i, Y_j = values of X, Y at mesh points (i, any j) and (any i, j) respectively with X(1) = 0.0 and Y(1) = -DP (see Figure 3-1)
$\rho_{i,j}$ = value of charge density at i, j
$\epsilon_{i,j}$ = value of permittivity at i, j

The parameters e_1, e_2 are unity except at boundaries where the permittivity changes. Their appearance is thus dictated by the boundary conditions of this system.

To obtain the values $\phi_{i,j}$ from equation (3-3), an iteration approach is used with initial conditions for $\phi_{i,j}$ being obtained by treating the gates V1, V2, V3, V4 as simple MOS capacitors. The potential under these gates can then be solved exactly and the resultant values used in initializing $\phi_{i,j}$. This technique obviously breaks down near the gate edges, but these values give the best initial approximation to the two-dimensional solution. An additional advantage of this initialization procedure is that the depletion width appropriate to each gate can be computed and used in the calculation. This situation is to be compared with conventional treatments in the depletion approximation wherein an average depletion is used for all gates. Once the $\phi_{i,j}$ is initialized, an iterative convergence scheme is used to obtain the correct $\phi_{i,j}$ values for the two-dimensional cell. This scheme basically: 1) computes a new $\phi_{i,j}$ value using the present conditions at the neighboring points $\phi_{i\pm1,j}$ and $\phi_{i,j\pm1}$; 2) compares this new value with the value before the iteration; and 3) stores the difference between the values. This process is then repeated for all mesh points in the cell and, upon completion, the differences obtained from step 3) are compared with a preset criteria value for convergence. If none of the differences exceeds this value, then a solution of equation (3-1) has been found. Otherwise, the iteration sequence begins again using the results of the latest iterative computation.

The time required for convergence by this approach is a function of the: 1) number of mesh points, 2) boundary conditions, and 3) initial conditions. Of these, the boundary conditions are set by the physical requirements of the CCIRID design. The number of mesh points is a function of the accuracy desired and the overall cell dimensions. Evidently, a compromise is required between the accuracy desired and the time required to achieve it. For the data reported below, the compromise was such that the surface potentials (value of ϕ (X, Y) along insulator-substrate interface) satisfy equation (3-1) to an accuracy of 3 mv. Such accuracy is more than sufficient for the selection of optimum parameter values, the goal of this model development. Finally, the choice of initial conditions has already been discussed above.

In specifying the model, it is essential that the boundary conditions used be presented. The conditions utilized in the present model are:

1. Surface gates V1, V3 specified and held fixed;
2. Region between surface gates on the upper cell boundary (Y = -DP) held at zero volts;
3. Buried gates V2, V4 specified and held fixed;
4. Substrate (lower cell boundary) held at zero volts; and
5. Potential at left boundary of cell (X = 0) must equal value at right boundary (X = WC), a condition resulting from the assumed device symmetry.

These conditions, in conjunction with equation (3-1) and the specified iterative sequence, result in a solution [in the form of a set of mesh point values $(\phi_{i,j})$] for the potential function of the unit cell. From this set of values, the surface potential is obtained directly for surface channel structures. The electric field along this interface is then computed using

$$E_{i,j} = -\frac{h_i\, \phi_{i+1,j} + (h_{i+1} - h_i)\, \phi_{i,j} - h_{i+1}\, \phi_{i-1,j}}{2\, h_i\, h_{i+1}} \qquad (3\text{-}4)$$

For completeness, note that this model is also applicable to buried channel structures. It follows that the parameters for such structures can be obtained in future contracts when and if it becomes desirable to fabricate buried channel CCIRIDs.

SAMPLE CALCULATIONS

As examples of the data obtainable from the model, a number of cases are given in Figures 3-2 through 3-7. In Figure 3-2, the surface potential profile is given for a device with parameter values typical of those for the 8580 InSb CCD which was developed and tested under the previous contract. The tangential electric field strength (E_x) is also given in this figure. Charge transfer is from left to right in this and future figures (+X direction) so that this case is the profile predicted for transfer from gate V1 to the V2 storage well. The gate biases for this case are V1, V3 = -10 volts; V2 = -8 volts; and V4 = -6 volts. The most distinctive feature for the device (buried gate 62 µm ≃ 2.5 mil, surface gate length 38 µm ≃ 1.5 mil) is the total absence of a tangential field in and near the gate center. This fact confirms expectations for the 8580 device as cited previously in the final report.[2] As a result, it is quite evident that charge transfer in this device is limited strictly by diffusion processes.

The effect of substrate doping density is shown in Figure 3-3. These data are for the same 8580 structure as modeled in Figure 3-2 but with different substrate densities. The densities shown are (1) $N_{SUB} = 1 \times 10^{14}/cm^3$, (2) $N_{SUB} = 2.5 \times 10^{14}/cm^3$, and (3) $N_{SUB} = 1 \times 10^{15}/cm^3$. There is clearly no large effect on the surface potential shapes but rather only a progressive decrease in the magnitudes of the potential as N_{SUB} increases. This shift will become damaging for substrate dopings at which the surface potential becomes zero. At this point, there will be a rapid decrease in the storage capability of a well. This capability is approximately measured by the

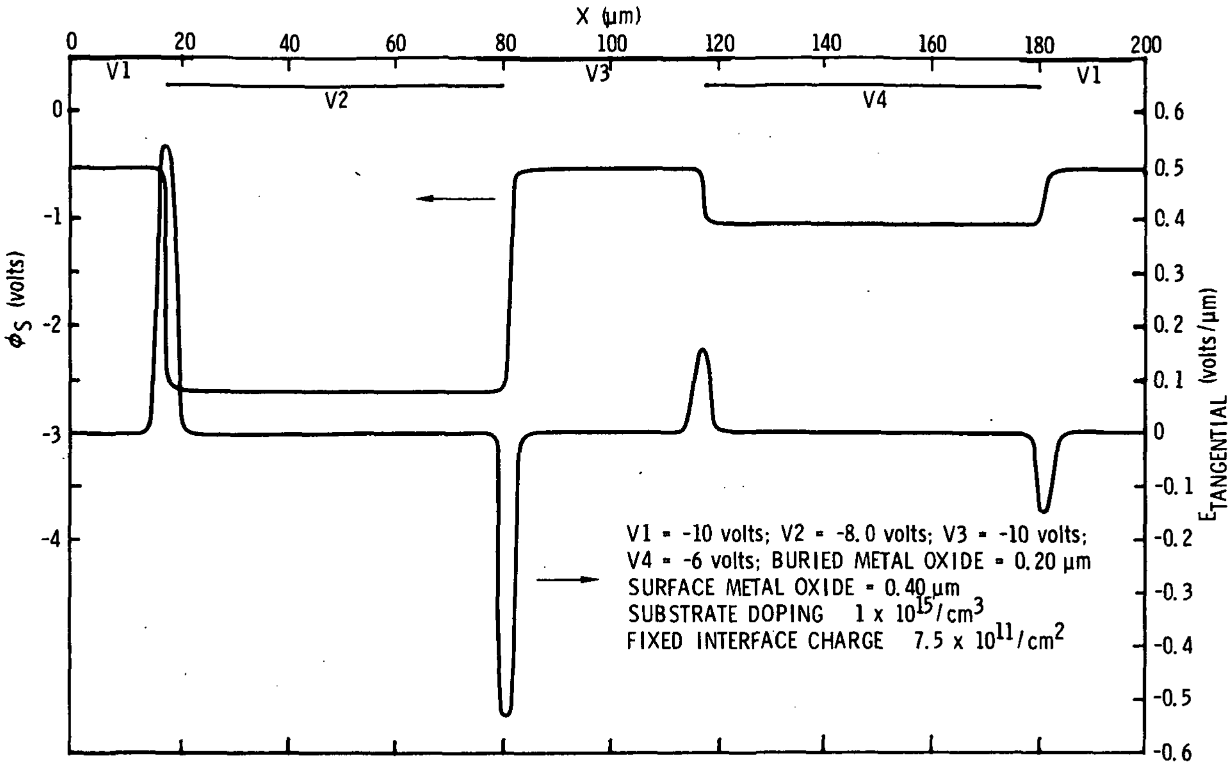


Figure 3-2. Potential Profile, Tangential Electric Field for 8580 Device

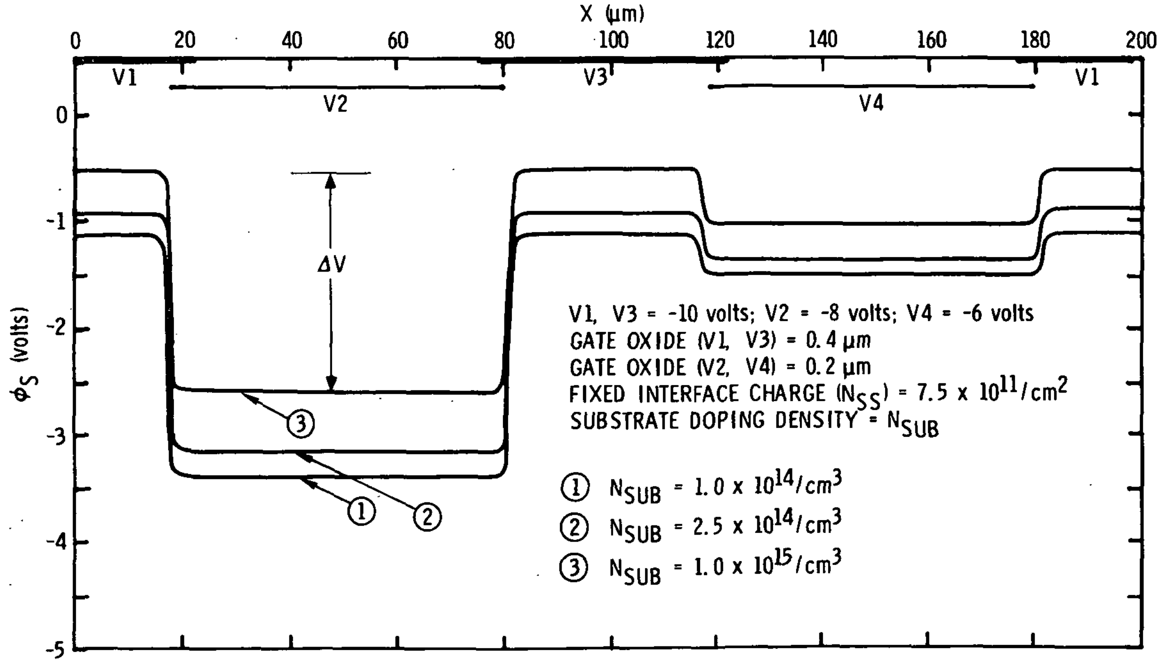


Figure 3-3. Potential Profiles for 8580 Device as a Function of Substrate Doping

parameter ΔV defined in Figure 3-3 for Case (3). If ΔV is measured for each of the cases in the figure and plotted as a function of substrate doping, the result is shown in Figure 3-4(a). The gradual decrease in ΔV is evident here with a shift of only 0.4 volt for a factor of 20 change in the substrate doping. This shift, though relatively small, will definitely impact charge storage in the device, and must be taken into account in the design and processing sequence. A similar variation is observed if a plot is made for the maximum tangential field as a function of N_{SUB} [Figure 3-4(b)]. This field occurs at the gate edges and, if it decreases, then charge transfer through the device becomes more and more dependent on pure diffusion. From the figure, it is clear that $|E_{tan}\ (\max)|$ changes by approximately 1000 volts/cm. Such a change may alter significantly the speed of charge transfer and must also be considered. Since both ΔV and the tangential field increase as the substrate doping is decreased, it is desirable to attempt fabrication of the InSb CCD on material doped less heavily than $1 \times 10^{15}/\text{cm}^3$, the level used thus far. Such a fabrication has been carried out for material with $N_{SUB} \simeq 2.5 \times 10^{14}/\text{cm}^3$, but adherence problems caused abortion of the run.

Although the results discussed above emphasize the effects of the gate lengths in the 8580 device, the model has also been used to predict profiles for the 8582 device, as well as two projected devices with 12-μm and 7.5-μm gates, respectively. The surface potential and tangential field for the 8582 device (26-μm gate length) is given in Figure 3-5. It is evident that, even with this shorter length, the tangential field is still effectively zero in the gate centers. But the field strength at the gate edge (gate 1, gate 2) increased to 1.05 volts/μm, up from a value of 0.52 volt/μm in the case of the 8580 device. This larger field at the edge will enhance charge transfer from the edge regions of the gates. As a result, the overall transfer of charge from gate 1 to gate 2, though still diffusion limited, is enhanced.

This effect is increased still further as the gate length is continuously decreased. For the cases considered here, the data are summarized in Figure 3-6. As this figure makes clear, the fringe field coupling between

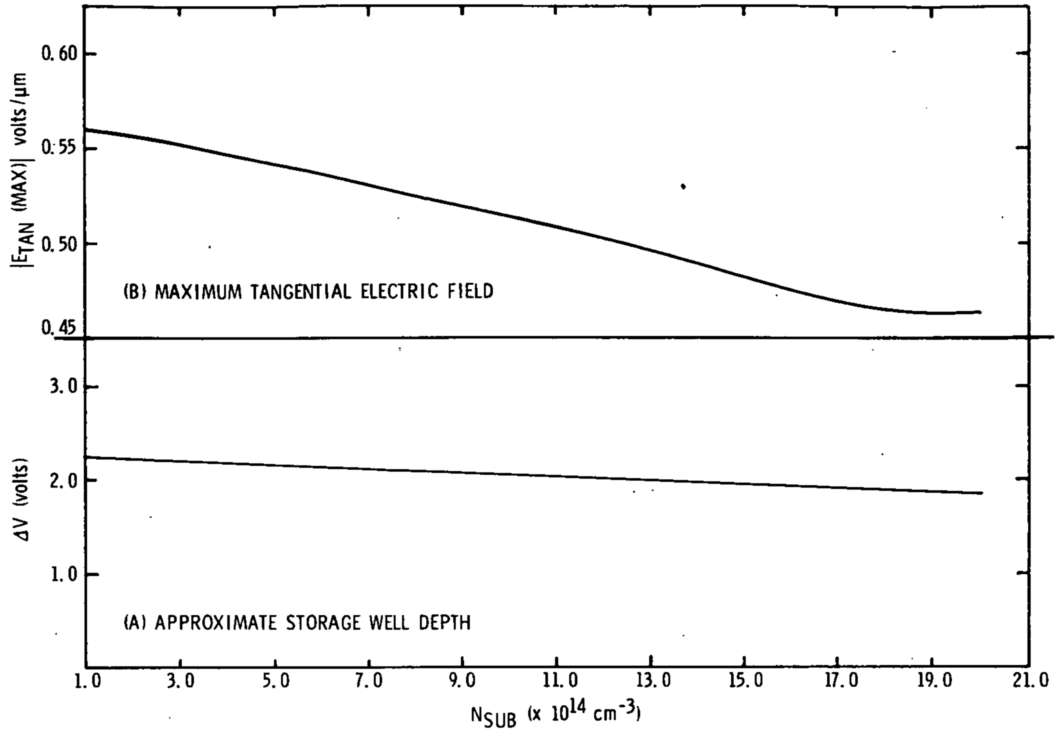


Figure 3-4. Effect of Substrate Doping Density on Storage Well Depth and Maximum Tangential Coupling Field (50-µm Gate Lengths)

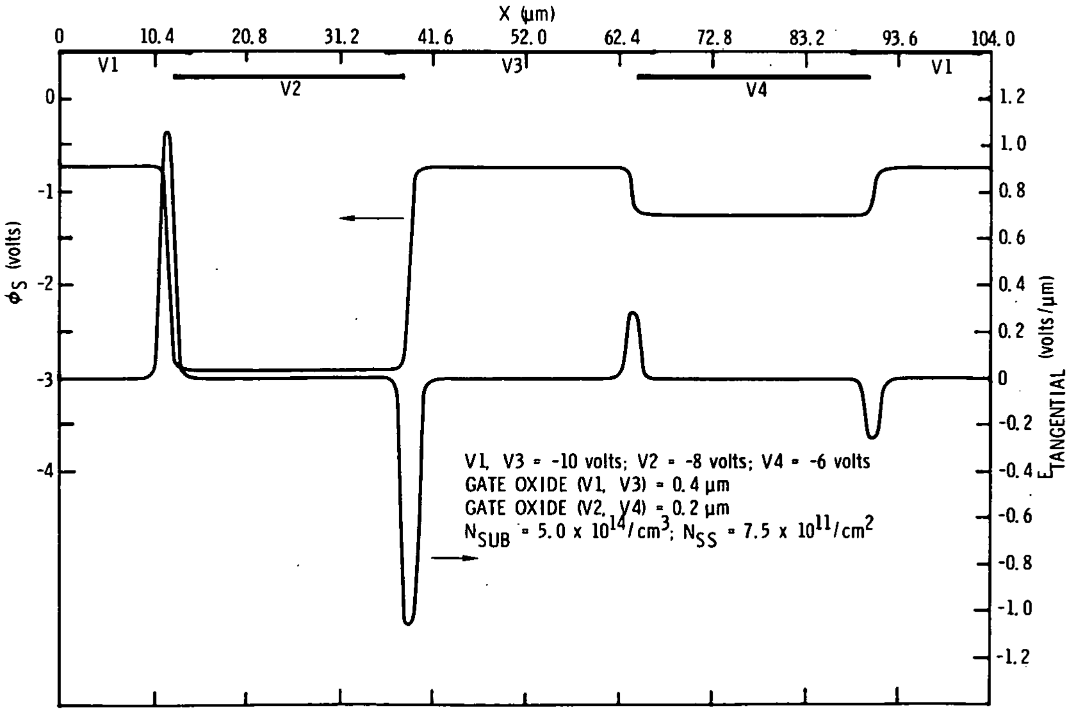


Figure 3-5. Potential Profile, Tangential Electric Field for 8582 Device

adjacent wells increases rapidly as the gate length becomes shorter than the 25-μm case represented by the 8582 device. The minimum tangential field also shows a marked increase with decreasing gate length. For the cases considered, the 12-μm and 7.5-μm structures exhibit minimum fields 4 and 7 orders of magnitude larger than the comparable fields of the 8580 and 8582 devices. It follows that the next generation InSb CCDs will possess considerably higher fringe fields than will be possible with the 8582. This fact alone will lead to an increased transfer efficiency relative to the presently designed devices.

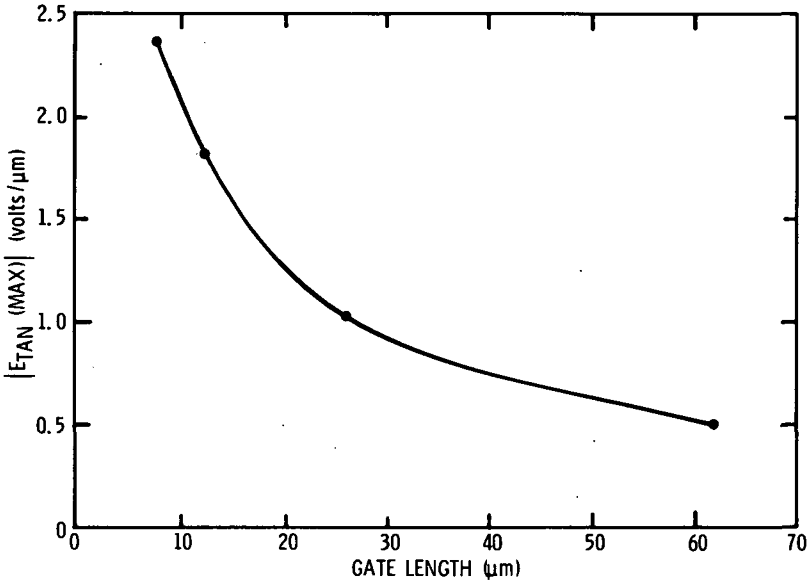


Figure 3-6. Maximum Tangential Electric Field as a Function of Device Gate Length

As is clear from Table 3-1, the model developed in this report period can treat the effects of fixed interface charge (Q_{SS}) as well as buried channel devices. The former case of Q_{SS} effects has been considered with the results being essentially a steady increase in surface potential magnitude as Q_{SS} is reduced. This behavior is illustrated by the results of Figure 3-7.

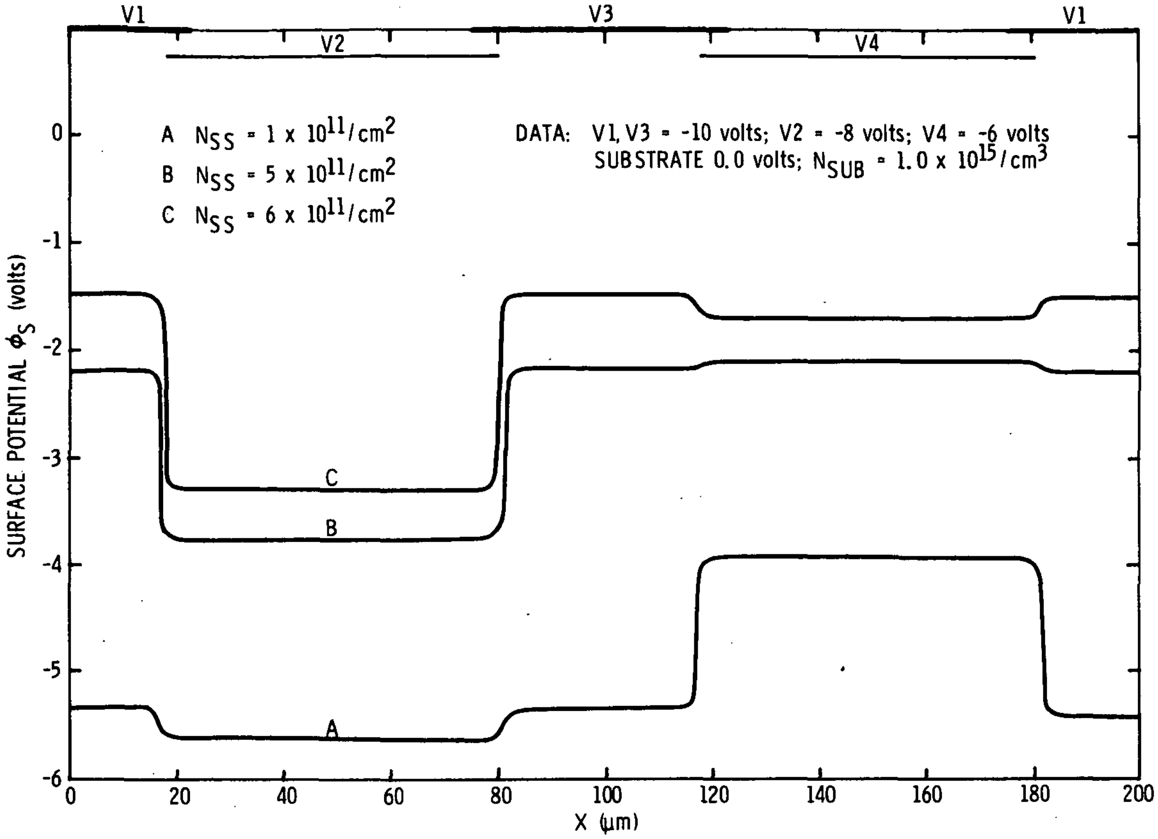


Figure 3-7. Surface Potential Profiles for 8580 Device as a Function of Fixed Interface Charge

No predictions for buried channel structures are given herein since the devices under development are surface channel. The model, however, is designed to accommodate buried channel devices; calculations for these structures can be carried out at any time. Not only the doping density of the channel but its vertical profile (e. g., Gaussian to represent implanted channels) can also be varied. As a result, the flexibility of this modeling effort is maximal.

In summary, a computer model for a 4ϕ CCD structure has been successfully developed. The existence of this model ensures that future designs, whether surface or buried channel, for InSb CCIRIDs will be undertaken with the maximum *a priori* knowledge of the critical parameter values.

Section 4

SYSTEMS CONSIDERATIONS

Applications of InSb CCIRIDs have been discussed in previous reports.[1, 2] In general, these applications can be classed in the two broad categories of 1) infrared imaging of the earth from orbiting observatories and/or satellites, and 2) infrared imaging of the outer planets via fly-by satellites such as the Mariner probes. The former class of studies can provide extensive earth resource information including the location and identification of mineral deposits, the location and mapping of forest fire activity, and the identification of some atmospheric pollutants. Outer planet infrared data will enable detailed studies of the planetary atmosphere. Identification of some atmospheric constituents as well as information on atmospheric dynamics can be obtained from such a program. If a satellite is placed in planetary orbit, then it is obvious that even more detailed investigations, such as complete infrared studies of the planetary surface, are feasible.

RESPONSIVITY AND THE MODULATION TRANSFER FUNCTION

To carry out these applications, it is first necessary to understand the limitations of the infrared sensors to be used. The CCIRID sensors of this effort are, of course, determined by the material characteristics of the InSb itself. Beyond this limitation, the detector design can also provide serious constraints on the performance of the sensing device. To examine the nature of these constraints, it is convenient to separate this design into the input section of the device and the output section. The input section for the CCIRID consists of the actual photosensor sites, the transfer gate from these sites into the CCD channel, and the assemblage of gates comprising the CCD readout register(s). The output section then consists only of the components and/or circuitry required to detect the signal charge. In the discussion below, the impact of each of these sections in limiting the performance of the CCIRID will be considered.

The performance of the CCIRID chip can be characterized by its responsivity (R) to incident radiation. This quantity is defined by

$$R = \frac{\text{output signal from chip (amps)}}{\text{input signal irradiance (watts/m}^2\text{)}} \tag{4-1}$$

or, since the output signal arises from effects in both the input and output sections of the CCIRID,

$$R = R_{\text{input}} R_{\text{output}} \tag{4-2}$$

The form of these separate contributions to R can now be considered.

The input section responsivity can be written as

$$R_{\text{input}} = AT_I R_\lambda \text{ MTF} \tag{4-3}$$

where A is the area of a single photosensor, T_I is the integration time for collecting photocharge, and R_λ is the photocharge collected per unit of incident radiation into a given photosensor. These quantities basically describe the responsivity of a single sensor element. Since the interest in the present discussion is the overall system response, no further discussion of A, T_I, and R_λ is given. The system response will then be discussed in terms of the MTF factor of equation (4-3). The quantity MTF (the modulation transfer function of the system) represents any modulations introduced into the system response to a signal due to such factors as the CCIRID design, transfer inefficiency in the CCD registers, and limitations of the system components exclusive of the CCIRID (e.g., lenses for focusing the infrared onto the CCIRID). These modulations typically degrade system response to scenes (signals) exhibiting high contrast per unit length, i.e., high spatial frequencies. Since the high spatial frequencies provide the scene detail, it is clear that the MTF factor is of great importance in system characterization.

It is convenient to separate the MTF into those parts arising solely from the CCIRID chip (MTC) and that part arising from external system components (MTX) such as lenses. The remainder of this discussion will treat the factor MTC and, in particular, the contributions to MTC due to transfer inefficiency in the CCD registers. The form of MTX is obviously quite dependent on the details of the system design. As a result, it is not appropriate to the general discussion presented here. The chip MTC consists of three separate components: one arising from transfer inefficiency (MTC_ϵ) in the CCD, one arising from the discrete nature (MTC_ℓ) of the sensors, and one from loss of signal charge to diffusion (MTC_d) processes.

The basic structure (Figure 4-1) of a CCIRID with M photosensitive elements can be reduced to a sequence of M stages. Each stage consists of a photoelement, a transfer gate, and one or more CCD bits (4 gates/bit for 4ϕ operation). The additional bits are included if more isolation is required between sensor elements. Since the added bits are not associated directly with a sensor site, they may also be termed "vacant" bits in the CCD array. The spatial separation of the sensor elements is denoted by ℓ which thereby defines the separation between stages as well. Identifying p as the phase condition (2ϕ, 3ϕ, 4ϕ, etc.) of the device, the number of transfers/stage is given by

$$(a + 1)\, p$$

and thus the maximum number of transfers for the M stage structure is

$$N = M\,(a + 1)\, p \tag{4-4}$$

assuming that detection of the output charge does not constitute a transfer. If the inefficiency/transfer is ϵ, then a transfer inefficiency/stage can be defined as

$$\epsilon_1 = (a + 1)\, p\epsilon \tag{4-5}$$

with the efficiency/stage then given by

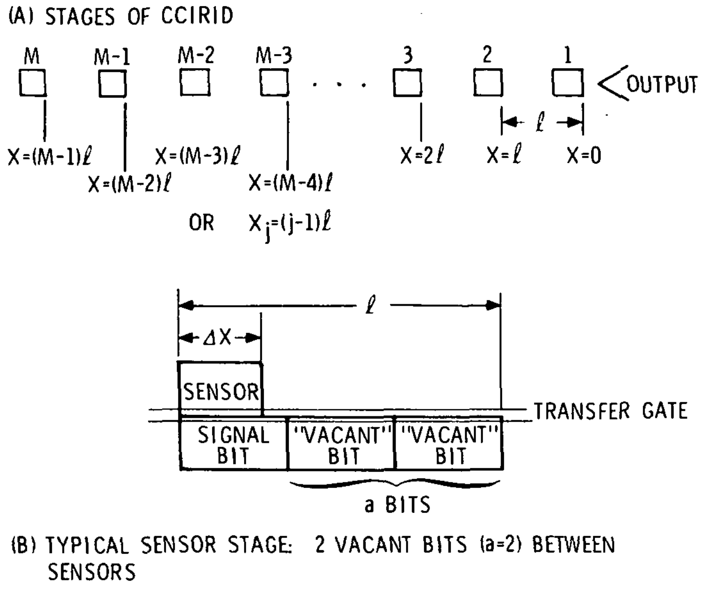
$$\alpha_1 = 1 - \epsilon_1$$

Finally, if the bit length is L_B, the separation between stages is

$$\ell = (a + 1)\, L_B$$

The sensor dimension along the array is frequently just the bit length, but, for generality, it is more convenient to designate this dimension by ΔX.

With these definitions, a complete discussion of the MTC of the CCIRID can be given.



(A) STAGES OF CCIRID

(B) TYPICAL SENSOR STAGE: 2 VACANT BITS (a=2) BETWEEN SENSORS

TRANSFER TIME THROUGH (a+1) BITS: $T_C = (a+1)p\ t_c$
WHERE p = PHASE OF CCD, t_c = CCD CLOCK PERIOD

Figure 4-1. Schematic Representation of M Stage CCIRID

For the contribution MTC_{ℓ}, note that the sensor arrangement is such that the sensitive sites are separated from one another by a distance $\ell - \Delta X$. In this region, no photoresponse is possible so that the resolution of the device is degraded. The extent of the degradation is dependent, however, on the spatial frequency (K) of the radiation falling on the device. For low K values, the information lost in the "dead" regions is not too significant since low frequencies are characterized by little variation in the scene detail. As a result, the information obtained at the sensor sites is not too different from that which is lost. The result is a faithful imaging of the scene. As the spatial frequencies increase, however, the situation changes rapidly. Much scene detail is then included in the optically dead ($\ell - \Delta X$) regions of the structure, so that imaging capability is drastically reduced. It is this behavior then which is described by the factor MTC_{ℓ} of the modulation function. An analytic expression for this factor is

$$MTC_{\ell} = \text{Sinc}\left(\frac{K}{K_{max}} \frac{\pi \Delta X}{\ell}\right) \qquad (4\text{-}6)$$

where $\text{Sinc}(a) = \frac{\text{Sin}(a)}{a}$. In this expression, K_{max} is the maximum spatial frequency which can be imaged without the occurrence of aliasing (Moire') effects. The significance of device design in affecting the parameters ΔX and ℓ is evident in this expression.

The loss of responsivity through diffusion effects (MTC_d) depends on the absorption of an incoming photon outside the depletion region(s) of the active sensor regions. Since absorption is governed by an exponential function ($\sim e^{-\delta x}$) with δ the absorption/unit length, this behavior can occur with finite probability for any incoming photon. Assuming that absorption within the depletion region (depletion width, W) assures collection of the charge as signal, it is equally clear that absorption at distances in excess of two or more diffusion lengths (L_D) beyond $X = W$ will ensure non-collection of the charge. This statement is valid since the only mechanism for charge collection for $X > W$ is the diffusion of the charge back to the well. As the distance $\Delta XW = (X - W)$ increases beyond a diffusion length, the probability of a charge diffusing back to the sensor depletion region rapidly becomes less than the probability of charge recombination. Even if absorption occurs at distances ΔXW less than L_D, a portion of this charge will diffuse laterally away from the sensor site and can even reach adjacent sensors (cross-talk) if the sensor separation is too small. The loss of charge from each of these mechanisms then yields a degradation of the device responsivity, a degradation represented by MTC_d. A phenomenological expression for this factor has been derived[5] for a backside-illuminated diode array and, with only minor modifications, the result can be applied to backside-illuminated CCD arrays. Application to frontside-illuminated CCD arrays, however, requires additional consideration of reflection and/or absorption effects of the particular CCIRID multilevel structure.

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[5] M. H. Crowell and E. F. Labuda, "The Silicon Diode Array Camera Diode," BSTJ 48, p 1487 (1969).

TRANSFER INEFFICIENCY AND MTF

The contribution of MTC_{ℓ} and MTC_d to the total MTC are noteworthy in that they are independent of the performance of the CCD register. The factor MTC_{ϵ} is, however, explicitly dependent on this performance. The purpose of the remaining discussion of the MTC is to examine the dependence in detail and to extrapolate, from MTC requirements, the maximum allowed values of transfer inefficiencies in the CCIRID readout registers as a function of the array size.

Identifying from Figure 4-1, it may be seen that the jth stage of the CCIRID is located at the position

$$X_j = (j - 1)\,\ell$$

The charge packet in this stage at time t is defined by $q_{x_j,\,t}$. Due to the finite α_1, ϵ_1 values of the CCD array, the value of this packet may be written as

$$q_{x_j,\,t} = \alpha_1\, q_{x_{j-\ell},\,t-T_c} + \epsilon_1\, q_{x_j,\,t-T_c} \tag{4-7}$$

where ℓ, T_c are identified by Figure 4-1. This relation is based entirely on the definitions of α_1, ϵ_1, and it does not require the lossless assumption ($\alpha_1 + \epsilon_1 = 1$) for its validity. The MTC degradation due to a finite ϵ can be obtained from a steady-state solution of this relation for a sinusoidal input. Thus, assuming (ϕ an arbitrary phase)

$$q_{xt} = A\,e^{i(kx - i\omega t + \phi)}$$

and inserting in equation (4-7), the result is

$$e^{-i\omega T_c} = \alpha_1\, e^{-ik\ell} + \epsilon_1 \tag{4-8}$$

The parameters ω, k represent the temporal and spatial frequency variations of the input signal. If this signal is not degraded as a function of spatial frequency, then k is the real quantity. Identifying ω as

$$\omega = \omega' + i\omega''$$

it is immediate that

$$e^{\omega''T_c} \cos \omega'T_c = \alpha_1 \cos k\ell + \epsilon_1$$
$$e^{\omega''T_c} \sin \omega'T_c = \alpha_1 \sin k\ell \qquad (4\text{-}9)$$

Solving these equations simultaneously, the results are

$$\omega' = \frac{1}{T_c} \tan^{-1} \left[\frac{\sin k\ell}{\cos k\ell + \epsilon_1/\alpha_1}\right] \qquad (4\text{-}10)$$

and

$$\omega'' = \ell n \left[(\alpha_1 + \epsilon_1)^2 - 2\alpha_1\epsilon_1 (1 - \cos k\ell)\right]^{1/2T_c}$$

The general solution to equation (4-7) is thereby

$$q_{xt} = \left[(\alpha_1 + \epsilon_1)^2 - 2\alpha_1\epsilon_1 (1 - \cos k\ell)\right]^{t/2T_c} A e^{i(kx-2\omega't+\phi)} \qquad (4\text{-}11)$$

To obtain MTC_ϵ, note that the packets for comparison are the charge magnitude at (stage M, time t = 0) and at (output, time $t = t_x$) where t_x is time required to transfer packet from stage M to the output. From Figure 4-1, one has

$$t_{x_m} = (M - 1)\, T_c$$

and

$$x_m = (M - 1)\, \ell$$

so that the value of MTC_ϵ is

$$MTC_\epsilon = \left|\frac{q_{o,\, t_x}}{q_{x_m,\, o}}\right| = \left[(\alpha_1 + \epsilon_1)^2 - 2\alpha_1\epsilon_1 (1 - \cos k\ell)\right]^{\frac{M-1}{2}} \qquad (4\text{-}12)$$

This expression can be further simplified — for the conditions $(\alpha_1 + \epsilon_1) \simeq 1$, $\epsilon_1 \lesssim 0.1$ and $M >> 1$ — to the relation

$$MTC_\epsilon \simeq \exp\left[-M\epsilon_1 (1 - \cos k\ell)\right] \qquad (4\text{-}13)$$

It is implicit from this derivation that the charge at each sensor site is integrated for the same period of time and then read out at the same time and in a single CCD register. This approach constitutes the serial readout mode. Other possibilities do exist, however, with two of the more obvious being: 1) read out only alternate sensor sites at a time while the remaining sites continue to collect signal charge, or 2) read out all sensors at the same time but into different CCD registers. Approach 1) is the familiar interlace technique[6] while 2) may be termed the parallel transfer[7] approach.

In each of these techniques, the result is to double the effective detector spacing (from ℓ to 2ℓ) since charge from adjacent sensor sites never mix in these approaches. The number of detectors is effectively halved, however, from M to M/2 since only one-half of the elements are read at any given time (interlaced) or in a given CCD register (parallel). The resulting MTC_ϵ for these readout techniques is thus obtainable from equation (4-13) by the substitutions $\ell \rightarrow 2\ell$ and $M \rightarrow M/2$ so that

$$\mathrm{MTC}_\epsilon \Big]_{\text{parallel}} \simeq \exp\left[-M\epsilon_1 \left(1 - \cos 2k\ell\right)/2\right] \tag{4-14}$$

Using equations (4-4) and (4-5), these expressions can be written in terms of the maximum number of transfers (N) and inefficiency/transfer ϵ as

$$\mathrm{MTC}_\epsilon \Big|_{\text{Serial}} = \exp\left[-N\epsilon \left(1 - \cos \pi K\ell\right)\right]$$

and (4-15)

$$\mathrm{MTC}_\epsilon \Big|_{\text{Parallel}} = \exp\left[-N\epsilon \left(1 - \cos 2\pi K\ell\right)/2\right]$$

where the definition $k = \pi K$ is inserted for convenience. The nature of the degradation imposed by these expressions, for different values of $N\epsilon$, is illustrated in Figure 4-2(a) and (b) as a function of the spatial frequency K normalized to the Nyquist frequency

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[6] D. F. Barbe, "Imaging Devices Using the Charge-Coupled Concept," Proc. of IEEE 63, p 38 (1975).

[7] H. H. Hosack and R. H. Dyck, "Transfer Inefficiency Effects in Parallel Transfer Charge-Coupled Linear Imaging Devices," IEEE Trans. Elec. Dev., V. ED-22, p 152 (1975).

$$K_{max} = 1/\ell$$

The effect of the different readout techniques is obvious from the figure and has been discussed elsewhere.[8]

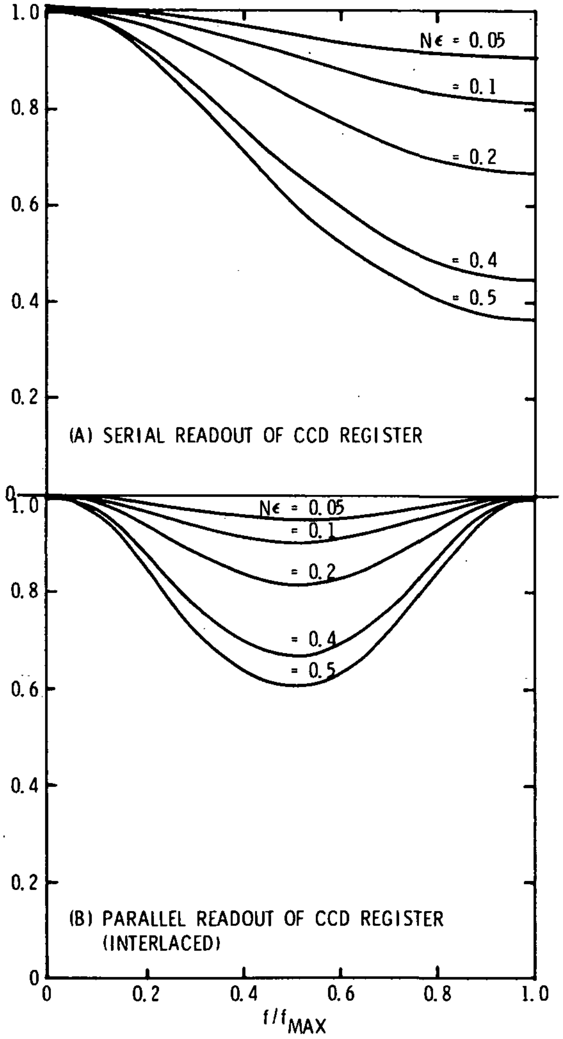

Figure 4-2. MTF Degradation in CCD Imager Due to Transfer Inefficiency

From the figure, it may be seen that the amount of degradation is greatest, for a given $N\epsilon$ product, in the serial readout mode. This result is verified analytically from equation (4-15) above wherein the minimum values of MTC_ϵ are easily shown to be

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[8] C. H. Séquin and M. F. Tompsett, Charge Transfer Devices, Supplement 8 to Advances in Electronics and Electron Physics, Academic Press (New York, 1975).

$$(S)_{MTF} = e^{-2N\epsilon} \text{ at } K = K_{max} \quad \text{Serial}$$

and

$$(P)_{MTF} = e^{-N\epsilon} \text{ at } K = K_{max/2} \quad \text{Parallel}$$

From these results, it may be concluded that the parallel (or interlaced) readout modes offer attractive MTF advantages over the serial mode.

These comments are amplified if one considers the results shown in Figures 4-3 and 4-4. The data in these figures provide a measure of the maximum allowed transfer inefficiency in the CCD register(s) as a function of the array size, i.e., the number of transfers through the device. The minimum permissible MTC_ϵ value is treated as a parameter. A 60% or 70% degradation in device responsivity ($MTC_\epsilon = 0.6$ or 0.7) is too severe for most applications, but the requirements on transfer inefficiency limits of the CCD registers of the infrared imager are correspondingly lax. Indeed, an MTC_ϵ value of 0.7 is possible with the 8582 imager for an inefficiency no larger than $\epsilon = 1.05 \times 10^{-2}$ ($\alpha = 0.989$) for the parallel or interlaced mode.

A more realistic degradation of $MTC_\epsilon = 0.9$, however, requires a much smaller value for the maximum allowed inefficiency. From the figures, it is evident that under this condition, the serial readout mode demands an $\epsilon = 1.6 \times 10^{-3}$ ($\alpha = 0.9984$) while the parallel modes require $\epsilon = 3.2 \times 10^{-3}$ ($\alpha = 0.9968$) for the 8582 structure. Present predictions of 8582 performance indicate that these values will be difficult to achieve even when the existing fabrication difficulties are solved. It can be done, however, by increasing the storage well depth (ΔV) of the CCD registers. As observed previously in this report, the value of this parameter strongly influences the ultimate predictions of Figure 2-7. Similar assessments of a 20-element and 100-element linear imagers can be obtained from Figures 4-3 and 4-4. The ϵ, α requirements for $MTC_\epsilon = 0.9$ and one vacant bit inserted between sensor elements are

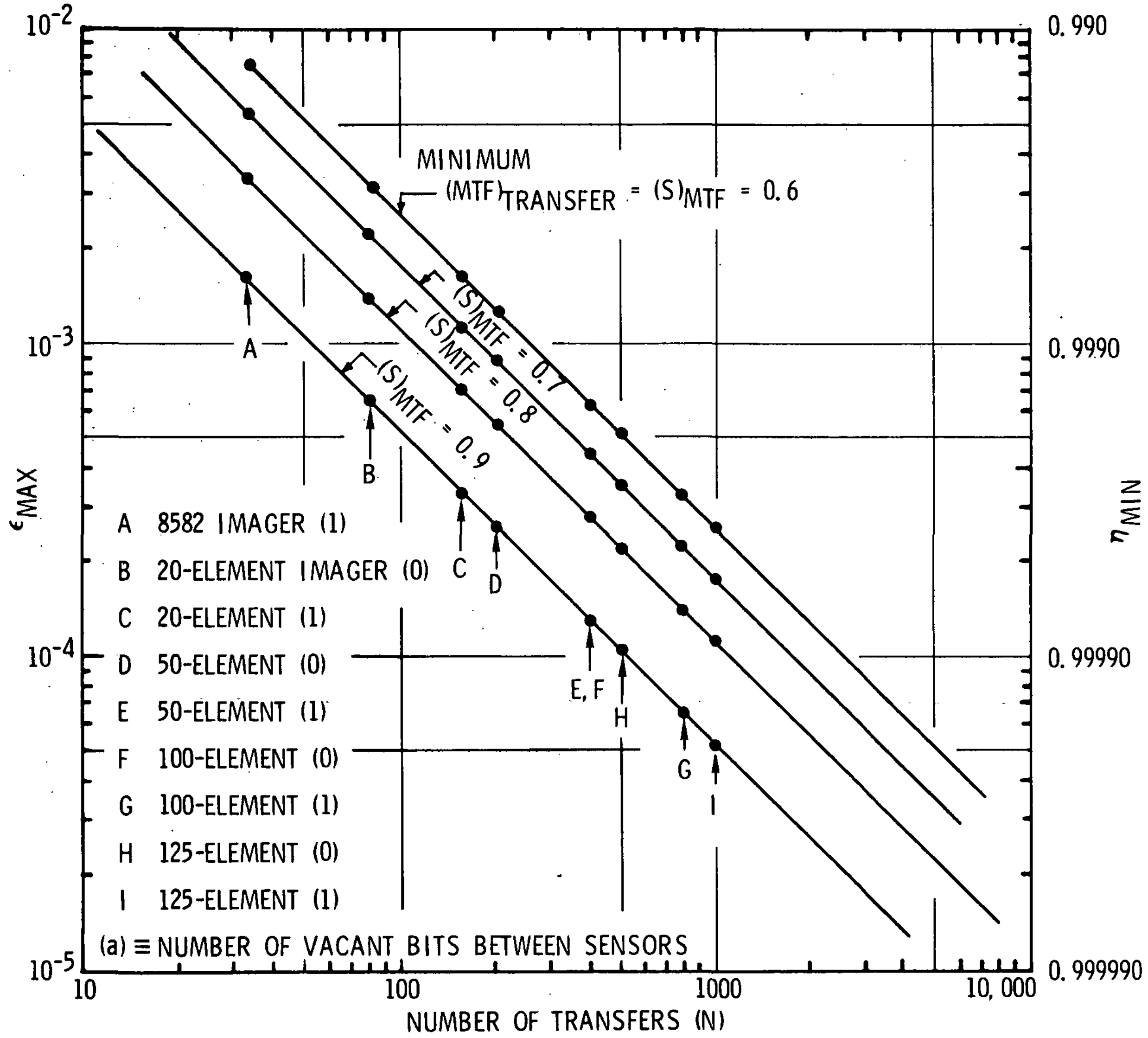

Figure 4-3. Maximum Allowed Transfer Inefficiency (ϵ_{max}) as a Function of Number of Transfers Through Device. Minimum (MTF) degradation (S_{MTF}) for serial readout of CCD register is shown as parameter.

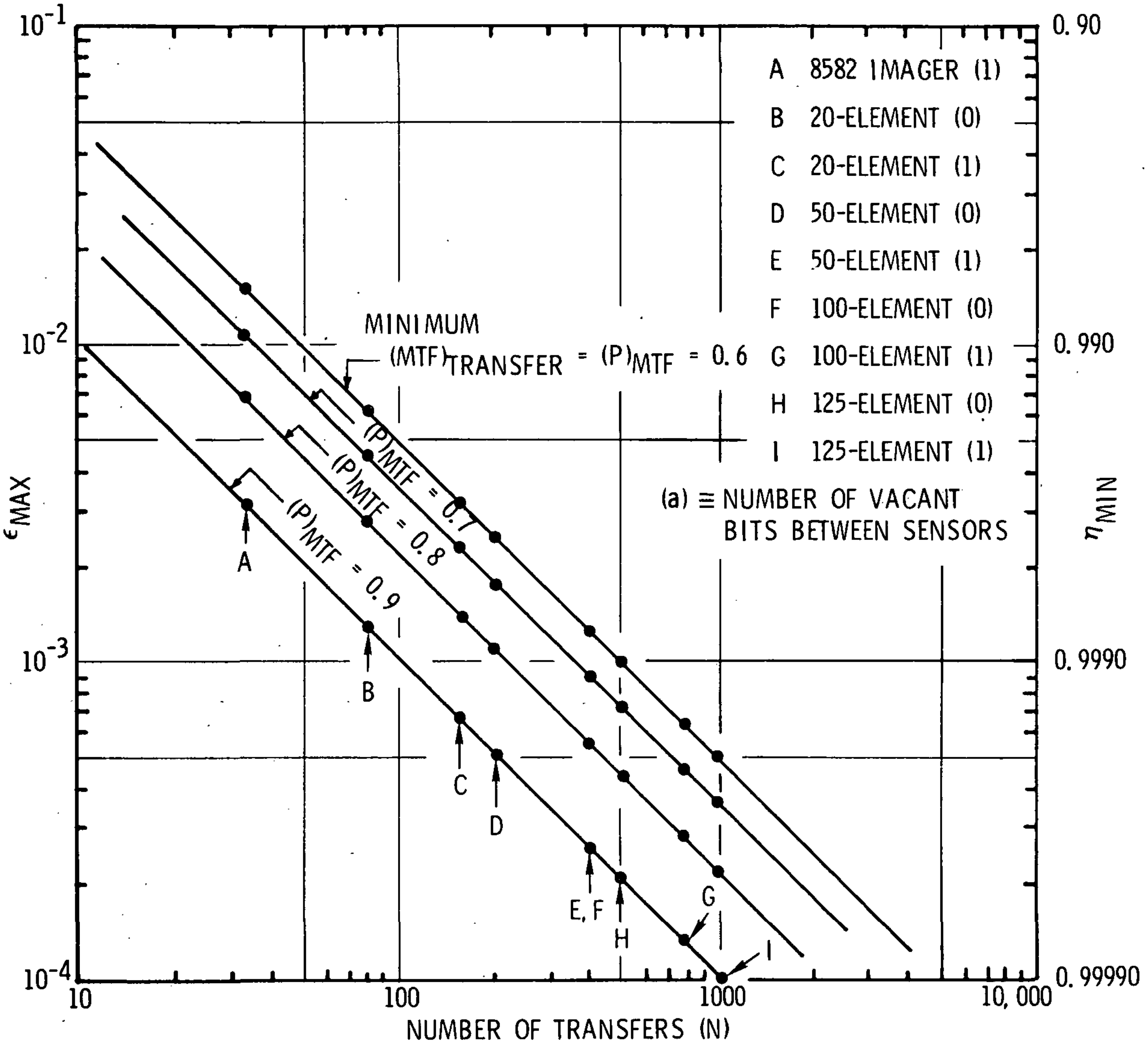

Figure 4-4. Maximum Allowed Transfer Inefficiency (ϵ_{max}) as a Function of Number of Transfers Through Device. Minimum (MTF) degradation (P_{MTF}) for parallel readout of CCD register is shown as parameter.

	Serial Readout		Parallel or Interlaced Readout	
	ϵ	α	ϵ	α
20-element	3.38×10^{-4}	0.99966	6.73×10^{-4}	0.99933
100-element	6.62×10^{-5}	0.99993	1.32×10^{-4}	0.99987

Based on the present predictions, it is clear that achievement of an $MTC_\epsilon = 0.9$ will require improvements in InSb processing technology. With current processing, a comparison of the figures and Figure 2-7 reveals that a 20-element imager with no vacant bits is feasible for a device design with 0.5-mil ($MTC_\epsilon \simeq 0.8$, $\epsilon \simeq 0.997$) gate lengths using either the serial or parallel readout modes. Similarly, a 50-element imager with 7.5-μm gate lengths and no vacant bits between sensors is feasible ($MTC_\epsilon \simeq 0.85$) at this time. *For longer linear arrays, however, improvements in processing technology are definitely needed.* These improvements will arise from the internally funded program now underway.

The contribution of the output section to the overall CCIRID responsivity is expressed through its amplifying characteristics and its noise properties. These properties are in turn influenced by the method used for detecting the signal charge packets from the CCD registers. All methods used for this purpose thus far depend on the observation of a voltage change — induced by the charge packet — of a pre-set charged capacitance. For these methods, the responsivity factor R_{output} can be expressed in terms of the effective transconductance (g_m) of the circuit used in amplifying the voltage change and the capacitance (C) of the input node of the amplifier circuit. The result is simply

$$R_{output} = \frac{g_m}{C}$$

so that an obvious means of increasing the output responsivity of the system is to decrease the charging capacitance. One approach to achieve this objective will be discussed below.

The conventional technique for detecting the CCD charge packet is the gated charge integrator. A schematic of this circuit is shown in Figure 4-5. This circuit consists basically of two MOSFETs, one operating as a source-follower and the other as a reset circuit. The gate of the source-follower FET is normally connected to an output diffusion of the CCD register, which is floating if the reset FET is "off," and charge is detected due to its effect on the bias level of this diffusion. Evidently, the diffusion is set to the bias V_{REF}, when the reset FET is "on," so it is the deviation of the diffusion bias from V_{REF} which identifies detection of charge.

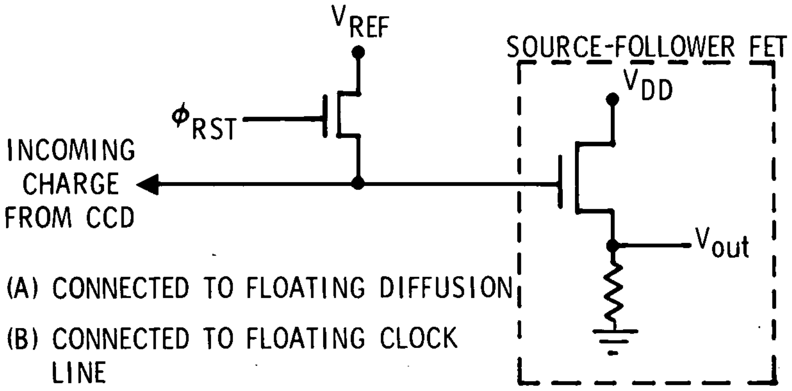

Figure 4-5. Gated Charge Integrator for Charge Detection

This approach is quite functional, but it does suffer from some disadvantages. First of all, the charge packet is destroyed by the act of detection, thus preventing any possibility of multiple detection of the same packet. This flaw is important since multiple detection can result in an increase in the signal-to-noise ratio (SNR) by a factor proportional to $\sqrt{N}$, where N is the number of detection stages. A second characteristic of this approach is a processing limitation. The output diffusion should have as small a capacitance as possible to ensure the largest voltage swing on the source-follower gate for a given size of charge packet. This requirement in turn means that the diffusion should be as small physically as possible since the diffusion capacitance scales as the area. But processing difficulties rise sharply, chiefly due to photolithographic tolerances, as the diffusion size decreases. As a result, a compromise between the desired size and these tolerances is required. For diodes not fabricated on silicon, a third constraint of using the floating diffusion for detection is the low bias voltage and lack of stability often associated with diodes of this type. These variations in the diode character can alter greatly the performance of the gated charge integration (GCI) circuit.

Due to these drawbacks, an alternate approach to detection of the CCD charge is desirable. One possibility is to use the GCI but, rather than sensing the bias change on a diffusion, instead sense the change on a clock line (Method B of Figure 4-5) of the CCD channel. By using the GCI to apply the clock pulse to the gate, charge can still be transferred normally in the register. But by using ϕ_{RST} to stop the clock pulse prior to injection into the clock well, the clock line effectively becomes a floating gate whose bias changes according to the magnitude of the charge packet beneath it. If $(\Delta V)_w$ is used to denote the storage well depth beneath the clock line, then the maximum swing in the floating clock bias voltage (from its pre-set "floating" value) is given by

$$(\Delta V)_{FC_{max}} = \frac{C_{ox}}{C_{net}} (\Delta V)_w$$

Here C_{ox} is the capacitance/unit area of the clock line only over the CCD channel while C_{net} includes not only C_{ox} but contributions from the clock line outside the channel, the pad for contacting the gate, and the GCI itself. It is clear that minimizing these external contributions is desirable for optimum operation of this technique.

By using a clock line as the detector, the advantage of nondestructive detection obviously is gained. As a result, the same charge packet can be sensed repeatedly, by other floating clock detectors, if desired, with a corresponding increase in the SNR. The approach also gains independence from the sensitivity problems of diodes on other than silicon substrates. With the floating clock as the prime detection mechanism, the primary purpose of the diode is to act as a "sink" to absorb the channel charge after detection is completed. Thus the diode can be simply set at a large reverse bias and then left alone. Finally, the floating clock approach gains some advantages over the floating diffusion since the overall size of the clock line is not limited by the physical requirements of the diffusion process. As a result, it is probable that achievement of a small capacitance for the clock line is easier than in the case of the diffusion.

All these factors then make the floating clock detection scheme an attractive alternative to the floating diffusion technique. For the 8582 structure, such an approach is especially preferred due to the large capacitance (≃22 pf) of the output diffusion. Unfortunately, application of the floating clock approach to the 8582 is handicapped by the lack of a thick-field oxide on the device. The result is a large contribution to the clock line capacitance by the pad and line portions external to the CCD channel. Since the pads are large, this contribution is approximately 10 pf. A small (≃35-mv) signal, about double that observed for the floating diffusion, is thus expected for the 8582 structure. As a result, the floating clock approach has not been attempted on the 8582 in lieu of extensive processing of the 9-bit 8582 linear imager and optical testing. The attractive features of the floating clock technique will, however, be utilized in the next generation of CCIRIDs and on the 8582 with the revised mask level of the buried metal insulator. Indeed, the floating clock and floating diffusion detection schemes will both be used, routinely, to determine the best approach for NASA applications.

Section 5

CONCLUSIONS

The following conclusions may be drawn from the results of this contractual effort:

1. A four-phase (4ϕ), overlapping gate CCD with 9 transfers (2-bits) and 1.0-mil gate lengths has been successfully operated with electrical input and the proper time delay in the output signal.
2. The measured transfer efficiency of $\alpha \simeq 0.975$ for this device is in excellent agreement with predictions for the reduced gate length device. This agreement is strong evidence that the next generation CCIRIDs with 12.5-μm (0.5-mil) gate lengths will achieve at least the predicted value of $\alpha \simeq 0.997$.
3. A completely functional 9-bit imager has not been successfully fabricated. Reasons for this failure have been identified as design flaws in the 8582 mask set and adherence difficulties of the channel stop and buried metal insulators.
4. Mask revisions of the channel stop metal on the 8582 mask set have been carried out with the result being a large increase in the dc yield of the tested devices. A further revision of the buried metal insulator should result in fully functional 9-bit CCIRIDs.
5. Partial optical sensitivity to chopped blackbody radiation has been observed for an 8582 9-bit imager. The optical response was totally controlled by the transfer gate of the imager. This observation is evidence that the collection of signal charge in the photosensors and subsequent transfer of this charge into the CCD readout registers via the transfer gate is feasible.
6. Analytical considerations of the MTF degradation caused by transfer inefficiency in the CCD registers have been presented. These results indicate that: a) 20-element imagers with 1-bit/sensor and 0.5-mil gates, and b) 50-element imagers with 1-bit/sensor and 7.5-μm gates are feasible with current processing technology.
7. For larger array lengths or for the insertion of isolated bits between sensors, improvements in InSb fabrication technology with corresponding decrease in the interface state density are required.

The information obtained during this contract period, coupled with the process development studies in progress as an internally funded effort, make the continued improvement in CCIRID technology a certainty. Revision of the 8582 buried metal insulator mask level will allow fabrication of the 8582 imager from which D* and quantum efficiency data will be obtained. Preliminary design studies of the next generation CCIRID structures have been carried out, and fabrication of a 20-element imager will begin early in the next program. The results obtained on this structure and the revised 8582 mask set will allow the orderly development of CCIRIDs on InSb to continue. The resulting detectors — with their 1- to 5-μm sensitivity, potential high signal-to-noise ratios, low weight and power requirements, and array uniformity — will be especially compatible with NASA payload requirements.