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NASA TM X-73427

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REGULATION OF A LIGHTWEIGHT HIGH EFFICIENCY CAPACITOR DIODE VOLTAGE MULTIPLIER DC-DC CONVERTER

by William T. Harrigill, Jr. and Ira T. Myers
Lewis Research Center
Cleveland, Ohio 44135

TECHNICAL PAPER to be presented at
Power Electronics Specialists Conference sponsored
by the Institute of Electrical and Electronics Engineers
Cleveland, Ohio, June 8-10, 1976

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by William T. Harrigill, Jr. and Ira T. Myers

National Aeronautics and Space Administration
Lewis Research Center
Cleveland, Ohio

E-8768

ABSTRACT

A method for the regulation of a capacitor diode voltage multiplier dc-dc converter has been developed which has only minor penalties in weight and efficiency. An auxiliary inductor is used, which only handles a fraction of the total power, to control the output voltage through a pulse width modulation method in a buck boost circuit.

INTRODUCTION

In previous papers the authors have described high frequency voltage multiplier circuits for ultra lightweight, high efficiency space type applications (1,2). Regulation of the output voltage against both input voltage variations and output power changes is normally required for most converter applications. To the best of the authors' knowledge, no lightweight high efficiency method of regulating or controlling multi-stage high frequency voltage multipliers has been developed.

This paper describes two open loop regulation techniques using small auxiliary inductors, which meet the requirements of minimizing loss and weight penalties. Although closed loop control was not attempted, no major barriers to closed loop operation appear evident.

DESCRIPTION OF REGULATION METHODS

Conventional methods considered and rejected either because of excessive losses or high component weights included direct pulse width modulation of the capacitor diode voltage multiplier(CDVM) chopper, dissipative series and shunt regulation, and total preregulation using buck, buck-boost, or boost methods. Finally, an approach was developed using one of the two voltage inputs of the voltage multiplier, (V_{2i} in Figure 1) as an additive control voltage. The output voltage V_L is given approximately by $V_L = \frac{KN}{2}(V_{1i} + V_{2i})$ where N is the number of capacitors in the voltage multiplier and K varies with the output power, but is near unity (1). Either V_{1i} or V_{2i} can be zero or chosen arbitrarily within component ratings. Because of the proportional relationship between the input voltages, and the output voltage, control of the voltage V_{2i} over a range ΔV_{2i} can be used to compensate for an input voltage change in the source voltage V_{1i} (1.7:1 in this work), or an output voltage change V_L due to load variation (20 to 100% in the present work).

In the present work, as in most cases, regulation is only required over a fraction of the system input or output voltages, so that V_{2i} and ΔV_{2i} can be only a fraction of V_{1i}. Thus the major part of the load power will come from V_{1i}, directly through the voltage multiplier, without passing through the regulator. Since V_{2i} supplies only a relatively small fraction of the total power, it can be generated using inductive storage methods with only moderate overall system penalty in weight and efficiency.

The first approach developed uses a small auxiliary inductor to replace both Q_2 and V_{2i} in the basic CDVM circuit in Figure 1. From Figure 2 it can be seen that the effective magnitude of V_{2i} is controlled by controlling the on and off times of the switching transistor Q. In this approach the inductor is charged from the voltage V_{1i} to an energy $1/2\ L\ i_{max}$, where i_{max} is given by $V_{1i}\ t_{on}/L$. This energy is discharged into the input of the CDVM during the transistor "off" period. An experimental model of this method worked reasonably well. Although it has the advantage of simplicity, it is limited to a minimum "on" time of 3 or 4 microseconds. This is the charging time required for the CDVM, since the same transistor switch drives both the inductor and the input to the CDVM. This means that the full control and regulation range expected with the inductor cannot be achieved.

This 3-4 microsecond charging time is caused by the stray inductance of the CDVM interacting with the input capacitance through the CDVM diodes to give a single half cycle charging wave shape with a 3-4 microsecond half period. Careful mechanical design and layout with consequent reduction in the stray inductance could perhaps improve this regulation range. However, it is estimated that this stray inductance is substantially less than a microhenry, so that it may be difficult to reduce it further.

A second method appears to be superior. In this method, the regulating voltage V_{2i} is developed from V_{1i} by a simple buck-boost circuit, with its own switching transistor, so that complete control down to very small "on" times is possible (See Figure 3).

This second method requires three transistors in place of one, plus an extra diode, inductor, and capacitor. Again, since the source V_{2i} furnishes only a small amount of the total power, the weight and efficiency penalty of this more complex approach is still small. Completion of the control loop with conventional pulse width modulation control is not expected to seriously impact either the weight or efficiency.

The operation of the buck-boost circuit is well known (3) and will not be described here. An important feature of the buck-boost circuit for this application is that the output voltage polarity is the negative of the input polarity. Thus V_{2i} has the opposite polarity of V_{1i}, as it must have for properly furnishing voltage to the CDVM. If V_{2i} and V_{1i} were of the same polarity, the load voltage would be given by $V_L = \frac{KN}{2}(V_{1i}-V_{2i})$ where the quantities V_{1i} and V_{2i} are scalar magnitudes.

In order to minimize inductor weight and simplify the drive circuit, the driving frequency was chosen to be 70 kHz, which is the same as the CDVM frequency. Only a moderate effort was made to obtain high efficiency in the buck-boost regulating circuit; it is likely that, with further work, improvements in efficiency and weight could be made.

The interaction of the buck-boost circuit efficiency and the CDVM efficiency is given by the following $\eta(\text{overall}) = \eta_{CDVM}\left(\frac{1+\alpha}{1+\alpha/\eta_{BB}}\right)$ where

η(overall) = overall system efficiency for dc-dc conversion.
η_{CDVM} = efficiency of unregulated CDVM
η_{BB} = efficiency of the buck-boost circuit
α = fractional regulation = $\frac{V_{2i}}{V_{1i}}$

A plot of η(system) was calculated as a function of α and η_{BB} and is given in Figure 4.

A description of the CDVM circuit losses has already been given (2). The additional losses due to the buck-boost circuit are given in Table I. The loss contributions to the overall system are in general quite small.

For the case given, only about 20% of the output passes through the buck-boost regulator circuit, and the losses in it represent only 2.7% of the total system power. This illustrates the advantage of the partial power regulation method.

No input filter was used to reduce feedback of the chopper frequency back to the power source. However, the input filter should be smaller for the 70 kHz operating frequency of the CDVM than for the more conventional converter operating at 5-20 kHz. No output filter was needed, since the CDVM serves as its own output filter.

EXPERIMENTAL RESULTS

The overall efficiency of the converter as shown in Figure 3 was measured using laboratory square wave pulse generators with variable on and off time to drive the switching transistors. The feedback control was manual, i.e., the pulse generator "on" time was controlled manually to maintain the output voltage constant (at 1000 V) while the input voltage and/or output power was varied. The input voltage was varied from 160 to 260 volts and the input power from 20 to 100 watts. The regulating ratio α (V_{2i}/V_{1i}) and the efficiency were measured. The results are given in Figures 5 and 6. The decrease in efficiency with decreasing input voltage V_{1i} is clearly seen in Figure 5. The decrease and rise in efficiency near the α=0 point is thought to be due to the interaction effect of the buck-boost diode and inductor which must carry the CDVM current even at $\alpha = 0$.

Figure 6 is a plot that shows efficiency variations with load at a constant input voltage. The efficiency is a well behaved function; it varies slowly with both input voltage changes and output power changes, and remains high over a wide range of both of these variables.

Figure 7 shows the wave shapes in the CDVM and in the buck-boost regulator for typical operation at 70 kHz for a power output of 100 watts. For the buck-boost regulator, the operation may be divided into three parts. First transistor switch Q_3 is turned-on to charge the inductor. During this time the inductor voltage is at the supply voltage V_{1i} and charges at the rate $di/dt = V_{1i}/L$. At the end of this charging period the transistor is turned-off and the inductor reverses polarity, matching voltage through the diode to V_{2i}. During this time Q_2 is also on, although the "on" time for charging the CDVM and the time the inductor is charging the capacitor across which V_{2i} is developed are not necessarily the same. The third period starts when the inductor is nearly discharged. Some voltage remains on the inductor and its associated stray capacitance after the diode begins to block current flow into the capacitor. This charge or energy resonates at about one-half megahertz rate (between the L of the inductor and its own stray capacitance) until the inductor charging is started again by turn on of Q_3. The positive and negative areas under the CDVM input current curves (Figure 7) can be seen to be equal. This is as expected since the input is a capacitor and at steady state operation there can be no net dc current flow. However, since V_{1i} is much larger than V_{2i}, and since the power furnished by the two voltage sources, has the same current, V_{1i} will normally furnish much more power than V_{2i}.

COMPONENT WEIGHTS OF PARTIAL POWER REGULATED CDVM

Table II gives a list of components and their weights. The capacitors makeup about one-half of the total component weight, while the inductor weight is only 20% of the total components. This, of course, is possible because the inductor only handles a fraction of the total power. These weights are strongly competitive for space type

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applications with more conventional dc-dc conversion methods.

CONCLUDING REMARKS

Measurements indicate that it is possible to regulate a capacitor diode voltage multiplier. This can be accomplished with relatively little loss in efficiency or increase in weight by taking advantage of the partial power regulation method, where only a fraction of the output power passes through the regulator. With presently available components, it appears that dc-dc converters with component weights in the 1-1.5 kg/kw range are possible, with efficiencies in the 90% range.

Although the basic concept of partial power regulation of the CDVM was demonstrated, full closed loop control, with measurements of dynamic response, overall stability, audio susceptibility of the CDVM circuit, and weight and loss of the input filter, remain to be done. However, no major barriers to closed loop operation appear evident.

REFERENCES

1. W.T.Harrigill,Jr., and I.T.Myers, "High Performance dc-dc Conversion With Voltage Multipliers", NASA TM-71566. 1974.

2. W.T.Harrigill, Jr., and I.T.Myers, "Efficiency and Weight of Voltage Multiplier Type Ultra Lightweight dc-dc Converter", NASA TM 71735, 1975.

3. D.R.Powell,"Modeling and Stability Analysis Of A Buck-Boost Switching Regulator Intended For the Power Conditioning of a Caesium Contact Ion Thruster," Spacecraft Power Conditioning Electronics Seminar. ESRO SP-103 September 1974. Proceedings of a seminar held at Frascati, Italy, 20-22 May 1974.

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TABLE I.

SYSTEM INEFFICIENCIES DUE TO
BUCK BOOST REGULATOR LOSSES

LOSS TYPE	FORMULA FOR LOSS	SYSTEM LOSS, % AT 100 W_o, 20 W SUPPLIED BY B.B. CIRCUIT
I^2R LOSS IN INDUCTOR	$i^2_{L(RMS)}R_L$	0.4
LOSS IN STRAY CAPACITANCE OF INDUCTANCE	$C_L(V^2_{2i} + V^2_{1i})$	.6
FORWARD VOLTAGE DROP IN DIODE	$i_{ave}V_{Fd}$	.6
SWITCHING LOSS IN DIODE	$f\tau/3\ P_{REG}$	.1
TRANSISTOR FORWARD DROPLOSS	$i_{AVE}V_{TFd}$	.1
TRANSISTOR SWITCHING LOSS	$f\tau/3\ P_{REG}$	.1
STRAY CAPACITANCE LOSS IN TRANSISTOR	$C_{JTR}(V_{2i} + V_{1i})^2 f$	.7
STRAY CAPACITANCE IN DIODE	$C_{JDR}(V_{2i} + V_{1i})^2 f$	.1
DRIVE CIRCUIT LOSS FOR Q_3		≈ 0

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TABLE II.

WEIGHT OF COMPONENTS IN EXPERIMENTAL
100 W REGULATED DC-DC CONVERTER

COMPONENT	WEIGHT, g
CAPACITORS	78
POWER TRANSISTORS	34
INDUCTANCE	30
DIODES	9
MISCELLANEOUS	14
TOTAL	165

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EITHER V_{1i} OR V_{2i} CAN BE ZERO OR CHOSEN ARBITRARILY WITHIN COMPONENT RATINGS

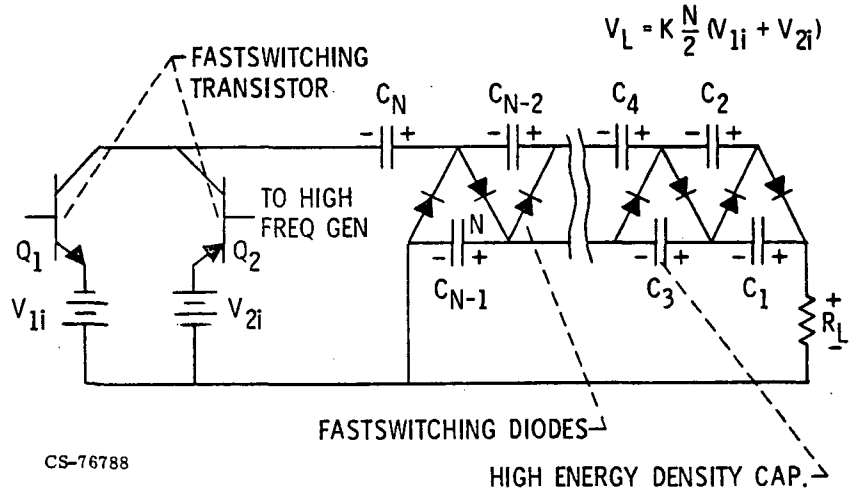

Figure 1. - Transformerless capacitor diode voltage multiplier DC-DC converter.

INDUCTANCE L SUBSTITUTES FOR BOTH POWER SOURCE V_{2i} & TRANSISTOR SWITCH Q_2

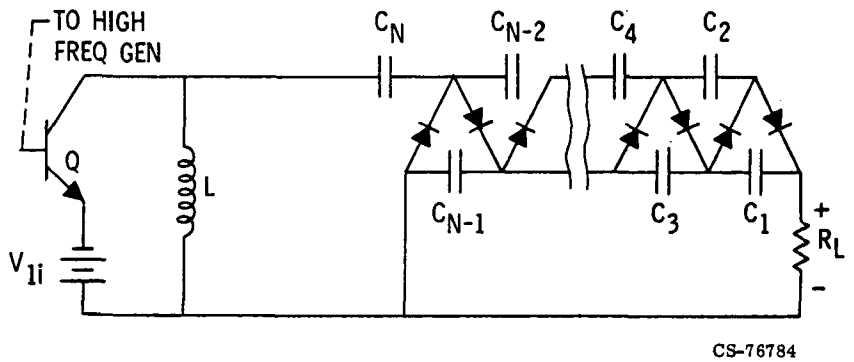

Figure 2. - Regulation of CDVM using single auxiliary inductance.

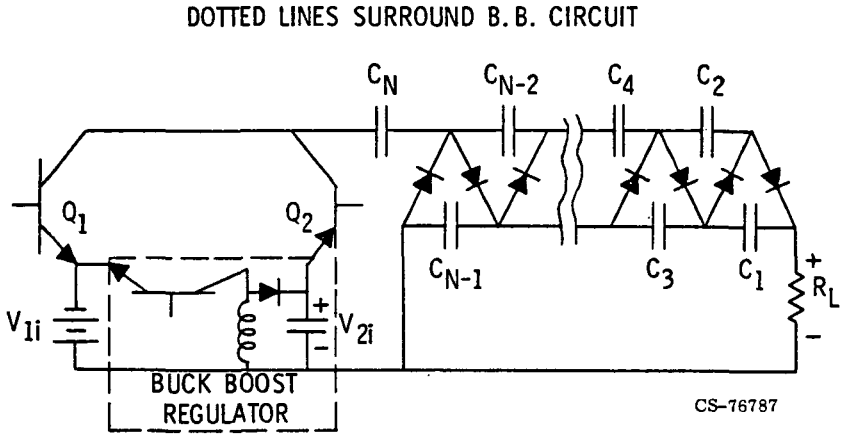

Figure 3. - Capacitor diode voltage multiplier with regulating voltage V_{2i} supplied by buck-boost circuit.

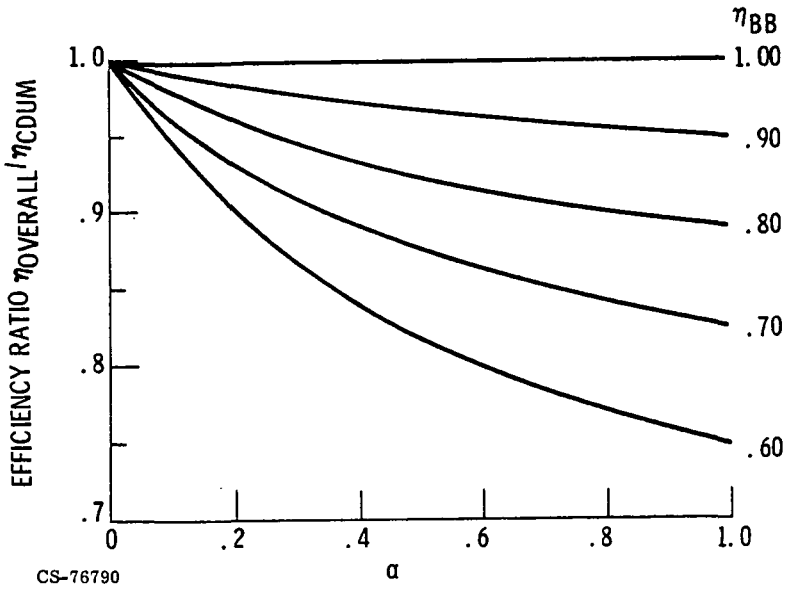

Figure 4. - Efficiency ratio versus regulating fraction α and buck-boost circuit efficiency.

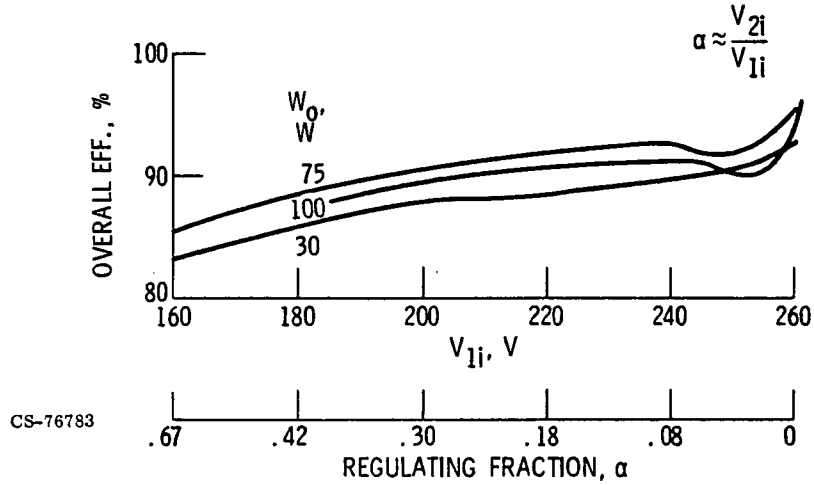

Figure 5. - Overall efficiency versus unregulated voltage (V_{1i}).

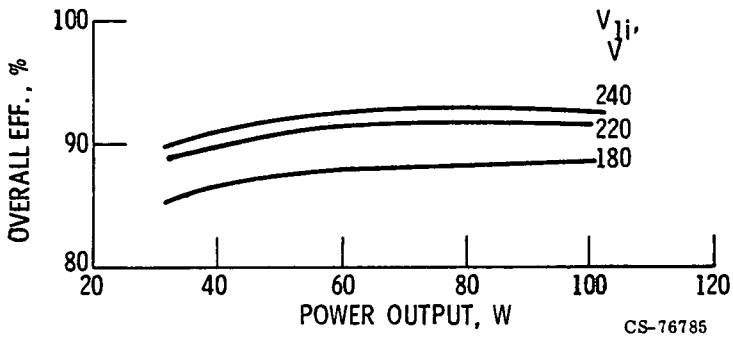

Figure 6. - Overall efficiency versus power output.

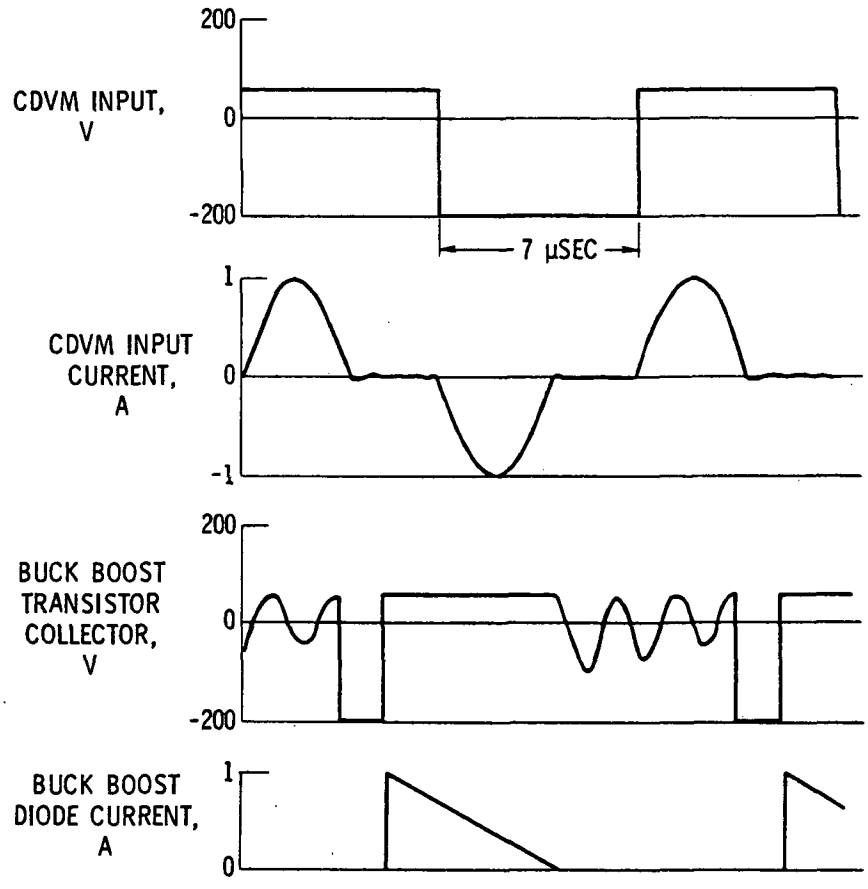

Figure 7. - Experimental circuit waveforms.