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AUTOMATED ARRAY ASSEMBLY

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QUARTERLY REPORT NO. 1

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

We have begun our study for the Automated Array Assembly Task by simultaneously evaluating present manufacturing techniques using expenses based on experience and studying basic cost factors for each step to evaluate expenses from a first-principles point of view. We are developing a formal cost accounting procedure which will be used throughout the study for cost comparisons. The first test of this procedure is

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PREFACE

This Quarterly Report, prepared by RCA Laboratories, Princeton, NJ 08540, describes work performed during February and March 1976 in the Communications Research Laboratory, K. H. Powers, Director; Process and Applied Materials Research Laboratory, P. Rappaport, Director; and Materials Research Laboratory, J. J. Tietjen, Director. The Project Supervisor and Project Scientist is B. F. Williams. Others who participated in the research and writing of this report are: J. Amick, D. Richman, D. Redfield, B. Shelpuk, R. Denning, and G. Schnable.

The JPL Project Monitor is Walter Hasback.

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SECTION I

SUMMARY

We have begun our study for the Automated Array Assembly Task by simultaneously evaluating present manufacturing techniques using expenses based on experience and studying basic cost factors for each step to evaluate expenses from a first-principles point of view. We are developing a formal cost accounting procedure which will be used throughout the study for cost comparisons. The first test of this procedure is a comparison of its predicted costs for array module manufacturing with costs from a study we have now completed which is based on experience factors. In this completed study, which is described in this report, we estimate a manufacturing cost for array modules of $10/W, based on present day manufacturing techniques, expenses, and materials costs.

Our analytical system to provide the input data for the cost analysis is also described. The analysis of different input sheet forms and quality has begun.

To provide the information needed to fill in the processing cost matrix, processing steps are being analyzed in terms of (1) consumed materials, (2) capital equipment costs, (3) labor, and (4) space requirements. State-of-the-art technology, as used in the fabrication of power transistors, serves as the point of departure for this analysis.

Initial estimates show that the materials consumed in diffusion and in cleaning can be in the few cents per watt range. Although epitaxy is currently expensive, improvements in the technology could lower consumed materials costs to the $0.10/W range. More complete cost estimates will be available after the capital, labor, and space costs are evaluated through our formal cost analysis.

Identification of a baseline circuit module configuration for the initial cost studies has begun. This module will have a 12- to 14-V dc output and uses 3-in.-diameter circular or semi-circular cells. It is packaged in a glass enclosed package using a fiberglass substrate. The process flow diagram to manufacture this module is now being developed.

An analytical effort to support the final module design on the basis of circuit, thermal, and stress parameters has been initiated. An investigation has been begun into existing automated semiconductor wafer handling and interconnecting equipment. This program's requirements exceed existing capability. However,

automation is beginning to emerge in this industry and potential for large-scale production equipment is promising.

As this report covers the first five weeks of this program, much of this work is still underway.

SECTION II

INTRODUCTION

The purpose of this study is to conceptually develop manufacturing processes for silicon solar array modules which may be sold for $0.50/W in 10 years assuming a yearly sales volume of 500 MW. These solar array modules are expected to have a power conversion efficiency of at least 10% and a life expectancy of 20 years. At such a price, these modules will be a factor of 10 to 100 less expensive than modules which are available presently.

In this study we are evaluating manufacturing processes beginning with some form of silicon sheet. The silicon may be in the form of wafers, EFG ribbon, dendritic web, etc. It is clear that the electrical performance characteristics, the mechanical characteristics, and the cost of each form will seriously impact the cost of the final modules. Therefore, an important part of this program is an evaluation of these various forms to provide an input to the processing study. No experimental work on the manufacturing of silicon sheets is being done in this program as that is the responsibility of Task I and Task II of the LSSA Program. Rather the developments in those tasks are being integrated with known developments taking place within the industry to provide data for the silicon quality materials matrix shown in Fig. 1. In this matrix, seven classes of silicon material are identified, each class defined by a general growth technique. These classes are:

(1) Wafers cut from single crystal ingots.

(2) Vapor phase epitaxial growth on silicon substrates.

(3) Vapor phase epitaxy on sapphire substrates.

(4) Ribbon growth from the melt.

(5) Dendritic web pulled from the melt.

(6) Rolled sheet silicon.

(7) Silicon deposited on glass.

For each class, the cost of producing silicon of a given quality is being developed under the program. Five grades of silicon quality are proposed:

(1) Semiconductor grade

(2) Solar cell grade

(3) Metallurgical grade

(4) Polycrystalline

(5) Amorphous

PREPARATIVE TECHNIQUE / QUALITY	WAFER CUT FROM INGOT	EPITAXY SILICON ON SILICON	EPITAXY SILICON ON SAPPHIRE	PULLED RIBBON	DENDRITIC WEBB	ROLLED SHEET	SILICON ON GLASS
SEMICONDUCTOR GRADE							
SOLAR CELL GRADE							
METALLURGICAL GRADE							
POLYCRYSTALLINE							
AMORPHOUS							

Fig. 1. Silicon quality materials matrix

"Solar Cell Grade" is, at present, not completely defined, although it is generally recognized that some relaxation in standards of semiconductor grade material can be allowed for solar cell fabrication. A solar cell grade will be defined based on the art at the termination of the contract. At the end of this program, estimates of the costs of these various forms in terms of $\$/m^2$ and the concomitant electrical and mechanical characteristics will be completed. This matrix provides data for the input to the processing matrix which is discussed below.

The processing matrix defines the cost of all processing and testing steps required to fabricate silicon solar array modules for all of the different grades of silicon quality as determined in the silicon quality materials matrix. This processing matrix is shown in Fig. 2.

In the course of this program we are filling in the processing matrix with the costs of each technological step, assuming a production of 500 MW of solar array modules in 1985. This analysis is not of the experience curve variety but a detailed evaluation of how best each of the existing technologies can be scaled up, and what the impact will be. It should be clear that from such a completed matrix, any module configuration or design, manufactured by a scaled-up existing technology, can be evaluated for cost. Cost bottlenecks will also be apparent from such a matrix.

The last steps of the processing matrix deal with the assembly and interconnection of the arrays. The costs in this area are derived from the array module cost analysis interaction diagram, Fig. 3.

The block diagram in Fig. 3 pulls together the factors supporting analyses and interactions which are being used to evaluate various array module configurations. It is obvious that this simplified study flow diagram indicates considerable interaction between its four major tasks. This may result in several iterations between design and manufacturing for each array module design generated.

The methodology used in this study calls for the engineering organization to develop conceptual circuit and mechanical array module designs. This organization is supported by a data base of environmental and photovoltaic information and computer-aided analysis tools in the areas of performance characterization, stress, and thermal response. Each concept studied is being analyzed in these areas to support specification of materials and configurations in the array module design. The output of these analyses, and the results of a study of testing requirements are then

	SEMICONDUCTOR GRADE	SOLAR CELL GRADE	METALLURGICAL GRADE	POLYCRYSTALLINE	AMORPHOUS
JUNCTION FORMATION					
DIFFUSION					
GAS PHASE					
SPIN/SPRAY					
SOLID					
CVD OXIDE					
METAL CONTACT					
ION IMPLANTATION					
EPITAXY					
TESTING & CONTROL					
INTERFACE					
METALLIZATION					
EVAPORATION					
SPUTTERING					
VAPOR DEPOSITION					
SILK SCREENING					
PHOTOLITHOGRAPHY					
TRANSFER TAPE					
OFFSET PRINTING					
TRANSPARENT LAYERS					
TESTING & CONTROL					
INTERFACE					
AR COATINGS					
SINGLE LEVEL					
MULTI LEVEL					
SURFACE TOPOLOGY					
TESTING AND CONTROL					
INTERFACE					
ENCAPSULATION					
EXPOSED					
ENCLOSED					
INTERFACE					
ASSEMBLY					
ELECTRICAL DESIGN					
MECHANICAL DESIGN					
CELL SIZE					
CELL BONDING					
CELL INTERCONNECTS					
SUBMODULE SIZE					
CELL SPACING					
TESTING & CONTROL					
CONCENTRATION					

Fig. 2. Processing matrix

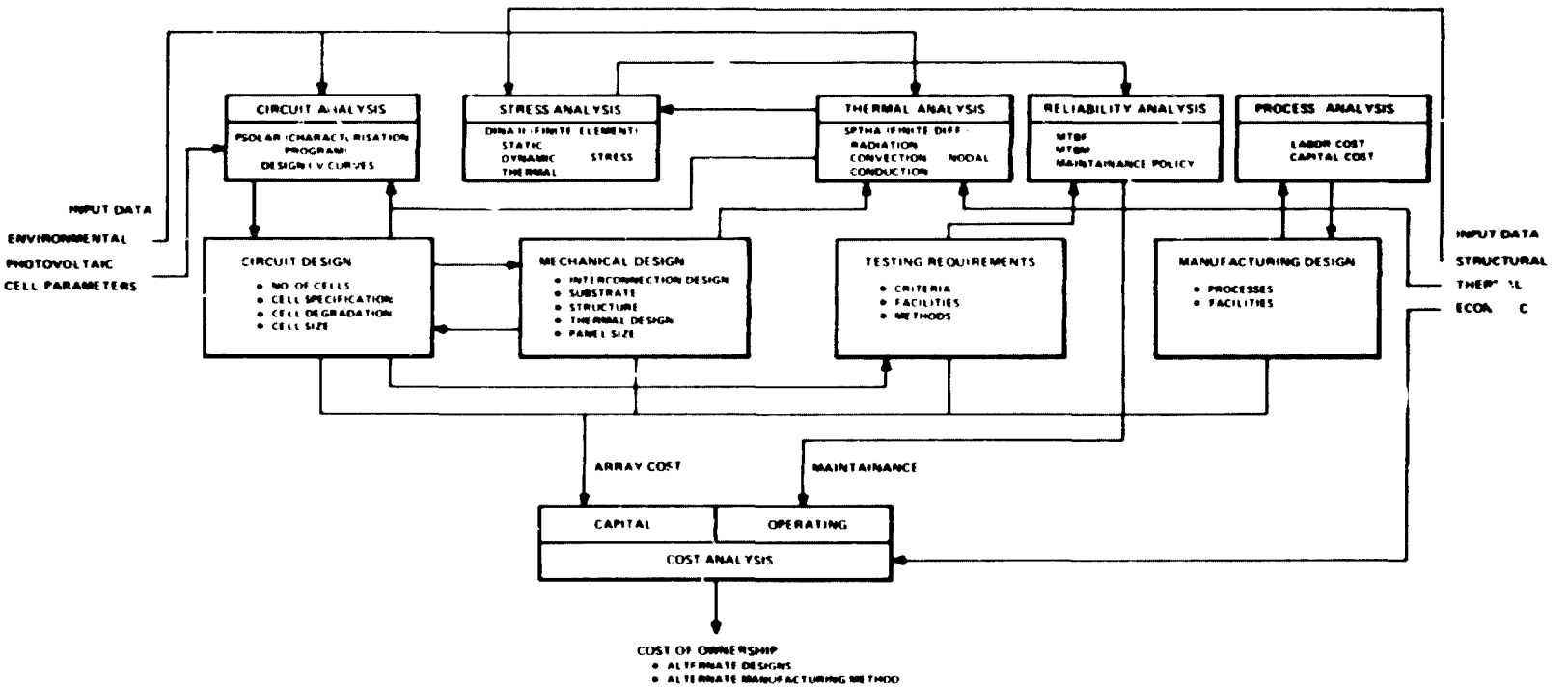

Fig. 3. Array module cost analysis interaction diagram

combined in a reliability analysis in order to establish a required maintenance policy dictated by the calculated failure rate. At the same time, the array module design is evaluated by manufacturing personnel in order to establish the capital and labor costs associated with manufacturing of each of the candidate array concepts.

The development of a formal cost accounting system to make possible the comparison of alternative manufacturing procedures is the first step in this program. In the next section we present our cost accounting procedure. An evaluation of the validity of this approach is under way. The first test is a determination of the costs of manufacturing a solar array module by existing techniques. This test is based on a generalized manufacturing procedure, and because it uses existing manufacturing techniques, the costs can be defined fairly accurately based on extensive semiconductor device manufacturing experience. This analysis is complete and is described in the next section. The data of this study are being put into the format which will be used in all the forthcoming comparison studies.

In addition to the analysis of the costs of manufacturing modules by the existing techniques, we have begun our basic studies of cleaning, diffusion, epitaxial growth, ion implantation, metallization, and interconnection. It should be noted that the reporting period covered in this report is the first five weeks of the program and, therefore, much of the technical discussion will deal with studies which are still underway.

SECTION III

TECHNICAL DISCUSSION

A. COST ANALYSIS PROCEDURE

For purposes of cost analysis, the manufacture of solar cell modules will be represented by a series of technological process. (See Appendix A for definition of terms and Appendix B for a simplified cost analysis description.) Each technological process must be described in terms of the following:

(1) Incoming material requirements.

(2) Value added - material, labor, overhead.

(3) Equipment requirements as a function of production levels.

(4) Process yield - ratio of output units to input units. (Note that this is a measure of *physical flow*, not product quality.)

After these parameters have been provided, alternative manufacturing processes can be defined in terms of a subset of these technological processes. For a specified level of output (measured in megawatts), cost data will be provided for each technological process and the total manufacturing process.

The following problems arise even in this simple cost model:

(1) The electrical characteristics of the output of two alternative technological processes may differ.

(2) The quality of two alternative processes may differ.

(3) Synergistic effects of combining various processes may need consideration.

In the initial model implementation, the material input to any technological process i will be M_i units. If y_i is the process yield and r_i is the number of input units constituting one output unit (e.g., 7.35 g per wafer), then the output M_i of this process will be $(M_i/r_i)y_i$. The number of input units scrapped in the process will be $M_i - M_i' r_i = M_i(1-y_i)$.

Figure 4 depicts a technological process used in the manufacture of solar cell array modules. M_i incoming units valued at $\$X_i$ per unit are processed. Direct material, direct labor, and overhead increase the value of each unit to $\$X_i'$. M_i' units leave the process and enter the next step; the remaining input units are

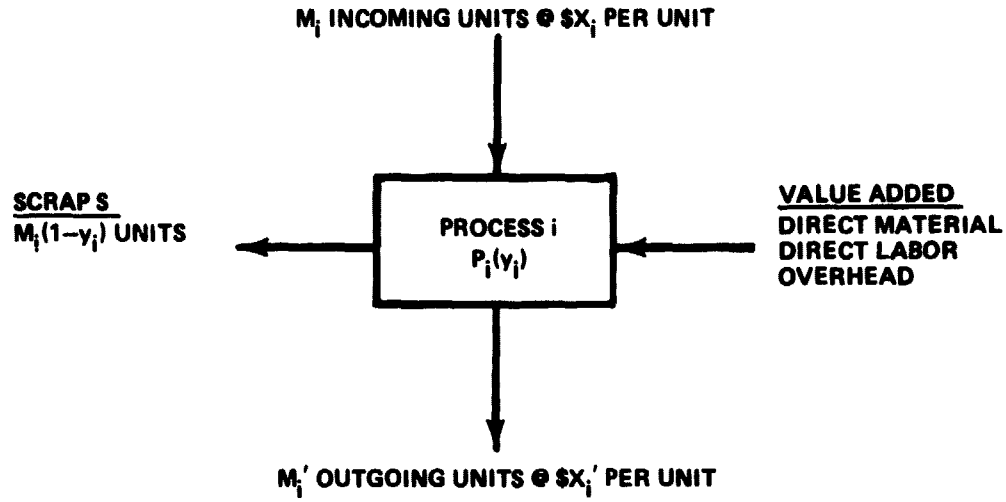

Fig. 4. Technological process representation

scrapped, with the salvage value being used to reduce process overhead. The average output unit cost X_i' is determined from process cost information, as shown in Appendix C.

It is important to note that the number of units entering a process normally will be greater than the number leaving the process. Hence, the capacity requirements of various processes may differ. This simple model assumes that flow is from one process to the next; no feedback of units to an earlier stage is currently permitted. Therefore, for a given megawatt requirement, the processing requirements of each technological process can be determined and then the cost of processing a unit computed ("overhead" is volume dependent, so the larger the volume the lower the overhead per unit). Appendix D shows a possible format for cost outputs of each process.

Once a description of each technological process has been made (see Appendix E), the user of the model must specify the output requirements (megawatts), the technological processes to be used, and the electrical characteristics of the final solar cells (electrical characteristics will be dependent upon the process used). The model will then compute the cost of output requirements and provide detailed cost estimates on a process basis. Alternative strategies can be explored. Also, sensitivity of cost to various parameters can be studied by varying the individual parameters.

Once a small number of feasible alternatives have been selected, a detailed financial analysis can be made of each alternative. This analysis could use a simulation approach in order to incorporate uncertainty rather than the deterministic

approach utilized in the initial screening process in order to estimate the risk involved in each alternative scheme.

This model should facilitate the analysis of alternative manufacturing approaches. It is only a first approximation, however, whose primary purpose is to systematize the financial analysis and permit comparisons with current state-of-the-art cost estimates. This initial model will need enhancements to incorporate some or all of the following items:

(1) Multi-year analysis capability utilizing discounted cash flow techniques.

(2) Distribution of electrical characteristics to represent the "quality" of individual processes. This would be based upon the performance approach described below.

(3) Synergistic effects of combining certain processes.

The selection of those features to be implemented will depend upon the number of different process combinations to be analyzed and the accuracy to which process parameters can be estimated.

The first test of this procedure is under way. The costs at each step for manufacturing solar array modules by existing procedures have been developed and these are being incorporated into this model. Insight into the refinements required to produce a realistic assessment of processing costs should then be forthcoming.

Thus far, our emphasis has been on developing processing costs on a per unit area basis. Since it is the goal to produce array modules which minimize the cost on a \$/W basis, it is necessary to evaluate the impact on module efficiency of each technological processing step. The starting point is the cell efficiency, η = power per unit area/irradiance (Irr). Since the Irr is taken to be fixed, the electrical power density P is directly calculable from an efficiency value. For air mass 1 irradiance on a 10% efficient cell $P = 92.5\ W/m^2$. In terms of the major electrical parameters of the cell J_{sc}, V_{oc}, and F, this P is

$$P = J_{sc} \cdot V_{oc} \cdot F$$

The values of these cell parameters for a 10% cell will be used as an arbitrary set of reference values I_r, V_r, and F_r against which our computed cell performance will

be compared. Each cell parameter is a known function of a number of physical variables such as carrier lifetime, surface recombination velocity, etc. Any single process may affect one or more of these variables and thereby affect the cell parameters. The values of the cell parameters, and, hence, a value of P, will be computed for the expected ranges of variables associated with this process while holding all the other variables fixed and equal to those of the reference cell. Then the ratio P/P_r is defined as the "performance index" (PI) for this process.

Any sequence of processing steps has a corresponding set of PI's; an overall figure of merit for the sequence will simply be the product of the individual PI's, provided that the processes are independent of each other. Thus, a figure of merit of 1 corresponds to a 10% cell. It should be clear that in order to obtain a module efficiency of $\geq$10%, the cell figure of merit will have to be strictly >1.

B. EVALUATION OF 1975 SOLAR ARRAY COSTS

As a first step in this study, and to provide a baseline for further cost estimates, we have evaluated the solar array cost estimate provided at the First Task Integration Meeting by JPL. The estimate provided included no "overhead" considerations by design. Beginning with the steps defined in that estimate, we have included overhead factors and have adjusted the processing yield terms to reflect our experience in this type of manufacturing. It should be noted that the JPL estimate began with polycrystalline silicon as a starting material and included costs for ingot growing and slicing. For completeness, we have included these same processes in our analysis of that estimate although we recognize that the Automated Array Assembly portion of the LSSA Program does not deal directly with that portion of this problem. The estimates for this portion can be fairly easily made because the art is well known.

1. Yields

In several cases the yield factors we estimate for the various processes are different from those assumed for the JPL estimate. The yields for each of the processing areas used for our calculation are given in Table 1.

Table 1. Process yield estimates

Process	JPL Yield	RCA Estimated Yields
Crystal growing	80	75
Slicing	95	85
Polish etch	100	96
Diffusion	95	95
Metallization	100	96
Test	80	80
Array production	100	96

Cost adjustments were made accordingly.

2. Labor Costs

Because of the basic nature of the JPL estimate, labor efficiency factors were not considered. Secondary operations such as handling, packing, inspections, etc., were not present in the JPL analysis.

An 85% labor efficiency was used in all process operations in the RCA study. A multiplication factor over the JPL labor cost calculation was used. These factors were judgment factors based on comparison of alike processes in actual high volume production. See Table 2.

Table 2. Labor cost estimates

Process	JPL Labor Cost	RCA Labor Factor	RCA Estimated Cost: Yield and Labor Factored
Crystal growing ($/g)	0.00972	1.3/0.85	0.0143
Slicing ($/cell)	0.0827	1.0/0.85	0.109
Polish etch ($/cell)	0.0067	1.3/0.85	0.011
Diffusion ($/cell)	0.0210	1.3/0.85	0.032
Metallization ($/cell)	0.0212	1.3/0.85	0.034
Test ($/cell)	0.001	1.5/0.85	0.002
Array production ($/cell)	0.080	1.5/0.85	0.140

3. Direct Expense

Direct expense is defined as additional direct cost items, other than direct materials or direct labor, associated with the manufacturing of the product. Direct expense costs increase linearly with production volume.

The direct expense cost items considered in the RCA analysis are:

(1) Supplies expense - chemicals, secondary materials, workclothes, tools, machine parts, holders, safety items, jigs, and fixtures.

(2) Indirect labor expense - foreman, quality control, overtime, night shift bonus, machine attendants, handling, etc.

(3) Power and gasses - direct measurable power and gas consumption or special power and gas requirements for the process.

(4) ESE (employees' service expense) - fringe benefits amount to 30% of base salaries.

Listed by process areas, a direct expense factor has been set up in our study. Areas that have high direct expense cost items are usually the areas with equipments requiring parts, power, and gasses significantly above those used to maintain the normal plant services.

A direct expense factor may be applied against the labor content in the process area. Some expense areas with a large labor content and minimal process expenses have a 1.0 direct expense factor against the total labor content.

Areas such as crystal growing can have a direct expense factor of 2 to 3 against labor cost because of high expense items.

In the RCA study the JPL "supplies cost" was included and considered as part of the direct expense. A factor based on high volume production experience was used.

These direct expense factors applied against labor content in each process area are listed in Table 3.

Table 3. Direct expense factors

	JPL Supplies Cost	Factor Based on Labor Cost	RCA Direct Expense
Crystal growing ($/g)	0.014	2.75	0.039
Slicing ($/cell)	0.042	2.30	0.250
Polish etch ($/cell)	0.007	2.30	0.011
Diffusion ($/cell)	0.021	2.30	0.032
Metallization ($/cell)	0.021	1.00	0.034
Test ($/cell)	0.001	1.00	0.002
Array production ($/cell)	0.050	1.00	0.140

4. Overhead

In the RCA study, overhead, the catchall of costs, includes: taxes, insurance, rent, administration costs, process engineering, equipment engineering, quality control engineering, furnace, rearrangement expense, superintendents, plant maintenance, telephone, group conference, standard power and gasses, heat, air conditioning, etc.

In this study, a 0.5 factor based on labor cost appears to satisfy a large-scale service and manufacturing overhead operation.

5. Interest and Depreciation

The numbers used in the RCA study for interest and depreciation were obtained from the JPL report with modifications due to RCA applied yields.

A summary of the costs for producing solar array modules is given in Table 4. In Tables 5 through 11, each processing area is listed with the RCA and JPL estimates. The total on each sheet is the cumulative total cost as the device is being processed. This entire analysis is based on processing a nominally 75-mm-diameter wafer. For a cell efficiency of 10% and assuming a reduction to 9% when the cell is incorporated in a module, the cost is $10/W. It must be noted that this value does not include post-manufacturing expenses such as marketing and profits.

Table 4. RCA cost estimation summary

	$/Cell	%	Major Step	Material	Labor	Interest & Depreciation	Direct Expense	Overhead Expenses
Polycrystalline silicon	1.115	28.3		1.115				
Labor	0.184	4.7			0.184			
Interest & depreciation	0.072	1.8				0.072		
Direct expense	0.506	12.8					0.506	
Overhead expense	0.092	2.3						0.092
Subtotal	1.969	49.9	Ingot	1.115	0.184	0.072	0.506	0.092
Slice & clean labor	0.162	4.1			0.162			
Interest & depreciation	0.073	1.9				0.073		
Direct expense	0.372	9.4					0.372	
Overhead expense	0.081	2.0						0.081
Subtotal	0.688	17.4	Slice		0.162	0.073	0.372	0.081
Chemical polish	0.061				0.016		0.037	0.008
Diffusion	0.053				0.014		0.032	0.007
Glass remove	0.053				0.014		0.032	0.007
Back remove	0.037				0.014		0.016	0.007
Metallize	0.376			0.243	0.044	0.023	0.044	0.022
Electrical test	0.005				0.002		0.002	0.001
Interest & depreciation	0.188					0.188		
Subtotal	0.773	19.6	Cell	0.243	0.104	0.211	0.163	0.052
Assembly material	0.110	2.8		0.110				
Labor	0.140	3.6			0.140			
Interest & depreciation	0.055	1.4				0.055		
Direct expense	0.140	3.5					0.140	
Overhead expense	0.070	1.8						0.070
Subtotal	0.515	13.1	Array	0.110	0.140	0.055	0.140	0.070
Total	3.946			1.468 37.2%	0.590 14.9%	0.413 10.5%	1.18 30.0%	0.295 7.4%

Table 5. Crystal growing cost estimate

	Yield	Efficiency	Material	Labor	Direct Expense	Interest & Depreciation	Overhead	Total
Material $65/kg	75	-	86.67 (81.25)					
Labor ($4 x 14 h)/8000) 30% for other	75	85		14.30 (9.72)*				
Expense 275% includes ESE, supplies	75	85			39.33 (13.89)*			
Interest & depreciation	75	85				5.65 (5.23)*		
50% Labor, est. overhead							7.15	
Total			86.67	14.30	39.33	5.65	7.15	153
*JPL basic estimate			81.25	9.72	13.89	5.23	-	110

Table 6. Slicing cost estimate

	Yield	Efficiency	Material	Labor	Direct Expense	Interest & Depreciation	Overhead	Total
Slice cost			0.637	0.105	0.289	0.041	0.053	1.13
Material	85	85	0.750	0.123	0.340	0.048	0.062	
Labor slice & clean				0.109 (0.083)*				
Expense 230% includes ESE, supplies					0.250 (0.0421)*			
Interest & depreciation						0.051 (0.0452)*		
50% Labor							0.055	
Total			0.750	0.232	0.590	0.099	0.117	1.86
*JPL basic estimate			0.628	0.158	0.150	0.86	-	1.02

Table 7. Polish etch cost estimate

	Yield	Efficiency	Material	Labor	Direct Expense	Interest & Depreciation	Overhead	Total
Slice cost	96	85	0.781	0.241	0.615	0.103	0.122	
Labor + 30%				0.011 (0.007)*				
Direct expense 230%					0.025 (0.031)*			
Interest & depreciation						-		
Overhead 50%								
Total			0.781	0.252	0.640	0.103	0.128	2.02
*JPL basic estimate			0.628	0.165	0.181	0.086	-	1.06

Table 8. Diffusion cost estimate

	Yield	Efficiency	Material	Labor	Direct Expense	Interest & Depreciation	Overhead	Total
Polish wafer cost	95	95	0.822	0.265	0.674	0.108	0.135	
Labor + 130%				0.032 (0.021)*				
Direct expense 230%					0.059 (0.084)*			
Depreciation & interest						0.0014		
Overhead 50%								
Total			0.822	0.297	0.733	0.109	0.151	2.2
*JPL basic estimate			0.661	0.194	0.275	0.092	-	1.2

Table 9. Metallization cost estimate

	Yield	Efficiency	Material	Labor	Direct Expense	Interest & Depreciation	Overhead	Total
Diffused wafer cost	96	85	0.856	0.309	0.763	0.114	0.157	
Material			0.187 (0.1793)					
Labor + 130%				0.034 (0.0212)*				
Direct espense					0.034			
Interest & depreciation						0.0175 (0.0168)*		
Overhead 50%							0.017	
Total			1.043	0.343	0.797	0.132	0.174	2.6
*JPL basic estimate			0.840	0.216	0.275	0.108	-	1.4

Table 10. Test cost estimate

	Yield	Efficiency	Material	Labor	Direct Expense	Interest & Depreciation	Overhead	Total
Metallized wafer cost	80	85	1.30	0.429	0.996	0.165	0.218	
Test labor 150%				0.002 (0.001)*				
Direct expense 100%					0.002			
Interest & depreciation						0.180 (0.180)*		
Overhead							0.001	
Total			1.30	0.431	0.998	0.345	0.219	3.4
*JPL basic estimate			1.05	0.270	0.343	0.315	-	1.9

Table 11. Array production cost estimate

	Yield	Efficiency	Material	Labor	Direct Expense	Interest & Depreciation	Overhead	Total
Tested cell	96	85	1.36	0.449	1.04	0.358	0.225	
Material			0.11 (0.102)*					
Labor 150%				0.140 (0.080)*				
Direct expense 100%					0.140 (0.050)*			
Interest & depreciation						0.055 (0.053)*		
Overhead 50%							0.070	
Grand total			1.47 37.2%	0.590 14.9%	1.18 30.0%	0.413 10.5%	0.295 7.4%	3.95
*JPL basic estimate			1.15 51%	0.350 15%	0.393 17%	0.368 16%	-	2.26

C. BASIC STUDIES

1. Materials Matrix

This segment of the report is concerned with our work in developing the silicon quality materials matrix (see Fig. 1). Since work in this area has just begun, we shall outline what we plan to accomplish.

In filling out the silicon quality materials matrix we have started with the cost and quality of single crystal silicon cut from pulled ingots. This can be prepared in quantity and with properties sufficient to give the highest efficiency solar cells. Such materials, the highest quality silicon available under present state-of-the-art, can be purchased today, sliced and etched, for $4.50 per 3-inch wafer (15 mils thick, 20 to 40 ohm cm resistivity, p-type (100) orientation). Proceeding from this point we are reviewing what the state-of-the-art cost and quality is for each of the other points in the matrix. For those points which are not yet state-of-the-art (i.e., rolled sheet) as well as those which are, we shall try to estimate what kind of cost reduction may be expected for a given change in the state-of-the-art and what the probability of success will be for achieving it. As an example, consider the discussion of epitaxial growth in the processing cost section below. The three largest expense items are H_2, HCl, and power. While redesigning the present reactors will effect some significant cost savings, what is really needed is a new design. In the event that silicon ribbon substrate is available, a reactor could be designed in which the ribbon moves continuously through the chamber and is directly heated by electrical contacts. This would significantly reduce power use, and would also reduce the HCl since the susceptor would be eliminated. Finally, the need for large H_2 flows would also be reduced since such a reactor would not have to operate in a high displacement mode as uniformity of deposition rate over the length of ribbon in the chamber is not a prime requirement. In the next quarter we shall estimate the savings to be expected as well as the probability of success in developing such equipment.

In each case, a similar analysis will be performed so that present and future costs and quality of silicon material will be available for the processing portion of this program.

2. Processing Studies

The first step in determining the processing costs for unit processes is to break the costs down into four categories: (1) consumed materials, (2) capital equipment, (3) labor, and (4) space. Analysis will then give a first order estimate of those processing steps which are too expensive in terms of today's technology. Cost reductions for these steps can be projected; the effort subsequently required and the probability of realizing these reductions can then be assessed. The first phase, gathering data on epitaxy, diffusion, cleaning, and etching operations, has now been completed.

Based on processing currently used, the *consumed materials costs* for epitaxial growth, diffusion, etching and cleaning processes have been evaluated. Typical flow rates through equipment and typical consumption rates for batch processes have been employed. From present practice, based on 2-in. or 2-1/4-in.-diameter wafers, extrapolations to 100 cm^2 have been made, assuming that the format of the silicon (web, ribbon, or wafer) will not affect the consumed materials costs appreciably if the silicon area is held constant.

Included in consumed materials are: (a) all liquid reagents used, including acids, bases, solvents, DI water; (b) all gases, including those used to provide furnace atmospheres, protective curtains, etc.; and (c) electricity, including that consumed in hoods, hotplates, motors, furnaces or equipment directly associated with the unit process.

The following costs were not included: boats, jigs, fixtures, furnace liners, glassware, etc., which is slowly consumed or replaced. These are typically a small part of the processing cost and their purchase price is strongly dependent on the exact shape and size. Also, the costs of electricity consumed in air conditioning, heating, and lighting are not included. These will be part of the "space" allocation for equipment. It was assumed that no materials are consumed in any testing or inspection step.

The costs in this analysis are not yet yielded. Since yields are less than 100% for any process, the costs must be multiplied by an appropriate factor. These factors are included in our formal cost accounting procedure.

a. Cleaning. The costs for consumed materials in each of the processing steps evaluated, based on current state-of-the-art technology, are shown in the second column of Table 12. From this analysis it can be seen that several cleaning processes are relatively inexpensive in terms of consumed materials: chemical cleaning with sulfuric/peroxide, megasonic cleaning,[1] or plasma techniques can be below $0.005. Particulate removal with wafer scrubber or megasonic equipment is about $0.01. This suggests that the materials consumed in cleaning with present day technology are within the limits set by $0.50/W.

Table 12. Current costs of processing

Processing Step	Consumed Materials per 100 cm^2 ($)	Capital Costs ($)	Rate per Unit (2¼-in.-diam wafers/h)	Rate per Hourly Operator (2¼-in.-diam wafers/h)	Space Needed (ft^2)
Diffusion sources					
Liquid ($POCl_3$)	0.014	9,000	300	1200	100
Spin-on commercial	0.29	10,000	500	1000	300
in-house	0.005				
Spray-on in-house	0.005	9,000	700	700	100
Solid source (e.g., BN)	0.06	9,000	50	300	100
Doped oxide source (silane CVD)	0.134	60,000	150	150	200
Electroless nickel source	0.018	9,000	250	250	100
Source strip/etch	0.006	9,000	400	400	100
Diffusion drive	0.0044	9,000	300	1200	100
Etching of silicon	0.095	9,000	600	600	100
Cleaning					
SC-1, 10% HF, SC-2	0.074	18,000	1200	600	200
Sulfuric peroxide (system "Z")	0.0014	9,000	1200	750	100
Plasma commercial gas	0.042	13,000	300	600	100
in-house gas	0.004				
Wafer scrubber	0.004	13,000	160	160	100
Megasonic	0.013	25,000	200	200	100

Costs of materials consumed in cleaning can be further reduced by (a) recycling DI water in a Hydronomic* type recycling system, and (b) by bulk purchase

[1]"Megasonic cleaning," an RCA proprietary cleaning technique, described in U.S. Patent 3,893,869 issued July 8, 1975 to A. F. Mazer and S. Shwartzman,
*Millipore Corporation trademark.

and bulk storage of reagents in large tanks. Estimates of the effectiveness of these approaches are indicated in the second column of Table 13 which gives projected costs based on reasonable extrapolations of today's technology.

Table 13. Projected costs of processing

Processing Step	Consumed Materials per 100 cm^2 ($)	Rate per Unit (2¼-in.-diam wafers/h)	Rate per Hourly Operator (2¼-in.-diam wafers/h)	Space Needed (ft^2)
Diffusion sources	No change			
Liquid ($POCl_3$)	No change			
Spin-on (in-house)	No change			
Spray-on				
Solid source (BN)	No change			
Doped oxide (silane CVD)	0.025[a]	150	150	300
Source strip/etch	No change			
Diffusion drive	No change			
Etching of silicon	0.02[b]	600	600	100
Cleaning				
SC-1, 10% HF, SC-2	0.50[c]	1200	600	200
Sulfuric peroxide	0.0010[c]	1200	750	100
Plasma - in-house gas	No change			
Wafer scrubber	0.0010[c]	300[d]	600	100
Megasonic	0.010[c]	200	200	100

a Assumes availability of silane at $ 5.00 per kg.
b Assumes lower cost reagents by bulk purchase, storage, extended reagent life by replenishment and reuse.
c Assumes decreased reagent costs by bulk purchase, storage, DI water recovery, reuse.
d Assumes mechanization of wafer scrubber plus reagent cost reduction by water recycling.

b. Diffusion. Deposition of a diffusion source can be accomplished for less than $0.02 in consumed materials using conventional $POCl_3$, spray-on, or spin-on techniques. Materials for CVD (silane) doped oxide sources represent about $0.13. If silane becomes available at $5.00/kg, an aim of the Union Carbide contract with JPL[2], the cost of materials for a silane oxide could be brought down to about $0.03 since most of the cost of the deposited oxide is in the silane starting material. From this analysis it is concluded that a variety of diffusion techniques are available in today's technology that meet the $0.50/W constraint, and that others are likely to be consistent with this goal if present programs of cost reduction are successful.

c. Etching. The cost of materials consumed in stripping an oxide source and rediffusing that source, if required, would add only about $0.01 to the processing.

Etching of silicon is an expensive process if material is to be removed from the entire wafer. The cost of about $0.10 (Table 12) represents removal of about 1 mil from the surface of a wafer and is largely in the costs of the reagents employed. Bulk purchase of reagents and more efficient replenishment of spent material could lower etching costs to $0.02 per 100 cm^2 (Table 13). If only the rim of a wafer is to be etched, then costs will drop by a factor of 10 or more. In this case, it is likely that etching costs are already consistent with a $0.50/W goal.

d. Epitaxy. Epitaxy is the most expensive of the processes evaluated in this phase of the program. Current estimates for 100 cm^2 suggest that a 1-mil layer can be grown on 100 cm^2 using present day technology for about $1.00 in consumed materials.*

The costs of the materials consumed, hydrogen, silicon source material, etchant, and electricity, are very large in epitaxy. Cost reductions can be projected, however, that may bring epitaxial growth into the range acceptable for a $0.50/W cell. At present, the hydrogen gas, used as diluent and reducing agent, is disposed of after one pass through the reactor. With suitable recovery techniques, such as those employed in the production of polycrystalline silicon from

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[2]W. C. Brenaman, "A Process for High Volume, Low Cost Production of Silane," prepared by Union Carbide under JPL Contract 954334.

*To achieve this goal, the susceptor would have to be designed to accommodate the silicon in whatever format it was provided.

trichlorosilane, the cost of hydrogen could be greatly reduced. Assuming an 80% recovery at a cost per unit volume of 10% of new hydrogen, the costs for hydrogen can be brought down to about one-fourth of the costs shown in Table 12. In addition, trichlorosilane can be substituted for silicon tetrachloride. This substitution lowers the cost of the silicon source, improves the thermodynamic efficiency of the deposition reaction, and permits increased deposition rates at lower temperature. This will lower the silicon source cost by almost a factor of 10 and will also decrease the electricity consumed by a factor of at least 2. Recovery of spent HCl from the effluent gas would permit lower cost stripping of susceptor blocks, decreasing the HCl cost by almost 10 times. With these modifications, the cost of consumed materials can be brought to about $0.25 for a 1-mil layer on 100 cm^2 as shown in Table 13. Clearly, increased costs result from the higher capital and operating costs of the recovery equipment. This is still under evaluation.

With additional engineering effort, the capacity of the RCA barrel reactor could be doubled, providing additional cost savings through improved susceptor design and through greater batch size at little additional capital cost.

Depending on the format of the starting silicon, it may be necessary to scale up the reactor design before solar cell manufacture could even be evaluated. Unless such programs are strengthened it is unlikely that the technology will be available in the 1980 time frame.

With a cost of $0.10 to 0.20 for an epitaxial layer, epitaxy can seriously be considered for solar cell manufacture, assuming there is a corresponding savings possible in the starting material or in the assembly processing when epitaxial construction is employed.

e. Other costs. Table 12 also shows the approximate *capital cost* of the unit equipment for each process, along with an estimate of the production rate available from this equipment. *Labor costs* can be determined from the production rates for an hourly operator included in Table 12. These are based on experience in the individual processes used for power transistor manufacture. Finally, the rough *space requirements* for each processing step are given in Table 12. From these data, assuming depreciation rates, labor costs, and rental costs, the rough costs for each process can be determined. These data then will be incorporated in the

cost accounting model described above. Completion of this analysis is the principal goal of the program for the next quarter.

f. Ion Implantation. We have begun to compile the information required to estimate present and future costs of ion implantation. This process offers a controlled, high purity diffusion source as well as a technique for directly creating a shallow junction profile. Its utility in fabrication of low cost solar cells depends on the possibility of utilizing lower quality substrates or of achieving profiles which permit higher cell efficiency. An example is an active system in which junctions are not created in regions where a severe defect exists in the substrate. This work has not progressed to the point where conclusions can be drawn.

g. Metallization. The metallization processes being considered at the moment include evaporation from tungsten coils, electron-beam evaporation, magnetron sputtering, and silk screening. Metallization materials being considered include aluminum and titanium-silver.

The analysis of the costs of silk screening of pastes on solar cells includes both a hand-fed machine and an automatic (magazine-fed) machine. Presently available automatic silk screening equipment has been designed for use with ceramic substrates such as 96% Al_2O_3 and has been reported to result in breakage problems when used with silicon wafers. While automatic handling of silicon wafers without breakage is considered feasible, development work would be necessary to improve commercially available magazine-fed screen printers to handle large silicon wafers.

Our preliminary estimate of the difference in cost for silver vs aluminum silk-screened metallization indicates that it would cost approximately 25% more for silver than for aluminum.

Silk screening involves a tradeoff between substrate area and resolution. Linewidth of 250 μm can be attained on 100-mm wafers; short runs of 125-μm linewidth can be attained on smaller substrates. It is desirable to use a metallization pattern in which occasional opens in collection grid lines do not significantly reduce cell efficiency. The impact of cell size begins to become apparent at this point. The costs for these various processes are being developed for the cost accounting procedure described in the beginning of this section.

3. Array Fabrication

Present space photovoltaic power supply assemblies are built up from 2 x 2 cm or 2 x 4 cm cells wired together in a series-parallel arrangement which meets the voltage and power needs of the application. Typically the cells are bonded to a honeycomb substrate using a silicone adhesive and are protected from the space environment by microsheet glass covers. The assemblies are designed to meet their most severe environmental requirement (thermal cycling) by careful consideration of stress in the cell interconnect and its metallurgical bond to the cell. Soldering methods have been used almost exclusively for this purpose. Automation of any of the assembly processes has never been justified since the volume or the produced product could not justify the required capital equipment.

The terrestrial application calls for substantially reduced constraints due to weight and environmental requirements. As a result, the baseline module will use circular or semicircular cells mounted on a fiberglass substrate. The circuit will consist of 12 parallel strings of 30 cells in series. This will deliver 8 A at 12 to 14 V dc in a 3- x 4-foot panel if the semicircular cell format is used. The baseline interconnection technique will utilize a simple nickel-plated copper ribbon reflow soldered in a continuous belt furnace. Automated ultrasonic and resistance welding equipment exists, and these interconnection techniques may be considered as alternate baseline methods. Finally, environmental protection will be provided by enclosing the circuit behind a glass window.

Implicit in high volume production is a high degree of automated material handling. When the material is large pieces of very fragile silicon sheet, the handling techniques must not only be fast but gentle if high yield is to be maintained. Existing equipment for transferring, indexing, aligning, and positioning silicon die is being studied for its application to wafer or sheet size elements. Such techniques as air guides, vacuum chucks, x-y drives, magazine loaders and unloaders will ultimately be incorporated into the overall processing system. While the design of such equipment cannot be described adequately in timely fashion to support the baseline cost study, this data base will support the conceptual design work which must be completed to eliminate process cost bottlenecks which we know exist.

In addition to processes and equipment, the other important factor determining panel cost is its design. Materials, sizes, and tolerances all affect cost in an

important way. In the first quarter we have identified the following three parameters as important in determining panel cost:

(1) Electrical circuit sorting requirements

(2) Thermal structural stress at the cell

(3) Cell operating temperature

Existing software packages have been identified in each area. The most complex analysis, by far, is the design of structural, cell size, substrate material, bonding and interconnect method, parameters which result in reliable module operation in the terrestrial environment. We are using Ansys, a commercially available finite element program which was developed and is continually upgraded by Swanson Analysis Inc. The effort in the first quarter has been directed to describing the problem in terms of the methodology of the program out of the enormous number of alternatives which can be considered. In this study we have defined our program as outlined below. The costs associated with manufacturing the designs of choice will be incorporated in the cost accounting procedure described in the first section of this report.

D. OUTLINE FOR STUDY OF AUTOMATED ASSEMBLY OF PHOTOVOLTAIC ARRAY MODULES

I. Establish Cost Baseline

- A. Establish Panel Design
- B. Assume 3-In.-Diam. Cells Per JPL & RCA Cost Estimates
- C. Cost AR Coating Alternatives
  1. SiO
  2. TaO_5
  3. $MgFl_2$
- D. Cost Interconnection Alternatives
  1. Soldering
  2. Resistance Welding
  3. Ultrasonic Welding
- E. Use Fiberglass on Aluminum Substrate
- F. Bond Cells Using RTV
- G. Use Glass Cover
- H. Test at Panel Level

II. Check Baseline Against Current Low Cost Panel Suppliers, if Possible

III. Identify Cost Breakdown Between:

- A. Materials
- B. Labor for Each Fab Step
- C. Testing Labor and Equipment

IV. Develp Conceptual Designs which Can Lead to Lower Cost.
Consider at Least:

A. Large Cells
B. Material Alternatives
C. Alternate Contact Techniques
D. Interconnection Alternatives
E. Substrate Alternatives
F. Protection Alternatives
G. Testing Requirements
H. Mechanical Assembly Alternatives

V. Analytic Support

A. Establish a Range of Operating Temperatures Based on US Climate and Panel Design
B. Establish Design Limitations Based on Structural Considerations including at Least
   1. Materials of Construction
   2. Low Cost Assembly Techniques
   3. Temperature Extremes
   4. Static and Dynamic Wind Effects
C. Establish a Basis for Sorting and Testing Criteria by Examining System Performance

VI. Cell Materials and Size

A. Establish Physical Parameters for the Three Most Promising Material Alternatives:
   1. Ribbon Silicon
   2. EPI on Poly or Sapphire
   3. Single Crystal Wafer
B. Parameters will Include:
   1. Dimensional Tolerance
   2. Surface Finish
   3. Thickness
   4. Bow and Taper
C. Establish Handling Requirements & Yield for Large Cells
D. Establish Performance Limits for Large Cells

VII. Interconnect Alternatives

A. Establish Cell Contact Requirements for Alternate Connection Techniques.
   These might include:
   1. Contact Material & Thickness
   2. Contact Pattern & Tolerance
   e. Method of Application
B. Establish Cost Parameters for Each Alternative Connection Method
   1. Operating & Maintenance Cost
   2. Capital & Development Cost
C. Identity Technical Characteristics of Interconnects
   1. Electrical Resistance
   2. Pull Strength
   3. Fatigue Life
   4. Repeatability and Reliability
   5. Nondestructive Testing Means
D. Develop Possible Integration with Other Assembly Steps
E. Identify Necessary Material Handling Equipment

VIII. Substrate Alternatives

A. Material Choices Include:
   1. Flexible Films
   2. Structural Materials
   3. Composite Structures
   4. Glass
   5. No Substrate

B. Structural Requirements
   1. Bonding
   2. Anchor
   3. Integration with Protection

C. Cost
   1. Dual Energy Output
   2. Integration of Processing Steps

D. Engineering Characteristics
   1. Temperature Stability and Strength
   2. Structural Properties
   3. Environment Resistance
      - Sunshine
      - Moisture
      - Wind & Sand Abrasion
   4. Electrical Properties
   5. Compatibility with Automation Process
      - Exposure to Process Temperature and Materials
      - Inspection of Assembly
      - Reduction of Process Flexibility

IX. Protection Alternatives

A. Assess the Threat
B. Interface JPL Integral Coating Program
C. Assess Protective Structure
   1. Impact on Array Structure
   2. Cost
   3. Possibility for Absorbing Part or All of Cost in Another Function
      - Building Heat
      - Building Structure

X. Testing Requirements

A. Incoming Inspection
B. In-Process Testing
C. Acceptance Criteria
D. Automation
E. Equipment Design and Cost
F. Electrical or Optical Signatures for Thermal or Structural Properties
G. Quality Control

XI. Mechanical Assembly

A. Component Handling
B. Final Wiring
C. Interface with Building Systems
D. Packaging and Handling

SECTION IV

CONCLUSIONS

In the absence of the demonstrated utility of our entire analytical procedure, which will be completed on time by the end of the second month, any conclusions would have to be considered extremely tentative; therefore, no definite conclusions are offered in this report.

However, based on the above estimates, it seems that the costs of processing a solar cell junction itself in terms of the materials consumed in the processing - cleaning, diffusion - are consistent with the goal of $0.50 per watt, i.e., a few cents per watt for this step. A program to cost-reduce epitaxial growth would be needed to meet this constraint, but the directions for this program can already be defined and the expected savings can be estimated. Further, initial cost estimates indicate that silk screening offers the lowest cost metallization capabilities if the resolution attainable (250-μm linewidth) is acceptable. This, of course, is cell-design sensitive and is being evaluated.

SECTION V

RECOMMENDATIONS

The scope of this analysis is very broad and in many instances the projections rely on data which either do not exist or are only now being developed. For example, performance data on sheet material grown by nontraditional methods such as those under development in Task II of the LSSA Program would be useful. This is a problem which we recognize is appreciated by everyone associated with this program, and will not be belabored. Many of these problems are subject to analysis and reasonable estimates can and will be made. However, to the extent that information may be made available at an early point in our analysis, the significance of this study will be increased. At this point in the program our only recommendation is to maintain vigilance in this area.

SECTION VI

NEW TECHNOLOGY

There are no new technology reports in this interval.

REFERENCES

1. "Megasonic cleaning," an RCA proprietary cleaning technique, described in U.S. Patent 3,893,869 issued July 8, 1975 to A. F. Mazer and S. Shwartzman.
2. W. C. Brenaman, "A Process for High Volume, Low Cost Production of Silane," prepared by Union Carbide under JPL Contract 954334.

APPENDICES

APPENDIX A

DEFINITION OF TERMS

Process:	a group of operations associated with a specific technology step. Each process will be considered to be a separate cost center.
Cost center:	smallest step in the manufacturing operation for which cost data is maintained.
Direct materials:	materials which are used in direct proportion to the number of incoming units.
Indirect materials:	materials which are constant over a range of activity.
Direct labor:	labor used in direct proportion to the number of incoming units. (Does not include fringe benefits.)
Indirect labor:	labor which is constant over a range of activity, e.g., supervisor salaries. (Does not include fringe benefits.)
Direct labor efficiency:	ratio of time worked to time paid.
Variable factory overhead:	an expense which is dependent upon the level of production. It will be assumed to have the form $\alpha_1 M + \alpha_2 L$, where M is the cost of direct materials and L the cost of direct labor. (Power, gases, etc. would be included.)
Fixed factory overhead:	a cost step function based upon the quantity of sheets processed (excludes depreciation).
Depreciation:	a periodic charge (expense) based upon the level of investment.
Investment:	first cost of fixed assets employed in manufacturing. It will be a step function dependent upon the level of manufacturing activity.
R&D expense:	expenditure required to develop a specified process.
Sheet:	an entity containing one or more solar cells (the number of solar cells per sheet is assumed constant for a given analysis).

Machine efficiency:	fraction of total time machine is available for use.
Employees service expense (ESE):	cost of "fringe benefits", computed as additional fraction of total labor expense.
Interest expense:	interest on borrowed funds.
Debt ratio:	fraction of total investment financed by debt.
Process yield:	the ratio of units out to (equivalent) units in.
Salvage value:	the recovery value of units discarded in a process.
Above line expense:	an expense which is computed for the factory as a whole and then allocated to the individual processes on some basis (floor area is used currently).
Below line expense:	an expense which is computed for the factory as a whole and subtracted from "manufacturing profit" because no meaningful process allocation approach exists.