DEVELOPMENT AND FABRICATION OF IMPROVED POWER TRANSISTOR SWITCHES

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16. Abstract

A new class of high-voltage power transistors has been achieved by adapting present interdigitated thyristor processing techniques to the fabrication of NPN Si transistors. Present devices are 2.3 cm in diameter and have achieved $BV_{CEO}(sus)$ of 850 V with a maximum $h_{FE}I_C$ product of 380 A at V_{CE} = 5 V. The electrical performance obtained is consistent with the predictions of an optimum design theory specifically developed for power switching transistors. The forward SOA of the experimental transistors shows a significant improvement over commercially available devices. The report describes device design, wafer processing, and various measurements which include DC characteristics, forward and reverse second breakdown limits, and switching times.

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1. SUMMARY

The overall objective of this program is the development of device design and processing techniques which permit the fabrication of NPN transistors suitable for high-efficiency switching applications where the required BV_{CEO} voltage is in the range of 400 to 800 V. An important aspect of the program has been the increase of the emitter area over that available in present commercial devices.

The transistors described in this interim report are 2.3 cm in diameter and have an emitter area that is approximately eight times larger than that practical with a TO-3 package. This "scale-up" has been achieved without serious side-effects such as voids at the Si/header interface and non-uniformities in the emitter current distribution.

The electrical performance achieved is consistent with the predictions of the optimum design theory used for the transistor design. Specific sections of the report describe the device design, wafer processing techniques, and also various measurements which include DC characteristics, forward and reverse second breakdown limits, and switching times. Also discussed are specific areas of interest that will receive attention during the remaining portion of the contract.

2. INTRODUCTION

There is substantial evidence that large-area transistors will fill a major need in present and future power electronics efforts. For example, devices are frequently paralleled (sometimes over 100 TO-3's) in order to achieve the necessary controllable current, the necessary safe-operating area, or the necessary circuit efficiency. In addition there are certain applications where paralleling devices presents problems due to non-uniform current distribution during turn-off. In these applications a single large transistor is needed.

The obvious question is: Can larger transistors be made and still be cost-competitive? We believe the answer to this question is "yes". For example, the techniques described in this report are routinely used to produce interdigitated thyristors up to 5 cm in diameter. While the steps necessary to adapt thyristor and rectifier processing techniques to transistors are not trivial, they pose no major technological hurdles. We are confident that many of the processing and design procedures worked out for the present 2.3 cm transistors will be applicable to even larger devices.

This interim report describes our approach to the adaptation of these techniques. The first section of the report describes the basic device design, with subsequent sections dealing with processing and experimental measurements.

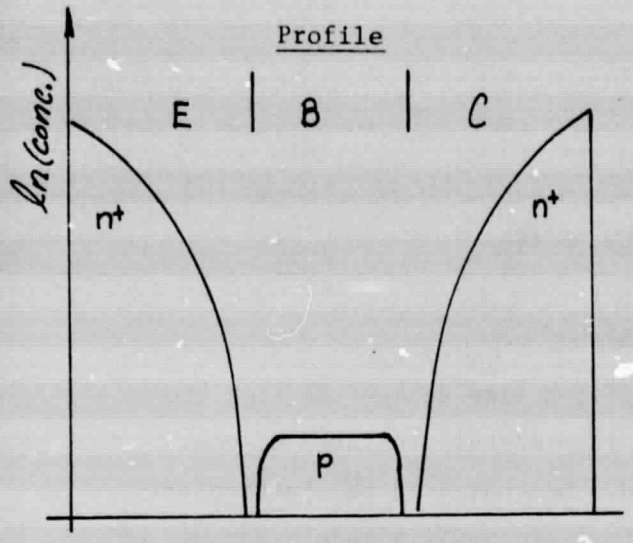
3. DEVICE DESIGN

3.1 Initial Considerations and Background

Before describing the specific device design used for the transistors, it is worthwhile to consider certain features of the different profiles that might be used. Depending on the particular application, power switching transistors are usually made using one of the profiles of Figure 1. In this section we give the reasons behind the choice made for the present contract effort.

Table 1 lists the desired DC characteristics to be achieved. From the standpoint of determining the initial device design, the most important characteristics are the blocking voltages (BV_{CEO} and BV_{CER}), the high-current conduction specifications, V_{CE} (sat) and h_{FE}, and the switching times which are listed in Table 2.

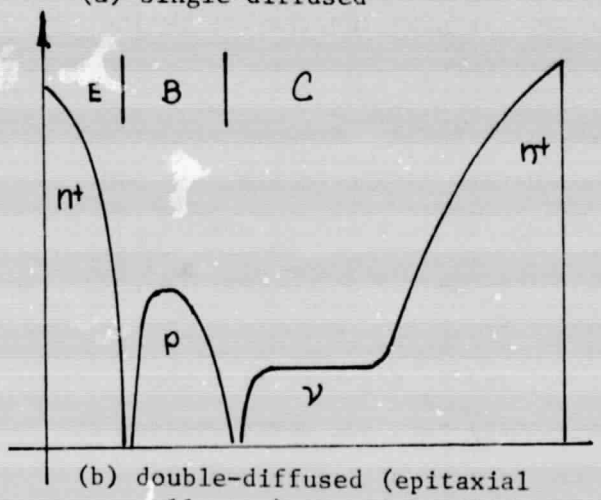
The values required for t_r, t_f, and t_s together with the BV_{CEO} and peak gain requirements, immediately rule out consideration of a single-diffused profile. This profile is also at a disadvantage because of the low current density obtainable in the on state. The pi-nu structure [1], which has lightly-doped regions on both sides of the collector-base junction, does have an advantage over a double-diffused profile with regard to the current density that can be controlled for a given h_{FE} and forward drop V_{CE}. However, this improvement is achieved at the expense of a wide, lightly-doped base region, which increases the base transit-time and significantly degrades the rise and fall times. Maximizing the on-current density is desirable from the standpoint of minimizing device size, weight, and cost. It is important to note that in some cases, a thermal dissipation requirement (e.g. a specification on junction-to-case thermal resistance) may place a bound on the minimum emitter area that can be used.



(a) single-diffused

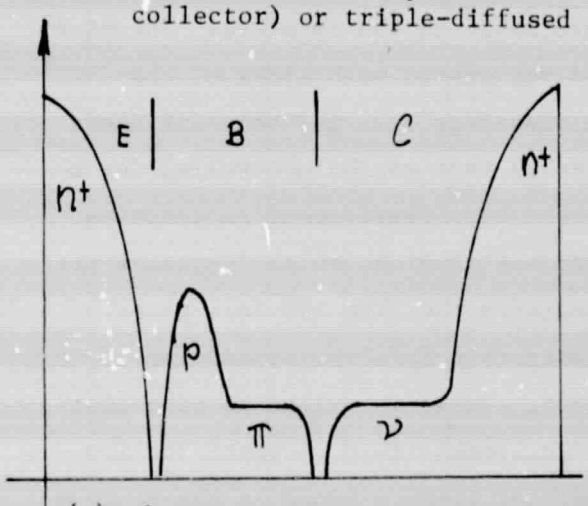
Remarks

Typical lifetimes ($\tau \approx 20$ μsec) limit BV_{CEO} to $\lesssim$ 250V for $h_{FEO} \gtrsim 30$. For a given BV_{CEO}, the on-current densities (I_C/A_E at a given h_{FE},V_{CE}) will be less than that of (b) or (c). Rise and fall times are largely determined by the base transit time and will be typically a few μsec. For a given I_C, $R_{\theta JC}$ will be less than (b) or (c).



(b) double-diffused (epitaxial collector) or triple-diffused

This profile provides the smallest rise and fall times of the three, typically in the sub-microsecond range if $BV_{CEO} \lesssim 1000V$. On-current densities can be larger than (a) but about 1/2 of (c).



(c) pi-nu

This profile has the largest on-current density for a given BV_{CEO}, which is achieved at the expense of increased rise and fall times over (b). For a given I_C and BV_{CEO}, $R_{\theta JC}$ will be greater than (a) or (b).

Figure 1 Impurity concentration profiles for various npn transistors.

Table 1 — Dc Characteristics

Symbol	Specification Number	Description	Value
$BV_{CEO}(sus)$	(1)	Minimum collector-emitter sustaining voltage, base open	600 V at 100 mA
$BV_{CER}(sus)$	(2)	Minimum collector-emitter sustaining voltage, R_{BE} = 47 ohm	800 V at 100 mA
BV_{EBO}	(3)	Minimum emitter-base breakdown voltage, collector open	8 V at 1 mA
I_{CER}	(4)	Maximum collector-emitter leakage current, R_{BE} = 47 ohm	0.1 mA at 600 V
$V_{CE}(sat)$	(5)	Maximum collector-emitter saturation voltage at I_C = 5 A, I_B = 0.25 A	0.4 V
$V_{CE}(sat)$	(6)	Maximum collector-emitter saturation voltage at I_C = 10 A, I_B = 1 A	0.8 V
$V_{BE}(sat)$	(7)	Maximum emitter-base saturation voltage at I_C = 5 A, I_B = 0.25 A	1.0 V
h_{FE}	(8)	Minimum dc forward current transfer ratio at I_C = 10 A, V_{CE} = 5 V	10
$I_{C, max}$	(9)	Dc collector current absolute maximum rating	15 A

Table 2 — Switching Times

Symbol	Specification Number	Description	RFP Value	Proposed Value	Units
t_r	(10)	Maximum collector current rise time*	0.1	0.15	μs
t_f	(11)	Maximum collector current fall time*	0.1	0.12	μs
t_s	(12)	Maximum collector storage time*	0.5	0.7	μs

*Resistive load with I_C = 5 A, $I_{B1} = I_{B2}$ = 1 A.

While the specifications of Table 1 contain no data on safe-operating-area or thermal resistance, measurement of these characteristics are part of the contract goals. In addition, the SOA will become important in future applications of the transistor. Therefore, it is believed that the double-diffused profile represents the best choice. It has the best switching performance, good on-current density (within a factor of two of the pi-nu), and good thermal dissipation capability (better than the pi-nu, but not as good as the single-diffused).

3.2 Minimum Area Needed for the DC Requirements

This section describes the results of an optimum design procedure [2], which takes the required blocking voltage, BV_{CEO} (sus), and a specification of the on-state, e.g. h_{FE} at I_C, V_{CE} as input data and then calculates a minimum A_E that will achieve both characteristics. This procedure is useful for estimating the minimum die and package size for these two specifications.

While this result is important to know for the present design, it is also worth noting that there may be reasons for increasing the metallurgical emitter area A_{EM} above the minimum value. As example:

- some additional voltage drop in the series emitter resistance R_E, which may be needed to provide ballasting for a forward SOA requirement, will reduce the effective value of V_{CE} across the "intrinsic" transistor thereby increasing the required A_E
- emitter current crowding may reduce A_E below A_{EM}
- specifications on the thermal resistance may require A_E to be larger than the minimum
- switching time considerations may require the smallest possible collector width W_C, which will deviate from the optimum W_C, and thereby require an increase in A_E. This topic is discussed further in Section 3.5.

Figure 2 shows the results of the minimization procedure using BV_{CEO} = 600 V and the I_C and h_{FE} values from specifications (5) and (6) of Table 1. It can be seen from this figure that the 5 A, V_{CE} (sat) specification is actually the most restrictive, since it requires an A_E = 0.5 cm^2. This area is larger than the 0.34 cm^2 needed for the 10 A specification.

3.3 Encapsulation Considerations

From Figure 2 it is clear that a package considerably larger than the familiar TO-3 size will be required. A considerable degree of "scaling-up" using conventional solder die-attach and wire-bonding procedures has been achieved [3] for die sizes up to 2 cm^2 ($A_{EM} \geq 1$ cm^2) using a TO-115 package, which is approximately 1.35 in (3.4 cm) in dia. This approach could be used for our devices; however, there are a number of problems which arise with the solder die-attach/wire bonding approach as the die size is increased. Furthermore, there is an attractive alternative in the compression-bonded-encapsulation (CBE) technique, which is presently used to manufacture interdigitated thyristors at the Westinghouse Semiconductor Division.

In the standard CBE technique, the silicon wafer (0.1 to 0.2 mm thick) is alloyed to a thick ($\sim$ 1 mm) molybdenum disc at a high temperature (800 to 900^{o}C). This temperature substantially reduces the likelihood of developing voids at the silicon-metal interface, a result that is important if the proper SOA is to be achieved.

The emitter contact is also different with CBE in that contact over the entire emitter region can be achieved by use of a "preform" as shown in Figure 3. The preform is usually 0.15 mm thick molybdenum which is etched to have the same geometry as the emitter region. Base contact is accomplished via a center contacting wire which is insulated from the emitter electrode.

This procedure allows the use of a planar emitter-base structure and avoids the need for multiple emitter wire bonds. In addition, a substantial amount of heat can be removed from the top of

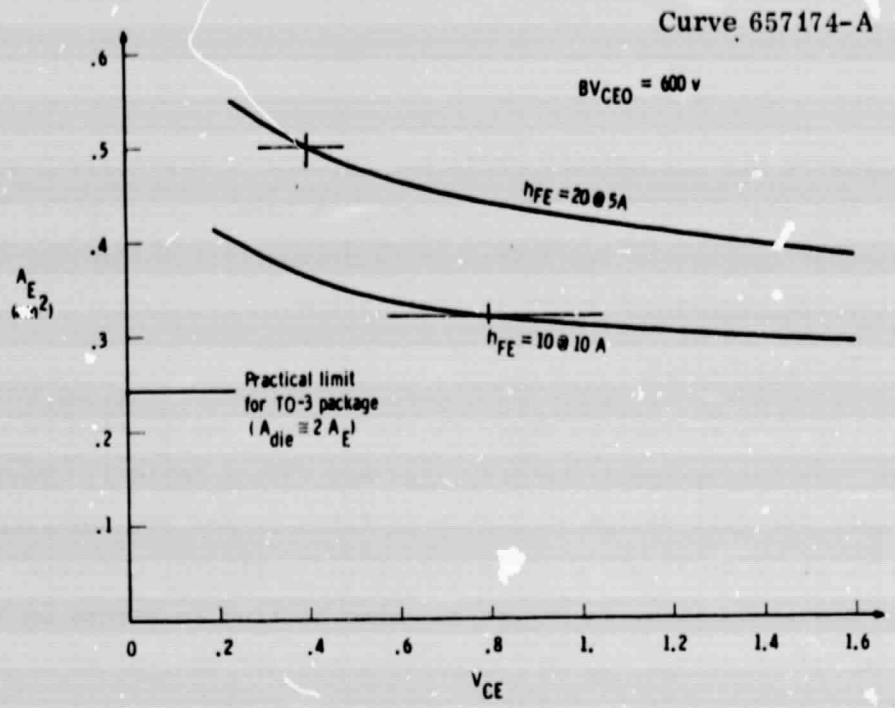


Figure 2 — Minimum emitter area vs. collector-emitter saturation voltage as required by the BV_{CEO}, I_C, and I_B values of specifications (1), (5), and (6).

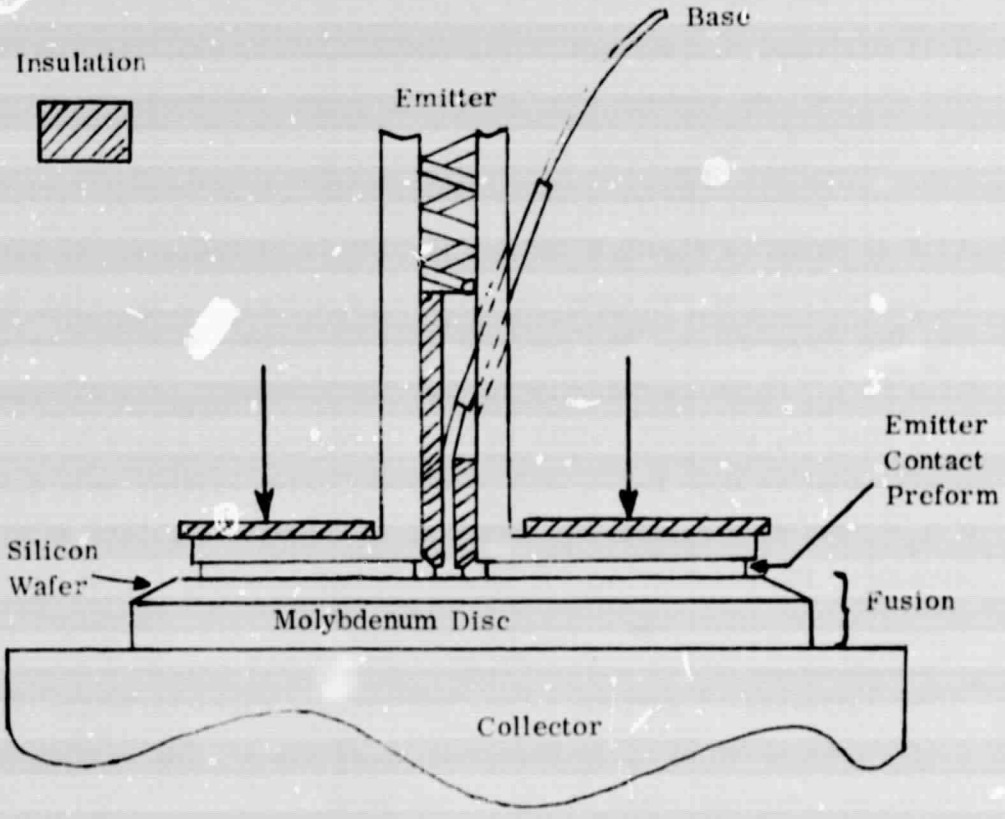


Figure 3 — Cross section of CBE assembly scheme. The external package (not shown) provides the compressive force indicated by the arrows.

the transistor via the emitter preform. In view of these advantages and also the practicality of fabricating even larger transistors (e.g. 5 cm diameter thyristors are presently in production) we decided to pursue the CBE approach for device fabrication.

3.4 DC Characteristics

In this section we describe the optimum design results using the most restrictive specifications, (1) and (5) of Table 1. Pertinent device data for this design is listed in Table 3, and the impurity profile is shown in Figure 4. The calculated collector characteristic for this design is shown in Figure 5. Also plotted as points on Figure 5 are the values of I_C, V_{CE} for specifications (5) and (6) with the corresponding values of I_B shown in parentheses. It can be seen that in all cases the calculated I_B curve lies above the I_B point, with the V_{CE} = 0.4 V, I_C = 5 A point lying fairly close to the calculated curve.

For the calculation of Figure 5, a series emitter resistance of 15 milliohms was assumed. This resistance, if properly distributed over the emitter contact area*, has a dominant influence on the shape of the forward SOA boundary [4].

Another characteristic of interest is the h_{FE} vs. I_C curve, which is shown in Figure 6 for the parameters of Table 3. At large values of I_C, emitter current crowding becomes important and h_{FE} will deviate from the ideal value. The onset of current crowding will occur at some value of I_{C2} which is normally in the region where h_{FE} is decreasing as I_C^{-1}, that is, where the widtn of the current-induced-base is approximately equal to W_C. For $I_C > I_{C2}$, the effective emitter area decreases as I_C^{-1}, and as a result, h_{FE} shows an I_C^{-2} proportionality at high currents. The value of I_C for which current crowding begins it termed the

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* The influence of various device and package characteristics on the effective value of R_E is presently under study. The results of this work will be contained in the Final Report.

Table 3 — Optimum Design for Specifications (1) and (5)

Symbol	Description	Value	Units
W_C	Metallurgical collector width	7.6×10^{-3}	cm
N_C	Collector donor density	6.0×10^{13}	cm^{-3}
Q_B	Total number of base acceptors per unit area. $Q_B = \int_0^{W_{BO}} N_A(x)dx$	2.0×10^{13}	cm^{-2}
A_{EM}	Metallurgical emitter area	0.6	cm^2
ESW	Emitter stripe width	0.076	cm
		(30	mil)
Z	Emitter perimeter	16	cm
		(6.3	in.)

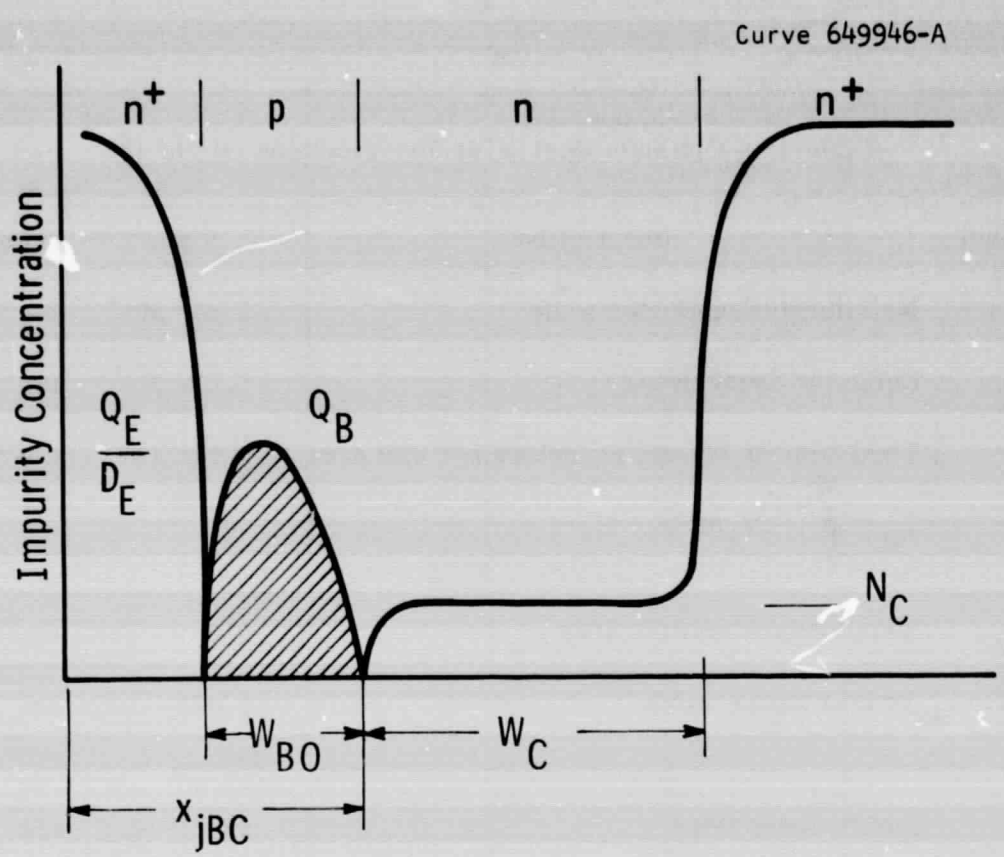


Figure 4 General shape of the impurity profile showing definition of terms used in Table 3.

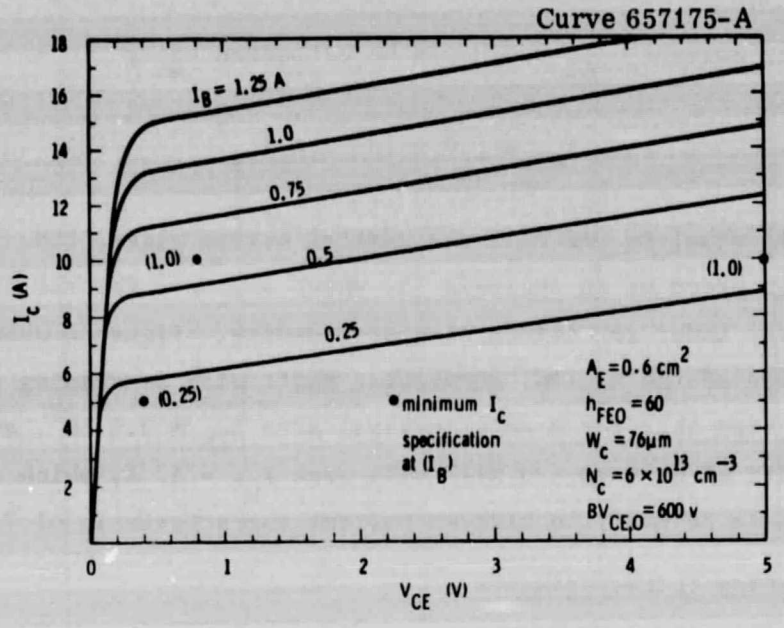


Figure 5 — Calculated collector characteristic for the device parameters of Table 3. The numbers shown in parantheses are the values of I_B (in amperes) given by specifications (5), (6) and (8).

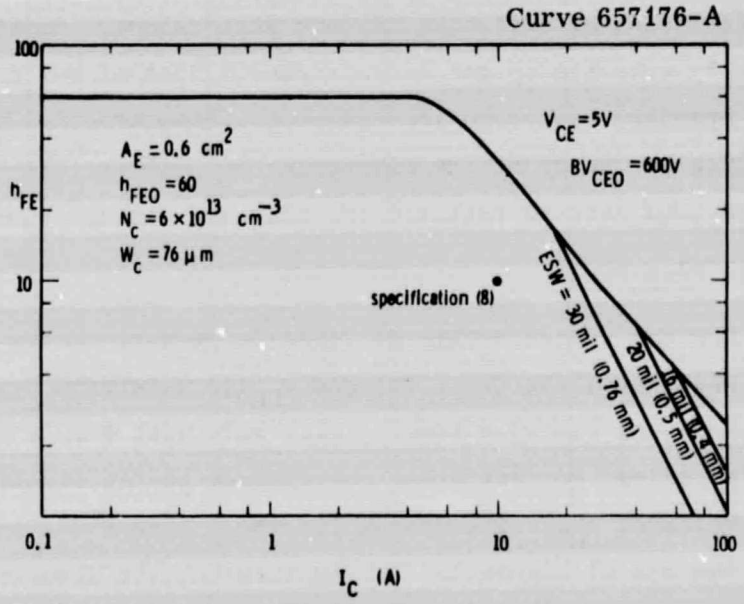


Figure 6 — Calculated current gain vs. collector current for different values of emitter stripe width.

"cross-over current" I_{C2} which can be estimated using

$$I_{C2} = 6.0 \times 10^{-2} \; A_E/L_E^2 \qquad (A) \qquad (1)$$

where L_E is equal to one-half the emitter stripe width, ESW. This equation is based on an analysis [5] which accounts for the lateral voltage drop under conditions of base-widening. Figure 6 shows how the I_C^{-2} portion of the $h_{FE}(I_C)$ curve will shift with decreasing stripe width. It can be seen that for a metallurgical area $A_{EM} = 0.6$ cm^2, an emitter stripe width of 0.76 mm (30 mil) will give $I_{C2} = 17$ A, which is more than adequate to meet the highest current characteristic of Table 1.

3.5 Switching Characteristics

At present there is no adequate design theory that relates the switching performance to the device variables. There are two problems. One is the lack of device models that work satisfactorily in the time domain. The second is the lack of a set of generalized test waveforms which can be used to measure device characteristics and still give a useful description of switching circuit performance. Nevertheless it is frequently possible to get an approximate idea of switching behavior using the standard resistive load circuit. Some progress has been made in predicting the shape of the waveforms for this circuit and these results are used here to estimate the rise and storage times.

3.5.1 Rise Time

For the device design of Table 3, we have used a charge control model [6] which predicts the $i_C(t)$ and $v_{CE}(t)$ waveforms during turn-on. Figure 7 shows how the rise time t_r will vary with supply voltage V_{CC}, where t_r is defined for different percentages of the steady-state collector voltage, V_{CE}. The reason for the V_{CC} dependence of t_r can be seen with the aid of Figure 8. During turn-on, the time required to travel the dashed portion of the load line will be relatively short, since the base transit time corresponds to that of the metallurgical base. The time required to move over the solid portion is considerably longer

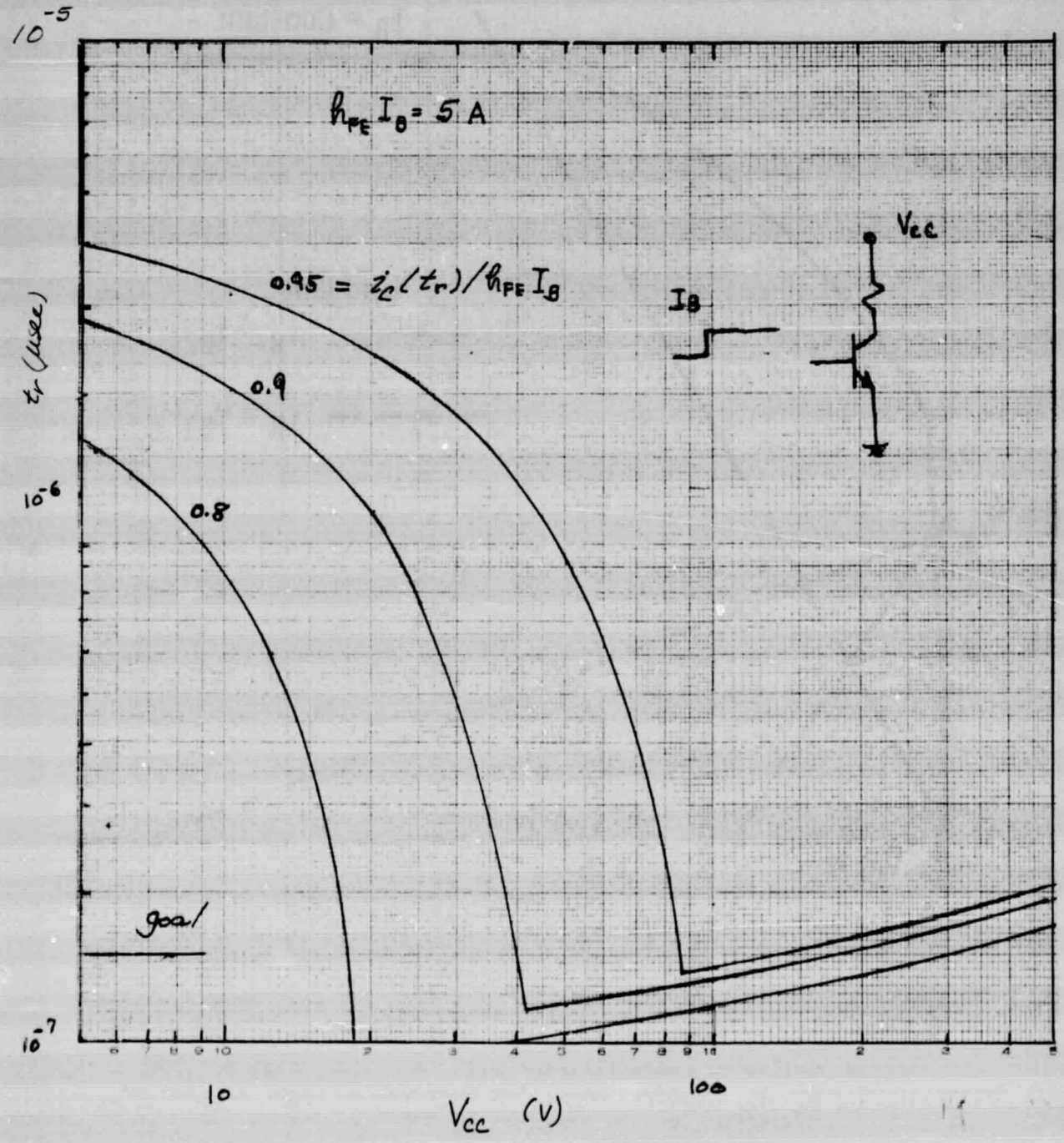


Figure 7 Collector current rise-time vs. supply voltage.

Curve 683128-A

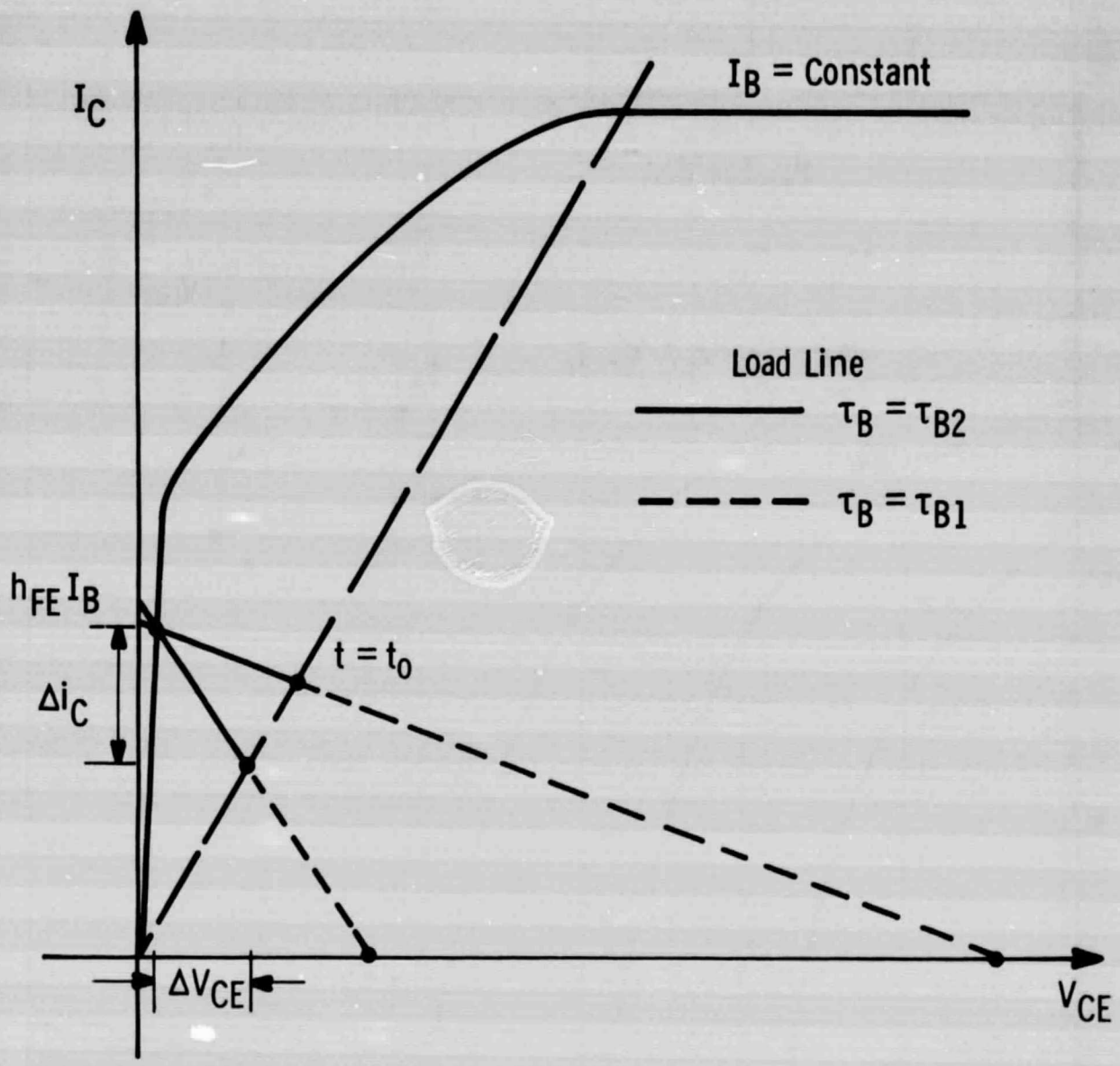


Fig. 8 Collector characteristic with load line drawn for two R_L, V_{CC} combinations. The incremental terms Δi_C and Δv_{CE} are shown for the smallest R_L and V_{CC}.

and can be related to an effective transit time of the collector region. Therefore, as V_{CC} is reduced, the fraction of $h_{FE}I_B$ due to operation in the quasi-saturation region will increase, and as a result, t_r will also be increased.

Although it is important to account for this effect during testing, it is unlikely to be a problem in most applications where the apparent value of V_{CC} will usually be a substantial fraction of BV_{CEO} and well beyond the quasi-saturation region.

For a 10-90 percent rise time of 0.15 μsec, Figure 7 shows that the design of Table 3 meets this requirement over a wide range of V_{CC} values. The theory for fall time has yet to be completed; however, it is expected that t_f will show a dependence and magnitude closely related to that given in Figure 7 for t_r.

3.5.2 Storage Time

Prediction of storage time is more involved than calculating rise time because the collector n-n^+ junction is usually injecting at the initiation of the turn-off pulse. In addition, charge storage under the base contact and at the edge of the emitter-base junction can be important. The overall problem of predicting storage and fall time will be studied during the final portion of the contract; however, we can make an estimate of the minimum storage time that will result when the collector n-n^+ junction is not strongly injecting. This will occur, for example, when there is only a slight amount of base "overdrive" at the initiation of turn-off, or when the lifetime in the n^+ collector region is low.

Using the same charge control model of [6], the minimum storage time can be approximated by:

$$t_{s,min} = \frac{h_{FE} W_C^2}{8 D_C} \ln \left(1 + \frac{I_{B1}}{I_{B2}}\right) \qquad (2)$$

For the transistor of Table 3, (2) gives $t_{s,min}$ = 0.73 μsec, which can be reduced slightly if W_C is decreased from the optimum value of 75 μm.

Typically t_s is larger than $t_{s,min}$ indicating that additional charge is stored in the collector region. Initial results indicate that the base lifetime and profile are important in determining the actual value of t_s.

4. TECHNOLOGY INVESTIGATION

4.1 Wafer Processing

Two approaches to wafer processing are being investigated, bevel-etch and planar. These terms refer to the method used to fabricate the base-collector junction, which must be capable of blocking at least 800 V and must have an area of approximately 1.5 cm^2. The bevel-etch technique is routinely used for large-area p^+-n junctions, where the p^+ layer is a relatively deep diffusion (50 to 80 microns).

For the transistor, we wanted to determine whether bevel-etch junctions suffer any serious degradation of BV_{CBO} as x_{jBC} is reduced to the range of 20 to 25 microns. This depth is set by the switching time requirements on the metallurgical base width W_{BO} and by the need for good reproducibility of W_{BO} using conventional diffusion profiles.

Even shallower junctions are possible with a planar structure [7] that uses a high-resistance polysilicon layer to achieve a linear grading of the surface potential. With proper selection of geometries, it is possible to achieve ideal or "bulk" values of breakdown voltage. We have achieved blocking voltages in excess of 4 kV with this technique; however, these results apply to relatively small-area junctions ($\tilde{=}$ 0.1 cm^2). Since at least a 20 fold increase in junction area is required for the present design, a considerable reduction of the defect density (obtained using conventional processing techniques) is required.

To date, most success has been obtained with the bevel-etch approach; however, considerable progress has been made in reducing the number of defects in the planar junctions. It is believed that the eventual benefits of the planar approach (higher frequency, more reliable junction passivation, reduced surface leakage current, and non-hermetic packaging possibilities) justify additional work in this area. Recent

results indicate that the defect density can be reduced to less than 1 per cm^2, which is approaching a satisfactory range.

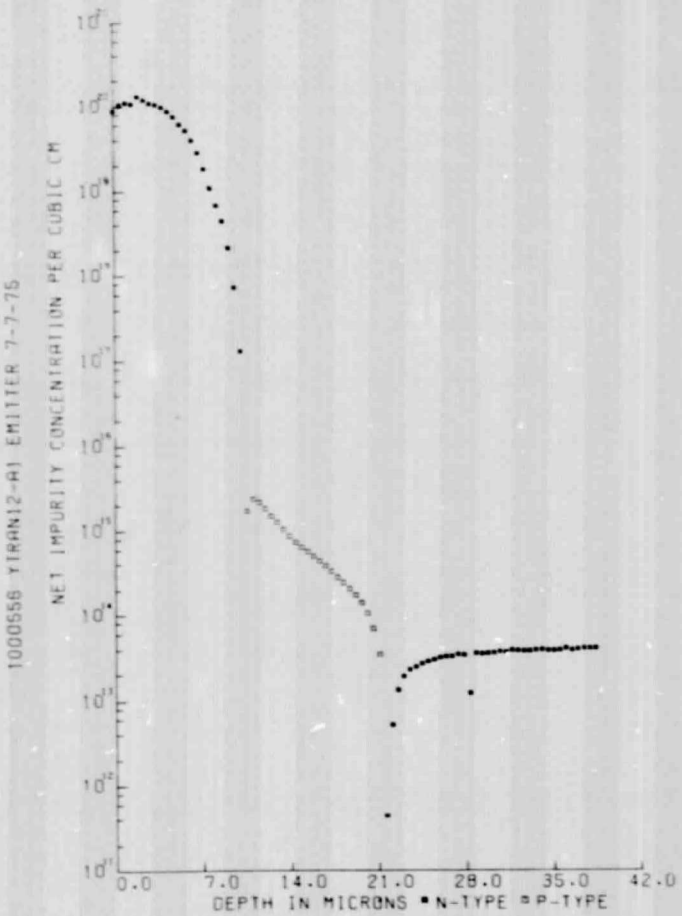
4.2 Triple-diffused Profile

Figure 9 shows spreading resistance impurity profiles which are representative of the bevel-etch devices made to date. The profile shown here is "triple-diffused", which requires a relatively long diffusion time to establish the collector n^+ region. Some double-diffused devices were made, where this n^+ diffused layer is absent and collector contact is made via an alloyed n^+ region. Although BV_{CBO} voltages as high as 1 kV were achieved with the alloyed junctions, the results were not always reproducible and it was decided to concentrate on the triple-diffused approach for fabrication of the sample devices. The process which has given the best overall results is outlined in Figure 10. The results of the experimental transistor runs using this and similar processes are described in Section 5.2.

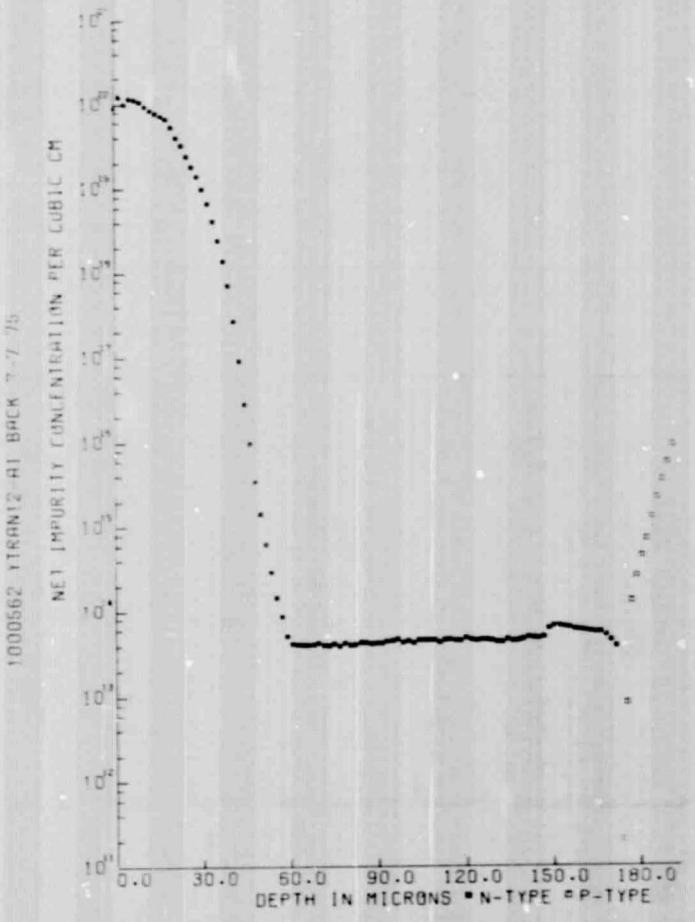
4.3 Emitter Geometry

Three mask geometries were used to fabricate the experimental transistors, and relevant geometrical data is summarized in Table 4. The GCS mask was used for the initial devices. Later runs were made using a modified thyristor mask, and the final devices were made using a geometry designated as 565, which is shown in Figure 11.

The metallurgical emitter stripe width of the geometries of Figure 11 is 1.3 mm (50 mil) for the snowflake and 1.0 mm (40 mil) for the 565 mask. These dimensions, although relatively coarse by transistor standards, are sufficiently small to handle the required currents. The permissible stripe width is directly related to the maximum current density to be controlled, which is related to BV_{CEO} [2]. Thus as BV_{CEO} is reduced it will be necessary to use narrower stripe widths than those shown in Figure 11. During the final period of the contract we intend to investigate the possibility of increasing the emitter area and perimeter to the degree permissible with the present fusion diameter.



(a)



(b)

Fig. 9 Measured impurity profiles obtained from spreading resistance data.
Profile (a) is through the emitter region.
Profile (b) is through the collector region which is at the left of the plot.

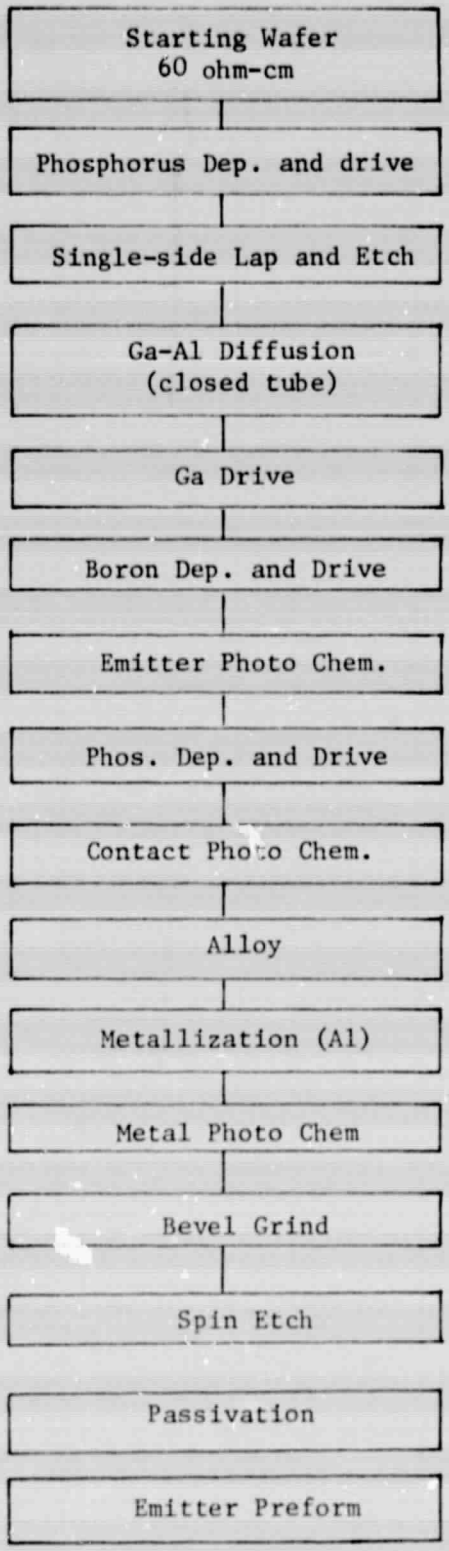


FIGURE 10 PROCESS OUTLINE

TABLE 4 EMITTER GEOMETRY DATA

Mask	A_{EM} (cm^2)	L_E (= ESW/2) (cm)	(mil)	Z (cm)	I_{C2}(*) (A)
GCS	0.506	2.54×10^{-2}	10	19.7	46.8
SF	1.625	6.35×10^{-2}	25	26.6	24.1
565	1.066	5.08×10^{-2}	20	14.4	24.7

* $Q_E/D_E = 5 \times 10^{13}$ cm^{-4}-sec.

Fig. 11 Metallized wafers for the 565 and snowflake geometries.

5. EXPERIMENTAL RESULTS

5.1 Base Diffusion

Initial work focused on developing a process that would give the required base width and still achieve the blocking voltage needed for the collector-base junction. Two methods of diffusing the base were investigated: closed-tube with Ga-Al as the source and open-tube with a BBr_3 source. The results of the first two experimental runs, which are summarized in Table 5, indicated that the closed-tube Ga-Al process would be satisfactory for subsequent transistor runs. Devices made using the BBr_3 process typically exhibited what we have termed "premature breakdown", where the name is due to the shape of the reverse I-V characteristic shown in Figure 12(a). A model has previously been proposed [8] which accounts for the observed behavior and is shown in Figure 12(b). For the BBr_3 devices of Table 5, the presence of this defect has been verified by a number of techniques. These include observation of light emission, anodization experiments, and correlation of observed spot size with measured R values. By way of additional confirmation it has been found that devices exhibiting premature breakdown after base diffusion frequently show a "pipe" characteristic after emitter. That is, there can be a resistive path between emitter and collector, which will occur if the defect happens to be in a region which receives the emitter diffusion.

It is also important to note that the defect density for our devices must be significantly less than would be acceptable for a multi-chip or integrated circuit type of device which is perhaps one-tenth the area. Efforts to reduce the defect density have been carried out in parallel with the experimental transistor runs, and recent results indicate that we now have an open tube BBr_3 process which is free of

TABLE 5 REVERSE I-V CHARACTERISTIC DATA (AVERAGED)

Process	V_o (V)	R (kohm)	BV (5 mA) (V)
Ga-Al (x_j = 17 um)	*	*	597
BBr_3 (x_j = 19 um)	16	125	150

Junction area = 3 cm^2

*No premature breakdown observed.

the premature breakdown problem. These techniques should permit the fabrication of high-voltage planar junctions having the largest area know to date.

5.2 Transistor Experiments

Several transistor runs have been processed and the results are summarized in Table 6. The values given in this table are representative of each particular run. Fifty-four sample devices were selected from Runs 10, 11B, 12A, and 12B, and have been delivered to NASA-Lewis RC. Individual data on these devices is given in Section 6.

5.3 DC Characteristics

Figure 13 shows a typical collector characteristic for the low-voltage, high-current region and also an I_C vs. V_{CE} plot with $I_B = 0$ under pulsed conditions. From the latter curve we can estimate $BV_{CEO}(sus)$ to be in the range of 800 to 850 V at 100 mA. This transistor meets the $V_{CE}(sat)$ specification with ample margin ($V_{CE}(sat) = 0.21$ V at $I_C = 5A$, $h_{FE} = 20$).

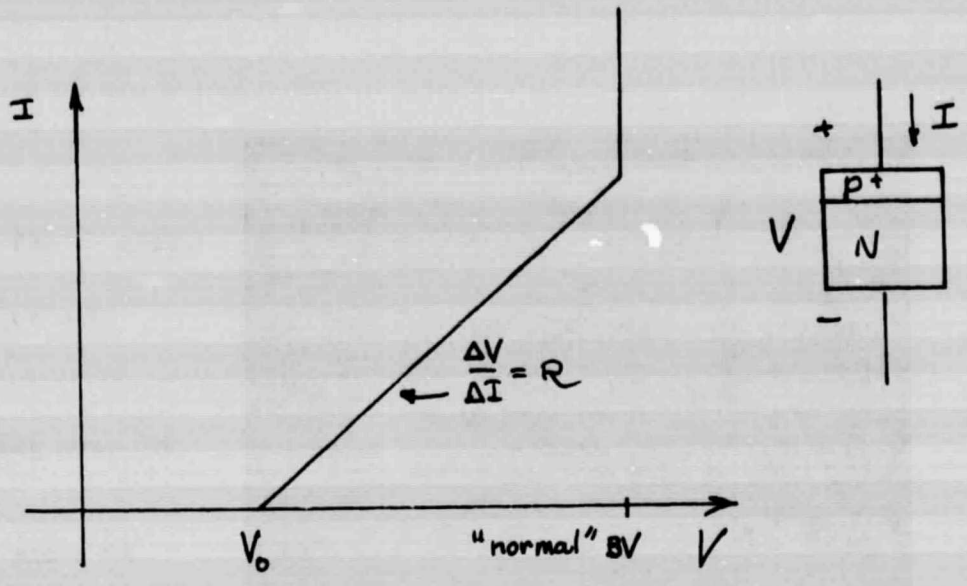
Comparison of the measured and predicted behavior in the quasi-saturation region is shown in Figure 14 for a transistor from Run 7, where it can be seen that the one-dimensional model predicts the correct behavior, at least over a portion of the characteristic. For $V_{CE} \gtrsim 3$ V and $I_C \gtrsim 35$ A, the onset of current crowding causes deviation from the one-dimensional model. This behavior is more clearly shown in Figure 15, where the measured h_{FE} values deviate from the one-dimensional calculation. At higher currents h_{FE} shows an I_C^{-2} behavior which corresponds to an effective emitter stripe width that agrees well with the metallurgical value of 50 mils.

5.4 Switching Characteristics

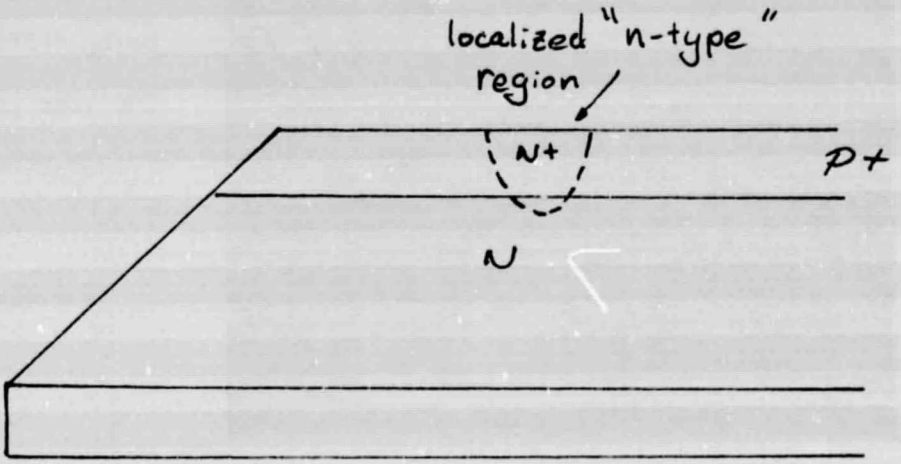
As can be seen from Table 6 the measured rise and fall times are larger than the goal of 0.15 μsec. Other measurements have shown that these values of t_r and t_f are artificially large by an amount estimated to be in the range of 0.10 to 0.15 μsec. This increase is

TABLE 6 SUMMARY OF TRANSISTOP EXPERIMENTS

RUN	MASK	BASE DIFFUSION	COLLECTOR CONTACT	W_C (μm)	N_C (cm^{-3})	Q_E/D_E (cm^{-4}-sec)	Q_B/D_B (cm^{-4}-sec)	h_{FEO} (--)	BV_{CEO} (V)	t_r (μsec)	t_f (μsec)	t_s (μsec)
4&5	GCS	Ga-Al	alloy	65	6×10^{13}	6×10^{13}	1×10^{12}	60	450	0.2	0.5	5.0
7	GCS&SF	Ga-Al	alloy	90 to 100	6×10^{13}	7×10^{13}	2.3×10^{12}	30	400 to 650	0.5	0.7	7.0
8&9	GCS&SF	Ga-Al/BBr_3	alloy	40 to 60	6×10^{13}	7×10^{13}	8.5×10^{11}	80	250 to 400	0.2	0.35	0.6
10	GCS&SF	Ga-Al	alloy	85 est.	6×10^{13}	(not measured)		20 to 30	850	(not measured)		
11	SF&565	Ga-Al/BBr_3	alloy	70 to 95	8×10^{13}	5×10^{13}	1×10^{12}	50	550 to 830	0.3	0.3	1.5 to 20
12	SF&565	Ga-Al	phos.	70 to 115	7×10^{13}	7×10^{13}	7×10^{11}	100	600 to 1000	0.36	1.0	6.0

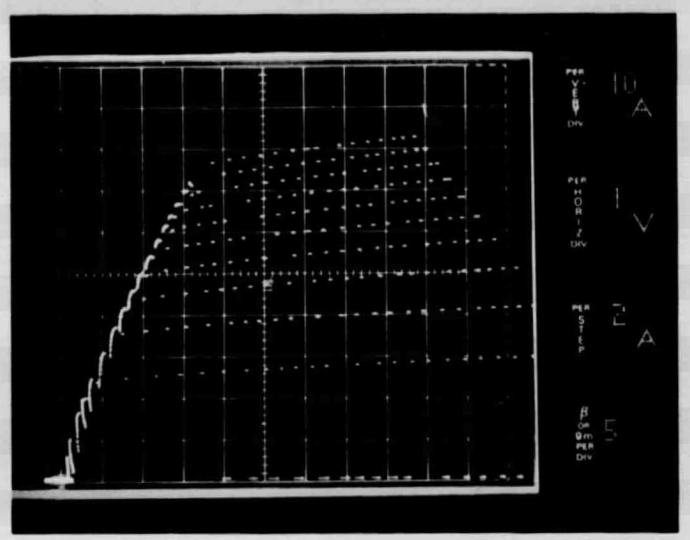


(a)



(b)

Fig. 12 (a) I-V characteristic of premature breakdown characteristic.
(b) Model of the defect.



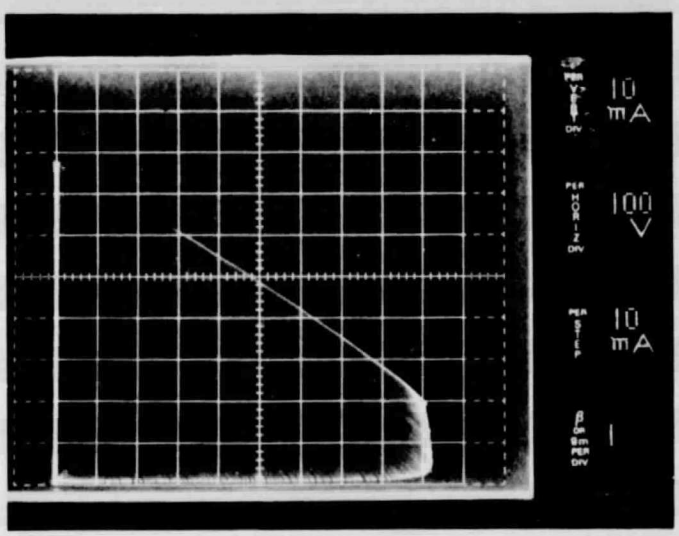
#156 565 Mask

Run 10

300 μsec pulses

10 steps

(a)



Using OFFSET and

300 μsec pulses

(negative)

2 steps

(b)

Fig. 13 (a) Collector characteristic in quasi-saturation region.
(b) Pulsed measurement of I_{CEO} vs. V_{CEO}, BV_{CEO} (sus) ≈ 800 to 850V @ 100 mA.

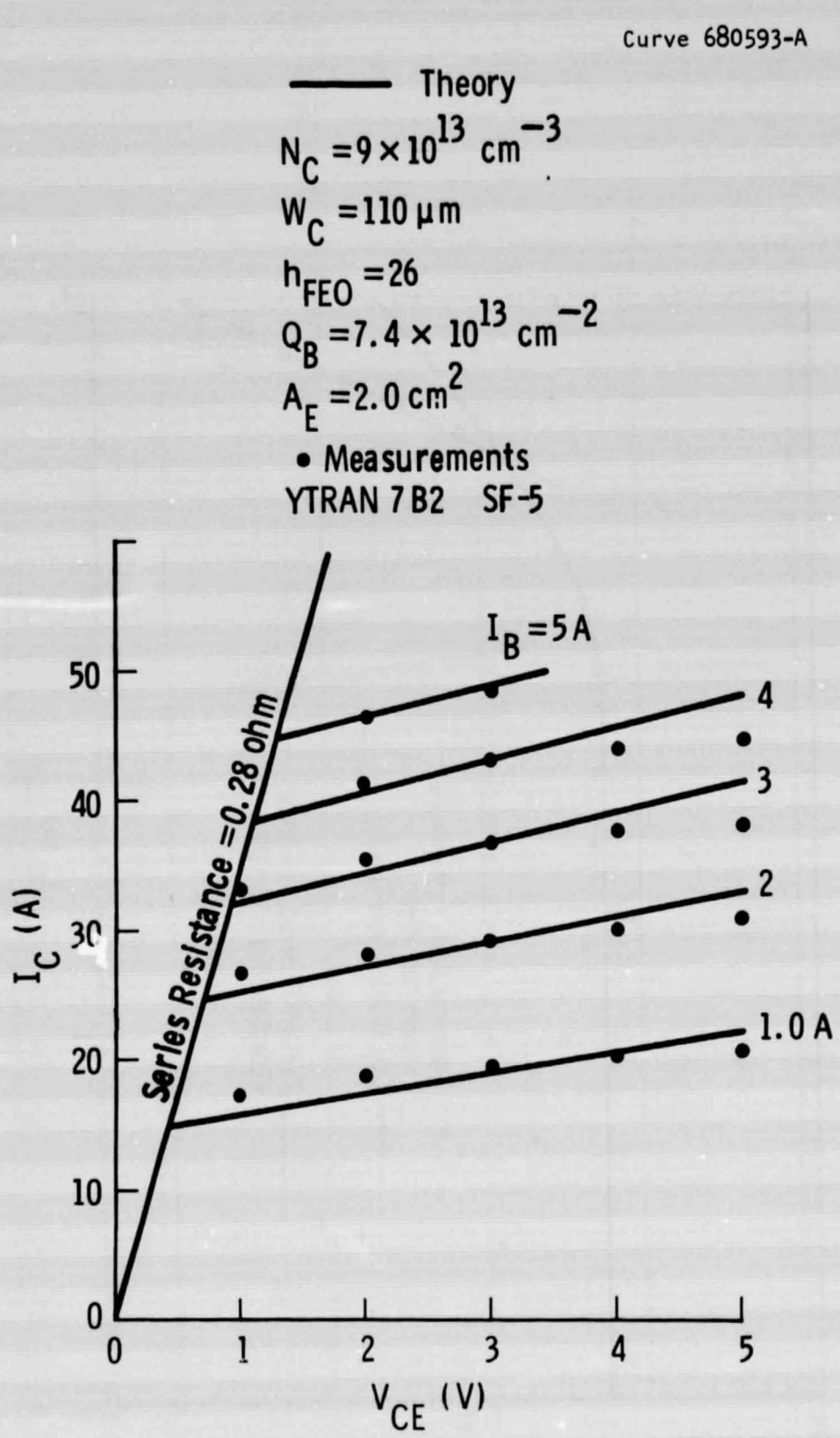


Fig. 14 Comparison of measured and predicted behavior in the quasi-saturation region.

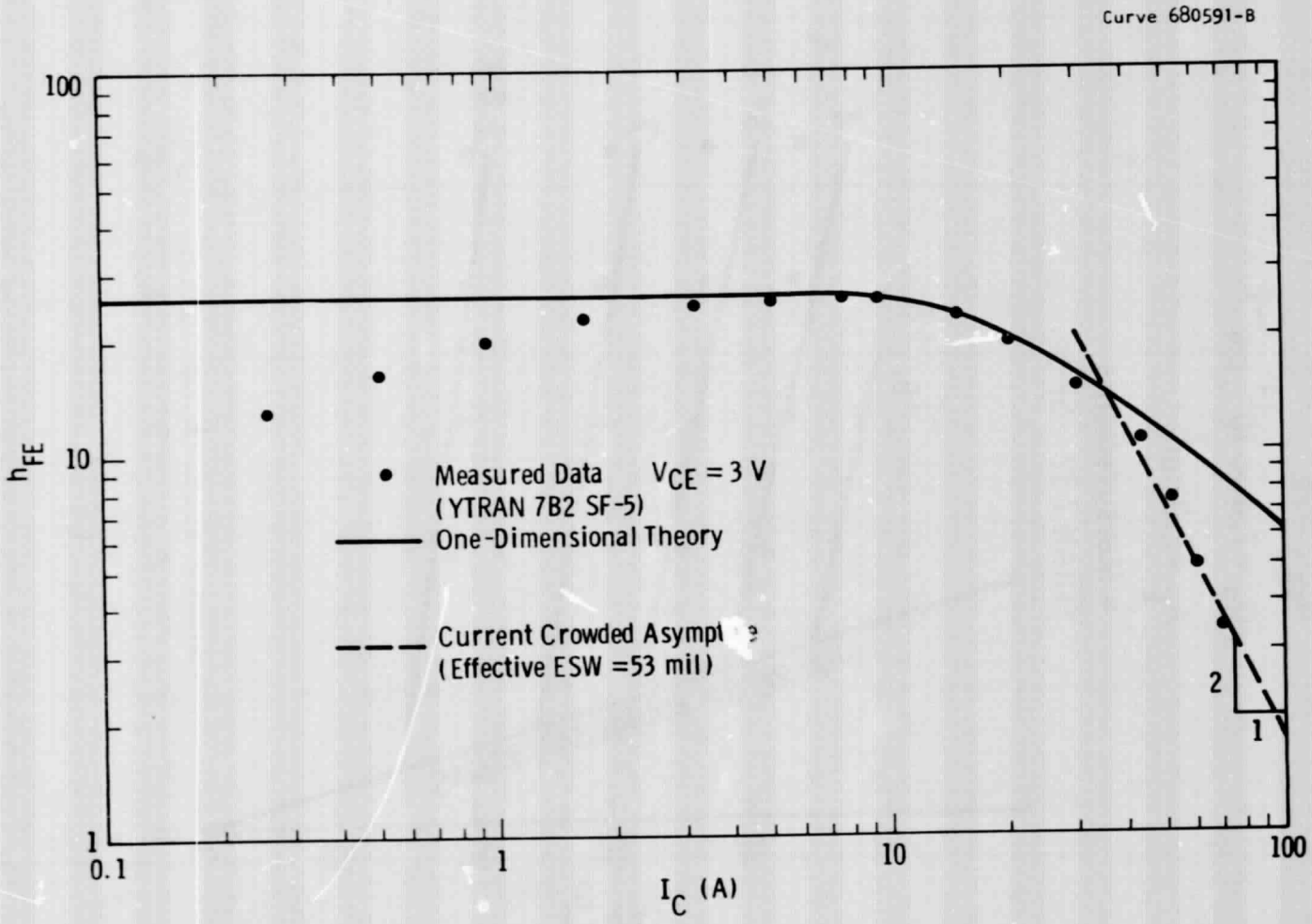


Fig. 15 Current vain vs. collector current.

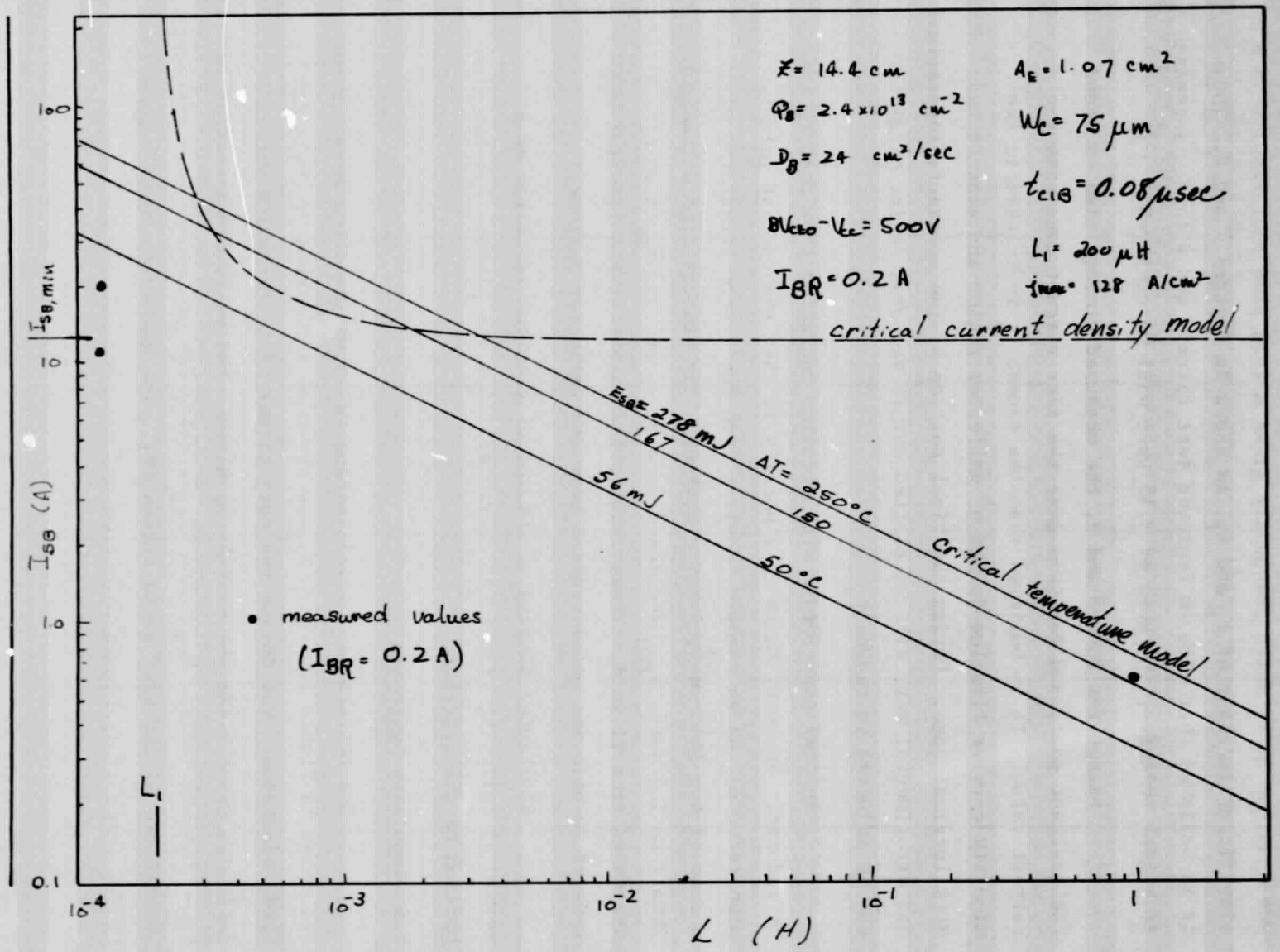


Fig. 16 - Second breakdown current for electrical and thermal models as a function of collector inductance. Measurements are for devices having 565 emitter geometry.

due to a base circuit inductance which could not be eliminated in our switching test circuit. In addition, V_{CC} for the switching measurements was equal to 25 V, which frequently gives a load line that results in a significant increase of t_r and t_f, as shown in Figures 7 and 8. Thus it is believed that with an improved test circuit and with V_{CC} increased to higher voltages, the goal of 0.15 μsec will be achieved.

Except for Runs 8 and 9, the measured storage time exceeded the contract goal, and for this case the test circuit does give the correct value. It is believed that the excess t_s is related to the minority carrier lifetime in the n^+ collector region and also in the metallurgical base. During the final portion of the contract, theoretical and experimental work will be carried out to see what device parameters can be adjusted to reduce t_s.

Initial experiments with electron radiation show that t_s can be reduced. However, there is a penalty in that the current gain is also reduced. As an example, devices from Run 7 were irradiated with a dose of 4×10^{13} cm^{-2}, 2 MeV electrons. The storage time decreased from 7 to 1.3 μsec, h_{FEO} decreased from 32 to 16, and h_{FE} @ 20 A, 5 V decreased from 21 to 6. These results indicate that the lifetime was reduced in both the metallurgical base and collector regions.

Additional studies of the use of electron radiation as a method of tailoring transistor characteristics are planned for the final portion of the contract.

5.5 Inductive Switching

The results of initial testing using an inductive load circuit are shown in Figure 16, where I_{SB} is shown as a function of collector load inductance. The points indicate values of I_C for which second breakdown occured for the reverse I_B given. The solid lines correspond to a critical energy, $E_{SB} = 1/2\ LI_{SB}^2$, which can be related to a critical temperature of the pinched-in region [9]. The dashed curve corresponds to the onset of avalanche injection and has been calculated using a

charge control model [10]. Based on the limited data obtained to date, it appears that I_{SB} for the present design is dominated by thermal effects. One of the topics that remains to be investigated is the use of an increased emitter perimeter, which should give increased I_{SB} values for both mechanisms.

5.6 Forward SOA

One of the important results demonstrated in the initial portion of the contract is a major increase in the safe-operating-area over what is presently available in commercial devices. Figure 17 shows the results of measurements and calculation of the SOA for conditions that correspond closely to DC operation. The open data points indicate the onset of current localization as determined from a measurement of V_{BE} during the power pulse. The solid points indicate the measured onset of second breakdown, which could not be detected for one device at 2A, 135 V due to power limitations of the test set. Additional measurements on a larger number of transistors indicate that greater than 50 percent will pass a 1 sec, 4A, 100 V power test.

Also shown in Figure 17 is the SOA boundary of the Westinghouse alloy transistor family, which is known to have the best performance of commercial devices from the standpoint of the steeply sloped (second breakdown) portion of the curve [11].

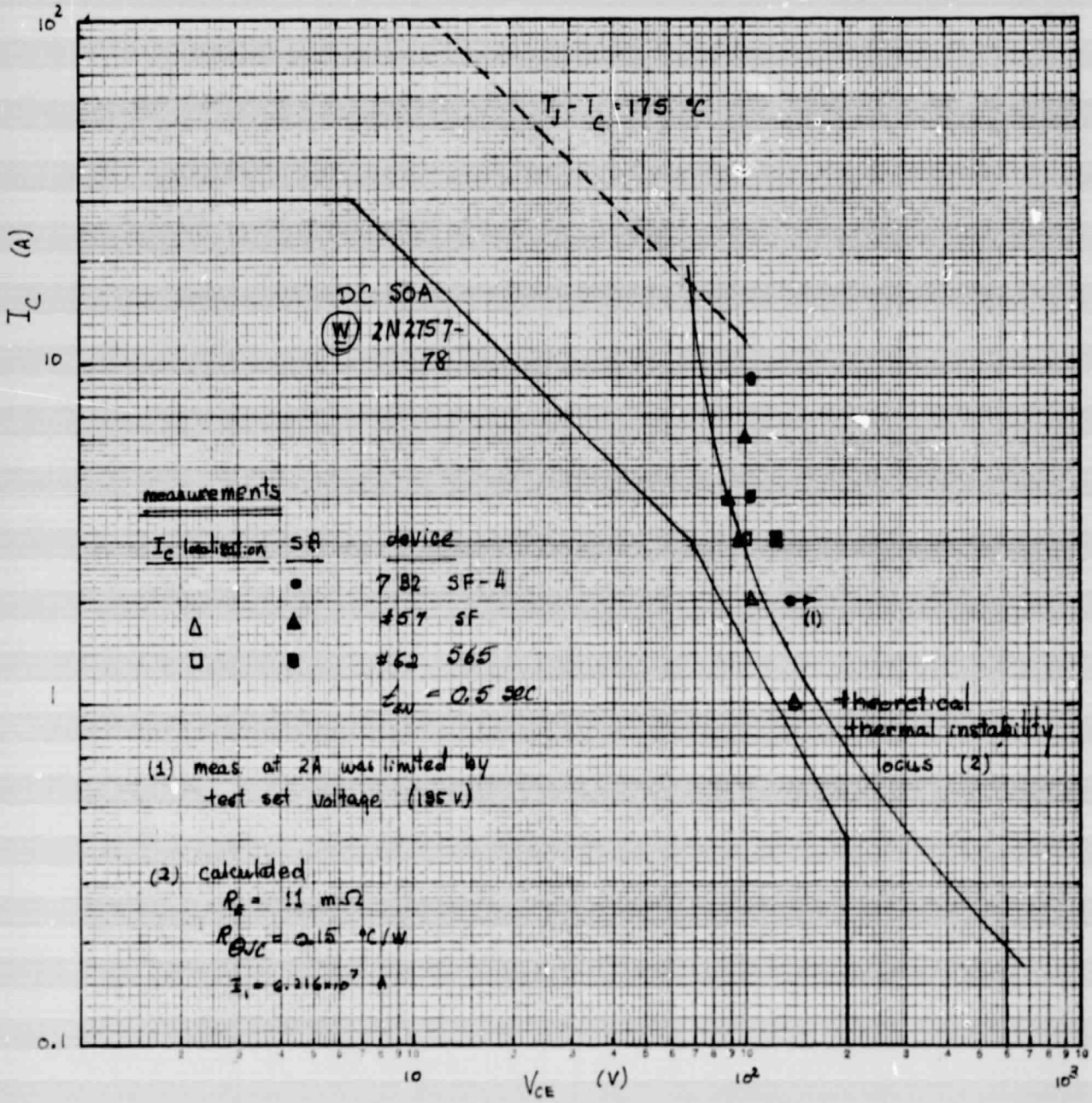


Fig. 17 Measured onset of current localization (open data points) and second breakdown (solid data points) for three different transistors.

6. TEST DATA

Table 7 lists measured data on a total of 54 devices which have been delivered to NASA-Lewis RC. The averaged results are:

	$V_{CE}(sat)$ (5)	$V_{CE}(sat)$ (6)	$BV_{CEO}(sus)$ (10)
Average of 50 devices	0.66 V	0.55 V	680 V
Desired	$\leq$ 0.4	$\leq$ 0.8	$\geq$ 600

As a confirmation of the design theory, a number of the devices did simultaneously meet all three requirements; however, on the average $V_{CE}(sat)$ at 5A was about 50 percent larger than the goal. The main reason for these results is that the collector width on most of the devices is thicker than the optimum value given in Table 3, e.g. for Run 12, W_C was purposely increased to about 110 microns so that even if a device did have a non-uniform alloyed region, the resulting reduction in BV_{CEO} would not decrease this quantity below 600 V.

Recent refinements in the alloying procedure have improved the collector contact uniformity and have given BV_{CEO} values close to the ideal. Consequently we believe that subsequent transistor runs will give results quite close to the predicted design for nearly all the devices in the run.

Table 7 Test Data on Sample Devices

Dev.#	Run	Mask	V_{CE}(sat) (V)	Break-down	V_{CE}(sat) (V)	V_{CEO} at I_{CEO} (V)	I_{CEO} (mA)	h_{FE} (--)	V_{EBO} at I_{EBO} (V)	I_{EBO} (mA)	BV_{CEO}(sus)	BV_{CER}(sus) R_{BE} = 47 ohm	L (mH)
	see note		1		2	3	3	4	5	5	6	6	6
63	12A	SF	0.40	D	0.30	400	0.1	65	<1	1	700/40	--	1000
65	12A	SF	0.49	D	0.42	600	0.01	46	<1	1	850	870	1000
79	12B	SF	0.52	D	0.31	600	< 0.5μA	50	<1	1	970/60	--	1000
81	12B	SF	0.70	D	0.45	600	0.002	50	<1	1	1000/20	1050/20	1000
83	12A	SF	0.53	D	0.36	600	0.002	54	<1	1	840/60	--	1000
89	12A	SF	0.45	D	0.33	525	0.1	50	<1	1	1000/50	--	1000
90	12A	SF	0.90	D	0.31	22	0.1	39	<1	1	1050/60	--	1000
95	12A	SF	0.74	D	0.41	1.2	0.1	41	<1	1	1000/60	--	1000
99	12B	SF	0.34	D	0.29	20	0.1	80	<1	1	800/20	--	1000
105	12A	565	0.69	S	0.50	480	0.1	46	8	0.5	540	680	1000
109	12A	SF	0.39	S	0.19	600	0.003	63	<1	1	1100/40	1100/40	1000
110	12B	SF	0.27	S	0.15	520	0.1	56	<1	1	870/80	870/80	1000
111	12B	SF	0.97	S	0.90	580	0.1	51	<1	1	920/40	950/40	1000
114	12A	565	>2.0	S	>2.0	425	0.1	17	8	0.01	620	750	1000
116	12B	SF	0.22	S	0.53	220	0.1	47	<1	1	700	750	20
117	12A	SF	0.72	S	0.50	600	0.002	47	<1	1	600	600	20
118	12B	SF	1.01	S	1.01	475	0.1	27	<1	1	570	580	20
119	12B	SF	0.78	S	0.85	600	1.5μA	31	<1	1	560	520 ?	20
121	12A	SF	0.53	S	0.25	550	0.1	49	<1	1	650	680	20
126	12B	565	0.59	S	0.46	420	0.1	50	8	0.2	530	640	20
128	12A	565	0.45	S	0.29	600	< 0.5μA	50	8	0.5	550	675	20
129	12B	565	1.14	S	1.20	600	1 μA	32	7.5	1	580	760	20
130	12A	565	0.66	S	0.50	600	1.3μA	54	8	0.01	525	600	20
132	12A	565	0.25	S	0.23	560	0.1	56	8	2μA	525	625	20
133	12A	565	0.65	S	0.36	530	0.1	34	8	0.1	650	775	20

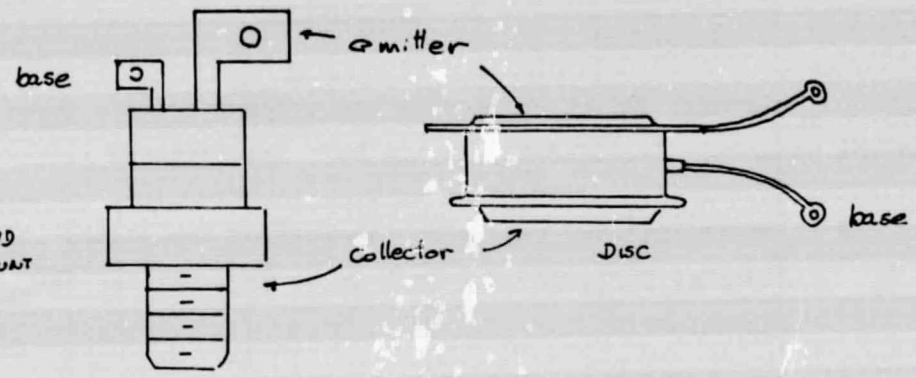
Table 7 (cont.)

Characteristic			V_{CE}(sat)		V_{CE}(sat)		V_{CEO} at I_{CEO}			h_{FE}		V_{EBO} at I_{EBO}		BV_{CEO}(sus)	BV_{CER}(sus) R_{BE} = 47 ohm	L
	Units		(V)	pack-age	(V)		(V)	(mA)		(--)		(V)	(mA)			(mH)
	see note		1		2		3	3		4		5	5	6	6	6
Dev.#	Run#	Mask														
134	12B	565	0.47	S	0.37		425	0.1		54		4	1	530	600	20
137	12A	565	0.66	S	0.46		600	< 1μA		48		8	0.1	500	625	20
138	12B	565	1.60	S	1.90		575	0.1		23		6.7	1	560	725	20
139	12B	565	0.92	S	0.88		335	0.1		40		3.5	1	515	650	20
140	12A1	565	0.30	S	0.44		500	0.1		50		<1	1	560	590	20
142	12A	565	0.90	S	0.80		260	0.1		27		7.5	1	500	650	20
144	12A	565	0.55	S	0.35		400	0.1		44		6	0.1	540	610	20
145	12B	565	0.91	S	0.74		350	0.1		43		<1	1	600	660	20
147	12A1	565	0.34	S	0.39		600	<0.5μA		51		8	8μA	520	660	20
150	12B	SF	0.53	S	0.23		600	0.5μA		54		<1	1	600	610	20
152	12A	SF	0.67	S	0.41		330	0.1		51		<1	1	600	600	1000
155	12B	SF	0.42	S	0.19		450	0.1		48		<1	1	700	725	20
156	10	565	0.21	S	0.27		600	0.02		32		8	0.2	800	1000	1000
164	12A	SF	0.42	S	0.19		8.5	0.1		59		<1	1	640	650	20
165	12B	565	1.75	S	>2.0		600	3μA		24		1.5	1	580	725	20
172	12A	565	0.61	S	0.36		50	0.1		36		1.5	1	580	780	20
182	12B	565	0.72	S	0.52		400	0.1		44		7.5	1	500	620	20
188	12A	565	0.65	S	0.35		140	0.1		35		5.5	1	500	610	20
194	12A	565	0.33	S	0.26		250	0.1		44		8	0.02	600	850	20
195	12A1	565	0.45	S	0.58		600	0.02		38		<1	1	525	540	20
200	11B	SF	0.72	S	0.24		22	0.1		32		<1	1	610	630	20
202	12B	565	0.26	S	0.23		600	1 μA		57		2.5	1	525	650	20
203	12A	565	0.32	S	0.25		600	1 μA		45		8	0.2	625	750	20
208	12A	SF	0.24	S	0.15		400	0.1		71		<1	1	525	550	20
210	12A	SF	1.04	S	0.87		60	0.1		39		<1	1	550	625	20

Table 7 (cont.)

Characteristic	V_{CE}(sat)		V_{CE}(sat)	V_{CEO} at I_{CEO}		h_{FE}	V_{EBO} at I_{EBO}		BV_{CEO}(sus)	BV_{CER}(sus) R_{BE} = 47 ohm	L
Units	(V)	package	(V)	(V)	(mA)	(--)	(V)	(mA)			(mH)
see note	1		2	3	3	4	5	5	6	6	6
Dev.# Run# Mask											
214 12A SF	1.62	D	1.70	2.5	0.1	29	1	1	675	700	20
84 12B SF	1.03	D	0.85	600	0.014	38	1	1	1175/40	--	1000
85 12A SF	0.31	D	0.26	520	0.1	62	1	1	925/40	--	1000
86 12A SF	0.35	D	0.31	600	0.003	60	1	1	1050/40	--	1000

Table 7 (cont.)



Notes

	Test	Conditions	Equipment Used
(1)	$V_{CE}(sat)$	I_C = 5A, I_B = 0.25A	Tektronix 576, 300μsec pulsed
(2)	$V_{CE}(sat)$	I_C = 10A, I_B = 1.0A	" " "
(3)	V_{CEO}, I_{CEO}	*	Tektronix 576, full-wave rectified, 60Hz

*I_{CEO} @ V_{CEO} = 600V or V_{CEO} @ I_{CEO} = 0.1mA, whichever occurs first as voltage is increased.

(4)	h_{FE}	I_C = 10A, V_{CE} = 5V	Tektronix 576, 300μsec pulsed
(5)	V_{EBO}, I_{EBO}	**	Tektronix 576, full-wave rectified, 60Hz

**I_{EBO} @ V_{EBO} = 8V or V_{EBO} @ I_{EBO} = 1mA, whichever occurs first as voltage is increased.

(6)	***$BV_{CEO}(sus)$, $BV_{CER}(sus)$	I_C = 100mA, except where noted by use of a slash, e.g., 950/40 means the voltage was measured at 40mA	(W) Semiconductor Division inductive test set. L = 20mH or 1000mH as noted.

***This test was initiated using L = 1000mH; however, destructive oscillations were sometimes observed with this inductance and L was reduced to 20mH for the remainder of the test.

7. CONCLUSIONS

Several important results are evident at this interim point in the program. Specifically it has been demonstrated that:

- Interdigitated thyristor fabrication techniques can be adapted to large-area ($\sim$ 4 cm^2), high-voltage ($BV_{CEO} \lesssim$ 1 kV) transistors.
- The forward SOA of the experimental transistors ($I_C \geq$ 4 A at V_{CE} = 100 V, for a 1 sec. power pulse) represents a significant improvement over the forward SOA of commercially available high-voltage transistors.
- Measured device performance shows good agreement with the predictions of a design theory that has been specifically developed for high-power switching transistors.

Finally, it should be noted that there is no major technological barrier to extending the techniques described here to the fabrication of even larger transistors. For example, 2 in. (50 mm) diameter thyristors are now in production. For a similar sized transistor, some effort would be required to increase the current capacity of the base lead. Nevertheless, a 2 in. transistor is a very real possibility.

What would the "volt-ampere" capability of such a transistor be? Listed below are estimates of the $h_{FE}I_C$ products for different BV_{CEO}(sus) values.

Predicted volt-ampere capability of a 2 inch (50 mm) diameter transistor

$BV_{CEO}(sus)$ (V)	$h_{FE}I_C$ @ V_{CE} = 3 V (A)	I_C (A)*	$I_C \cdot BV_{CEO}(sus)$ (kVA)*
400	9,000	1,800	720
500	6,100	1,220	610
600	4,000	800	480
800	2,060	412	330

*h_{FE} = 5

It is believed that a device of this size would open up major new applications for transistors (large motor control, transportation, induction heating, etc.) and thereby make a significant contribution to the field of power electronics.

8. PAPERS PUBLISHED UNDER THIS CONTRACT

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