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DJANAL USER'S MANUAL

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16. ABSTRACT

The DJANAL (DisJunct ANALyzer) Program provides a means for the LSI designer to format output from the Mask Analysis Program (MAP) for input to the FETLOG (FETSIM/LOGSIM) processor.

This document presents a brief description of the operation of DJANAL and provides comprehensive instruction for its use.

It is assumed that the reader is familiar with the purpose and utility of the MAP and FETLOG programs; thus, no attempt is made to describe either unless it is essential to the understanding of DJANAL.

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PREFACE

The DJANAL (DisJunct ANALyzer) program provides a means for the LSI designer to format output from the Mask Analysis Program (MAP) for input to the FETLOG (FETSIM/LOGSIM) processor.

This document presents a brief description of the operation of DJANAL and provides comprehensive instruction for its use.

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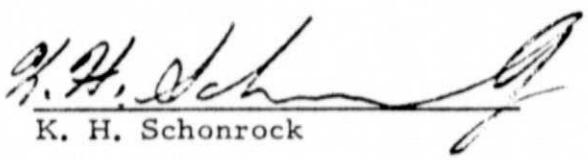

K. H. Schonrock

1. INTRODUCTION

The production of DJANAL arose out of a need for a means to transform the primitive output of the MAP processor into a form suitable for use as input to the FETLOG processor. Since due to its very nature the MAP processor generates fragmentary data for each device in a design, it is required that the pieces be put together to form the more common place lumped devices traditionally used in network simulation programs. Also, more importantly, the transistor equations generated by the MAP "BOOL" command must be analyzed to isolate and characterize disjunct circuits so that the logical function of the design ultimately may be determined.

DJANAL has been designed to allow the user to inject additional devices into the network via card input so that he may include off chip loading or modify effectively the MAP generated data. A natural extension of this capability provides the facility for analyzing a network that is input manually in its entirety.

Two output files are produced by the program with an attendant listing on the printer. The first output file consists of an input file for the LOGSIM portion of the FETLOG processor. This file will consist of at least one ROM card and an accompanying NET card for each disjunct circuit in the design. The disjuncts that have more than one output will have a ROM and a NET card for each such output. The second output file consists of a collection of input decks to the FETSIM portion of the FETLOG processor. There will be one FETSIM deck for each and every disjunct circuit in the design.

DJANAL has been designed to accept parametric and excitation data in an attempt to relieve the user of the burden of injecting this data at FETLOG run time. It is anticipated that editing of DJANAL output prior to running FETLOG will be unnecessary.

2. TECHNICAL DESCRIPTION

As previously discussed, the geometric nature of the MAP processor gives rise to data that is generally unusable and difficult to interpret in terms of lumped network devices. The first goal of the DJANAL processor is to organize and format the MAP output so that the devices are recognizable in their traditional form. Transistors are organized in a gate-source/drain node list; capacitors and resistors are organized in a from-to node list. Transistor channel dimensions are determined from MAP output that describes the source/drain boundaries of the transistors and must be created in a precise form with the MAP commands. The masks that are required are illustrated in Figure 2-1 and may be produced as depicted in the sample MAP command set presented in Appendix B. The DJANAL processor will expect parallel pairs of unit wide rectangles for channel dimension calculation. Any deviation from this requirement is certain to produce erroneous results. Please note that the MAP "RANG" command is insufficient to p luce channel information since the resulting output bears no distinction between channel width and channel length. As capacitors are read from the MAP file, successive capacitors between the same nodes will be added in parallel prior to being entered into the DJANAL data base. Resistors will be treated in the same manner with due regard for the different method for adding in parallel.

Once the internal representation of the network is established, DJANAL commences isolation of disjunct circuits by collecting groups of transistors having common source/drain nodes. Once a disjunct has been isolated, its output nodes are determined first by determining if any of the disjunct nodes connect to a transistor gate node of a transistor external to the disjunct and then by determining if any of the disjunct nodes have been specified as a circuit output. Once the disjunct and its output nodes have been identified, DJANAL finds the gate signal combinations that are required to connect the output to ground, the output to power, and to connect ground to power. Entries are made subsequently in a truth table according to the truth value of ground and power (negative true logic is supported) for each legal gate combination for the output being considered. Combinations that either connect ground to power or connect neither ground nor power to the output are considered illegal. Illegal combinations will have a truth table entry of indeterminate and will be resolved ultimately by the FETLOG processor.

As each disjunct is analyzed, a LOGSIM ROM card and a LOGSIM NET card is output for each output node and a FETSIM input deck is produced to represent the disjunct circuit. List output will be produced concurrent with the creation of the LOGSIM and FETSIM files to provide user insight to the results of the process.

TRANSISTOR CHANNEL MASKS

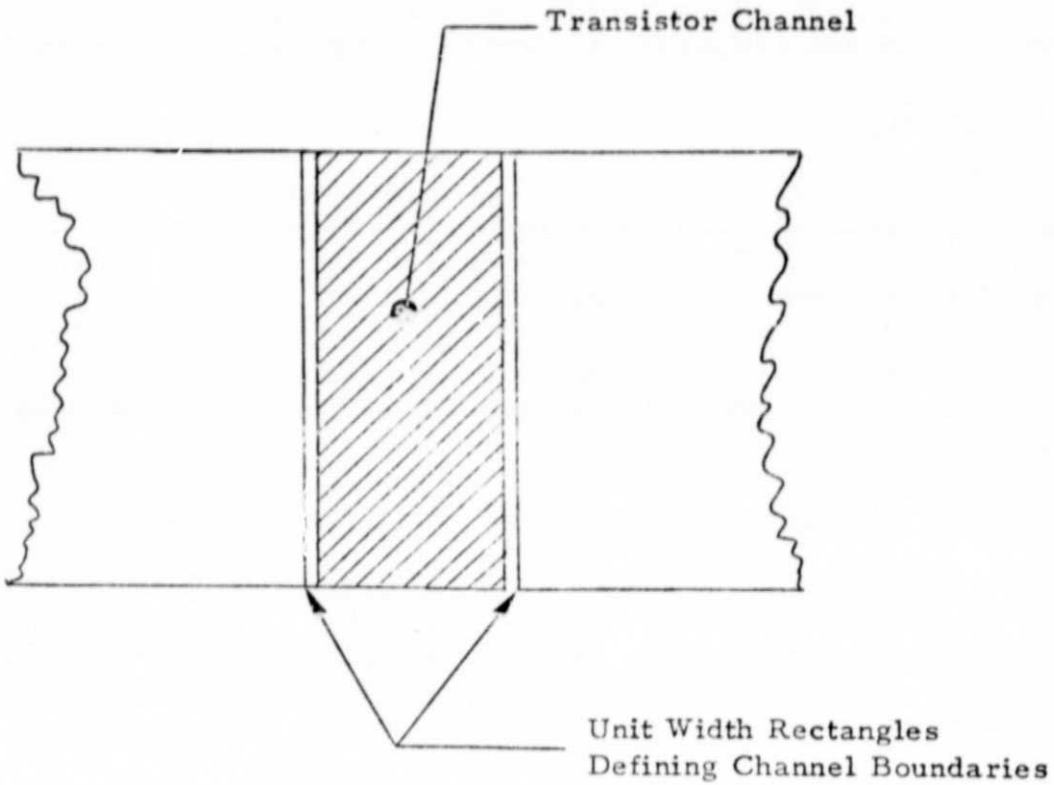

Figure 2-1

3. OPERATING INSTRUCTIONS

This section consists of ins ons for preparing DJANAL input data, a description of the format an tent of DJANAL output data and of job set-up instructions required t ecute the program on the Sigma-5 computer. Table 3-1 presents a summary of the files utilized by DJANAL.

3.1 Input Files

Input for DJANAL consists of a control input deck and a MAP put file (optional) containing data to describe the design components an the manner in which they are interconnected and excited. Table 3-2 describes the format of the input deck and Table 3-3 describes the format of the MAP file. The MAP file must be formatted and ordered precisely as shown for DJANAL to execute properly. It is permissible to omit any of the transistor, capacitor or resistor sections of the file as long as the specified order is maintained.

3.2 Output Files

Tables 3-4 and 3-5 describe the output produced for the LOGSIM and FETSIM portions of the FETLOG processor. List output consists of error message output and of summarizing information for each disjunct analyzed. Error messages are self-explanatory and usually cause premature termination of the program.

3.3 Scratch Files

Three scratch files are utilized by DJANAL to provide temporary storage of large amounts of data. Two of these files are consecutive files and require no further discussion; the third is a random access file and must be allocated with sufficient size to accommodate the design being processed. The number of words required for this file may be determined as follows:

$$W = T \times 7 + C \times 3 + R \times 3 + E \times 20$$

where: W = Number of words required
T = Number of transistors in design
C = Number of capacitors in design
R = Number of resistors in design
E = Number of cards in excitation deck.

FILE CHARACTERISTICS SUMMARY

Logical Unit No.	Organization	Mode	Format	Contents
5	Consecutive	Input	Card Images	DJANAL CONTROL INPUT
6	Consecutive	Output	Line Images	DJANAL LIST OUTPUT
10	Random	Scratch	Binary	
11	Consecutive	Scratch	Card Images	
12	Consecutive	Output	Card Images	FETSIM FILE
13	Consecutive	Scratch	Card Images	
14	Consecutive	Input	Card Images	MAP INPUT FILE
15	Consecutive	Output	Card Images	LOGSIM FILE

Table 3-1

DJANAL INPUT DECK

Card	Col	Format	DESCRIPTION
1.0	1-10	A	Enter "Parameters" in CC 1-10.
1.1	1-4	A	Process technology code: SOS - Silicon on sapphire CMOS - Metal gate CMOS. PMOS - Metal gate PMOS. NMOS - Metal gate NMOS.
	5-12	F	Threshold voltage for P-type transistors
	13-20	F	Threshold voltage for N-type transistors
1.2*	1-6	F	Relative permitivity of silicon dioxide
	7-12	F	Relative permitivity of silicon substrate
	13-18	F	Channel mobility of electrons
	19-24	F	Channel mobility of holes
	25-33	E	Doping level of N-substrate
	34-42	E	Doping level of P-well
	43-51	E	Gate oxide thickness
	52-57	F	Saturation curve slope for N-MOS
	58-63	F	Saturation curve slope for P-MOS
	64-67	F	Mobility variation factor for N-MOS
	68-71	F	Mobility variation factor for P-MOS
1.3			Provide "NAME" card as described on page 28 of LOGSIM User's Manual (may be omitted).
1.4			Provide "CONT" card as described on page 28 of LOGSIM User's Manual (may be omitted).
			*Refer to FETSIM Users Manual for a complete description of these parameters.

Table 3-2

DJANAL INPUT DECK
(Continued)

Card	Col	Format	DESCRIPTION
2.0	1-11	A	Enter "TRANSISTORS" in CC 1-11.
	13-15	A	Enter "MAP" in CC 13-15 if transistor data is to be read from MAP file.
	17-26	E	Scale factor for MAP transistor dimension data. Must be a value that will normalize MAP data to mils.
2.1	1	A	P = P-type transistor N = N-type transistor
	2-6	I	Gate node number of transistor
	7-11	I	Drain node number of transistor
	12-16	I	Source node number of transistor
	17-25	F	Effective channel width of transistor (Mils)
	26-34	F	Effective channel length of transistor (Mils)
	35-43	F	Threshold voltage for transistor (required only if it is desired to override value entered in card 1.1)
			• • •
			Repeat card type 2.1 as required to define all manually input transistors.
3.0	1-10	A	Enter "CAPACITORS" in CC 1-10.
	13-15	A	Enter "MAP" in CC 1-10 if capacitor data is to be read from MAP file.
	17-26	E	Scale factor for MAP capacitor data. Must be a value that will normalize MAP data to picofarads.
3.1	1-5	I	A node to which the capacitor is connected.
	6-10	I	The other node to which the capacitor is connected.
	11-22	E	Value of capacitance (picofarads)
			• • •
			Repeat card type 3.1 as required to define all manually input capacitors.

Table 3-2
(Continued)

DJANAL INPUT DECK
(Continued)

Card	Col	Format	DESCRIPTION
4.0	1-9	A	Enter "RESISTORS" in CC 1-9.
	13-15	A	Enter "MAP" in CC 13-15 if resistor data is to be read from MAP file.
	17-26	E	Scale factor for MAP resistor data. Must be a value that will normalize MAP data to K-ohms.
4.1	1-5	I	A node to which the resistor is connected
	6-10	I	The other node to which the resistor is connected
	11-22	E	Value of resistance (K-ohms)
			• • •
			Repeat card type 4.1 as required to define all manually input resistors.
5.0	1-10	A	Enter "EXCITATION" in CC 1-10.
5.1	1-4	A	Time scale for simulation: "MILL" - Milliseconds "MICR" - Microseconds "NANO" - Nanoseconds "PICO" - Picoseconds
	5-10	I	Maximum simulation time in units of specified time scale
	11	A	Logic value of ground ("L" for logic low, "H" for logic high)
	12-16	I	Node to which ground is connected
	17-24	F	Supply voltage - VDD (Volts)
	25-29	I	Node to which supply voltage is connected
	30-37	F	Clock voltage - VGG (Volts)
	38-42	I	Nodes to which VGG is connected
	43-47	I	Make entries as required for 2 phase and
	48-52	I	4 phase logic
	53-57	I	

Table 3-2
(Continued)

DJANAL INPUT DECK
(Continued)

Card	Col	Format	DESCRIPTION
5.2*	1-8	F	Voltage at which a signal is to be considered as switched from the low logic state to the high logic state
	9-16	F	Voltage at which a signal is to be considered switched from the high logic state to the low logic state
	17-24	F	Voltage rate of change for which a signal is considered to be stabilized
	25-32	F	Number of digits of numerical accuracy desired for simulation
	33-40	F	Initial integration time interval
	41-48	F	Simulation dwell value for output excursion
5.3			Provide a LOGSIM "GENF" card for each clock node as specified in CC 38-57 in card no. 5.1.
5.4			Provide LOGSIM "GEN" and "GENF" cards as required to define each logic input.
6.0	1-7	A	Enter "OUTPUTS" in CC 1-7.
6.1	1-72	8A8	Enter circuit output node numbers. Repeat card 6.1 as required to define all circuit outputs.
			*See FETLOG User's Manual for complete description of card 5.2 parameters.

Table 3-2
(Continued)

MAP INPUT FILE

Card	Col	Format	DESCRIPTION
1.0	10	I	The number "6" must be present in column 10.
1.1	1-10	I	Device number
	11-20	I	Source/drain node number
	21-30	I	Drain/source node number
	31-40	I	Gate node number
	41-50	I	Device Type code: = 2 for PNP transistor ≠ 2 for NPN transistor
	51-60	I	Functional Device Code: = 0 or 1 - device is transistor ≠ 0 or 1 - device is not a trans. and will be ignored
• • • •			Card type 1.1 repeated for each transistor
1.2	1-60	6I10	"-1" must be present in all fields to signal termination of transistor interconnect data.
2.0	10	I	The number "6" must be present in column 10.
2.10	1-10	I	Device number
	11-20	I	Pair number
	21-30	I	X1 - Coordinate pair defining endpoints
	31-40	I	Y1 of the diagonal of a unit wide
	41-50	I	X2 rectangle that defines edge
	51-60	I	Y2 of transistor channel
2.11	1-20	I	Device number
	11-20		Pair number (must match that of card 2.10)
	21-30	I	X1 - Coordinate pair defining endpoints
	31-40	I	Y1 of the diagonal of a unit wide

Table 3-3
(Continued)

MAP INPUT FILE
(Continued)

Card	Col	Format	DESCRIPTION
2.11	(Cont'd)		
	41-50	I	X2 rectangle that defines other
	51-60	I	Y2 edge of a transistor channel.
• • •			Card types 2.10 and 2.11 repeated for each transistor
2.2	1-60	6I10	"-1" must be present in all fields to signal termination of transistor dimension data.
3.0	10	I	The number "4" must be present in column 10.
3.1	1-10	I	Node number to which capacitor is connected
	11-20	I	The other node number to which capacitor is connected
	21-30	I	Whole number representing scaled capacitance
	31-40	I	Exponent (power of 10) by which capacitance (CC 21-30) is scaled
• • •			Card type 3.1 repeated for each capacitor
3.2	1-60	6I10	"-1" must be present in all fields to signal end of capacitor data.
4.0	1-10	I	The number "4" must be present in column 10.
4.1	1-10	I	Node number to which resistor is connected
	11-20	I	The other node number to which resistor is connected
	21-30	I	Whole number representing scaled resistance
	31-40	I	Exponent (power of 10) by which resistance is scaled
• • •			Card type 4.1 repeated for each resistor
4.2	1-60	6I10	"-1" must be present in all fields to signal end of resistor data.

Table 3-3
(Continued)

LOGSIM OUTPUT FILE

Card	Col	Format	DESCRIPTION
1			"SPEC" card as described in LOGSIM User's Manual. Parameters will be automatically generated by DJANAL.
2			"NAME" card copied directly from input deck.
3			"CONT" card copied directly from input deck.
4.0 • • 4.n			"ROM" cards specifying logical behavior of each output node of each DisJunct.
5.0 • • 5.n			"NET" cards specifying the interconnect structure of the DisJunct circuits.
6.0 • • 6.n			"GENF" and "[illegible]N" cards copied directly from input deck.

Table 3-4

FETSIM OUTPUT FILE

Card	Col	Format	DESCRIPTION
1.0	1-6	F	Relative permittivity of silicon dioxide.
	7-12	F	Relative permittivity of silicon substrate.
	13-18	F	Channel mobility of electrons.
	19-24	F	Channel mobility of holes.
	25-33	E	Doping level of N substrate.
	34-42	E	Doping level of P well.
	43-51	E	Gate oxide thickness.
	52-57	F	Slope factor for N-MOS.
	58-63	F	Slope factor for P-MOS.
	64-67	F	Mobility variation factor for N-MOS.
	68-71	F	Mobility variation factor for P-MOS.
1.1	1	I	= 1 to indicate SOS; blank otherwise.
	2-5	A	Time scale code: MILL indicates milliseconds. MICR indicates microseconds. NANO indicates nanoseconds. PICO indicates picoseconds.
	6	A	"+" to indicate positive true logic. "-" to indicate negative true logic.
	8-15	A	Node to which ground is connected.
	16-21	F	Value of V_{DD} (volts).
	22-29	A	Node to which V_{DD} is connected.
	30-35	F	Value of V_{GG} (volts).
	36-43	A	Nodes to which V_{GG} is connected. (entries as required for two and four phase logic)
	44-51	A	
	52-59	A	
	60-67	A	
1.2	1-8	F	Voltage at which a signal is to be considered as switched from the "low" logic state to the "high" logic state.

Used only for dynamic logic

Table 3-5

FETSIM OUTPUT FILE
(Continued)

Card	Col	Format	DESCRIPTION
	9-16	F	Voltage at which a signal is to be considered as switched from the "high" logic state to the "low" logic state.
	17-24	F	Voltage rate of change for which a signal is to be considered as stabilized.
	25-32	F	Number of digits of numerical accuracy desired for analog portion (FETSIM) of simulation.
	33-40	F	Initial integration time interval.
2.0	1-4	A	Circuit name.
	5-8	I	# of circuits of this type (will be set=1 by DJANAL).
	9-12	I	# of P transistors.
	13-16	I	# of N transistors.
	17-20	I	# of resistors.
	21-24	I	# of capacitors.
	25-28	I	# of input nodes.
	29-32	I	# of dependent nodes.
	33-36	I	# of output nodes.
	37-40	I	Initialization parameter (will be set=0 by DJANAL).
2.1			(Provide a type 2.1 card for each P transistor.)
	1-8	A	Gate node name.
	9-16	A	Drain node name.
	17-24	A	Source node name.
	25-33	F	Threshold voltage.
	34-42	F	Channel width (mils).
	43-51	F	Channel length (mils).
2.2			(Provide a type 2.2 card for each N transistor formatted identically as a type 2 card.)

Table 3-5
(Continued)

FETSIM OUTPUT FILE
(Continued)

Card	Col	Format	DESCRIPTION
2.3			(Provide a type 2.3 card for each resistor)
	1-8	A	From node name
	9-16	A	to node name
	17-25	F	resistance in KΩ
2.4			(Provide a type 2.4 card for each capacitor.)
	1-8	A	From node name
	9-16	A	to node name
	17-25	F	capacitance in picofarads
2.5	1-72	9A8	Output nodes of DisJunct, one name per eight column field. Repeat card type 2.5 as required to specify all output
2.6	1-72	9A8	Input nodes of Disjunct, one name per eight column field. Repeat card type 2.6 as required to specify all inputs.
			Repeat card types 2 as required to specify all Disjuncts in circuit.

Table 3-5
(Continued)

3.4 Sigma 5 Job Set-up Instructions

Presented below is the deck set-up required to execute **DJANAL** on the Sigma-5 computer using the CP-V operating system.

```
!JOB USER,ACCOUNT
!LIMIT (CORE,50),(TIME,10)
!ASSIGN F:5,(DEVICE,CR),(IN)
!ASSIGN F:6,(DEVICE,LP)
!ASSIGN F:10,(FILE,RAND),(RANDOM),(OUTIN),(RSTORE,50)
!ASSIGN F:11,(FILE,TEMP1),(OUTIN),(REL)
!ASSIGN F:12,(FILE,FETOUT),(OUT),(SAVE)
!ASSIGN F:13,(FILE,TEMP2),(OUTIN),(REL)
!ASSIGN F:14,(FILE,MAPFLE),(IN)
!ASSIGN F:15,(FILE,LOGOUT),(OUT),(SAVE)
!RUN (LMN,DJANAL)
!DATA
    :
  CARD INPUT DECK
    :
!FIN
```

APPENDIX A

Presented is a sample run of the DJANAL software on the Sigma-5 computer. Included is the list output, the resulting LOGSIM and FETSIM files, and the control input file used to run the program.

```
 17:13 JUL 07,'76 ID=00EF
JOB MSO3,EC45001
LIMIT (CORE,50),(TIME,10)
ASSIGN F:5,(FILE,SDAT1),(IN)
ASSIGN F:6,(DEVICE,LP)
ASSIGN F:10,(FILE,RAND),(RANDOM),(OUTIN),(RSTORE,50)
ASSIGN F:11,(FILE,TEMP1),(OUTIN),(REL)
ASSIGN F:12,(FILE,FETOUT),(OUT),(SAVE)
ASSIGN F:13,(FILE,TEMP2),(OUTIN),(REL)
ASSIGN F:14,(FILE,MAPFLE),(IN)
ASSIGN F:15,(FILE,LOGOUT),(OUT),(SAVE)
RUN (LMN,DANAL)
```

```
***** DISJUNCT CIRCUIT DETECTED AND ANALYZED, DESCRIPTION FOLLOWS *****

     DISJUNCT NAME:  A010

     P TRANSISTORS: SOURCE  DRAIN  GATE
                      4       1      7

     N TRANSISTORS: SOURCE  DRAIN  GATE
                      8       4      7

     CAPACITORS  :  FROM      TO
                      1        4
                      4        7
                      8        4

     OUTPUT NODES :     4

     INPUT NODES :     7


   ***** LOGIC ANALYSIS *****

        OUTPUT NODE    : OUT=    4

        GATE  TERMINALS:  G1=   7

             TRUTH TABLE:  G1   : OUT
                          ......:.....
                             0   :  1
                             1   :  0
 *** THE FOLLOWING ROM SPECIFICATION AND NET CARD HAVE BEEN GENERATED TO SIMULA
ROM      1  1A01110
NET      4         A011                    7
```

```
***** DISJUNCT CIRCUIT DETECTED AND ANALYZED, DESCRIPTION FOLLOWS *****

     DISJUNCT NAME:  A020

     P-TRANSISTORS: SOURCE  DRAIN  GATE
                      7       1      3
                      7       1      5
                      7       1      2
                      7       1      6

     N-TRANSISTORS: SOURCE  DRAIN  GATE
                     11       7      6
                     11      10      2
                     10       9      5
                      9       8      3

     CAPACITORS  :  FROM     TO
                      1       7
                      8       7
                      7       2
                      7       3
                      7       5
                      7       6
                      7       8
                      8       7
                      9       3
                      9       5
                      9       7
                     10       2
                     10       5
                     10       8
                     11       2
                     11       6
                     11       7
                     11       8

     OUTPUT NODES :    7

     INPUT NODES :     3       5       2       6

   ***** LOGIC ANALYSIS *****

        OUTPUT NODE     : OUT=    7

        GATE  TERMINALS: G1=    3
                         G2=    5
                         G3=    2
                         G4=    6

            TRUTH TABLE:  G1   G2   G3   G4   : OUT
                          ..................:.....
                           0    0    0    0   :  1
                           .    .    .    .   :  .
                           1    1    1    0   :  1
                           1    1    1    1   :  0
  *** THE FOLLOWING ROM SPECIFICATION AND NET CARD HAVE BEEN GENERATED TO SIMULA
ROM     1  4A021111111111111110
NET     7        A021                        3,5,2,6
  *STOP* END OF DJANAL EXECUTION
```

```
PCL
C FETBUT TB LP
 3.90011.700 500.0 400.0.1500E 16.1500E 16.1200E-04  .020  .010  .000  .000
 NANB+LB       10.0001          .000000      0      0      0
   9.500     .500     .010    7.000     .010    .000    .000    .000
A010  1   1   1   0   3   3   1   1   0
7        1        4              -1.500    4.605      .401
7        4        8               1.500    3.200      .201
1        4             .360
4        7             .150
8        4             .003
4
7
A020  1   4   4   0  18   6   4   1   0
3        1        7              -1.500    1.300      .401
5        1        7              -1.500    1.300      .401
2        1        7              -1.500    1.300      .401
6        1        7              -1.500    1.300      .401
6        7       11               1.500    3.600      .201
2       10       11               1.500    3.600      .201
5        9       10               1.500    3.200      .201
3        8        9               1.500    3.200      .201
1        7             .374
8        7             .150
7        2             .014
7        3             .010
7        5             .014
7        6             .135
7        8             .485
8        7             .193
9        3             .102
9        5             .102
9        7             .020
10       2             .113
10       5             .113
10       8             .485
11       2             .121
11       6             .113
11       7             .026
11       8             .485
7
3        5        2       6
```

```
C LOGOUT TO LP
SPEC    NAND 800,2,4
NAME
CONT
ROM     1  1A01110
ROM     1  4A021111111111111110
NET     4        A011                    7
NET     7        A021                    3,5,2,6
GEN       2
GEN       3
GEN       5
GEN       6
```

```
!PCL
PCL DOO HERE
<C SDAT1
PARAMETERS
 SOS    -1.5     1.5
   3.9  11.7  500.  400.   .15E16   .15E16  .12E-04   .02   .01   0   0
NAME
CONT
TRANSISTORS MAP         1.E-6
CAPACITORS  MAP        1.E-15
RESISTORS
EXCITATION
NAND   BOOL    8     10.    1
9.5     0.5     .01     7.      .01
GEN       2
GEN       3
GEN       5
GEN       6
OUTPUTS
    4
```

APPENDIX B

Presented is a MAP command set that adequately generates the data required for DJANAL execution. Other command sets may be equally appropriate if the resulting output conforms to the standards set forth in the body of this manual.

```
COMM  ABBREVIATED CMOS DESIGN ANALYSIS SET.  REVISED:  5/76
COMM  SCALE = 0.001 MIL
COMM
COMM  NEGATION OF THE N MASK
OPER  N = NGTV N
COMM
COMM       NODAL TRACE
COMM       -----------
COMM  PREPARE RECTANGLE ID'S FOR TRACE
SPEC  R1@0,S1@# 1,I1@# 1,R2@0,S2@# 1,I2@# 0
OPER  W = SAME W
SPEC  R1@0,S1@1 W,I1@# 1,R2@0,S2@# 2,I2@# 0
OPER  P = SAME P
SPEC  R1@0,S1@1 P,I1@# 1,R2@0,S2@# 3,I2@# 0
OPER  N = SAME N
SPEC  R1@0,S1@1 N,I1@# 1,R2@0,S2@# 4,I2@# 0
OPER  T = SAME T
SPEC  R1@0,S1@1 T,I1@# 1,R2@0,S2@# 5,I2@# 0
OPER  C = SAME C
SPEC  R1@0,S1@1 C,I1@# 1,R2@0,S2@# 6,I2@# 0
OPER  M = SAME M
COMM
TRAC  /M:C/C:M,P,N/P:C/N:C/
COMM
COMM       GENERAL ARTWORK CHECKING - PHASE 1
COMM       ---------------------------------
COMM
COMM  MINIMUM N-P SPACING BETWEEN DIFFERENT NODES = 0.4 MIL
SPEC  PRNT,TEMP,MAXW=399
OPER  NPSE = TWIX N,P              DIFF
COMM  MINIMUM METAL LINE WIDTH = 0.4 MIL
SPEC  MAXX=399
OPER  MLWX = SAME M
SPEC  MAXY=399
OPER  MLWY = SAME M
SPEC  PRNT,TEMP
OPER  MLWE = PLUS MLWX,MLWY
FREE  MLWX,MLWY
COMM  MINIMUM METAL-METAL SPACING = 0.3 MIL FOR LINES < 10 MILS LONG
SPEC  PRNT,TEMP,MAXW=299
OPER  MMSE = TWIX M                DIFF
COMM  MINIMUM METAL-METAL SPACING = 0.4 MIL FOR LINES > 10 MILS LONG
SPEC  PRNT,TEMP,MINL=10001,MAXW=399
OPER  MMSE = TWIX M                DIFF
COMM  MINIMUM METAL-TOX SPACING = 0.2 MIL
SPEC  PRNT,TEMP,MAXW=199
OPER  MTSE = TWIX M,T
COMM
COMM  SEPARATION OF P DIFFUSION INTO ACTIVE OR GUARD BAND AREAS
OPER  PA = NLNK P,W                LINE,LINE
OPER  PG = NINT P,PA
COMM  SEPARATION OF N DIFFUSION INTO ACTIVE OR GUARD BAND AREAS
```

```
OPER  NA = INTR N,W
OPER  NG = NINT N,NA
COMM
COMM  MINIMUM N GUARD BAND WIDTH = 0.4 MIL
SPEC  PRNT,TEMP,MAXA=399
OPER  NGWE = SAME NG
COMM  MINIMUM P GUARD BAND WIDTH OUTSIDE OF WELL = 0.6 MIL
SPEC  PRNT,TEMP,MAXA=599
OPER  PGWE = NINT PG,W
COMM  WELL PERIMETER MUST MEET OR OVERLAP P GUARD BAND
OPER  WPER = EDGE W              SAM1
OPER  WPER = EXPN WPER           5,5
SPEC  PRNT,TEMP,MINA=10
OPER  WPER = NINT WPER,PG
COMM  N GUARD BAND MAY NOT INTERSECT P GUARD BAND
SPEC  PRNT,TEMP
OPER  NWEE = INTR NG,PG
COMM  N GUARD BAND MUST TOTALLY SURROUND ALL P ACTIVE AREAS
OPER  VNG = VTWX NG              SAME
OPER  VNG = LINK VNG,PA          LINE,LINE
OPER  HNG = HTWX NG              SAME
OPER  HNG = LINK HNG,PA          LINE,LINE
SPEC  PRNT,TEMP
OPER  SURE = EXOR HNG,VNG
FREE  VNG,HNG
COMM
COMM      P TRANSISTOR IDENTIFICATION / CHECKING
COMM      ---------- ------------ --------
COMM
COMM  LOCATION OF PROSPECTIVE P CHANNELS
SPEC  MAXW=1000,R1@0,S1@# 1,R2@0,S2@# 1
OPER  PPC = TWIX PA              DIFF
SPEC  MINA=100
OPER  PC = INTR PPC,T
SPEC  MINA=100
OPER  PC = INTR PC,M
OPER  QPC = LINK PPC,PC          NONE,AREA
SPEC  R1@1,S1@# 1
OPER  QPC = LINK QPC             LINE
FREE  PPC,PC
COMM  MINIMUM P CHANNEL LENGTH = 0.3 MIL, WIDTH = 0.7 MIL
SPEC  MAXW=299,MAXL=699
OPER  PCE = TWIX PA              DIFF
SPEC  PRNT,TEMP
OPER  PCE = LINK PCE,QPC         NONE,AREA
COMM  MINIMUM THIN OXIDE WIDTH OUTSIDE EDGES OF P CHANNELS = 0.2 MIL
OPER  PCE = EXPN QPC             200,200
SPEC  PRNT,TEMP
OPER  PCE = NINT PCE,T
COMM  MINIMUM METAL WIDTH OUTSIDE EDGES OF P CHANNELS = 0.1 MIL
OPER  PCE = EXPN QPC             100,100
SPEC  PRNT,TEMP
OPER  PCE = NINT PCE,M
COMM
COMM  LOCATION OF P SOURCES AND DRAINS
SPEC  R1@0,S1@# 1
OPER  PSD = SAME PA
OPER  PSD = LINK PSD,QPC         LINE,LINE
OPER  PSD = INTR PSD,PA
```

```
COMM
COMM   P SOURCE AND DRAIN MINIMUM WIDTH = 0.1 MIL
SPEC   PRNT,TEMP,MAXA=99
OPER   PSDE = SAME PSD
COMM   MINIMUM SPACING OF TOX TO OUTSIDE P SOURCE/DRAIN EDGES = 0.1 MIL
OPER   PSDE = EXPN PSD              5,5
SPEC   PRNT,TEMP,MAXA=104
OPER   PSDE = NINT PSDE,T
COMM
COMM   LOCATION OF P CHANNEL GATE METAL
SPEC   R1@0,S1@# 1
OPER   PGM = SAME M
OPER   PGM = LINK PGM,QPC           LINE,AREA
OPER   PGM= INTR PGM.M
COMM
COMM   MINIMUM P CHANNEL GATE METAL OVERLAP ON N GUARD BAND = 0.2 MIL
OPER   PGME = EXPN NG               50,50
SPEC   PRNT,TEMP,MAXA=249
OPER   PGME= INTR PGM,PGME
COMM   P CHANNEL GATE MUST CROSS N GUARD BAND EDGE BEFORE THICK OX. STEP
OPER   PGME = LINK T,NG             LINE,LINE
OPER   PGME = TWIX NG,PGME
SPEC   PRNT,TEMP
OPER   PGME = INTR PGM,PGME
COMM
COMM        N TRANSISTOR IDENTIFICATION / CHECKING
COMM        ---------------------------------------
COMM
COMM   LOCATION OF PROSPECTIVE N CHANNELS
SPEC   MAXW=1000,R1@0,S1@# 1,R2@0,S2@# 1
OPER   PNC = TWIX NA                DIFF
SPEC   MINA=100
OPER   NC = INTR PNC,T
SPEC   MINA=100
OPER   NC = INTR NC,M
OPER   QNC = LINK PNC,NC            NONE,AREA
SPEC   R1@1,S1@1 QPC
OPER   QNC = LINK QNC               LINE
FREE   PNC,NC
COMM
COMM   MINIMUM N CHANNEL LENGTH = 0.3 MIL, WIDTH = 0.7 MIL
SPEC   MAXW=299,MAXL=699
OPER   NCE = TWIX NA                DIFF
SPEC   PRNT,TEMP
OPER   NCE = LINK NCE,QNC           NONE,AREA
COMM   MINIMUM TOX WIDTH OUTSIDE EDGES OF N CHANNELS = 0.2 MIL
OPER   NCE = EXPN QNC               200,200
SPEC   PRNT,TEMP
OPER   NCE = NINT NCE,T
COMM   MINIMUM METAL WIDTH OUTSIDE EDGES OF N CHANNELS = 0.1 MIL
OPER   NCE = EXPN QNC               100,100
```

```
SPEC  PRNT,TEMP
OPER  NCE = NINT NCE,M
COMM
COMM  LOCATION OF N SOURCES AND DRAINS
SPEC  R1@0,S1@# 1
OPER  NSD = SAME NA
OPER  NSD = LINK NSD,QNC        LINE,LINE
OPER  NSD = INTR NSD,NA
COMM
COMM  N SOURCE AND DRAIN MINIMUM WIDTH = 0.1 MIL
SPEC  PRNT,TEMP,MAXA=99
OPER  NSDE = SAME NSD
COMM  MINIMUM SPACING OF TOX TO OUTSIDE N SOURCE/DRAIN EDGES = 0.1 MIL
OPER  NSDE = EXPN NSD           5,5
SPEC  PRNT,TEMP,MAXA=104
OPER  NSDE = NINT NSDE,T
COMM
COMM  LOCATION OF N CHANNEL GATE METAL
SPEC  R1@0,S1@# 1
OPER  NGM = SAME M
OPER  NGM = LINK NGM,QNC        LINE,LINE
OPER  NGM = INTR NGM,M
COMM
COMM  MINIMUM N CHANNEL GATE METAL OVERLAP ON P GUARD BAND = 0.2 MIL
OPER  NGME = EXPN PG            50,50
SPEC  PRNT,TEMP,MAXA=249
OPER  NGME = INTR NGM,NGME
COMM  N CHANNEL GATE MUST CROSS P GUARD BAND EDGE BEFORE THICK OX. STEP
OPER  NGME = LINK T,PG          LINE,LINE
OPER  NGME = TWIX NG,NGME
SPEC  PRNT,TEMP
OPER  NGME = INTR NGM,NGME
COMM
COMM      GENERAL ARTWORK CHECKING - PHASE 2
COMM      ----------------------------------
COMM  MINIMUM SPACING BETWEEN P NON-SOURCE/DRAIN NODE AND ANY OTHER P
COMM  NODE = 0.4 MIL
OPER  PNSD = NINT P,PSD
SPEC  PRNT,TEMP,MAXW=399
OPER  PPSE = TWIX PNSD,P        DIFF
COMM
COMM  MINIMUM SPACING BETWEEN N NON-SOURCE/DRAIN NODE AND ANY OTHER N
COMM  NODE = 0.4 MIL
OPER  NNSD = NINT N,NSD
SPEC  PRNT,TEMP,MAXW=399
OPER  NNSE = TWIX NNSD,N        DIFF
COMM
COMM  MINIMUM CONTACT WIDTH = 0.3 MIL, LENGTH = 0.4 MIL
SPEC  MINA=300
OPER  CS = SAME C
SPEC  PRNT,TEMP
OPER  CSE = NINT C,CS
```

```
SPEC  PRNT,TEMP,MAXA=399
OPER  CSE = SAME CS
FREE  CS
COMM  MINIMUM SEPARATION OF STEPPED OX. AND CONTACT OPENING = 0.1 MIL
OPER  EXC = EXPN C              100,100
SPEC  PRNT,TEMP
OPER  CTOE = NINT EXC,T
FREE  EXC
COMM  MINIMUM SEPARATION OF CONTACT OPENING TO SOURCE/DRAIN = 0.2 MIL
OPER  SD = PLUS PSD,NSD
SPEC  PRNT,TEMP,MAXA=199
OPER  SDCE = NINT SD,C
COMM  METAL MUST COVER SOURCE/DRAIN CONTACT OPENINGS
OPER  SDC = LINK C,SD           LINE,AREA
SPEC  PRNT,TEMP
OPER  MCOE = NINT SDC,M
COMM  MINIMUM METAL OVERLAP OVER EDGE OF OTHER CONTACTS = 0.2 MIL
OPER  OC = NINT C,SDC
OPER  EXOC = EXPN OC            200,200
SPEC  PRNT,TEMP
OPER  MCOE = NINT EXOC,M
FREE  SDC,OC,EXOC,PNSD,NNSD
COMM  MINIMUM PENETRATION OF TOX IN GUARD BAND FOR GATE CROSS = 0.2 MIL
OPER  GM = PLUS PGM,NGM
OPER  GB = PLUS PG,NG
OPER  TOXE = INTR GM,GB
SPEC  PRNT,TEMP,MAXA=199
OPER  TOXE = INTR T,TOXE
FREE  GM,GB
COMM  MINIMUM SEPARATION BETWEEN TOX AND OUTSIDE SOURCE/DRAIN = 0.2 MIL
SPEC  PRNT,TEMP,MAXW=199
OPER  TOXE = TWIX T,SD
COMM  MINIMUM SEPARATION OF TOX AND OUTSIDE METAL = 0.2 MIL
SPEC  PRNT,TEMP,MAXW=199
OPER  TOXE = TWIX T,M
COMM
COMM      EQUATION GENERATION
COMM      -------------------
COMM
SPEC  E2@1
OPER  PG = SAME PG
SPEC  E2@1
OPER  NG = SAME NG
BOOL  /&/PG:0/NG:1/PSD:PSD,'PGM/NSD:NSD,NGM/
COMM
COMM      CALCULATION OF CHANNEL DIMENSIONS
COMM      ---------------------------------
COMM
SPEC  E2@1
OPER  OC = PLUS QPC,QNC
SPEC  R1@0
```

```
OPER  QC = EXPN QC  1,1
SPEC  E2@1
OPER  SD= SAME SD
OPER  QC = INTR SD,QC     SAM2
SPEC  MAXX=1,MAXY=1
OPER  Q = SAME QC
OPER  QC = NINT QC,Q
FREE  Q
FILE  6,0,QC
FREE  QC
FREE  SD
COMM
COMM       CAPACITANCE CALCULATION
COMM       ---------- -------
COMM  EXPAND AND COMBINE DIFFUSIONS
OPER  EXP = EXPN P              50,50
OPER  EXN = EXPN N              50,50
OPER  DIFF = PLUS EXP,EXN
COMM  CATEGORIZE METAL BY TOX
OPER  MTHN = INTR M,T
OPER  MTHK = NINT M,MTHN
OPER  MTHN = NINT MTHN,C
COMM
COMM  SETUP JUNCTION CAPACITANCE-SCALED MASKS
OPER  JCA = SCAL EXP            7,-2
OPER  JCHE = HEDG EXP
OPER  JCHE = EXPN JCHE          1,50
OPER  JCVE = VEDG EXP
OPER  JCVE = EXPN JCVE          50,1
OPER  CAP = PLUS JCVE,JCHE
OPER  CAP = PLUS CAP,JCA
OPER  CAP = LINK CAP,NG         NONE,POIN
FREE  JCA,JCHE,JCVE,EXP,EXN
COMM
COMM  SETUP CROSSOVER CAPACITANCE-SCALED MASKS
OPER  DTHK = INTR DIFF,MTHK
OPER  DTHN = INTR DIFF,MTHN
OPER  DTHN = SCAL DTHN          10,1
OPER  CAP = PLUS CAP,DTHK
OPER  CAP = PLUS CAP,DTHN
FREE  DTHK,DTHN
COMM
COMM  SETUP SUBSTRATE CAPACITANCE-SCALED MASKS
OPER  STHK = NINT MTHK,DIFF
OPER  STHK = LINK STHK,NG       NONE,POIN
OPER  STHN = NINT MTHN,DIFF
OPER  STHN = SCAL STHN          10,1
OPER  STHN = LINK STHN,NG       NONE,POIN
OPER  CAP = PLUS CAP,STHK
OPER  CAP = PLUS CAP,STHN
COMM
COMM  GENERATE CAPACITANCE VALUES
AREA  6,CAP,-50000
FREE  DIFF,MTHK,MTHN,STHK,STHN,CAP
```


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