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SOLID STATE, CCD - BURIED CHANNEL, TELEVISION CAMERA STUDY AND DESIGN

Final Report

July 1976

For

NASA LYNDON B. JOHNSON SPACE CENTER

FAIRCHILD IMAGING SYSTEMS
A Division of Fairchild Camera and Instrument Corporation
300 Robbins Lane, Syosset, New York, 11791

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SOLID STATE, CCD-BURIED CHANNEL, TELEVISION CAMERA STUDY AND DESIGN

Final Report
February 5, 1976 through June 15, 1976
By
K.A. Hoagland
H. Balopole

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Approved by: ____________
I. Hirschberg
Director, Electro-Optical Systems

ABSTRACT

An investigation of an all solid-state television camera design, which uses a buried channel charge-coupled device (CCD) as the image sensor, was undertaken. A 380 x 488 element CCD array is utilized to ensure compatibility with 525 line transmission and display monitor equipment. Specific camera design approaches selected for study and analysis include (a) optional clocking modes for either fast (1/60 second) or normal (1/30 second) frame readout, (b) techniques for the elimination or suppression of CCD blemish effects, and (c) automatic light control and video gain control (i.e., ALC and AGC) techniques to eliminate or minimize sensor overload due to bright objects in the scene. Preferred approaches are determined and integrated into a design which addresses the program requirements for a deliverable solid state TV camera.

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SECTION I

INTRODUCTION

The objective of this program for NASA/JSC is to design, develop, test and deliver an all-solid state television camera utilizing a buried channel CCD (charge coupled device) as the image sensor. This Final Report describes the results achieved during the initial Study and Design phase of the program, as defined by the Exhibit "A" requirements of Contract No. NAS 9-14844. The report covers the period from 5 February to 15 June, 1976.

The report is organized in four sections. General background information concerning buried channel CCD image sensors and CCD-TV camera design is presented in Section 2. Section 3 describes detailed Study and Design results. These results are briefly summarized in Section 4. It is concluded that NASA/JSC objectives for the deliverable solid-state TV camera (in accordance with Exhibit "B" requirements of NAS 9-14844) can be achieved.

SECTION 2

TECHNICAL BACKGROUND

The Fairchild design approach to the NASA/JSC requirement is based on the utilization of basic CCD sensor and camera design principles which fully address the requirement for compatibility with 525-line television standards. This section presents general background information concerning these principles.

2.1 CCD SENSOR

Charge-coupled image sensors integrate photon-generated minority carriers in depletion wells formed by the application of a bias voltage to elements of a control electrode (gate) structure overlaying photosensitive regions of the substrate. Following an integration period, the carriers are transported as individual signal packets by potential well motions induced by clocking the gate electrodes. After a sequence of transport steps determined by device organization, signal packets corresponding to element rows are serially shifted to an on-chip detector for conversion to an output video signal.

The cell organization of a CCD and the number of charge transport gates (phase lines) per cell, are of concern to the camera designer since precisely timed gate drive waveforms must be supplied to the device for self-scan operation. The interline-transfer (ILT) organization is used exclusively for the Fairchild family of area array CCD's, which includes designs with 100 x 100, 190 x 244 and 380 x 488 elements. These designs employ two-phase (2Ø) charge transport principles which, in combination with the ILT organization, minimizes the number and complexity of gate drive waveforms necessary for device operation. In addition, these designs all utilize buried-channel charge transport principles. In a buried-channel CCD, the signal carriers are kept away from the silicon surface by an electrical field associated with an implanted layer of ions. Thus the trapping of carriers by surface states is inhibited resulting in high charge-transfer efficiencies which are essentially independent of the signal charge magnitude. For the 190 x 244 and 380 x 488 designs, buried-channel operation has been combined with on-chip low-noise floating-gate amplifiers. The combination of features extends the CCD performance range to threshold signal levels of a few tens of electrons per depletion well.

Figure 1 illustrates the ILT organization and the forcing-function inputs required for self-scan operation as a TV image sensor. The unit cells contain one photosensor site and an adjacent light-shielded site

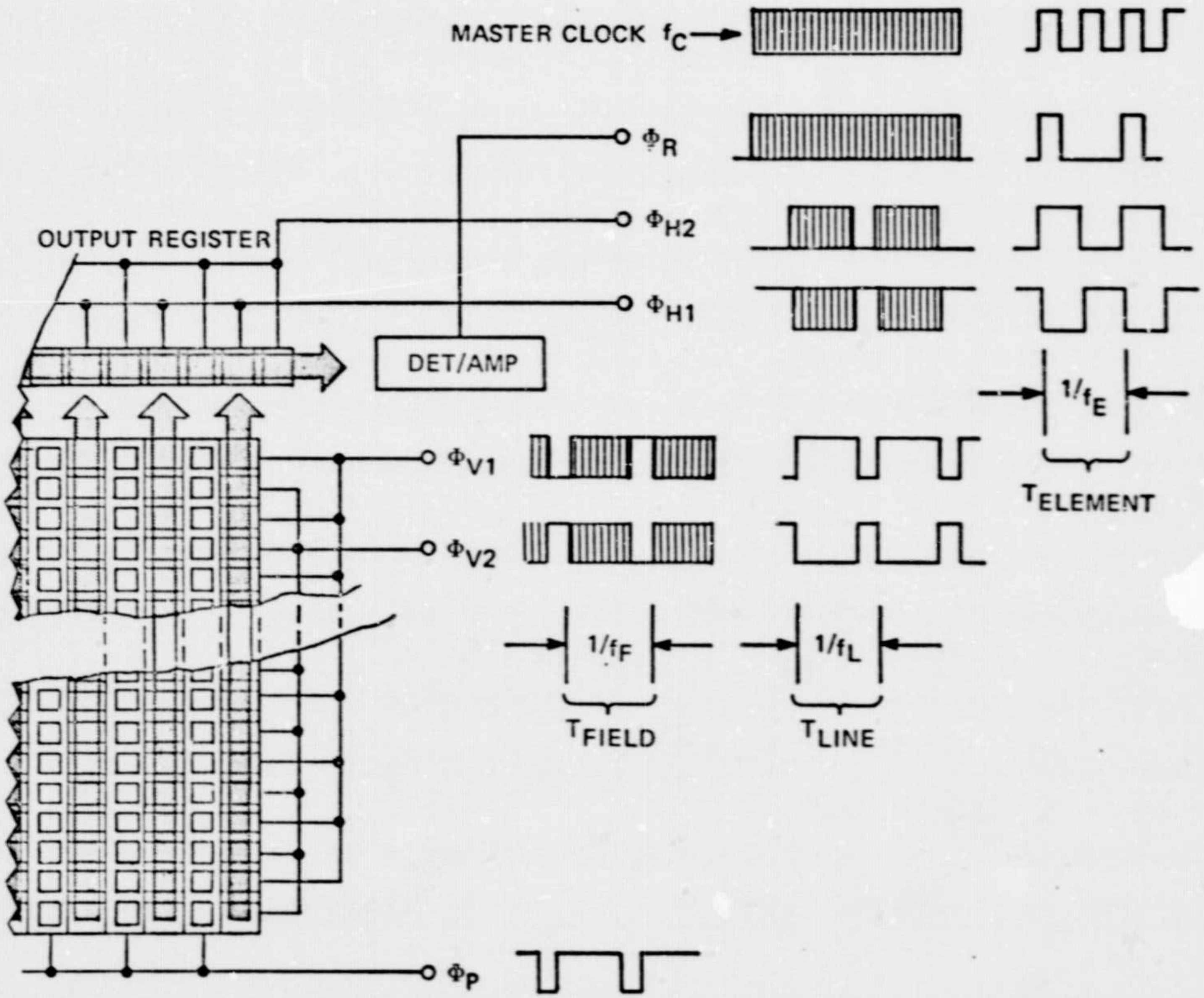


FIGURE 1

INTERLINE TRANSFER CCD ORGANIZATION AND DRIVE INPUT WAVEFORMS

75-1030

which is one-half stage of a 2ϕ vertical-transport register. Cell dimensions are defined by comb channel stop boundaries on three sides of the photosite. Alternate cell rows are uniquely assigned to each of the two fields comprising a TV frame resulting in higher vertical MTF than for beam-scanned or frame-transfer type image sensors. An implanted potential barrier at the photosite/transfer site interface inhibits transfers to the vertical column register, except when the photogate (ϕ_p) is LOW and the adjacent transfer gate (ϕ_{V1} or ϕ_{V2}) is HIGH. Thus, 2/1 interlace readout is achieved by pulsing ϕ_p LOW during each vertical blanking interval and applying complementary ϕ_{V1}, ϕ_{V2} waveforms with HIGH states during alternate V-blanking periods.

At the start of the ODD field readout, elements corresponding to odd number rows are first shifted in unison into adjacent ϕ_{V1} sites for row transport along the column registers to the output register. The EVEN field sequence is similar except the initial shift is into ϕ_{V2} sites. Row transfers at the output register interface (for both ODD and EVEN rows) are effected by holding ϕ_{V1} LOW and ϕ_{H1} HIGH during the horizontal blanking interval. Complementary square-wave pulses at element rate are applied to the ϕ_{H1}, ϕ_{H2} transport gates to serially shift packets to the output detector.

2.2 CAMERA DESIGN FOR 525-LINE TELEVISION

Circuit functions for a TV camera using interline-transfer image sensors are illustrated in the block diagram, Figure 2. With the exception of the CCD and its associated gate drive waveforms, similar functions (plus horizontal and vertical scanning) are necessary for conventional camera designs using beam-scanned image sensors. A typical ILT-CCD camera logic design employs a crystal clock at frequency $f_C = 2f_E$, where f_E is the element readout rate, to provide decoding edges for pulses shorter in duration than an element period. All CCD gate waveforms, and the display sync and blanking signals, are derived from f_C by divide-down counters and combinational logic circuits.

A beam-scanned camera design requires relatively complex logic circuits to conform with 525-line TV system specifications such as EIA RS-170. In this case, the function of the logic is to synthesize synchronization and blanking waveforms with timing edges defined from the output of a master clock operating at a high multiple of the line scan frequency f_L. A typical single-chip MOS-LSI TV signal generator, such as the Fairchild type 3262, is controlled by a crystal clock operating at $910f_L$, facilitating the generation of a synchronous NTSC color subcarrier output at the nominal US Standard 3.58 MHz rate . Decoding edges for either monochrome or color system outputs are derived from an on-chip square wave clock at $130f_L$.

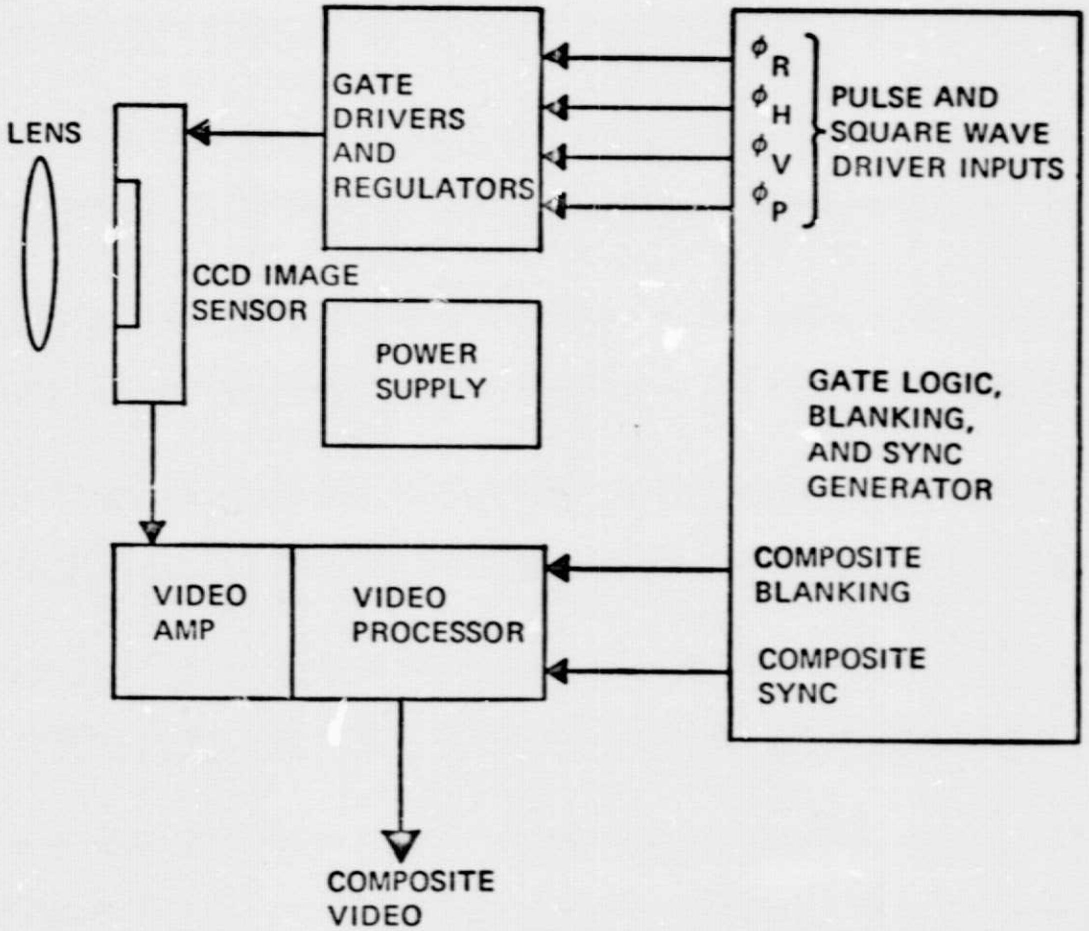


FIGURE 2

FUNCTIONAL REQUIREMENTS FOR A CCD-TV CAMERA UTILIZING AN ILT AREA IMAGE SENSOR

75-1031

Although existing waveform generators such as the 3262 do not provide CCD gate signal outputs, a modified CCD/RS-170 compatible design is feasible if the CCD design conforms to system specifications. For CCD imaging sensors, conformance implies a precisely defined number of readout lines per field. Also, if the CCD sensor element counts per line are properly defined, a simplified camera logic design using a single master clock input is possible.

In accordance with 525-line monochrome system specifications, the nominal values required for readout scan parameters are: line rate f_L = 15,750 Hz; field rate f_F = 60 Hz; and frame rate f_P = 30 Hz (with 2/1 field/frame interlace). The RS-170/3262 vertical blanking interval is (20 + 22/130) line periods/field, defining a minimum of (525-40) = 485 active scan lines, hence sensor element rows per frame.

Horizontal blanking is defined as (22/130) horizontal line periods, which is equivalent to: $(22/130)(n_A + n_B) = (22/130)\, n_T$ where n_A, n_B and n_T define the active, blanked, and total number of element periods/line period, respectively. If n_T is selected to be 910/2 = 455, a single master clock can be used to satisfy the requirements for both RS-170 and CCD gate-drive waveform synthesis. For this condition, $n_B = (22/130) \times 455 = 77$, and $n_A = (n_T - n_B) = 378$. The CCAID-488 sensor has 380 elements/row, and 488 rows, hence a few terminal rows and columns can be blanked off when blanking signal edges are properly centered with respect to the active format region.

SECTION 3

STUDY AND DESIGN RESULTS

This section presents a technical synopsis of program results for each of the tasks defined by Section 3.0 requirements of the contract Exhibit "A" Statement of Work. Major subsection headings conform with the subsection nomenclature of Exhibit "A".

3.1 STUDY REQUIREMENTS

Study tasks were selected to develop alternate approaches and concepts applicable to SOW objectives. These were then examined in detail, including breadboard tests where necessary, to determine preferred approaches and concepts to be implemented in the deliverable solid state camera. Study task results are described in the Clocking Options, Blemish Suppression and Light Control subsections which follow.

CLOCKING OPTIONS

The 380 x 488 CCD sensor was specifically designed for 2/1 interlaced readout with separate photosensor rows for addressing each active line of the displayed TV frame. The integration time for the normal high-resolution readout mode is 1/30 second. There is an alternate readout clocking scheme which can be used when it is desirable to shorten the integration time to 1/60 second. In this mode charge packets from vertically adjacent sites along the even and odd field rows are added together in the vertical shift register before the normal charge transport clocking begins. Although the alternate mode has less vertical resolution than the normal mode the difference can be minimized by performing the addition differently on alternate fields. For example during the first field sensor rows 1 and 2, 3 and 4, 5 and 6, etc., are added together. During the next field sensor rows 2 and 3, 4 and 5, 6 and 7, etc. are added, with the row-addition sequence for subsequent fields alternating at field rate.

Because of the digital nature of the charge transport functions, relatively simple circuit modifications can be used to change the clocking system from normal to alternate mode operation. Feasibility for alternate mode operation was established by breadboard tests. Vertical resolution was observed to be about 2/3 of the normal Nyquist limit value. It was also determined that it is feasible to design the deliverable camera with a selector switch to enable operation in either mode.

Although the alternate mode has less static vertical resolution than the normal mode, there are compensating advantages: (1) shorter integration times can improve resolution when viewing moving images and (2) since all photosensing sites are read out during the same field interval, the alternate mode is preferred for sequential color TV applications.

BLEMISH SUPPRESSION

Early 380 x 488 arrays were relatively free of cosmetic defects except for isolated single element blemishes which appeared as white spots in the video display. To suppress these blemishes a Field Programmable Logic Array (FPLA) was considered for inclusion in the video processor circuit. The FPLA is a digital memory which can be used to store the locations of defective CCD elements. As shown in Figure 3 the FPLA accepts inputs from synchronous line and element counters. When a count corresponding to the location of the defective element is decoded, the FPLA provides a pulse output which can be used to inhibit the defective readout.

During the breadboard test phase of the FPLA investigation, significantly improved blemish quality was achieved with 380 x 488 arrays from runs being fabricated for NAVELEX program requirements. A number of arrays were free of blemishes larger than one element when tested at room temperature and several devices exhibited near-zero defect counts when cooled to reduce the average dark current level. Nearly all defects were adequately suppressed at -10°C.

Since Fairchild is confident that further improvements in array quality can be expected, the FPLA blemish suppression technique, which adds circuit complexity, is not considered a desirable feature for inclusion in the deliverable camera. A means for array temperature control, such as a thermoelectric cooler, is desirable since it has been established that both dark signal and blemishes can be significantly reduced by cooling.

LIGHT CONTROL

Wide-range light control is necessary to prevent overload of the CCD sensor when viewing solar illuminated scenes in a space environment. Table 3-1 illustrates a calculation for the minimum control range assuming 100% diffuse reflectance scene surfaces exposed to solar illumination outside the earth's atmosphere. If the camera is equipped with a f1.4 lens, the effective lens f value must be increased to at least f93 to prevent overload, indicating a minimum light control range of $4.4 \times 10^3/1$.

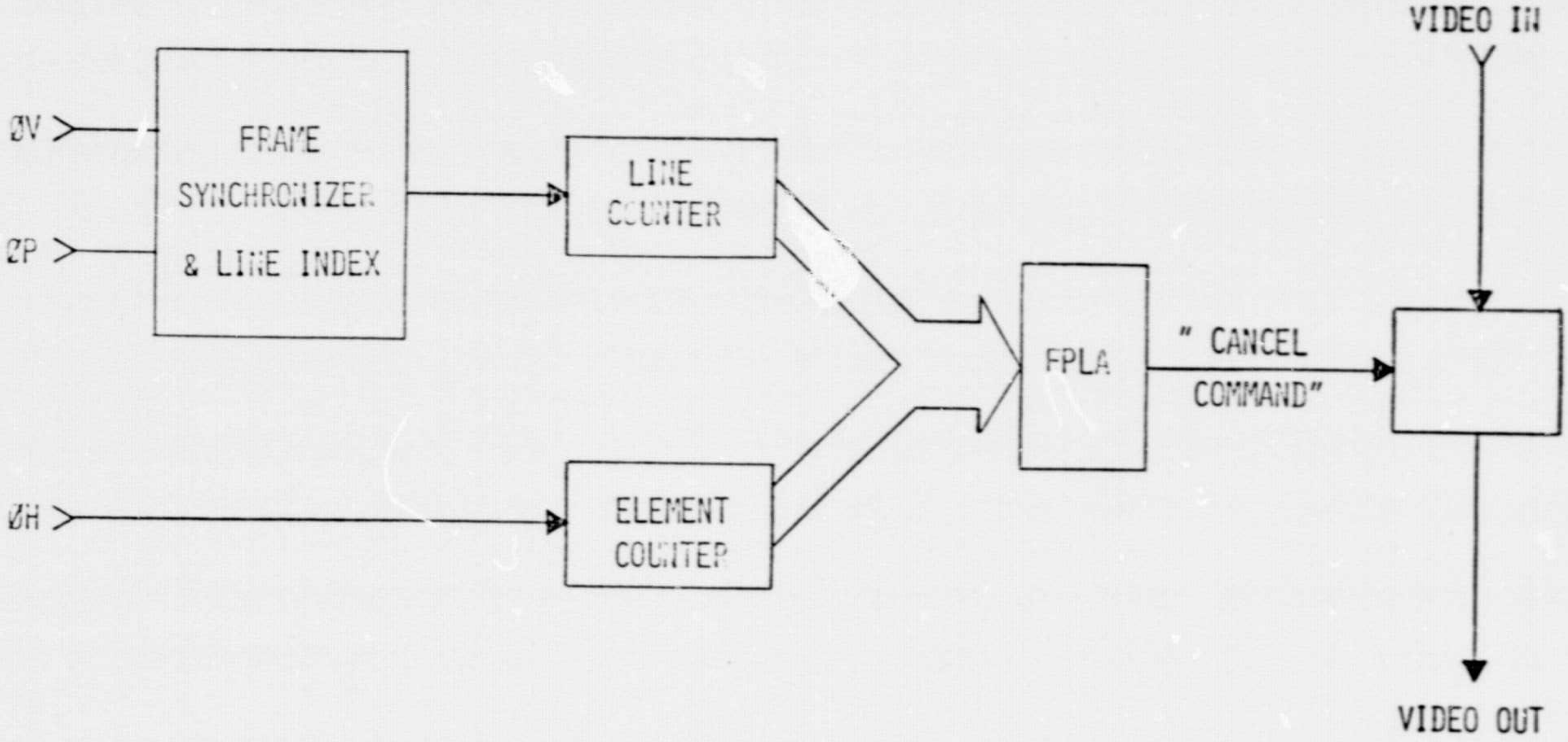


FIGURE 3

FPLA BLEMISH CANCELLATION

TABLE 3-1

LIGHT CONTROL RANGE

SENSOR SATURATION: $I_{max} \simeq 0.3$ lumens/sq. ft., 6000°K

SCENE LUMINANCE: Max. highlight, $B_{scene} = 1.3\times10^4$ lumens/sq. ft

OPTICAL EFFICIENCY, α : $\alpha = \frac{t}{4f^2} = 0.2/f^2$

$$\alpha_{min} = I_{sensor}/B_{scene} = 0.3/1.3\times10^4 \simeq 2.3\times10^{-5}$$

LIGHT CONTROL RANGE: $f_{max} = (0.2/2.3\times10^{-5})^{1/2} \simeq 93$

$f_{max}/f_{min} = 93/1.4 = 66.4$

$\therefore$ Minimum Control Range $= (f_{max}/f_{min})^2 \simeq 4.4\times10^3/1$

CONDITIONS: 25 mA/W, 2854K CCD response; 30F/S

Solar Illuminance, 100% Diffuse Reflectance Surfaces

Transmission, $t = 0.8$

$f_{min} = 1.4$

In order to assess the problem if specularly reflecting test objects are considered, an outdoor simulation test was conducted using a Fairchild Type MV201 CCD-TV camera. The results of this test are given in Table 3-2. In this case an attenuation in the optical path equivalent to f1100, was necessary to avoid overload with the standard Fairchild minus-red filter in front of the lens. With smaller f-values than those indicated, specularly reflected spot images caused CCD sensor blooming along the column direction.

Specular solar images can be expected if the camera is required to view space objects with a polished metallic finish, or other reflective-type surface. To minimize blooming for this condition, the light control range should be two or three orders of magnitude greater than the value indicated in Table 3-1 for diffuse reflectance surfaces.

Techniques for light control over the required range include a number of approaches such as filter wheels, movable film-strip filters, and lens iris-spot filters, which can be broadly classified as approaches requiring electro-mechanical control. The electro-optical approaches investigated, such as PLZT and liquid-crystal light valves were limited in control range (i.e. 10^2 to 10^3) with relatively poor open state transmission characteristics ($t \approx 0.2$)

The approach selected for the deliverable camera is based on the iris-spot filter principle, as implemented in commercially available Cosmicar type ES auto-iris lenses. Characteristics for three lenses, with 12.5, 25, and 50 mm focal lengths, are given in Table 3-3.

The light control range of the lens ($\cong 7 \times 10^4$) will be extended by utilizing the dynamic range inherent in the CCD sensor. This is implemented with separate control loops for the automatic light control (ALC) and automatic gain control (AGC) functions of the camera electronics, as indicated in Figure 4.

3.1.1 Design Requirements

The concepts and theories emanating from the study effort have been integrated into a preliminary design for the deliverable solid-state camera. The camera circuitry is shown in block diagram form in Figure 5. The logic, driver and video processor circuits are similar to existing circuitry developed on contract No. N00010-75-C-0289 for a Missile Guidance Camera utilizing a 380 x 488 CCD array. These circuits are contained on three printed circuit cards.

TABLE 3-2

MV 201 OUTDOOR TEST RESULTS

"DR" Test Object Luminance, B = 8800 ft. L.

Solar Illumination, I = $8800/0.9 \cong 10^4$ fc

Array Sat, "DR" Test Object		f equiv.
With MR Filter:	f2.8 + ND 2	f28
Without Filter:	f8.0 + ND 2	f80

Array Sat "SR" Test Object		
With MR Filter:	f11 + ND 4	f1100
Without Filter:	f22 + ND 4	f2200

(MR Filter Factor Equiv. To Schott KG-3, 5.5 mm)

NOTES:

1. "DR" test object is a Kodak Test Card, diffuse reflectivity $\cong$ 0.9.
2. "SR" test object is a mettalic-coated plastic film (with surface wrinkled).
3. MR filter is a Fairchild CCD-TV minus-red filter.
4. ND indicates neutral-density filter value
5. f equiv. indicates the equivalent f-value of the objective optics required to suppress blooming in the column direction.

TABLE 3-3

COSMICAR AUTO-IRIS "ES" SERIES LENSES

Specification	B1214AES	B2514CES	B5018AES
		Model No.	
Focal Length	12.5mm	25mm	50mm
Maximum Aperture	1 : 1.4	1 : 1.4	1 : 1.8
Iris Range	1.4 - 360	1.4 - 360	1.8 - 360
Illumination Ratio	66,000X	66,000X	40,000X
Image Size	2/3" & 1"	2/3" & 1"	2/3" & 1"
Shortest Focus Distance	0.3m	0.6m	1.0m
Flange Back		17.526mm	
Focal Adjustment	Straight Helicoid: Rotating Angle 210° Torque 450±200g.cm.		
Mount		C Mount	
Filter Size		Ø = 49.0mm	
Overall Dimensions		66 x 51mm	
Weight	380g	350g	370g

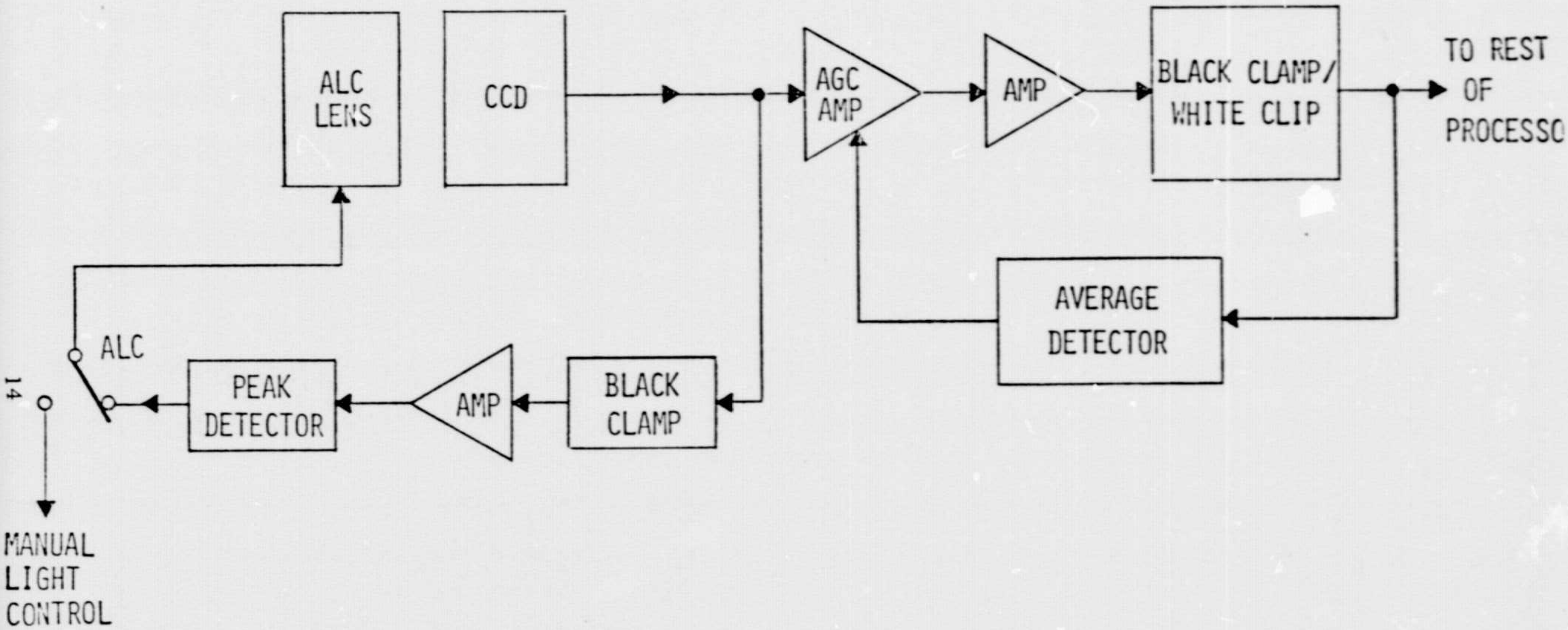


FIGURE 4

VIDEO PROCESSOR - AUTOMATIC LIGHT CONTROL/AUTOMATIC GAIN CONTROL BLOCK DIAGRAM

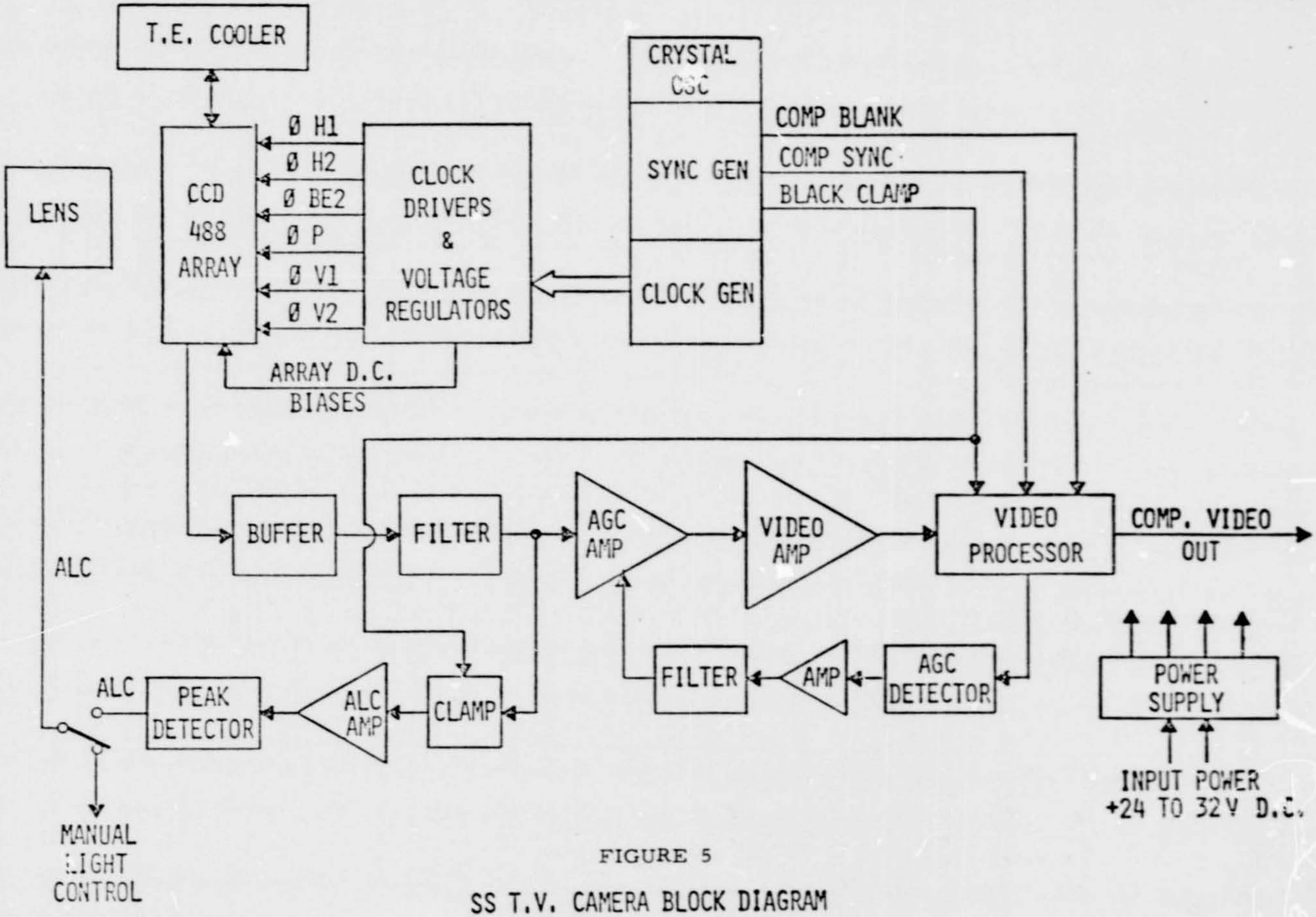


FIGURE 5

SS T.V. CAMERA BLOCK DIAGRAM

The first card contains all TV sync, drive, and blanking signals in accordance with EIA-RS-170. A National MM4320 LSI-TV sync chip, combined with a crystal oscillator and output buffer stages, is used to generate these TV timing signals. Additional counters, gates, flip-flops and buffers are used to generate the timing logic signals for the CCD array.

The second board contains the array logic driver stages, voltage regulators and setup pots for the array. FSDS hybrid drivers are used to drive the capacitive load of the array.

The third circuit board contains all of the video circuits, which consists of: an input buffer; a Nyquist filter; a variable gain AGC stage; a fixed-gain video amplifier and video processor stages, which perform black-level clamping, pedestal adjustment, blanking insertion and sync insertion. In addition, there is an AGC detector, filter and amplifier stage, and the ALC circuits to control the auto-iris lens. There is provision for operating with either manual light control or with ALC.

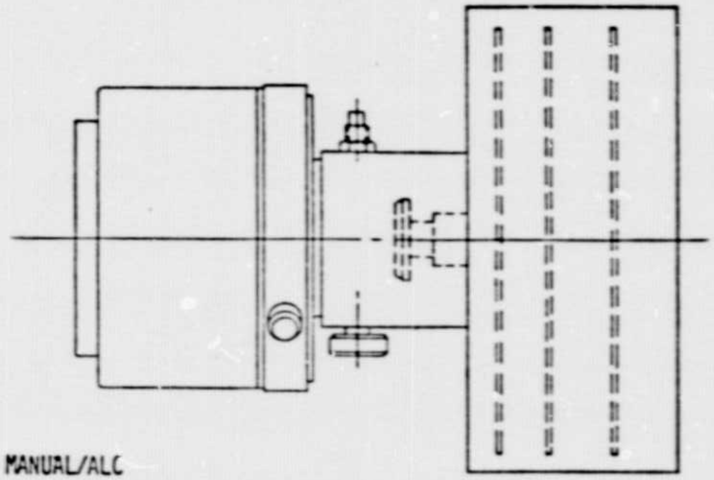
Figure 6 illustrates a packaging concept for the deliverable camera. The CCD and a thermoelectric cooler are contained in a separate short housing affixed to the front face of a main rectangular housing containing the three circuit boards. All controls and connectors are mounted on the sides of the CCD housing, making use of the space available between the lens flange and the CCD focal plane.

A summary of preliminary specifications for the deliverable camera is given in Table 3-4.

3.2 DESIGN SPECIFICATIONS

Table 3-5 summarizes the detailed performance specifications applicable to the deliverable solid state camera. These specifications are in conformance with both Exhibit "A" and Exhibit "B" requirements of the contract Statement of Work for all paragraphs 3.2 through 3.2.17, inclusive.

FAIRCHILD CCAID-488 SSTV CAMERA
(PRELIMINARY NASA/JSC DESIGN)



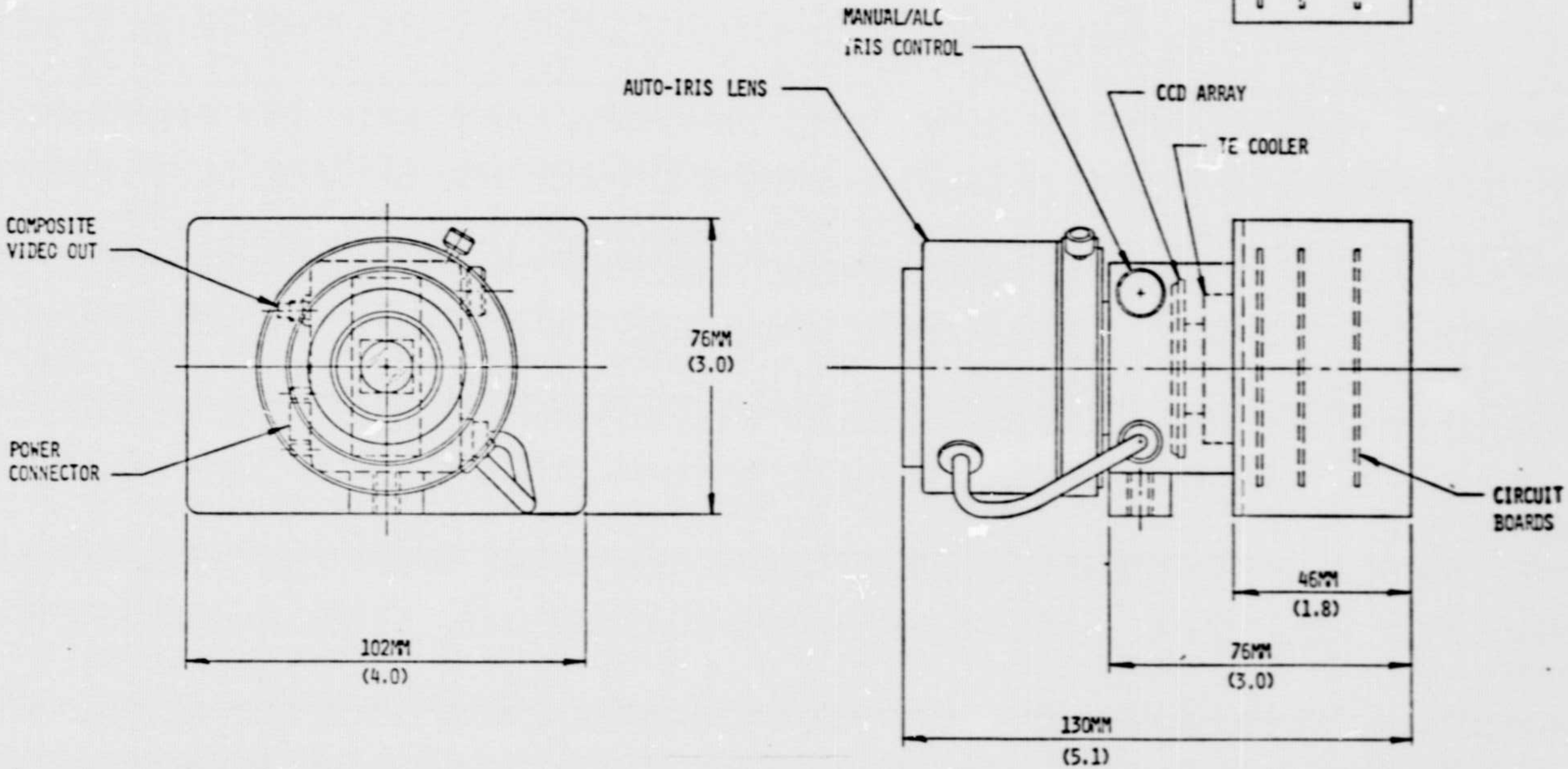


FIGURE 6

TABLE 3-4

PRELIMINARY SPECIFICATIONS

CCAID-488 SSTV CAMERA - (NASA/SSC PROTOTYPE)

Sensor	Fairchild CCD 488 x 380 array
Spectral Response	0.45 to 1.1 Micrometer
Optics	Auto-Iris f1.4-f360, "C" Mount
Sensitivity (Note 1)	Sensor Illuminance 2×10^{-4} fc
Electronic AGC	100:1 Range
Geometric Linearity	No Camera Distortion. System Performance limited by lens and display.
Frame Rate	30 Frames/sec.
Line Rate	15,750 Lines/sec. (nominal)
Format	488 lines: 380 picture elements/line
Sync	2:1 standard interlace
Video Output	1V p-p, composite video (RS 170)
Video Line Output	500 ft., 75 ohm
Power (uncooled)	6 watts (Note 2)
Camera Size (excluding lens)	$<$420 cc (see drawing)
Weight (excluding lens)	$<$0.5 kg
Ambient Temperature	0° to 50° C

NOTES:

1. Highlight illumination with 2854°K source (tungsten) for a S/N ratio of 1 (peak signal to temporal RMS noise ratio).

2. The camera will operate with ±12 VDC and +5 VDC. A dc to dc converter will be supplied for operation from an unregulated +28 VDC supply.

TABLE 3-5

DETAILED CAMERA PERFORMANCE SPECIFICATIONS

		Ref. Exhibit "A" SOW Paragraph No.
RESOLUTION, TVL/PH		
Overlap interlace mode	285x325 (HXV)	3.2.1, 3.2.9
High resolution mode	285x485 (HXV)	
FIELD/FRAME INTERLACE RATIO	2 to 1	3.2.2
FORMAT ASPECT RATIO, HXV	4 x 3	3.2.3
VERTICAL SCAN		3.2.4
Frame rate	60/sec	
Field rate	30/sec	
Line periods/frame	525	
GRAY SCALE STEPS ($\sqrt{2}$)	10	3.2.5.1
DYNAMIC LIGHT RANGE (with ALC)	500/1 min.	3.2.5.2
OPERATING VOLTAGE	+28V $\pm$ 4VDC	3.2.6
POWER (uncooled)	6W, max	3.2.7
OUTPUT VIDEO FORMAT		3.2.8
Load Impedance	75Ω $\pm$ 5%	3.2.8.1
Composite video polarity	Black negative	3.2.8.2.1
Signal levels, IRE units		3.2.8.2.2
reference white	+100	
blanking level	0	
sync	-40	
peak-to-peak	140	
Composite output video voltage	1V p-p (nom.)	3.2.10
Blanked picture signal, with setup	0.714 $\pm$ 0.1V	3.2.10.1
Sync signal (from OVDC, ref.)	0.286 $\mp$ 0.05V	3.2.10.2
Setup, blanking level to reference black level, (IRE units)	7.5 $\pm$ 5	3.2.11

TABLE 3-5 (Cont.)

		Ref. Exhibit "A" SOW Paragraph No.
SIGNAL-TO-NOISE RATIO	35db (min)	3.2.11
CEOMETRIC DISTORTION (exc. lens)	<2%	3.2.12
SPOTS AND BLEMISHES	(See below)	3.2.13
BLOOMING	ALC/AGC inhibited	3.2.14
CAMERA OPTICS	Cosmicar Model B2514CES 25mm, f1.4-f360	3.2.15
CAMERA CONTROLS	Power ON/OFF Light Control AUTO/MANUAL Vertical Scan OVERLAP/NORMAL	3.2.16
CAMERA INTERFACES Connectors	Output Video Camera Power Lens Control	3.2.17
SPOTS AND BLEMISHES		3.2.13

A spot or blemish shall be defined as a video signal transition equal to or greater than 7% of the CCD sensor saturation signal observed with the sensor uniformly illuminated at a level corresponding to 50% saturation. The size of a spot or blemish shall be determined by counting the number of scan lines on which the transition occurs; i.e., the number of lines per frame on which the transition is greater than 7% of saturation signal. The total number of white and dark spots shall be less than or equal to:

10 spots over 1 but less than or equal to 4 TV lines/frame
2 spots over 4 but less than or equal to 8 TV lines/frame
0 spots over 8 TV lines/frame

No horizontal or vertical black lines resulting from a failed CCD element shall be allowed. Shading signal variations along any line averaged over sections of 10% of picture width shall not exceed 10% of V_{sat} at 50% uniform sensor illumination.

SECTION 4

SUMMARY AND CONCLUSIONS

CCD image sensors of the buried-channel interline-transfer type have features which make these devices particularly useful for solid-state TV cameras where small size, low power/low voltage operation, high sensitivity and extreme ruggedness are either desirable or mandatory characteristics. The solid-state camera design which has evolved as a result of this NASA/JSC program is expected to satisfy the requirements for a deliverable end product which can demonstrate feasibility for application in future space missions.

The camera design utilizes a 380 x 488 element CCD to insure full compatibility with 525 line television transmission and display monitors without requiring the use of pseudo resolution or special formating techniques. Several additional features recommended for inclusion in the deliverable camera address specific aspects of the NASA/JSC requirement:

1. Dual-mode clocking has been included to demonstrate feasibility for operation with full-frame readout intervals of either 1/60 second or 1/30 second.

2. A thermoelectric cooling feature for the CCD is recommended to minimize thermally-generated dark current defects, and to reduce the average dark-signal level, thereby effecting an increase in useful sensitivity and dynamic range.

3. Wide-range automatic light control, supplemented by a video AGC technique, has been included to minimize or eliminate CCD overload effects caused by intense point sources in the field-of-view.