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UNIVERSITY OF UTAH (WALLOPS) PRECISION METEOROLOGICAL DATA DIGITIZER

Robert M. Garn

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Revised and edited by
K. W. Atwood

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NASA Wallops Station
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THE UNIVERSITY OF UTAH METEOROLOGICAL DATA DIGITIZING SYSTEM

I. Introduction

Data from conventional meteorological rocketsondes and radiosondes is transmitted in the form of a train of radio-frequency pulses. The time period between pulses represents the quantity which is being transmitted. The resulting pulse repetition rate varies in the range of 20 pulses/second to 200 pulses/second. Electronic circuits in the AN/GMD or other receiving system converts the slowly varying audio frequency into a varying voltage level. This voltage level is used to control the position of a pen and pointer on an AN/TMQ-5 or similar type of paper strip recorder. At all points in the conventional system, the information is in analog form, such as a frequency, a voltage level, or a pen position.

The University of Utah Meteorological Data Digitizing System takes the pulsed signals in the AN/GMD receiver and converts the information (the time interval between pulses) into a digital form. This digital information is recorded on a magnetic tape. The information on the magnetic tape then is fed into a digital computer which processes the information.

The digitizing system records the digital data on a seven-track computer tape in 6-bit bytes plus parity. The data is recorded on the tape in 1,542-byte records. The first 6 bytes of each record contains the time of year in days, hours, minutes, seconds, and milliseconds. The following 1,536 bytes in the record contains the digitized data from

the AN/GMD. The digitizing system counts the number of microseconds in the period between two successive data pulses from the AN/GMD. Each period is counted by a binary counter and presented as an 18-bit word. Each of these words is broken up into three 6-bit bytes for the tape recorder. Thus, the 1,536 bytes of data in the record represent 512 data words. A single rocket flight may result in several hundred 1,542-byte records.

A computer using 36-bit words reads the tape in records of 257 words. The first word (6 bytes of 6 bits each) is interpreted appropriately as time of year. The remaining words must be "split" into two data words each for processing by the computer.

II. The Basic Digitizer Configuration

A general block diagram of the digitizer is given in Fig. 1. The *master sequencer* in this diagram is the control unit for the digitizer. When the digitizer is turned ON and a GO switch on the digitizer is activated, the *master sequencer* allows data from the *range time* unit to be stored in the *multiplexer*. These stored *range time data* are then fed into the tape recorder. Since the tape recorder writes one 6-bit byte each step of the tape transport, the 36-bit range time word is recorded in six tape transport steps. The tape recorder requires about eight milliseconds to record this range time word.

While the range time is being recorded, the *master sequencer* begins counting cycles from a 1 MHz clock and summing this count in the *data counter* or *accumulator*. These data in the *accumulator* represent

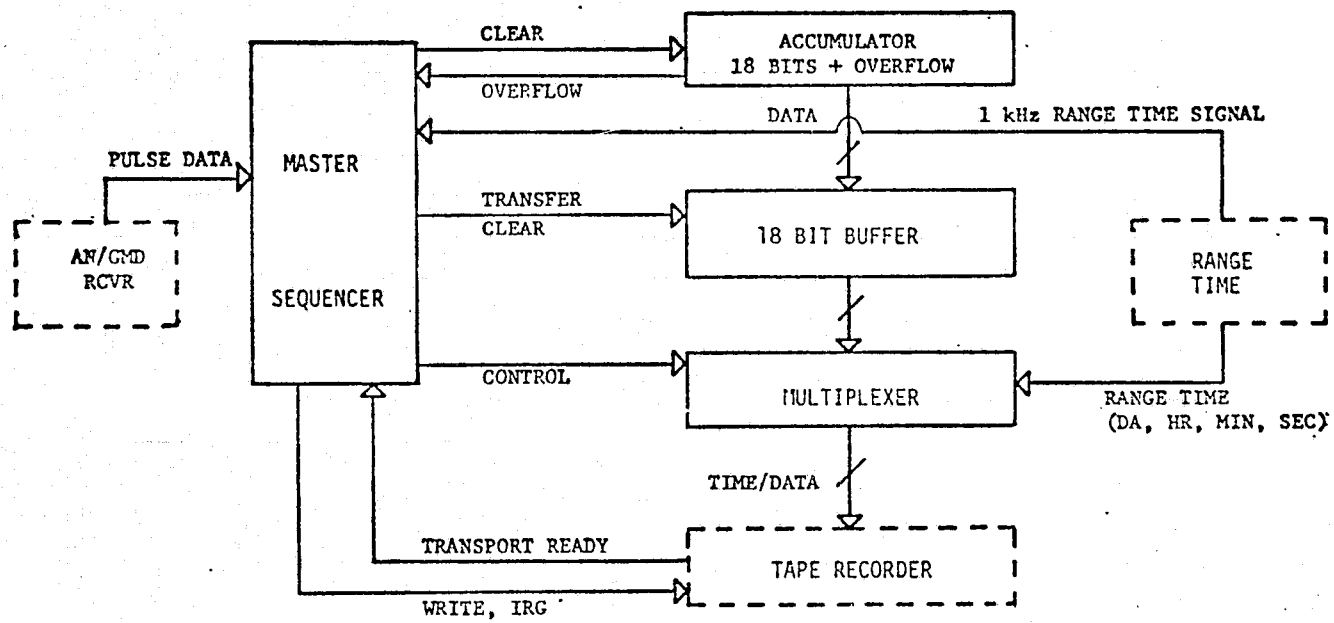


Fig. 1. General block diagram of the digitizer.

the elapsed time from the previous data pulse from the AN/GMD in microseconds. (Of course, the one megahertz clock produces one pulse per microsecond.) When the next data pulse arrives from the AN/GMD, the *master sequencer* checks to see if the *range time* word has been written on the tape. Usually, this second data pulse occurs before the *range time* word has been written. When this situation occurs, the *master sequencer* continues to sum the count from the 1 MHz clock in the *accumulator*. The *accumulator* is a 19-bit register with the 19th bit serving as an "overflow" indicator. In the absence of a second data pulse, the *accumulator* will count up to 2^{18} microseconds or 262.144 milliseconds. Then an overflow occurs into the 19th bit of the *accumulator*. This overflow produces a signal to activate the *master sequencer* the same as an additional data pulse. After the *range time* has been written on the tape, the next data pulse or *accumulator overflow* activates the *master sequencer* which gates the contents of the *accumulator* into the "*buffer*" and clears the *accumulator*. This transfer of data to the *buffer* and clearing of the *accumulator* occurs within a one microsecond clock period. Immediately, the *accumulator* starts counting the microseconds until the next data pulse or *accumulator overflow*. In the meantime, the *master sequencer* passes the 18-bit data word from the *buffer* through the *multiplexer* to the tape recorder in three 6-bit bytes. The digitizer is activated by the leading edge of the data pulse. Consequently, the data word is the number of microseconds between the leading edges of the data pulses.

Successive data words are written as each data pulse is sensed by the *master sequencer*. After 512 data words are recorded, the *master*

sequencer calls for an *interrecord gap* (IRG). A typical data tape would appear as shown in Fig. 2.

The *master sequencer* ignores data pulses which occur while the tape transport is advancing for an IRG or while the tape recorder is writing on the tape. Consequently, the first data word of every record is large and corresponds to the total time accumulated over the preceding IRG and writing of the *range time* word.

The maximum tape recorder speed is 750 steps/s. Since three steps are required for each data word, the maximum data frequency is limited to 250 Hz. The 18-bit *accumulator* capacity limits data words to a maximum of about 0.26 seconds. Nevertheless, there is no lower limit to recorder data frequency because data words longer than 0.26 seconds will cause an *accumulator overflow.* The *accumulator overflow* words are recorded as zeros, and are subsequently recognized by the computer as 0.262144 seconds and are summed with neighboring data zeros (if any exist) to the next nonzero data word. Thus periods much longer than 0.26 seconds can be measured by the system.

In sufficiently dense data, the occurrence of occasional lost pulses (dropout), or even successive sets of two, three, etc., lost pulses, are recognizable in the computer by their appearance as submultiples of the data frequency.

After the recorder has stored a record of 512 data words, the *sequencer* executes the IRG, and the entire sequence is repeated beginning with the *range time* word as the first word of the next record.

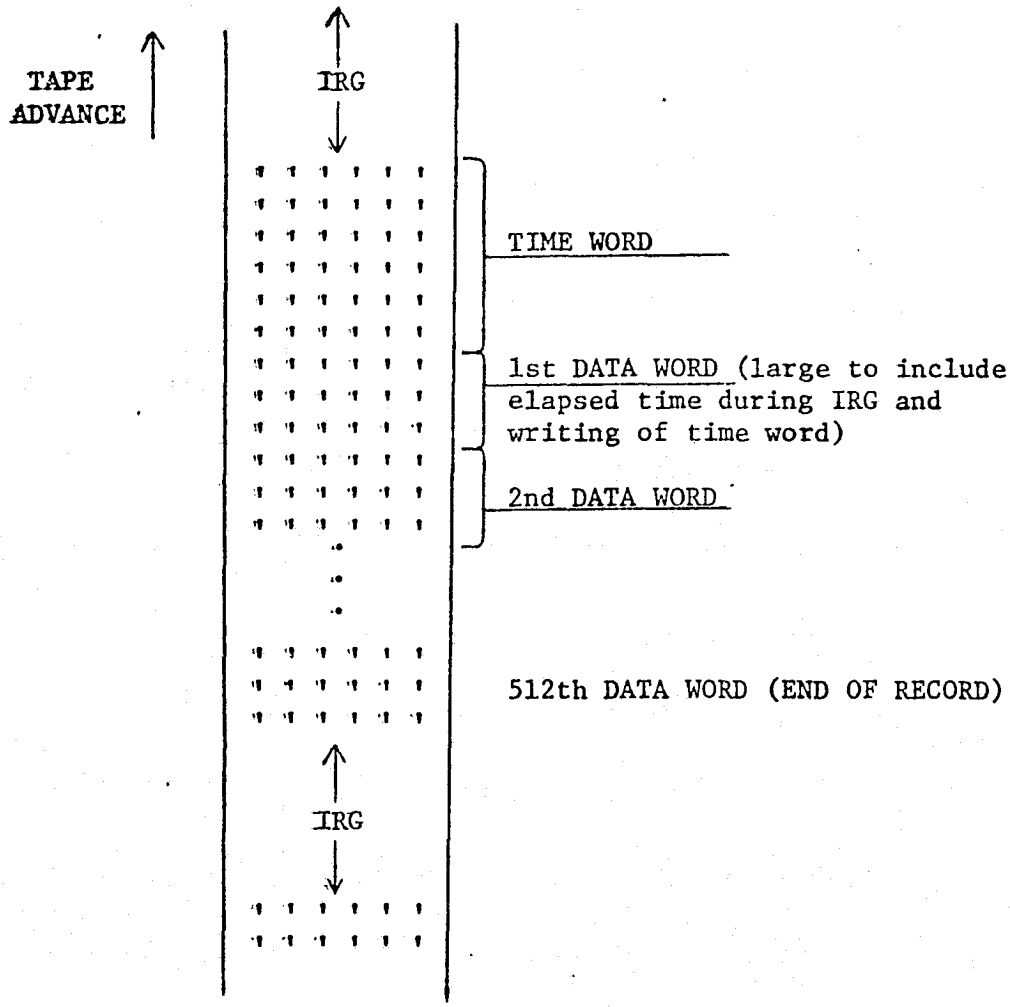


Fig. 2. Longitudinal order of data written on tape. For lateral order of bits, parity, and further details of writing and format, see Operating and Service Manual, Incremented Write Tape Transport Model No. 1507, Serial No. 305300, Peripheral Equipment Corporation, 9600 Irondale Avenue, Chatsworth, California 91311; phone (213) 882-0030.

III. Details of the Digitizer Operation

A Functional Block Diagram of the digitizer is given in Fig. 3. This diagram, which is much more detailed than that given in Fig. 1, will be useful as the detailed operation of the digitizer is considered. However, note that some of the OR gates in Fig. 3 are intended to represent a *function* and may *not* correspond to a single given hardware component. While the different components are interconnected and the operation of one unit is not independent of the operation of other units, we will try to consider each block of Fig. 1 separately for ease of understanding.

A. The Master Sequencer

The *master sequencer* is the basic control unit of the digitizer. This *master sequencer* is a state type of counter with eight different states. The digitizer proceeds through these eight steps to complete its task of operation. The eight states of this counter are denoted as shown in Table 1. The state diagram of this *master sequencer* is given in Fig. 4.

Table 1. State designation of the master sequencer.

Decade Notation	Binary Notation
P_0	0 0 0
P_1	0 0 1
P_2	0 1 0
P_3	0 1 1
P_4	1 0 0
P_5	1 0 1
P_6	1 1 0
P_7	1 1 1

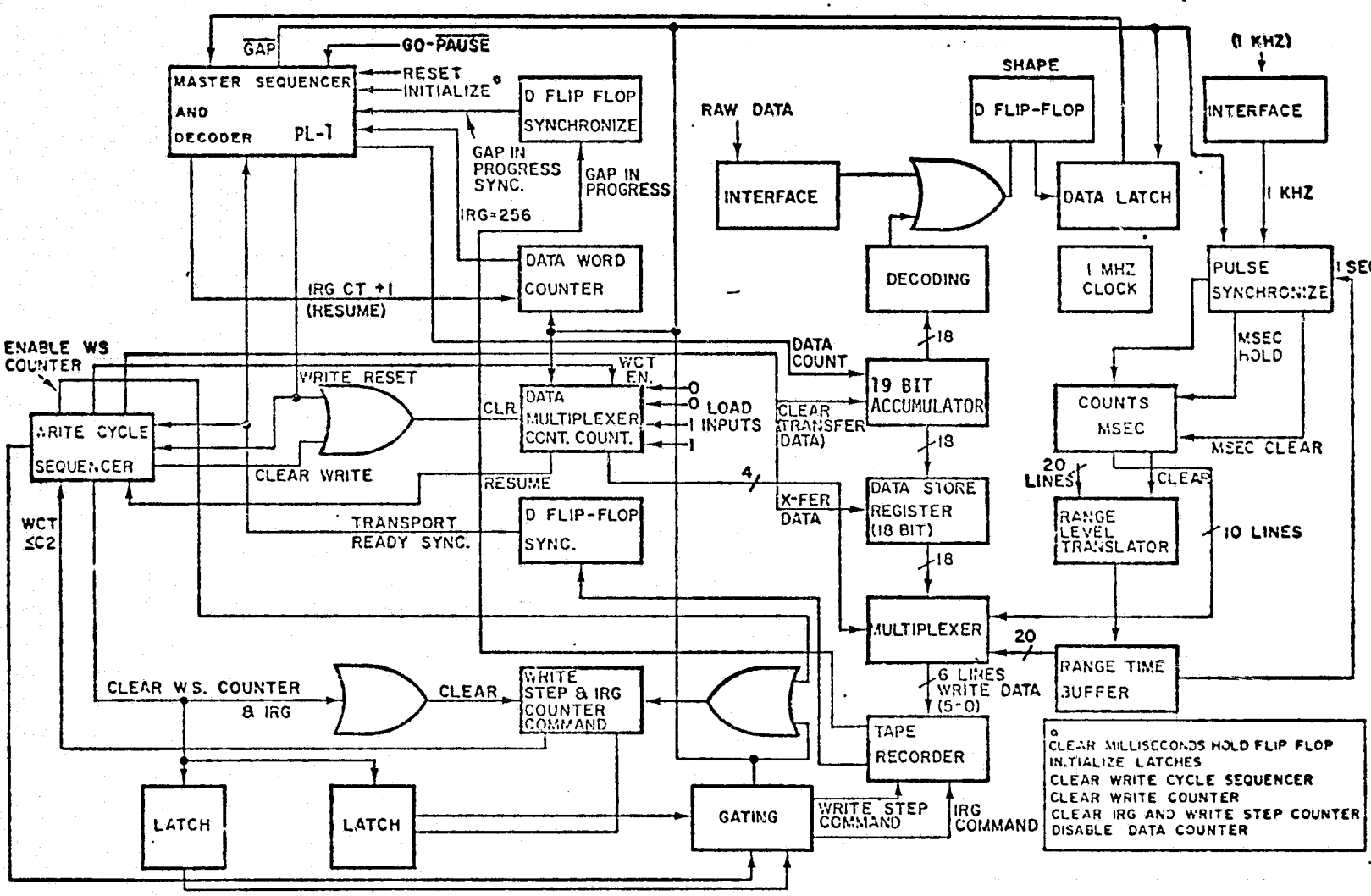


Fig. 3. A functional block diagram of the entire digitizer.

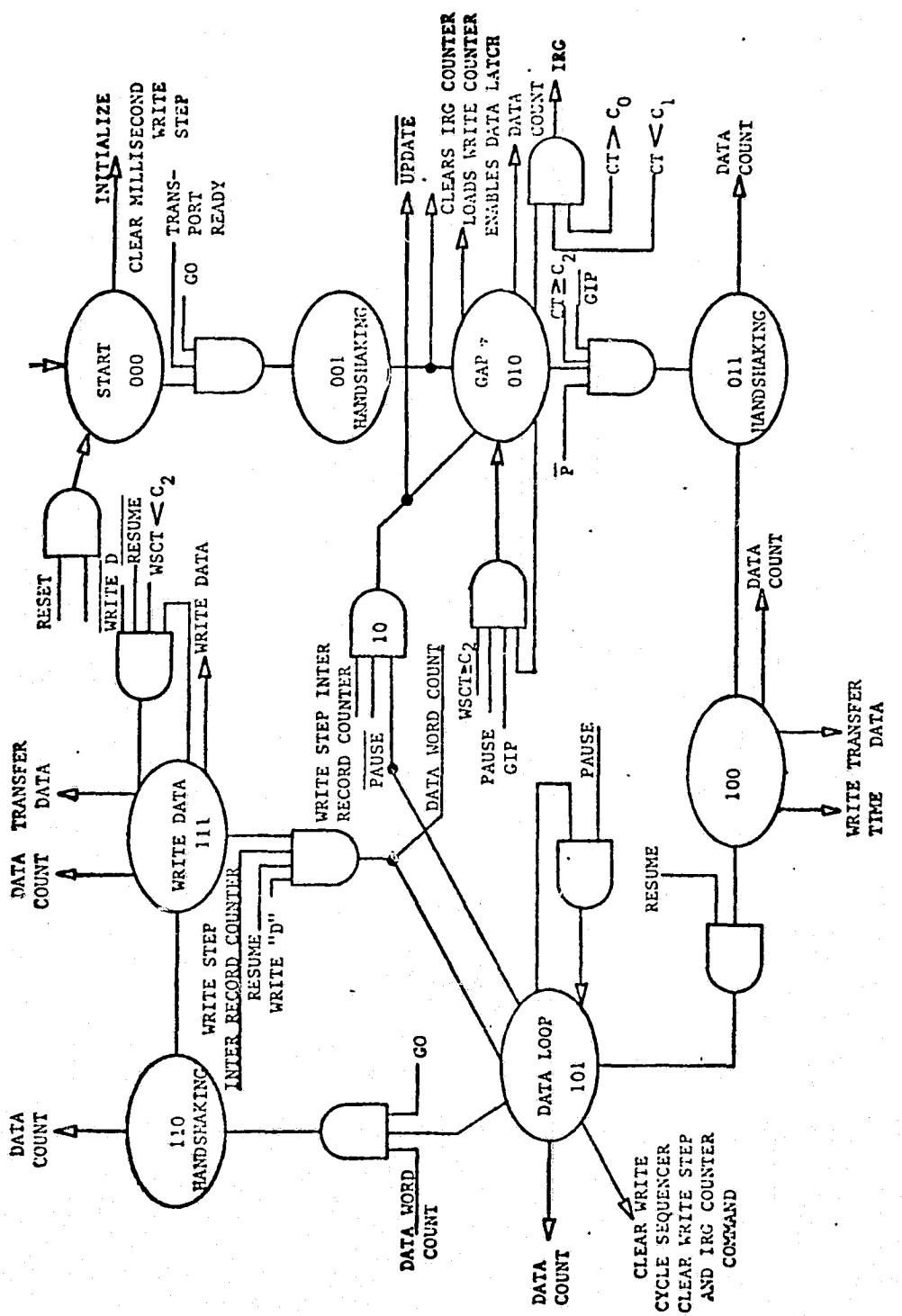


Fig. 4. Master sequencer state diagram.

When the power switch is turned ON, the *master sequencer* is reset to the 0 0 0 or P_0 state. The sequencer remains in this "start" state until the GO switch on the front panel is activated. When the GO switch is activated and the tape transport is enabled, the *master sequencer* switches to the 0 0 1 or P_1 state. The P_1 state is an *idle* state and transfers the *master sequencer* to the 0 1 0 or P_2 state. The P_2 state is the *gap* state. In this state, several things happen simultaneously:

1. *Range time* is transferred into the *range time buffer*.
2. A signal is sent to the tape recorder to start the tape transport and produce an *interrecord gap* (IRG).
3. The IRG counter is reset to zero.
4. The *accumulator* starts to count one microsecond intervals.

The *master sequencer* is held in state P_2 until the IRG is completed. When the IRG is complete, the *master sequencer* shifts to the 0 1 1 or P_3 state. The P_3 state is an *idle* state (sometimes referred to as a *handshaking state* since it is merely an intermediate state between states P_2 and P_4). The *accumulator* continues the data count while the *master sequencer* is in state P_3 as well as all subsequent states.

The *master sequencer* shifts from state P_3 to state 1 0 0 or P_4. In the P_4 state, the *range time* (which was shifted into the *range time buffer* in state P_2) is written on the tape in six 6-bit bytes. This writing sequence requires a *subsequencer* which will be discussed in more detail under the heading of *Write Cycle Counter*. When the *range time* has been written on the tape, a *resume* signal is generated and the *master sequencer* shifts from state P_4 to state 1 0 1 or P_5.

State P_5 is the first state of the *write-data* loop of the *master sequencer*. The *master sequencer* remains in this state until the *writing subsequencer* is reset. When the next data pulse (or *accumulator overflow*) occurs, the data in the *accumulator* are transferred to the *data store register* and the *master sequencer* shifts to state 1 1 0 or P_6. State P_6 is an *idle state* and shifts to state 1 1 1 or P_7. State P_7 is the *write-data* state and the data in the *data store register* are transferred to the tape recorder. In addition, the *interrecord counter* is advanced one count to indicate one data word has been recorded. When the *write-data* sequence in the *subsequencer* is complete, the *master sequencer* shifts back to state P_5 and prepares for the next data word. The *master sequencer* remains in the P_5, P_6, and P_7 loop until 512 data words have been recorded.

When the *interrecord counter* has reached 512, the *master sequencer* shifts from state P_7 (upon completion of the write cycle) back to state P_2. A new *interrecord gap* is produced and the IRG counter is reset. The *master sequencer* then continues on through the sequence again.

Notice that the *master sequencer* enters the P_0 and, consequently, the P_1 state only when the power is first turned ON. There is no other command to enter these first two states. The *master sequencer* only enters the P_2 state when an IRG is required. The *master sequencer* actually spends most of its time in the P_5, P_6, and P_7 loop writing data on the tape.

The actual hardware arrangement is shown in plate 1 and plate 5. The integrated circuit (IC) No. 6 is the actual *master sequencer counter*.

Then, IC No. 7 is used to decode the binary output of IC No. 6. A voltage signal appears on a specific terminal of IC No. 7 for a specific state of IC No. 6. Table 2 indicates the relationship between the counter (IC No. 6) and the decoder (IC No. 7).

Table 2. Decoder signal output.

State	State of IC No. 6	Terminal of IC No. 7 Where Signal Appears
P_0	0 0 0 0	1
P_1	0 0 0 1	2
P_2	0 0 1 0	3
P_3	0 0 1 1	4
P_4	0 1 0 0	5
P_5	0 1 0 1	6
P_6	0 1 1 0	7
P_7	0 1 1 1	9

Integrated circuits No. 9 through No. 14 are used to shift the counter to the proper state and also to act as gating to the other sections. This gating action enables the hardware to carry out the operations of that particular state.

B. Write-Cycle Counter

The actual write cycle is initiated by the *master sequencer* but is controlled by a *subsequencer* or *write-cycle counter*. This *write counter* is composed of two J-K flip-flops (I.C. No. 25 on plate 2) and has four states which can be written 0 0, 0 1, 1 1, and 1 0 in binary notation. These states are denoted A, B, C, and D, respectively. The state diagram of this counter is given in Fig. 5.

Initially the counter is set to the 0 0 or A state, which is an *idle* state. The counter remains in this *idle* state until a *write-data* pulse or a *write-time* pulse occurs. Then, the counter shifts to the 0 1 or B state. In the transition from the A to the B state, data are transferred to the *data store register* and the *data counter* is reset to zero. Simultaneously, the *write step counter* and the *interrecord gap counter* are reset. In state B, the *data multiplexer control counter* is initialized. The counter remains in state B until a *transport ready* signal is received from the tape deck. This signal indicates the tape recorder has finished writing and is ready for the next data byte. When the *transport ready* signal is received, the counter shifts to the 1 1 or C state. The C state is a *handshaking state* and the counter continues to the 1 0 or D state. The D state is the *write state D* (WS"D") where the tape deck is given the command to write.

From state D, the counter may return to either state A or state B. If the *subsequencer* is writing a *range time word*, the counter must go through the B-C-D loop six times before it shifts back to the A state.

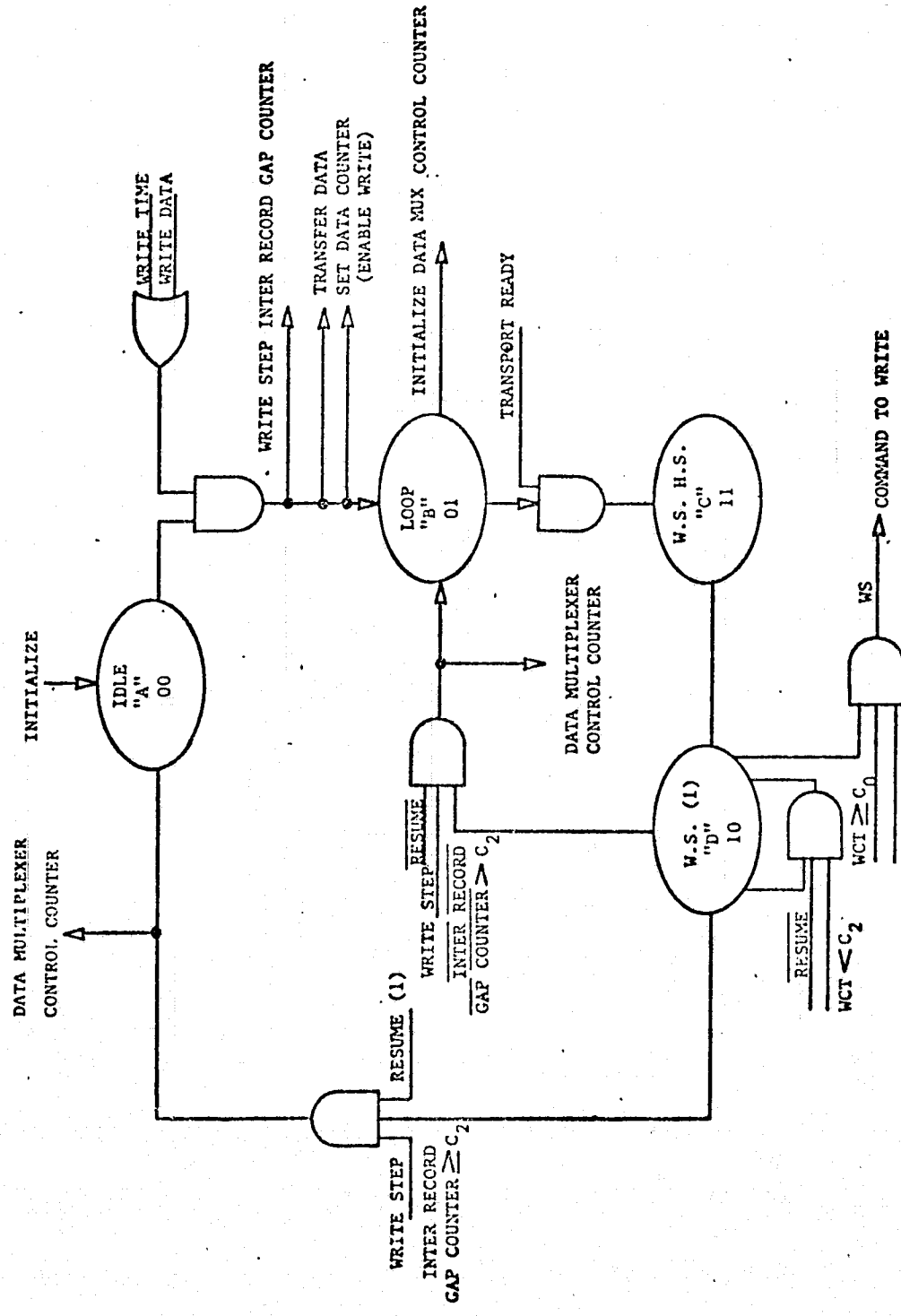


Fig. 5. Write cycle state diagram.

However, if the *subsequencer* is writing a *data word*, the counter will only go through the B-C-D loop three times before it shifts back to the *idle* or A state. In order to shift back to state A, the *inter-record gap counter* must be greater than or equal to C2 and the *resume* signal must be present.

The *write-cycle counter* is activated by the *master sequencer* in state P_4 to write a *range time word* and in state P_7 to write a *data* word. After completing a *write* command, the counter returns to the *idle* A state to await a new *write* command.

The actual *write-cycle counter* is contained on IC No. 25, which is a dual J-K flip-flop. The *write* command is generated in IC No. 7 (the decoded output of the *master sequencer*) terminal 5 (state P_4 output) or terminal 9 (state P_7 output). This *write* command proceeds through an OR gate (9C) on IC No. 9 (plate 1) to a NAND gate (26C) on IC No. 26 (plate 2). If the *write-step counter* is in state A, both Q outputs on the *write-cycle counter* are zero and the *write* command proceeds through an OR gate (31C) on IC No. 31 to J-K inputs of the "A" flip-flop in the *write-cycle counter*. On the next clock pulse, this counter shifts from state A (0 0) to state B (0 1). In state B, the outputs $\bar{Q}_A$ (terminal 13 of IC 25) = 1 and Q_B (terminal 9 of IC 25) = 1, so the AND gate (30A) on IC 30 has two high inputs and produces a signal on the *write B* line. The *write B* signal clears the *write step* and IR counter (through OR gate 22C) of plate 1 and sets the *latches* (IC Nos. 3, 4, and 5) in preparation for the *write "D"* command.

With Q_B high and $\bar{Q}_A$ high, a signal is transmitted through the NAND gate (26B) on IC No. 26 and through the OR gate (28A) on IC No. 28 to

produce a "high" on the J-K inputs of the "B" flip-flop. On the next clock pulse, the "B" flip-flop changes state and the counter shifts to the C state (1 1). We now have Q_A and Q_B both high. The "A" flip-flop is activated through the NAND gate (28B) on IC No. 28 and the OR gate (31C) on IC No. 31 to produce a "high" signal on the J-K inputs of the "A" flip-flop. When the next clock pulse appears, flip-flop "A" changes state and the counter is now in the D state (1 0). Notice that state 1 1 only existed to transfer the counter from state B to state D and is simply a *handshaking* state.

When the counter is in state D, the *write "D"* line is activated through gate 30B on IC No. 30 and inverter 29D. This *write "D"* line is connected to terminal 2 of a three-input AND gate (22A) on IC No. 22 (plate 1). One of the other inputs to this AND gate comes from the C_0 latch which passes the digitized data 8 microseconds after initiation in order to insure stability of the information. The third input to the AND gate comes from the C_1 latch. This C_1 latch has a delay of 64 microseconds, which allows the tape recorder to settle down before writing the information on tape. When all three of these inputs are at a logical one level, the *write step* command is initiated.

The *write D* command is also applied to gate 20A of IC No. 20 (plate 1) terminal 2. The output of this OR gate is connected to terminals 7 and 10 of IC Nos. 3, 4, and 5, which enables these three counters of the *write step* and *interrecord counter* to begin their evaluation of the incoming data.

C. The Hold Function for the Master Sequencer

A *hold* command is generated to hold the *master sequencer* in some specific states until certain conditions are met. In plate 1, the *hold* signal is applied to terminal No. 7 on the *master sequencer counter* on IC No. 6. This *hold* signal is generated by the NAND gate (9D) on IC No. 9 which is also shown on plate 1. Three states can produce the *hold* function. These are states P_0 (the *idle* state), P_2 (the *gap* state), and P_5 (the *data loop* state). The OR gate (10A) of IC No. 10 feeds these signals into the NAND gate (9D) on IC No. 9. In state P_0, the GO switch allows the counter to proceed. In state P_2, the GIP (gap-in-process) signal does not release the *master sequencer* from the *hold* condition until the gapping between records is complete. In state P_5, the IRGCT > RS signal becomes important. This signal originates in the data word counter (plate 2) IC No. 37 terminal 13. The IRGCT > RS signal indicates when the 256 data words have been recorded and resets the *master sequencer* to state P_2 through the NAND gate (13B) on IC No. 13, the OR gate (24D) on IC No. 24, and the inverter (23B) on IC No. 23. This signal also clears the *write step* and *interrecord* counter.

D. The Multiplexer Control Counter

The *data multiplexer control counter* allows the proper data bits to be transferred to the tape recorder. The state diagram of this *data multiplexer control counter* is given in Fig. 6. The corresponding truth table for this multiplexer is given in Table 3. The multiplexer output signals are denoted as MA, MB, MC, and MD. Table 3 indicates

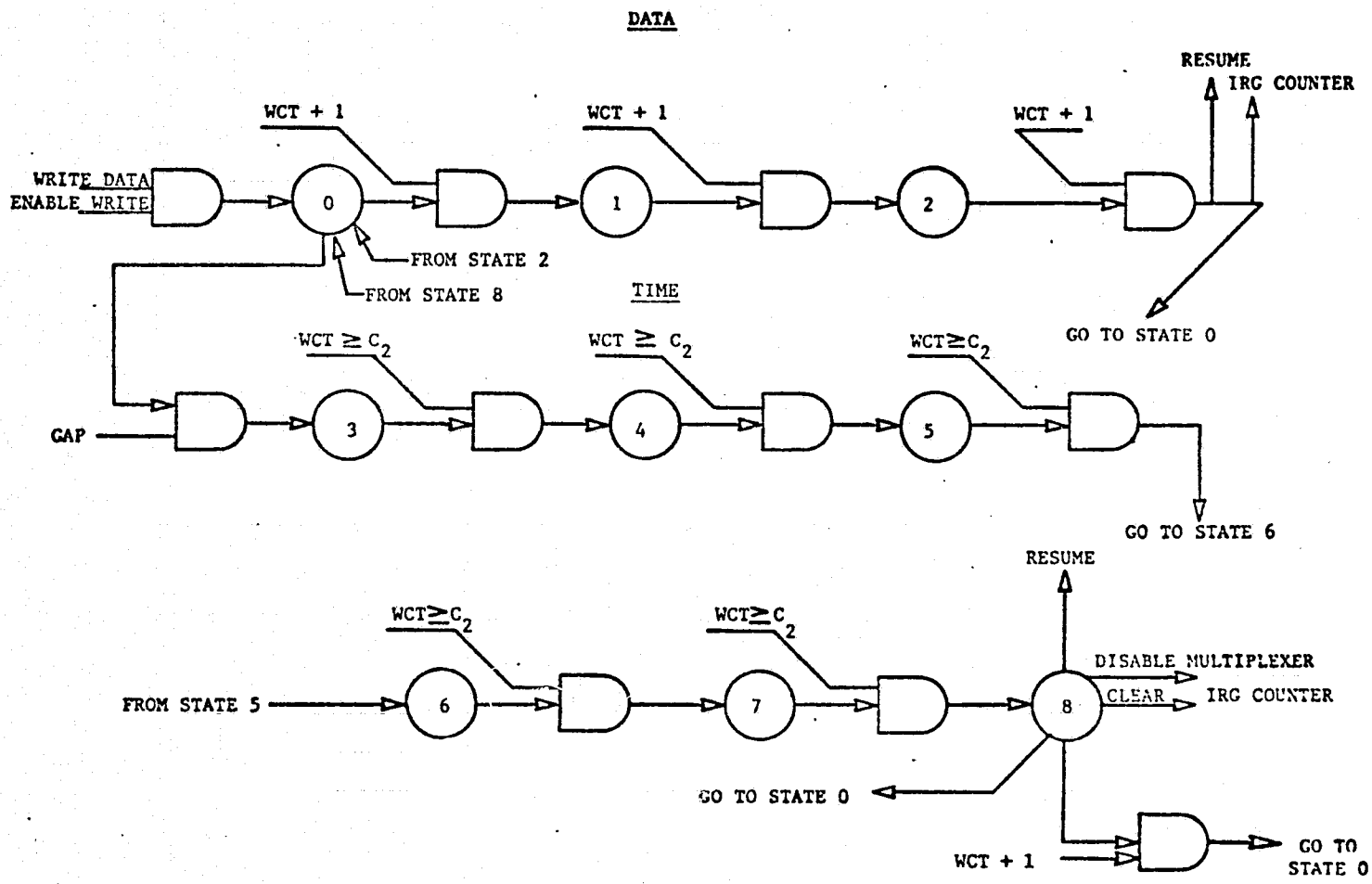


Fig. 6. Write counter.

Table 3. The truth table for the multiplexer control counter.

State	MD	MC	MB	MA	P_5	P_4	P_3	P_2	P_1	P_0
0	0	0	0	0	D17	D16	D15	D14	D13	D12
1	0	0	0	1	D11	D10	D9	D8	D7	D6
2	0	0	1	0	D5	D4	D3	D2	D1	D0
3	0	0	1	1	T19	T18	T17	T16	T15	T14
4	0	1	0	0	T13	T12	T11	T10	T9	T8
5	0	1	0	1	T7	T6	T5	T4	T3	T2
6	0	1	1	0	T1	T0	M9	M8	M7	M6
7	0	1	1	1	M5	M4	M3	M2	M1	M0
8	1	0	0	0	0	0	0	0	0	0

the corresponding terms which will be written on the tape. The bits of a *data word* are denoted as D0, D1, etc., up to D17. The first set of six data bits are recorded when the multiplexer is in state 0. The next six data bits are recorded when the multiplexer is in state 1 and the final six data bits are recorded when the multiplexer shifts to state 2. Each time a data word is written, the multiplexer will shift through states 0, 1, and 2.

In order to write a time word, the multiplexer must start in state 3 and proceed through states 4, 5, 6, and 7 to state 8. The range time is connected to the digitizer through twenty *level translators* (IC Nos. 69 through 78 on plate 4). The output signals from these *level translators* are transferred to the *time storage buffers* (IC Nos. 64 through

68 on plate 3) whenever an *update time* signal is received. The data stored in the *time storage buffers* are transferred to the tape recorder as the multiplexer proceeds from state 3 to state 8.

In terms of the actual hardware, the multiplexer control counter is IC No. 38 on plate 2. The signals MA, MB, MC, and MUXEN are connected to the multiplexer chips on plate 3 to activate the proper storage registers also given on plate 3.

When the *master sequencer* reaches state P_2, the decoder (plate 1) issues a GAP command to terminal 9 of IC No. 38 (plate 2). This signal (on terminal 9) sets the counter to state 2. The count proceeds through states 3, 4, 5, 6, and 7 to state 8. In the process, the *time* word is written on the tape.

If a *clear write* command is issued (through gate 24B and inverter 33F) to terminal 1 of IC No. 38, the counter is reset to state 0. Then the count proceeds through states 1 and 2. Then, the output signals from the multiplexer counter are passed back through gates No. 34B, 30D, 39A, and 29B to reset the counter to state 0. This sequence of commands writes one data word on the tape. The command signal from the inverter 29B on IC No. 29 has been named *resume* and is used in the block diagrams and the plates.

Transfer of data is initiated in the *write-cycle sequencer* as a $\overline{\text{DATA TRANSFER}}$ from NAND gate 31A. This $\overline{\text{DATA TRANSFER}}$ signal is produced by a 0 0 output level from the dual J-K flip-flops of IC No. 25 (plate 2) and a high voltage level from the *write* command by either a P_4 or P_7 state in the *master sequencer* (plate 1). A *write reset* signal from the *master sequencer* (plate 1) in state P_5 resets the multiplexer to state 0

so it is ready to write a new *data* word.

E. The Data Counter

The *data counter* is composed of IC Nos. 44, 45, 46, 47, and 48 on plate 2. The transfer data signal from the *write-cycle sequencer* is applied to these IC's through terminal 9. This signal resets these counters so they can begin counting the number of microseconds between data words. The data from these counters are denoted as C0 to C17. The *data count* signal is applied to pins 7 and 10 of the data counters and enables the counters to count. This signal is continually present during and after the *gap* state (or state P_2). This *data count* signal is developed by gate No. 30C of IC No. 30 (plate 1). Gate 30C is an AND gate and only produces an output when both inputs are a logical one. Thus, all states except P_0 and P_1 will produce a *data count* signal.

The outputs of the *data counter* are connected to the 8 input NAND gates of IC Nos. 40 and 42. These signals are then applied to gates Nos. 39C and 28C. When all 18 *data counter* outputs are at a logical 1 level, the counter will have a count of 2^{18}. At this count, a pulse will be sent into the shaped data section of plate 1. If the *master sequencer* is in state P_5, a *data transfer pulse* will be generated. The *data transfer pulse* then clears the *data counter* by a high pulse to terminals 1 of IC Nos. 44, 45, 46, 47, and 48. The register has now "dumped" its data and is ready to accept a new data count.

F. The Pulse Synchronizer

The AN/GMD system has a *range time code generator* which produces

a 1 kHz square wave. Since the digitizer must interact with this *range time code generator* in order to read range time, a means of synchronizing the two clock signals must be provided. The *pulse synchronizer* on plate 1 provides this needed synchronizing action.

The 1 kHz signal from the *range time code generator* is applied to the base of a 2N3904 transistor (plate 1). The output signal from this transistor is passed through a 2-input NAND gate (18B) in IC No. 18, which acts as an inverter to compensate for the inversion produced by the 2N3904 transistor. The 1 kHz signal is then applied to terminal 6 of IC No. 2 (plate 1) which is a 4-bit counter.

The state diagram of the pulse synchronizer is given in Fig. 7. The 1 kHz signal from the *range time code generator* is a pulse signal. When this 1 kHz signal is high, all the lines with a "1" by them will be high. When the 1 kHz signal is low, all the lines with an "0" by them will be high. If the counter is starting in state 0 0 0 and the 1 kHz signal is low, the AND gate keeps *command* in state 0 0 0. When *command* is in state 0 0 0 and the 1 kHz signal is high, *command* is transferred to state 1 0 0. In order for command to be transferred to state 1 0 0, both the pulse from the *range time code generator* and the clock pulse from the digitizer must occur at or very near the same time. Therefore, if the two pulses are in synchronism, a *pulse in synch.* signal will be generated and passed through the OR gate in Fig. 7. This *pulse in synch.* signal is passed through gate Nos. 15A, 8A, and 23D to gate No. 16A to produce a $\overline{\text{CLEAR MS CT}}$ signal.

The action of the counter can be visualized by assuming we are

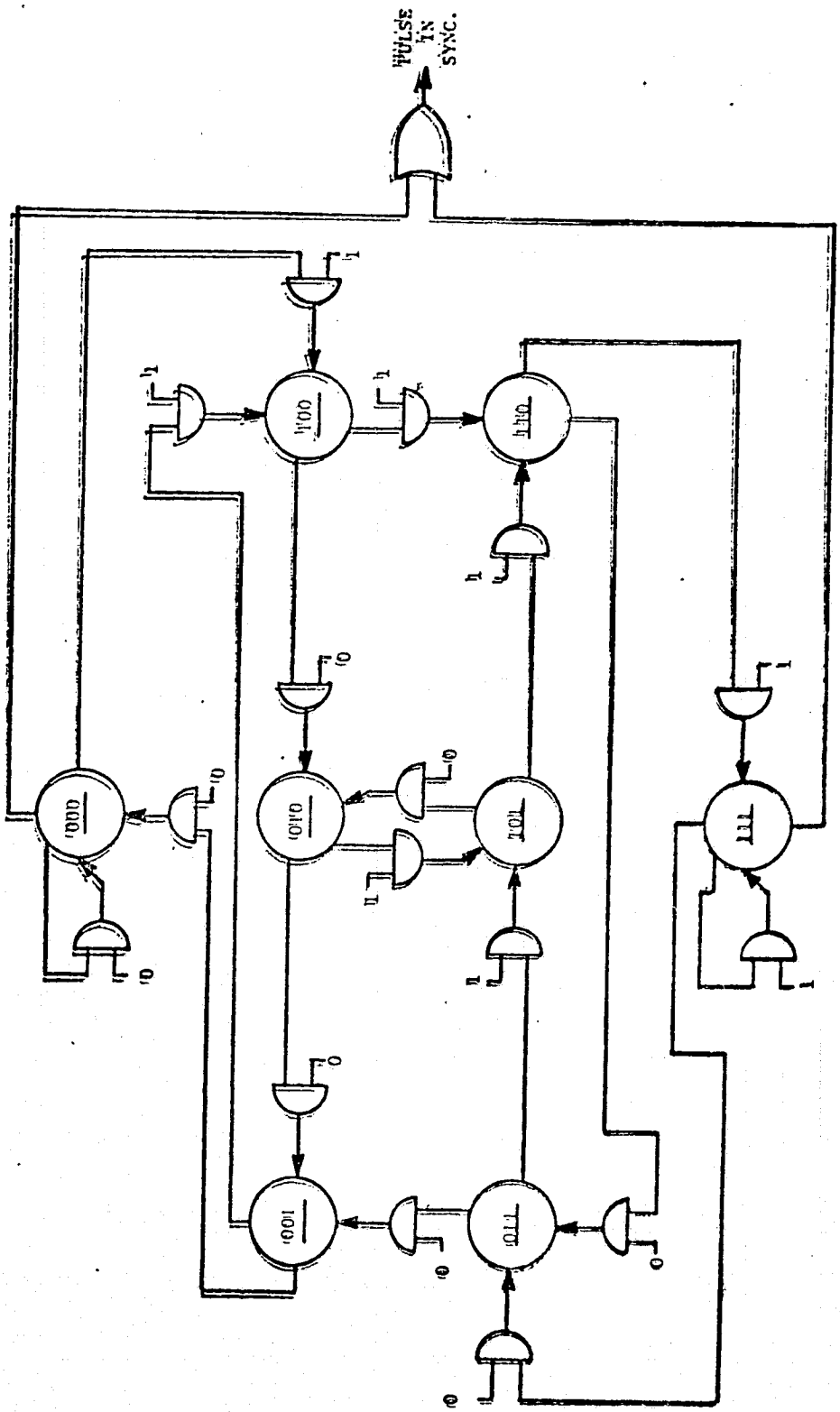


Fig. 7. Pulse synchronizer.

in state 0 0 0 and the local clock pulse and the external 1 kHz pulse occur simultaneously. A *pulse in synch.* signal is generated and the counter shifts to state 1 0 0. On the next pulse, the counter shifts to state 1 1 0. The next pulse shifts the counter to state 1 1 1. The counter then remains in state 1 1 1 and produces a *pulse in synch.* output whenever the pulses occur.

All other states in Fig. 7 are only subordinate states which continually attempt to get the *command* back to state 0 0 0 if the signals are not synchronized and into state 1 1 1 if the signals are synchronized.

IV. Definition of Terms Used

Master Sequencer -- The master sequencer is the section of the digitizer which acts as the "brain" of the system. The master sequencer issues enabling commands to the digitizer that initiates functions to be performed. Figure 4 shows a state diagram of the decoder of the master sequencer.

WCT $\geq$ C2 -- Word counter greater or equal to the count C2. This command finally indicates to the master sequencer that an incoming frequency pulse has been rejected by the write step and interrecord counter because its frequency is too low.

T.R. -- Tran Ready -- Transport Ready -- Transport ready is a signal from the tape recorder indicating that the tape recorder is not doing a functional operation and is available to receive a command from the digitizer.

T.R. Synch. -- Transport Ready Synchronous -- This signal indicates the transport ready has been synchronized to the 1 MHz clock of the digitizer.

GIP -- Gap in Progress -- A signal from the tape recorder signaling the digitizer that the tape recorder is gapping between records, thus disabling the writing capabilities of the digitizer.

GIP Synch. -- Gap in Progress Synchronizer -- This signal indicates the GIP signal is synchronized to the 1 MHz clock.

Write Reset -- A signal from the master sequencer in the idle state or data loop of Fig. 4, which clears the write cycle sequencer and data multiplexer control counter on plate 2. This signal merely readies the digitizer for another data word.

$\overline{\text{GAP}}$-GAP NOT -- $\overline{\text{GAP}}$ is a control signal from the master sequencer clearing the data word counter, because a new record is starting, and this section keeps an accounting of the number of words/record and loads the data multiplexer control counter. Note that this control counter will start a count according to the coding of the inputs. From plate 2, channels A and B will have a logical 1 and C and D have a zero, or 1 1 0 0 which in binary is the number three. In Fig. 6, note that the number three appears in the first block of the write time section. Thus, we observe a direct correlation between the state diagrams and the hardware.

Data Count -- Each pulse of the 1 MHz clock that is contained in each data word is a data count. This count occurs during states 3 to 8 of the master sequencer. In states 1 and 2 there is no data count.

IRGCT $\geq$ RS -- Ir errecord gap greater or equal to record size. A command from the data word counter indicating that the digitizer has written the required 256 words in the current record. This command will ultimately clear the master sequencer and decoder in order to prepare for a new record.

$\overline{\text{WRITE DATA}}$ -- A command signal from the master sequencer and decoder to the master sequencer section of plate 1 to indicate data are being written. The master sequencer is inhibited until the writing has been completed.

$\overline{\text{WRITE TIME}}$ -- A command signal from the master sequencer and decoder to the master sequencer to indicate time is being written. The master sequencer is inhibited from changing until the time has been written on tape.

Write -- Initiates in states 4 or 7 of the master sequencer on plate 1 and is transferred to the write-cycle sequencer. The signal triggers the dual J-K flip-flop in the write-cycle sequencer on the "B" side, changing its output to its complement. Then, depending on the condition of IC Nos. 26 and 31, to which the write command goes, a write "B" or write "D" will be issued.

CLR DATA -- The clear data signal is produced by gate 27B when the write cycle is in state D and shifts the write cycle counter back to stab A. This signal indicates the write cycle has been completed.

Write "B" -- Write B is a pulse initiated by the output of the dual J-K flip-flop of the write-cycle sequencer. It is the command pulse that clears and readies the write step and IR counter in order to prepare to write some type of data on the tape. It also sets the WCT $\geq$ C1 and C0 latches to 0.

WCT $\geq$ C1 -- Word Count $\geq$ Count C1 is the pulse checker section which checks duty cycle and pulse duration. The WCT $\geq$ C1 section rejects any input signal falling outside the following limits. 8 Hz $\geq$ f $\geq$ 300 Hz. Count C1 is the 300 Hz control signal and count C2 is the 8 Hz control signal.

Write Step and IR Counter -- The write step and IR counter is shown on plate 1 and is the section of the digitizer which checks the quality of the incoming data word. There is a high and low frequency limit and duty cycle checker.

MSCT Hold -- Millisecond Counter Hold -- This signal is used in order to ready the digitizer to write time data on the tape recorder. In effect the time is frozen in the storage time buffer until it has been transferred to tape.

$\overline{\text{UPDATE TIME}}$ -- The inverted logical signal of update time also called update time not -- This signal commands the time storage buffer shown on plate 3 to load the time input information.

$\overline{\text{CLR MS CT}}$ -- Clear Millisecond Counter Not -- This command clears the millisecond counter shown on plate 3 on every second on the output of the pulse synchronizer (see pin 3 on IC No. 16, plate 1).

Pulse Synchronizer -- The pulse synchronizer is a section of the digitizer which takes the 1 kHz pulse from the ground range time unit and synchronizes this signal and the 1 MHz oscillator of the digitizer.

Shape Data -- a latch and synchronizing section following the raw input section which sharpens up each data pulse.

Resume -- A signal in the data multiplexer control counter of plate 2 which couples the state of the multiplexer's output to the write cycle sequencers gate logic. If the multiplexer while counting goes to a complete count, i.e., 1 1 1 1, and the record size is still not exceeded, resume allows the multiplexer to clear and resume its operation of gating data or time onto the tape recorder.

MUX EN -- Multiplexer enable is one of four command lines from the data multiplexer control counter to the multiplexer, which allows the selected inputs of the multiplexer to be written on tape. (MA, MB, and MC are the other three control lines.)

Data Multiplexer Control Counter -- This is the logic element which allows either time or data information to be written on tape. The type of command to the clear and load input will determine whether the data multiplexer begins counting at 0 or 3. If beginning at 3, time will be written; if beginning at 0, data will be written, as shown by the write counter of Fig. 6.

Write "D" -- is the command to write.

Count CO -- Count CO is the pulse checker on incoming frequency data. This signal has an 8 μ second delay after the beginning of the data pulse in order to insure stability of the digital data.

V. Appendix

IC's on the Digitizer

1-6: ~~RAY-7339~~ 74163 = 4-bit counters.
7: 7442 - 4-line-to-10-line decoders (1-of-10).
8: 7410 = triple 3-input positive NAND gates.
9: 7400 = quadruple 2-input positive NAND gates.
10: 7410 = triple 3-input positive NAND gates.
11: 7430 = 8-input positive NAND gates.
12: 7420 = dual 4-input positive NAND gates.
13: 7410 = triple 3-input positive NAND gates.
14: 7404 = hex inverters.
15: 7427 = triple 3-input positive NOR gates.
16: 7432 - quadruple 2-input positive NOR gates.
17: 7473 = dual J-K flip-flops with clear.
18-20: 7400 = quadruple 2-input positive NAND gates.
21: 7402 - quadruple 2-input positive NOR gates.
22: 7427 = triple 3-input positive NOR gates.
23: 7404 = hex inverters.
24: 7400 = quadruple 2-input positive NAND gates.
25: 7473 = dual J-K flip-flops with clear.
26: 7410 = triple 3-input positive NAND gates.
27: 7420 = dual 4-input positive NAND gates.
28: 7400 = 8-input positive NAND gates.
29: 7404 = hex inverters.
30: 7408 = quadruple 2-input positive AND gates.
31: 7410 = triple 3-input positive NAND gates.
32: Blank
33: 7404 = hex inverters.
34: 7413 = dual 4-input positive NAND schmitt triggers.
35-38: RAY-7339 = 4-bit counters.
39: 7427 = triple 3-input positive NOR gates.
40: 7430 = 8-input positive NAND gates.
41: Blank
42: 7430 = same as number 40.
43: Blank
44-56: 74163 = 4-bit counter.
57-62: FAIRCHILD ~~7413~~ 2512 - the multiplexer.
63: 74174 = hex/quadruple d-type flip-flops with clear.
64-68: 74163 = 4-bit counter.
69-78: FAIRCHILD ~~6848~~ 9328 = level translator.
79: 7412 = triple 3-input positive NAND gates.

Plate 1

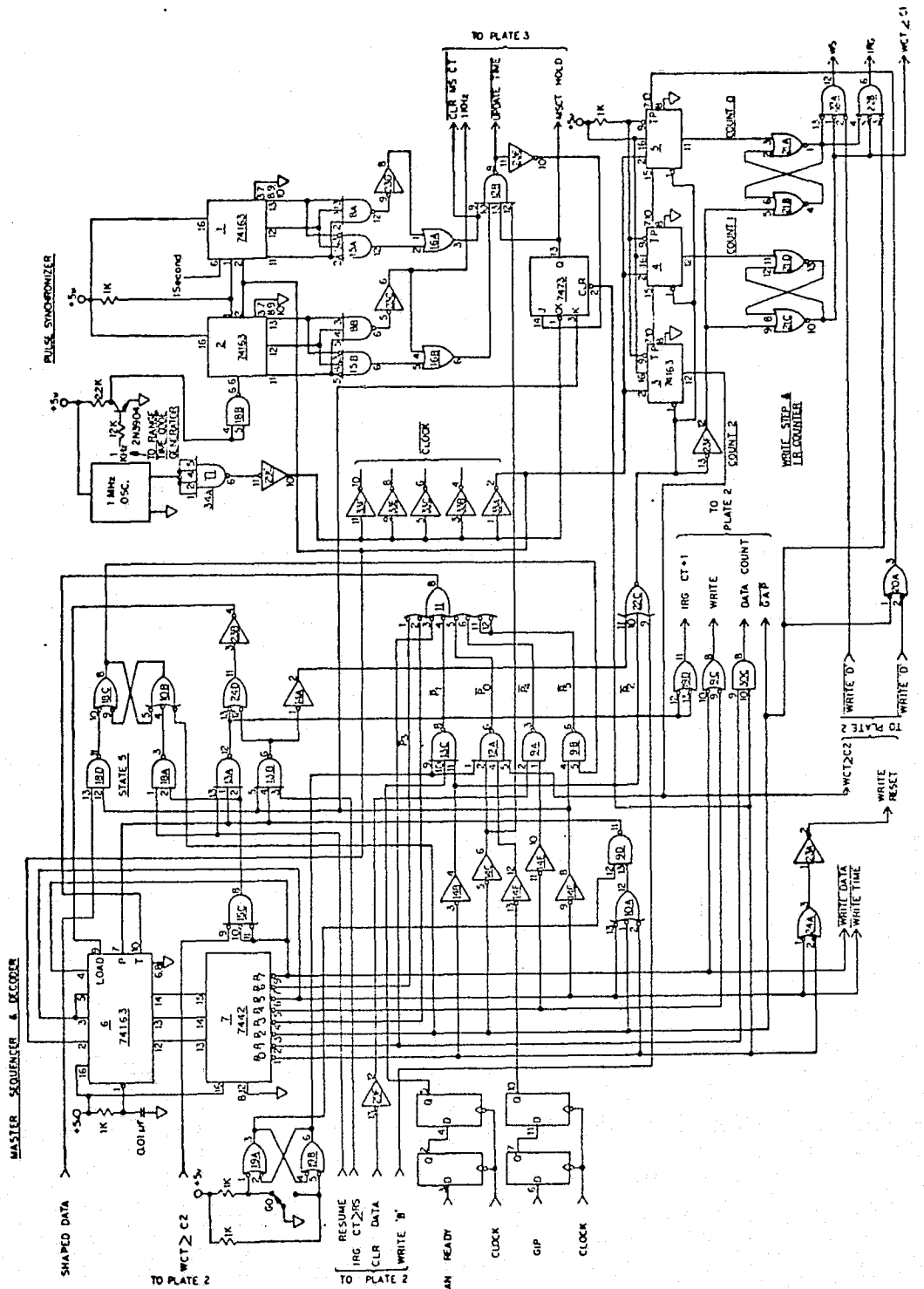
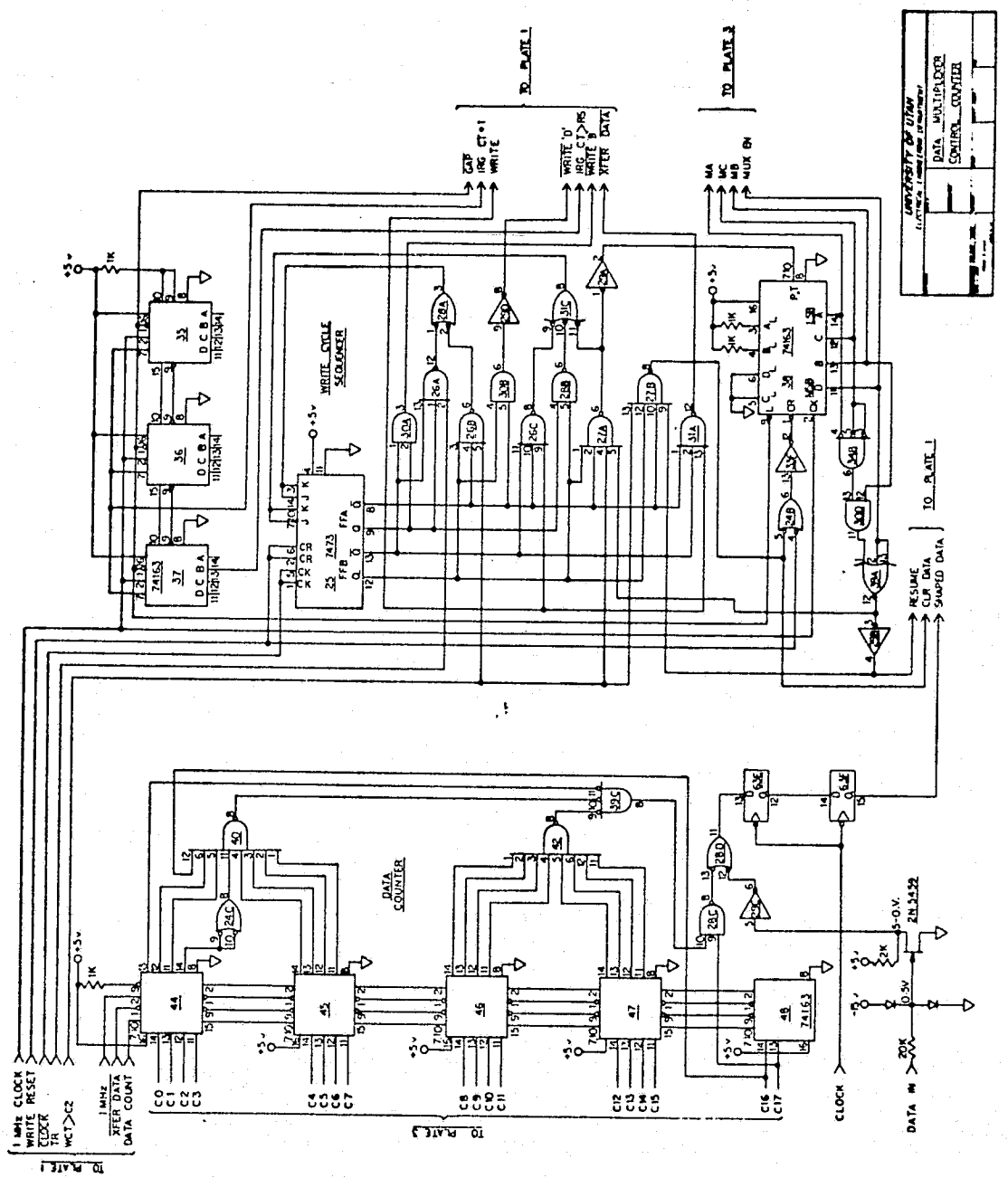


Plate 2



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OF POOR QUALITY

Plate 3

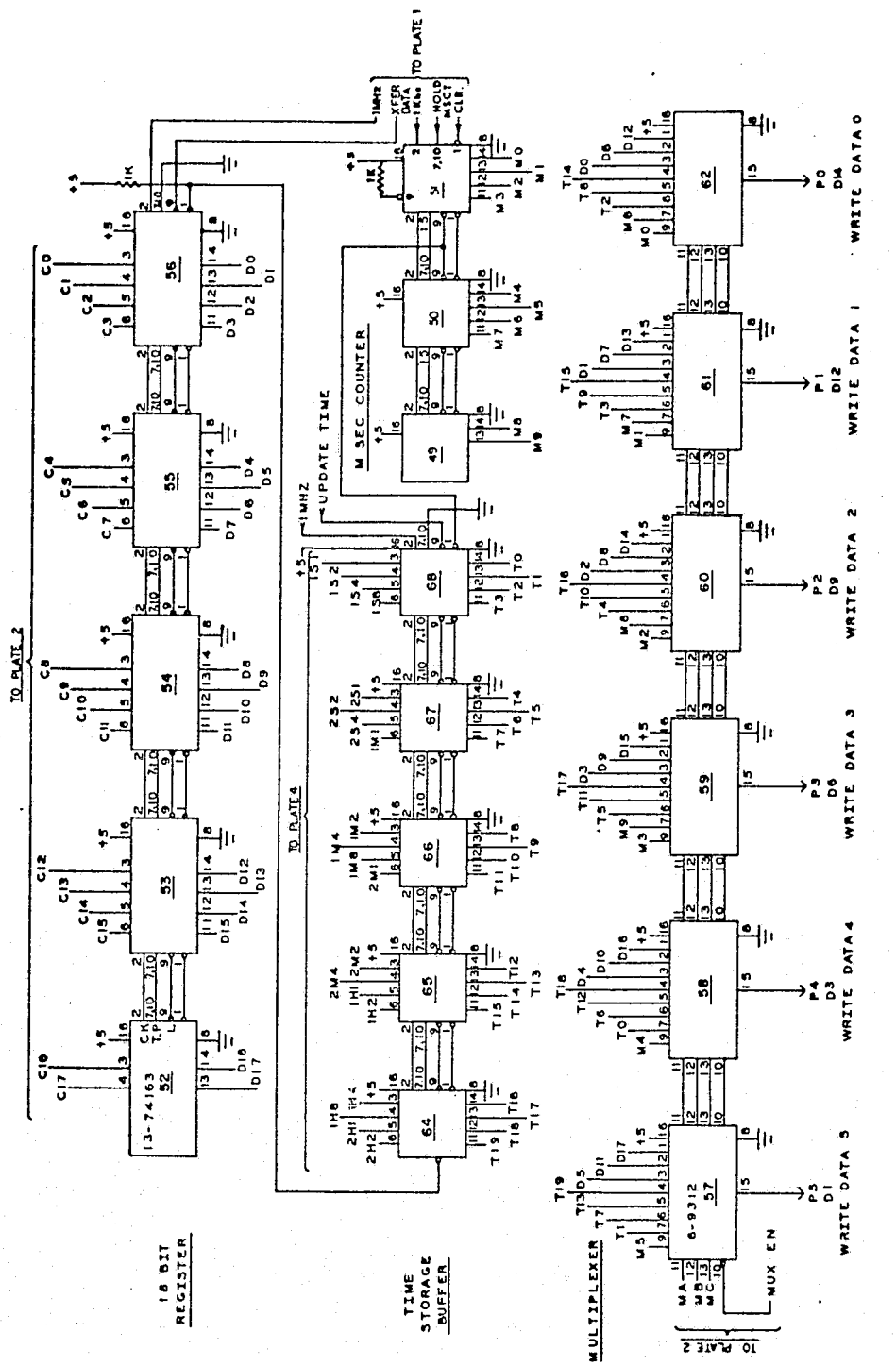
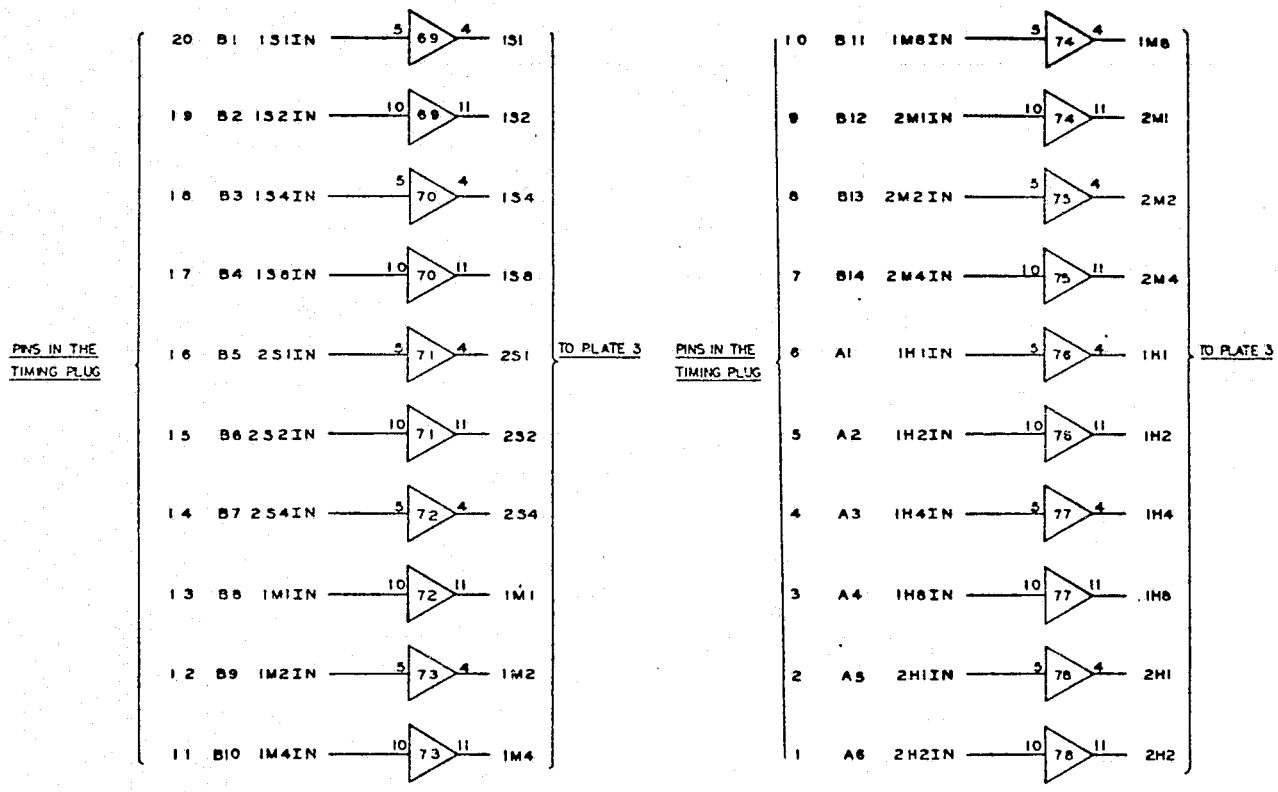


Plate 4

LEVEL TRANSLATORS



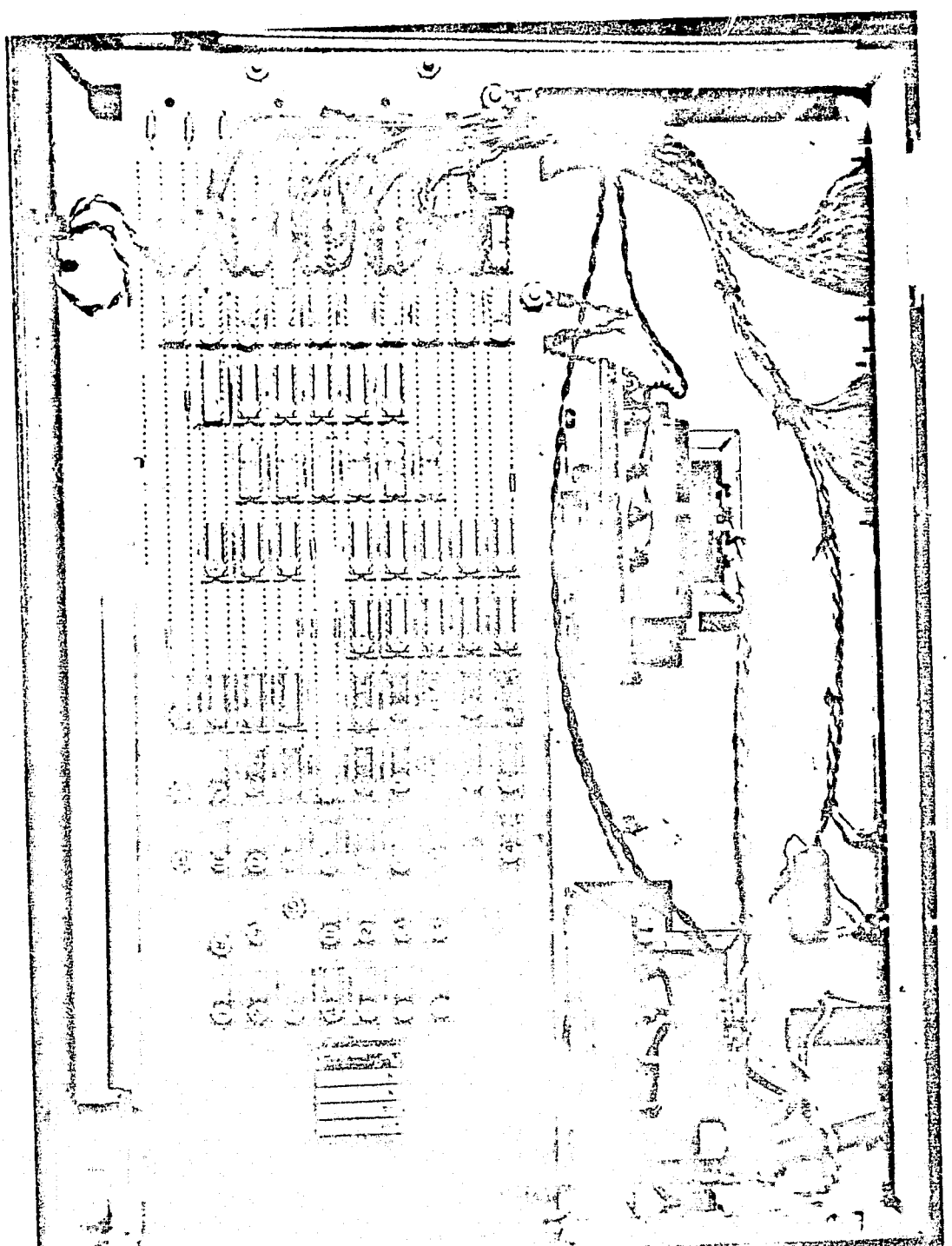
Note: Common Power Connections

V_{cc} - Pin 14

V_{dd} - Pin 7

Gnd - Pin 1

Plate 5



The original University of Utah precision meteorological data digitizer unit was designed, constructed, and applied to rocket meteorological sensor research purposes at the University of Utah by Thomas L. Bates in 1969. The time word provision was added by Joseph D. Terry, Jr. With minor modification, the unit continues to serve the University research project, both in direct-digitizing in the field and in post-flight digitizing in the laboratory of direct-recorded flight data. A second unit constructed by the University for operational use at Wallops Flight Center proved unreliable under continuous field conditions. The present Wallops unit was completely redesigned by R. M. Garn in early 1974, according to this document, for use in rocket soundings for which precision and complete recording of the data are required for research or other special purposes. Acknowledgment is due Russell L. Smith and Gus H. Liapis whose assistance in construction and documentation, respectively, contributed significantly.

It is noted that the digitizer described herein provides for convenient interfacing for real-time data monitoring.