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STUDY OF SEM INDUCED CURRENT AND VOLTAGE CONTRAST MODES TO ASSESS SEMICONDUCTOR RELIABILITY

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PREFACE

The purpose of the scanning election microscopy (SEM) study was to review the failure history of existing integrated circuit technologies to identify predominant failure mechanisms, and to evaluate the feasibility of their detection using SEM application techniques. The study investigated the effects of E-beam irradiation damage and contamination deposition rates; developed the necessary methods for applying the techniques to the detection of latent defects and weaknesses in integrated circuits; and made recommendations for applying the techniques.

FOREWORD

This effort was conducted for the George C. Marshall Space Flight Center in contract NAS8-31567, Study of SEM Induced Current and Voltage Contract Modes to Assess Semiconductor Reliability. The study was conducted by the Martin Marietta Corporation, Denver Division.

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I. INTRODUCTION

Since the arrival of the scanning electron microscope (SEM) at the market place in 1964, many applications for semiconductors have evolved. Some have provided a valued capability for examining, measuring, analyzing, and evaluating semiconductor surfaces and interconnect systems, while others have been considered novelties.

The SEM is widely accepted for providing visual examination of physical characteristics for semiconductor metalization and oxide surfaces. These inspections are conducted on a sample basis for individual production lots and are limited to the detection of lot common defects. Sampling is necessitated because the electron beam exposure may result in electrical degradation to the semiconductor. Investigations show that some devices have been electrically degradated from electron beam exposure. The majority of this work has involved the study of MOS semiconductor technologies. The deposition of a contaminating layer during electron beam exposure has also been a concern.

Another SEM application is the voltage contrast operating mode. This mode has been used primarily for fault isolation in integrated circuits (ICs). The possibility of irradiation damage during examination has generally been ignored or discounted. The interaction of the electron beam and electrical circuit operation has also been a questionable area.

The application of electron beam-induced current (EBIC) or specimen current operating mode has generally found little practical use. This mode of operation requires a good understanding of the specific semiconductor device construction and electron beam interaction with the semiconductor.

The primary objective of this study was to evaluate the feasibility of developing and using SEM applications for screening historic latent defect escapes in production devices. To accomplish this, it would be necessary to perform a 100% SEM examination of production devices. If a 100% examination were not possible, this screening would not be applicable to defects having a random or low-frequency occurance rate. For a 100% examination to be feasible, significant electron beam degradation of the semiconductor device cannot be tolerated.

Throughout this study, it was determined that electron beam degradation for a cross section of semiconductor devices was severe. This necessitated redirecting the primary objective of this study to developing semiconductor failure analyses and destructive sample applications.

The applications described in this report should be valuable tools for semiconductor reliability and process engineers.* It was the intent of this study that the applications not require elaborate SEM instrument modification or additional accessories.

Table 1 Parts List

Circuit Complexity	Part Family	Part Type
SSI	Bipolar Digital	54L04 Hex Inverters
	Bipolar Linear	LM111 Comparator
	MOS Digital	G116 5-Channel PMOS FET Switch
MSI	Bipolar Digital	54L95 4-Bit Shift Register
	Bipolar/MOS Linear	2700 Operational Amplifier
LSI	Bipolar Digital	IM5523C 256 x 1 Bit RAM
	MOS Digital	S8501 256 x 1 Bit ROM

Table 1, above lists a cross section of integrated circuit devices which were identified for use as test specimens. The devices were selected to include different levels of circuit complexity, MOS and bipolar technologies and digital and linear circuits. Five each of the devices were purchased and used as test specimens for this study.

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*They may provide a more practical method of disclosure and, thereby, an improved understanding of their significance.

II. HISTORICAL DATA REVIEW FOR INTEGRATED CIRCUIT FAILURES

Integrated circuit (IC) reliability history was reviewed to obtain an overview of IC failure experience. The primary area of interest was defects that showed a potential for detection or evaluation through SEM/electron beam techniques. The failure experience considered in this review was that which followed piece-part level screening and acceptance. This experience would therefore be representative of failures that had not been detected by the particular level of screening and testing that was employed. The review was limited to IC part experience that had passed, as a minimum, the screening requirements of MIL-STD-883, Method 5004, Level B, or equivalent.

A. GIDEP HISTORICAL DATA REVIEW

The Government Industry Data Exchange Program (GIDEP) alert summaries were reviewed for the period from 1968 through July 1975. There were 133 alert summaries reviewed for microelectronic circuits (Sections 515.00 through 515.90). The alert reports selected for review were those that described defects that may have been detected by SEM techniques. There were 36 alert reports (or 27% of the summaries) identified for review. Of the 36 reports reviewed, four were eliminated because of alert retractions or because they were supplemental reports for previous alerts. One alert report identified two failure defects, so the total number of failure defects reviewed was 33. Table 2 shows the failure modes, problem categories, and frequency. The metalization defects were separated from the operational degradation group to show that these defects have been eliminated through the use of SEM inspection. SEM inspection began around 1971 and was in general use by 1972. A summary of the defects and the cause responsible for failure in each group is given in Table 3. A comparison of failure mode, process technology, and circuit complexity is shown in Table 4, and a comparison of failure mode, circuit type and circuit complexity is shown in Table 5.

Table 2 GIDEP Alert Historical Review

Failure Mode	Problem Category	68	69	70	71	72	73	74	75	Total
Operational Degradation	Manufacture	2	2	1			1	4	1	11
Metallization Defect	Manufacture	2	1	1	3	1				8
Die Defect	Manufacture								2	2
Deficient Operation	Design	1		1	1	2	3	1		9
Erroneous Operation	Application							2	1	3

Table 3 GIDEP Alert Review

Failure Mode	Problem	Cause
Operational Degradation (11)	Defective Mask (4)	Metalization Bridge (2) Missing Cross under Diffusion (1) Surface Inversion (1)
	Surface Contamination (3)	Solder Glass on Die (1) Sodium Contamination (1) Si Crystal Orientation (1)
	Diffusion Defect (1)	Open Buried Resistor (1)
	Oxide Defect (1)	Capacitor Oxide Breakdown (1)
	Insufficient Data to Classify (2)	
Metallization Defect (8)	Open at Oxide Step (7)	Insufficient Metal Coverage (6) (No SEM Lot Inspection)
	Overnotched (1)	Breakdown of Photoresist (1) (No SEM Lot Inspection)
Die Defects (2)	Bulk Defects (2)	Decreased Isolation Breakdown Voltages (2)
Deficient Operation (9)	Circuit Design (5)	Changes in Circuit Design (1) Four Layer Latchup (1) No Output Short Circuit Protect (1) Insufficient Differential Input Breakdown Voltage (1) Circuit Instability (1)
	Mask Design (2)	V_{cc} Interaction (1) Floating N Minus Layer (1)
	Oxide Design (1)	Surface Inversion (1)
	Insufficient Data to Classify (1)	
Erroneous Operation (3)	Unique Stimulus Application (2)	Circuit Design (2)
	Misapplication of Part (1)	Exceeded Design Rating (1)

Table 4 GIDEP Alert Historical Review

Failure Mode	Process Technology	SSI	MSI	LSI
Operational Degradation	Bipolar	7	3	-
	MOS	-	1	-
Metalization Defect	Bipolar	6	-	1
	MOS	-	1	-
Die Defect	Bipolar	1	-	-
	MOS	-	1	-
Deficient Operation	Bipolar	5	2	-
	MOS	1	1	-
Erroneous Operation	Bipolar	1	2	-
	MOS	—	—	-

Table 5 GIDEP Alert Review

Failure Mode	Circuit Type	SSI	MSI	LSI
Operational Degradation	Digital	2	3	-
	Linear	5	1	-
Metalization Defect	Digital	2	1	1
	Linear	4	-	-
Die Defect	Digital	-	1	-
	Linear	1	-	-
Deficient Operation	Digital	2	2	-
	Linear	4	1	-
Erroneous Operation	Digital	1	-	-
	Linear	-	2	-

B. MARTIN MARIETTA FAILURE DATA REVIEW

Martin Marietta conducted a review of integrated circuit failure data compiled during the Viking '76 Mars lander program. These data represent IC device experience for parts that had passed stringent high reliability (hi rel) screening and testing requirements. These data were reviewed to identify multiple failure incidents that resulted within individual lots because of inherent surface or near surface defects. From these data, six failure cases were identified (two were diffusion related defects, two were mask related defects, and two were oxide defects). These six failure modes represented six of a total of 38 device types used on this program. A summary of these failures is shown in Table 6. A comparison of discrepancy, process technology, circuit type, and circuit complexity is shown in Tables 7 and 8.

Table 6 Martin Marietta Failure Data Review

Discrepancy	Problem	Cause
Operation Degradation (4)	Defective Mask (2)	Metalization Bridge (1) Missing Diffusion (1)
	Oxide Defect (2)	Pinholes in Oxide under Interconnect Metalization (2)
Die Defect (1)	Bulk Defects (1)	Resulted in Diffusion Pipes and Increased I_{CEO} (1)
Deficient Operation (1)	Mask Design (1)	Resulted in Discontinuity in a Buried Resistor (1)

Table 7 Martin Marietta Failure Data Review

Discrepancy	Process Technology	SSI	MSI	LSI
Operational Degradation	Bipolar	1	1	1
	MOS	-	-	1
Die Defect	Bipolar	-	1	-
	MOS	-	-	-
Deficient Operation	Bipolar	-	1	-
	MOS	-	-	-

Table 8 Martin Marietta Failure Data Review

Discrepancy	Circuit Type	SSI	MSI	LSI
Operational Degradation	Digital	1	1	2
	Linear	-	-	-
Die Defect	Digital	-	1	-
	Linear	-	-	-
Deficient Operation	Digital	-	-	-
	Linear	-	1	-

C. DATA REVIEW FROM THE MICROCIRCUIT MANUFACTURING CONTROLS HANDBOOK

This handbook is a consolidation of current failure mechanism information on microcircuits. The handbook lists failure mechanisms, methods for detection, possible causes, and corrective action for elimination of the problem. This handbook was conceived and sponsored by RADC. ICE, RADC, and a service/industry committee cooperated in its preparation. It was published in July 1975 and is periodically updated so it provides a current failure mechanism reference source for this data review. Out of the approximately 60 microcircuit failure experiences reported, about half were field failures. ' review of the failure description showed 10 that may have been detected by SEM techniques. These failures are summarized in Table 9.

Table 9 Microcircuit Manufacturing Control Handbook Review

Discrepancy	Problem	Cause
Operational Degradation (4)	Oxide Defect (2)	Variation in Gate Oxide Breakdown (1) Poly Si to Aℓ Shorts (1)
	Surface Contamination (1)	Surface Leakage (1)
	Glass Passivation Cracks (1)	Discontinuity in Thin-Film Resistors (1)
Metalization Defect (1)	Open at Oxide Step (1)	Insufficient Coverage (1)
Die Defects (2)	Bulk Defects (2)	Diffusion Pipes Resulting in Increased I_{CEO} (2)
Deficient Operation (3)	Mask Design (3)	Unguarded Diffusions (1) Buried Resistor Discontinuity (1) Inversion of Nonmetalized Gate Region (1)

D. RAC MICROCIRCUIT RELIABILITY REPORT REVIEW

This report (MDR-1) was prepared by the reliability analysis center at the Rome Air Development Center. It is a data summary of digital generic data providing reliability and experience information for digital microcircuit devices. The device failure information provided in this report was reviewed to obtain experiences related to particular failure modes. Failures related to diffusion, passivation, and metalization anomalies were of primary interest.

The bipolar DTL data experience includes dielectric and junction isolated circuits and standard, high threshold, low power, and radiation hardened families. Included in this review are data for circuits that were screened to MIL-STD-883 Class A and B, or equivalent. Only failures that had been classified could be included in this review. For example, of 1604 reported DTL failures, only 963 included sufficient detail for failure classification in the data summary. Therefore, only a partial overview of this failure history was possible. Note too that these data indicated a reduction in use for DTL in new design after 1972. The data reviewed represented a total of 6.8×10^{10} hr of part operation or a calculated 0.024 FPMH. A matrix was prepared listing the failure classifications and frequency of occurrence (see Table 10).

Table 10 RAC Microcircuit Reliability Report Review

Area Related to Failure	Point of Failure	68	69	70	71	72	73	74	75
Glassivation	Screen								
	Field								
Die Metalization	Screen					1			
	Field	1	139		1			2	
Die Thermal Oxide	Screen								
	Field	100	4	13					
Die Surface	Screen								
	Field		4	5					
Thin Film Element (Radiation Hardened)	Screen								
	Field			10				7	

DTL Microcircuits, MIL-STD-883 Class A and B, or equivalent.

The bipolar TTL data experience included standard, high speed, low power, and schottky circuit families. All employed junction circuit isolation. Only data from circuits that were screened to MIL-STD-883 Class A and B, or equivalent, were included in this review. Out of 424 failures reported, only 13 were classified in this data summary. Therefore, a data matrix was not prepared. The data reviewed represented a total of 4.0×10^8 hr of part operation or a calculated 1.06 FPMH.

E. HISTORICAL DATA REVIEW SUMMARY

It was difficult to obtain a reasonable failure experience overview from military and aerospace systems. The actual failure mechanism identification depends on the depth to which the failure is analyzed and the accuracy of the analysis. A thorough compilation of failure data can provide a valuable tool for understanding and evaluating individual technology performance and the credibility of inspection and screening criteria.

The results of this data review show no trends that would suggest the feasibility of sample screening. The defects that are escaping current inspection and screening are from low incidence to random occurrences. They can occur periodically in clusters having a population in the area of 10% or randomly distributed with a population of less than 1%. Some problems are basic to circuit design or processing; it is difficult or impractical to detect them using typical inspection and screening techniques. Other defects result from the accumulation of tolerances or a deterioration in process control.

The data review shows that a significant number of device defect escapes are surface related and may be disclosed through SEM examination. This data review can only be used to provide trends and does not reflect a quantitative estimate of defect escapes. One area that was not identified is the delay that results in product shipment when a part type fails to pass inspection and screen test at the supplier's facility. This can be nearly as serious a problem with its impact on system production schedules as defect escapes can have on system failures, and both are heavily dependent on part quality and reliability.

The SEM applications initially proposed for development study still appear to be good. The EBIC applications included oxide defect and junction defect identification, metalization integrity at oxide steps and location of surface leakage paths. The voltage contrast applications included diffusion depth measurement, location of surface leakage paths, and functional circuit testing.

III. ELECTRON BEAM IRRADIATION DAMAGE AND CONTAMINATION

A. IRRADIATION DAMAGE

Examination of semiconductors by SEM has been considered to be degrading to the electrical characteristics. The possibility of damage has been identified through studies of electron beam irradiation effects on semiconductor surfaces and practical experience with the SEM. Little information is available to provide the SEM operator with an appreciation for the sensitivity of current semiconductor devices to electron beam damage.

This investigation was made to determine whether semiconductors might be examined on a production basis. Some of the questions to be answered were:

1) Does degradation occur?

2) What parameters are affected?

3) How much degradation would occur under typical SEM operating conditions?

4) How quickly does degradation occur?

5) What is the mechanism for degradation?

6) Are MOS devices more susceptible than bipolar?

To better understand these questions, it is necessary to review the mechanics of electron-solid interaction. In the SEM, electrons are emitted from the cathode and are accelerated within the electron gun. The acceleration of the electron is determined by the voltage potential difference between the cathode and anode in the gun. The energy of the electron is measured in electron volts (eV). An electron that has been accelerated through a potential of 20 kV has an energy of 20 keV. As the electrons travel through the electron column, they alternately diverge and converge along the optical axis as they pass through magnetic lenses. This is the process of demagnifying the electron crossover point from the electron gun to a finite point on the specimen. During their travel down the electron column, electrons having greater or lesser energy levels than nominal are removed by the apertures. Therefore, the primary electrons arriving at the specimen surface are considered to be monoenergetic.

The electron interactions with the specimen surface are very complex. However, the two basic mechanisms are elastic and inelastic electron scattering. It is basically through these mechanisms that the primary electron energy is dissipated. Elastic scattering is described as a change in electron direction with little energy loss. Inelastic scattering is described as an energy loss with little change in electron direction. An elastic interaction or collision results from an interaction between an electron and the nucleous of an atom. The elastic collisions produce the backscattered electrons. An inelastic collision consists of two mechanisms. They are the interaction between an electron and the nucleus of an atom and the interaction between an electron and an electron of an atom. The first interaction produces Brensstralung x-rays, and the second produces secondary electrons and elemental characteristics x-rays. Those electrons that travel into the specimen and are absorbed produce specimen current.

As electrons penetrate the specimen surface the direction of travel becomes random. It is determined by the number of collisions and the angle of deflection for each. Also, the distance of penetration depends on the number of collisions and the initial energy of the primary electron. Therefore, the amount of energy dissipated in a solid depends on the density of the material, the energy of the primary electron, the rate of primary electrons incident on the specimen surface, or the exposure time and the area scanned. Electron beam damage is a result of electron penetration and electron energy dissipation in the specimen surface.

Many studies have investigated the physical characteristics of electron damage in semiconductors. Many of these studies have investigated the electrical changes that are experienced by MOS and MIS devices (Ref 1-10). Electrical changes in bipolar devices have been studied to a lesser degree, (Ref 11-14). The studies have shown that the electrical changes have resulted from positive charges trapped in the oxide or insulator. Grove & Snow (Ref 1) and Mitchell (Ref 3) have shown these positive charges are located within 200 Å of the insulator/semiconductor interface.

There are two irradiation damage mechanisms that can occur with electron beam exposure. They are atomic displacement and trapped charge. Atomic displacement, which occurs through the Rutherford scattering mechanism, is an interaction between an incident electron and the nucleus of an atom. The energy lost by the electron is small and depends on the incident electron energy. For atomic displacement to occur through Rutherford scattering, the incident electron energy would have to be in the area of 500 keV. The proposed model (Ref 3 and 4) for trapped charge is that the charge is created when electrons and holes generated by the incident radiation are

trapped at preexisting electron-hole traps. Based on these two models, it appears that electrical changes in irradiated semiconductors are due to trapped charges in the thermal oxide.

However, another study Simons *et al.* (Ref 15), shows that the annealing behavior of MOS structures irradiated with low energy electrons suggests that the trapping of electrons and holes in an insulator may be invalid. The data show that for an activation energy of 0.28 eV, the trapped charge would be expected to decrease to 37% of its initial value after 10 minutes at a temperature of -113°C. The experimentally observed temperature for this anneal rate was 227°C.

A preliminary investigation by Venables (Ref 16) suggests a third mechanism. This mechanism appears to have good agreement with previously described models and with other reaction characteristics that were previously unexplained. This irradiation damage mechanism is atomic displacement through ionization of the atom. This is identified as the Varley mechanism (Ref 17 and 18). This damage is described as the formation of atomic vacancies and interstitials, some of which persist as nonequilibrium defects after irradiation. Venables suggests that as a result of the atomic displacement in an insulator, with ionic or partially ionic bonding, an intrinsic charge would be formed. Three important factors were identified by Venables that would be expected to lead to a predominately positive charge formation by this mechanism. First, the relative amounts of positive and negative charge produced by atomic displacement will be dependent on the anion and cation ratios in the insulator. This may explain radiation damage susceptibility differences between SiO_2 and Si_3N_4 insulator materials and the propensity toward positive trapped charges. The reasons for a greater radiation tolerance of Si_3N_4 have not been well defined. The second factor is that the ratio of anion to cation vacancies formed would depend on the formation energy. Again for SiO_2, this would favor a positive charge formation. The third, and most important, factor is related to the annealing processes that may take place in the material during irradiation. It has been well established for many materials that some radiation induced defects are highly mobile at room temperatures and a great amount of annealing may occur. Therefore, the residual damage after radiation may be more dependent on the recovery processes than on the generation processes. Venables reports that preliminary investigation has also shown the generation of defect clustering in crystalline quartz. These defects may be due to the clustering of oxygen interstitials. The defect clustering and disappearance of the electron diffraction pattern have occurred over a period of approximately 3 minutes. A thinned crystalline quartz sample was exposed to electron bombardment in a transmission electron microscope. The defect clusters were observed to develop under normal beam intensities and at acceleration voltages as low as

50 keV. It is expected that the irradiation damage would be similar for amorphous SiO_2. Venables also reported that examination of Si_3N_4 microstructure in the electron microscope has shown the damage rate (defect clustering) to be orders of magnitude lower than SiO_2.

The significance of the proposed atomic displacement damage by the Varley mechanism is that crystaline damage may be generated rather than trapped electrical charge. It is also probable that this mechanism would occur in a SEM for acceleration voltages in the area of 10 kV and higher. The minimum acceleration voltage required to cause damage is that which would provide an electron penetration range greater than the SiO_2 thickness.

A test program was developed to better appreciate the susceptibility to radiation damage for current device technologies. Common NPN and PNP discrete transistors and N and P channel MOSfets were used to "ballpark" the electron beam and exposure parameters. The NPN transistors were 2N2222A and the PNP transistors were 2N2905. The N channel MOSfets were 3N171 and the P channel were 3N163. The discrete devices were used to allow *in situ* measurement of device beta or channel current threshold. This was accomplished by interconnections between the device in the SEM and a transistor curve tracer. This provided the capability to measure electrical parameters following each radiation exposure period.

The SEM instrument used throughout this study is a Cambridge Stereoscan S180. This instrument provides a three digit digital meter for displaying acceleration voltage and sample current. The beam current was measured with a Faraday cup located adjacent to the specimen.

The first test sample was a 2N2222A NPN transistor. The SEM parameters were E_B = 10 kV and $I_B = 1 \times 10^{-8}$ A. Two betas were initially measured on the transistor. B_1 was 140 for I_C = 10 μA, V_{CE} = 10 V and B_2 was 200 for I_C = 1 ma, V_{CE} = 10 V. In the time required to set up the instrument (approximately 15 sec), the betas had been extremely degraded, B_1 to 3 and B_2 to 24. During irradiation, the transistor emitter, base, and collector were terminated at ground. The estimated electron fluence was 1.22×10^{15} e/cm^2.

> Note: All radiation exposure levels will be given as electron fluence. Dose (Rads SiO_2) were not calculated.

For the second test using the same device type, an E_B = 10 kV and $I_B = 2 \times 10^{-10}$A were used. (B_1 is I_C = 10 μA and V_{CE} = 10 V and B_2 is I_C = 1 ma, V_{CE} = 10 V). During irradiation, E-B-C were terminated at ground.

B_1	B_2	Cumulative Irradiation Time, sec	Fluence, e/cm^2
100	180	Initial	-
18	88	+10	1.6×10^{12}
17	84	+14	8.1×10^{12}
14	76	+18	1.5×10^{13}
12	76	+22	2.1×10^{13}
12	70	+26	2.8×10^{13}
11	66	+30	3.4×10^{13}

Following 24-hr storage at room temperature and atmosphere, the betas were remeasured. B_1 was 13 and B_2 was 72. Irradiation damage occurred very rapidly, and recovery at room ambient was small. The degradation was larger than anticipated and particularly for the 1 ma beta. The degradation rate was exponential and it tended to plateau rather quickly.

Additional devices were irradiated using SEM parameters of 20 kV and 1×10^{-10}A, which are more typical of normal operating conditions. The resultant degradation was similar to previous data. Devices also were irradiated with voltage applied and no difference in degradation rate or degree was apparent.

The other discrete device types were irradiated with similar experience. The rate of degradation for the MOSfet devices was dependent on the level of gate voltage applied. For a MOSfet irradiated with gate voltage applied and then with gate voltage removed the degradation did experience some recovery. Also the degradation saturation point was found to be dependent on the gate voltage level.

This preliminary testing was conducted to approximate the anticipated degradation rates for integrated circuits. The circuits selected for radiation testing were LM111, 54L00, G116, and HA2700. To obtain a more accurate assessment of the degradation experienced by the individual transistors, the transistor betas or conduction thresholds were individually measured before and after irradiation exposure. The circuits with glass passivation were irradiated with the glass in place. This test approach is more difficult to perform. However, it was felt that other approaches would severely compromise the results.

The procedure used for irradiation of one each integrated circuit type was to individually probe and record transistor betas or conduction thresholds. The transistors were selected to provide a representative sample of diffusion geometries, input and output transistors. The selected transistor cell or cells were irradiated and the E_B, I_B, area irradiated and cumulative irradiation time were recorded.

The first circuit evaluated is a 54L00 quad two input nand gate (non-glass passivated). In-circuit betas were measured for the four phase splitter transistors (Q2) and one current sink transistor (Q4). Transistor locations are identified in Figure 1. The second circuit evaluated is a G116 five-channel P MOSfet switch (glass passivated). Conduction thresholds (V_{GDth}) for I_D = 100 ua were measured for each fet. Various V_{GD} bias voltages were applied during irradiation. Fet locations are identified in Figure 2. The third circuit evaluated is an LM111 differential comparator (glass passivated). In-circuit betas were measured for the transistors identified in Figure 3. The fourth circuit evaluated is an HA2700 operational amplifier (glass passivated). In-circuit betas were measured for the transistors identified in Figure 4. Transistors from each circuit were irradiated at various magnifications and exposure times. The individual parameters were remeasured. Delta changes and electron fluence levels were calculated. The results are given in Table 11.

The degradation was much greater than anticipated. The data show that for these irradiation levels the examination of production integrated circuits cannot be recommended. The electron beam parameters used are typical for general SEM application. The magnifications and exposures were less than typical for most applications. Any increase in these factors will result in increased electron fluence. This may result in a greater degree of electrical degradation. No significant difference was observed for the susceptibility of biased and nonbiased bipolar devices. Transistors with higher gains were found to be more susceptible to degradation. The rate of degradation was found to be exponential, then reaching a plateau or saturation. For digital circuits, the beta may plateau at a level above the circuit design minimum. For these cases, the circuit will remain functional.

The irradiation damage mechanism may be atomic displacement. This is considered to have a greater electrical significance than an electron accumulation or deficiency in the oxide. Questions arise concerning the electrical characteristics of an irradiated circuit. What is the electrical stability of an irradiated circuit? What are the time and temperature parameters for annealing the irradiation damage? What is the electrical stability of an irradiated and annealed circuit? These are areas that require further investigation and analysis.

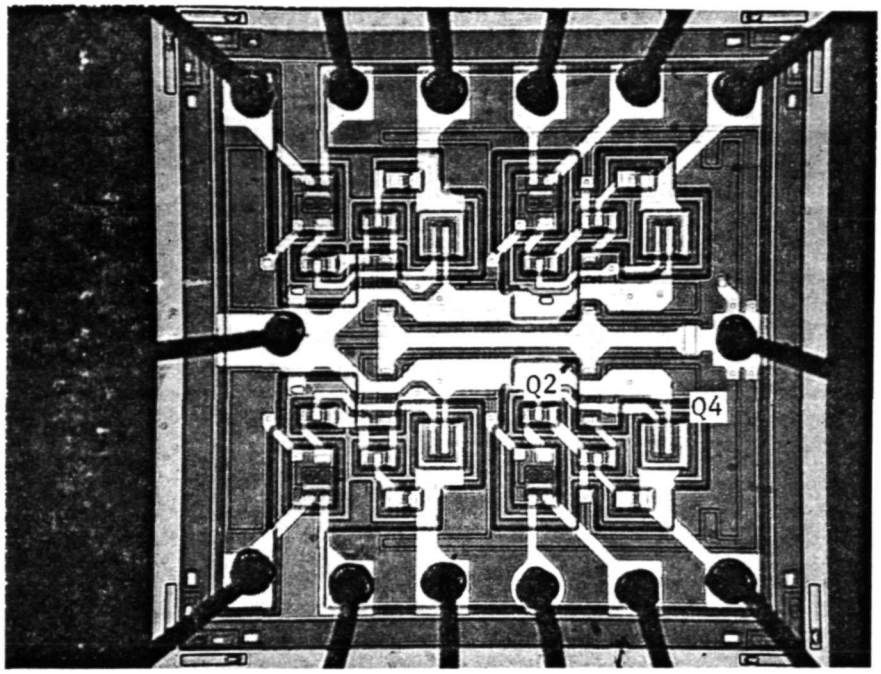

Figure 1. Photograph of 54L00 Identifying Transistor Locations, (X70)

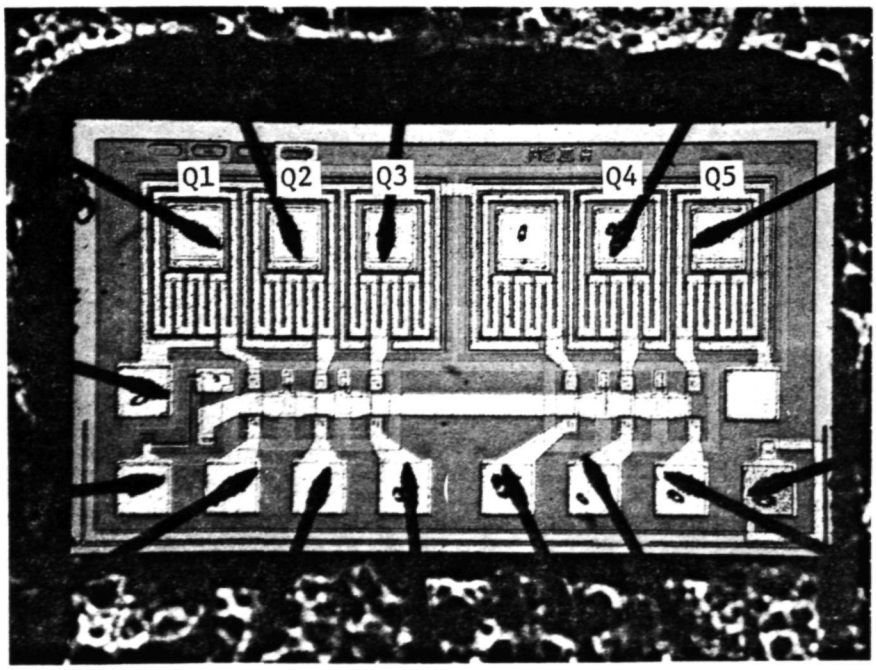

Figure 2. Photograph of G116 Identifying Fet Location, (X60)

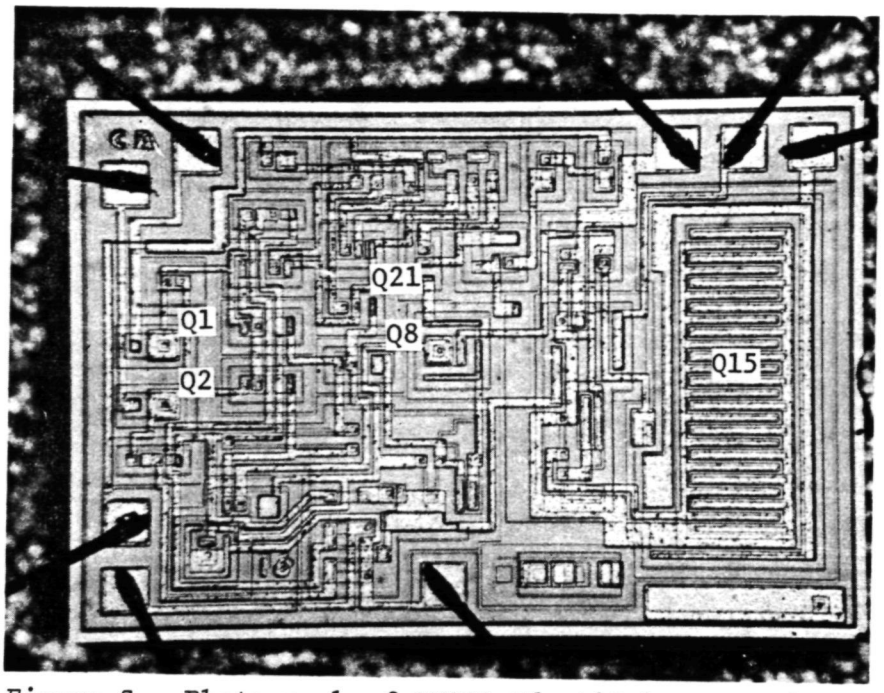

Figure 3. Photograph of LM111 Identifying Transistor Locations, (X60)

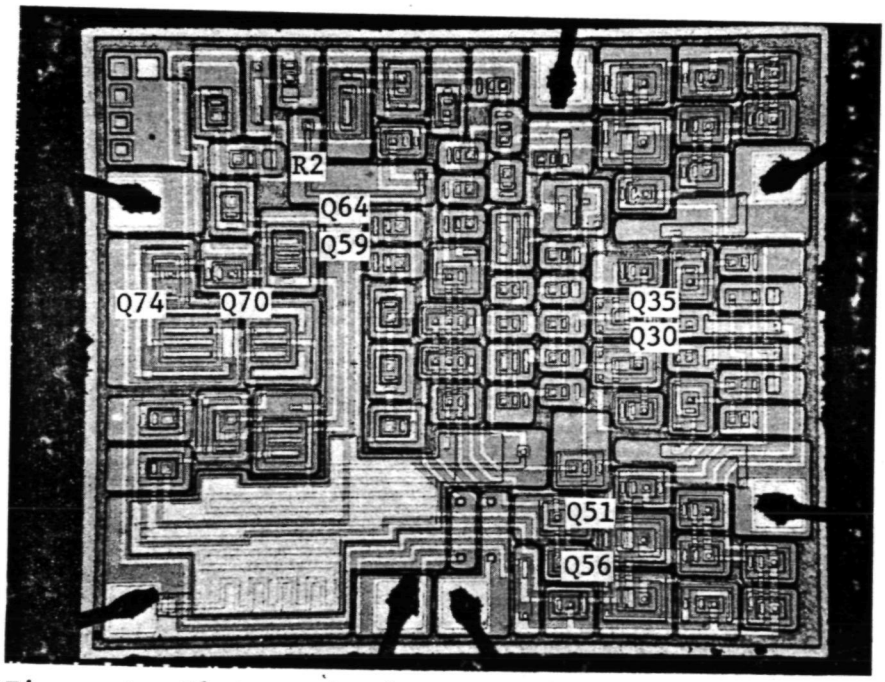

Figure 4. Photograph of HA2700 Identifying Transistor and Resistor Locations, (X60)

Table 11. Irradiation Degradation Data

Circuit 54L00 E_B = 20 kV $I_B = 1 \times 10^{-10}$A, All Terminals at Ground

Transistor	Initial Beta	Post Beta	Δ, %	I_C	V_CE, V	Exposure Magnification	Irradiation Time, sec	Fluence, e/cm^2
Q2 Circuit 1	40	15,6	-61	150 μA	1	X1200	60	4.3×10^{14}
Q2 Circuit 2	40	11.3	-72	150 μA	1	X1200	500	3.6×10^{15}
Q2 Circuit 3	39	11.5	-70	150 μA	1	X2000	240	5.2×10^{15}
Q2 Circuit 4	39	17.5	-55	150 μA	1	X 370	500	3.5×10^{14}
Q4 Circuit 4	26	14	-46	2 ma	1	X 370	500	3.5×10^{14}

Circuit G116 E_B = 20 kV $I_B = 1 \times 10^{-10}$A

FET	Initial V_{GDth}	Post V_{GDth}	Δ, %	Irradiation V_{GD}, V	I_D	Exposure Magnification	Irradiation Time, sec	Fluence, e/cm^2
Q1	-5.34	-6.56	23	-5.8	10 μA	X340	8	4.5×10^{12}
Q2	-5.36	-6.95	30	0	10 μA	X340	45	2.5×10^{13}
Q3	-5.38	-6.93	29	0	10 μA	X340	30	1.7×10^{13}
Q4	-5.42	-6.34	17	-6.0	10 μA	X340	8	4.5×10^{12}
Q5	Used for setup.							

Circuit LM111 E_B = 20 kV $I_B = 1 \times 10^{-10}$A All Terminals at Ground

Transistor	Initial Beta	Post Beta	Δ, %	I_C	V_{CE}, V	Exposure Magnification	Irradiation Time, sec	Fluence, e/cm^2
Q15 NPN	15.6	11.1	-29	25 ma	1	X100	90	5.1×10^{12}
Q8 NPN	86.7	60	-31	500 μA	1	X840	24	2.1×10^{13}*
Q21 NPN	15	1.6	-89	400 μA	1	X840	40	1.5×10^{14}
Q1 PNP	250	85	-66	100 μA	1	X640	20	4.1×10^{13}
Q2 PNP	250	55	-78	100 μA	1	X640	90	1.9×10^{14}
								*$I_B = 2.3 \times 10^{-11}$A

Circuit HA2700 E_B = 20 kV $I_B = 1 \times 10^{-10}$A All Terminals at Ground

Transistor	Initial Beta	Post Beta	Δ, %	I_C	V_{CE}, V	Exposure Magnification	Irradiation Time, sec	Fluence, e/cm^2
Q35 NPN	263	44	-83	100 μA	1	X1000	60	3.5×10^{14}
Q30 NPN	275	38	-86	100 μA	1	X1000	120	7.0×10^{14}
Q56 PNP	120	19	-84	200 μA	1	X 620	60	2.0×10^{14}
Q51 PNP	123	17	-86	200 μA	1	X 620	120	3.9×10^{14}
Q59 NPN	285	68	-76	250 μA	1	X 800	60	2.0×10^{14}
Q64 NPN	288	63	-78	250 μA	1	X 800	120	4.0×10^{14}
R2	(5KΩ)	(5KΩ)	0	250 μA	-	X 500	120	1.5×10^{14}
Q70 NPN	293	94	-68	800 μA	1	X 460	120	1.3×10^{14}
Q74 PNP	142	24	-83	400 μA	1	X 460	120	1.3×10^{14}

The irradiation damage data were reviewed with NASA-MSFC. It was requested that the annealing of irradiated circuits be further investigated. Approval was given to redirect the objective of the study from production screening applications to failure analysis and production sampling applications.

The literature was reviewed to obtain estimates for irradiation damage anneal time and temperature. Simons *et al.* (Ref 15) reported that positive charge in SiO_2 on MOS devices could usually be completely removed by annealing at 300°C for 5 or 10 minutes. Snow *et al.* (Ref 12) reported complete annealing at 300°C for a period greater than 5 minutes.

A test program was developed to better approximate the anneal time and temperature to be used for the irradiated integrated circuits. Small signal PNP bipolar transistors (2N2907) were used for these tests. The DC electrical parameters were used as damage and anneal indicators for these tests. These electrical parameters were measured initially, following irradiation, and after each anneal period. All betas were measured with V_{CE} = -10 V. Delta percentages for betas were calculated as posttest to pretest values. A control device was used to track equipment variations. Irradiation was performed with E_B = 20 kV and $I_B = 1 \times 10^{-10}$A. The annealing chamber was purged with dry nitrogen to reduce oxidation and contamination. The first anneal was conducted at 200°C, and Table 12 shows the test data. The electron fluence levels are listed in the right-hand column. The values for beta and percentage of change were rounded off to nearest whole number.

These test data show that junction leakage, collector base breakdown, and V_{BE} saturation voltages increased due to irradiation. Transistor beta showed very significant decreases. The anneal response rate to high-temperature bake appears to be exponential as was the irradiation damage developed previously. The data show very good agreement between devices for beta recovery by percentile.

A second test was conducted under the same conditions as the previous test with three exceptions. The test cell consisted of four transistors rather than three. The fourth device was the same generic type; however, the die was glass passivated. Second, the anneal temperature for this test was 280°C. Third, a transistor beta measurement was made for a 10 µA collector current. This is not a specified parameter for this part but it provided a more sensitive degradation and anneal indicator. Table 13 shows the test data results for the 280°C anneal.

Table 12. 200°C Anneal Data (20 kV)

S/N	I_{CBO} V_{CB} = -50 V (na)	I_{EBO} V_{EB} = -3.5 V (na)	BV_{CBO} I_C = 10 μA (V)	BV_{EBO} I_E = 10 μA (V)	h_{fe_1} I_C = 100 μA	Δ, %	h_{fe_2} I_C = 1 ma	Δ, %	h_{fe_3} I_C = 10 ma	Δ, %	h_{fe_4} I_C = 150 ma	Δ, %	$V_{BE\ SAT}$ (V) I_C = 150 ma I_B = 15 ma	$V_{CE\ SAT}$ (V) I_C = 150 ma I_B = 15 ma	Notes
11478	7.8	0.00	91.5	6.8	135		142		148		125		0.134	0.879	Initial Data
	9.1	0.69	106	6.8	16	-88	35	-75	62	-58	68	-46	0.155	0.870	2.6 x 10^{13} e/cm^2
	7.8	0.00	95.2	6.8	90	-33	109	-23	123	-17	110	-12	0.137	0.877	Post 20 hr
	11.8	0.00	94.3	6.8	101	-25	116	-18	128	-14	112	-10	0.134	0.878	Post 44 hr
	6.7	0.00	93.9	6.8	108	-20	122	-14	132	-11	114	- 9	0.133	0.876	Post 138 hr
	7.0	0.00	93.8	6.8	111	-18	124	-13	134	-10	115	- 8	0.135	0.876	Post 208 hr
	8.7	0.01	93.5	6.8	110	-19	123	-13	133	-10	114	- 9	0.149	0.888	Post 301 hr
11486	0.03	0.01	88.4	6.6	158		165		169		140		0.124	0.893	Initial Data
	1.0	0.02	94.2	6.6	29	-82	57	-66	89	-47	87	-38	0.134	0.884	2.0 x 10^{13} e/cm^2
	0.21	0.01	94.0	6.6	106	-33	126	-24	141	-17	122	-13	0.129	0.908	Post 20 hr
	0.13	0.06	92.9	6.6	117	-26	134	-19	147	-13	125	-11	0.128	0.945	Post 44 hr
	0.08	0.01	91.9	6.6	122	-23	137	-17	148	-123	125	-11	0.129	0.905	Post 138 hr
	0.02	0.00	91.9	6.6	126	-20	141	-15	151	-11	128	- 9	0.133	0.971	Post 208 hr
	0.20	0.04	91.4	6.6	124	-22	138	-16	149	-12	125	-11	0.169	0.942	Post 301 hr
12717	0.21	0.03	89.6	6.9	158		175		187		155		0.133	0.881	Initial Data
	0.62	0.07	96.7	6.9	60	-62	95	-46	128	-32	120	-23	0.138	0.878	5.8 x 10^{12} e/cm^2
	0.60	0.04	90.5	6.9	116	-27	140	-20	159	-15	138	-11	0.135	0.969	Post 20 hr
	0.25	0.05	89.1	6.9	122	-23	145	-17	163	-13	139	-10	0.139	0.937	Post 44 hr
	0.33	0.03	88.8	6.9	129	-18	150	-14	167	-11	142	- 8	0.151	0.923	Post 138 hr
	0.22	0.00	88.7	6.9	131	-17	152	-13	168	-10	143	- 8	0.132	0.908	Post 208 hr
	0.40	0.04	88.2	6.9	130	-17	150	-14	167	-11	141	- 9	0.139	0.931	Post 301 hr
Control Sample															
11475	0.00	0.00	95.1	6.8	181		194		203		162		0.142	0.876	Initial Data
	0.03	0.01	94.9	6.8	176		190		199		160		0.136	0.878	20-hr Point
	0.06	0.02	94.9	6.8	174		189		198		158		0.136	0.876	44-hr Point
	0.01	0.02	95.0	6.8	172		188		197		158		0.136	0.876	138-hr Point
	0.00	0.00	95.1	6.8	173		189		199		158		0.138	0.875	208-hr Point
	0.05	0.01	95.1	6.8	171		187		196		157		0.146	0.883	301-hr Point

Table 13. 280°C Anneal Data (20 kV)

S/N	I_{CBO} V_{CB} = -50 V (na)	I_{EBO} V_{EB} = - 3.5 V (na)	BV_{CBO} I_C = 10 µA (V)	BV_{EBO} I_E = 10 µA (V)	h_{fe_0} I_C = 10 µA	Δ, %	h_{fe_1} I_C = 100 µA	Δ, %	h_{fe_2} I_C = 1 ma	Δ, %	h_{fe_3} I_C = 10 ma	Δ, %	h_{fe_4} I_C = 150 ma	Δ, %	$V_{BE\ SAT}$ (V) I_C = 150 ma I_B = 15 ma	$V_{CE\ SAT}$ (V) I_C = 150 ma I_B = 15 ma	Notes
11474	0.07	0.00	86.9	6.9	157		167		180		192		160		0.132	0.873	Initial Data
	2.3	0.23	97.7	6.9	21	-87	41	-76	74	-59	109	-43	109	-32	0.144	0.865	2.0 x 10^{13} e/cm^2
	0.23	0.01	88.9	6.9	121	-23	138	-17	158	-12	175	- 9	148	- 8	0.131	0.872	Post 30 min
	0.30	0.00	87.9	6.9	129	-18	143	-14	162	-10	179	- 7	151	- 6	0.131	0.875	Post 2.5 hr
12925	0.03	0.00	91.7	6.8	133		142		154		162		136		0.145	0.878	Initial Data
	3.1	0.27	98.6	6.8	17	-87	33	-77	61	-60	93	-43	89	-35	0.152	0.868	2.0 x 10^{13} e/cm^2
	0.24	0.03	91.1	6.8	112	-16	124	-13	140	- 9	151	- 7	128	- 6	0.139	0.874	Post 30 min
	0.20	0.01	89.7	6.8	120	-10	130	- 9	143	- 7	154	- 5	129	- 5	0.138	0.878	Post 2.5 hr
12926	0.00	0.00	98.6	6.9	166		186		207		219		174		0.141	0.880	Initial Data
	1.4	0.19	104	6.9	21	-88	42	-77	80	-61	123	-44	120	-31	0.151	0.872	2.0 x 10^{13} e/cm^2
	0.23	0.03	93.8	6.9	133	-20	157	-16	182	-12	199	- 9	161	- 8	0.150	0.878	Post 30 min
	0.43	0.03	92.7	6.9	148	-11	168	-10	191	- 7	206	- 6	164	- 6	0.139	0.882	Post 2.5 hr
10	0.35	0.06	128	7.2	128		156		187		216		194		0.181	0.878	Initial Data
	1.4	0.15	132	7.2	42	-67	76	-52	123	-34	169	-22	165	-15	0.232	0.927	2.0 x 10^{13} e/cm^2
	0.53	0.10	131	7.2	131	2	160	3	192	3	219	1	170	-12	0.212	0.918	Post 30 min
	0.34	0.09	130	7.2	128	0	158	1	189	1	216	0	196	1	0.185	0.897	Post 2.5 hr
Control Sample																	
12922	0.00	0.00	97.5	6.8	132		145		159		169		140		0.129	0.876	Initial Data
	0.07	0.06	97.8	6.8	130		144		160		169		140		0.141	0.874	30-min Point
	0.05	0.03	97.6	6.8	127		141		157		168		138		0.130	0.877	2.5-hr Point

These test data show an irradiation response that was similar to the transistors in the previous test. However, the anneal response was more rapid and the recovery was greater. The data for transistor S/N 10, which contained a glass passivated die, showed complete recovery including h_{fe0}. This is significant as the majority of the integrated circuits that were irradiated were also glass passivated. The glass passivation itself does not improve the radiation hardness of a device. It only serves to increase the material thickness above the Si/SiO_2 interface. This results in reducing the electron range with respect to the interface. Therefore, the energy dissipated in the thermal SiO_2 is decreased for the same acceleration voltage.

A third radiation damage test was conducted to demonstrate the effects of a lower acceleration voltage. All test conditions were the same as in the two previous tests except that the acceleration voltage used was E_B = 5.0 kV. The anneal temperature was the same as Test 2, 280°C. Two of the three test transistors contained glass passivated die. The results of these tests are shown in Table 14.

These test data show the significance of decreasing the electron acceleration voltage. These data represent much longer electron beam exposure periods. S/N 11485 and 11 exposures were 9 minutes each and S/N 12 was 1 hr. The importance of this test will be addressed later in the Voltage Contrast Applications section.

Based on the data obtained from these tests, the irradiation damage anneal response for the integrated circuits was evaluated at 280°C. Before anneal, the integrated circuit transistor parameters were remeasured. Approximately 3-1/2 months had passed since these devices had been irradiated and parameters measured. During this period, the devices were stored at room temperature. Measurement at this point provides an assessment of the recovery and a reference for the anneal response. All delta percentages were calculated with reference to the initial measurement. Following parameter measurement the circuits were baked at 280°C for 1 hr in a nitrogen ambient. The parameters were remeasured, and deltas were calculated. The data for these tests are shown in Table 15.

The percentage of residual degradation for 3-1/2 months storage at room temperature and the 280°C anneal were as follows:

Table 14. 280°C Anneal Data (5 kV)

S/N	I_{CBO} V_{CB} = −50 V (nA)	I_{EBO} V_{EB} = −3.5 V (nA)	BV_{CBO} I_C = 10 μA (V)	BV_{EBO} I_E = 10 μA (V)	h_{fe_0} I_C = 10 μA	Δ, %	h_{fe_1} I_C = 100 μA	Δ, %	h_{fe_2} I_C = 1 ma	Δ, %	h_{fe_3} I_C = 10 ma	Δ, %	h_{fe_4} I_C = 150 ma	Δ, %	$V_{BE\ SAT}$ (V) I_C = 150 ma I_B = 15 ma	$V_{CE\ SAT}$ (V) I_C = 150 ma I_B = 15 ma	Notes
11485	0.01	0.00	88.6	6.8	142		144		152		159		133		0.143	0.879	Initial Data
	0.41	0.04	89.2	6.8	137	-4	141	-2	149	-2	156	-2	130	-2	0.150	0.876	4.6×10^{13} e/cm^2
	0.16	0.01	93.1	6.8	146	3	147	2	155	2	161	1	133	0	0.138	0.879	Post 30 min
	0.25	0.01	92.5	6.8	146	3	146	1	154	1	159	0	133	0	0.139	0.885	Post 2.5 hr
11	0.46	0.14	92	7.4	100		134		175		217		209		0.139	0.870	Initial Data
	1.0	0.16	91.9	7.4	103	3	137	2	178	2	217	0	207	-1	0.134	0.861	4.6×10^{13} e/cm^2
	1.0	0.12	92	7.4	103	3	137	2	177	1	217	0	207	-1	0.134	0.863	Post 30 min
	0.64	0.15	92	7.4	103	3	137	2	177	1	215	-1	205	-2	0.132	0.865	Post 2.5 hr
12	0.30	0.10	127	7.1	136		164		197		227		204		0.168	0.875	Initial Data
	0.35	0.11	127	7.1	125	-1	165	1	198	1	224	-1	200	-2	0.164	0.869	3.1×10^{14} e/cm^2
	No High Temperature Anneal																
Control Sample																	
12922	0.00	0.00	97.5	6.8	132		145		159		169		140		0.129	0.876	Initial Data
	0.07	0.06	97.8	6.8	130		144		160		169		140		0.141	0.874	30-min Point
	0.05	0.03	97.6	6.8	127		141		157		168		138		0.130	0.877	2.5-hr Point

Table 15. Irradiation Damage Anneal Data

Circuit 54L00 $Beta_{Q2}$ I_C = 150 ma, V_{CE} = kV $Beta_{Q4}$ I_C = 2 ma, V_{CE} = 1 V

Transistor	Initial Beta	Post Irradiation	Fluence, e/cm^2	Δ, %	Post 3.5 Months at 25°C	Δ, %	Post 1 hr at 280°C	Δ, %
Q2 Circuit 1	40	15.6	4.3×10^{14}	-61	16.7	-58	45	13
Q2 Circuit 2	40	11.3	3.6×10^{15}	-72	14.4	-64	45	13
Q2 Circuit 3	39	11.5	5.2×10^{15}	-70	14.5	-63	42.5	10
Q2 Circuit 4	39	17.5	3.5×10^{14}	-55	19.4	-50	45	16
Q4 Circuit 4	26	14	3.5×10^{14}	-46	15	-42	27	4

Circuit G116 V_{GDth} at I_D = 10 μA

Fet	Initial V_{GDth}	Post Irradiation	Fluence, e/cm^2	Δ, %	Post 3.5 Months at 25°C	Δ, %	Post 1 hr at 280°C	Δ, %
Q1	-5.34	-6.56	4.5×10^{12}	23	-6.54	23	-5.64	- 6
Q2	-5.36	-6.95	2.5×10^{13}	30	-6.95	30	-5.32	1
Q3	-5.38	-6.93	1.7×10^{13}	29	-6.94	29	-5.97	-11
Q4	-5.41	-6.34	4.5×10^{12}	17	-6.33	17	-5.74	3

Circuit LM 111

Transistor	Initial Beta	I_C	Post Irradiation	Fluence, e/cm^2	Δ, %	Post 3.5 Months at 25°C	Δ, %	Post 1 hr at 280°C	Δ, %
Q15 NPN	15.6	25 ma	11.1	5.1×10^{12}	-29	12.8	-18	15.8	1.3
Q8 NPN	86.7	500 μA	60	2.1×10^{13}	-31	65	-25	85	-2
Q21 NPN	3	400 μA	1.6	1.5×10^{14}	-47	1.6	-47	1.8	-40
Q1 NPN	250	100 μA	85	4.1×10^{13}	-66	85	-66	115	-54
Q2 PNP	250	100 μA	55	1.9×10^{14}	-78	58	-77	125	-50

Circuit HA2700

Transistor	Initial Beta	I_C	Post Irradiation	Fluence, e/cm^2	Δ, %	Post 3.5 Months at 25°C	Δ, %	Post 1 hr at 280°C	Δ, %
Q35 NPN	263	100 μA	44	3.5×10^{14}	-83	63	-76	225	-15
Q30 NPN	275	100 μA	38	7.0×10^{14}	-86	57	-79	225	-18
Q56 PNP	120	200 μA	19	2.0×10^{14}	-84	24	-80	110	- 8
Q51 PNP	123	200 μA	17	3.9×10^{14}	-86	21	-83	109	-11
Q59 NPN	285	250 μA	68	2.0×10^{14}	-76	85	-70	254	-11
Q64 NPN	288	250 μA	63	4.0×10^{14}	-78	78	-73	250	-13
Q70 NPN	293	800 μA	94	1.3×10^{14}	-68	110	-63	273	- 7
Q74 PNP	142	400 μA	24	1.3×10^{14}	-83	30	-79	133	- 6

Circuit	Recovery* 25°C 3.5 Months	Recovery† 280°C 1 Hr
54L00	3 to 8%	Complete
G116	0%	-11 to 0%
LM 111	0 to 11%	-54 to 0%
HA2700	3 to 7%	-18 to -6%

*Percentage of parameter improvement from post irradiation to preanneal.

†Percentage of parameter improvement from initial measurement (prior to irradiation) to post anneal.

The integrated circuit transistors that showed the poorest recovery were those that had the highest betas. A transistor with high beta at low collector current is very sensitive to surface states. Therefore, it would be expected to recover more slowly and require a greater degree of damage annealing. From these data, it is estimated that for complete recovery, a 1-hr bake at 325 to 350°C would be required. This is considered to be an unacceptable exposure for assembled and unsealed production circuits.

1. Summary

At the beginning of this study, a number of questions were raised regarding the degradation of transistor parameters from electron beam radiation. The degradation of transistor beta for relatively brief SEM exposure times was severe. Degradations as high as 85% were realized for some low collector current betas. The rate of degradation is exponential with the larger amount of damage occurring within the first 5 to 10 sec of exposure. The majority of the dc parameters measured for the 2N2907 exhibited some change as a result of irradiation. The parameter most sensitive was beta and particularly at the lower collector currents.

Between the MOS and bipolar devices evaluated in these tests, the bipolar was found to be the most susceptible to damage and more difficult to anneal. However, from a functional circuit point of view it is dependent on circuit design margins. In some bipolar integrated circuits a transistor can experience 50 to 80% loss in beta and still function over a limited temperature range. This is more frequent in the case with digital circuits than with analog circuits. A small percentage of change in the gate threshold voltage would generally result in functional failure of the circuit. The electron fluence levels in this study should be considered lower than typical for any high magnification SEM applications. The highest magnification used during irradiation was X2000. The irradiation damage was found to be quite stable at room temperature. The temperature required to anneal the damage is above 300°C.

The exposure of an assembled device to this temperature could result in a severe reduction in reliable performance. The question of parameter stability after an irradiation damage anneal must be further evaluated.

A question that remains to be answered is what is the damage mechanism? There is a good possibility that electrical degradation is the result of atomic displacement which occurs by the Varley mechanism. Further study is needed to better understand this damage mechanism in SiO_2 and Si_3N_4 films for low energy electrons (10 to 100 keV).

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B. CONTAMINATION

Before considering SEM screening of production semiconductor devices, the effect of surface contamination on reliability must be evaluated. Related literature was reviewed to obtain a qualitative viewpoint regarding the characteristic of the contamination. Some of the questions that resulted were: What is a typical film formation rate? Will it result in electrical leakage? How can the contamination rate be reduced? Can the contamination be removed?

Generally, the concern for specimen surface contamination has been its effect on reducing secondary electron yield (Ref 1) and image resolution (Ref 2 and 3). No references were found that recommended or suggested the use of a SEM for screening production semiconductors.

There are many sources from which the contamination may originate. A primary source in an oil-pumped vacuum system is the roughing and diffusion pump oil. Other sources are O-ring grease, stage lubricants, contamination on internal surfaces of the specimen chamber, specimen attachment adhesive and conductive paint outgassing and residual films on the specimen surface. Some of these sources are intrinsic to the instrument and others are dependent on maintenance and procedural practices. Oil vapor from vacuum pumps in an oil-pumped vacuum system can be reduced by foreline and cold traps, or simply eliminated by the substitution of an ion pumped vacuum system. However, many of the other sources common to the specimen chamber remain. Contaminants form by molecular deposition or condensation on exposed surfaces in the specimen chamber. The rate of deposition or condensation is related to the vacuum pressure at the specimen surface. For a pressure of 10^{-6} torr, a monolayer of contamination can form over a period of a few minutes. Other factors related to the rate of formation such as the type of diffusion pump oil used (Ref 4) type of specimen, the temperature of the specimen and the hydracarbon partial pressure. Electron Beam bombardment results in the polymerization of the deposited film. As the contamination film continues to form, it is also polymerized by the beam.

Conru and Laberge (Ref 4) studied the hydracarbon contamination rate in a SEM. A method is described for measuring contamination rates in a SEM. A focused beam generates a cone of contamination and the cone volume to beam exposure time yields a contamination rate. They reported this volumetric formation rate of polymerized oil was approximately linear with time for a specific beam current. The rates reported were: 1.6×10^{-16} cm^3/sec for $I_B = 4 \times 10^{-10}$A, 3.8×10^{-16} cm^3/sec for $I_B = 5 \times 10^{-12}$A and 5.3×10^{-16} cm^3/sec for $I_B = 2.5 \times 10^{-11}$A. The highest rate occurred at an $I_B = 2.5 \times 10^{-11}$A. The vacuum pressure for these rates was reported to be less than 10^{-6} torr.

This method (Ref 4) was used to measure hydracarbon deposition rates for this study. The worst-case rate was measured at minimum pump downtime and worst-case vacuum pressure of 1×10^{-5} torr. The beam voltage was 20 kV, beam current was 1×10^{-10}A and exposure time was 3 minutes. The vacuum system had a foreline trap and the LN_2 cold trap was not charged. The deposition volume for the 180-sec period was calculated to be 125×10^{-15} cm^3 or 6.9×10^{-16} cm /sec (see Figure 5). This rate is slightly higher than the worst case reported by Conru and Laberge (Ref 4) of 5.3×10^{-16} cm^3/sec for $I_B = 2.5 \times 10^{-11}$A. Using 6.9×10^{-16} cm^3/sec and

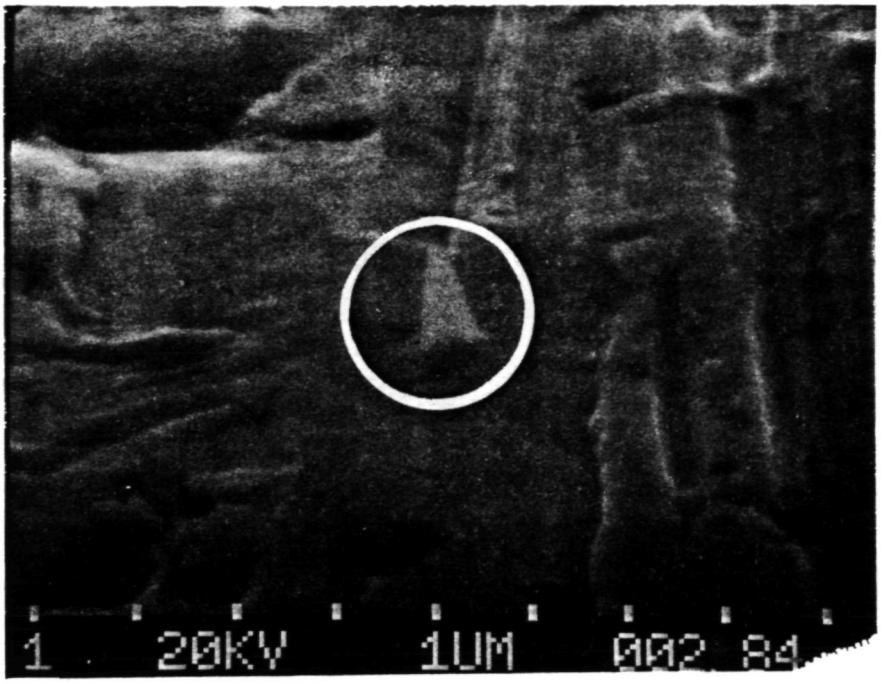

Figure 5. SE Micrograph Showing the Cone of Contamination (Circle) E_B = 20 kV, I_B = 1 x 10^{-10}A x 14000)

assuming a constant volume deposition rate, film thicknesses were calculated for scan magnifications of X1000 and X10,000. A 5-minute exposure at X1000 would result in an average film thickness of 0.2 Å over an area of 11.5 x 10^{-3} cm by 9.0 x 10^{-3} cm; and at X10,000 an average of 20 Å for an area of 11.5 x 10^{-4} cm by 9.0 x 10^{-4} cm.

This contamination rate measurement technique provides a good method for periodically measuring the contamination rate of an instrument and for the evaluation of instrument cleaning or sample preparation procedures. When using this technique, a means of marking the specimen surface should be used to help in locating the hydracarbons cones after coating.

Routine maintenance of the instrument is important in reducing hydracarbon contamination rates. Periodic cleaning of the electron column, specimen chamber and stage help to reduce sources for contamination (Ref 5). The use of dry nitrogen for backfilling the electron column and specimen chamber, when returning them to atmospheric pressure, will reduce surface trapping. Cleanliness of the specimen and care in applying conductive paints and allowing them to completely dry are important factors related to contamination. Maintenance schedules and procedure adequacy can be evaluated through the measurement of contamination rates.

The formation of a hydracarbon film on a semiconductor surface raises a question regarding its reliability. The electrical and chemical stability would be difficult to predict for a film with a multitude of possible chemical and physical combinations. Craig (Ref 6) and Echlin (Ref 5) have analyzed the gas spectra in typical vacuum systems and showed methods for improving the vacuum pressure. Yakowitz *et al.* (Ref 7) reported the deposited films they studied were found to be conductive. The most effective approach to this problem would be to eliminate the contamination. Currently this is impractical because of the evacuation time required to achieve a 10^{-8} to 10^{-9} torr pressure. This would also require an ion-pumped system. Another solution would be to clean the devices following SEM examination. One method that has shown very good results is oxygen plasma cleaning. Our experience to date has involved a limited number of devices from bipolar and MOS technologies with very good success. Further investigation and evaluation is required to establish the quality of cleaning and the effect on an assembled semiconductor device.

1. Summary

With the data available at this time there is nothing to indicate that the contamination is detrimental to semiconductor reliability. At this time it remains a question. There is no data base with which to assess the effect on reliability, and it is too early to determine whether an oxygen plasma or other method can remove the film without adversely affecting the part reliability.

2. Contamination References

1. H. Seiler and M. Stark: "Determination of Mean Free Paths of Secondary Electrons in Polymerised Films." *Z. Phys.*, Vol 183, 1965, pp 527 and 531.

2. O. C. Wells: *Scanning Electron Microscopy*. McGraw-Hill Book Company, New York, 1974, pp 89-94.

3. J. I. Goldstein and H. Yakowitz (Ed): *Practical Scanning Electron Microscopy*. Plenum Press, 1975, p 212.

4. H. W. Conru and P. C. Laberge: "Oil Contamination with the SEM Operated in the Spot Scanning Mode." *Journal of Phys, E.*, Vol 8, 1975, pp 136-138.

5. P. Echlin: "Contamination in the Scanning Electron Microscope." *SEM/1975 Proceedings of the 5th Annual SEM Symposium, IITRI*, Chicago, Ill, 1975, pp 679-686.

6. R. D. Craig: "Improvements in Vacuum Systems." *J. Physics E.*, Vol 3, 1969, pp 338-339.

7. H. Yakowitz *et al.*: "The Cylindrical Secondary Electron Detector As a Voltage Measuring Device in the Scanning Electron Microscope." *SEM/1972 Proceedings of the 5th Annual SEM Symposium, IITRI*. Chicago, Ill., 1972, pp 33-40.

IV. ELECTRON BEAM-INDUCED CURRENT APPLICATION TECHNIQUES

The electron beam-induced current (EBIC) mode of SEM operation is a powerful tool for analyzing and evaluating semiconductor devices. The EBIC mode could very well surpass the secondary electron or surface imaging mode in value for semiconductor applications. EBIC provides the capability for measuring subsurface electrical and physical parameters. These measurements are performed without mechanical damage to the surface.

Earlier, some basics were discussed regarding the electron/solids interaction and the penetration of electrons into the solid. Two basic factors that determine the electron range in solids are the acceleration voltage and the atomic density of the solid. Therefore, a desired range can be preselected based on the material density. If an electron beam strikes the surface of a given thickness of material and the range is sufficient for partial electron penetration, the majority of these electrons can be collected and measured. Figure 6 shows how the number of collected electrons is related to the film thickness. This figure assumes a constant acceleration voltage and a similar atomic density on each side of the detector gate. Electrons that cross the detector gate are measured. The detected electron signal is inversely proportional to the film thickness and depicts the complement of the surface topography. At position "A," no absorbed electrons are measured, at "C" a majority are measured and at "B" and "D" a portion are measured. A visual interpretation of the detected signal will provide a qualitative assessment of the surface topography, and measurement of the detected electrons, in conjunction with a calculated range, can provide a quantitative assessment of the film thickness. To better understand how this can be accomplished, the mechanics of electron penetration in solids will be reviewed later.

A. TEST DEVICE INTERCONNECT CIRCUITRY

Basic requirements for the interconnect circuitry are 1) low noise pickup, 2) low leakage current, 3) package adaptation flexibility, 4) operation flexibility, and 5) minimal electron beam interference. To reduce noise pickup and leakage current, it is necessary to minimize lead lengths and circuitry external to the specimen chamber; to obtain operational flexibility, it is necessary to make interconnect circuit changes external to the specimen chamber; therefore, the best compromise is to locate the interconnect programming switches at the socket interface.

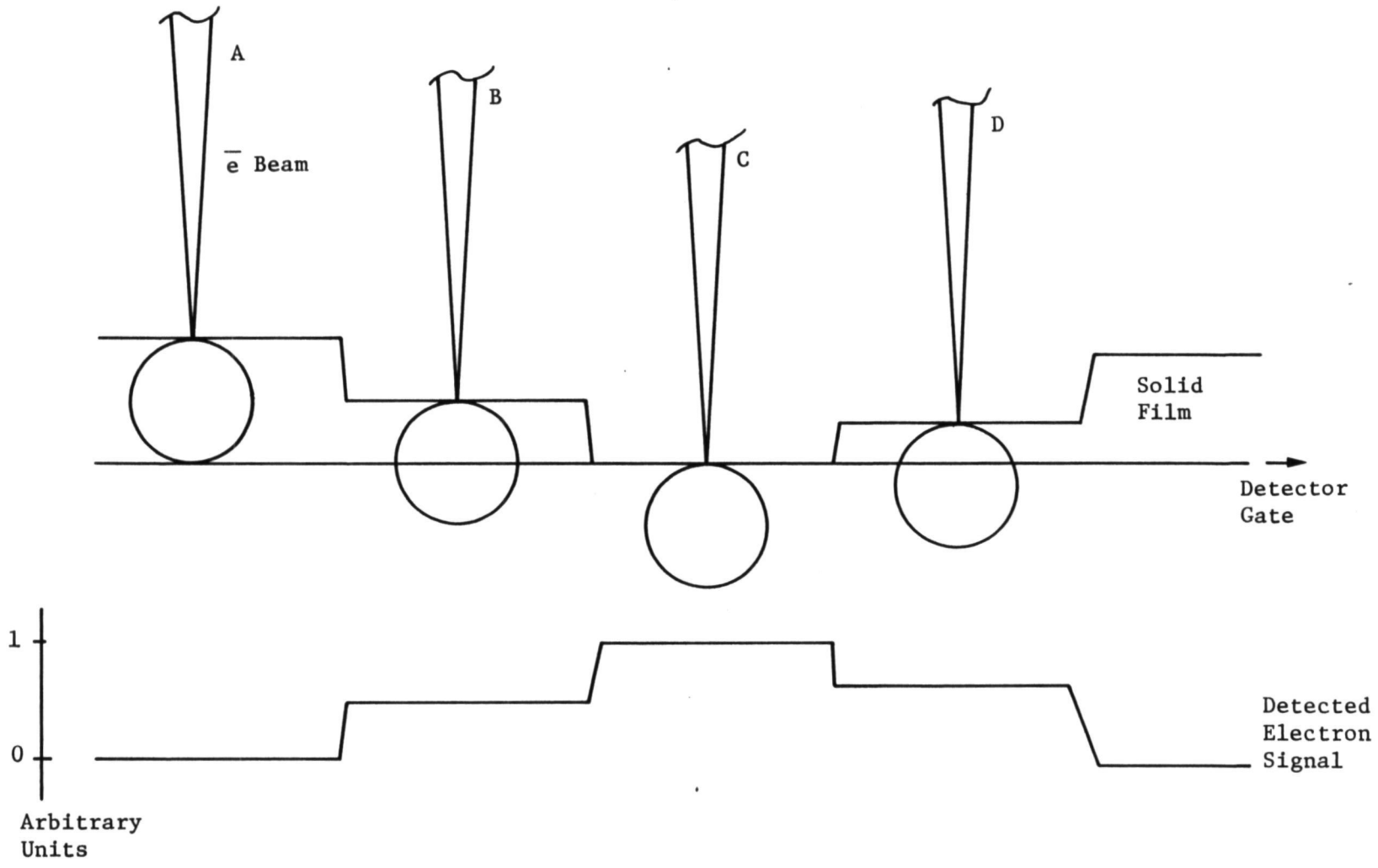

Figure 6. Electron Range as a Function of Film Thickness

The specimen stage contained an 18-pin electrical feedthrough. To increase the number of feedthroughs, a high density 61-pin vacuum rated connector was installed (Fig. 7). These two connectors were wired to connectors internal to the specimen chamber. The internal connectors provide a package adapter disconnect (Fig. 8). Mating connectors, interconnect wires, and a package test socket provide the different adapters needed for various device package styles (Fig. 9 and 10). An effort was made to use plug-in sockets for all device packages; however, a suitable mechanical holder could not be found for flatpack style packages. Until a better technique becomes available, the flatpack devices are tack-soldered to a printed circuit card. Metal shields were used to minimize direct exposure of nonconductive package surfaces to the electron beam. Also, nonconductive surfaces on the adapters were coated with conductive paint. Note: This was more important to voltage contrast interference than EBIC interference. All interconnect wiring between the test adapter and the disconnect socket was shielded with a grounded wire sleeve.

A switch matrix was constructed to be used externally to the chamber and immediately next to the interface connectors. Mechanical DIP switches were used to reduce the switch matrix size. Single-pole single-throw switches were used. The 18-pin connector was used for ground termination switching and the 61-pin connector was used for current amplifier switching (Fig. 11 and 12). If single-pole double-throw DIP switches are available with satisfactory isolation ratings, a complete switch matrix could be constructed on a single connector. The isolation obtained for these switch matrices after assembly, cleaning, and vacuum bake was less than 100 pA at 20 volts per switch channel. Subsequent vacuum baking has not been necessary to maintain this isolation; however, it is recommended that it be examined for each case and especially in high humidity environments. A schematic circuit for the switch matrices is shown in Figure 13.

The same adapters and interface connectors were used for voltage contrast studies. A 60 x 10 crosspoint patch board was used to supply the required signal and supply voltages. The patch board is shown in Figure 14. All interconnecting wires were shielded. Special care should be taken to prevent vibrations from being transmitted along the interconnecting cable to the specimen chamber and electron column. Blowers in equipment mounted in the same cabinet are typically the major sources of vibration.

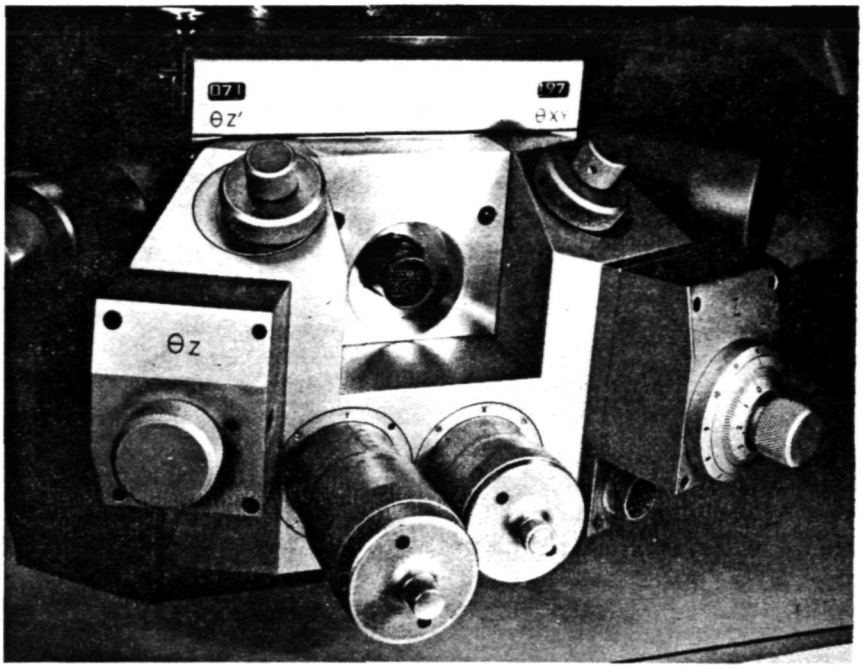

Figure 7. Specimen Stage Showing the External Electrical Feedthrough Connectors.

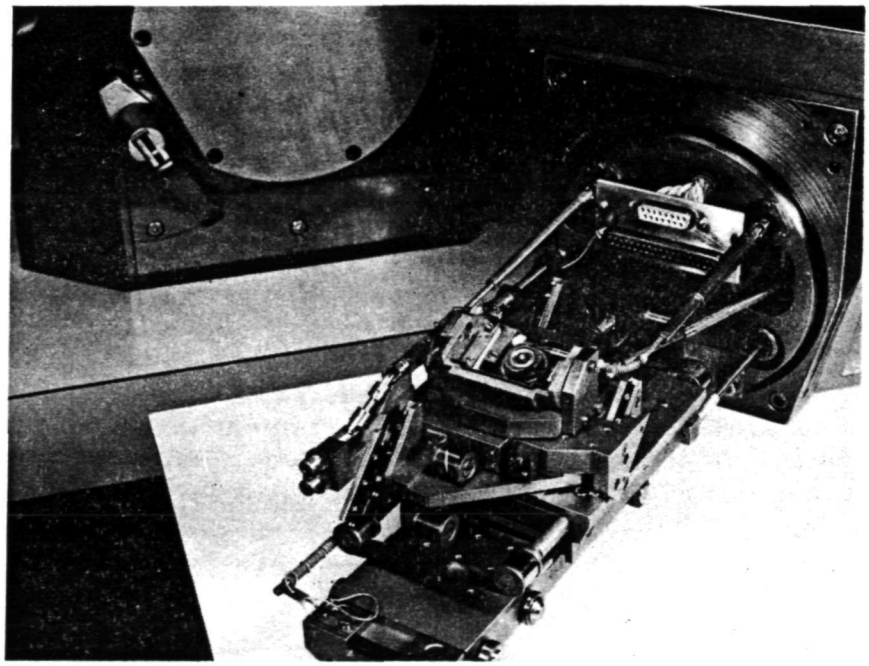

Figure 8. Specimen Stage Showing the Connectors that Provide the Internal Adapter Disconnects.

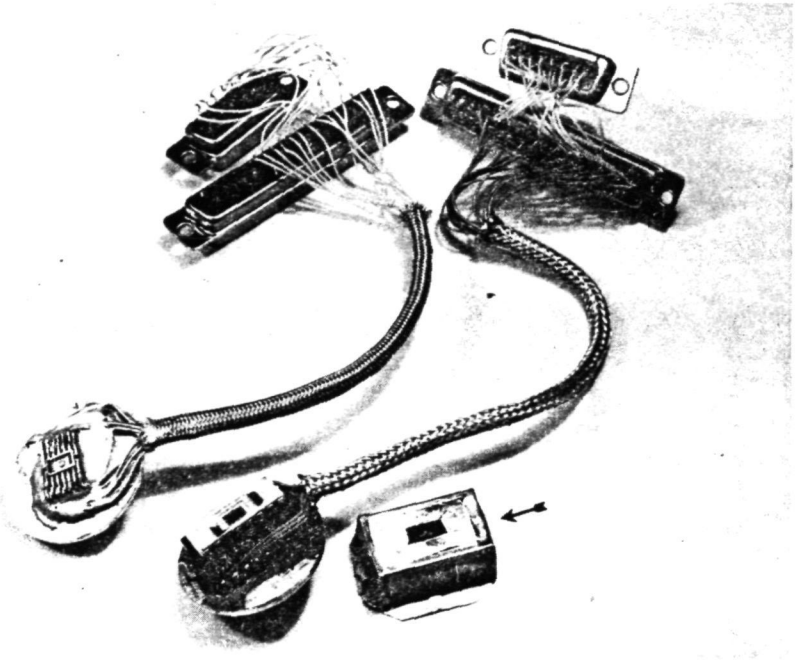

Figure 9. Flat Pack and Dual-in-Line Package Adapters. (This Dual-in-Line Adapter has the Metal Shield Removed [Arrow].)

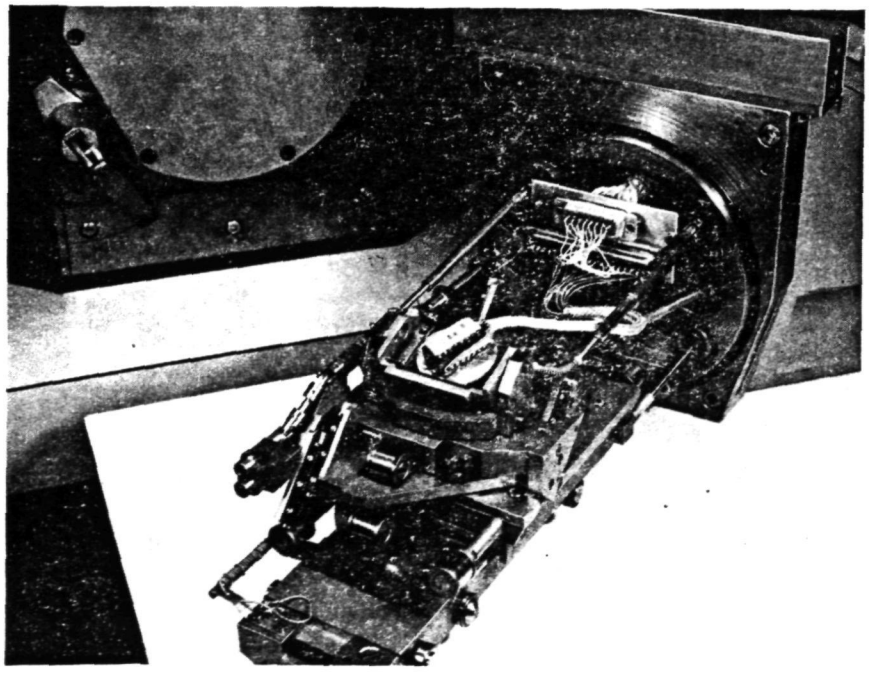

Figure 10. Dual-in-Line Adapter Installed on the Specimen Stage. (The Metal Shield for the Device Package and Test Socket is Not Installed.)

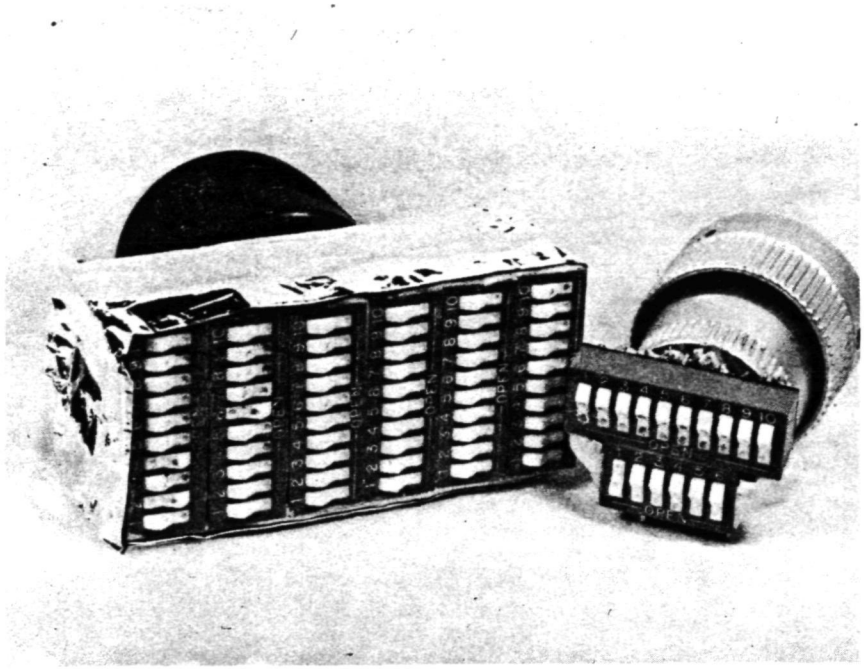

Figure 11. Two Switch Matrices Used for Selecting Device Pin Interconnect Configuration.

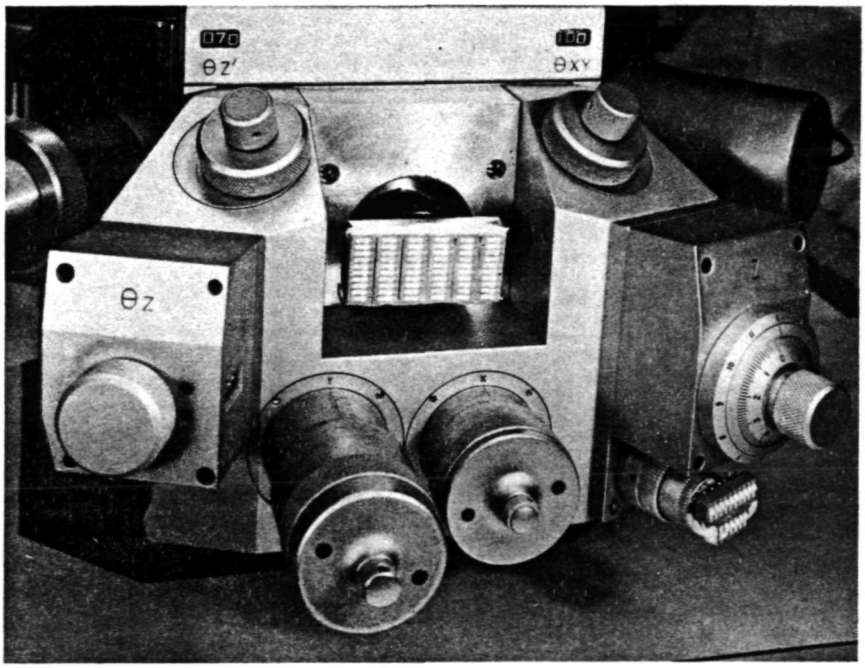

Figure 12. Two Switch Matrices Installed on the Specimen Stage.

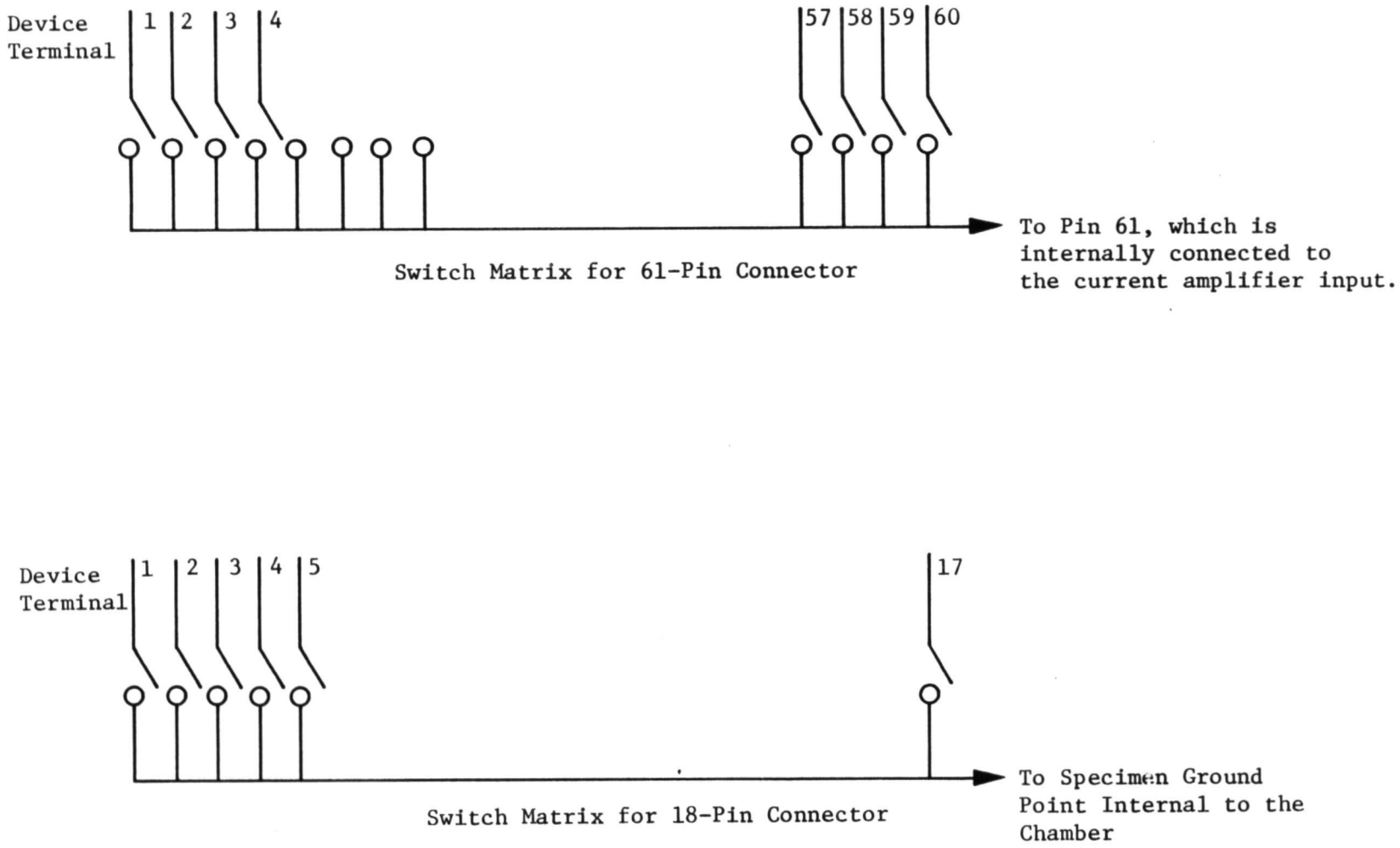

Figure 13. Schematic Circuit for Switch Matrices.

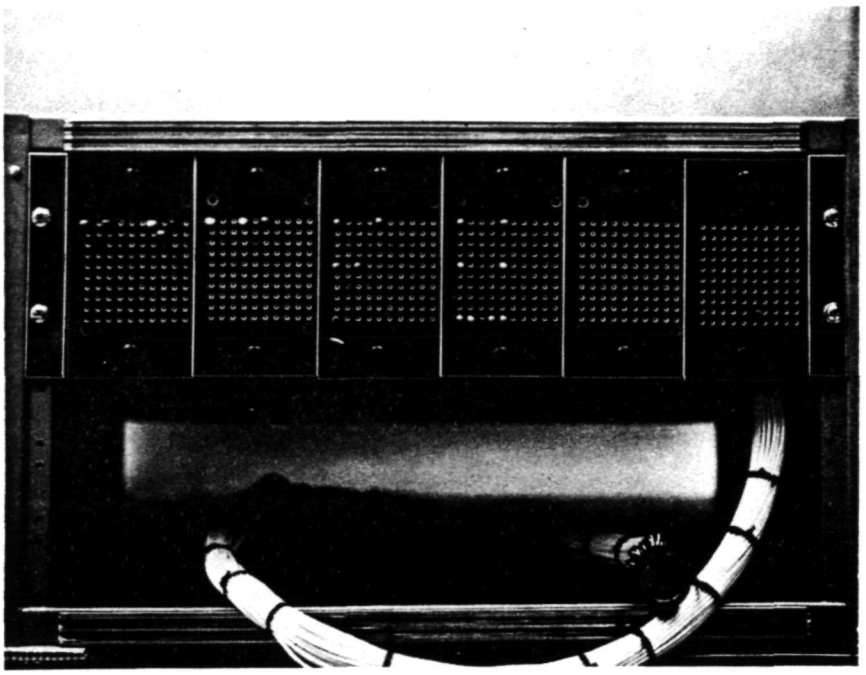

Figure 14. Patch Board and Interconnect Cable

B. RANGE OF ELECTRON PENETRATION IN SOLIDS

The electron interaction and penetration in solids has been an area that has been studied in detail. For those interested in a detailed discussion, a review of the chapters in the reference SEM text books (Ref 1-4) is recommended. Many of the papers identified in the bibliography also will address this subject.

As expressed earlier, the interactions between an electron beam and a solid surface are complex. A wealth of energy spectra are emitted from a specimen surface. Aside from the back scattered electron (BSE) energy, the energy emitted from the surface has little effect on the magnitude of absorbed electron current. The primary electron energy is dissipated by two basic mechanisms, elastic and inelastic electron scattering. Elastic scattering, or a change in electron direction with minimal energy loss, is a result of an interaction between an electron and the nucleous of an atom. Inelastic scattering, or an energy loss with minimal change in direction, results from an interaction between an electron and the nucleous of an atom or an interaction between an electron and an electron of an atom.

Elastic scattering is the primary mechanism for reflecting energy from the specimen surface, and inelastic scattering is the primary mechanism for absorbed current and electron-hole pair current.

The absorbed current in a specimen is the difference between the electron beam current and the specimen reflected current. This current, commonly referred to as sample or specimen current, must have a return to instrument common to prevent sample charge accumulation. A second current induced in the specimen is an electron-hole pair current. Electron-hole pairs are produced in the specimen by inelastic interaction between a primary electron and the valance electron of an atom. An ionizing energy frees the valence electron leaving a hole. A single primary electron can produce 10^4 electron-hole pairs. Electron-hole multiplication is the primary mechanism for absorbed electron energy dissipation. For example, electron-hole generation requires approximately 4 eV. Therefore, a 15 keV electron can generate 3.8×10^3 electron hole pairs. In most semiconductors containing N and P diffusions, the applied or generated fields cause the electrons and holes to flow in opposite directions. Metal atoms in semiconductors produce traps which can severely reduce the recombination current. The electrons or holes that diffuse across a junction will produce an external current. The number of electrons or holes that diffuse across the junction depend on the distance from the point of generation to the junction depletion region and the diffusion length for the diffused region. Diffusion length is the average distance of carrier travel from the point of generation to recombination. The resultant external current flow is typically 10^3 times greater than the primary electron current. It is this electron-hole multiplication current that is used in EBIC applications.

Many theoretical studies and experimental measurements have been conducted to determine the electron range for various elemental materials. Some of these studies evaluated the probabilities for collision, extent of interaction, resultant electron energy loss and change in direction of travel. This is a random interaction mechanism and must be evaluated by probability approximations. Other studies have used experiments in which the degree of electron penetration through various elemental thin films could be measured. Through the evolution of these studies came expressions for deriving the electron range based on these theoretical and experimental data. The electron ranges derived from these expressions do not generally yield the same result. This is due in part to the definition of electron range and the basis from which the expression evolved. Electron range may imply the measurement of the average electron path length, or the practical/extrapolated range as measured from the point of beam incidence on the specimen surface. The measurement of the average path length would yield a greater distance than the average range from beam incidence. (The electron

does not travel in a straight line from the point of incidence). For this study, the electron range as measured from the point of beam incidence is used.

Two equations were selected for calculating the electron ranges for EBIC applications. One equation was derived by Everhart and Hoff (Ref 5), which is based upon energy-dissipation range. The range equation is valid for acceleration voltages of 5 to 25 keV and atomic elements 10 through 15. This would include semiconductors employing aluminum, silicon dioxide, and silicon systems. The equation is:

$$R_G = 4.0\ E_B^{1.75}$$

where E_B is the beam energy in keV and R_G is the range in $\mu g/cm^2$ (ρR). The equation was plotted showing the relationship of electron range in microns and acceleration voltage in keV for Aℓ, Si, and SiO_2 (see Figure 15).

The second equation was derived by Kanaya and Okayama (Ref 6), which is based upon a modified diffusion model. This range equation is valid for acceleration voltages of 10 to 1000 keV for all elements. This would include all semiconductor material and metallization systems. The equation is:

$$\rho R = \frac{2.76\times10^{-11} A\ E_o^{5/3}}{Z^{8/9}} \frac{\left[1 + (0.978\times10^{-6} E_o)\right]^{5/3}}{\left[1 + (1.957\times10^{-6} E_o)\right]^{4/3}}$$

where E_o is the beam energy in eV, A is the atomic weight in g, Z is the atomic number, ρ is the density in g/cm^3 and R is the range in cm. This equation was plotted showing the relationship of electron range in microns and acceleration voltage in keV for Au, Cu, Aℓ, Si, and SiO_2. See Figure 16. These ranges were extrapolated below 10 keV to approximate the electron range for smaller film thicknesses. The extrapolated range may be less than the actual range. From these data an acceleration voltage can be determined that will produce a sufficient electron range to penetrate the oxide and metal films on semiconductors.

These graphs of electron range versus acceleration voltage show the significance of film density on electron range. A comparison (from Kanaya and Okayama) (Ref. 6) of electron range and energy dissipation profiles for Aℓ and Au are shown in Figure 17. This represents the respective ranges for a 15 kV beam voltage. The energy dissipation profile is important in determining average electron range.

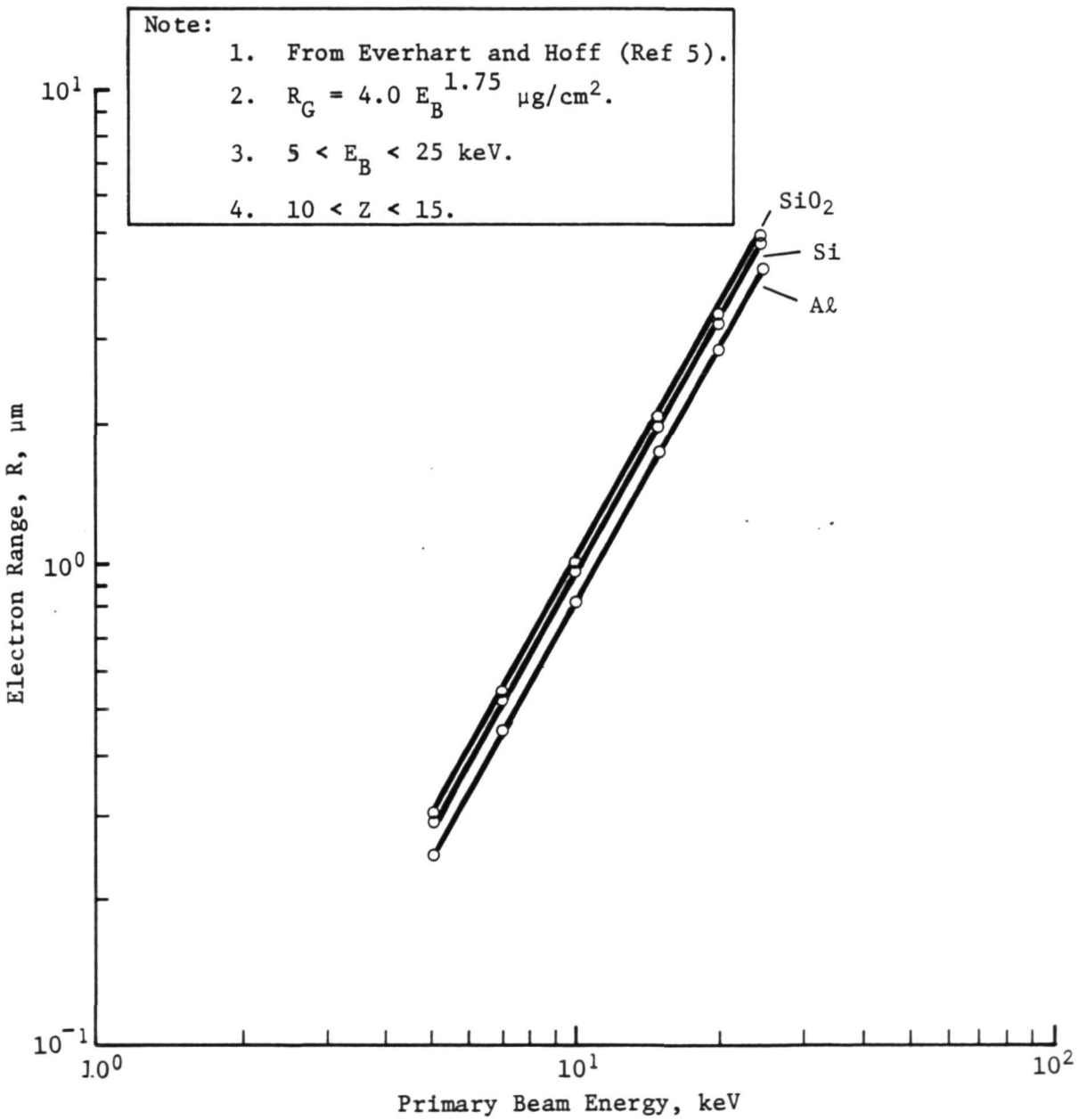

Figure 15. Electron Range (R) Versus Primary Beam Energy

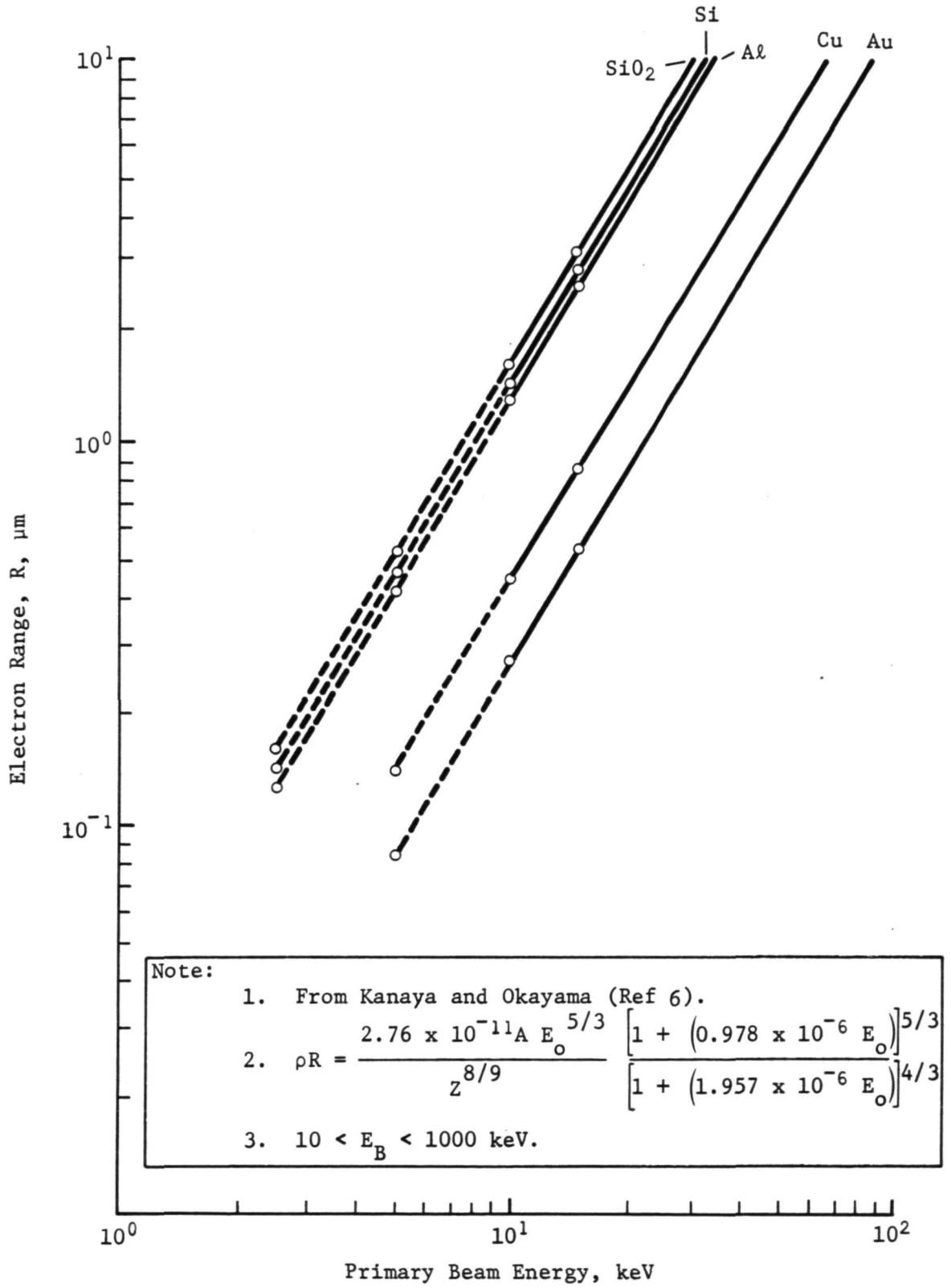

Figure 16. Electron Range (R) Versus Primary Beam Energy

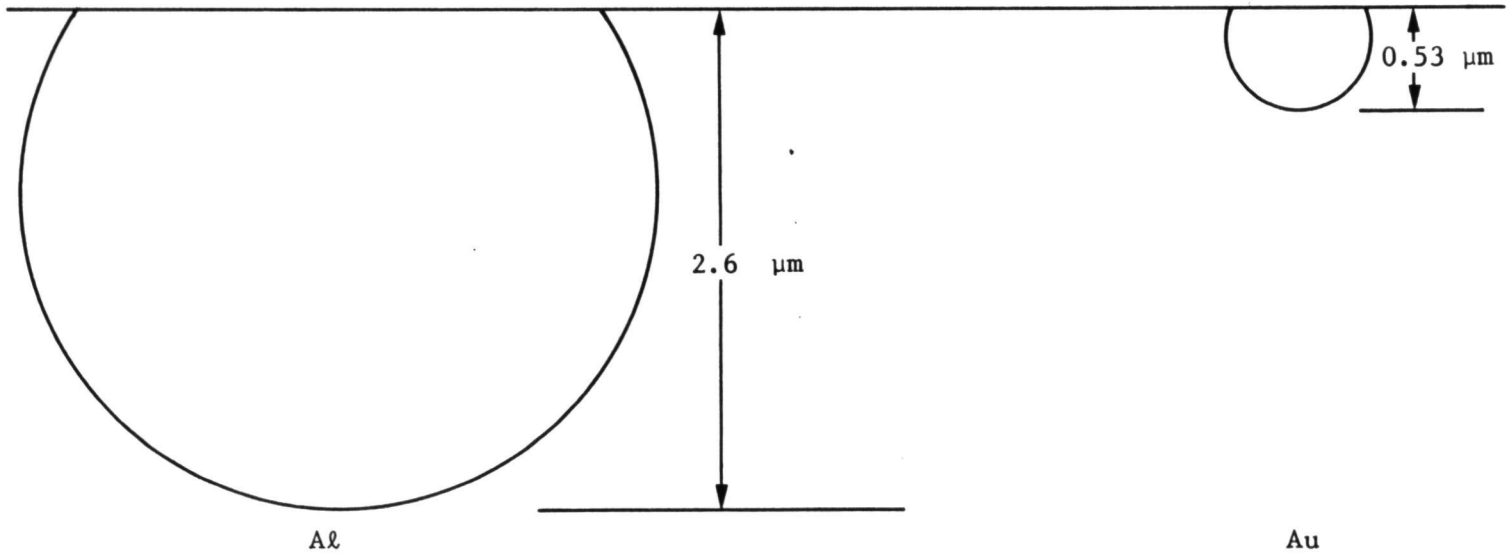

Figure 17. Electron Range and Electron Energy Dissipation for Aluminum and Gold at 15 keV (from Kanaya and Okayama Ref 6)

The application of range data in conjunction with semiconductors provides a quantitative and qualitative analysis capability. This capability is related to surface and junction characteristics in conjunction with the underlying diffusions. The diffusions act as an electron energy analyzer. As discussed earlier, the beam-induced electron-hole multiplication current is the major current for these applications, and the semiconductor provides a unique capability for measuring this current. Figure 18 shows a representative cross section of a PNP transistor. In this example the beam-induced current is measured from the base. The holes (minority carriers) generated in the base, which diffused across the base-emitter or base-collector junction, produce a net increase in electrons. The increase in electrons results in a current flow through the current amplifier input and ground to the respective emitter or collector junction where they recombine with excess holes. The multiplication current flows only when an electron beam generated bias or external reverse bias is applied to at least one junction of the transistor. For example if the emitter and collector were disconnected from ground, the current flow measured at the base would be the absorbed electron beam current. In the example in Figure 18, if the current amplifier were connected to the emitter or collector with the base at ground, the amplifier input polarity would be inverted and the current level would be indicative of the recombination current for the respective junction.

Measuring the beam-induced currents in a discrete transistor is straightforward. When measuring EBIC in integrated circuits the measurement points are not as accessible. Figure 19 shows the schematic circuit for a low power TTL inverter. The transistor junctions that have a resistor or resistors in parallel with the junction produce poor EBIC levels. This is due to the majority of recombination current flowing through the parallel resistance, therefore all junctions are not accessible. When necessary it may be possible to open the parallel reistance circuit by scribing open metalization. Current amplifier input impedances are generally greater than 10 megohms.

EBIC micrographs were made to provide typical examples for a transistor and an integrated circuit. The transistor is a nonglass passivated PNP 2N2905. A secondary electron (SE) micrograph of this device is shown in Figure 20. Figure 21 is a typical EBIC micrograph measured from the base with emitter and collector at ground. This is an intensity-modulated image and the intensity from black to white represents increasing current levels and decreasing surface film thickness. To obtain an accurate image in EBIC, the angle of incidence for the beam should be approximately normal to the surface. The majority of this work was

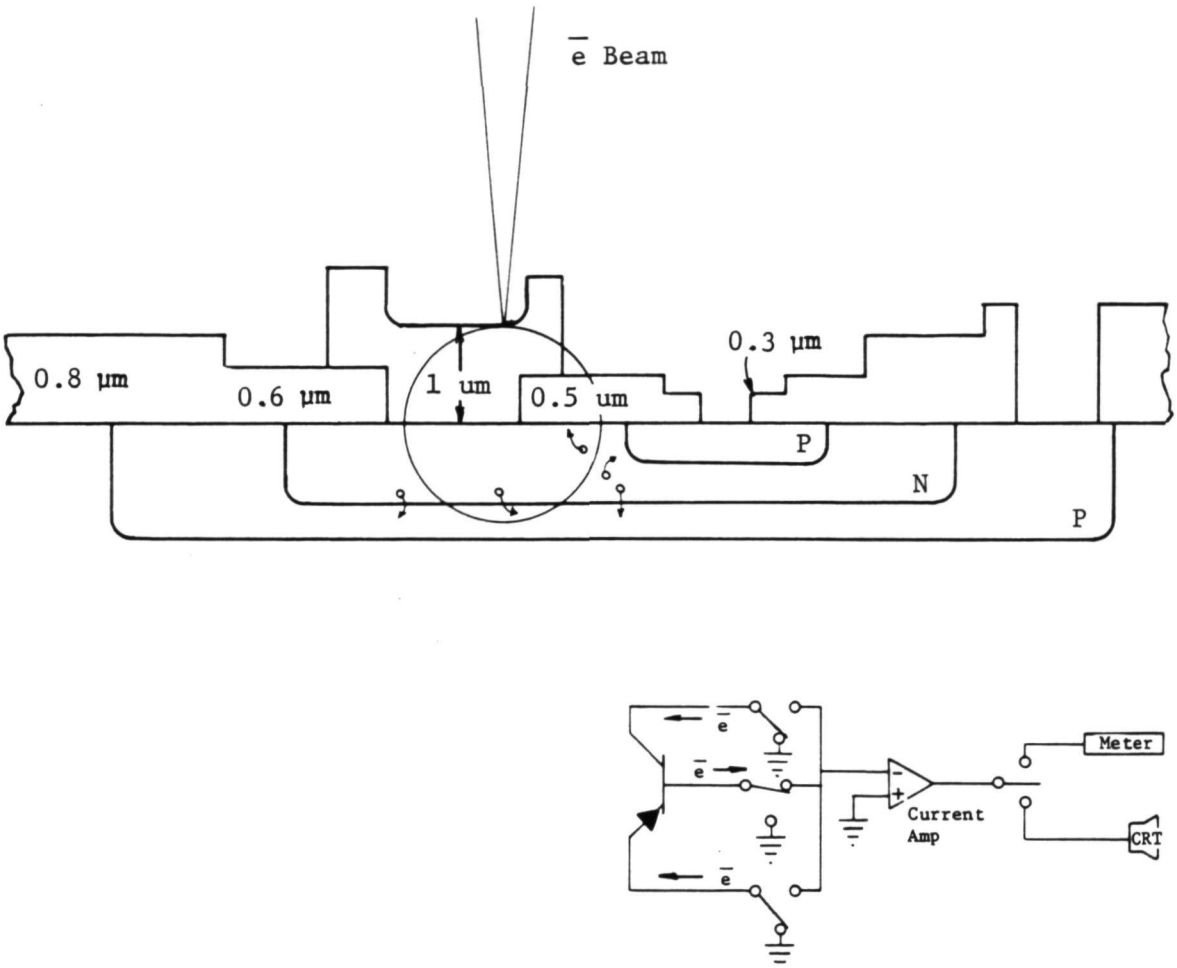

Figure 18. Cross Section Showing a Typical PNP Transistor and Current Amplifier Interconnect Circuit.

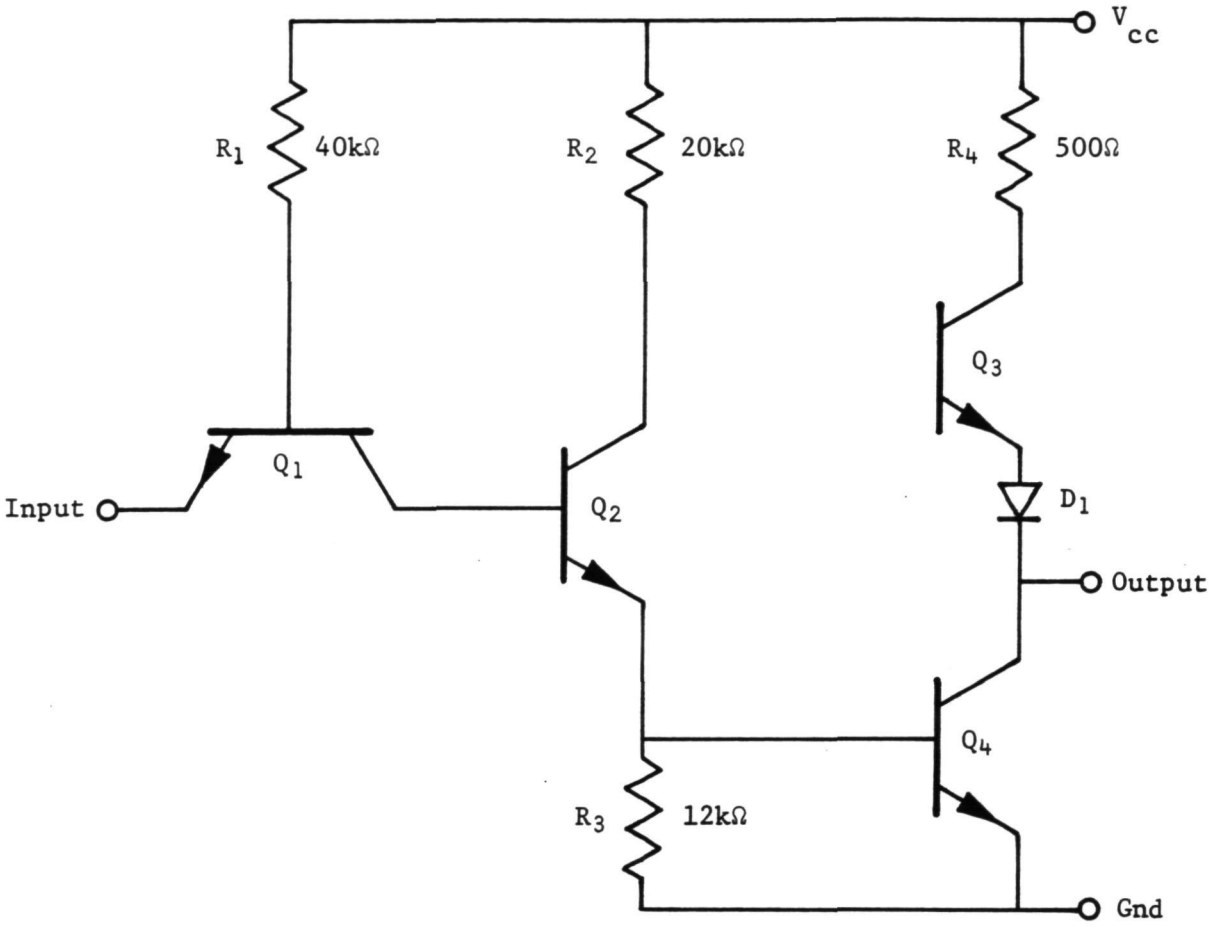

Figure 19. 54L04 Inverter Stage

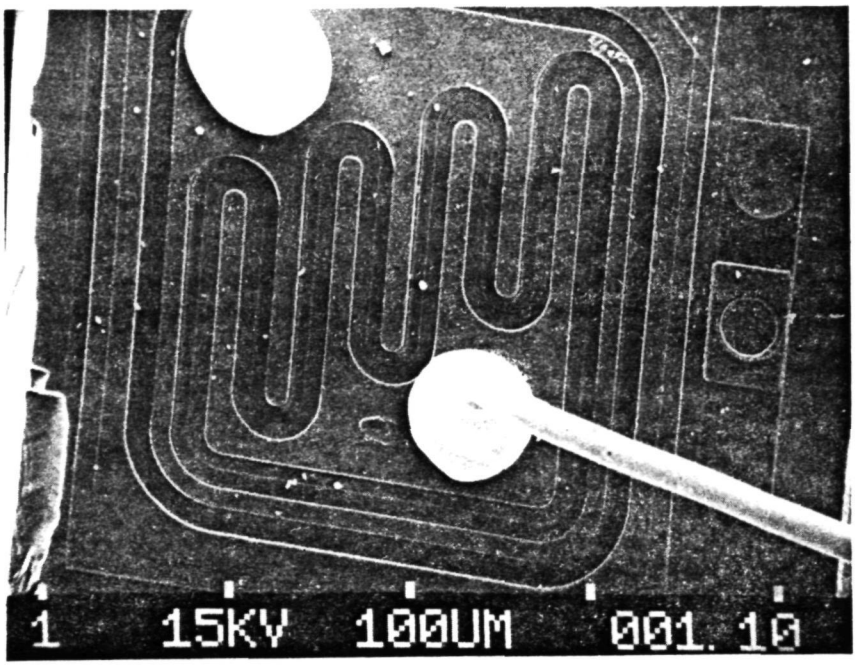

Figure 20. SE Micrograph of 2N2905 PNP Transistor. (E_B = 15 kV, $I_B \simeq 1 \times 10^{-10}$A, Beam Angle of Incidence = 10 deg, Mag x 250.)

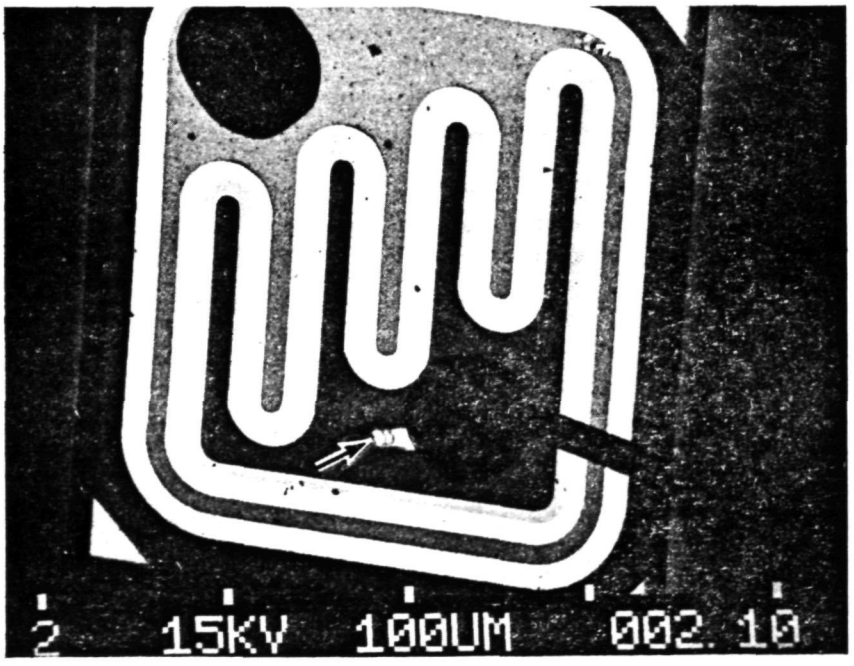

Figure 21. EBIC (Z Mod) Micrograph of 2N2905 PNP Transistor (Current measured from this base with emitter and collector at ground. Bright area [arrow] next to emitter bond is die probe imprint. E_B = 15 kV, $I_B \simeq 1 \times 10^{-10}$A, Beam Angle of incidence = 10 deg, Mag x 250.)

performed at a 10 degree angle of incidence. Figure 22 is a double exposure showing the SE image with an EBIC line scan superimposed. The line scan provides a better display of the EBIC variations.

The highest amplitude points are adjacent to the base metalization where base silicon is exposed. The lowest amplitude points are the emitter metalization fingers. This area represents the greatest thickness for the electrons to penetrate. Figure 23 shows a sequential line scan or Y modulated EBIC micrograph. This provides a quasi three-dimensional image. Figure 24 is an EBIC micrograph measured from the emitter and collector with the base at ground. This image is the inverted image of Figure 21. Figure 25 is an EBIC micrograph measured from the base with the emitter open and the collector at ground. In this configuration the electrons landing on the emitter must penetrate the emitter metalization and diffusion to contribute to recombination current in the base. This imaging configuration could be used for locating diffusion non-uniformities in the emitter region, i.e., diffusion defects along the vertical junction or pipes along the horizontal junction. If the pipe results in a short to the collector, it cannot be located because the emitter to base and collector isolation would be lost. Care must be taken to make certain the "junction defect" is not a blemish on the surface. It is always helpful to relate the EBIC image to a SE image. The image intensity (range threshold) for the emitter region can be adjusted by the current amplifier gain or by changing the acceleration voltage to increase or decrease the electron range. For example, the image intensity level can be set so that a change in current can be observed as a change in image contrast. See Figure 26.

For the second example, a 54L04 hex inverter was used. This die has a Au metalization system with glass passivation and the passivation was not removed. Figure 19 is a schematic for each of the six inverters. An SE micrograph of this die is shown in Figure 27.

Figure 28 shows an EBIC micrograph for the total die. The junction around the die perimeter provides the isolation for the diffused resistors. Figure 29 shows a single gate from this device and many of the diffusions are visible. The bright areas represent electron flow into the current amplifier and the dark areas represent electron flow out of the amplifier. The transistor locations are identified per the schematic in Figure 19. The EBIC micrographs in Figures 30 through 33 show the variations in EBIC images with respect to circuit pin imaging combinations. Table 16 lists the diffusions from which high recombination currents could be measured with respect to the pin configuration. Those diffusions that could not be displayed have a parallel resistor or a diode junction in the recombination current path. For instance, the base diffusion for Q2 in Figure 29. The recombination current must flow from the emitter of Q2 to ground through the current amplifier to the collector of

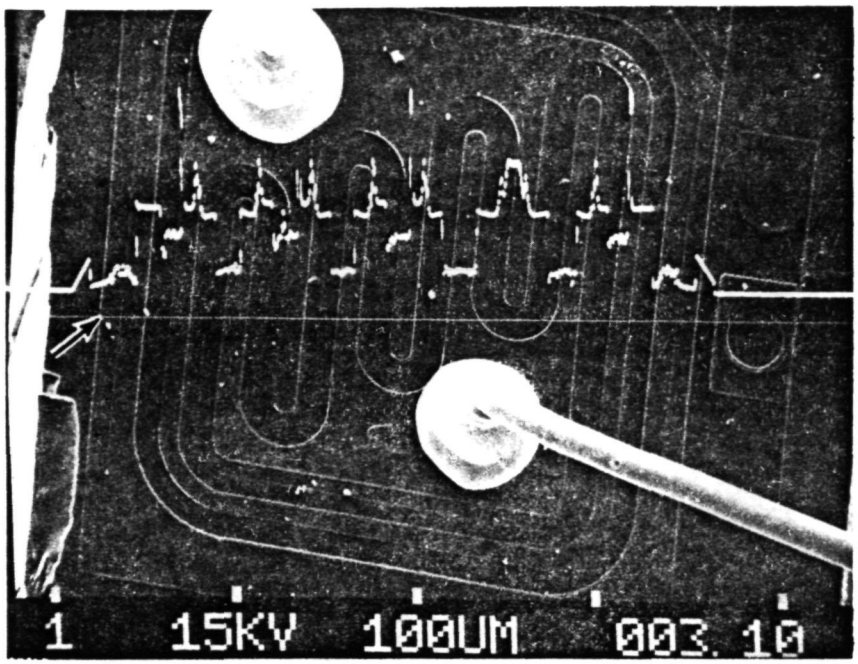

Figure 22. SE Micrograph with EBIC Line Scan Superimposed (The cursor line [Arrow] designates the location of line scan. The EBIC line has X axis coincidence with the cursor line. E_B = 15 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 250.)

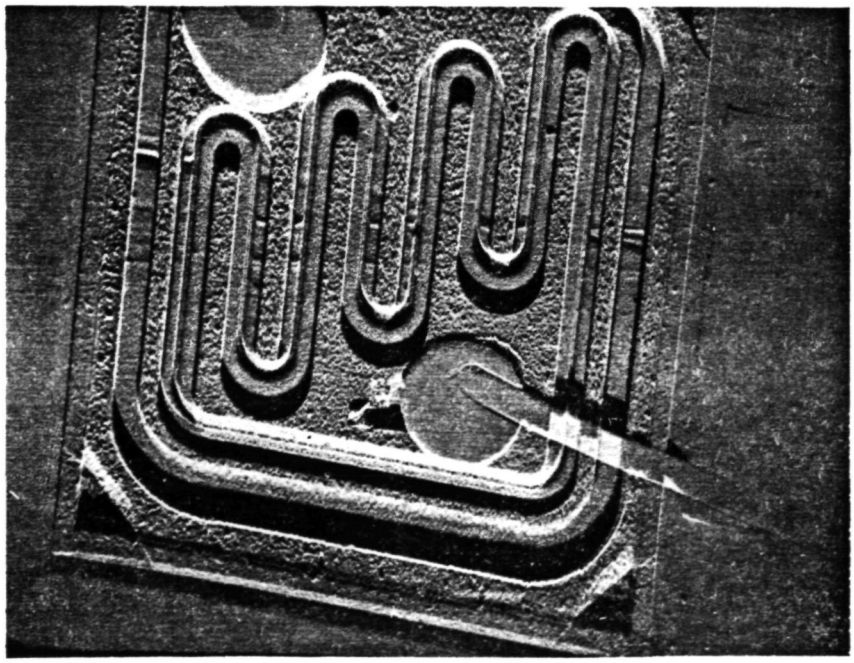

Figure 23. EBIC (Y-Mod) Micrograph. (This is the same image as Figure 21 except the modulation is superimposed on the Y-Axis scan. E_B = 15 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 250.)

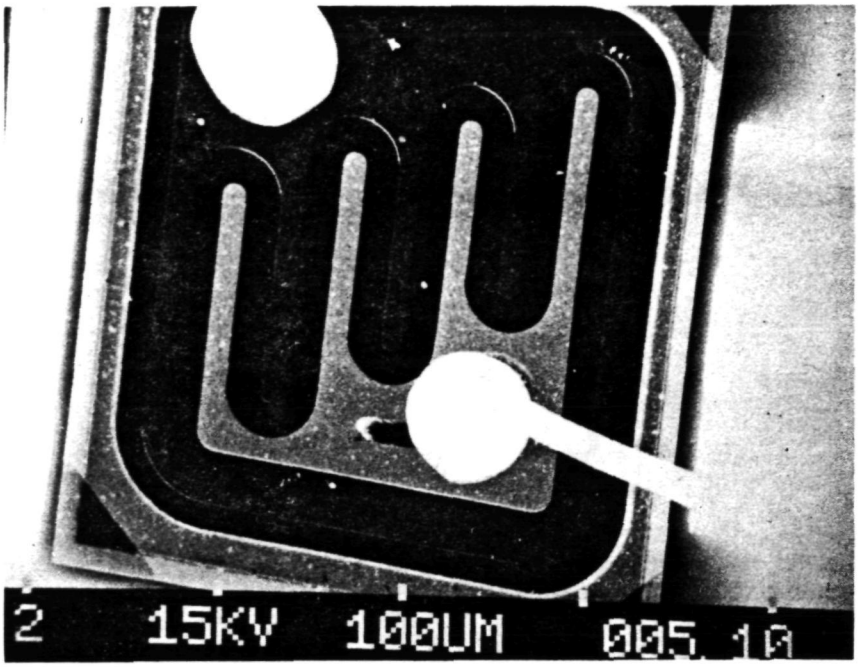

Figure 24. EBIC (Z Mod) Micrograph (Current measured from emitter and collector with base at ground. E_B = 15 kV, I_B ≈ 1 x 10^{-10}A, Mag x 250.)

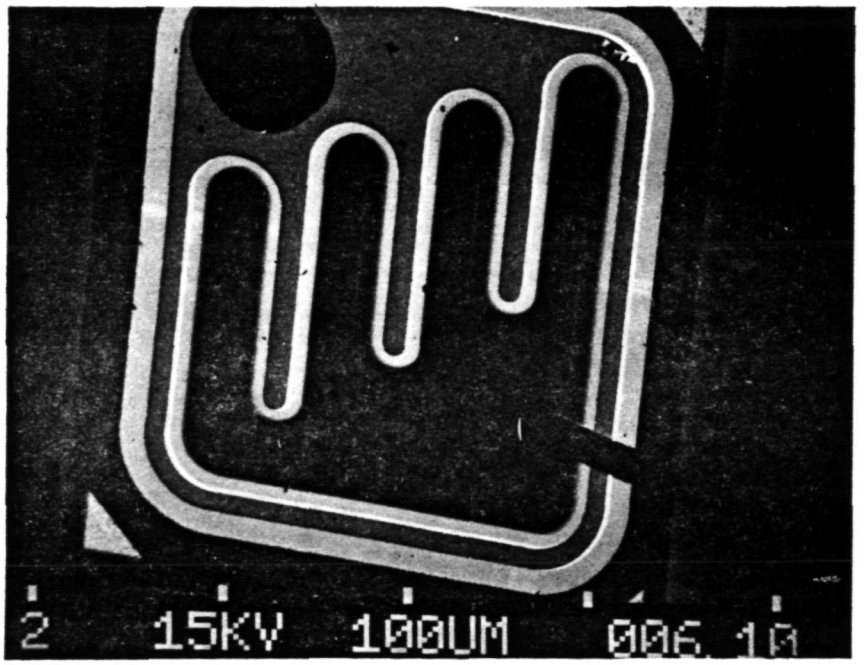

Figure 25. EBIC (Z Mod) Micrograph (Current measured from the base with emitter open and collector at ground. E_B = 15 kV, I_B ≈ 1 x 10^{-10}A, Mag x 250.)

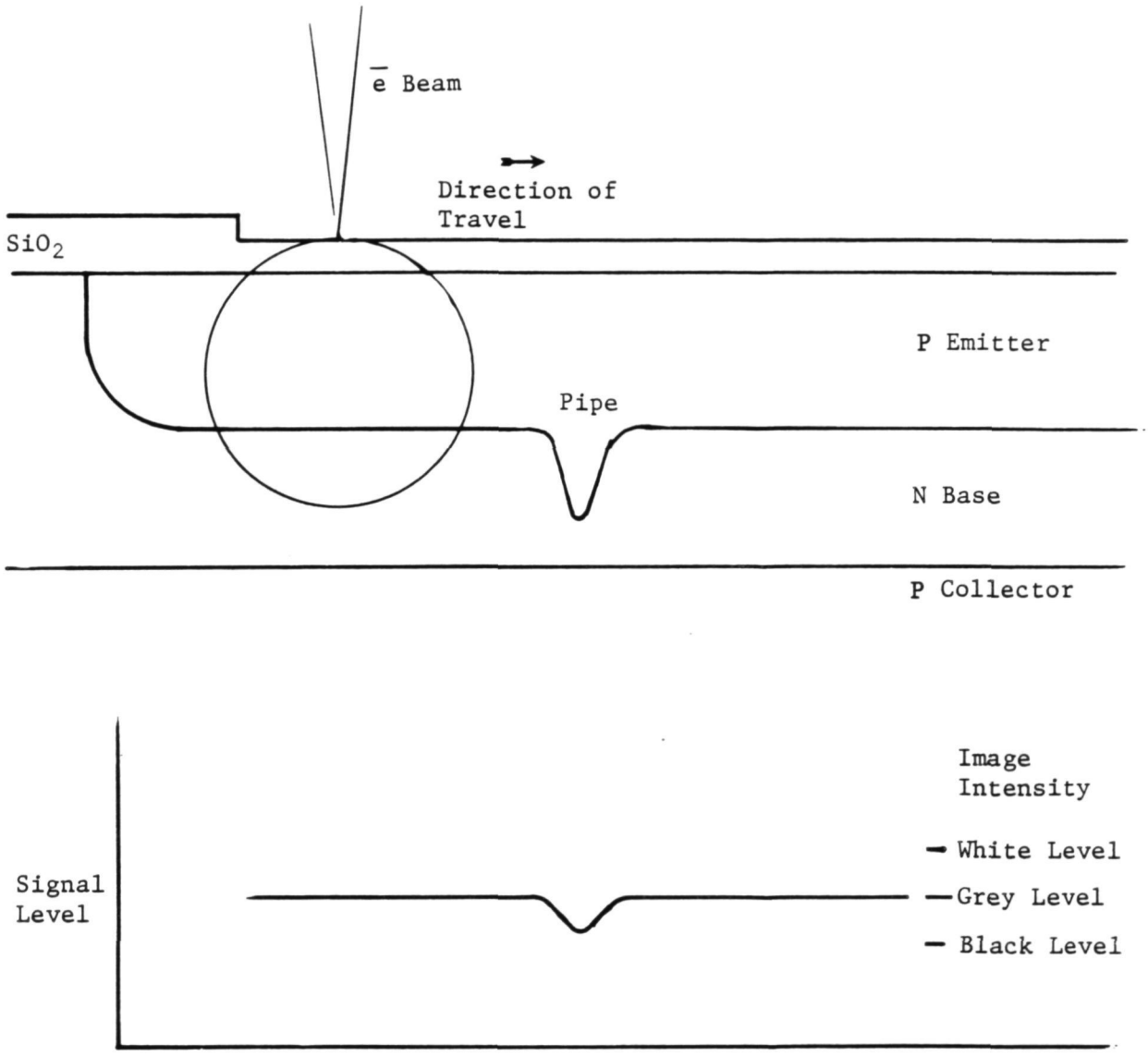

Figure 26. Image Intensity and Electron Range can be Used to Locate Pipes. (The current would be measured from the base with the emitter open and collector at ground. If the electron range does not penetrate the emitter diffusion or the signal level is set near the black level the pipes will not be detected.)

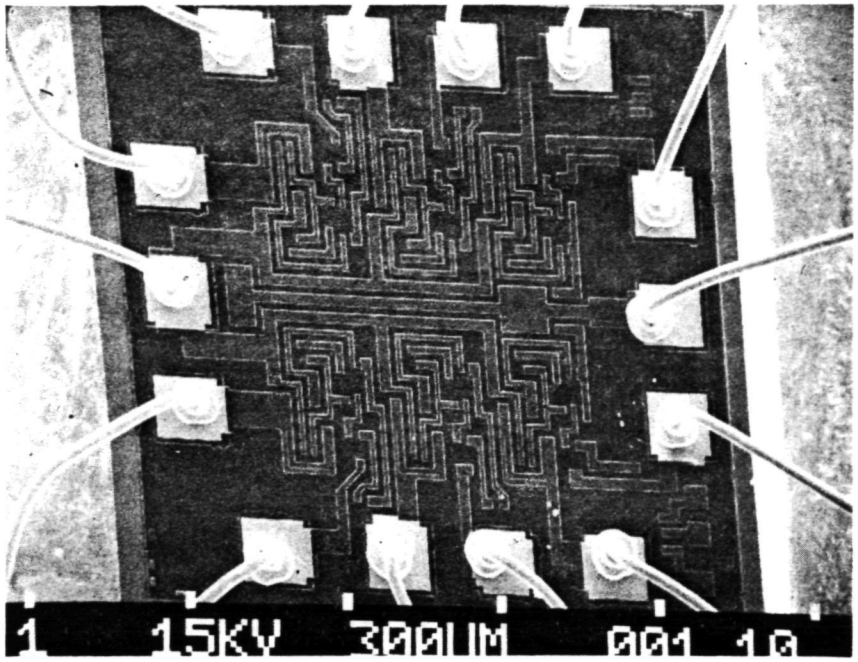

Figure 27. SE Micrograph of 54L04 Hex Inverter. (E_B = 15 kV, $I_B \approx 1 \times 10^{-10}$A, Beam Angles of Incidence = 10 deg, Mag x 70.)

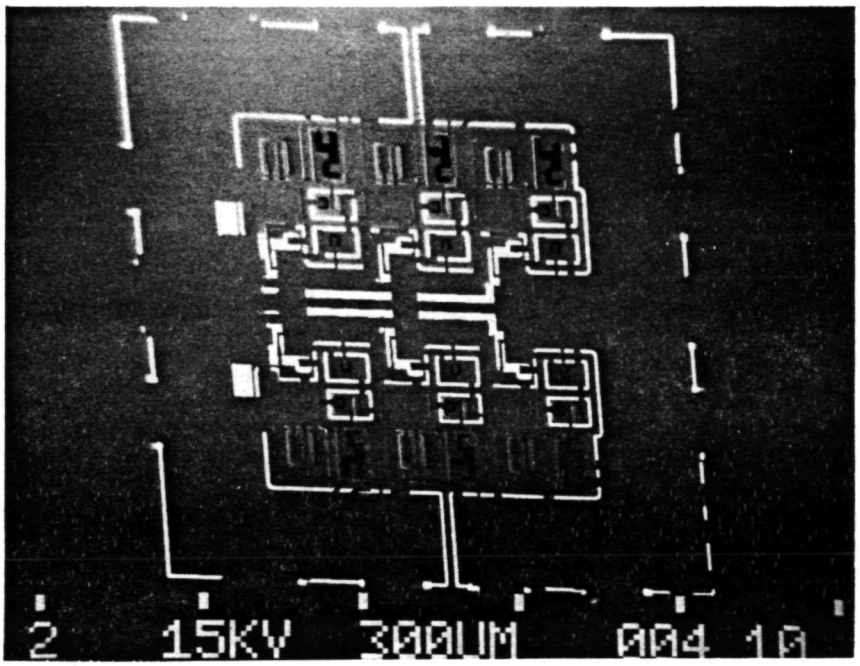

Figure 28. EBIC (Z Mod) Micrograph of 54L04 Hex Inverter. (Current measured at Pin 4 with Pin 11 at ground. E_B = 15 kV, $I_B \approx 1 \times 10^{-10}$A, Beam Angle of Incidence = 10 deg, Mag x 70.)

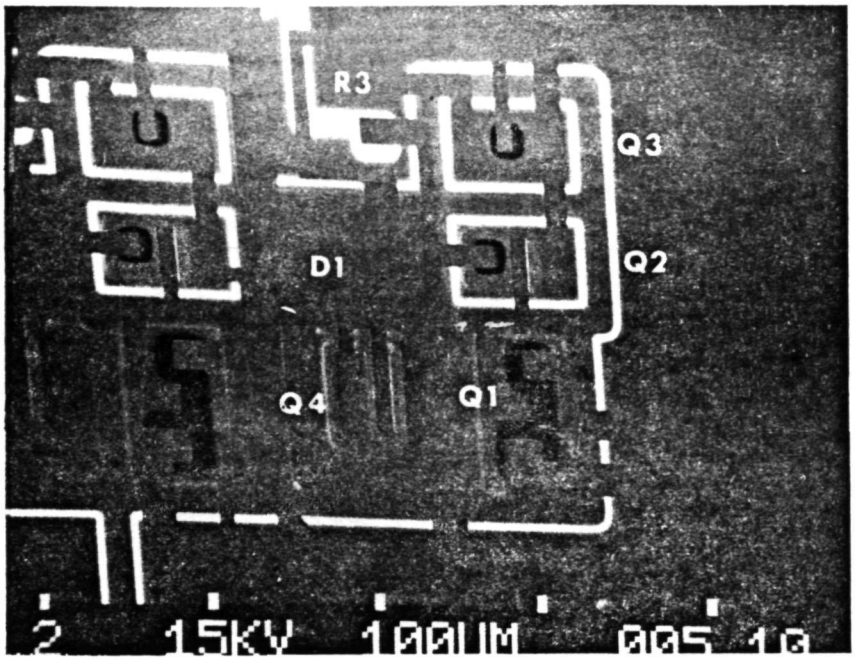

Figure 29. EBIC Micrograph Showing One of the Inverter Circuits (Pins 2 and 3). (Current from Pin 4 with Pin 11 at ground. Transistor location per Figure 19. E_B = 15 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 225.)

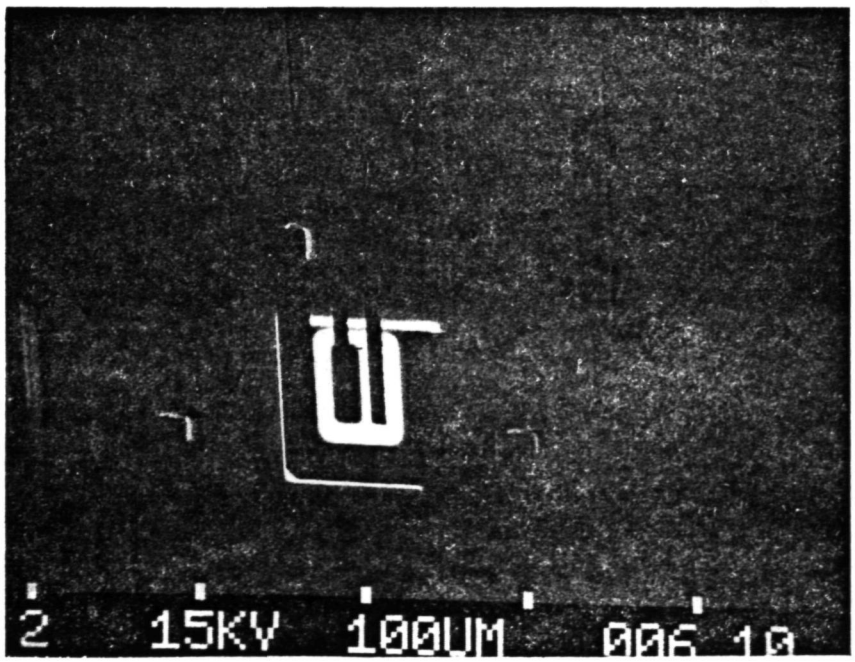

Figure 30. EBIC Micrograph of Same Area in Figure 29. (Current from Pin 2 with Pin 11 at ground. E_B = 15 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 225.)

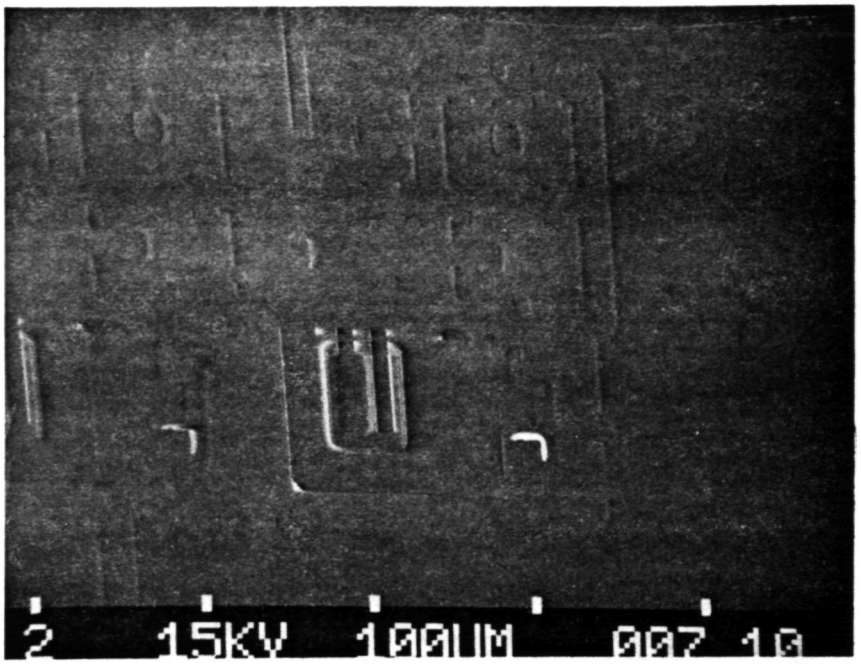

Figure 31. EBIC Micrograph of Same Area in Figure 29. (Current from Pin 3 with Pin 11 at Ground. E_B = 15 kV, I_B = 1 x 10^{-10}A, Mag x 225.)

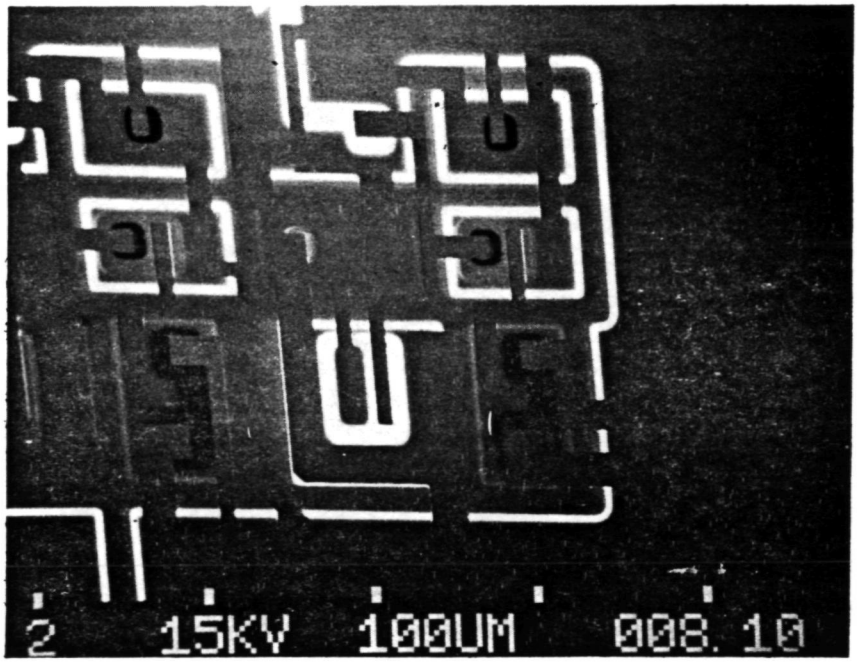

Figure 32. EBIC Micrograph of Same Area in Figure 29. (Current from Pins 2 and 4 with Pin 11 at Ground. E_B = 15 kV, I_B ≈ 1 x 10^{-10}A, Mag x 225.)

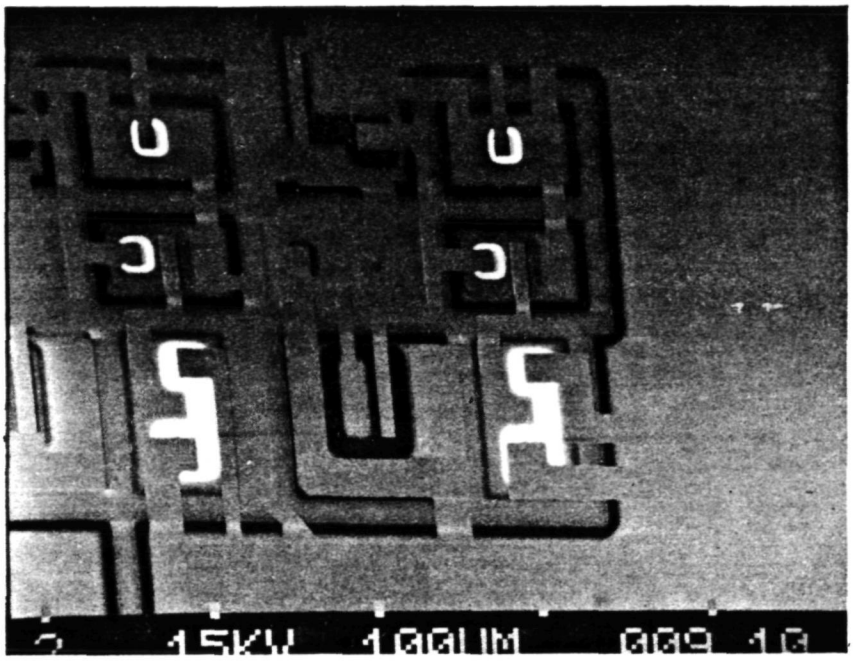

Figure 33. EBIC Micrograph of Same Area in Figure 29. Current from Pin 11 with Pins 2 and 4 at ground. E_B = 15 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 225.)

Table 16. Diffusions for which High Recombination Current can be Measured

Current Amp Input	Ground	Diffusions Observed
Pin 4	Pin 11	Q2 Base (Limited) Q2 Collector Isolation R3 Q3 Collector Isolation
Pin 2	Pin 11	Q4 Base Q4 Collector Isolation D1 Cathode
Pin 3	Pin 11	Q1 Emitter
Pin 11	Pin 4	Q1 Base Q2 Emitter Q3 Emitter

Q2 and then to the base. For current to flow (10^{-8}A), the potential between base and collector must be sufficient for forward conduction. This also results in base-emitter forward conduction and a large number of the electron-holes recombine in the transistor. Sometimes it is difficult to relate a specific point on a die to its location on an EBIC image. In these cases it is helpful to superimpose two images as shown in Figures 34 and 35.

From these basic examples, the importance of the circuit schematic and understanding of the diffusion geometries are obvious. Without them the application of EBIC and interpretation of EBIC images are difficult.

EBIC APPLICATIONS INVESTIGATED

The areas proposed for investigation were oxide defect identification, junction defect location, metal integrity at oxide steps, and surface leakage location. The proposed areas were conditional on the findings of the historical data review. During the study of EBIC applications, it appeared that the measurement of diffusion depths was possible so it was included as an area for EBIC investigation.

The study of qualitative EBIC applications will be described first.

Oxide Defect Identification

The detection of oxide defects is based on the relative beam-induced current level for a given beam acceleration voltage. A pinhole or etch defect in the surface oxide represents a decrease in surface thickness. The relative beam penetration depth is greater for the defect region than for a normal region. This results in an increase in recombination current immediately beneath the defect. The EBIC image for this area of the device may indicate the defect location.

Each of the IC test specimens was visually examined with a light microscope at 100 to 500X magnification for oxide defects. Possible oxide defects were identified on on LM111 and one IM5523C. (Note: The significance of these defects is not important. They are examples used only to demonstrate the application.) The LM111 was placed in the SEM for EBIC evaluation. Of six possible defects identified by light microscopy, one was verified by EBIC. The other five were found to be blemishes on the glass passivation. Figures 36 and 37 show SE and EBIC micrographs. This particular defect is located in the glass passivation. If it had been located beneath the adjacent aluminum conductor, it also would have been

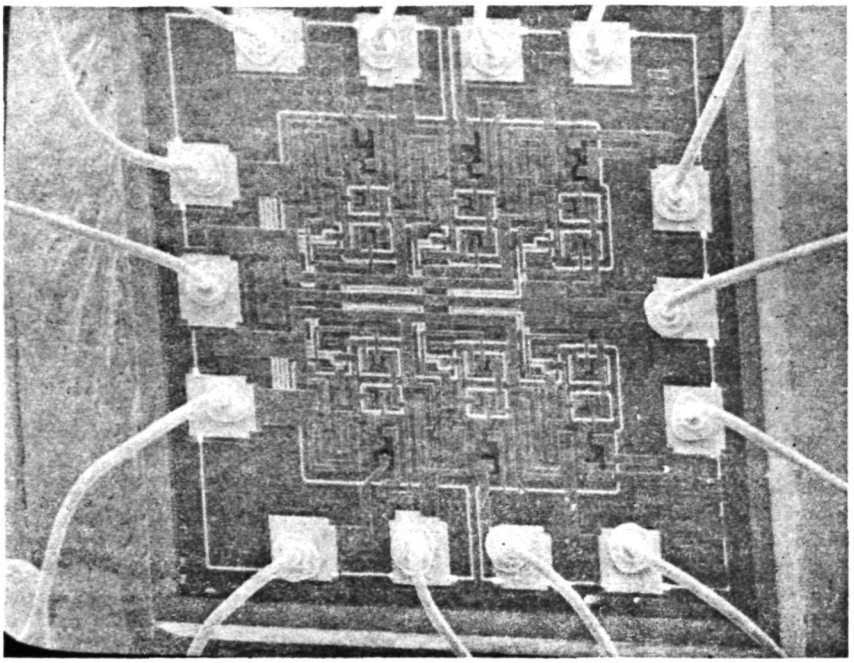

Figure 34. Superimposed SE and EBIC Images of 54L04. (Current from Pin 4 with Pin 11 at Ground. E_B = 15 kV, $I_B \simeq 1 \times 10^{-10}$A, Mag x 70.)

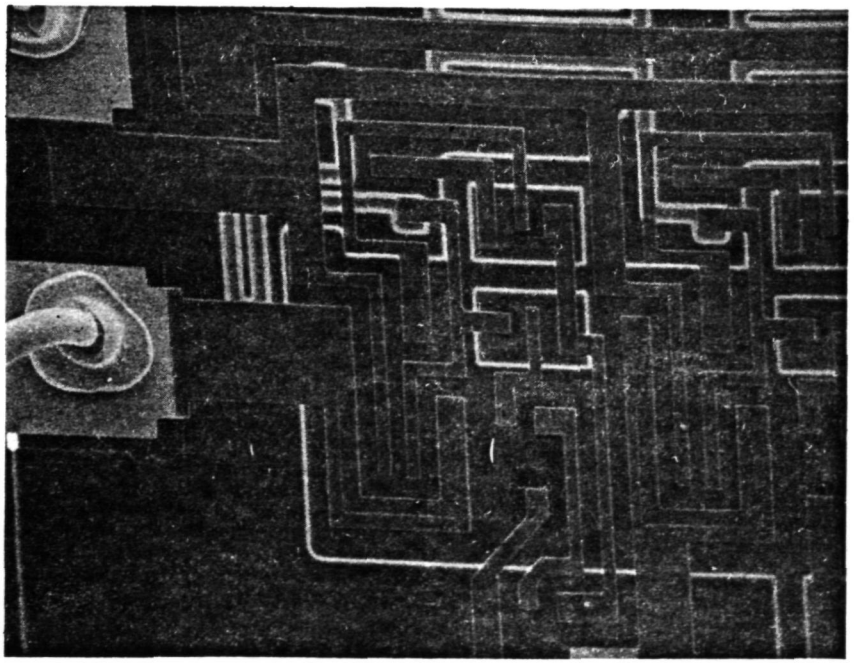

Figure 35. Superimposed SE and EBIC Images of 54L04 Inverter. (Current from Pin 4 with Pin 11 at ground. E_B = 15 kV, $I_B \simeq 1 \times 10^{-10}$A, Mag x 200.)

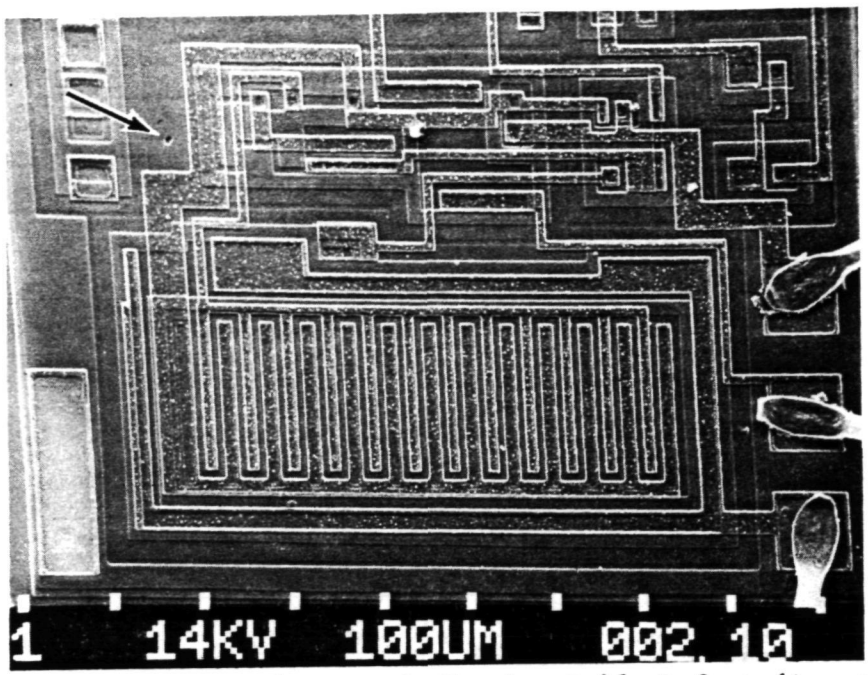

Figure 36. SE Micrograph Showing Oxide Defect (Arrow) in LM 111. (E_B = 14 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 125.)

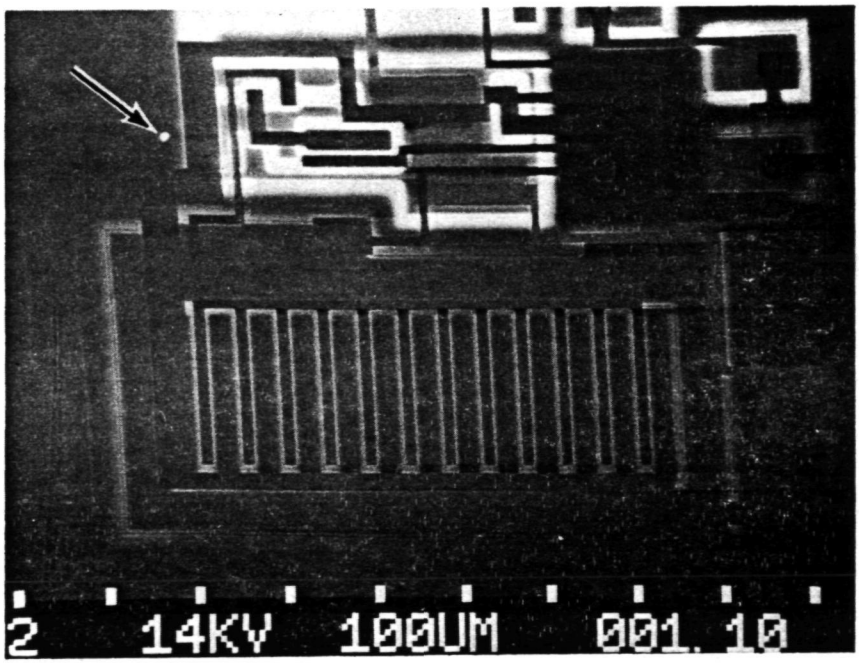

Figure 37. EBIC Micrograph Showing Oxide Defect (Arrow). (Same view as Figure 35. Current from Pin 8 with Pins 1 and 4 at ground. E_B = 14 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 125.)

visible by EBIC. The application is limited to surface films located above diffusions from which significant recombination currents can be monitored. In many cases this could represent less than 40% of the total die surface area.

Figure 38 shows the input circuitry for the same LM111 device. Figure 39 is an EBIC micrograph of the same area of Figure 38. High recombination currents from isolation, resistor, and base diffusions are indicated by the brighter areas. Also, metalization damage can be seen on the bonding pads from die probing. Figure 40 shows the inverted image of Figure 39. The current flowing in the major portion of the image is not much greater than the absorbed beam current level. This indicates a low recombination current gain. Recombination current gain is expressed as a ratio of recombination current (I_S) to beam current (I_B) or I_S/I_B.

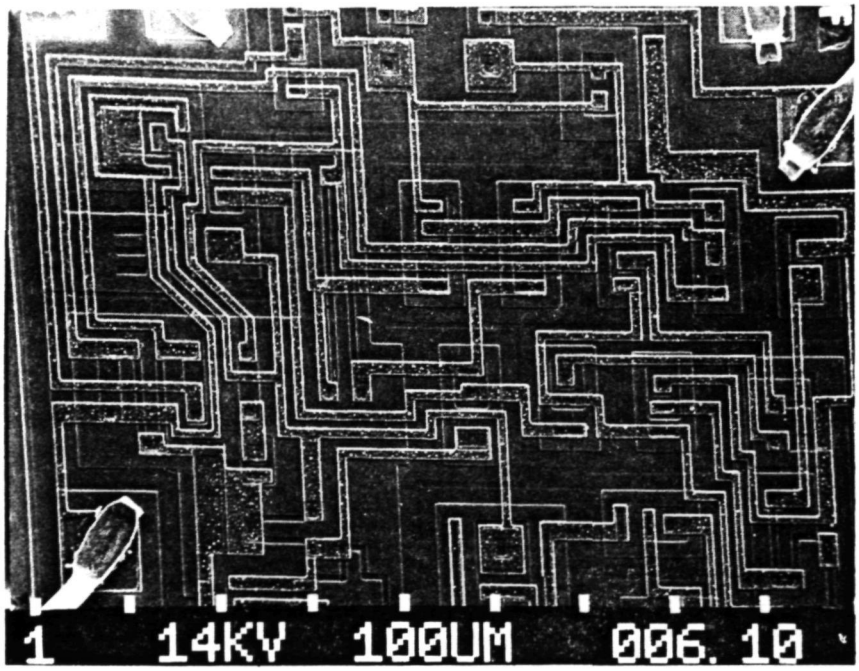

Figure 38. SE Micrograph Showing the Input Circuitry of the LM 111. (E_B = 14 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 130.)

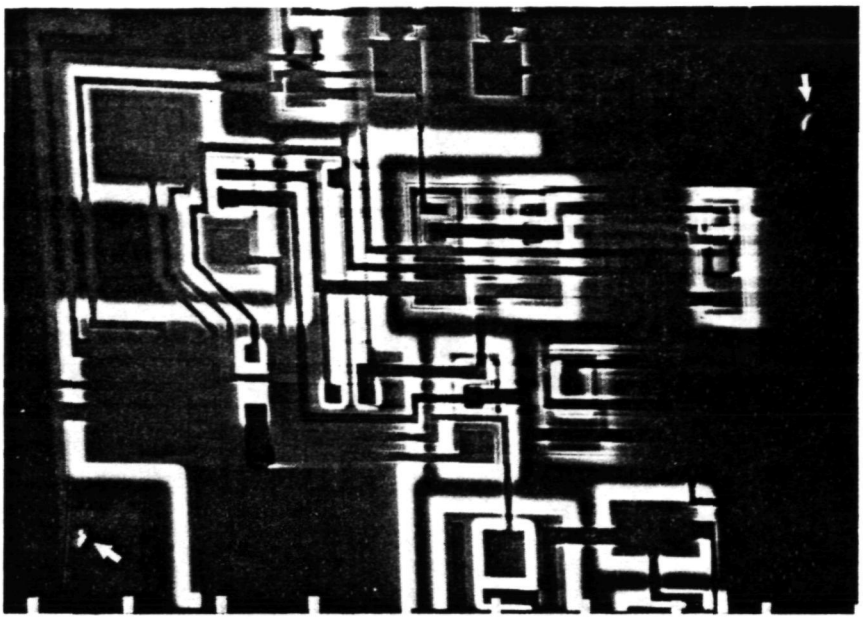

Figure 39. EBIC Micrograph of Same Area Shown in Figure 38. (The Electrical Probe Sites are Visible Adjacent to the Wire Bonds [Arrows]. Current from Pin 8 with Pins 1 and 4 at ground. E_B = 14 kV, $I_B \simeq 1 \times 10^{-10}$A, Mag x 130.)

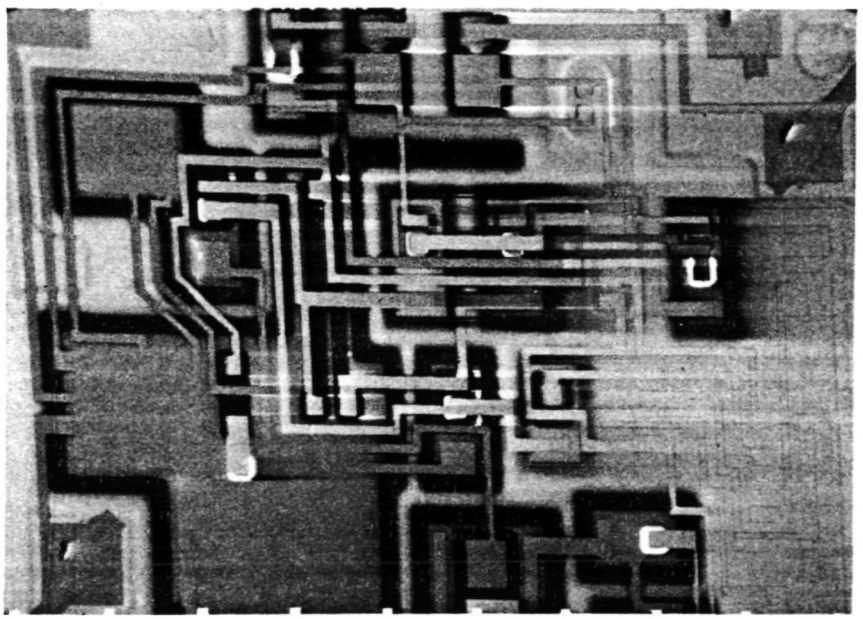

Figure 40. EBIC Micrograph of Area Shown in Figure 38. (A larger area is visible in this view; however, this current gain is low except for the emitters. E_B = 14 kV, $I_B \simeq 1 \times 10^{-10}$A, Mag x 130.)

Light microscopic examination of the IM5523 die, 256 x 1-bit Ram identified over 10 possible oxide defect locations. The die is shown in Figure 41. Evaluation of this device, using EBIC, showed the suspected defects were not pinholes. Examination by SE imaging failed to show that they were surface blemishes. It appears that the suspected defects were subsurface flaws that did not significantly increase or decrease the oxide thickness. This device was further examined using the EBIC mode to locate a circuit anomaly. For a device of this complexity it is necessary to scan the device at 500 to 800X magnifications. At lower magnifications the EBIC image was too "busy" for cursory inspection and detection of an anomaly. Figure 42 shows the EBIC image for the complete die. In memory circuits there is a large amount of diffusion and circuit repetition. This provides a common image pattern and simplifies the recognition of variations and anomalies. The memory cell images were inspected using this method of examination. This resulted in the location of pinhole defects in the glass passivation. Figures 43 and 44 show the EBIC and SE images for these defects. The SE image indicates these defects were located in the glass passivation. It was extremely difficult to see these defects during subsequent rexamination by light microscopy at 620X using polarized light.

The two examples show that oxide defects can be located using EBIC. It is limited by the accessibility of recombination current generated in the semiconductor circuit. Routine examination of circuits having MSI and LSI levels of complexity are time consuming. To obtain a reasonable image for examination, the magnification needs to be 500 to 1000X. The time required to examine a complete circuit could exceed one hour; therefore, using present examination techniques, this application is more practical for failure analysis than product screening. In failure analysis a defect can be localized to a specific area and EBIC can then be used to examine the area and locate the defect.

2. Junction Defect Identification

The identification of junction defects uses EBIC images to delineate diffusion boundaries. This application provides the capability of examining junction uniformity and identifying missing diffusions, junction defects, and discontinuities in diffusions. It is also capable of locating localized overstress and junction breakdown sites.

A junction boundary can be described as the transition point for majority carriers. The beam-induced recombination current originates at the junction boundary. Minority carriers that diffuse from the point of origin across the junction produce the recombination current; therefore, the beam-induced recombination current image delineates the junction boundary. A sample of the IC test

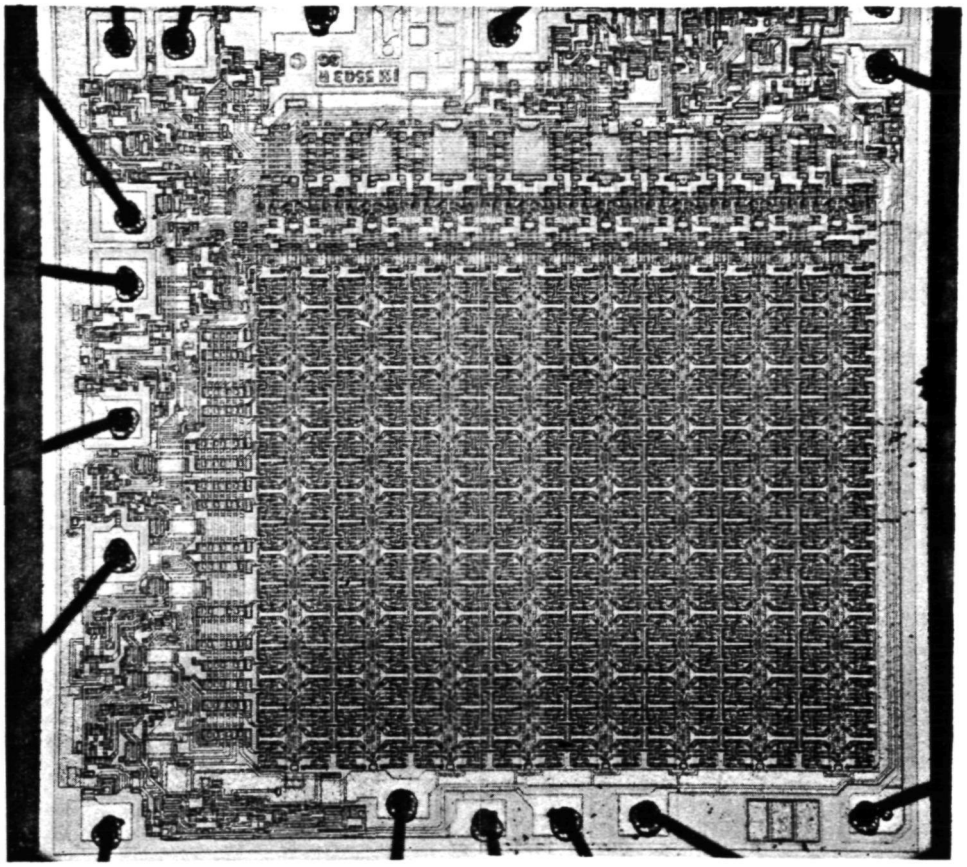

Figure 41. The IM5523 Die. (Examination by light microscopy had disclosed over 10 possible oxide defects. Mag x 50.)

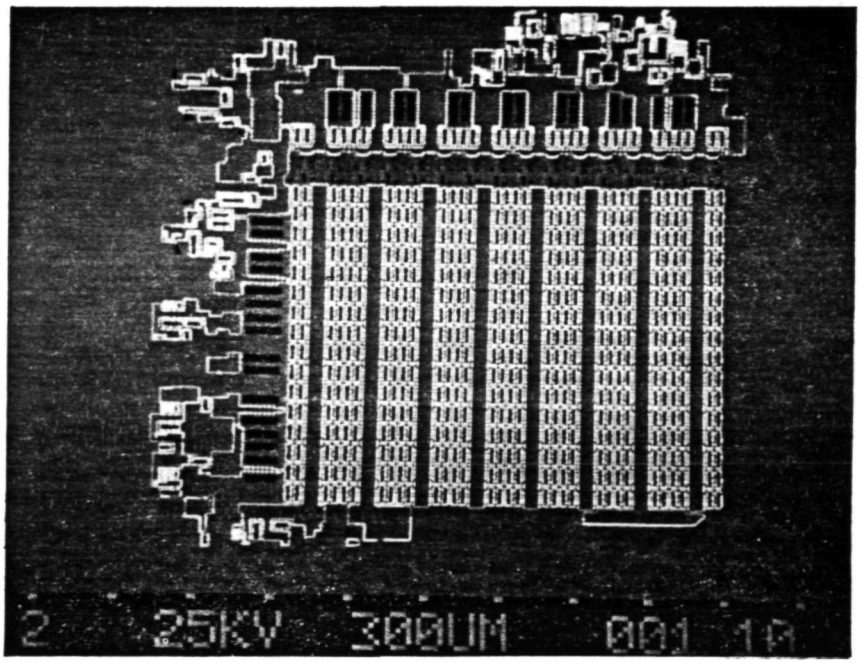

Figure 42. EBIC Micrograph for the Overall Device Circuit. (Current from Pin 16 with Pin 8 at ground. E_B = 25 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 35.)

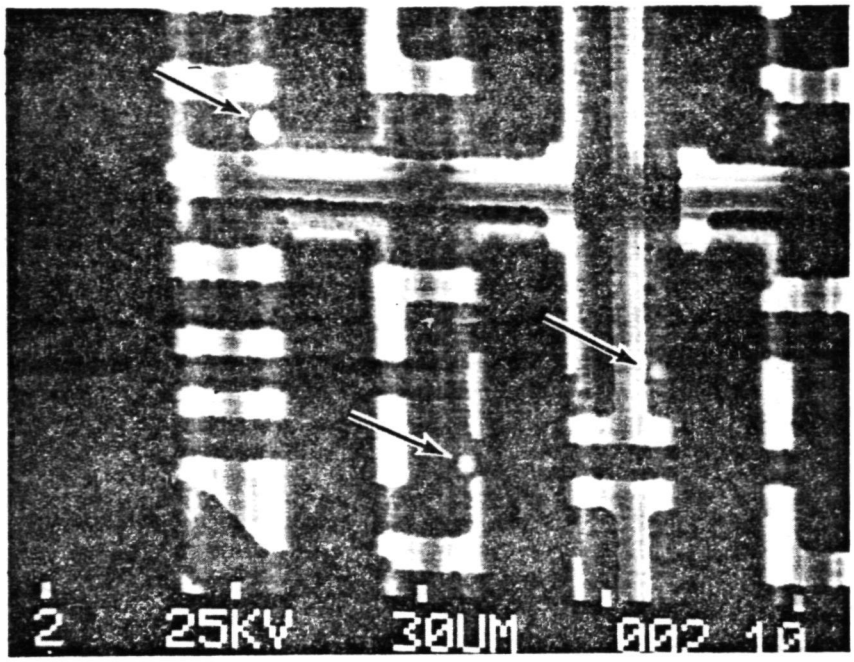

Figure 43. EBIC Micrograph Showing the Location of Three Pinholes in the Glass Passivation (Arrows). (Current from Pin 16 with Pin 8 at ground. Mag x 850.)

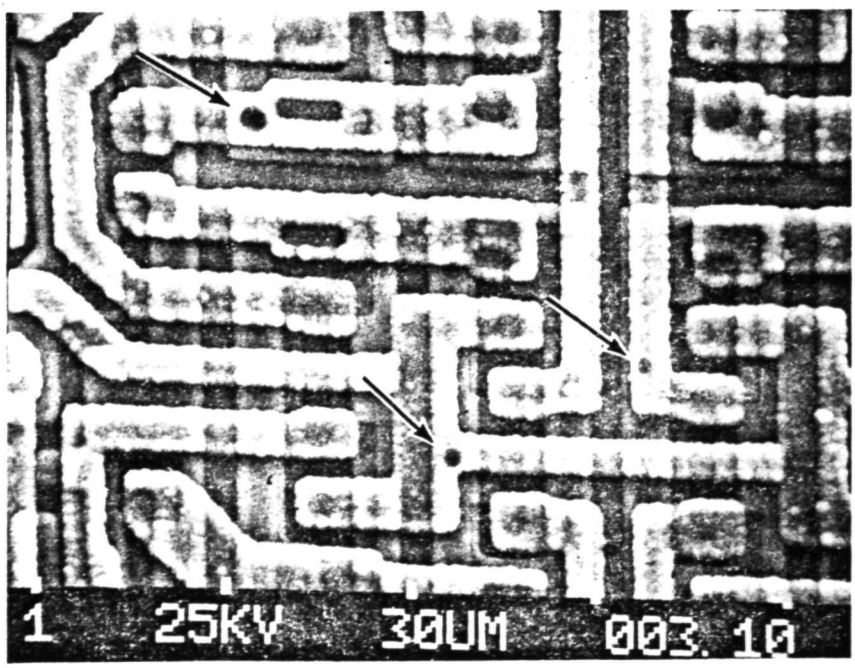

Figure 44. SE Micrograph of the Same Area Shown in Figure 43 Showing the Three Pinholes. (Arrows). (Mag x 850.)

specimens was examined by EBIC in an attempt to identify defects related to this application. No defects were identified. Two samples were selected from devices that were evaluated during this study. One is a DTL930 circuit with a 6638 date code. This device had been selected for evaluation to provide an example of earlier metallization processing. During EBIC evaluation junction non-uniformities were observed in the resistor diffusions. The second sample is a 2N3921 N-channel junction FET. This sample provides a typical example of localized overstress.

The DTL 930 die is not glass passivated. A photograph of the die is shown in Figure 45. Figure 46 shows one area in which junction non-uniformities or defects were observed. The EBIC image for this circuit is shown in Figure 47. This circuit was examined using several different EBIC pin sampling configurations. Figure 48 is an EBIC micrograph showing a part of one resistor. In this micrograph the defect sites are easily identifiable. The difference in image contrast between Figure 47 and Figure 48 was due to different current amplifier gain settings. In Figure 47 the current amplifier gain was set so the resistor signal level resulted in saturation of the current amplifier. In Figure 48 the gain was set to observe the variations in EBIC. An SE micrograph of the same area of Figure 48 is shown in Figure 49. These were found to be more difficult to detect with a light microscope or by SE imaging.

The 2N3921 die is glass passivated. See Figure 50. This device exhibited a high reverse leakage as a result of electrostatic discharge across the gate to drain junction. The I_{GSS} leakage current measured 6.5 μA at V_{GS} = -30V. The I_{GSS} specification maximum is 350 pA at V_{GS} = -30V. This device was first examined using the standard EBIC configuration of source and drain connected to the current amplifier and gate at ground. The EBIC image was examined under various current amplifier sensitivities but a damage site could not be detected. The measured I_{GSS} leakage current levels for this device were 18 pA for V_{GS} = -0.5V, 170 pA for V_{GS} = -5.0V, and 9 nA for V_{GS} = -10,0V. These data indicate that the beam-induced potential developed across the gate-drain junction was not sufficient to involve the damage site; therefore, the gate to drain-source junctions were externally reverse biased at V_{GS} = -10.0V. Reexamination of the EBIC image disclosed the damage site. See Figure 51. This EBIC micrograph shows the damage site as a low brightness spot (decreased EBIC current). The location of the site is in the N+ diffusion for the drain. See Figure 52. The decreased EBIC current indicates a decreased carrier lifetime that

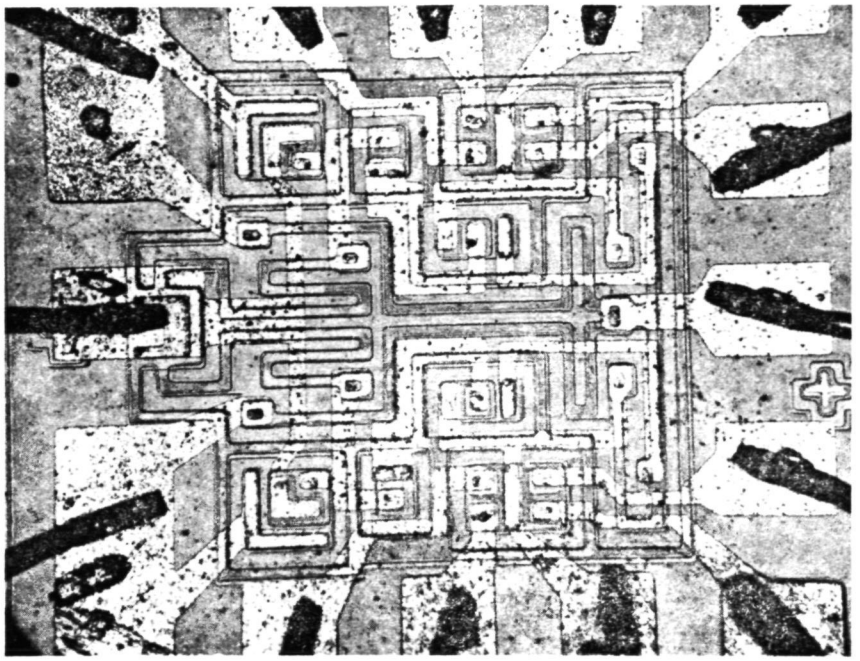

Figure 45. DTL930 Die. (Mag x 115.)

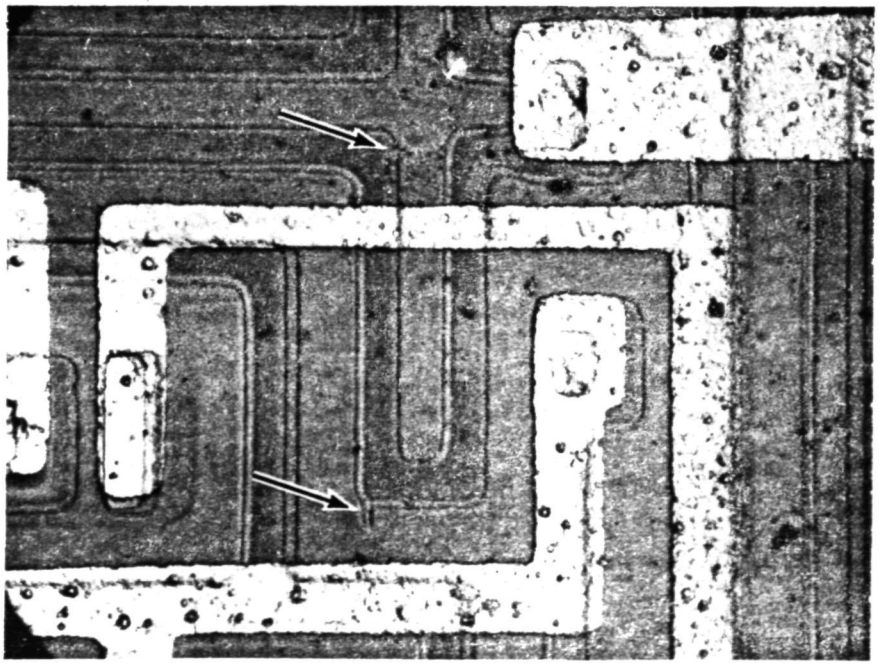

Figure 46. Visual Appearance of the Diffusion Defects Along a Resistor. (Arrows). (Mag x 500.)

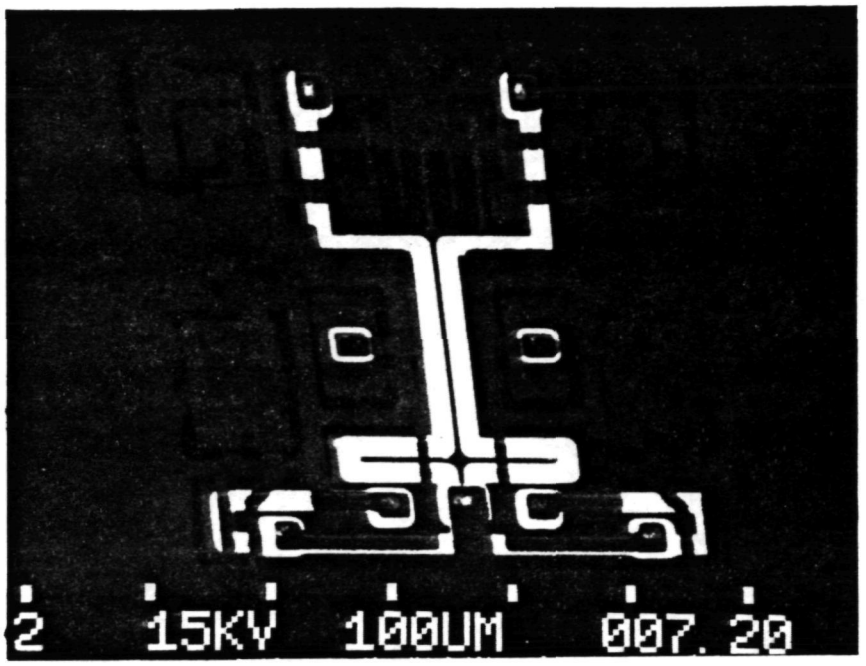

Figure 47. EBIC Micrograph of the DTL930 Die. (Current from Pin 7 with Pin 14 at ground. E_B = 15 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 170.)

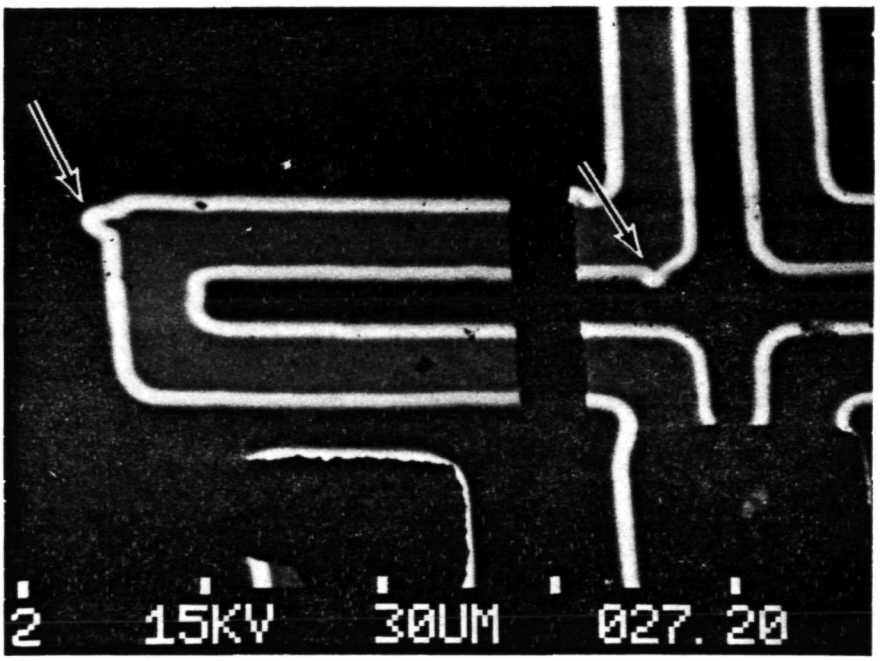

Figure 48. EBIC Micrograph Showing Two Diffusion Defects Along a Resistor. (Arrows). (Current from Pin 7 with Pin 14 at ground. E_B = 15 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 830.)

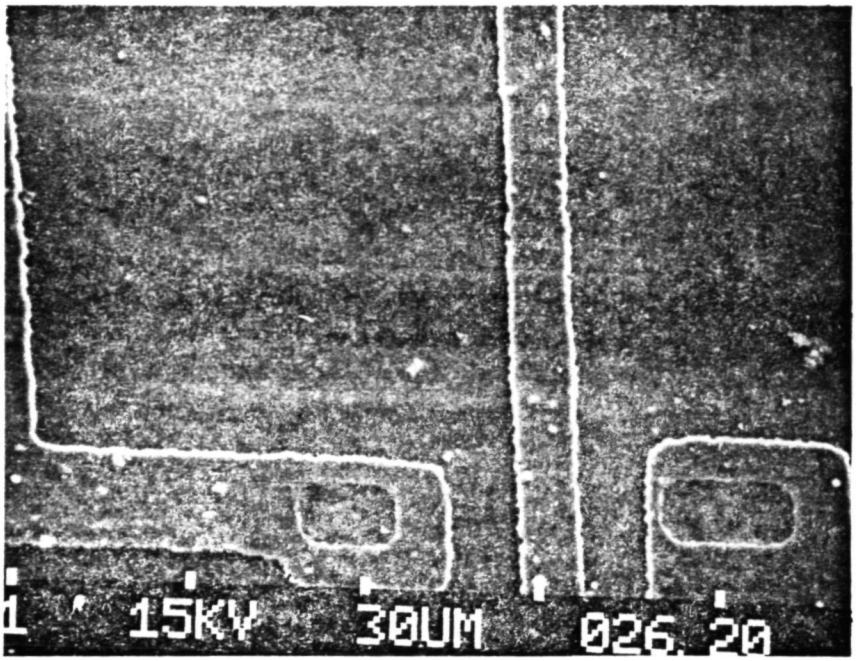

Figure 49. SE Micrograph of the Same Area Shown in Figure 48. (The defects have less contrast in this image. Mag x 830.)

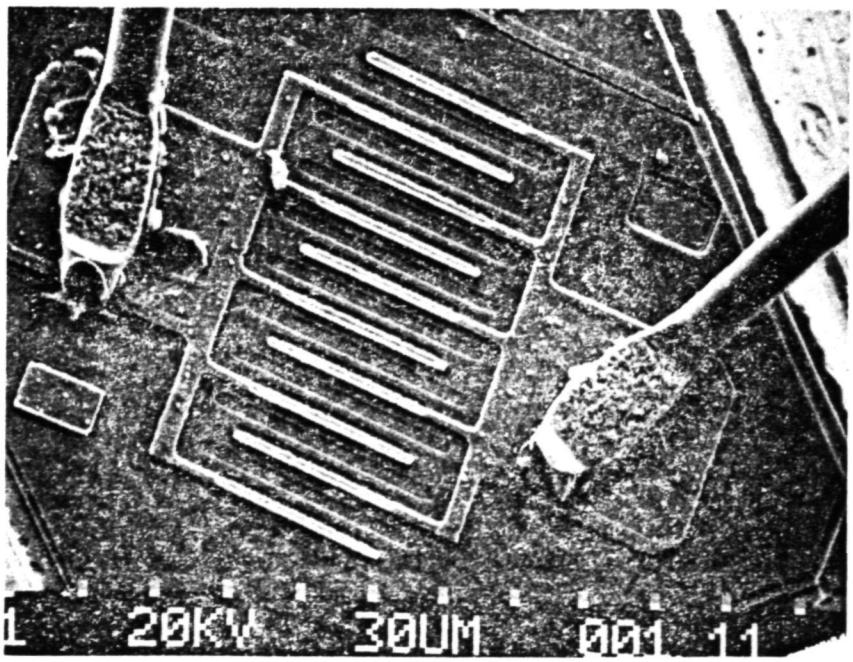

Figure 50. SE Micrograph of the 2N3921 FET Die. (Mag x 350.)

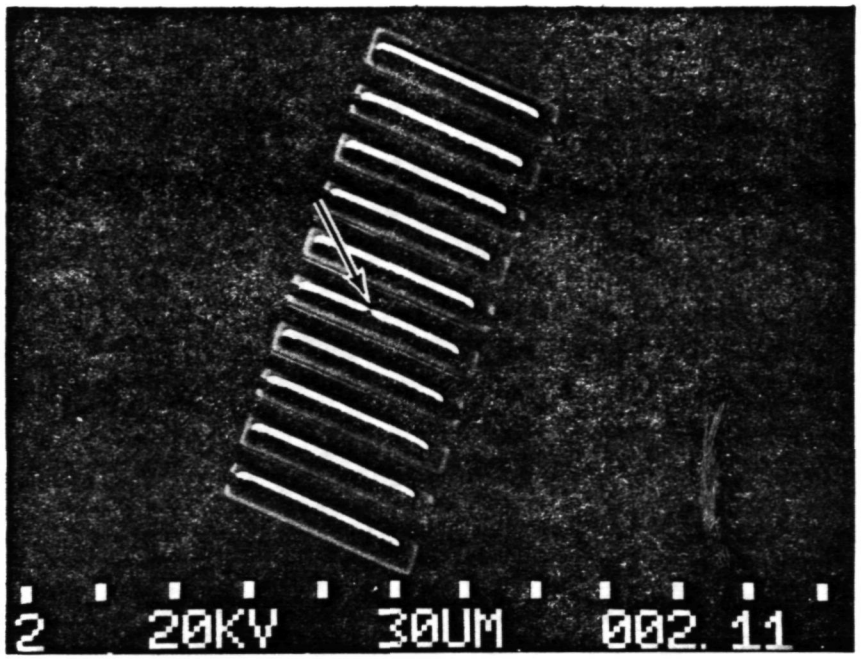

Figure 51. EBIC Micrograph of the Same Area Shown in Figure 50. (V_{GS} = -10 V. Damage site is visible (Arrow). (E_B = 20 kV, I_B ≈ 1 x 10^{-10}A, Mag x 350.)

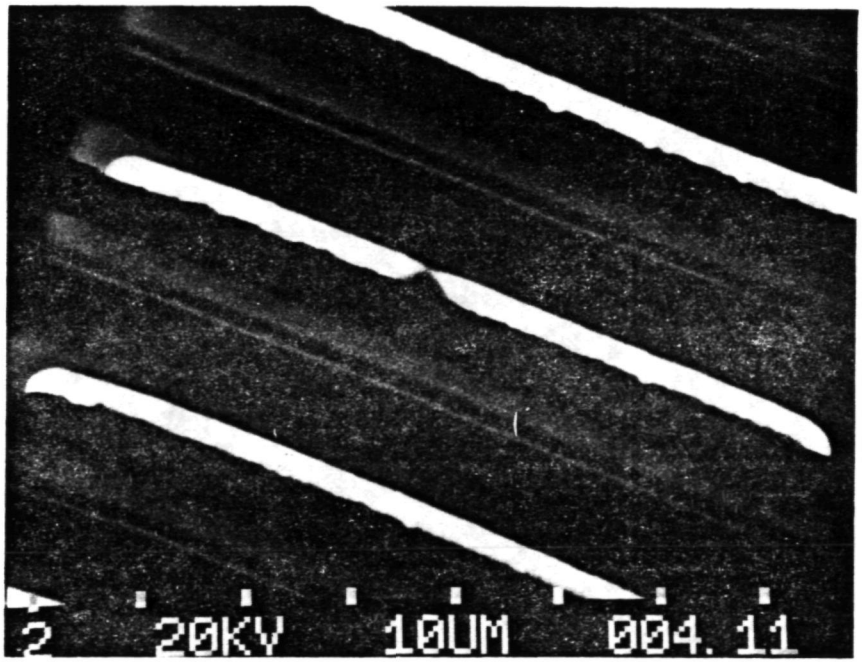

Figure 52. EBIC Micrograph Showing Damage Site at Increased Magnification. (Same conditions as Figure 51. Mag x 1500.)

is probably due to aluminum diffusion. This is characteristic of electrostatic discharge damage. Examination of the damage site by light microscopy and SE imaging failed to disclose any visible evidence of damage. An SE micrograph of this area is shown in Figure 53.

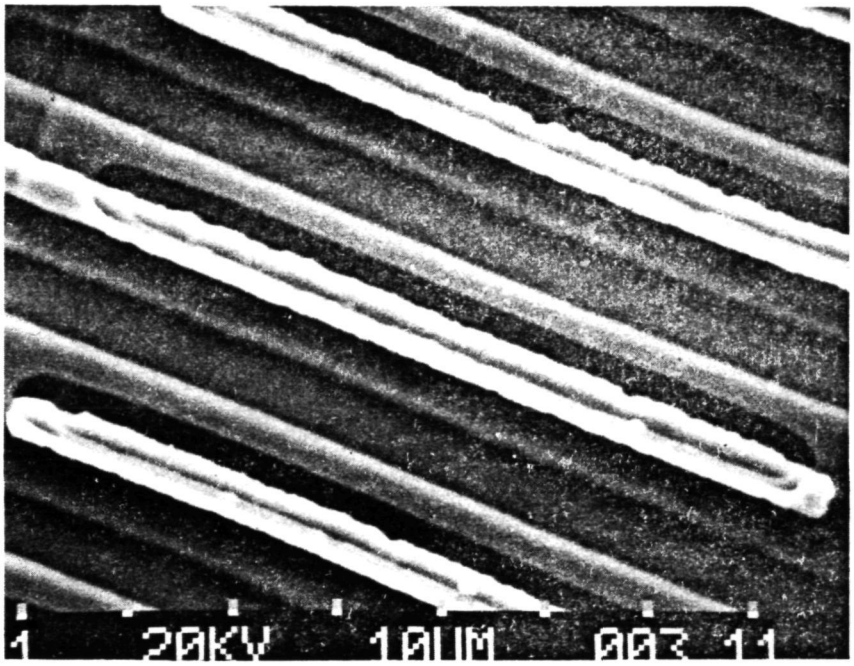

Figure 53. SE Micrograph of the Same Area in Figure 52. (No evidence of a damage site is visible. Mag x 1500.)

The application of an external bias across a junction during EBIC imaging results in two currents flowing in a common circuit. See Figure 54. One is the EBIC current and the other is the leakage current. For a stable leakage current the current amplifier dc offset can be adjusted to cancel it. The offset range is generally limited to compensating dc levels up to 10 times greater than the current amplifier's full scale range. The second method is to use a capacitor in series with the current amplifier input to block the dc flow. See Figure 55. In addition to the blocking capacitor, a resistor (R_S) is needed to develop the ac signal. A circuit time constant must be selected that is compatible with the line scan rate. The time constant can be approximated by the product of

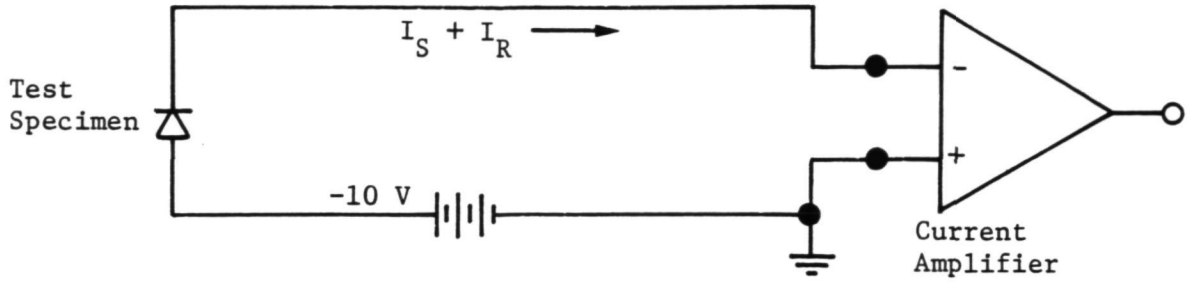

Figure 54. External Bias Supply Configuration. (I_S = EBIC, IR = Reverse Junction Leakage.)

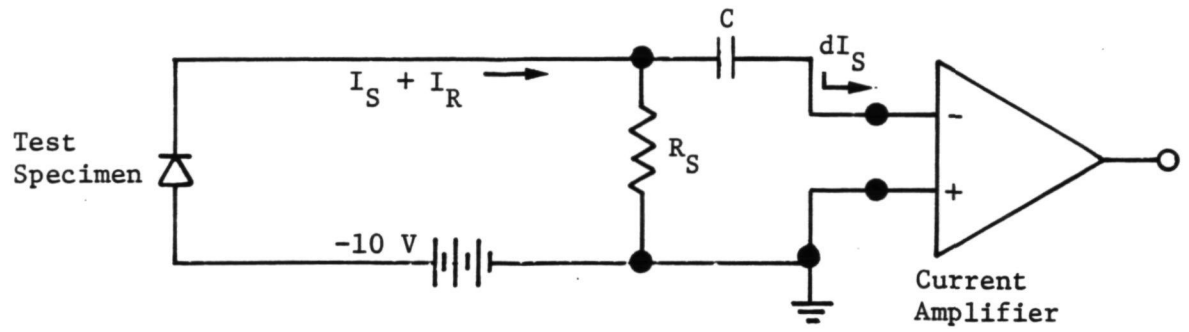

Figure 55. Capacitor-Coupled Configuration. (I_S = EBIC, I_R = Reverse Junction Leakage.)

$3x10^{-3}$ x line scan period. The current amplifier offset compensasation method is preferred. This was the method used for the J-FET example. It provides a direct, modulated EBIC image that displays the relative current levels.

The application approach and the results for two examples are described. The use of an externally applied bias for initiating or enhancing defect current is demonstrated. The location of subtle degradation sites at semiconductor junctions in the past has been, at best, difficult. This application provides a sensitive, high resolution, and nondestructive method of location. The greatest use of this application will probably be failure analysis. The application can also provide an accurate and rapid method for detecting mask defects that result in missing and incomplete diffusions.

3. Surface Leakage

Surface leakage for the purpose of this study is defined as leakage that occurs in localized areas due to trapped ionic charge and conductive residue or thin films. It had been anticipated that the low current, high resolution characteristics of the electron beam would be ideally suited for this application. During the study of semiconductor irradiation damage the effects of surface electron bombardment were better appreciated. It had been suspected and was confirmed during this study that trapped ionic charge would be dissipated by electron bombardment. A device that exhibited a channel leakage characteristic was examined using EBIC. The channel region could not be located and postelectrical measurement showed the channel was no longer present. The evaluation was performed without external bias applied to the device. Of the two surface leakage mechanisms, inversion due to trapped ionic charge would have been more detectable. The inverted region of the semiconductor would produce recombination current that should increase the detection sensitivity.

This is not the case for the conductive residue or thin film. Actual test specimens were not available for study so the practicality was reviewed on a theoretical basis. The contribution to an EBIC signal would be the absorbed energy or current related to the film density; this would represent a percentage of the beam current. For most cases it is considered that the magnitude of the absorbed current would be nondiscernible; therefore, the application of EBIC for detection of surface leakage does not appear feasible at this time.

This concludes the evaluation of qualitative EBIC applications. There were two quantitative EBIC applications evaluated during this study. They were diffusion depth measurement and the evaluation of metallization integrity at oxide steps.

4. Diffusion Depth Measurement

The measurement of diffusion depth is based on locating the electrical junction near the surface with EBIC. The magnitude of beam induced recombination current is related to diffusion depth and carrier diffusion length. As the point of electron-hole generation approaches a junction the quantity of minority carriers that diffuse across the junction increases. The maximum beam-induced recombination current occurs when the electron beam incidence is directly over the junction as shown in Figure 56. The centroid of the EBIC level line scan display marks the location of the junction. A method is required to physically relate the centroid to the device surface and to the diffusion distance. The physical relation is determined by photographically superimposing the line scan signal on the SE image. The diffusion distance is measured from the diffusion oxide cut boundary to the electrical junction as indicated by the line scan signal. The measurement assumes that the vertical and horizontal diffusion rates are equal. Based on this assumption, the horizontal diffusion distance would be equivalent to the vertical diffusion depth.

Diffusion depth measurements using EBIC were made for six transistors. Three transistors were 2N2905 and three were 2N3720. The emitter diffusion depth were measured for the 2N2905 transistors. The base-collector junctions were covered by guard ring metalization and were not measured. Both emitter and base diffusion depths were measured for the 2N3720 transitors. A typical line scan is shown in Figure 57. This is a line scan for a 2N2905 with the aluminum metalization removed. Typical line scans for other transistors are shown in Figure 58, 59, and 60. These measurements were performed with no external bias applied. (Note: Care was taken not to move the film between exposures.)

Following EBIC measurement, the six transistors were mounted in epoxy, microsectioned, and etched. The nominal angle selected for microsection was 15 degrees. This provided an approximate 4:1 magnification of the diffusion depths. The polished sections were etched for 10 to 15 seconds with a sirtl etch. The diffusion depths were measured at X1000 magnification using a calibrated reticle. The mounted transistors were then sectioned at a right angle to this original section. The original angle of section was then measured microscopically. The data for the measurements are contained in Table 17. These data show significant errors between the microsection and EBIC measurements for the emitter diffusions. The error appears to be in the EBIC measurement. This indicates that the initial assumption of isotropic diffusion profiles was incorrect.

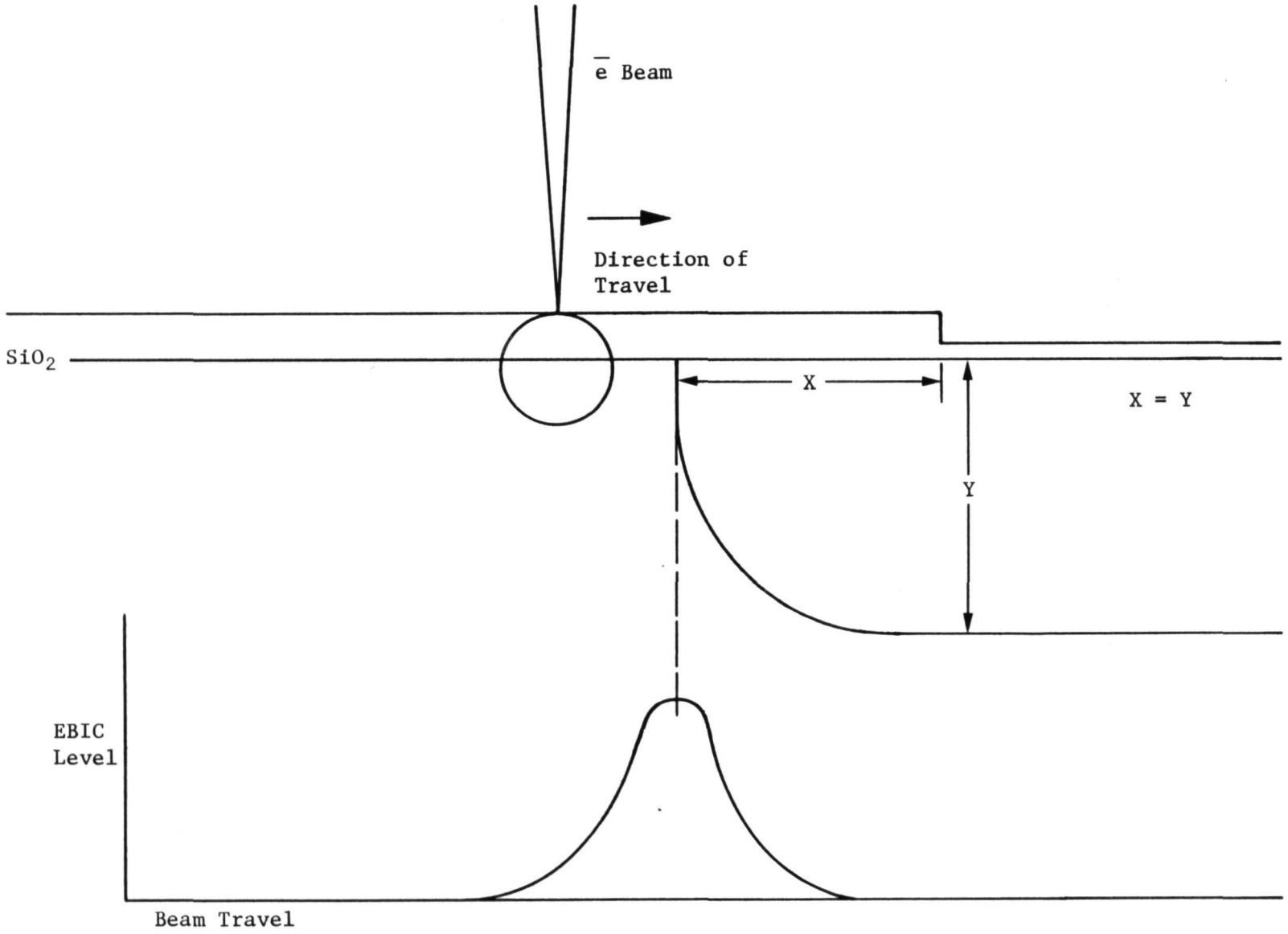

Figure 56. EBIC Level as a Function of Electron Beam Scan Across a Junction.

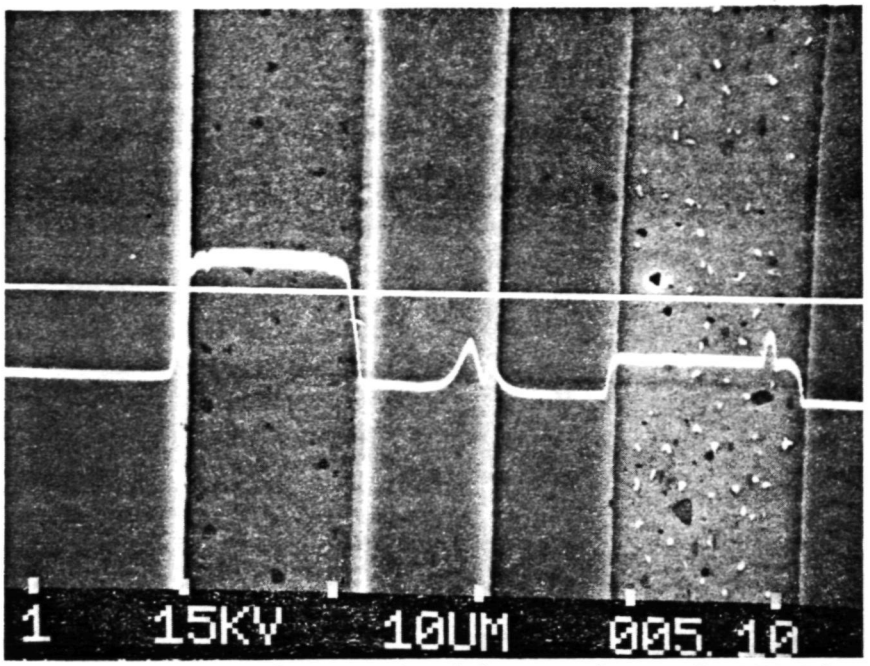

Figure 57. SE Micrograph with Superimposed EBIC Line Scan. (The EBIC line has X axis coincidence with the cursor line. current from base with emitter and collector at ground. E_B = 15 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 2000.)

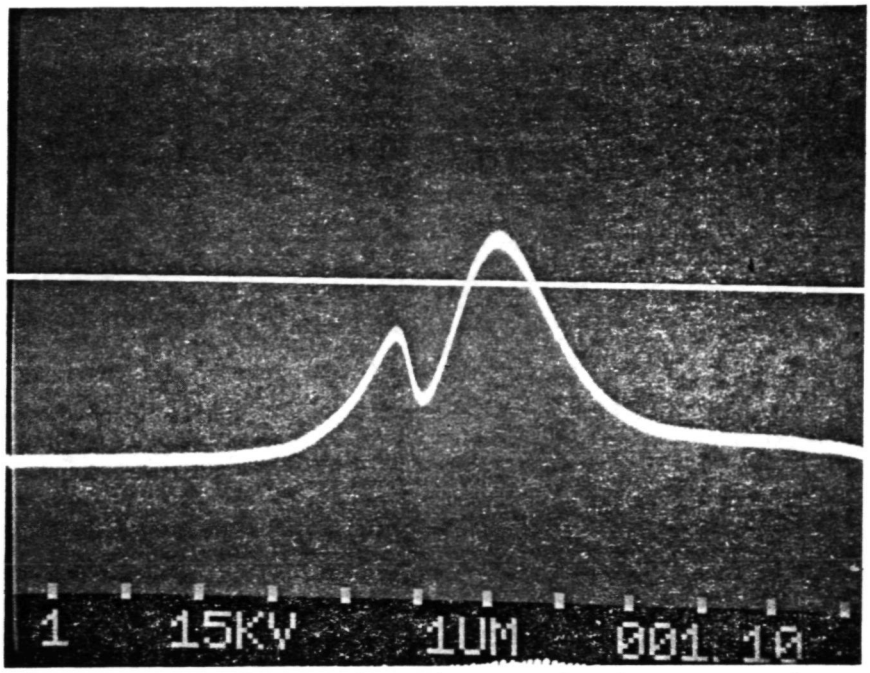

Figure 58. SE/EBIC Line Micrograph of 2N2905, S/N S Emitter Diffusion Depth. (Current from base with emitter and collector at ground. E_B = 15 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 10,000.)

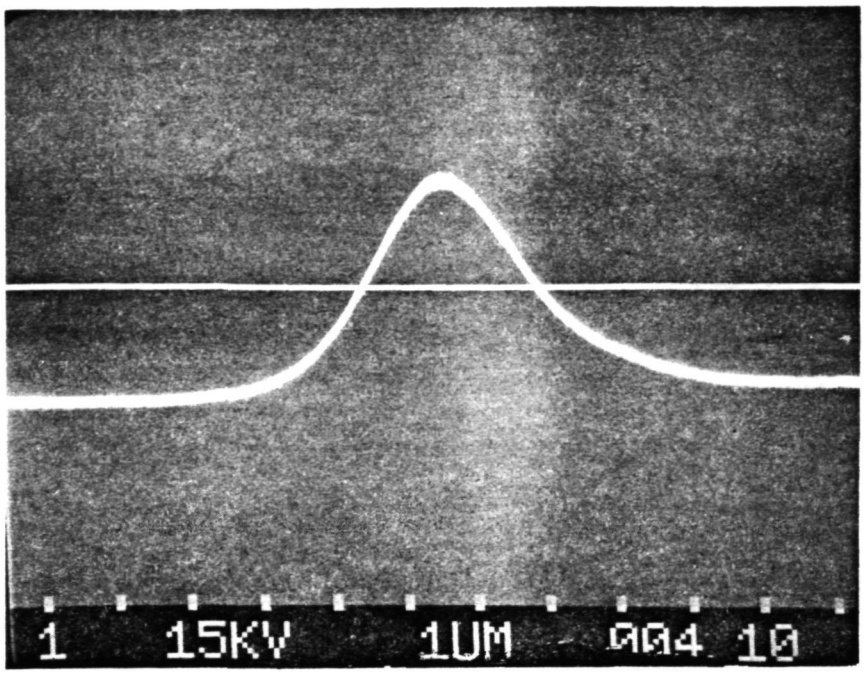

Figure 59. SE/EBIC Line Micrograph of 2N3720, S/N E Emitter Diffusion Depth. (Current from base with emitter and collector at ground. E_B = 15 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 10,000.)

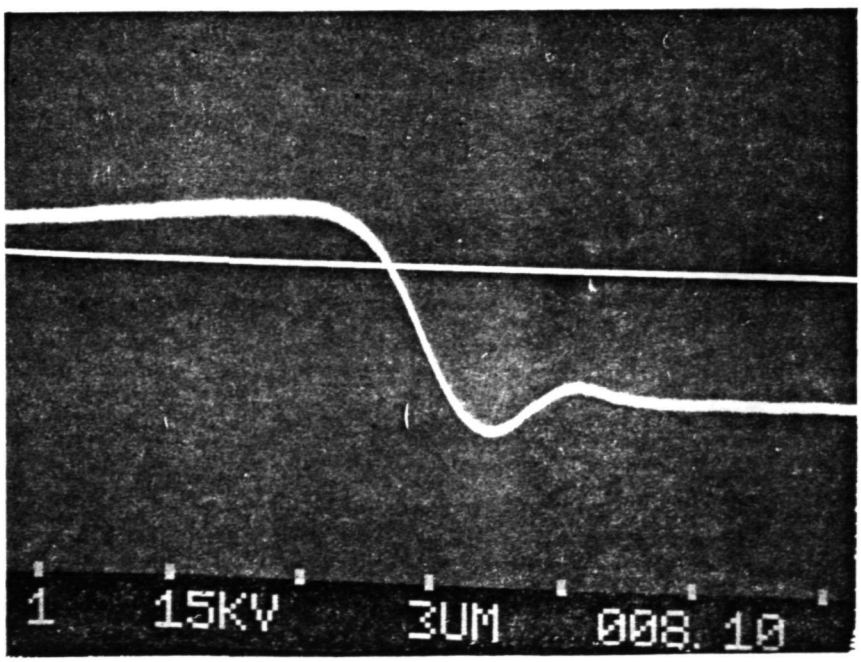

Figure 60. SE/EBIC Line Micrograph of 2N3720 S/N F Base Diffusion Depth. (Current from base with emitter and collector at ground. E_B = 15 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 6000.)

Table 17. Tabulated Data from Microsection and EBIC Diffusion Depth Measurements

Sample Type & No.	Emitter Measurement, μm	Base Measurement, μm	Angle of Section, deg	Microsection Diffusion Depth, μm		EBIC Diffusion Depth, μm		Error Microsection to EBIC, %	
				Emitter	Base	Emitter	Base	Emitter	Base
2N2905									
R	7.4	10.1	22	2.77	3.78	1.55	-	-44	-
S	11.0	15.6	13.7	2.61	3.69	1.36	-	-48	
T	6.9	10.1	19.5	2.30	3.37	1.29	-	-44	
2N3720									
D	14.2	20.1	14	3.44	4.86	1.30	4.15	-62	-15
E	20.2	27.6	11.5	4.03	5.50	1.48	4.36	-63	-21
F	18.8	36.6	10.5	3.43	6.67	1.73	4.41	-50	-34

The measurement technique appears to be a valid approach to diffusion depth measurement; however, for this to become a reality, the diffusion variables must be defined. The diffusion variables must then be evaluated to determine if they can be practically related to this application.

5. Metalization Integrity Evaluation at Oxide Steps

The need for this application arose from the limitations experienced with the existing inspection method. The SE image provides a high resolution visual display of the physical surface. The acceptability of metalization coverage at oxide steps can be qualitatively judged using this method. It has proved to be a valuable method for screening lot-related defects and eliminating metalization failure at oxide steps. The limitation of this method is in the marginal or questionable area of acceptability. In this area it many times is difficult, if not impossible, to make a judgement based on the surface appearance. For some cases a conservative position is to judge the lot unacceptable. In other cases the lot may be judged acceptable. The point is the decision can have serious and expensive consequences if the decision is incorrect. Program delays can occur if good parts are rejected and system failures can result from accepting bad parts. From this experience it was obvious that the ability to further evaluate the metalization integrity would be invaluable. In addition to this application the ability to measure variations in film thickness would be valuable in other applications.

The principal for this measurement is based on the electron range for a given acceleration voltage in a material of known density. As an electron beam is moved from point to point on a film having variations in its thickness, the quantity of electrons capable of penetrating the film will vary inversely with the film thickness. Measurement of the penetration electron quantities, in conjunction with beam energy and current, should be related to film thickness.

Literature related to electron range and energy dissipation in solids was reviewed. The electron range equations were studied and electron ranges were calculated for typical semiconductor film thicknesses. Experimental measurements with different acceleration voltages were made using test transistors and these data were evaluated for possible correlation to film thickness. This was unsuccessful. A discussion of this evaluation showed that the effects of junction diffusion length on the EBIC level had not been considered. (Ref. 8). Junction diffusion length is a variable that has to be determined for each device before film thickness measurement. This was considered to be impractical.

A review of the literature identified two previous studies that described film thickness measurement techniques. One of the studies described an approach to measuring films on semiconductors (Ref 7). The study shows that film thicknesses could be approximated through the relation of recombination current gain and acceleration voltage. This gain was the ratio of recombination current to beam current. An intercept voltage was extrapolated from a plot of gain versus acceleration voltage. The intercept voltage is representative of the acceleration voltage where the gain approaches zero. The intercept voltage is then used to derive an electron range using a range equation. The film thickness is derived from the electron range.

Sample measurements were made for test transitors using this approach Evaluation of these data showed reasonable correlation to estimated oxide and aluminum film thicknesses. A test program was developed to better define the approach and evaluate the measurement repeatability and accuracy. Transistors were primarily used in this test program to eliminate the possibility of inter-circuit effects of ICs on measurement accuracy. The transistor SiO_2 and Aℓ film thicknesses were measured by stylus profilometry. The stylus tip radius was 0.25 cm and the stylus force was approximately 15 milligrams. Recombination current gains were measured at specific points on the SiO_2 and Aℓ film for different acceleration voltages. The beam current was maintained at a value near 1×10^{-10}A and was measured for each test measurement point. The gain versus acceleration voltage data were evaluated by least squares linear regression to determine the intercept voltage. The electron range was calculated using the intercept voltage and range equations in Figures 61 and 62. To obtain the average electron range the calculated electron range was multiplied by 0.5. The average electron range should be more representative of the measured film thickness. The profilometry data were compared to the calculated electron range data and the average electron range data. The percent of deviation was calculated for the profilometry thickness to electron range data. EBIC measurements were repeated to evaluate the repeatability. These data are contained in Table 18. The acceleration voltage measurement points were varied in quantity and voltage range to evaluate the sensitivity of the measurement to these factors.

A review of the measurement data revealed some interesting points. The measurement of six points over a 5 kV range gave good results. The least squares error fit for the six data points typically were 0.999. The acceleration voltage range used should provide a recombination current gain of greater than 500 if possible. Below this gain level the gain versus acceleration voltage becomes nonlinear. This point can be better appreciated from a plot of gain versus acceleration voltage. See Figure 63. A plot of the data can be an aid for locating data errors. A poor least squares fit may be due to a data point error. Current measurements were made using

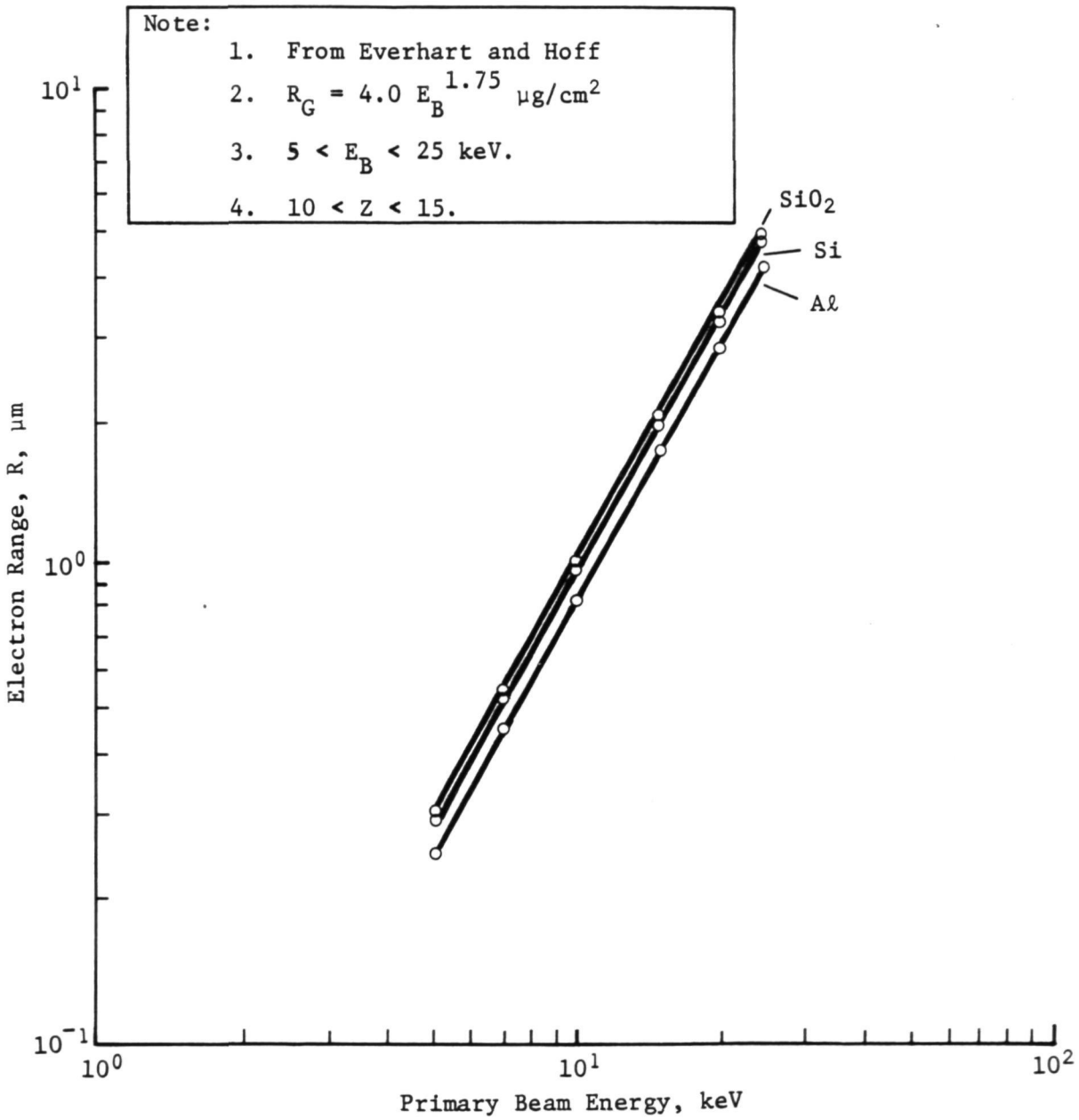

Figure 61. Electron Range (R) Versus Primary Beam Energy

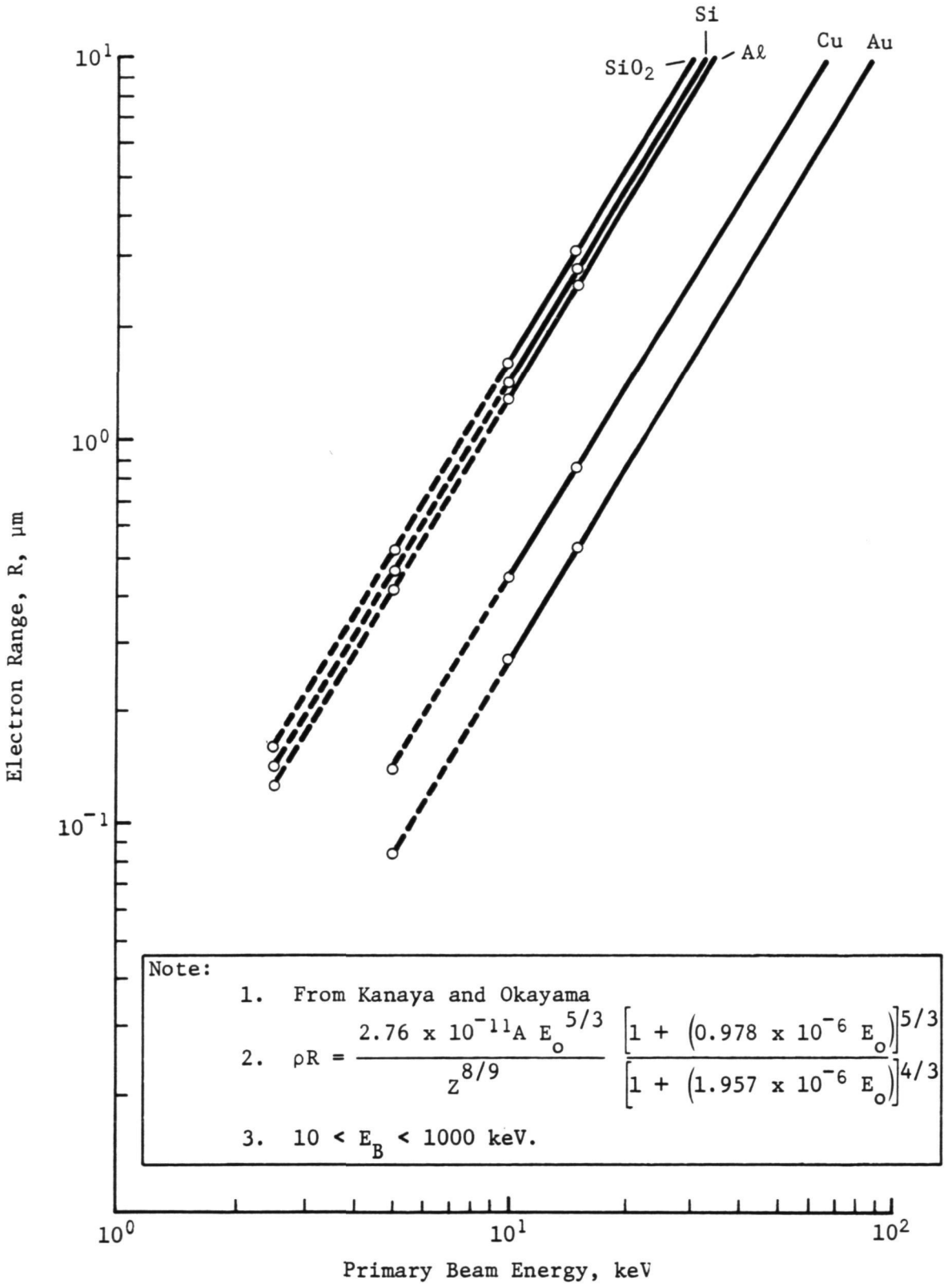

Figure 62. Electron Range (R) Versus Primary Beam Energy

*Table 18 EBIC Film Thickness Measurement Data**

Measurement Run Number	Region Measured	Profilometry Measurement	K&O Range	Deviation, %	K&O Range/2	Deviation, %	E&H Range	Deviation, %	E&H Range/2	Deviation, %	Acceleration Voltage Points Measured
2N2905 S/N X_2											
1	Base Oxide	7213	20395	183	10198	41	12528	74	6264	-13	15, 20, & 25 kV
2	Base Oxide	7213	20015	177	10008	39	12282	70	6141	-15	15, 20, 25, 30, & 35 kV
2	Base Oxide	7213	20572	185	10286	43	12643	75	6322	-12	15, 20, 25, 30, & 35 kV
2	Base Oxide	7213	20135	179	10086	40	12360	71	6180	-14	15, 20, 25, 30, & 35 kV
2N2905 S/N X											
1	Base Oxide	11176	25764	139	12882	15	16040	44	8020	-28	15, 20, 25, & 30 kV
1	Base Aℓ	9652	18721	94	9361	-3	12278	27	6139	-36	15, 20, 25, & 30 kV
2	Base Oxide	11176	26343	136	13172	18	16421	47	8211	-27	15, 20, 25, 30, & 35 kV
2	Base Oxide	11176	24384	118	12192	9	15132	35	7566	-32	15, 20, 25, 30, & 35 kV
2	Base Aℓ	9652	19288	100	9644	-0.1	12672	31	6336	-34	15, 20, 25, 30, & 35 kV
3	Base Oxide	11176	25803	131	12901	15	16065	44	8033	-28	25, 26, 27, 28, 29, & 30 kV
3	Base Aℓ	9652	19162	99	9581	-0.1	12585	30	6292	-35	25, 26, 27, 28, 29, & 30 kV
4	Base Oxide	11176	27342	144	13671	22	17081	53	8541	-24	25, 26, 27, 28, 29, & 30 kV
4	Base Aℓ	9652	21096	119	10548	9	10916	13	5458	-43	25, 26, 27, 28, 29, & 30 kV
2N2905 S/N E											
1	Base Oxide	8940	17813	99	8907	-0.4	10859	21	5430	-39	15, 20, 25, 30, & 35 kV
1	Base Aℓ	13572	27874	106	13937	3	18711	38	9356	-31	15, 20, 25, 30, & 35 kV
2	Base Oxide	8940	19342	116	9671	8	11486	33	5743	-36	25, 26, 27, 28, 29, & 30 kV
2	Base Oxide	8940	18687	109	9344	5	11422	28	5711	-36	15, 20, 25, 26, 27, 28, 29, 30, & 35 kV
2	Base Aℓ	13572	31749	135	15875	18	21478	59	10739	-21	25, 26, 27, 28, 29, & 30 kV
2	Base Aℓ	13572	27501	104	13751	2	18445	37	9223	-32	15, 20, 25, 26, 27, 28, 29, 30, & 35 kV
2N2905 S/N P											
1	Base Oxide	7315	22117	202	11059	51	13649	87	6825	-7	15, 20, 25, 30, & 35 kV
1	Base Aℓ	11379	24380	114	12140	7	16237	43	8119	-29	15, 20, 25, 30, & 35 kV
2	Base Oxide	7315	23769	225	11885	62	14729	101	7365	0.7	25, 26, 27, 28, 29, & 30 kV
2	Base Aℓ	11379	24215	113	12108	6	16120	42	8060	-29	25, 26, 27, 28, 29, & 30 kV
3	Base Oxide	7315	22857	212	11429	56	14132	93	7066	-3	25, 26, 27, 28, 29, & 30 kV
3	Base Oxide	7315	22755	211	11378	56	14066	92	7033	-4	15, 20, 25, 26, 27, 28, 29, 30, & 35 kV
3	Base Aℓ	11379	25952	128	12976	14	17347	52	8674	-24	25, 26, 27, 28, 29, & 30 kV
3	Base Aℓ	11379	23740	109	11870	4	15785	39	7893	-34	15, 20, 25, 26, 27, 28, 29, 30, & 35 kV

Table 18 (concl)

Measurement Run Number	Region Measured	Profilometry Measurement	K&O Range	Deviation, %	K&O Range/2	Deviation, %	E&H Range	Deviation, %	E&H Range/2	Deviation, %	Acceleration Voltage Points Measured
2N3720 S/N A											
1	Base Oxide	14732	34429	134	17215	17	21801	48	10901	-26	15, 20, 25, 30, & 35 kV
1	Base Aℓ	17475	32073	84	16037	-8	21710	24	10855	-38	15, 20, 25, 30, & 35 kV
2	Base Oxide	14732	35076	138	17538	19	22235	51	11118	-25	25, 26, 27, 28, 29, & 30 kV
2	Base Oxide	14732	41956	185	20978	42	26883	83	13442	-9	15, 20, 25, 26, 27, 28, 29, 30, & 35 kV
2	Base Aℓ	17475	41426	137	20713	19	28482	63	14241	-19	25, 26, 27, 28, 29, & 30 kV
2	Base Aℓ	17475	33500	92	16750	-4	22736	30	11368	-35	15, 20, 25, 26, 27, 28, 29, 30, & 35 kV
2N3720 S/N B											
1	Base Oxide	16358	39369	141	19685	20	25129	54	12565	-23	25, 30, & 35 kV
1	Base Oxide	16358	33037	102	16519	1	20869	28	10435	-36	15, 20, 25, 30, & 35 kV
1	Base Aℓ	21641	40611	88	20306	-6	27887	29	13944	-36	25, 30, & 35 kV
1	Base Aℓ	21641	32183	49	16092	-26	21789	0.7	10895	-50	15, 20, 25, 30, & 35 kV
2	Base Oxide	16358	40324	147	20162	23	25776	58	12888	-21	25, 26, 27, 28, 29, & 30 kV
2	Base Oxide	16358	34375	110	17188	5	21764	33	10882	-33	15, 20, 25, 26, 27, 28, 29, 30, & 35 kV
2	Base Aℓ	21641	41979	94	20990	-3	28886	33	14443	-33	25, 26, 27, 28, 29, & 30 kV
2	Base Aℓ	21641	34420	59	17210	-20	23399	8	11670	-46	15, 20, 25, 26, 27, 28, 29, 30, & 35 kV
2N3720 S/N 1											
1	Base Oxide	14224	37051	160	18526	30	23564	66	11782	-17	25, 30, & 35 kV
1	Base Oxide	14224	31749	123	15875	12	20008	41	10004	-30	15, 20, 25, 30, & 35 kV
1	Base Aℓ	15646	37510	140	18755	20	25633	64	12817	-18	25, 30, & 35 kV
1	Base Aℓ	15646	30601	96	15301	-2	20655	32	10328	-34	15, 20, 25, 30, & 35 kV
2	Base Oxide	14224	38192	169	19096	34	24333	71	12167	-14	25, 26, 27, 28, 29, & 30 kV
2	Base Oxide	14224	32468	128	16234	14	20488	44	10244	-28	15, 20, 25, 26, 27, 28, 29, 30, & 35 kV
2	Base Aℓ	15646	38373	145	19187	23	26259	69	13130	-16	25, 26, 27, 28, 29, & 30 kV
2	Base Aℓ	15646	28319	81	14160	-10	19027	22	9514	-39	15, 20, 25, 26, 27, 28, 29, 30, & 35 kV

*Values are given in angstroms.

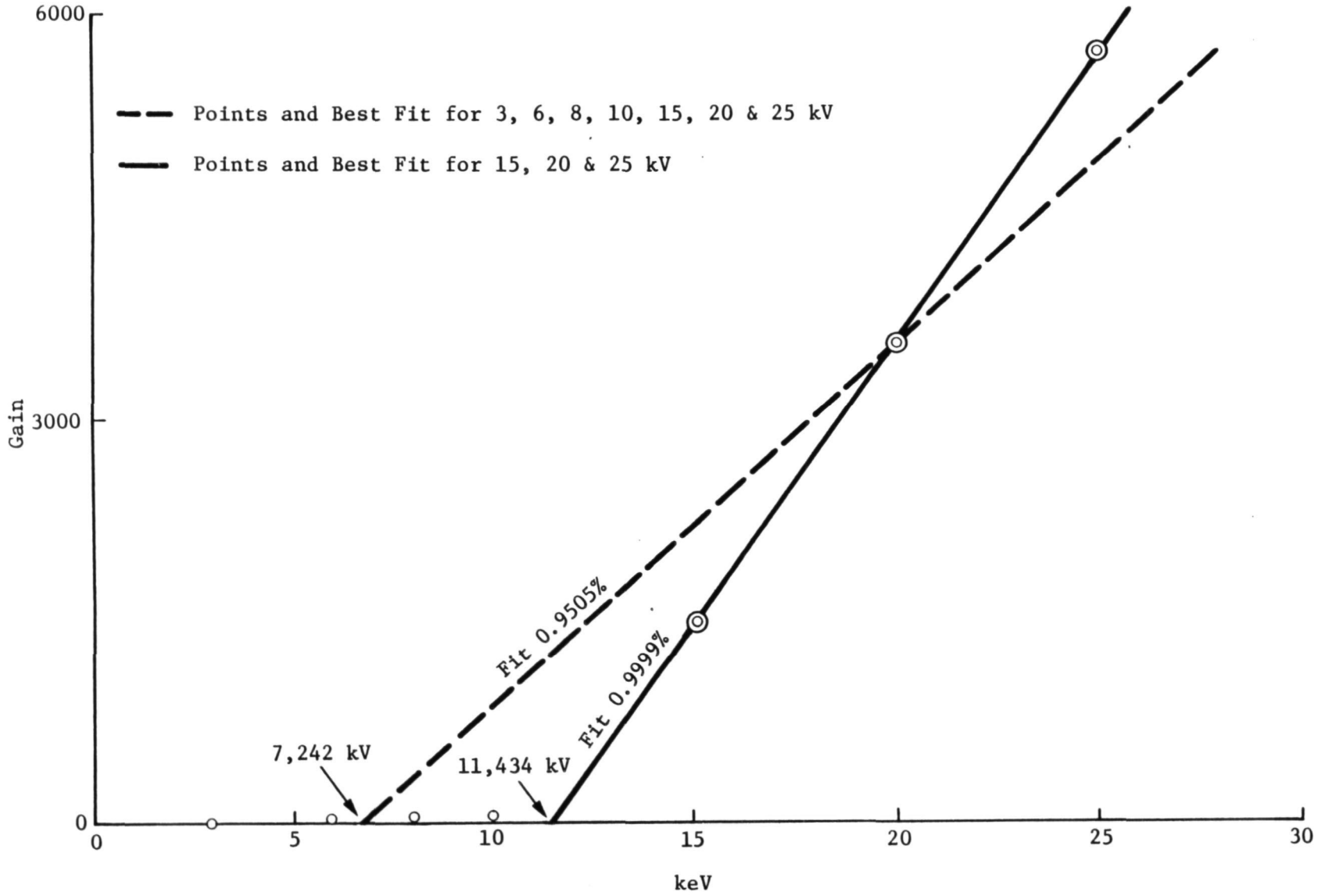

Figure 63. Gain Versus Acceleration Voltage

both an external current meter and the SEM current meter. The results were the same. The deviation percentages were statistically evaluated for the four calculated range groups (Kanaya & Okayama and Everhart & Hoff range equations). The results were as follows for 49 data points.

	$\bar{X}$(%)	σ
K&O*	130	40
K&O/2	15	20
E&H**	48	23
E&H/2	-26	11.5

*See Figure 61.
**See Figure 62.

The K&O/2 range shows the best statistical accuracy. The percent error spread for K&O/2 and E&H/2 were 62 to -26% and +0.7 to -50% respectively. Thickness measurements were made on an integrated current. The first circuit was a 54L95 4-bit shift register. The EBIC gain versus acceleration voltage relation exhibited a nearly constant gain value. This was suspected to be due to Au doping but it was not confirmed. This could be a limiting factor for EBIC applications.

A second circuit selected was a 54L04 hex inverter. A surface profile measurement was made of the die surface. This die has a Au metallization system and is glass passivated. EBIC thickness measurements were taken at 11 locations on the die. The profile thickness to EBIC thickness comparison errors were not calculated. This would require a detailed analysis of the oxide layer thicknesses and conductor material composition and thicknesses. The conductor metallization contains layers of different metals/densities that would require a rigorous analysis to identify its effective density. The multiple metal systems could present complex problems to EBIC thickness measurement. The EBIC measurements for this device was found to be feasible and there were no internal circuit affects noted. The evaluation of other circuit types has shown EBIC measurement to be feasible; however, further study is needed to better understand the interferances of semiconductor processes and adjacent circuit current paths.

The reason for modifying the calculated electron range is to normalize the range from a maximum or practical range to an average range. The range equations derive the practical or maximum ranges. Only a minority of the primary electrons reach this depth; therefore, the electron range was normalized to approximate the average range for a primary electron. The factor of 0.5 was a first order approximation based on a spherical energy dissipation volume. The

relative energy dissipation versus depth has been derived by Everhart and Hoff (Ref 5). The integral

$$\int\lambda(Y) = \int 0.60 + 6.21Y - 12.40Y^2 + 5.69Y^3$$

was evaluated to determine the energy dissipation 50% point (Ref 8). The evaluation showed that the 50% energy dissipation point occurs at 40% of the calculated electron range. This indicates that, for normalizing the calculated electron range to estimated film thickness, the correction factor, 0.4, is a better approximation.

The measurement procedure is not complicated and the time required to perform measurements on the SEM are reasonable. Measurements for four locations on a device at six acceleration voltages require approximately one hour. Before starting the measurement procedure it is important to verify the accuracy and linearity of the instruments used in measuring the acceleration voltage and beam current. These instruments are the key indicators for determining the film thickness. The instruments used in this study were within ±5% of reading. An acceleration voltage is selected based on the surface film materials and approximate thicknesses. (Note: If approximate thicknesses are not available the acceleration voltage can be selected on the basis of recombination current gain.) The beam current is set to a desired level, i.e., 1×10^{-10}A, using a Faraday Cup and current meter. (Note: No further adjustments should be made to the electron column that would effect the beam current setting.) The area to be measured is selected on the sample and the image focus is optimized. (Note: No further focus adjustments should be made as it will effect the beam current level. The beam incidence should be approximately perpendicular to the specimen surface.) To help in returning to the same measurement point or points on the specimen, "bench marks" were identified on the visual display CRT face with a china marker. During this study measurements were evaluated using a reduced raster scan at high magnification and a point beam. A reduced raster scan can help to average an irregular surface. On an aluminum film, it is important to return to the same point for each measurement. If the beam location is changed between two adjacent grains that have different thicknesses, this would result in deviations equivalent to these thicknesses. For this study the beam locations were made at X6000 to X10000 magnification. Once the beam is located the EBIC level is recorded with its acceleration voltage. When the selected points have been measured the beam is returned to the Faraday Cup and the beam current is measured and recorded. The beam current level must remain stable during this measurement period. The next acceleration voltage is set and this beam current is set using the Faraday Cup. The procedure is continued until all measurements are made for each voltage.

The EBIC gains are calculated (I_S/I_B). Using the calculated gains and acceleration voltages an acceleration voltage intercept is calculated using the least squares curve fit. This can be performed on most scientific calculators. The expression is

$$a = \frac{\Sigma X_i Y_i - \frac{\Sigma X_i Y_i}{n}}{\Sigma X_i^2 - \frac{(\Sigma X_i)^2}{n}}$$

where a is the intercept ($Y = ax + b$).

It is also helpful to evaluate the "goodness of fit". The expression is

$$r^2 = \frac{\left[\Sigma X_i Y_i - \frac{\Sigma X \Sigma Y}{n}\right]^2}{\left[\Sigma X_i^2 - \frac{(\Sigma X_i)^2}{n}\right]\left[\Sigma Y_i^2 - \frac{(\Sigma Y_i)^2}{n}\right]}$$

where $0 \leq r^2 \leq 1$ and $r^2 = 1$ indicates a perfect fit. The "goodness of fit" typically ranged from 0,99 to 0.999 for this study.

The acceleration voltage intercepts are evaluated using one of the range equations (Figure 61 and 62) and the respective film constants. The calculated electron range is normalized using the correction factor to obtain an estimated film thickness.

A measurement accuracy was not established for this application. This is an area for future study. Until an accuracy can be identified the measured thicknesses should be considered as approximations.

The principles of this application can be described better using qualitative EBIC images. Examples selected were a DTL circuit, a FET, and a 54L04 circuit.

The 930 DTL circuit provides an example of metal coverage at a resistor contact window. Figure 64 shows a SE micrograph of this window area. Figure 65 shows an EBIC micrograph of the same area.

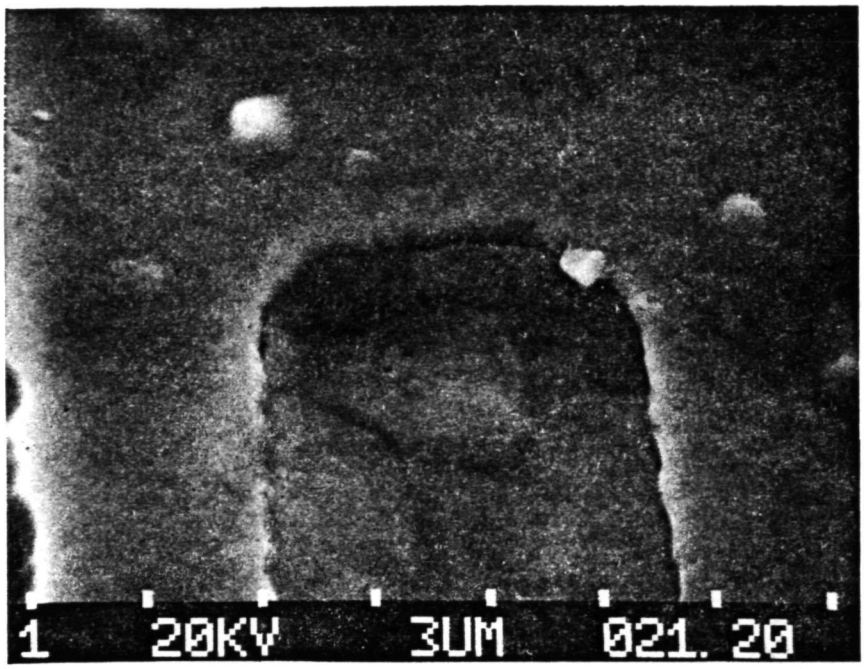

Figure 64. SE Micrograph of Resistor Contact Window on a DTL 930 Circuit. (Mag x 5400.)

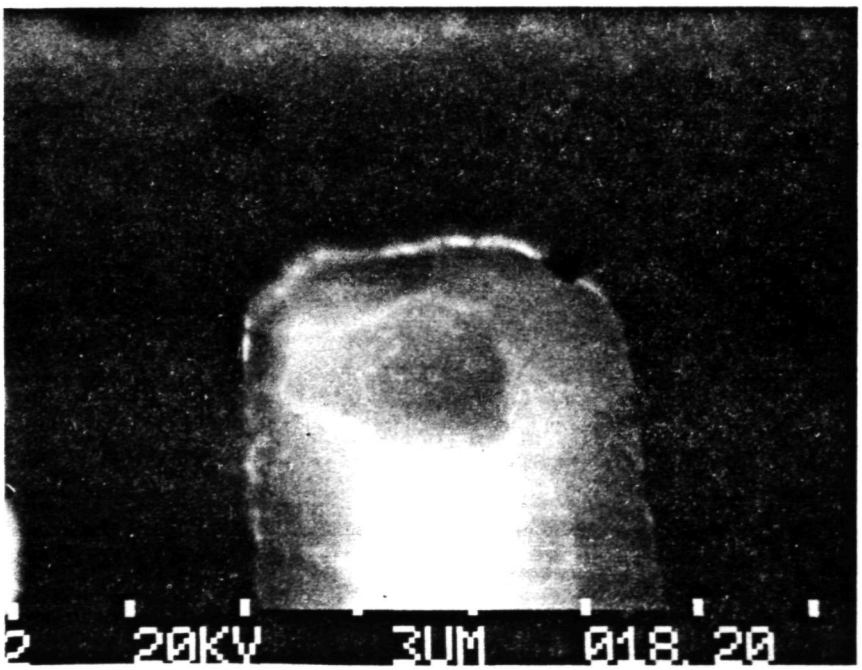

Figure 65. EBIC Micrograph of Same Area Shown in Figure 64. (Current from Pin 14 with Pin 7 at ground. E_B = 20 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 5400.)

Figure 66 shows a Y modulation EBIC micrograph of this area. Note the "knife edge" along the oxide step. Film thickness measured along the step indicated a film thickness decrease of approximately 25%. This does not necessarily imply the metal thickness has only decreased 25% because SiO_2 may be present under the step area. SiO_2 has a density very similar to aluminum; therefore, great care must be exercised in taking these measurements.

A 2N5196 junction FET provides a second example of metalization coverage at an oxide step. Figure 67 shows a SE micrograph of this step. Figure 68 is an EBIC micrograph of this area and Figure 69 is a Y modulation EBIC micrograph. The "knife edge" can be seen in this micrograph also. Figure 70 shows an EBIC line scan superimposed on the SE image. Figure 71 is a SE micrograph of the step area at X10,000.

A 54L04 circuit provides the third example. This is a glass passivated die with Au metallization. Higher acceleration voltages are required for electron penetration of the Au metalization. Figure 72 is a SE image showing one of the transistors. Figure 73 is an EBIC line scan superimposed on a SE image. The line scan does not show a deflection at the base/collector junction. Figure 74 shows this is due to the EBIC signal only being measured from the emitter diffusion. This application is also limited by the accesibility to diffused regions.

This application can also be used to quantitatively determine the degree of oxide defect involvement. Measurement is possible for areas beneath metalization except for high density metals such as Au where the oxide-to-metal ratio of energy dissipation is very low. Some of the measurement error (profilometry to EBIC) was due to variations in film thicknesses between the profilometer and EBIC measurement sites. The data from this study show that the normalized E&H thickness measurement will provide a conservative estimate of film thickness. The measurement accuracy should realize an improvement with further study.

The principles of EBIC generation and methods for application were presented. The application methods for oxide and junction defect identification and metal integrity evaluation are described. The development of applications for locating surface leakage and diffusion depth measurement was unsuccessful.

The EBIC resolution and sensitivity are impressive and provide a capability for these areas of application that is unprecedented. The improvements in detection and evaluation will result in greater semiconductor reliability.

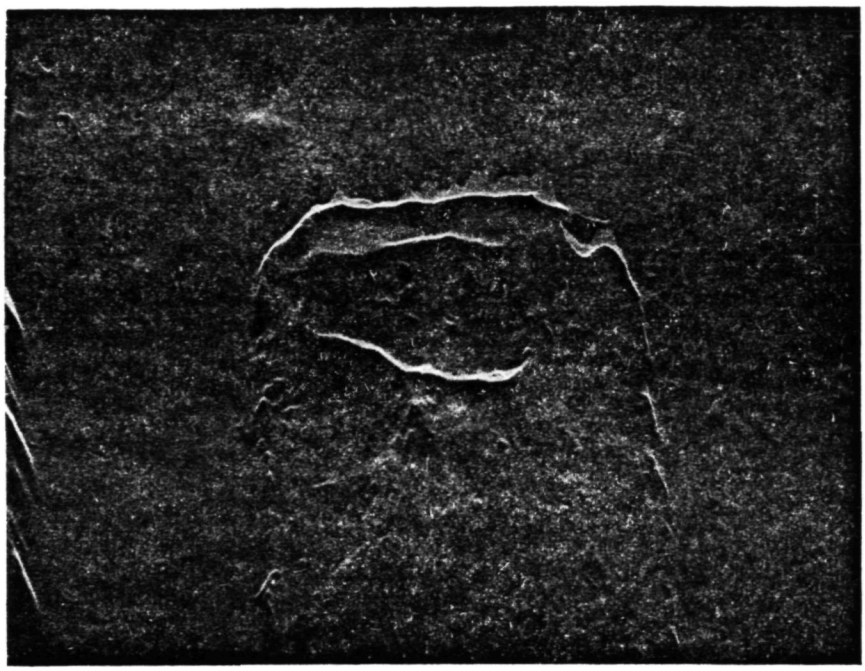

Figure 66. Y Modulation EBIC Micrograph of Same Area Shown in Figure 64. (Current from Pin 14 with Pin 7 at ground. E_B = 20 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 5400.)

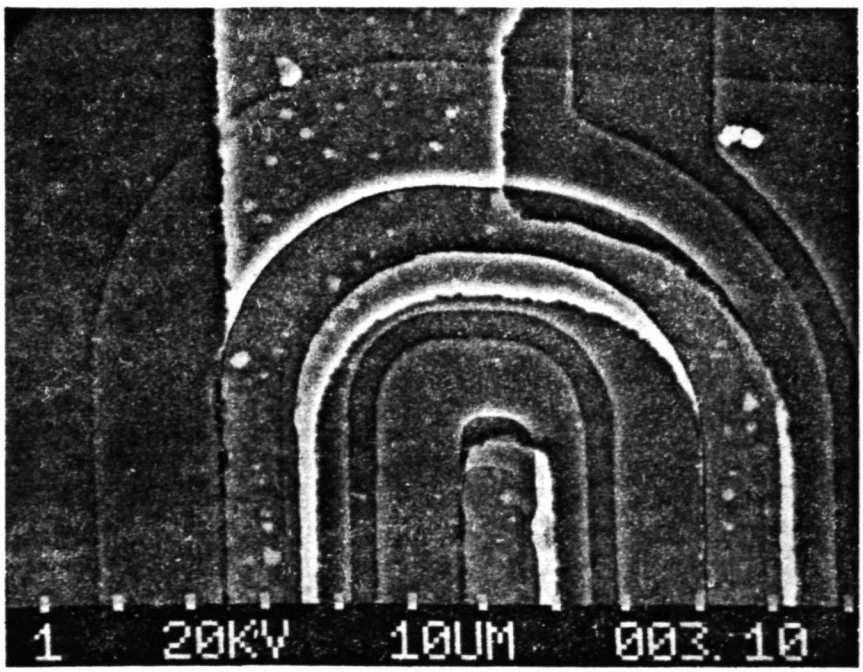

Figure 67. SE Micrograph of Drain Metalization Contact on a 2N5196 FET. (Mag x 1000.)

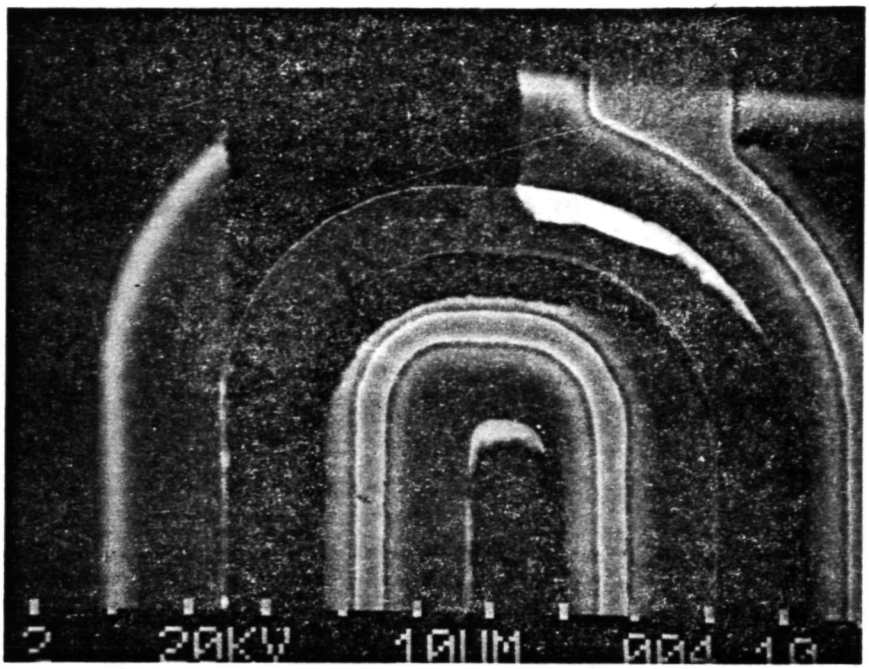

Figure 68. EBIC Micrograph of 2N5196 FET. (Current from drain with gate at ground and source open. E_B = 20 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 1000.)

Figure 69. Y Modulation EBIC Micrograph of Same Area and Conditions as Shown in Figure 68. (The oxide step is located by arrow. Mag x 1000.)

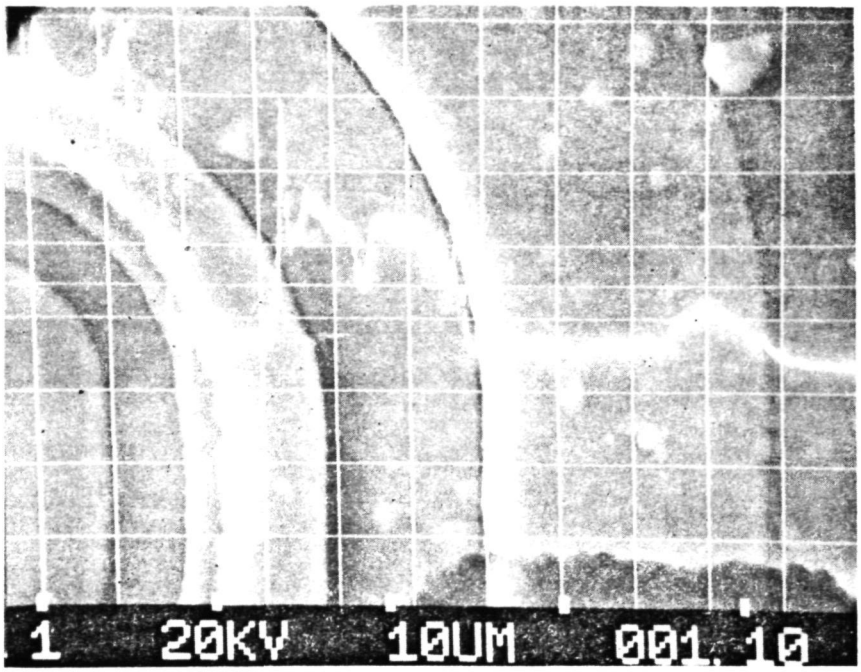

Figure 70. EBIC Line Scan Superimposed on SE Image. (This provides better correlation for the line scan, Mag x 2400.)

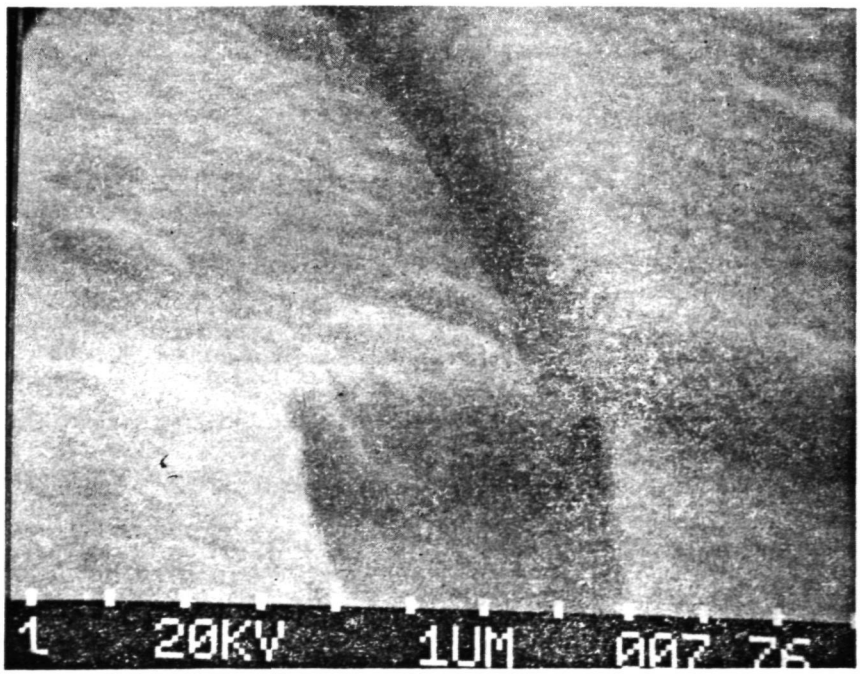

Figure 71. SE Micrograph of Metal Coverage at this Oxide Step. (Mag x 10,000.)

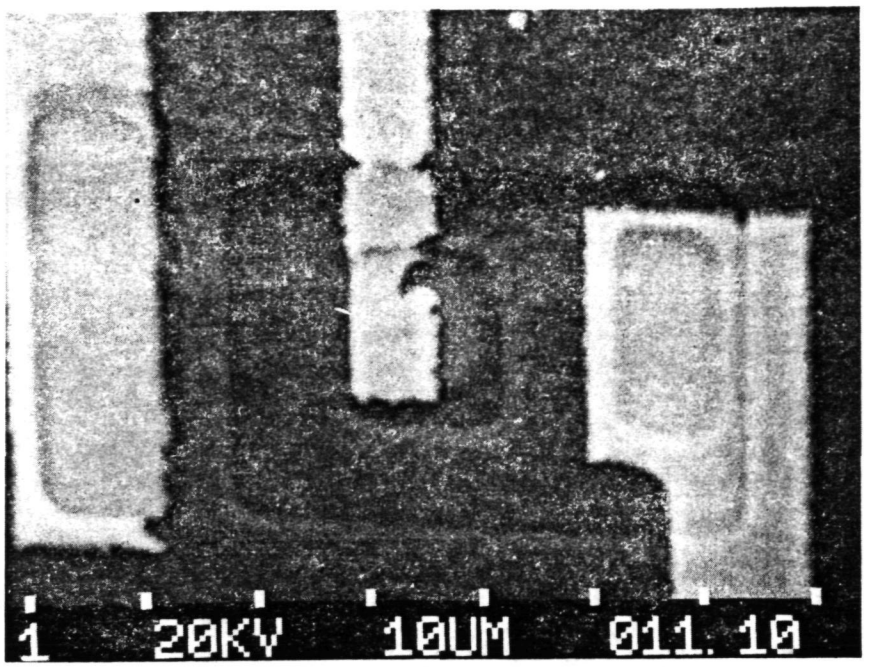

Figure 72. SE Micrograph of a Transistor in a 54L04 Circuit. (This circuit is glass passivated. Mag x 1600.)

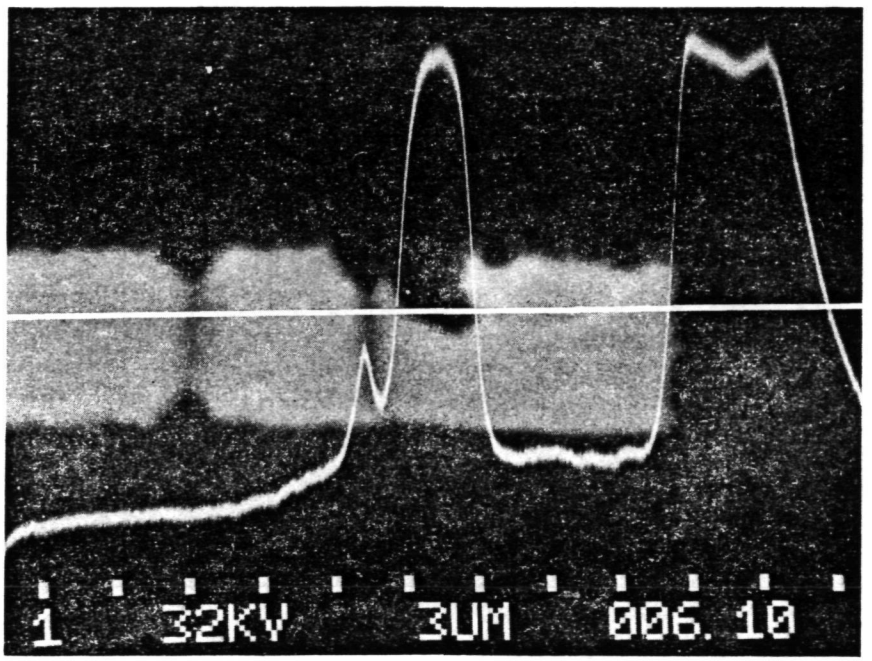

Figure 73. EBIC line scan Superimposed on SE Image. (This shows the relative EBIC current variations for the Au metallization. Current from Pin 11 with Pin 4 at ground. E_B = 32 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 3600.)

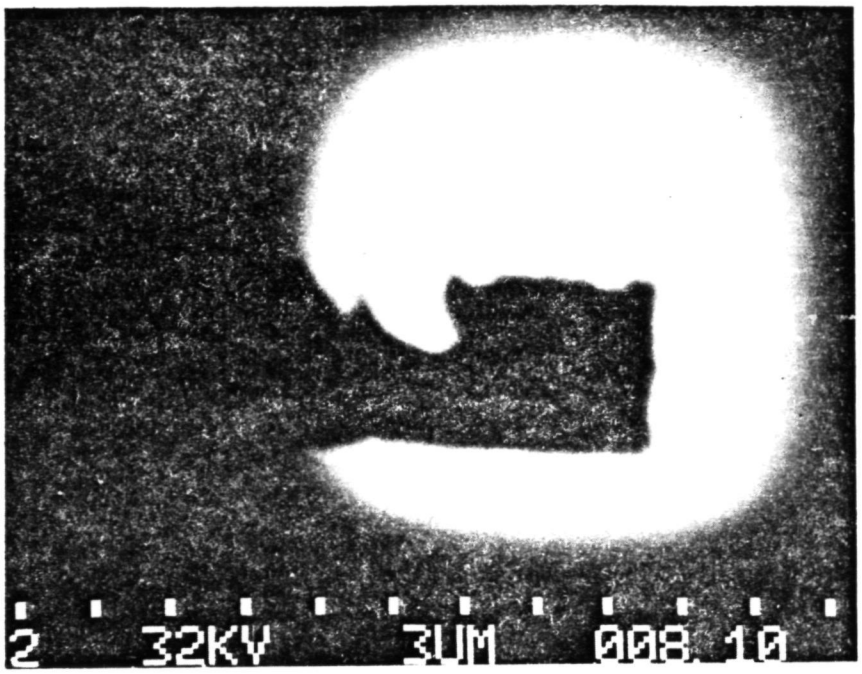

Figure 74. EBIC Micrograph of Emitter Diffusion. (This shows why only one oxide step transition can be seen in Figure 73. The other is located over the base region where EBIC is not being measured. Mag x 3600.)

All EBIC applications described, except for metalization integrity, requires as a minimum, a SEM equipped with a specimen current amplifier capable of imaging a range of 10^{-7} to 10^{-10}A. The application of metalization integrity requires only a current measurement capability. The addition of Y deflection modulation and line scan provide an improved image display capability. Small image contrast variations are more difficult to resolve visually on an intensity-modulated display. These subtle contrast variations can be enhanced for easy detection using Y modulation and line scan display modes.

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V. VOLTAGE CONTRAST APPLICATION TECHNIQUES

Voltage contrast has been widely used in the study and isolation of failures in semiconductors. Voltage potentials on a semiconductor surface produce variations in the detected secondary electron signal. This results in a displayed image containing contrast variations that are representative of voltage levels present on the test specimen. The contrast level-to-test specimen voltage potential relation is nonlinear without special SEM modification. Therefore voltage contrast applications provide quantitative data. The resolution for voltage contrast can approach 0.25 V but this is very dependent on the test specimen surface, immediate area of the specimen, and the electron beam parameters.

A positive potential on a specimen surface will attract and capture the majority of secondary electrons having an equivalent energy of up to the applied potential. For example, if 10 V were applied to the specimen surface, secondary electrons having 10 eV or less energy would probably be captured in the immediate area of emission. For a negative potential on a specimen surface, the secondary electron emission level is enhanced. Electrons that could not escape on a zero-V surface are assisted by the presence of a negative potential. The effect on the SE image is that a positive potential causes a decrease in image brightness and a negative potential causes an increase in brightness. The energy range for secondary electrons is, by definition, 0 to 50 eV. Therefore relatively low potentials can greatly influence the number of detected secondary electrons. This is an important point to remember for all SE image applications.

The interconnection of external voltages to the test specimen was discussed earlier. A part of the interconnection circuitry is the prevention of charge accumulation. If nonconductive surfaces are not minimized in the area of the test specimen, charges are likely to build up and severely influence the SE signal. These surfaces will charge more rapidly if the electron beam is allowed to strike these surfaces. Voltage contrast can be completely lost by surface charge accumulation.

A. DIFFUSION DEPTH MEASUREMENT

The measurement of diffusion depth from the surface was investigated using voltage contrast. For this application the junction would be located by the contrast transistion boundary. The approach used here has the same fault as experienced for EBIC, i.e., unequal vertical-to-horizontal diffusion distances. The measurement using voltage contrast exhibited two additional problems. The applied voltage effect on the junction depletion region must be factored into the measurement. This further complicates the measurement. Also the contrast transition boundary was found to

be very difficult to locate at magnifications above X5000. To delineate the P-N junction by voltage contrast, the electrons must penetrate the surface passivation layer. Based on these findings, measurement by EBIC would appear to be the better method for further development.

B. SURFACE LEAKAGE

This investigation was conducted in conjunction with the EBIC investigation of surface leakage. The dissipation of a trapped charge on a semiconductor surface due to electron bombardment would also apply for voltage contrast. Therefore the application of voltage contrast for locating surface inversion does not appear to be feasible.

The location of surface leakage paths that result from conductive residue or thin conductive films would be possible. The application of a voltage across the leakage path would produce a variation in contrast. Secondary emission depths are typically 100 Å from the surface. Therefore it would seem possible that contamination films in the area of 500 Å or less may be located. Test specimens exhibiting surface leakage due to contamination were not available for this study. This application requires further study to determine the detection parameters.

C. FUNCTIONAL CIRCUIT TESTING

This application of voltage contrast is very familiar to SEM operators and in particular to failure analysts. Functional circuit examination has been widely utilized as a visual troubleshooting tool in failure isolation. This investigation will primarily address applications related to circuit failure isolation. The principal goals for failure isolation are to minimize the risk of damage to the circuit and to develop methods that can be routinely utilized.

Some of the questions addressed are:

-What voltage contrast display modes are available and what are some of the advantages and disadvantages?

-How can electrical degradation of the test sample be avoided?

-How can the electron beam influence circuit operation?

-Do glass passivation layers have to be removed for functional circuit observation?

Many of the answers to these questions are directly related to the factors of electron range and energy dissipation in the semiconductor surface.

Three voltage contrast display modes will be described. They are image contrast modulation by low frequency, beat frequency and stroboscopic excitation. Low frequency contrast modulation utilizes pulse excitation frequencies of less than 1000 Hz. A circuit excitation frequency is selected to provide the desired resolution of circuit function. Different excitation frequencies can be applied to circuit inputs to obtain visual separation of the circuits. The frequency depends on circuit complexity, magnification, and frame period. A functional circuit image can be viewed at slow scan and TV scan rates and recorded on film.

The beat frequency-generated image utilizes excitation frequencies that are multiples of the frame or line scan frequencies. The stability of the excitation frequency is critical and therefore should be synchronized with the SEM sweep generator. The excitation frequency must be adjusted whenever the sweep rates are changed. The use of different frequencies is complicated by harmonic mixing in the test circuit. A functional circuit image can be viewed at slow scan and TV scan rates and recorded on film. Beat frequency synchronization requires increased setup time.

Stroboscopic voltage contrast requires excitation and electron beam synchronization and control circuits. As its name implies, a "stop action" image is displayed with the circuit actually operating at high frequency rates. Stroboscopic imaging provides the ability to view the circuit operation at its normal operating frequency. Digital circuit switching transistions can be observed incrementally by controlling the phase relation between the electron beam and circuit excitation frequency. The principle of SEM stroboscopy is that the electron beam is pulse-modulated in synchronization with a specific test circuit event. In effect the circuit voltage contrast signal is being continually sampled at a specific logic state or segment thereof. The electron beam is turned off or blanked by deflecting it off axis. Beam blanking response times are typically 500 ns or less. As stroboscopy is a sampling technique, circuits have been observed while operating at frequencies above 10 GHz. As the sampling period is decreased, the SE signal and signal-to-noise ratios also decrease. Stroboscopic SEM imaging is a dynamic imaging mode and therefore can only be viewed using TV scan rates and recorded by video tape recording. The SEM also must be equipped with electron beam blanking. Being a sampling technique, stroboscopic imaging is comparable to that of dc voltage contrast. Therefore voltage contrast imaging of devices having glass passivation is not practical. This is also due, in part to the decreased SE signal-to-noise ratios.

To stay with the original goals of developing applications that require a minimum of additional SEM modifications and that minimize the requirements for specimen preparation and risk of damage to the test specimen, these voltage contrast applications will basically apply to low frequency and beat frequency imaging. The procedures for these imaging modes are generally uncomplicated, are flexible to handle most circuits, can be applied routinely, and circuit operation can be photographically documented.

As demonstrated during electron beam irradiation damage, the electrical degradation can practically be eliminated by reducing the acceleration voltage. By decreasing the acceleration voltage, the electron energies are reduced, the electron range is reduced, and the electron energy is dissipated near the oxide surface and removed from the very sensitive Si/SiO_2 interface. The lower acceleration voltages also produce better voltage contrast. The recommended procedure is to initially start at an acceleration voltage of 1 to 2 kV and progress up to obtain the optimum voltage contrast.

Circuit operation can be influenced by the electron beam when the acceleration voltage is sufficient for electron penetration of the oxide. As stated earlier, EBIC gains of 10^3 to 10^4 can be realized. For $I_B = 1 \times 10^{-10}$A, currents on the order of 100 μA can be generated. There are many times where beam currents are much higher and therefore the EBIC would be higher. These levels can produce changes in electrical circuit operation during examination.

Glass passivation layers do not have to be removed to obtain voltage contrast images with ac signal excitation. The voltage contrast for dc levels is lost after a few seconds due to surface charge accumulation on the glass. The examination of failed circuits without requiring the removal of glass passivation reduces the risk of damaging the circuit and the possibility for losing the failure. Also the rate of charge accumulation on the glass depends on the electron beam current. If glass passivation charging is a problem it may be alleviated by reducing the beam current.

Input signals can be different frequencies or can be coded by changing bit patterns. Figure 75 shows a glass passivated CMOS CD 4001 circuit. Different frequencies were applied to the two inputs to provide visual separation of the related circuitry. The frame scan is made from die corner to corner to provide a 45° intercept to the die metalization conductors. Figure 76 is a non-glassed TTL 5473 dual J-K flip-flop circuit. Different frequencies were applied to the J-K inputs and the clock input. The use of low

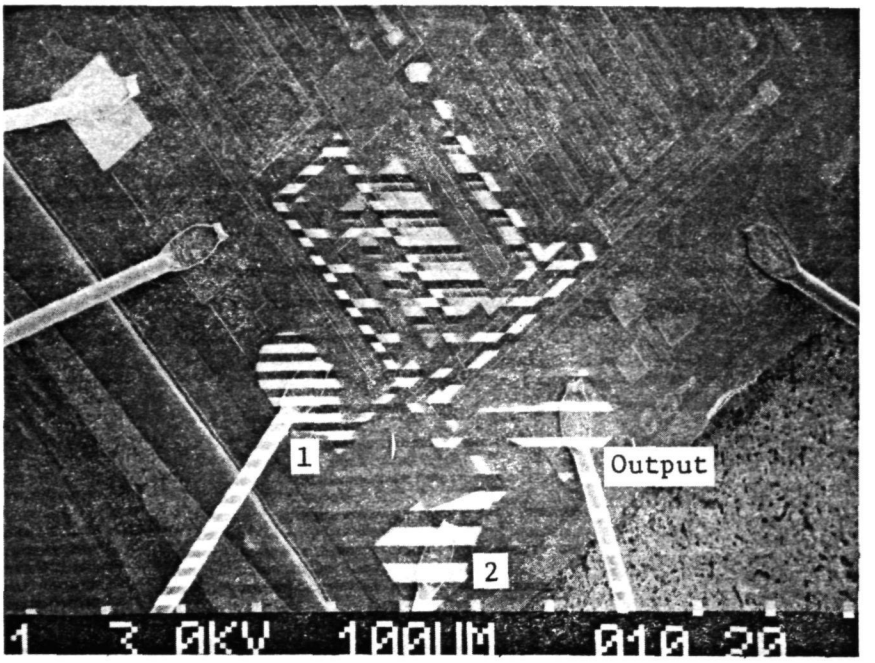

Figure 75. SE V/C Micrograph of CD 4001 Circuit. (The frame period was 30 seconds with Pin 1 input ≈ 10 Hz and Pin 2 ≈ 5.5 Hz. E_B = 3.0 kV, Mag x 100.)

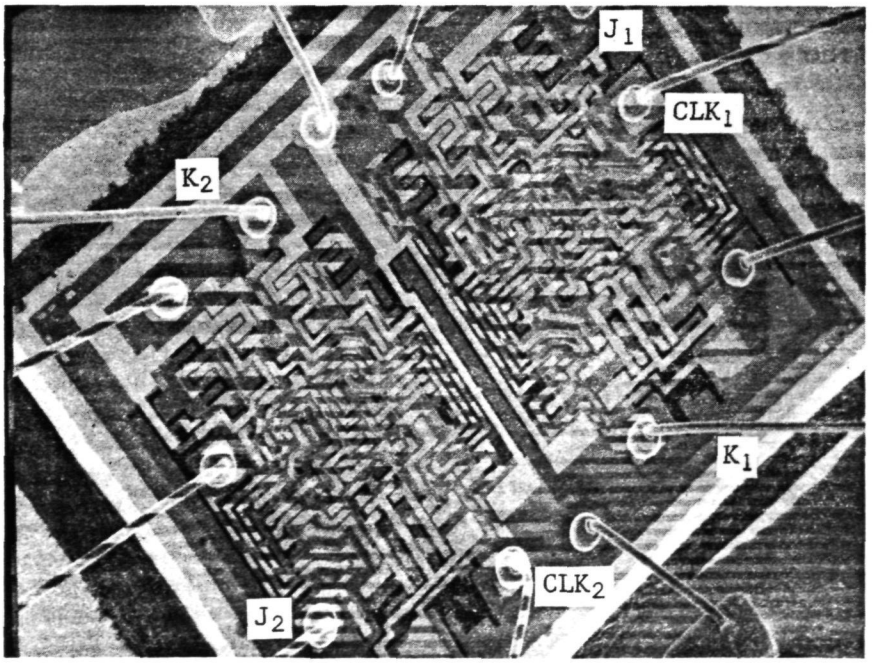

Figure 76. SE V/C Micrograph of 5473 Circuit. (The frame period was 30 seconds with J & K Inputs ≈ 10 Hz and CLK ≈ 5 Hz. E_B = 5 kV, Mag x 60.)

acceleration voltages also improves voltage contrast on Au metalized circuits. Figure 77 is a part of this same circuit showing the voltage contrast patterns. This micrograph looks very "busy" but circuit operation is easily traced using this recording method. Figure 78 shows a micrograph of an IM 5523, 256 x 1 bit ram. A circuit of this complexity is difficult to trace at this magnification. There are two methods for increasing the "visibility" for complex circuits. One is to print a photograph enlargement from a film negative to increase the circuit details. The other method is to make a micrograph(s) of the specific area of failure. This is the more difficult of the two for circuit tracing due to image discontinuities (Figure 79).

The combination of voltage contrast and EBIC provides a powerful tool for failure analysis. A 54L04 TTL Hex Inverter is used as an example. This has a glass passivated die with Au metalization. The inputs for three inverters were subjected to a simulated electrostatic discharge. Figure 80 shows all six inverters are functional at the nominal V_{cc} of 5 V. Electrostatic discharge stress has historically resulted in failure to function at low temperature. Many high and low temperature functional anomalies can be disclosed by increasing and decreasing circuit supply voltages. The V_{cc} level was decreased to 4 V and circuit 1 (pins 2 & 3) failed to function (Figure 81). The V_{cc} level was further reduced to 2.5 V and all three of the stressed inverters failed to function (Figure 82). The isolation of the failure site was made for circuit 1. Figure 83 shows the normal operation of circuit 1 at V_{cc} = 5 V. Figure 84 shows the failed state at V_{cc} = 4 V. Figures 85 and 86 are EBIC images of the failure site in the base/emitter junction of the phase splitter transistor. This damage resulted in decreased beta for the phase splitter transistor. This is one example demonstrating the use of SEM applications for failure isolation and defect location without the need for glass passivation removal or mechanical probing of the die surface. The damage sites for the remaining circuits were also located using these same techniques. These defect sites could not be detected by light microscopy examination.

These application techniques are being used routinely for failure isolation and defect location for all circuit types. This has resulted in eliminating many analytical errors that are incurred during isolation by the previous conventional techniques. It has also reduced the average time for circuit failure analysis. Isolation time can be reduced to up to 90% of the previously required time.

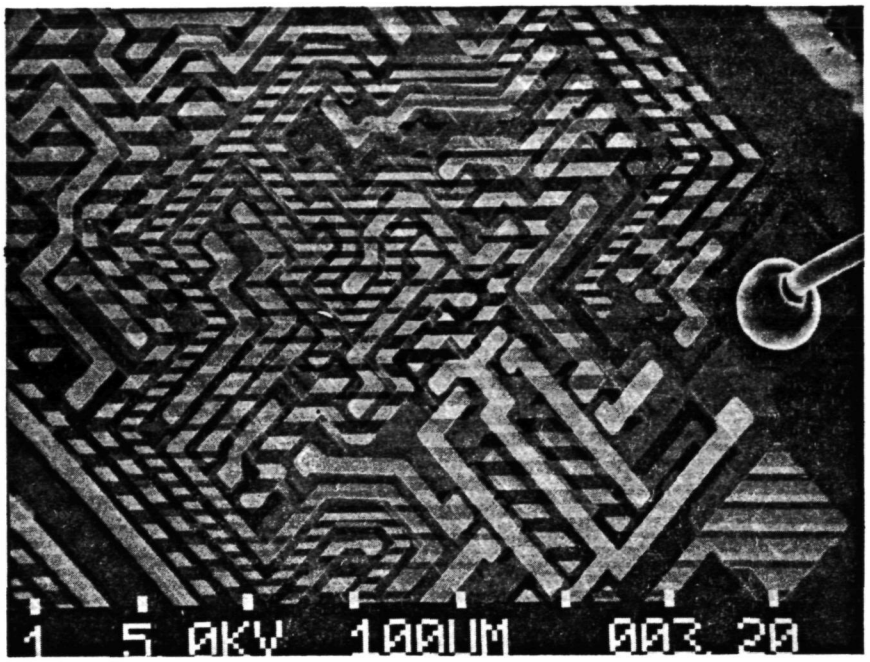

Figure 77. SE V/C Micrograph of 5473 Circuit Showing a Part of Circuit in Figure 76. (E_B = 5 kV, Mag x 150.)

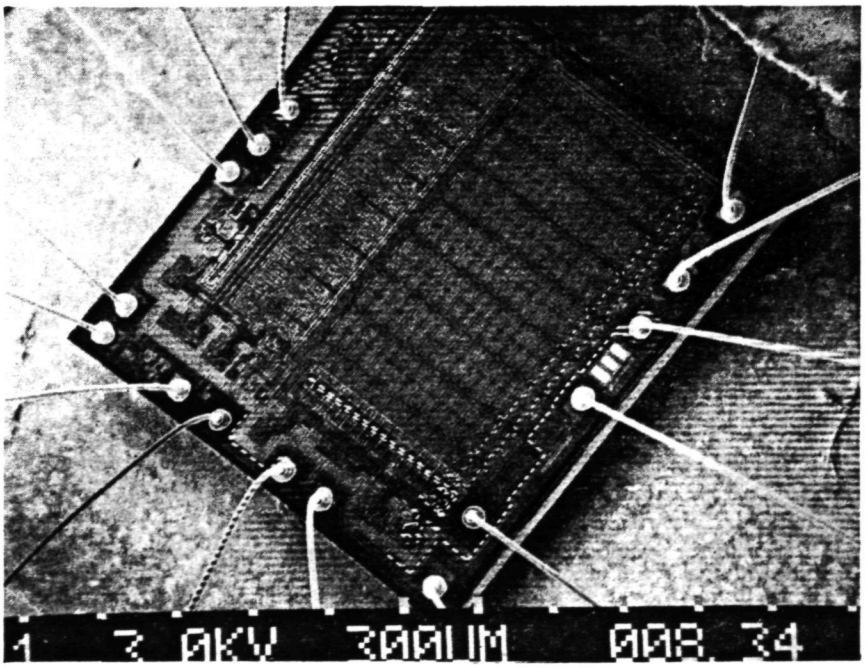

Figure 78. SE V/C Micrograph of an IM 5523 256 x 1 Bit RAM. (A 50 Hz input was applied to two address lines. E_B = 3 kV, Mag x 33.)

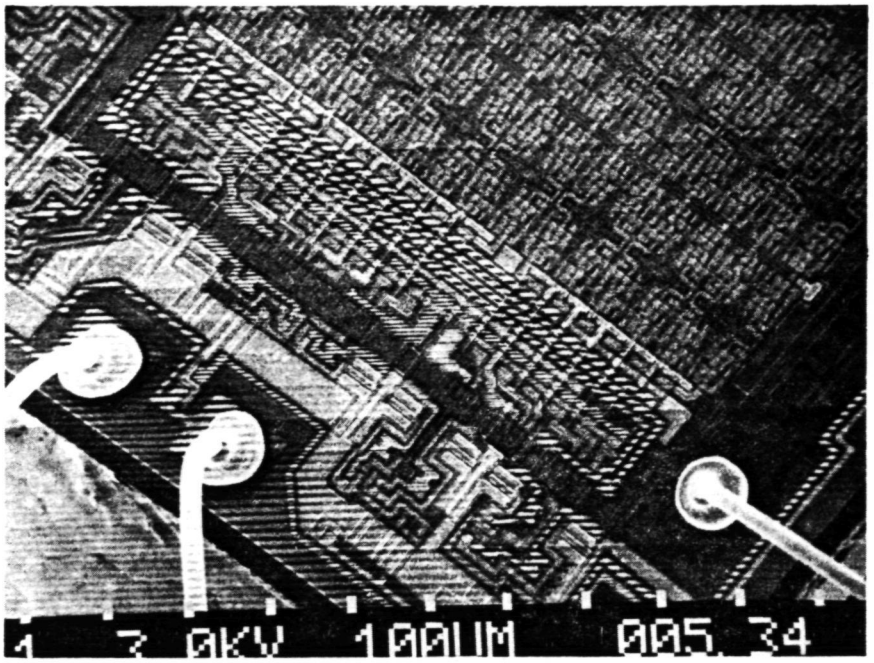

Figure 79. SE V/C Micrograph of Circuit in Figure 80. All address input lines were exercised. (E_B = 3 kV, Mag x 100.)

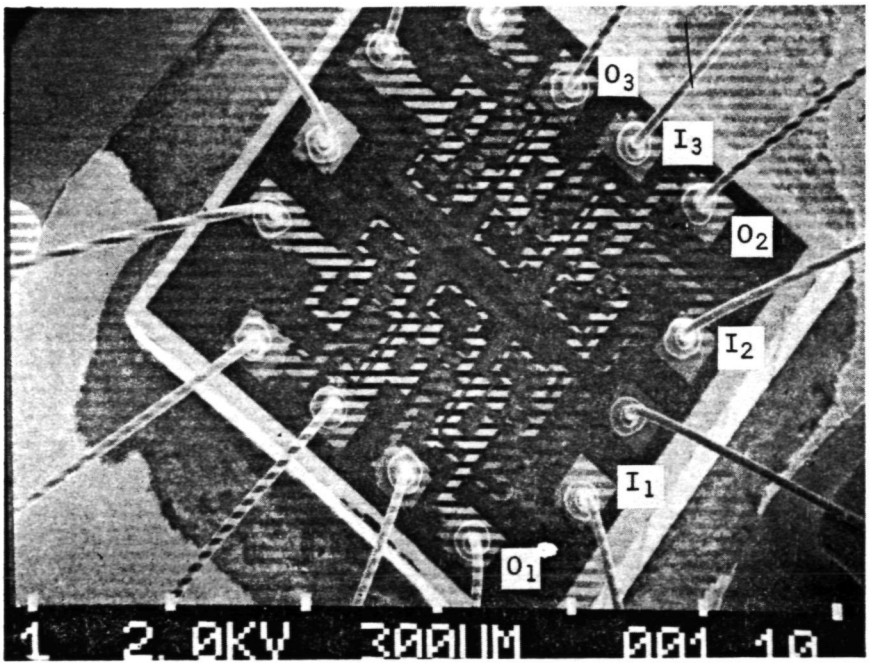

Figure 80. SE V/C Micrograph of 54L04 T/L Hex Inverter. (All six inverters were functioning with V_{cc} = 5 V. E_B = 2 kV, Mag x 60.)

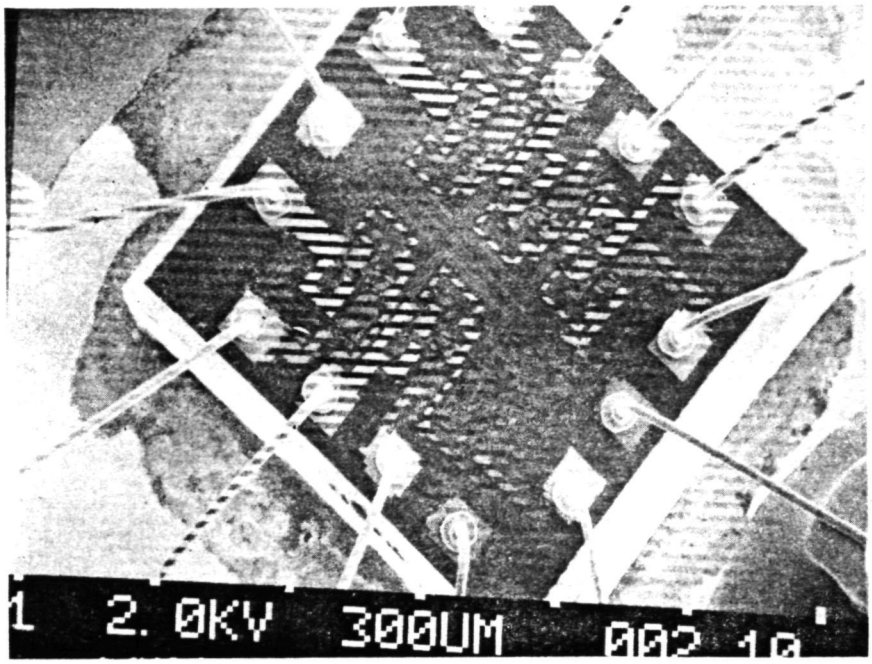

Figure 81. SE V/C Micrograph with V_{cc} = 4 V. (Inverter 1 has stopped functioning. E_B = 2 kV, Mag x 60.)

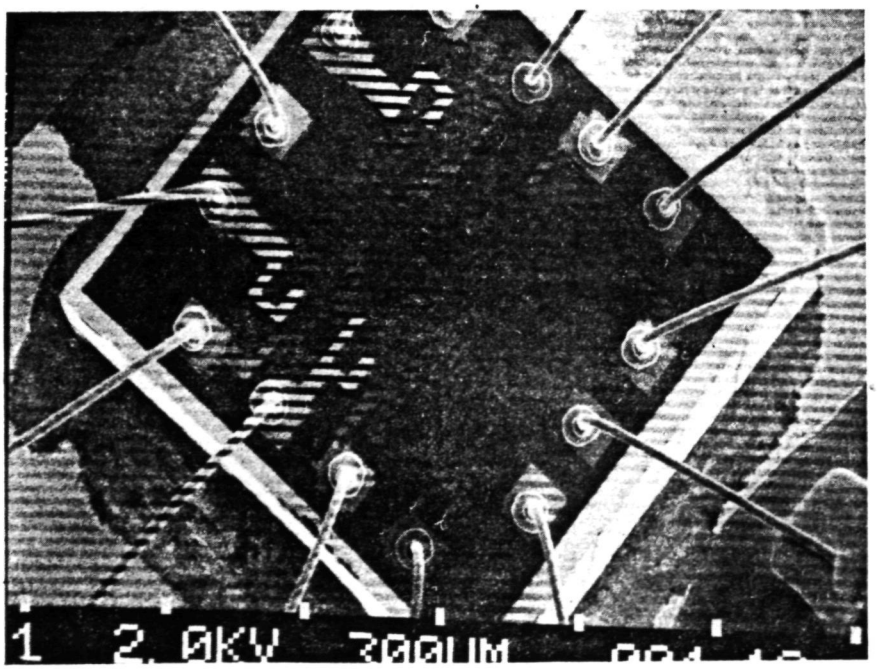

Figure 82. SE V/C Micrograph with V_{cc} = 2.5 V. (Inverters 1, 2 & 3 have stopped functioning. E_B = 2 kV, Mag x 60.)

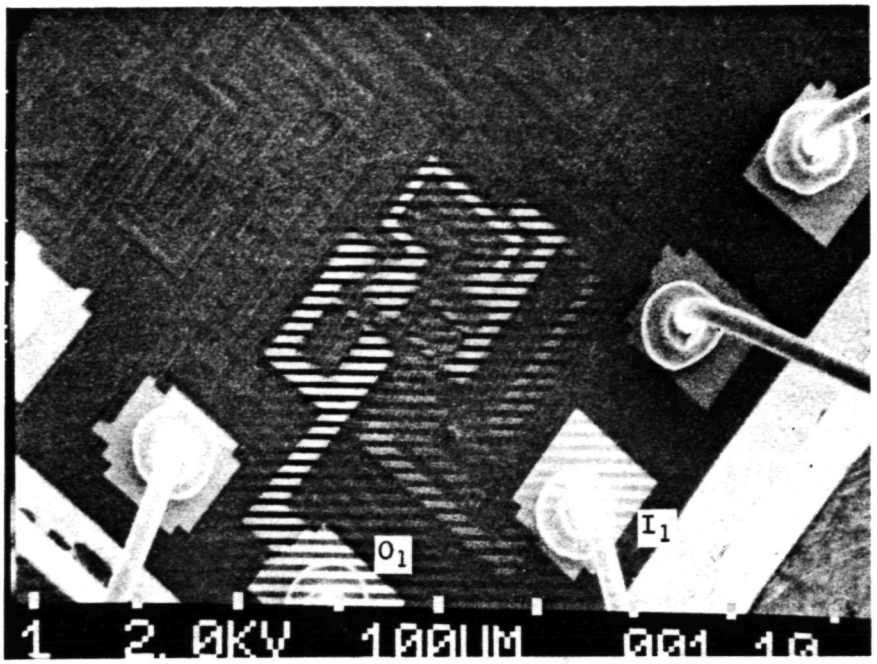

Figure 83. SE V/C Micrograph of Circuit 1 with V_{cc} = 5 V. (Normal circuit function. E_B = 2 kV, Mag x 130.)

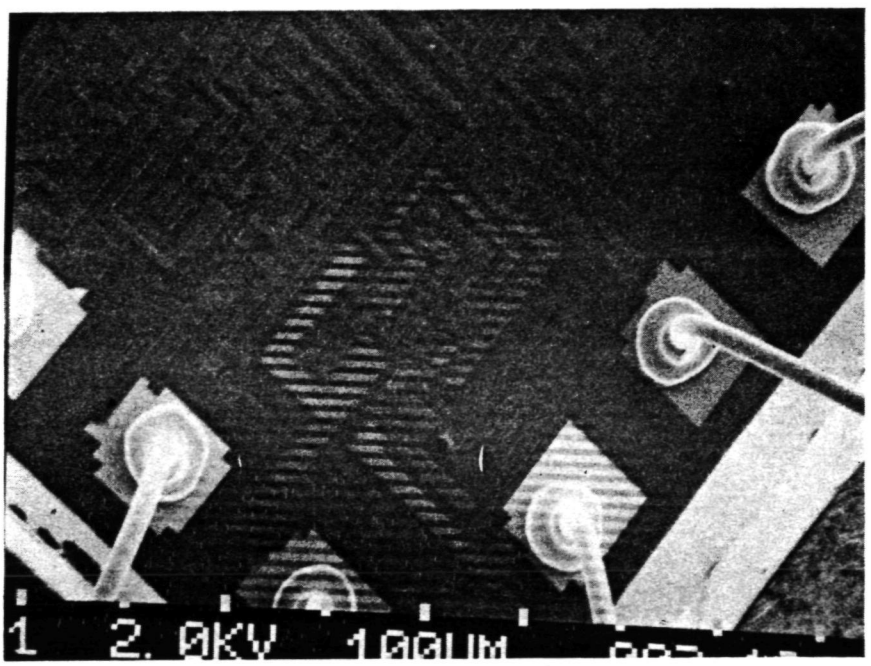

Figure 84. SE V/C Micrograph of Circuit 1 with V_{cc} = 4 V. (Circuit output is not functioning. E_B - 2 kV, Mag x 130.)

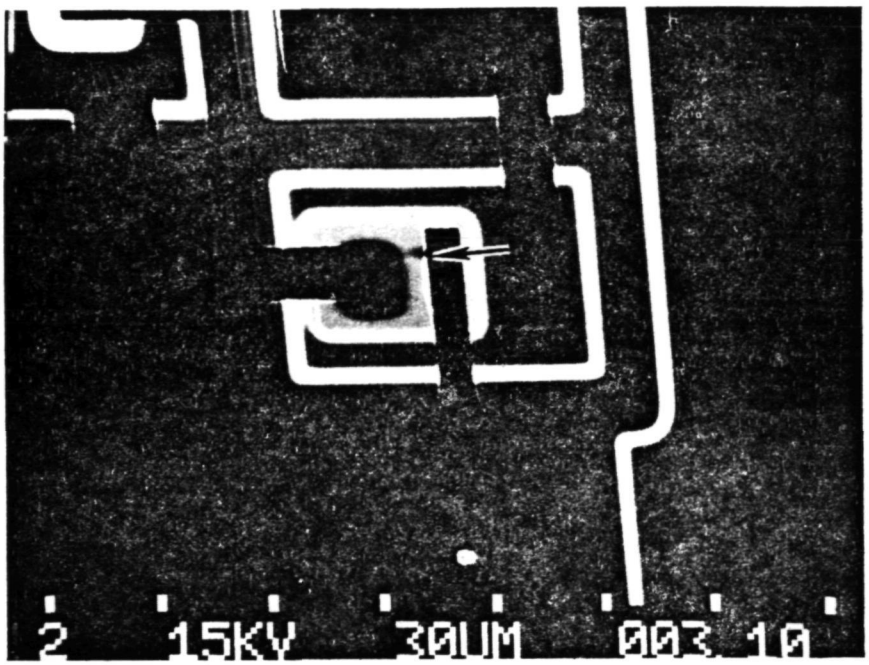

Figure 85. EBIC Micrograph of Circuit 1 Showing Damage in Base/Emitter Junction of Phase Splitter Transistor. (Current from Pin 4 with Pin 11 at ground. E_B = 15 kV, $I_B \approx 1 \times 10^{-10}$A, Mag x 500.)

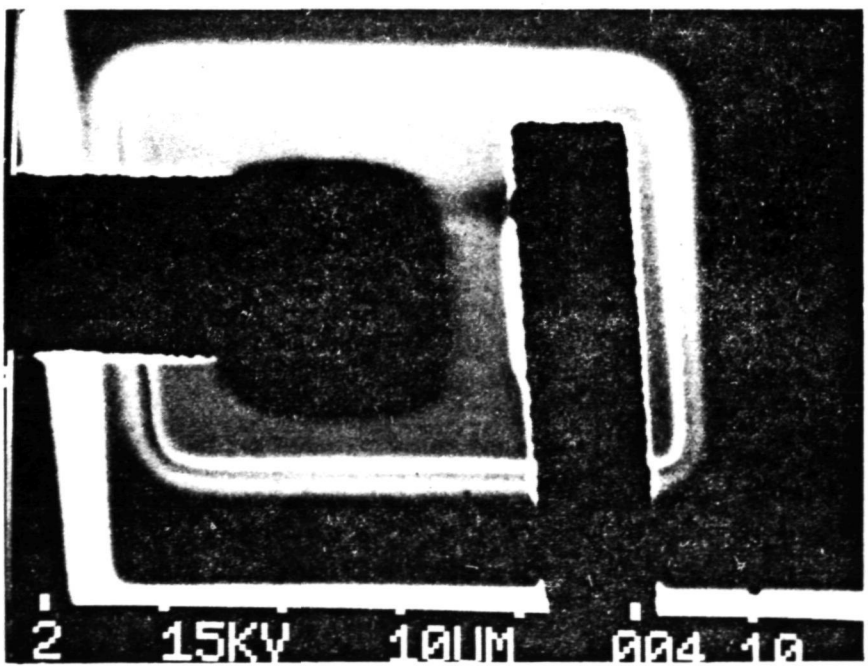

Figure 86. EBIC Micrograph of Same Transistor in Figure 85 at Increase Magnification. (Mag x 1600.)

VI. APPLICATION TO WAFERS

In consideration of EBIC and V/C applications to semiconductor wafers, it is first necessary to evaluate electron beam degradation. At this time it would appear to be feasible to anneal irradiation damage to the surface. The temperature required for annealing would appear to be compatible with wafers. The question still remains regarding residual damage and the effects on operational life. Changes also have been reported in etch rates for surfaces exposed to an electron beam. This could complicate further processing of the wafer following electron beam exposure.

Contamination deposited during electron beam exposure is another area that needs further study. A question that remains is: Can contamination be successfully removed following SEM examination? Irradiation damage and surface contamination present primary roadblocks at this time.

The application of EBIC and V/C operating modes would appear to be feasible at this time. They would require instrument modification for wafer probing, wafer position incrementing, and reject die identification. Inspection criteria identifying procedure, tolerances, applications, and documentation requirements must be developed. The wafer probe must provide the capability for X-Y positioning of the die during examination. Die examinations require magnifications in the range of 500 to 1000X for reasonable defect recognition. Detection could be improved through electronic enhancement of the displayed image. At this time the feasibility of wafer examination appears to be better than packaged and unsealed circuits. For the present time, sample inspection of devices, in particular devices that have exhibited surface problems, could lead to early detection and possible identification of the source of the problem.

VII. SUMMARY

Qualitative and quantitative SEM application methods and guidelines have been described. They provide a valuable and unique capability for semiconductor surface defect analysis. It is intended that these application descriptions will provide an improved understanding and appreciation for these SEM operating modes and that these examples may serve to generate new and improved SEM application techniques.

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