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BREADBOARD LINEAR ARRAY SCAN IMAGER USING LSI SOLID-STATE TECHNOLOGY

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16. Abstract

The objective of the program is to evaluate the performance of large scale integration (LSI) photodiode arrays in a linear array scan (pushbroom) breadboard for application to multispectral remote sensing of the Earth's resources. This final report describes the technical approach, implementation, and test results of the program. Several self-scanned linear array visible photodetector focal plane arrays were fabricated and evaluated in an optical bench configuration. A 1728-detector array operating in four bands (0.5 - 1.1 μm) was evaluated for noise, spectral response, dynamic range, crosstalk, MTF, noise equivalent irradiance (NEI), linearity, and image quality. Other results include image artifact data, temporal characteristics, radiometric accuracy, calibration experience, chip alignment, and array fabrication experience. Special studies and experimentation were included in long array fabrication and real-time image processing for low-cost ground stations. A unique aspect of the program was the use of computer image processing. High quality images were produced and all objectives of the program were made.

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PREFACE

This document is the Final Report for Contract NAS 5-21806, entitled Breadboard Linear Array Imager Program. The report describes the objectives, approach, implementation, and test results of the program.

The objective of the program is to evaluate the performance of large scale integration (LSI) photodiode arrays in a linear array scan imaging system breadboard for application to multispectral remote sensing of the Earth's resources.

The Final Report is submitted in compliance with Deliverable Item 5a, Final Report of NASA Goddard Space Flight Center, Contract NAS 5-21806. The final report was prepared in accordance with GSFC specification S-250-P-1C, March 1972, entitled "Contractor-Prepared Monthly, Periodic, and Final Reports."

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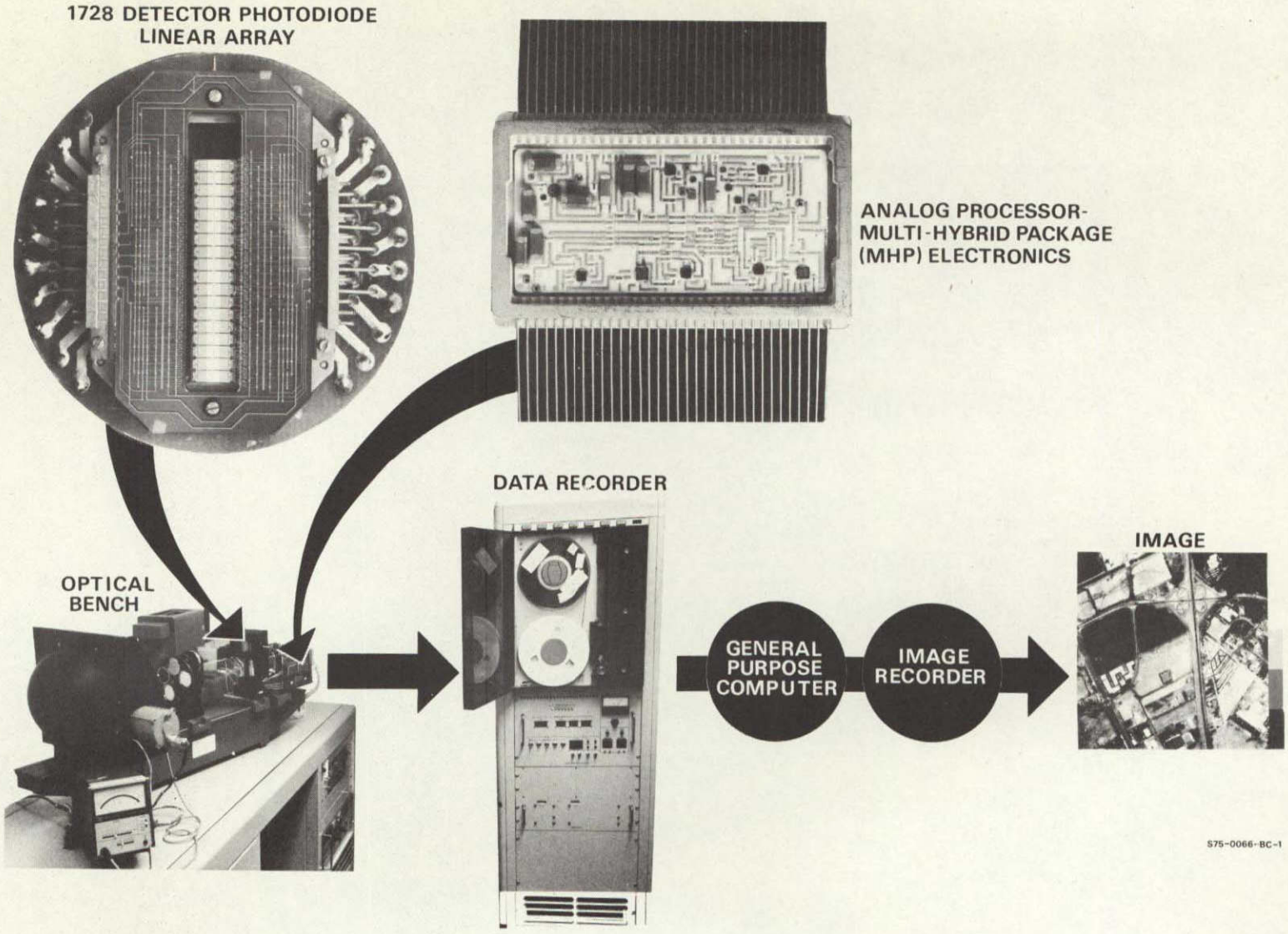
LIST OF ILLUSTRATIONS

LIST OF ACRONYMS

CMOS	Complementary Metal Oxide Semiconductor
ERTS	Earth Resources Technology Satellite
HPBW	Half Power Band Width
IFOV	Instantaneous Field-of-View
LSB	Least Significant Bit
LSI	Large Scale Integration
MHP	Multichip Hybrid Package
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOST	Metal Oxide Semiconductor Technology
MTF	Modulation Transfer Function
NEI	Noise Equivalent Irradiance
OPD	Optical Path Difference
RMS	Root-Mean-Square
RSS	Root-Sum-Square
SNR	Signal-to-Noise Ratio
TTL	Transistor-Transistor Logic



Frontispiece. Breadboard Linear Array Imager Program

1. BACKGROUND

In the evolutionary development of earth observation sensors, demands on improving reliability and resolution are ever present. The use of a long array of photodetectors in the image plane of a geocentric stabilized spaceborne telescope used in the "pushbroom" scanning mode offers the opportunity to achieve both higher reliability and finer resolution. Improved reliability is achieved by the elimination of complex mechanical scanning mechanisms using point detectors, and finer resolution is achieved by increasing the number of detectors in the image plane per picture width.

The advent of large scale integration (LSI) CMOS (Complementary Metal Oxide Semiconductor) technology has allowed the inclusion of detector sampling and commutation circuitry on the same chip[1] as the silicon diode photodetectors. Heretofore, the use of conventional interconnection techniques made it impossible to connect the large quantity of photodetectors to subsequent signal processing circuitry. Thus, the application of pushbroom scanning using long arrays[1] of photodetectors has become a viable technique for future flight sensors.

The Breadboard Linear Array Scan Imager program was begun to exploit this emerging technology. The goal of the program is to demonstrate through experimentation and testing that the technology is feasible for use in future high resolution multispectral imaging sensors for earth and ocean survey applications.

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[1] The term chip used in this report is the component containing 96 photodetectors and associated electronic circuitry (see figure 1). An array is a contiguous line of chips.

1.1 INTRODUCTION

Solid-state linear array photodetector technology is being put to use to develop electronically-scanned multispectral imaging systems. Experience has shown that assembling discrete photodetectors into a long array produces a complex maze of wiring to access each detector element. Thus, a monolithic approach has been developed which results in a single substrate with many detectors interconnected within the chip. The detector outputs are multiplexed onto a few output lines minimizing the physical wiring required. A shift register provides time multiplexing of detectors and is within the chip to reduce the number of physical connections. The chip used on this program has 96 photodetectors and on-chip signal processing provides spatial sequential output time sharing on four common output lines. The chip requires less than two dozen external wires to be attached. Each chip is capable of being physically butted to provide a continuous line of photodetectors of thousands of resolution elements per line. Multiple chip sharing of the data output lines is possible by serially connecting the shift registers of butted chips, thus reducing external processing requirements to a minimum. The use of this approach allows the development of solid-state imaging systems with thousands of resolution elements requiring no mechanical scanning.

To investigate the characteristics and capabilities of fabricating solid-state arrays, NASA/GSFC issued contract NAS 5-21806, entitled Breadboard Linear Array Imager Using LSI Solid-State Technology, in July 1972. The governing technical specification and statement of work is included in NASA-GSFC document S-731-P-128, Specification for a Breadboard Linear Array Imager Using LSI Solid-State Technology, dated January 1972.

The original contract includes the design, fabrication, and test of a 576-detector element array. In late 1973, a contract change order was received to design, fabricate, and test an 18-chip (1728 detector) linear array which has been completed. In accordance with contract requirements, a test plan document was prepared and used as the test criteria for performance evaluation. The final system test program on the 6-chip array was completed in

June, 1973. A similar test program was completed on an 18-chip array in February, 1974.

In June of 1974, a second contract change order was received to design, fabricate, and test multichip hybrid package (MHP) analog processing circuits and to perform a study to determine improved techniques for mechanically aligning linear photodiode detectors in long arrays. The goal of the MHP analog processor development was to provide a design which would more closely achieve detector-limited noise performance. The work performed on the multichip hybrid package analog processing circuits is discussed in paragraph 2.4.2.2. The array fabrication improvement study is included in paragraph 2.6.

In January 1975, a third contract change order was received to design, fabricate, and evaluate the effects of a real-time offset and gain correction capability for a 576-element array. The goal of the program was to demonstrate that good quality imagery can be provided with a real-time correction system. The work performed and analysis results are discussed in paragraph 2.7.

1.2 SUMMARY OF RESULTS

The results of the Breadboard Linear Array Scan Program Imager Program have conclusively shown that photodiode linear arrays can be applied to multispectral remote sensing of earth resources. A summary table including the performance objective and the actual performance achieved on the program is shown in table 1, Summary of Results. The table also includes a reference to the paragraph number or appendix that discusses the source of the performance data.

1.3 TYPICAL APPLICATIONS

The work documented in this report shows that self-scanned photodiode linear arrays can be effectively applied to future spacecraft instruments. The generic class of instruments that are most appropriate for applying this technology are similar in scope to that of the familiar

TABLE 1

SUMMARY OF RESULTS

Performance Objective or Functional Evaluation (Spec S-731-P-128 par No.)	Performance/Evaluation Obtained
Noise (par 3.1)	System level NEI (equivalent to 0.4 to 0.8 μm band) $\cong 1.4\ \mu J/m^2$ (see par 2.5.1 1)
Spectral Response (par 3.1)	Typical silicon photodiode response (see par. 2.5.1 6)
Dynamic Range (par. 3 1)	Greater than 600.1, (see par. 2.5.1.4)
Calibration Problems (par. 3.1)	Image streaking due to thermal drift in array temperature (see par 2 5 2 5)
Image Artifacts (par 3 1)	Artifacts due to geometrical and electrical characteristics (see par. 2.5 2)
Cross Talk Between Detectors (par 3 1)	Not detectable (see par 2 5.1.5)
Reliability (par. 3.1)	Detectors meet Mil-883 level B; see Appendixes C and D for failure analyses
Temporal Characteristics	No apparent long-term (six-months) temporal problems, although a precise assessment of performance was not possible in laboratory environment (see appendix G)
Obtain Imagery	Extensive image production and evaluation was obtained (see par 2.5.1.7)
Determine Array Fabrication Problems	Primary fabrication problem was found to be chip handling and intricacy of alignment (see par. 2 4.7 2). Corrective techniques discussed in par. 2.4 3.2 and par. 2.6
Performance Goals (par. 4 1)	
• 500 elements (later changed to 1728)	Three arrays were fabricated (two each 576 and one each 1728 detectors/array) (see par 2 4.3 1)
• Four Spectral Bands (par. 4 2)	Spectral bands were: (1) 0 50 – 0 58 μm (2) 0 62 – 0.68 μm (3) 0 73 – 0 81 μm, and (4) 0 8 – 1.1 μm See par. 2.4 1.3
• Radiance Conditions (par. 4.3)	Various radiance conditions used (see par. 2 4.1 2)
• SNR_1 Goal 22 (par 4.4)	For 0.5 – 0.6 μm band, system SNR of 40 was achieved for low radiance, low spatial frequency target (see par 2.5 1.1)
• SNR_2 Goal 2 (par. 4 4)	For 0.5 – 0.6 μm band, system SNR of 4 was achieved for low contrast, high spatial frequency (see par. 2.5 1.1)
MTF Along Scan and Across Scan	The detector geometry was chosen to provide equal MTF along and across track. (see figure 9)
Radiometric Accuracy, 5 percent of High Radiance, (par 4 6)	HP 8330A radiometer calibration shows absolute uncertainty of better than 5 percent (see Appendix I)
Detector Geometric Linearity of 1 percent (par. 4.7)	Array chips positioned to within less than 1 percent of array length (see par 2.6 2)
Chip Alignment	Chip alignment of 1/4 resolution element was achieved (see par. 2 6.2)
NEI (Noise Equivalent Irradiance) of Detector to be Less Than 1.2 $\mu J/m^2$	The mean detector noise is less than $1.2\ \mu J/m^2$ (see par. 2.5 1 1)
Linearity Within 2 percent of Best Fit Line (par. 5.6)	Linearity measurements and detector data indicate a 2 sigma variation of less than 3 percent of full signal from a best fit line (see par 2 5.1.2)
Detector Requirements (par. 5.7)	
• < 5 percent Element-to-Element Variation After Processing	For the signal quantization interval (approx. 30 to 50 intervals full scale signal) and 2 calibration levels and irradiance used this exceeds limit (peak error of 6 percent)
• No Dead Elements	Chip manufacturing data provided on 30 chips used on this program indicated only one bad element for all chips.
• End Elements to have Response of > 60 percent Mean Full Scale	Most of the chips used for this program had an end element response better than 60 percent of the mean response; however, limited availability of chips made this parameter an impractical selection criteria

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Landsat Multispectral Scanner (MSS) and the next-generation instrument called Thematic Mapper. These are sensors dedicated to remote sensing for earth resource survey and land use evaluation.

The limits to the ability to resolve targets of interest for these two instruments (80 m ground sample distance for the MSS and 30 m for the Thematic Mapper) exemplifies a fundamental difference between a mechanical scanner and a solid-state pushbroom instrument. That difference is that the solid-state linear array approach is limited in its ability to resolve targets only by the optical system quality, while the mechanical scanner is limited by optics quality and the intricacies of the scanning mechanism; also, at the higher resolutions, by signal-to-noise ratio as compared to solid-state technology.

Examples of typical applications are:

a. To provide a solid-state instrument equivalent to the Landsat MSS on a small Scout-launched satellite

b. To provide redundant solid-state multispectral scanners (SSMSS) to achieve a 6 to 10 year lifetime for an operational earth resources satellite

c. To provide a large solid-state high resolution instrument for a Shuttle-launched earth observation satellite.

The applications are discussed below. A tabular summary of application studies is included in table 2.

1.3.1 Solid-State MSS for Small Scout-Launched Satellite

The characteristics of the SSMSS are shown in table 3, and a physical configuration of the instrument is shown in figure 1. The 20 kg SSMSS instrument of figure 1 is shown mounted to a small 120 kg Scout-launched satellite.

TABLE 2

SUMMARY OF APPLICATION STUDIES

HRPI Point Design Study, Westinghouse Electric Corporation
Report under NASA Contract NAS 5-21953, 29 August 1973

The purpose of the HRPI Point Design Study was to produce a preliminary design of a high-resolution (10-meter GSD), off-track pointable, four-band visible, solid-state linear array sensor. The instrument design included a single f/3.0, 1.5 meter focal length telescope with a dichroic and prism spectral separator. The telescope is capable of incrementally pointing crosstrack ± 30°. The solid-state focal plane includes four 4800-detector self-scanned linear array photodetectors operating in four bands within 0.5 to 1.1 μm. The composite data rate is 90 megabits per second. This instrument was to be contained within one-meter diameter, 2.5 m long cylinder with a mass less than 1100 kg and dissipate less than 100 watts.

All objectives of the study were achieved. It was concluded that the design was of sufficient detail to have high confidence that a flight instrument can be built. The study was completed in September of 1973.

Support of EOS Systems Definition Study Prime Contractors (HRPI), Final Report, Westinghouse Electric Corporation
Report under NASA Contract NAS 5-20612

The purpose of this study was to provide technical support to the three prime contractors performing the EOS Systems Definition Study. In the first phase of the contract, technical assistance was provided in the general area of instrument integration. In the second phase, specific technical tasks were addressed. The tasks included: (1) development of a simplified pointing mechanism, (2) improved image processing techniques, (3) improved optical materials selection, (4) concept formulation of onboard processing to minimize ground display complexity, and (5) fabrication of a scaled mock-up of the HRPI pushbroom instrument.

The study was completed in May of 1975.

High Resolution Pointable Imager (HRPI) Lightweighting Study, Final Report,
Westinghouse Electric Corporation
Report under NASA Contract NAS 5-20700, 15 November 1974.

The purpose of this study was to determine the effects of parametric change upon the weight and volume of the HRPI instrument. In this study, various approaches and design techniques were evolved to minimize the weight of the solid-state pushbroom HRPI. Twelve major findings resulted from the study. Two important findings relative to physical considerations were that, (1) a relaxation in the precision of pointing repeatability resulted in a major weight reduction, and (2) a nominally geocentric pointing gimballed telescope (without a pointable mirror) is the minimum weight configuration. The study developed some useful parametric design aids which include, (a) dependence of instrument weight and volume on Northern latitude irradiance requirements, (b) development of an optimization aid using a figure-of-merit of SNR/volume, (c) an aid to determine resolution degradation as a function of offset pointing angle, (d) a computerized model to predict weight of optical components, and (e) a preliminary cost model.

The study was completed in November of 1974.

Proposal for Solid-State MSS (AAFE),
Westinghouse Electric Corporation, dated 31 May 1974.

This independent design study was for a solid-state MSS (multispectral scanner). The all solid-state instrument includes an f/3.5, 20 cm focal length telescope with a dichroic/prism spectral separator, and the focal plane contains four linear self-scanned photodetector arrays with 2,688 detectors per array. The instrument with a composite data rate of 14.4 Mbps operates in four bands within the 0.5 - 1.1 μm range and is designed to exceed a SNR of 250 (for high contrast, low spatial frequency targets) at an MTF of 0.3 for a ground sample distance of 69 meters. The estimated mass of the instrument is 12.3 kg contained within a volume of 1400 cc with an average power dissipation of less than 37 watts.

The study was completed in May of 1974.

TABLE 3

SSMSS INSTRUMENT PARAMETERS

Parameter	Value
IFOV	86 microradians
Field-of-View	10°
Optics Aperture	6 cm
Size	22 x 20 x 43 cm
Weight	14 kg
Power	35 W
Data Rate	8.1 megabits per second

Signal-to-Noise Performance in MSS Spectral Bands.*

Wavelength (μm)	S/N
0.5 μm - 0.6 μm	520
0.6 μm - 0.7 μm	460
0.7 μm - 0.8 μm	440
0.8 μm - 1.1 μm	500

* High contrast, low spatial frequency target using a dwell time that is 25% of the 10 msec available for an 86 μrad IFOV.

1.3.2 Operational Earth Resources Observation Satellite

The concept shown in figure 2 is for a future earth resources operational satellite where extremely high reliability is required (i.e., 6 to 10 year life-time). The approach in this concept is to use small and inherently more reliable solid-state multispectral sensors (SSMSS) in a redundant configuration to attain the required operational lifetime of 6 to 10 years.

For the benefit of candidate users of future solid-state linear array instruments such as the SSMSS, noise equivalent reflectance (NER) has been calculated. The curves of figure 3 are of noise equivalent reflectance in percent as a function of solar zenith angle for average scene conditions in each of the four MSS spectral bands.

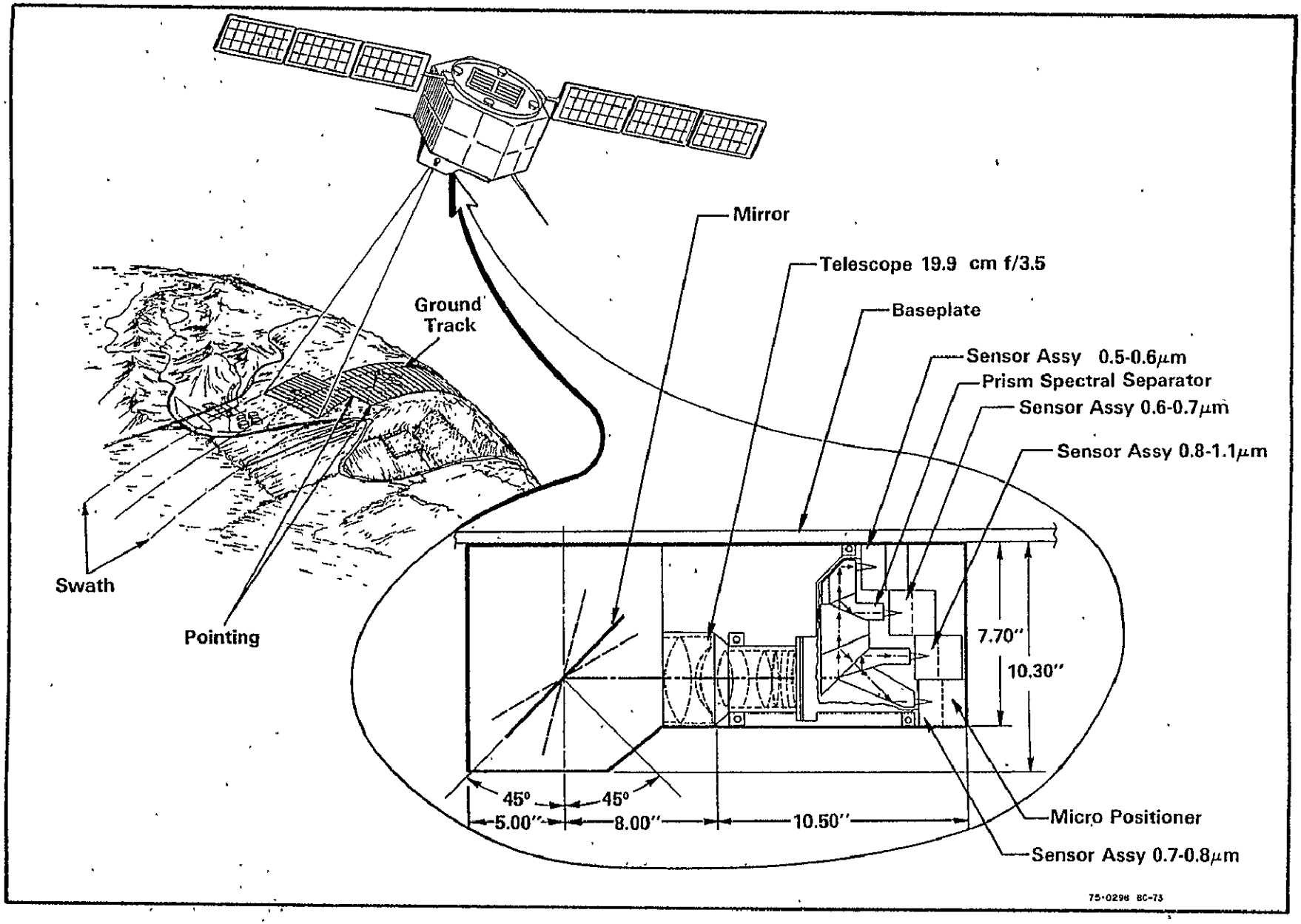

Figure 1. Solid-State Multispectral Scanner on a Typical Scout-Launched Satellite

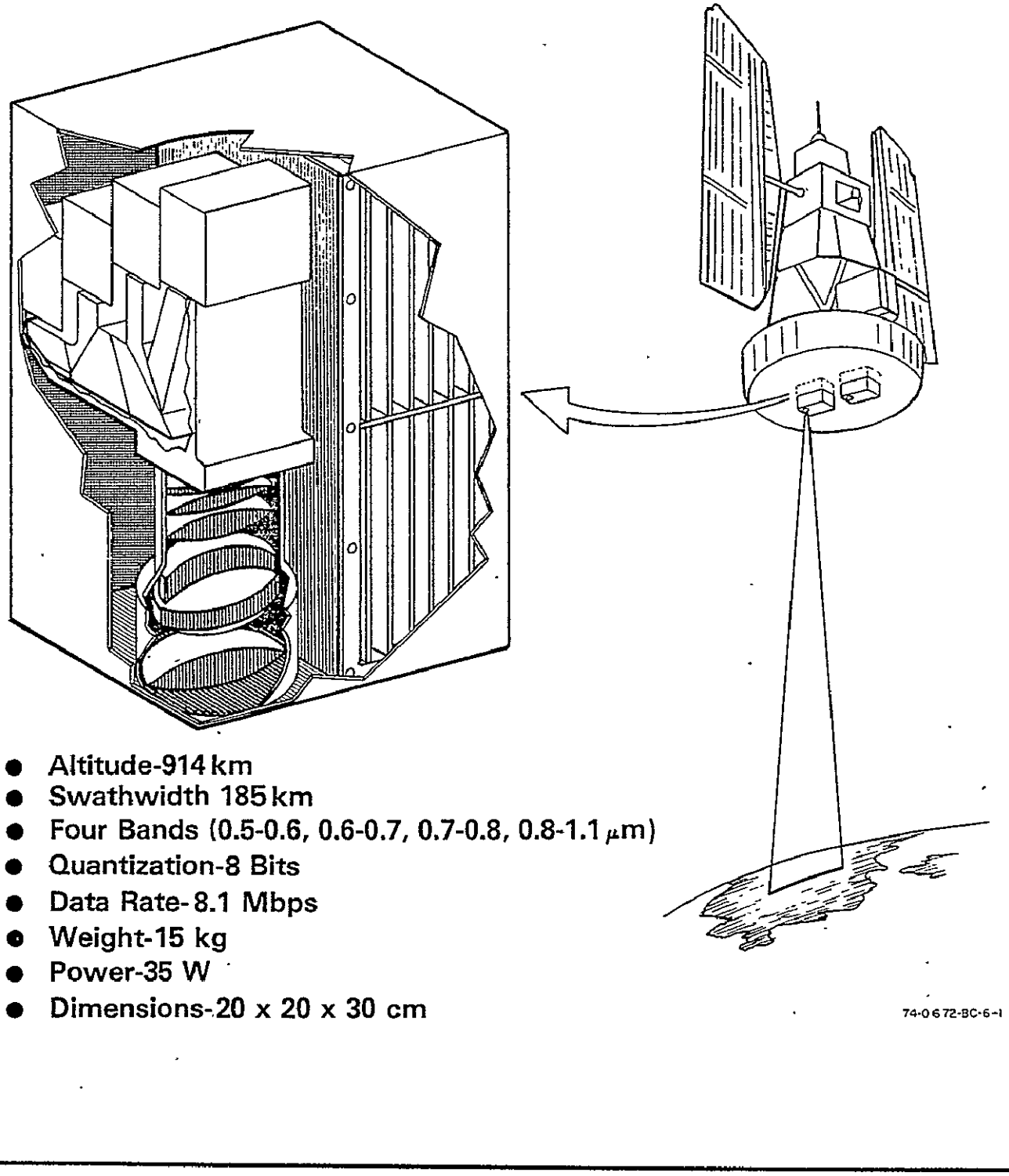

Figure 2. Redundant Sensors for Long-Life Earth Resources Observation Satellite

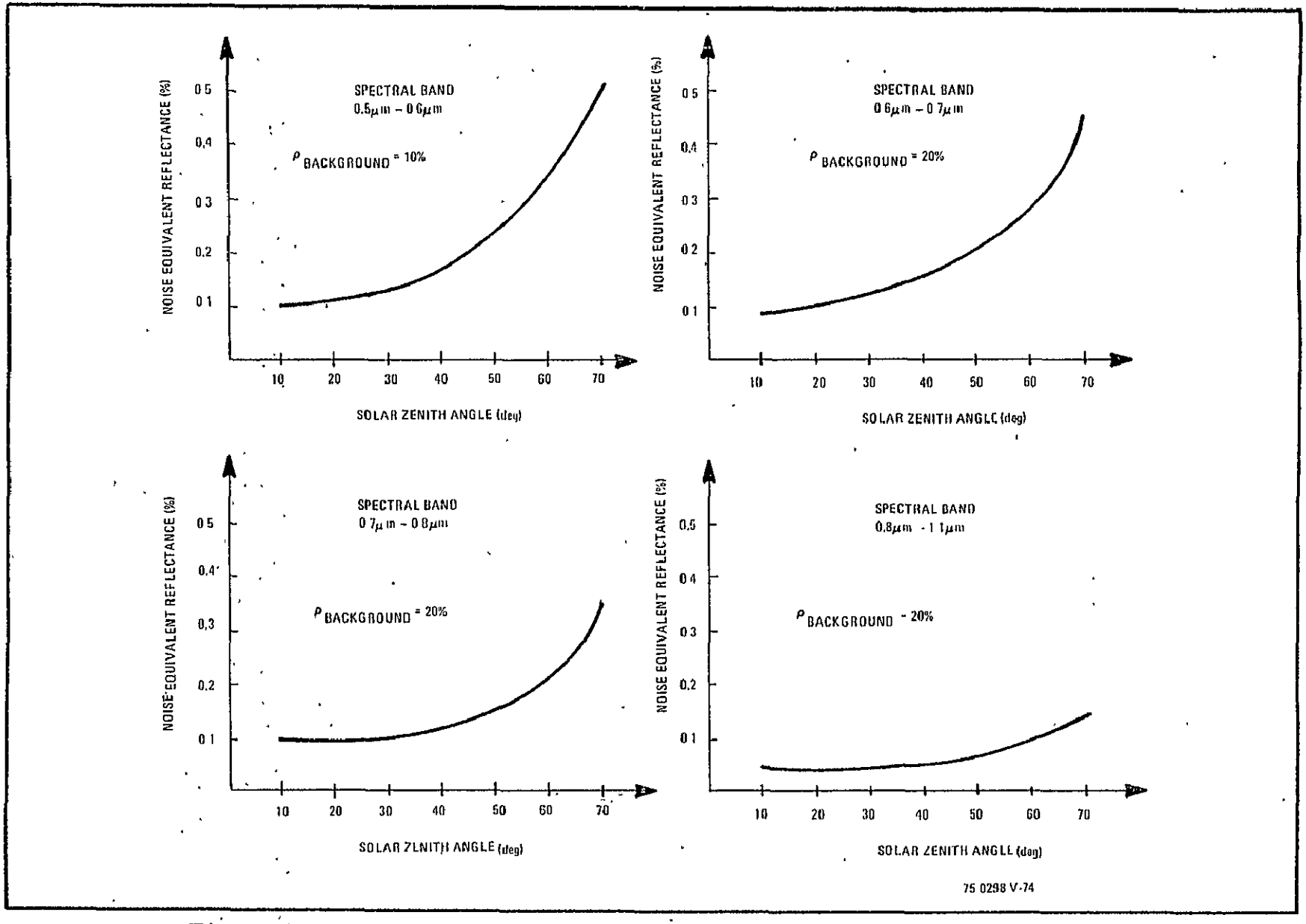

Figure 3. Performance of Solid-State MSS for Various Solar Angles and Average Scene Conditions

1.3.3 Shuttle-Launched Earth Observation Satellite

Another candidate application that has been studied extensively is an instrument for use on a shuttle-launched earth observation satellite. This concept and pertinent performance and physical aspects are shown in figure 4.

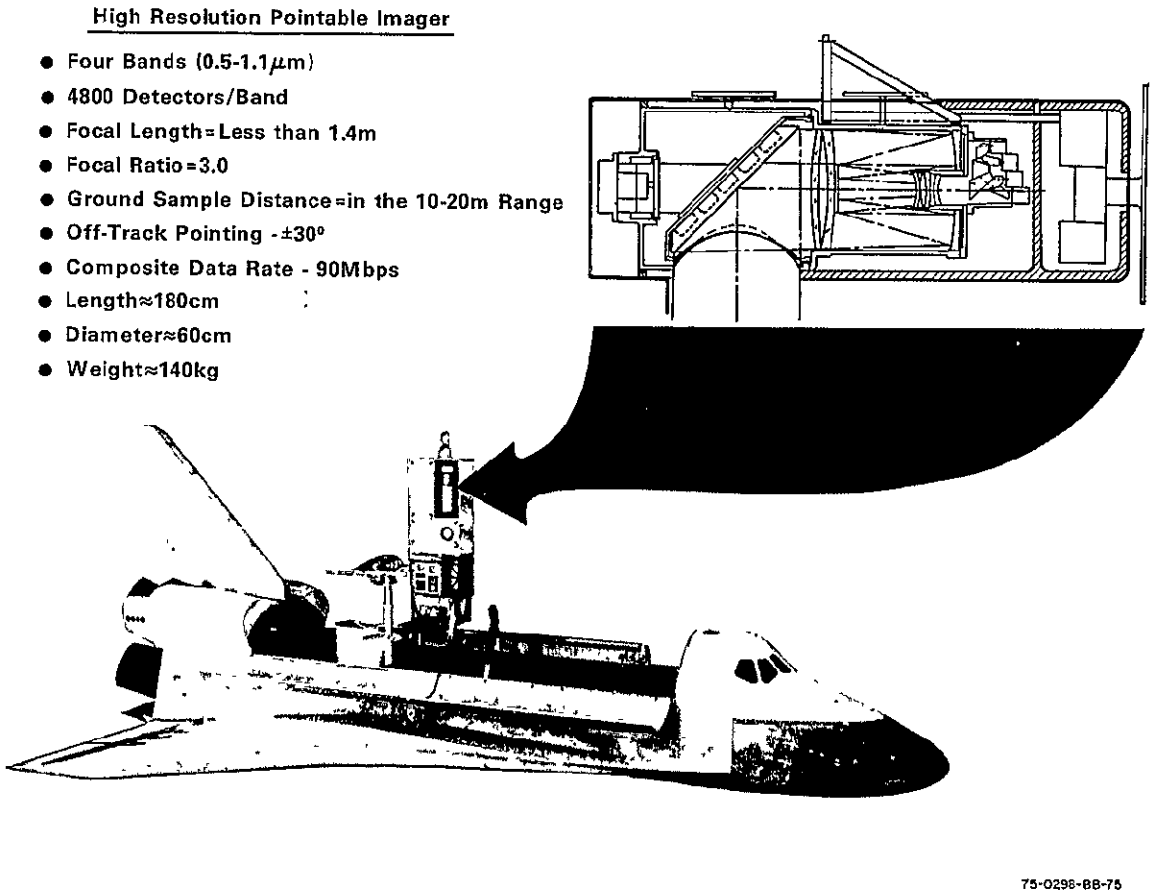

Figure 4. Solid-State Sensor on Shuttle-Launched Large Earth Observation Satellite

2. TECHNICAL REPORT

2.1 PROGRAM OBJECTIVE

The objectives of the program as stated in the Technical Specification are:

- To evaluate the performance of LSI photodiode arrays in a linear array scan imaging system. Emphasis will be placed on determining noise characteristics, calibration problems, spectral response, dynamic range, image artifacts, crosstalk between contiguous detectors, reliability, and temporal performance.
- To evaluate total system performance, especially for conditions simulating ERTS scenes.
- To provide high quality images from the camera system.
- To determine fabrication problems associated with making long arrays from many short arrays.

2.2 PERFORMANCE OBJECTIVES

The Technical Specification contains a listing of system performance objectives which are summarized below:

- Minimum of 500 detectors per array (this was later changed to 1728 detectors)
- Four passbands of interest are 0.5-0.6 μm, 0.6-0.7 μm, 0.7-0.8 μm and 0.8-1.1 μm.
- The system is to be evaluated with nominal ERTS scene conditions as follows:

Passband (μm)	Scene Radiance (W/cm^2 - sr)	
	High	Low
0.5-0.6	2.48×10^{-3}	1.20×10^{-4}
0.6-0.7	2.00×10^{-3}	2.00×10^{-4}
0.7-0.8	1.76×10^{-3}	2.80×10^{-4}
0.8-1.1	4.60×10^{-3}	6.7×10^{-4}

- After signal processing, the system is to have a signal-to-noise ratio in excess of 22 for the low radiance conditions (0.5-0.6 μm) with a high contrast, low spatial frequency target.
- For the low radiance conditions of the 0.5-0.6 μm passband and a target contrast ratio of 2 to 1, the system is to have a SNR greater than 2 at the limiting spatial frequency.
- The modulation transfer function (MTF) (at the limiting spatial frequency) in the along-scan and across-scan direction is to be approximately equal.
- After signal processing, relative radiometric measurements are to be accurate to 5 percent of the high radiance test conditions.
- The linear dimension geometric accuracy of the detector arrays is to be maintained to one percent.
- The system is to operate at room temperature.
- The bilinear staggered self-scanned LSI detector is to have a rectangular diode aperture with a cross-track to along-track dimensional ratio of 1.3:1 with an effective sample distance of 15.24 μm. The mean value of noise equivalent signal (NEI) is to be 1.2 $\mu J/m^2$ for a spectral interval of 0.4 μm to 0.8 μm for a 6000K source.
- The diode array is to have a dynamic range (in terms of input radiant energy from NEI) of 600:1.
- The detector response linearity defined as percent error from the best straight line fit to the mean response curve for the full range is not to exceed two percent.
- Objectives in detector variation are: (1) after processing, the element-to-element variation for a given video output bus on a chip shall be less than or equal to ±5 percent of the full scale response, (2) there are to be no dead elements, and (3) after processing, the end element response is to be at least 60 percent of the mean full scale response.

2.3 PHOTODETECTOR ARRAY CHIP

The photodetector chip used on the breadboard linear array program is an array of 96 photodiodes on 0.6-mil centers with the associated electronics necessary to form an array of light detectors for image scanning (see figure 5). The scene image is formed by periodically sampling each photodiode in the line array. The on-chip electronics furnishes the first level of preamplification and the multiplexing necessary to periodically sample each sensor

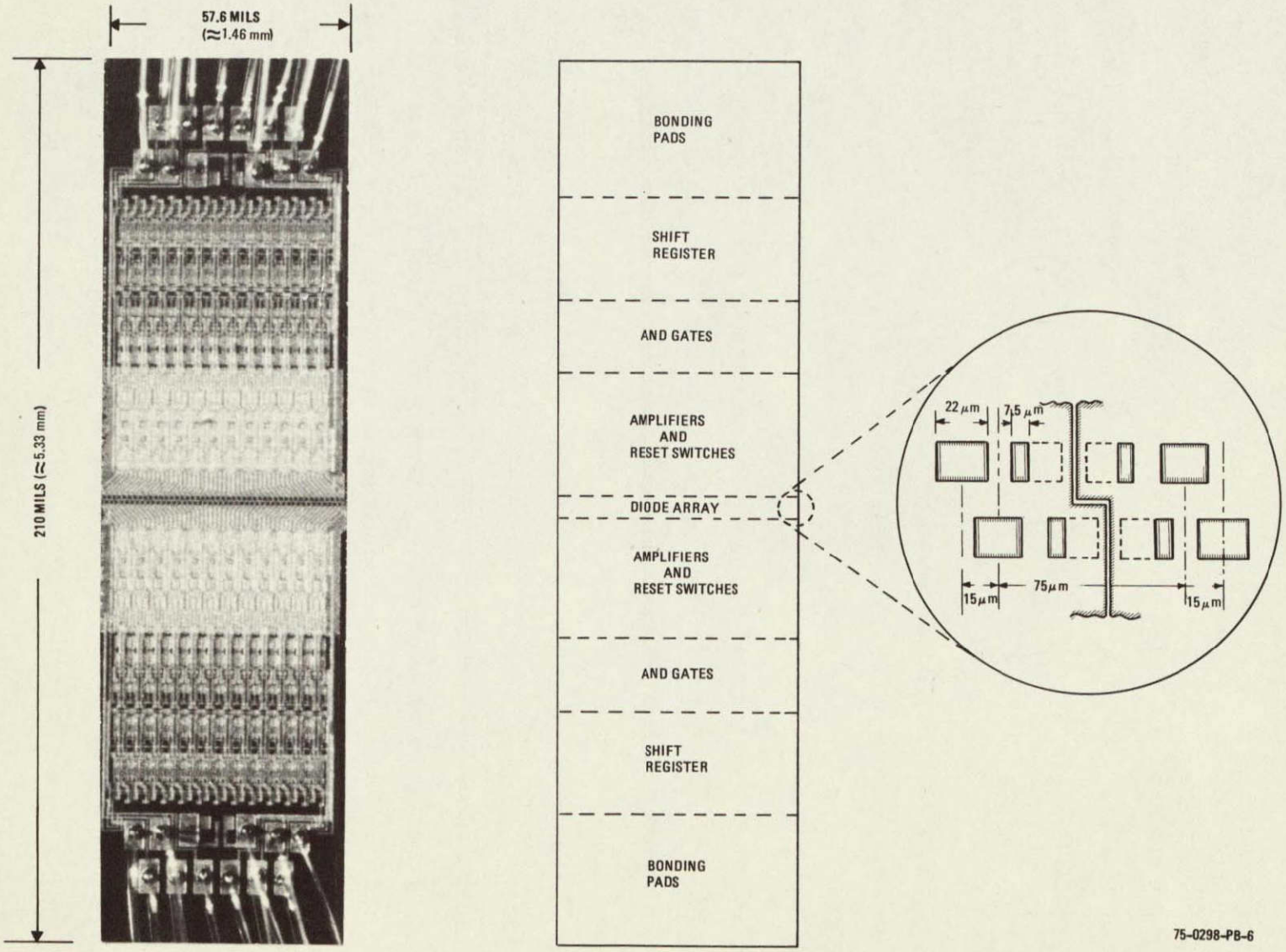

Figure 5. 96-Photodiode Detector Chip Showing Associated Electronics and Geometry

and commutate the sensor outputs onto one of four output buses. The chips are fabricated using the complementary metal-oxide insulated-gate semiconductor transistor technology (MOST) which is compatible with the diode fabrication.

A schematic diagram of the chip is shown in figure 6. To perform the functions necessary of the array, a sensor, amplifier, and address and control circuitry are associated with each diode position in the line array. The photodiode, operating in the integration mode, and a reset switch form the sensor whose output is taken from the node between the two devices. The output of the sensor is connected to the gate of a single MOST whose drain current is the measured variable commutated to the output line. The address circuitry consists of a shift register stage and an AND gate to control the reset switch.

The schematic diagram of the detector and the amplifier is shown in figure 7 where Q_1 is the reset switch, Q_2 is the amplifier, Q_3 is the amplifier commutating switch, and the external amplifier is the output current detector.

The photodiode detector is operated in the integration mode. Initial conditions for the integration mode are established when the photodiode is reverse biased by switching Q_1 on. When Q_1 is switched off, the photodiode remains reverse biased because of the charge stored on the input capacitance of the amplifier, the parasitic capacitance of the interconnects and the reset switch, and the capacitance of the diode itself. The rate with which this voltage will decay toward zero is proportional to the leakage of the diode, the parasitic leakage of the node, and the light proportional reverse current of the photodiode. After a period t, Q_1 is again turned on and the capacitance is recharged. This mode of operation ensures that the diode is detecting during the entire period between reset pulses and offers an efficiency proportional to the ratio of the integration period to the total period from reset pulse to reset pulse. The measure of irradiance may be the peak recharge current,

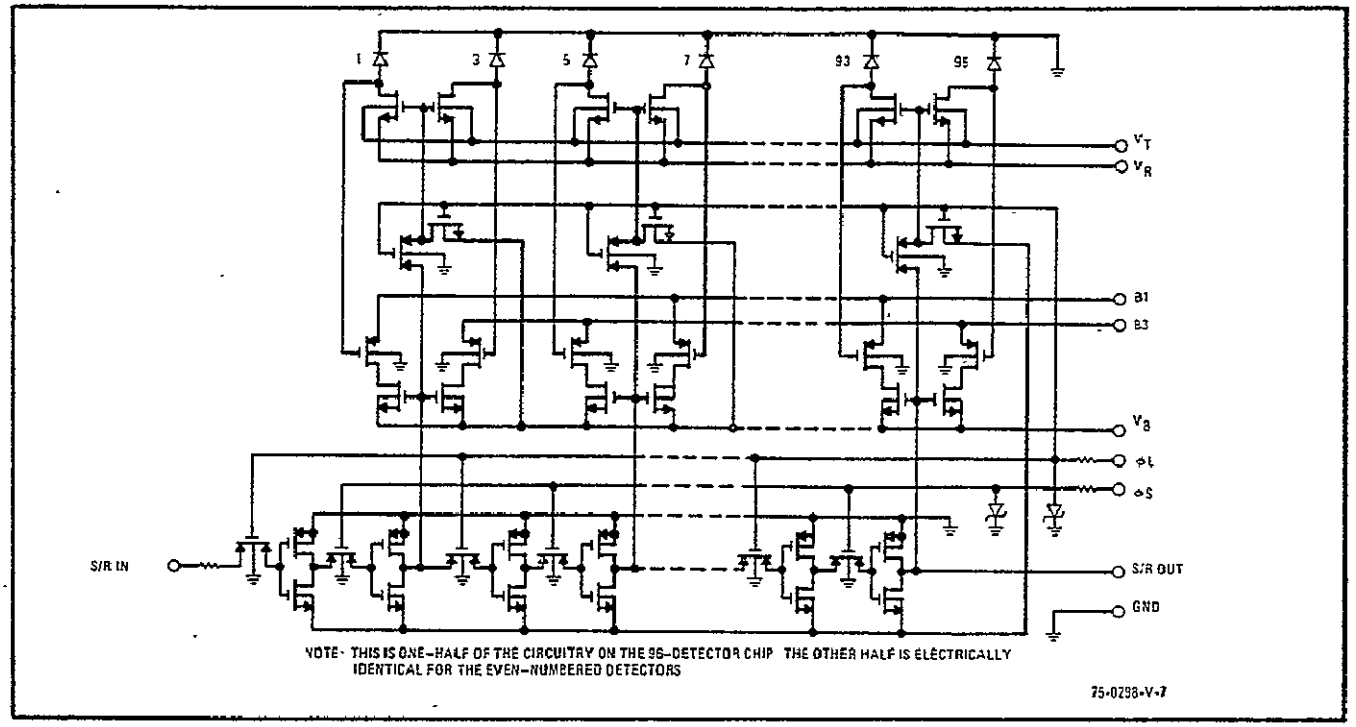

Figure 6. Schematic Diagram of 96-Detector Chip

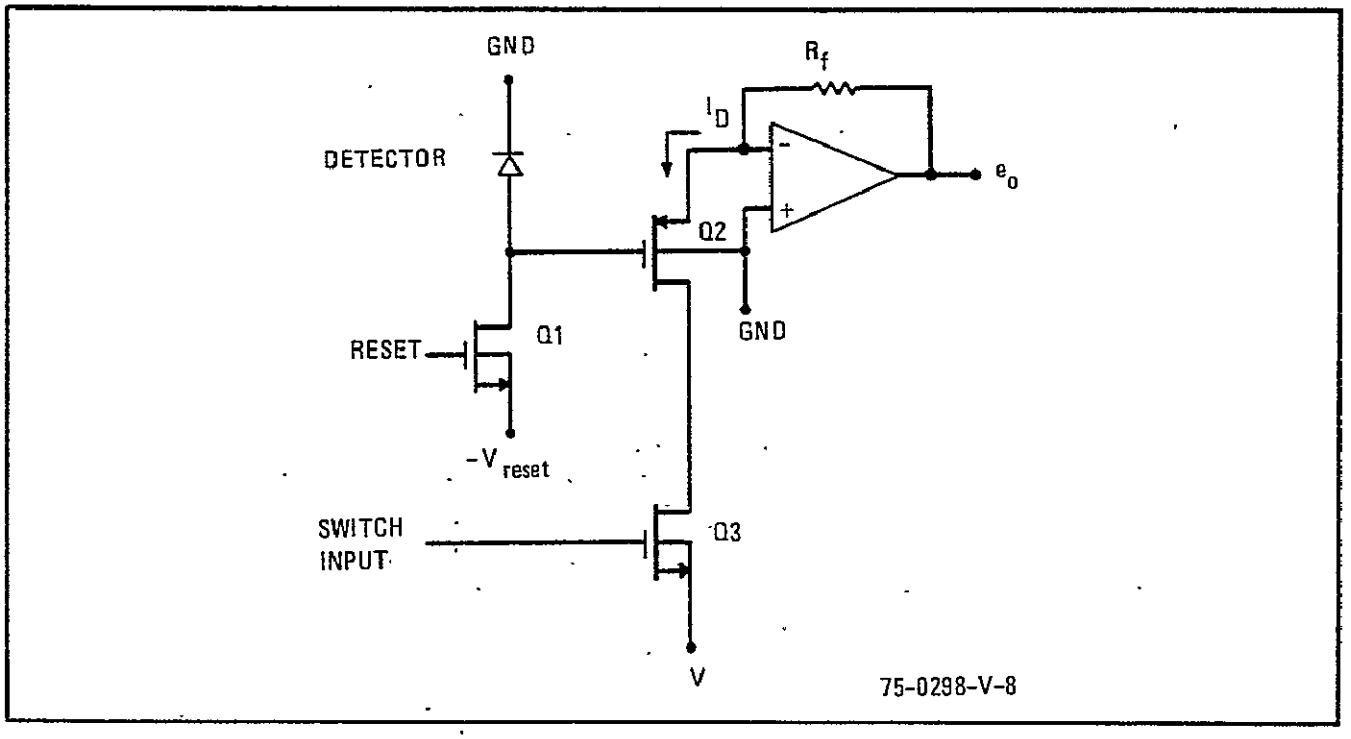

Figure 7. Schematic of Photodiode Detector and Amplifier

the total replaced charge, or the voltage across the diode prior to reset. This last approach is used on the 96-detector chip.

The detector amplifier is the single p-channel MOST, Q_2, shown in figure 7. The voltage between its gate and the output bus is the integrated signal which in turn determines the source current flowing through R_f (the measured variable). The series n-channel MOST, Q_3, between the supply and the amplifier enable this current to flow through the amplifier when addressed by a 1 during the sample period and inhibits the current when addressed with a 0 between samples.

Figure 7 shows that the output bus is connected to the summing point of an operational amplifier which is referenced to ground. The output bus is thus a virtual ground with an impedance of R_f/A_v. This being the case, many amplifiers may be multiplexed onto this line without channel interaction. Thus, a substantial reduction in the number of output leads is made possible. The scene energy is converted into small analog signals and thus is available for further processing.

2.4 PROGRAM IMPLEMENTATION

The principal objective of the subject program is to evaluate the performance of large scale integration (LSI) photodiode arrays in a linear array scan imaging breadboard. To perform this evaluation required the construction of a test tool capable of performing appropriate quantitative tests. The integrated test tool and evaluation program consists of the breadboard imager, computer software programs for image data processing, and display software. An overall block diagram of the entire process of image generation, detection, signal processing, data processing, and display is shown in figure 8.

This program required the design and fabrication of a test bench, the design and fabrication of detector arrays, the preparation of computer software programs, and the conduct of a test and evaluation program.

The following sections of this report describe the details of program implementation. The report includes an evaluation of test results.

2.4.1 Test Bench

The test setup for the Breadboard Linear Array Program consists of the array, optics, and scene simulator mounted on an optical bench. Analog processing circuitry is situated close to the array and the analog-to-digital conversion and digital processing and timing are remotely located. A separate console contains the digital data tape recorder and its associated processing circuitry. The composite test bench and data recording system are shown in figure 9. The optical bench is shown in figure 10.

The test setup allows testing of a six-chip (576 element) array and an 18-chip (1728 element) array. Since every effort was made to minimize the processor changes to meet these two operating conditions, only a few changes were made to accommodate these conditions and are noted in the technical discussion.

2.4.1.1 Scene Simulation

The simulated scene is a 2-inch by 2-inch transparency mounted on a positioning table to form a moving target scene simulator. The table is moved across-scan (along-track motion) and scene motion is provided by a 0.1-inch lead ball screw driven by a precision stepping motor. The motor drive is synchronous with the array scan, allowing at least one full integration period to occur while the scene is stopped. It is this line of data which is processed. Each step is a fraction of a resolution element. Because of a magnification difference required for the 576-detector and 1728-detector arrays, different motor steps are required per resolution element motion of the scene. Positional accuracy is better than 2.5 percent of a resolution element per scan line and 15 percent maximum per scene due to a nonaccumulative 5 percent of motor step contributed by the motor and a 0.0005 in/ft for the lead screw. These accuracies prevent scene distortions due to the scene simulator but use standard quality components.

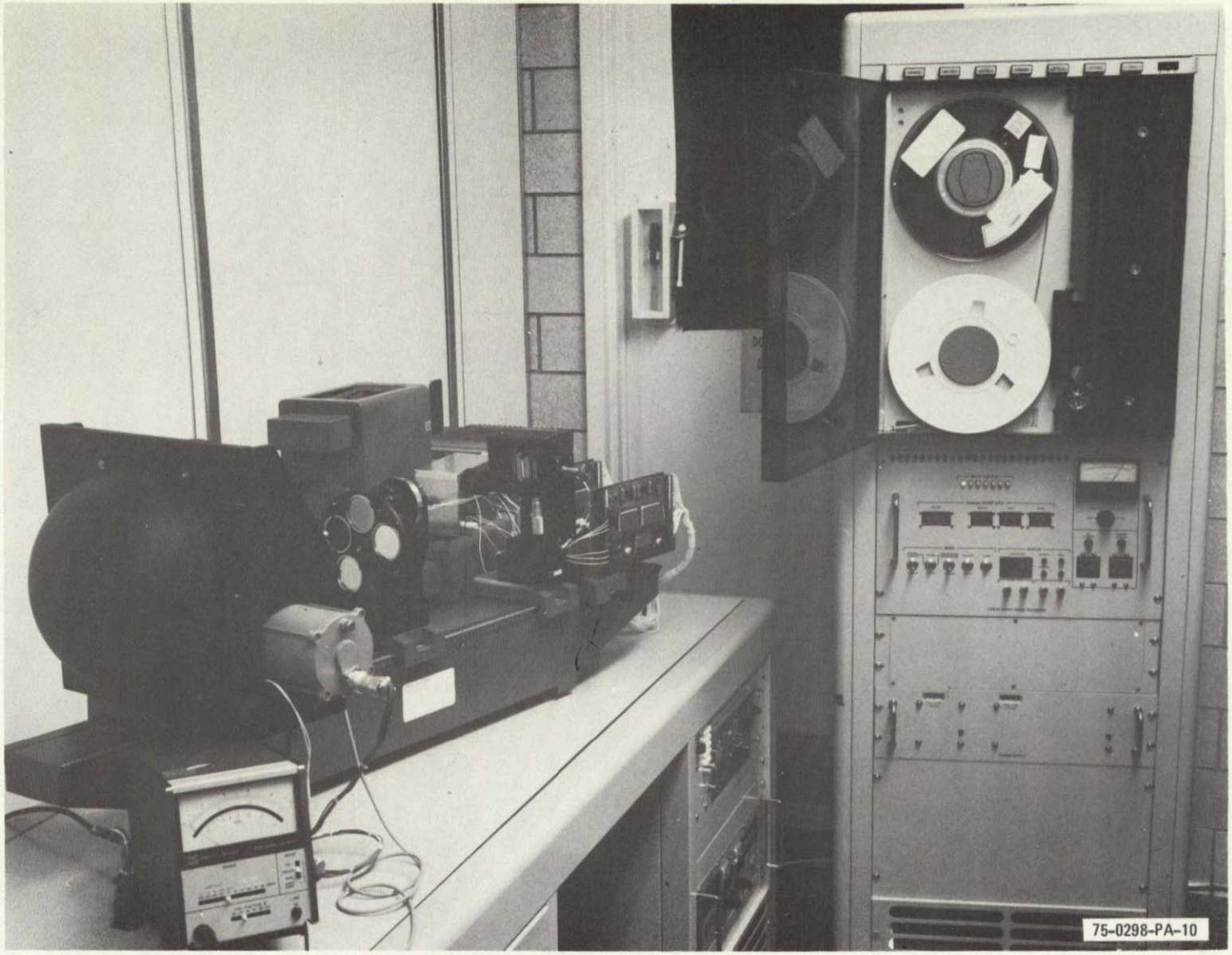

Figure 9. Test Bench and Data Recording System

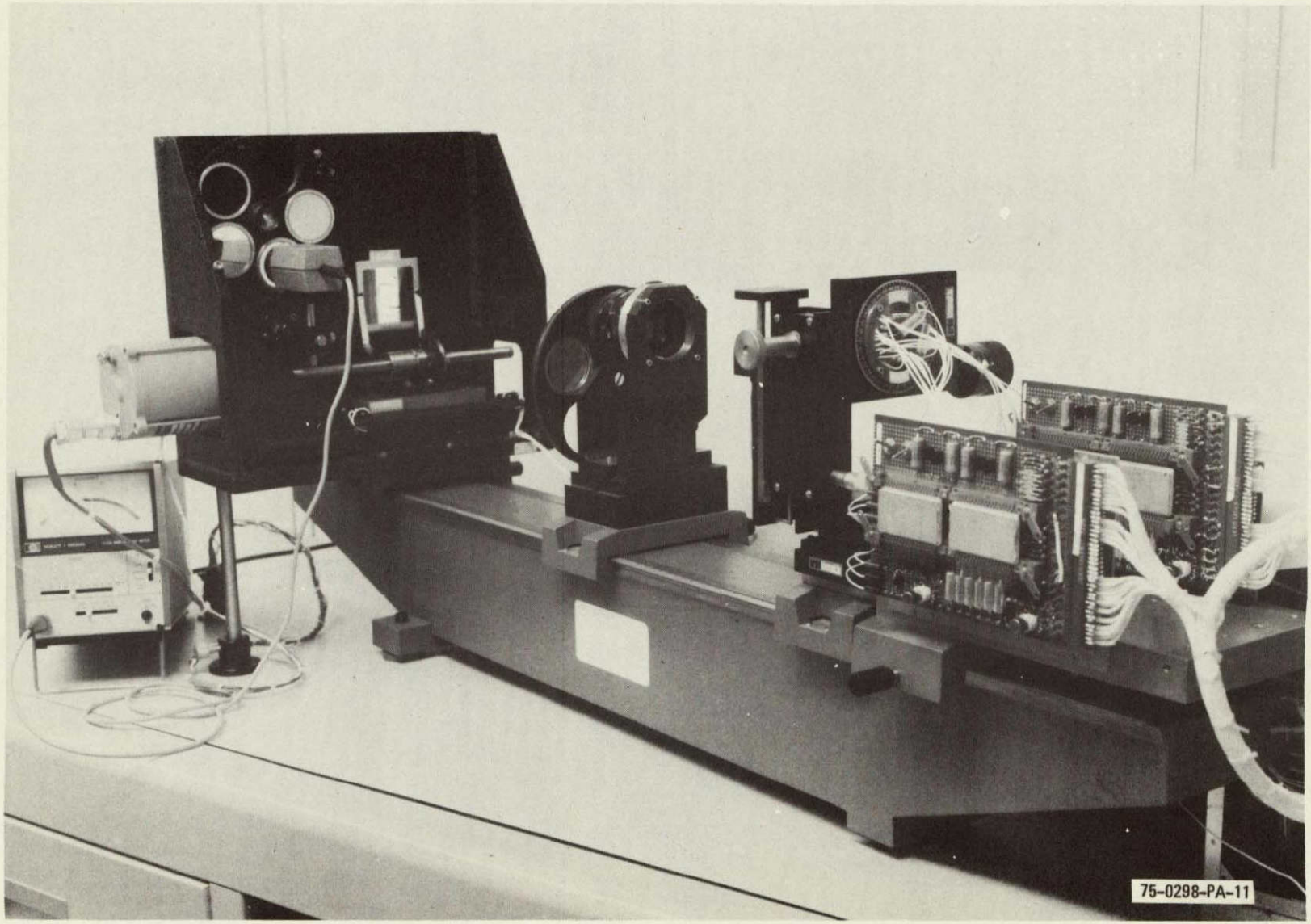

Figure 10. Optical Bench Showing Light Source, Scene Translator, Filter Wheels, Linear Detector Array and Mount, and Analog Processing Electronics

2.4.1.2 Radiant Source

The radiant source is a 10-inch diameter hemisphere with a high reflectance white interior. A 150 watt dc tungsten (3300K) bulb is located at the radius center and two apertures are cut in the flat surface cover. These apertures are: (1) a slit to back-irradiate the scene transparency, and (2) a circle to allow direct radiance measurement. The aperture areas are approximately equal, thereby minimizing the radiance measurement error. A Hewlett-Packard Radiant Flux Meter and Detector (Model 8330A/8334A) with an Infrasil window and thermopile detector are used for radiance monitoring. Levels are controlled by adjusting the dc lamp power supply. This source with the radiometer provides the capability for the specified radiance levels and the 5 percent of the full-scale measurement range. See Appendix I for the radiometer calibration results.

2.4.1.3 Spectral Separation

Spectral separation is achieved with thin film filters. Three bandpass filters centered at 0.55, 0.65, and 0.75 microns with 0.08-micron width are used. A long pass filter with a short wavelength cutoff at 0.8 micron provides the near IR band. The filters have a peak transmission greater than 60 percent. Characteristics of the filters are shown in figure 11. Although these "off the shelf" filters did not meet the 70 percent peak transmission of the original specification, they were chosen with NASA concurrence as fullfilling the intent of the program.

2.4.1.4 Detector Array Mount

The detector array is mounted in a micropositioning mount (see figure 12). It is adjustable along each axis and can be rotated about the optical axis and about the axis orthogonal to both the array and optical axis. This allows enough freedom to align the array relative to the scene and to finely adjust the focus. Either the 576- or 1728-detector array can be used in the micropositioner. This capability was required to overcome the coarse focus capability of commercial optics.

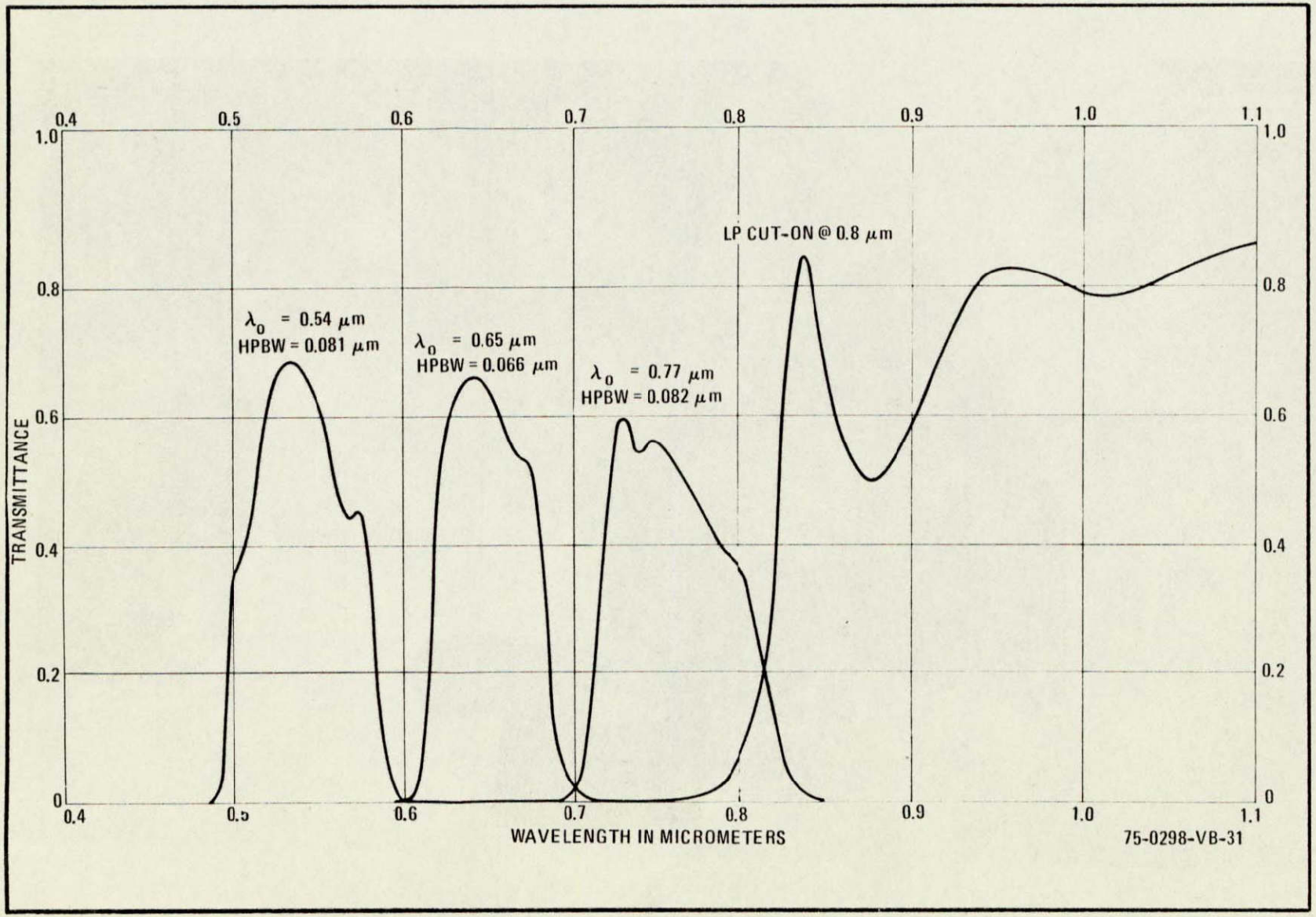

Figure 11. Filter Characteristics

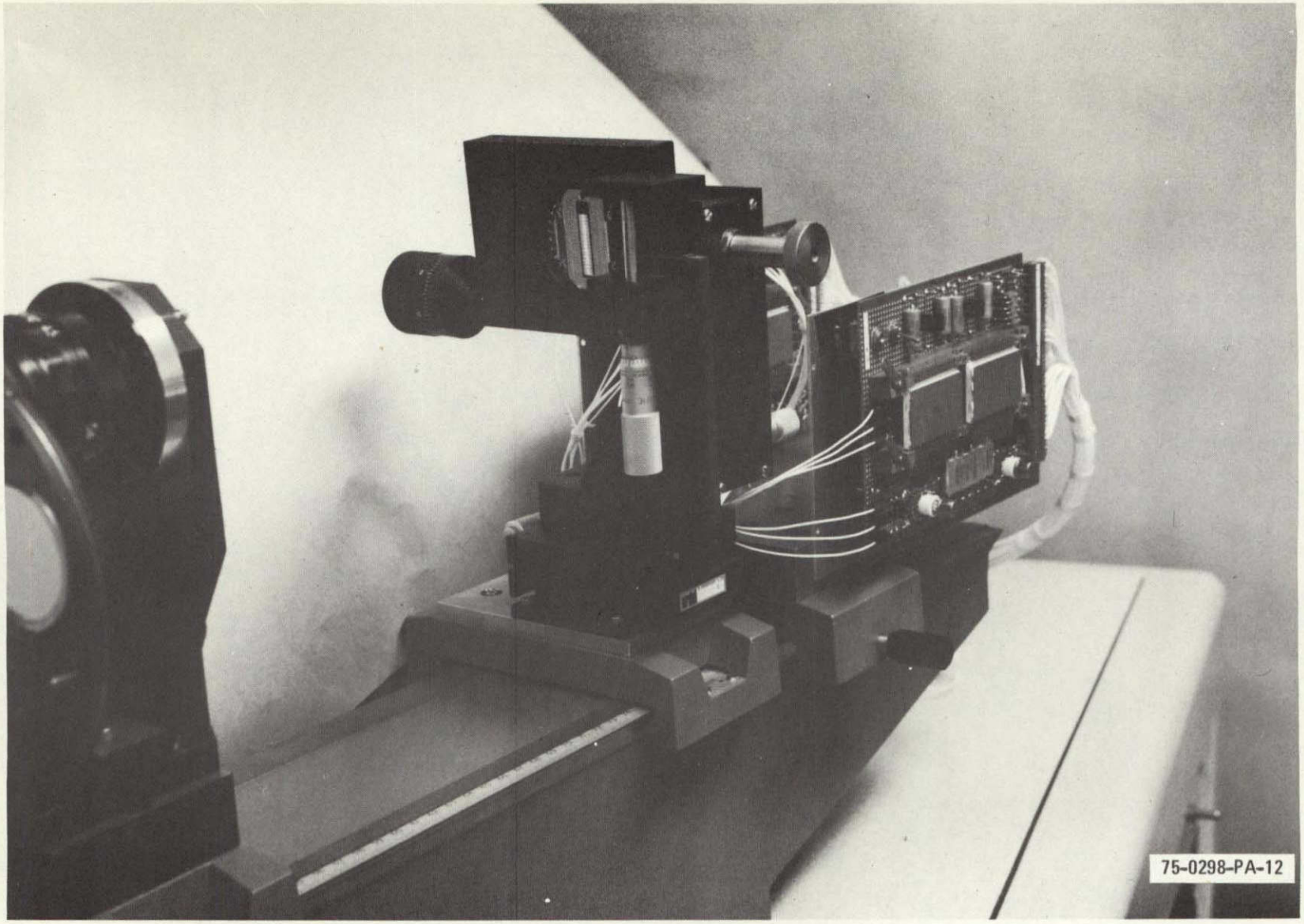

Figure 12. Detector Array in Micropositioning Mount

2.4.1.5 Optics

High quality commercial photographic lenses are used for the optical system. A 55 mm, f/3.5 lens optimized at 610 mm (2 feet) is used for the 576-detector array. The 1728-detector array uses a Nikon 150 mm, f/5.6 El-Nikkor enlarger lens. Optical distances and magnification were arranged to allow an integral number of motor steps per IFOV. For the 576-detector array, the object to image distance is 434 mm with a magnification of 0.172. The 1728-detector array has an object to image distance of 642 mm and a magnification of 0.600.

A squarewave MTF measurement was made using the 150 mm lens set at f/8. The measurement was made using the breadboard's spectral filters. The optical distances were made equivalent to the breadboard with a silicon detector used in the image plane to measure the response. The results of these squarewave MTF measurements for the 150 mm lens are shown in figures 13 through 16.

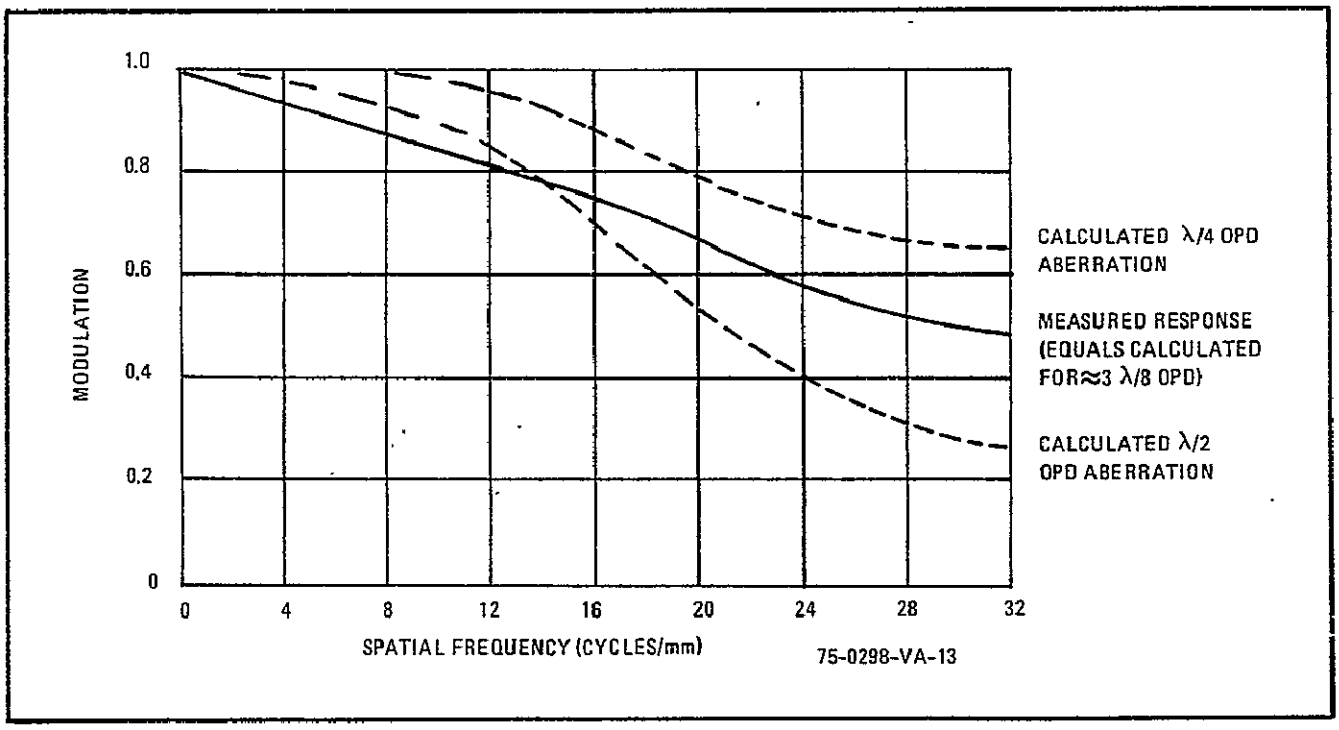

Figure 13 Lens MTF (Squarewave Response) for $\lambda = 0.55$ μm

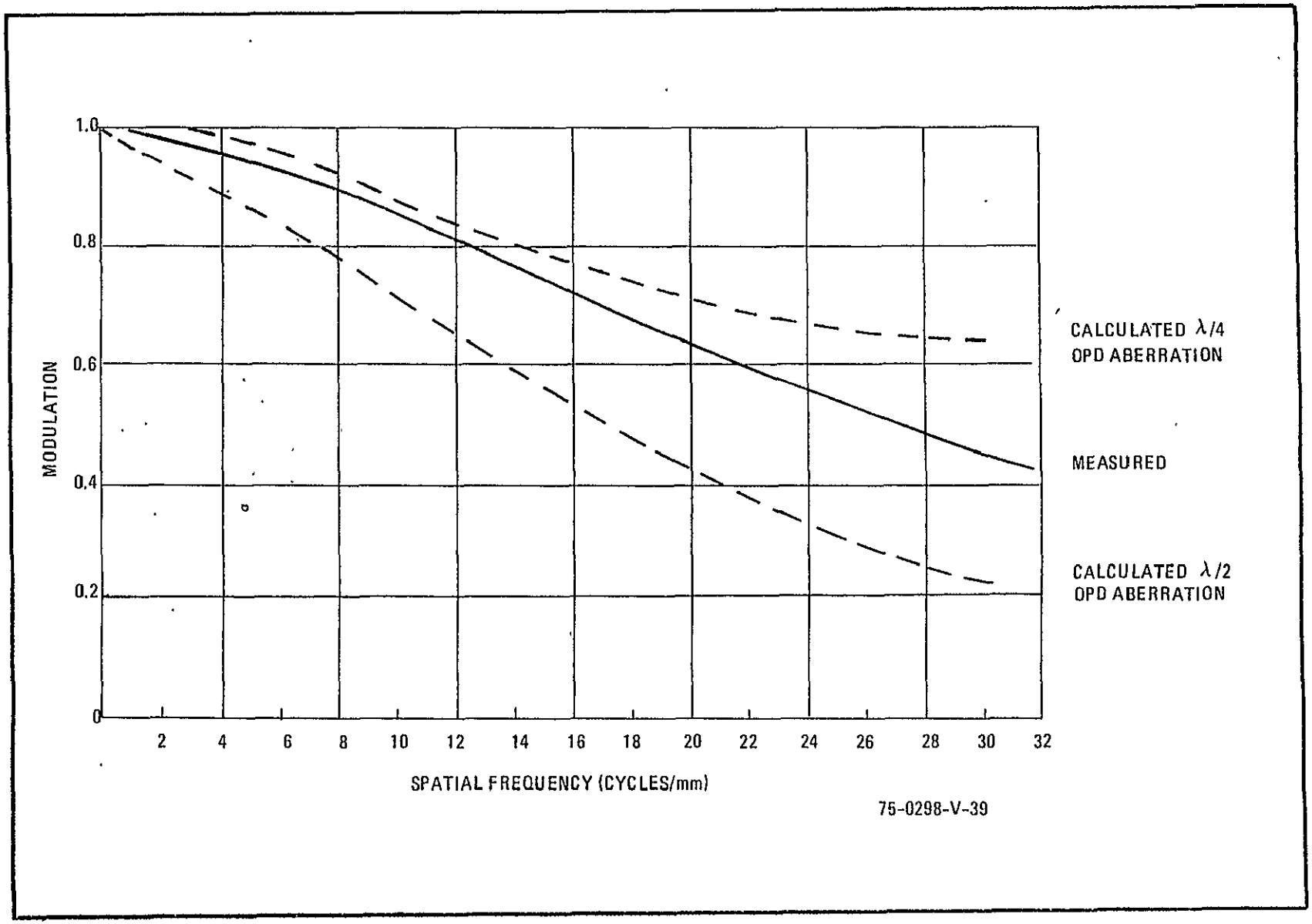

Figure 14. Lens MTF Squarewave Response 0.65 μm = λ

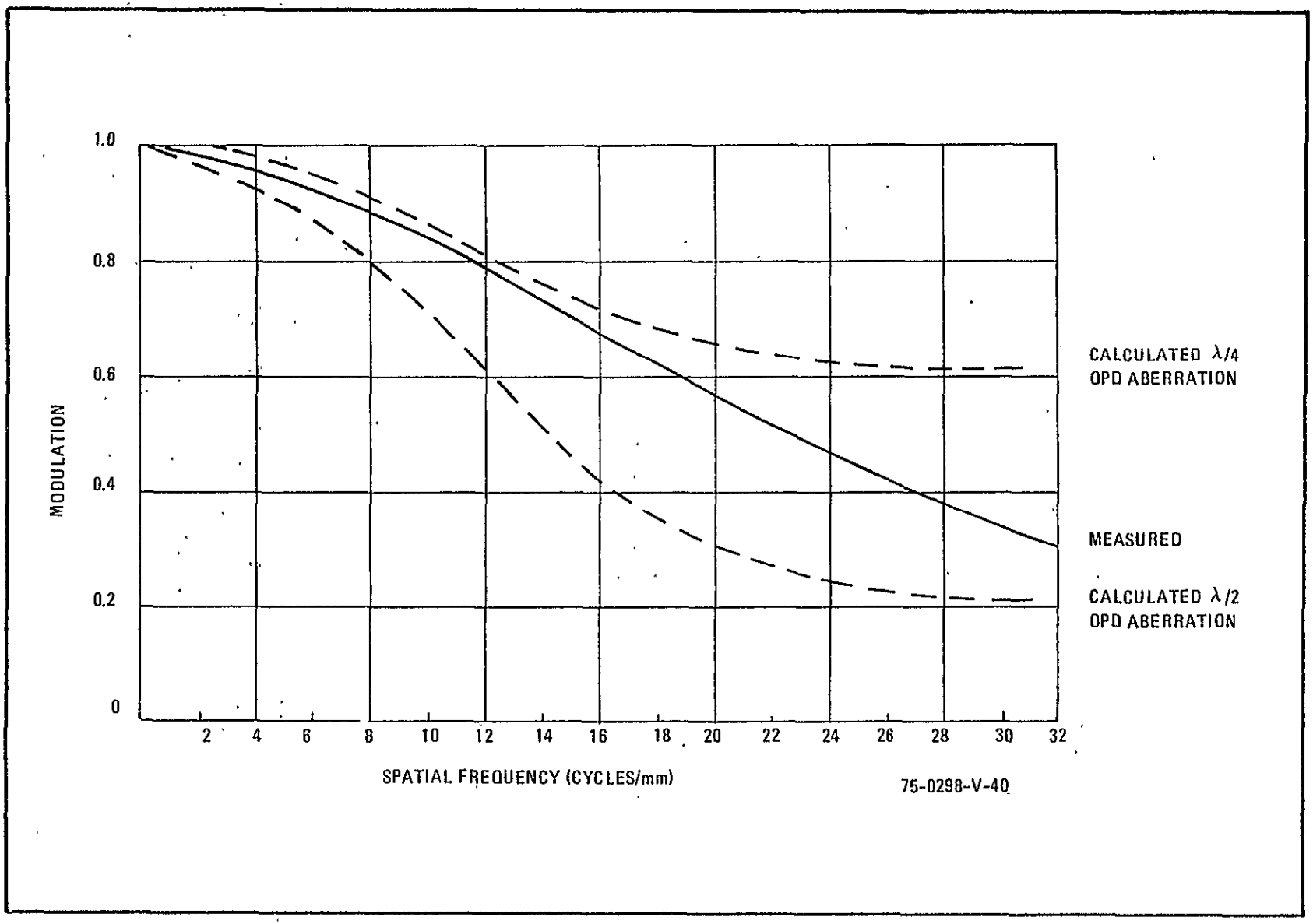

Figure 15. Lens MTF Squarewave Response 0.75 μm = λ

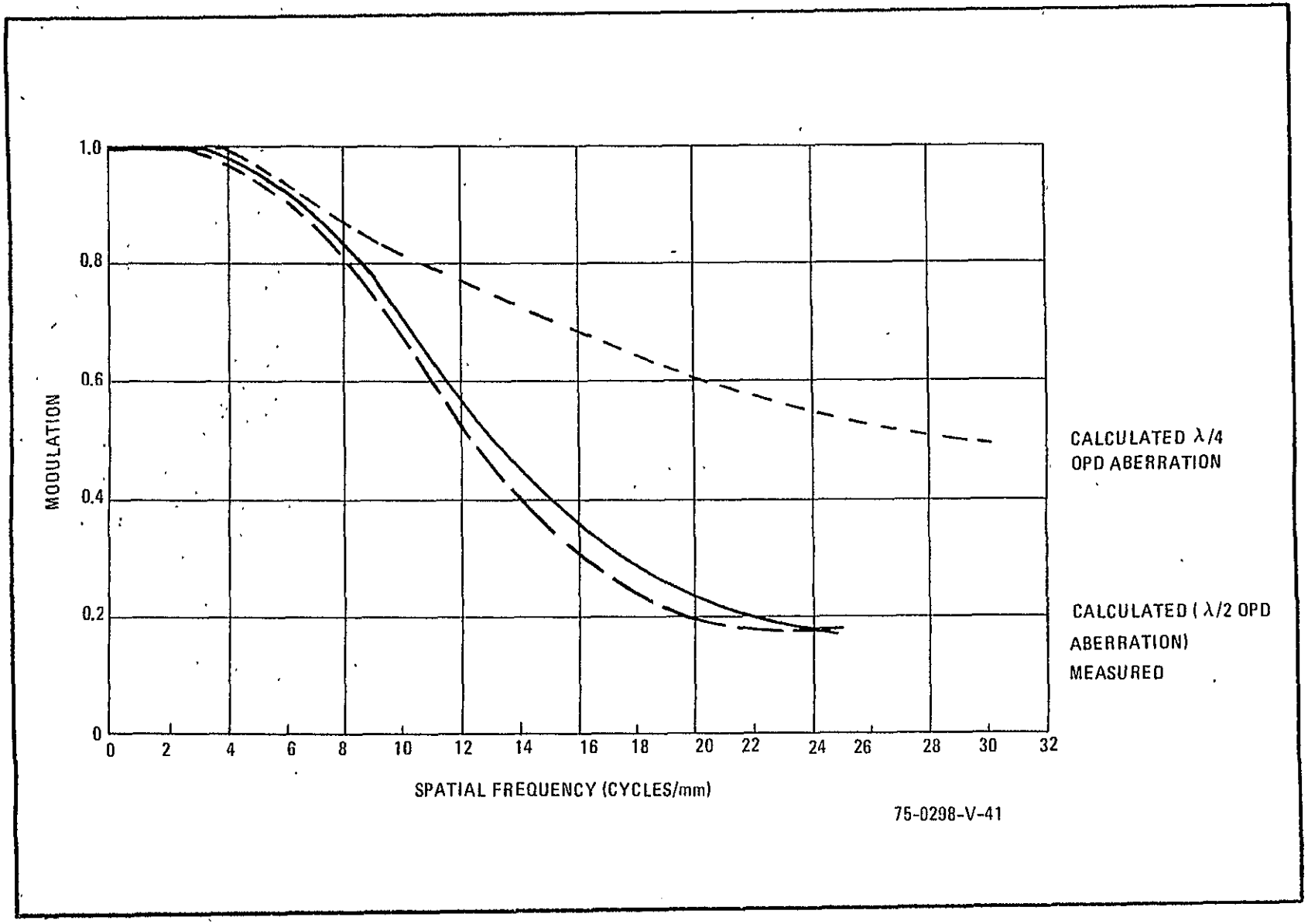

Figure 16. Lens MTF Squarewave Response 1 μm = λ

These figures include the calculated squarewave response for $\lambda/4$ and $\lambda/2$ OPD (optical path difference) third order spherical aberation.[2] An f/number of 12.8 is used for the calculation. The f/12.8 is the effective f-number calculated for the image distance of the breadboard.

The photographic lenses used in the breadboard although of high commercial quality were not diffraction limited, therefore contributed to a reduction of system MTF. The lenses, however, were of sufficient quality to produce high quality imagery, a primary program objective.

2.4.2 Electronic Processing and Timing

The following sections describe the analog processing and timing circuits required to process the photodiode video data. It is important to note that the analog processor demonstrated an ability to meet program requirements. The timing circuits performed all functions satisfactorily and were flexible enough to permit the operation of two different size arrays (576 elements and 1728 elements).

2.4.2.1 Analog Signal Processing

The analog processor accepts the detector array output, derives the video signal, amplifies the signal, then stores it for A/D conversion. Figure 17 is a simplified schematic of the circuit configuration. Early in the program, discrete, hardwired components were used in the analog processor. A later phase modified the processor to a multichip hybrid package (MHP). The conversion from the discrete component analog processor to the multichip hybrid package is discussed in paragraph 2.4.2.2.

There are several constraints on the performance of the first analog processor amplifier. This amplifier must provide as much gain as possible to minimize the latter stage gain, but not exceed its dynamic range with detector chip bias current differences. The frequency response (and slew rate) must be wide enough to allow sufficient video sample time and small error even after

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[2] Smith, Warren J., Modern Optical Engineering, McGraw-Hill Book Company, page 322.

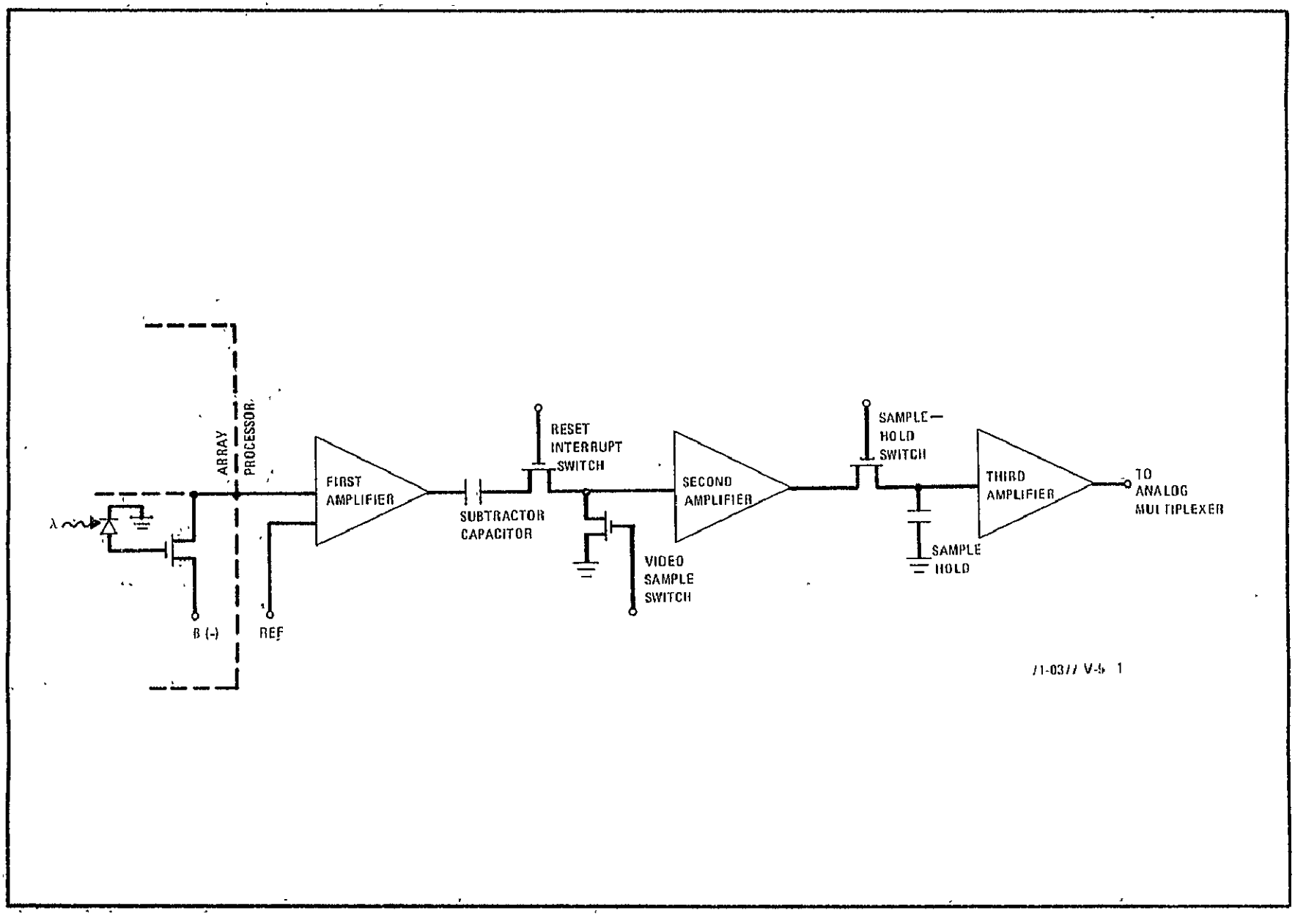

Figure 17. Simplified Signal Processing Schematic

chip transitions, but preferably narrow enough to keep the noise bandwidth low and therefore, a low noise amplifier is required. In the breadboard, a Westinghouse type WA 1006 operational amplifier is used. Since the WA 1006 must operate on low power supply voltages, such as +5 and -2, the available dynamic range is limited. The bias current variations in the group of chips used in the array was in the range of 300 to 400 μA. With a 4-volt maximum output range, the feedback resistor was limited to 10kΩ. An input resistor was selected to provide the nominal bias current for each of the four buses. This typical resistor was 2kΩ. The amplifier bandwidth is approximately 800 kHz and voltage gain is 5, giving a Johnson noise at the amplifier output of approximately 25 μV rms. A measurement of a typical amplifier output indicated that a factor of 3 increase in noise is likely due to the amplifier. This gives a total processor-only noise of 75 μV rms at the first amplifier output. The gain from the first amplifier output to the analog channel output is 210. Additions to noise beyond the first amplifier are considered negligible since the first stage noise gain is greater than five. The RSS (root-sum-square) for noise contribution at the second stage (assuming a noise equal to the first stage input) increases the total noise by 2 percent. The impedance of the second stage is lower than the input and thus contributes even less noise.

A computer processed noise run (see Appendix B) using the MHP amplifiers indicated that the average noise is 0.566 counts (see table 4). This is equivalent to 100 μV at the first amplifier output or an NEI of 0.39 μjoule/m^2 in the 0.5 to 0.6-μm spectral band. Three buses (A, B, D) show 0.32 μjoule/m^2 noise and one bus (C) indicates a 0.48 μjoule/m^2 equivalent noise. The analog-to-digital quantization uncertainty is 0.2 μjoules/m^2 (see table 5) in the 0.5 to 0.6 μm band. The quantization uncertainty[3] is the quantization interval/$\sqrt{12}$.

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[3] Schwartz, M., "Information Transmission Modulation and Noise," McGraw-Hill, page 329.

TABLE 4

144 RMS NOISE SAMPLES FOR EACH OF FOUR MHP ANALOG PROCESSORS

MPH NO.

1	2	3	4	3	4	1	2	1	2	3	4	3	4	1	2
.37	.69	.25	.42	.42	.45	.46	.71	.51	.77	.50	.50	.44	.50	.49	.79
.50	.74	.50	.50	.48	.49	.49	.77	.50	.73	.51	.51	.46	.49	.49	.73
.50	.75	.50	.50	.46	.50	.49	.74	.50	.73	.50	.49	.48	.50	.50	.76
.50	.71	.50	.50	.48	.48	.50	.69	.50	.76	.50	.50	.47	.51	.50	.77
.49	.75	.51	.50	.48	.49	.50	.69	.51	.75	.50	.50	.47	.49	.49	.72
.48	.74	.51	.50	.48	.49	.50	.75	.50	.75	.50	.50	.48	.50	.49	.73
.50	.64	.50	.50	.50	.51	.51	.71	.51	.75	.50	.50	.48	.50	.51	.72
.48	.70	.50	.49	.47	.50	.49	.77	.49	.73	.50	.50	.47	.50	.49	.74
.49	.73	.50	.50	.47	.49	.52	.70	.50	.72	.50	.49	.47	.49	.50	.78
.48	.71	.50	.50	.46	.49	.50	.78	.49	.75	.51	.52	.48	.50	.50	.74
.50	.69	.50	.50	.47	.50	.51	.71	.49	.71	.50	.50	.47	.50	.49	.70
.49	.74	.51	.50	.49	.50	.49	.71	.50	.76	.50	.50	.47	.50	.51	.74
.48	.73	.50	.50	.47	.50	.50	.67	.49	.81	.50	.50	.48	.51	.50	.77
.49	.68	.50	.50	.48	.50	.51	.74	.49	.72	.50	.50	.47	.49	.50	.68
.46	.70	.50	.50	.48	.50	.50	.70	.48	.72	.50	.50	.48	.50	.51	.76
.49	.73	.50	.50	.48	.50	.50	.75	.49	.69	.50	.50	.47	.50	.51	.75
.48	.69	.50	.50	.48	.50	.50	.75	.48	.72	.51	.49	.48	.50	.51	.72
.49	.77	.52	.51	.47	.50	.50	.63	.48	.69	.50	.50	.47	.50	.50	.73
.48	.72	.51	.50	.47	.50	.52	.79	.49	.69	.50	.50	.47	.50	.51	.75
.48	.73	.50	.50	.48	.50	.50	.74	.49	.71	.52	.51	.46	.50	.52	.71
.50	.74	.50	.50	.47	.50	.51	.73	.48	.78	.50	.50	.47	.50	.50	.72
.53	.67	.51	.50	.48	.50	.52	.69	.48	.68	.50	.50	.51	.49	.51	.73
.47	.70	.50	.50	.48	.50	.50	.66	.52	.72	.51	.51	.47	.50	.52	.72
.49	.79	.50	.50	.50	.49	.50	.73	.49	.71	.54	.50	.49	.50	.50	.76
.48	.72	.50	.50	.47	.50	.50	.97	.46	.70	.50	.50	.49	.50	.50	.68
.51	.77	.53	.50	.48	.50	.51	.72	.52	.72	.51	.50	.47	.50	.52	.75
.48	.69	.50	.50	.50	.50	.49	.72	.49	.74	.50	.48	.49	.51	.52	.72
.50	.75	.51	.50	.48	.50	.54	.71	.50	.70	.50	.50	.52	.50	.50	.72
.49	.75	.51	.48	.49	.50	.52	.76	.52	.78	.50	.50	.48	.50	.51	.76
.48	.74	.50	.50	.48	.50	.49	.71	.49	.77	.53	.50	.45	.49	.50	.70
.49	.73	.51	.51	.46	.50	.52	.69	.48	.77	.50	.50	.49	.49	.50	.75
.49	.79	.54	.49	.48	.50	.50	.78	.51	.76	.50	.50	.48	.49	.55	.79
.48	.76	.50	.50	.50	.51	.50	.71	.49	.73	.50	.50	.47	.50	.50	.71
.49	.72	.51	.50	.46	.50	.53	.75	.49	.66	.51	.49	.48	.50	.50	.72
.49	.74	.50	.50	.46	.50	.51	.73	.52	.73	.50	.50	.47	.50	.49	.71
.50	.70	.50	.50	.49	.50	.50	.71	.49	.72	.50	.83	.48	.50	.50	.70

AVERAGE RMS NOISE IN $\mu J/M^2$	MHP NO. 1
0.35	1
0.50	2
0.35	3
0.36	4

THIS IS THE COMPUTER PRINTOUT (SEE APPENDIX B) OF THE MHP ANALOG PROCESSOR RMS NOISE. FOR THIS CALCULATION, THE SYSTEM GAIN FROM SOURCE TO OUTPUT IS 1.3 COUNTS/$\mu J/m^2$. THE AVERAGE OF THE RMS VALUES FOR THE MHP ANALOG PROCESSOR IS 0.39$\mu J/m^2$ FOR A LENS TRANSMISSION OF 90 PERCENT IN THE 0.5-0.6μm BAND. THIS MEASUREMENT WAS MADE WITH A RESISTOR TO SIMULATE THE ARRAY IMPEDANCE.

TABLE 5

ANALOG-TO-DIGITAL RMS QUANTIZATION ERROR

PICTURE NO. 1
DET NOISE HI GAIN MAX INPUT = 24.50
QUANTIZING ERROR

.86	.33	.21	.21	.20	.19	.27	.19	.25	.17	.20	.19	.19	.17	.28	.16
.25	.16	.19	.18	.19	.17	.27	.16	.25	.16	.19	.17	.18	.17	.26	.16
.24	.15	.18	.17	.17	.16	.25	.16	.23	.15	.18	.17	.17	.16	.25	.16
.23	.15	.18	.17	.17	.16	.24	.15	.23	.15	.19	.17	.17	.16	.25	.16
.23	.15	.18	.17	.17	.16	.25	.16	.23	.15	.18	.17	.17	.16	.24	.15
.22	.15	.18	.17	.16	.16	.23	.16	.22	.15	.19	.17	.18	.16	.39	.21
.00	.22	20.33	.19	.00	.18	.20	.16	.24	.17	.00	.19	.72	.20	.12	.18
.14	.16	.19	.17	.20	.19	.25	.17	.18	.18	.19	.19	.18	.17	.21	.16
.25	.16	.19	.18	.18	.18	.25	.16	.23	.17	.18	.18	.17	.18	.25	.16
.15	.17	.41	.19	.18	.19	.30	.16	.24	.18	.20	.19	.00	.19	.18	.17
.26	.18	.23	.19	.20	.20	.29	.17	.25	.18	.19	.19	.17	.18	.25	.17
.24	.18	.20	.20	.17	.19	.27	.17	.24	.18	.20	.19	.17	.19	.40	.22
.00	.00	.00	.22	.19	.20	.24	.20	.24	.16	.18	.19	.21	.19	.26	.18
.25	.17	.20	.19	.18	.19	.28	.17	.25	.18	.20	.20	.19	.19	.28	.17
.25	.18	.20	.19	.20	.19	.16	.18	.31	.17	.19	.19	.19	.19	.29	.18
.24	.18	.20	.20	.20	.19	.28	.18	.25	.18	.20	.20	.20	.20	.28	.18
.25	.18	.21	.21	.16	.18	.28	.17	.25	.17	.20	.20	.20	.19	.27	.18
.25	.17	.19	.20	.18	.19	.27	.18	.24	.22	.20	.19	.18	.19	.39	.23
.00	.23	.17	.17	.18	.16	.19	.15	.23	.16	.18	.18	.17	.18	.27	.17
.25	.17	.18	.17	.17	.17	.26	.16	.25	.16	.18	.16	.17	.17	.25	.16
.25	.16	.18	.16	.16	.17	.26	.16	.26	.16	.18	.17	.16	.17	.26	.16
.25	.16	.18	.17	.16	.18	.27	.17	.27	.16	.19	.17	.16	.18	.27	.17
.26	.17	.19	.17	.15	.18	.25	.17	.25	.17	.18	.17	.16	.18	.27	.17
.26	.17	.18	.17	.17	.18	.26	.16	.26	.17	.19	.17	.19	.19	.45	.00
1.05	.28	.18	.21	.17	.18	.22	.18	.28	.16	.16	.16	.15	.15	.24	.16
.27	.15	.16	.16	.15	.15	.24	.15	.26	.15	.15	.16	.15	.15	.26	.15
.26	.14	.15	.15	.15	.14	.24	.15	.26	.14	.15	.16	.15	.15	.23	.15
.25	.14	.15	.15	.14	.15	.24	.15	.26	.14	.15	.17	.14	.15	.23	.16
.25	.15	.15	.16	.14	.16	.23	.16	.24	.15	.14	.17	.14	.15	.22	.16
.25	.14	.15	.16	.14	.16	.23	.15	.25	.15	.15	.16	.15	.00	.38	.00
.00	.00	.25	.33	.20	.18	.23	.20	.22	.17	.19	.19	.20	.20	.28	.19
.27	.20	.21	.21	.23	.21	.30	.19	.29	.19	.21	.20	.19	.19	.27	.18
.26	.18	.20	.20	.20	.20	.26	.19	.25	.18	.19	.19	.20	5.26	.30	.12
.32	.11	.22	.15	.17	.11	.00	.16	.23	.18	.20	.20	.19	.22	.24	.19
.26	.21	.19	.22	.20	.22	.26	.19	.25	.20	.20	.21	.19	.20	.25	.20
.23	.19	.19	.20	.17	.19	.22	.18	.25	.18	.18	.20	.17	.23	.33	.00

THIS IS THE COMPUTER PRINTOUT OF THE RMS QUANTIZING ERROR DUE TO ANALOG-TO-DIGITAL CONVERSION. THE NUMBERS IN THE TABLE ARE DETERMINED BY DIVIDING THE MEASURED QUANTIZATION INTERVAL BY $\sqrt{12.}$ IN THIS PRINTOUT, THE QUANTIZATION ERROR TABULATED IS IN $\mu J/m^2$. IN CALCULATING THE AVERAGE OF THE RMS ERROR, INOPERATIVE DETECTORS ARE EXCLUDED. THE AVERAGE OF THE RMS NOISE VALUES FOR ANALOG-TO-DIGITAL CONVERSION IS $0.2\,\mu J/m^2$.

The array output is a current which includes the video information and a large bias level (see figure 18). The image information is the amplitude difference between the pre-reset (video) and post-reset (reference) current. This difference current is 20 μA or less, assuming a peak irradiance of 0.5 W/m^2 and a 1.5-msec integration period. The bias current is 1 mA or less and varies from chip to chip. Without chip selection, the chip-to-chip bias variation could be several orders of magnitude greater than the video signal level.

The first amplifier provides a dual function of current to voltage conversion and removal of the average bias level.

The pre- and post-reset differencing to extract the video is performed by a "keyed-clamp" circuit. A capacitor is charged to the pre-reset level by clamping one side to ground at the pre-reset time interval. At all other times, the clamp is opened. The clamp circuit output is the instantaneous first amplifier output less the stored value on the capacitor.

A series switch is included in this same area to open circuit the system during the reset period to prevent amplifier saturation. The combination series and clamp switches provide the charging impedance for the subtraction capacitor. It should be noted that this bandwidth essentially matches that of the first amplifier (800 kHz).

Selection of the time constant for the keyed clamp circuit involves the tradeoff of noise and offset. The circuit must have the speed to remove an offset that is much greater than the signal, but slow enough so as not to store noise pulses. The bias current changes between chips is nominally 10 times the 0.55-μm band, low level, full scale signal. In order to keep the coupled offset during chip to chip transitions below 1 percent of the full scale, a time constant of less than 1/7 of the pre-reset gate width is required. A factor of 1/10 was used, giving a coupling of 0.05 percent (0.5 to 1 percent of the signal full scale).

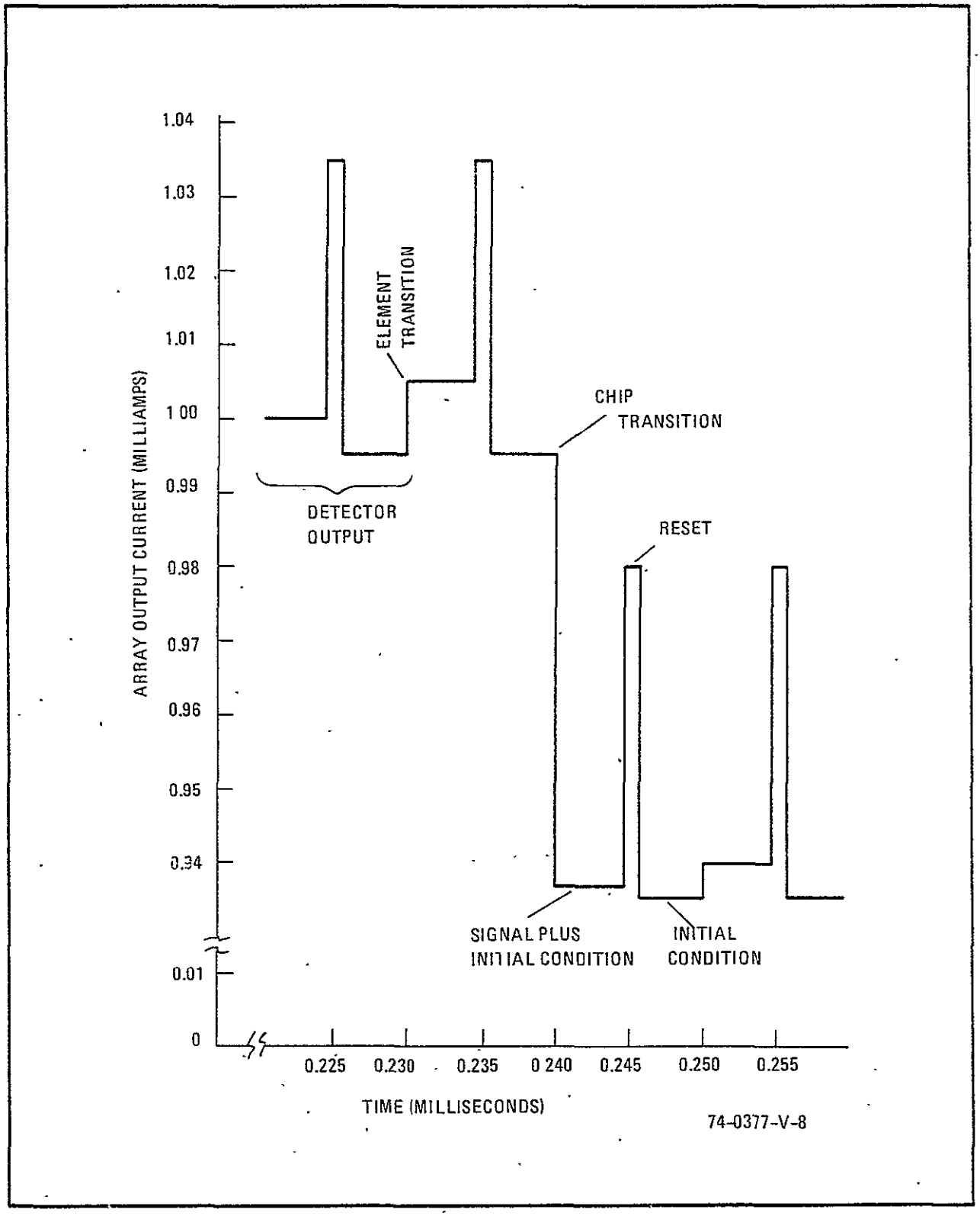


Figure 18. Array Signal Current (Waveform Representation)

The second amplifier provides gain and a buffer between the keyed clamp subtractor capacitor and the sample-hold circuit and has a gain of 21 switchable to a gain of 3. There is no external bandwidth limiting added to this amplifier. It is desirable to have the amplifier recover from degraded elements or high offsets as rapidly as possible. The internal amplifier response gives a closed loop bandwidth near 800 kHz.

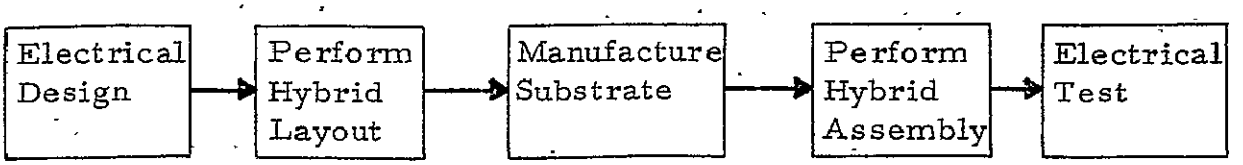
The sample-hold circuit samples the second amplifier output during the post-reset video period and holds it until the next element is sampled. A time constant to sample time ratio of 1/5 is used to keep signal cross-coupling below 1 percent.

The final amplifier provides a buffer and line driver. A National Semiconductor LH0003 is used with a gain of 10. This provides the 10-volt capability required for the A/D converters and causes a droop less than 1/2 an LSB (least significant bit) over the 10-μsec holding period.

A 4-μsec per conversion A/D converter is used for each channel. At the end of each element conversion, the data is stored in an 8-bit holding register. The data is multiplexed and sent to the recording encoder on eight lines in the correct pixel sequence. A clock signal is sent with each data word.

2.4.2.2 Analog Processor Conversion to Multichip Hybrid Package (MHP)

A change order to the contract provided for the conversion of the analog process electrical schematic (see figure 19) into a microminiature module. The MHP was expected to give more nearly detector-limited performance. The design procedure is shown below. The 1" x 2" package was chosen because it meets both the requirements of small size and ease in manufacture. The layout takes into consideration the output lines and the minimization of interconnection lead lengths between amplifier stages and the use of power line bypassing in several places to ensure decoupling.



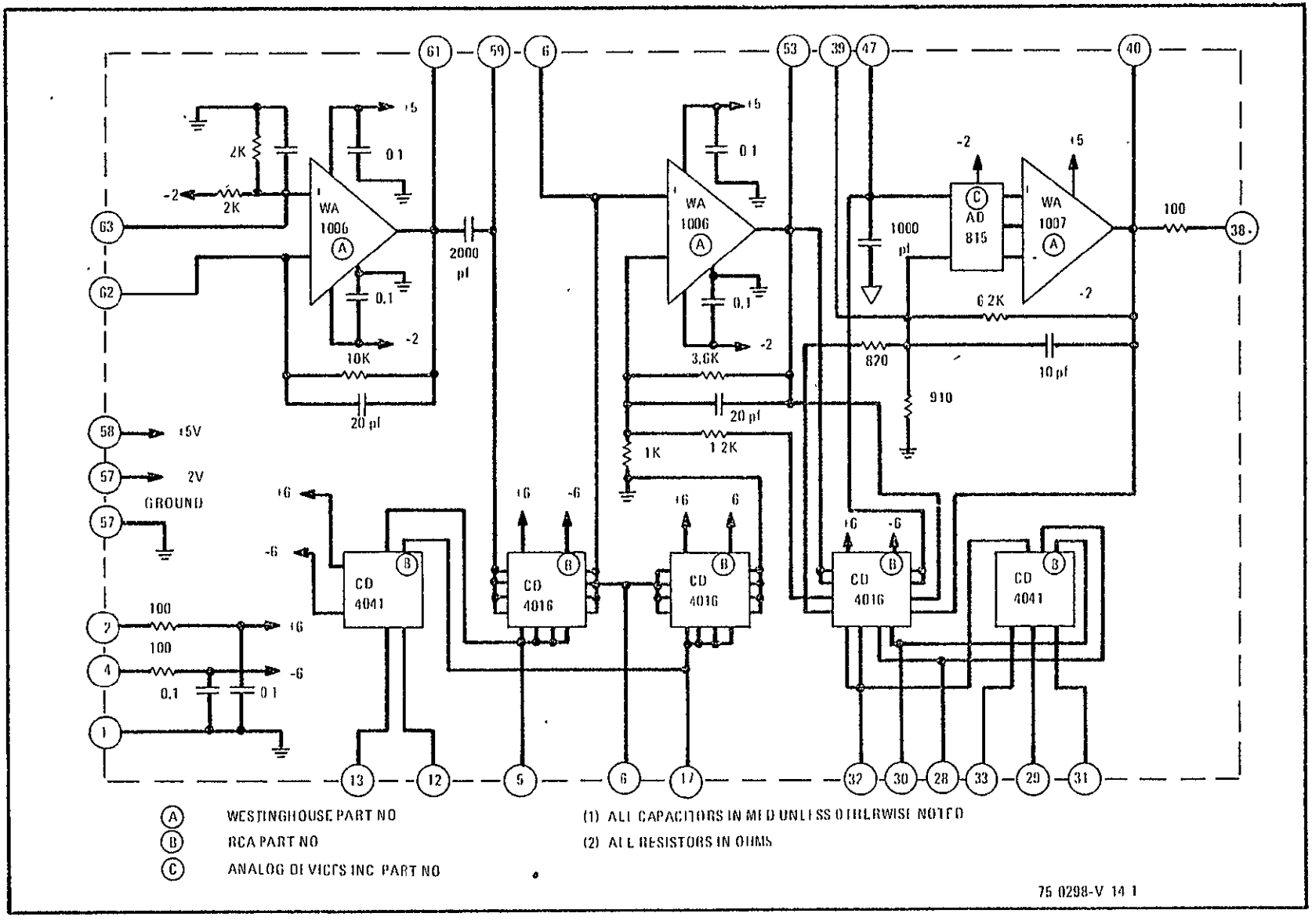


Figure 19. Analog Processor MHP Schematic

The layout is in three layers. The first layer is the main conductor layer where 85 percent of all necessary interconnections are made. The second layer is a dielectric which provides insulation between conductor layers as well as providing an insulation over which a wirebond passes. The third layer is the second conductor layer; this layer serves to interconnect the lines on the first conductor layer.

The layout, after it was checked for accuracy, was next converted into artwork necessary for the manufacture of the substrate. Each layer was screened, then fired onto the substrate and visually examined. After the third layer was screened and fired, the substrate was again visually examined and electrically checked, thus assuring a quality substrate. The amplifier substrate consists of two thick film-deposited conductive layers with one dielectric layer and is inspected. The components which already have been visually examined are mounted in their respective places using nonconductive adhesives. After curing, the components are wirebonded using gold thermocompression ball bonding techniques. This assures a reliable connection between component and conductor.

The finished analog processor is shown in figure 20.

2.4.2.3 Timing and Control

All timing and control functions, except for recorder encoding and control, are provided by the main timing circuitry. Figure 21 is the system timing diagram. A 3.6-MHz clock is divided to provide the 400-kHz data rate clock. A preset counter counts to 576 (96 times 6) at the 400-kHz rate to provide an end-of-line signal to enable synchronizing at the line scanning rate. A shift register provides 0.28-μsec, the basic timing interval over a 10-μsec period. All analog gates, A/D control, holding register load, and array clocks are determined by decoding the proper interval from the shift register.

The maximum rate at which the digital data tape recorder can accept data is significantly less than the detector array can produce. Therefore, the record rate is designed to accept only one of sixteen scan lines. The scan

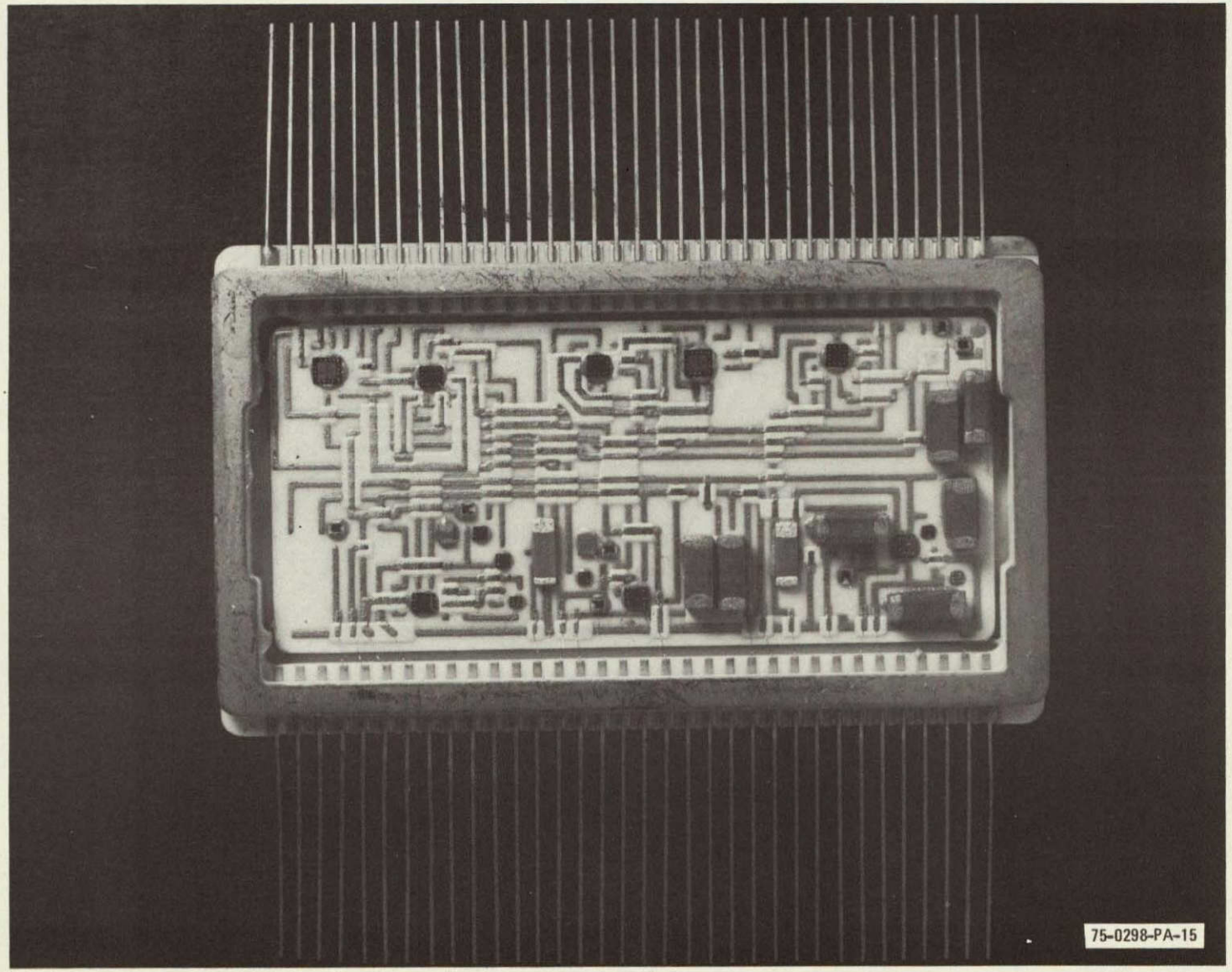


Figure 20. Analog Processor MHP

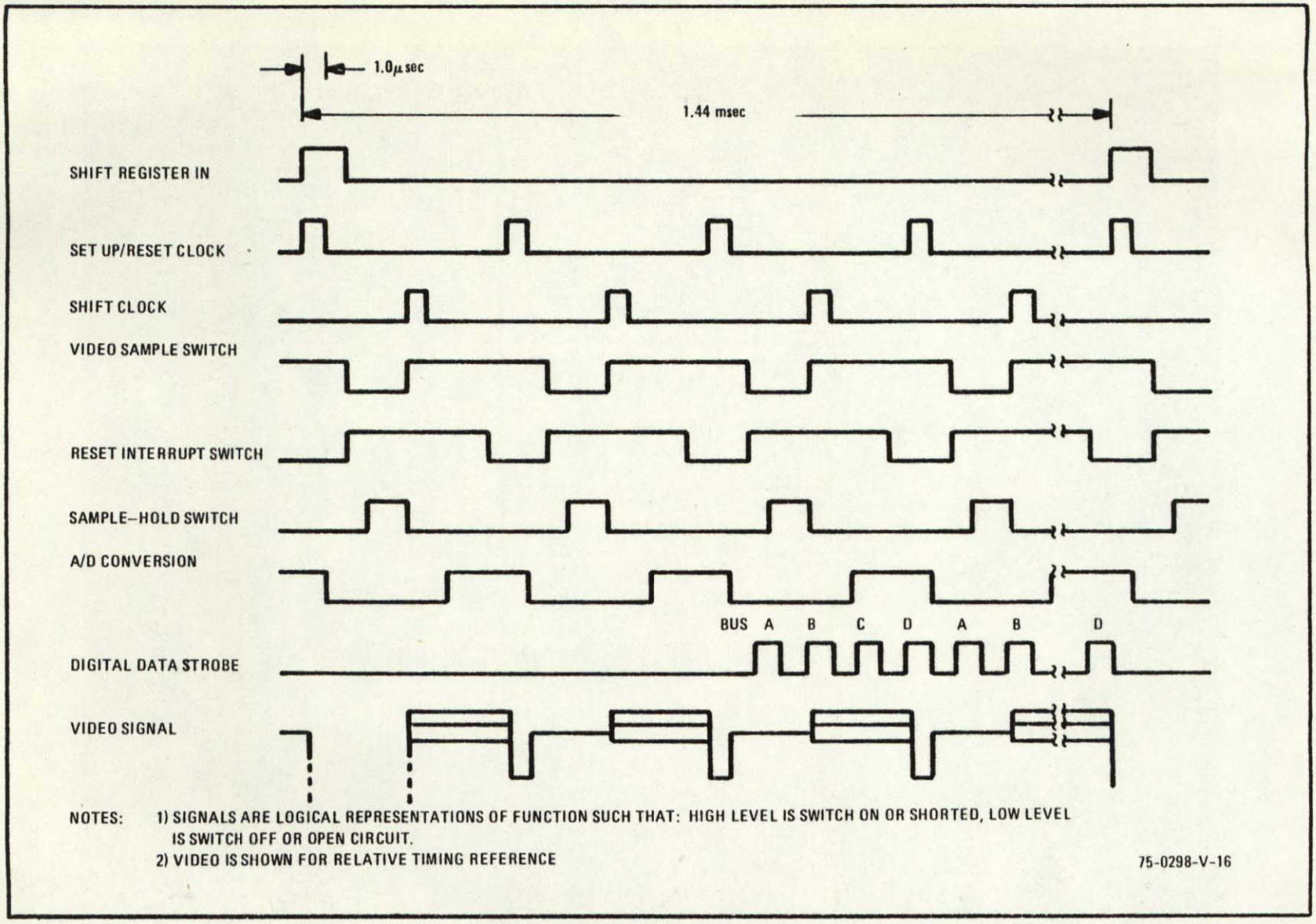


Figure 21. System Timing Diagram

line that is recorded represents one contiguous IFOV of the scene. During the interval between recorded data lines, the scene is translated and stopped prior to recording. The timing and logic is arranged to provide the correct number of motor steps (2 motor steps for the 18-chip array and 7 for the 6-chip array) to accommodate the different field-of-views required for the 6-chip and 18-chip arrays.

The clock signals used to control the timing of the analog processor and array use open collector TTL to increase the voltage limits. This 12V signal is ac-coupled for the negative voltage biased array and the bipolar analog gates. A CMOS CD4041 driver interfaces between the TTL and array inputs. CMOS CD4041 drivers also interface with the CD4016 analog switches in the processor.

2.4.3 Detector Array Design and Fabrication

A major objective of the breadboard program was to determine the feasibility of fabricating long detector arrays for possible use on future earth observation sensors. This section discusses the fabrication of detector arrays and both achievements and problem areas are identified.

2.4.3.1 Fabrication Techniques

An early program decision was to select a design which would allow replacement of individual chips. This was of particular importance with the limited number of chips available. During the program, several chips were successfully replaced.

The selected approach shown in figure 22 uses the "chip carrier" concept and the use of multi-level substrate interconnections. Each detector is cemented to a precisely machined chip carrier. The carriers are assembled on a baseplate with each aligned such that the chips form a contiguous line of detector elements. An appendage on the carriers extends beyond the chip edges, on alternating sides, providing a surface with up to twice the chip width for baseplate mounting. Figure 23 shows the assembled 6-chip array with this carrier arrangement. It is well to remember that one chip contains 96 detectors; therefore, six chips is equal to 576 detectors.

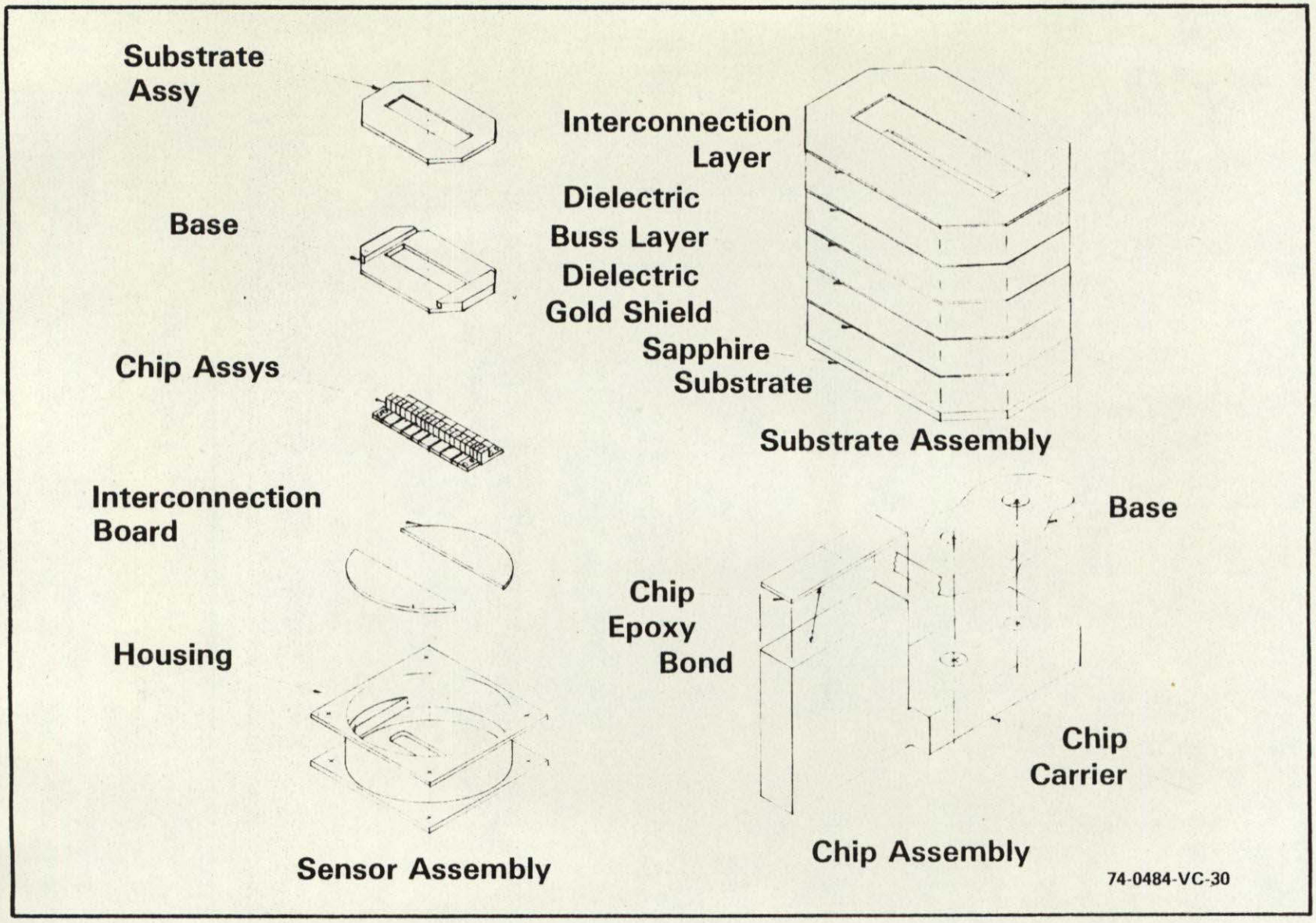


Figure 22. Chip Carrier and Array Assembly Technique

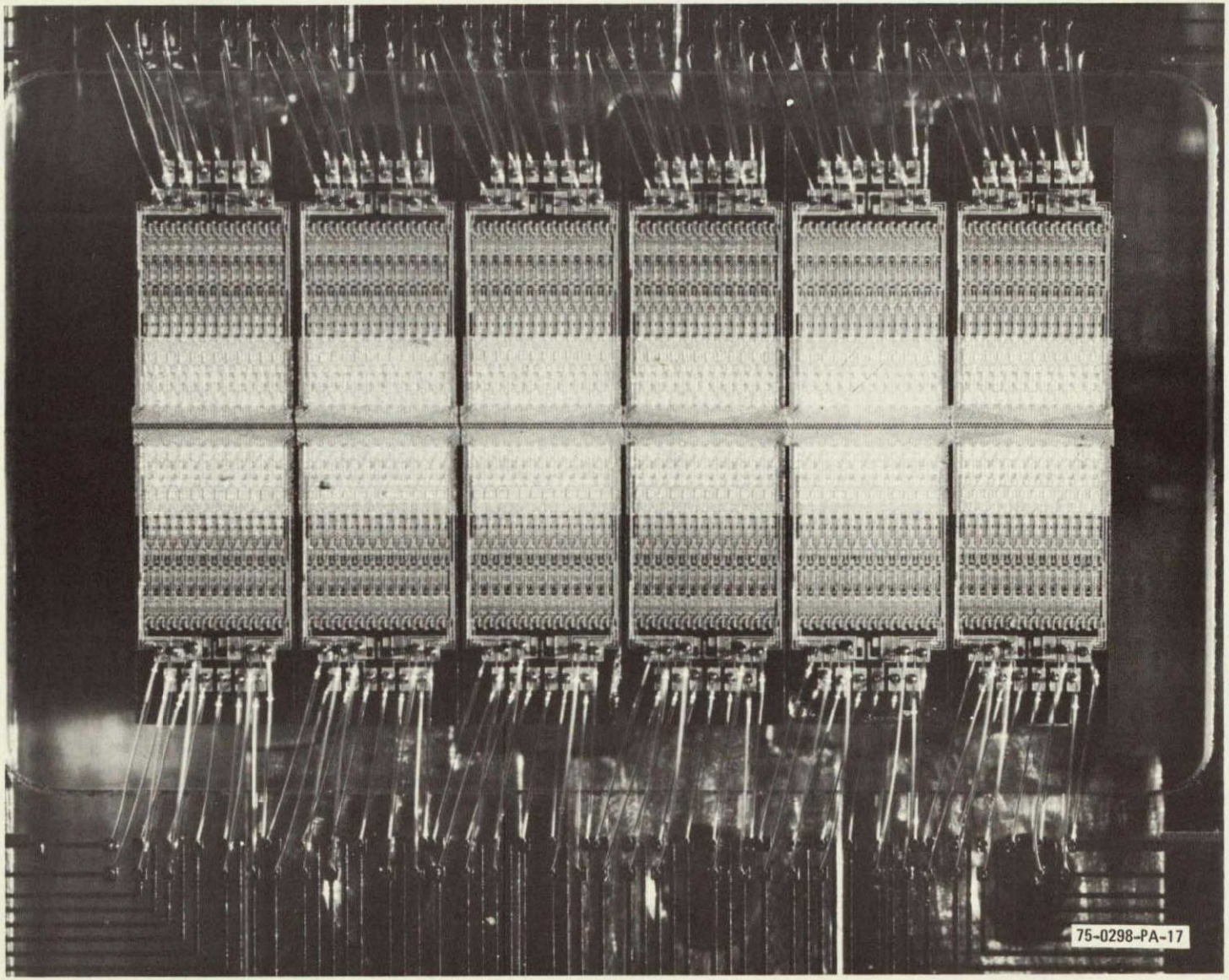


Figure 23. 6-Chip Array (576 Detectors)

The chips are cemented to the carriers with an epoxy cement double-sided film. The film cement eliminated possible metering problems associated with liquids. This also eased the handling and prevented seepage onto the chip surface. Curing is performed at 150°C and a jig is used to align the chip on the carrier during the cement curing period.

The chip alignment was performed by manipulating the baseplate mounted carriers while viewing the detector elements through a microscope. A custom fixture was used to elevate the array during alignment to allow access to the screws on the bottom surface. The chip carrier mounting screws could, therefore, be tightened while observing the chip alignment to detect movement of the carrier. A measuring stage was used with the microscope providing a means of measuring the final alignment accuracy. Using this measuring capability, all chips were assembled relative to a datum to prevent error accumulation. It is important to note that with this technique errors in the along scan direction are not accumulated. However, positional error can occur from one chip to an immediate neighbor chip. A measurement made on the 18-chip array indicated a maximum error of 0.15 mil (3.8 μm) between adjacent chips.

With the use of a measuring microscope, an imaginary reference line (best fit) was developed which minimized the maximum detector lateral excursion from the reference line. For the 6-chip array, the maximum lateral excursion was 0.2 mil (5.1 μm) and for the 18-chip array, the maximum lateral excursion was 0.3 mil (7.5 μm).

The errors in detector lateral excursion in the across-scan direction and positional error between adjacent chips in the along-scan direction are within the specification requirement of 1 percent of the array linear dimension.

For interconnecting the chips electrically, a substrate of synthetic sapphire was used on which gold conductor patterns had been deposited. This also provided the connection to the array package interface leads. All interconnect wires within the array package were gold and ultrasonically bonded. Rework of the gold-to-gold bonds was made many times with

excellent results. The gold-aluminum (chip pads) bonds were reworked, but the number of times an aluminum pad could be used with a good bond was less than three.

The array package was assembled in a standard 1 inch by 1 inch microelectronic package. This package was attached to an adapter ring for assembly into the micropositioner. A filter board was connected to the rear surface of the adapter ring and wires run through the adapter and filter for connecting the array to the signal processing and power supplies.

Photographs of the 576 detector (6-chip), the 1728 detector (18-chip) and the fully assembled 18-chip array are shown in figures 23, 24, and 25. From an observation of the photographs, it is readily seen that a major objective of the breadboard program was achieved. Thus it is fully demonstrated that the fabrication of long arrays is totally feasible. Achieving this objective was not devoid of problem areas, however. Some of the problem areas encountered during the array fabrication phase are discussed in the following paragraphs.

2.4.3.2 Fabrication Problem Areas

Throughout the fabrication and test phases, both accomplishments were made and problem areas became apparent. Those problems which could readily be resolved were improved with the later 18-chip array fabrication. This section discusses the problem areas and possible solutions.

Many of the early chip failures were similar, occurring after several hours of operation. One of these damaged chips was sent to NASA-GSFC for failure analysis (see Appendix C, Failure Report SN-2979). The conclusion was that the chip had a probable electrical overstress although some manufacturing scrapes could have been contributing factors.

Later in the program, there was a long period during which no failures occurred until some electrical modifications were performed. The coincidence of electrical circuit modifications and the occurrence of array failure may have been due to the use of an ungrounded soldering iron. The extremely

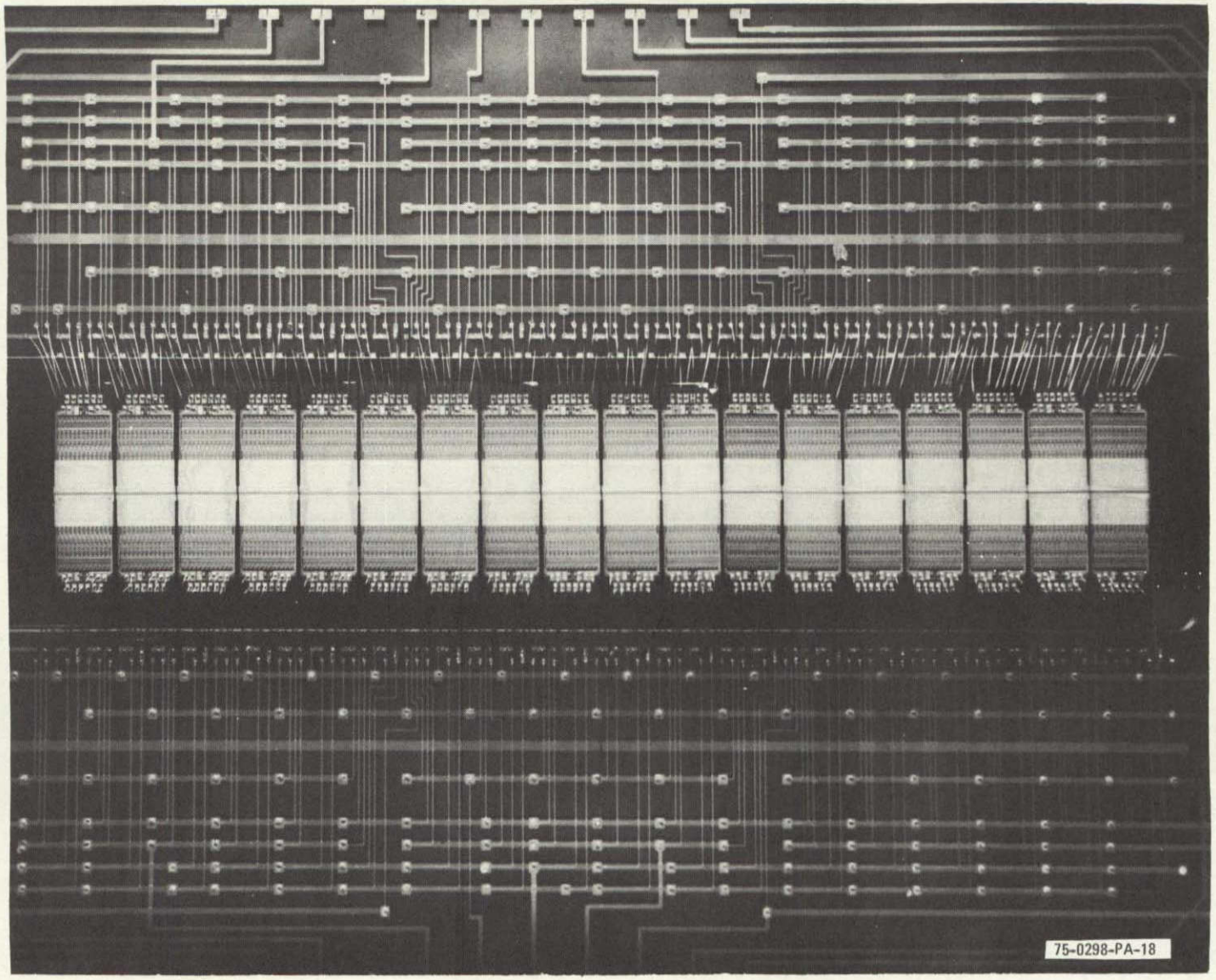


Figure 24. 18-Chip Array (1728 Detectors)

Figure 25. Fully Assembled 1728-Detector Focal Plane Array

high impedance of the MOSFET devices make them very susceptible to static charge damage. For the 18-chip assembly, special care was used to do all wiring with a grounded soldering iron thus preventing failure due to static charge effects. Also, the power lines are decoupled with large capacitors, zener diodes, and resistors to remove the possibility of power line transient damage to the array. The data buses were decoupled by the first amplifier resistances and the MOSFET gates are protected on the chips with zener diodes. No failure occurred during an operating period of many months with the 18-chip array, indicating that the electrical induced problems were resolved.

Probably the most critical problem area is the chip sensitivity to handling. The chip is very brittle, making the chips very susceptible to nicks and cracks from pressure or edge contact. Pressure on the front surface can cause breakdown of the thin dielectric between conductors. These are the most probable causes of the majority of chip failures seen during the array fabrication. Many of the visible damage problems are caused during the array assembly and alignment. The cause of problems during this phase is the awkwardness of handling the small chips while performing the required assembly procedure. Particularly during alignment and tightening, it is necessary to manipulate the chips which are now mounted to their carriers while viewing the procedure through a microscope. The microscope objective depth of field is so limited that it allows only one surface to be visible. Beyond the focal plane, small spurs or debris on the chip edges can come in contact with an adjacent chip causing a piece to be broken off. It must be remembered that the chip-to-chip nominal spacing between edges is 7.6 μm (0.3 mil). In addition, the staggered geometry has interlocking edges which also interfere with the alignment (see figure 26). As the chip carrier screws are tightened, these edges can be overlapped (confused by the out-of-focus condition) and the chip broken or cracked.

The 6-chip array carriers were mounted to the top surface of the baseplate, with the sapphire substrate sandwiching the chip carriers between it

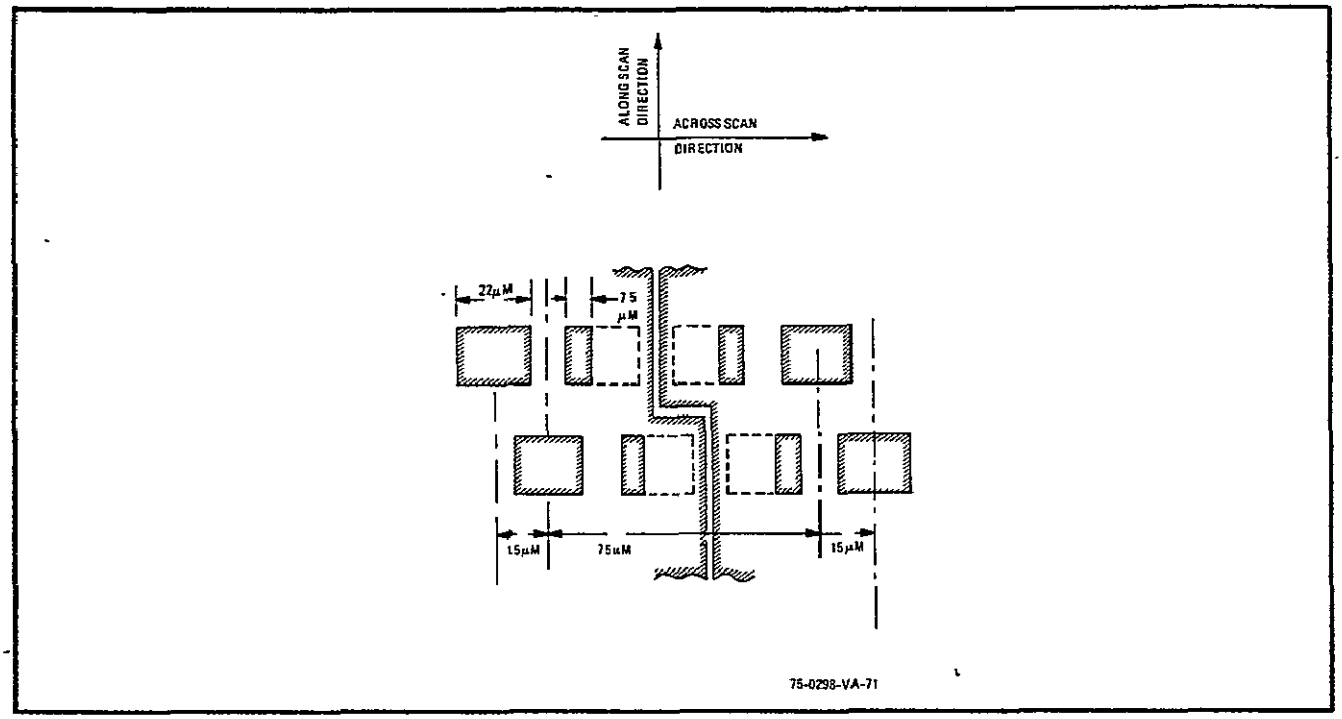


Figure 26. Bilinear Design (Detector and Edge Element Geometry)

and the baseplate. This technique provided the chip replaceability but required removal of all chip wirebonds for a single chip change. Because of the gold-to-aluminum bonds on the chips, a maximum of three reworks were possible, but each rework had a good possibility of completely destroying a good chip bonding pad so that it also had to be replaced. This was an obvious limitation to the fabrication technique requiring improvement.

A modification to the mounting technique was incorporated into the 18-chip array. The chip carriers were modified to allow mounting to the bottom of the baseplate. This technique allows removal of individual chips without disturbing other chips of the array. Several chips were replaced in this array showing the great advantage of this technique.

A more subtle problem, because of the lack of visible damage, is the dielectric breakthrough. This can be caused by any front surface contact with even relatively small amounts of pressure. Most of the 18-chip failures, not attributed to nicks and cracks during the assembly phase, have been traced to front surface contact (see the Failure Analysis Report in Appendix D).

A basic requirement of the breadboard program is to develop a totally contiguous array of photodetectors, i.e., no gaps between end-element detectors. The use of bilinear staggered detector geometry shown in figure 22 meets this requirement. But, as was stated in a previous paragraph, the physical interlocking of the chip edges is an extremely tedious, but feasible, mechanical assembly operation.

2.4.4 Computer Processing

The photodiode linear array detectors exhibit differences in signal offset and gain. Data from the program has shown that on a per bus basis, a majority ($\approx$ 80 percent) of the elements vary from each other by less than 15 percent of full scale. There is a finite number of elements with much larger offsets. Dynamic range and gain variations are relatively closely matched for all working elements. From this, it is seen that radiometric correction is the prime driving function in computer processing.

These characteristics (signal offset and gain) obscure the real information content of the raw data and therefore require removal prior to data evaluation. With the discrete element configuration, the linear array is ideally suited for computer processing of its data. The computer, therefore, was an important tool used during the breadboard linear array test phase.

The computer has two primary functions in this program: reordering of the staggered geometry and normalizing the data. During the data manipulation, other capabilities of the computer were also used for image cosmetics and data analysis. Although the listing (Appendix E) is lengthy, the actual function is not complex as can be seen in the simplified flow diagram of figure 27. The following paragraphs provide a more informative description of the computer functions.

Initially the data tape was formatted for 6-chip data. Rather than modify the hardware, when the 18-chip array was fabricated, the same 6-chip format was used. To process the data from the 18-chip array, three runs were made with each of three 6-chip segments. The software was modified to read

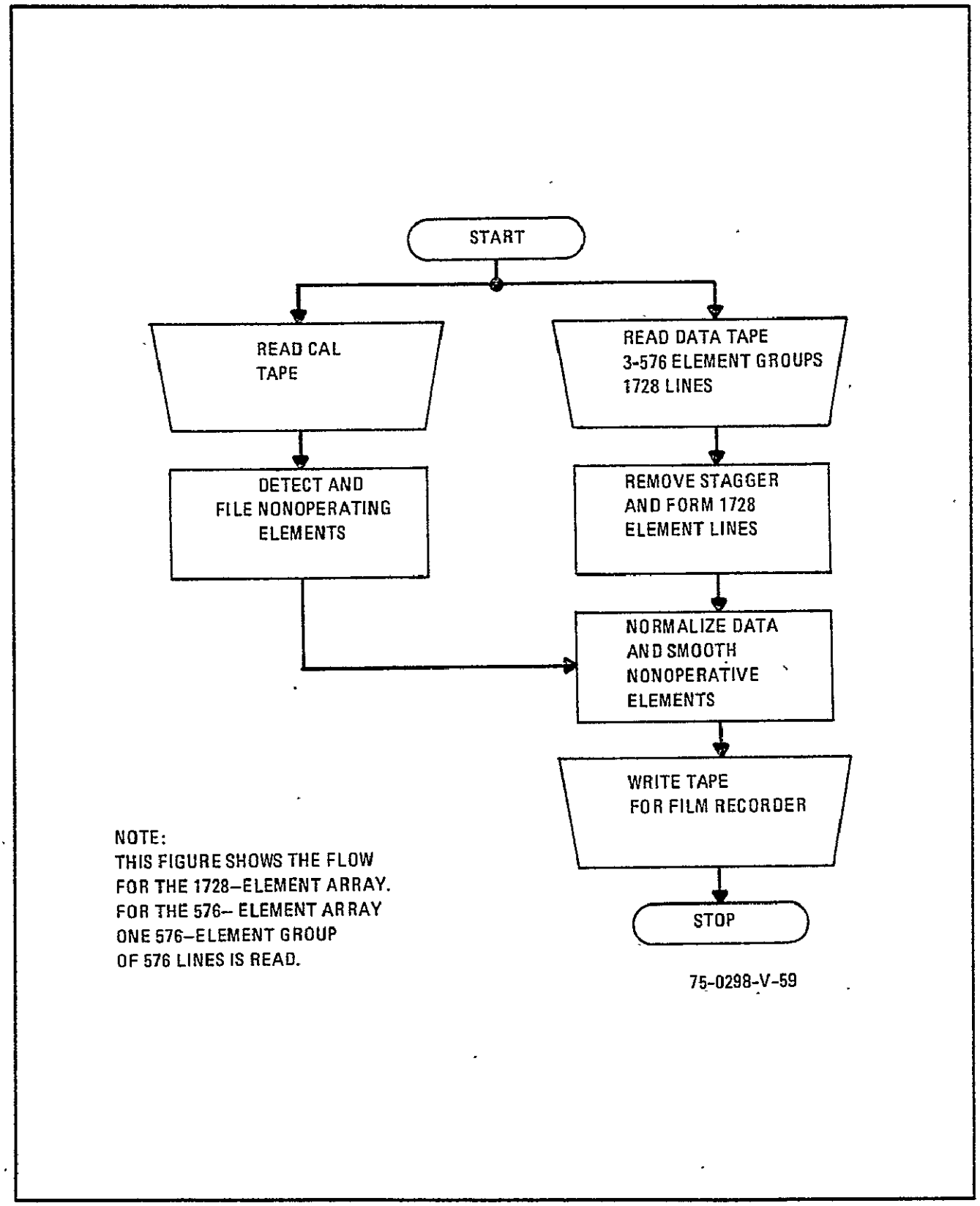


Figure 27. Simplified Flow Diagram

1728 lines of 576 elements each and then repeat the 6-chip process for each segment. The simple tape (calibration and scene data) format for the 6-chip array was changed to a two tape (one for calibration and one for scene data) format to handle the increased data requirement of the 18-chip array. The Appendix E program listing and the flow chart is for the 18-chip format.

The first information entered into the computer is the calibration data. These are array outputs for each element at five predetermined radiance levels. Five hundred seventy-six (576) samples are run for each element at each level. The computer averages these samples and stores the results for use in normalizing the picture data. While reading the tape data, the computer also smooths inoperative elements by averaging between the two adjacent elements to compensate for the missing data.

The next step is for the computer to read and store the image data. During the reading of this data, the inoperative elements are also removed by adjacent element averaging. Two 576 element data lines are read into the computer per tape access. The even numbered elements are stored for one tape access interval and then placed into the storage array with the data from the odd numbered elements read during the next interval forming a 576 element line. This removes the two pixel displacement (across scan) inherent in the staggered photodiode array. The elemental data values are compared to the calibration data and, by interpolation between the nearest higher and lower calibration values, normalized to a range of 0 to 255. One thousand, seven hundred twenty eight (1, 728) lines of normalized data from each 6-chip section are accumulated in a drum storage area until the scene data from all three sections have been read.

The final step of a scene data process is to retrieve the data from the drum, taking a line from each 6-chip section, to form a single 1728 element data line. Values equivalent to each of the five calibration levels are added to the data lines (one level for each of 376 lines). This data is recorded on a magnetic tape for playback on a film recorder.

Another benefit obtained from the computer usage was the obtaining of noise calculations. The same scene software was used except the scene processing was removed and an rms routine inserted. The rms deviation from the average level was calculated using 557 samples. This rms value was normalized to the 0 to 255 range for easy comparison to the signal levels. An rms value was then printed for each of the 1728 elements.

The computer was also used to obtain a comparison of temperature data. This was a simple plotting routine using the peripheral plotter. Room temperature and 0° C plots were made of the dark level for the 6-chip array. The effects of temperature become readily apparent with the plotted data as shown in Appendix F.

2.5 TEST PROGRAM

A comprehensive test program was performed on the Breadboard Linear Array Imager. Prior to performing the test program, a test plan, entitled Test Plan for Breadboard Linear Array Imager, Specification No. 21806-1, was prepared. This plan enumerated performance parameters to be evaluated.

2.5.1 Test Results

Test results are discussed in the following paragraphs. Each significant test parameter as identified in the test plan and technical specification is discussed as an individual performance item.

2.5.1.1 Noise

The noise contributors to the breadboard imaging system are from the detector, analog processor, and quantization. The detector noise was from 1.0 to 1.3 $\mu J/m^2$ based on measured manufacturing data in a 0.4 to 0.8-μm bandwidth with a 6000K source. A detector noise (NEI) distribution histogram of a typical 96-element chip is shown in figure 28. The MHP analog processor noise was measured at 0.39 $\mu J/m^2$ and the quantization noise was calculated to be 0.2 $\mu J/m^2$.

The breadboard system radiance band used for the noise measurements is centered at 0.54 μm with an 0.082-μm width with a source of approximately 3000 K. Although the measured manufacturing detector noise spectral

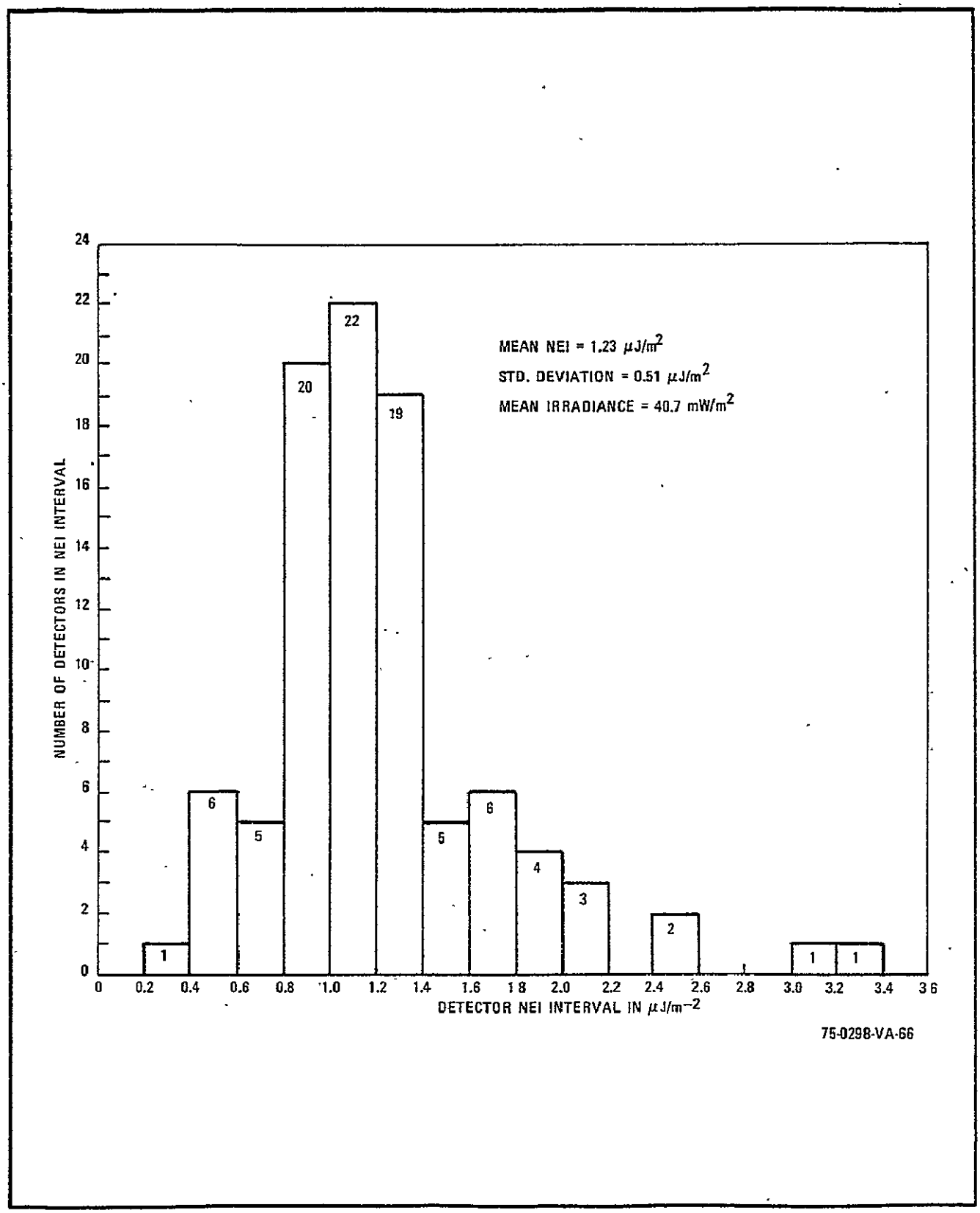


Figure 28. Detector NEI Histogram For A Typical 96-Element Chip

bandwidth is not the same as that of the breadboard, the product of the average detector response and integrated irradiance produces an error of less than 5 percent between the two measurements.

For tests on the breadboard, the two measurements (wide band and 0.5 - 0.6 μm narrow band) are considered to be equivalent. Taking the rms noise of each component of the system, detector, processor, and quantization noise, a total noise is calculated to be between 1.1 and 1.4 $\mu J/m^2$. A typical calculation of system noise (RSS) is:

$$\text{System noise} = \sqrt{(\text{detector noise})^2 + (\text{analog processor noise})^2 + (\text{quantization noise})^2}$$

where

- detector noise = 1.3 $\mu J/m^2$
- analog processor noise = 0.39 $\mu J/m^2$
- quantization noise = 0.2 $\mu J/m^2$

and,

$$\text{System noise} = \sqrt{(1.3)^2 + (0.39)^2 + (0.2)^2}$$

$$\cong 1.4\ \mu J/m^{-2}$$

The noise measurement on the 6-chip array yielded a noise of 1.9 $\mu J/m^2$ (see table 6). To improve this condition, a processor change was made to correct a cross-coupling problem. The 18-chip array noise was then obtained yielding the maximum expected 1.4 $\mu J/m^2$ (see table 7).

The use of the MHP analog processor was expected to result in lower system noise. As seen above, the analog processor contributes less than 10 percent of the total system noise. For example, a 50 percent reduction in the MHP noise results in a reduction of 3 percent in system noise. The replacement of several detector chips in the 18-chip array coupled with the uncertainty in making precision analog measurements have obscured the effects of lower MHP noise. Therefore, the quantitative performance of the MHP has not been established. Actually, the test results of table 8 showed an

TABLE 6

RMS NOISE FOR 576 DETECTOR ARRAY WITH DISCRETE-COMPONENT ANALOG PROCESSORS

6.66	6.72	3.95	4.57	3.06	4.26	4.40	3.98	5.24	5.52	4.07	5.31	3.22	5.03	4.95	3.87
4.98	4.47	3.88	5.18	3.03	4.16	4.55	3.92	5.32	4.55	4.46	4.55	#11.38	3.77	4.57	3.76
4.74	4.23	3.70	3.95	3.30	3.89	4.74	3.78	4.89	4.00	3.51	4.21	3.03	3.32	4.33	4.06
4.79	4.88	3.07	4.23	3.95	4.19	4.87	4.70	5.33	6.05	3.70	5.87	3.61	5.19	5.51	4.09
5.15	6.16	3.54	6.03	3.23	4.93	5.00	3.72	5.33	6.00	3.34	5.83	3.26	4.51	4.55	4.14
5.15	6.05	3.48	6.07	3.17	5.51	5.14	4.26	2.79	5.49	4.03	5.63	4.56	5.47	6.45	5.33
-21.30	5.81	-11.38	4.33	5.14	4.24	4.39	4.29	5.61	4.37	4.27	4.96	4.27	5.74	4.78	4.27
4.53	4.21	3.80	4.75	3.99	4.17	4.85	4.35	4.63	4.10	3.69	5.03	3.93	4.42	4.26	4.20
4.53	3.88	3.44	4.49	4.04	4.85	4.82	4.61	4.83	3.99	3.48	4.80	3.72	4.61	4.54	4.05
4.52	4.17	3.75	5.18	3.54	4.78	4.62	4.39	4.98	4.20	3.51	4.86	3.70	4.78	4.71	4.11
5.00	4.40	3.91	5.13	4.19	5.03	4.52	4.47	4.91	4.41	3.99	5.04	10.90	4.94	4.61	4.34
4.43	3.88	3.94	3.95	3.94	5.21	4.76	4.03	5.06	4.40	4.30	5.44	3.87	5.52	7.50	6.15
6.11	5.81	4.37	5.29	4.22	4.47	5.09	4.81	5.37	4.31	4.08	4.57	4.22	4.62	5.03	4.62
5.57	4.36	4.16	4.97	4.92	4.68	5.58	4.73	5.04	4.42	4.16	5.09	5.02	5.31	5.17	4.84
5.34	4.56	4.32	5.29	3.91	4.68	4.67	4.25	4.89	4.18	4.11	4.44	4.10	4.71	4.67	3.97
5.15	4.36	4.08	4.83	4.03	4.76	5.01	4.21	5.17	4.26	4.34	4.94	4.27	4.61	5.08	4.38
4.98	4.20	4.27	4.27	4.21	4.33	4.96	4.43	5.05	4.28	4.28	4.79	4.40	4.58	4.91	4.43
4.92	4.47	4.18	4.42	3.91	4.50	4.75	4.65	5.19	4.34	4.31	5.49	4.38	6.19	7.48	-255.23
5.75	5.46	3.43	3.76	2.93	3.74	4.43	3.79	4.15	3.50	3.47	4.00	3.12	3.88	4.41	3.77
4.65	4.73	3.66	4.63	2.96	4.17	4.33	3.80	4.48	5.21	3.80	4.55	2.99	3.83	4.49	3.66
4.27	5.07	3.21	4.44	2.76	3.52	4.32	3.44	4.25	4.15	3.34	4.14	2.75	3.47	4.10	3.52
4.06	3.61	3.33	3.34	2.77	3.43	4.11	3.66	4.47	4.52	3.35	4.19	2.98	4.50	4.59	3.53
4.59	5.22	3.24	5.00	3.10	4.10	4.62	3.93	4.93	6.18	3.32	5.72	3.04	4.64	4.80	3.79
4.31	3.95	3.54	4.58	3.00	4.06	4.91	3.83	5.04	13.24	3.49	-9.28	4.62	-9.28	6.82	-6.87
4.54	4.10	3.20	1.57	3.05	3.44	4.18	4.26	4.86	3.72	3.83	3.89	3.61	5.54	5.52	4.58
4.88	4.25	3.54	5.27	3.19	4.94	4.37	6.70	5.06	3.94	3.64	5.37	3.01	3.88	4.26	3.69
4.25	3.67	3.65	3.94	3.03	3.40	4.15	3.49	4.33	3.77	3.46	3.98	3.00	3.53	4.15	3.42
4.41	4.19	3.38	4.12	3.01	3.45	4.21	3.55	4.65	4.10	3.66	4.43	3.21	3.56	4.30	3.57
4.81	4.07	3.78	4.09	3.32	3.94	4.67	3.47	4.49	3.82	3.42	4.20	3.14	3.55	4.49	3.58
4.74	3.98	3.95	4.15	3.00	3.57	4.04	3.51	4.93	3.93	3.88	4.51	3.49	3.66	6.33	4.56
6.05	5.75	2.78	3.70	2.96	4.23	4.06	6.11	4.43	6.36	3.25	4.96	2.70	3.83	4.42	3.51
4.45	3.70	2.78	3.70	2.88	3.65	4.29	3.30	4.30	3.50	2.56	3.49	2.89	3.28	3.99	3.27
4.27	3.50	2.67	3.51	2.98	4.20	5.00	3.45	4.39	4.04	2.51	3.60	2.63	4.82	5.53	3.63
4.47	4.79	2.96	4.03	2.87	3.83	4.45	3.67	4.31	3.70	3.17	4.14	2.77	3.71	4.25	3.61
4.42	3.81	2.92	3.90	2.85	3.37	4.05	3.27	4.53	3.43	2.80	3.80	3.06	3.41	4.31	3.33
4.39	3.63	2.91	3.59	2.84	3.60	4.37	3.40	4.57	3.74	4.24	5.15	6.86	10.37	22.26	31.20

THIS IS THE COMPUTER PRINTOUT OF RMS NOISE (0.5-0.6 μm BAND) FOR 576 DETECTORS IN THE 6-CHIP ARRAY USING DISCRETE-COMPONENT ANALOG PROCESSORS. THE NOISE IN THE TABLE IS IN DIGITAL COUNTS WHERE ONE COUNT IS .45 $\mu J/m^2$. THE AVERAGE OF THE RMS NOISE VALUES IS 1.9 $\mu J/m^2$ WHICH INCLUDES 90 PERCENT LENS TRANSMISSION EFFICIENCY. INOPERATIVE DETECTORS ARE EXCLUDED.

75-0298-T-3

TABLE 7

RMS NOISE FOR THE 1728 DETECTOR ARRAY WITH DISCRETE COMPONENT ANALOG PROCESSORS

9.02	8.65	5.21	5.86	4.90	5.99	5.42	4.77	5.52	5.69	5.23	4.99	5.88	6.55	5.88	6.08
6.07	5.36	5.39	4.72	5.46	6.57	5.71	6.47	5.32	5.27	4.99	4.67	5.44	6.01	5.33	6.42
5.31	4.92	4.88	4.71	4.87	5.43	4.95	5.53	5.45	5.29	5.03	4.74	5.03	5.39	4.90	5.06
5.14	5.40	5.25	4.63	4.85	5.54	4.57	4.76	5.72	5.05	5.30	4.58	5.07	5.60	5.25	5.38
5.67	5.10	5.23	4.60	6.83	6.46	4.86	6.44	5.39	5.15	5.06	4.45	4.71	5.55	4.89	5.22
5.12	4.92	4.81	4.25	5.20	5.16	4.74	5.16	4.97	4.85	4.97	4.69	7.01	6.76	4.63	5.27
-17.09	7.18	-513.06	5.68	-82.19	6.17	-485.91	4.95	4.93	4.95	4.37	5.35	5.75	5.93	5.17	5.33
5.37	4.93	5.18	4.93	5.90	5.73	4.97	5.09	-10.95	5.04	5.33	4.81	5.66	5.57	5.00	4.88
4.83	4.93	5.47	4.94	22.04	5.59	4.44	4.45	5.42	4.85	5.46	4.91	4.57	5.53	4.45	4.32
5.02	-8.33	5.12	4.39	5.55	6.22	4.91	4.30	5.29	4.96	5.19	4.97	5.22	5.79	5.12	4.73
4.96	5.01	5.06	4.49	5.38	6.03	4.51	4.88	4.83	5.18	5.24	4.83	5.53	5.95	5.02	4.87
5.16	5.16	5.46	5.34	5.02	5.84	4.63	4.93	4.97	5.08	5.08	4.75	7.42	8.00	5.05	4.65
-.66	.00	-67.05	5.21	5.05	6.39	4.64	4.81	5.21	5.33	4.95	4.69	5.06	6.32	4.96	6.26
5.22	5.49	5.11	4.83	5.29	6.03	5.10	6.08	5.44	5.60	5.29	4.71	5.02	5.88	5.02	5.65
5.48	5.46	5.12	5.03	5.29	6.47	5.01	6.37	5.31	5.02	4.86	4.84	5.31	6.91	4.93	6.72
5.38	5.28	5.13	4.95	5.54	6.06	5.35	6.11	5.52	5.40	4.98	4.58	5.52	6.43	4.93	4.96
5.00	5.37	5.10	5.34	5.28	5.89	4.87	5.49	5.47	5.56	4.74	4.66	5.50	5.97	5.00	5.53
5.24	5.41	4.96	4.69	5.08	5.78	5.00	5.85	5.31	7.34	5.02	4.98	6.01	7.72	4.88	5.69
-9.38	7.82	4.70	5.08	5.51	6.15	5.88	5.33	5.94	5.51	5.48	5.76	5.66	6.63	5.96	5.92
5.64	5.68	5.60	5.67	6.07	6.57	5.42	6.30	5.96	5.49	5.46	5.31	5.32	6.46	5.82	5.83
5.42	5.45	5.19	5.27	6.29	6.54	5.60	6.03	5.58	5.56	5.30	5.07	5.83	6.81	6.01	6.18
5.96	5.41	5.98	5.48	5.78	6.65	5.74	6.45	5.58	5.48	5.34	5.17	6.19	6.63	5.82	6.32
5.82	5.54	5.76	5.51	5.57	6.20	5.40	5.62	5.73	5.69	5.39	4.91	5.78	6.68	5.65	5.91
5.80	5.20	5.25	4.78	5.90	6.67	5.72	5.95	5.57	5.25	5.66	5.11	7.83	.00	5.89	5.61

THIS IS THE COMPUTER PRINTOUT OF RMS NOISE (0.5–0.6 μmBAND) FOR 1728 DETECTORS IN THE 18–CHIP ARRAY USING DISCRETE–COMPONENT ANALOG PROCESSORS. THE NOISE IN THE TABLE IS IN DIGITAL COUNTS WHERE ONE COUNT IS 0.28 $\mu J/m^2$. THE AVERAGE OF THE RMS NOISE VALUES IS 1.4 $\mu J/m^2$ WHICH INCLUDES 90 PERCENT LENS TRANSMISSION. INOPERATIVE DETECTORS ARE EXCLUDED.

75-0298-T-4

TABLE 8

RMS NOISE FOR THE 1728 DETECTOR ARRAY WITH MHP ANALOG PROCESSORS

5.19	2.09	1.73	1.12	2.01	1.03	1.78	1.34	1.47	1.34	1.05	1.43	2.03	1.61	2.12	1.47
1.84	1.52	1.85	1.82	1.05	1.29	1.52	1.32	1.47	1.27	.91	1.27	.99	1.21	1.71	1.26
1.58	1.30	1.32	1.41	.91	1.15	1.61	1.19	1.48	1.22	1.14	1.31	1.16	1.27	1.60	1.20
1.44	1.27	1.42	1.50	.98	1.17	1.43	1.23	1.41	1.30	1.41	1.32	.81	1.17	1.49	1.23
1.48	1.44	1.61	1.71	1.01	1.37	1.69	1.46	1.36	1.20	.99	1.36	.78	1.14	1.51	1.27
1.37	1.11	.95	1.35	1.03	1.34	1.62	1.73	1.39	1.37	1.33	1.41	.87	1.25	2.43	1.61
.00	2.36	27.07	2.05	1.00	1.05	.98	1.03	1.40	1.35	.00	1.30	17.62	1.57	12.27	1.59
1.40	1.77	1.92	1.61	1.92	1.48	1.76	1.54	1.46	1.59	1.71	1.42	1.27	1.23	1.38	1.35
1.66	1.30	1.41	1.53	1.33	1.38	1.54	1.46	1.50	1.25	1.49	1.36	1.21	1.46	1.44	1.31
1.70	1.50	.31	1.77	2.20	1.43	1.79	1.27	1.86	1.59	1.89	1.71	.00	1.21	1.31	1.15
1.57	1.17	2.84	1.56	2.08	1.53	1.45	1.12	1.76	1.28	1.35	1.42	1.25	1.46	1.66	1.27
1.48	1.42	1.22	1.63	.88	1.28	1.45	1.11	1.54	1.44	1.43	1.58	1.30	1.40	2.21	1.46
.00	.00	.00	1.49	.76	.79	1.25	1.09	1.34	1.63	1.15	1.43	1.01	1.49	1.85	1.29
1.34	1.68	1.09	1.58	1.34	1.38	1.99	1.38	1.70	1.74	1.33	1.67	1.61	1.36	1.84	1.44
2.15	2.03	2.53	1.94	.00	1.31	1.00	1.27	2.02	1.16	2.46	1.49	1.84	1.68	2.01	1.62
1.49	1.57	1.03	1.56	.87	1.22	1.41	1.14	1.68	1.61	1.25	1.75	1.42	1.67	1.95	1.45
1.58	1.46	1.30	1.65	.70	1.20	1.42	1.17	1.67	1.46	1.07	1.87	1.05	1.27	1.44	1.22
1.50	1.48	.95	1.56	.87	1.13	1.49	1.24	1.55	2.24	1.56	1.79	1.10	1.17	2.05	1.46
.00	2.16	1.54	1.57	1.06	1.63	1.69	1.85	1.54	1.44	1.35	1.75	1.16	1.97	2.10	1.92
2.56	2.09	1.81	1.71	1.23	1.96	2.14	1.80	2.88	2.17	1.96	1.68	1.36	1.87	2.39	2.06
2.76	2.07	1.81	1.71	1.37	1.97	2.29	1.92	2.63	1.86	1.61	1.59	1.08	1.85	2.13	1.83
2.74	1.73	2.00	1.72	1.13	1.99	2.39	1.93	2.80	1.88	1.54	1.55	1.31	2.13	2.41	1.93
2.77	1.92	1.68	1.71	1.51	2.14	2.14	1.81	2.92	2.21	2.10	1.74	1.09	1.94	2.24	1.78
2.73	2.01	1.53	1.62	1.13	2.04	2.21	1.84	2.83	2.13	1.69	1.69	.96	1.27	3.31	.00
10.20	3.31	2.45	2.10	1.05	1.83	1.70	2.20	2.53	1.94	2.81	1.61	1.94	2.45	1.96	2.24
1.90	1.80	2.39	1.58	1.81	2.24	1.88	2.04	1.62	1.58	1.96	1.38	1.80	2.20	1.94	1.83
1.72	1.66	2.11	1.56	1.61	2.07	1.70	1.89	1.87	1.58	2.04	1.54	1.86	2.29	1.73	1.97
1.91	1.58	2.14	1.46	1.83	2.15	1.84	1.81	1.93	1.67	2.11	1.55	1.96	2.09	1.71	1.78
1.90	1.70	2.03	1.53	2.01	2.39	2.31	2.54	1.80	1.73	2.05	1.62	1.91	2.46	1.80	2.26
2.18	1.76	2.27	1.64	1.90	2.22	1.83	2.04	1.95	1.83	2.23	1.63	1.22	.00	3.46	.00
.00	.00	1.80	1.61	1.00	.74	1.51	1.36	1.63	2.10	1.43	1.83	2.39	1.72	2.47	1.81
2.46	1.93	1.82	1.90	1.12	1.51	1.74	1.35	2.27	2.18	2.20	1.90	.93	1.15	1.42	1.20
1.60	1.62	1.19	1.69	1.10	1.44	1.62	1.45	1.57	1.65	1.00	1.64	1.06	26.64	2.13	1.34
2.22	.87	1.51	.96	1.24	1.02	.00	1.29	1.67	1.46	.73	1.35	1.23	1.62	1.39	1.51
1.69	1.64	1.30	1.70	1.83	2.03	1.60	1.50	1.52	1.81	1.22	1.79	1.93	1.69	1.94	1.49
1.93	1.70	2.03	1.62	1.02	1.26	1.57	1.36	1.84	1.79	1.81	1.72	2.06	2.44	3.45	.00

THIS IS THE COMPUTER PRINTOUT OF RMS NOISE (0.5–0.6 μmBAND) FOR 1728 DETECTORS IN THE 18–CHIP ARRAY USING MHP ANALOG PROCESSORS. THE NOISE IN THE TABLE IS IN $\mu J/m^2$. THE AVERAGE OF THE RMS NOISE USING THE MHP ANALOG PROCESSOR IS 1.5 $\mu J/m^2$. INOPERATIVE DETECTORS ARE EXCLUDED.

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increase of 0.1 $\mu J/m^2$ up to 1.5 $\mu J/m^2$. It is concluded that this increase is not due to the MHP but to the use of replacement detectors with higher NEI.

Figure 29 is a histogram showing the system NEI distribution of approximately 576 detectors. The noise is plotted in terms of $\mu J/m^2$ in the 0.5 to 0.6 μm band.

In summary, noise equivalent irradiance (NEI) of 1.4 $\mu J/m^2$ has been achieved. With this NEI, signal-to-noise in excess of 200 is obtained from typical ERTS scenes, i.e., scene radiance of 10 W/m^2 - sr in the 0.5 - 0.6 μm band with an f/4.7 optical system.

At the specified radiance of 1.2 W/m^2 - sr (0.5 - 0.6 μm band), and with the f/4.7 lens setting and an NEI of 1.4 $\mu J/m^2$, a SNR in excess of 40 is achieved. The SNR of 40 significantly exceeds the program goal of 22.

For the specified condition using a target with a radiance ratio of 2:1 at the limiting frequency and an NEI of 1.4 $\mu J/m^2$, the low contrast SNR is calculated to be 4. This exceeds the program goal of 2 for the same conditions.

2.5.1.2 Linearity

Linearity measurements were made by making three independent runs with different irradiance levels. The upper level of each lower range was adjusted to be close to the low-level of the adjacent higher range and one amplifier gain change was made. Irradiance attenuation was produced by adjusting the aperture within a range and using the detector and radiometer between ranges. Since discontinuities are unlikely, errors between ranges were removed to make a smooth transition. The high radiance level outputs were increased by 7 to account for the gain change. Noise was removed by averaging 500 samples of each element. The full dynamic range covered is nominally 700:1.

The data indicated that the vast majority of the elements fall within 2 percent (full scale) of a best fit straight line. Only a few elements deviated from a straight line by not more than 3 percent.

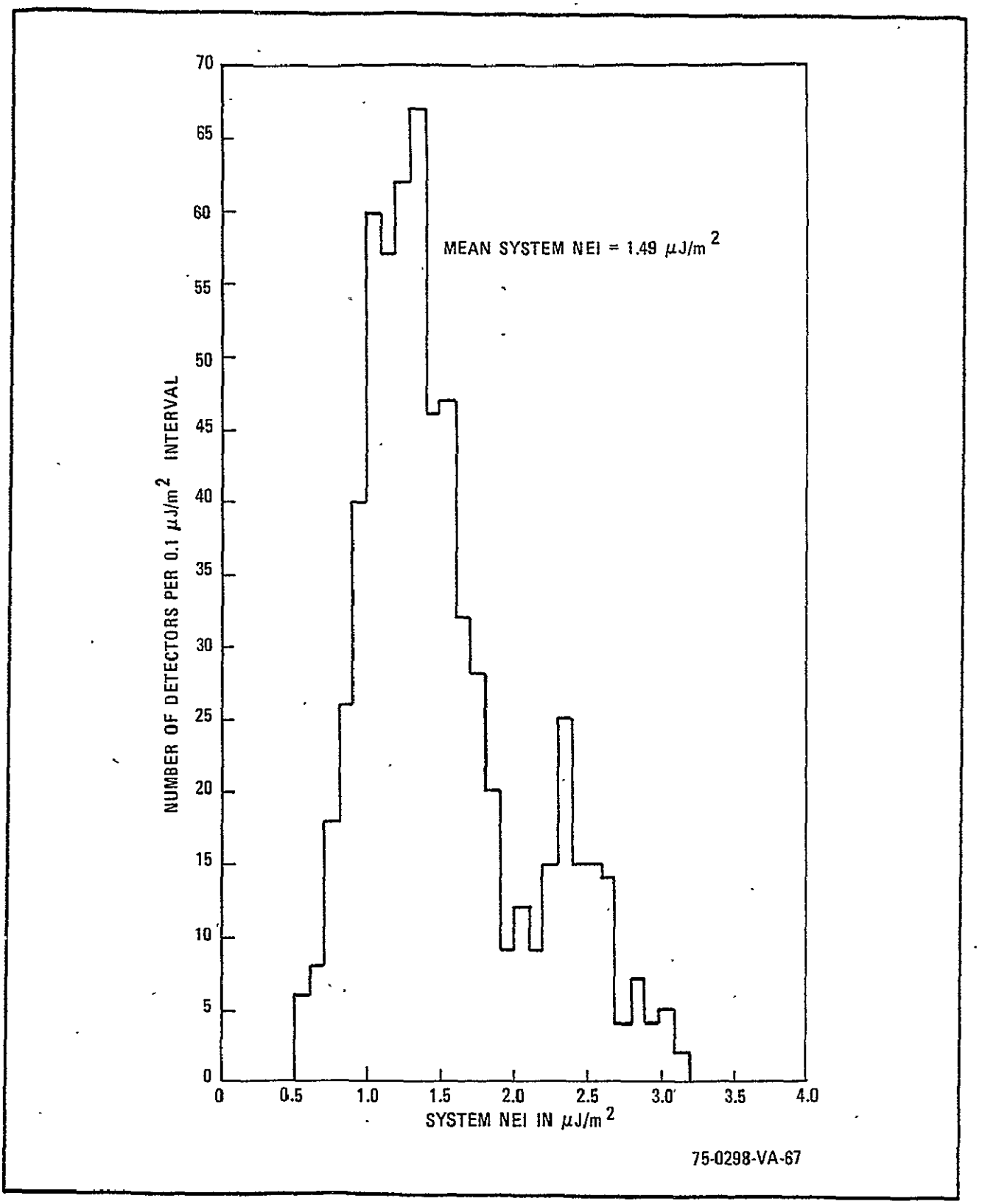


Figure 29. System NEI Histogram for 576 Detectors

Chip manufacturing data (see Appendix H) indicates that a 2 to 3 percent deviation from a straight line can be expected. With careful design, the signal processing electronics will not add further nonlinearity.

2.5.1.3 Modulation Transfer Function (MTF)

The system modulation transfer function (MTF) for the breadboard system consists of the lens MTF, detector window function, image motion, temporal response of electronics, phase of image, and a Fourier coefficient factor for the squarewave targets used in the measurements. For the breadboard, a stationary scene is used and, therefore, image motion is not a factor. The electrical bandwidth (800 kHz) of signal processing electronics is very much greater than the array output frequency for a target period equal or less than the pixel spacing (0.6 mil), and therefore there is no temporal component. Phasing has also been removed by adjusting for maximum and minimum outputs. The detector window MTF component is rectangular, having a sine (X)/X transfer function. The argument X is π times (detector window dimension) times (target spatial frequency). The lens factor was taken from Smith[4] with aberration indicated from the lens measured data.

The specification requires that the system MTF in the along-scan and across-scan direction to be approximately equal. Tests were performed to determine the extent to which this requirement was met. The experimental MTF in the across-scan and along-scan directions for the 6-chip and 18-chip arrays are shown in figures 30 and 31. It is seen from the figures that the MTF's are nearly the same. The effect of optics MTF can be clearly seen by observing the ideal detector response curve.

It is concluded from this experimental data that the specification of equal MTF in the along-scan and across-scan directions has been met.

[4] Smith, Warren J., page 322.

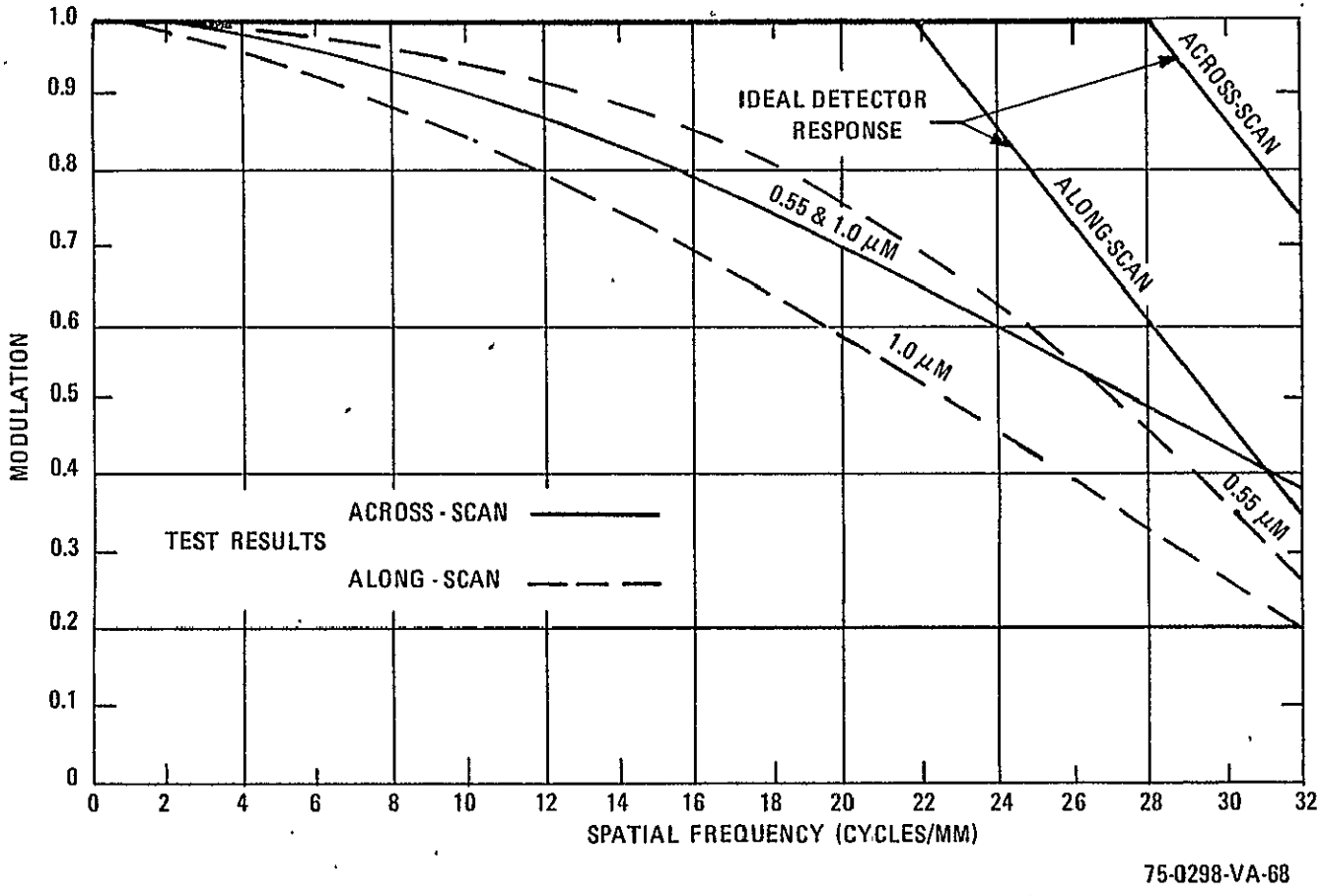


Figure 30. Squarewave MTF With Optics For 6-Chip Array

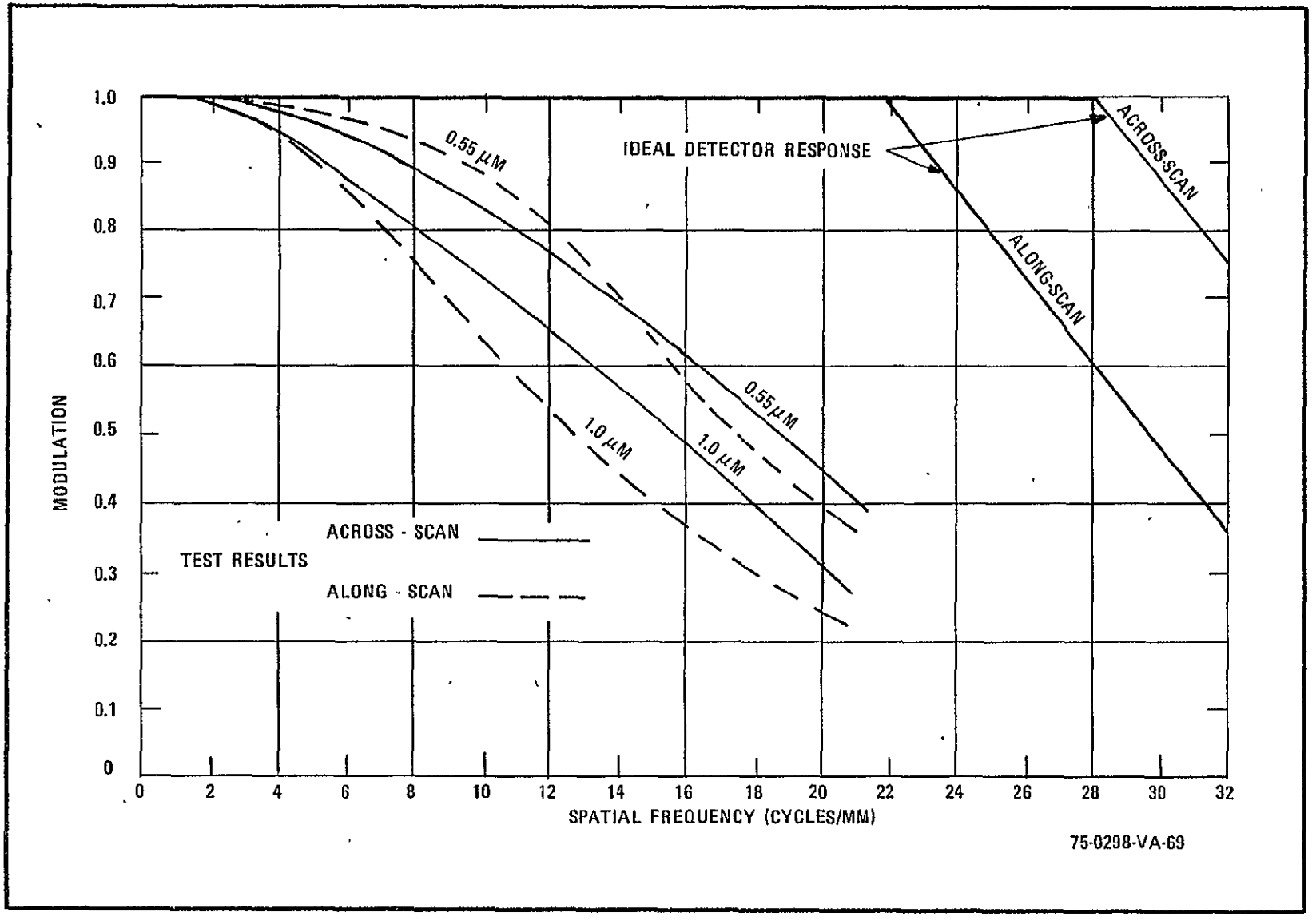


Figure31 . Squarewave MTF With Optics For 18-Chip Array

2.5.1.4 Dynamic Range

A performance goal of the breadboard is to demonstrate that the detector array is to have a dynamic range (in terms of input radiant energy relative to NEI) in excess of 600-to-1. Test results indicate that this goal was achieved.

Measurements of dynamic range were complicated by different bandwidths of the HP 8330 radiometer and detector, and the finite maximum energy output of the light source. For these conditions, a special procedure was developed to obtain dynamic range. The dynamic range of the detectors is measured by a procedure starting at low radiance and increasing to saturation. The procedure is to set the reference radiance to 0.7 to 0.8 μm with the use of bandpass spectral filter. This level is measured with an HP 8330 radiometer and the voltage level of a detector element output is also measured. For this test, the source clear aperture is more than 2 orders of magnitude greater than the detector element FOV. The spectral filter is then removed and the irradiance at the detector reduced with neutral density filters and the lens aperture until the original detector voltage is obtained. By removing the neutral density filters and changing the aperture settings the radiant energy to the detector is increased until saturation (no voltage change) is observed at the detector output. The neutral density and aperture changes required to achieve saturation provide a scale factor to be applied to the original radiometer reading.

2.5.1.5 Cross-Talk

Observation of the 6-chip MTF data reveals that cross-talk between adjacent detectors is not a significant factor in system performance. If cross-talk were present, it would be most predominant in the long wavelength (0.8- to 1.1-μm) band due to increased photon penetration at the high wavelength. Tests show the measured data higher, by 14 percent, along-scan, and 40 percent, across-scan, than the calculated value. A further examination of the measurement uncertainties involved show that the lens spectral

characteristics can cause a 25 percent variation in MTF (ΔMTF between $\lambda = 0.8$ and $1.0\,\mu m$). A 10 percent uncertainty in detector aperture dimension produces an 18 percent uncertainty in MTF. System noise is also a contributor by making high spatial frequency MTF measurements less precise. From the measured results and the known uncertainties, it can be seen that the 1 percent or less expected cross-talk is not detectable in the breadboard system.

2.5.1.6 Spectral Response

Spectral response data for the chips used in the 1728 detector (18-chip) array is shown in figure 32. The figure shows the mean spectral response of 96 detectors on one chip of the array and also the range of mean response for all of the chips. From the figure it is seen that the useful band extends from 0.4 μm to greater than 1.0 μm and the spread of mean responses is minimal. At wavelengths less than 0.8 μm, the peak-to-peak deviation is 6 percent, and at wavelengths greater than 0.8 μm, the peak-to-peak deviation is less than 12 percent. It is important to note that these spectral variations are removed in subsequent image processing operations.

2.5.1.7 Temperature

Although temperature testing was not a specific part of the initial program, the knowledge gained during the program indicated that temperature was a critical parameter for future array usage. In order to better understand the thermal effects on the data, a simple temperature test was run.

The array was mounted in a temperature chamber with the processor outside. A light source was placed in the chamber and all ports sealed. Two reference scans were made at 20° C, a dark level and a light level, to obtain a mid-range output. The lamp voltage was measured to allow later repetition of the same light level. The array was again operated at 0° C at both the dark and same light level as set by the lamp voltage. A third dark level was run at 10° C. Each of the runs consisted of 576 samples with the samples averaged to reduce the noise uncertainty. Appendix F includes the listing of the average data for each element.

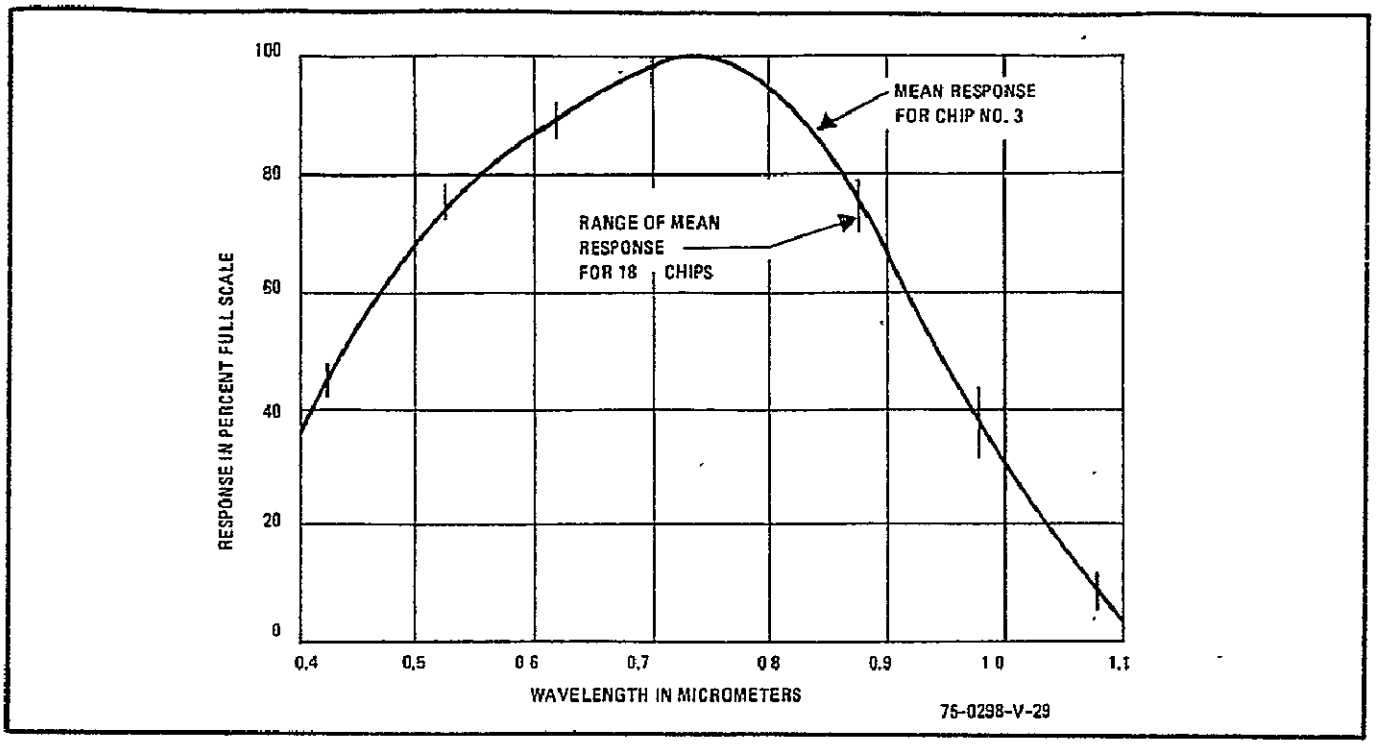


Figure 32. Spectral Response

The average dark level of the data reduces significantly at 0°C. But, of more interest, it was determined that the element to element offsets reduced by a nominal factor of 4 between 20°C and 0°C. This effect reduces the dynamic range required of a system since the offset is a significant portion of the typical signal level. It also reduces the temperature sensitivity of a system by making changes in offset a small fraction of a scene level. A composite plot of the dark level at 0°C and 20°C is given in Appendix F.

Although the temperature test did not provide a rigorous proof of gain variation factors, it did show that the effect is small. A total change of less than 10 percent was indicated over the 20°C temperature range.

2.5.1.8 Inoperative Elements

A goal of this program was to use detectors with no dead elements. With the 30 chips made available for the program, this goal has been nearly met with only one chip of the 576 element array having a dead element and none of the 1728 element array chips having dead elements prior to alignment.

Although the results of the program have shown the feasibility of producing linear array imaging systems, a perfect array was not achieved during the program. The 576 element array was fabricated with 1.2 percent inoperative elements and a 1728 element array with 5.5 percent was fabricated. These failures are attributed to handling and static discharge and a promising means of avoiding the problem in future systems is addressed in the fabrication improvement study discussed in paragraph 2.6.

2.5.2 Image Evaluation

The previous sections have presented the quantitative results of the breadboard linear array test program. This section presents the more subjective results of image evaluation.

2.5.2.1 Gray Scale Reproduction

An important requirement for a remote sensing system is its ability to faithfully reproduce scene gray levels. The results of scanning a non-standard gray scale image show that the linear array technology is capable of meeting that requirement.

The plot of figure 33 shows the results of scanning a multi-level gray scale. Full scale irradiance at the detector (including a 90 percent lens efficiency) is 450 $\mu J/m^2$ providing a typical mission scene range. At 100 percent film transmission, the array output in counts would be 255. The plotted data shows an excellent relative linearity of within 1 percent of full scale for a best fit straight line. It also shows that the array output faithfully reproduces the gray levels within 3.7 percent absolute. Figure 34 is a film reproduction of the gray scale image from the array. The film fidelity is shown by the gray scale at the right, showing maximum irradiance, dark, and three factors of 2 steps.

2.5.2.2 576-Detector Array Imagery

Figure 35 shows four scenes made from the 576-detector array. The IFOV is 0.23 mrad with an irradiance of 0.03 mW/cm^2 in the 0.5 to 0.6 μm band.

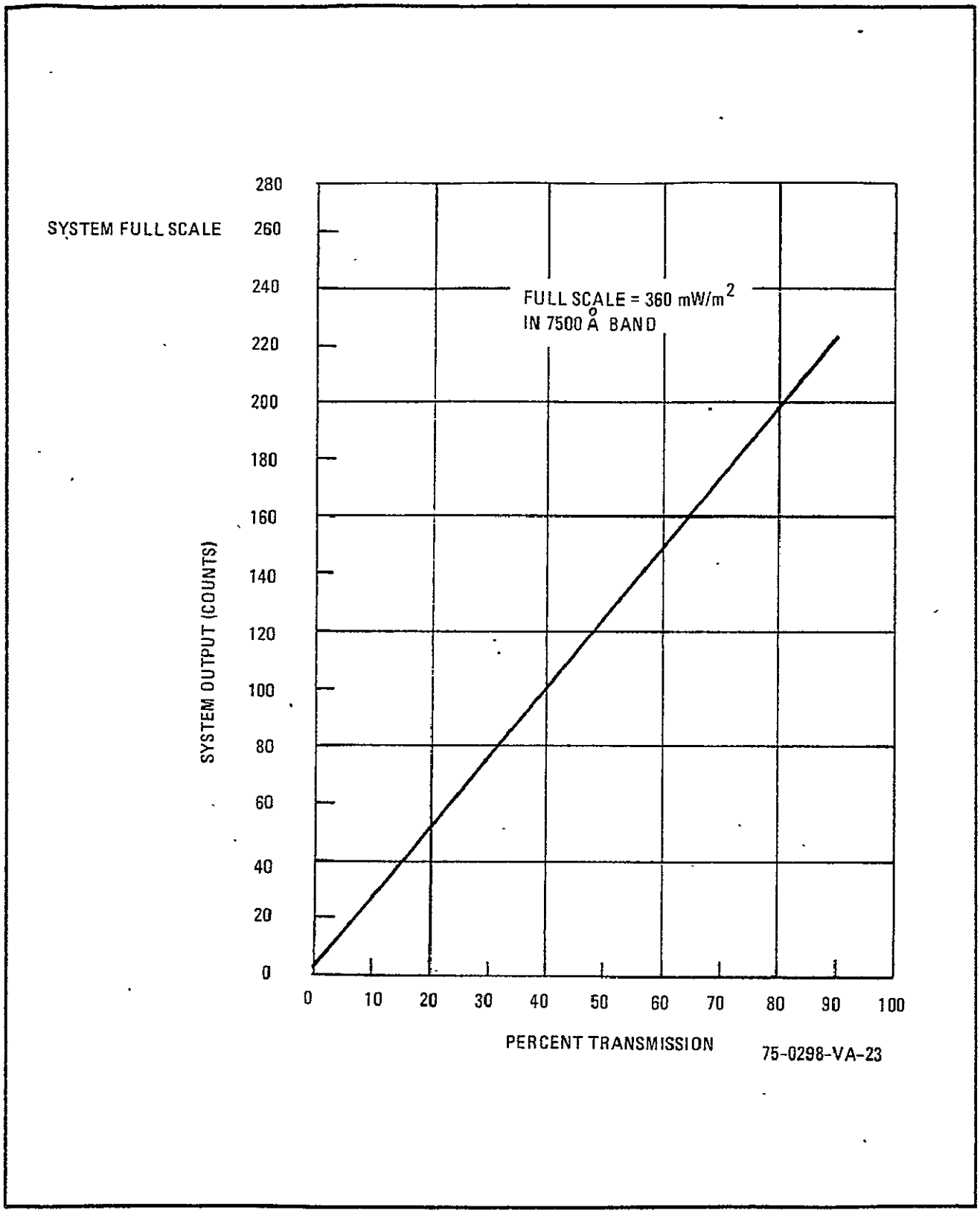
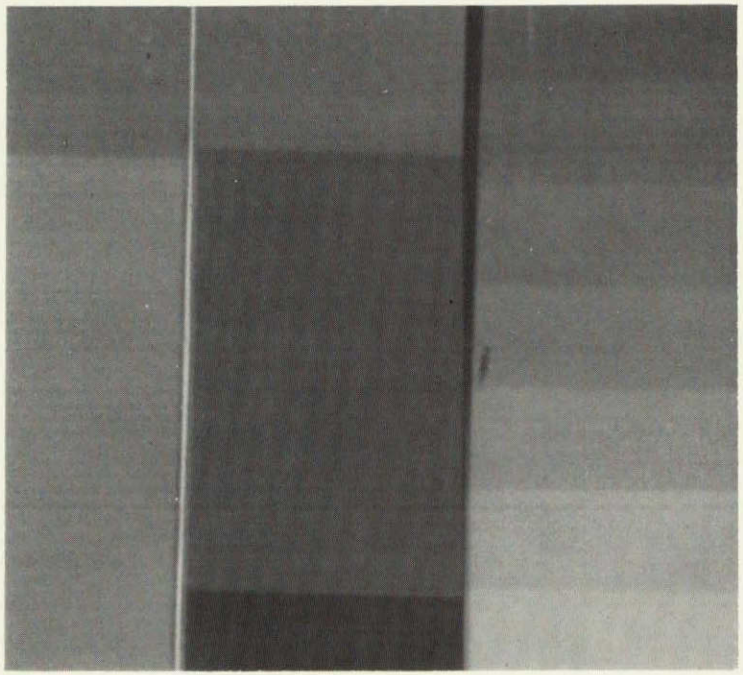
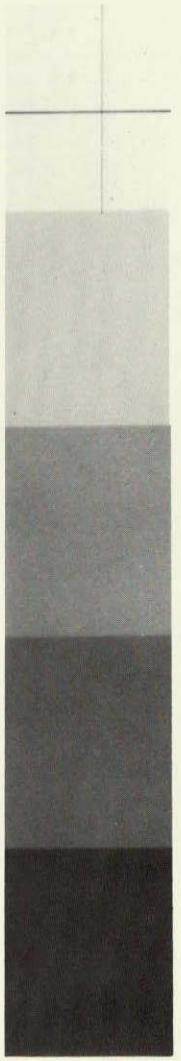


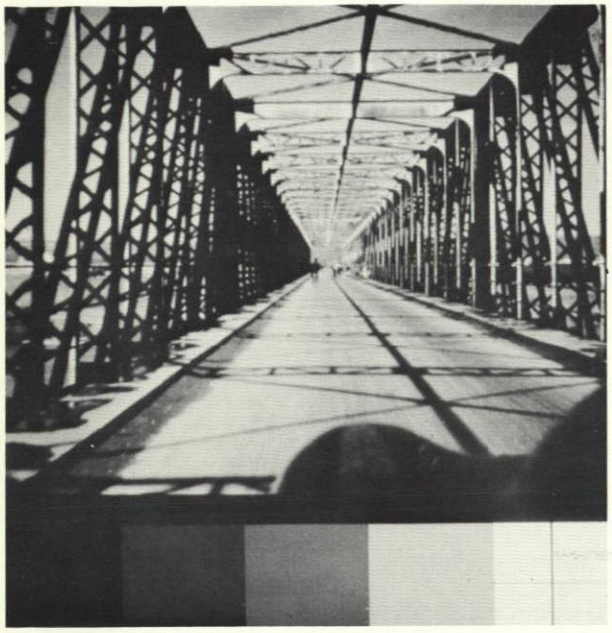
Figure 33. System Output as a Function of Gray Scale Transmission

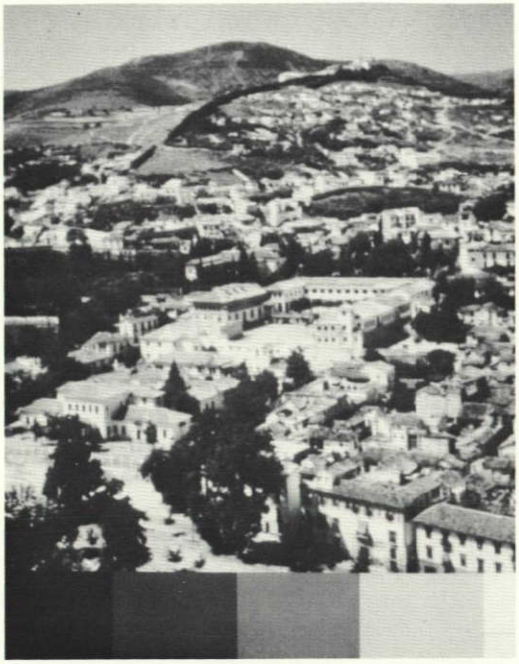




75-0298-PA-70

Figure 34. Gray Scale Image





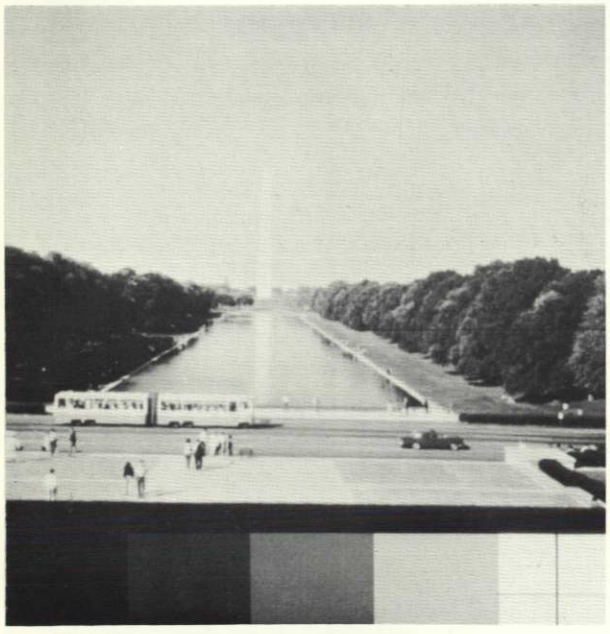


Figure 35. 576-Detector Array Imagery

2.5.2.3 1728-Detector Imagery

Figure 36 is a 1728-detector image produced from the breadboard from an aerial transparency provided by the U.S. Geological Survey. The figure is a contact print made from the exposed film produced from an Optronics P-1500 Photowrite display system. The facsimile recorder has a LED source which is optically focused and modulated to form an image with 64 gray levels and a square illumination spot size of 50 μm.

The image of figure 36 was produced from the 1728-detector, self-scanned photodetector linear array placed in the focal plane of the breadboard. The detector-to-detector spacing is 0.6 mil (15.6 μm) which results in an array length of 1.0368 inch. The scene radiance was 3.0 mW/cm^2-sr in the 0.7- to 0.8-μm spectral band. Using the breadboard lens at a focal length of 240 mm results in an effective focal ratio of f/12.8. The angular resolution under these conditions is 62 microradians.

Figure 36. 1728-Detector Image

Irradiance at the detectors for this image is 210 $\mu J/m^2$ and for an experimental noise equivalent irradiance (NEI) of 1.4 $\mu J/m^2$, a system signal-to-noise ratio of 150 was obtained.

2.5.2.4 Image Artifacts

One of the objectives of the breadboard program is to evaluate the performance of photodiode linear arrays in the context of image artifacts. Figure 37 is a bar chart target image obtained from the 1728-detector array and several image artifacts are identified. The artifacts are:

a. Nonoperating Elements

These are either seen as either black or white or white streaks and may be due to:

(1) The detector does not respond to light.

(2) The detector has a characteristic such as offset which is much different than the normal value.

(3) The detector has a high offset (or low) such that only a portion of the illumination range is within the linear processor range. This artifact is not likely to be observed on a bar target, but appears to be operating intermittently in a general scene.

b. Wave Effects

(1) In the across-scan direction, a waviness is seen which is due to phasing between detector and the scene edge (see figure 38).

(2) In the along-scan direction, both waviness and steps can be seen. This is due to both phasing between detector and scene edge and chip-to-chip alignment error.

c. Leakage Lines at Chip Edges

This is seen as a white line protruding into a dark area and is due to light leakage at non-metallized chip edges.

d. Tooth-Effect

The tooth-effect as shown in the figure is not an artifact and is included to show the effect of a computer program error. This error shows the detector stagger effects.

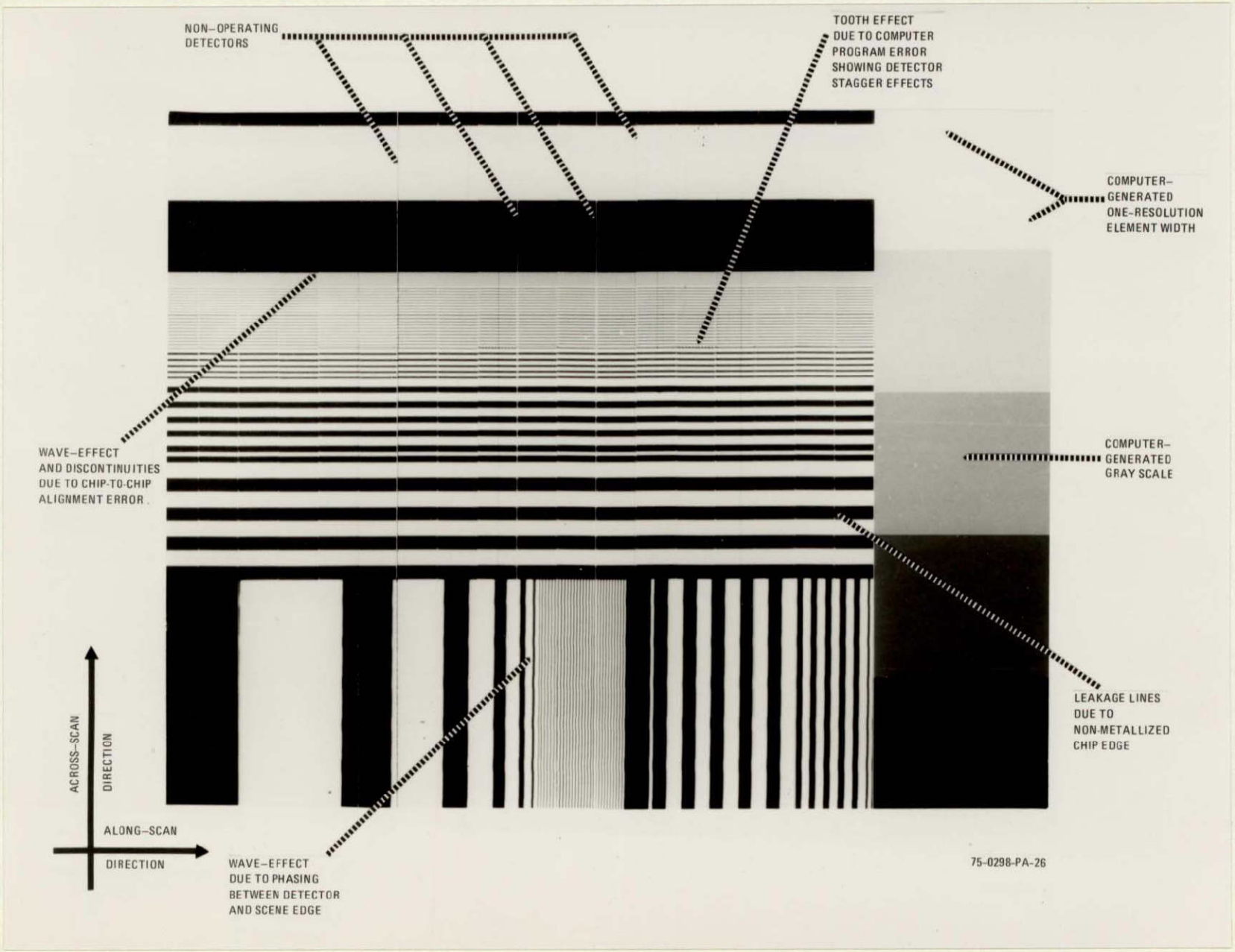


Figure 37. Examples of Image Artifacts on Bar Chart

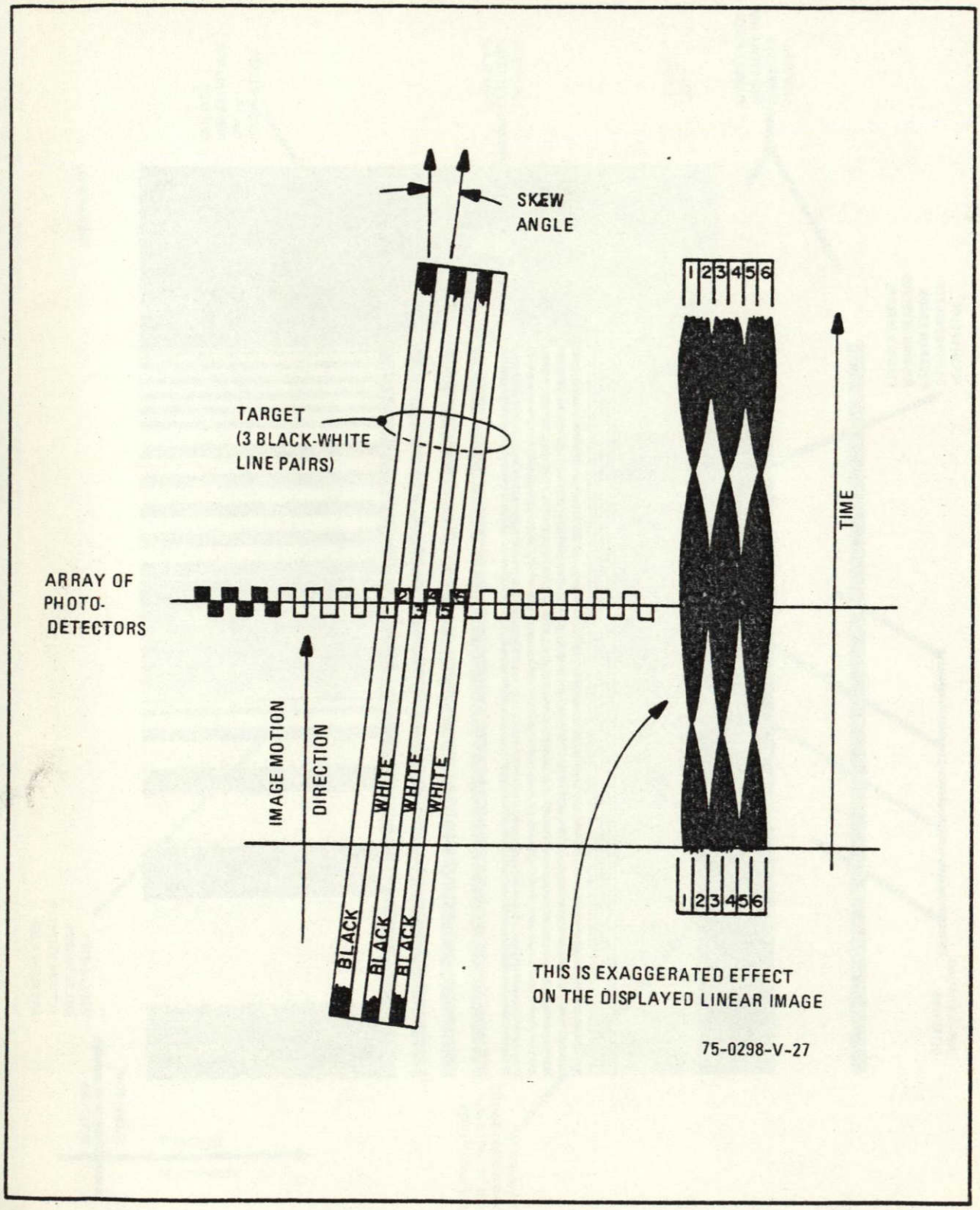


Figure 38. Wave-Effect Due to Phasing Between Detector and Scene Edge

e. Thermal Streaking

This is due to the effect of the difference in temperature of detectors at calibration and when a real image is recorded.

2.5.2.5 Thermal Streaking

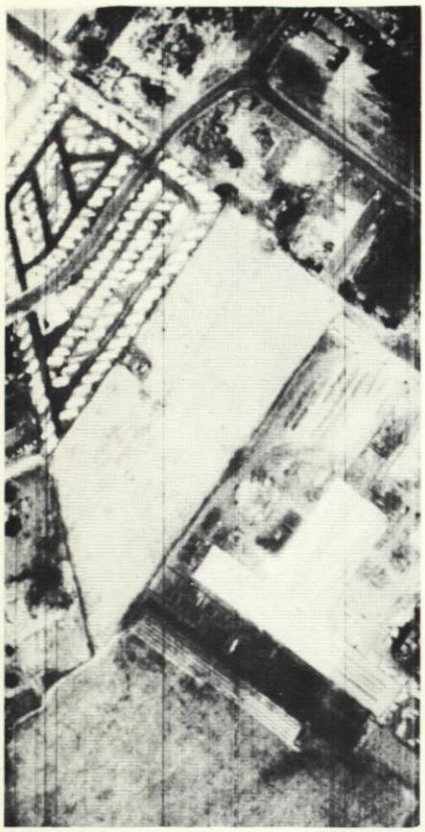
Tests performed on the breadboard system resulted in a phenomena which is referred to as thermal streaking. This phenomena is common to highly parallel processing systems where it is caused by changes in dark current as a result of temperature changes of the detector array. For example, a change of 10°C results in a 2:1 change in dark current (see Appendix F). Figure 39 shows two pictures, one with thermal streaking and one without. Full scale of these pictures is 211 $\mu J/m^{-2}$ and the streaking shown is equivalent to a 2°C temperature change at an ambient of +20°C. The most predominant lines are equivalent to a 50 $\mu J/m^{-2}$ error or 25 percent of the full scale scene. For an uncooled array (nominally 20°C) maintained at ±1°C, thermal streaks of ±2 percent of full scale would occur. If the array is cooled to 0°C and maintained to within ±2°C, thermal streaks less than ±1 percent will occur. The results of this test strongly indicate that for operational applications, thermal control of detector arrays is desirable.

2.6 ARRAY FABRICATION IMPROVEMENT STUDY

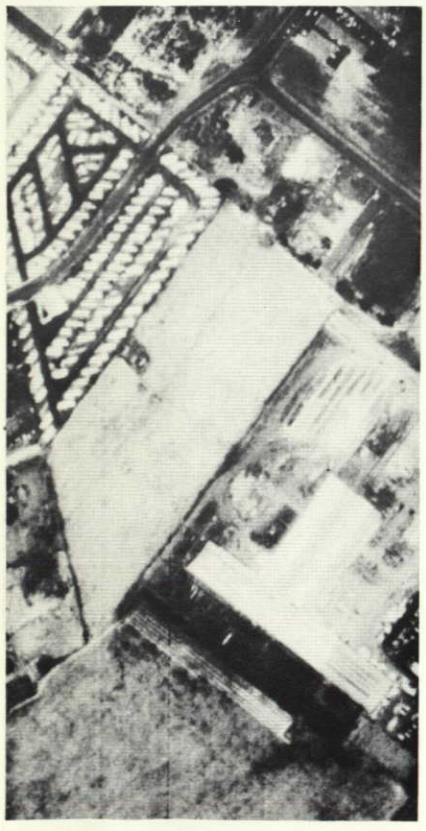
2.6.1 Introduction

In compliance with the Statement of Work, an array fabrication improvement study was performed. The purpose of the study was to show the status of array fabrication, experience gained, and improved fabrication methods to achieve higher yield, reduced assembly and alignment time.

The methods proposed and the equipment recommended also serve the purpose of advancing detector array fabrication from the development to a limited production stage, a transition necessary prior to entering into a flight program.



This scene includes lines attributed to a thermal streaking phenomena. The calibration curve used for data normalization and the scene data were taken at different times (and temperatures) in a laboratory without temperature control. Since the offset varies 5 percent/^{o}C, the 10 percent change in level between the calibration and scene runs indicates a 2^{o}C temperature difference, well within the temperature range encountered in the room.



This scene was made with the calibration and scene data taken within a short time interval; i.e., 15 minutes. With the short interval involved, the array temperature did not change significantly. This shows the data improvement which can be obtained by thermal control of the array.

Figure 39. Example of Thermal Streaking

Since the beginning of the breadboard linear array program, three detector arrays have been fabricated, two 576 diode arrays and one 1728 diode array. In the assembly of a detector array there are many stages in assembly; the most complex steps are the joining of the photodiode chip to the chip carrier, the assembly of the chip carrier assembly to the baseplate, and alignment of the photodiode chips in the desired geometric position.

2.6.2 Alignment Results

As was expected, using manual methods of alignment resulted in some positional error in the arrays. Measurement results taken on the 6-chip (576-detector) array in the across-scan direction were:

- Average deviation from nominal position = 2.3 μm
- Maximum deviation from nominal position = 5.1 μm

In the along-scan direction, or along the chip common axis, the measurements were:

- Average deviation from nominal position = 2.5 μm
- Maximum deviation from nominal position = 5.1 μm

From these test results, it is concluded that the maximum deviation from the reference (best fit) line is:

- 0.28 (or 5.1 μm/18.0 μm) of the detector dimension in the across-scan direction
- 0.23 (or 5.1 μm/22 μm) of the detector dimension in the along-scan direction

With the use of a measuring microscope, an imaginary reference line (best fit) was developed which minimized the detector lateral excursion from the reference line. For the 6-chip array, the maximum lateral excursion was 0.2 mil (5.1 μm) and for the 18-chip array, the maximum lateral excursion was 0.3 mil (7.5 μm). These results are within the specification requirement.

In terms of resolution elements, the results of breadboard programs indicate that a positional accuracy of about 1/4 resolution element has been achieved. Expressed in terms of the linear dimension of an array chip, the alignment error is less than 0.3 percent of that dimension.

2.6.3 Problem Areas

When assembling and aligning chips in the detector arrays, two problems were observed. First, due to manual alignment and assembly, there is no mechanical control or assistance present during the movement of the chip into position. The operator must rely solely on manual dexterity. Occasionally this will result in collision between the chip being aligned and an adjacent assembled chip. This can result in a chip edge damage and possibly the loss of an end photodiode.

The second problem arises during chip positioning or alignment when the chip carrier assembly is assembled to the baseplate. The fixing screws are lightly torqued so that further damped movement of the chip carrier assembly in relation to the baseplate is possible. It is at this stage that final alignment takes place and is implemented by very light taps at suitable points on the chip carrier. Due to the several variables, including variations in surface roughness at the baseplate and chip carrier interface, and slight variations in applied torque, overshoot and undershoot may occur during alignment. There is also the possibility that while positioning on the X and Y axis, the chip carrier may commence to turn about the Z-axis (optical axis). This adds complications and increases time required to complete the alignment.

Therefore, techniques used on the breadboard were costly both in time and materials. To eliminate this condition for future applications, a study was performed to determine improved methods of assembly.

2.6.4 Study Objective

The objective of the fabrication improvement study is to identify improved methods of array assembly intended to improve manufacturing efficiency and reduce cost.

Improved manufacturing methods will not only result in efficiency and lower cost, but will also permit greater accuracy in chip alignment. Therefore, it is reasonable to reduce the experimentally achieved deviation of 1/4 resolution element to 1/10 resolution element.

Another important parameter is the chip Z-axis dimensional tolerance and is directly related to focus. For the breadboard, this adjustment was made manually during the process of cementing the chip to the chip carrier. This procedure resulted in lack of good control of chip face angle and coincident chip-to-chip face position on the Z-axis.

Figure 40 shows the relationship between depth of field and f/No. for the wavelength covered by the photodiode chips, assuming that the Rayleigh criterion is a reasonable design objective. For a candidate future sensor, an optical system with a focal ratio of f/4 is required. It is seen from the figure that the depth of focus for $\lambda = 0.5$ μm will be ±16 μm. Improved techniques will ensure placement of chip within this limit.

2.6.5 Candidate Approaches

The operator skill required to align photodiodes on the breadboard model detector arrays was of the highest order. It follows, therefore, that for future applications, the number of operators available to perform such a function will be minimal, and the skill required from the operator cannot be guaranteed to be continuous. The degree of skill will vary from day to day because of human factors. The higher the degree of skill required, the lower the chances of maintaining such skill at peak level.

It is clear that in a flight program involving many arrays, it would be advantageous to find a way to reduce the necessity for highly skilled operations with attendant low yield high cost and prolonged assembly time.

The type of equipment required to minimize manual skills must be of a kind which eliminates the necessity for direct contact between the operator's hands and the parts to be aligned.

The approaches available generally fall into two categories. The first approach using micropositioners has certain disadvantages such as the greater possibility of involuntary overshoot while positioning and the possibility of mechanical crosstalk because of the need to control several axes from one source. All this can be avoided by using the second choice -

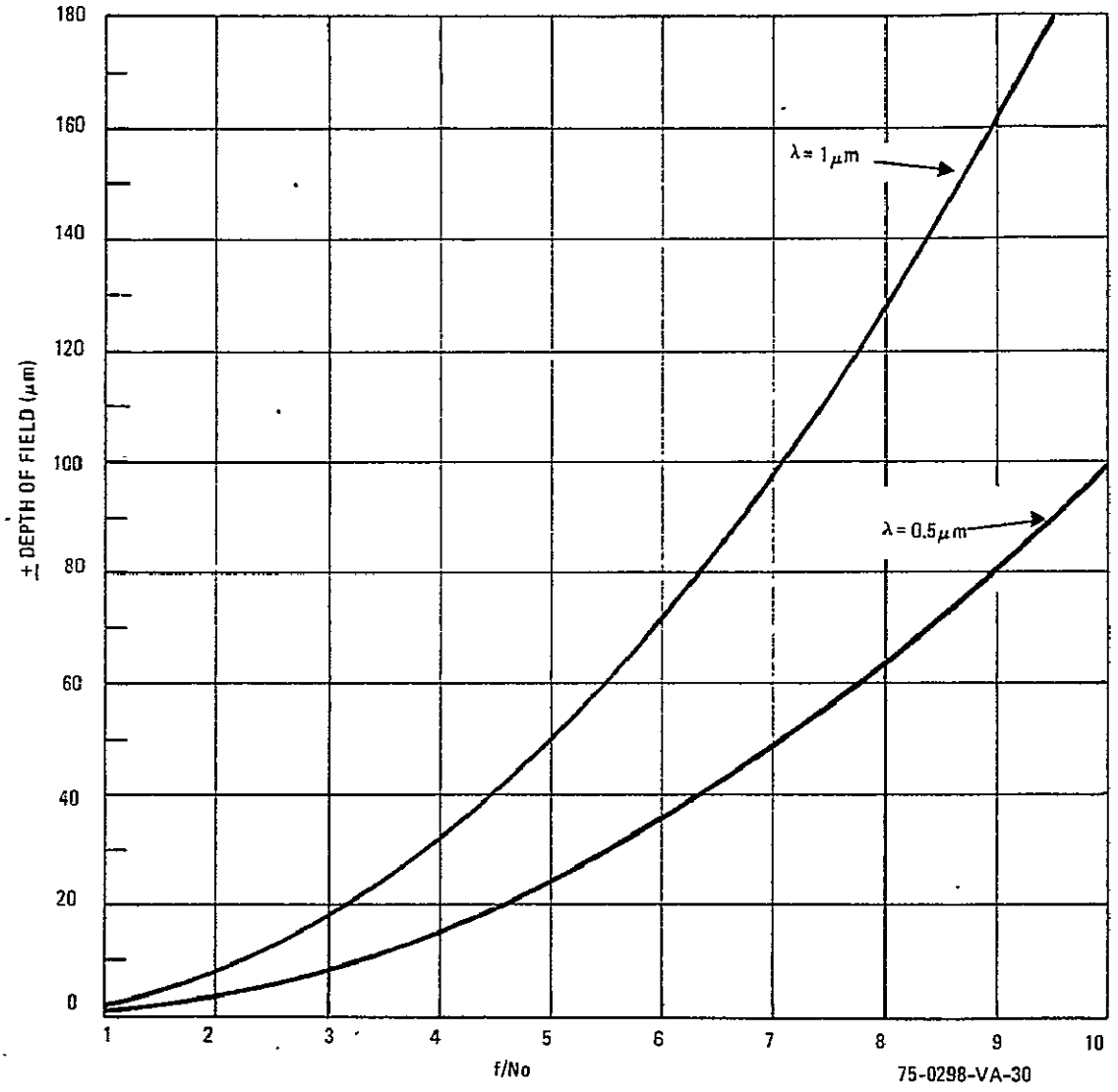


Figure 40. Depth of Field vs F-Number (Assumes Rayleigh $\lambda/4$ Criterion and Depth-of-Field Given as Deviation From Nominal)

whereby each axis movement is controlled separately, thus eliminating the possibility of crosstalk. Direct axis movement would be implemented using micrometer controlled positioning. The latter ensures smooth, damped, predictable movement without overshoot. Thus, this latter approach has been selected as the preferred approach.

2.6.6 Preferred Approach

The preferred micropositioner, including the microscope used for observation during positioning, is shown in figure 41 and comprises the following:

a. Detector Array Fixture
b. Goniometric Turntable, Phase Z
c. Extension Plate
d. Translation Stage, X-Axis
e. Translation Stage, Y-Axis
f. Laboratory, Z-Axis
g. Baseplate
h. Device for Holding Chip Carrier during Assembly.

Additional views of the micropositioner are shown in figures 42 and 43. The entire equipment is mounted on the microscope stage plate. During assembly of the development arrays, a microscope with total magnification of 25X was used for observation during assembly, and 100X magnification for final alignment. Illumination during assembly is obtained from a source in the base of the microscope which provides a silhouette of the chip carrier as it approaches its optimum position in the detector array. In this way, an observed clearance can always be maintained while the carrier is moved into position, thus minimizing the possibility of chip edge damage.

Before operating the micropositioner, the chip carrier will be placed and held on an electromagnet so that the center of chip will be aligned with the axis of the turntable. By appropriate setting of the various micrometer controls of the positioning equipment, the chip carrier assembly will be

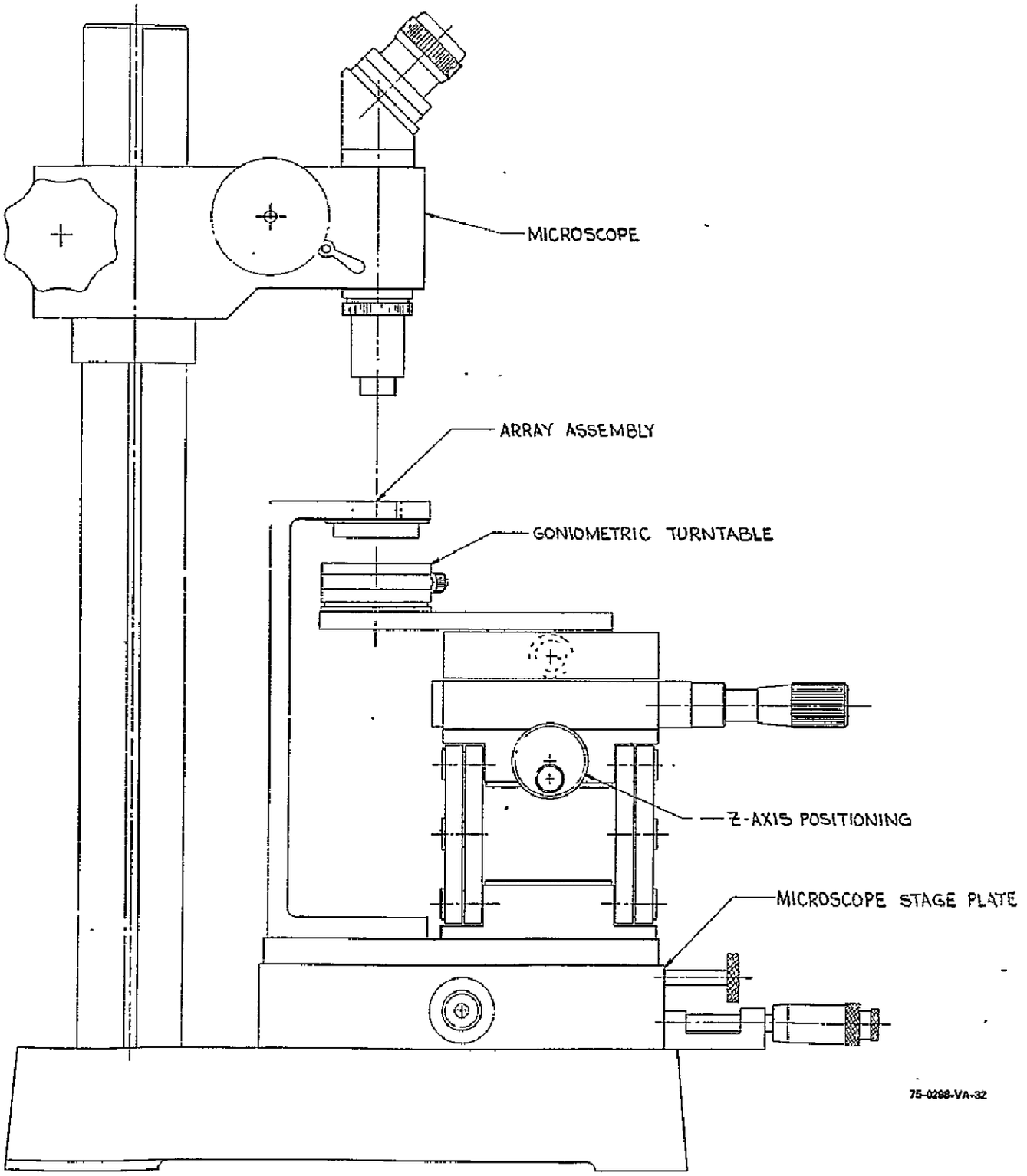


Figure 41. Chip Carrier Assembly Micropositioner and Microscope

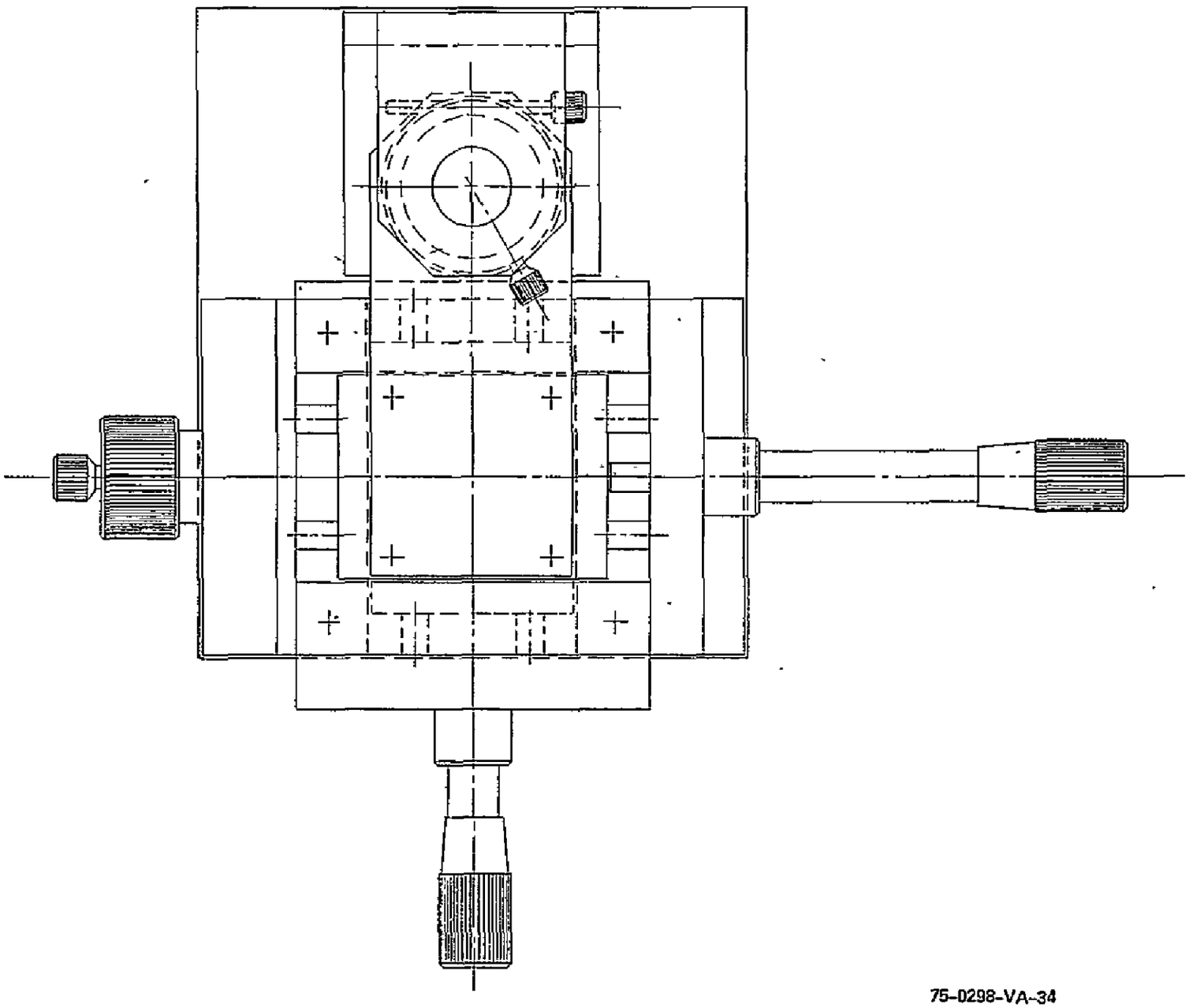


Figure 42. Chip Carrier Assembly Micropositioner (Top View)

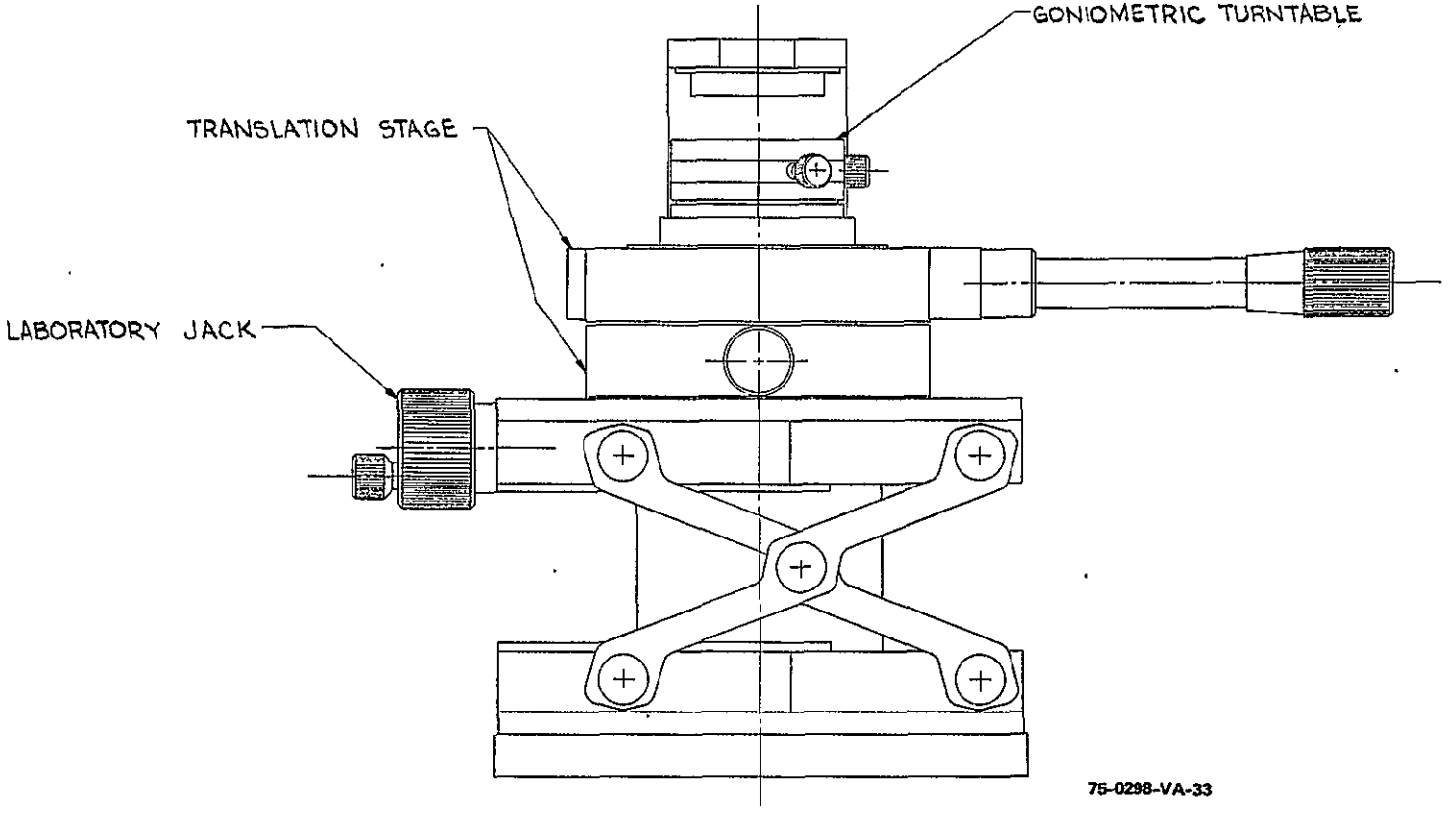


Figure 43. Chip Carrier Assembly Micropositioner (Side View Showing Jack)

elevated to the level of the detector array baseplate and then moved to and held in the desired position - at which time the chip carrier screws will be inserted and tightened. The process will be repeated until the whole array is finally assembled. Figure 44 shows an exploded view of the array assembly. Figure 45 is a view of the assembled chip carrier.

There are indications that, in the future, greater detector positional accuracy will be required although not yet precisely specified. With this in mind, the micropositioning equipment chosen will have the capability of positioning chips within 1/10 of a resolution element. To achieve this result depends on the use of high sensitivity micrometers and the rigidity of structural members holding the positioning system together.

Due to the variation in chip thickness, it was not possible in the breadboard program to control chip surface height variation in the image plane. However, a jig has been designed (see figure 46) which reduces the variation in height of the chip surface plane above the chip carrier mounting surface to an acceptable value. The jig is constructed in such a way to make it fully adjustable and capable of being set to a precise position by the use of gage blocks.

In the sequence of chip-to-chip carrier assembly, the chip is placed face down in the bottom of the jig resting on a reference surface. The part of the chip in contact with this surface contains none of the circuitry or bonding pads associated with the electrical-optical configuration and, therefore, no damage to the active surface of the chip is anticipated. Physical contact is made only with the bare silicon chip which presents a standard reference contact for all chips.

The insertion of the chip will be followed by the chip carrier with chip mounting surface facing down. The mounting surface contains a narrow slot into which is pressed a preformed epoxy film adhesive of suitable volume.

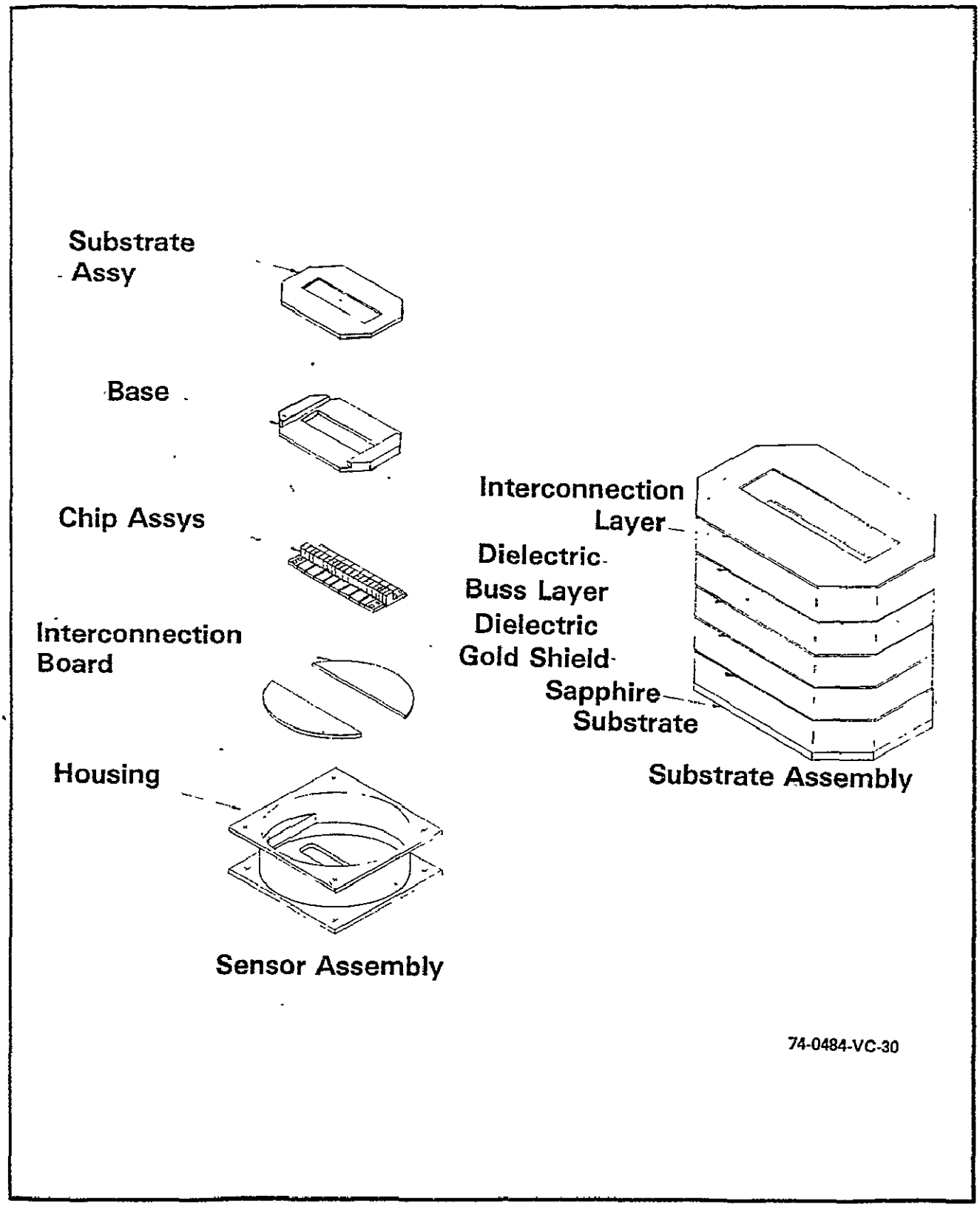


Figure 44. Exploded View of Array Assembly

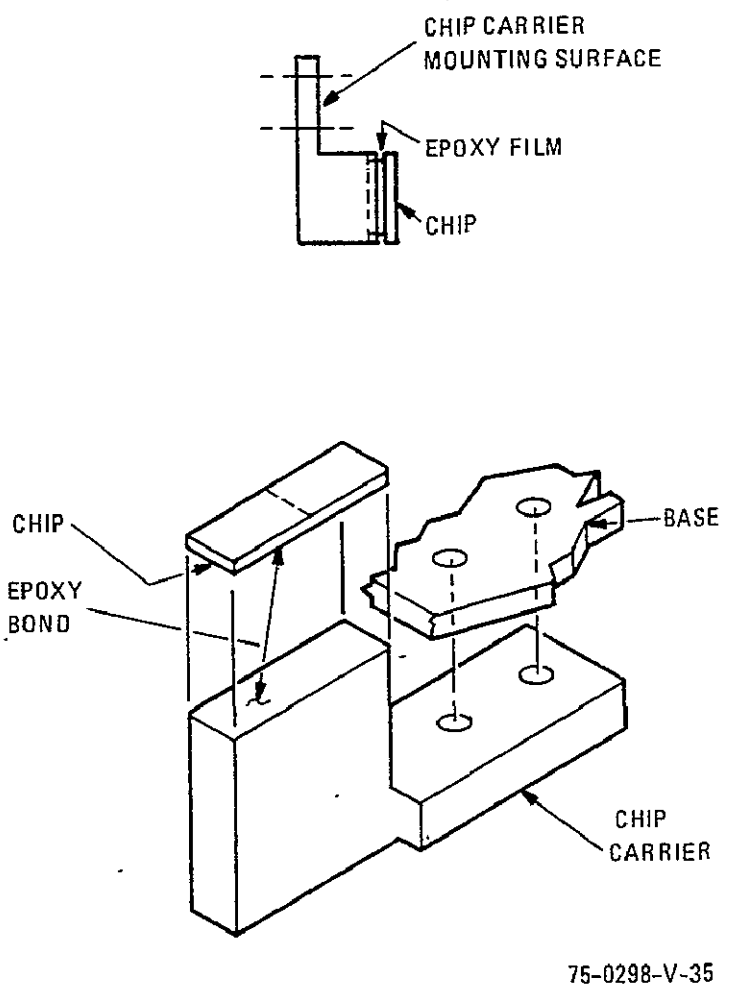


Figure 45. Assembled Chip Carrier

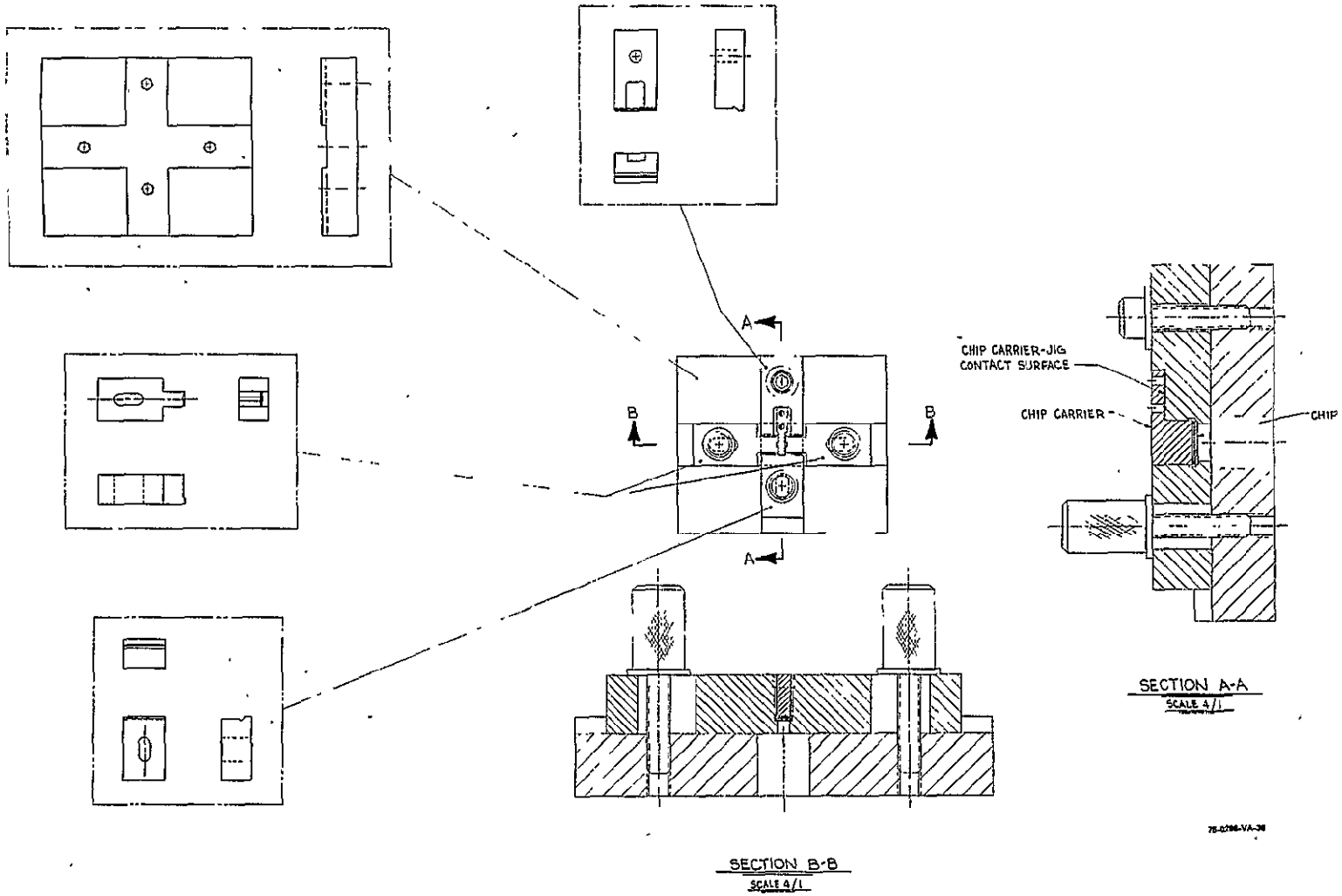


Figure 46. Chip Carrier Assembly Jig

With the chip carrier in place, there will be a gap between the chip carrier mounting surface and the chip carrier jig contact surface. The gap is caused by the thickness of the epoxy film now in contact with the underside of the chip.

Upon application of heat to the jig of a temperature sufficient to cause the film epoxy to flow, and upon the application of a light pressure to the chip carrier base, the epoxy will flow and the gap will close. This will ensure that the distance between the active surface of the chip and the carrier mounting surface will be uniform on all chip carrier assemblies. Further application of heat will cause the epoxy to cure. All chip carrier mounting surfaces will be assembled to a common baseplate reference in the detector array. This will keep the Z-axis chip surface deviation to a minimum.

There are many factors contributing to the quality of the final product. Reference has been made to suitable equipment to assist in accurate positioning of detectors. However, the operator must have the means to observe and check the accuracy of his operation. Not only must the positioning of detectors be accurate, they must be seen to be accurate.

This brings to mind the problem of seeing. During the assembly of the development arrays, use was made of Leitz Simplex Microscope System, and the accuracy of observation of this system depends upon the operator's ability to achieve parallax focusing. Failure to do this causes an apparent shift of the filar line in relation to the object being measured. This occurs if the eye is unconsciously moved off the optical center. This may happen after many observations and is probably due to eye fatigue.

A system that will eliminate subjective errors of this nature is the Tele-Microscope, a closed circuit television system. This comprises a Leitz microscope, and a video camera head and display. The camera head is fitted to the microscope tube and replaces visual observation by the eye through the normal microscope eyepiece. Unlike the human eye, the video

head cannot move and parallax error is eliminated and thus improves overall fabrication accuracy. A further added advantage with the Tele-Microscope is the useful magnification up to 400X, and the electronically generated filar lines displayed. Together with an associated measurement computer and digital readout, measurements as small as 0.1 μm can be made provided the edges of the photodiodes are sharply defined. Such a system will mean faster and more accurate measurements with only moderate operator skill requirements.

A flow diagram of the entire fabrication procedure for potential use on a future flight program is shown in figure 47.

2.6.7 Fabrication Study Summary

The experiential learning gained from the breadboard program has been extraordinarily beneficial in many areas. The experience gained in the fabrication arrays has shown that it is totally feasible to fabricate long arrays. Although positional accuracies of about 1/4 resolution element were achieved, where 1/10 is a suggested goal, the experience gained in this preliminary program strongly indicates that the latter positional accuracy can be achieved for future requirements.

2.7 REAL-TIME OFFSET AND GAIN CORRECTION

A modification extended the scope of this contract to fabricate, test, and evaluate a real-time offset and gain correction capability. Appendix J describes the recommended approach. The following paragraphs discuss the mechanization of the modification and the effects of real-time correction of the data. It is concluded that onboard real-time correction can be used to ensure that a low cost ground station is available to produce high quality imagery from a completely solid state remote sensing system.

2.7.1 System Impact

2.7.1.1 Calibration

A calibration means is required for any remote sensor from which accurate radiometric data is required. The nonuniformity of gain, linearity, and dark level between individual photoelements of an array increases the necessity

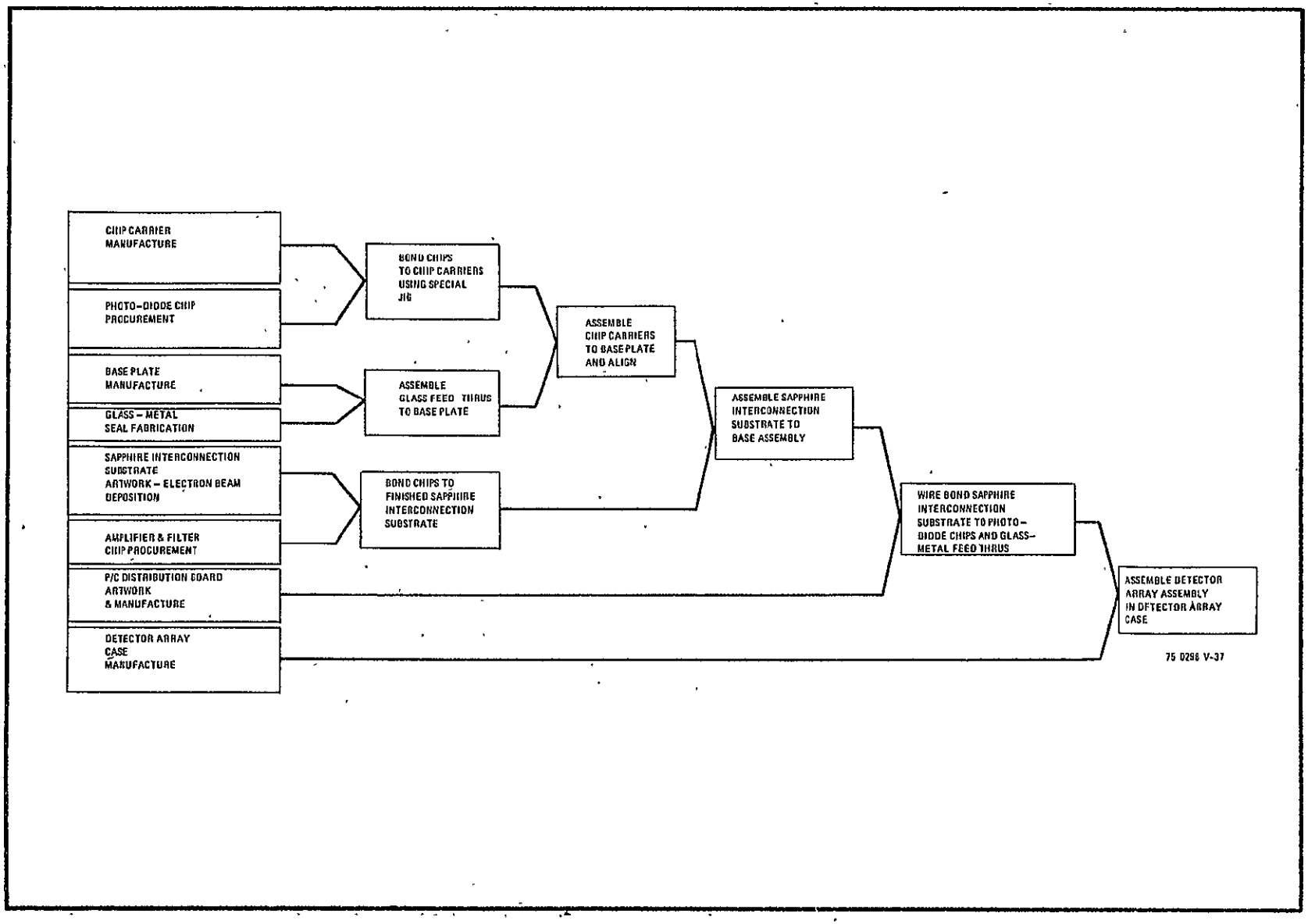


Figure 47. Detector Array Assembly Functional Flow Diagram

for calibration. Of importance in this discussion is the understanding that, unlike most point detector systems, an array cannot and (with proper system design) need not calibrate on every line. Inclusion of a real-time processor does not change the necessity or the technique of calibration of the solid state array. What is accomplished by the use of the real-time processing is the increased flexibility of calibration.

For on-board dark reference calibration, it is necessary for the remote sensor instrument to block the aperture by using a shutter for a dark level reference; also to provide a source of illumination such as a solar input or tungsten bulb as a gain reference. These inputs are scanned, thus providing the data for either ground or real-time processing. The difference occurs in the timeliness and sophistication of the calibration data usage.

It is obvious that a ground facility can provide very sophisticated data processing by means of a large scale computer. With several calibration levels, equations can be computed to normalize the data, removing most nonlinearities and, thereby, providing very accurate relative radiometric data. For many users, this (large computer) capability is required. However, with this type of capability, it is likely that data turnaround time will be slow and the facility costs will be high. It is also a necessity that calibration data be not only registered to a particular sensor, if stored on ground, but also time-registered to the data being processed if multiple calibration cycles have been performed per data transmission cycle.

The onboard processing in real-time will not provide the sophistication of the ground system, but it does provide an effective means to simplify the ground collection and film recording system. The application of calibration to the collected data is immediate because it was the last-obtained calibration data. This feature is of primary importance when related to thermal control, discussed in a later paragraph. There is no necessity to correlate the particular calibration sequence to the data.

The onboard processor does not preclude the use of the large ground processing facility where extreme accuracy is important. Several gray levels can be transmitted, and ground processing could provide the same results as is obtained without the real-time system.

Multilevel versus two-level calibration is of interest with real-time processing. Two levels - dark and one radiance level - are required to establish the basic dark and gain profile. After the two-level normalization, subsequent processing and transmission need not handle the larger signal dynamic range of data containing dark offset and gain errors. Figure 48 shows a typical array channel output, without real-time processing, indicating the dynamic range lost to gain and dark-level variations. It can be seen that removal of gain and offset will be a reduction of several significant digital bits (a factor of 4 or more). Additional calibration levels will improve the data accuracy at the cost of a large increase in hardware. Each additional level would proportionately increase the hardware while the data improvement would not be recognizable to a simple ground station. The maximum improvement would be to correct the 3 percent linearity (shown in an earlier paragraph) which is compatible with a 32 gray level data range. Increasing the resolution to finer than 32 levels would not recognizably change the photographic reproduction[5] and, therefore, would be of little value to users of primarily photographic imagery.

In summary, calibration techniques are the same for real-time or ground processing. In addition, realtime processing does not limit the ability to include calibration levels for higher quality ground processing. Real-time onboard processing permits the implementation of simplified ground processing and display.

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[5] "Computer Eye - Handbook of Image Processing," Spatial Data Systems, Inc., 1975.

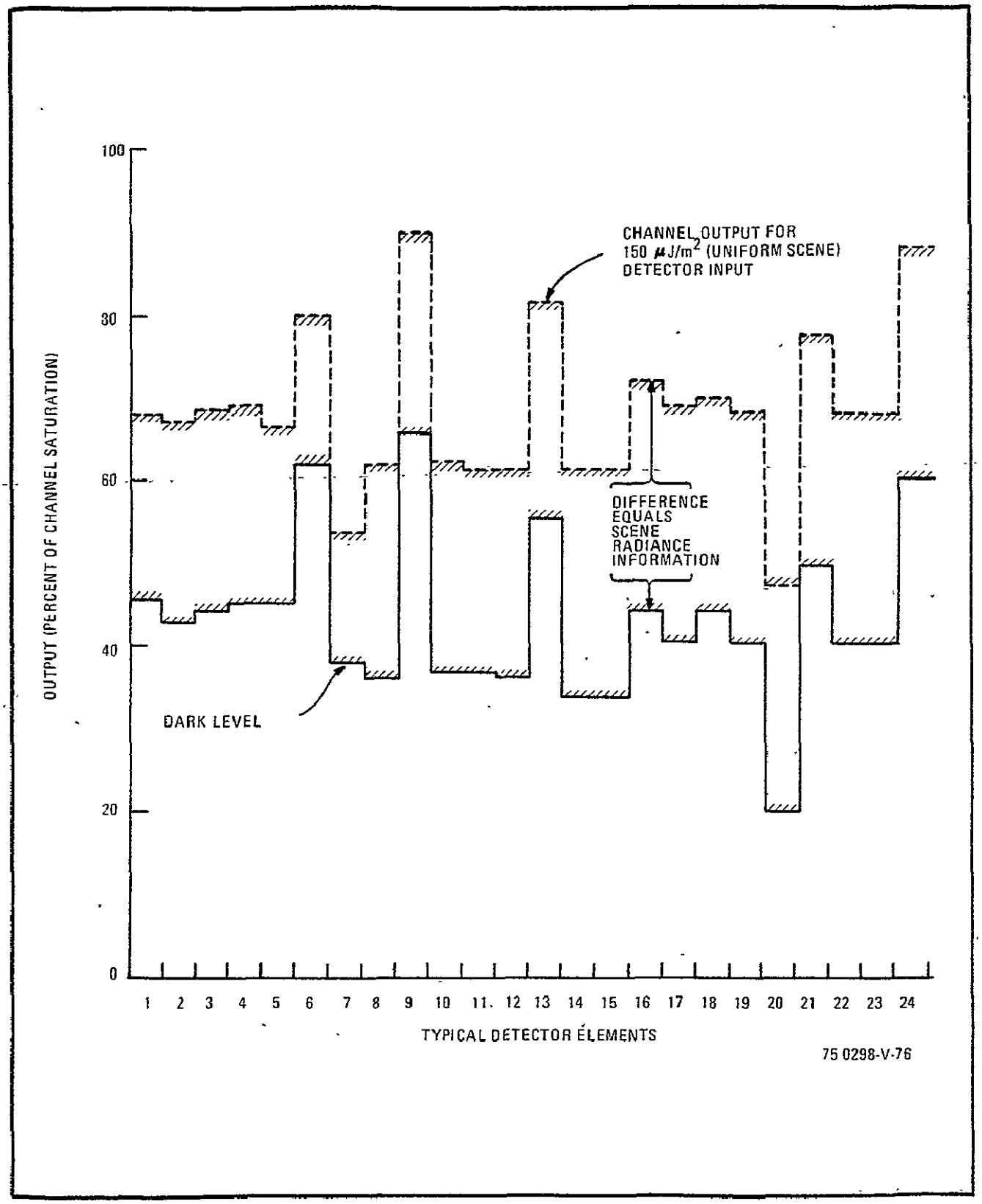


Figure 48. Typical Channel Dynamic Range Usage with a Solid-State Line Array Imager

2.7.1.2 Thermal Control

Thermal drift is one of the more significant problems of the photodetector arrays. Real-time processing provides a means of greatly reducing the thermal effects which, in turn, would ease the onboard thermal control of the photodetector arrays.

The greatest thermal effect is the change of dark level. Consistent with dark current thermal variations in silicon, the dark offset changes approximately by a factor of 2 for each 10°C temperature change. If we consider that the offsets between elements can vary up to 600 $\mu J/m^2$ equivalent input (i.e., a scene at the subsolar point using f/4 optics and $\rho = 0.2$) at 25°C, it can be seen that even a very small temperature change causes a large signal error. The direct approach to minimize this error is to lower the temperature and precisely control it. Simplification of the thermal control system by widening the temperature tolerance can be achieved by real-time processing.

At 0°C, a ±0.5°C thermal drift would cause a peak to peak error equivalent to 3.5 $\mu J/m^2$ irradiance, or about 1 percent of the irradiance from a typical scene at the subsolar point. For a system design requiring the drift error to be held below the general noise level, it would be necessary to either control the 0°C baseline temperature to within ±0.1°C or else lower the baseline to -30°C controlled to ±0.5°C, with a resultant error of 1 $\mu J/m^2$. A system with real-time processing could allow a 0.2°C/min drift rate about the nominal 0°C baseline, while maintaining the 1 $\mu J/m^2$ maximum error, by performing a dark reference at 30 sec intervals. The shutter mechanism causes some data loss (possibly a few milliseconds), and at least three scans are necessary to ensure a good reference. Therefore, for a data loss of less than 0.1 percent (i.e., 200 m loss out of 200 km ground track at 900 km orbit altitude), tight thermal control can be avoided.

2.7.1.3 Noise Impact

The imaging system with real-time processinghas several noise-related characteristics. Random niose creates errors in the offset and gain factors as they are read into memory, causing errors in the gray levels. A coherent gray level error is created during the normalization process. The results and possible solutions of the error sources are discussed in the following paragraphs.

Noise is always present and is contributed by both the detector and the data processor. This noise is low level and random, and in high radiance scened it does not itself significantly degrade an image. The rms noise level of the breadboard image system is less than 1 percent of the maximum irradiance. The greater problem is the effect of niose on the real-time processor. The present mechanization uses a single scan line for each calibration level. On the basis of that line, the real-time processor removes offset or applies a multiplication factor. Noise on that line, therefore, becomes a coherent error in the data, which creates streaks in the processed image.

The first step of the processor is to remove the elemental offset by subtracting the stored dark level from each data line. If we consider that the maximum error is only plus or minus one count, this does not seem to be a big problem. However, because of the way in which the logic is designed, there is a minimum multiplication factor of 2; this means that the minimum effective error is really plus or minus two counts at the imager system output. From element to element, this represents a four-count possible difference. Figure 49 shows that a four-count coherent error is readily observable. Complicating the problem somewhat is the factor of three possible in the gain variations between elements. The lower gain elements will have a higher correction factor creating a greater error.

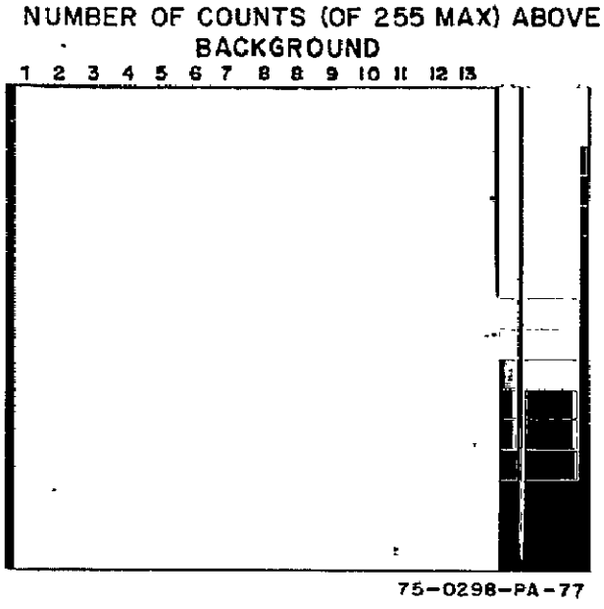


Figure 49. Observability of Count Errors

Similar to the offset correction, noise can affect the gain factor selected. In the minimum correction situation, a plus or minus one count variation will change the gain factor ±1.5 percent, or ±3.8 counts at full scale. This effect, unlike the offset error, is proportional to the input level. It, therefore, becomes more prominent at high levels and is effectively nonexistent at low levels. This effect also will become worse with lower gain elements. The gain variation can be as much as 3:1, although the majority of elements do not exhibit that gain spread. A full scale error of ±10 counts could exist for the plus or minus one count noise with the low gain elements. Thus, as in the case of noise in the stored offset reference, it can be seen that small amounts of noise in the gain correction reference can also contribute significant coherent, errors particularly at high irradiance levels.

Another pehnomenon is created, not by the detector or thermal noise, but by the quantizing of the data. The original processing circuitry mechanization quantized the data to eight bits (256 levels), and this range was not changed by the addition of the real-time processor. To simplify the arithmetic circuitry in the real-time processor, an assumption was made that at least 128 counts of the detector array digital output would correspond to the offset signal at dark. This is a real condition at typical radiance levels of 25 W/m^2-sr and room temperature operation and therefore is considered valid. This leaves a possible maximum signal dynamic range of seven bits (127 levels). A maximum radiance scene irradiating the highest gain detector element will, therefore have a dynamic range limited to 127 levels at the input to the real-time processor. As each detector of the array has a unique gain with a total possible variation of a factor of 3, the lowest-gain detector element irradiated by the same maximum radiance scene will be quantized to 42 levels and the highest-gain detector to 127 levels. Detectors at these limits will respond to radiance changes of 2.4 percent (1/42), and 0.8 percent (1/127), respectively, of a maximum radiance uniform scene.

The real-time processor normalizes the response of each detector to a 255 level maximum. Therefore, with a maximum radiance scene, both the high and low gain detector outputs will be 255 counts after the real-time processor. The signal information has not been changed and, although the actual data word has a level equivalent to 0.4 percent (1/255) radiance changes, the actual data will have only those values corresponding to the prenormalized percentage response (0.8 percent of 255 and 2.4 percent of 255).

Figure 50 shows the responses, for a short segment of the scene dynamic range, of the high and low gain elements after normalization. The high gain element changes only two counts per transition and will look continuous in a photograph, but the low gain element transitions in six count increments, which may be observable. Between the two elements shown, each gain condition (43 levels to 126 levels) also are possible. That means that for any radiant input an output spread can exist of up to six counts. This can

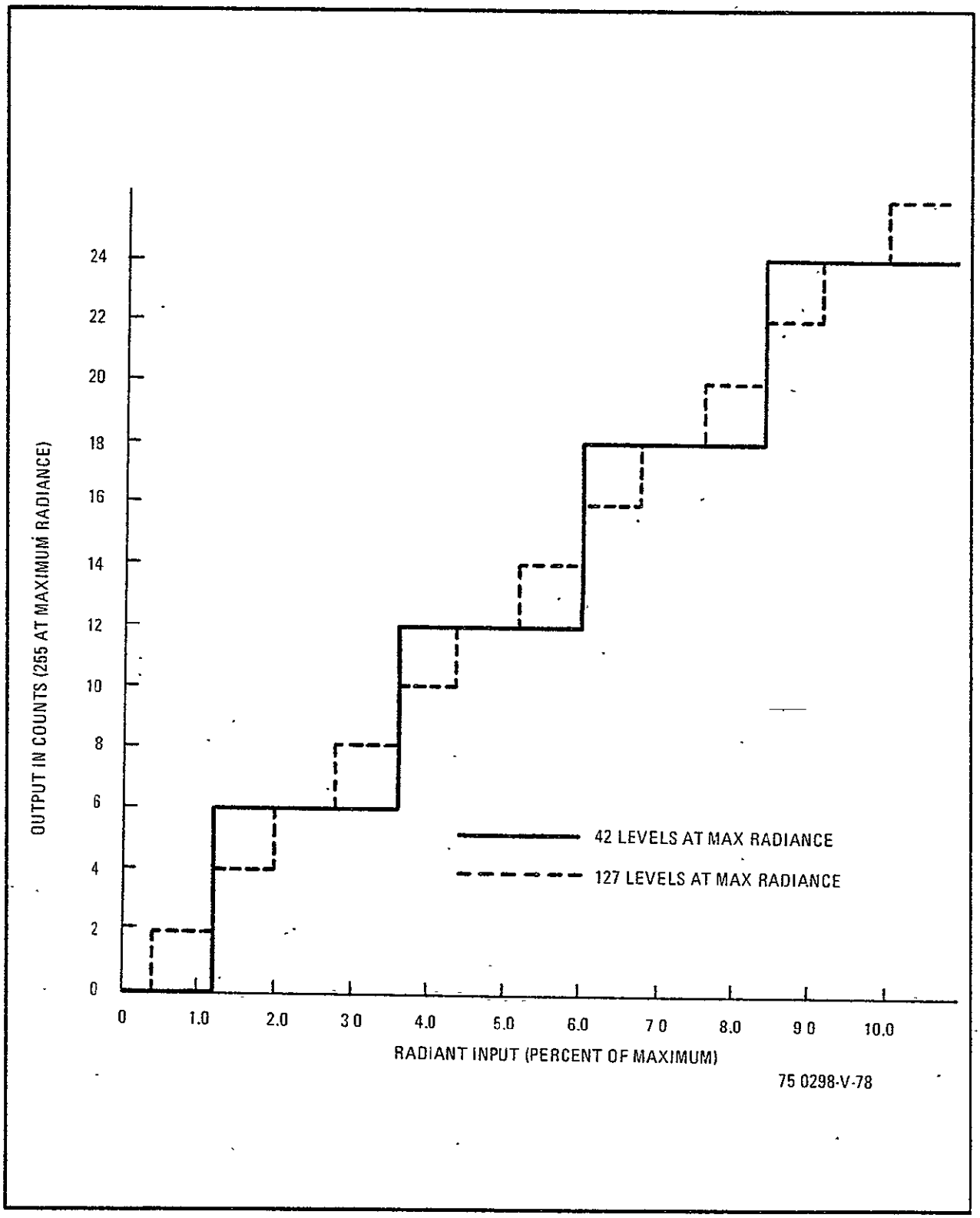


Figure 50. Quantizing Interval for Two Quantization Dynamic Ranges

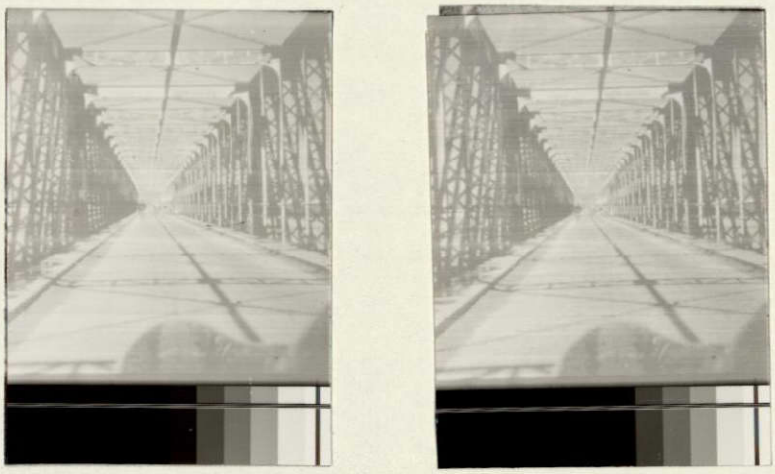
be seen by using an input near (but less than) the 1.2 percent an element with 43 level range would have transitioned to the first level (six counts at the output). While the 42 level element is still zero, the 127 level element is at six counts. At radiant levels less than this the count spread will be lower until below 0.4 percent all elements will be zero count.

A count spread exists for all radiant levels above 0.4 percent up to 100 percent. The effect of this variation in counts will be most visible in nearly uniform scenes with small radiance differences. Its visual effects can be reduced by rounding off the data to the nearest level of the lowest gain element. Figure 51 shows scenes with and without roundoff. Since there is no apparent change in the picture quality, it is concluded that the streaks are not caused by this phenomenon. It is more likely that they are a result of noise in either the offset or gain reference values.

To summarize the discussion of the impact of noise in a real-time correction system, it is seen that the effect of noise can be a significant factor in image degradation. It should be emphasized however, that it is possible to improve the data by averaging the calibration data over several scan lines. This could be easily performed either in real-time or in the ground station as dictated by the system requirements. This becomes a tradeoff between onboard weight and power versus transmission time, data storage, and ground station complexity for the added calibration function.

2.7.1.4 Complexity Comparison Between Noncorrecting and Real-Time Correction

An estimate of relative electronics complexity between noncorrecting and real-time correcting systems in terms of components count can be made. The comparison assumes that the sensor electronics will consist of modules interconnected to form arrays of the required number of resolution elements. Figure 52 is a block diagram of a typical four-band sensor using linear arrays. Each module will operate largely independently, providing the detectors and processing for a segment of the complete array. Some additional electronics, common to all the modules, for power distribution,



(a) 255 GREY LEVELS – NO ROUNDOFF

(b) ROUNDOFF TO 32 GREY LEVELS

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Figure 51. The Effect of Roundoff on Picture Quality

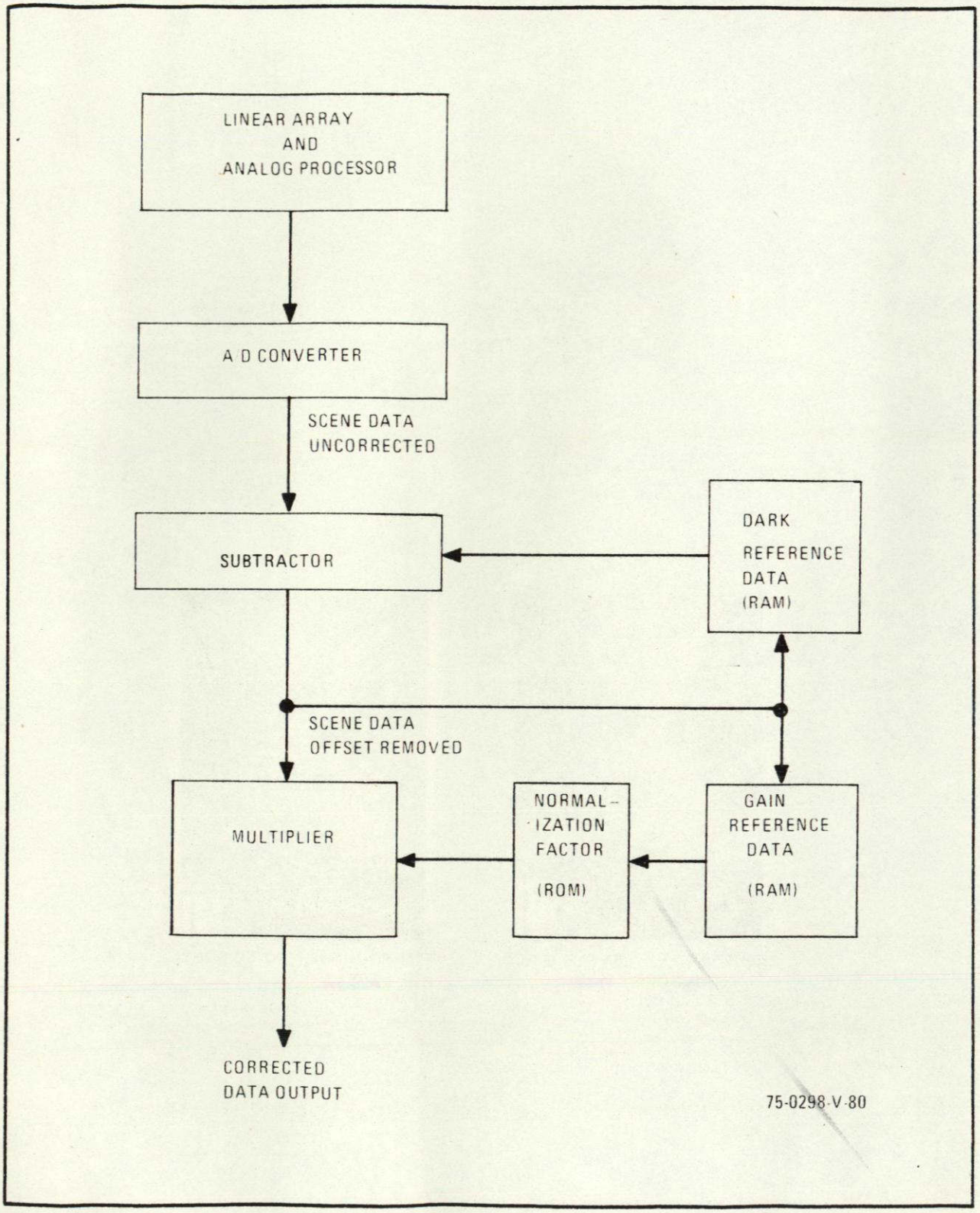

Figure 52. Simplified Block Diagram of the Real-Time Processor

synchronization, and multiplexing, complete the system. It is also assumed that the detector modules internally multiplex the data to four output busses. With integration times of 1.5 msec to 2.5 msec and allowing 8 μsec to 10 μsec per element per bus to process data, a module containing 600-1200 elements is expected.

For a module of 1200 elements with eight bit processing resolution, an estimate of complexity can be determined. It is estimated that processing circuitry for the module requires three circuit boards; real-time correction circuitry requires two boards; the common power supplies, and such requires an equivalent of five boards. With this estimate presented graphically on the stack chart of figure 53, several significant features are apparent. First, the circuitry that is common to the entire system becomes less significant as the system size increases, since its complexity is only slightly dependent on system size. Circuitry for the noncorrecting processing increases stepwise with the addition of modules, but it is a weak function of the number of

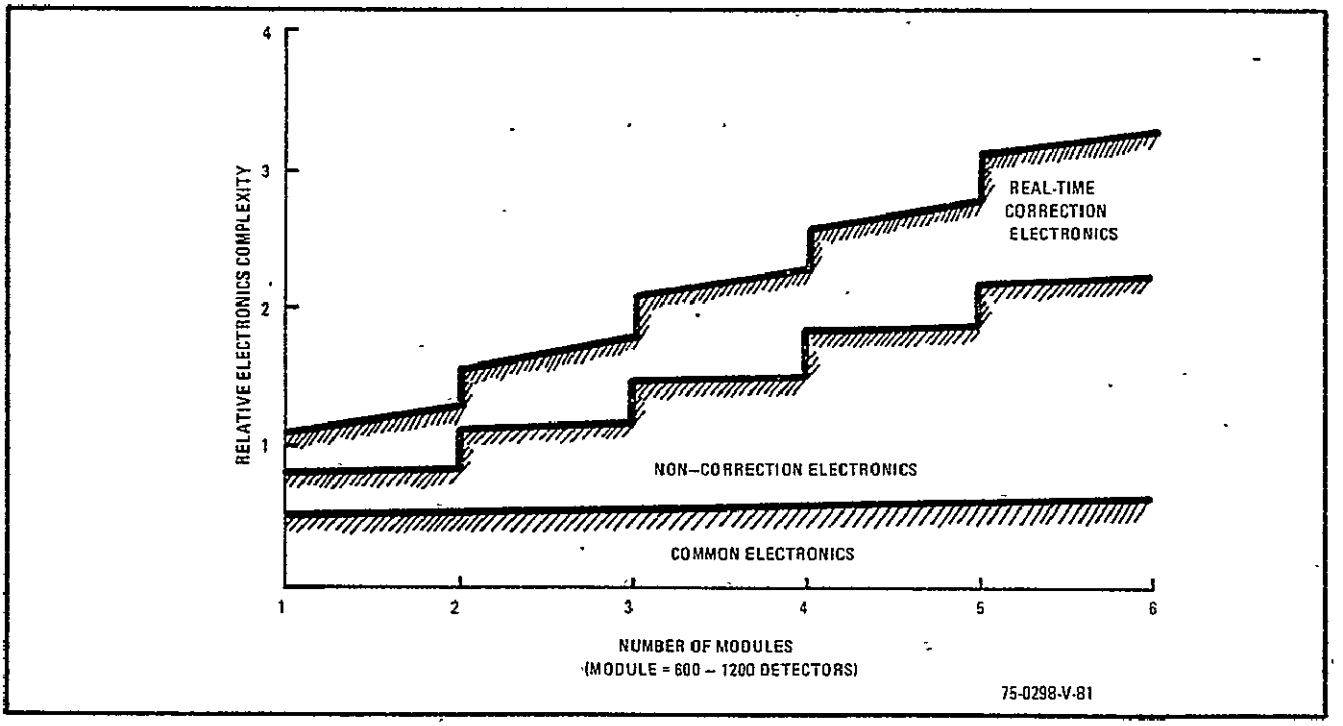

Figure 53. Relative Electronics Complexity with Real-Time Processing

elements within the module. The large proportion of the real-time correction devoted to data storage for each element causes a stronger dependence on module size in addition to the step increase for additional modules.

Figure 53 shows that, for a sensor containing from 3600 to 7200 elements (six modules), about one-third additional electronics complexity is required. This is a significant tradeoff to consider in configuring future space sensors.

2.7.1.5 Power Requirements Impact

The power required to perform the correction processes is strongly dependent on the specific parameters of the system - in particular, the number of detectors, the sampling rate, and the quantization requirements. Nonetheless, the laboratory model built for this contract can provide some general insight into power consumption. The significant power drain falls into three functional areas: the memory used to store calibration data, the multiplier circuitry, and the shift registers used to compensate the staggered array geometry.

The random access memories (RAM's) for offset and gain calibration data each store one word for each element of the array. For a nominal array length of 1000 elements, using eight bit quantization, 16,000 bits of storage are required. The breadboard system uses CMOS chips consuming approximately 35 mW per kilobit, or about 1/2 watt for a 1000 element system. Note that this power level for the CMOS RAMS is with a cycle rate of 100 kHz. If a 500 kHz rate were required, a fivefold increase in power would result. If speeds reached the point where bipolar logic were needed, 1/2 watt per kilobit would be a reasonable power budget. Silicon on sapphire technology[6] offers speeds comparable to TTL at power levels of a few microwatts per bit. This technology could provide very large power savings for larger systems.

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[6] Silicon on sapphire as implied is a thin silicon layer on a sapphire substrate. The low sapphire dielectric constant keeps the capacitance low; hence, higher speeds are possible with the high impedance circuitry. Westinghouse is involved in RAM's and other devices using this technology.

The multiplier used in the breadboard uses 4 watts, producing a product in about 150 nsec. Although the power required is a substantial portion of the breadboard power budget, the circuit is not being used to its full capability in that system. For integration times of 2 msec, up to 10,000 elements could be handled by one multiplier if redundancy is not a design factor. Thus, as the system increases in size, the multiplier power could become less significant with a design maximizing its use.

The shift registers used to delay data for geometric compensation of the staggered array must hold two lines of data for half the elements. For a 1000 element array with eight bit quantization, 8000 bits are stored. The breadboard system uses MOS shift registers for this function, consuming about 0.5 watt per kilobit. Although not so straightforward logically, RAM storage of the type used for gain and offset data could be used for this function with substantial power savings in larger systems. Whichever design is used, power for this function is strongly rate dependent.

In summary, the following paragraphs discuss some of the main elements contributing to a system power budget for the real-time processor capability. Projecting a total power for such a system without clear requirements would be somewhat unrealistic because of the many interactive parameters in the power calculations. Data rates, reliability, and component state of the art are highly variable and can impact on circuitry power by orders of magnitude.

2.7.2 Real-Time Processing Mechanization

Real-time digital processing in earlier configurations of the linear array system was limited to multiplexing and formatting the digitized array data. In these systems, a large scale computer (Univac 1108 or 1110) operated on the recorded data to remove the element-to-element offset, normalize the element-to-element gain variations, and compensate for the spatial offset caused by the staggered layout of the detectors in the array. This paragraph describes the mechanization used to incorporate real-time processing hardware into the original 576-element system. This system mechanization uses

a two calibration point algorithm (dark and half scale). Figure 54 is a block diagram of the real-time processor function.

2.7.2.1 System Operation

2.7.2.1.1 Geometric Corrections. - The staggered layout of elements in the array requires that outputs from half the elements be delayed to produce a contiguous image. The delay is achieved using two eight-bit-wide delay lines inserted into the system between the A/D converter and the bus multiplexer. While the undelayed busses are input directly to the multiplexer, the busses to be delayed are input to 512 stage shift registers. The output is 144 data words per line per bus; therefore, 288 stages of the shift registers are used to hold data for two lines. The system is mechanized to use only every 16th scan, so that the signals from the intervening 15 lines can be used as pseudo-data to fill the rest of the shift register, keeping the delayed data properly aligned with the undelayed data.

2.7.2.1.2 Offset Correction. - Offset correction is the process of subtracting the dark output of each cell from its operating output. An eight-bit subtractor performs the arithmetic operation using operating data from the multiplexer and offset data stored in the offset RAM. The offset correction system is calibrated by covering the array to exclude any illumination and forcing the subtrahend of the subtractor to zero. One scan of data (minus zero) is then stored in the offset RAM. (The third scan is actually the one stored because before that time; the data from the delay lines is undetermined). On subsequent lines the data stored in the offset RAM is input to the subtrahend of the subtractor in synchronism with the operating data at the minuend. Thus, the subtractor output is the operating data with the offset removed.

2.7.2.1.3 Gain Correction. - Gain correction is the process of normalizing the gain variations of the detectors. Once the offset has been removed, the transfer function for the cells is approximately linear, so that a single multiplicative factor can be used. The digital components involved in the arithmetic operation are the gain RAM, calibration factor ROM, multiplier, and bit selector.

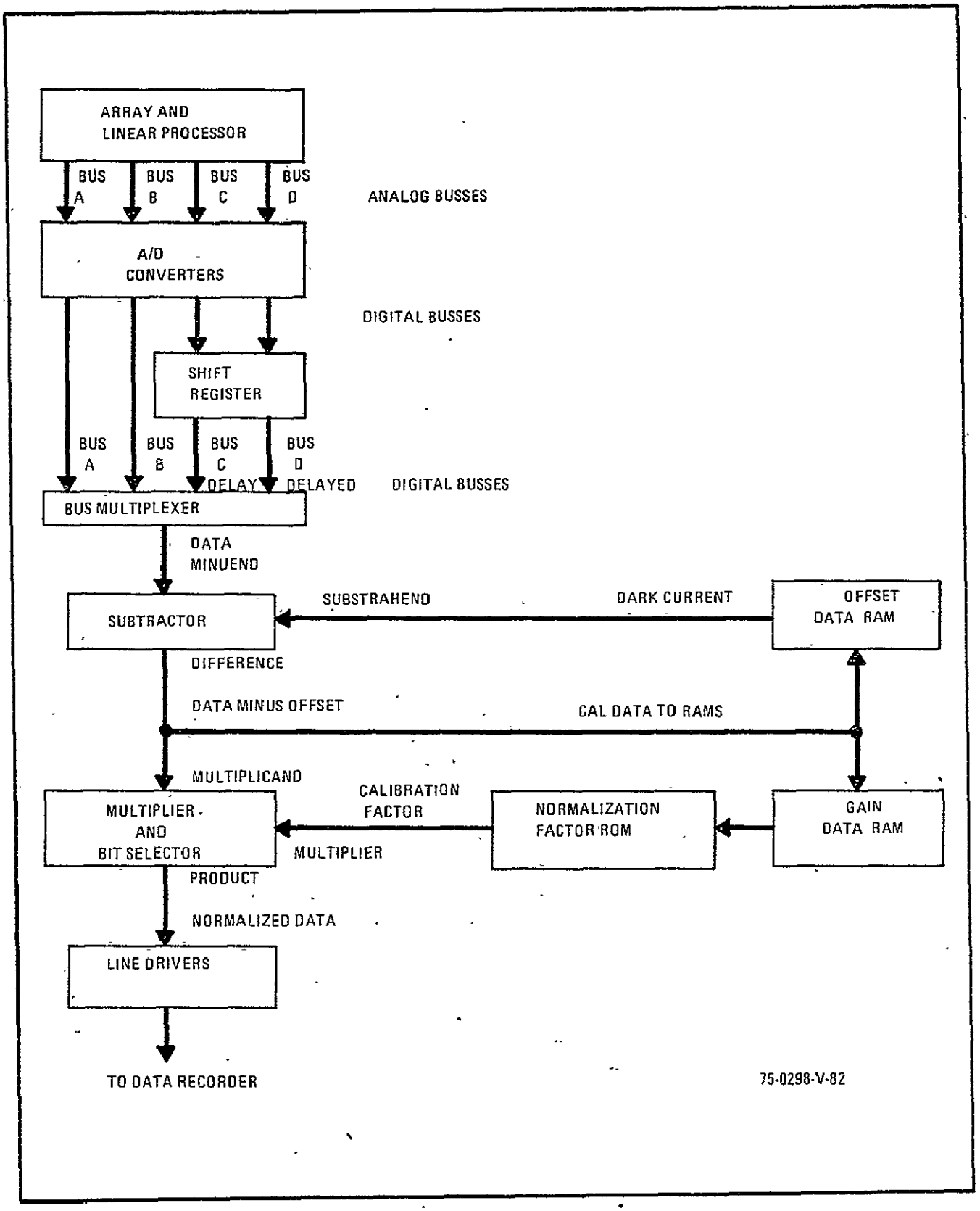

Figure 54. Arithmetic and Geometric Correction Block Diagram

To calibrate the system, the array is illuminated with one half of the maximum scene irradiance. A data point with the offset removed is stored in the gain RAM. As with the offset, the third line of data is stored. For each element, because the offset of up to one half of the dynamic range is removed, the half of maximum irradiance will produce a maximum digital output that is 25 percent of the uncorrected maximum output for the highest gain element (i. e., 63 counts). Therefore a minimum overall system gain of 2 is required in the real-time processor to make full use of the dynamic range of the digital system. An element with the lowest gain correctable by the real-time processor will produce a digital output of only eight counts with the same input irradiance.

The RAM data is used on a cell-by-cell basis for two purposes. First, it addresses the calibration factor ROM to select an appropriate multiplicative factor. Second, it controls the bit selector to select eight of the 16 bits output by the multiplier. This second function is equivalent to division and thus serves to extend the range of the multiplicative factors available.

Table 9 lists the multiplicative factors and divisors for each output. The multiplier and bit selector produce the eight-bit product of the offset corrected data and the normalizing gain factor. The data at this point, corrected for offset, gain variations, and staggered array geometry is output to the recording system in the same format as for earlier configurations.

2. 7. 2. 2 Arithmetic Mechanization

2. 7. 2. 2. 1 Subtraction. - The subtractor is required to produce the difference between two eight-bit positive binary numbers for which the minuend is larger than or equal to the subtrahend. With these restrictions on the inputs, an eight-bit adder can be used to produce an eight-bit binary difference by complementing the input (which becomes the subtrahend) and adding a one

TABLE 9

LINEAR ARRAY GAIN CORRECTION

Digitized Cell Cal Output With Offset Removed	Relative Cell Gain	ROM Cal Factor	Divisor*	Overall System Gain
0–7	0.125	–	–	Bad Elt**
8	0.125	127	8	1.98
9	0.141	113	8	1.99
10	0.156	102	8	1.99
11	0.172	92	8	1.98
12	0.188	85	8	1.99
13	0.203	78	8	1.98
14	0.219	73	8	2.00
15	0.234	68	8	1.99
16	0.250	127	16	1.98
17	0 266	120	16	1.99
18	0.281	113	16	1.99
19	0 297	107	16	1.99
20	0 313	102	16	1.99
21	0.328	97	16	1.99
22	0 344	92	16	1.98
23	0 359	88	16	1 98
24	0 375	85	16	1 99
25	0.391	81	16	1.98
26	0.406	78	16	1.98
27	0.422	75	16	1.98
28	0.438	73	16	2.00
29	0 453	70	16	1 98
30	0 469	68	16	1 99
31	0.484	66	16	2.00
32	0.500	127	32	1.98
33	0.516	123	32	1.98
34	0.531	120	32	1.99
35	0 547	116	32	1 98
36	0.563	113	32	1.99
37	0 578	110	32	1.99
38	0 594	107	32	1.99
39	0.609	104	32	1 98
40	0.625	102	32	1.99
41	0.641	99	32	1.98
42	0.656	97	32	1.99
43	0 672	95	32	1.99
44	0.688	92	32	1.98
45	0.703	90	32	1.98
46	0.718	88	32	1.98
47	0.734	87	32	2.00
48	0 750	85	32	1.99
49	0 766	83	32	1.99
50	0.781	81	32	1.98
51	0.797	80	32	1.99
52	0.813	78	32	1 98
53	0 828	77	32	1.99
54	0.844	75	32	1 98
55	0.859	74	32	1 99
56	0.875	73	32	2.00
57	0.891	71	32	1.98
58	0.906	70	32	1.98
59	0 922	69	32	1.99
60	0 938	68	32	1.99
61	0 953	67	32	2.00
62	0 969	66	32	2.00
63	0.984	65	32	2.00
64–256	1	–	32	System Saturates**

Notes

* For a divisor of 8, multiplier bits, 2^3 through 2^{10} are used. For a divisor of 16, bits 2^4 through 2^{11} are used. For a divisor of 32 bits 2^5 through 2^{12} are used.

** Elements with outputs less than 8 or greater than 63 for the cal cycle are nonworking elements.

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at the least significant bit through the carry in (creating a 2's complement[7] negative number). The input adder, and output, are eight-bit with only positive outputs required. Therefore, the subtraction uses an imaginary ninth bit as the 2's complement sign bit. With the stated restrictions, the output sign bit is always positive and therefore the ninth bit can be ignored, permitting the use of the eight-bit adder.

2.7.2.2.2 Gain. - The central circuit in the gain normalization logic is the multiplier. The multiplier used is intended to form a 16-bit 2's complement output from two eight-bit 2's complement inputs. A foreknowledge of the inputs allows the use of the 2's complement device with true binary eight-bit inputs without the added complexity of 2's complement conversion. The product also will be in true binary. The assumptions, design limitations, and mechanization are discussed in the following paragraph.

As previously asserted in paragraph 2.7.1.3, the input signal dynamic range is seven-bits after offset removal. This seven-bit number is one of the multiplier inputs. Since the MSB of the eight-bit word is not used, it will always be zero, creating a word which signifies the same magnitude in either 2's complement or true binary (e.g., 0101 is +5 in either 2's complement or true binary).

A variable divisor is achieved with a bit selector to be described shortly. The bit selector enables the use of a seven-bit ROM factor without creating too large a quantization error for small multiplicative factors. The ROM factor is an input to the multiplier as a positive number (MSB bit 8 is 0). An assumption has been made that only an 8 to 1 gain variation will be corrected.

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[7] 2's complement is a method of representing signed binary numbers in a convenient usable form. A negative number representation is formed by subtracting the absolute value of the binary number from zero with an imaginary MSB (most significant bit) for the borrow. The sign of a 2's complement binary code can be recognized as positive or negative by the most significant bit of the number (i.e., a zero indicates a positive number) More information on this or other complementary number systems can be obtained from any good logic technique handbook or textbook.

This is sufficient to meet the 3 to 1 detector variation and 2 to 1 or more error in adjusting the reference illumination.

Without the bit selector, the ROM factor range would need to be 127 (maximum from a seven-bit word) to 16. The quantization error at the low end would be one part in 16, or greater than 6 percent. With the bit selector, the minimum ROM factor is 64, giving a maximum quantization error of one part in 64, or 1.5 percent. The bit selector then changes divisors shifting the selected eight bits from the 16 bit multiplier output. The minimum overall correction factor is 2, so the maximum divisor is 32 (i.e., 64 ÷ 32 = 2). For the maximum correction of approximately 16, the divisor is 8 (127 ÷ 8 = 15.9). The intermediate divisor of 16 is also used to maintain continuity.

An example of the gain correction function using the multiplier and bit selection is shown in figure 55. Table 9 presents the parameters associated with the gain correction factor for each possible detector gain. Note that, throughout the 8 to 1 correction range, the maximum error contributed by the correction algorithm is 1 percent.

2.7.2.2.3 Additional Processing by the Real-Time Correction Circuit. - Elements with low gain (calibration cycle output less than 8) are considered nonfunctional. These elements are flagged in the data by forcing the output to a full scale count of 255. These elements then can be recognized easily and smoothed by subsequent computer processing.

For very low levels of illumination, noise may make the subtrahend for the subtractor exceed the minuend. This is incompatible with the data handling scheme, but it is circumvented by forcing the output to zero when the "carryout" is a one, indicating a negative number.

2.7.3 Test Results

The primary objective of the linear array imager is the generation of high quality imagery. Since all objective measurements of array parameters were made during the earlier phases of this program, most of this phase was devoted to producing and analyzing the imagery. Figure 56 illustrates the results.

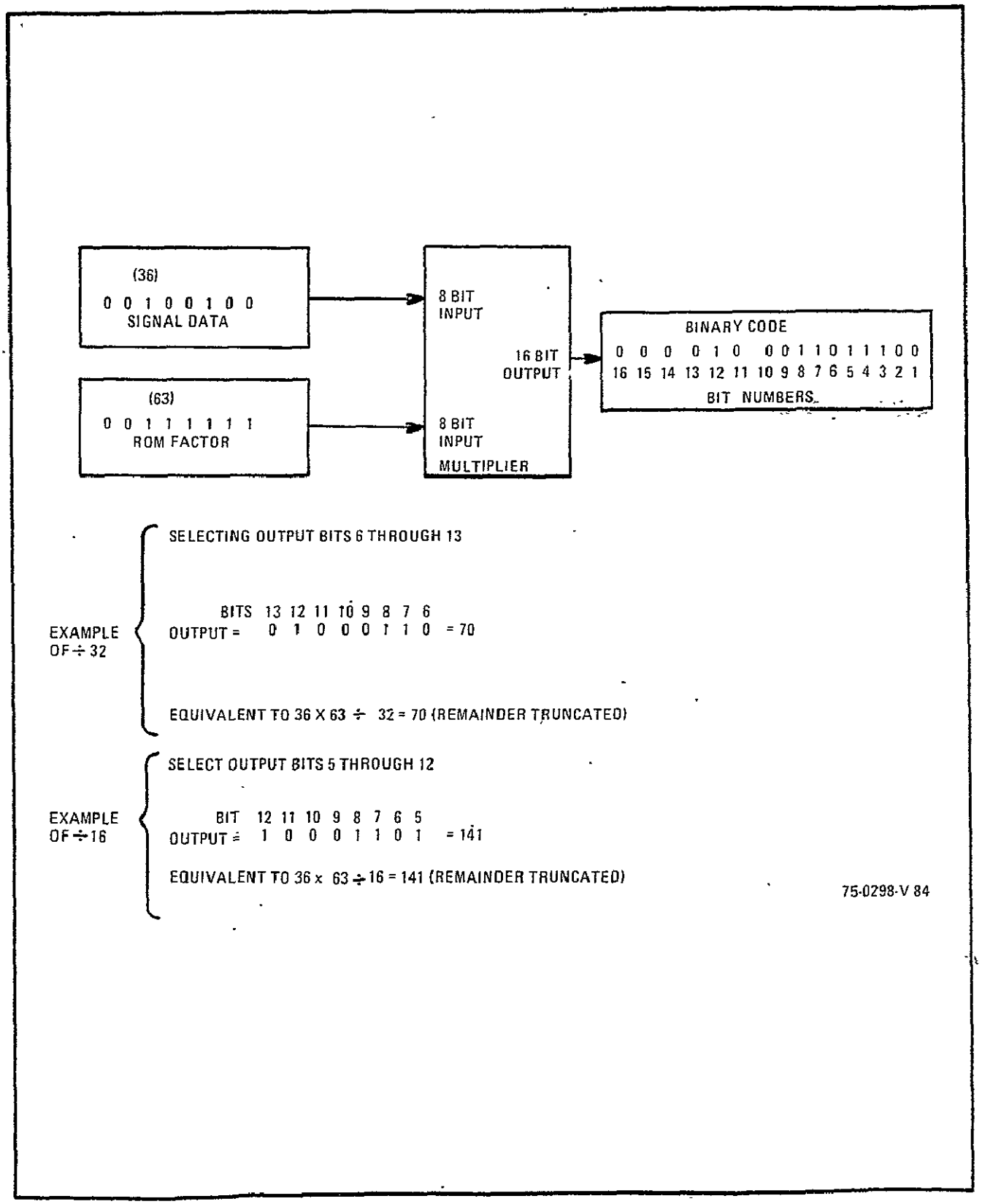
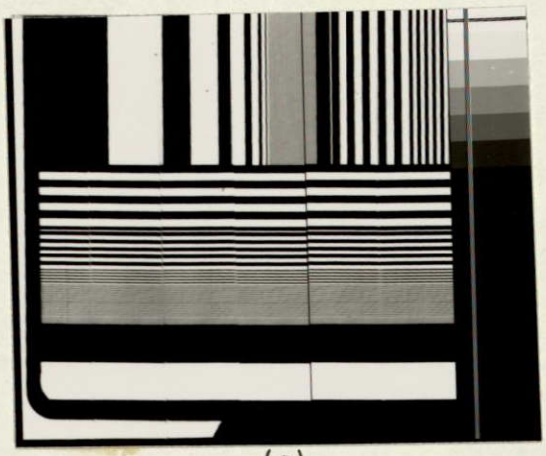
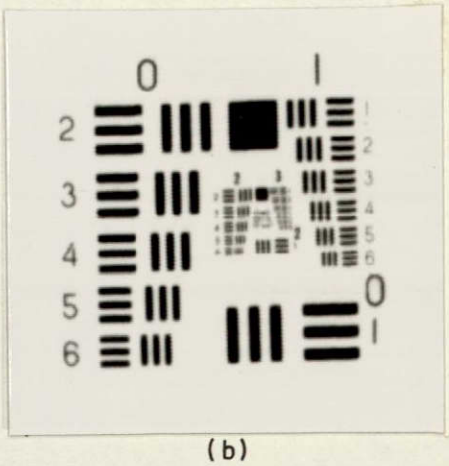


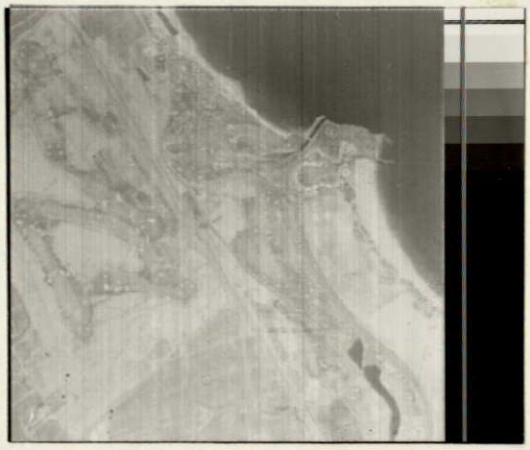
Figure 55. Gain Correction Function



(a)



(b)



(c)

(d)

(e)

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Figure 56. Imaging Test Results

The bar targets, such as are shown in figure 56a, provide an objective view of the real-time processor operation. Note that there is no streaking due to offset and gain. Image artifacts are similar to those seen in figure 37, made previously by using a general purpose computer to perform the processing. The resolution is excellent with f_o (Nyquist sampling limit frequency) bars easily detected, as well as the effects of element phasing relative to those bars. Two times f_o is the highest frequency bars, and it appears as a gray area (between the lower and middle quarter of the picture). The geometric correction to remove the element stagger has been performed correctly, as shown by the clean line edges. An uncorrected scene would appear similar to the upper edge of the image (first two scan lines) as a distinct black and white comb effect.

Figure 56b is the USAF 1951 standard resolution chart confirming the results of the prior bar chart. This shows that bars up to group 2, target 5, are readily discernible. Factoring in the optical magnification, that represents a frequency of 36.9 lp/mm. The sampling frequency of the detector is 32.8 lp/mm. This indicates that the system MTF is very close of the theoretical value (see figure 30), being limited by the array itself.

Some typical scenes were run as shown in figures 56c, 56d, and 56e. The scenes of parts c and d were of very low contrast; therefore figure 56c was enhanced by additional computer processing. As expected, the enhancement of the scene also increased the streaking effects. Scenes d and e also show low level streaking as expected (see paragraph 2.7.1.3). As can be seen from figure 56d, the streaks are much more apparent in constant level type scenes. In figure 56e the streaking is not as obvious, but it can be seen in the fields and roadway. The wider discontinuities are not noise contributed streaks, but rather are nonworking detectors within the 576 element array that have been smoothed by the computer. It should be noted that, although these scenes used a 256 level input (eight-bit digital), the output could have been transmitted as 64 level (six-bit) data with no visible loss of information, as mentioned in paragraph 2.7.1.1.

2.7.4 Conclusion on Real-Time Processing

It can be seen from the images generated that real-time processing will provide high quality imagery. The advantage of this technique is that there is a significant reduction in ground data processing complexity. The disadvantage is that additional electronics complexity is required in potential spacecraft sensor applications. For future applications, the tradeoff between simplified ground data processing and more complex onboard processing must be given careful attention.

APPENDIX A

MTF COMPARISON FOR IDEAL SYSTEM

Throughout the text, several MTF measurements have been presented. The data presented is for non-diffraction limited optical systems and square-wave targets at f/4.7 and f/12.8. It is considered of interest to include (in this appendix) theoretical MTF for diffraction limited optics and theoretical detector response. Figure 57 compares the diffraction limited MTF (sine-wave) of an f/4 and f/2 optical system. Figure 58 presents the ideal square-wave response of the detector (along scan) and the system MTF for various lens parameters. The detector corner frequency relationship (on the normalized frequency scale) is detector center spacing/detector linear dimension in direction of MTF.

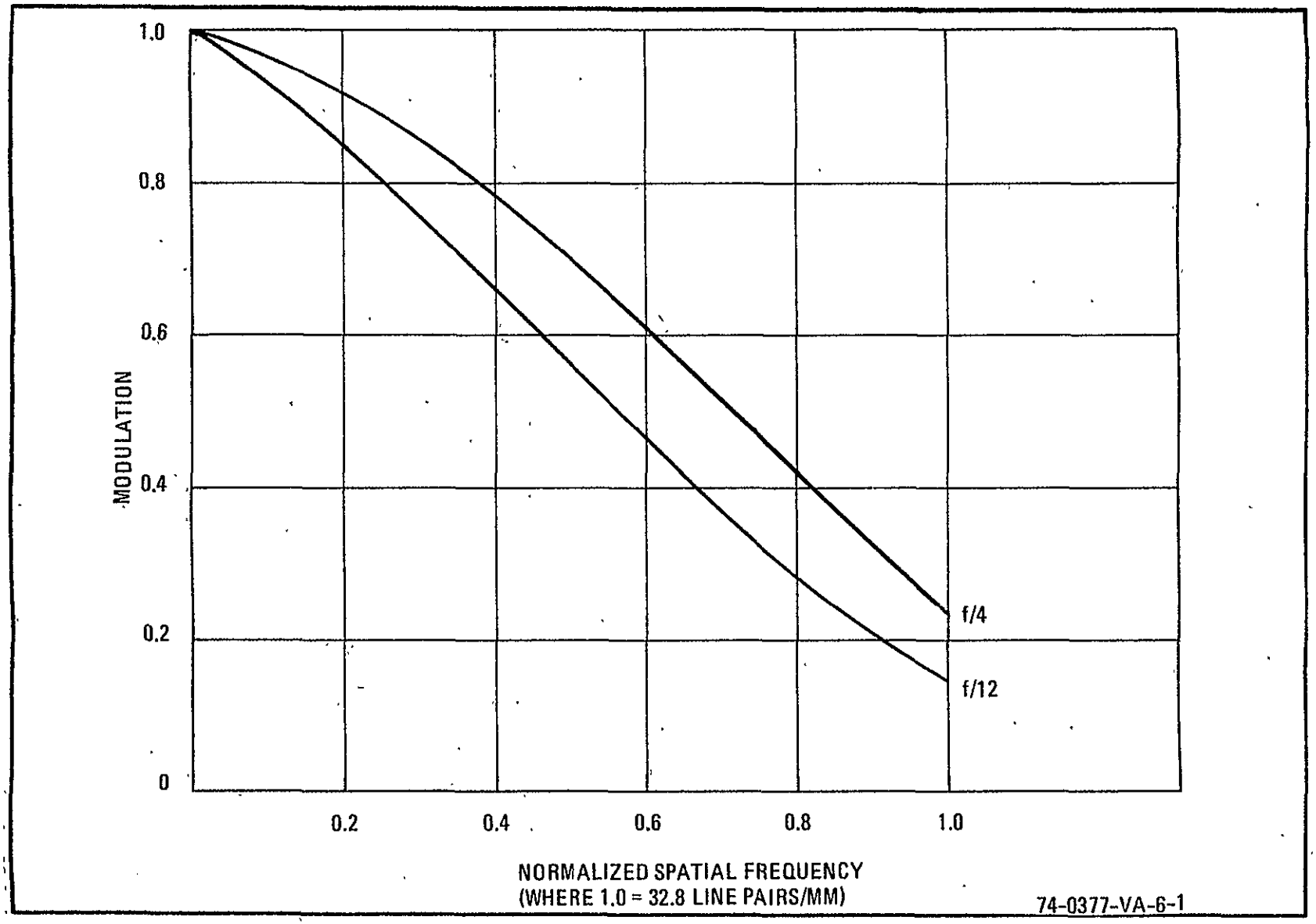

Figure 57. Comparative MTF with f/4 and f/12 Optics for $\lambda = 1.0$ μm

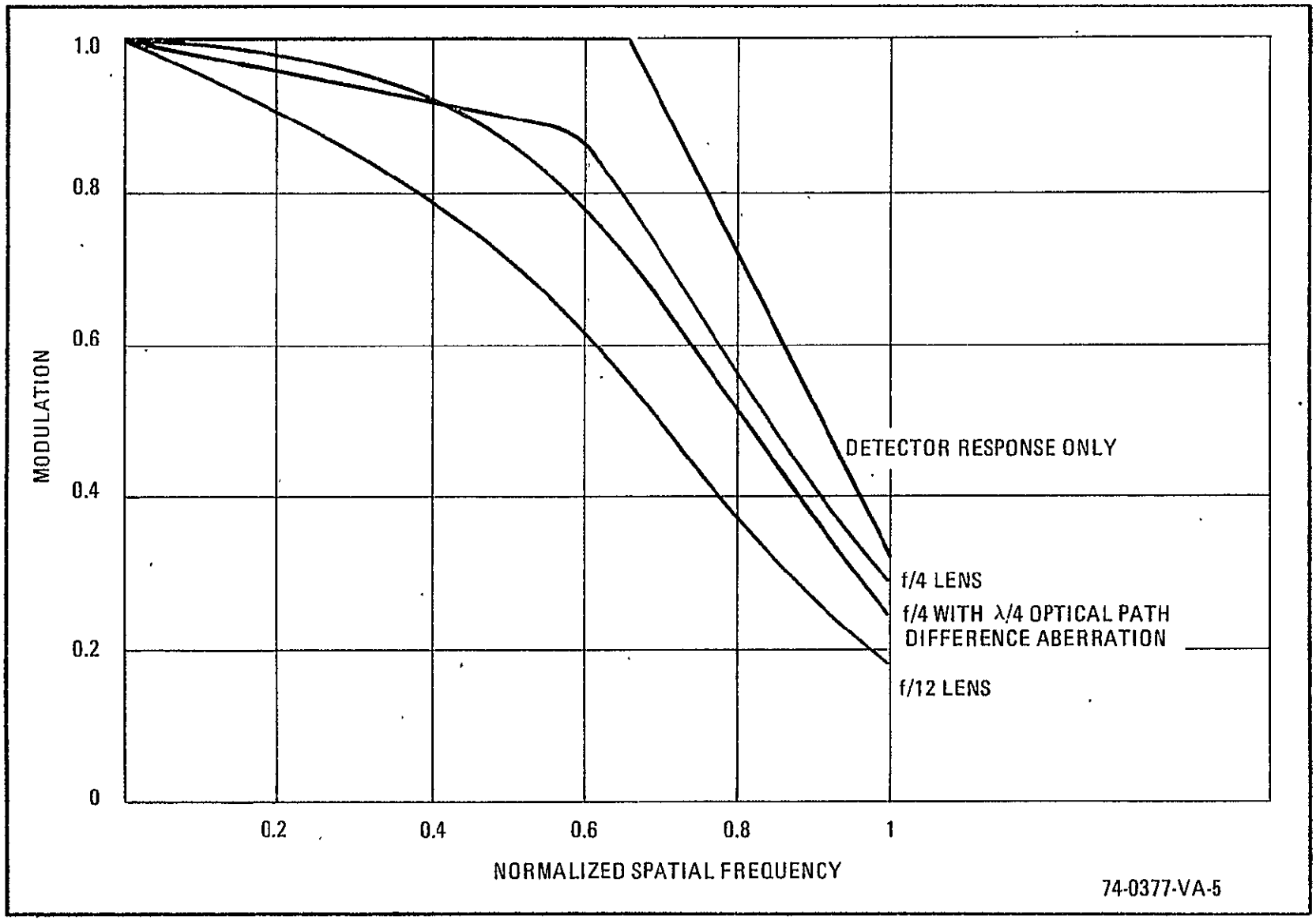

Figure 58. Comparative MTF Response to Squarewave Input

APPENDIX B

BREADBOARD LINEAR ARRAY SCAN IMAGER NOISE PROGRAM

A computer program was written to process the linear array data and provide a rms noise output. The listing of the program is included in figure 59.

This program collects 576 samples from each detector element at each of two input radiance levels. These inputs are averaged to provide a gain measurement for each element. The rms deviation from the average is calculated for each element and referred to the input using the measured gain factor. A composite noise level is also determined. For the composite value, nonoperable elements are not included.

An additional feature of the noise program is to generate the quantization noise uncertainty for each element. This value is also referred to input irradiance.

APPENDIX C

FAILURE ANALYSIS OF A WESTINGHOUSE PHOTODIODE ARRAY INTEGRATED CIRCUIT

This appendix is a failure analysis report performed by the NASA Goddard Space Flight Center on a 96-element photodiode detector array. Figure 60 is a copy of a Failure Analysis Report; figures 61 and 62 are micrographs.

GODDARD SPACE FLIGHT CENTER

FAILURE ANALYSIS SECTION TERMINATION REPORT

Serial No. 2979

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TASK DESCRIPTION (BRIEF)			PROJECT NAME
Failure analysis of one Westinghouse Electric Corporation photodiode array integrated circuit.			SRT JOB ORDER NO. 311-160-20-53-40 REQUESTED BY L. Thompson (731) INITIATED DATE 6/6/73
REPORTED BY (INVESTIGATOR) M. Baluck	DATE	MANHOURS THIS PERIOD	COMPLETION DATE (ASSIGNED) 7/11/73
GROUP LEADER	DATE	MANHOURS TOTAL 90	SUBMISSION DATE 7/27/73
SUPERVISOR R. Grant	DATE	STATUS ☐ TESTING ☐ DATA ANALYSIS ☐ REPORT IN PROCESS	

A Westinghouse Electric Corporation custom photodiode array integrated circuit (SN A14) failed during system tests of an SRT linear sensor circuit at Westinghouse Electric Corp., Baltimore, Maryland. It was reported that the shift register stage in one of the two halves of the die had an output which remained in a constant "logic 1" state. The integrated circuit was submitted to the GSFC Failure Analysis Laboratory for investigation.

The subject device (Figure 1) is a multilayer, silicon, monolithic integrated circuit. The center portion of the die contains an array of 96 photodiode light sensors. This array is flanked on each side by an MOS electronic section which contains 24 shift register stages, 24 AND gates, and 48 amplifiers. (The dimensions of the die are 1.47 millimeters (mm) (58 mils) x 5.33 mm (210 mils)). There are three layers of aluminum contact metallization which are separated by insulating oxide layers. The die surface is covered with a protective overlay. Gold wires are used for interconnecting to the die metallization.

REVIEWED BY	DATE	REPORT ISSUED

310-14 (7/71)

PROJECT MANAGER — COPY NO. 5

75-0298-VA-43

Figure 60. Failure Analysis Report (Sheet 1)

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The submitted die, which was bonded to a gold sheet, was received mounted on a stainless steel block with non-conductive epoxy. It was not housed within a package. There were no identification markings on the die. The interconnection wires had been severed, presumably when the device was removed from the failed circuit.

The submitted integrated circuit was manufactured by Westinghouse Electric Corporation, Advanced Technology Laboratory, Baltimore, Maryland. The device was not screened or incoming tested.

No functional electrical tests could be performed because all the intercomnection wires had been severed.

An examination of the die surface using an optical microscope disclosed two anomalies in the failed half of the die: a severe scrape in a metallization stripe associated with the "Φ_4 shift" bonding pad and one dark region on the die surface where some of the metallization stripes appeared to be irregular.

Pin-to-pin electrical tests of both the good and failed halves of the die surface were performed using a micromanipulator in conjunction with a curve tracer. These tests showed that the B^- power supply pin associated with the failed half of the die was open-circuited. No other serious anomalies were detected.

The die surface was examined using a scanning-electron microscope. It was observed that the scrape in the "Φ_4 shift" metallization stripe previously mentioned had nearly open-circuited this stripe. There were only small filaments of aluminum maintaining continuity (Figure 2a). This scrape appeared to have resulted during probing of the bonding pads by the manufacturer.

The region of the irregular appearing metallization stripes noted earlier was examined more closely. This examination disclosed that several of the stripes had been smeared (apparently during manufacturing) and that two of the stripes were open-circuited. One of these stripes was common with ground and the other was common with the B^- supply. In addition, there was a small portion of apparently melted aluminum

310-14A (7/71)

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75-0298-VA-44

Figure 60. Failure Analysis Report (Sheet 2)

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at the site of the open-circuited metallization stripes (Figure 2b).

(The open circuit in the B⁻ supply metallization isolated this pin from all the other pins and accounted for the pin-to-pin electrical test results. The open circuit in the ground metallization apparently isolated this pin from some, but not all of its normal connections. This explains why this pin was not open-circuited during pin-to-pin tests.)

Electrical probing of the B⁻ metallization (beyond the point of the open circuit) disclosed that this metallization was short-circuited to several other points including ground. Because of the damage to the die, it was not possible to determine whether or not these short circuits contributed to or resulted from the failure.

Removal of the various metallization and insulating oxide layers and additional SEM examinations did not reveal any further anomalies.

Conclusions

Although no functional tests could be performed in an attempt to reproduce the exact reported failure, the investigation of the submitted integrated circuit disclosed an anomaly which would explain why the failed half of the die would not function. The B⁻ supply line was completely open-circuited and the ground line was open-circuited from some of its normal connections. Based upon the melted aluminum detected at the site of these open circuits, it is concluded that the damage resulted from an electrical stress. However, it should be noted that these open-circuited stripes had been smeared initially during manufacturing. It is possible that this smearing either reduced the cross-sectional area (and consequently, the current handling capability) of the metallization or damaged the underlying insulating oxide between metallization layers (permitting a short circuit between metallization layers to occur). These factors may have permitted the failure to occur under normal electrical conditions.

The scrape detected in the "ϕ_4 shift" metallization stripe is considered to be a serious reliability hazard. This damage can result in an open circuit or a short circuit between metallization layers and cause a catastrophic failure.

Figure 60. Failure Analysis Report (Sheet 3)

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Due to the complexity of the multilayer construction and the high density of the die in submitted part type, it is recommended that in the future, similar parts be subjected to stringent internal microscopic examinations to eliminate devices containing defects such as serious metallization scrapes and smears. In addition, all devices being considered for use in GSFC high-reliability applications should be screened and incoming tested.

310-14A (7/71)

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75-0298-VA-46

Figure 60. Failure Analysis Report (Sheet 4)

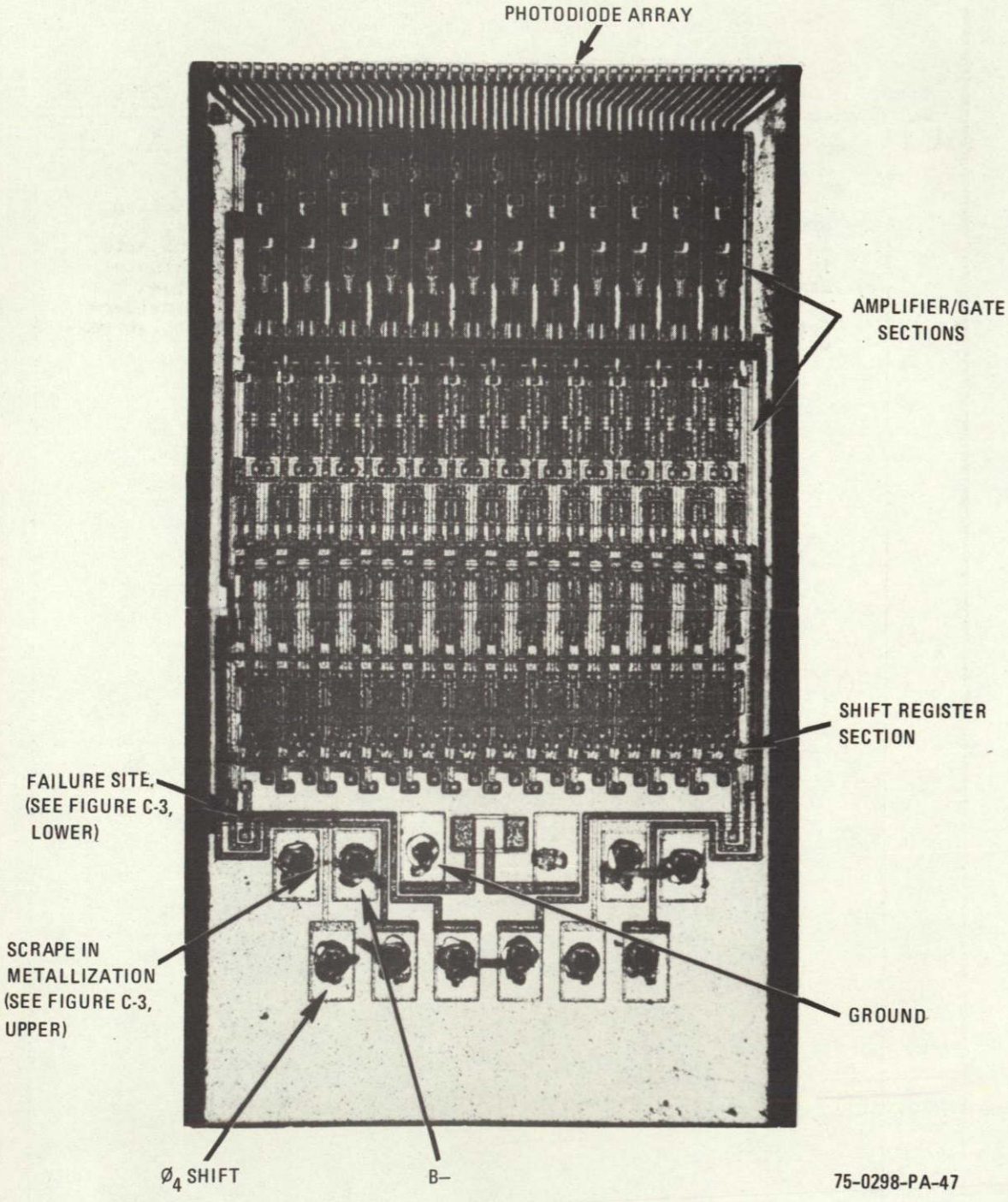
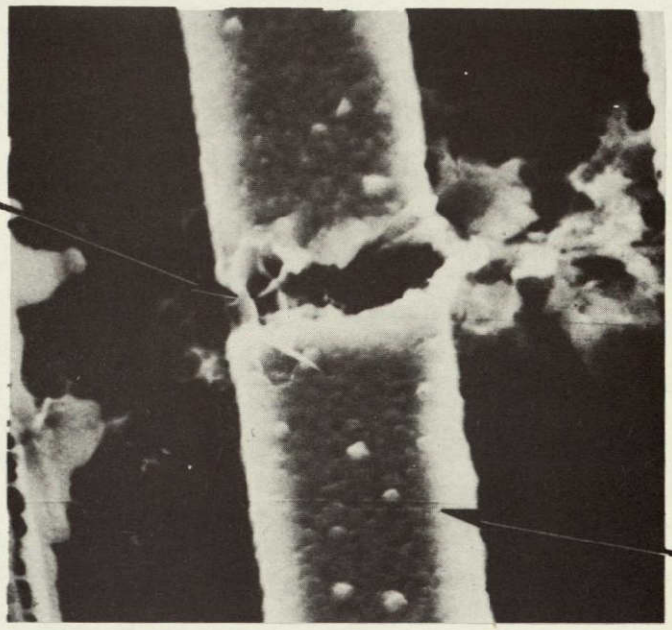
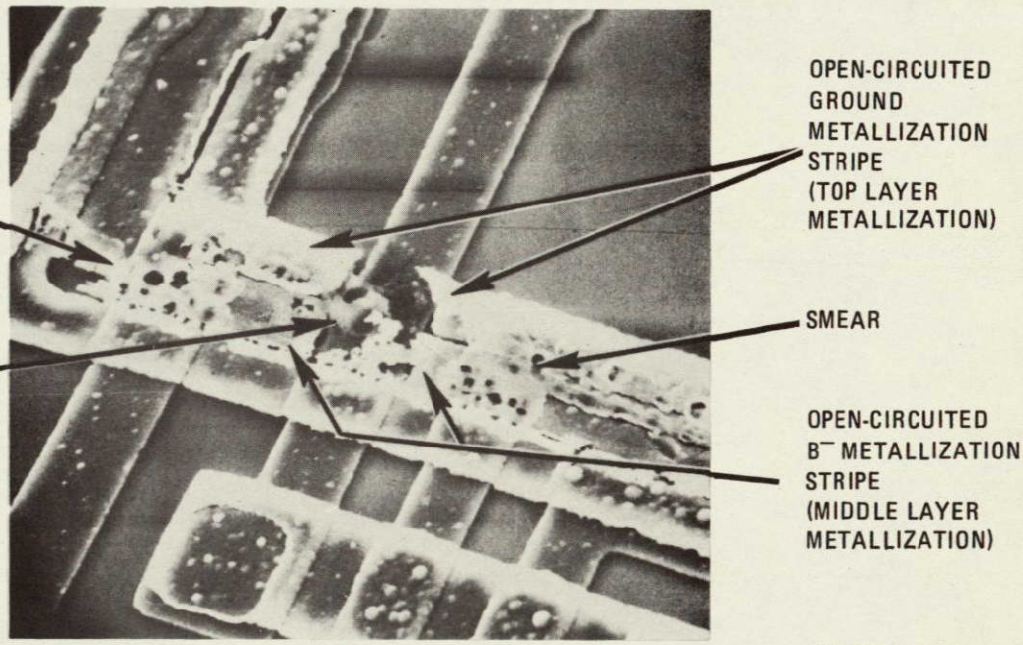


Figure 61. Failed Half of Silicon Die of Submitted Westinghouse Integrated Circuit - 65 X Magnification



SCRAPE IN "$\emptyset_4$ SHIFT" METALLIZATION STRIPE. 1200X



FAILURE SITE 800X

75-0298-PA-48

Figure 62. Scanning Electron Micrographs of Anomalies Detected in Submitted Device

APPENDIX D

WESTINGHOUSE FAILURE ANALYSIS REPORT ON FOUR PHOTODIODE LINEAR ARRAY CHIPS (NAS 5-21806)

MICROANALYSIS REPORT #451

February 7, 1957

SUBJECT: The Westinghouse Failure Analysis Laboratory was authorized to perform a failure analysis of four 96-detector element photodiode linear arrays. The chips were removed from the 18-chip array developed under NASA contract NAS 5-21806, Breadboard Linear Array Scan Imager. The purpose of the failure analysis was to determine the probable nature of failures which occurred during system level testing.

PROBLEM: Four (4) photodiode chips were submitted for failure analysis with the following comments:

Chip 5 (229-9-68)

Alpha side - phase B shorted to GND since initial turn on

Beta side - Bus C shorted to GND after 2 to 3 months of operation

Chip 9 (262-7-35)

Beta side - Bus B shorted to GND since initial turn on

Chip 10 (237-9B-38)

Beta side - V_R shorted to GND since initial turn on

Chip 14 (262-4-6)

Alpha side - Bus A shorted to GND since initial turn on

RESULTS OF ANALYSIS

The procedure used in this analysis was to mount the chips in 40 pin dual-in-line packages (for ease in handling), verify the shorts electrically, and trace the shorted bus lines to intersections with GND areas to search for possible physical damage.

Chip 5 - No shorts to GND were found on either side of this chip. Figures 63 and 64 show scratches in the third metal shield.

Chip 9 - No shorts to GND were found on the beta side. On the alpha side phase B, B^-, and bus B were all shorted to GND. Figure 65 shows phase B, B^-, and GND along with smeared metal from Pad B^- intersecting all three (3) lines. (GND is third metal, B^- and phase B are second metal lines.) Figure 66 shows a scratch in the third metal GND shield over the second metal bus B line. Figure 67 shows scratches in the third metal shield on the beta side (one scratch is over the second metal bus B line).

Chip 10 - The V_R line was found shorted to GND on the beta side. Figures 68 and 69 show scratches in the third metal GND shield over the second metal V_R line.

Chip 14 - Output bus A was found shorted to GND on the alpha side. Figure 70 shows scratches in the third metal GND shield over the second metal bus A line.

CONCLUSIONS

The shorts found on chips 9, 10, and 14 were low resistance shorts (10 ohms). Based on previous work with chips of this type, these shorts were probably caused by physical damage which breaks through the layer of glass separating third and second metal. Shorting of these metal layers usually results. The B^- and phase B shorts to GND were probably caused by physical damage at the time of bond removal, as suggested by figure 66.

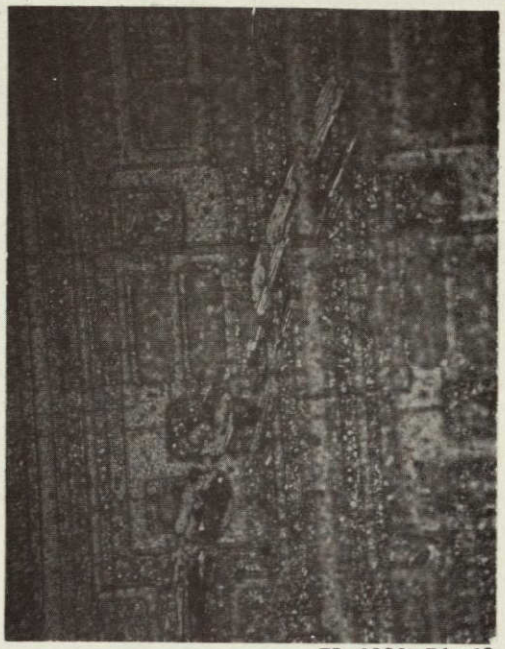


Figure 63. Scratches in the Third Metal Shield

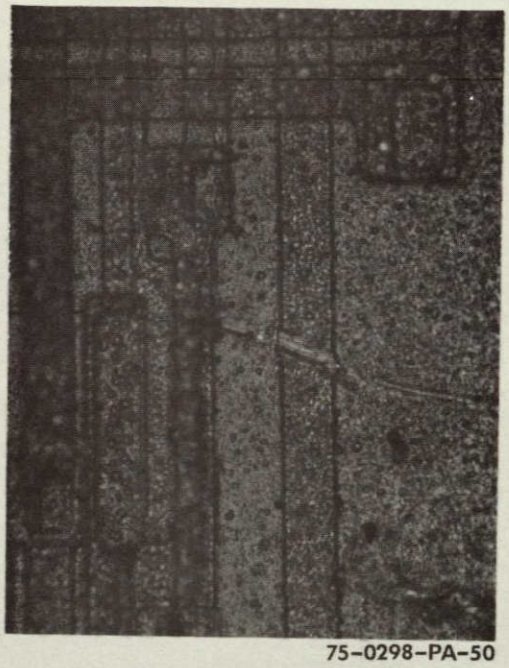


Figure 64. Scratches in the Third Metal Shield

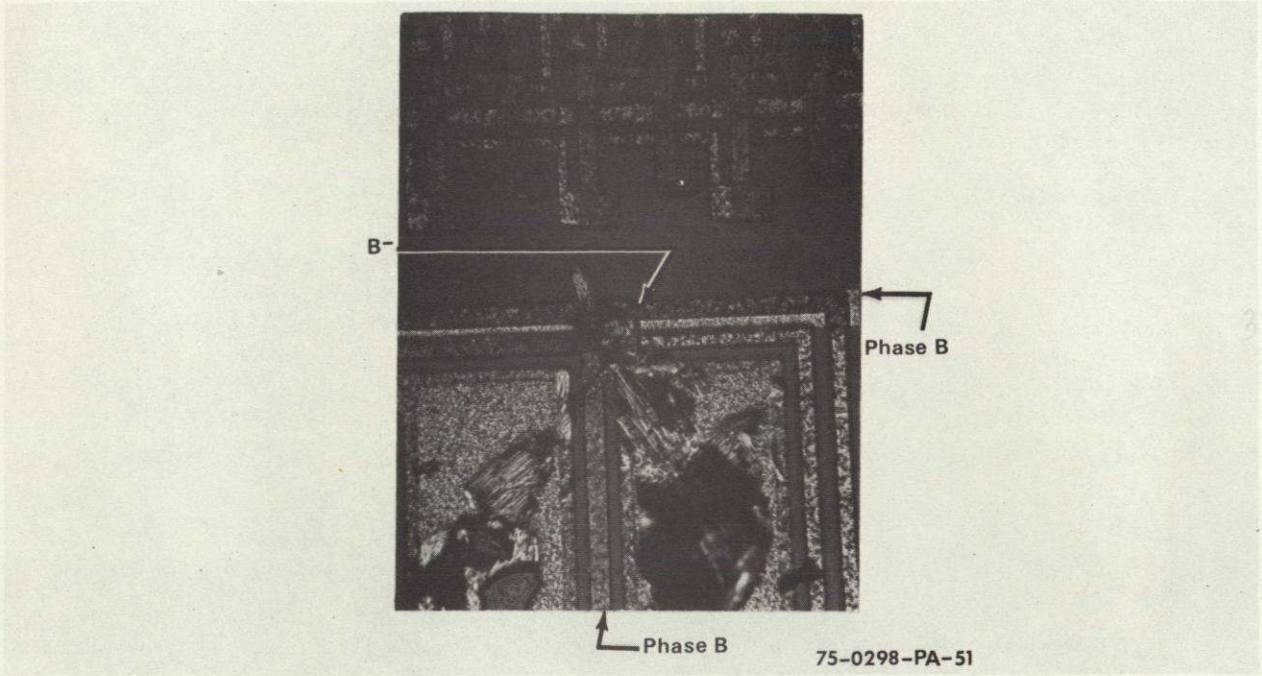


Figure 65. This Photo Shows a Scratch Causing Phase B, B⁻, and Bus B all Shorted to Ground and Smeared Metal from Pad B⁻ Intersecting all Three Lines

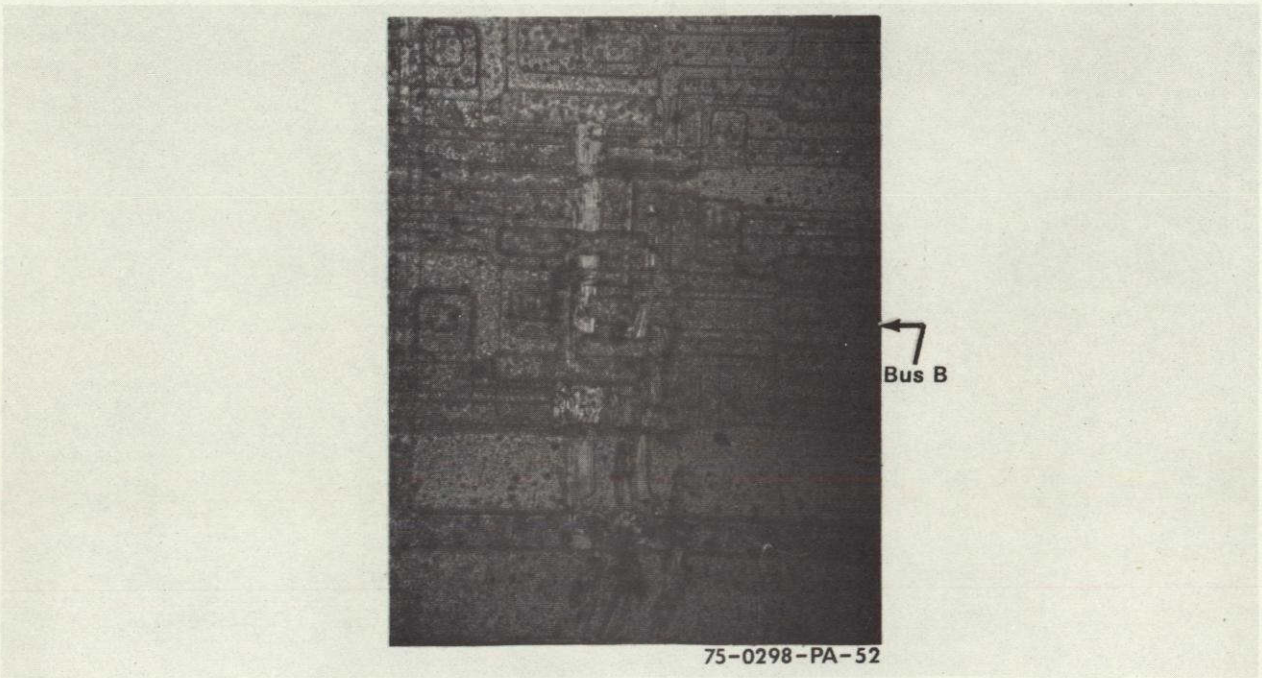


Figure 66. This Photo Shows a Scratch in the Third Metal GND Shield

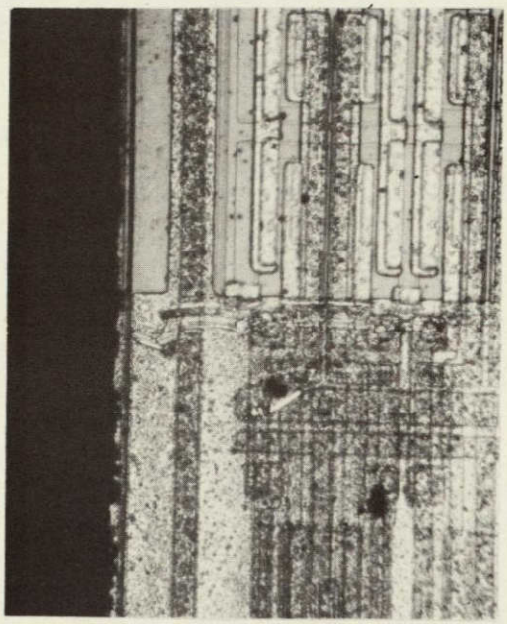


Figure 67. This Photo Shows Scratches in the Third Metal Shield on the Beta Side

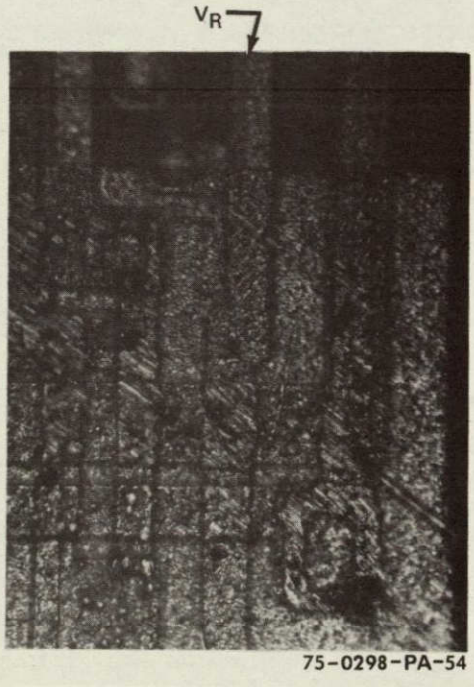


Figure 68. This Photo Shows Scratches in the Third Metal GND Shield Over the Second Metal V_R Line

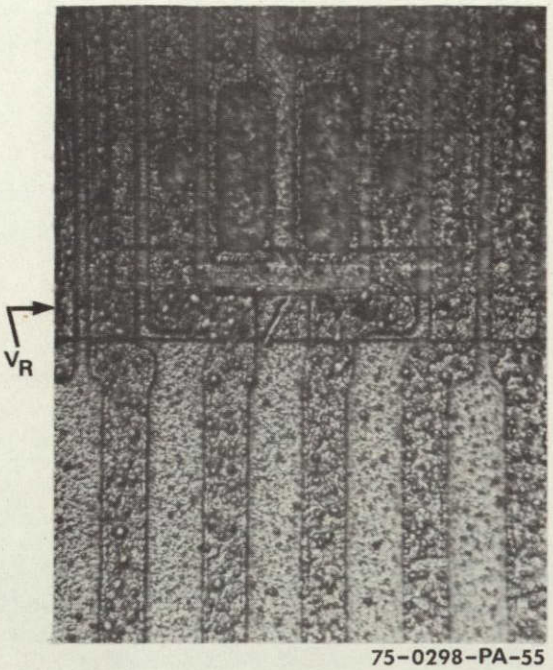


Figure 69. Shows Scratch in Third Metal GND Shield Over the Second Metal V_R Line

Figure 70. Shows Scratches in the Third Metal GND Shield Over the Second Metal Bus A Line

The information received with chip 9 may have been mislabeled since the bus B short was found on the alpha side. Although no electrical shorts were found on chip 5, scratches were found on the third metal shield. Heating these chips during the mounting process may have caused previously shorted intraconnects to open.

Although laser debris can be seen (by a skilled observer) in several photographs, the debris is not considered a source of scratches.

APPENDIX E

COMPUTER PROCESSING OF PHOTODIODE LINEAR ARRAY DATA

This appendix describes the use of the computer in processing image data on the breadboard program.

The computer has two primary functions in this program - reordering of the staggered geometry and normalizing the data. During the data manipulation, other capabilities of the computer were also used for image cosmetics and data analysis. Although the listing in figure 71 is lengthy, the actual function is not complex as can be seen with the simplified flow diagram in figure 72. The following paragraphs provide a more informative description of the computer functions.

The first information entered into the computer is the calibration data. These are array outputs for each element at five predetermined radiance levels. A total of 576 samples are run for each element at each level. The computer averages these samples and stores the results for use in normalizing the picture data. While reading the tape data, the computer also smooths malfunctioning elements by averaging between the two adjacent elements.

The next step is for the computer to read and store the image data. During the reading of this data, the malfunctioning elements are also removed by adjacent element averaging. Two 576 element data lines are read into the computer per tape access. The even numbered elements are stored for one tape access interval and then placed into the storage array with the data from the odd numbered elements read during the next interval forming a 576-element line. This removes the two pixel delay (across scan) inherent

in the staggered photodiode array. The elemental data values are compared to the calibration data and, by interpolation between the nearest higher and lower calibration values, normalized to a range of 0 to 255. A total of 1,728 lines of normalized data from each 6-chip section are accumulated in a drum storage area until the scene data from all three sections have been read.

The final step of a scene data process is to retrieve the data from the drum to form a single 1,728-element data line. Values equivalent to each of the five calibration levels are added to the data lines. This data is recorded on a magnetic tape for playback on a film recorder.

Another benefit obtained from the computer usage was the obtaining of noise calculations. The same scene software was used except the scene processing was removed and an rms routine inserted. The rms deviation from the average level was calculated using 557 samples. This rms value was normalized to the 0 to 255 range for easy comparison to the signal levels. An rms value was then printed for each of the 1,728 elements.

The computer was also used to obtain a comparison of temperature data. This was a simple plotting routine using the peripheral plotter. Room temperature and 0°C plots were made of the dark level for the 6-chip array. The effects of temperature become readily apparent with the plotted data.

APPENDIX F

DETECTOR TEMPERATURE TEST RESULTS

The data shown plotted in figure 73 is the measured dark level at +22°C and 0°C using five bilinear staggered chips. Only the chip temperature was varied. Each data point is the average of 576 samples. The channel gain is 2.3 digital counts/mW/m^2. The plots show that at 0°C, a significant (≈ factor of 4) reduction of the peak-to-peak difference in elemental offsets occurs. This means that less of the dynamic range needs to be reserved for transmitting offsets. It also reduces the temperature sensitivity allowing coarser temperature control requirements.

APPENDIX G

TEMPORAL TEST

A rigorous test for temporal stability has not been performed, therefore no conclusion about time related drifts can be made. However, measurements of offset in the room ambient environment were conducted over a 3-month period during which the baseplate temperature was monitored. Some of these results are plotted in figures 74 through 78.

Figure 74 data was taken over a period of 35 minutes with an initial measurement made, one at 20 minutes and one at 35 minutes. Although during this period the level changed, it was accompanied by a temperature change of 2.2° C. The magnitude and polarity of the change are consistent with the change in temperature. The average change is only 6 $\mu J/m^2$ equivalent input which indicates that, if a short term temporal change occurred, its magnitude is very low and undetectable with the 1.4 $\mu J/m^2$ NEI.

A longer temporal run three runs over a 2-month period is shown in figures 75 through 78. These again show variations attributable to the ambient temperature differences with little change in the general level. There is again no evidence of a temporal drift.

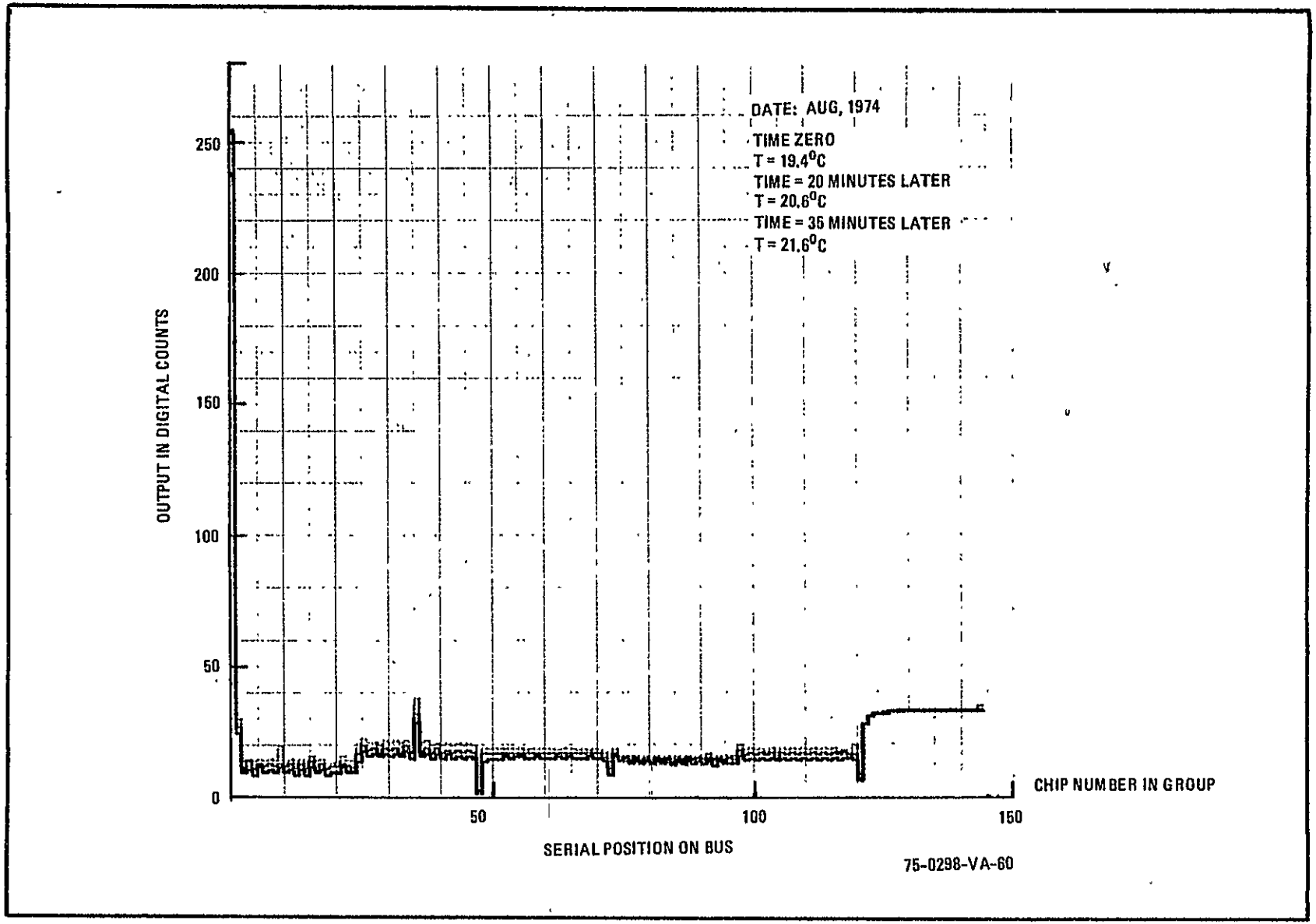


Figure 74. Output at Dark vs Time and Temperature
Six Chip Array - Bus A

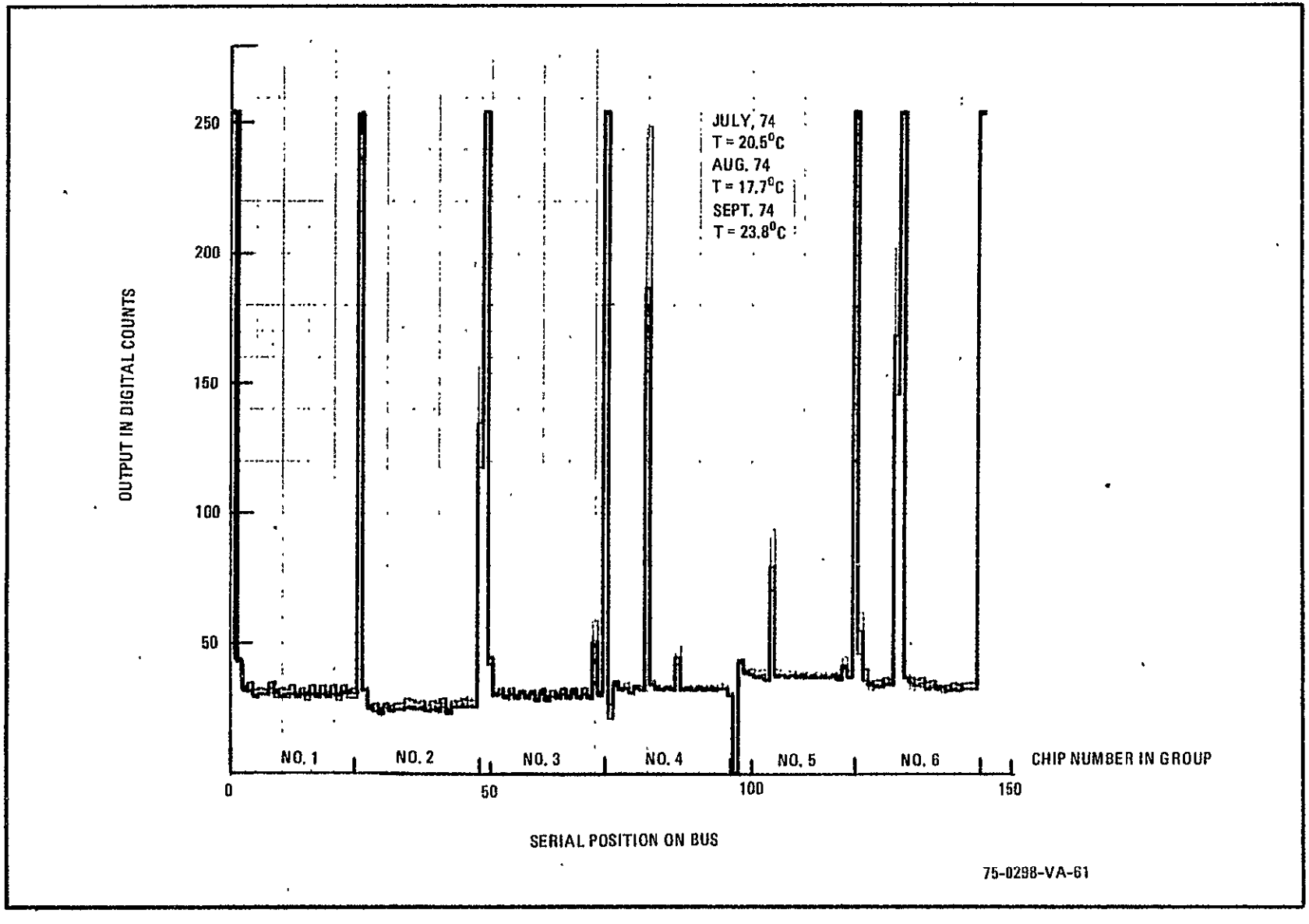


Figure 75. Output at Dark vs Time and Temperature
Bus A of Group 2

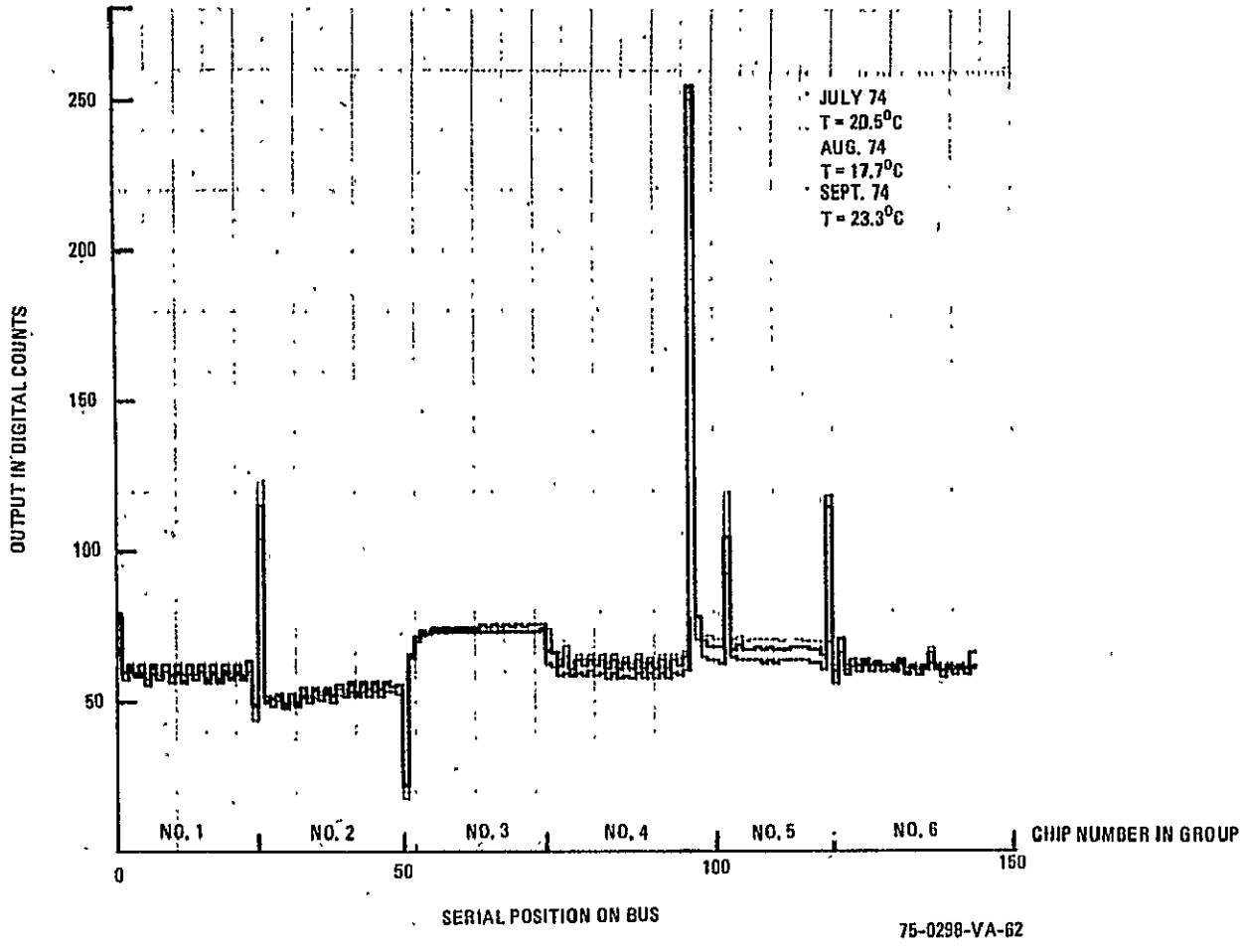


Figure 76. Output at Dark vs Time and Temperature
Bus B of Group 2

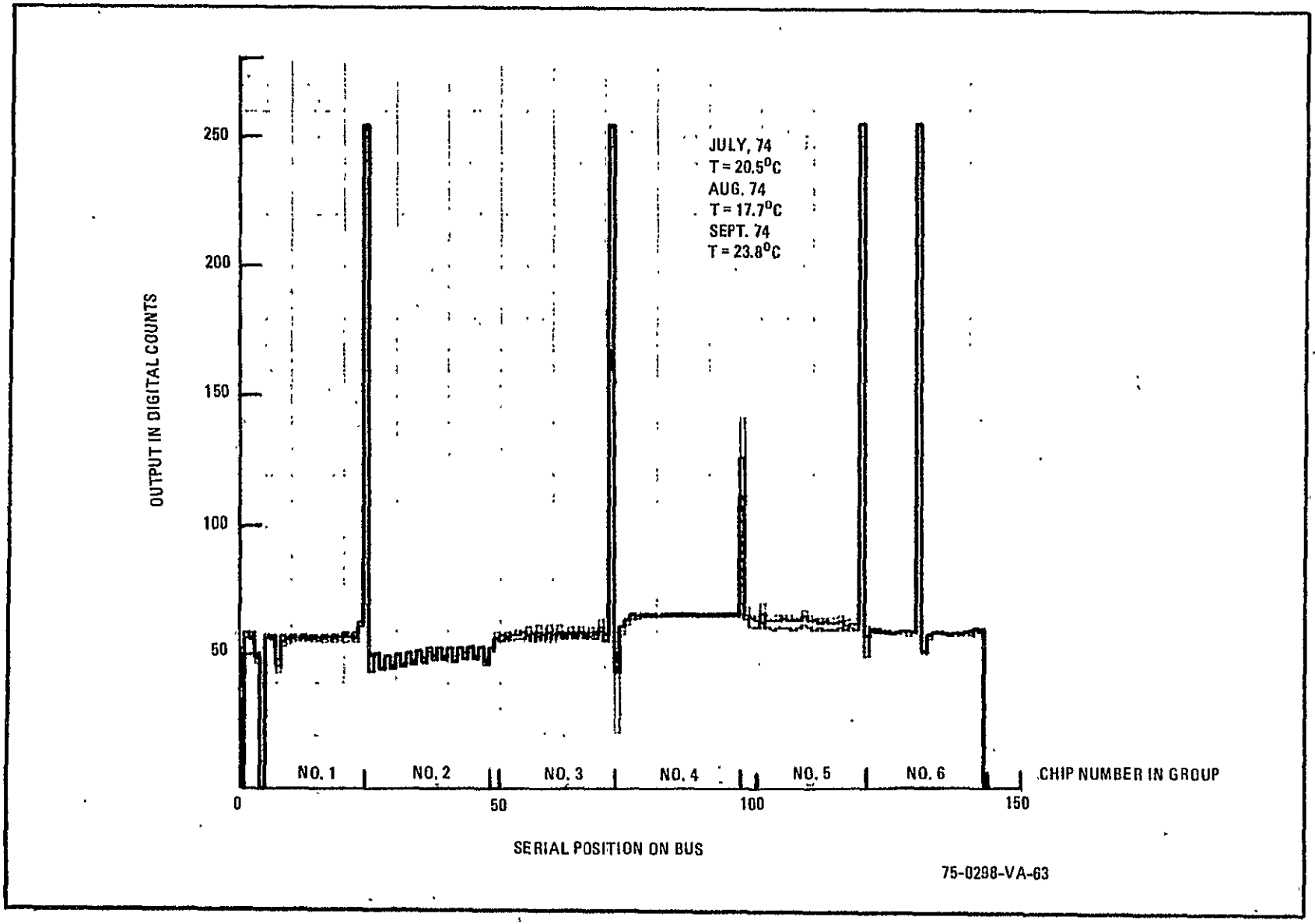


Figure 77. Output at Dark vs Time and Temperature
Bus C of Group 2

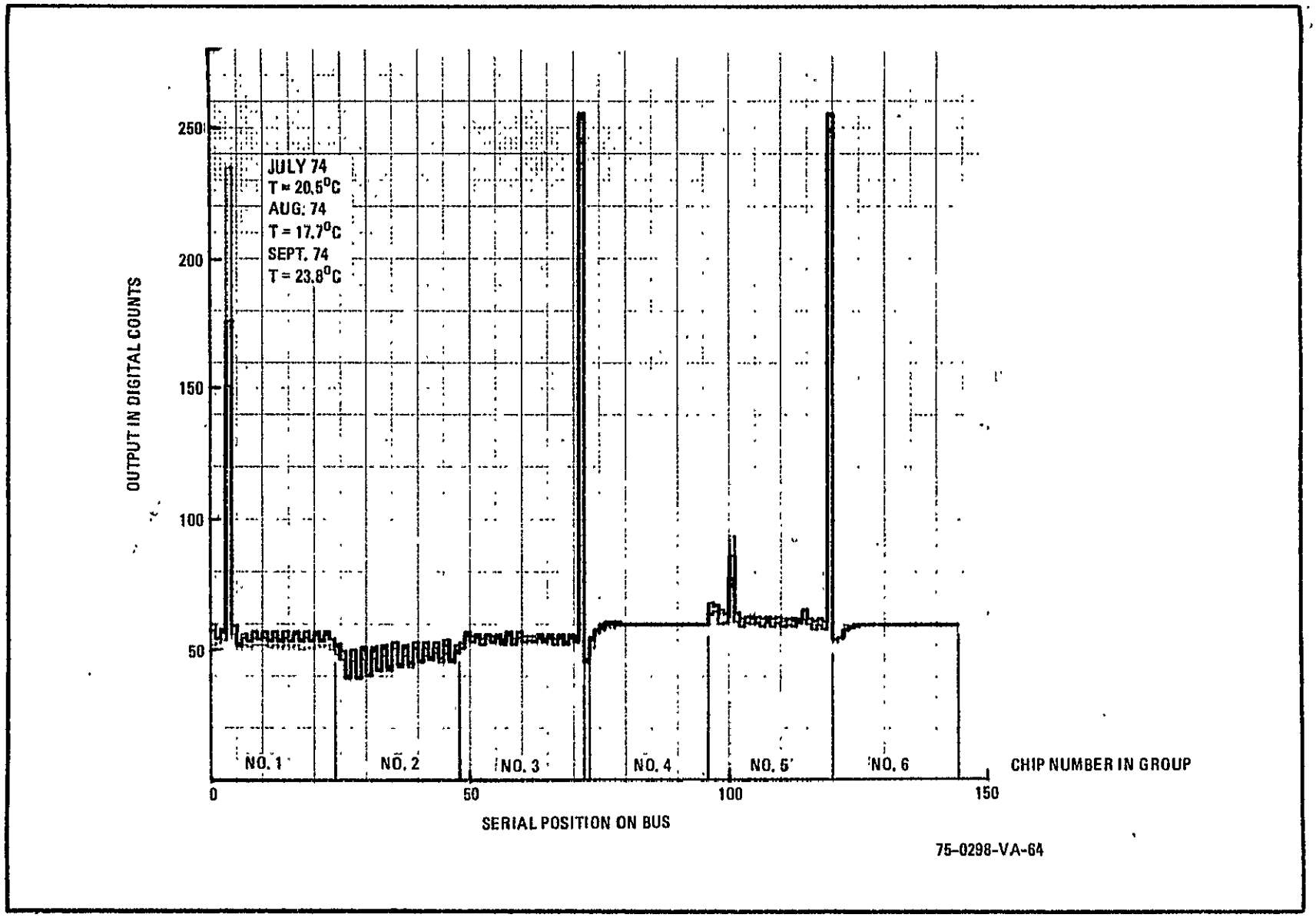


Figure 78. Output at Dark vs Time and Temperature
Bus D of Group 2

APPENDIX H

EIGHTEEN CHIP ARRAY DETECTOR TEST DATA

This appendix contains actual test data for a 96-element photodetector array chip. This performance data is typical of the chips used to fabricate the eighteen-chip array.

Included herein are six data tables which are:

Table 10	Summary Tables
Table 11	Response Minus Dark Current
Table 12	Quantizing Interval
Table 13	RMS Deviation
Table 14	Noise
Table 15	Linearity

TABLE 10

SUMMARY

CPES FUNCTION TEST DATA TABLES

CHIP: TYPE 808 LOT 168 WAFER 4 CHIP 3 RUN 24

BIAS: B1 285, B2 251, B3 287, B4 297, 1024 SAMPLES PER ELEMENT 2 A DUAL FUNCTION IT=1.0MSEC

COMMENTS: 20.530 32.260 19.940 32.84

HEATER A= 2 HEATER B= 1

RESPONSE MINUS DARK (PERCENT FULL SCALE) * IT=4.0MSEC

EXPOSURE LEVELS (MICROJOULES/SQ. METER) * * *

ELE	.0	48.5	144.7	236.0	354.8	578.9	943.9	1419.2
B1	22.54	4.26	12.56	20.52	30.92	50.61	75.58	76.42
B2	20.03	4.28	12.76	20.78	31.37	45.54	74.03	76.58
B3	21.00	4.78	13.91	22.67	34.17	54.56	76.11	77.42
B4	20.94	4.93	14.67	23.71	35.81	58.51	78.16	78.16

QUANTIZING INTERVAL (MICROJOULES PER BIT)

B1	1.12	1.13	1.13	1.13	1.12	1.22	1.82
B2	1.13	1.12	1.12	1.12	1.12	1.34	1.94
B3	.99	1.02	1.02	1.02	1.04	1.62	1.81
B4	.96	.97	.97	.97	.97	1.12	1.78

RMS DEVIATION (PERCENT FULL SCALE)

B1	.12	.13	.13	.13	.14	.02	.00
B2	.13	.13	.15	.15	.15	.14	.02	.00
B3	.12	.13	.14	.13	.14	.16	.01	.00
B4	.14	.14	.15	.15	.14	.16	.00	.00

NOISE (MICROJOULES PER SQ. METER)

EXPOSURE LEVELS (MICROJOULES/SQ. METER)

	24.2	96.6	192.3	288.4	386.4	761.4	1181.8
B1	1.47	1.50	1.49	1.53	1.51	1.13	1.73
B2	1.52	1.63	1.74	1.72	1.69	1.13	.24
B3	1.27	1.41	1.41	1.39	1.52	2.61	.06
B4	1.36	1.44	1.45	1.42	1.44	1.48	.00

LINEARITY (ABSOLUTE UNITS) - BETWEEN LEVELS 2 AND 3

B1	.9863
B2	.9997
B3	.9756
B4	.9897

74-0484-V-2

TABLE 11

RESPONSE MINUS DARK CURRENT

REFERENCE MINUS DARK (PERCENT FULL SCALE)					BUS NUMBER 81			
CHIP 1	TYPE 808	LOT 166		WAFER 4	CHIP 3		RUN 24	T
EXPOS	10	48.5	144.7	256.C	354.8	578.5	945.8	1419.2
1	23.36	3.71	1C.55	1E.CE	27.27	44.67	72.7C	76.74
7	21.60	4.40	1E.61	2C.4C	3C.89	5C.5A	76.44	76.44
9	22.19	4.20	1E.51	2C.43	3C.69	5C.1E	77.22	77.22
15	22.68	4.11	1C.12	15.E4	29.72	4A.6F	75.46	75.46
17	22.68	3.81	11.5C	15.1E	28.64	46.8E	76.44	77.42
23	22.58	4.20	12.EE	15.54	3C.11	45.17	75.EE	76.86
25	22.09	4.11	13.5C	15.EE	29.52	4E.E9	76.8E	76.83
31	21.51	4.30	1E.51	2C.4C	3C.79	5C.EA	77.32	77.32
3C	21.41	4.30	1E.61	2C.42	31.C9	5C.5C	76.C4	76.34
39	21.91	4.40	13.CC	21.21	3F.C6	5E.C5	76.EE	74.83
41	21.60	4.40	13.6C	21.4C	32.36	5E.EE	76.2E	76.2E
47	22.15	4.40	1C.5E	21.8C	32.94	5A.1E	76.5E	76.93
45	22.39	4.50	1C.25	21.8C	32.75	5C.E7	76.5E	75.95
5E	22.58	4.40	1C.1C	21.21	32.16	5E.5E	76.5E	76.93
57	23.66	4.30	1E.71	2C.8E	31.38	61.F2	71.1E	71.16
6C	22.29	4.40	1E.5C	21.11	31.87	5E.2C	76.7A	76.74
65	21.80	4.40	1C.CC	21.11	31.56	5E.1C	76.6A	76.64
71	21.70	4.40	1E.5E	21.0E	31.47	61.71	76.6A	76.64
7C	21.51	4.40	1E.7A	2C.3E	31.18	5C.5C	76.5A	76.54
75	21.80	4.50	1C.6C	21.51	32.45	5C.CE	76.7A	76.74
E1	21.90	4.59	1C.45	21.8C	32.94	5C.E6	76.5A	76.E4
E7	22.39	4.50	13.2C	21.81	32.55	5E.C7	76.7A	76.74
EE	22.09	4.50	1C.2C	21.81	32.A5	5A.CE	76.EA	76.E4
5E	21.38	3.13	9.C9	15.C5	22.68	3E.CC	62.C7	77.22
8	19.36	2.A4	8.CE	15.2C	19.75	32.46	52.52	77.63
E	18.87	4.20	1E.61	2C.7E	31.A8	61.5E	A1.CA	81.CA
1C	19.26	4.40	1E.5C	21.CE	31.77	61.61	7E.CE	7E.CE
1E	32.04	4.11	1E.51	2C.23	3C.89	5E.5E	8E.5E	8E.59
1E	19.55	4.20	1E.41	2C.33	3C.69	5C.1E	8C.2E	8C.25
2A	2C.23	4.20	1E.41	2C.1A	3C.A0	5A.EE	7E.4E	7E.46
2E	18.67	4.40	1E.71	2C.7E	31.28	5C.EC	8C.4E	8C.45
32	18.47	4.40	1C.2C	21.61	32.55	5E.27	7E.2E	7E.28
3A	18.28	4.40	1C.1C	21.21	32.26	5E.EE	8C.CE	8C.C6
4C	27.86	4.50	1C.4E	22.CE	33.CA	61.EA	81.EA	81.E6
42	19.16	4.50	1C.2E	21.8C	32.84	5C.7E	72.52	77.52
4E	19.16	4.59	1E.4E	22.1E	33.43	5E.1C	7E.5E	79.96
5C	19.26	4.59	1C.6E	22.1E	33.53	5E.1C	7E.67	79.67
56	19.45	4.40	1C.1C	21.51	32.16	5E.5E	7E.5E	79.96
6F	19.06	4.59	1E.2C	21.41	32.36	62.6E	7E.77	7E.77
6A	12.12	4.40	1C.CC	21.11	32.C6	44.1E	7E.6A	1CC.C0
66	18.57	4.40	1C.CC	21.21	31.56	5E.2C	7E.E6	7E.86
7E	18.47	4.50	1C.2E	21.51	32.55	5C.1E	7E.5E	79.96
7A	18.47	4.40	1E.1C	21.41	32.36	5E.5E	7E.5E	7E.96
9C	18.77	4.50	1C.4E	21.8C	33.C4	5A.1E	7E.8E	7E.86
8E	18.77	4.50	1C.2E	21.7C	32.7E	5C.67	7E.5E	7E.96
8E	19.16	4.50	1C.2E	21.51	32.55	5C.67	7E.5E	7E.96
9C	18.96	4.40	1C.2E	21.6C	32.55	5C.C7	7E.8E	7E.86
9E	27.46	5.32	9.57	1E.42	24.54	4C.5E	6E.9E	8C.65
A	22.29	4.69	1A.CE	2E.57	34.7C	5E.5E	7E.AC	7E.A0
B	2C.14	5.0A	1A.E7	2C.A6	3E.6E	5E.CE	7E.AC	7E.A0
11	22.29	4.60	1E.2C	21.41	32.36	5E.7E	7E.AC	7E.A3
1C	20.92	4.69	1C.3E	21.8C	32.A4	5C.A7	77.5E	77.82
1E	21.02	4.30	1E.71	2C.5E	31.28	61.CC	7E.CB	7E.CB
21	20.82	4.69	1C.2E	21.7C	32.7E	5C.C7	77.71	77.71
27	2C.23	4.69	1C.2E	21.7C	32.55	5C.CE	7E.7E	7E.79
2E	20.33	4.69	1C.EE	22.3E	33.82	5E.CC	7E.5C	7E.3C
2E	2C.04	4.79	1E.8E	22.6E	34.12	5E.6E	7E.1C	7E.1C
37	20.23	4.89	1A.17	2C.17	35.C0	67.1E	7E.4E	7E.49
4C	24.05	4.A3	1A.17	2E.2E	3A.1D	5E.B9	6E.5E	6E.B6
4E	20.53	4.08	1A.E6	2A.1A	36.36	5E.6E	7E.4E	7E.A9
51	1C.46	4.69	1E.EE	22.5E	3A.C2	34.5C	6E.6E	1CC.C0
5C	25.90	4.99	1A.C7	2E.3A	35.1D	67.1E	5E.C6	5E.C6
5E	2C.82	4.6A	1C.6E	22.1E	33.53	5A.EE	7E.C1	7E.C1
61	20.63	4.89	1A.17	2E.57	3A.2C	66.7E	7E.3C	7E.3D
67	20.33	4.69	1E.6E	22.1E	33.43	54.CE	7E.1C	7E.1C
6E	20.23	4.89	1A.CE	2C.67	3A.7C	66.7C	7E.3C	7E.3C
7E	2C.23	4.79	1C.6E	22.5E	3A.12	6E.6E	7E.1C	7E.1C
77	20.33	4.79	1C.5E	22.67	3A.6C	66.6C	7E.2C	7E.3C
8C	20.53	4.79	1A.CE	22.57	3A.6C	66.7C	7E.C1	7E.C1
8E	2C.63	4.99	1A.A7	2C.A6	35.3B	67.E7	7E.2C	7E.3D
91	2C.63	4.89	1A.17	23.C7	3A.8D	6E.8E	7E.C1	7E.C1
9C	3C.3D	4.69	1A.17	2C.C7	3A.7D	67.E7	7A.3C	7E.3D
A	21.91	4.69	1A.CE	2E.7E	3A.41	6E.C1	7E.2E	7E.2E
E	2C.53	4.89	1A.7E	2A.CE	36.36	6E.EC	7E.2E	7E.2E
12	2C.72	4.69	1E.4E	22.1E	33.63	5A.6A	77.81	77.81
14	21.21	4.69	1A.17	2E.97	3A.8D	6E.EE	7E.C1	7E.C1
6C	21.02	4.50	1C.2E	21.8C	32.A4	5C.A7	7E.6E	7E.69
2E	2C.92	4.89	1A.A7	2C.A6	35.2B	67.77	77.5E	77.52
2E	2C.33	4.79	1E.8E	22.5E	3A.12	6E.4C	7E.6E	7E.E9
3C	2C.33	4.8D	1A.6E	2C.7E	3E.7B	6E.6E	77.9E	77.52
3E	2C.C4	4.99	1A.C7	2C.A6	35.4B	5E.CE	7E.2C	7E.3D
4E	2C.23	5.0B	1E.2E	2A.6B	37.AA	61.C5	77.81	77.81
44	19.75	5.1B	1A.6E	2C.8E	3A.17	6E.C4	8C.3E	8C.35
46	2C.72	5.2B	1E.6A	2E.1E	3B.1E	6C.CE	7E.1C	7E.1D
4E	2C.82	4.99	1A.7E	2C.5E	35.97	5E.6E	77.71	77.71
5A	21.11	4.99	1A.8E	2A.2A	36.56	6C.CE	7E.1C	7E.1D
6C	2C.82	4.79	1A.17	2E.87	3A.7D	6E.6C	77.81	77.81
6E	2C.72	5.0B	1A.5E	2A.C4	3E.7B	6E.5E	77.51	77.91
6E	2C.33	4.AB	1A.C7	2C.2E	3E.1B	57.4E	7E.C1	7E.01
7C	2C.72	5.0B	1E.1E	2A.5A	37.1D	6C.7C	7E.6A	7E.64
7E	2C.23	4.79	1A.17	2C.2E	3E.09	57.3E	7E.C1	7E.C1
7E	2C.63	4.99	1E.CE	2A.4A	3E.9E	6C.A1	77.81	77.81
8A	2C.63	4.79	1A.CE	2E.57	3A.6D	6E.6C	77.51	77.91
8E	2C.92	5.0B	1A.5E	2A.4A	3E.8B	6C.E1	77.81	77.81
9E	2C.1A	4.99	1A.6E	2C.1E	3E.97	6E.5E	77.F1	77.81
9A	28.25	5.3B	1E.7A	2E.81	3B.71	6C.5C	82.C1	82.C1

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TABLE 12

QUANTIZING INTERVAL

QUANTIZING INTERVAL (MICROFARADS PER BIT) BLS NUMBER B1

CHIP: TYPE 808 LOT 1EE WAFER A CHIP 3 RUN 24

EXPOS	+0	A8A5	1AAA7	2C6AC	3B4A8	5782S	5A3A5	1A19A2
1		1.28	1.2E	1.2E	1.27	1.27	1.27	1.81
7		1.08	1.1E	1.13	1.12	1.1E	1.21	1.81
9		1.14	1.1E	1.1E	1.13	1.1C	1.1E	1.80
1E		1.15	1.17	1.16	1.17	1.16	1.22	1.84
17		1.24	1.2C	1.2C	1.21	1.21	1.21	1.79
23		1.13	1.16	1.16	1.15	1.15	1.2E	1.83
2E		1.15	1.15	1.17	1.17	1.17	1.2C	1.81
31		1.10	1.1C	1.13	1.13	1.1C	1.1E	1.79
37		1.10	1.12	1.12	1.12	1.11	1.21	1.82
3E		1.08	1.C5	1.C5	1.08	1.CE	1.2C	1.81
41		1.08	1.C7	1.C7	1.07	1.C7	1.21	1.82
47		1.C8	1.C6	1.C6	1.C5	1.C4	1.2C	1.80
4E		1.C5	1.C6	1.C6	1.C6	1.C6	1.21	1.83
5E		1.08	1.C8	1.C8	1.C8	1.CE	1.2C	1.80
57		1.10	1.11	1.11	1.11	1.1C	1.CE	1.7E
6C		1.0A	1.1C	1.C9	1.09	1.CE	1.2C	1.81
4E		1.0A	1.C5	1.C5	1.C8	1.C5	1.2C	1.81
71		1.C8	1.1C	1.1C	1.10	1.C9	1.2C	1.81
7C		1.C8	1.11	1.11	1.11	1.11	1.21	1.81
7E		1.0B	1.C7	1.C7	1.07	1.C7	1.2C	1.81
81		1.03	1.CE	1.C6	1.C5	1.CE	1.21	1.81
87		1.05	1.C7	1.C7	1.07	1.C6	1.2C	1.81
8E		1.0B	1.C7	1.C7	1.07	1.C7	1.21	1.81
9E		1.91	1.9E	1.9C	1.93	1.95	1.95	1.80
9		1.C9	1.76	1.75	1.76	1.74	1.74	1.80
8		1.13	1.1C	1.11	1.10	1.1C	1.14	1.21
1C		1.0A	1.1C	1.1C	1.C9	1.C5	1.17	1.75
1E		1.15	1.12	1.14	1.12	1.12	3.47	5.22
1E		1.13	1.14	1.12	1.13	1.1C	1.1E	1.73
24		1.13	1.14	1.16	1.14	1.14	1.22	1.84
2C		1.0A	1.11	1.11	1.11	1.13	1.15	1.72
2E		1.0B	1.C7	1.C7	1.C7	1.C6	1.16	1.75
34		1.0A	1.0E	1.0F	1.08	1.C7	1.1E	1.73
4C		1.05	1.C5	1.C4	1.C5	1.3E	3.22	3.33
42		1.05	1.C6	1.C6	1.C6	1.C5	1.15	1.79
4A		1.03	1.C5	1.C4	1.C3	1.C3	1.1E	1.73
5C		1.C3	1.CC	1.C4	1.C3	1.C3	1.16	1.74
5E		1.0B	1.CE	1.C7	1.0A	1.C9	1.1E	1.73
5E		1.03	1.C7	1.CE	1.C7	1.C7	1.16	1.74
64		1.04	1.C5	1.C5	1.08	1.2E	1.2C	1.89
6E		1.0A	1.C5	1.C5	1.08	1.CE	1.16	1.74
72		1.C5	1.C6	1.C7	1.C7	1.C6	1.1E	1.73
7A		1.0B	1.CF	1.0E	1.C7	1.C7	1.1E	1.73
8C		1.05	1.CE	1.C6	1.C5	1.C4	1.16	1.74
4E		1.C5	1.C6	1.C6	1.C6	1.C5	1.1E	1.73
8A		1.C5	1.C6	1.C7	1.C7	1.C6	1.1E	1.73
9C		1.08	1.C6	1.C7	1.C7	1.C6	1.16	1.74
9E		1.43	1.4E	1.4C	1.41	1.3E	1.3E	1.72
C		1.C1	1.CC	1.CC	1.C0	1.9E	1.1F	1.77
5		.93	.97	.98	.97	.97	1.1F	1.77
11		1.05	1.C7	1.CF	1.C7	1.C7	1.27	1.82
1C		1.01	1.C6	1.C6	1.C6	1.C6	1.1E	1.79
1E		1.10	1.13	1.1C	1.11	1.11	1.17	1.75
21		1.04	1.CE	1.CE	1.C6	1.CE	1.1E	1.79
27		1.01	1.CC	1.C6	1.C7	1.C7	1.17	1.76
2E		1.01	1.CC	1.CC	1.C3	1.CC	1.1E	1.77
35		.99	1.CE	1.C2	1.C2	1.C1	1.1F	1.78
37		.97	1.CC	1.CC	.99	.9E	1.1E	1.77
4C		1.01	1.CC	.9E	1.C0	.9E	1.47	2.22
4E		.93	.95	.96	.95	.9E	1.1E	1.77
51		1.01	1.C2	1.C2	1.C2	1.42	1.34	1.39
5C		.95	.9E	.9E	.99	.9E	1.1E	2.39
5E		1.01	1.C3	1.C4	1.C3	1.C4	1.1E	1.78
61		.97	1.CC	1.CC	1.C0	1.CC	1.1E	1.77
67		1.01	1.CC	1.C4	1.C4	1.C4	1.1F	1.78
6E		.97	1.CC	1.CC	1.C0	1.CC	1.1E	1.77
76		.99	1.CE	1.C2	1.C2	1.C2	1.1E	1.78
77		.99	1.C1	1.C1	1.C0	1.CC	1.1E	1.77
7C		.99	1.CC	1.CC	1.C0	1.C1	1.1E	1.78
8E		.95	.9E	.9E	.98	.9E	1.1F	1.77
91		.97	1.CC	1.CC	1.C0	.95	1.1E	1.78
92		.97	1.CC	1.CC	1.C0	.9E	1.1E	1.77
A		1.41	1.CC	1.C1	1.C1	1.CC	1.21	1.82
C		.97	.9E	.9E	.95	.9E	1.16	1.75
1E		1.C1	1.CE	1.C4	1.C3	1.C4	1.15	1.78
1A		1.C1	1.CC	1.CC	1.C0	.99	1.1E	1.78
2C		1.05	1.C6	1.C6	1.C6	1.C6	1.17	1.76
2F		.97	.9E	.9E	.98	.9E	1.1E	1.79
3E		.99	1.C2	1.CE	1.C2	1.C2	1.17	1.76
4C		.97	.9E	.97	.97	.97	1.1E	1.79
5A		.95	.9E	.9E	.98	.97	1.1E	1.77
5E		.93	.9E	.9E	.93	.9E	1.1E	1.78
6A		.91	.9E	.97	.96	.9E	1.1E	1.73
6E		.99	.9E	.9E	.9C	.9E	1.1E	1.78
7E		.95	.9E	.97	.96	.9E	1.1E	1.79
8A		.95	.9E	.9E	.95	.9A	1.1E	1.78
6C		.99	1.CC	1.C1	1.C0	1.CC	1.1E	1.78
6E		.93	.9E	.9E	.94	.9A	1.1F	1.78
6E		.97	.9E	.9E	.99	.9E	1.1E	1.78
7C		.93	.9C	.9A	.93	.9C	1.2C	1.81
7E		.99	1.CC	.9E	.99	.9E	1.1E	1.78
7F		.95	.9A	.9A	.94	.9A	1.1E	1.78
8A		.99	1.CC	1.CC	1.C0	1.CC	1.1E	1.78
8E		.93	.9E	.9A	.94	.9A	1.1E	1.78
9E		.9B	.9E	.97	.96	.97	1.1E	1.78
9A		.88	.9C	.95	.90	.8E	1.1C	1.69

74-0484-V-4

TABLE 13

RMS DEVIATION

RMS DEVIATION (PERCENT FULL SCALE) PLS NUMBER 81
CHIP1 TYPE ADC LOT 168 WAFER # CHIP 3 RUN 24

EXPOS	+0	48.5	144.2	226.0	354.8			
1	+08	+09	+16	+12	+08	+10	+10	+00
7	+12	+19	+11	+10	+15	+11	+00	+00
9	+13	+11	+16	+10	+11	+16	+00	+00
15	+11	+15	+11	+10	+14	+12	+00	+00
17	+11	+13	+08	+11	+11	+10	+14	+00
20	+11	+17	+11	+10	+12	+10	+00	+00
25	+18	+10	+15	+10	+15	+15	+00	+00
31	+11	+14	+10	+10	+13	+15	+00	+00
33	+11	+11	+11	+11	+14	+15	+00	+00
35	+10	+15	+20	+12	+11	+12	+00	+00
41	+11	+12	+14	+17	+14	+17	+00	+00
47	+15	+17	+11	+15	+12	+12	+00	+00
45	+11	+10	+11	+12	+10	+17	+00	+00
51	+12	+09	+12	+23	+15	+12	+00	+00
57	+13	+14	+11	+11	+13	+16	+00	+00
61	+10	+16	+14	+12	+16	+15	+00	+00
65	+10	+11	+11	+12	+12	+14	+00	+00
71	+13	+11	+20	+10	+18	+16	+00	+00
75	+11	+15	+05	+16	+11	+15	+00	+00
75	+11	+11	+10	+11	+13	+18	+00	+00
81	+19	+10	+18	+18	+18	+18	+00	+00
87	+12	+14	+11	+23	+15	+17	+00	+00
85	+15	+13	+18	+12	+13	+10	+00	+00
95	+17	+23	+05	+12	+15	+10	+15	+00
2	+10	+07	+14	+11	+20	+08	+18	+00
4	+22	+13	+11	+10	+15	+17	+00	+00
10	+12	+18	+16	+14	+15	+15	+00	+00
16	+17	+12	+17	+26	+11	+00	+00	+00
18	+19	+14	+14	+17	+16	+15	+00	+00
24	+13	+15	+11	+11	+15	+21	+00	+00
26	+15	+12	+22	+17	+08	+15	+00	+00
32	+12	+15	+14	+16	+17	+14	+00	+00
34	+12	+19	+21	+12	+12	+15	+00	+00
40	+11	+13	+16	+11	+16	+00	+00	+00
46	+11	+16	+12	+15	+13	+15	+00	+00
4F	+08	+16	+10	+14	+12	+20	+00	+00
50	+11	+09	+18	+14	+12	+22	+00	+00
56	+10	+12	+16	+15	+18	+17	+00	+00
58	+12	+19	+15	+12	+14	+14	+00	+00
6A	+11	+16	+15	+11	+16	+10	+16	+00
6E	+13	+10	+13	+13	+13	+11	+00	+00
7E	+11	+13	+12	+16	+16	+14	+00	+00
74	+11	+14	+10	+16	+17	+15	+00	+00
80	+20	+09	+14	+16	+17	+16	+00	+00
82	+21	+11	+14	+12	+16	+14	+00	+00
88	+12	+19	+12	+24	+20	+14	+00	+00
90	+15	+14	+16	+18	+17	+15	+00	+00
96	+13	+14	+20	+15	+13	+19	+16	+00
2	+10	+11	+11	+07	+12	+12	+00	+00
E	+11	+14	+12	+07	+15	+10	+00	+00
11	+12	+16	+16	+05	+12	+10	+00	+00
1C	+11	+13	+14	+12	+14	+15	+00	+00
19	+11	+12	+14	+12	+13	+15	+00	+00
21	+12	+13	+12	+11	+13	+14	+00	+00
27	+12	+11	+10	+10	+13	+15	+00	+00
25	+13	+12	+12	+12	+14	+17	+00	+00
3E	+11	+15	+10	+13	+14	+18	+00	+00
37	+10	+13	+18	+13	+12	+14	+00	+00
4C	+13	+19	+14	+21	+15	+15	+00	+00
45	+14	+10	+14	+14	+14	+16	+00	+00
51	+12	+13	+14	+14	+12	+14	+18	+00
52	+14	+12	+14	+14	+16	+14	+00	+00
58	+12	+15	+18	+14	+13	+17	+00	+00
61	+14	+12	+14	+10	+15	+17	+00	+00
67	+14	+12	+12	+12	+13	+16	+00	+00
65	+14	+13	+15	+16	+16	+18	+00	+00
75	+11	+11	+11	+11	+13	+00	+00	+00
77	+13	+13	+17	+14	+13	+15	+00	+00
8C	+15	+11	+18	+12	+14	+14	+00	+00
85	+12	+14	+12	+22	+12	+13	+00	+00
91	+13	+14	+16	+15	+14	+16	+00	+00
93	+11	+16	+11	+15	+16	+12	+00	+00
A	+11	+10	+12	+17	+19	+13	+00	+00
E	+15	+14	+14	+16	+15	+16	+00	+00
12	+14	+13	+12	+17	+13	+19	+00	+00
14	+15	+14	+14	+15	+12	+14	+00	+00
2C	+12	+12	+14	+13	+15	+10	+00	+00
2E	+13	+14	+15	+14	+18	+17	+00	+00
32	+17	+13	+11	+15	+13	+16	+00	+00
3C	+18	+19	+16	+21	+13	+17	+00	+00
46	+11	+09	+00	+11	+16	+15	+00	+00
4E	+16	+14	+16	+10	+13	+15	+00	+00
54	+14	+17	+18	+08	+15	+14	+00	+00
46	+12	+19	+12	+16	+11	+15	+00	+00
52	+11	+14	+14	+15	+15	+20	+00	+00
54	+11	+16	+15	+15	+11	+14	+00	+00
6C	+12	+13	+14	+16	+18	+12	+00	+00
62	+13	+16	+11	+14	+15	+16	+00	+00
68	+18	+13	+18	+08	+17	+14	+00	+00
7C	+15	+17	+17	+16	+17	+15	+00	+00
7E	+14	+11	+21	+14	+15	+17	+00	+00
78	+17	+12	+12	+12	+13	+14	+00	+00
84	+14	+13	+15	+10	+12	+15	+00	+00
86	+14	+16	+16	+12	+17	+16	+00	+00
92	+12	+13	+14	+18	+14	+17	+00	+00
94	+20	+19	+00	+15	+14	+14	+00	+00

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TABLE 14

NOISE

NOISE (MICROVOLTS PER SQ. METER) PUS NUMBER 81

CHIP*	TYPE BOB	LAT LEE	WAFER A	CHIP 3		RUN
EXPOS	2+12	98.6	1SC.C	2SE.4		
1	1+12	1+65	1+6C	1+CE	1+06	1+ZE	E+EE
2	1+44	1+62	1+E7	1+4A	1+25	+7E	+CC
3	1+39	1+57	1+AE	1+21	1+55	1+C7	+CC
4	1+64	1+63	1+4E	1+6E	1+61	+2E	+CC
5	1+4A	1+26	1+1E	1+35	1+40	1+4A	3C+AE
6	1+62	1+70	1+E7	1+3E	+.6A	+E2	+CC
7	1+67	1+32	1+AA	1+E5	1+70	+EC	+CC
8	1+38	1+42	1+15	1+3E	1+6A	1+C4	+CC
9	1+27	1+31	1+2E	1+45	1+71	1+1C	+CC
10	1+36	1+94	1+75	1+4E	1+52	+E7	+CC
11	1+27	1+45	1+65	1+72	1+62	1+3C	+CC
12	1+76	1+43	1+6E	1+62	1+18	+5E	+CC
13	1+14	1+14	1+EE	1+E3	1+48	1+AE	+CC
14	1+15	1+17	1+56	2+1C	1+38	+5C	+CC
15	1+52	1+45	1+E4	1+3E	1+42	1+A5	+CC
16	1+46	1+71	1+AZ	1+E1	1+61	1+CE	+CC
17	1+15	1+22	1+2Z	1+33	1+5A	1+C2	+CC
18	1+31	1+74	1+E4	1+7C	1+77	1+17	+CC
19	1+42	1+36	1+25	1+81	1+77	1+3C	+CC
1A	1+20	1+33	1+34	1+3E	+.32	+5E	+CC
1B	1+52	1+30	1+EC	1+2E	1+6J	+55	+CC
1C	1+41	1+38	1+EE	2+CC	1+63	1+24	+CC
1D	1+59	1+55	1+AE	1+3W	1+23	+5E	+CC
1E	3+11	2+60	1+EE	2+CE	1+74	1+92	2+34
1F	1+65	1+78	2+16	2+77	1+76	1+37	1+3E
20	2+00	1+33	1+AC	1+54	1+7A	1+C2	+CC
21	1+66	1+90	1+6E	1+61	1+77	1+EE	+CC
22	1+71	1+66	2+EC	2+C3	2+9b	+CC	+CC
23	1+49	1+41	1+F1	1+86	1+42	+2C	+CC
24	1+61	1+E4	1+2C	1+47	1+89	1+A7	+CC
25	1+48	1+97	2+21	1+C7	1+46	+EA	+CC
26	1+61	1+60	1+EE	1+35	1+64	1+C1	+CC
27	1+47	1+97	1+F6	1+3E	1+96	1+2E	+CC
28	1+3C	1+51	1+4C	1+48	1+15	+CC	+CC
29	1+51	1+51	1+4E	1+5C	1+49	1+1E	+CC
2A	1+22	1+41	1+E7	1+3A	1+79	1+4A	+CC
2B	1+68	1+45	1+7C	1+3E	1+78	1+6E	+CC
2C	1+21	1+34	1+71	2+1C	2+02	1+1Z	+CC
2D	1+64	1+69	1+AE	1+37	1+39	+56	+CC
2E	1+53	1+26	1+E7	1+5E	1+4A	1+6E	1+EE
2F	1+24	1+27	1+AE	1+47	1+E2	+EE	+CC
30	1+33	1+40	1+E5	1+73	1+55	+5E	+CC
31	1+41	1+64	1+7E	1+E1	1+78	1+CE	+CC
32	1+57	1+26	1+E7	1+7E	1+55	1+1A	+CC
33	1+71	1+34	1+AE	1+E3	1+39	+5E	+CC
34	1+66	1+72	2+CE	2+2E	1+40	+55	+CC
35	1+6C	1+60	1+E7	1+5E	1+43	1+CE	+CC
36	1+92	2+58	2+EE	2+3E	2+0A	6+31	2+EA
37	1+08	1+51	+.EC	+.E3	1+20	1+3C	+CC
38	1+23	1+62	1+EA	1+C7	1+6E	1+EC	+CC
39	1+48	1+E4	1+1E	1+1A	1+75	1+E3	+CC
3A	1+20	1+49	1+AC	1+3E	1+45	1+2A	+CC
3B	1+28	1+48	1+41	1+42	1+43	+57	+CC
3C	1+3b	1+37	1+2E	1+3C	1+62	1+EE	+CC
3D	1+23	1+36	1+4E	1+AE	1+6b	1+27	+CC
3E	1+29	1+27	1+2E	1+34	1+40	1+6E	+CC
3F	1+32	+.45	1+3E	1+41	1+60	1+7C	+CC
40	1+11	+.60	1+5E	1+E7	1+41	1+E5	+CC
41	1+2R	1+30	1+7E	1+E3	1+49	1+EC	+CC
42	1+17	+.22	1+41	1+3E	1+60	1+77	+CC
43	1+30	1+42	1+44	1+C4	1+73	1+6E	+CC
44	+.25	+.33	1+4C	1+5E	1+1b	1+81	+CC
45	1+36	1+76	1+7E	1+3E	1+31	1+1E	+CC
46	1+29	+.34	1+EC	1+E5	1+3J	1+6A	+CC
47	1+31	+.F4	1+EE	1+31	1+22	1+E1	+CC
48	1+30	1+42	1+EC	1+6C	1+53	E+CE	+CC
49	1+C7	1+17	1+2C	1+2E	1+52	1+EC	+CC
4A	1+34	1+56	1+EE	1+5C	1+34	1+AE	+CC
4B	1+3C	1+51	1+E2	1+EC	1+39	1+2A	+CC
4C	+.28	+.26	1+7E	1+2C	1+40	1+6E	+CC
4D	1+33	1+49	1+EE	1+4E	1+46	1+6Z	+CC
4E	1+13	1+40	1+54	1+EE	1+28	1+1E	+CC
4F	+.C9	1+14	1+EC	1+EE	1+27	1+CE	+CC
50	+.46	1+38	1+E1	1+4E	1+29	1+1C	+CC
51	1+37	1+34	1+E1	1+E7	1+28	1+1E	+CC
52	1+47	1+43	1+E4	1+3E	1+77	1+44	+CC
53	1+27	1+43	1+4E	1+AE	1+76	1+27	+CC
54	1+36	1+49	1+4E	1+6C	1+6b	1+C5	+CC
55	1+64	1+27	1+3E	1+4A	1+74	1+55	+CC
56	1+62	1+53	1+E6	1+6E	1+62	1+55	+CC
57	+.83	+.55	1+5E	1+C5	1+72	1+47	+CC
58	1+40	1+58	1+3E	1+E5	1+56	1+1E	+CC
59	1+41	1+74	1+2E	1+1E	1+4J	4+EE	+CC
5A	1+21	1+30,	1+3E	1+E3	1+63	1+E1	+CC
5B	1+18	1+56	1+44	1+47	+.79	1+7C	1+34
5C	1+32	1+50	1+A6	1+2A	1+36	2E+67	+CC
5D	1+24	1+34	1+E4	1+6E	1+6b	1+2E	+CC
5E	1+39	1+3b	1+2E	1+3E	1+6b	1+AE	+CC
5F	1+53	1+60	1+2E	1+2E	1+67	1+6C	+CC
60	1+49	1+39	1+2E	1+E7	1+75	1+4E	+CC
61	1+28	1+67	1+7E	1+4E	1+64	1+6E	+CC
62	1+40	1+17	1+2C	1+2E	1+61	1+E7	+CC
63	1+34	1+62	1+4E	1+1E	1+44	1+E4	+CC
64	1+44	1+58	1+6E	1+6E	1+25	1+1E	+CC
65	1+C0	1+26	1+E5	1+E6	1+42	1+3E	+CC
66	1+78	1+96	1+7E	1+34	1+18	1+CE	+CC

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TABLE 15

LINEARITY

LINEARITY (ABSOLUTE UNITS) - BETWEEN LEVELS 2 AND 3 - BUS NUMBER 81

CHIP: TYPE 808 LOT 168 WAFER 4 CHIP 3 RUN 24

1	.9872
7	.9602
9	.9971
15	.9889
17	1.0134
23	.9737
25	.9730
31	.9744
33	.9820
39	.9900
41	1.0049
47	1.0198
49	.9903
55	.9974
57	.9897
63	.9826
65	.9900
71	.9845
73	.9676
79	.9830
81	.9835
87	.9830
89	.9830
95	.9735
2	1.0986
4	1.0204
10	.9825
16	1.0208
18	.9893
24	.9899
26	.9676
32	1.0049
34	.9974
40	1.0049
42	.9976
48	.9835
50	.9977
56	.9974
58	.9621
64	.9900
66	.9900
72	.9903
74	.9974
80	1.0049
82	.9976
88	.9903
90	1.0123
96	1.0049
3	1.0048
5	.9598
11	.9830
13	.9560
19	.9897
21	.9692
27	.9491
29	.9769
35	.9707
37	.9714
43	1.0118
45	.9791
51	.9909
53	.9655
59	.9770
61	.9714
67	.9769
69	.9647
75	.9707
77	.9775
83	.9844
85	.9720
91	.9714
93	.9714
4	1.0049
6	1.0114
12	.9630
14	1.0118
20	.9903
22	.9915
28	.9707
30	1.0049
36	.9655
38	1.0113
44	.9480
46	.9826
52	.9917
54	.9983
60	.9912
62	.9855
68	.9848
70	.9984
76	.9912
78	1.0114
84	.9844
86	.9856
92	.9852
94	.9805

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APPENDIX I

HP-8330A CALIBRATION REPORT

Westinghouse Electric Corporation Industry & Defense

Defense & Electronic Systems Center
Aerospace & Electronic Systems Division

Friendship International Airport
Box 746
Baltimore Maryland 21203

Standardizing Laboratory

REPORT OF CALIBRATION

for

THERMOPILE
(Radiant Flux Detectors)

MFR: HEA MODEL: 8330A SERIAL NO: 00520

Submitted by

SDDE (Tracy)

The relative spectral response of this instrument was determined by comparison to an EPPLEY thermopile equipped with a window of known spectral transmittance. A 250 mm monochromator with a 20 nm bandpass was used to provide the monochromatic radiation.

The absolute response was measured at 632.8 nm using a helium-neon laser as the source. The radiation field was 3.0 cm in diameter and was produced with a spatial filter and lenses. The calibration factor was found to be 96%.

The uncertainties in the measurement arise from the repeatability of the test instrument, stray light in the monochromator and non-uniformity in the radiation field.

Uncertainty of the relative response is estimated to be within $\pm$ 2.0% with the absolute response estimated to be $\pm$ 5.0%.

The relative response normalized to 632.8 nm with a calibration factor of 96% is tabulated in Table 1.

For the Manager

Carroll G. Hughes, III
Senior Engineer

Test No: 75020606

Date: 11 February, 1975

TABLE 16

ELATIVE SPECTRAL RESPONSE AT SELECTED WAVELENGTHS, NORMALIZED TO 632.8 nmi

Wavelength (nmi)	Relative Spectral Response
500	0.80
600	0.93
632.8	1.00
700	1.01
800	1.00
900	0.96
1000	0.99
1100	1.00
1200	1.08

Test No: 75020606

Date: 11 February 1975

APPENDIX J

STUDY TO DETERMINE THE RECOMMENDED APPROACH FOR DARK LEVEL AND RESPONSIVITY CORRECTION

This study was performed to determine the preferred technique for a real-time dark level and responsivity correction design to be incorporated in the solid state linear array processor. It is concluded that an all-digital approach with CMOS memory is preferred.

J.1 INTRODUCTION

Modification 9 of NAS 5-21806 (Breadboard Linear Array Scan Imager Program) calls for fabricating a real-time offset and gain correction capability. Prior to the actual fabrication, the contractor is required to perform a study to determine the recommended approach (item 14 A-1). Approval of the recommended approach is required by the Technical Officer before fabrication is to begin. This appendix provides results of the study and identifies the recommended approach.

J.2 REQUIREMENTS

In the present breadboard linear array scan imager, the input data to the processor consists of 576 data samples, each with a unique dark level (zero illumination offset) and responsivity. Data is processed by four parallel channels for four simultaneous data samples and 144 steps per line. The initial processing is analog to the point where a sufficient signal level is obtained for A/D conversion. Thereafter it is digitally processed, including the multiplexing into a single sequential data stream.

To include the dark level and responsivity correction function requires that the breadboard by modified to:

a. Store calibration information for 576 data elements

b. Perform the arithmetic correction using the stored information.

The first requirement is readily resolved. Experience has shown that it is awkward and not practical to store this much data using analog storage. The information must be stored digitally. The problem then becomes selection of the best storage technique. The most likely candidate for digital storage is CMOS memories. Although weight, volume, and power are not limitations in the breadboard system, it is important to consider them in anticipation of flight applications. Memories such as plated wire are relatively heavy, and alternative TTL solid state devices consume large amounts of power. CMOS provides a good compromise of very lower power, low weight, and low volume. Commercial CMOS memories are available "off the shelf" and are being applied on space programs. They are also available in chip form for high density packaging; however, for the breadboard, commerical packaging will be used.

The second problem, that of arithmetic correction, is more complex. Again, the tradeoff is between analog and digital operations. In this case however, the selection is not as straightforward as for data storage.

The arithmetic correction involves removal of the offset component (dark level) of each element and application of a scale factor (gain correction). For simplicity, it is preferable to remove the offset prior to applying the scale factor. The memory stores the offset factor and scale factor for each element.

Removing the offset can be accomplished via either an analog or digital approach. The analog approach is to convert the stored data to an analog signal, which is fed into an operational amplifier summing point. The feedback signal is made equal and of opposite polarity to the offset signal. This is essentially a dc restoration loop, causing the analog channel output to be zero volts at dark input. The digital approach is to subtract the stored value from the data; zero output then does not occur until after the digital subtractor.

Examining the advantages and disadvantages of each approach indicates that the primary advantage of the analog approach is the removal of offsets prior to A/D conversion. This extends the possible dynamic range and

reduces the required range of the A/D. The analog disadvantage is the high noise injection probability. Every attempt has been made to minimize system noise and it is not technically desirable to increase the noise. For both approaches the information is in digital form and no further signal degradation occurs if the remaining process is digital. Therefore, digital offset removal is the recommended approach.

For responsivity correction, several analog and digital techniques are possible. The analog methods are to use

a. Switched resistors as dividers or amplifier feedback

b. A variable resistance FET with a control circuit

c. The nonlinear characteristics of a device such as a diode with gain controlled by the bias current.

Of these three analog approaches, the preferred method is to use switched resistors for simplicity and linearity. However, the same limitations exist for responsivity correction as applied to offset removal. A switching circuit is an even more undesirable addition to the analog channel. The best approaches are a digital lookup table or a multiplier. At this time, the multiplier is the preferred choice since less memory and simpler processing is involved. Off-the-shelf LSI multipliers are readily available. The recommended approach therefore, is the use of a digital LSI multiplier.

J.3 CONCLUSIONS AND RECOMMENDATIONS

It is concluded that, because of noise considerations, a digital correction technique is preferable to an analog one. The factor of 2 to 4 in dynamic range (two bits digital) that an analog system saves is not a major consideration. An important point is that fewer more complex components are required for the digital processes, and much historical data is available on TTL. The all-digital approach is also considered more reliable than the analog approach because of the vast store of user data available on digital devices. Although CMOS memories are still relatively new, considerable emphasis is not being applied and will continue to be applied to this technique for spaceflight applications. It is, therefore, recommended that an all-digital

approach be used to implement dark level and responsivity correction for the breadboard linear array scan imager.