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SOLID STATE TELEVISION CAMERA (CID)

August 1976

FINAL TECHNICAL REPORT

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OPTOELECTRONIC SYSTEMS OPERATION

ELECTRONIC SYSTEMS DIVISION

GENERAL ELECTRIC

Syracuse, N.Y.

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Charge Injection Device
Solid State Imager
Camera

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This report describes the design, development and test of a Charge Injection Device (CID) camera using a 244x248 element array. The resulting camera was delivered to NASA.

The end product of this contractual effort was a CID camera employing scanning techniques which allow the CID to be used with conventional monitor displays meeting EIA standards. The camera was designed to provide state-of-

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the-art performance in CID technology. The 244x248 element array is presently the highest resolution CID array that can be produced. A number of video signal processing functions are included which maximize the output video dynamic range while retaining the inherently good resolution response of the CID. In addition, the camera provides two switchable scanning options, two switchable readout options and various internal video and timing signals at the back panel of the camera. The combination of options and externally provided signals will allow this camera to become a valuable evaluation tool for determining future design goals. The following is a summary of some of the unique features of this CID camera.

Low light level performance	- NDRO readout mode with built in thermo-electric cooling at .13 ft candle scene illuminations.
High S/N Ratio	- In excess of 50 DB for both pattern and random noise components.
Anti-Blooming	- Inherently excellent optical overload response.
Geometric Distortion	- Inherently excellent geometric linearity.
Sequential Scanning	- Sequential scan mode, all lines in proper vertical sequence.
AGC	- The first utilization of AGC in a CID camera.

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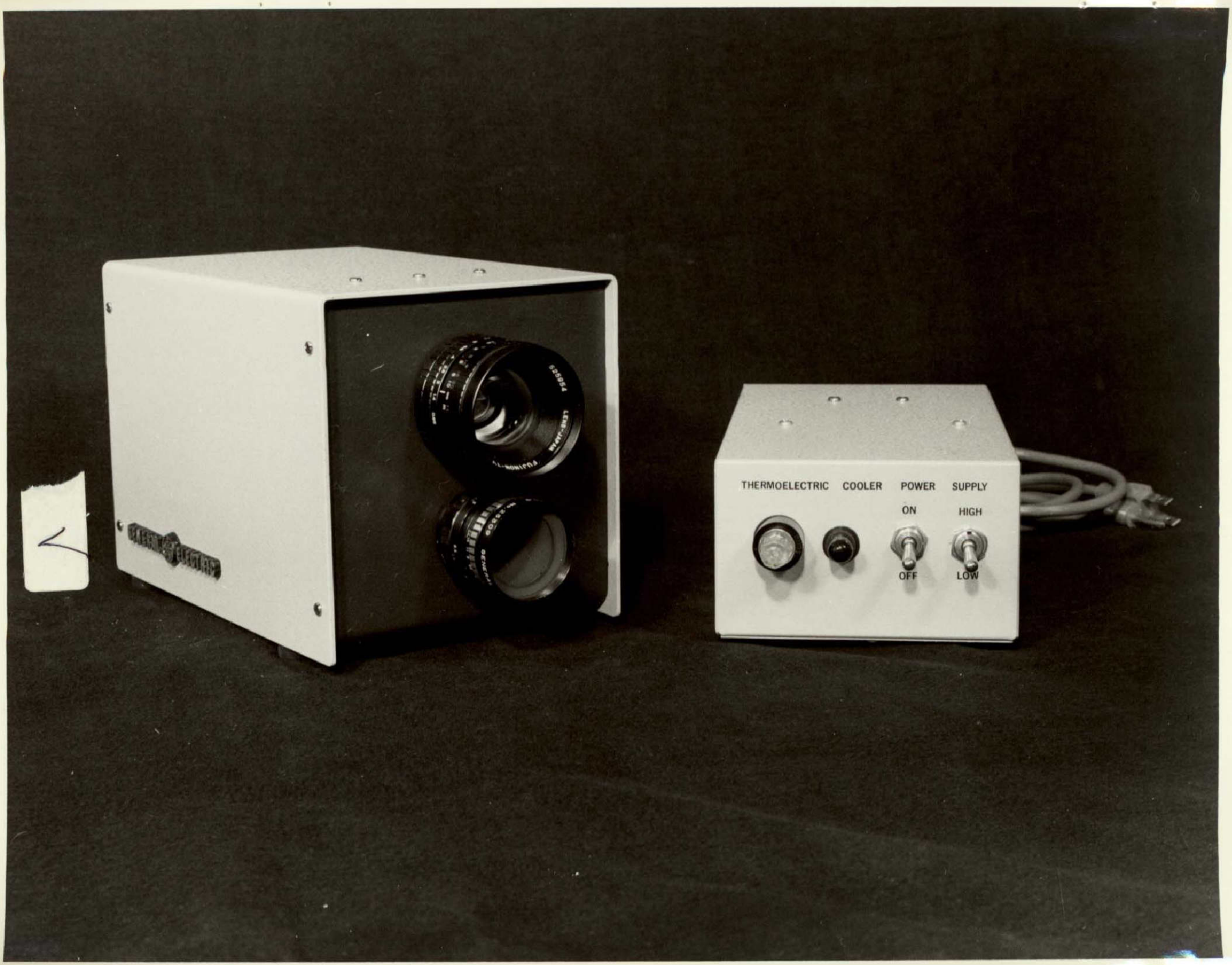
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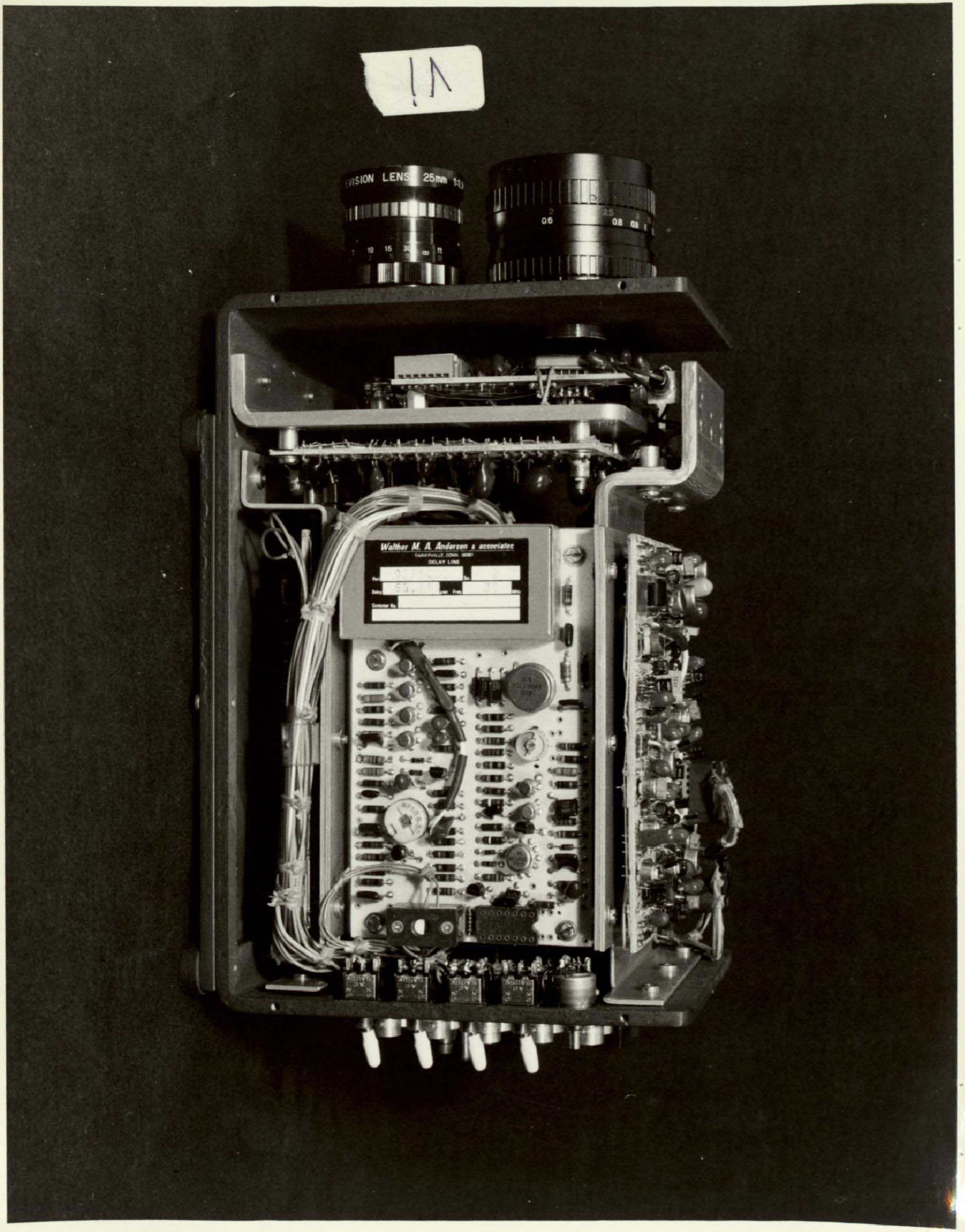

VISION LENS 25mm
Walther M. A. Andersen & associates
DELAY LINE

1.0 Purpose

1.1 Objective

The objective of this Final Report is to summarize, in a detailed manner the effort required to perform the engineering design, development and test of a totally solid-state television camera.

1.2 End Product

The end product of this contractual effort is a solid state television camera which uses a CID (Charge Injection Device) as the image sensor. The camera employs scanning techniques which allow the CID to be used with conventional monitor displays meeting EIA standards. A number of significant options have been incorporated in the product design to facilitate experimental study of CID camera technology.

2.0 Scope

General Electric has provided the necessary resources to perform engineering design, development and test of a solid state television camera using a CID for the image sensor. A large number of diverse tasks were performed in building the end product. A study of scanning techniques and subsequent experimental evaluation resulted in the choice of the two present CID camera scanning modes, normal RS170 and synthetic interlace. A study of readout alternatives and their experimental evaluation resulted in the choice of two selectable readout modes, normal pre-inject, and NDRO. A thermoelectric cooler study initiated in support of the NDRO readout mode, resulted in the incorporation of a thermoelectric cooler, heatsink and nitrogen purging capability. Investigations, which had occurred during the progress of an in-house program running parallel to this effort, resulted in the valuable addition of a comb filter option. In an effort to provide as much versatility as reasonably possible, several video and digital interfaces were made available externally. A detailed discussion of the work performed is described in Section 3 of this report.

3.0 Technical Requirements

3.1 Study, Design and Development Requirements

Purpose: To study, design and develop a number of alternate approaches and concepts that are applicable to the design of a CID camera having state-of-the-art performance.

Scope: To perform engineering study, design and development the areas of CID array size, camera scanning techniques, readout modes and video processing.

Performance:

1. Evaluated various array sizes for state-of-the-art resolution and reasonable availability consistent with the timing of the program. A 244 line x 248 array was chosen for use in the camera.

2. Evaluated several scanning schemes in an effort to find techniques which provide video lines in proper vertical sequence. The difficulty being to both satisfy the readout constraints imposed by the pattern noise rejection techniques utilized in CID video processing, and to meet the video output specifications imposed by EIA standards. As a compromise, two scanning schemes were provided, individually selectable via switching on the rear panel of the camera. The "normal" scanning mode is one which has greater vertical aberration however supplying the full compliment of lines (none blanked) and satisfying EIA standards for total number of lines (525 with 488 being visable) and interlace. The "synthetic interlace" mode (outerlace) provides fully sequential video information, however, supplies only 244 visable vertical lines per frame (every other line is blanked), and non-interlaced fields. An additional video processor was added, a comb filter, which corrects to some extent the vertical distortion incurred during the "normal" scanning mode. This scheme also augments pattern noise rejection as an additional benefit.

3. Evaluated various readout modes for the CID imager from the standpoint of providing a maximum of versatility for a reasonable amount of hardware. Two readout modes, the normal "pre-inject" mode

and the NDRO (Non Destruct Readout) were provided, individually selectable via rear panel switches. The pre-inject mode has the best signal to pattern noise ratio of any of the studied CID readout schemes, however, it has a conventional fixed 33 millisecond optical integration time for each element.

The NDRO mode provides for a variable amount of optical integration time (up to several seconds) while maintaining a continuous readout of the image signal charges being accumulated by the CID at standard TV video rates. The incorporation of this mode was augmented by the addition of three significant hardware elements, a thermo-electric cooler, video threshold detector, and AGC. The thermo-electric cooler is used to cool the CID, thus maintaining dark current integration at a reasonably low value during the three second maximum integration period. Thermal electric cooling involved a thermal design study and an iterative mechanical design to achieve a compromise between dark current levels (proportional to CID temperature) and the size and weight of the camera package. The video threshold detector determines when the accumulated signal charge is near saturation in the array and subsequently injects that charge starting a new integration period. (The threshold detector can be bypassed and a manual inject signal via a rear panel BNC connector can be utilized to control injection). The video AGC is utilized to maintain a constant video envelope. (peak to peak video swing during the scene integration/readout time.) (Note: The AGC can be used for both readout modes).

3.2 Scanning Technique

3.2.1 Resolution

Purpose: To develop a CID camera which simulates the resolution required by the EIA standards. To maximize the resolution available from the CID array.

Scope: To utilize various scanning and video processing techniques that significantly enhance the resolution of the CID array limited by reasonable hardware size.

Performance: Two selectable scanning modes are provided by the camera, "normal" and "synthetic interlace". A switch (S3) on the rear panel of the camera is used to determine which is used by the camera, the "normal" scanning mode produces the vertical scanning sequence as described by Figure 1A. The out of sequence line format for this mode comes about by the use of redundant data (which is available from the pattern noise rejection circuitry) for every other line in each field in combination with the standard interlaced TV display format. One would prefer to use a scheme (assuming a 244 line CID) which produced the vertical scanning sequence as described by Figure 1B. It is not practical to achieve this at the present time as evidenced in the results of our preliminary study. The practical alternate to this is the synthetic interlace mode (outerlace) which has the scanning sequence as in Figure 1C. Simply put, this mode is accomplished by elimination of the interlaced TV format (by not allowing the extra 1/2 line/field to occur) and by blanking out the out of sequence redundant information which is available from the pattern noise rejection circuitry. The result is a sequential presentation with no loss of unique video lines information (244 unique visable lines available/frame) and direct compatibility with standard TV monitors. For the "normal" scanning mode, video processing by the comb filter changes the video line sequence to that shown in Figure 1D. The effect on the "normal" scanning mode is that of interpolation and smoothness of the video information vertically from line to line. This results in a more subtle vertical aberration along with, as an added benefit, better pattern noise rejection.

3.2.2 Formatting

Purpose: To maintain EIA video standards assuring that the camera will be compatible with conventional TV monitors and video transmission characteristics.

Scope: To develop camera modes and circuitry with the intent of meeting EIA video standards for sync and video levels, interlacing, and scan rates.

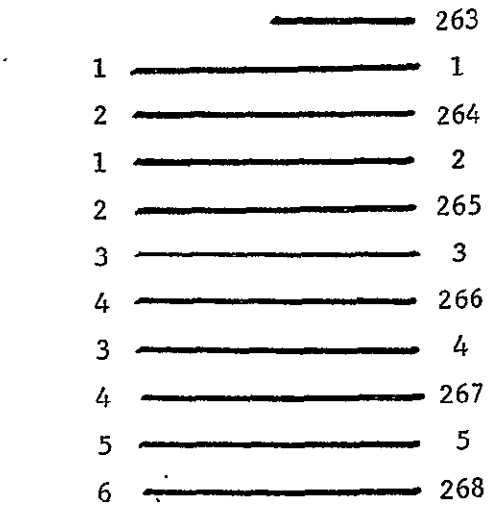


Figure 1A

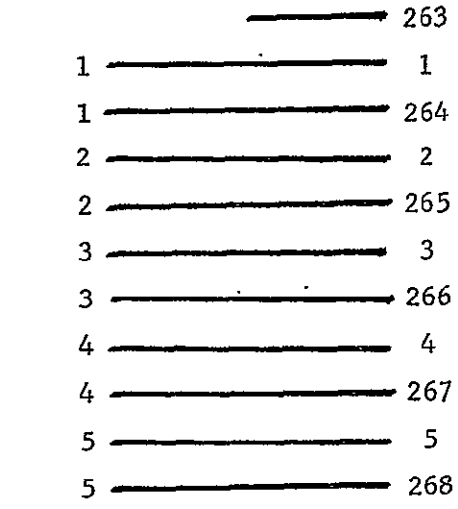


Figure 1B

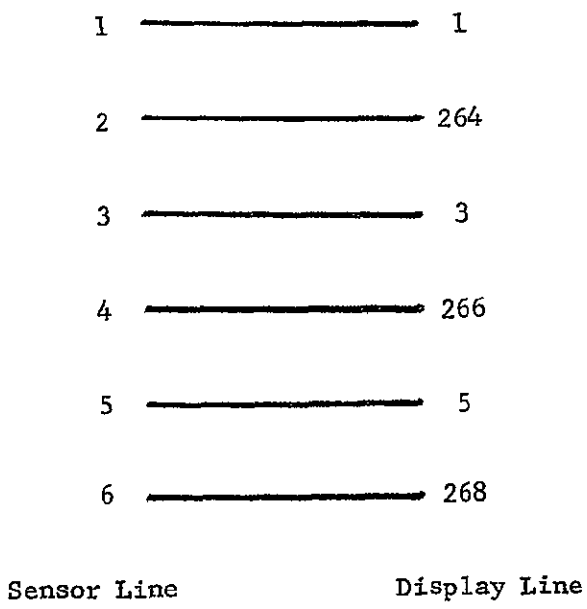


Figure 1C

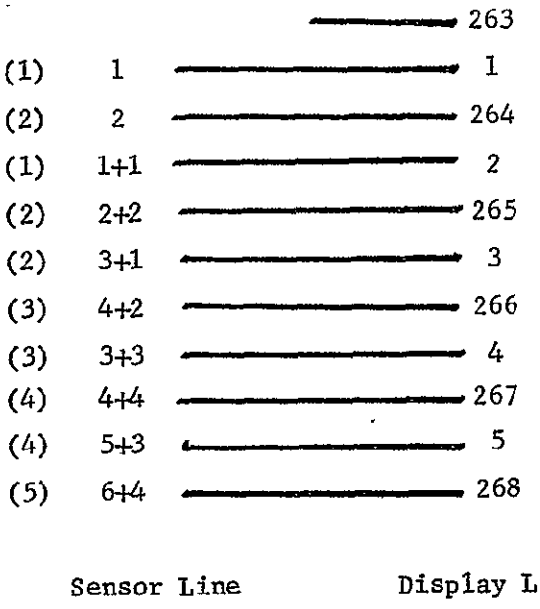


Figure 1D

Performance: The camera accomplishes the intent outlined in "scope" taking a small liberty in the way in which the sequential scan mode is accomplished. This particular mode poses no problem in compatibility with conventional equipment (.1% change in scanning frequency).

3.3 Design

3.3.1 Resolution

Purpose: To specify minimum resolution requirement for the CID matrix and to assure that EIA standards are met.

Scope: To maintain a nominal array size no smaller than 250x250 elements. To maintain compatibility of synthesized lines with EIA positive interlace format.

Performance: An array size of 244 lines x 248 elements/line was chosen as the only reasonable alternative which could meet or exceed the minimum nominal requirement of 250x250 elements. This array selection resulted from a best fit between required resolution, array availability and baseline circuit design availability. The EIA positive interlace format is met where possible, the intent of this standard (i.e. compatibility) being met for all modes of the camera.

3.3.2 Interlace Ratio

Purpose: To assure interlace compatibility.

Scope: Specify interlace ratio of 2 to 1.

Performance: Interlace ratio is 2 to 1 with the exceptions as outlined previously.

3.3.3 Aspect Ratio

Purpose/Scope: Specify an aspect ratio of 4 horizontally by 3 vertically.

Performance: The 244x248 CID array is designed with and provides an aspect ratio of 4 horizontally by 3 vertically.

3.3.4. Vertical Scan

Purpose/Scope: To specify that the vertical scan be nominal - 60 fields/second, 30 frames/second, and 525 lines/frame.

Performance: The vertical scan is nominal - 60 fields/second, 30 frames/second, and 525 lines/frame. A minor exception being the "sequential" scan mode where there are 524 lines/field.

3.3.5 Operating Light Ranges

3.3.5.1 Gray Scale Response

Purpose: To define the camera's ability to resolve scene contrast ratio and generate a proportional voltage to display same on a television monitor.

Scope: When the camera is activated under nominal conditions and a logarithmic gray scale with 10 steps (32:1 contrast ratio) is imaged onto the sensor faceplate with a highlight illumination as indicated below (via a standard reflectance-type gray scale chart), the camera shall resolve the 10 steps when its output is displayed on a suitable television monitor and shall exhibit a signal/noise ratio as defined in Section 3.3.11 and is indicated below:

Camera	Highlight Illumination (faceplate)	S/N Ratio (random noise)		S/N Ratio (fixed pattern noise)	
		Min	Design Goal	Min	Design Goal
244x248 Array	0.13 ft-c*	38db	48db	33db	43db

The illumination source shall be a standard tungsten lamp at 2854 K color temperature. *The highlight illumination shown corresponds to 1/2 the amount required for array saturation.

Performance:

Readout Mode	S/N Ratio (Random Noise)	S/N Ratio (Fixed Pattern Noise)
Normal pre-inject	39.6 db	33.6 db
NDRO	> 30 db	32 db

(Commentary on comparisons between specified and achieved. Great difficulty in making accurate NDRO measurements).

3.3.5.2 Dynamic Light Range

Purpose: To define the camera's ability to respond to varying light levels with a fixed lens iris setting. It must still retain the ability to resolve the 10 logarithmic gray scale steps (as described in 3.3.5.1) when the camera output is displayed on a suitable television monitor, over a range of illumination levels.

Scope: The test procedure is defined to be: 1) adjust lens iris setting to obtain maximum signal/noise ratio without exceeding array saturation; i.e., the highlight illumination reflected from the gray scale chart shall be within 10% of array saturation; 2) adjust lens iris setting until the 2 blackest shades of the 10 step gray-scale chart are no longer resolved on the monitor display (camera AGC functions to maintain constant signal output over this range); 3) calculate dynamic light range from the relationship:

$$\text{Dynamic Light Range} = \frac{f\# \text{ (loss of gray-scale)}}{f\# \text{ (saturation)}}$$

Dynamic Light Range specifications are as follows:

Camera	Dynamic Light Range Min.	Des.Goal
244x248 Array	7:1	14:1

This specification may be interpreted to mean that as a minimum, one can always adjust the lens iris one f stop in either direction without losing the ability to resolve any of the 10 logarithmic gray shades (with proper light level adjustment for nominal operating conditions).

Performance:

Camera	Dynamic Light Range	
Normal pre-inject	30.25:1	(F4-F22)

(Commentary on comparisons between specified and achieved).
(AGC performed extremely well - refer to photos 8 through 15).

3.3.6. Operating Voltage

Purpose: To assure primary power capability. To assure I/O control logic compatibility.

Scope: The camera shall operate with a nominal input voltage that is buffered such that standard TTL logic drive circuits can be interfaced with the CID sensor electronics.

The camera circuits shall be so isolated as to prevent noise from the power line or other circuits from appearing on the video output.

Performance: The primary power requirements for the camera and associated thermoelectric cooler power supply are nominal 115V AC 50/60 Hz. Electronic regulation is used to derive DC voltages used to power electronic devices internal to the camera. The distribution lines are additionally bypassed at each circuit card within the camera electronics assembly. Each circuit card has a ground plane in close proximity to its bottom side.

3.3.7 Power Consumption

Purpose/Scope: The design of this camera shall be such that power consumption shall be minimized.

Performance: (see 6.2)

Voltage	Power (watts)
115V AC Primary input to camera 50/60 Hz	27
115V AC Primary input TE cooler P.S. 50.60 Hz	≈20
+12V DC Camera electronics	4.5
-12V DC Camera electronics	4.2
+5V DC Camera electronics	3.3

3.3.8 Output Video Format

Sections 3.3.8.1 through 3 define the standard output video load impedance, composite picture signal, polarity, and signal levels required by EIA television broadcast standards. The current 244x188 prototype camera meets all these standards, and the proposed cameras will not deviate from them other than in the area of

Sync Signal Waveform (3.3.8.3). The timing relationships of the sync signals will depend upon the choice of scan format developed during the course of this program. There could be slight deviations from the RS-170 Standards; however, the deviations will not be sufficient to result in incompatibility with conventional TV monitors and transmission characteristics.

3.3.8.1 Standard Load Impedance

Purpose: To define and specify the video output impedance of the camera.

Scope: The standard load impedance is defined as the complex ratio of voltage to current in a two-terminal network, expressed in ohms. The output impedance shall be 75 ohms $\pm$5% over the frequency range of the camera and shall be connected for single-ended operation.

Performance: The measured impedance = 72.0 at J1, 75.6 at J4

3.3.8.2 Composite Picture Signal

The composite picture signal is the signal which results from combining a blanked picture signal (the result of the scanning process) with the synchronizing (sync) signal.

3.3.7.2.1 Polarity

Purpose/Scope: The picture signal polarity is defined as the sense of the potential of a portion of the signal representing a dark area of a scene relative to the potential of a portion of the signal representing a light area. Polarity of the composite is thus stated as "black-negative" or "black-positive". The standard polarity of the output of the camera shall be black-negative.

Performance: The camera is black-negative.

3.3.8.2.2 Signal Levels

Purpose/Scope: The levels of the composite picture signal shall be defined in terms of Institute of Radio Engineers (IRE) units. Reference white level shall be +100 IRE units; blanking level shall be 0 IRE units; sync level shall be -40 IRE units.

Thus, the peak-to-peak level of signal extending from reference white to sync tip shall be 140 IRE units.

The subject level shall be measured by means of an oscilloscope capable of measuring such a signal with the accuracy of ± 2% of the actual value over the voltage range of -0.5 to +1.5 volts. Some means of calibration shall be provided so that signal level measurements can be made in volts as well as in IRE units.

Measurements of signal levels shall be made in accordance with appropriate portions of 58 IRE 23.51 IRE Standards on Television: Measurement of Luminance Signal Levels, 1958, or latest revision thereof.

Performance: Composite picture levels 138 at J1, 142 at J4 IRE units/volts (see 6.3.2)

3.3.8.3 Sync Signal Waveform

The timing relationships of the sync signals shall depend upon the choice of scan format developed during this program as discussed above. Slight deviations from the RS-170 standard in the area of syn sync signal waveform are acceptable; however, these deviations shall not be sufficient to result in incompatability with conventional TV monitors and transmission characteristics.

3.3.9 Output Resolution Response

Purpose/Scope: In television systems, a measure of ability to delineate picture detail is resolution expressed in terms of the maximum number of TV lines (alternate black and white lines) per picture height discriminated on a standard test chart. The ratio of (1) the peak-to-peak signal amplitude, given by a test pattern consisting of alternate black and white bars corresponding to a specified line number (resolution), to (2) the peak-to-peak signal amplitude, given by large area blacks and large area whites having eh same luminance as the test pattern, is defined as the resolution response.

The methods of measurement shall be as specified in Institute of Electrical and Electronic Engineers (IEEE) 208, 60 IRE 23.52, Standards on Video Techniques: Measurement of Resolution of Camera

Systems, 1961 or latest revision thereof, be used. For the measurement of resolution response, the picture signal shall be applied to a picture monitor properly adjusted per the IEEE standard above. The limiting horizontal and vertical resolution response is determined by observing the point at which the individual lines of the graduated wedges are no longer distinguishable as separately defined images.

The horizontal resolution response shall not be degraded by the video processing chain of the camera systems, at least to an upper limit defined by the number of CID elements. The limiting resolution shall be no less than 70% of the number of TV elements - for example, for a camera system employing 250 horizontal elements, the limiting resolution shall be better than 175 TV lines per picture width.

Performance: Limiting resolution $\geq$175 elements. (See 6.5)

3.3.10 Output Video Voltage (Unblanked).

Purpose/Scope: The composite picture signal, as measured from the sync tip to reference white level across the standard load impedance (see Section 3.3.8.1), shall be nominally 1 volt peak-to-peak with the following component signal levels and tolerances comprising the total signal level.

Performance: Composite picture signal .990 at J1, .960 at J4 (see 6.3.2)

3.3.10.1 Blanked Output Video Voltage

Purpose/Scope: The blanked picture signal with setup (i.e., noncomposite), as measured from blanking level to reference white level, shall be 0.714 $\pm$0.1 volt (nominally 100 IRE units).

Performance: .738 at J1, .705 at J4

3.3.10.2 Synchronizing Signal

Purpose/Scope: The synchronizing signal, as measured from 0 volts dc shall be +0.286 $\pm$0.05 volts (nominally 40 IRE units).

Performance: .236 at J1, .240 at J4 (see 6.3.2).

3.3.10.3 Setup Levels

Purpose/Scope: The standard setup shall be 7.5 ±5 IRE units as measured across the standard impedance from blanking level to reference black level.

Performance: 7.5

3.3.11 Signal-to-Noise Ratio S/N

Purpose: To determine the S/N for nominal camera operation (i.e., highlight illumination at 1/2 that required for array saturation) shall be as outlined below. S/N for temporal noise sources (random noise) shall be determined by measurement on an oscilloscope, at the camera output, (across the standard load impedance) of the peak-peak noncomposite picture signal voltage and the peak-peak random noise voltage. S/N is the ratio of peak-peak signal voltage to rms $(\frac{\text{peak-peak}}{5.6})$ random noise voltage. S/N for fixed pattern noise sources shall be determined by measurement on an oscilloscope, at the camera output, (across the standard load impedance) of the peak-peak noncomposite picture signal voltage and the peak-peak fixed-pattern noise voltage across any one selected line of video. S/N is the ratio of peak-peak signal voltage to peak-peak fixed pattern noise voltage.

Scope:

	S/N (Random Noise)		S/N (Fixed Pattern Noise)	
Camera	Min.	Des. Goal	Min.	Des. Goal
244x248 Array	38db	48db	33db	43 db

Performance:

Camera Mode	S/N (Random Noise)	S/N (Fix.Pat.Noise)
Normal Preinject	39.6 db	33.6db
NDRO	> 30 db	> 32db

3.3.12 Geometric Distortion

Purpose/Scope: The TV camera geometric distortion exclusive of the lens shall not exceed a displacement of any picture element from its true position in the object being viewed by more than ±2% of the

picture height within Zones 1 and 2 and ±5% of the picture height within Zone 3. For any increment of 5% of the picture height, the rate of change of displacement of any picture element shall not be greater than 0.5% of the picture height. Zone 1 shall be defined as the area within an inscribed circule centered within the scanned area, the diameter of which is one-half the picture height. Zone 2 shall be the area included within an inscribed circle centered within the scanned area with a diameter equal to the picture height, but excluding the area of Zone 1. Zone 3 shall be the remaining area of the scanned picture outside of or excluding Zones 1 and 2.

3.3.13 Spots and Blemishes

Purpose/Scope: A spot or blemish shall be defined as a video signal transition of 7 IRE units or more in the output picture signal not present in the original scene, and which is the direct result of a sensor defect. The difference in sensitivity between any two adjacent CID elements in any direction shall be no more than 10%. Also, the difference in sensitivity from raster edge to edge (horizontally and vertically) shall be no more than 10%. No horizontal or vertical black lines resulting from a failed CID element shall be allowed. The size of a spot shall be determined by counting the number of scan lines on which the transition occurs; i.e., the number of lines per frame on which the transition is greater than 7 IRE units. The total of white and dark spots shall be less than or equal to:

10 spots $\leq$ 4 TV lines per frame

2 spots $\leq$ 8 TV lines per frame.

To determine the presence of spots, smudges, etc., a uniform grey background shall be observed which is illuminated by light source(s) of the appropriate color temperature and of the intensity to allow nominal camera operation (i.e., S/N shall not be such that spots and blemishes are masked by noise). Any gain operation by the camera shall also be considered.

Performance: See photograph #7

white spots 3 # black spots 6

3.3.14 Blooming

The solid-state image sensor is particularly susceptible to "blooming" - the spreading of an optical overload-generated charge into adjacent regions. The contractor shall propose various solutions to minimizing the blooming problem, incorporate the most acceptable solution into the camera, and include in the final report a detailed discussion of the solutions proposed and further work that may be done in this area.

Performance: See photographs #16 and #17

3.3.15 Camera Optics

Purpose/Scope: The camera shall be equipped with a lens with a fixed focal length between 25 mm and 50 mm with manual aperture and focus controls. The aperture control range shall be between f/2.2 to f/16 or better. The lens shall be mounted to the camera such that it will be interchangeable with other lenses. The lens shall be considered a part of the camera for all specifications herein. No development is intended in the optics area.

Performance: The camera has been equipped with two interchangeable lenses each optimized for a specific area of experimentation. A large F.85 to F11, 25 mm lens is provided for experimentation at low light levels, especially suitable where the camera is operated in the NDRO readout mode. A small F1.9 to F22 lens is provided for experimentation at high light levels. The recessed objective of this lens makes it suitable in applications of extreme side light intensities such as produced from large areas of high reflectance scene material.

3.3.16 Camera Controls

The camera shall be equipped with external controls that are accessible to the operator. The controls shall be so located, positioned, and labeled with sufficient size and contrast to allow ease of reading and operation.

Performance: See outline drawing

3.3.17 Camera Interfaces

Purpose/Scope: The camera shall include two connectors so as to facilitate the provision of camera power from one source and camera video to a standard commercial-type TV monitor. The contractor shall select the appropriate connectors to meet all the requirements of this specification. They shall be small with a minimum number of pins and and have a positive locking mechanism. Pin assignments are to be determined by the contractor.

Performance: A standard 115V AC chassis mount, 3 pronged male plug, J12, serves as the primary power input to the camera. All input and output signal interfaces are provided with standard female BNC chassis mount connectors (see 6.1).

3.3.18 Non-Destruct Readout Mode

A non-destruct readout (NDRO) mode shall be provided such that a video output signal meeting with requirements of this specification shall be atainable for all scene integration times up to and including 3 seconds for scene highlight illuminations of 0.1 foot-candle or greater. A selectable capability shall be provided that will allow either automatic integration cutoff at saturation or continuous integration (the minimum S/N specification shall not apply for the latter). To achieve the necessary low noise level for proper NDRO mode operation, a thermoelectric cooling device shall be incorporated which shall maintain the CID operating temperature at $0^{o}C \pm 5^{o}C$.

Performance: A measured temperature of $+4^{o}C$ was obtained with the CID and cooler exposed to room temperature and humidity. Refer to 6.1 for electrical performance.

3.4 Prototype Development and Test

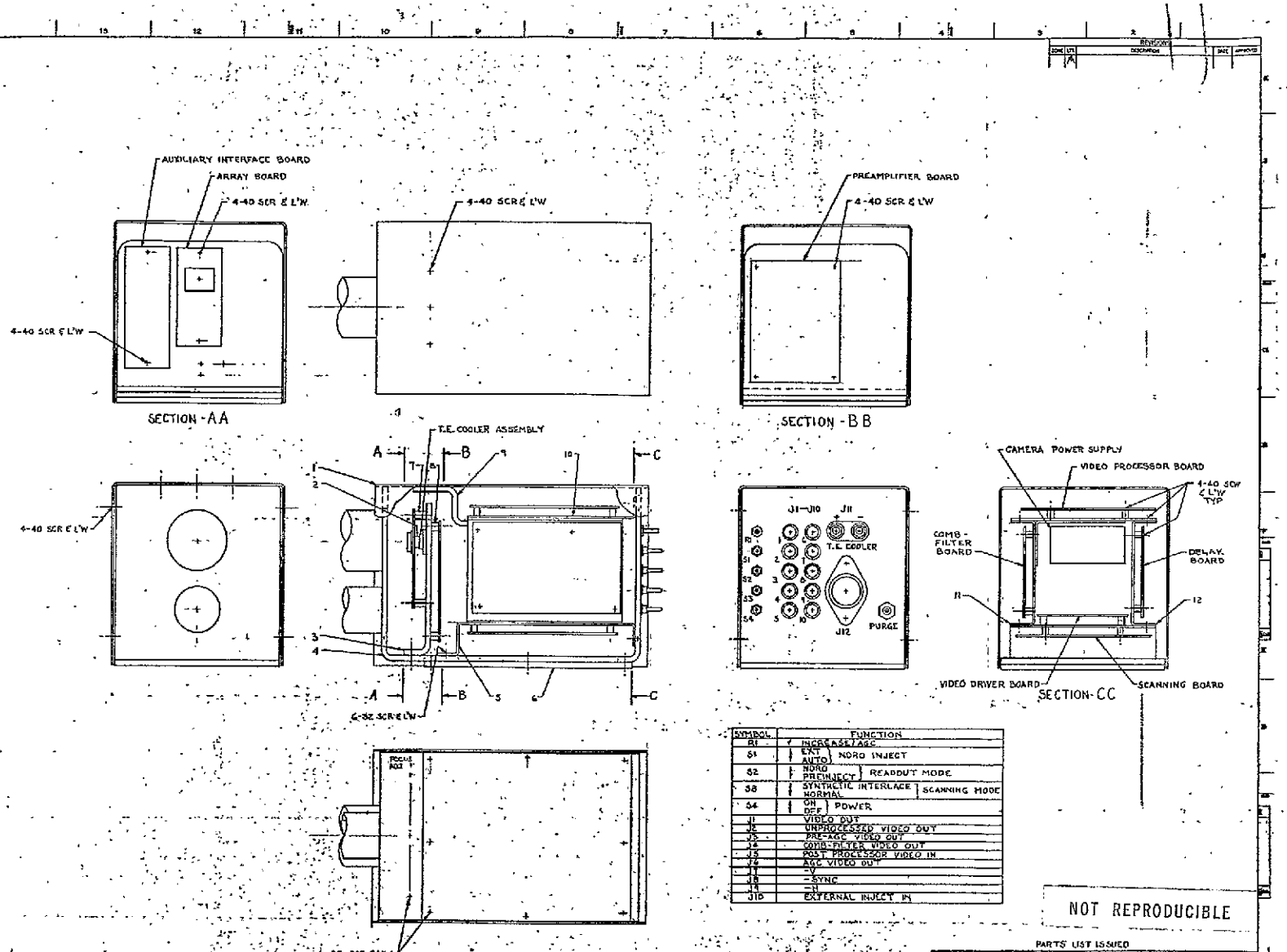
One prototype solid-state TV camera employing CID's as the image sensor which meets the design requirements of Section 3.3 shall be developed, tested and delivered to NASA/JSC.

Performance: Delivered 8/6/76.

3.5 Design Reviews

There shall be at least two (2) design reviews with the presentations to be held at the contractor site.

Performance: Design Review #1 - 12/75
Design Review #2 - 4/76



SYMBOL	FUNCTION
R1	INCREASE/AGC
S1	EXT / AUTO — NORD INJECT
S2	NORD PREINJECT — READOUT MODE
S3	SYNTHETIC INTERLACE / NORMAL — SCANNING MODE
S4	ON / OFF — POWER
J1	VIDEO OUT
J2	UNPROCESSED VIDEO OUT
J3	PRE-AGC VIDEO OUT
J4	COMB-FILTER VIDEO OUT
J5	POST PROCESSOR VIDEO IN
J7	AGC VIDEO OUT
J8	+V
J9	-SYNC
J10	-V
J11	EXTERNAL INJECT IN

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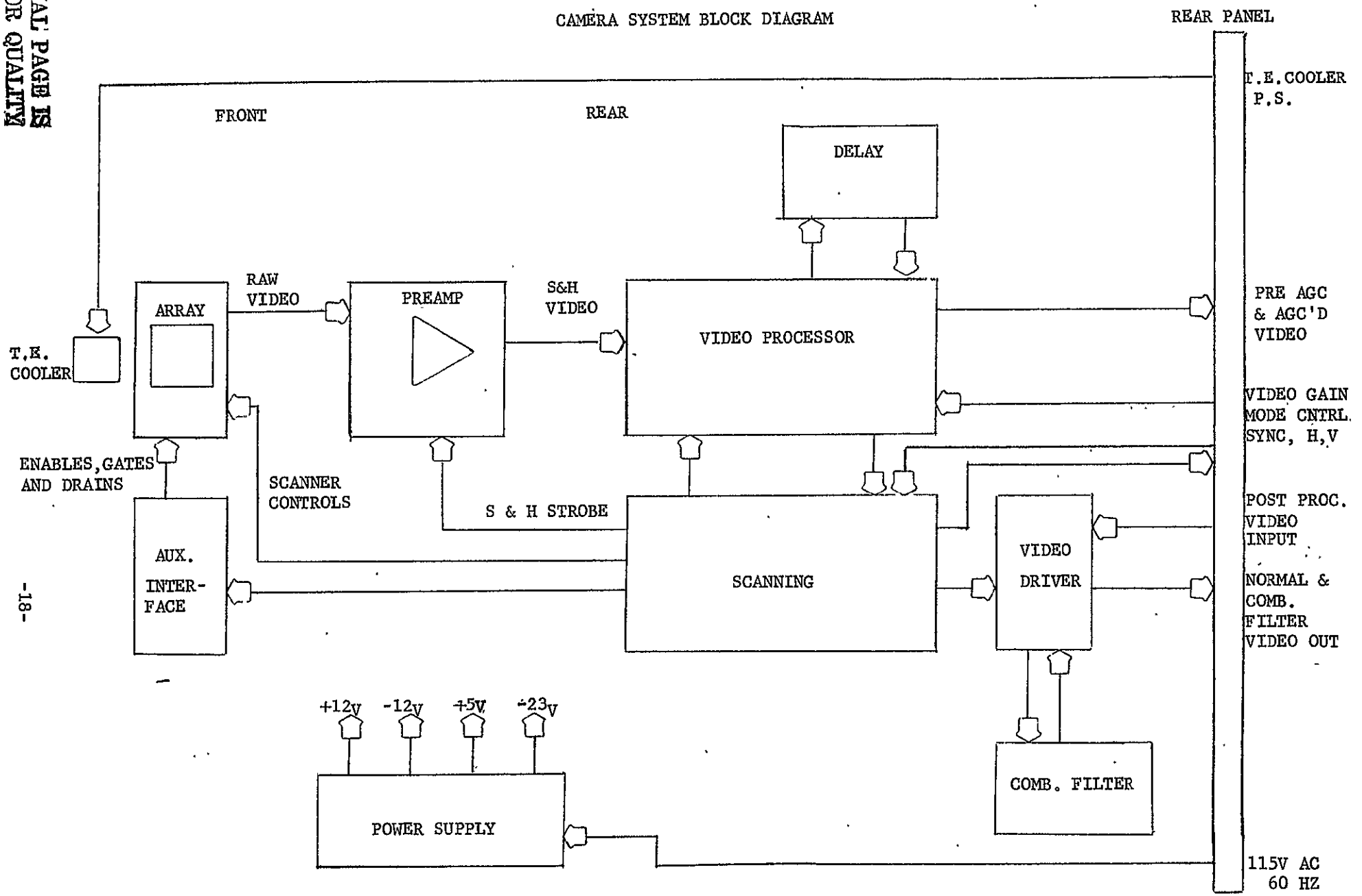

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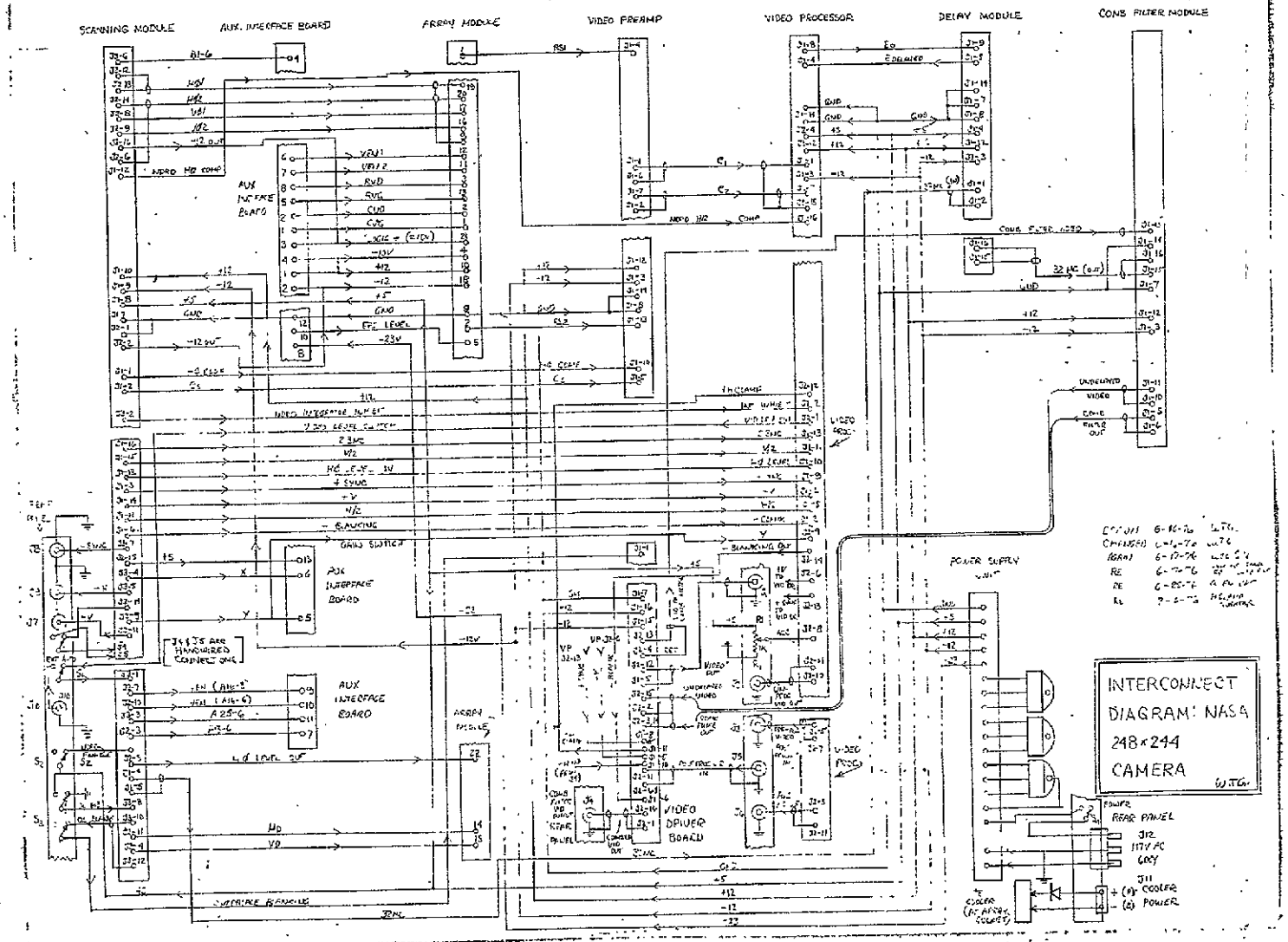

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4.0 Camera Operation

4.1 Preamplifier Board

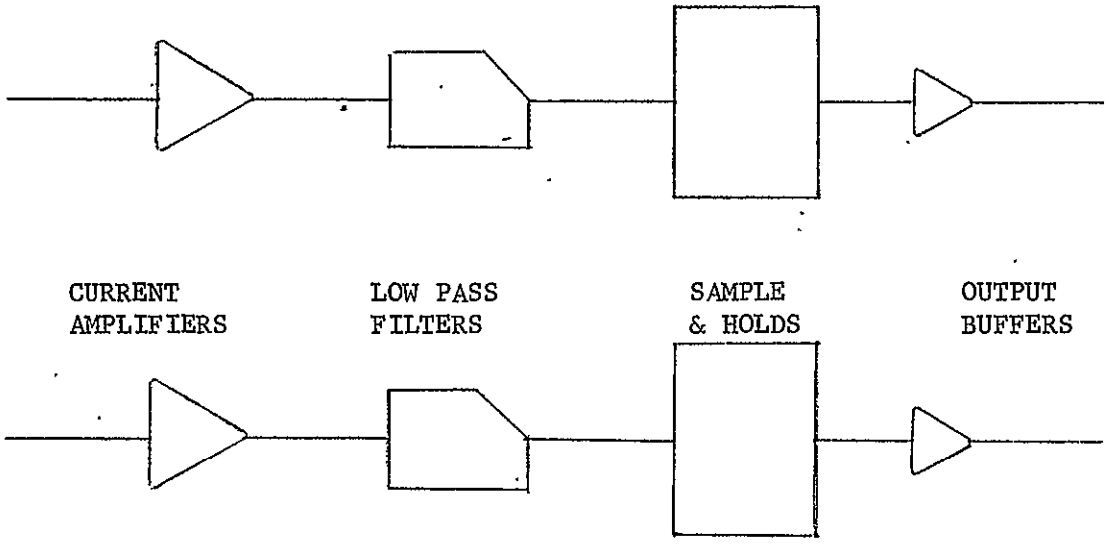
The preamplifier board contains two channels. One channel is connected to the "odd" columns of the array; the other to the "even" columns. Each channel is identical to the other. A pre-amp channel consists of a low-noise feedback type input stage, a filter section with buffers, and a sample-and-hold circuit. The input stage has a gain of approximately 0.67 V/μA. The equivalent RMS input noise is 0.62 nanoamps (measured with a 2 MC sharp-cutoff filter and a 39 pF capacitor to simulate the CID array capacitance).

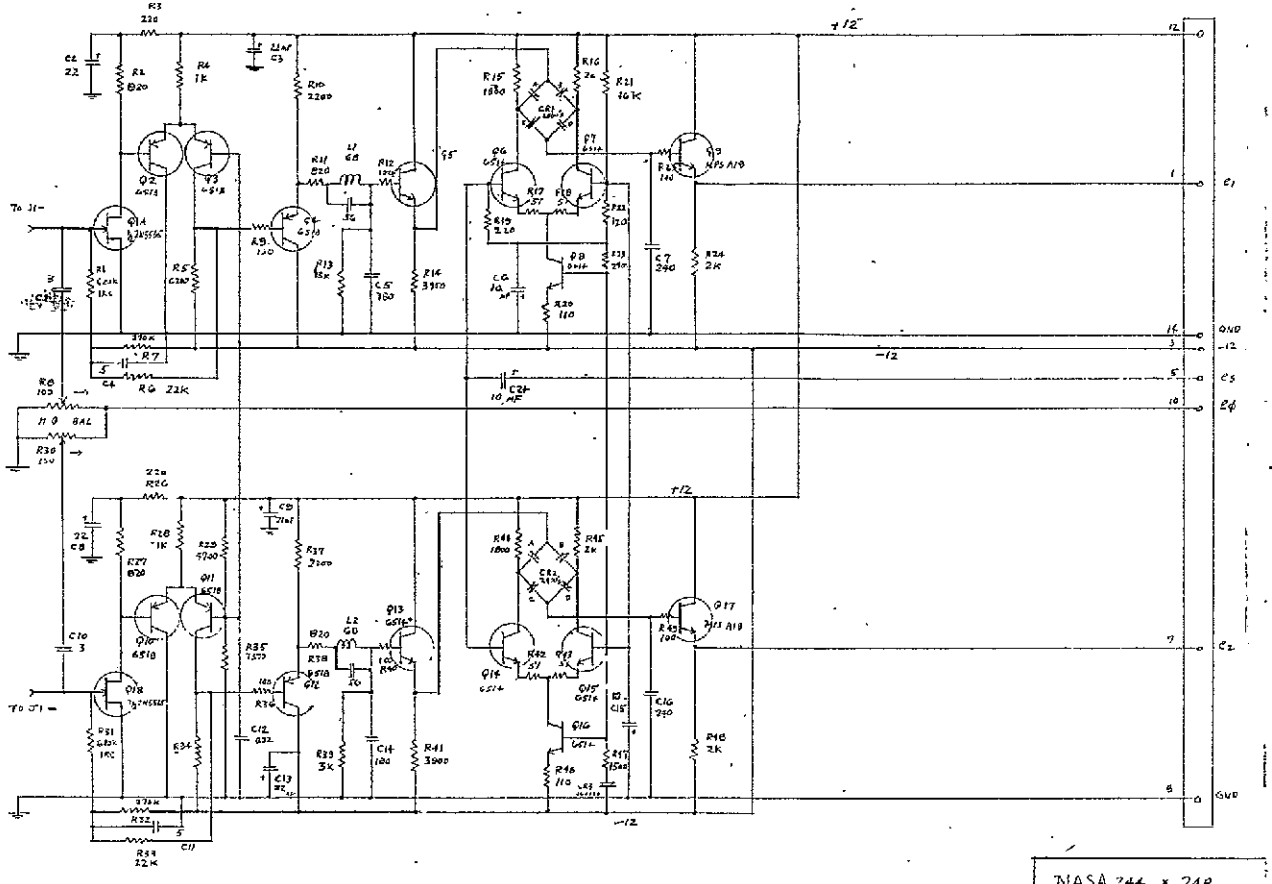
The input amplifier is followed by the filter section. Without this filter, the sampling wave at 2.3 MC will alias with noise voltages in the region of 2.3 MC and low frequency "difference" signals will appear in the output of the samples. These noise voltages, being low frequency, are very objectionable when viewed on a display monitor. To minimize this "conversion noise", a filter with the response shown in Figure 1 is used which has high attenuation at the sample frequency. As seen in Figure 1, a step wave passed through such a filter has rather slow rise time. It is necessary, therefore, to delay the sample pulse almost the full element period so that the full MTF of the CID can be realized.

The filter has about 10% overshoot but the time delay of the sampling pulse is chosen to occur as the signal is just passing through the 100% point. As a result, the overshoot is not reproduced in the sampled output.

The sampling circuit is designed to provide fast acquisition time (60 nanoseconds) and with minimum feedthrough of the sampling gate pulse. The feedthrough spikes are ± 8 MV in amplitude and are about 10 nanoseconds wide. These spikes, although small to begin with, are filtered out by the 3 MC low-pass filter in the processor.

VIDEO PREAMPLIFIER BOARD





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4.2 Video Processor

The two pre-amp signals e_1 and e_2 are fed to the processor module where they are multiplexed together in a way that provides the lowest possible noise. A block diagram is shown in Figure 2 and the signal waveforms in Figure 3. Signal e_1 is delayed for a 220 nanosecond delay line - the period of an element. This delayed signal, e_{1D}, is then added to e_2 to form the signal shown in Figure 3a. The waveform used, indicates the output of a vertical white bar or window scene. The two singals add directly whereas the noise voltages, from 2 separate preamps, add inquadrature. The S/N of the combined signal is therefore 3 db better than each preamp by itself.

Referring again to Figure 2, e_{1D} and e_2 are subtracted, yielding the waveform of 3b. In this case the low frequency video is cancelled leaving only edges or transitions as shown. Noise is not cancelled, however, so this "edge" signal is fed through a base-line clipper which removes the noise (random noise and pattern noise) except during edges or transitions (see Figure 3c). The result is that large flat areas of the TV image, where there is no detail, will have little or no added noise.

The wave of Figure 3c could be used directly to correct the rise time of 3a. Instead, additional pulse shaping with an R-L-C circuit forms the wave of 3d which is then added to 3a as shown. A pot controls the amount of correction and the picture may be slightly over-corrected if desired to optimize subjective sharpness in the final picture.

A 2.4 mc switching voltage, in phase with the sampling pulse, is required to keep the HF correction wave polarized properly when the image transition moves from an odd to an even column, or vice versa.

The combined signal of Figure 3e is amplified and routed to a 1-H delay circuit which is used to cancel pattern noise*. A block

---

*The video crosstalk term which appears with pre-inject readout is also cancelled by the delay line circuit.

diagram is shown in Figure 4 along with the pertinent waveforms. Each line of the imager is read twice. The first "read" contains the signal plus pattern noise as indicated by the arrows in Figure 4. The second read contains only pattern noise. The input signal is delayed by exactly one horizontal line period and is subtracted from the undelayed signal. Since the pattern noise is the same on each line, it is cancelled out. The video signal is not cancelled since it only appears on alternate lines. The delayed video at this point could be thrown away or, as in this case, inverted again and added to the real-time video as shown in Figure 4e. A subtle advantage of doing this is as follows: any residual pattern noise not completely cancelled by the delay line appears in opposite phase on alternate horizontal lines and provides additional optical cancellation of the pattern noise. This has been indicated by the single arrows of Figure 4e.

The remaining video processor functions are DC level setting via keyed clamps, video gain, blanking addition, blanking clipping, white level clipping, sync addition and a 75 ohm output for the normal video output. Additionally, three other functions are provided. An analog switch is employed to blank redundant video lines for the synthetic interlace scan mode. An AGC function is provided which, via back panel connections, can be used or bypassed for all modes. The mean value of the AGCed video signal may be controlled via the AGC threshold control, also located on the back panel. An NDRO inject circuit is provided to control image charge injection during the NDRO readout mode. It is essentially a video level detector which produces a logic "1" level when the average video level reaches a certain presettable value (on inject). When used, the AGC output from the video processor board is routed, via rear panel connections (J6 to J5), to the video driver board where white level clipping, blanking and sync addition is incorporated into the video waveform.

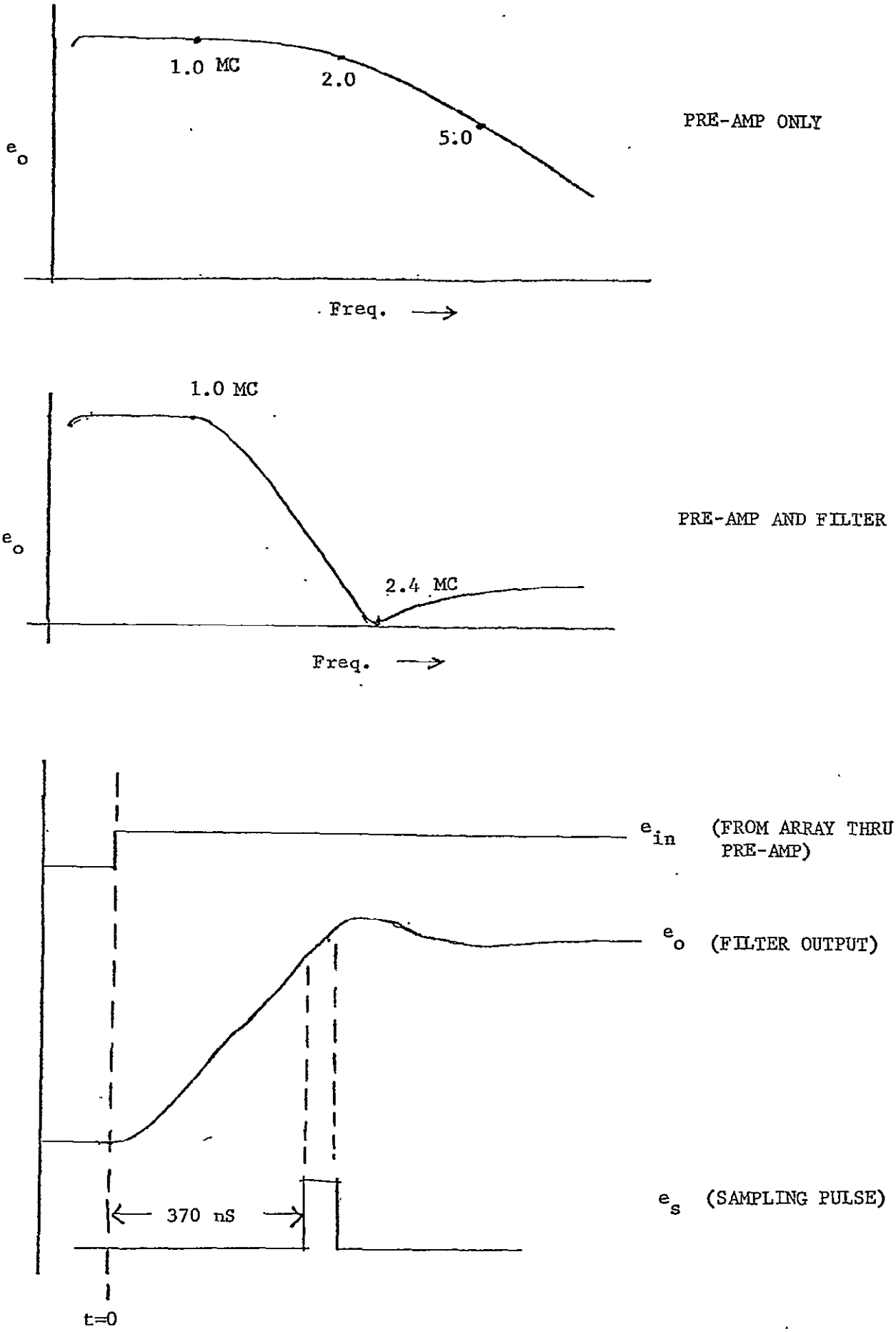


Figure 1. Response of Pre-amp With and Without Filter.

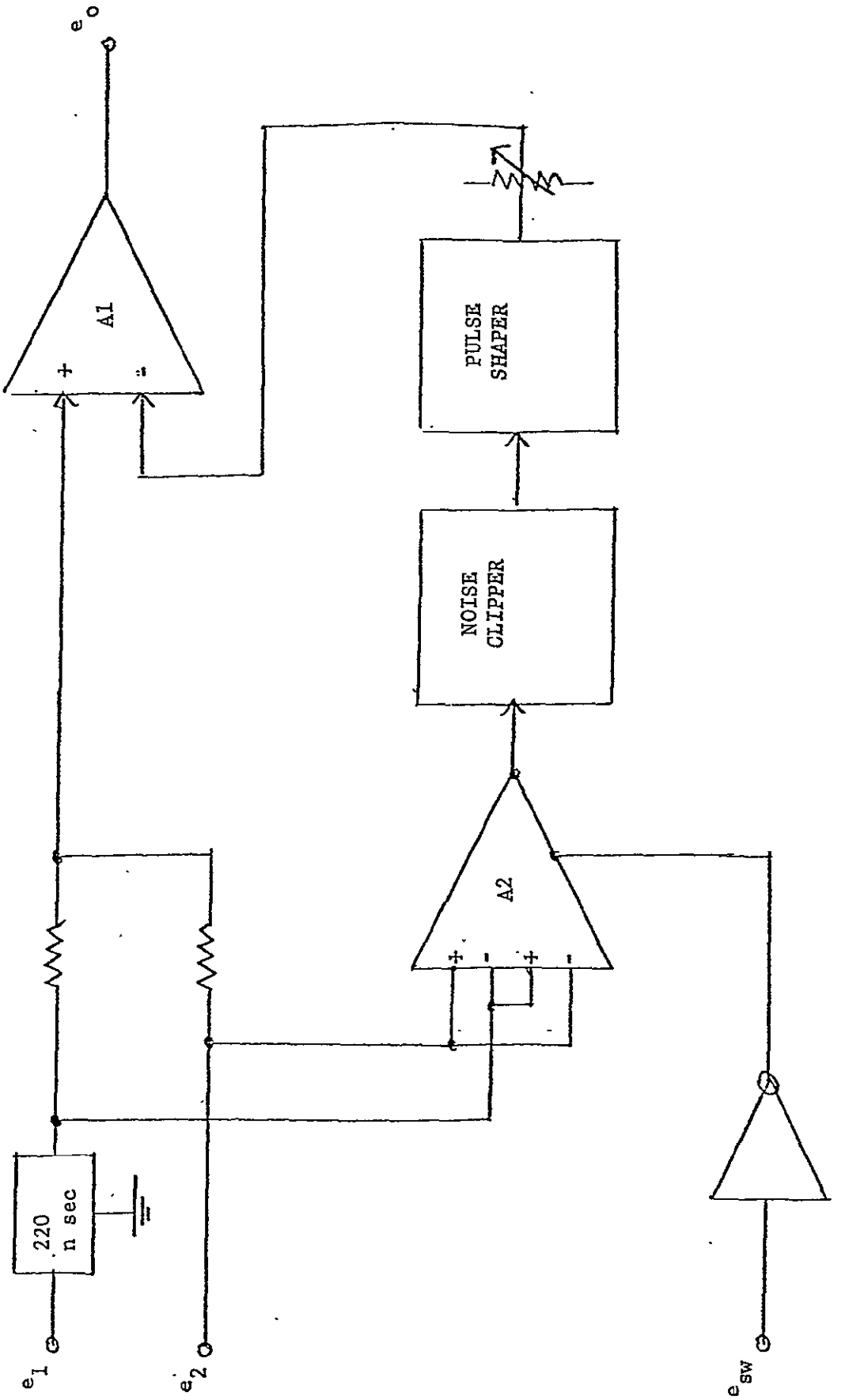


Figure 2. Block Diagram of Processor Module Showing the Multiplexing of the Two Pre-amp Signals.

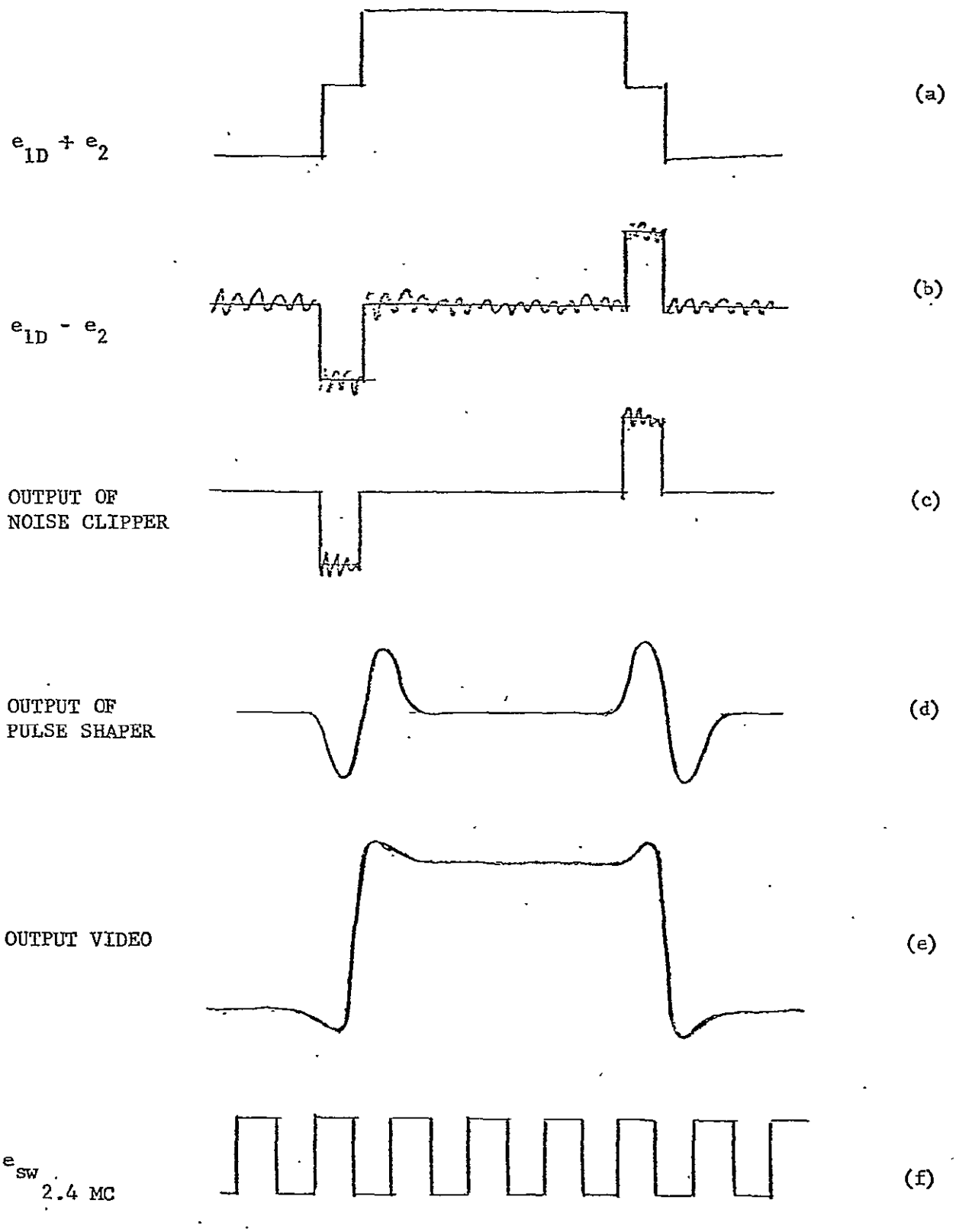


Figure 3. Waveforms in the Processor Module

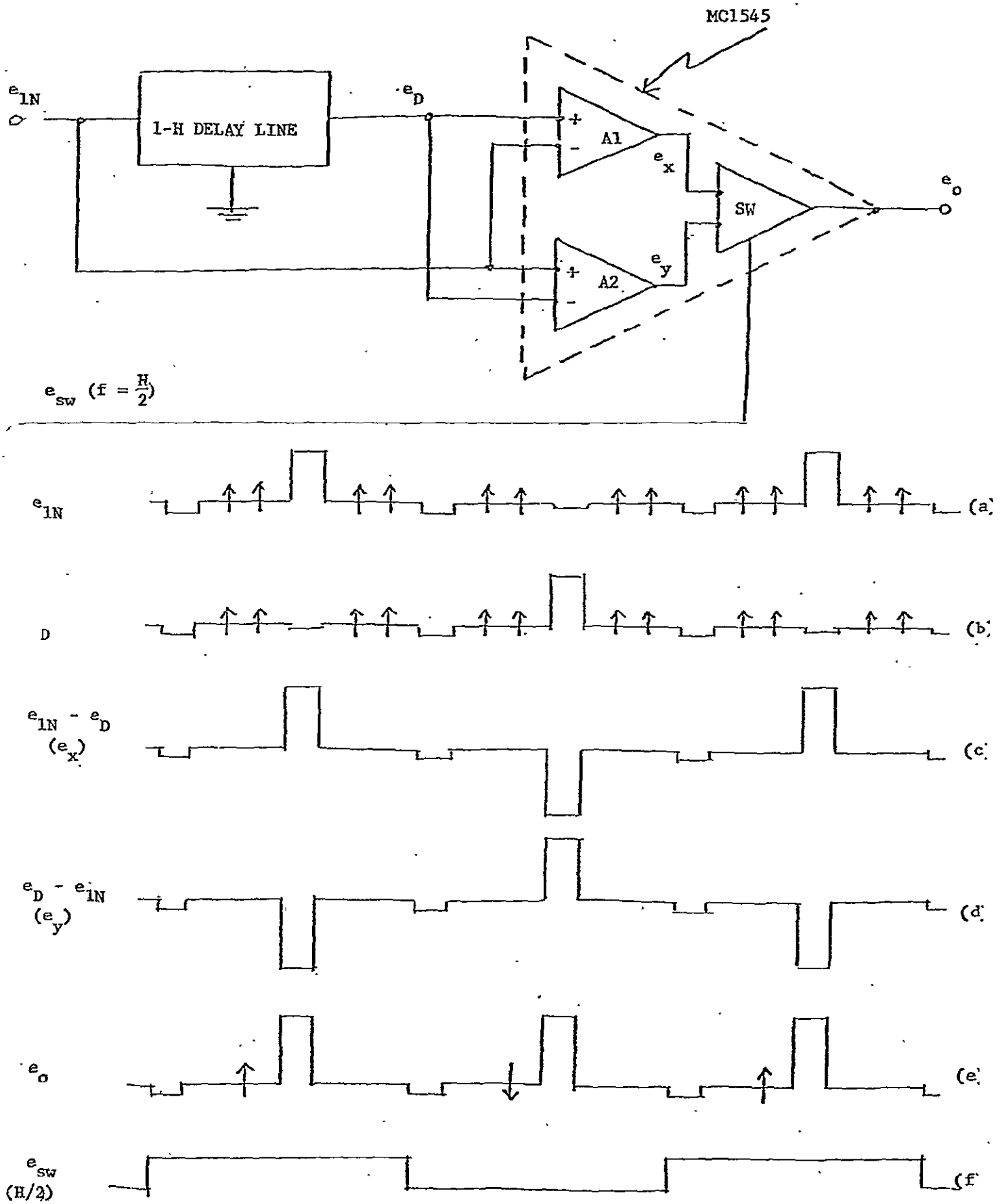
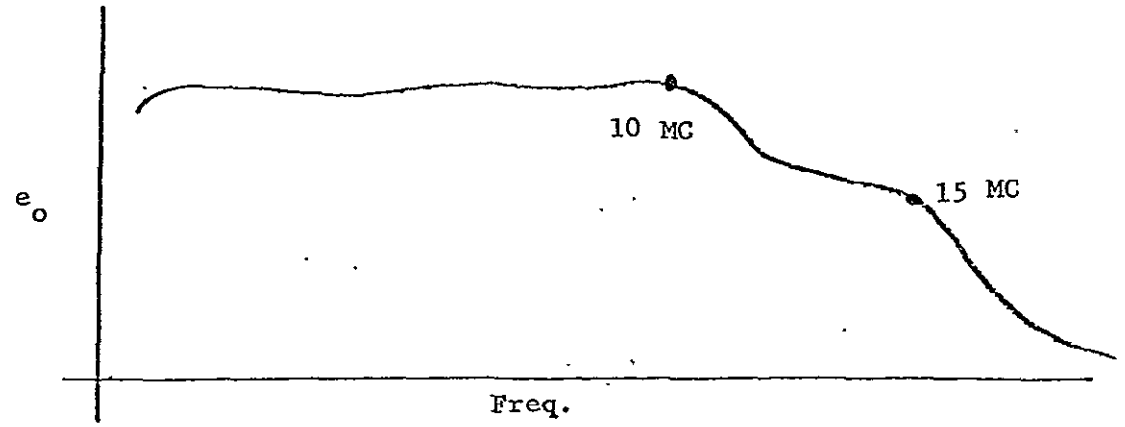
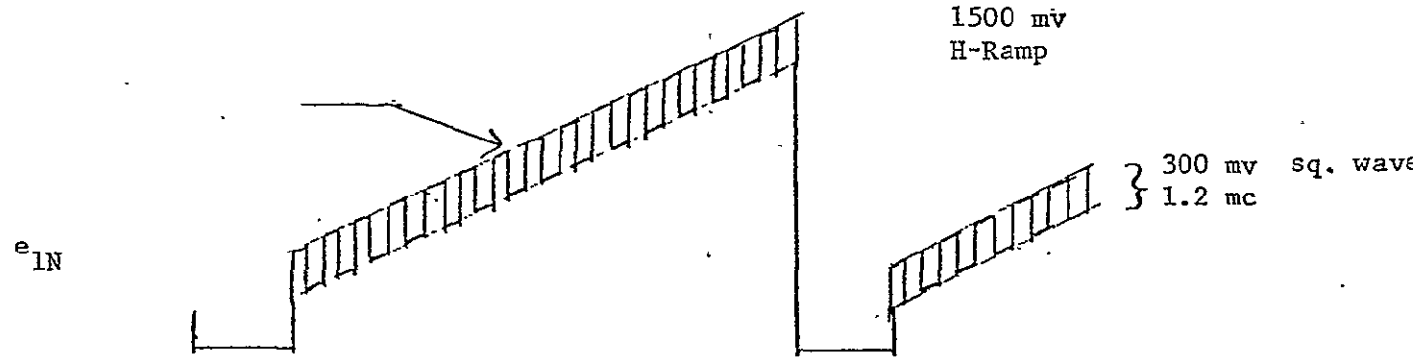


Figure 4. Block Diagram of Circuit Used to Cancel Fixed Pattern Noise Along with Pertinent Waveforms.



DELAY CHANNEL FREQ RESPONSE



DIFFERENTIAL GAIN + PHASE TEST SIGNAL

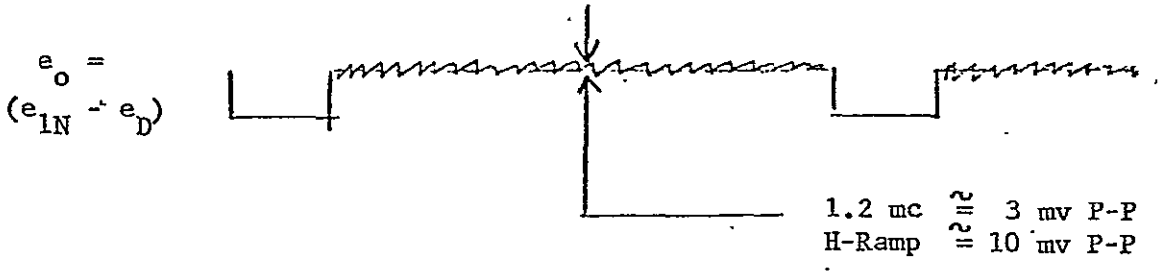
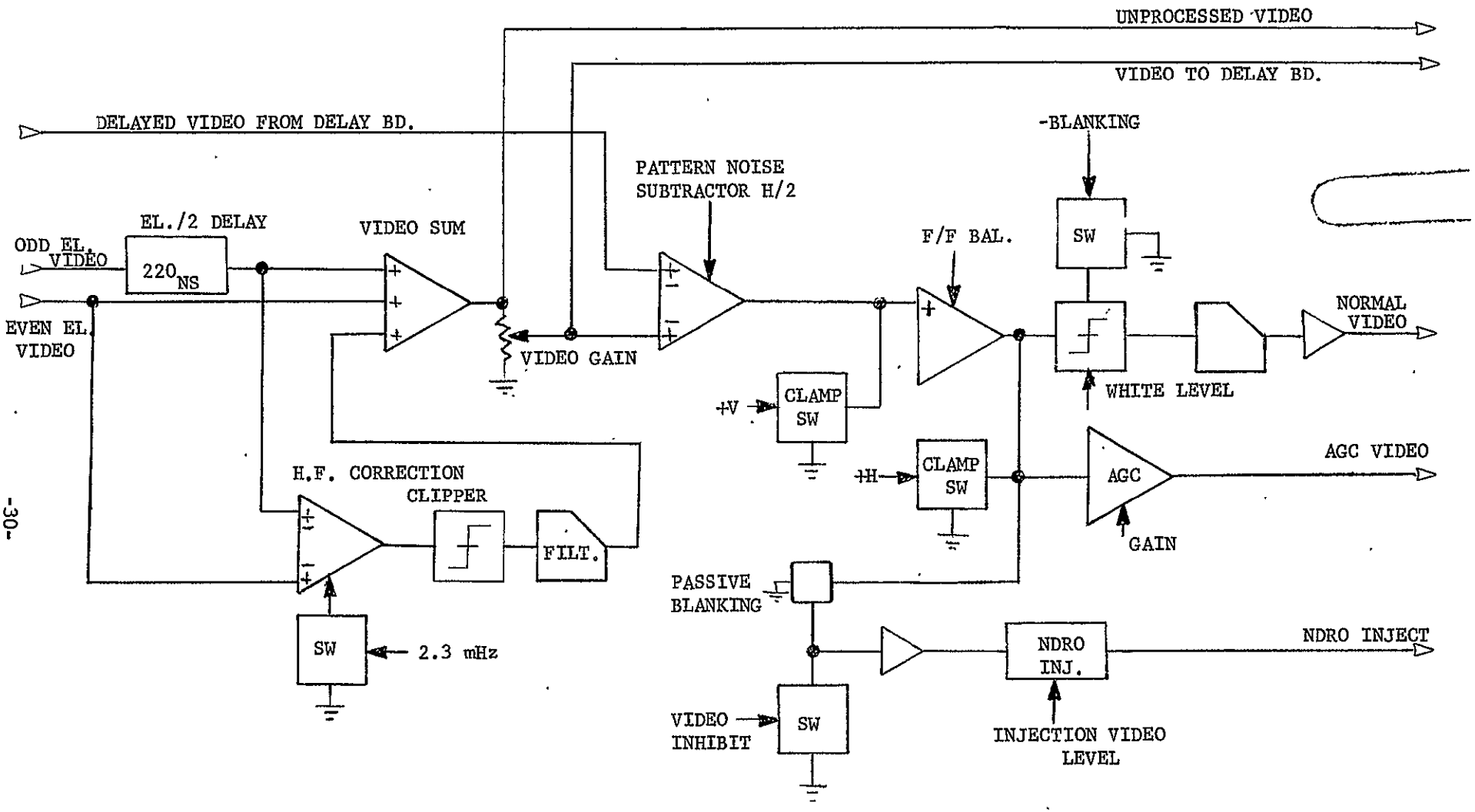
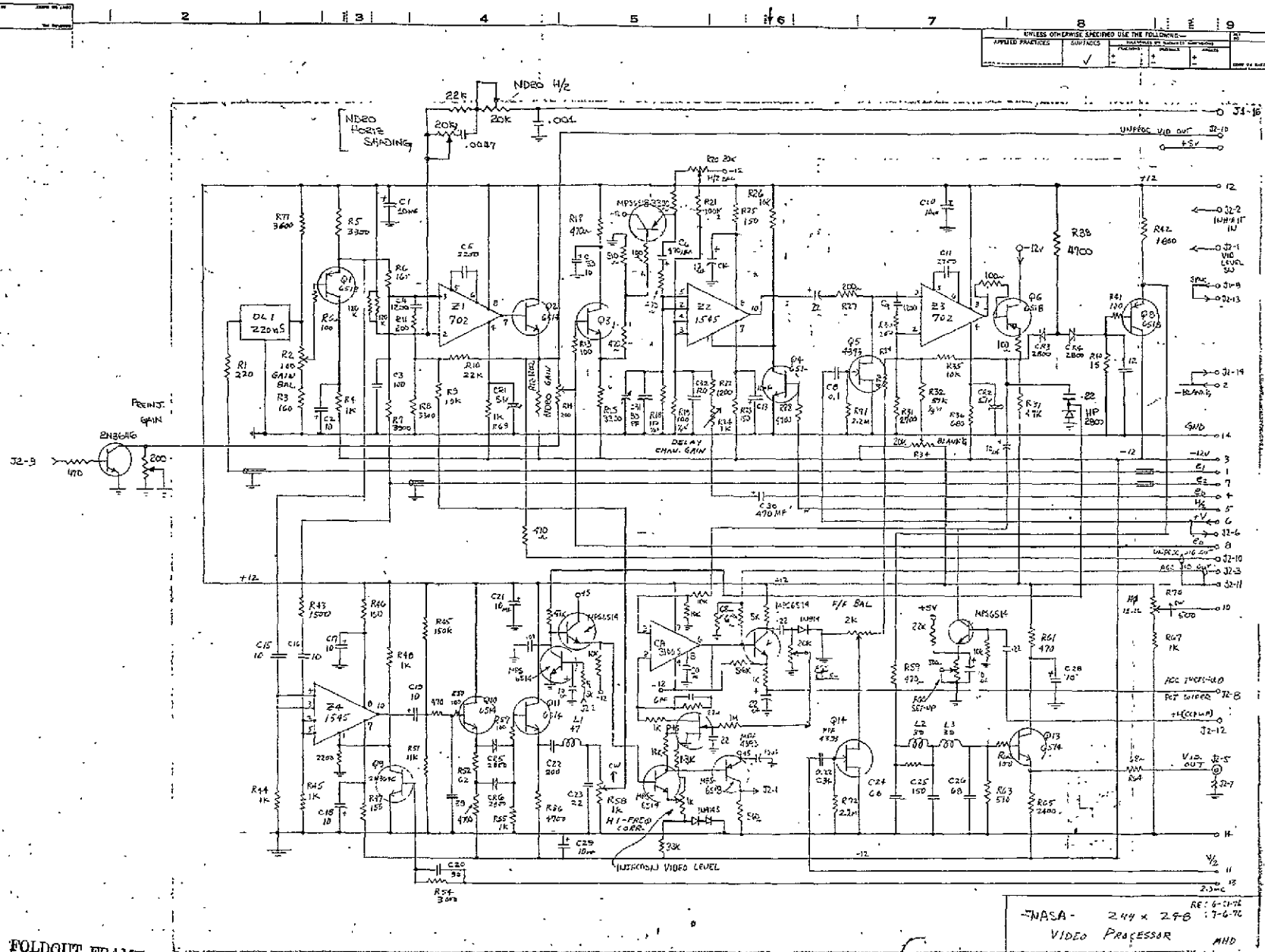


Figure 5. Delay Channel Frequency Response.



VIDEO PROCESSOR BOARD



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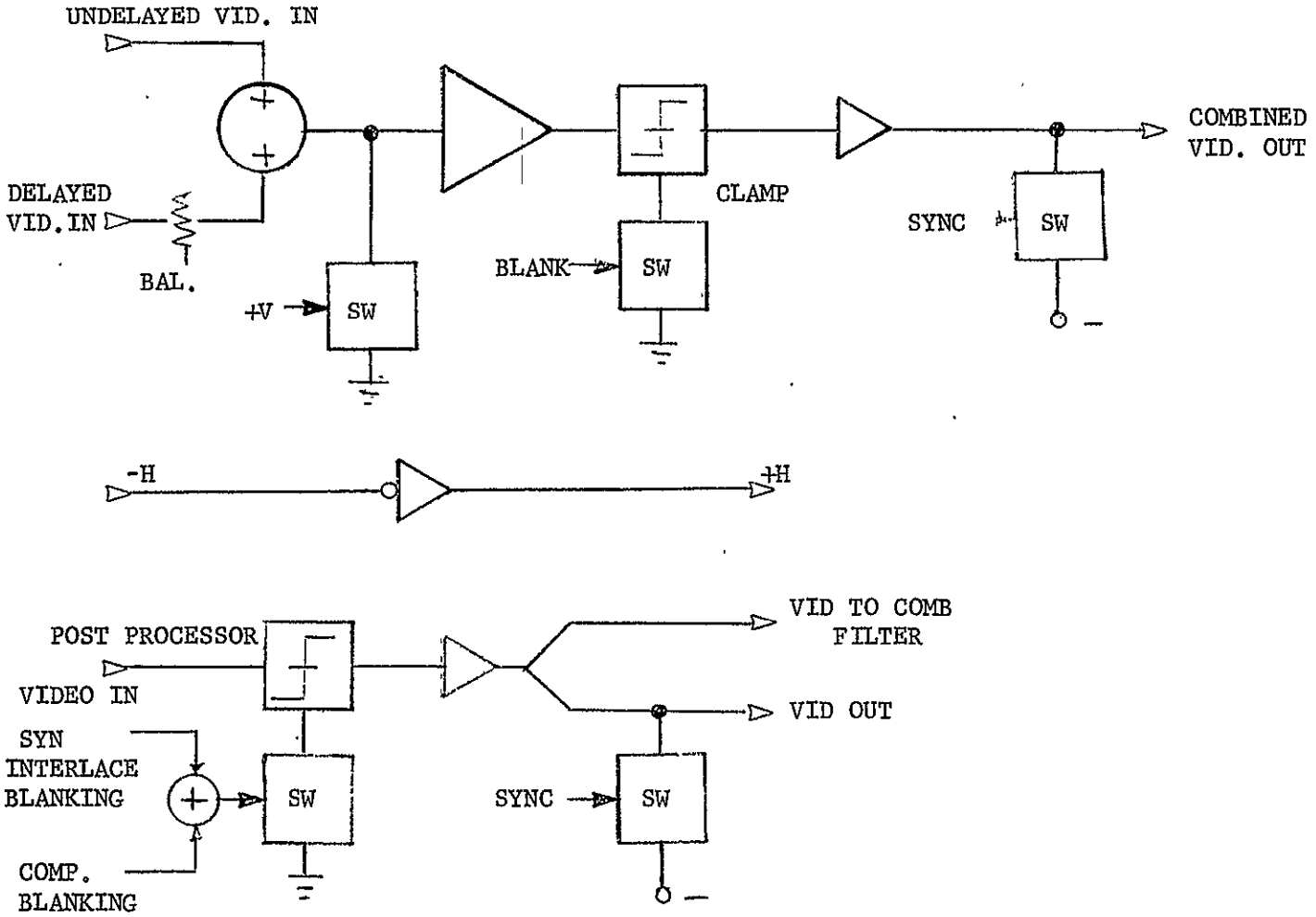
VIDEO PROCESSOR MHD

-31-

4.3 Video Driver Board

The video driver board has the functions of video buffering and comb filter processing. The two primary video output signals provided at the rear of the camera, J1 - "Video Out" and J4 - "Comb Filter Video Out", are buffered on this board.

Sync and blanking is incorporated into these waveforms along with a 75 OHM driver for each output. Also located on this board is a buffer for the video sent to the comb filter board. The comb filter processor operates by summing the 1H delayed video from the comb filter board with undelayed video, thereby adding together alternate video lines within each field. There are two benefits in using the comb filter. During the normal scanning mode of operation, it softens the vertical aberration due to out of sequence lines. This is due to the averaging function that occurs which smoothes and interpolates line information in a nearly proper sequence. The other benefit lies in the fact that the residual pattern noise not removed by the video processor has the characteristic of having opposite phase (180°) on alternate lines. When the alternate lines are summed together, this residual pattern noise is considerably reduced.


UNDELAYED VID. IN
DELAYED VID. IN
BAL.
+V
SW
BLANK
SW
CLAMP
SYNC
SW
COMBINED VID. OUT
-H
+H
POST PROCESSOR
VIDEO IN
SYN INTERLACE BLANKING
COMP. BLANKING
SW
SYNC
SW
VID TO COMB FILTER
VID OUT

GENERAL ELECTRIC

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
	✓	FRACTIONS ±	DECIMALS ±	ANGLES ±

TITLE: VIDEO DRIVER BOARD

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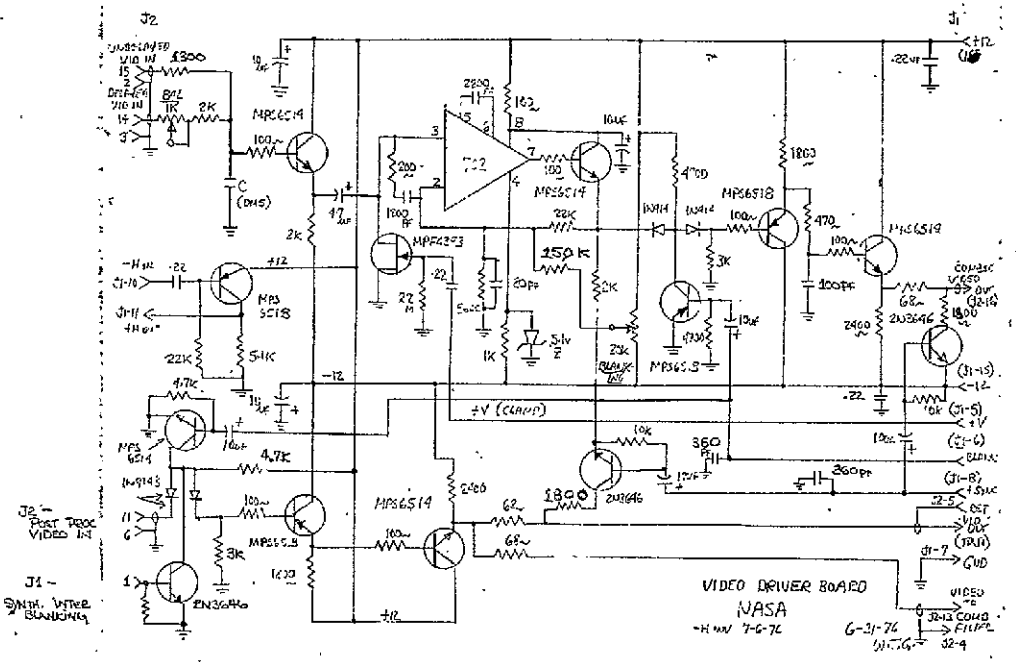

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4.4 Delay and Comb Filter Boards

The delay and comb filter boards are identical with the exception of the 32 MHz crystal oscillator which is contained on the delay board and not on the comb filter board. To achieve the performance necessary for good noise cancellation, the following requirements are critical:

Exact 1 H delay

Stable delay time

Faithful impulse response

Very low amplitude distortion (differential gain)

Very low differential phase distortion

Low self-generated random noise.

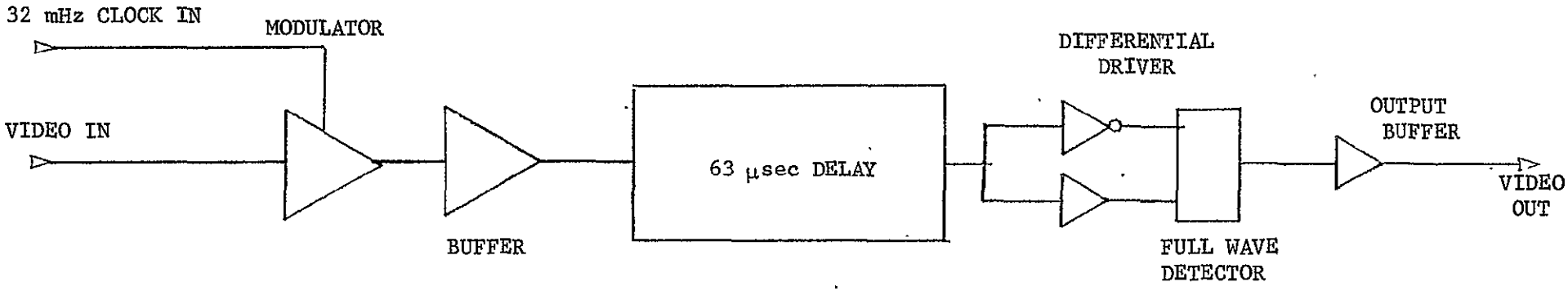
These requirements are most nearly fulfilled by a zero T. C. glass delay line. The video signal is AM modulated onto a 32 MC carrier which is generated by a crystal oscillator. This same frequency is divided down and used to generate the various voltages required to scan the CID. In this way, any possibility of beat-frequencies is eliminated.

The modulated carrier is then amplified and fed to the delay line. The line has about 30 db of loss so that additional amplification is required before demodulation. The demodulator is a full-wave type using hot-carrier diodes. This circuit was found to have lower differential gain and phase distortion than some integrated circuit types. The response of the entire delay channel is shown in Figure 5. It is flat to 10 MC; down to less than 6 db at 16 MC. This response is considerably broader than the 2-1/2 or 3 MC needed for the video information. However, to faithfully reproduce the shape of the pattern noise, which is needed for maximum cancellation, a wide bandwidth is required. Figure 2 also protrays a differential gain and phase test signal similar to that used in standard television systems. In this case, the H-ramp simulates a low frequency

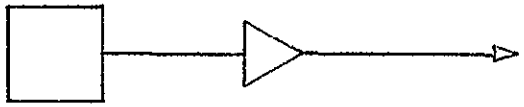
video signal which covers the full amplitude range. The 1.2 MC square wave, which is added to the ramp, simulates the pattern noise from the imager.

Such a signal was fed through the delayed channel and subtracted from the undelayed signal. The pattern noise cancellation over the entire amplitude range was 100:1. In earlier camera designs, this ratio was 15:1.

COMB FILTER/*DELAY BOARD



*(DELAY BOARD CONTAINS CLOCK GENERATOR BELOW, IN ADDITION TO ABOVE DELAY)



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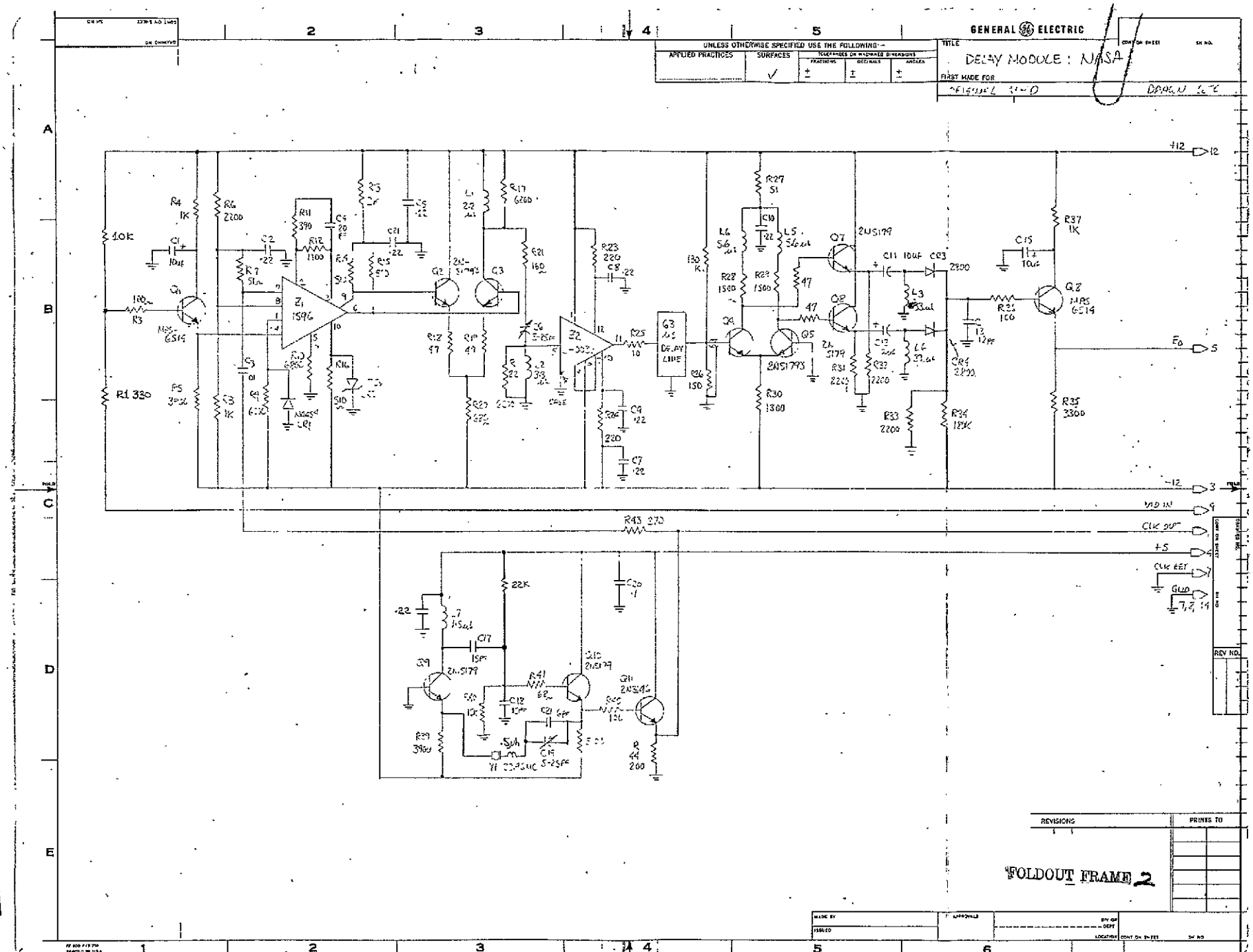

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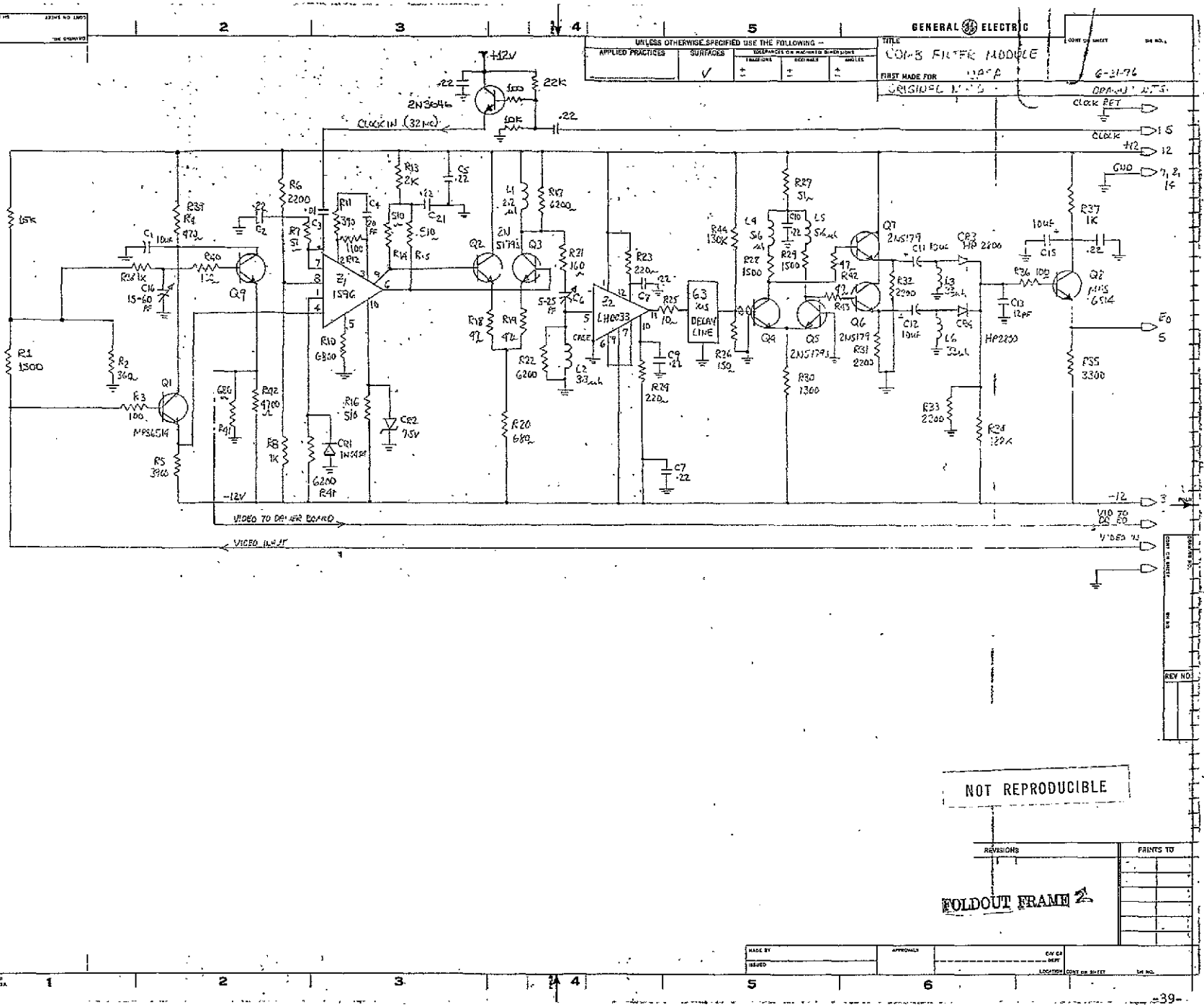

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4.5 Scanning Board

The scanning module consolidates circuitry used to generate scanning logic required by the CID imager, clamp, sample and other pulses required by the analog signal processing loop, and synchronizing and blanking pulses applicable to closed circuit TV systems.

Essentially, the scanning module consists of three sections:

a) A counter and multiplex circuitry which generates the imager horizontal phase (Ø) pulses, processor loop sample pulses, a 2.4 MC switching voltage, and a 2 MC sync generator clock.

b) The TV horizontal and vertical rate section, employing a 3262 ADC MOS sync generator chip and appropriate processing logic to produce imager H and V data pulses, vertical phase (Ø) pulses, vertical enable pulses, and a row load device gate signal - as well as synchronizing, blanking, and field and line rate pulses required by the Camera Video Processing System.

c) Assorted logic for performing readout and scanning mode changes, and for controlling injection during the NDRO mode.

A) The counter section is comprised of devices A2, A3, A4, A5, A6, A7 and portions of A1 and A12. 32 MC clock pulses generated on the delay board are applied to cascaded sections of A2 and A3 (divide by 16). The resulting 2 MC square wave is applied to the sync generator chip (discussed later). A 16 MC square wave (clock divided by 2) is brought out from A2a and is applied to a divide by 7 counter consisting of A4, A5, and A6. The Q1 through Q6 outputs of A4, and the Q(7) output of A5 have a duration of 61 ns and are delayed from the previous Q output by a 61 ns period (see Figure 6). A6 multiplexes the outputs to derive a data pulse which resets the counter at the end of the 7th interval.

The Q7 output of the counter (2.4 MC) is applied to A5b (divide by 2) deriving the 1.2 MC square wave and its complement which become the HØ pulses. Note that counter output Q7 "times" the HØ interval (Figure 6). The Q6 output of the counter occurring at the end of the

HØ pulse, is inverted in A1a, becoming the system sample pulse. A7a, in conjunction with A1b, and A1, generates the 2.4 MC high frequency gate signal used in the video processor module. The sample pulse rise initiates the sync wave; the inverted output of A12 which represents Q1-1/2, ends the period (see Figure 6).

B) The horizontal and vertical rate section of the scanning module processes various A8 (sync generator) outputs to obtain additional imager scanning pulses, and video processor signals.

Horizontal data pulses are obtained by sampling and delaying, at A15 and A14, a portion of the burst flag output of A8.

Vertical data pulses are obtained by sampling and delaying, at A15, a portion of the "ov'ed" field index outputs of A8 which are available at A13.

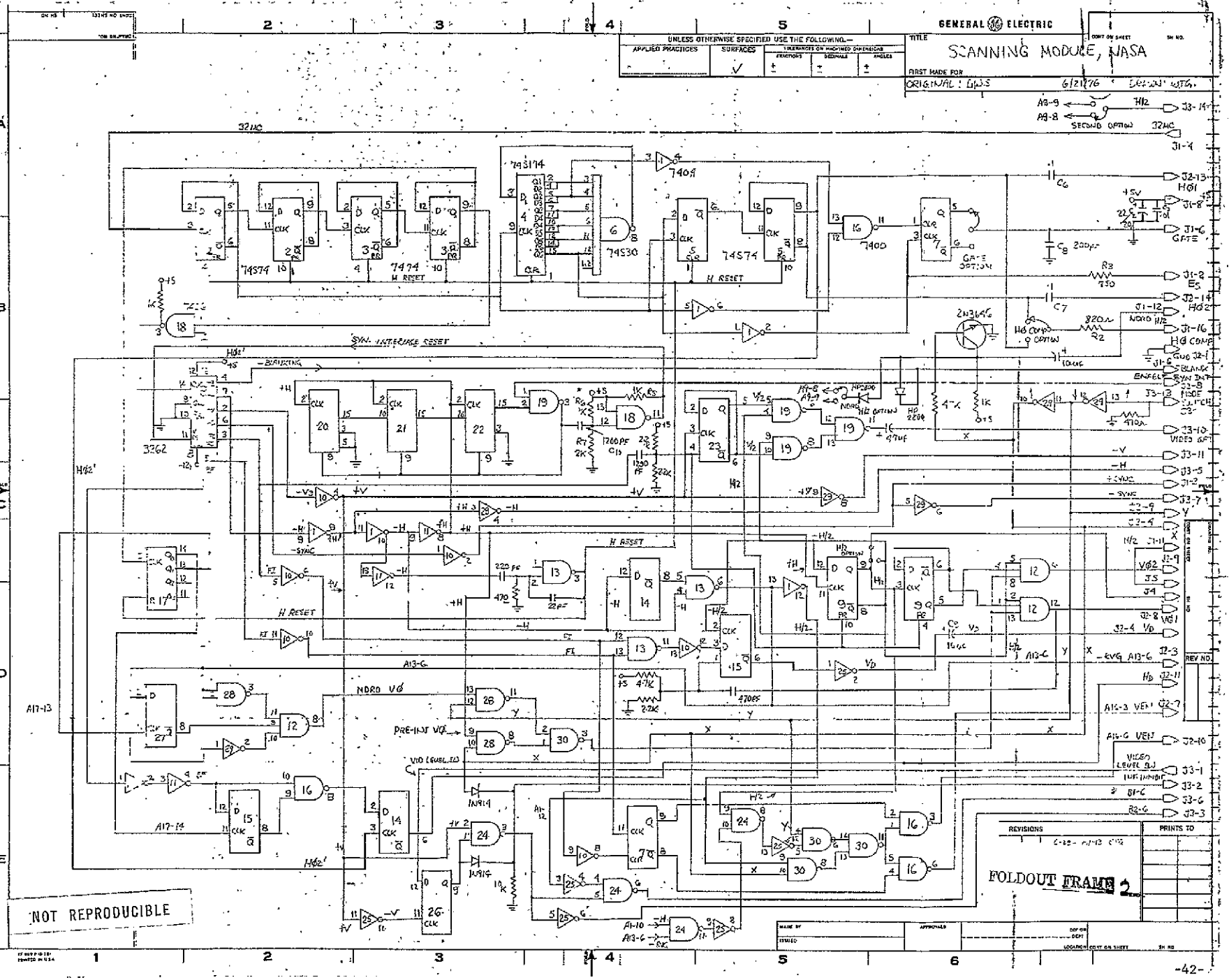
Vertical phase (Ø) pulses result from gating, at A12, divided down horizontal drive pulses, A9, produced by A8.

Vertical enable pulses result from gating a field index counter, A7, with a multiplexed signal which is readout mode dependent. This multiplexed signal is a function of VØ, H, and R_{VG}, VØ being readout mode dependent.

The R_{VG} pulse is derived from a sampled and delayed -H pulse available from A8.

Horizontal reset pulses required by various counter sections, are derived from differentiated and inverted horizontal drive pulses, +8, at A13.

C) The A20, 21, 22 counter sections comprise a 262 line counter which is used to reset the sync generator A8 at the beginning of each field during the "synthetic interlace" scan mode. A19, 23 generate the video gate signal which is also required for the synthetic interlace scan mode. The purpose of this gate signal is to blank alternate (redundant but out of spatial sequence) video lines from each field. Even lines are blanked for field #1 and odd lines are blanked for field #2. A26, 24, 25 utilize the video level switch output from the video processor board to generate signals to control the injection of charge at the CID during the NDRO readout mode.



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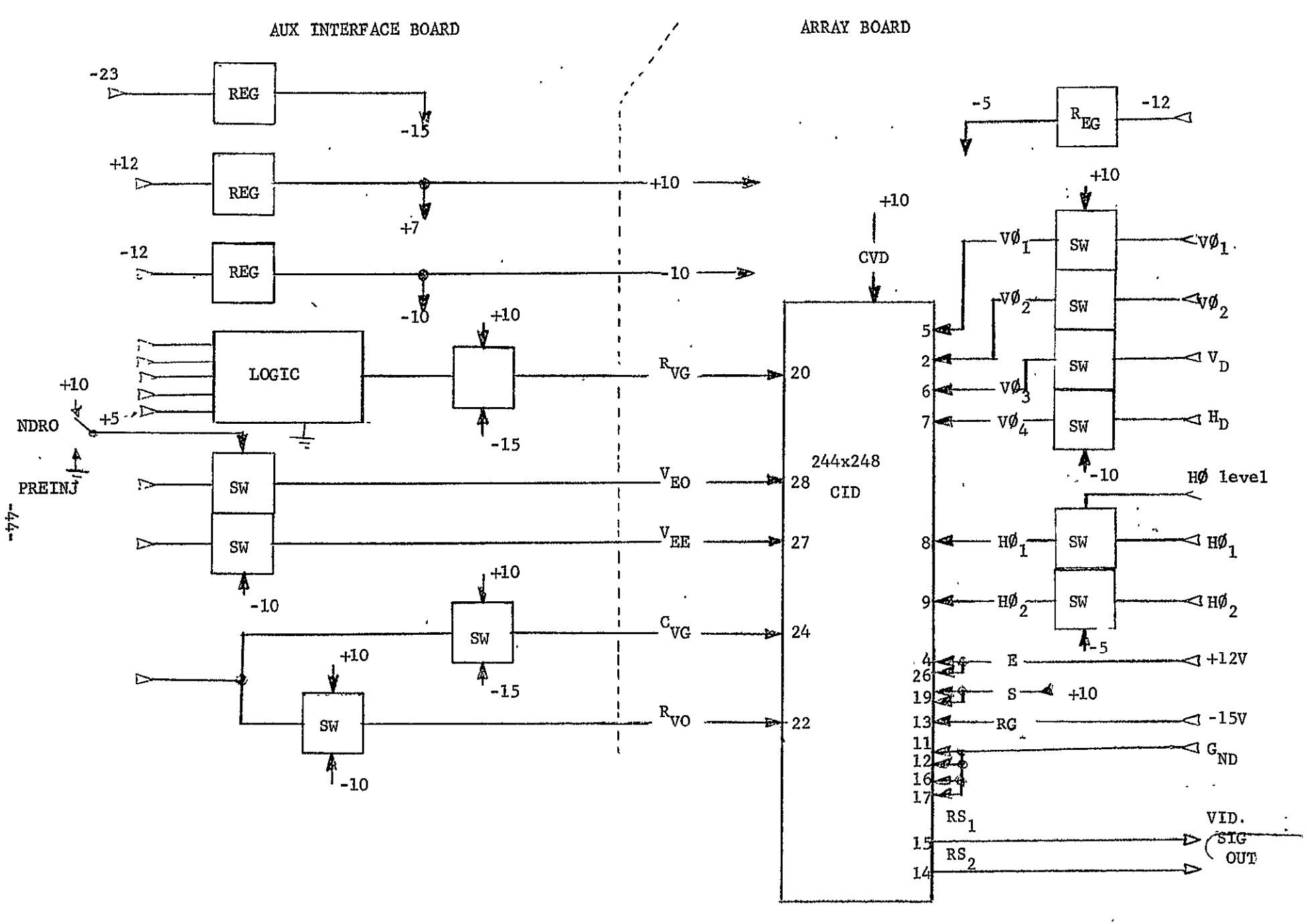


Figure 6. Auxiliary Interface and Array Boards

4.6 Auxiliary Interface and Array Boards

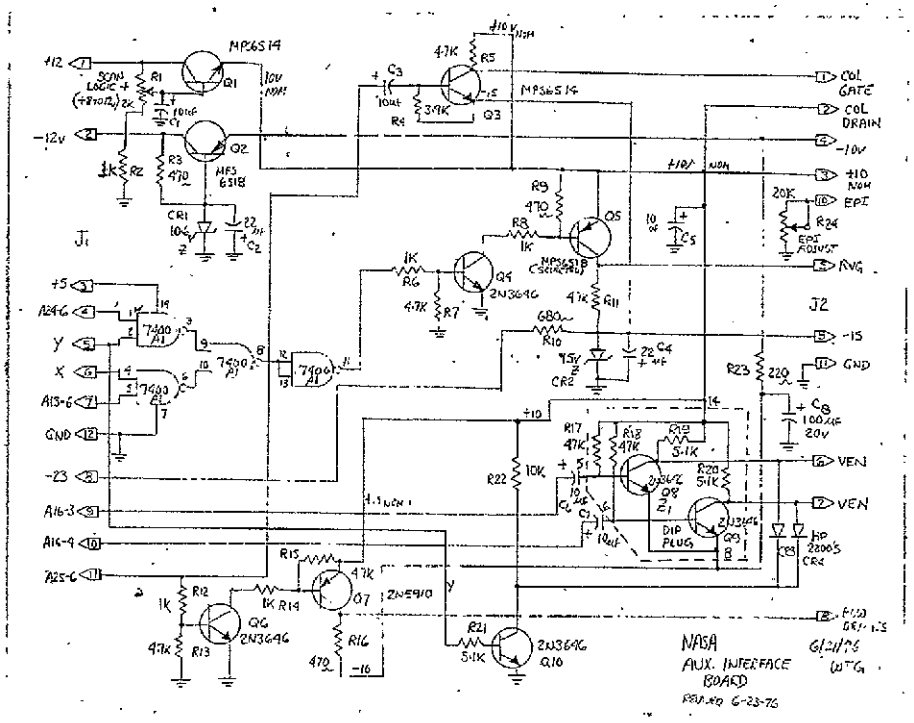
The CID array requires several DC and switching voltages to operate properly. The non-standard DC voltages (i.e., not directly available from the DC power supply) and the non TTL level, switching voltages are provided by the auxiliary and array boards. The array board also serves to provide mounting for the CID. Figure 6 describes the major functions performed on these boards and their relationship to the CID. It is important to note that the switches denoted SW on the diagram are essentially digital level translators. They accept standard TTL input signals and provide switching voltages that swing nearly to the limits of the DC voltages provided to them. In addition, the R_{VG} generation, provided on the auxiliary interface board, takes into account the selected readout mode (preinject-NDRO). The required logic for readout mode switching is included on this board.

GENERAL ELECTRIC

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES ✓ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

TITLE: AUXILLIARY INTERFACE

FIRST MADE FOR



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REVISIONS: A

PRINTS TO

FOLDOUT FRAME 2

FOLDOUT FRAME 1

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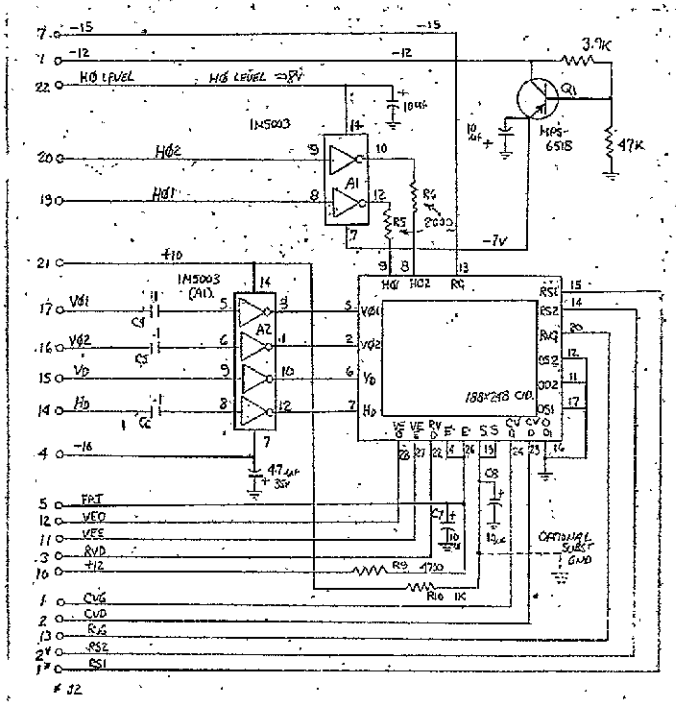
GENERAL ELECTRIC

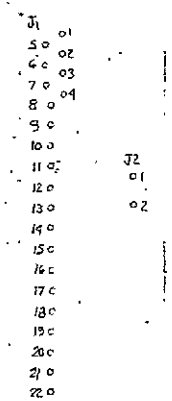
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING.—

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	✓	±	±	±

TITLE ARRAY BOARD

FIRST MADE FOR





ARRAY BOARD-
NASA

6-21-76
WTG.

REVISIONS

PRINTS TO

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FOLDOUT FRAME 2

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4.7 Camera Power Supply

The camera power supply is mounted internally to the camera. It supplies three regulated voltages, +12V (.25A), -12V (.25A) and +5V (1A). Regulation is performed by three series pass IC regulators mounted on a heat sink which is in thermal contact with the top cover of the camera. All regulated outputs are over current protected and in addition, the +5V output is over voltage protected. An unregulated +23V is also supplied. This voltage is subsequently regulated to -15V with a Zener diode on the auxiliary interface board.

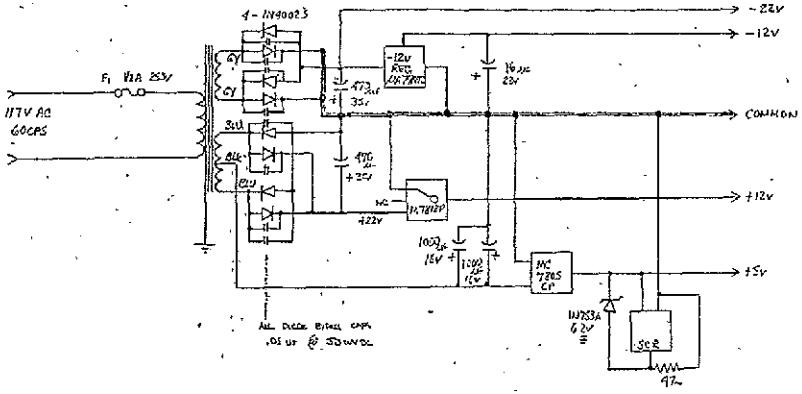
GENERAL ELECTRIC

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING: –

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	✓	±	±	±

TITLE: CAMERA POWER SUPPLY

FIRST MADE FOR



POWER SUPPLY
(NASA)

7-8-76

NOT REPRODUCIBLE

REVISIONS

PRINTS TO

FOLDOUT FRAME 2

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FOLDOUT FRAME 1

4.8 Thermoelectric Cooler

A provision is made for cooling the CID thermoelectrically for use in the NDRO readout mode. A two stage thermoelectric cooler (Nuclear Systems, Inc. $5HF_2$) is mounted to a heat sink plate which is in thermal contact with the bottom of the camera chassis (hot surface). The cold end of the cooler is in thermal contact with the back of the CID via an intermediary copper block cold finger. A separate thermoelectric cooler power supply is provided which connects to J11 on the rear of the camera. Proper polarity must be observed in this connection. A protective diode mounted on the T.E. cooler heat sink prevents inadvertent current flow in the wrong direction. The power supply has a high and a low power switch. The high switch position should be used only for rapid cooldown of the CID and subsequently, the unit should be placed in the low position for continuous running. It should be noted that it is extremely important that the heat sink be in good thermal contact with the camera chassis, i.e. thermal grease at this junction and fully tightened focus adjustment screws (which mechanically mount the heat sink to the camera chassis). Failure to note this may cause permanent damage to both the thermoelectric cooler and the CID. Additionally, it is important that a moderate rate of dry nitrogen flow be maintained into the "purge" connection while the camera is being thermoelectrically cooled. This will prevent excessive condensation in the area of the CID which will cause a slow but reversable deterioration in performance.

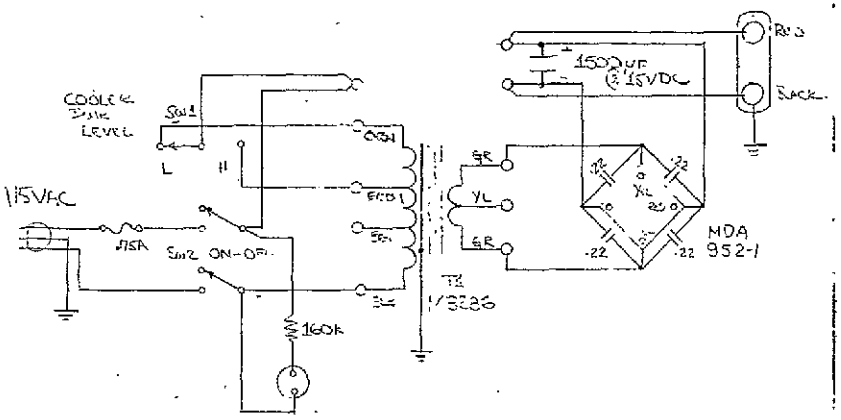
GENERAL ELECTRIC

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—

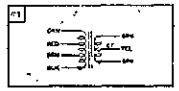
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	✓	±	±	±

TITLE: T.E. COOLER POWER SUPPLY

FIRST MADE FOR



T1 – MICROTRAN



M8286	Bk-Br-Rd-Or 0-105/115-125	Gn-Yel c.t.-Gn 6.3V c.t.-6.0A

NOT REPRODUCIBLE

REVISIONS

PRINTS TO

FOLDOUT FRAME 2

FOLDOUT FRAME 1

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5.0 Controls and Their Function

Video Processor:

HØ Level	Controls positive excursion of HØ pulses and is adjusted for minimum patterning consistent with reliable horizontal scan.
Blanking:	Controls "setup"; the level between the most positive excursion of camera sync and the most negative (black) video component.
F to F:	(Field to Field) compensates where necessary for differing array sensitivity field to field.
H/2:	Compensates for line to line DC level variation.
Delay Channel Gain:	Adjusts gain of the delay channel such that it matches exactly that of the undelayed channel thus optimizing pattern noise cancellation.
Delay Bal:	Balances undelayed channel time delay such that it matches exactly that of the delay line channel for optimum pattern noise cancellation.
High Freq:	Aperture corrects video signal to re-constitute element rate MTF (may be adjusted to exceed 100%).
AGC Level:	Controls DC feedback in the AGC loop. Control should be left in the fully CW position.
PI Gain:	Sets processor gain when camera system is in the pre-inject mode.
NDRO Gain:	Sets processor gain when camera system is in the NDRO mode. This control and the PI gain control tend to interact.
Vid Lev SW Th'ld:	(Video level switch threshold) controls integration time when camera is in the NDRO mode and determines the video level at which injection of the array occurs. Control is adjusted (when the cooler has stabilized) such that array is injected just short of saturation on low light level scene material.

Gain Bal: Compensates for possible pre-amp channel gain imbalance. Control is adjusted for minimum element rate patterning in scene highlight (PI mode).

NDRO H Shade: Compensates for possible horizontal shade due to dark current effect in CID.

NDRO H/2: Compensates for H/2 offset characteristic of preamp video in the NDRO mode.

Delay Module:

XO Frequency: Allows for trimming crystal oscillator frequency. Control is adjusted along with processor delay channel gain and delay balance for minimum pattern noise.

Response Trim: Adjusts 1 H delay channel RF bandpass for optimum response. (Sweep generator required).

Comb Filter:

Comb Delay Bal: Trims undelayed channel time delay to match that of of the 1 H delay channel.

Response Trim: Adjusts 1 H delay channel RF bandpass for optimum response (sweep generator required).

Video Driver Board:

Comb Gain Balance: Adjusts 1 H delayed channel gain such that it matches exactly that of the undelayed channel.

Comb Blanking: Controls setup in the comb filter video channel (see video processor "blanking").

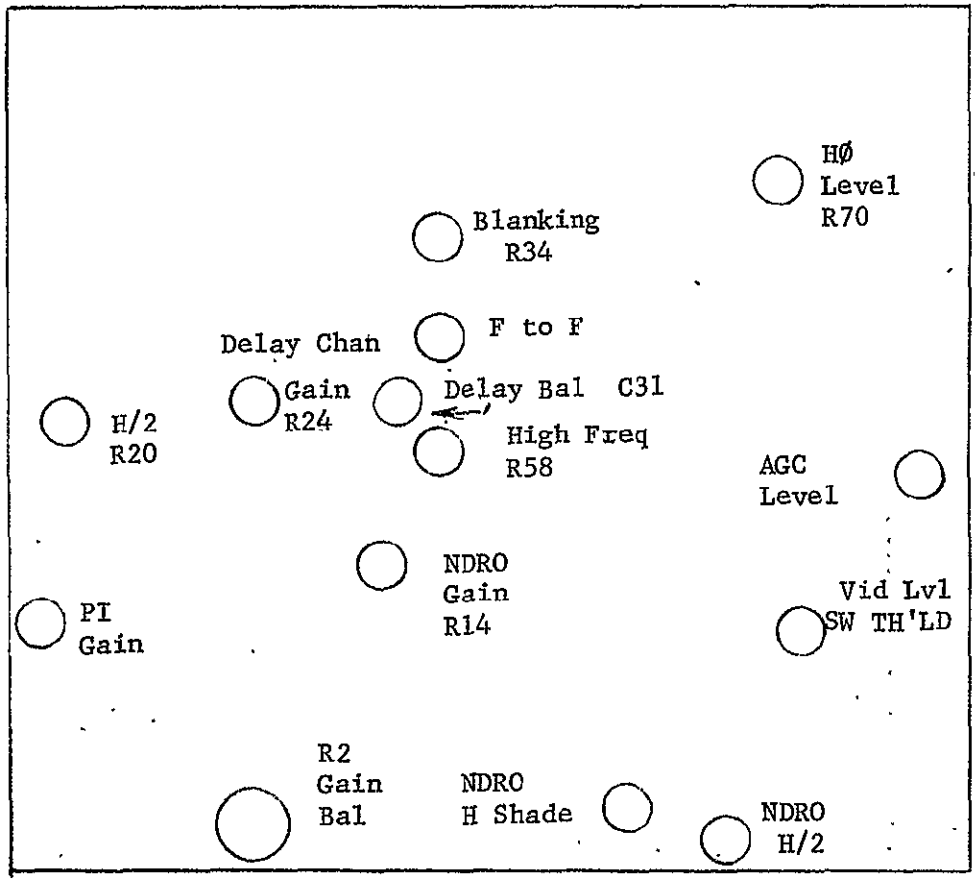
Video Preamp:

HØ Comp (R8, R30): Compensates for HØ crosstalk in odd and even preamp channels. Controls are adjusted for minimum element/2 rate square wave at each preamp output.

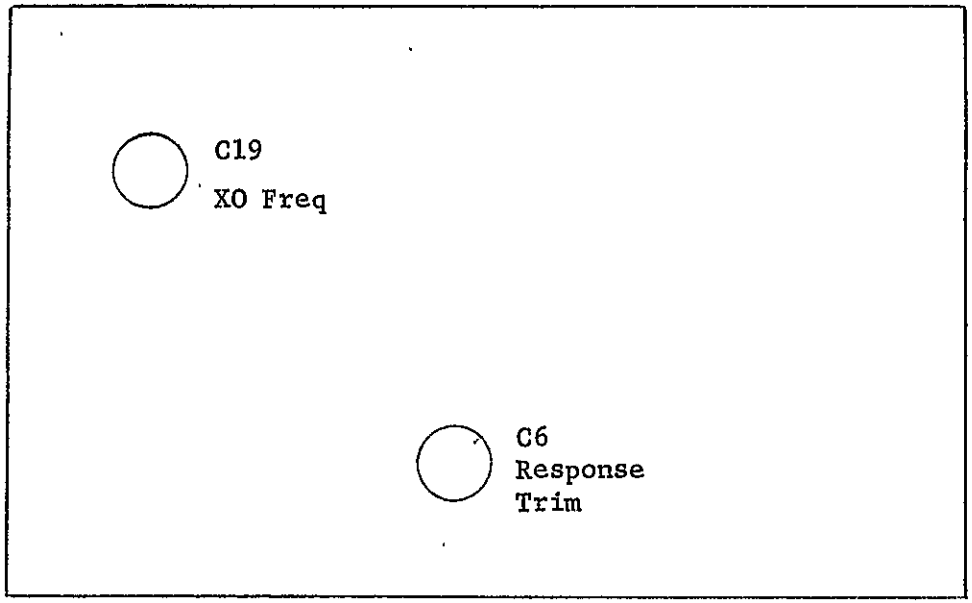
Aux Interface:

Scan Logic: Controls positive excursion of scan logic. Control is adjusted for nominal level of ≈ +7V.

Epi Adjust: Controls array epitaxial layer bias. Control is set for epi level of ≈ 8.1V.



VIDEO PROCESSOR-
CONTROL LOCATION



DELAY MODULE

CONTROL LOCATION

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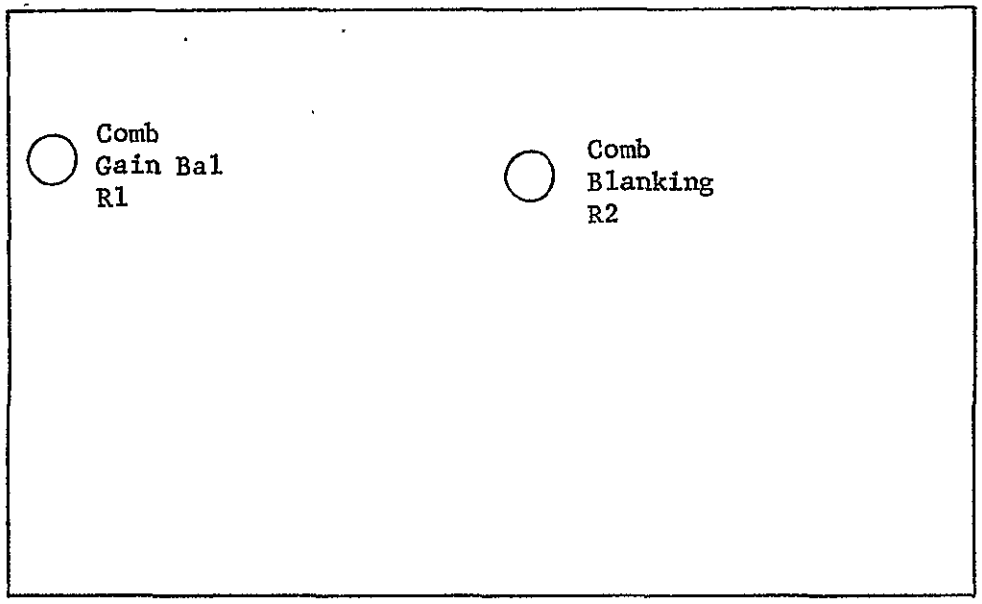
COMB FILTER
CONTROL LOCATION



VID DRIVER BD -
CONTROL LOCATION

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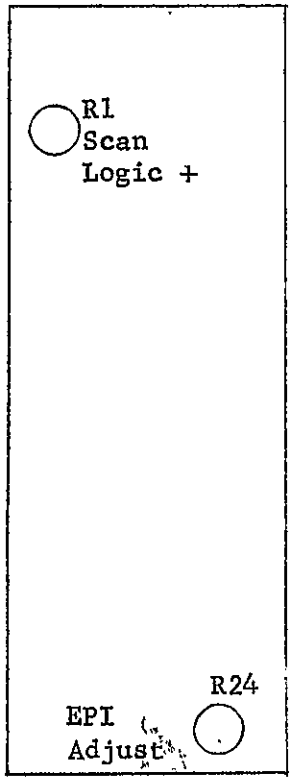
VIDEO PREAMP
CONTROL LOCATION



AUX. INTERFACE
CONTROL LOCATION

GENERAL ELECTRIC

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING –

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	✓	±	±	±

TITLE: MODE OPTIONS

FIRST MADE FOR

OPERATIONAL MODES

INPUT / OUTPUT FUNCTIONS ON REAR PANEL	NORMAL SCAN PREINJECT READOUT	NORMAL SCAN NDRO READOUT	SYNTHETIC INT. SCAN PREINJECT READOUT	SYNTHETIC INT. SCAN NDRO READOUT
SYNTHETIC INTERLACE S3 SWITCH UP (SYN. INTERLACE) SWITCH DOWN (NORMAL)	SWITCH DOWN ↓	SWITCH DOWN ↓	SWITCH UP ↑	SWITCH UP ↑
NDRO ENABLE S2 SWITCH UP (NDRO PREFERRED THAT T.E. COOLER + NITROGEN PURGE BE IN OPERATION) SWITCH DOWN (PREINJECT)	SWITCH DOWN ↓	SWITCH UP ↑	SWITCH DOWN ↓	SWITCH UP ↑
EXT / AUTO INJECT S1 SWITCH UP (EXTERNAL INJECT) SWITCH DOWN (AUTO INJECT)	SWITCH DOWN ↓	USE FOR EXT. INJECT (VIA 1 AT J10) USE FOR AUTO INJECT	SWITCH DOWN ↓	USE FOR EXT. INJECT USE FOR AUTO INJECT
VIDEO OUTPUT J1 COMB FILTER VIDEO OUTPUT J4	USE THIS OUTPUT FOR NORMAL VIDEO OR USE THIS OUTPUT FOR COMB FILTER VIDEO	→	(PREFERRED)	(PREFERRED)
J3 TO J5 [PRE AGC VIDEO TO POST PROC. VIDEO IN] J6 TO J5 [AGC VIDEO OUT TO POST PROC. VIDEO IN] AGC	USE THIS CONNECTION FOR NO AGC OR USE THIS CONNECTION FOR AGC	→	→	→
		(PREFERRED)	→	(PREFERRED)

CAMERA SETUP PROCEEDURE

1. SELECT AGC IN OR OUT (VIA JUMPER CABLE)
2. SELECT SCAN MODE (VIA S3)
3. SELECT READOUT MODE (VIA S2) NOTE: VERIFY PROPER S1 POSITION
4. SELECT COMB FILTER (VIA J4) OR VIDEO OUT (VIA J1) AS A CAMERA VIDEO OUTPUT

REVISIONS: A

PRINTS TO

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FOLDOUT FRAME 2

FOLDOUT FRAME 1

6.0 Predelivery Acceptance Test Procedure

6.1 Camera Interfaces

The following outputs will be appropriately terminated and monitored by a scope to verify proper signal levels.

Location	Description	Verified
J1	Video Output	X
J2	Undelayed Video	X
J3	Pre AGC Video	X
J4	Comb. Filter Video Out	X
J6	AGC Video Out	X
J7	-V (1 U.L.)	X
J8	-Sync (1 U.L.)	X
J9	-H (1 U.L.)	X

The following input functions will be exercised to verify proper operation.

Location	Description	Verified
J5	Post Processor Video In	X
J10	External Inject	X
S1	Ext/Auto Inject	X
S2	NDRO Enable	X
S3	Synthetic Interlace Enable	X
S4	Power	X
R1	Video Gain	X

6.2 Power Consumption

Camera power consumptions external and internal to unit:

Nominal Voltage	Description	Power (Watts)
115V AC	Total Primary Input to Camera	27
4.8/5.15V DC(a)	TE Cooler (Input to Camera)	13.92/16.99
+12V DC	Camera Electronics	4.50
-12V DC	Camera Electronics	4.21
+5V DC	Camera Electronics	3.26
Camera electronics independent of cooler and power supply inefficiency.		11.97

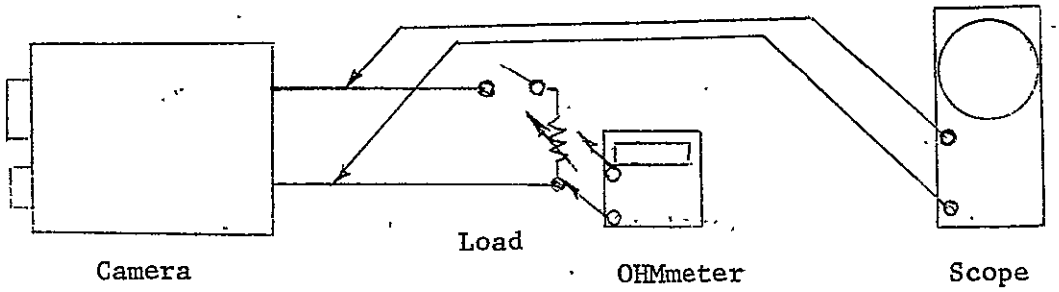
6.3 Output Video Format

6.3.1 Standard Load Impedance

The standard load impedance is defined as the complex ratio of voltage to current in a two-terminal network, expressed in ohms.

Procedure:

The following test circuit will be used:



The open circuit output video voltage will be measured with a scope. The pot will then be used to terminate the output and be subsequently adjusted to yield an output voltage of 1/2 the previously measured open circuit voltage. The pot will then be removed from the output circuit and measured with a digital ohmmeter.

The output impedance shall be 75 ohms ±5% over the frequency range of the camera and shall be connected for single-ended operation.

J1 Measured impedance 72.0 Ω

J4 Measured impedance 75.6 Ω

6.3.2 Composite Picture Signal Measurements

The composite picture signal is the signal which results from combining a blanked picture signal (the result of the scanning process) with the synchronizing (sync) signal.

The subject level will be measured by means of an oscilloscope capable of measuring such a signal with the accuracy of ± 2% of the actual value over the voltage range of -0.5 to +1.5 volts. Some means of calibration shall be provided so that signal level measurements can be made in volts as well as in IRE units.

The following composite signal measurements were made in accordance with appropriate portions of 58 IRE 23.51 IRE Standards on Television: Measurement of Luminance Signal Levels, 1958, or latest revision thereof:

	Required	J1 Verified	J4 Verified
Polarity	Black Negative	X	X
Signal Levels			
White	100 IRE units	100	100
Blanking	0 IRE units	0	0
Sync	-40 IRE units	-38	-42
Setup	7.5±5 IRE units	7.5	7.5
Output Video Voltage (with 75 ohm termination)			
Composite	1V p-p	990 MV	960 MV
Blanked Picture Signal with setup (non composite)	.714 ± .1V p-p	738 MV	705 MV
Synchronizing Signal	+.286 ± 05V p-p	236 MV	240 MV

6.4 Spots and Blemishes

A spot or blemish shall be defined as a video signal transition of 7 IRE units or more in the output picture signal not present in the original scene, and which is the direct result of a sensor defect. The difference in sensitivity between any two adjacent CID elements in any direction shall be no more than 10%. Also, the difference in sensitivity from raster edge to edge (horizontally and vertically) shall be no more than 10%. No horizontal or vertical black lines resulting from a failed CID element will be allowed. The size of a spot shall be determined by counting the number of scan lines on which the transition occurs; i.e., the number of lines per frame on which the transition is greater than 7 IRE units.

To determine the presence of spots, smudges, etc., a uniform grey background shall be observed which is illuminated by light source(s) of the appropriate color temperature and of the intensity to allow nominal camera operation (i.e., S/N shall not be such that spots and blemishes are masked by noise). Any gain operation by the camera shall also be considered.

The total of white and dark spots shall be less than or equal to:

10 spots $\leq$ 4 TV lines per frame

2 spots $\leq$ 8 TV lines per frame

The total of white and dark spots measured: 9 [3 significant white, 6 significant black]

Measured at room temperature (white spots halve in intensity for approximately each 8°C reduction in CID temperature)

6.5 Output Resolution

In television systems, a measure of ability to delineate picture detail is resolution expressed in terms of the maximum number of TV lines (alternate black and white lines) per picutre height discriminated on a standard test chart. The ratio of (1) the peak-to-peak signal amplitude, given by a test pattern consisting of alternate black and white bars corresponding to a specified line number (resolution), to (2) the peak-to-peak signal amplitude, given by large area blacks and large area whites having the same luminance as the test pattern is defined as the resolution response.

The methods of measurement are as specified in Institute of Electrical and Electronic Engineers (IEEE) 208, 60 IRE 23.52, Standards on Video Techniques: Measurement of Resolution of Camera Systems.

Resolution: The limiting horizontal and vertical resolution response is determined by observing the point at which the individual lines of the graduated wedges are no longer distinguishable as separately defined images. For the measurement of resolution response, the picture signal shall be applied to a picture monitor properly adjusted per the IEEE standard above.

The horizontal resoltuion response shall not be degraded by the video processing chain of the camera systems, at least to an upper limit defined by the number of CID elements. The limiting resolution shall be no less than 70% of the number of TV elements.

	Desired		Measured	
Scanning Mode	Horizontal	Vertical	Horizontal	Vertical
Normal	174 lines	171 lines	>200 lines	175 lines
Synthetic Interlace	174 lines	171 lines	>200 lines	>200 lines

Resolution Response

Measured Resolution Response $\geq$ 175 lines
(See photographs #1 through #6)

6.6 Operating Light Ranges

6.6.1 Gray Scale Response

The gray scale response is defined as the camera's ability to resolve scene contrast ratio and generate a proportional voltage to display same on a television monitor.

When the camera is activated under nominal conditions and a logarithmic gray scale with 10 steps (32:1 contrast ratio) is imaged onto the sensor faceplate with a highlight illumination as indicated below (via a standard reflectance-type gray scale chart), the camera shall resolve the 10 steps when its output is displayed on a suitable television monitor and shall exhibit a signal/noise ratio as defined and indicated below:

The S/N for temporal noise sources (random noise) shall be determined by measurement on an oscilloscope, at the camera output, (across the standard load impedance) of the peak-peak noncomposite picture signal voltage and the peak-peak random noise voltage. S/N is the ratio of peak-peak signal voltage to rms $(\frac{\text{peak-peak}}{5.6})$ random noise voltage. S/N for fixed pattern noise sources shall be determined by measurement on an oscilloscope, at the camera output, (across the standard load impedance) of the peak-peak fixed-pattern noise voltage across any one selected line of video. S/N is the ratio of peak-peak signal voltage to peak-peak fixed pattern noise voltage.

Mode	Highlight Illumination (Faceplate)	S/N Ratio (Random)		S/N Ratio (Fixed Pattern)	
	1/2 amount required for array saturation (.4 ft-c)	Min NR	Meas >50 DB	Min NR	Meas 46 DB
Normal Preinject	(.13 ft-c nominal)	38DB	39.6 DB	33DB	33.6 DB
NDRO	1/2 amount required for array saturation with a scene integration time of 3 seconds (.1 ft-c nominal)	38DB	>30 DB	30DB	32 DB

The illumination source shall be a standard tungsten lamp at 2854K color temperature.

6.6.2 Dynamic Light Range

The dynamic light range is defined as the camera's ability to respond to varying light levels with a fixed lens iris setting. It must still retain the ability to resolve the 10 logarithmic gray scale steps (as described previously) when the camera output is displayed on a suitable television monitor, over a range of illumination levels.

The test procedure is defined to be: 1) adjust lens iris setting to obtain maximum signal/noise ratio without exceeding array saturation; i.e., the highlight illumination reflected from the gray-scale chart shall be within 10% of array saturation; 2) adjust lens iris setting until the 2 blackest shades of the 10 step gray-scale chart are no longer resolved on the monitor display (camera AGC function to maintain constant signal output over this range); 3) calculation dynamic light range from the relationship:

$$\text{Dynamic Light Range} = \left(\frac{f\# \text{ (loss of gray-scale)}}{f\# \text{ (saturation)}}\right)^2$$

Measurement performed with camera in the normal preinject readout mode:

	Dynamic Light Range		
	Required	Meas.	
With AGC	7:1	30.25:1	F4 to F22
Without AGC	NR	7.84:1	F4 to F11

Refer to photographs #8 through #15.

6.6.3 Signal-to-Noise Ratio (S/N)

The S/N for nominal camera operation (i.e., highlight illumination at 1/2 that required for array saturation) shall be as outlined below. S/N for temporal noise sources (random noise) shall be determined by measurement on an oscilloscope, at the camera output, (across the standard load impedance) of the peak-peak noncomposite picture signal voltage and the peak-peak random noise voltage. S/N is the ratio of peak-peak signal voltage to rms $(\frac{\text{peak-peak}}{5.6})$ random noise voltage. S/N for fixed pattern noise sources shall be determined by measurement on an oscilloscope, at the camera output, (across the standard load impedance) of the peak-peak noncomposite picture signal voltage and the peak-peak fixed-pattern noise voltage across any one selected line of video. S/N is the ratio of peak-peak signal voltage to peak-peak fixed pattern noise voltage.

Readout Mode	S/N (Random Noise) Required	S/N (Random Noise) Measured	S/N (Fixed Pattern) Required	S/N (Fixed Pattern) Measured
Normal Preinject	38 DB	39.6 DB	33 DB	33.6 DB
*NDRO	38 DB	>30 DB	30 DB	32 DB

*The highlight illumination shall be at 1/2 that required for array saturation for a scene integration time of 3 seconds (cooler in operation).

6.6.4 Blooming

The CID image sensor is particularly insensitive to blooming. Due to this fact, the measurement of the effect becomes difficult to do at the camera as the optics and signal processing circuitry of the camera tend to obscure the inherently low value of the charge spreading which occurs at the sensor. Tests have been performed using a laser focused on a single element of a CID sensor. The results of these tests indicate a nominally small amount of spreading even for extremely intense light levels.

In lieu of performing a laser test, photos are provided which depict the camera's overall response to an intense red light overload (from lighted match) under a nominal camera system gain with the camera system gain at maximum level.

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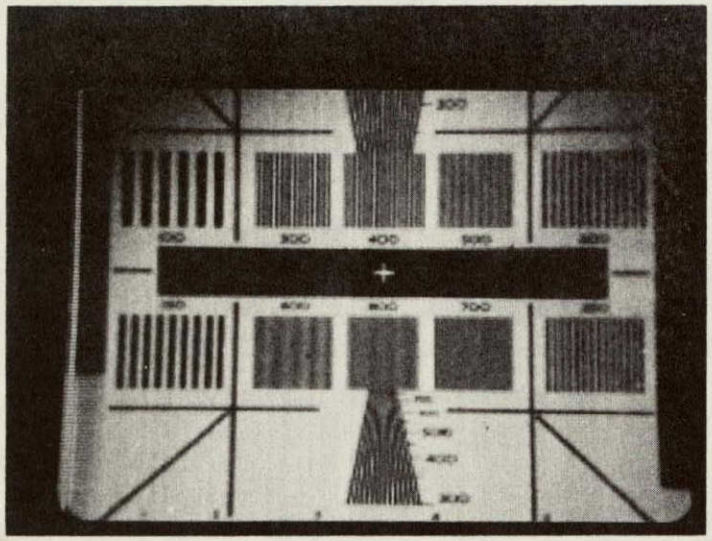
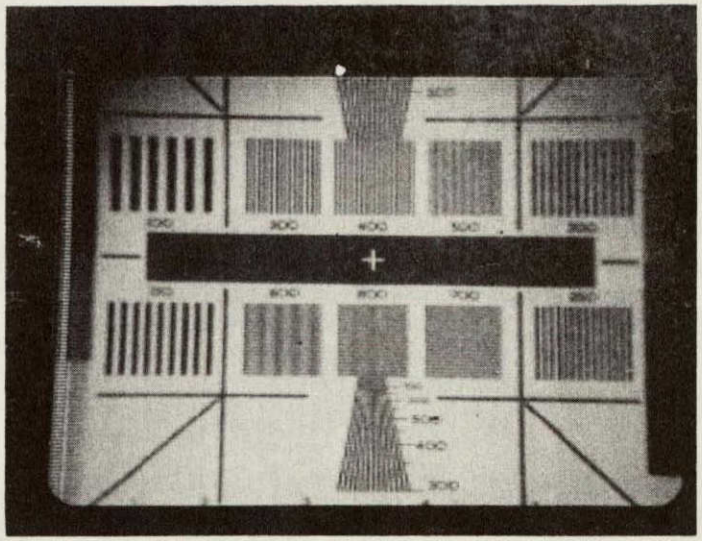
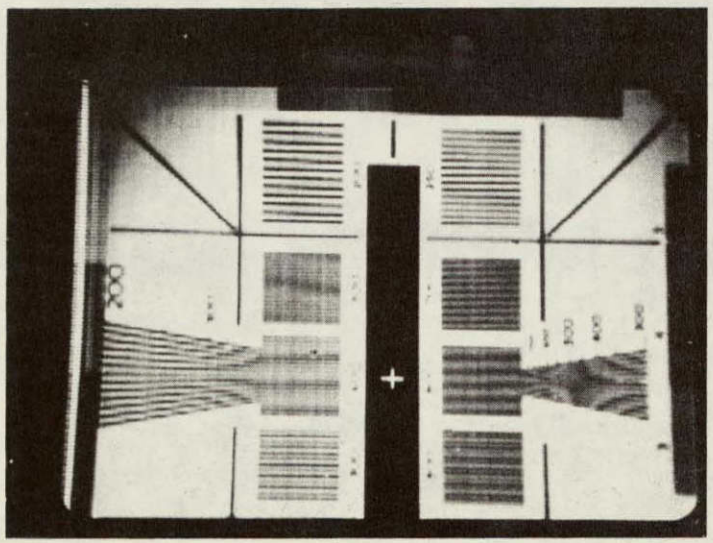
VERTICAL AND HORIZONTAL RESOLUTION MEASUREMENTS



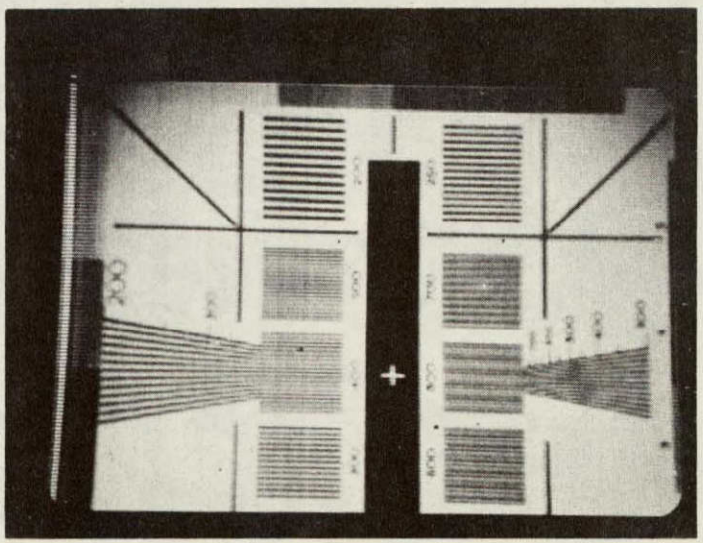
PH #1. Horizontal Resolution, Normal Scan > 175 Lines.



PH #2. Horizontal, Resolution, Synthetic Interlace > 175 Lines.



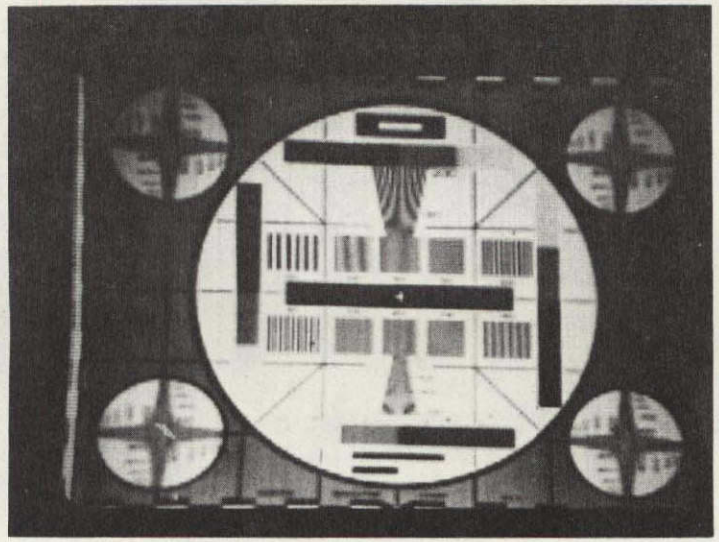
PH #3. Vertical Resolution, Normal Scan ≈ 175 Lines.



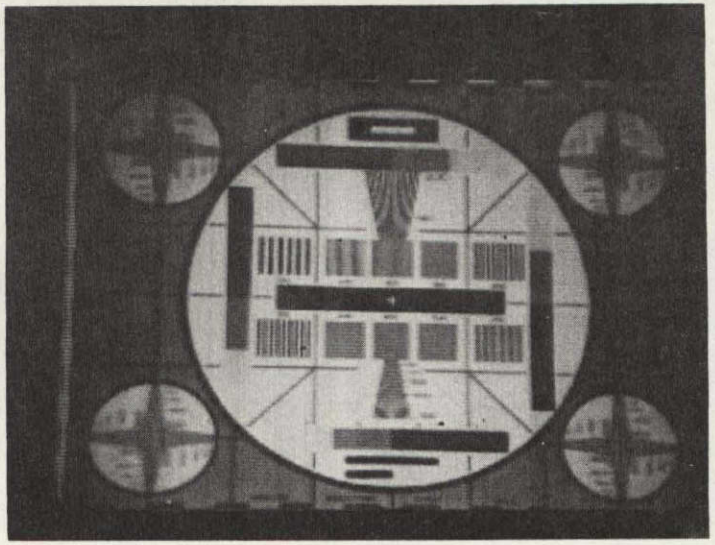
PH #4. Vertical Resolution, Synthetic Interlace > 200 Lines.

To facilitate resolution measurements, only the center portion of the resolution chart (shown in PH #5 and PH #6) was used. This area corresponds to 1/2 width of chart X 1/2 height of chart. The areas used above, therefore, are at 1/2 resolution and resolution numbers are 1/2 that shown.

RESOLUTION CHART



PH #5. Normal Scan Mode



PH #6. Synthetic Interlace Scan Mode

The above photos demonstrate the need for the use of a scaled down resolution chart as used in PH #1, 2, 3, 4 to make accurate resolution measurements.

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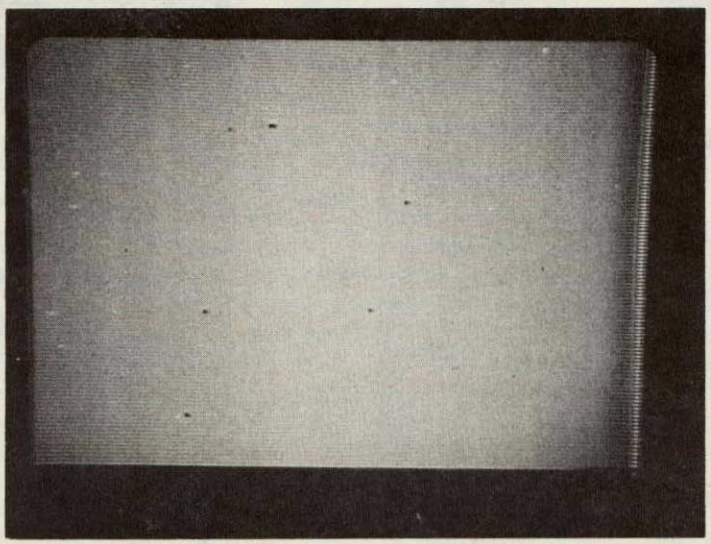
ARRAY DEFECT MEASUREMENTS



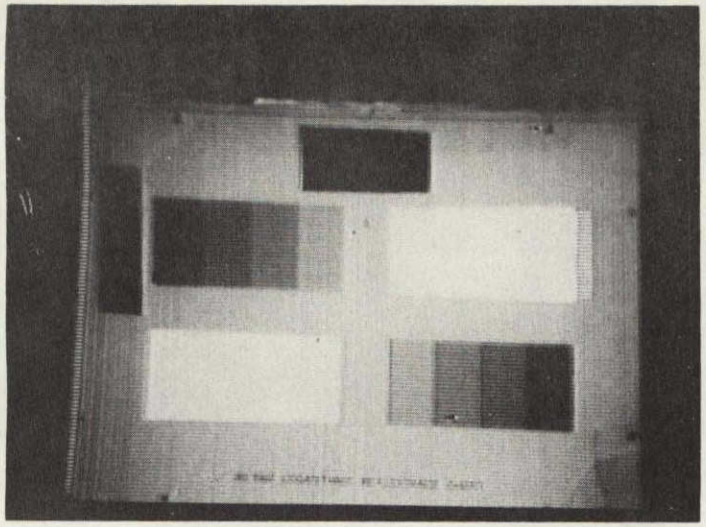
PH #7. White and Black Spot Defects

Each defect occupies only 1 line.
White spot defects present only on 1 field.
There is a total of 9 "significant" defects.

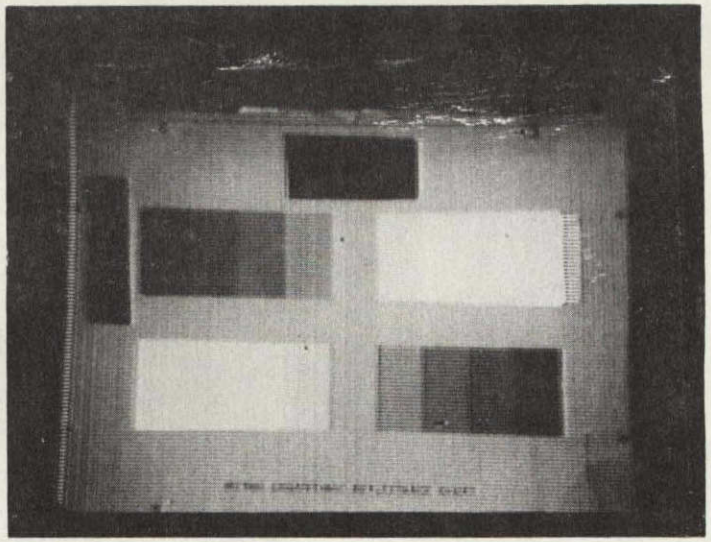
3 white spots (nominally 20 IRE units
6 black spots

Note: Above measurements made at room temperature and with a nominal scene illumination (AGC not used).

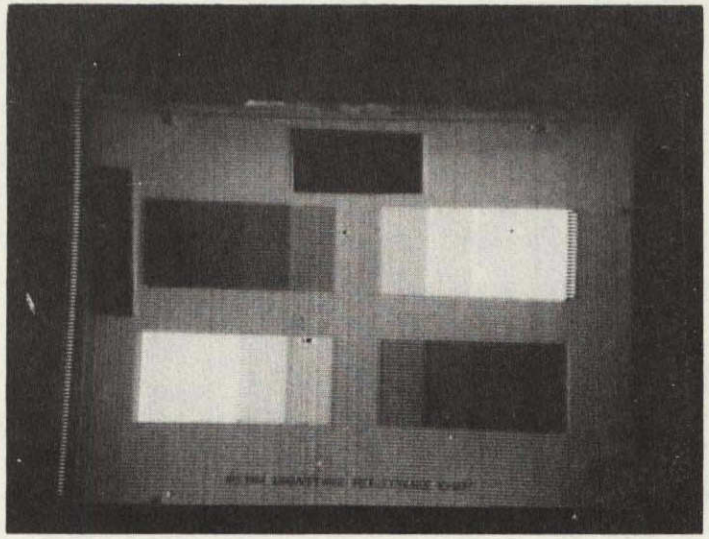
AGC PERFORMANCE (UPPER PORTION OF DYNAMIC RANGE)



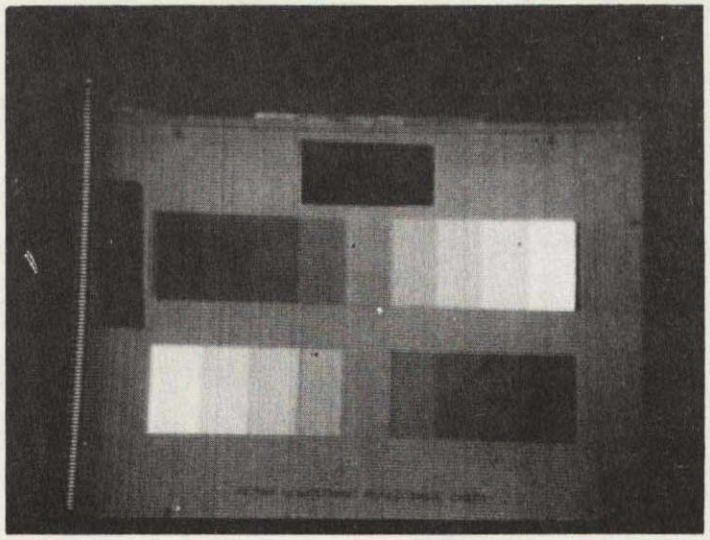
PH #8. F 2.5



PH #9. F 2.8



PH #10. F 4



PH #11. F 5.6

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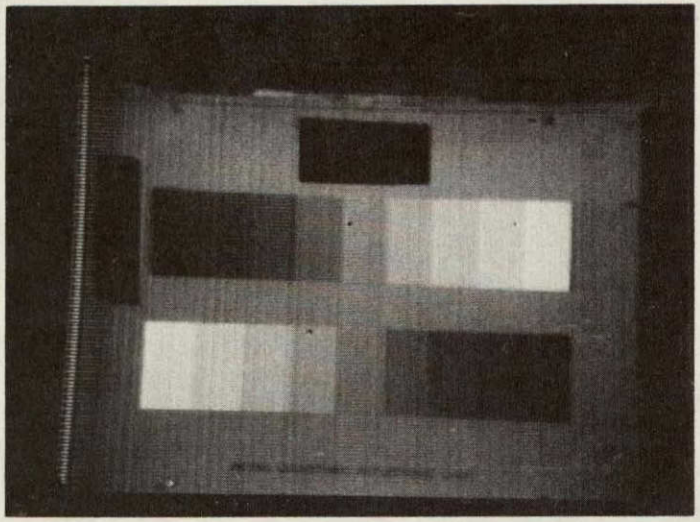
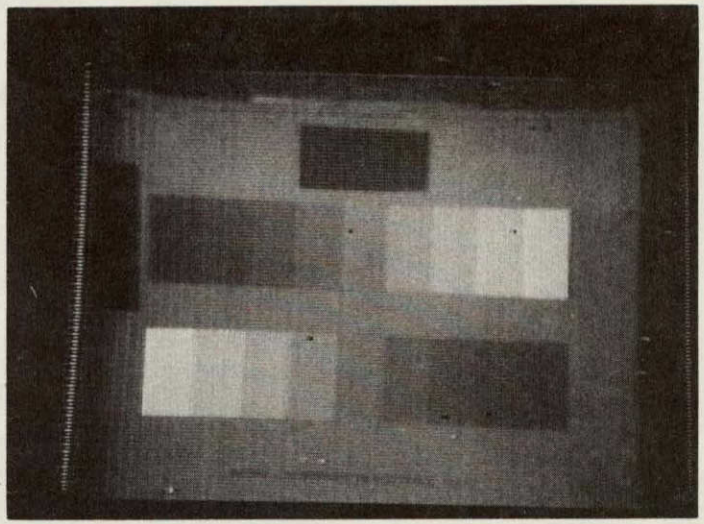
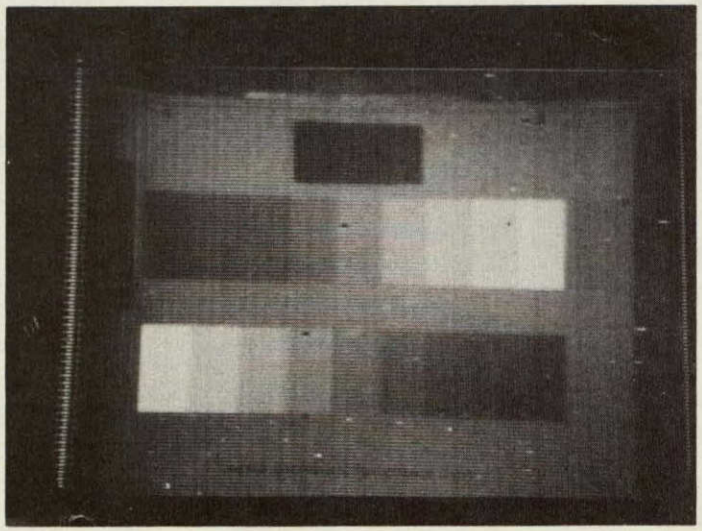
AGC PERFORMANCE (LOWER PORTION OF DYNAMIC RANGE)



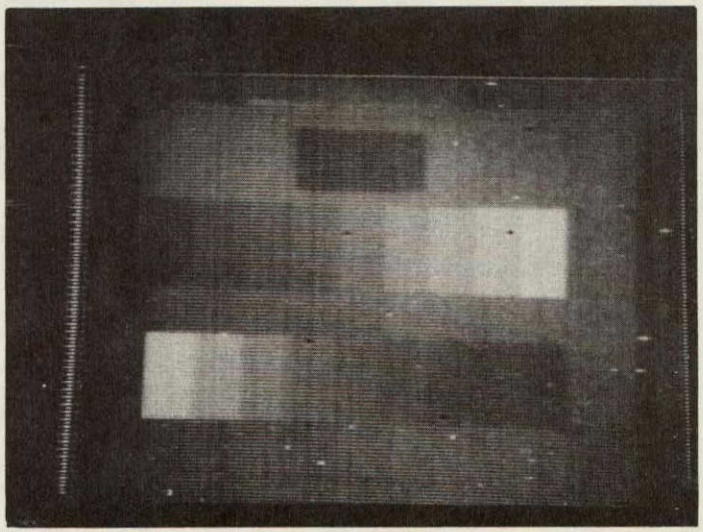
PH #12. F 8



PH #13. F 11



PH #14 F 16



PH #15 F 22

ANTI BLOOMING RESPONSE

PH #16 Nominal Lighting

PH #17 Low Level Lighting
(AGC at full gain)

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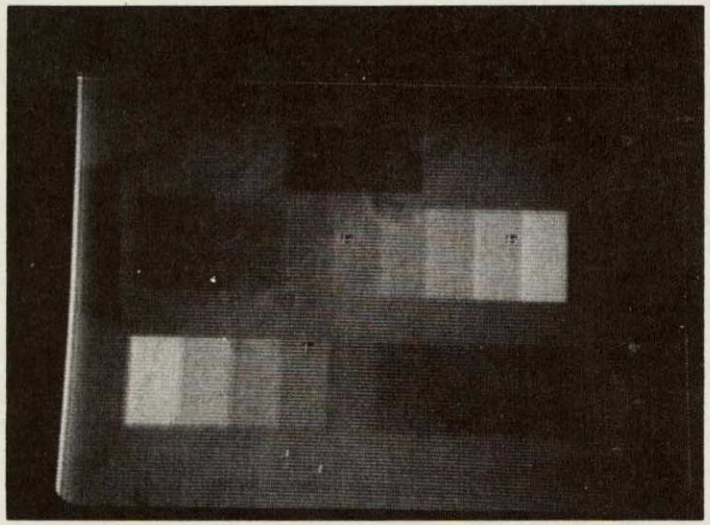
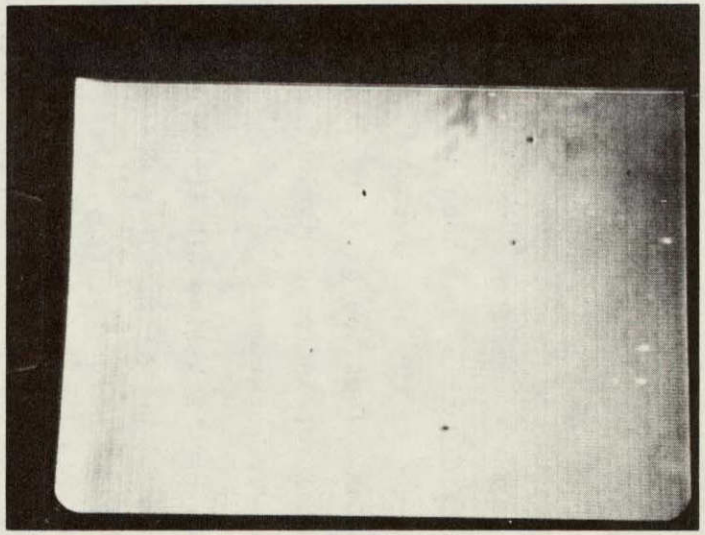
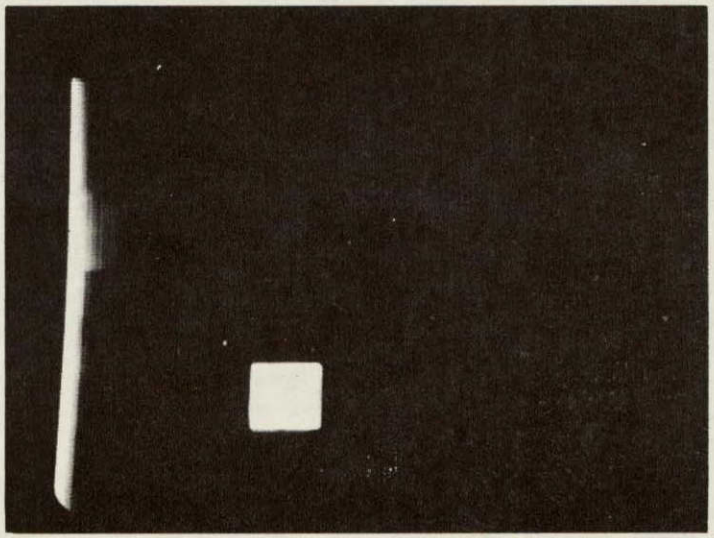


PH #18. F 22, 1/2 sec Integration Light Level of Brightest Chip 130 Foot Lamberts



PH #19. Bias Charge Variations after 3 second Integration



PH #20. F 22, 1 sec Integration, Light Box at 100 Foot Lamberts Condition used to Measure S/N Ratio (No AGC)

7.0 New Directions for CID Camera Design

7.1 Higher Resolution

Three significant efforts are underway in the area listed below in the sequence in which they will be addressed during in-house development:

1. A 324 element X 244 line CID array has been designed, and a sample lot will be evaluated in the near future. This next step up in resolution retains all of the previous CID structure and will produce a horizontal resolution equivalent to that obtainable in current color TV receivers.

2. A high density 248 element x 244 line CID array has been developed and produced in small quantity. This design significantly shrinks the pixel size within the array, thus leading the way toward greater array densities. An overlapping electrode readout structure is also incorporated in this design which impacts color response.

3. A row readout chip has been developed to the point where a test chip is available waiting for a breadboard camera to be built. It is a 248 element x 244 line device manufactured in a way that will allow video to be read simultaneously from two sequential lines at one time. If successful, this will eliminate the requirement for the cascaded double line readout technique now required for successful pattern noise rejection. The door will thus be open for a full 488 visable line camera with the CID operating at present readout rates.

As a goal, consideration is being given toward array structures with horizontal resolutions significantly greater than those currently being developed.

7.2 Greater Sensitivity

There are two areas that are currently being developed to increase camera sensitivity.

Signal to Noise Ratios Improvement -

A number of techniques have been developed and are now available for significantly reducing pattern noise at the output of the CID camera. Many more avenues of improvement are yet to be explored. Efforts directed toward an increase in delay line performance will yield substantial reductions in noise, allowing higher video gains to be used in the camera to accommodate a higher sensitivity requirement. It is also felt that the use of the row readout CID will result in a better overall signal to noise ratio. This is due to the inherent pattern noise reduction that can occur in processing directly following the CID and the possibility of certain crosstalk noise not being present to the degree that it is in current CID structures.

Larger Effective Pixel Area -

The actual photo receptive area of a pixel can be increased significantly over what is now possible with a careful choice of materials used in the construction of row and column lines on the CID. At present total or blue wavelength obscuration occurs over the large area taken up by these lines. The use of transparent conductive materials has been under investigation at the General Electric Corporate Research and Development Center. It has yet to be successfully implemented into a fully operational CID camera. It is probable that significant gains in cell sensitivity and in flatness of spectral response (especially in the blue region) would result from efforts in this area.

7.3 Color Performance

Three areas of development are most promising:

1. Three imagers optically registered with a prism could produce high quality color images. It is significant to note that the innate geometric stability of the CID imager is an advantage over vidicon devices in this technique. The optical alignment, once performed, is complete and electrical tracking requirements between imagers is a minor task.

2. A single imager color stripe filter approach is now under serious consideration for a CID color camera. The fact that a single imager is used and the potentially simple optical system, makes this approach attractive from an economic standpoint. Development work is now under way in this area.

3. The field sequential color camera capability is currently available based upon a preliminary evaluation at NASA, LBJ Space Center, Houston, Texas with the delivered 248 element X 244 line camera. Adequate color rendition was obtainable with the use of a color wheel. The vidicon-like scanning sequence made the camera directly compatible with standard color wheel hardware. Since silicon image devices in general have attenuated blue response, a minimal effort at enhancing the electrical performance of the camera during the blue channel readout would be of significant benefit. Overall, the field sequential approach can yield high quality color imagery having bandwidth requirements identical to that of B&W with the disadvantages of motion sensitivity and the need for a scan converter.

7.4 Stereo

This third dimension of TV imagery has yet to show its true importance. Depth information may be the missing link in the successful application of TV to critical visual and measurement systems. In a visual system, the information added in the perceived image may easily be greater than double that provided by a single sensor. Depth, as a sorting clue, can unclutter a scene, highlighting the essential details without ignoring the total. The fact that each sensor is indeed an independent sample of a field-of-view, and that the human visual perceptive system has the innate ability to marry and correlate common elements of each view, allows the subjective resolution of the stereo system to be at least double that of a single sensor system. Visual measurement systems on the other hand could be made to greatly benefit from depth information extracted computationally from the scene. Manipulator devices requiring closed loop feedback of relative position would be given the benefit of distance measurement relatively independent of object size and shape. Additionally, absolute size measurements could be made independent of changes in distance.

Presently, we are aware of the existence of one stereo system using CID devices. General Electric is currently under contract to build a stereo CID camera for the NASA Marshall Space Flight Center.

7.5 Smart Cameras

Television is increasingly being considered as the measurement sensing technique for a large variety of industrial processes. It is recognized that solid state sensors, in general, are very suitable for measurement systems due to their fixed and accurate geometry, reliability and small size. CID devices, in particular, have the additional features of antiblooming, relatively wide spectral response and readout flexibility that allow them to be applied in situations where other solid state imagers can not. Recognizing this industrial need for video sensoring devices, General Electric has begun the development of a smart camera system. This system will provide not only standard TV rate video information, but will additionally have a capability of being programmed for limited classes of measurements and decisions relating to objects within its visual field.

Processed output from the camera will be standard digital format suitable for computor or other digital processing equipment. The smart camera will then be a true peripheral sensing device requiring a minimum of interface. General Electric is currently working in close cooperation with two industrial firms having requirements in this area.

APPENDIX

CHARGE INJECTION DEVICE (CID) CONCEPT

1. Introduction

The charge injection imaging techniques make use of a two-dimensional array of coupled MOS capacitors to collect and store photo-generated charge. Coincident X-Y selection is used to inject the store charge into the bulk and the time integrals of the charging currents to the MOS capacitor plates are detected for readout. Shift registers along two edges of the imaging array are used for raster scanning. Some features of this technique are design simplicity, compatibility with standard MOS processes, high defect tolerance and excellent signal-to-noise performance. This section will describe the basic sensor mechanism, the X-Y scanning and various readout techniques.

2. The Basic Sensor Mechanism

The basic device is an integrating photon detector consisting of an MOS capacitor biased above threshold. Minority carrier charge generated by the incoming photons is collected and stored in the surface inversion regions under the capacitor electrodes. Since most CID imagers have been p-channel devices constructed on n-type substrates, holes are the minority carriers and negative voltages are applied to the gates of the MOS capacitors. As holes are collected in the inversion layer under the MOS capacitor, the capacitance increases. If now the gate is pulsed close to zero volts, the collected charge is injected into the substrate where it recombines or is collected. On reapplication of the negative voltage, the signal charge is absent and the capacitance of the MOS capacitor returns to a lower value close to the depletion layer capacitance. For readout one can detect signal charge by integrating the charging currents or measure the capacitance change. These will be discussed later when the various readout techniques are described.

For the substrate and the drive line readout techniques, the injected signal charge must be rapidly eliminated. In bulk substrates, this occurs principally by means of recombination centers in the silicon. Since these

centers are also a source of dark current, their number should be kept small. This compromise between low dark current and recombination of injected charge set a speed limitation of about one microsecond for the injection pulse width. This limitation has been overcome by use of n-epitaxial layers on p-substrates. This places a p-n junction below the sensing site which collects the injected charge as in a bipolar transistor. The use of the epitaxial substrates has been shown to be highly effective for injection pulse widths in the order of 100 nanoseconds. In fact, reverse biasing of the p-n junction virtually eliminates the injection problem. The use of "p-streets" adjacent to the sensing capacitors has also been shown to be an effective collector of injected charge.

3. X-Y Scannable Structure

The simple MOS structure described above, while suitable for one dimensional (line) imaging, requires modification of use in area imaging. If two MOS capacitors at each sensing site are coupled together so that stored charge can be transferred from one capacitor to the other, then a two-axis selection method can be used for scanning. The basic approach is to design each capacitor such that it can store the signal charge when voltage is removed from the other capacitor electrode. Injection will then occur only when both electrode voltages are switched off.

Various methods can be used to couple surface charge between adjacent electrodes. Among these are fringing fields, which require a very narrow interelectrode gap, overlapping but insulated electrodes, or the use of an interconnecting diffused region. Both overlapping electrodes and interconnecting diffused regions have been used by General Electric.

In order to clearly explain the operation of this image sensing technique, the concept of potential wells in MOS structures will be used. When voltage is applied to a MOS structure in which the oxide capacitance is much greater than the depletion capacitance, and there is no charge stored in the surface inversion region, then most of the applied voltage appears across the depletion region. The potential of the silicon surface under the metal electrode is slightly less than, but approximately equal

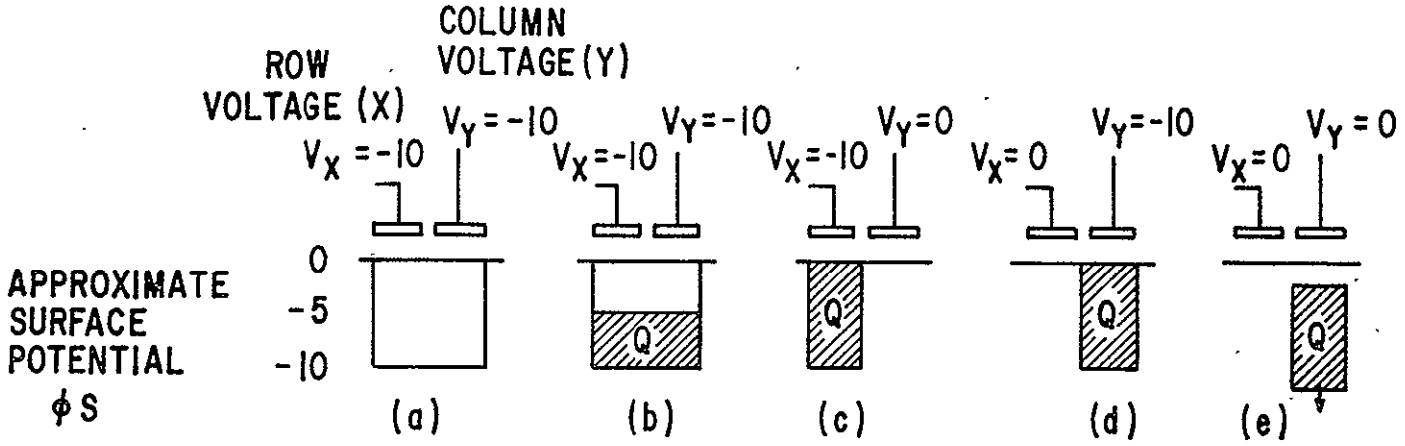
to, the applied voltage minus the threshold voltage. This surface potential can be thought of as a potential well in which inversion region charge can be stored. As the quantity of charge stored increases, the surface potential decreases in magnitude and reaches approximately zero when the inversion region is saturated (completely filled) with charge. The diagrams in Figure 1, which illustrate the distribution of surface potential and stored charge between the coupled MOS capacitors under various drive conditions, are useful in explaining the operation of this structure.

The surface potential distribution between a pair of electrodes is shown in Figure 1(a) when the indicated voltages are initially applied. Figure 1(b) illustrates the conditions that would apply if the maximum value of charge were stored at a sensing site. Note that the potential wells are not saturated. If the Y-line voltage is switched to zero while X-line voltage is still applied, the conditions of Figure 1(c) apply. Charge has been transferred from the Y electrode to the X electrode but not injected. When a row is selected for readout, the X-line voltage is switched to zero. The charge that was stored under X electrode transfers to the adjacent Y electrodes, Figure 1(d). Subsequent pulsing of the Y-line voltage to zero results in injection of the stored charge at the selected site, Figure 1(e).

Scanning for a raster type of readout involves switching each row, in sequence, to zero volts, and sequentially pulsing all of the column voltages to zero while each row is selected. Each sensing site has voltage applied to either or both electrodes for the total frame time less the injection pulse width applied to the Y electrodes; therefore, photon integration time is very nearly equal to the frame time.

A very simple topological structure results with this image sensing technique. Two MOS capacitors at each sensing site are coupled either with an electrically floating p^+ island or by a fringing field resulting from an overlapping gate structure. Array connections are readily made using the two level conductor capability of self registered MOS processes such as silicon gate.

SENSING ELEMENT SURFACE POTENTIAL



(a) INITIAL CONDITION, STORED CHARGE $Q_S = 0$

(b) $Q_S = Q_{FULL\ SCALE}$

(c) UN-SELECTED LINE

(d) SELECTED LINE PRIOR TO INJECTION

(e) SELECTED LINE, INJECTION

Figure 1. Sensing Element Surface Potential for Various Operating Conditions.

4. Parallel Injection Readout

The injection-detection process in the drive line readout at each sensing site is itself sequential and consists of the following operations:

- Charge injection
- Amplifier overdrive recovery
- Signal level sample-hold
- Integrating capacitance voltage reset.

To reduce the cycle time even further, one can use parallel injection readout, which eliminates the first two operations listed above.

This method involves maintaining the row electrodes at a more negative voltage than the column electrodes such that all the charge is stored beneath the row electrodes. This effectively isolates the stored charge from the column electrodes and voltages. This permits the setting of all the columns to a reference voltage (Vs), through column load resistors, by pulsing the S-control as shown in Figure 2. If the voltage of the selected row (X3) is switched to zero, the signal charge will transfer from the X3 row pads to the column pads. The voltage on each of the column lines will then be reduced by an amount approximately equal to the signal charge divided by the column capacitance. The signal charge then can be sensed by sequentially connecting each column line to a video amplifier by the use of a scanning register and MOS switches. The readout operation would consist of resetting the video amplifier input to the reference voltage, and then stepping the scanning register to the next column line. After all the columns of the array have been scanned, the charge in the column pads of the selected row could be injected simultaneously by switching all the columns to zero voltage. This would be done again through the load resistors by setting Vs to zero and turning on the load resistor gates. This parallel injection would take place during the horizontal line blanking. Alternatively, the charge need not be injected but can be returned to the row pads for further integration or future processing, effectively resulting in a non-destructive readout.

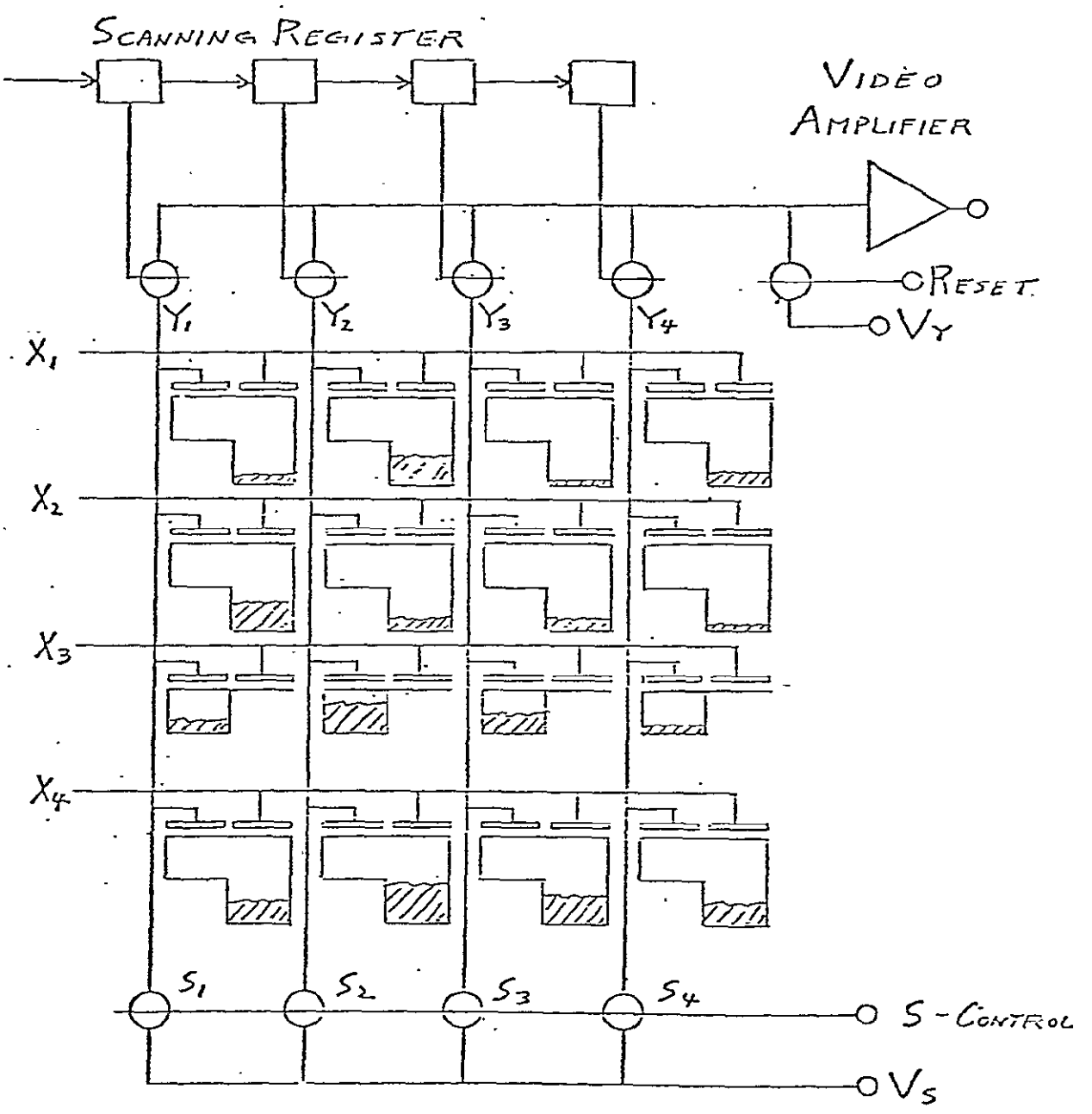


Figure 2. Parallel Injection Readout

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The non-destructive readout characteristic of the parallel inject scheme has been evaluated on high density CID arrays, the arrays were operated at reduced temperature to minimize dark current and thereby achieve long storage time intervals.

Storage time in excess of three hours has already been achieved at operating temperatures of approximately -70°C. Furthermore, arrays have been read continuously over these same period non-destructively at least 300,000 times with no detectable information loss.

Two experiments have been performed which serve to identify the potential limiting factors in NDRO (Non-Destructive Read-Out). In the first, a charge pattern for image was generated and stored by momentarily opening the camera shutter. The array was continuously read out at a rate of 30 frames per second until image degradation was noted. At an array temperature of -70°C, images were readout far in excess of three hours (324,000 NDRO's) with no detectable charge loss.

In the second experiment, a series of time exposures were made at successively lower light levels and the time required to reach a given signal level was measured. The results, Figure 3, show conclusively that there is no reciprocity failure between the inverse of exposure time and light intensity level. The readout charge losses per NDRO is clearly less than one carrier per CID site per frame.

This readout method results in a cycle time for each element consisting of only two operations, a sense amplifier reset and a signal level sample-hold. Besides the apparent speed advantage, this method permits the use of an on-chip amplifier which will reduce noise level considerably. This method has been tested on arrays and was shown to have the expected properties. Both small and large scale arrays have already been successfully implemented using this readout scheme.

5. Pre-Injection Readout

A fourth readout technique, dubbed "pre-injection", is similar in some respects to the parallel injection technique, but has some novel and useful consequences. Basically, the readout occurs as follows (see Figure 4):

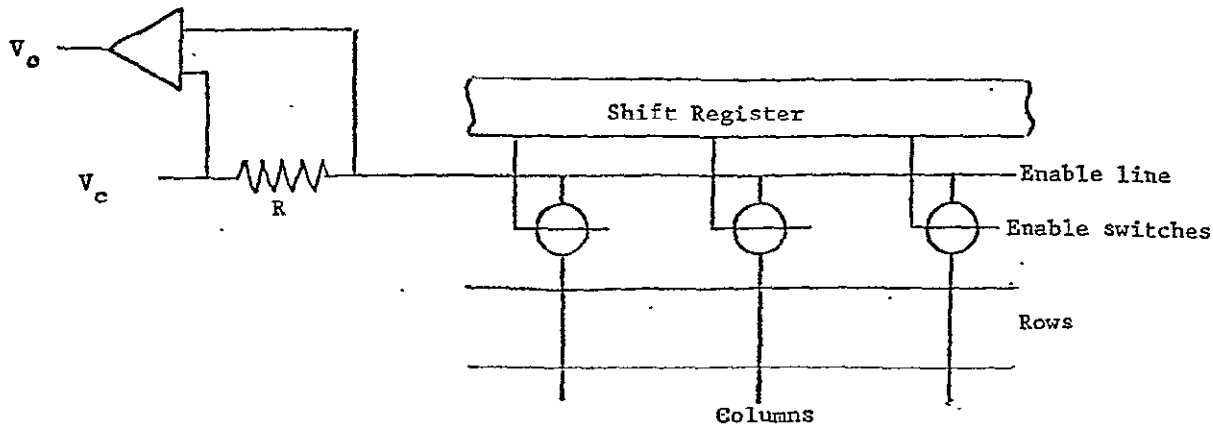
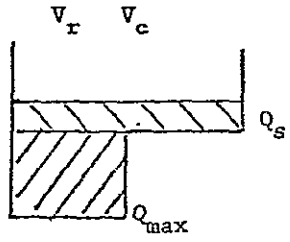
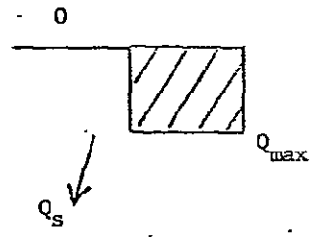


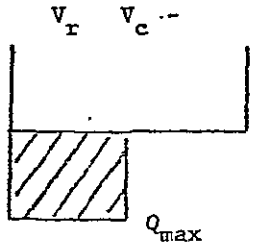
Figure 3. , Pre-injection Readout Circuit



a) Before Row Selection

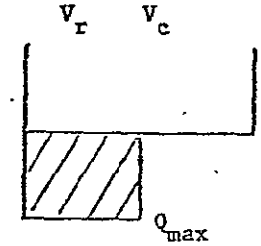


b) Row Selection/Pre-injection



$$V_{col} \approx V_c - \frac{Q_s}{2\,C_{col}}$$

c) Row Reset



$$\Delta V = \frac{Q_s}{2\,C_{col}}$$

d) Read/Reset

Figure 4. Read Out Sequence

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a) The rows are at a reference voltage V_R and the columns are at a reference voltage V_C. At each site there is a bias charge which, by proper selection of voltages, can be entirely under the row pad, and a signal charge, which is equally shared by the two pads. The bias charge is equal to the maximum charge that can be stored under a column pad. The columns are connected sequentially by the shift register to the voltage V_C through a load resistance R. Thus, the columns float at all times except when they are selected for readout. At that time, they are reset to the voltage V_C if their voltage has changed since the previous line was read out. The voltage will have changed if there has been a net change in the charge stored in the column wells. The current or charge that flows during reset constitutes the video signal.

b) A row is selected by raising its voltage to, say, zero. Charge is transferred simultaneously from all the row wells into the column wells. Because of the bias charge, the column wells become completely filled and the excess charge, the signal charge that has accumulated since the previous selection of the row, is injected.

c) The row voltage is reset to V_R which, if it is approximately twice the column voltage, results in the transfer of the column charges back into the row wells. Before injection, half the signal charge (positive) was under the column pads. After injection, the wells under the column pads are empty. Since the columns are floating, the column voltages are now more negative than the reference voltage by an amount equal to the charge difference, half the signal charge, times the line capacitance.

d) The columns are reset, sequentially, to V_C. The variations in column voltage appear across R and are amplified by the amplifier A. This video can be used directly, but is freer of extraneous noise if it is sampled periodically.

There are several consequences of this readout procedure.

(1) The column voltage varies between interrogations not only because charge is injected from the selected sites (which tends to make the column voltage more negative), but also because charge is accumulating under the pads at unselected sites (which tends to make the column voltage become more positive). The net change in voltage of a column then depends upon the relative magnitude of the injected signal charge (which has been accumulating for a frame time) and the sum of all the changes that have accumulated since the previous reset, i.e., during one line time. If the entire column is uniformly illuminated, the net signal is very small:

$$\Delta V = (1/C_{col}) \; (-Q_s/2 + (N_r - 1) \; Q_s/2 \; N_r)$$

where Q_s is the signal charge collected at each site during one frame time, and N_r is the number of rows.

For a more general illumination, the voltage on column j at the time row i is read out is:

$$\Delta V_{ij} = (1/C_{col}) \; (-Q_{sij}/2 + \sum_{n \neq i} Q_{snj}/2 \; N_r).$$

Clearly, there is no disadvantage if the image is a small number of isolated sources.

(2) Note that only half the signal charge at a site appears under the column pad and is detected. Thus the output voltage is half that observed using parallel injection readout, and, if noise sources are identical, the pre-injection technique will be less useful at low light levels. However, the maximum output voltages are identical (Q_{max}/C_{col}) and the dynamic ranges are the same.

(3) Under overload the pre-injection technique performs uniquely and to great advantage. Consider, for example, a single site overloaded by a factor of 10. Once the row containing the overload has been read out, the next $N_r/10$ rows will exhibit a positive going (black) signal of amplitude $10 \; Q_{max}/N_r$ in the column containing the overloaded site. The wells at the overloaded site will then be full and

no further signal will be observed until the affected row is again read out. In other words, there is partial black column blooming, with the length of the black line decreasing as the overload increases.

(4) The amplitude of the signal readout from the overloaded site is also affected, to a degree that depends upon its position along the row (i.e., depending upon which column it is in). This occurs because, once injection occurs (at row selection time) charge can again start to integrate under the column pad so that, at read time, it is no longer empty, but contains charge proportional to the time since injection. This time is a fraction of a line time and the charge is undetectable at normal illumination levels. However, at very high light levels (e.g., an overload of 10X) if the overloaded site is in the last column, the readout signal will be reduced by the fraction $10/N_r$.

(5) Signal processing techniques can, of course, remove the "unselected signal", as well as the black column blooming, from the video output.

6. Differential Row Readout

An extremely interesting variation of the CID NDRO charge sensing method is in a readout strategy that promises to eliminate a major component of noise, namely KTC noise, while simultaneously cancelling fixed pattern (spatial) noise.

All solid state imagers (CCD as well as CID) are limited in dynamic range by a fixed spatial noise background caused by variations in structure and by the readout process; not by temporal (random) noise. The non-destructive readout capability of the parallel injection CID structure makes it possible to measure the output with and without signal charge and to take the difference. In principle, this would result in complete cancellation of fixed pattern noise.

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