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STATUS OF SILICON SOLAR CELL TECHNOLOGY

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ABSTRACT

Major progress in solar cell technology leading to increased efficiency has occurred since 1970. In this time period, cell efficiency has increased by about 50 percent. Technical approaches leading to this increased output include surface texturizing, improved antireflection coatings, reduced grid pattern area coverage, shallow junctions and back surface fields (e.g., n^+-p-p^+ structures). The status of these developments and their incorporation into cell production is discussed. Future research and technology trends leading to further efficiency increases and substantial cost reductions are described.

INTRODUCTION

Since 1970, the efficiency of silicon solar cells has increased dramatically. At that time, the average outer space efficiency of silicon solar cells was 10.5 percent. In 1976, laboratory cells have reached efficiencies of 15.5 percent and cells produced in high volume have efficiencies over 13 percent. Most of this increased output has resulted from increased short circuit current, with only minor increases in open circuit voltage being reported. It is the purpose of this paper to review the past accomplishments and to examine the potential of further efficiency increases and cost reductions so that potential research areas can be identified.

STATE OF PRESENT TECHNOLOGY

Short Circuit Current

Solar cell short circuit current can be increased in two ways: first, the amount of light absorbed by the cell can be increased and secondly, the efficiency of collecting the minority carriers generated by absorbed light can be increased. Both paths have contributed substantially to improvements in cell output.

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Increased Absorption

The amount of light entering the cell can be increased by reducing the area of the cell surface covered by the grid pattern and by reducing the reflectivity of the cell surface.

Grid pattern. - In 1970, the standard grid pattern on a 2- by 2-cm cell covered about 10 percent of the surface. Improved metal masks capable of forming lines 50 μm wide instead of 150 μm or the use of photoresist technology to form very fine lines are now in routine use. With these technologies the area covered by the grid pattern has decreased to about 5 to 7 percent.

Antireflection coatings. - The antireflection coating in use in 1970 was a quarter-wavelength thickness of SiO. SiO was used because its refractive index was a good match between the silicon surface and an air interface. However, when these cells were covered with a silicone adhesive and the cover glass needed in the space environment, a loss in current of about 3 percent was observed as shown in Table I. This loss occurred because the refractive index of the adhesive was not the 1.0 of air or vacuum but about 1.43. Reoptimization of the antireflection coating to account for this difference required higher refractive index coatings such as TiO_x, Ta_2O_5, or CeO_2. As shown in Table I, these coatings produce cells with lower currents than those covered with SiO prior to cover glassing. However, upon addition of the cover glass the current increased to a level about 7 percent greater than a cover-glassed, SiO coated cell.

Texturizing. - The most important advance in increasing the amount of light entering the cell came through the use of surface texturizing (refs. 1 and 2). In this process, the surface of ⟨100⟩ orientation silicon crystals is etched with alkaline chemical etchants such as KOH, NaOH, or hydrazine-hydrate. These etchants result in surfaces covered with a myriad of pyramids as shown in figure 1. The first benefit of this surface is to substantially reduce the reflectivity. This reduction occurs because the incoming beam undergoes multiple reflections as shown in figure 2. About 33 percent of the light is reflected from the first surface onto the second, the remainder having been refracted into the silicon. Similarly

33 percent of the remaining beam is reflected from the second surface. This leads to a total reflectivity of about 11 percent. Addition of a high refractive index antireflection coating and a cover glass results in a reflectivity of only 3 percent. Furthermore, the reflectivity of this surface is almost independent of wavelength. For comparison, the reflectivity of a smooth cell coated with SiO (1970 technology) depends strongly on wavelength (ranging from 1 to 35 percent) and averages about 10 percent.

The second benefit arises from the oblique path of the refracted light beam through the silicon. This longer path length leads to increased absorption of infrared light. Furthermore, the infrared light is totally internally reflected from the smooth back surface of the cell. Thus, the path length of infrared light is about three times the actual cell thickness and results in thin cells having very high responses in the infrared.

Increased Collection

Increased collection of minority carriers generated by the light has resulted from improvements in cell design and processing procedures.

Texturizing. - The second benefit of surface texturizing occurs because light is being refracted and absorbed on a path roughly parallel to the pyramid surfaces. The p-n junction has been diffused into the surfaces of the pyramids. Thus light absorption occurs roughly parallel to the junction thus leading to increased collection efficiency.

Shallow junctions. - Shallow junctions have been used to offset the poor collection efficiency of the diffused region. Sheet resistances in the 120 to 500 $\Omega/\square$ range resulting from phosphorus diffusions in the 800° C temperature range are in common use (ref. 3). These diffusion conditions lead to junction depths on the order of 0.1 to 0.2 μm. Such shallow junctions have resulted in substantial increases in the blue region of the cell spectral response.

Increased minority carrier lifetime. - The minority carrier lifetime measured in n^{+}-p silicon solar cells ranges from 6 to 10 microseconds (ref. 4), independent of lifetime of the starting ingot. Extensive studies have shown that processing is not the cause for this loss in effective lifetime. Rather, it is the front and back surface recombination velocities coupled with wafer thickness that significantly influence the measured lifetime (refs. 5 and 6). For example, a 300 μm thick cell has a lifetime of about 8 μsec, while a 100 μm thick n^+-p cell has a lifetime of only about 1 μsec (ref. 7). This reduction is caused by the infinite surface recombination velocity plane resulting from the ohmic back contact moving closer to the junction. As this plane approaches the junction it causes recombination of substantially more of the minority carriers that otherwise would have been collected by the junction.

Use of a back surface field (e.g., n^+-p-p^+ structure) yields a back surface with a zero surface recombination velocity. Thus minority carriers are no longer recombining at the surface and the apparent lifetime increases to 30 to 40 μsec in the cells (ref. 8). This increase in lifetime leads to increases in current of a few percent but leads to a more important effect on cell voltage.

Open Circuit Voltage

Cell open circuit voltage can be increased most straightforwardly by increasing the base doping level of the cell. This leads to increases in voltage to the 0.6 V level. A second approach to increasing voltage came through the back surface field structure.

Back surface field. - The inclusion of the back surface field in cells made from 10 Ω-cm p-type material produced an increase in voltage of about 50 mV as shown in figure 3. Two factors lead to this increased voltage. First, the zero surface recombination velocity plane at the rear of the cell leads to basic alteration to the theoretical equation describing the reverse saturation current of the diode (ref. 9). Secondly, the true bulk material lifetime must be used in the I_0 equation. This value of lifetime is larger than believed previously from measurements on cells with ohmic back contacts but is consistent with present measurements and theoretical understanding. Use of the long lifetime and the proper theoretical expressions leads to voltages independent of thickness as shown in figure 3. The addition of the back surface field (BSF) raised cell voltage to the same level of performance as cells made from 1 Ω-cm material. Inclusion of the BSF in 1 Ω-cm material has resulted in no alteration to cell voltage but a slight increase in current.

Device Performance and Production Status

Increased device performance results from inclusion of the above technologies into the cell. However, transition from the laboratory to cost effective production is difficult and represents a significant barrier to rapid introduction of new, marketable solar cell devices. Table II summarizes the technologies used and the production status of current improved efficiency cells. As can be seen in the table, all of the advantageous technologies described above have been incorporated into one or the other of the advanced cells. However, a gap of two or more years between announcement of an improved performance cell and its introduction into high volume production is not unusual.

Table III compares the performances of the 1970 cell with two of the new technology cells. All cells have cover glasses. As described in Table II, the helios and violet cells are similar in characteristics; therefore, only the helios cell was included in Table III because of its advanced production status. The violet cell has a slightly higher open circuit voltage than the helios cell because of the use of 2 Ω-cm material. This leads to a slightly higher efficiency of 13.5 percent. The highest performance is achieved by the CNR cell at 15.3 percent. All efficiencies are at air mass zero irradiance.

From Table III it is clear that most of the improved output comes from increased short-circuit current. The increased voltage comes from use of the p^+ back surface field and lower resistivity material. Improved fill factor is the result of both improved grid geometry and junction processing procedures. A comparison of the spectral response of a CNR cell and a 1970 cell is shown in figure 4. The CNR cell has a quantum yield (electrons collected per incident photon) above 90 percent over most of the response region. This includes the 3 to 4 percent of light reflected away. Thus it appears that little additional increase in short circuit current can be anticipated in the future.

Future Research and Technology Trends

Although developments to date have been significant and exciting, additional research and development opportunities exist. Further efficiency increases can be expected and cost reductions by orders of magnitude can be predicted. Both basic research and high technology will play important roles.

Open-Circuit Voltage

The last substantial barrier to achieving the maximum practical efficiency of about 19 percent (ref. 10) is the open-circuit voltage. Although simple diode theory predicts an increasing voltage with decreasing resistivity, contrary results are obtained experimentally as shown in figure 5. The highest voltage reported for 0.1 Ω-cm material is 0.61 V instead of the 0.7 V calculated. Also the base region minority carrier lifetimes in the 0.1 and 0.01 Ω-cm cells are sufficiently great so as to yield much larger open-circuit voltages. Thus it appears that a low emitter efficiency of the diffused region is the cause of poor voltages. Several effects may act to reduce the voltage. These include band gap narrowing due to heavy doping effects (refs. 10 and 11), increased interband transition rates (recombination effects) (ref. 11), defect clustering (ref. 11), and photovoltage saturation (ref. 12). Band gap narrowing acts to alter the intrinsic carrier concentration (n_i) in silicon. This would increase I_o for the emitter by several orders of magnitude. Figure 6 shows the results of calculations of the magnitude of this effect on presumed Gaussian impurity profiles having maximum surface concentration values from 1×10^{19} to 4×10^{20} cm^{-3} (ref. 10). At all but the lowest surface concentration, band gap narrowing effects have substantially altered the presumed profile and resulted in retrograde effective doping profiles. These retrograde profiles would lead to increased recombination of minority carriers at the surface and hence lower collected currents even with long lifetimes.

Increased interband transition rates of minority carriers would substantially reduce the lifetime in the diffused region. This would also increase I_o from the emitter by several orders of magnitude. Until recently, no experiment had separated these two effects, each of which could explain the reduced voltage. Measurements of both the minority carrier lifetime and the charge stored in the emitter of 0.1 Ω-cm cells disclosed high stored charge and high minority carrier lifetime consistent with a band gap narrowing mechanism (ref. 13).

Defect clustering and photovoltage saturation have not been fully explored at this time. Defect clustering would result in localized shorting of the cell voltage. Photovoltage saturation is a basic phenomenon that occurs at high injection levels and its importance in the 0.1 Ω-cm cell has not yet been established.

The mechanisms described above also influence bipolar transistor current gain and frequency response. Thus they represent areas in need of focussed attention.

Several approaches to increase cell voltage have begun to be explored. The use of alternate dopants, ion implantation, and epitaxial structures have received initial attention. At the present time, the most significant results have been obtained using epitaxial structures. Fabrication of the p^+-p-n-n^+ graded base structures shown in figure 7 has resulted in a cell whose open circuit voltage exceeded 630 mV (ref. 14). The significance of use of the p on n structure is not presently clear. While this gain is modest it points with optimum to the future.

Short Circuit Current

The most significant remaining research area relating to short circuit current is reduction of surface recombination velocity, S. Measurements of the surface recombination velocity of the antireflection layer covered, diffused cell surface were made using MOS capacitor structure shown in figure 8 (ref. 15). These measurements, since verified by a scanning electron microscope technique indicated the number of surface states to be about 2×10^{13} cm^{-2} with a surface dopant concentration of 3×10^{20} cm^{-3}. This results in a surface recombination velocity between 5×10^3 and 10×10^3 cm/sec. This value is about one order of magnitude lower than previously estimated. A reduction of S to 10^3 cm/sec at the most is required before full cell short circuit current can be achieved.

Low Cost Technology

The most significant barrier to the widespread use of solar cells in the terrestrial environment is cost. Reduction in the cost of solar cell arrays from the present \$20 per watt to the 10 to 50 cents per watt level appears to be necessary to achieve widespread use (ref. 16). The ERDA National Photovoltaic Program in the United States of America and Project Sunshine in Japan are clearly focussed in this target. Both automated, high rate cell, and array production and various new technologies appear to be required to meet these stringent cost requirements. A variety of cost reduction approaches can be identified.

Near term approaches. - Table IV summarizes some near term cost reduction approaches that are currently under investigation (ref. 17). Currently, 100 mm diameter round cells are being produced in small quantities on demand and 75 mm cells in volume production. Improved saving techniques that would reduce kerf loss are being studied. A prototype semi-automatic production line using non-vacuum processes including screen printed contacts and spin-on anti-reflection coatings is in operation. The use of non-gaseous dopant sources such as spin-on and solid sources and ion implantation are being explored. Automatic vacuum processing of cells is possible, but no large scale investigation of this approach are underway. Full scale implementation of these techniques into high volume automated production could reduce cell costs below \$2 per watt in the next few years.

Long range approaches. - Before the cost goal of 10 to 50 cents per watt can be reached approaches outlined in Table V appear necessary. Reductions in the cost of raw silicon starting material and high rate production of silicon ribbons will play a significant role.

Reduction in the cost of raw silicon material has centered on two approaches (ref. 17). One has been assessing the minimum purity necessary for high efficiency solar cell production. The other has examined the economics and feasibility of reduction of silicon compounds other than trichlorosilane. The first approach has shown that impurity levels of 10^{14} to 10^{15} cm^{-3} of most elements do not appear to significantly reduce cell performance. This tolerance to high impurity levels suggests that significant cost reduction are possible.

Secondly, cost reductions to below $10/kg from the present level of $60/kg appear to be possible with reduction of SiH_4 rather than $SiHCl_3$. Verification of these results awaits further study.

A variety of techniques for producing ribbon silicon are currently underway. These include: EF6 (edge-defined film-fed growth), web dendrite, Stepanov process, horizontal Si ribbon growth, and the ribbon float zone (ribbon-to-ribbon) approach. Major technical barriers to be surmounted include high rate production of ribbon having high perfection and long minority carrier lifetimes. To date, only the web dendrite approach has yielded cells with terrestrial efficiencies in excess of 12 percent (ref. 18). The other processes are still in early stages of development and further increases in quality are expected.

Finally, the development of thin film cells may yield further cost reductions. To date, efficiencies of about 6 percent have been achieved in thin film silicon cells. However, cell efficiency appears to be proportional to grain size; hence a major study of the recombination mechanisms present within the grains and at the grain boundaries is needed.

Thus a vigorous, wide ranging research and development program is underway to achieve the goal of 10 to 50 cents per watt solar cell arrays. Key research and technology opportunities exist in all areas of cell development.

SUMMARY

An increase in silicon solar cell efficiency of 50 percent has taken place since 1970. The 15 percent efficiency achieved in laboratory cells has been accomplished primarily through increases in short circuit current. Substantial increases in voltage will be needed in the future if the 19 percent efficiency practical limit is to be achieved. The last major barrier to widespread terrestrial use of solar cells is cost. Significant research and development opportunities exist in achieving automated, high volume production of solar cells made from ribbon silicon or thin film layers.

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TABLE I. - EFFECT OF COVER GLASSING ON SHORT-CIRCUIT CURRENT OF SOLAR CELLS

	SHORT-CIRCUIT CURRENT	
	SIO	Ta_2O_5
COATED CELL ONLY	142 mA	140 mA
COATED CELL WITH COVER GLASS AND ADHESIVE	138 mA	147 mA

TABLE II. - SUMMARY OF PRESENT HIGH EFFICIENCY SOLAR CELLS

DESCRIPTION	STATUS
HELIOS CELL 20 Ω-CM P^+ BACK SHALLOW JUNCTION THIN GRID FINGERS Ta_2O_5 AR COATING	IN PRODUCTION BY SPECTROLAB
VIOLET CELL 2 Ω-CM P^+ BACK VERY SHALLOW JUNCTION FINE GRID FINGERS Ta_2O_5 AR COATING	NEARING PRODUCTION BY OCLI
COMSAT NON-REFLECTIVE CELL ETCHED, LOW REFLECTION SURFACE OTHERWISE LIKE VIOLET CELL	LABORATORY, NOT OPTIMIZED COMSAT CORP.

TABLE III. - PERFORMANCE COMPARISON OF SILICON SOLAR CELLS

	1970 PRODUCTION CELL	HELIOS CELL	CNR CELL
SHORT CIRCUIT CURRENT, I_{sc}	138 mA	157 mA	181 mA
OPEN-CIRCUIT VOLTAGE, V_{oc}	545 mV	585 mV	595 mV
MAXIMUM POWER, P_{max}	55 mW	70 mW	83 mW
FILL FACTOR*, FF	73%	76%	77%
EFFICIENCY (AMO), η	10.2%	13%	15.3%

$$*FF = \frac{P_{max}}{V_{oc} I_{sc}} \times 100$$

TABLE IV. - NEAR TERM SOLAR CELL COST REDUCTION APPROACHES

IMPROVE MATERIALS UTILIZATION

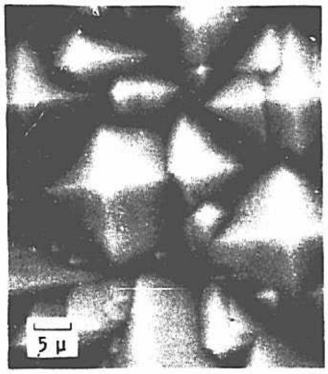
- USE LARGER DIAMETER SINGLE CRYSTAL INGOTS
- REDUCE SAWING LOSSES
  - USE ROUND CELLS
  - REDUCE KERF LOSS

AUTOMATE CELL MANUFACTURING PROCESSES

- ELIMINATE VACUUM PROCESSES
  - USE SCREEN PRINTING FOR CONTACTS
  - USE "SPIN ON" TECHNIQUES FOR ANTIREFLECTION COATINGS
- ELIMINATE GASEOUS DOPANT SOURCES
  - USE "SPIN ON" TECHNIQUES
  - USE ION IMPLANTATION

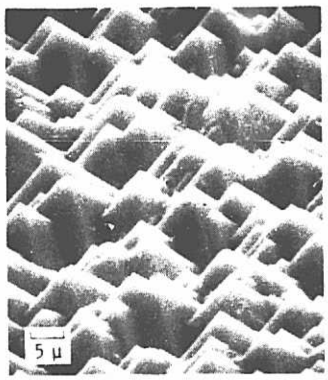
TABLE V. - FAR TERM SOLAR CELL COST REDUCTION APPROACHES

- REDUCE COST OF POLYCRYSTALLINE SILICON STARTING MATERIAL
- HIGH VOLUME PRODUCTION OF RIBBON SILICON
- DEVELOP THIN FILM CELLS



PERPENDICULAR TO SAMPLE

45° OBLIQUE VIEW



45° OBLIQUE VIEW ROTATED 70°

Figure 1. - Views of texturized surface.

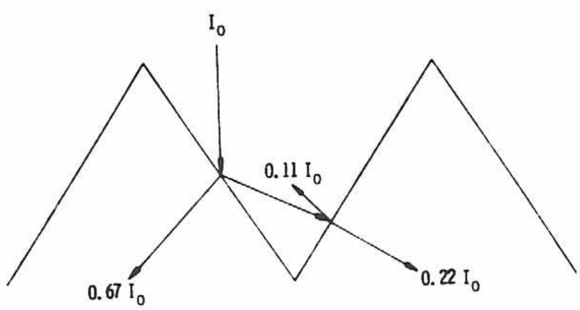


Figure 2. - Optical path diagram of tetrahedral texturized surface.

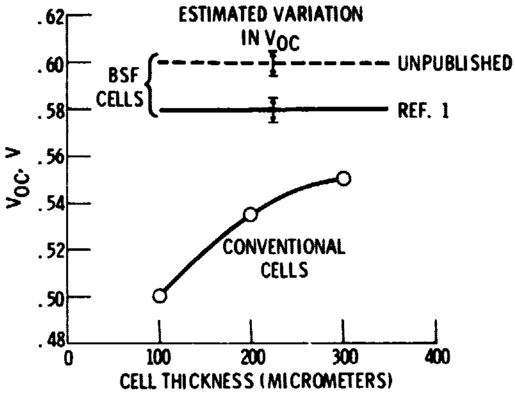


Figure 3. - Experimental thickness-voltage performance of BSF and conventional 10 ohm-cm cells.

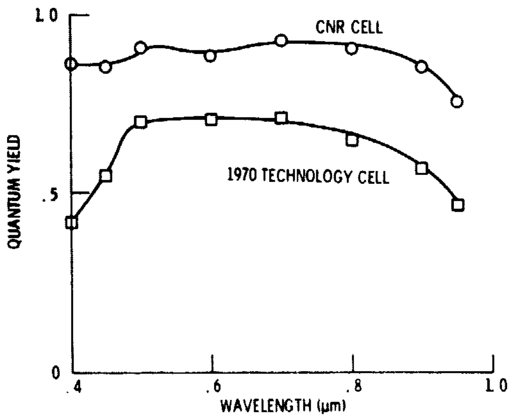


Figure 4. - Quantum yield comparison of solar cells.

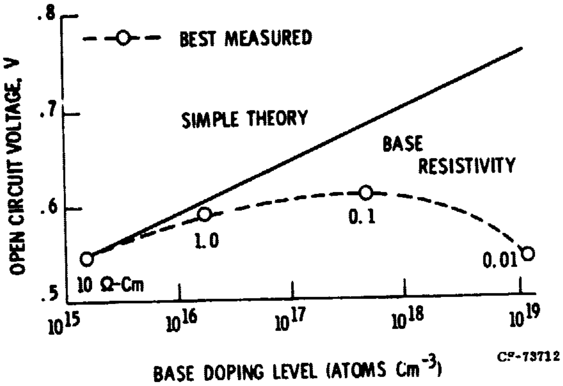


Figure 5. - Dependence of solar cell open circuit voltage on doping level.

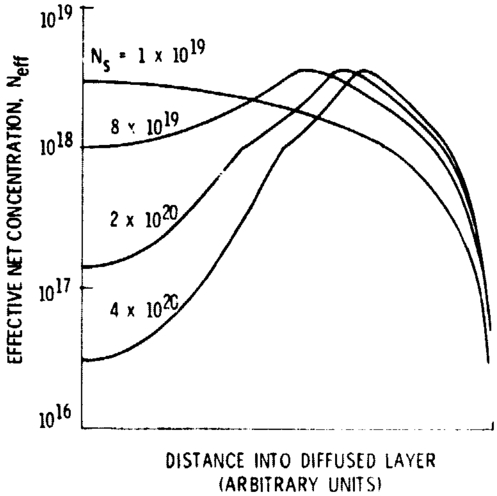


Figure 6. - Effective impurity profile in diffused layer of a solar cell.

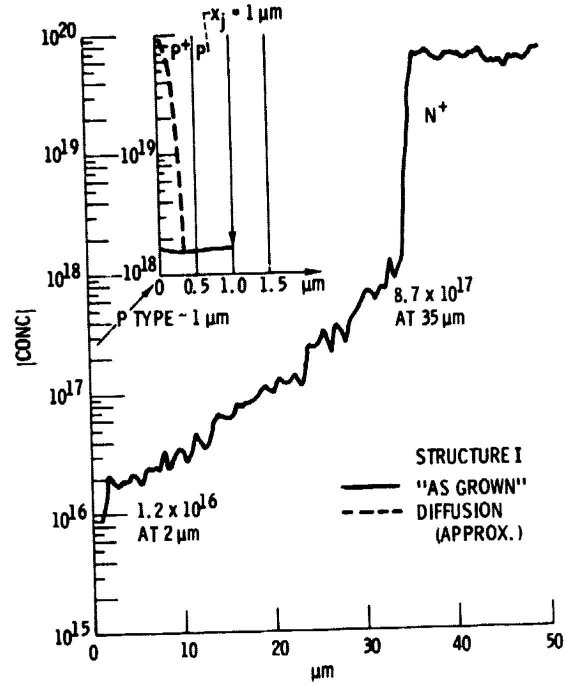


Figure 7. - Impurity profile in the epitaxial high voltage solar cell structure.