X-311-76-266
PREPRINT

A SURVEY OF PARTICLE CONTAMINATION IN ELECTRONIC DEVICES

John W. Adolphsen
William A. Kagdis
Albert R. Timmins

DECEMBER 1976

GSFC
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

For information concerning availability
of this document contact:

Technical Information Division, Code 250
Goddard Space Flight Center
Greenbelt, Maryland 20771

(Telephone 301-982-4488)

X-311-76-266

A SURVEY OF PARTICLE CONTAMINATION IN ELECTRONIC DEVICES

John W. Adolphsen
William A. Kagdis
Albert R. Timmins

December 1976

GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

FOREWORD

This report is organized so that the first four sections contain a synopsis of the particle contamination problem, including background, purpose of this report, conclusions, and recommendations. The last section, "Technical Information," provides supporting information, including a discussion of various schemes for eliminating particles, for detecting their presence, or for insulating susceptible elements of a part from their presence or effects. Therefore, this section provides the technical basis for the committee's findings, for the conclusions drawn, and for the actions recommended.

The information presented in this report is not documented in any rigorous manner. Many individuals interviewed made some failure and cost data available, but did so on an informal, nondocumented basis. However, despite the lack of formal documentation, the committee feels that this report accurately reflects the status of the particle contamination problem at this time.

A SURVEY OF PARTICLE CONTAMINATION IN ELECTRONIC DEVICES

John W. Adolphsen, William A. Kagdis, and Albert R. Timmins
Office of Flight Assurance

ABSTRACT

Conductive particle contamination in electronic devices, a recurring problem in NASA launch vehicles and spacecraft, DOD space projects, and commercial space applications, sometimes causes spectacular failures. A number of solutions to the problem have been proposed, with a wide variation reported in effectiveness of the different proposals. This report reviews the experiences of a number of National Aeronautics and Space Administration (NASA) and Space and Missile System Organization (SAMSO) contractors with particle contamination, and the methods used for its prevention and detection, evaluates the bases for the different schemes, assesses their effectiveness, and identifies the problems associated with each. It recommends specific short-range tests or approaches appropriate to individual part-type categories and recommends that specific tasks be initiated to refine techniques and to resolve technical and application facets of promising solutions.

CONTENTS

A SURVEY OF PARTICLE CONTAMINATION IN ELECTRONIC DEVICES

BACKGROUND

Conductive particle contamination has presented problems in electrical and electronic devices since the earliest time of their manufacture. Its incidence and severity appears to be cyclic, occasionally causing catastrophic failures in systems and in missions. Its continued existence implies that its solution is not simple and that its causes are many. The electronics industry's general disregard of this problem in favor of others that more consistently affect manufacturing yields on the production line indicates that vendor losses attributable to conductive particles run at rates that are "acceptable" to them. Only when process control is lost, inspection "escapes" are excessive, or high reliability users pressure for improvements, do vendors take corrective actions.

The question of the importance of particle contamination appears to be highly subjective. An acceptable incidence to some vendors and users is too high for others. For example, some manufacturing processes or products are particularly prone to a high level of particle contamination, as in the case of power transistors in conventional resistance welded packages, where weld splatter is a prevalent problem. Although this source of particles can be virtually eliminated by using a different package, other problems occur, and costs may be increased by almost an order of magnitude. In the highly competitive market, the vendor usually reasons that it is better to have sales of a product that contains particles and is therefore subject to limited, occasional returns than to have no sales at all. On the other hand, users of Hi-Rel products normally press for a product that is less prone to a high incidence of particles and possible catastrophic failure. Because of budget and schedule limitations, other users may establish a different level of acceptability, assume a higher risk of part or system failure, and knowingly use a device that is susceptible to particle contamination.

The end effects of particle contamination are less arguable. Historically, the Delta project has experienced considerable difficulty with particle contamination in semiconductor devices. Power transistor failure caused by particles was determined to be the most probable cause of the failure of two Delta launch vehicles, and is suspected to have caused an "anomaly" in a third. In addition, because of the presence of particles, the Delta project has had to perform considerable rework and special testing on hybrid microelectronic devices in its guidance computer and, to a lesser extent, on other systems used on the vehicle. Particle contamination was also attributed as the cause of several Air Force launch vehicle failures. Other Goddard Space Flight Center (GSFC) projects or projects

with GSFC experiments that have experienced particle problems in microcircuits, hybrids, relays, transistors, and diodes are Atmosphere Explorer, Applications Technology Satellite, Earth Resources Technology Satellite, Geostationary Operational Environmental Satellite, International Sun-Earth Explorer, Mariner Jupiter/Saturn, Mariner Venus/Mercury, Nimbus, Small Astronomy Satellite, Synchronous Meteorological Satellite, Pioneer, and Sounding Rockets.

When the Delta project instituted the Particle Impact Noise Detection (PIND) test, an alarming number of parts were found to contain conductive particles large enough to cause short circuits. These parts had been procured in accordance with specification requirements and policies commensurate with standard GSFC procurement practices for devices used in "Hi-Rel" programs. The test results suggested that the problem could be wide-spread, and not limited to Delta's experience.

When GSFC management was informed of the situation, a three-man committee was appointed to investigate the subject on a broad basis. The scope of the investigation was to encompass the general problem of conductive particle contamination in cavity-type electrical and electronic devices. The committee's efforts included: (1) a review of the literature, (2) visits to microelectronic vendors, NASA and SAMSO* contractors, and NASA Centers (which were all engaged in the procurement, manufacture, test, or use of electronic parts), (3) telephone conversations with individuals in industry and government, and (4) examinations of processes and techniques as implemented. Because of time constraints, the committee performed no testing itself for this report.

PURPOSE

The purposes of this study were:

- To obtain factual information from government and industry sources concerning such problems as failures, costs, and schedule impacts attributable to particle contamination, as well as their broader ramifications.

- To evaluate the severity of conductive particle problems in electrical and electronic devices with cavities.

- To determine if and how devices containing particles could be identified.

*Space and Missile System Organization.

- To determine if conformal coatings exist that would immobilize particles.

- To use the foregoing information and evaluations for making appropriate recommendations to GSFC management as to what GSFC policy should be regarding particle contamination.

SUMMARY

The following paragraphs summarize the salient information inputs and the observations and conclusions of the committee.

Particle contamination is frequently a serious problem, particularly in space applications in which mobility of the particles may cause failure in an item that had passed ground-based tests.

This committee could not obtain accurate cost information on failures caused by particle contamination from those interviewed. Some idea of the cost may be gained from the estimated losses of $32 million on Delta launches and $300 thousand on Nimbus retrofit costs. Approximately 12 other GSFC projects have incurred significant costs from particle contamination. In addition, five failures that were proven to be due to particles occurred in the Apollo and Skylab programs. The Air Force has reportedly had similar problems.

In addition to different interpretations as to how severe particle contamination may be, there often is disagreement within a project as to its importance in relation to other problems on that project. Assigning priorities and identifying which problems to address and to what degree are often difficult decisions, particularly with the present limited funding. However, because of the catastrophic nature of problems caused by particle contamination and the enormous actual and potential costs involved, it is essential that particle contamination at least be identified as a problem for possible action. Such project and economic factors have been considered by the committee in arriving at their specific recommendations.

Particle contamination problems in cavity electronic devices can be eliminated by using a conformal coating. Limited tests indicate that the use of Parylene, a vapor-deposited conformal coating material, is an effective solution to the particle contamination problem, but implementing the process by most of the industry poses formidable problems. The most important of these are (1) the general lack of information and understanding by semiconductor manufacturers of the process, (2) the skepticism by these manufacturers as to the severity of a particle problem, resulting in a strong negative attitude towards

adding Parylene coating as another process step, (3) the limited availability of production equipment, (4) the limited expertise for implementing application techniques to a variety of packages and products in a timely fashion, (5) the high cost of equipment installation, and (6) unknown, but reportedly high, handling losses associated with the application of Parylene. Additional long-term life and temperature limitation data are also needed before recommending Parylene for general use.

Steps can be taken to significantly reduce the incidence of particle contamination. Although proper manufacturing process controls, cleanliness in the manufacturing facility, and pre-cap visual inspection are major factors in significantly reducing the number of particles, they cannot be relied upon to eliminate them entirely.

Testing of the finished product for the presence of particles is widespread throughout the industry. The most common method of testing is X-ray inspection; other tests include monitored vibration (devices are electrically powered), monitored vibration with mechanical shock during vibration, X-ray followed by vibration followed by X-ray, and acoustic particle detection. Except for the latter, these tests are severely limited by inherent instrument and technique problems, with correspondingly poor test effectiveness. The best acoustic particle detection scheme—the PIND test—has been widely used throughout the industry. Initial and operating costs are very low,* and it can be effective in many applications. Although the effectiveness of this test can be seriously impaired by improper and inadequate implementation techniques, this problem is recognized and, together with other questions of calibration and standards, is being addressed and can be solved. This will enable more general use of the PIND test and will give the user greater confidence in its effectiveness.

PIND testing was originally specified for about 80 percent of the 14,000 hybrids in the Shuttle Orbiter. However, Johnson Space Center (JSC) is now considering the use of Parylene as a conformal coating to immobilize particles. It may be expected that, if costs and implementation problems are not prohibitive, many Shuttle hybrids (but probably not all) will be Parylene coated.

*Capital equipment costs are less than $4000. When PIND testing of a device is performed by the manufacturer as part of the specified screening procedure, his direct costs can be as low as 5 to 10 cents per device. Special PIND testing subsequent to part delivery, small quantity purchases, or change orders to vendors or to contractors and their subcontractors can result in dramatic cost increases of up to $100 per device. (See Appendix B.)

For many years, molded plastic semiconductor devices have been heavily used instead of hermetic cavity devices in commercial applications. Recent improvements in these devices may solve many reliability problems previously associated with these devices. The committee has discussed spaceflight applications of molded plastic devices with many individuals and companies, and has included a number of their comments with its observations in this report. The committee believes that the use of plastic devices in some space-flight systems requires further investigation. The Product Assurance Division of GSFC plans to initiate a modest effort to evaluate molded plastic devices.

RECOMMENDATIONS

The committee believes that only two ultimate solutions to the problem of conductive particle contamination may be possible at this time. (Parts that operate by mechanical action, such as relays and switches are not now considered.) These solutions are: (1) the use of Parylene as a vapor-deposited conformal coating* over all internal constituent elements of a cavity device; and (2) the use of molded plastic devices. The availability of money (from SRT/ART** or other sources), manpower, and time will determine if and when certain problems and questions associated with each can be answered. At the same time, the committee believes that PIND testing has great merit and is immediately applicable for selected part categories, but that it should be further refined at the same time as efforts continue on Parylene and plastic devices. This three-pronged approach should enable early determination of the most practical solutions.

The following specific recommendations, which apply to the foregoing statements, are grouped into two categories: (1) those that should be implemented immediately and (2) those that should be initiated immediately, but will require further time for study results to be known and conclusions to be drawn.

IMMEDIATE IMPLEMENTATION

- All discrete transistors in metal-can enclosures (except for power transistors with silicone conformal coatings), all microcircuits in metal enclosures with thick bottoms, and all hybrids in metal

*Parylene is a proprietary material of Union Carbide. Although other materials may be satisfactory for this purpose, they have not been developed to the extent that Parylene has.

**Supporting Research and Technology/Advanced Research and Technology.

enclosures should be PIND tested, including mechanical shocking during vibration. (A determination of the effectiveness and proper technique of shocking prior to vibration is needed.)

- Semiconductors and microelectronic devices packaged in ceramic-body flatpacks with ceramic or thin metal bottoms should be PIND tested, but to prevent damage, mechanical shocking should not be employed during vibration at this time. It is recognized that the effectiveness of this test is reduced by a factor up to 10 by not including mechanical shock during vibration.

- If a hybrid manufacturer either has Parylene equipment or has access to it and has the technical expertise to implement the process, that manufacturer should apply Parylene to the interior of hybrid devices in preference to PIND testing.

- Procurement documents should specify that all semiconductors and microcircuits, whether packaged as discrete units or incorporated into hybrids, be coated with either silicon dioxide (glassification) or silicon nitride.

- Power transistors, which often are not glassivated or nitrided for technical reasons, should be procured with a thin silicone conformal coating (such as Dow Corning DC-647 or DC-648 or equivalent) applied to the die, wire, and header surfaces.

- It is impossible to make a single recommendation that applies to all types of electrical and electronic devices. Appendix A gives a detailed breakdown by part-type category (transistor, relay, microcircuit, hybrid, etc.) and generic type (power transistor, small signal transistor, etc.) of the proper screen or means of protection appropriate to each category of device.

LONG RANGE IMPLEMENTATION

- A study task should be initiated for resolving doubts and for refining the test techniques for shocking fragile packages noted in the second recommendation. This task will enable more effective implementation by increasing the sensitivity of the PIND test on critical types of packages.

- NASA should support the work on the PIND test now under way at the National Bureau of Standards (NBS) (sponsored by SAMSO through

September 1976 only) by furnishing additional funding. This work is needed to develop the information on which adequate specifications can be developed for the PIND test equipment and for a standardized test procedure.

- NASA should take the lead in applying Parylene coatings to hybrid circuits as a certain means of eliminating particle contamination. To do this will require: (1) a study to determine solutions to implementation problems, (2) a study to define the scope of and estimate the costs involved for different device types and different vendors, and (3) a study to ensure that no compatibility or long-term aging problems will occur. As part of the latter study, a comparison of Parylene C with other Parylenes, such as Parylene D, is necessary for determining which type or combination of types is best for NASA applications.

- NASA should develop procedures and techniques for handling and using currently manufactured molded plastic semiconductors and microcircuits in NASA space, launch-vehicle, and ground applications. The committee believes that a cost savings of as much as 50 to 80 percent can be realized by using these devices. The committee also recommends that a study be undertaken to investigate the practical aspects of obtaining plastic molded devices that have been Parylene-coated before molding.

TECHNICAL INFORMATION

This section contains information used as the basis of the findings, conclusions and recommendations given in the preceding sections. The subject matter is discussed in some depth and supporting data for the Committee's conclusions and recommendations are included.

Traditionally, conductive particle contamination has been a problem only in devices that have cavities. The different techniques for coping with the problem may be grouped into three basic categories:

- Eliminating particles
- Testing for the presence of particles
- Using insulating coatings to immobilize particles

The first approach includes pre-cap visual inspection, source surveillance, process control, and the use of noncavity molded plastic devices. The principal techniques used in the second approach are X-ray, vibration tests, and acoustic testing. The third category includes conformal coatings such as Parylene, silicones, and other insulating materials. Glassivation (silicon-dioxide coating), silicon-nitride coating, and similar techniques are applicable to semiconductor devices only, and will be considered here as a special form of coating in the last category.

ELIMINATION OF PARTICLES

Pre-cap Visual Inspection

All individuals interviewed agreed that although pre-cap visual inspection has some advantages, it cannot be relied upon to totally eliminate particle contamination. Some semiconductors are designed in such a way that very small conductive particles (as small as 0.3 mils) can cause failures. Nonconductive particles of this size can cause failure in switches and relays by becoming lodged between contacts and armatures. In some cases, particles of various compositions as long as 50 mils have been found in devices that had been visually inspected before encapsulation.

The pre-cap visual inspection test specified in MIL-STD-883, Method 2010.2, is comprehensive and detailed. To perform this test properly, laminar-flow hoods, high- and low-powered metallographic microscopes, and talented, skilled technicians are required. For many complex devices, an inordinate amount of time is required for inspecting some of the larger device packages, for example, 3-inch-square hybrid microcircuits. These packages may contain between 100 and 200 semiconductor dice, a "mother-daughter" substrate mounting (in which smaller substrates are mounted on larger ones), multilayered substrates, and as many as 2000 wire bonds on each device. To rigorously comply with all minute detail inspections required for these devices is not practicable, not only because of the amount of time required for conscientiously performing the inspections, but also because of problems associated with inspection requirements and characteristics of inspection equipment. For example, internal inspection of the package must often be performed at magnifications of 100X to 200X. At these powers, the depth-of-field limitation of the examining microscope makes it impossible to focus on both the surface of the die and the floor of the package simultaneously. Focusing on the floor of the package is particularly difficult at this magnification because the wall of the package is usually relatively high, and, for the microscope to focus on the package floor, its objective lens must be close to the package wall and/or the wire interconnect leads. The act of focusing the microscope may cause the lens to touch the package or the leads, thereby damaging the part.

In other ways, visual inspection can be a meaningless term. The configuration of a relay often prevents proper inspection because of the presence of numerous crevices in which particles can lodge and remain hidden from view. In addition, particles may be introduced into transistors and microcircuits after the pre-cap visual inspection because of the characteristics of a lid-sealing process, or because the devices were not properly protected, or because the protection devices were contaminated. For example, the practice of stacking trays and the use of contaminated lids or covers have been identified as sources of contamination that introduced particles into devices after pre-cap visual inspection. Particles from these sources have caused many failures. In many cases, the particles either contained or were made of materials not used in the device (e.g., stainless steel and copper).

Processing anomalies that occur during lid sealing or final closure are common sources of particle contamination. Solder and solder preforms are a principal source of conductive particle contamination. Contamination from these sources has caused many failures in integrated circuits, hybrids, and relays. Weld splatter in power transistors and power diodes (lid sealing and tubulation sealing) is another common source of particle contamination. These types of contamination have caused system failures in programs other than those of NASA.

Particles have been found after final assembly or during testing even in devices that were ostensibly free of contamination. Particles arising from silicon, epoxy and eutectic die-attach materials, conductor material, glass, wire, and lid-plating and sealing materials have been either dislodged from a crevice or broken free from a loose attachment during temperature cycling, mechanical shock, acceleration, lead bending, handling and insertion, and in particular, during vibration testing.

Process Controls

Some of the individuals interviewed believe that particle contamination could be reduced by implementing process controls at the vendor's plant. An extreme example of such a control is the S-line at Texas Instruments Company (TI), which produces a limited selection of Series 54 integrated circuits under a SAMSO contract. Such a production line, which is separately situated, controlled, and funded, is called a "captive line." Captive lines offer the advantage that the customer can impose requirements on the manufacturer that relate to all phases of manufacturing, testing, and inspection.

Most procurements for government-related projects do not require a product volume large enough to justify the establishment of a captive line. Normally the variety of devices required for any particular project is too diverse for this approach to be universally applied. Therefore, it is limited to a device family or two comprising the largest percentage of components used in the system. Standardization is a desirable goal, and a captive line is one means of achieving that goal. However, inherent in the captive line concept is the tendency to restrict designers from using state-of-the-art parts by requiring them to limit their use of parts to device types produced on these lines. Because this restriction can greatly penalize designs and system capabilities, designers resist and resent it. Most government projects are funded uniquely for specific time periods. Because of this fragmented funding policy, the captive-line approach cannot usually be sustained for long periods.

Some firms and government agencies use fewer controls because they often cannot, or will not, assume the expense of maintaining a captive line. Often, the number of piece parts intended to be procured makes the captive-line approach an economic absurdity. At the opposite extreme are firms that rely entirely on the manufacturers to police their own manufacturing lines. Other firms, between the two extremes, rely on military-type specifications which have been prepared either individually by each firm or by the Department of Defense (DOD), and which impose a universally accepted set of standard requirements that has evolved over the years. Most NASA centers have chosen the latter approach. In fact, by policy, NASA is committed to support the military specification and standardization system for several types of electronic parts and is an equal partner with the three services in coordinating military specifications for those parts. These specifications have served as the bases for volume purchases, such as the GSFC complementary-metal-oxide-semiconductor (CMOS) integrated circuits Common Buy, and will be the bases for purchases made under the proposed NASA-wide Consolidated Procurement Program. Such volume purchases facilitate user-monitoring of the manufacturer, and provide increased assurance of product quality.

A few organizations, which have established a large usage rate for specific device types, maintain their own source surveillance programs. Even with this approach, the depth and detail to which it is applied varies according to the policies and desires of the company or government agency. Very few of these firms or agencies supply Goddard or other NASA centers with systems that are made with devices manufactured under these controls.

Most manufacturers object to having survey teams and source inspectors in their plants, particularly when the dollar volume is low, because production flow is often disrupted by uniquely imposed customer requirements.

It is noteworthy that, regardless of which process control philosophy was applied, particle contamination has caused failures in launch vehicles and spacecraft during assembly and in flight.

Molded Plastic Devices

Almost 90 percent of the semiconductors produced today are molded plastic devices intended for the commercial market. As the name implies, they are conventionally wire-bonded (usually gold compression bonds) chips that are completely encased in plastic by an injection molding process.

These semiconductors possess many attributes that make them attractive for Hi-Rel applications. Having no cavities, they are not susceptible to latent failure because of loose particles. Because they are completely encapsulated, only the most severe external mechanical stresses affect them. Because they are mass-produced by automatic machines, they are inexpensive. Many of the screening tests performed on hermetically sealed devices, such as hermeticity testing, mechanical shock, acceleration, and PIND testing, are not applicable to molded plastic devices. The reduction in the number of screening tests that must be performed is of obvious cost significance.

Considerable testing has been performed by the Army Electronics Command, Rome Air Development Center and Naval Ammunition Depot (Crane), on molded plastic devices to determine their inherent weaknesses. Two major concerns that have caused these devices to be universally banned for use in Hi-Rel applications are an operating temperature-range limitation and a susceptibility to the effects of humidity. Most currently manufactured molded plastic devices are designed to operate within a temperature range of 273 to 343 K, which is satisfactory for most commercial applications. On the other hand, hermetically sealed devices, which are intended primarily for the military market, are designed to operate within a temperature range of 218 to 398 K. These experiments have shown that, when many types of molded plastic devices are subjected to temperature stresses outside their (commercial) design limits, they are prone to failure. In most Hi-Rel applications, the temperature limitations are not as great a concern as their susceptibility to moisture. This testing, together with experiments performed by TI, indicate that the penetration of moisture into the devices causes degradation of device operating characteristics and corrosion of the metallization on the surface of the die that can eventually lead to a time-dependent failure mechanism.

In many NASA applications, the temperatures to which systems are subjected are benign and, in most cases, closely approximate the "commercial" range. In addition, the most severe humidity environment to which devices are exposed occurs before spacecraft integration and testing. The spacecraft is then

stored in a controlled atmosphere. The use of plastic molded devices by NASA, DOD, and other aerospace users can be rationalized if appropriate temperature limitations are observed and if precautions are taken to protect the devices from exposure to excessive humidity up to the point of spacecraft packaging. It is appropriate for NASA to determine the limitations of molded plastic devices, to compare these limitations with actual use requirements, and to determine the useful life expectancy of currently manufactured devices that are stored and used in environments reflecting actual use conditions.

Manufacturers are constantly attempting to improve plastic devices to overcome their two basic deficiencies. Probably the most significant discovery, however, has been made by the Hughes Aircraft Company in cooperation with T[illegible] under a Marshall Space Flight Center (MSFC) contract (Reference 1). Experiments conducted by Hughes Aircraft Company on Parylene-coated devices that were subsequently molded with mineral-filled Novalac epoxy indicated that, ". . . a method of protection is available that offers promise for creating a low cost plastic encapsulated alternative to the hermetically sealed devices now used in high reliability applications."

The Hughes Aircraft Company discovery that molded plastic devices coated with Parylene prior to molding are nearly equivalent to and, in some cases superior to, their hermetically sealed cavity-containing counterparts, is of tremendous significance. A technology that can produce devices that are equivalent (regarding resistance to thermal fatigue and humid environments) to hermetically sealed devices should signal a turning point in Hi-Rel philosophy. The ability of plastic devices to withstand these environments, together with their greater inherent mechanical ruggedness, should make their use very attractive.

NASA should exploit this promising development by supporting a study to identify and solve problems associated with implementing this approach.

TESTS FOR DETECTING PARTICLES

Vibration

Electrical monitoring during vibration is often used for particle detection. The testing procedure may include several combinations and variations of vibration, shock, and electrical or acoustical monitoring. However, the three basic variations now used are: (1) sinusoidal vibration with power applied to the device, referred to in this report as "monitored vibration"; (2) sinusoidal vibration with mechanical shocks applied at various intervals, while the devices being tested are under power and functionally operative, referred to in this

report as the "Autonetics test" (also known as the "Mann test" or the "monitored vibration-shock-vibration test"); and (3) the sinusoidal vibration test with acoustical detection, referred to in this report as the "PIND test" (also called the acoustic particle detection (APD) test or loose particle detection (LPD) test.

Monitored Vibration—In this test, devices are subjected to a sinusoidal vibration either at a fixed frequency or swept over a range of frequencies. Power is applied to the device during this time, and some means of detecting an electrical malfunction, usually a latching circuit, is employed. This test is a relatively lengthy and expensive method of detecting conductive particles and is often specified for power transistors and diodes. A variation of this test, the "miss" test, is often specified for use with relays. In miss testing, the relay is electrically operated at a low repetition rate while the contacts are monitored for failure to open or close appropriately.

This testing technique is not considered to be effective for either semiconductors or relays, and its continued use is of doubtful value. In both cases, if a particle is present and occupies one of many specific locations at a specific time, it will make its presence known. In fact, in rare cases, a number of very small particles, under the influence of the electric field between two interconnect paths on a semiconductor die, can become aligned and form a conductive path that bridges the gap between the paths. In semiconductors, particularly integrated circuits, hybrids, and many transistors, not all conductive paths will have potentials applied between them at all times, thus limiting the detectability available at the outset. This test suffers degradation in sensitivity because small particles become bound by electrostatic or other attraction forces and may not be free to move during the test.

Autonetics Test—This test can be considered as an extension of monitored vibration tests that, as previously noted, are subject to loss of sensitivity because electrostatic or other forces cause many particles to be captured and bound on the interior surface of a package. In the Rockwell International/Autonetics test, these forces are released and the particles are maintained in an unbound state by subjecting the device to shocks of 150 to 200 g's at frequent intervals. After they are released by a mechanical shock, particles move about within the package cavity. As in the simple monitored vibration test, even a momentary positioning of a conductive particle between two points at different potentials is sensed by a fast-response latching circuit, thus identifying the defective device. In any vibrational detection scheme, this mechanical shock is necessary for releasing particles of less than 4 to 5 mils. In the Autonetics test, the shocks are applied to the center of a circular metal plate by a solenoid hammer. The efficiency of the test procedure is increased by simultaneously

testing 60 devices mounted in individual monitoring jigs and located near the edge of the 32-inch-diameter plate. Although multiple testing increases the throughput, the relatively high cost of designing and fabricating the equipment for this quantity is a disadvantage. Also, each distinct device type to be tested requires the design of a monitoring latching circuit peculiar to that device type. The more complex the device, the more extensive and complex must be the driving and monitoring circuitry to enable it to detect a malfunction. Extensive analysis of the device to be tested, based primarily on the topographical map of exposed metal on the semiconductor die, and the designed function of the device are necessary for proper malfunction detection. Simple biasing of inputs is superficial and largely ineffectual.

The Autonetics test was designed 5 or 6 years ago and appears to be based on sound principles. The originators of this method performed an extensive analysis of the movement of a particle within a cavity and the kinetic, gravitational, and electric-field forces involved, and from this information estimated the required shake times. References on the electrostatic binding forces influenced the design of the hammer shock used for breaking them. Autonetics also made a short movie of the interior of a package under vibration that demonstrates how the smaller particles are captured and held immobile until a shock of sufficient magnitude releases them. Texas Instruments Company and IBM also made similar movies.

Shortly after this system was completed, JSC, MSFC, and Jet Propulsion Laboratory (JPL) experienced particle problems (References 2, 3, 4, and 5) on Series 54L integrated circuits intended for Apollo and the Viking Lander. Several thousands of these devices were subsequently subjected to the Autonetics test. Unfortunately, JPL concluded that test results indicate that this test is <u>not</u> effective. Correlation of data on devices identified as containing particles and the results of construction analyses on the same devices were poor. Construction analysis of "good" devices indicated that many contained particles. Retesting of a "screened" lot also indicated poor correlation in again identifying as failures those devices that had originally been identified as such.

GSFC experience with the Autonetics test is limited to a single group of Series 54L integrated circuits that were tested in 1973. Of the 815 devices tested, eight were identified as containing particles. These eight devices were opened, and loose conductive particles were found in six devices. However, because of project requirements, no "good" devices were opened for the purpose of determining the number of escapes and the effectiveness of this test. It should be noted that this percentage of failures (about 1 percent) is in line with the reject

rate reported by JPL in their testing of several thousand devices. JPL opened a number of "good" devices and determined that the escape rate was about equal to the detection rate. That is, about one-half of the packages that contained particles were actually identified as such.

Further, some believe that the mechanical stresses imposed during the Autonetics test actually generate particles, thus making the test self-defeating.

The Autonetics test is therefore judged to be an impractical means of identifying devices with particles because of: (1) high cost, (2) limitation of available test equipment (only two or three exist), (3) high cost of the basic mechanical instrumentation (about $20 thousand), (4) time and dollar costs involved in designing and instrumenting the driving and monitoring circuitry (for new devices), and (5) low confidence in its effectiveness.

PIND (Particle Impact Noise Detection) Test

As early as 1965, TI published information on acoustic particle detection test results (Reference 6). Since then, Lockheed Missile and Space Company (LMSC) and TI have developed and used PIND testing. LMSC's initial development effort in acoustic detection made it possible to identify relays that contained particles, and they have used this technique during the past 5 to 10 years to screen some types of relays for flight use.

The PIND test is a variation of the vibration test, but, because of its widespread use and unique acoustic-detection feature, it is treated separately from the other forms of vibration testing previously discussed.

The PIND test determines the presence of loose particles in a cavity device by detecting the sound energy generated when particles strike the package. The test specimen is attached to an accelerometer that is mounted on a vibrator. When mechanical excitation is applied to the specimen, the transducer detects the sound energy generated by the impact of a loose particle with the device enclosure. The sound energy extends into the ultrasonic frequency range well above the response capability of the human ear. The output from the transducer is fed to a 100- to 300-kHz filter, which removes the shaker frequency and background noises. The amplified signal is then used to provide both visual (oscilloscope) and audio monitoring of the test. Although some firms use only one of these monitors, most of them believe that detection capability is enhanced by using both monitors simultaneously.

Opinions of the value of the test differ greatly. Although operator training is not a difficult problem, users do not always understand the more subtle technical aspects of the instrumentation. For instance, noise isolation, signal-to-noise levels, optimum vibration frequency, shock techniques, calibration techniques, etc., affect the sensitivity of the test. One company, which had studied the PIND test variables, experimentally verified a prediction from a mathematical model that a maximum acoustic emission was associated with a particular vibration frequency (Reference 7). This frequency was different for different cavity geometries and volumes. Another company's investigation indicated that the frequencies generated by the impacts were a function of the composition and thickness of the package structural material and of the distance between the top and the bottom of the device.

The committee saw a wide variation in the sensitivity of the test as practiced by different companies. Part of this is attributed to the lack of research by the manufacturer of the equipment, Dunnegan-Endevco Corp. A discussion with the manufacturer revealed that they concluded that the size of the potential market for the test equipment did not justify allocation of research and development funds.

Another serious problem with the PIND test is the immobilization of the contaminating particle by a charge effect. Although the nature of the charge is not completely understood, it has been described as electrostatic charge, triboelectric effect, molecular attraction, etc. Most users of the test have seen and documented the effect of the charge on a particle. The effect is to get no signal at all, or only a momentary one, indicating the presence of the particle, before it disappears. Tapping the device with a shaped wire or another device (such as a dental amalgam packer) is normally used to try to dislodge the particle and confirm its presence. This shock aspect of the test is another debatable point on which opinions conflict. Tapping with the wire can easily produce a shock of 200 g's, while LMSC's investigation of the effect of the shock showed that particles were generated by a shock of only 40 g's. They also found that some particles, immobilized by static charge, required as much as 3000 g's (centrifuge) to dislodge them. This is an over-simplification of a rather extensive investigation. However, in reviewing this work and results from other companies, the committee believes that the devices used in the investigation were not representative of good processing and that the excessive debris detected would not have been found on devices made under good manufacturing practices. This is an area that needs additional investigation. Fortunately, an independent investigation is under way. SAMSO has provided funds for the National Bureau of Standards (NBS) to investigate various aspects of the PIND test. NBS personnel are approaching the problems in a systematic way

and are using information from various users, including some that the committee visited. This study should provide some much-needed information, such as improvement in standardization, calibration, effect of shock levels, and understanding and elimination of the static-charge effect. NBS issued a report on this work in August 1976 (Reference 8).

Although the discussion thus far has emphasized limitations of the PIND test, some uses of the test have been very successful. When first instituting the PIND test, the Singer-Kearfott Company was getting 50 to 60 percent rejects. Changes in its processing, indicated by particle contamination analyses, reduced the reject level to 5 percent. They found that a reject device could be recovered by having a 30-mil hole in the lid of the device covered by sticky tape and vibrating it. The sticky tape caught the contaminating particles, removing them from the device.

Teledyne Microelectronics instituted PIND testing and recovered particulates from the rejects by the sticky-tape technique. Analysis of the particles using a scanning electron microscope indicated that 20 percent of particles were conductive. Sources of contamination identified by these results were: (1) acoustic ceiling tiles, (2) plastic containers, (3) aluminum panels, and (4) wash cases and boxes. Feedback of this information to the production line resulted in corrective actions and a reduction in the reject rate from 16 percent to less than 3 percent. For example, in May of this year, only 1.9 percent of 5000 hybrids that were PIND tested, were rejected. In half of the rejects the particles were conductive.

Sperry (Phoenix) had 15 to 20 percent rejects when they started PIND testing. The reject rate is now 2 to 4 percent, and they estimate that most of the particles are nonconductive. They apply a 1000-g shock three times during their PIND test to activate any immobilized particles, and are not concerned that this shock level may generate particles. On the basis of some limited comparisons, they believe the PIND test is superior to the monitored vibration test.

Although some companies find that 20 percent of the particles present are conductive, TI reports that this figure is closer to 80 percent. This variation is undoubtedly attributable to a combination of factors, such as workmanship, manufacturing processes, ambient environment, etc.

TI was outstanding from the standpoint of experience, knowledge, and investigative results. This company has funded work on the PIND test because the company endorses the development of test methods. They have made seeded

specimens using TO-5 and TO-18 package devices. The contaminants used for seeding included different particle sizes of lead, aluminum, gold, and silicon. Based on their work, the following information is considered valid:

- One-mil particles are not consistently detectable.
- Two-mil particles can be consistently detected, but this may vary between companies.
- Hangup of particles is greatest for particle sizes less than 2 mils.
- Four-mil gold particles do not hang up, and are recommended for a standard to calibrate the test equipment.
- Finger tap is recommended for applying shock for dislodging particles.
- Devices that show either visual or audio signal should be rejected.
- A small scope is recommended as more effective and easier for the operator to use than a large one.

Dunegan-Endevco produces nearly all of the equipment being used for this test. A complete system for conducting the PIND test costs about $4000. Some individual costs are: shaker, $500; oscilloscope, $925; special switch, $125; amplifiers, controls, etc., $2400. About 500 complete units have been sold by Dunegan-Endevco.

One criticism of the PIND test is that because it cannot differentiate between conductive and nonconductive particles, parts will be rejected that contain the harmless nonconductive ones, thus reducing the yield of useable devices. This is a condition for which there is no known solution at the present time and is a price the user will have to pay if he relies upon this test as a screen for conductive particles.

In summary, the PIND test is useful in reducing the number of devices with contaminating conductive particles. As the size of the particle contaminant increases, the effectiveness of the test increases. This test has also been effective in identifying sources of contamination, and in identifying processes that were not properly controlled. Although it cannot eliminate the conductive-particle problem, it is recommended as an economical way to reduce the incidence of catastrophic failures in launch vehicles and spacecraft electronic devices.

X-Ray Testing

X-ray is one of the more easily performed tests and is inexpensive. However, some of the conductive particles that have been found in packages are invisible to X-rays because of their composition, thickness, and size. Because of the resolution limit of the X-ray, small particles of less than 1 mil are not detectable. Also, small particles that rest on a die that is eutectically attached to the package with silicon-gold die attach material cannot be detected because they are masked by this material. This problem often results in different, subjective interpretations of X-ray radiographs. In spite of the limitations of this test, it can be effective in detecting the presence of larger, more massive particles, as well as some manufacturing process deficiencies, and the use of this procedure is therefore recommended.

X-Ray/Vibration/X-Ray

In this test method, the device is first X-rayed and a radiograph is made. After subjecting the device to a vibration stress to induce movement, it is again X-rayed. Visual comparison of the "before" and "after" pictures enhances particle detection capability, since specific questions of particle identification can be resolved by the movement of the particles.

This test method is not often used. Among the persons interviewed during this investigation, none indicated that they were using it, and none recommended that it be used for detecting the presence of loose particles.

INSULATING COATINGS

Glassivation and Nitriding

During semiconductor wafer fabrication, several types of materials can be applied for protecting the surfaces of the dice from chemical and mechanical contaminants. These are distinguished from conformal coating materials that are applied at the device level after assembly.

Silicon dioxide (SiO_2) can be deposited from the vapor phase by various means, such as by reacting silane (silicon hydride) with carbon dioxide. The deposit is an amorphous glass whose density depends on the deposition parameters of rate of flow, temperature, and concentration of reacting gases present. The process is known as "glassivation," "Silox" deposition, or "SiO_2" deposition.

Silicon nitride layers of indefinite composition (SiN_X) can be similarly applied from the vapor phase by reacting silane and ammonia (NH_3) or other nitrogen-bearing compounds.

Glassy layers can also be applied by sedimentation techniques that use finely divided glass powders in suspension in a liquid, followed by high temperature firing, or by the simple oxidation of silicon in the presence of oxygen or water vapor.

All these coatings have the advantage that they cover almost the entire surface of a die and are electrically and chemically inert. To make contact with the die, however, the pads to which bonding wires will be attached are exposed by etching. The top surface edges of dice are also exposed at the wafer stage so that the wafer can be scribed and broken into individual dice. Since all these elements—the bonding pads, the wires, and the dice edges—are unprotected, they are subject to shorting by loose conductive particles.

SiO_2 coatings were originally designed to protect the soft aluminum interconnect system on the surface of the die from mechanical damage, such as scratching during handling, and from chemical contamination. Silicon nitride coatings were originally designed to act as a chemical barrier. Both coatings offer mechanical protection from loose particles and are often specified for this purpose as well. Neither coating provides complete protection from potential damage by particles because they do not cover the entire surface of the die. In semiconductor history, standard practice has been to apply glassivation, and sometimes nitride coatings, to all newly designed devices. They are therefore normally present on the die even if not specifically requested by the user. However, some older devices, such as the diode transistor logic (DTL) and emitter coupled logic (ECL) families, and on some large devices, such as power transistors and diodes, the original photolithographic masks were not cut with the intent of using these coatings and, for economic reasons, have never been redesigned to accommodate them. Therefore, some of the older devices are not presently supplied with glassivation or nitride coatings.

In a particular device on which these coatings have been applied, the smallest particles that can cause shorting may be equal to the distance between bonding pads. This distance is often about 4 mils. Without coatings, the critical distance may be reduced to as little as 0.5 mils—the distance between the metalization stripes on the surface of the die. Because the smallest particle that can cause a problem is reduced from approximately 4 mils to 0.5 mil, the use of these coatings is highly recommended.

These coatings are normally and properly referred to as "passivation" coatings, but they are sometimes erroneously called "conformal coatings." Although they both passivate and conformally coat, the latter term is more properly applied to organic materials or inorganic elastomeric materials that are applied by brushing, dipping, spraying, or similar techniques at a final state of assembly of the device.

Conformal Coatings

Semiconductor manufacturers have often used conformal coating materials for passivation inside sealed devices. In the early stages of development, problems arising from their use initiated an unfavorable reaction to them. This reaction is manifest today in almost all Hi-Rel specifications, particularly those controlled by the military, which strictly forbid the use of conformal coatings. Nevertheless, conformal coatings are now commonly used in devices intended for the commercial market. Conformal coatings may be vapor deposited, brushed on, dipped, sprayed, or applied with a hypodermic syringe.

Parylene—Parylene coatings are achieved by vaporizing a paraxylylene dimer in an evacuated, heated chamber and by then allowing it to condense on parts contained in a cooler part of the chamber.

The now disbanded NASA Electronics Research Center (ERC) initiated investigations on the use of Parylene on electronic parts and first supported its use as a conformal coating on printed circuit boards, a technique that is in practical use today. ERC also proposed, and did initial studies on its use as a conformal coating in semiconductor devices. GSFC (Reference 9) and MSFC (Reference 10) supported further investigations in this application by the Hughes Aircraft Company; concurrently, Northrup, Draper Labs, IBM, and others performed privately funded studies. Later, GSFC and Lewis Research Center (LeRC) jointly funded a study at Teledyne in the application of Parylene to their hybrids. LeRC is presently funding the qualification and use of this material on the Centaur guidance computer.

Parylene is a vapor-deposited material that will coat every surface which has been exposed to it. It has an inordinate ability to penetrate into minute cracks and crevices. The coating is normally applied to semiconductor devices in thicknesses of 0.1 to 0.4 mil. When Parylene is applied internally to semiconductor devices, it completely and permanently immobilizes all loose particles that may be present and adds additional strength to die and wire bonds. It provides chemical and moisture protection to surfaces to which it has been applied.

In the work performed to date, no substantial degradational effects have been attributed to Parylene. When it is used in contact with all types of materials used in semiconductor devices, Parylene appears to be completely inert.

The upper temperature limit is somewhere between 100° and 150°C. Above this temperature the material may craze or crack. At 100°C in air (i.e., with oxygen present), tests at Teledyne show that this may occur in 200 hours. At 150° C in nitrogen, thin coatings remain intact after 2000 hours. Although all authorities agree that a temperature limitation exists, they do not all agree on what this limit is, or on the thickness/time/temperature/ambient-environment relationship.

Although from a technical standpoint, Parylene appears to be an excellent solution to the conductive particle problem, it is not practical to recommend that it be applied to current production for most electronic device types at this time. The reasons for this are based either directly or indirectly on various aspects of implementation.

Because many manufacturers of semiconductor products and hybrids are not familiar with Parylene, they are reluctant to incorporate this process into their manufacturing lines without extensive testing on <u>their</u> products. They are concerned from both a technical standpoint and a cost standpoint, and no conclusions or cost estimates are now available. Their lack of enthusiasm is compounded by the fact that most vendors sincerely do not believe they have a particle problem. They therefore see no need to provide safeguards against an incidence that they consider "acceptably" low, even though the committee considers it to be significant and unacceptable.

One of the biggest hurdles is associated with the equipment and technology itself. Several individuals who are involved in specifying Parylene and are considering its use still consider it to be in the research and development stage, as applied to electronic devices. Only Union Carbide now manufactures the equipment, and the two models it offers have limited throughputs. The equipment capacity is low, the operation time is long, and daily cleaning and maintenance of the equipment is necessary. Although Union Carbide supplies the equipment, they do not support sales by offering consultant services in applying Parylene to semiconductors. In fact, virtually the sole authorities for application are Robert Rohal and Thomas Riley of LeRC and F. Oberin of the Hughes Aircraft Company. In connection with the guidance computer for the Centaur launch vehicle, Rohal and Riley spent about 6 man-months at Teledyne setting up the system to coat hybrids. Although less time would probably be required for a new installation elsewhere, some adjustment to the procedure must be evaluated to compensate for different package styles and products used by other projects.

At this time, costs are relatively high, as can be expected for a new process. At Teledyne, LeRC is paying from $10 to $20 per hybrid, based on a production of 5,000 to 10,000 pieces. These costs are in addition to the set-up costs of about $230,000, which include the equipment, the license from Union Carbide, installation costs, evaluation test costs on the units to be coated, masking fixtures, and formal qualification test costs. This figure also includes costs incurred in learning how to operate the equipment properly (such as the maximum deposition rate) and learning how to design masking fixtures. Since much of this learning process would not have to be repeated, and since evaluation and qualification tests could be significantly reduced, the estimated set-up costs for new installations is estimated at about $80,000. Another factor in the cost is the parts loss that may occur in processing devices with a Parylene coating. At Teledyne, this cost was initially about 20 percent, and although this cost may not be typical of other vendors, other production procedures, and other packages, it indicates that proper handling techniques must be learned. Finally, from a device standpoint, more data are necessary for increasing confidence in the inertness of Parylene. Extended life tests and accurate temperature limitation determinations must be made on a variety of part types not now characterized, such as sensitive, low-current-level CMOS integrated circuits of much higher complexity than those already tested.

Although implementation problems will prevent widespread use of Parylene in the near future, efforts to overcome these problems are well justified. If the Shuttle program decides to proceed with Parylene coating, other users may be able to take advantage of the equipment that Shuttle is considering installing at five or six sites throughout the country. Increased requirements for Parylene in procurement specifications and increased acceptance by other vendors should improve the availability of this process with time.

Other Conformal Coatings—Depending on the design of the device and the characteristics of the coating materials, there are some unique instances where coatings other than Parylene have been safely used in semiconductor devices.

Commercial manufacturers have been using silicone conformal coatings in power transistors for many years. For commercial and military markets, the devices are often physically identical, except for the absence of coatings in the latter devices. Military specifications prohibit the use of such coatings because the types of silicones and "varnishes" applied during early testing of conformal coatings had undesirable mechanical and electrical properties and were subject to cracking and flaking at the upper temperature limit of the military test range.

Silicone coatings usually adhere poorly to surfaces normally found in semiconductor devices. The coatings often move or lift during mechanical stressing,

such as constant acceleration, and impart mechanical stresses to the internal bonding wires. GSFC has found that these stresses may cause bonds to lift and fall back into place at the completion of the mechanical test, and, on subsequent temperature cycling testing, the damaged bonds may exhibit intermittencies that might be interpreted as having been induced by the temperature cycling test. Small signal transistors, integrated circuits, and hybrids contain small wires that have low bond strengths and are susceptible to such stresses. Because heavier wires are often used in power devices, the use of silicone coatings can be specified with the assurance that mechanical stressing will not damage the devices. Some projects now ignore military specification restrictions on the use of silicone conformal coatings in power transistors in order to avoid problems with weld splatter. This committee endorses this philosophy.

Conformal coatings may be used in other applications if use and testing limitations are observed. For example, these coatings can probably be used on more fragile devices, but, if this is done, testing and use stresses must be confined to levels that are not detrimental.

With silicone conformal coatings, the use of silane adhesion promoters may permit moderate mechanical stress testing and a more extended temperature range. The Western Electric Company routinely uses silicone conformal coatings on beam-leaded hybrid devices with adhesion augmented by a silane primer. In the latter case, the purpose of using the adhesion promoter is to provide better resistance to the effects of humidity. The improved adhesion prevents moisture from penetrating through the interface between the coating and the surfaces to which it has been applied.

ACKNOWLEDGMENTS

The Committee gratefully acknowledges the cooperation and contributions of those individuals interviewed personally or by telephone and listed below. Without generous committments of their reports, time, and insight, and of their candid comments, this survey report could not have been generated.

Aerospace Corporation - Joseph Howell, Mary Neudorffer, Donald Fresh

Boeing - Don Robinson

Delco - Wally Sterner

Dunegan-Endevco - Paul Knaus, Adrian Pollock

General Dynamics Corporation - John Phillips, Ken Strowig, Robert Eilers

Honeywell (St. Petersburg) - Dick Backman

Hughes Aircraft Company - William Hurd, Ken Tendick, R. A. Brennan, R. McGowen

IBM (Owego) - Tom Martin, Malcolm Young, Fred Curtis, Michael Bloomfield-Brown

Jet Propulsion Laboratory - Larry Wright

Johnson Space Center - Sevario Gaudiano, Scott Simpkinson, Joe Levine, Tom Edwards, Billy Stewart

Langley Research Center - Hugh Milteer

Lewis Research Center - Robert Rohal, Thomas Riley

Lockheed Missiles and Space Company - Rod Pfeil, Robert Blair, Daniel W. Sisley, Chuck E. Leake, Roger Kisk, Warren Gile

Marshall Space Flight Center - Sal Caruso, Leon Hamiter, John Berkebile, Michael Nowakowski

Martin Marietta Corporation (Denver) - R. S. Cooper, P. Carter, Ron Economakis, Virgil Young

McDonnell Douglas Astronautics/West - Douglas Hastings, John Slocum

McDonnell Douglas Astronautics/East - Morton Stitch

Motorola - Glen Shaw

National Bureau of Standards - John S. Hilten, Carol Vizzetti, Paul Lederer

National Semiconductor Corporation - Dick Kramer

RCA/Solid State Division - Ron Jarl

Rockwell International Autonetics Division - Jack Mann

Rockwell International Space Systems Division - Charles Murphy, Peter Zantos, Ken Harris, John Bean, Moe Alverez

Rome Air Development Center - Joseph Brauer

Singer Kearfott - Wilson Reilly, George Abel

Sperry (Phoenix) - Jim Lawson, Tom Brennan, Joe Ivanesco, Dick Roddy, Jim Hoheimes, Alan L. McDonald, Walt Robinson

Teledyne Microelectronics - Sid Eichel, Ralph Redemski, Vidyadhar Kale

Texas Instruments Company - Ralph McCullough, Willie Reynolds, Don Denton, Don Wallser, Peter Schenkle, Wayne Howse

Thompson-Ramo Wooldridge, Inc. - R. Blessing

REFERENCES

1. Development for Application of Parylene Coatings. Final Report NASA Contract NAS8-29940 (supplement 3). December 1975.

2. Government Industry Data Exchange Program. Alert MSC-71-04, Corona, California. July 14, 1971.

3. Government Industry Data Exchange Program. Alert MSFC-71-21. Corona, California. November 16, 1971.

4. Government Industry Data Exchange Program. Alert E4-A-73-01. Corona, California. March 8, 1973.

5. Government Industry Data Exchange Program. Alert E4-A-73-01A. Corona, California. April 11, 1973.

6. L. D. Clark, J. C. Burrus, and R. D. Clark. "Evaluation of Selected Methods for Detecting Contaminations Within Semiconductors." Proceedings of the Institute of Environmental Sciences. 1965.

7. J. L. Angleton and S. L. Webster. "Techniques for Standardization of Particle Noise in Electronic Packages," 12th Annual Proceedings of Reliability Physics Symposium. 1974.

8. P. S. Lederer, J. S. Hilton, and C. F. Vezzetti. "Loose Particle Detection in Microcircuits." National Bureau of Standards Interim Report #182. August 31, 1976.

9. Hughes Aircraft Co. "Study of Methods for Protecting Hybrid Microcircuits from Contaminating Particles." NASA/GSFC Report No. Pacer 10-005. June 1971.

10. "Development for Application of Parylene Coatings." Final Report NASA Contract NAS8-29940. June, 1974.

APPENDIX A

SPECIFIC PARTICLE CONTAMINATION RECOMMENDATIONS BY PART TYPE

APPENDIX A

SPECIFIC PARTICLE CONTAMINATION RECOMMENDATIONS BY PART TYPE

It is impossible to make a single recommendation that applies to all types of electrical and electronic part types. The specific recommendation appropriate for each part type depends on a variety of factors, such as whether it is electronic or electromechanical; the processes used in manufacturing the device; the ability and inclination of manufacturers to modify manufacturing and test procedures; the availability of equipment, training, or consultant expertise necessary for implementing a process or test; the construction of a device and its package; costs of implementation; and relative effectiveness of the test. The following recommendations consider all these factors as applied to cavity devices.

Part Type		Recommendation*
Capacitors (tantalum only)		PIND test with shock
Crystals		(No particle test recommended)
Diodes		PIND test with shock
Hybrids		Parylene coating preferred PIND test with shock acceptable
Microcircuits	Thick bottoms	PIND test with shock
	Ceramic or thin metal bottoms	PIND test with no shock**
Microswitches		PIND test with shock
Relays		PIND test with shock
Transistors	Power types (flange) or stud-mount packages (i.e., TO-66 packages and larger)	Conformal coating preferred PIND test with shock acceptable
	All other types	PIND test with shock

*All references to shock mean that a shock should be applied directly to the device while it is being vibrated. The shock tool is a shaped piece of No. 8, 10, or 12 solid copper wire.

**Normal shocking of this part may damage it. A modified shock technique should be developed to increase the sensitivity of this test.

APPENDIX B

SURVEY RESULTS

	AEROSPACE	DELCO	GEN. DYNAMICS	HUGHES	HONEYWELL	IBM	LOCKHEED	MARTIN-MARIETTA	MDAC/EAST	MDAC/WEST	MOTOROLA	RADC	RCA	RI/AUTONETICS	RI/SPACE SYS.	SINGER-KEARFOTT	SPERRY	TELEDYNE	TI	TRW	JPL	JSC	LARC	LERC	MSFC
1. IS PARTICLE CONTAMINATION A PROBLEM IN:																									
A. I.C.'S, TRANSISTORS, DIODES OR HYBRIDS;	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	N	–	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
B. POWER TRANSISTORS;	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y
C. CAPACITORS, CRYSTALS, SWITCHES AND RELAYS?	–	Y	–	Y	–	N	Y	Y	–	Y	Y	–	–	Y	Y	Y	Y	Y	Y	Y	–	–	–	–	–
2. HAVE YOU HAD FAILURES DUE TO PARTICLES:																									
A. PIECE PART INSPECTION;	Y	Y	–	Y	Y	Y	Y	Y	–	Y	Y	–	–	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y
B. BOARD LEVEL;	Y	P	–	Y	–	Y	Y	Y	–	Y	Y	–	–	Y	Y	P	Y	Y	–	Y	–	Y	–	Y	Y
C. SUBSYSTEM TESTING;	Y	P	–	Y	–	Y	Y	Y	–	Y	Y	–	–	Y	Y	P	Y	Y	–	Y	–	Y	–	Y	Y
D. SYSTEM TESTING;	Y	Y	–	Y	–	Y	Y	Y	–	Y	Y	–	–	Y	Y	Y	Y	Y	–	Y	–	Y	–	Y	Y
E. IN THE FIELD?	Y	Y	–	Y	–	Y	Y	Y	–	Y	**	–	–	Y	–	**	Y	Y	–	N	–	Y	–	N	N
3. WHICH IS THE MOST EFFECTIVE METHOD IN DETECTING PARTICLES:																									
A. PIND?	√	–	√	√	√	√	√	–	–	√	√	–	√	√	√	√	√	–	√	√	–	√	–	√	√
B. MONITORED VIBRATION?	–	–	–	–	–	–	–	–	–	–	–	–	–	√	√	–	√	√	√	–	–	–	√	–	–
C. X-RAY?	–	–	√	–	–	–	–	–	–	–	–	√	–	–	–	–	–	–	–	√	–	–	–	–	–
D. QUALITY CONTROL AT SOURCE?	–	–	–	–	–	–	√	–	√	–	–	√	–	–	–	–	–	–	–	√	–	–	–	–	–
E. PRE-CAP VISUAL?	–	–	–	–	–	–	√	–	√	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

Y – YES
N – NO
P – PROBABLY

– NO ANSWER; ANSWER NOT CLEAR; QUESTION NOT ASKED
** DIDN'T KNOW

	AEROSPACE	DELCO	GEN. DYNAMICS	HUGHES	HONEYWELL	IBM	LOCKHEED	MARTIN-MARIETTA	MDAC/EAST	MDAC/WEST	MOTOROLA	NASA	RCA	RI/AUTONETICS	RI/SPACE SYS.	SINGER-KEARFOTT	SPERRY	TELEDYNE	TI	TRW	JPL	JSC	LARC	LERC	MSFC
4. IS PRE-CAP VISUAL INSPECTION 100% EFFECTIVE IN ELIMINATING PARTICLES?	N	N	–	N	N	N	N	N	N	N	Y	N	–	N	N	N	N	N	Y	N	N	N	–	N	N
5. CAN IT BE MADE 100% EFFECTIVE?	P	N	–	N	N	N	N	N	–	N	Y	N	–	N	N	N	N	N	–	N	–	–	–	N	N
6. SHOULD PRE-CAP VISUAL INSPECTION TO DETECT PARTICLES BE CONTINUED?	–	–	–	Y	–	–	Y	–	–	–	–	–	–	Y	Y	Y	Y	Y	Y	–	Y	–	–	Y	Y
7. IS MONITORED VIBRATION AN EFFECTIVE TEST?	Y	–	–	N	–	Y	–	–	–	–	–	N	–	Y	Y	–	–	Y	Y	–	N	–	–	–	N
8. PIND TEST:																									
A. SMALLEST SIZE PARTICLE (IN MILS)																									
1) DETECTABLE AT ALL.	–	–	–	0.5	**	1.5	0.5	–	–	0.5	1	1	–	– (AUTONETICS TEST)	1	–	0.5	0.1	1	–	–	–	–	1	–
2) DETECTABLE 100% OF TIME.	–	–	–	5	**	–	5	1 GM	–	10	–	3	5	0.5	3	1	0.5	–	2	1	–	–	–	10	1
B. TRAINING																									
1) SPECIAL REQUIRED	–	Y	–	Y	Y	Y	Y	Y	–	Y	Y	–	–	Y	Y	Y	Y	Y	Y	Y	–	–	–	–	–
2) TIME REQUIRED (WEEKS)	–	–	–	4-8	1 HR	–	12	–	–	3	–	–	–	◁	1	1	... 1	2	1	1	–	–	–	–	–
C. COST PER DEVICE																									
1) ACTUAL COST	–	–	–	–	–	–	–	–	–	–	–	–	–	–	$10	–	$10	–	$10	–	–	–	–	–	–
2) CUSTOMER CHARGE	–	–	–	–	–	–	–	–	–	–	–	–	–	$60 TO $6	$5	$1	–	–	–	–	–	$20	–	–	$100
D. TIME TO PERFORM TEST.	–	–	–	10-30 SEC	1 MIN	–	–	–	–	–	–	–	–	60/ 2 HR	–	15 MIN	2 MIN	30 SEC	30 SEC	–	–	–	–	–	–
E. NUMBER DEVICES TESTED.	–	–	–	–	–	–	200K TO 300K	–	–	–	–	–	–	–	10K	–	2K MON	50K	3 TO 4M	–	–	–	–	5K	–

Y – YES
N – NO
P – PROBABLY

– NO ANSWER; ANSWER NOT CLEAR, QUESTION NOT ASKED

	AEROSPACE	DELCO	GEN. DYNAMICS	HUGHES	HONEYWELL	IBM	LOCKHEED	MARTIN-MARIETTA	MDAC/EAST	MDAC/WEST	MOTOROLA	RADC	RCA	RI/AUTONETICS	RUSPACE SYS.	SINGER-KEARFOTT	SPERRY	TELEDYNE	TI	TRW	JPL	JSC	LARC	LERC	MSFC
9. DO YOU REQUIRE GLASSIVATION?	–	Y	–	Y	Y	Y	Y	Y	–	Y	N	–	–	Y	Y	N	Y	Y	Y	Y	Y	Y	–	Y	Y
10. ARE YOU INVESTIGATING A CONFORMAL COAT?	–	N	–	Y	Y	N	Y	N	N	Y	N	–	–	Y	Y	N	N	Y	N	N	–	Y	–	Y	Y
11. DO YOU NORMALLY REQUIRE A CONFORMAL COAT?	–	N	–	N	–	N	N	Y	N	N	N	–	Y	N	N	N	N	Y	Y	N	–	N	–	Y	N
12. DO YOU EVER REQUIRE A CONFORMAL COATING?	–	–	–	–	–	–	Y	–	–	–	–	–	Y	Y	–	–	–	–	–	–	–	–	–	Y	N
13. HOW DO YOU OVERCOME THE ELECTROSTATIC PROBLEM?																									
DO NOTHING.	–	–	–	–	√	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
SHOCK DURING PIND TEST.	√	√	–	√	–	–	√	√	–	√	√	–	–	√	√	√	√	√	√	–	–	–	√	–	–
SHOCK PRIOR TO PIND TEST.	–	–	–	–	–	–	–	–	–	–	–	–	–	–	√	–	√	–	√	√	–	√	√	√	√
TEMPERATURE BAKE.	–	–	–	–	–	–	√	√	–	–	–	–	–	√	–	√	–	√	–	–	–	–	–	–	–
DEGAUSSING.	–	–	–	–	–	–	–	√	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
14. WHAT DO YOU BELIEVE IS THE BIGGEST PROBLEM WITH PLASTIC DEVICES?	–	–	–	①	–	–	②	–	–	–	–	–	–	②	–	–	①	①	①	–	–	–	–	–	①
15. DO YOU USE PLASTICS?	–	–	–	N	–	–	N	–	–	–	–	–	–	N	–	–	N	N	N	–	–	–	–	–	N
16. CAN YOU USE PLASTICS?	–	–	–	Y	–	–	N	–	–	–	–	–	–	Y	–	–	N	N	Y	–	–	–	–	–	Y

① MOISTURE
② MOISTURE & CHEMICAL CONTAMINATION
Y – YES
N – NO
– NO ANSWER; ANSWER NOT CLEAR; QUESTION NOT ASKED.