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Technical Report

INTERFACE STANDARDS FOR
COMPUTER EQUIPMENT

September 1976

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INTERFACE STANDARDS FOR COMPUTER EQUIPMENT

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Data Systems Laboratory
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Huntsville, Alabama

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Prepared By
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ABSTRACT

The ability to configure data systems using modules provided by independent manufacturers is complicated by the wide range of electrical, mechanical, and functional characteristics exhibited within the equipment provided by different manufacturers of computers, peripherals, and terminal devices. A number of international organizations have been and still are involved in the creation of standards that enable devices to be interconnected with minimal difficulty, usually involving only a cable or data bus connection that is defined by the standard.

This report examines the elements covered by an interface standard, and identifies and describes the most prominent interface standards presently in use. In addition, it presents an index of the important standards organizations, along with addresses where standards information may be obtained.

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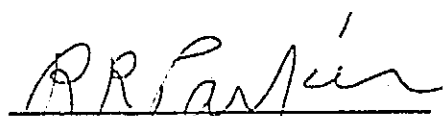
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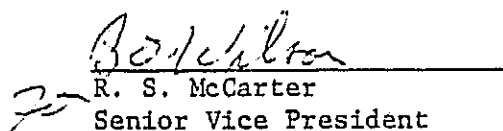
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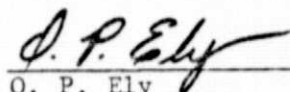R. R. Parker, Ph.D.   R. S. McCarter
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1. INTRODUCTION

Modern day data systems are comprised of wide and ever increasing numbers and types of modular devices that provide data to, receive data from, and are under the control of a computer or computers within a given system. A typical system will include some combination of processors, memory, standard peripheral equipment (magnetic tapes, disks, etc.), terminal devices (alphanumeric display devices, graphic display devices, keyboards, etc.), communications links to other computers and to remote terminal, data acquisition equipment (electronic counters, digital voltmeters, etc.), instrumentation sen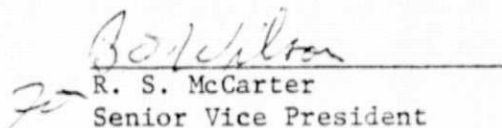sors (digital pressure, temperature, and voltage transducers, etc.), and control systems (process control, numerical control, etc.). All of the devices within a system communicate with a central processor and among themselves via the boundary or interface that connects one device to another. The ability to communicate is governed by the ability to transfer data in an orderly manner across the system interfaces. This study discusses the issues associated with data communications within a modular data system and identifies what is being done in the area of standardization in order to reduce the complexity and associated cost of configuring and rapidly reconfiguring modular systems.

Typically, a computer has one or more busses that are used for input and output of data. Each vendor independently designs the I/O systems for its line of computers, meeting the criteria that best satisfy particular technical and marketing goals. Independent device manufacturers produce equipment to be pin compatible with a particular computer (usually an IBM computer), or they manufacture for the OEM market and provide an interconnection interface that is unique to their product. Consequently, integrating a data system with equipment from a number of vendors presents a formidable interconnect problem. Theroetically, if the user has n computers and m dissimilar devices, the number of interfaces is $n \times m$ in order for all modules to communicate.

An organization such as NASA, or any center within NASA, has literally hundreds of computers and thousands of interfacing devices. Substantial savings in time and hardware costs can be realized if it is possible to freely reconfigure and update systems to permit the sharing of devices between system configurations and to add new devices that take advantage of current technology. Such reconfiguration and updating is presently expensive and time consuming because of the interfacing problems, but the application of standard interfaces holds promise for reducing the cost in the future.

The study is intended to provide a guide to the types of standards that exist and to provide an understanding of some of the more prominent standards, with emphasis on the function characteristics of these standards. The study is organized as follows:

- Section 2 discusses interface requirements and identifies the areas covered by standards.

- Section 3 discusses the current status of interfacing standards, with emphasis on three prominent standards.

- Section 4 presents conclusion regarding the future of standards and makes recommendations regarding NASA's role in fostering the adoption of standards for the future.

- The Appendix identifies the most prominent standards organizations and provides addresses for these organizations.

2. PERIPHERAL INTERFACE REQUIREMENTS

IEEE Standard 488-1975 (one of the most encompassing interface standards in use today) defines an interface as, "a shared boundary between a considered device and another device, or between parts of a device, through which information is conveyed." The interface exists to facilitate communications between the devices comprising the system, and accomplishes its mission by matching the devices electrically, mechanically, and functionally. The interface is distinguised from the controller, which provides functional control of devices, and which is connected to the processor via its own interface.

The functional capabilities of the interface as discussed herein are communications oriented as opposed to device functional capabilities for purposes of device control. Thus, the functional capabilities of the interface are limited to those functions necessary to initiate and control the flow of data across the interface, including interface configuration, status checking, (e.g., data available, ready for data, data accepted, etc.), and data transmissions. An example is the handshake cycle that occurs between byte transfers across an interface. The handshake consists of a hardwired interlocked sequence of status and control signals that must occur in a defined sequence in order to permit data to cross the interface.

The paragraphs that follow discuss design considerations that affect the ability to standardize interfaces. Devices satisfying these considerations can be connected simply with a cable without concern for electrical, mechanical and functional differences.

2.1 DATA SYSTEMS INTERFACES

Most modern computers have two paths for input and output of data, the CPU I/O bus and the Direct Memory I/O bus (Figure 2-1). Typically these busses include the following types of signal lines:

COMPUTER

CPU I/O BUS

CPU

DATA LINES

DEVICE ADDRESS LINES

DEVICE CONTROL LINES

HANDSHAKE LINES

MEMORY

DIRECT MEMORY I/O BUS

DATA LINES

MEMORY ADDRESS LINES
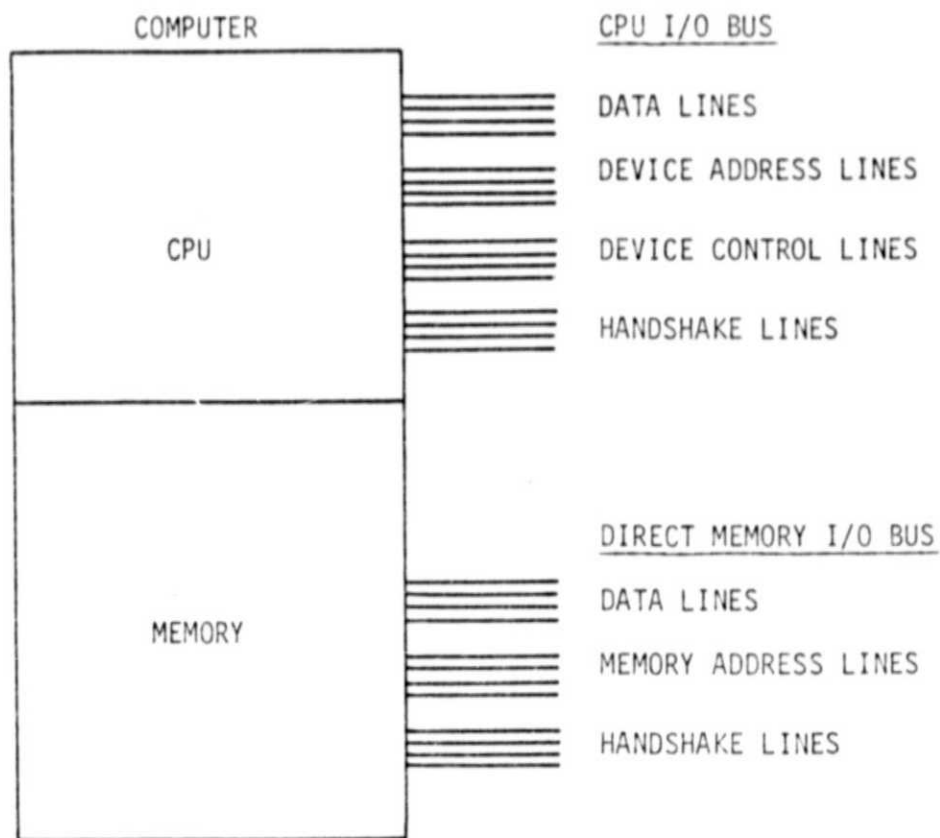
HANDSHAKE LINES

FIGURE 2-1
COMPUTER I/O BUS CONFIGURATION

CPU I/O BUS

- Data Lines (usually bidirectional)
- Device Address Lines
- Device Control Lines
- Handshake Lines

DIRECT MEMORY I/O BUS

- Data Lines
- Memory Address Lines
- Handshake Lines.

There are, of course, many variations. On some computers (e.g., IBM 1130 and a number of microcomputers) a single set of lines is time multiplexed for the communication of device address and data on the CPU I/O bus. A number of computers (IBM 370/360, Varian V-70, Datacraft 6020) have internal channel controllers that generate memory addresses, eliminating the need for memory address lines on the Direct Memory I/O Bus. On the other hand, for some computers (e.g., PDP-11) the Direct Memory Access Bus is a direct extension of the system's internal bus.

It does not seem likely that there will be a standardization of computer I/O busses in the foreseeable future.

Connecting an arbitrary peripheral to a computer usually requires the several units of equipment shown in Figure 2-2. The device controller (e.g., magnetic tape controller, disc controller) controls the operation of one or more identical or similar devices. If the device controller is designed for a specific computer it can connect directly to that computer's I/O busses. Otherwise, an additional unit is required for effecting the electrical and mechanical interface of the device controller to an I/O bus.

Controllers and/or interfaces are a major expense for NASA in the integration of data systems that use independently manufactured peripherals.

The effectiveness of future data management systems will depend to a large extent on the practicality of readily configuring and re-configuring large and complex data system networks using independently

I/O BUS

INTERFACE

PERIPHERAL "A" CONTROLLER

PERIPHERAL "A_n"

PERIPHERAL "A_1"

INTERFACE

PERIPHERAL "B" CONTROLLER

PERIPHERAL "B_n"
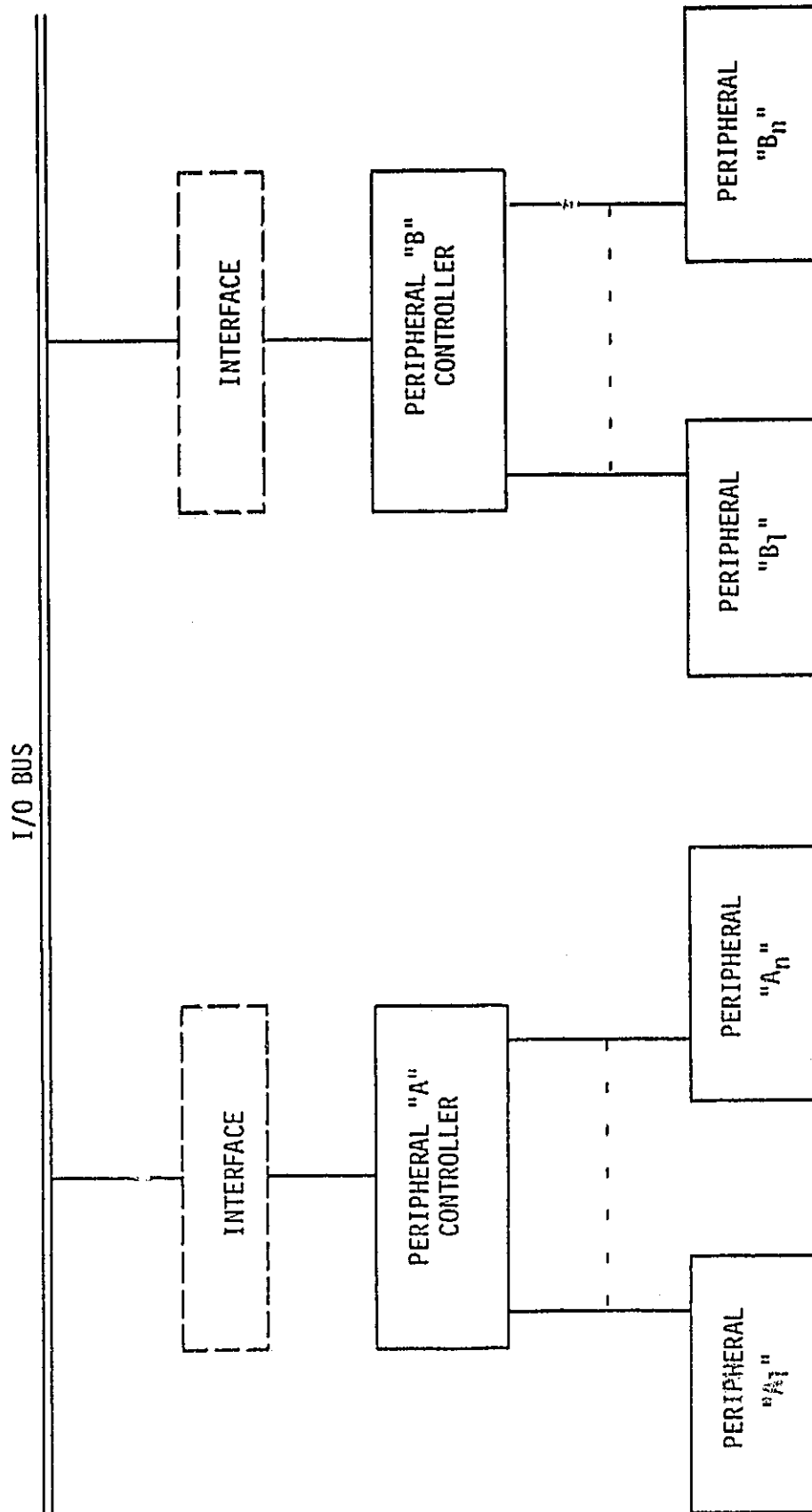
PERIPHERAL "B_1"

FIGURE 2-2

PERIPHERAL INTERFACE TO COMPUTER I/O BUS

2-4

manufactured devices. While this is technically feasible presently, it is expensive and frequently time consuming, thus negating the rationale behind modular systems.

Several recently adopted interface standards (IEEE 488-1975 and IEEE 583-1975) define communication interface characteristics that can be employed for transmitting messages between peripherals and a computer. The objective of these standards is to rearrange the functions of a conventional I/O system so that interface functions and device specific functions are clearly separate and distinct, providing an opportunity to standardize the interface functions. Figure 2-3 shows a configuration that illustrates an application of the standards to the interconnection of peripherals and a computer.

The standards define the electrical and mechanical characteristics of the interface bus and the functional requirements for communicating messages on the bus. A special device, the interface controller, acts as an interface between the computer and the interface bus; its design is unique to each model of computer, depending on specific characteristics of the computer's I/O bus. The other devices on the interface bus are the peripherals and their associated peripheral controllers. Of course, each peripheral controller is unique to the peripheral, but its interface functions relate only to the operation of the interface bus and not to properties that are peculiar to a specific computer.

The principal benefit of the configuration in Figure 2-3, relative to that in Figure 2-2, is the greatly reduced need for special interfaces. Once an interface controller is available for a particular computer, any peripheral that satisfies the interface standard can be used with that computer. Further, networks of computers and peripherals can be reconfigured readily so long as each computer has the standard interface controller connected to its I/O busses and all peripheral controllers meet the standard. Increasingly, such peripheral controllers are available from the peripheral vendors.

Beyond the standardization identified above, there is a definite trend to integrate all device specific functions into the peripheral,
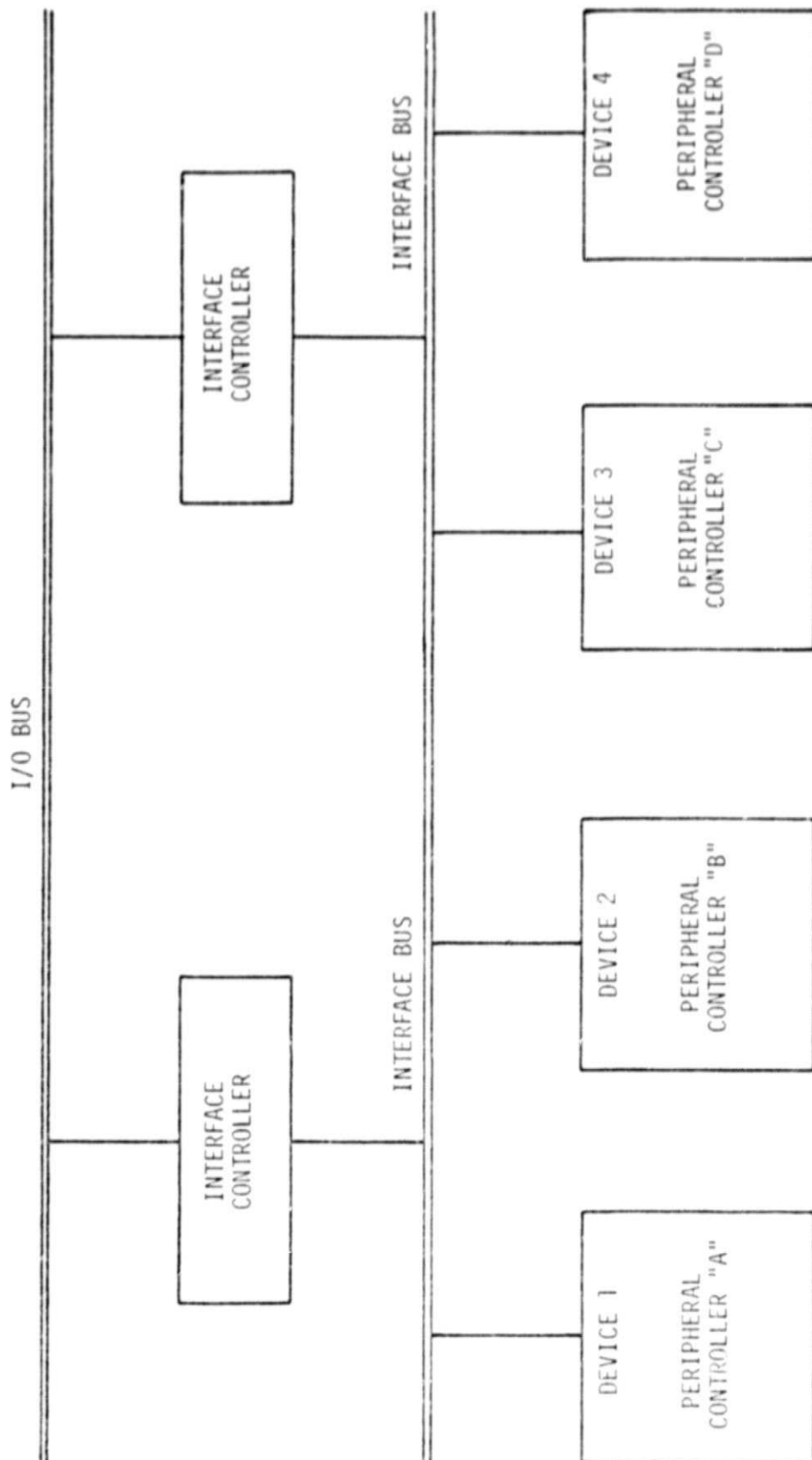
FIGURE 2-3

PERIPHERAL INTERFACE TO STANDARDIZED INTERFACE BUS

obviating the need for a separate and distinct peripheral controller. Some disc drive manufacturers now offer units with integrated controllers, and most line printers now include buffer memories and all device specific functions in the enclosure with the printer mechanical assembly. Unfortunately, few if any of these newer products satisfy one of the recently adopted standards for bit-parallel interfacing of dissimilar devices.

2.2   THE INTERFACE SYSTEM

An interface system is comprised of the hardware and functional elements required to achieve the electrical, mechanical, and functional compatibility necessary to communicate between system devices. Included within the hardware elements are the cables, connectors, driver and receiver circuits, and functional logic circuits. The functional elements include the signal line descriptions and the timing and control or protocol conventions necessary to transfer the data between devices. The paragraphs that follow discuss the considerations that affect the design and implementation of an interface system.

2.2.1   Electrical Interfacing Considerations

Electrical interfacing considerations cover the definition of all electrical characteristics as these characteristics relate to the interface, including voltage and current levels, impedence, hi and low state definitions, pulse widths, pulse rates, signal rise times, permissible delay between signals, grounding, resistive and capacitive loading, cabling interconnections, maximum cable lengths, cable impedence, receiver noise specifications, and power requirements.

The specifications on the electrical system (pulse width, pulse rate, rise time) establish the bandwidth of the system and define the ability to support high speed devices. Bandwidth requirements impose a heavy impact on the cost and performance of systems and are frequently considered to be the most critical factor in system design. This is particularly true in todays environment where emphasis is on processing and I/O speed. Thus, the electrical interface characteristics set the pace for system performance.

2.2.2 Mechanical Interfacing Considerations

Mechanical interfacing considerations are primarily related to cabling and connectors for mating the interfaces of the devices within the system. In the case of some standards (e.g., IEEE 583-1975), the mechanical considerations include the design and installation of interfacing modules that fit into existing rack structures. Such modules may connect into a motherboard within the rack.

Mechanical considerations must be exact, but these factors rarely affect performance other than to provide ease of configuration and reconfiguration.

2.2.3 Functional Interfacing Considerations

Functional interfacing considerations may be defined (as in IEEE Std. 488-1975) in terms of three major functional areas:

1) Device functions,
2) Interface functions, and
3) Message coding logic.

Device functions are application dependent and are not included within the scope of this report. Interface functions and message coding logic may be considered as applications independent, and as such are considerations that govern the interface definition.

Included within the category of functional parameters that affect interface designs are those protocol and timing functions such as:

- Definition of interface states
- Handshaking between interface modules
- Interrupt servicing
- Polling
- Command definition
- Status indicators
- Message coding and formatting
- Message frequency
- Timing and synchronization.

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Precise definition of the functional and message coding parameters are required in order to communicate between modules. Each interface state must be capable of being achieved only through a prescribed sequence of events that occur concurrently and in accordance with defined message formats and timing conventions. Although the definition of the interface functions must be specific and detailed, the options available must be broad and still general enough to permit the standard to be used with a number of applications, and where feasible to take advantage of new technology. Discussions of specific standards in the following section emphasize the functional characteristics of the standards.

3. CURRENT STANDARDS

Three primary standards and a number of less important standards exist for interfacing devices in data systems. The three primary standards are:

1) IEEE Standard Digital Interface for Programmable Instrumentation (IEEE Std. 488-1975),

2) IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC) (IEEE Std. 583-1975), and

3) Interface Between Data Processing Terminal Equipment and Data Communications Equipment (EIA RS-232-C).

Versions of the RS-232-C standard have been in existance for more than a decade. The two IEEE standards listed above were adopted in 1975, although IEEE Std. 583 was developed by the European Standards on Nuclear Electronics (ESONE) in 1969. The adoption of these two standards represents a major step in interface standards, and manufacturers of digital equipment appear to be rapidly accepting the standards.

IEEE Std. 488-1975 and IEEE Std. 583-1975 are both directed at byte-oriented computer-to-peripheral type interfaces, whereas, EIA RS-232-C applies to interfacing bit-serial data terminal equipment to bit-serial data communication equipment. In a typical configuration connecting a computer to a remote terminal, the RS-232-C interface standard applies to the modem-to-computer connection via the communications controller and to the modem-to-terminal connection at the remote site.

The three primary standards are discussed in subsequent paragraphs. The less important standards are listed below without further elaboration. Addresses for obtaining copies of the standards are provided in Appendix A.

EIA RS-422-75 Electrical Characteristics of Balanced
Voltage Digital Interface Circuits

EIA RS-423-75 Electrical Characteristics of Unbalanced
Voltage Digital Interface Circuits

EIA RS-408-73 Interface Between Numerical Control
      Equipment and Data Terminal Equipment Employing
      Parallel Binary Interchange

EIA RS-366-69 Interface Between Data Terminal Equipment
      and Automatic Calling Equipment for Data Communications

EIA RS-357-68 Interface Between Facsimile Terminal Equip-
      ment and Voice Frequency Data Communications Terminal
      Equipment

EIA RS-334-67⎫ Signal Quality at Interface Between Data
ANSI X3.24-68⎭
      Processing Terminal Equipment and Synchronous Data
      Communications Equipment for Serial Data Transmission

ANSI X.28-1971 Procedures For the Use of Communications
      Control Characters of American National Standard Code
      for Information Interchange in Specified Data Communi-
      cations Links

ANSI X3.15-1966 Bit Sequencing of the American National
      Standards Code for Information Interchange in Serial-
      by-Bit Data Transmission

ANSI X3.16-1966 Character Structure and Character Parity
      Sense for Serial-by-Bit Communications in the American
      National Standard Code for Information Interchange

ANSI X3.1-1966 Synchronous Signaling Rates for Data
      Transmission

ISO 1155-1973 Information Processing - Use of Longitudinal
      Parity to Detect Errors in Information Messages

ISO 1177-1973 Information Processing - Character Structure
      for Start/Stop and Synchronous Transmission

ISO 2628-1973 Basic Mode Control Procedures - Compliments

ISO 2629-1973 Basic Mode Control Procedures - Conversational
      Information Message Transfer

ISO 2593-1973 Connector Pin Allocations for Use With High
      Speed Data Terminal Equipment

ISO 2110 - Data Communications - Data Terminal and Data
      Communications Equipment Interchange Circuits - Assign-
      ment of Connector Pin Numbers

ISO R1745 - Basic Mode Control Procedures for Data Communi-
      cations Systems.

3.1 IEEE STANDARD DIGITAL INTERFACE FOR PROGRAMMABLE INSTRUMEN-
TATION (IEEE STD. 488-1975/ANSI MC1.1-75)

3.1.1 Applicability

IEEE Std. 488-1975 applies to interface systems used to connect
both programmable and nonprogrammable electronic measuring apparatus with
other apparatus and accessories necessary to assemble instrumentation
systems. Although written primarily for instrumentation systems, the
standard is quoted as being applicable to other instrumentation elements
such as processors, stimulus, display or storage devices, and terminal
units. This is indeed true and it is borne out by the number of manu-
facturers that are applying the standard to a variety of products.

The standard applies to the interface of asychronous data systems,
or portions of them where:

1) Data exchanged among the interconnected apparatus is
   digital;

2) The number of devices that are connected by one contiguous
   bus does not exceed 15;

3) The total path length over the interconnecting cable
   does not exceed 20 meters; and

4) The data rate across the interface does not exceed 1 Mbs.

The standard, which is written for byte-serial, bit-parallel
interfaces, specifies the device-independent mechanical, electrical and
functional interface requirements that independently manufactured apparatus
shall meet in order to be interconnected and communicate unambigiously via
the interface.

3.1.2 Functional Characteristics

The functional characteristics of the interface system are defined
and controlled by a set of 16 signal lines that are used to carry all
information, interface messages, and device dependent messages among inter-
connected devices. Messages may be coded on one or a set of signal lines
as determined by the particular message content and its relationship to
the interface system. The bus structure, which is illustrated in Figure 4-1,

UP TO 15 DEVICES

DEVICE A

ABLE TO
TALK, LISTEN,
AND CONTROL

(e.g. calculator)

DEVICE B

ABLE TO
TALK AND
LISTEN

(e.g. digital
multimeter)

DEVICE C

ONLY ABLE
TO LISTEN

(e.g. signal
generator)

DEVICE D

ONLY ABLE
TO TALK

(e.g. counter)

DATA BUS

*DATA BYTE
TRANSFER
CONTROL*

*GENERAL
INTERFACE
MANAGEMENT*

DIO 1...8 } SUBCHANNEL "A" (DEVICE
FUNCTIONAL & COMMUNICATIONS
CONTROL MESSAGES)

DAV
NRFD
NDAC

IFC
ATN
SRQ
REN
EOI

SUBCHANNEL "B" (COMMUNICA-
TIONS CONTROL MESSAGES)

FIGURE 4-1

INTERFACE CAPABILITIES AND BUS STRUCTURE
IEEE Std. 488-1975

is organized into three sets of signal lines. Lines DIO1 thru DIO8 are designated as Subchannel "A" and these lines carry device functional and communication control messages, where the control messages are issued in conjunction with one of the five general interface management bus signal lines that are designated as follows:

1) ATN (Attention) is used to specify how data on the DIO signal lines are to be interpreted and which devices must respond to the data;

2) IFC (Interface Clear) is used to place the interface system, portions of which are contained in all inter-connected devices, in a known quiescent state;

3) SRQ (Service Request) is used by a device to indicate the need for attention and to request an interruption of the current sequence of events;

4) REN (Remote Enable) is used (in conjunction with other messages) to select between two alternate sources of device programming data; and

5) EOI (End or Identify) is used to indicate the end of a multiple byte transfer sequence or, in conjunction with ATN, to execute a polling sequence.

The three remaining lines are designated as the Data Byte Trans-fer Control Bus, and are used to effect the transfer of each byte of data on the DIO signal lines from an addressed talker to addressed listeners. (See definitions of talkers and listener below). The functions of the three lines are:

1) DAV (Data Valid) is used to indicate the condition (availability and validity) of information on the DIO signal lines;

2) NRFD (Not Ready For Data) is used to indicate the condition of readiness of device(s) to accept data; and

3) NDAC (Not Data Accepted) is used to indicate the con-
    dition of acceptance of data by device(s).

The DAV, NRFD, and NDAC signal lines operate in what is called
a three-wire (interlocked) handshake process to transfer each data byte
across the interface. The Handshake Process Timing Sequence is included
herein as Appendix B.

Devices that are interconnected in accordance with this standard
are designated as either listener, talker, or controller, where the
three categories are defined as follows:

1) A device with the capability to <u>listen</u> can be addressed
    by an interface message to receive device dependent
    messages from another device connected to the interface
    system.

2) A device with the capability to <u>talk</u> can be addressed
    by an interface message to send device dependent messages
    to another device connected to the interface system.

3) A device with the capability to <u>control</u> can address
    other devices to listen or to talk. In addition, this
    device can send interface messages to command specific
    actions within other devices. A device with only this
    capability neither sends nor receives device dependent
    messages. NOTE: The use of the word controller applies
    strictly to the management (control) of the interface
    system and does not imply the broad capabilities
    typically associated with the word in the data processing
    context.

Listener, talker, and controller capabilities occur individually and
collectively in devices interconnected via the interface system. A
system has only one controller at any given time, but the standard
permits control to be passed from one device to another within the
system.

3.1.3 Industry Usage

This standard is finding rapid acceptance among instrumentation manufacturers, led by Hewlett Packard (the originator of the basic interface concepts embodied in the standard). There are commercially available adapters that allow the 16 wires to be connected to the switched common carrier network via EIA RS-232-C compatible modems, and recent product announcements by Hewlett Packard and Tektronics indicate that the interface standard can and will be adopted by computer and computer peripheral manufacturers.

Twenty companies that offer 96 products compatible with IEEE 488 were identified in a recent interview with Hewlett Packard's Corporate Standards Engineer. A sampling of these products is provided in Table 3-1.

In addition to those products available from the referenced list, the interface promulgated by this standard is highly compatible with present microprocessor technology in terms of speed and channel bandwidth. Single chip microprocessor-to-IEEE-488 channel interfaces are available now for most 8-bit microprocessors.

3.1.4 IEEE 488-1975 Summary

In summary, the document is comprehensive in its presentation and will likely serve as a model for future standards. The document is sometimes criticized for not covering the software aspects of interfacing sufficiently. However, the lack of required software specifications permits a flexibility that is a strength in its own right.

The reader is referred to the standards document for a more thorough discussion of the standard. The document is organized into six sections and seven appendixes as follows:

1) General (Introductory with definitions and overview).

2) Functional Specifications (Functional partitioning, interface function concepts, message concepts, definition and state diagrams for the interface function repertoire, and message coding definitions).

VENDOR	TYPICAL PRODUCT
Boonton Electronics	1 MHz Bridge
Data Works Instrument	Bus Interface Coupler
Dana Laboratories	Timer/Counter
Dana Exact	Frequency Synthesizer
Decca	Communications Receiver
Fluke Manufacturing	Signal Generator
Hewlett Packard	21MX Computer Interface, many others
Interface Technology	Word Generator
Interstate	Signal Generator
Ithaco	Programmable Filter
Motorola	Bus Transceivers
Nicolet Instruments	Printer
Philips	DVM
Physical Data	Transient Recorder
Process Dynamics	Flexible Disk System
Rhode & Schwarz	Card Reader
Systron Donner	Programmable Power Supply
Tektronix	Graphic Computing System
Wavetek	Waveform Generator

TABLE 3-1. IEEE 488-1975 Vendors & Products

(Extracted from July, 1976 Electronics Products Magazine)

3) Electrical Specifications.

4) Mechanical Specifications.

5) System Applications and Guidelines for the designer.

6) System Requirements and Guidelines for the Users.

Appendix A- Typical Instrument System

Appendix B- Handshake Process Timing Sequence

   (Include as Appendix B herein)

Appendix C- Interface Function Allowable Subset Reference List

Appendix D- Interface Message Reference List

Appendix E- Multiline Interface Messages: ISO Code Representation

Appendix F- Logic Circuit Implementation

Appendix G- Parallel Polling Sequence

3.2   IEEE STANDARD MODULAR INSTRUMENTATION AND DIGITAL INTERFACE
       SYSTEM (CAMAC: COMPUTER AUTOMATED MEASUREMENT AND CONTROL)
       (IEEE STD. 583-1975).

   3.2.1 Applicability

   IEEE 583-1975 is intended to serve as a standard for a range of
modular instrumentation capable of interfacing transducers and other
devices to a digital controller for data and control. The standard,
which was originally developed by the European Standards on Nuclear
Electronics (ESONE) in 1969, has been used widely in nuclear laboratories
for more than six years and is now beginning to be used in medical research,
astronomical studies, and industrial process control, among many other
applications.

   The basis for IEEE 583 is the crate-module pair and the data bus
or Dataway illustrated in Figure 3.2. The crate houses the individual
modules and contains the Dataway or Motherboard, which is simply an
interconnection method for the modules and the crate controller. Since
the entire system is centered around the crate configuration and the
modules, the mechanical specifications take on a particularly significant
importance for this standard. The basic mechanical and electrical charac-
teristics for the crate and the interfacing modules are defined in detail
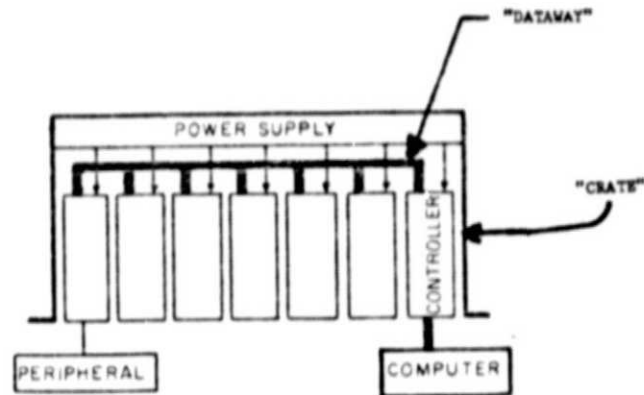
FIGURE 3.2
Standard Arrangement. Data Channel (Dataway)'
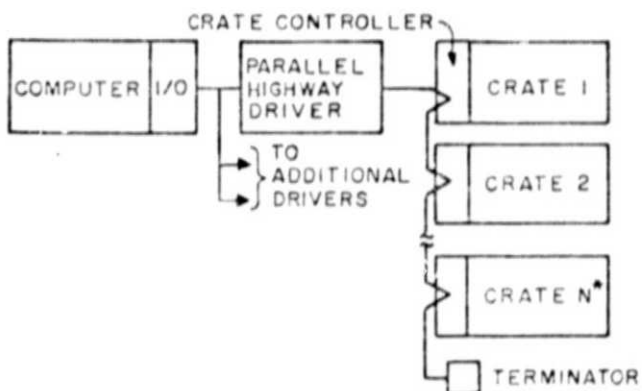is heavy black line going to all modules

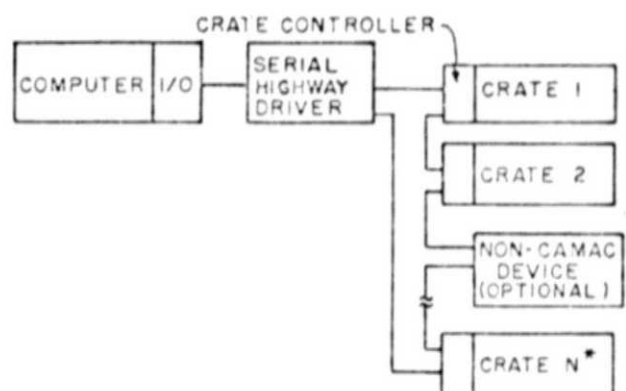FIGURE 3.3

Parallel Highway System
*Typically N = 7 max

Figure 3.4

Serial Highway System
*Typically N = 62 max

in this standard. A crate configuration consists of the crate with the dataway and up to 24 plug-in modules, one of which is the crate controller. As described herein, a controller refers to a unit occupying the control station and one normal station.

The controller serves as the device for controlling access to the dataway on a time-shared basis. All instruments and other functional modules on the data bus are under the control of the controller, and can communicate with each other, with peripherals, with computers, and with other external controllers as illustrated in Figure 3.2.

Both single-crate and multiple-crate systems can be assembled. Figure 3.3 shows a multiple-crate configuration capable of bit-parallel, byte-parallel operation, and Figure 3.4 shows a serial system in which the data is transferred bit or byte serial. The parallel configuration is useful for very high data rate systems, whereas, the serial configuration is useful for applications involving long distances and where interconnection cost is a factor.

3.2.2 Functional Characteristics

The functional characteristics of IEEE 583-1975 are centered around the use of the Dataway lines. Table 3-2 (extracted from the standard) summarizes the use of the 86 dataway lines. Figure 3.5 shows the dataway configuration, which consists of bussed connections except for the Station Lines, N, and the Look-At-Me (LAM or Service Request) lines, L. The latter two groups of lines are individually connected from the controller to each module in the crate.

When the controller wants to issue a command to one or more modules, the N line to the affected modules is set to a one. Similarly, when a module wants to demand serivce, it sets the L line to the active or one state.

Figure 3.6 shows the crate controller/module interface in terms of the line functions, including the N and L lines. Brief descriptions of the line functions and operational modes are presented in subsqeuent paragraphs.

Table 3-2
Standard Dataway Usage

| Title	Designation	Contacts	Use at a Module
Command			
Station Number	N	1	Selects the module (individual line from control station)
Subaddress	A1, 2, 4, 8	4	Selects a section of the module
Function	F1, 2, 4, 8, 16	5	Defines the function to be performed in the module
Timing			
Strobe 1	$S1$	1	Controls first phase of operation (Dataway signals must not change)
Strobe 2	$S2$	1	Controls second phase (Dataway signals may change)
Data			
Write	$W1$-$W24$	24	Bring information to the module
Read	$R1$-$R24$	24	Take information from the module
Status			
Look-at-Me	L	1	Indicates request for service (individual line to control station)
Busy	B	1	Indicates that a Dataway operation is in progress
Response	Q	1	Indicates status of feature selected by command
Command Accepted	X	1	Indicates that module is able to perform action required by the command
Common Controls			*Operate on all features connected to them, no command required*
Initialize	Z	1	Sets module to a defined state (Accompanied by $S2$ and B)
Inhibit	I	1	Disables features for duration of signal
Clear	C	1	Clears registers (Accompanied by $S2$ and B)
Nonstandard Connections			
Free bus lines	P1, P2	2	For unspecified uses
Patch contacts	P3-P5	3	For unspecified interconnections. No Dataway lines
Mandatory Power Lines			*The crate is wired for mandatory and additional lines*
+24 V dc	+24	1	
+ 6 V dc	+ 6	1	
- 6 V dc	- 6	1	
-24 V dc	-24	1	
0 V	0	2	Power return
Additional Power Lines			*Lines are reserved for the following power supplies:*
+200 V dc	+200	1	Low current for indicators, etc
+ 12 V dc	+ 12	1	
- 12 V dc	- 12	1	
117 V ac (Live)	ACL	1	
117 V ac (Neutral)	ACN	1	
Clean Earth	E	1	Reference for circuits requiring clean earth
Reserved	Y1, Y2	2	Reserved for future allocation
Total		86	
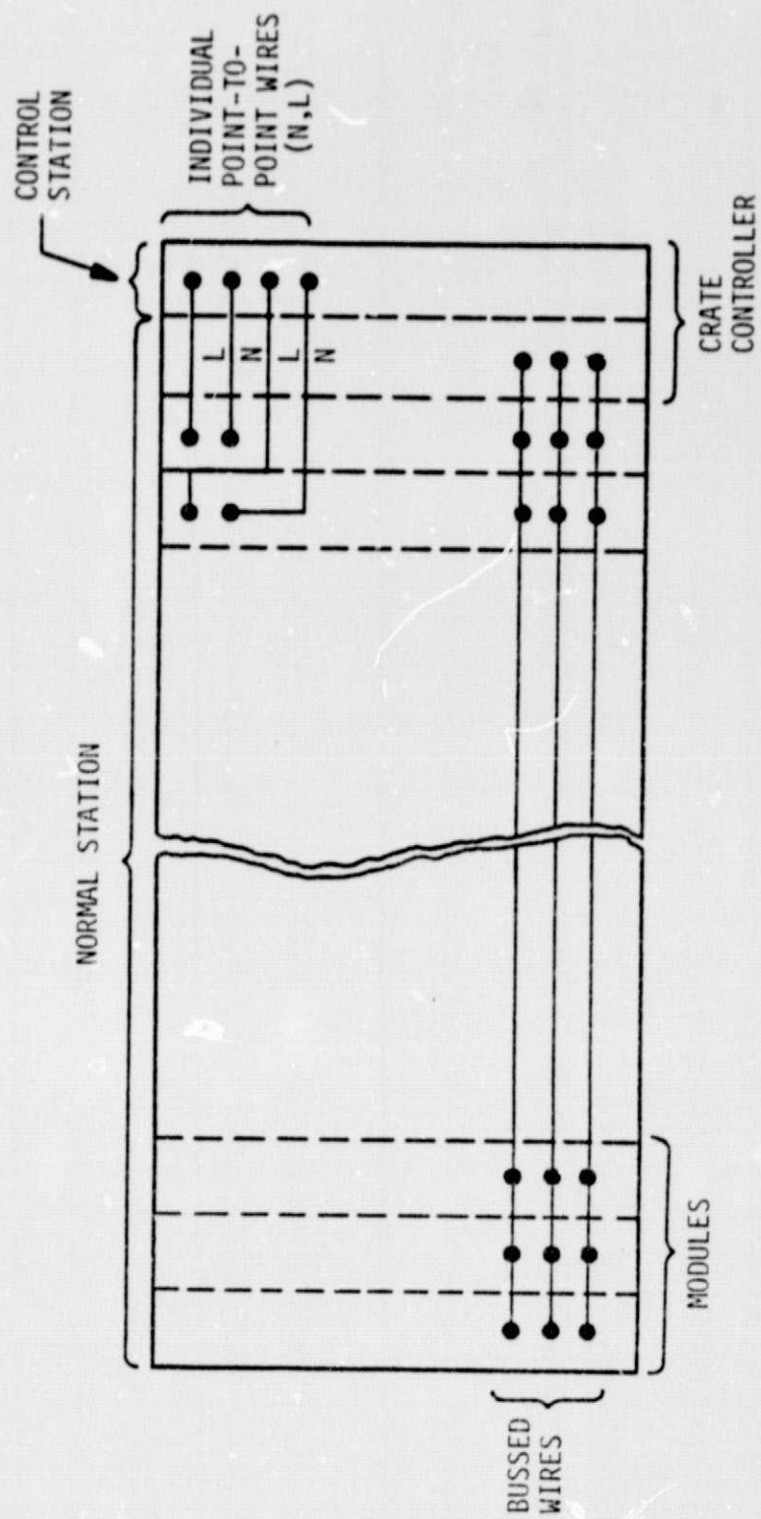
FIGURE 3.5

DATAWAY CONFIGURATION
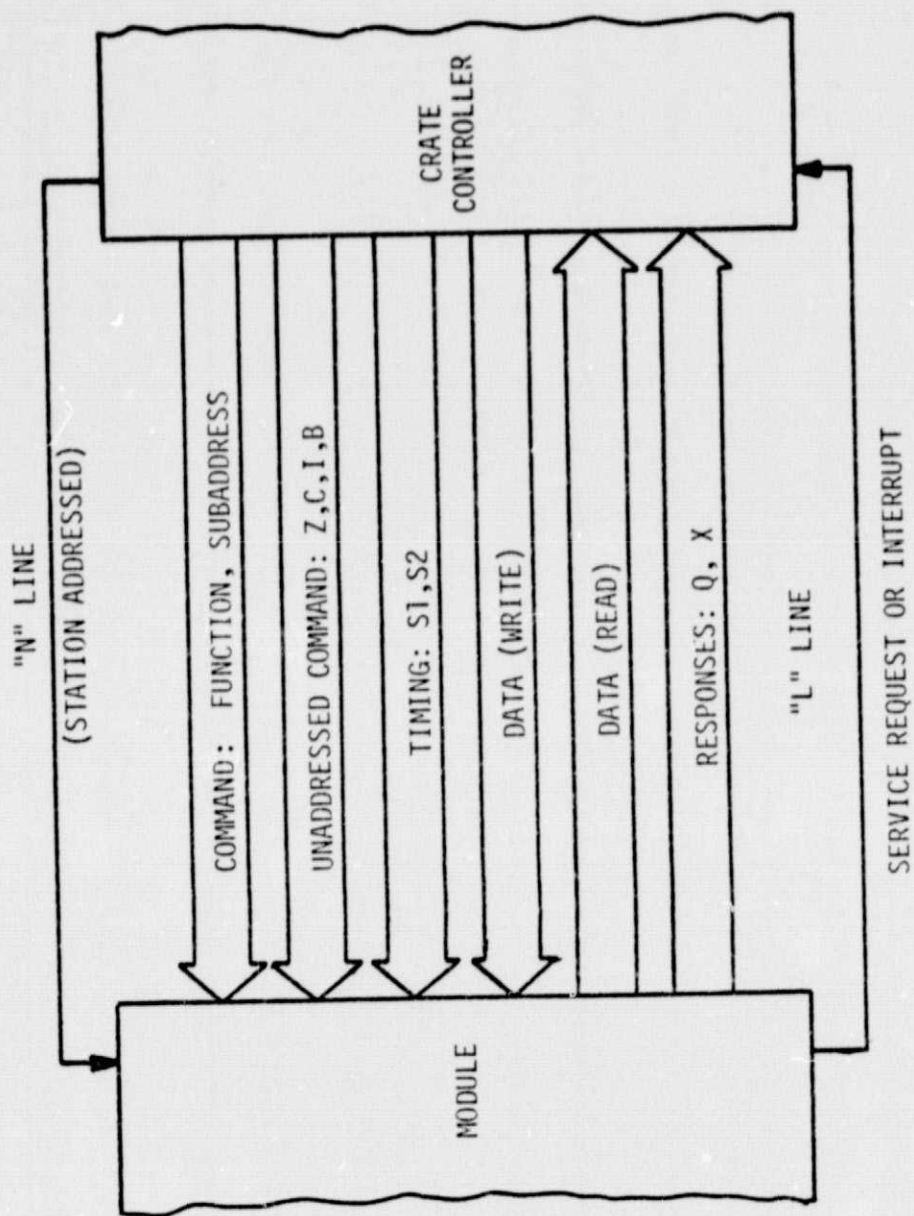
FIGURE 3.6

CRATE CONTROLLER/MODULE INTERFACE

Two types of Dataway operations are permissible when using IEEE 583-1975 compatible modules. During Command Operations the controller generates a command consisting of signals on individual Station Number Lines to specify one or more modules, on the Subaddress Bus Lines to specify a subsection of the module, and one the Function Bus Lines to specify the operation to be performed. During Unaddressed Operations there is no command, but the controller generates one of the common control signals on the Initialize or Clear Bus Lines, and this operates on all modules connected to the bus line. During command operations and unaddressed operations the controller generates a signal on the Busy Bus Line. The Busy signal is available at all stations to indicate that a Dataway operation is in progress. Two timing signals, Strobes S1 and S2, are generated in sequence on separate bus lines during command operations. Only Strobe S2 is mandatory during unaddressed operations, but S1 may also be generated.

During a Dataway command operation there may be either a Read data transfer from a module to the controller, a Write data transfer from the controller to a module, or neither.

In response to a Read command the addressed module generates Read data signals, which are available to the controller from the time of Strobe S1 onward. In response to a Write command the addressed module accepts Write data signals from the controller at the time of Strobe S1.

The addressed module indicates by a signal on the Command Accepted Bus Line whether it is able to perform the action required by the command. It may also transmit one bit of status information on the Response Bus Line. The controller accepts the Command Accepted and Response signals at the time of Strobe S1.

Any module may generate a signal on its individual Look-At-Me line to indicate that it requires attention.

Three common control signals are available at all stations, without requiring addressing by a command, in order to either Initialize all units (typically after switch-on), Clear data registers, or Inhibit features such as data taking.

3.2.3 Industry Usage

As pointed out previously, this standard has been widely accepted
in the nuclear electronics field for more than six years and acceptance
is growing. Table 3-3 presents a representative list of vendors and
products that are currently using the standard. The list is intended to
be representative and is by no means complete. In fact, more than 1000
functionally different modules from more than 40 vendors are available
as IEEE 583 compatible devices.

3.2.4 IEEE 583-1975 Summary

IEEE 583-1975 is comprehensive in its presentation and it serves
a valuable function for many interfacing situations. It is especially
useful for high speed data applications and has gained wide acceptance
by a large number of users. The most significant limitation to the system
appears to be the requirement to use the crate and the requirement to use
only one controller per crate. Although a crate is not expensive, (A
fully powered unit costs approximately $1500.), the unit consumes space
which may be awkward for applications involving only a few modules.

The limitation of only one controller per crate could produce
conflicts in situations where there is need for multiple controllers.
This limitation can be overcome through the use of multiple crates, but
it compounds the space problem and cost begins to become a factor.

These problems tend to be offset by the lack of software complexity
in the system. If a system is configured using modules that satisfy these
standards, it is ready to function when the modules and the applications
software are installed and working.

The users of this standard are enthusiastic in their support of
it, and there is every indication that this support is increasing.

The reader is referred to the standards document for a more
thorough discussion of the standard. The document is divided into nine
sections and six appendixes as follows:

VENDOR	PRODUCTS
Bi-Ra Systems Inc.	Counters
Digital Equipment Corp.	Timers
EGG/Ortec, Inc.	Register (In, Out, Serial, Parallel)
General Automation, Inc.	Analog Multiplexer
Joerger Enterprises	D/A Converter
Jorway Corp.	Paper Tape Reader
Kinetic Systems Corp.	Magnetic Tape Control
LeCroy Research Systems Corp.	Card Reader
Nuclear Enterprises, Inc.	Graphic Display
Nuclear Specialties, Inc.	Line Printer
Packard Instruments Co.	Crates & Hardware
Standard Engineering Corp.	Crate Controllers (for PDP-8,11,NOVA,HP 2100)
Tektronix, Inc.	Branch Drivers

TABLE 3-3   IEEE 583-1975 VENDORS & PRODUCTS

(Extracted From April, 1976 IEEE Spectrum)

1) Introduction

2) Intrepretation

3) Basic Features

4) Mechanical Characteristics

5) Use of the Dataway Lines

6) Dataway Commands

7) Signal Standards

8) Power Line Standards

9) Forced Air Ventilation

Appendix A - Definition of Module and Controller

Appendix B - Digital Signal Classes and Standard Markings
for Coaxial Connectors

Appendix C - Preferred Connectors and Contact Assignments

Appendix D - Typical Crate Mounted Power Supply and Venti-
lation Unit with Crate/Power Supply Interface
Housing

Appendix E - CAMAC Categories

Appendix F - Bibliography

3.3   INTERFACE BETWEEN DATA PROCESSING TERMINAL EQUIPMENT AND DATA COMMUNICATIONS EQUIPMENT (EIA RS-232-C)

3.3.1 Applicability

EIA RS-232-C is a non-comprehensive standard describing the
electrical, mechanical, and the logical interface between data processing
terminal equipment and data communications equipment. The scope of the
standard is illustrated in Figure 3.7, which involves the use of terminals
and computers connected via communication lines and modems. As
illustrated in the referenced figure, RS-232-C covers only the interface
between the terminal and the communiations interface (i.e., the modem)
and it does not make provisions for:

- The interface between the data communications equipment
  and the communications channel (BC-DC), or

FIGURE 3.7

EIA RS-232-C SCOPE

- Communications control procedures, whether between
  terminal and communications equipment (AB-DE) or
  end-to-end between data terminal equipment (A-E).

The standard covers bit-serial communications between devices
that are interconnected via modems and to certain direct connections
between a communication controller and terminal equipment where "null
modems" are used. The bit-rates covered by the standard range from zero
to nominally 20,000 bits per second.

3.3.2 Functional Characteristics

RS-232-C partially defines the logical or functional communications
control language in terms of the interface lines shown in Figure 3.8.

The lines are divided into four types as discussed below.

Type 1: Data Signals

- Transmitted Data (to the modem). Data generated by the
  terminal for transmission.

- Received Data (to the terminal). Data received by the
  modem for the terminal.

The transmitted and received data contain communications control
messages as well as device functional data. It is the function of the
terminal devices to recognize and separate these data from the serial
bit-stream.

Type 2: Timing Signals

- Transmitter Signal Element Timing. Two connections are
  defined. One sends signal element timing information
  from the transmitting terminal to its modem. The other
  sends timing information from the transmitting modem to
  its terminal.

- Receiver Signal Element Timing. Two connections are de-
  fined. One sends signal element timing information from
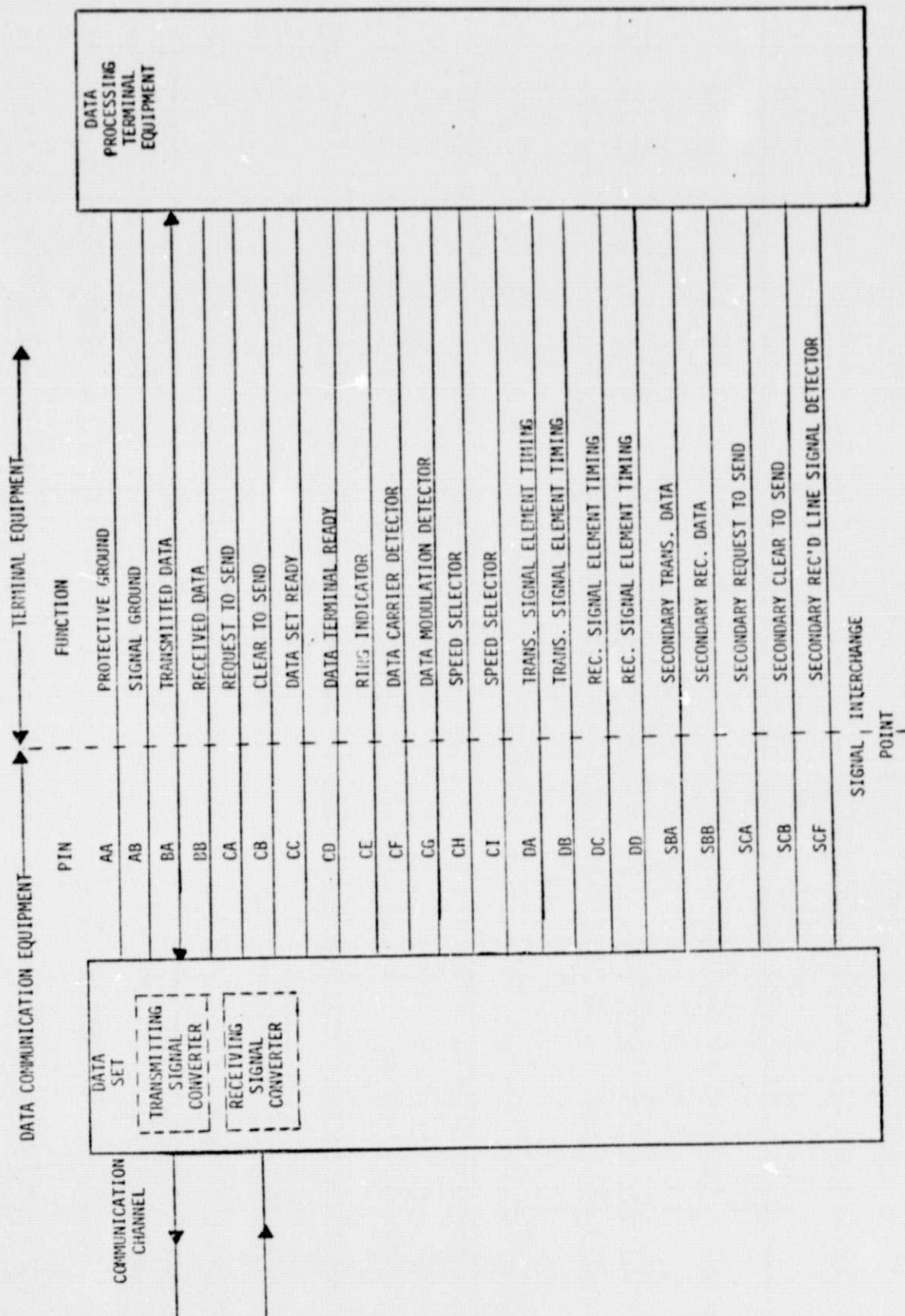
FIGURE 3-8

EIA RS-232-C INTERFACE FUNCTIONS

PIN	FUNCTION
AA	PROTECTIVE GROUND
AB	SIGNAL GROUND
BA	TRANSMITTED DATA
BB	RECEIVED DATA
CA	REQUEST TO SEND
CB	CLEAR TO SEND
CC	DATA SET READY
CD	DATA TERMINAL READY
CE	RING INDICATOR
CF	DATA CARRIER DETECTOR
CG	DATA MODULATION DETECTOR
CH	SPEED SELECTOR
CI	SPEED SELECTOR
DA	TRANS. SIGNAL ELEMENT TIMING
DB	TRANS. SIGNAL ELEMENT TIMING
DC	REC. SIGNAL ELEMENT TIMING
DD	REC. SIGNAL ELEMENT TIMING
SBA	SECONDARY TRANS. DATA
SBB	SECONDARY REC. DATA
SCA	SECONDARY REQUEST TO SEND
SCB	SECONDARY CLEAR TO SEND
SCF	SECONDARY REC'D LINE SIGNAL DETECTOR

the receiving terminal to its modem. The other sends timing information from the receiving modem to its terminal.

The timing signal connections are optional. A modem for START-STOP transmission does not use them.

Type 3: Control Signals

- Request to Send (to the modem). Signals on this connection are generated by the transmitting terminal when it wishes to transmit. The modem's carrier signal is transmitted during the ON condition of this connection. (With half-duplex operation, the OFF condition of this connection holds the modem in the receive-data state.)

- Clear to Send (to the terminal). Signals on this connection are generated by the transmitting modem to indicate that it is prepared to transmit data. They are a response to the Request to Send signal from the transmitting device. (With full-duplex operation the modem is in the transmit state at all times.)

- Data Set Ready (to the terminal). Signals on this connection are generated by the local modem to indicate to the transmitting machine that it is ready to operate.

(The following control signals are optional.)

- Data Terminal Ready (to the modem). When the terminal sends the ON condition on this connection it causes the modem to be connected to the communication line. The OFF condition causes it to be disconnected, in order to terminate a call or free a line for a different use.

- Ring Indicator (to the terminal). A signal on the connection informs the terminal that the modem is receiving a ringing signal from a remote location.

3-22

- Data Carrier Detector (to the terminal). A signal on this connection indicates to the terminal that the carrier (the sine wave that carries the signal) is being received. If the carrier is lost because of a fault condition on the line, the terminal will be notified by an OFF condition in this connection.

- Data Modulation Detector (to the terminal). An ON condition on this connection informs the terminal that the signal is being demodulated correctly by the modem. When the quality of demodulation drops below a certain threshold the terminal may take corrective action such as requesting retransmission or requesting that a lower transmission rate be used.

- Speed Selector. There are two speed selector connections, one to the modem and one to the terminal. Using them, the transmission rate may be changed.

Type 4: Grounds

- Protective Ground. Attached to the machine frame and possibly to external grounds.

- Signal Ground. Establishes the common ground reference potential for the circuits.

In addition to the primary functions described above, RS-232-C provides for a number of secondary functions. These functions serve a twofold purpose: (1) all functions are similar to primary functions except that data is transferred via the secondary channel in lieu of the primary channel, and (2) Selected functions and/or lines are used for circuit assurance or to interrupt the flow of data in the primary channel (less than 10 baud capability).

3.3.3 Industry Usage

RS-232-C is widely used by the manufacturers of terminal equipment and modems. In fact, every major manufacturer of such equipment claims

compatibility with the standard. Thus, this standard is currently the most widely adhered to interface standards in existance and there is every reason to believe that it will continue to be the predominant standard for bit-serial transmission via analog communication lines.

3.3.4 EIA RS-232-C SUMMARY

Although widely accepted and used, RS-232-C does not define procedures for using the interface functions defined by the standard. The standard resolved electrical and mechanical incompatibilities between devices without imposing any restriction on serial data stream content or line usage procedures. These procedures are implemented as required in the data processing terminal equipment, which is an ideal solution from a cost standpoint if the terminal equipment is programmable. Where terminal equipment is not programmable, however, procedures for line turn around, message acknowledge, and so on are part of the terminal hardware. As a result, two terminal devices may both be RS-232-C compatible, but impossible to interconnect directly (without modems) due to control message differences.

4. CONCLUSIONS AND RECOMMENDATIONS

The increased use of independently manufactured modules as components in data systems has created a definite need for a computer-independent method of interfacing the modules to computer systems. The cost of interfacing multiple modules with differing interfaces increases the cost of modular systems to the point that such systems are not economically attractive, which defeats the purpose of these systems. As a result, independent manufacturers are being pressured indirectly to conform to standards that make their devices economically attractive to the user community. The rather rapid acceptance of IEEE 488-1975 and IEEE 583-1975 by a number of independent manufacturers is somewhat the result of this pressure, and is evidence of the eagerness of many vendors to build to a standard that enables them to interface directly with a wider range of devices. At the same time, however, standards do not generally achieve broad acceptance by some of the larger vendors until either a major vendor (e.g., IBM) or a major user (e.g., the Government) adopt the standard and specify that it will be used on either a major line of equipment (e.g., the IBM 360/370 series) or on upcoming procurements. In view of this fact and in view of the importance of standards to an organization such as NASA, it is recommended that NASA begin preparations to adopt either IEEE 488-1975 or IEEE 583-1975 as the standard that will apply to future procurements of modular instrumentation equipment and to selected peripheral equipment, possibly excluding very high speed, high priority devices such as mass storage systems.

The question of precisely what type of peripheral devices to apply the standard to should be the subject of a more detailed study. The first question to be answered is what are the limiting conditions for applying the standard to such devices as high speed mass storage systems. If it is necessary to have a different standard for these special devices, then this different standard might also apply to other categories of peripherals. Thus, it is not a question of whether IEEE 488 and IEEE 583 apply to specific peripheral devices, because they do. It is primarily a consideration of how to minimize the number of standards to which manufacturers must conform.

In addition to data structure and data rates, other considerations that might affect the selection of one standard over another is the preferred or the cost effective method of controlling the data flow across an interface. IEEE 488 uses a controller (possibly the primary computer or computers within the network) and is capable of switching control from one device to another as long as there is only one device in control at a given time. Control is achieved via software that is not defined in the standard since such software is generally unique to the device. On the other hand, IEEE-583 uses a crate controller that usually consists of an internal microprocessor that virtually eliminates the need for remote intelligence. The controller is programmed in accordance with the protocol and timing conventions of the dataway, which is standard for all crates. Thus, when using IEEE-583 compatible modules, the modules are plugged into the Dataway and when the controller is turned on, the modules are ready to function immediately. This is in contrast to IEEE-488 compatible modules, which require rather complex software to function, but which appear to offer a degree of flexibility not readily achievable with IEEE-583.

In view of the above considerations, it should not be too difficult to select a preferred approach to satisfy a given situation, once the requirements for a data system are defined.

A major question that still exists is: "What can be expected in the interface standards area for the future?" One thing is sure. Interface standards are here to stay, and within a very few years all electronic instruments and peripherals will conform to one or more sets of standards. Exactly which standards will be dominant, or how these standards will compare to existing standards is difficult to predict, but it is highly probable that the three primary standards discussed in Section 3 will form the basis for the interface standards of the future. The real test of any standard is its use and acceptance in the field, and the response of the user will determine the changes that will be required. The various groups that developed the original IEEE standards discussed herein are continuing to work on improving their original outputs, espically in the areas of software. This work will continue for a number of years.

One of the Standards (RS-232-C) has been in existance for over a decade and is closely adhered to by terminal manufacturers. This standard permits a wide flexibility as to how it is used, and in fact two devices using the standard may be hardware compatible and still not be able to communicate because of the differences in how the signals are used internally to the devices. The standard reached its present state of development over a number of years. It is presently in its fourth release (Revision C). New technology may cause another revision, or it may require a completely new standard.

For example, the Electronic Industries Association released a new standard (EIA RS-423) in April 1975 to define the electrical characteristics of unbalanced voltage digital interface circuits. The standard specifies the electrical characteristics of the unbalanced voltage digital interface circuits normally implemented in intergrated circuit technology for data terminal equipment and data communication equipment. This new standard does not specify the complete interface (i.e., protocol, timing, pin assignments, etc.) but it may be used in conjunction with standards such as RS-232-C to completely define an interface. The two standards may continue to be used individually, or they may eventually be combined into one standard.

In view of what is happening in the standards area and the impact that it can have on the cost of NASA data systems, it is strongly recommended that NASA/MSFC and/or a contractor representative become an active participant in the more prominent standards groups such as the IEEE. This participation is particularly important in view of NASA's role as the data collector and as the focal point for data management within the user community. The community represented by NASA in the future comprises the single largest body of users of commercial data systems, and as such they deserve a voice in the definition of standards.

5. BIBLIOGRAPHY

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Horelick, Dale, and Larsen, R.S., CAMAC: A Modular Standard, California IEEE Spectrum, April 1976

Conway, John, What you should know about the 488 and 583 Interface Standards, Massachusetts: Electronic Design News, August 1976

APPENDIX A - STANDARDS ORGANIZATIONS

A number of national and international organizations are actively engaged in formal interface standardization. Their efforts include:

- study of interface techniques adopted by equipment manufacturers;

- analysis of the interface problem in general, with special emphasis on defining the problem and adopting a common language for interface discussion;

- development of requirements for interface standard documentation;

- development of actual interface standards, both concept and documentation;

- promotion of formally adopted interface standards among equipment manufacturers;

- education of design engineers to the application of existing standards.

There is considerable interaction among standards groups. The European organizations have to this point played a leading role in introducing interface standards which have subsequently been adopted by American standards organizations. This transfer is expedited by American participation (through membership) in the various European standards committees. The principal organizations involved in interface standards activity to date are listed below.

- International Organization for Standardization (ISO)

    > 1 rue de Varembe'
    > 1211 Geneva 20

    (publications available from ANSI)

This organization pursues internation interface standardization through its Technical Committee 97, Subcommittee 13 (Interconnection of Equipment), and Subcommittee 6 (Data Communications). ANSI is the United States representative to the ISO, and chairs its data communiations group. The Interconnection of Equipment Subcommittee is chaired by West Germany.

- International Electro-Technical Committee (IEC)
                    1 rue de Varembe'
                    1211 Geneva 20
            (publications available from ANSI)

The organizational arm of the ISO concerned solely with electrical and electronic standards, the IEC was a leader in promulgating what is referred to in this report as IEEE Std. 488-1975. U.S. participation in the IEC is through the United States National Committee to the IEC, a unit supported by ANSI.

- Consultative Committee on International Telegraphy and Telephony (CCITT)
                    1 rue de Varambe'
                    1211 Geneva 20

CCITT is concerned in part with data communications, and is the organization responsible for the CCITT standard, which is the European counterpart of (but not equivalent to) EIA Std. RS-232-C.

- European Society of Nuclear Engineers (ESONE)

                    Contract: B. Rispoli
                    CNEN
                    Viale Regina Margherita 125
                    Roma, Itale

The European organization participating in the development of the CAMAC standard, subsequently designated IEEE Std. 583-1975.

- American National Standards Institute (ANSI)
                    1430 Broadway
                    New York, N.Y. 10018

Pursues interface standards thru its USA Standards Committee for Computers and Information Processing (designated X3), Subcommittee T9 (I/O Interfaces), and Subcommittee J3 (Data Communications). ANSI maintains active liason with most standards organizations in the U.S. and abroad, and is the principal standards organization in this country.

- National Bureau of Standards (NBS)

        Institute for Computer Sciences
            and Technology
        Office of Information Processing Standards
        Washington, D.C.   20234

Pursues interface standards on behalf of the Federal Government through
its Institute for Computer Sciences and Technology, participates in ANSI,
and publishes the Federal Information Processing Standards (FIPS pubs.)
under the provisions of Public Law 89-306 (the Brooks Bill). Interface
standards are classified as Category 1 (Hardware), Subcategory (b)
(Codes and Media), Subcategory (c) (Transmission), and Subcategory (d)
(Interface).

- Electronics Industries Association (EIA)

        Engineering Department
        2001 Eye St. N/W
        Washington, D.C.   20006

    Concerned exclusively with electrical and electronic standards,
this organization is best known in the interface area for EIA Std. RS-
232-C dealing with data terminal to data communications equipment inter-
connection.

- Institute of Electrical and Electronic Engineers (IEEE)

            345 East 47th Street
            New York, N.Y.   10017

    The professional organization for electrical engineers in the
United States, the IEEE publishes standards in its areas of interest. Two
of these (IEEE Std. 488 and 583) are discussed subsequently.

- Nuclear Instrumentation and Measurement Committee (NIM)

                Contact: Louise Costrell
                Center of Radiation Research
                National Bureau of Standards
                Washington, D.C.   20234

A committee of the U.S. Energy Research and Development Admini-
istration (ERDA) whose work in conjunction with the European Society
of Nuclear Engineers (ESONE) led to the development and adoption of IEEE
Std. 583, discussed subsequently.

- Computer and Business Equipment Manufacturer's Association
  (CBEMA)

  1828 L Street N/W

  Washington, D.C. 20036

The U.S. Association of Manufacturers of Computers and Computer
Peripheral Equipment participates in all aspects of interface standardi-
zation in this country through the various Institutes.

- Department of Defense

  Naval Publications and Forms Center

  (NPFC105)

  5801 Tabor Avenue

  Philadelphia, PA 19120   .

  (documents available from Superintendent of

  Documents, U.S. Government Printing Office,

  Washington, D.C. 19120)

Publishes MIL Std. 188C, which is the military counterpart to EIA
Std. RS-232-C, for data terminal to communications terminal interconnection.

APPENDIX B - HANDSHAKE PROCESS TIMING SEQUENCE

B1. General Comments

Each data byte transferred by the interface system uses the handshake process to exchange data between source and acceptor. Typically, the source is a talker and the acceptor a listener.

Fig B1 illustrates the handshake process by indicating the actual waveforms on the DAV, NRFD, and NDAC signal lines. The NRFD and NDAC signals each represent composite waveforms resulting from two or more listeners accepting the same data byte at slightly different times due to variations in the transmission path length and different response rates (delays) to accept and process the data byte.

Fig B2 represents the same sequence of events, in flow chart form, to transfer a data byte between source and acceptor.

The annotation numbers on the flow chart and the timing sequence diagram refer to the same event on the list of events.

B2. List of Events for Handshake Process

(1) — Source initializes DAV to high (H) (data not valid).

(2) — Acceptors initialize NRFD to low (L) (none are ready for data), and set NDAC to low (L) (none have accepted the data).

(3) t_{-2} Source checks for error condition (both NRFD and NDAC high), then sets data byte on DIO lines.

(4) $t_{-2} \rightarrow t_0$ Source delays to allow data to settle on DIO lines.

(5) t_{-1} Acceptors have all indicated readiness to accept first data byte; NRFD lines goes high.

(6) t_0 Source, upon sensing NRFD high, sets DAV low to indicate that data on DIO lines is settled and valid.
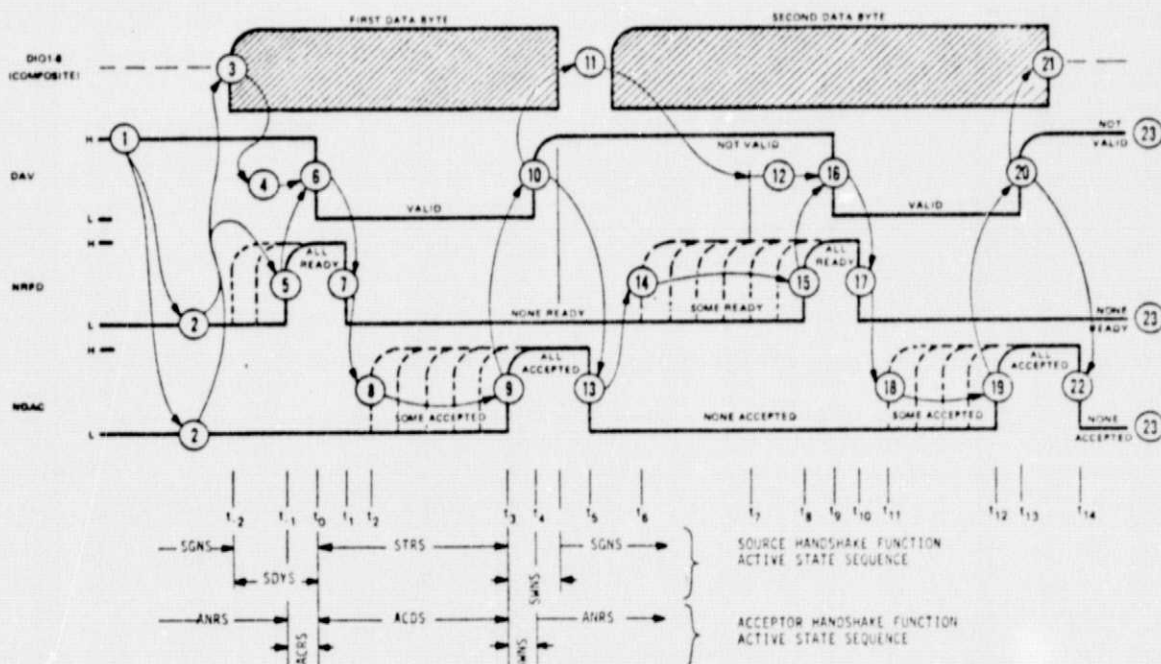
Fig B1
Signal Line Timing Sequence for One Talker and Multiple Listeners
Using Handshake Process
(See Fig B2 and List of Events) $H \geq +2.0$ V; $L \leq +0.8$ V
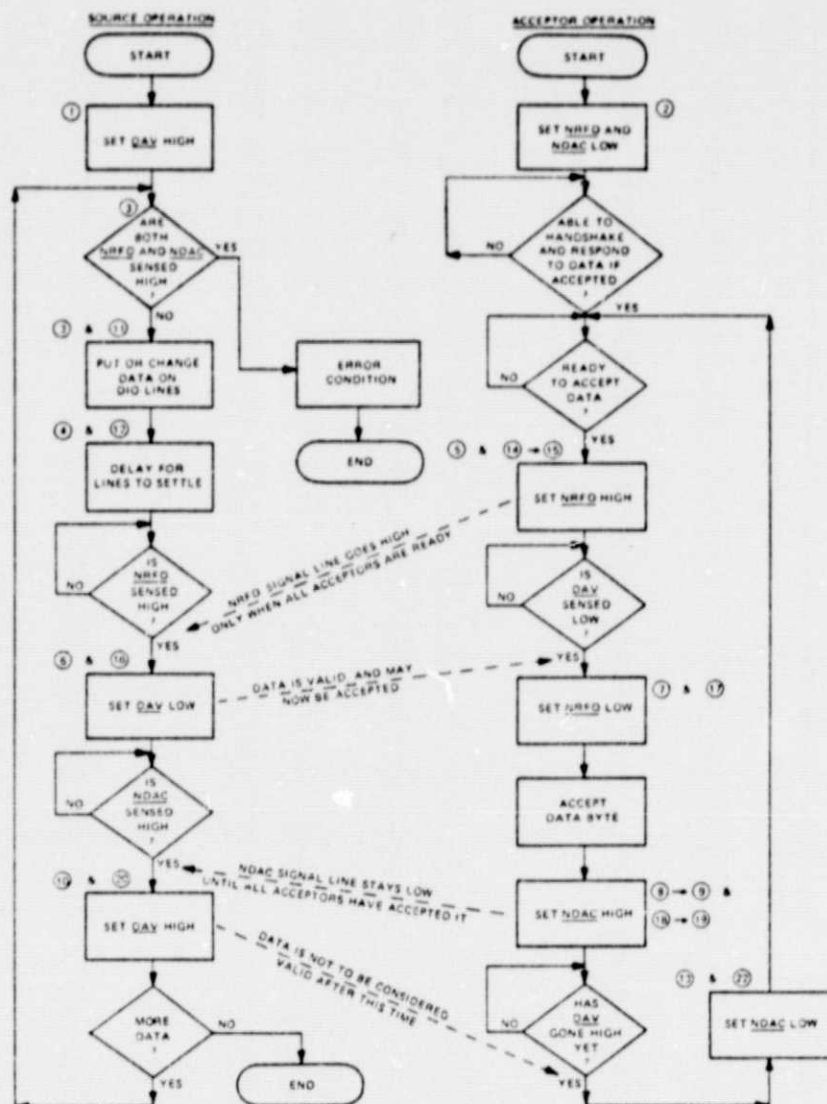
Fig B2
Logical Flow of Events for Source and Acceptor When
Transferring Data Using Handshake Process
(See List of Events) (This flow diagram is not intended
to represent the only method of implementing an acceptor
handshake. See Section 2.4.5, paragraph three)

(7) t_1 First acceptor sets NRFD low to indicate that it is no longer ready, then accepts the data. Other acceptors follow at their own rates.

(8) t_2 First acceptor sets NDAC high to indicate that it has accepted the data. (NDAC remains low

due to other acceptors driving NDAC low).

(9) t_3 Last acceptor sets NDAC high to indicate that it has accepted the data; all have now accepted and the NDAC line goes high.

(10) t_4 Source, having sensed that NDAC is high, sets DAV high.

This indicates to the acceptors that data on the DIO lines must now be considered not valid.

(11) $t_4 - t_7$ Source changes data on the DIO lines.

(12) $t_7 - t_9$ Source delays to allow data to settle on DIO lines.

(13) t_5 Acceptors, upon sensing DAV high (at 10) set NDAC low in preparation for next cycle. NDAC line goes low as the first acceptor sets the line low.

(14) t_6 First acceptor indicates that it is ready for the next data byte by setting NRFD high. (NRFD remains low due to other acceptors driving NRFD low).

(15) t_8 Last acceptor indicates that it is ready for the next data byte by setting NRFD high; NRFD signal line goes high.

(16) t_9 Source, upon sensing NRFD high, sets DAV low to indicate

that data on DIO lines is settled and valid.

(17) t_{10} First acceptor sets NRFD low to indicate that it is no longer ready, then accepts the data.

(18) t_{11} First acceptor sets NDAC high to indicate that it has accepted the data [as in (8)].

(19) t_{12} Last acceptor sets NDAC high to indicate that it has accepted the data [as in (9)].

(20) t_{13} Source, having sensed that NDAC is high, sets DAV high [as in (10)].

(21) — Source removes data byte from DIO signal lines after setting DAV high.

(22) t_{14} Acceptors, upon sensing DAV high, set NDAC low in preparation for next cycle.

(23) — Note that all three handshake lines are at their initialized states [as in (1) and (2)].