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(NASA-CR-149810) LONG LIFE TESTING OF SPARE MARINER VENUS '67 HARDWARE Final Report (Boeing Co., Kent, Wash.) 55 p HC A04/MF A01 CSCL 22B

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DOCUMENT NO. D180-19861-1 MODEL

TITLE LONG LIFE TESTING

OF

SPARE MARINER VENUS '67 HARDWARE

FINAL REPORT

ORIGINAL RELEASE DATE

ISSUE NO TO

ADDITIONAL LIMITATIONS IMPOSED ON THIS DOCUMENT WILL BE FOUND ON A SEPARATE LIMITATIONS PAGE

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ABSTRACT

This report summarizes the results of the 76 months of continuous operation, starting in March 1970, under simulated space environment of the Electrical Power Conditioning Electronics (PCE) for the Mariner Venus '67 Spacecraft. This power subsystem had evolved from the original Mariner 62 (M62) design and was successfully flown by the Jet Propulsion Laboratory (JPL) on the Mariner V (MV '67) Spacecraft. Since then the subsystem design has undergone further development culminating with the power subsystem used on the Viking '76 Mars Orbiter. This work was performed because the original Mariner power system had proved to be so flexible and could still be used as the basis for future spacecraft power subsystem designs, including those for long duration missions.

The objective of this program was to verify the long life capability of the equipment to perform its power control and conditioning functions in a space environment. Spare flight hardware was operated in vacuum at temperatures simulating spacecraft environmental conditions while performance was monitored using JPL Operational Support Equipment.

Weekly functional tests supplemented by daily monitoring verified that the PCE equipment can perform to its intended functions for at least six years without apparent performance degradation. Since there were no recurring failures and performance throughout the test period was very stable, there are no circuit or redundancy improvements to be considered.

When the equipment was examined after the test was completed, there was no evidence of any physical damage nor any difficulty in disconnecting the wiring connectors.

The faultless performance of the MV '67 Power Conditioning Electronics throughout six years of continuous operation in a simulated space environment confirms the basic soundness of the original design and indicates that with adequate derating and conservative design it is possible to achieve design lives of at least six years.

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, under JPL Contract 952600.

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1.0 INTRODUCTION

1.1 General

This document reports the results of long life testing of spare Mariner Venus'67 electrical power conditioning equipment in a space simulated environment. The test was started in March 1970 and was completed in May 1976. The equipment was tested at the Boeing Space Center located at Kent, Washington.

The equipment tested is identified as Power Conditioning Electronics (PCE). Its major components consist of the Main Booster Regulator, the Maneuver Booster Regulator, the Battery Charger, the Power Synchronizer, the Main 2400 Hz Inverter, the Maneuver 2400 Hz Inverter and the 3-Phase 400 Hz Inverter. These components are interconnected as shown in the power subsystem block diagram (Figure 1.1-1).

Figure 1.1-2 shows the functional flow diagram which was followed for the equipment setup and test. The JPL-furnished PCE was checked out using the JPL-furnished Operational Support Equipment (OSE) supplemented with Boeing-supplied instrumentation. After installation of the PCE in the vacuum chamber, complete functional tests were performed both at room ambient conditions and at a vacuum of 1×10^{-4} torr with temperature at 80°F. The equipment was then put into the normal life test mode of operation with temperature stepped with time as shown in Figure 1.1-3. Monitoring was done with the OSE in automatic test mode with daily manual checks and weekly abbreviated functional tests. Procedures were established to evaluate and repair failures or degradation as indicated in Figure 1.1-2. At completion of the life test, complete functional testing of the PCE was performed under vacuum conditions and at room ambient conditions, followed by a visual inspection of the PCE.

1.2 Test Hardware

The function of the MV '67 power subsystem is to generate, store, and convert all electrical power necessary for operation of the spacecraft. In order to perform this function, suitable switching, control, energy conversion, and power conditioning functions are provided.

Primary spacecraft power is provided by four photovoltaic solar panels. These panels were not included in the long life test; they were simulated by laboratory power supplies. Energy storage in a spacecraft is provided by a rechargeable battery but the battery was not included in the long life test either. Relays are provided to switch operating modes, including battery charging, booster switching, and inverter switching. The power synchronizer supplies frequency synchronization signals to the power inverters. There are two booster regulators which boost the bus voltage to a regulated 52 volts D.C. The main

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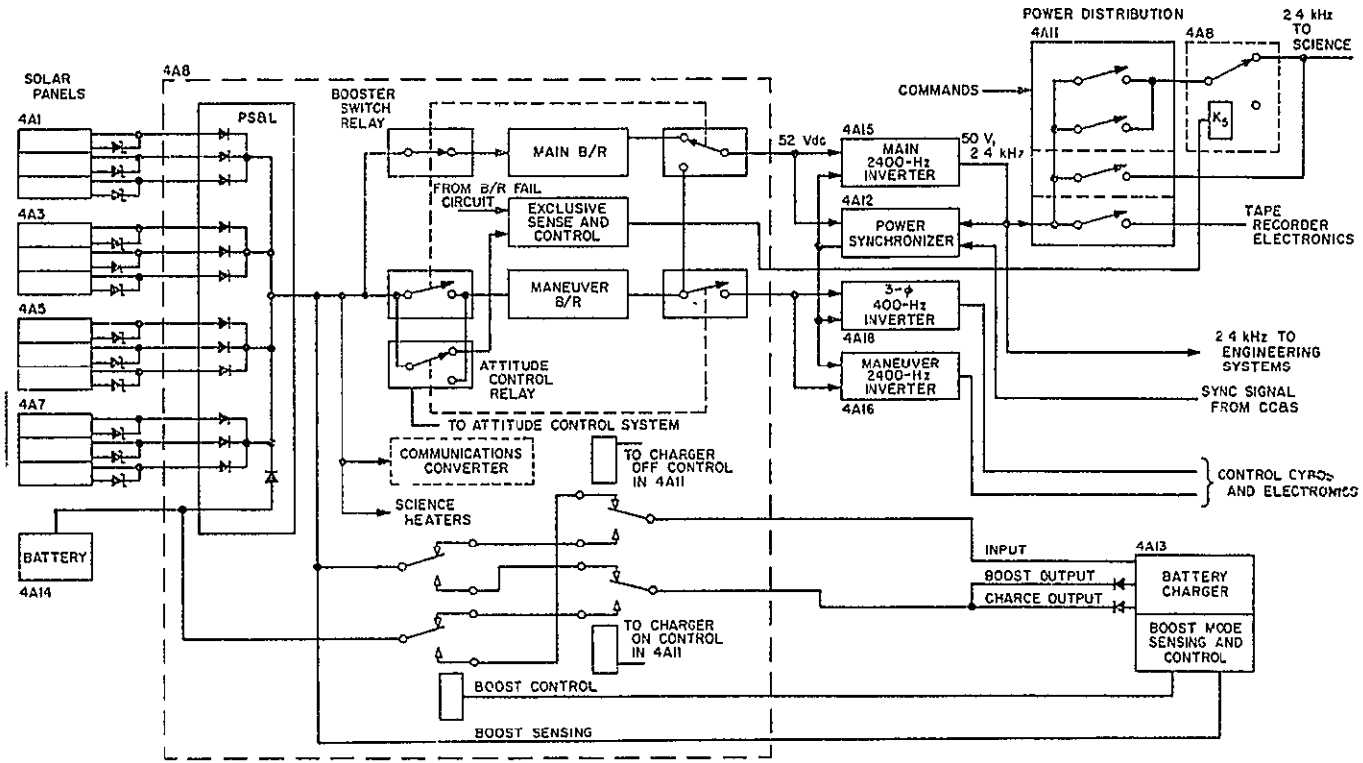

FIGURE 1.1-1

MARINER VENUS '67 POWER SUBSYSTEM

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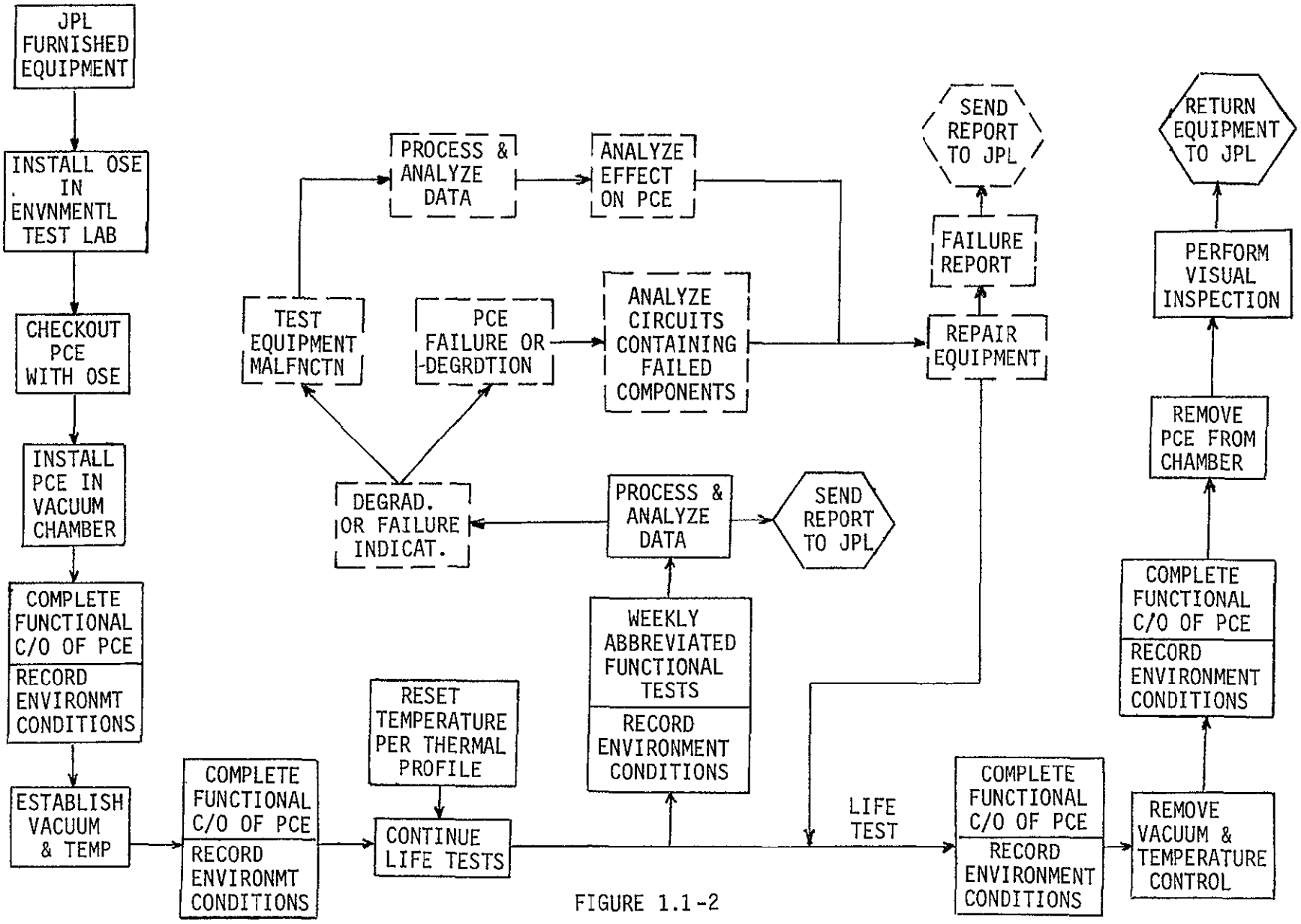

FIGURE 1.1-2

PROGRAM FUNCTIONAL FLOW DIAGRAM

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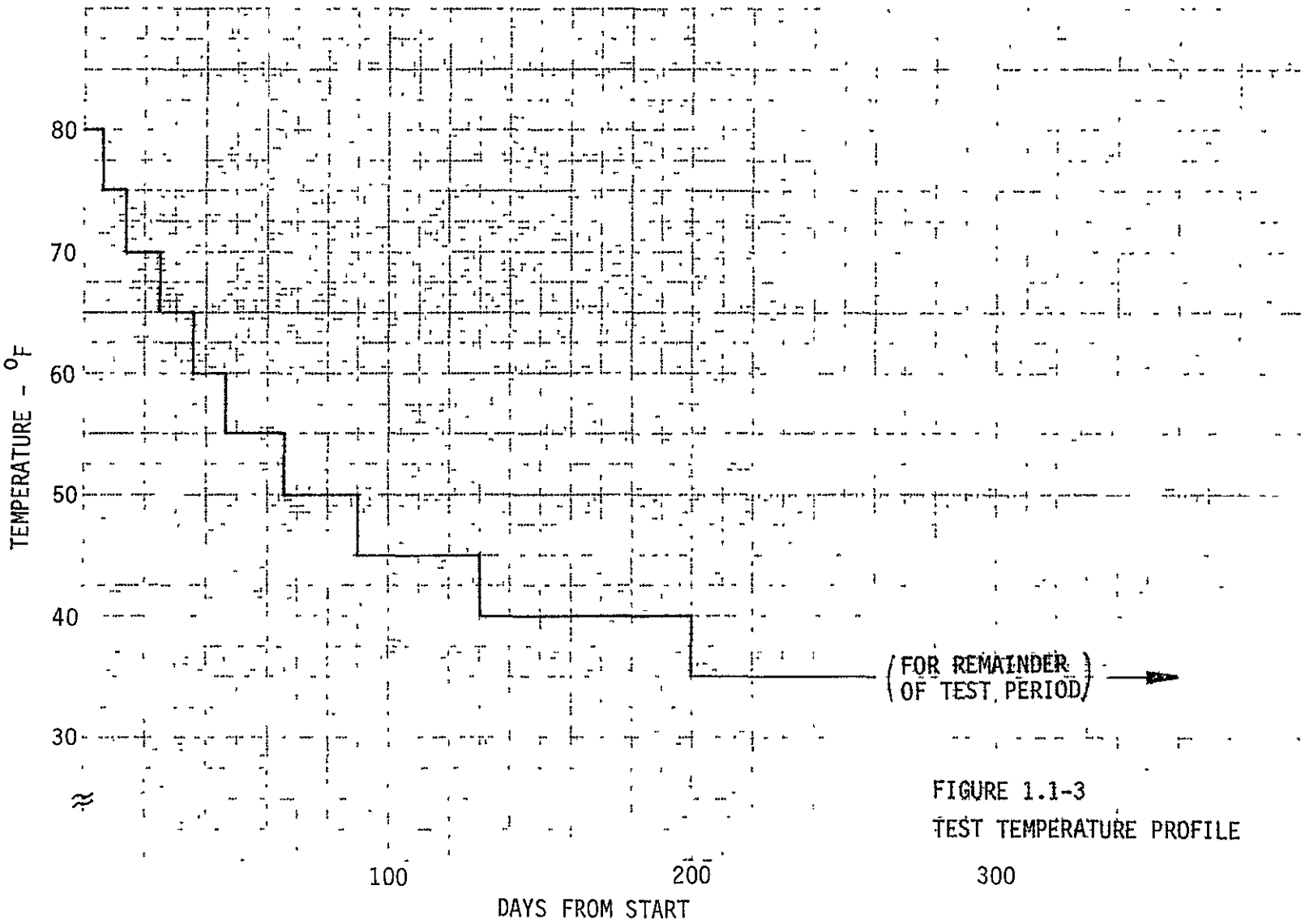

FIGURE 1.1-3
TEST TEMPERATURE PROFILE

booster handles the cruise power demands, and the maneuver booster handles the additional power demands during a maneuver. Error detection circuitry will replace the main booster by the maneuver booster if the main booster fails.

There are two modes of operation of the battery charger. In the first, the battery is charged during periods of sun orientation. In the second, it boosts the system voltage to remove the battery from the sharing mode of operation.

The main inverter supplies 50 volts, 2400 Hz power to spacecraft loads. The maneuver inverter supplies the same kind of power to the attitude control gyro electronics and the autopilot. These inverters will free-run at 2400 Hz in the absence of a sync signal.

The three phase 400 Hz inverter supplies 27 volt power to the attitude control gyro spin motors. This inverter will not free-run in the absence of the sync signal.

The PCE is contained in two cases as shown in Figure 1.2-1, and is shown in the space environment chamber in Figure 1.2-2.

1.3 Test Procedure

The test was conducted in accordance with the procedures of Boeing document T2-121715-1, "Long Term Life Test of Spare Mariner Venus '67 Space Flight Hardware - Test Procedures." Periodic functional tests were performed while the equipment was operated continuously. The complete functional test was performed in a room ambient temperature prior to beginning the life test, after establishing the vacuum, and at the end of life test prior to and immediately after removing the vacuum. An abbreviated functional test was performed on a weekly basis to confirm proper operation in all major operating modes. Daily monitoring verified proper equipment operation by printing a set of data. The results of the weekly and daily tests have been reported to JPL in monthly reports during the entire program. Test data has been submitted to JPL at two month intervals. The data submitted dated 25 June 1976 included the end of life test complete functional test data.

The Power Conditioning Electronic equipment was installed in the space simulation chamber as shown in Figure 1.3-1. Its performance was monitored by the JPL supplied Operational Support Equipment shown in Figure 1.3-2.

Test conditions include a vacuum environment of at least 1×10^{-4} torr and a temperature profile varying from 80°F at start of test to 35°F from 200 days to end of test.

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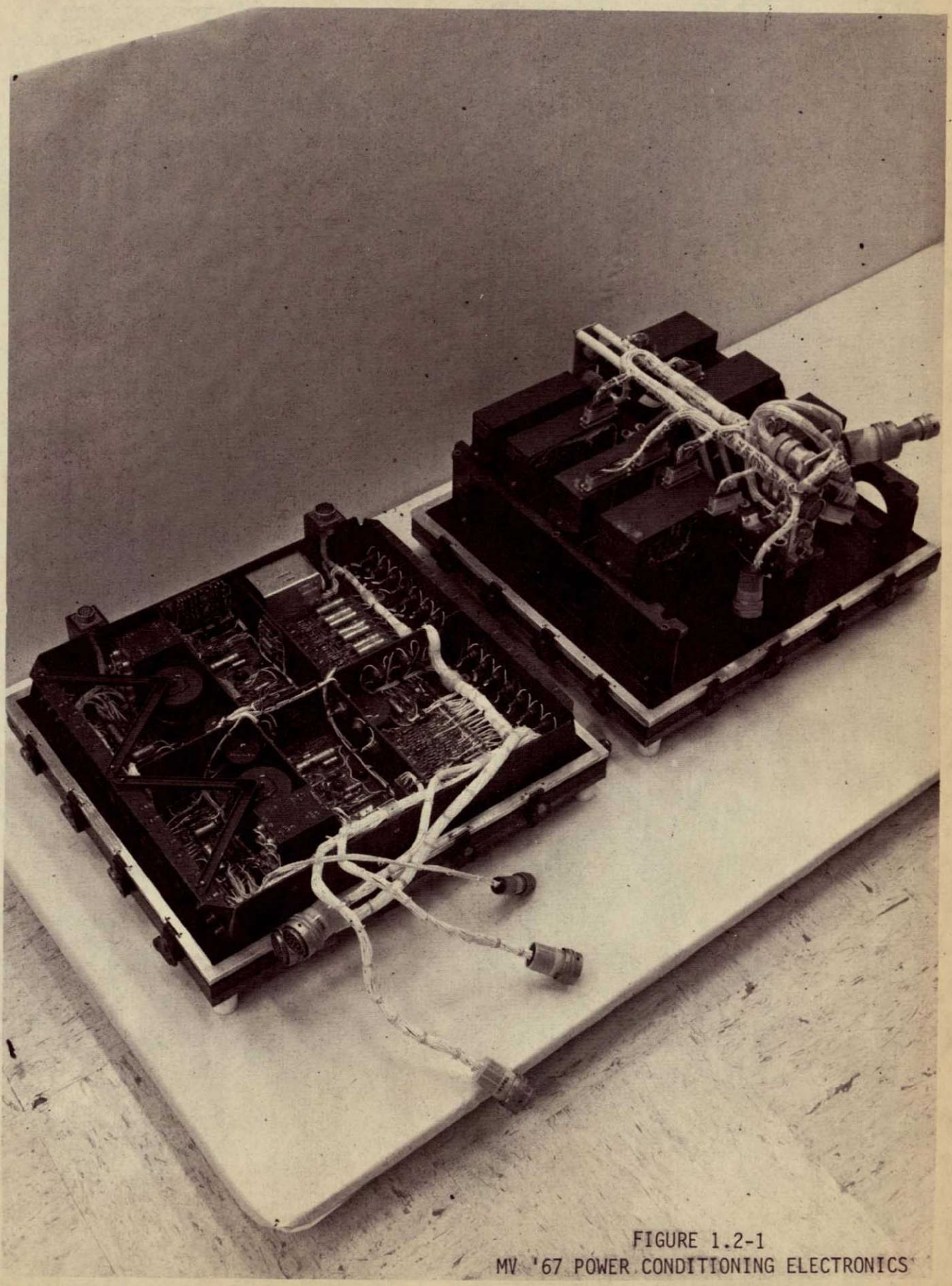

FIGURE 1.2-1
MV '67 POWER CONDITIONING ELECTRONICS

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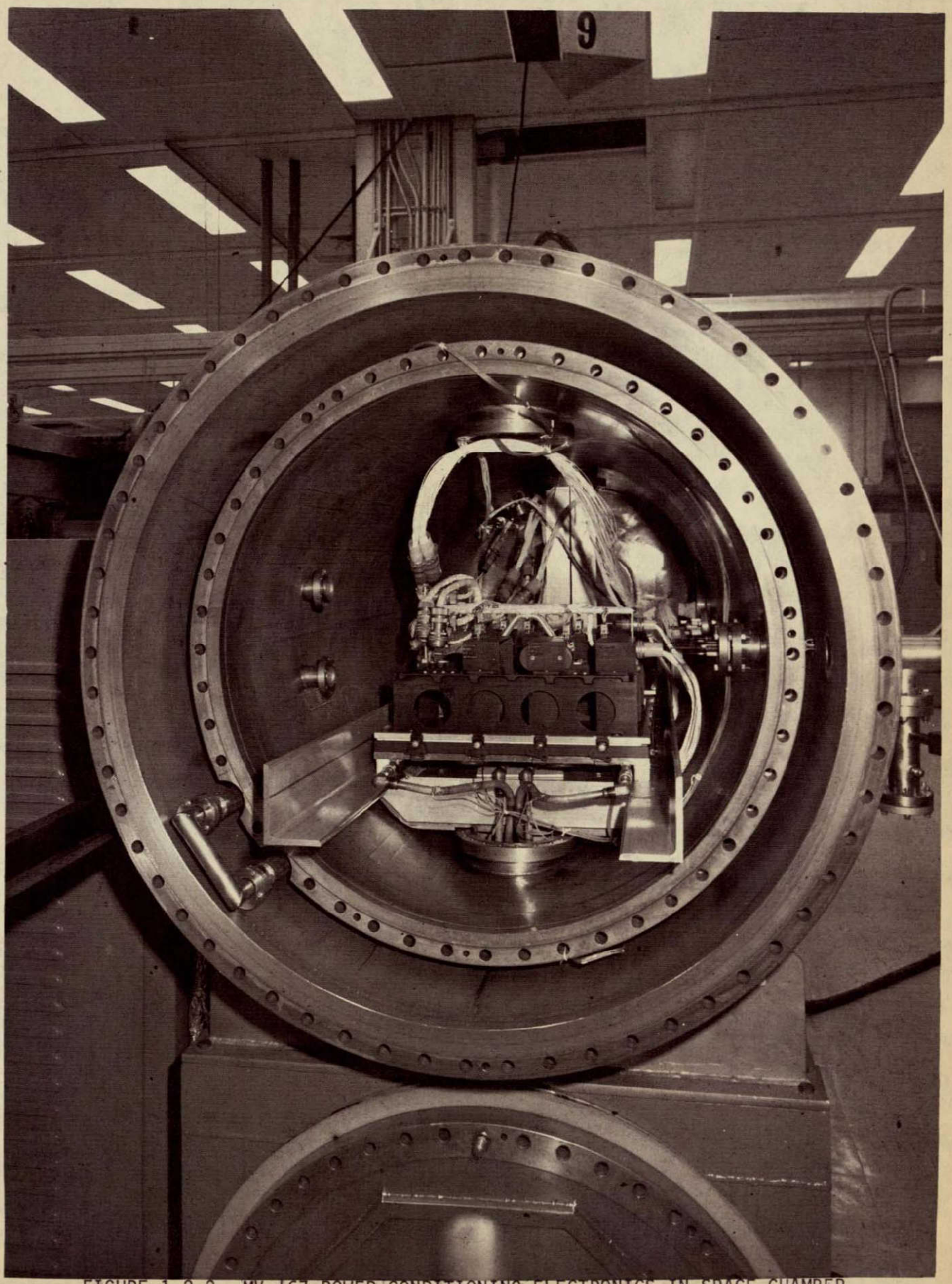

FIGURE 1.2-2 MV '67 POWER CONDITIONING ELECTRONICS IN SPACE CHAMBER

FIGURE 1.3-1
MV '67 ELECTRONICS BEING INSTALLED IN THE SPACE CHAMBER

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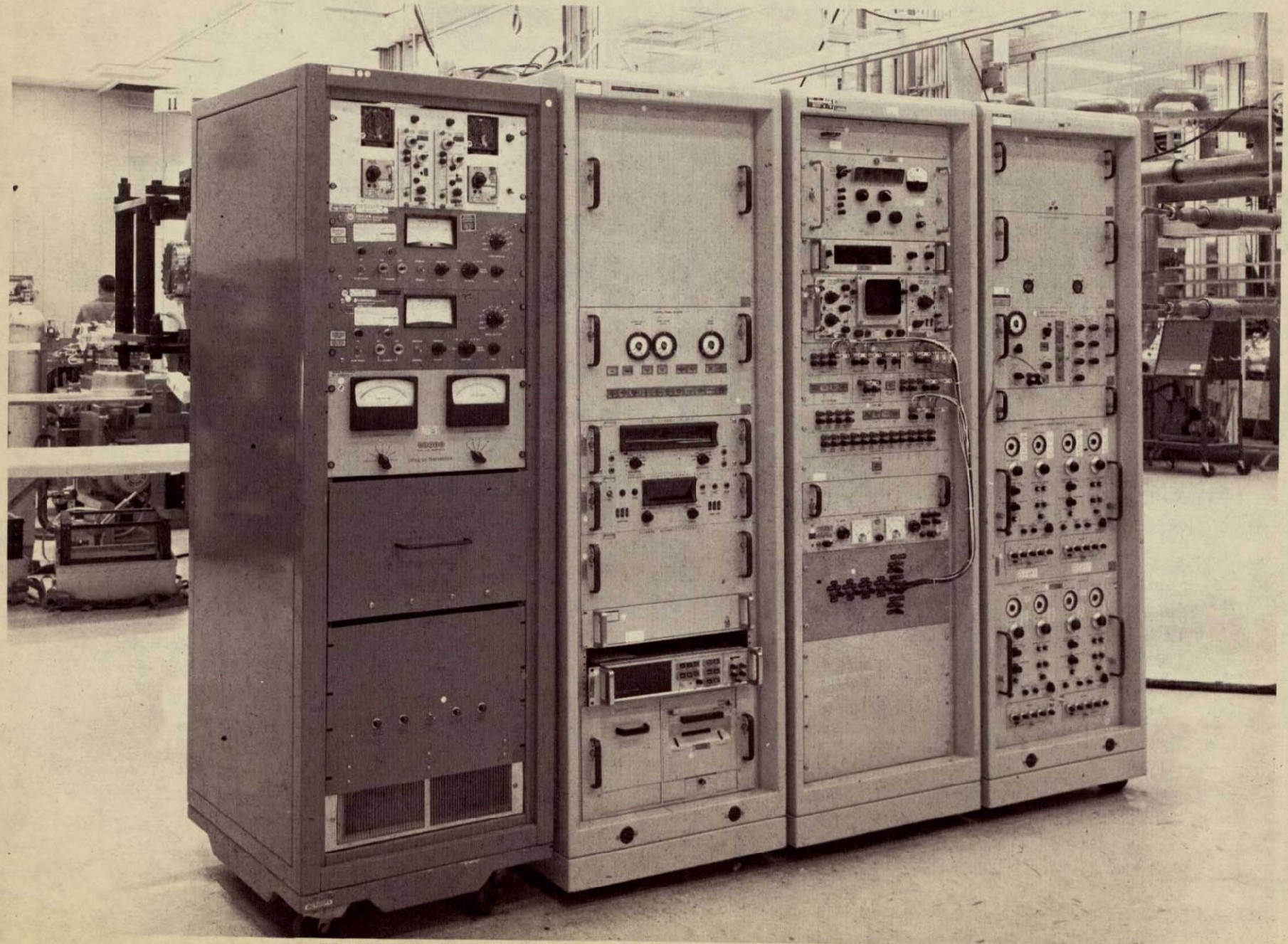

FIGURE 1.3-2 MV '67 PCE OPERATIONAL SUPPORT EQUIPMENT

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2.0 TEST RESULTS

Main booster regulator, main inverter, and 3-phase inverter outputs have been plotted and reported in each monthly report submitted during the program. The graphs are given in Figures 2.0-1 through 2.0-7.

There is no long term degradation evident in these graphs. The output voltages and currents remained within narrow limits inside specification tolerances except for infrequent errors due to instrumentation failures. Output limits and specification tolerances are compared in Table 2.0-1.

	Measured Range		Specification Tolerance	
	Voltage	Current in Amperes	Voltage	Current in Amperes
Main Booster Regulator	52.1±0.1	2.26±0.02	52±.75	2.26±1%
Main Inverter	48.1±0.1	1.96±0.02	$48^{+.5}_{-2}$	2.0±0.1
3-Phase Inverter	27.9±0.1	.441±0.002	27.8±.3	.44±1%

Table 2.0-1: Subassembly Outputs

The plots of daily observations also show no long term degradation and no variation which could be attributed to the temperature profile.

Main booster and main inverter parameters for the first 20 days of testing are plotted in Figures 2.0-10 and 2.0-11. Comparison of output currents and voltages on these graphs with the same parameters in Figures 2.0-12 and 2.0-13 for the last two weeks of testing shows very little variation.

Output voltages and currents for the main subassemblies of the PCE at the beginning of life test and at the end of life test are compared in Table 2.0-2.

	End of Test	Beginning of Test
Boost Regulator	52.175 to 52.191V 2.263 to 2.273A	51.79 to 52.19V 2.200 to 2.280
Main 2400 Hz Inverter	48.333 to 48.384V 1.951 to 1.964A	47.75 to 48.31V 1.944 to 1.962A
400 Hz, 3-Phase Inverter	27.785 to 27.964V .4396 to .4414A	27.81 to 27.99V .4388 to .4420A

Table 2.0-2: Test Parameter Comparisons

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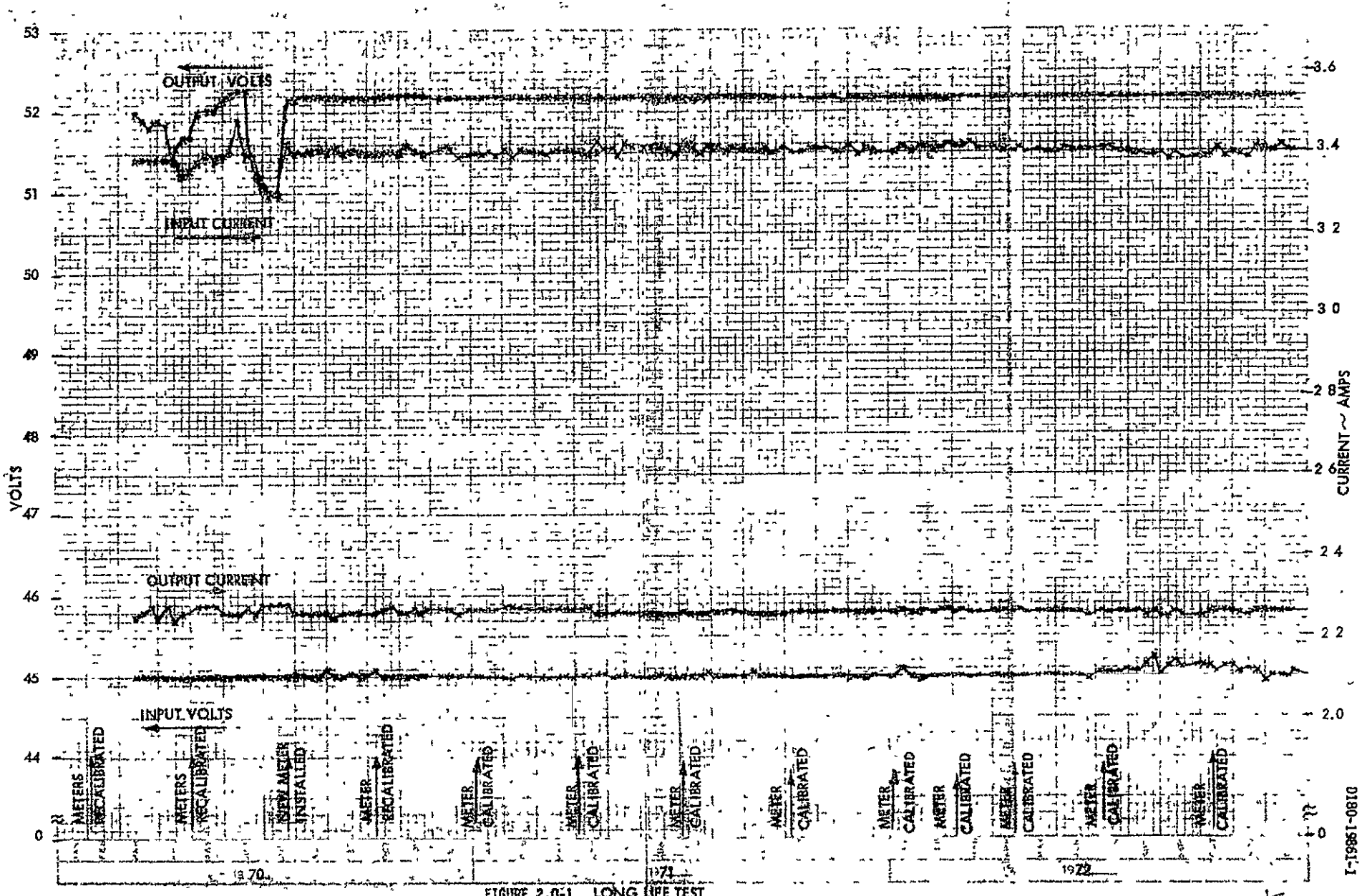

FIGURE 2.0-1 LONG LIFE TEST
MAIN BOOSTER REGULATOR

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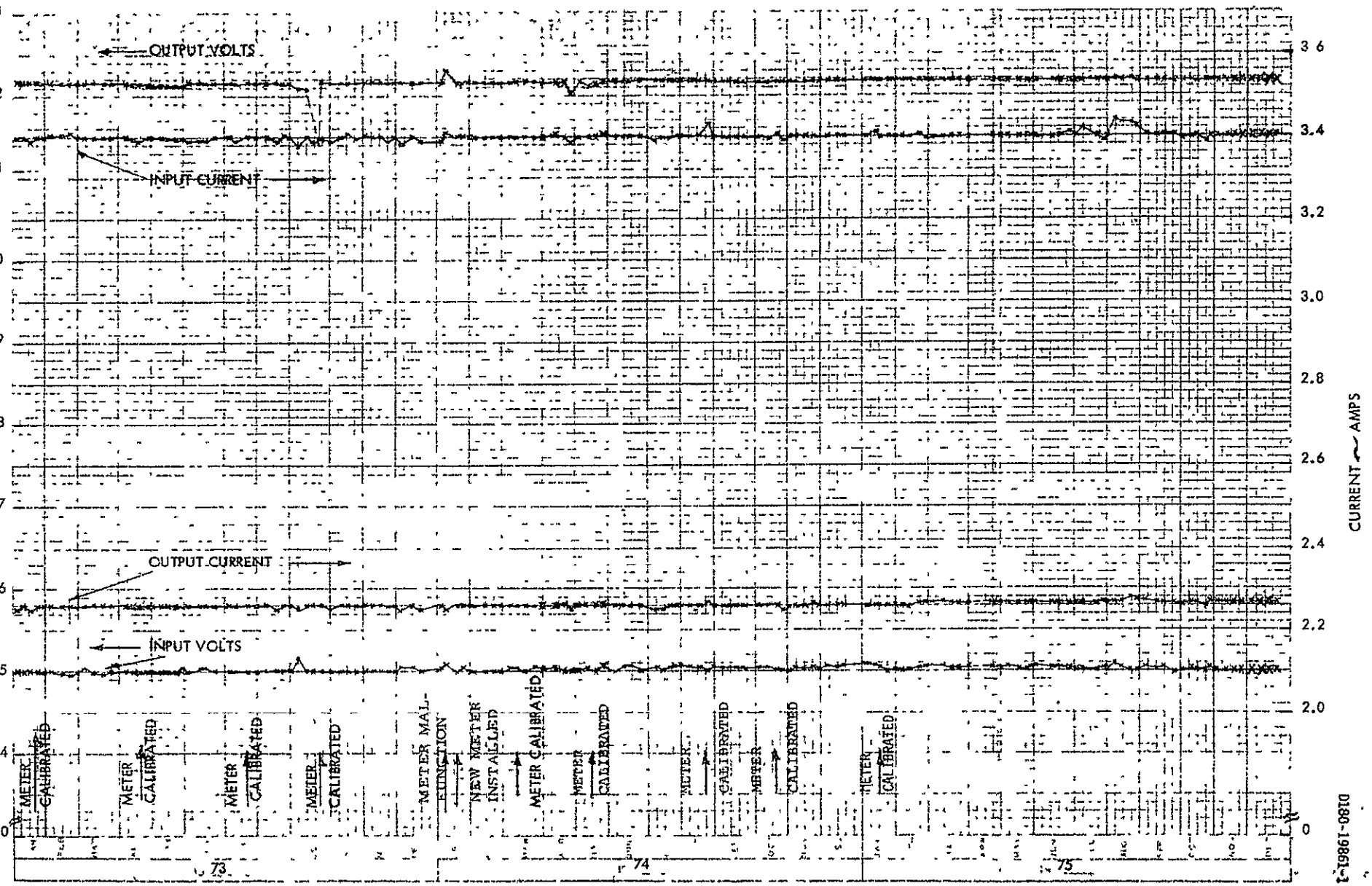

FIGURE 2 0-2 · LONG LIFE TEST
MAIN BOOSTER REGULATOR

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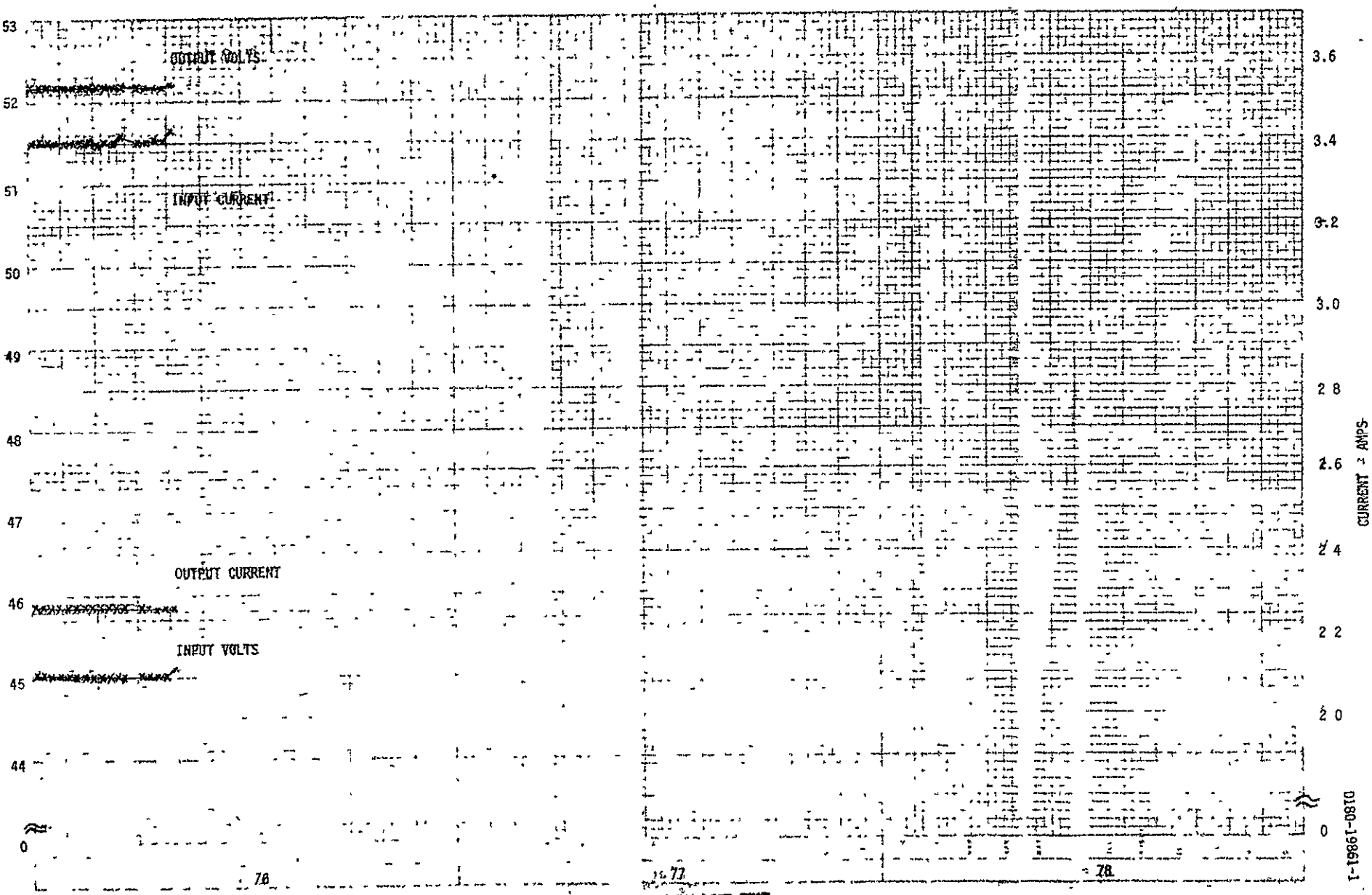

FIGURE 2.0-3 LONG LIFE TEST
MAIN BOOST REGULATOR

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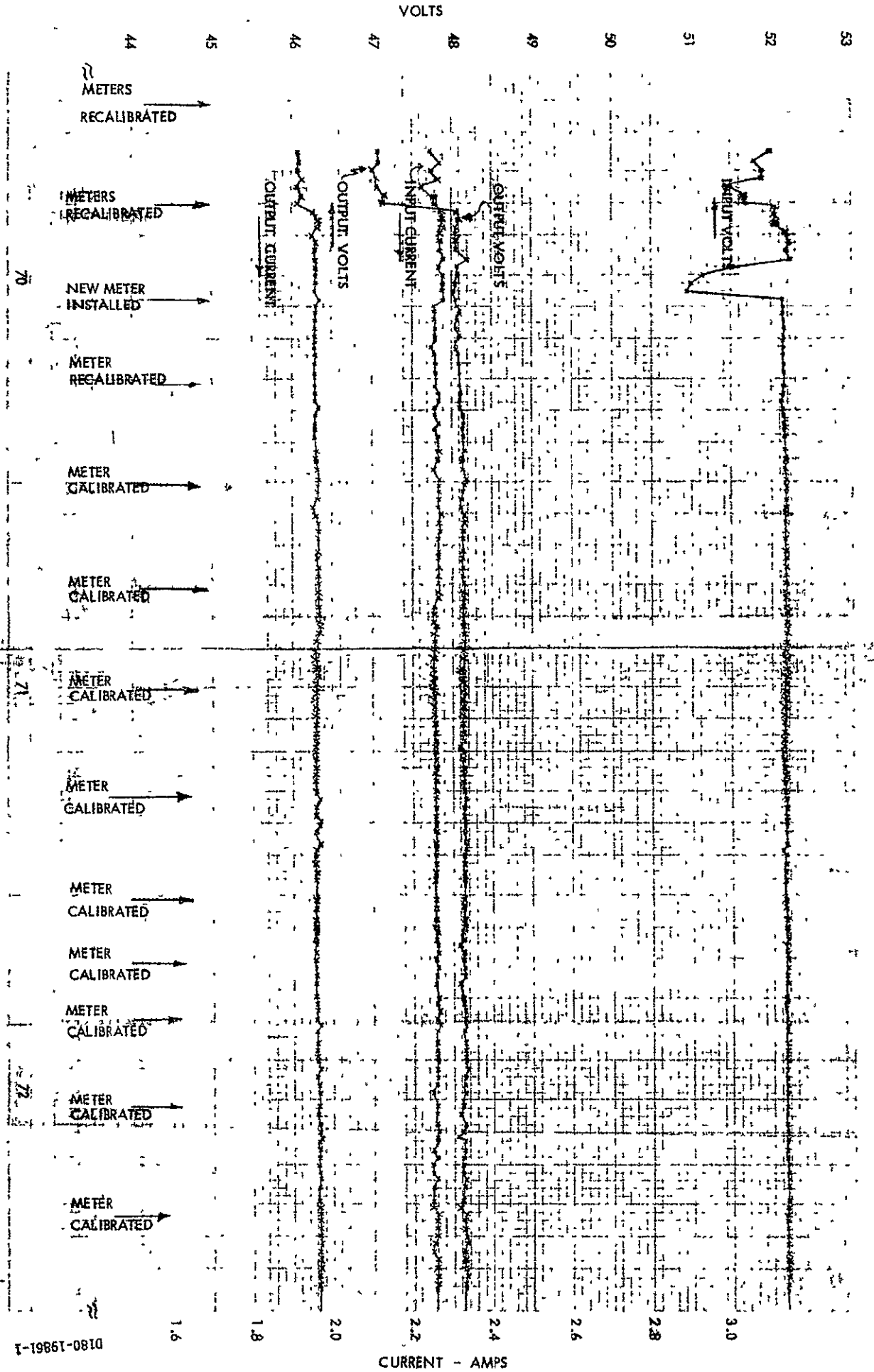

FIGURE 2.0-4 - LONG LIFE TEST -

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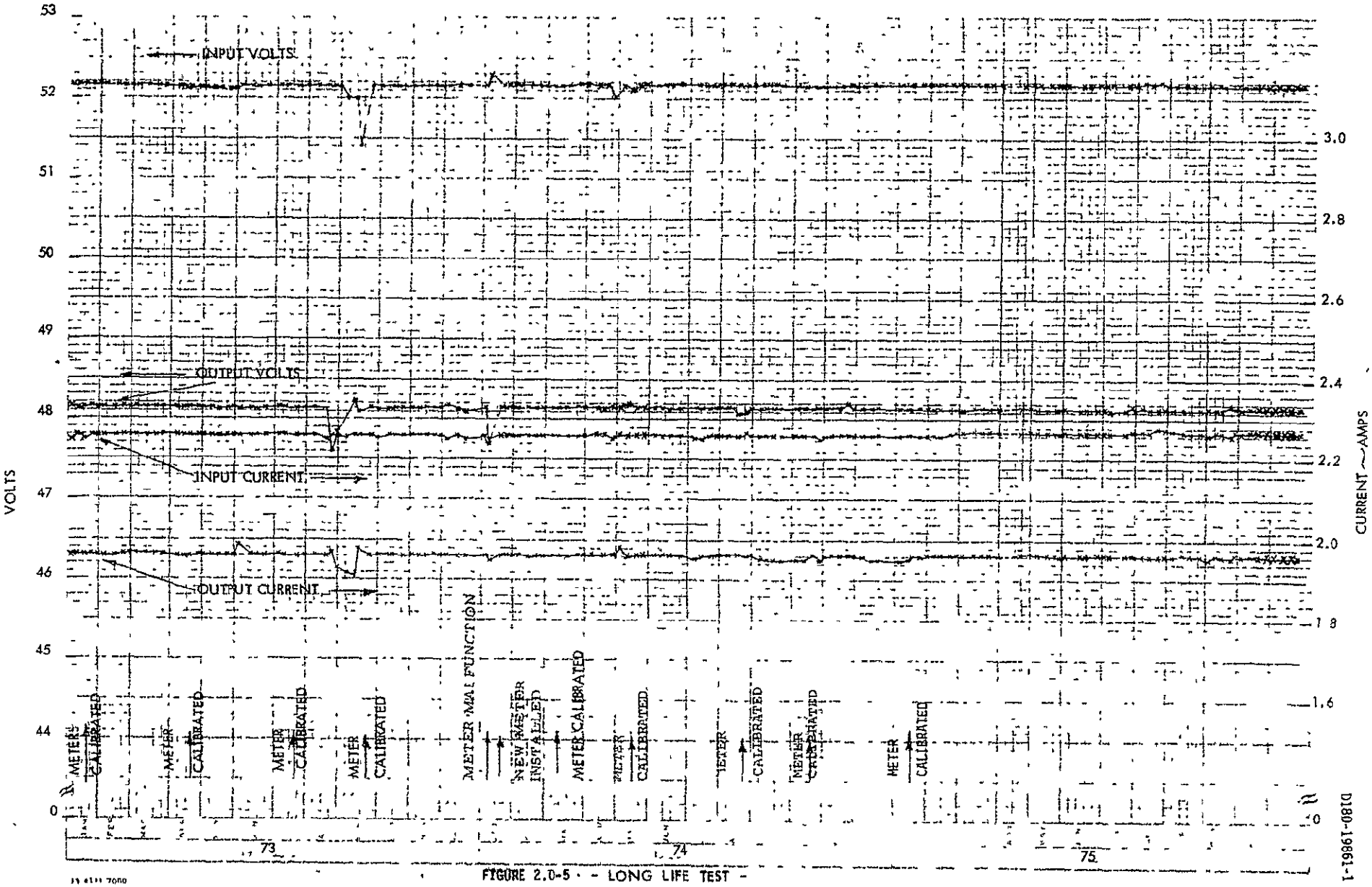

FIGURE 2.0-5 - - LONG LIFE TEST - MAIN INVERTER

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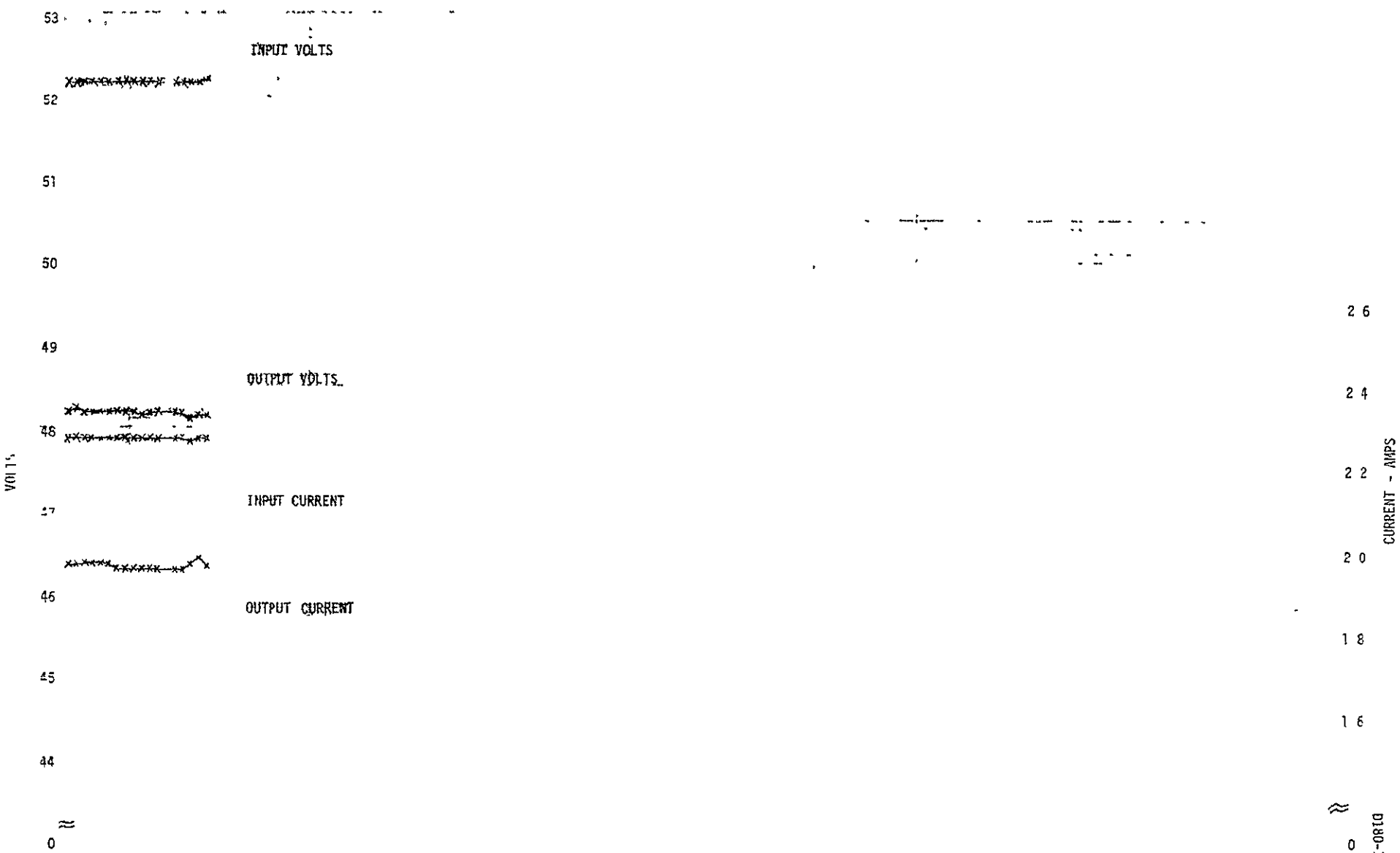

FIGURE 2 0-6 LONG LIFE TEST
MAIN INVERTER

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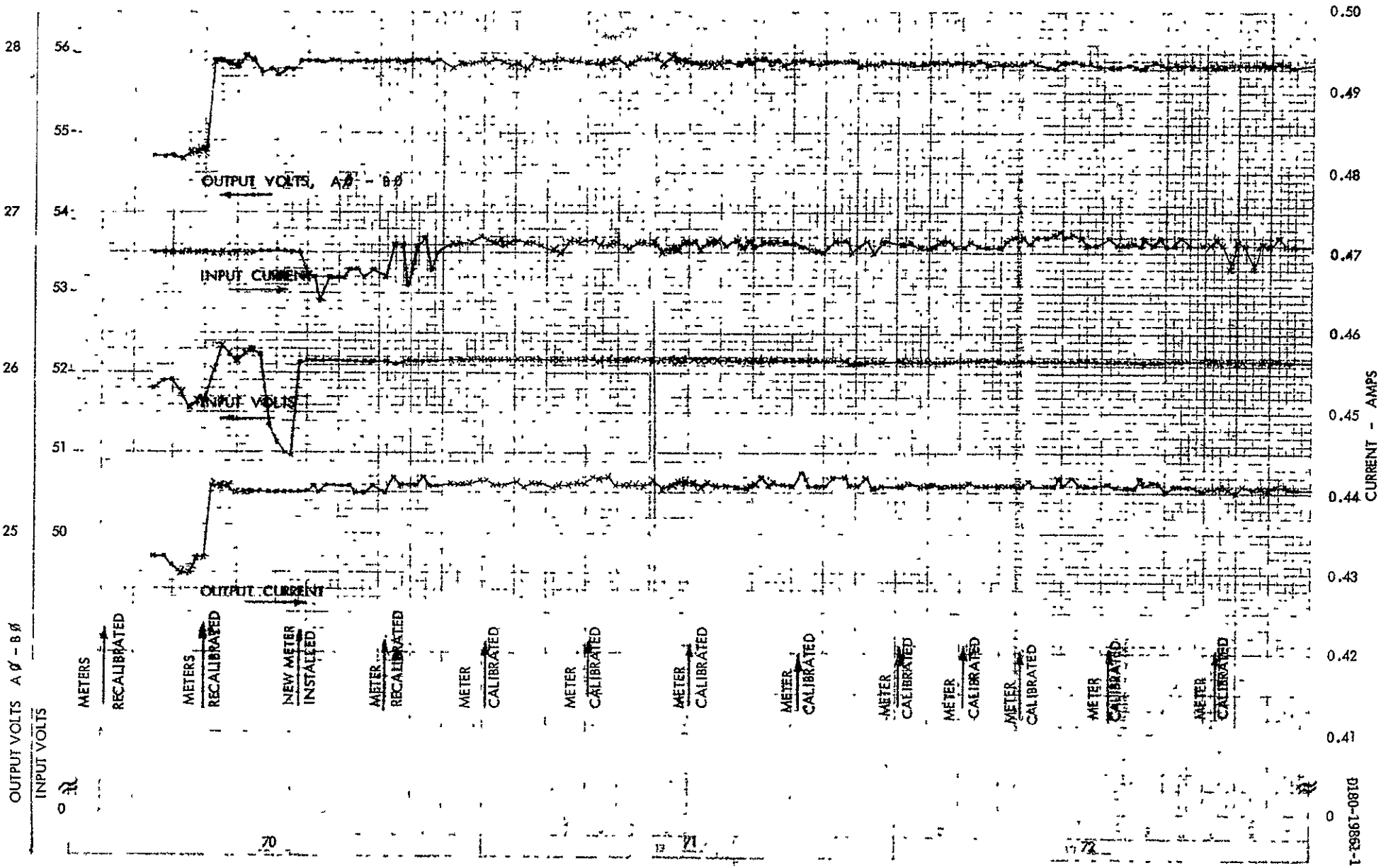

FIGURE 2 0-7: - LONG LIFE TEST -

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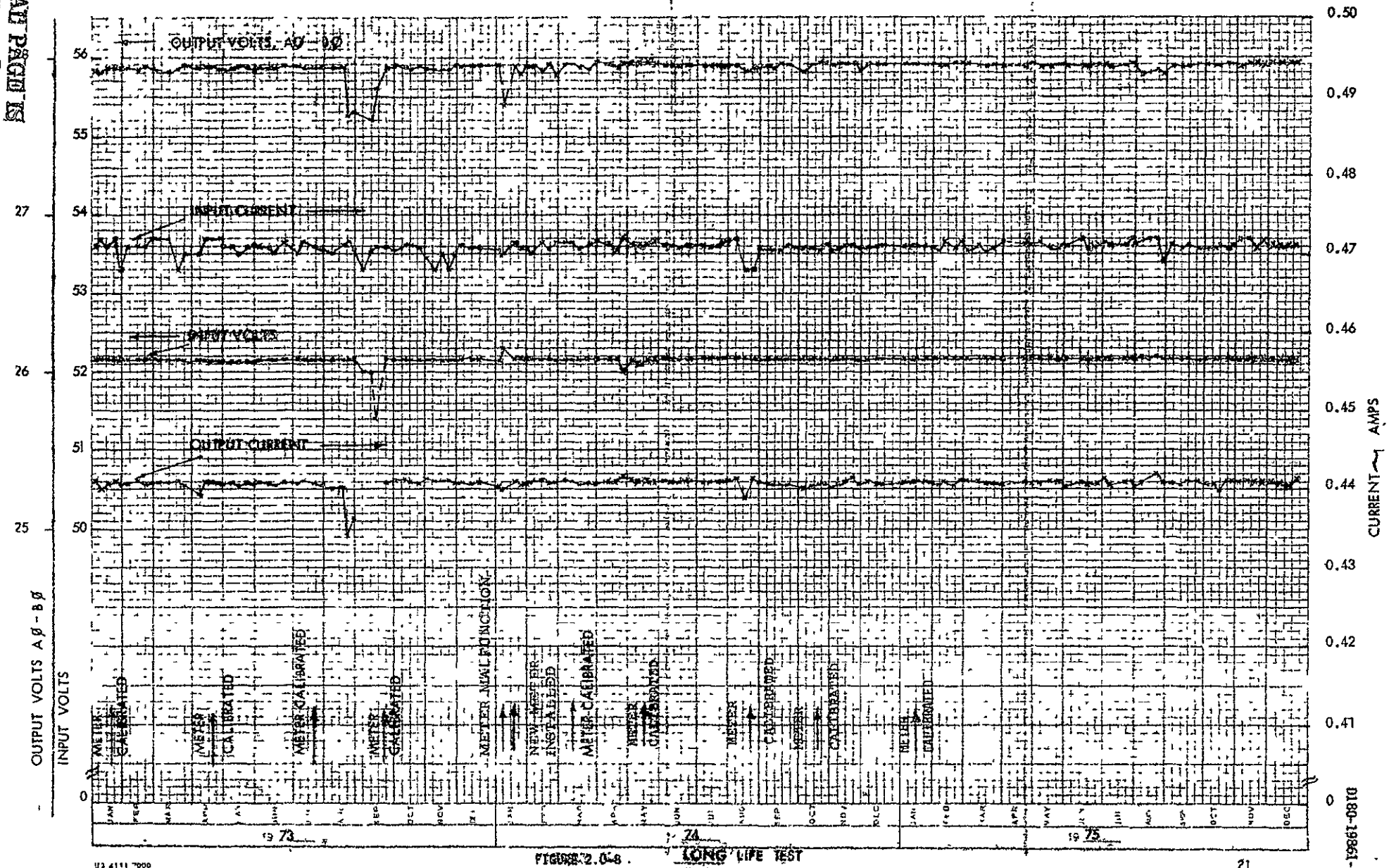

FIGURE 2.0-8. LONG LIFE TEST
400 Hz. 3 Ø INVERTER

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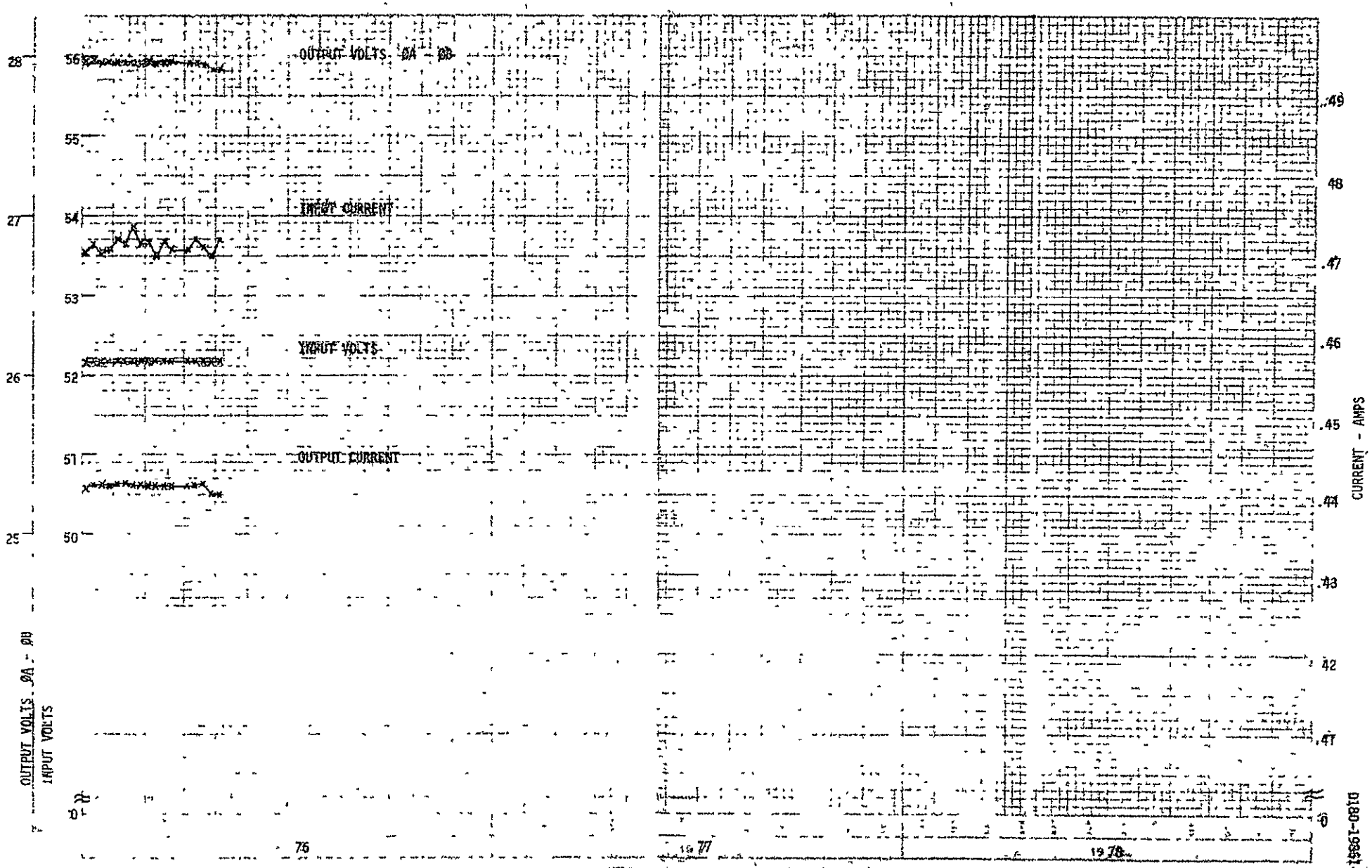

FIGURE 2.0-9 LONG LIFE TEST
400 Hz 3 Ø INVERTER

K+E 12 X 20 TO THE INCH 46 1970
7 X 10 INCHES MADE IN U.S.A.
KEUFFEL & ESSER CO.

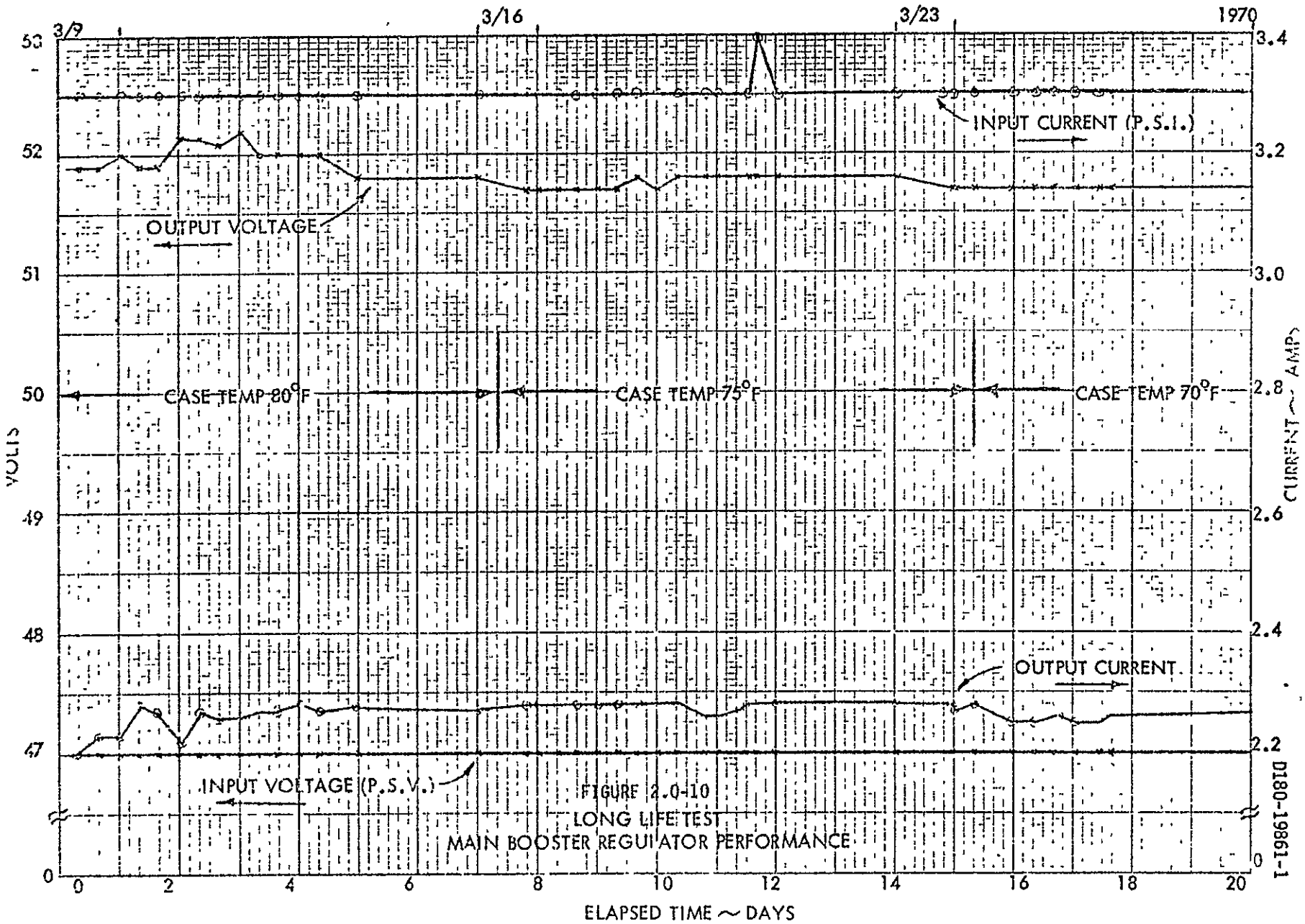

FIGURE 2.0-10
LONG LIFE TEST
MAIN BOOSTER REGULATOR PERFORMANCE

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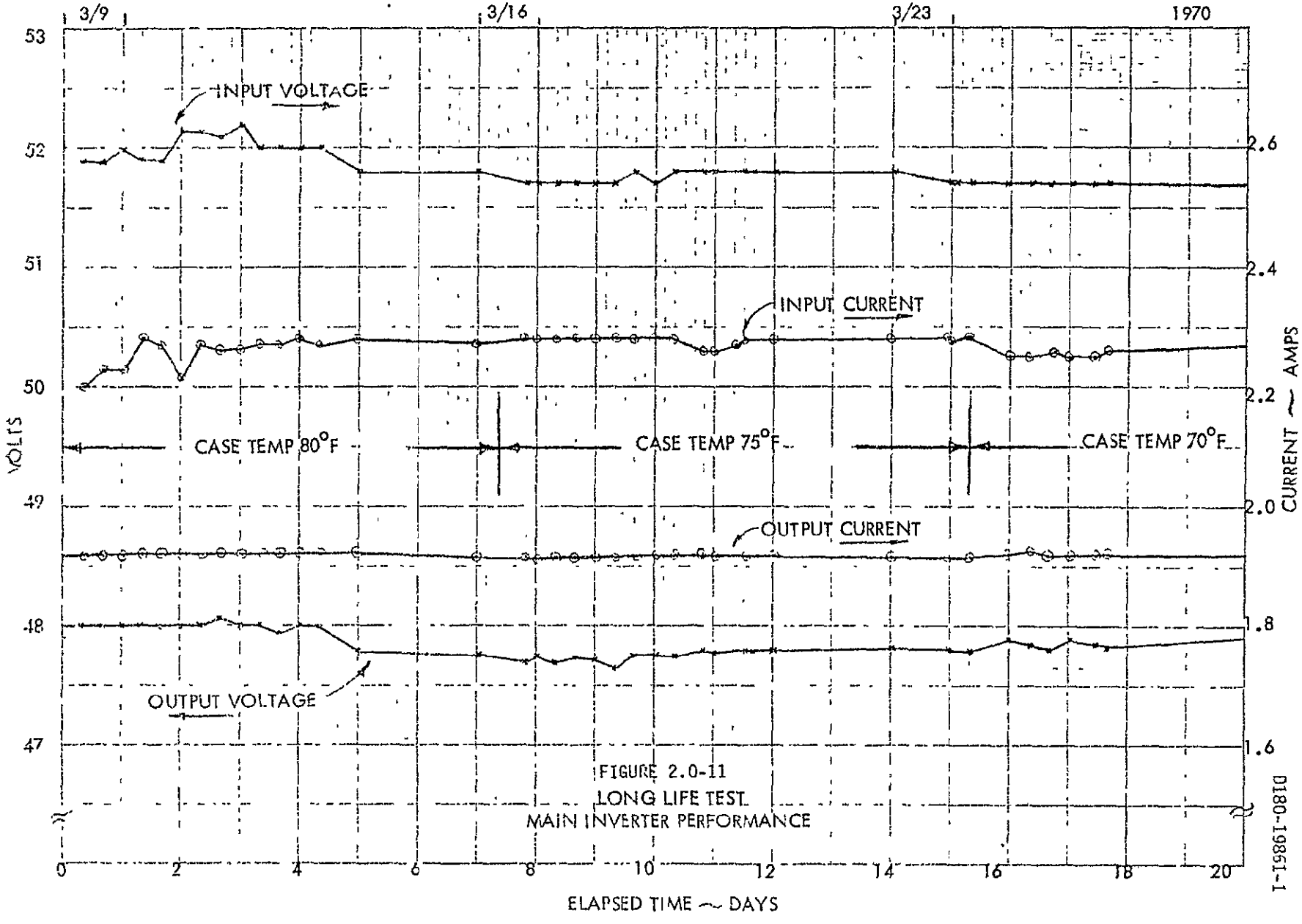

FIGURE 2.0-11
LONG LIFE TEST
MAIN INVERTER PERFORMANCE

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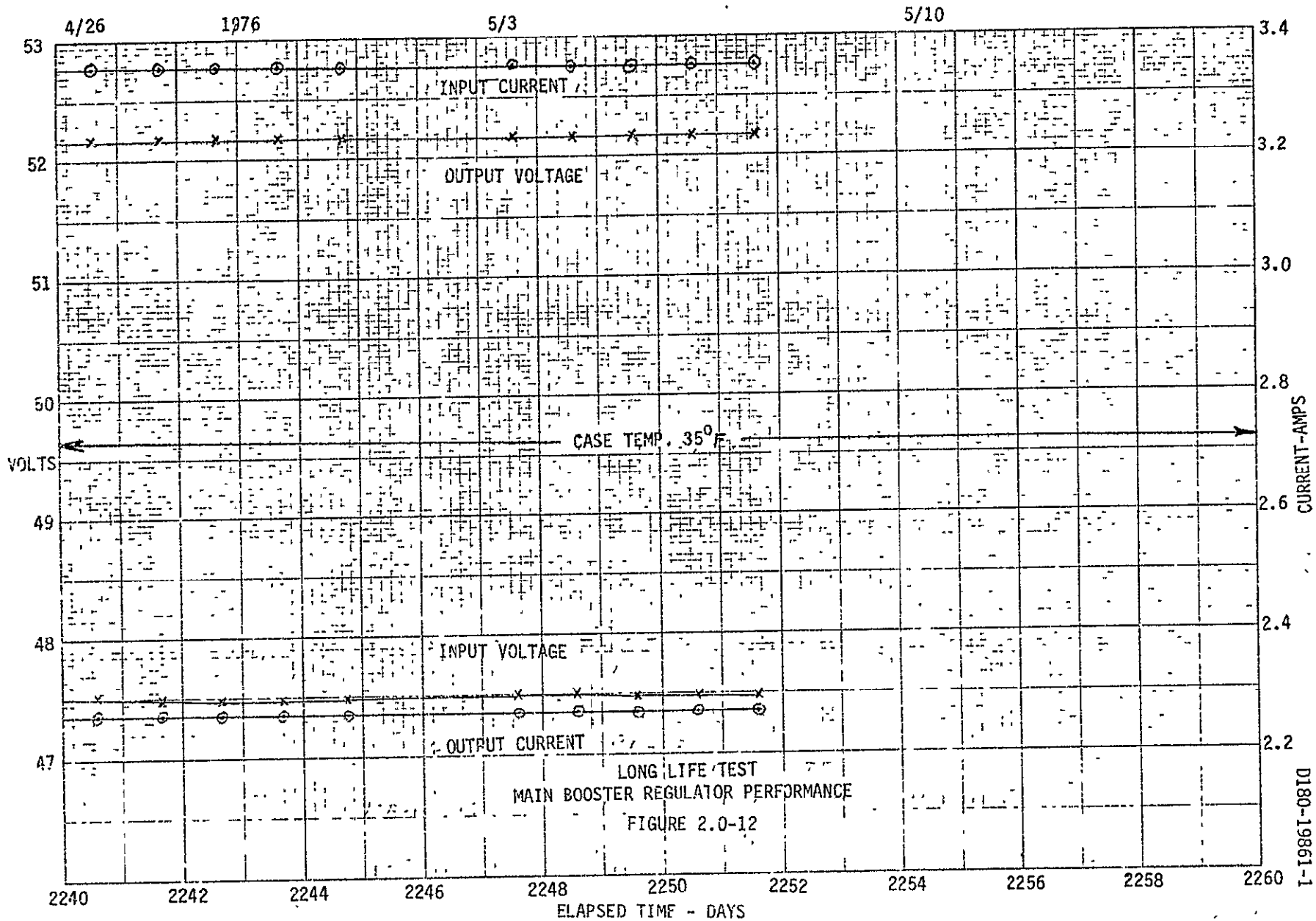
K+E 12 X 20 TO THE INCH 46 1970
7 X 10 INCHES MADE IN U.S.A.
KEUFFEL & ESSER CO.



LONG LIFE TEST
MAIN BOOSTER REGULATOR PERFORMANCE
FIGURE 2.0-12

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K&E 12 X 20 TO THE INCH 46 1970
7 X 10 INCHES MADE IN U.S.A.
KEUFFEL & ESSER CO.

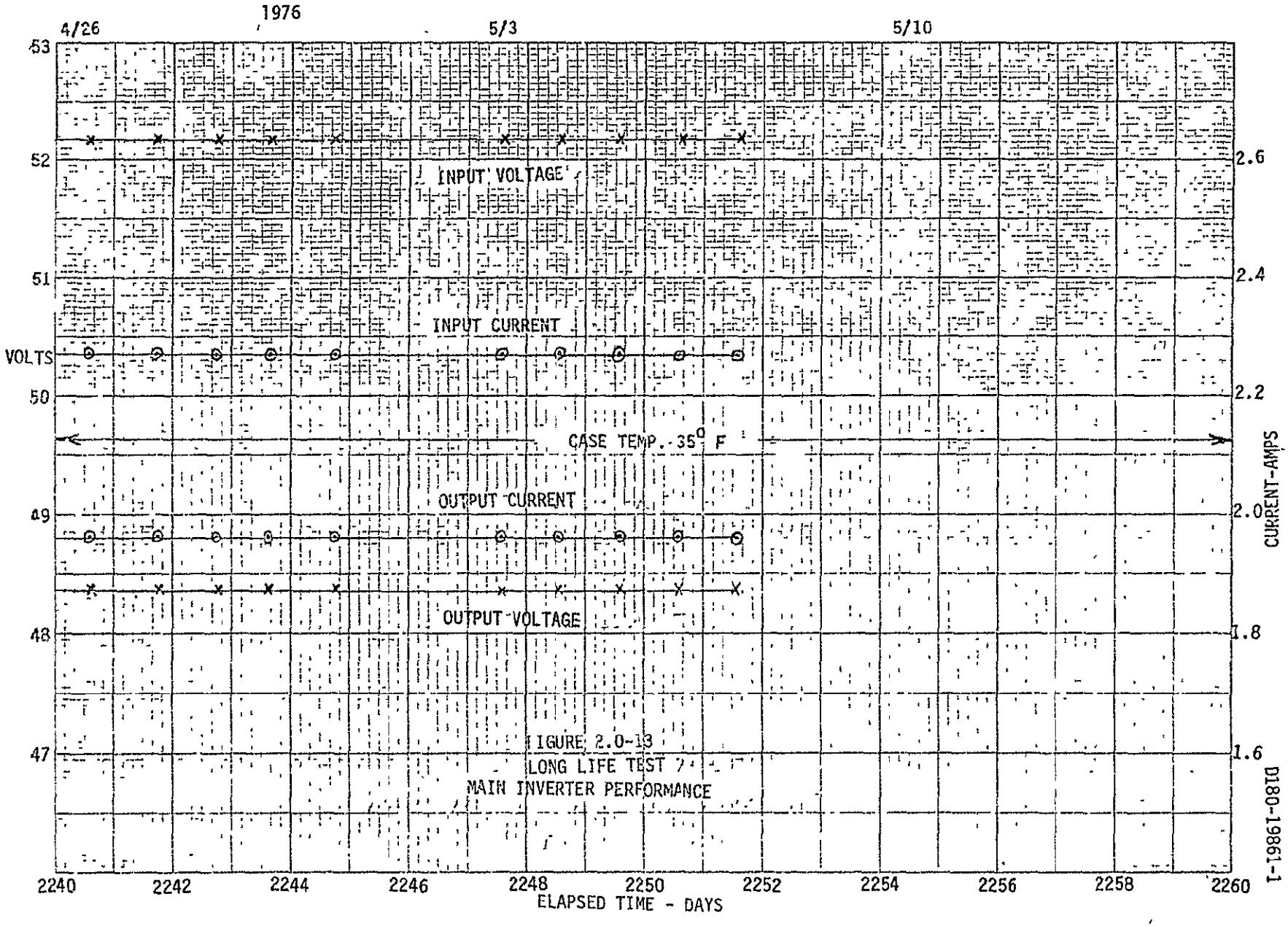

FIGURE 2.0-13
LONG LIFE TEST
MAIN INVERTER PERFORMANCE

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2.0 TEST RESULTS (Cont.)

When the equipment was examined after the test was completed, there was no evidence of any physical damage nor any difficulty in disconnecting the wiring connectors, i.e., there was no 'self-welding.'

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3.0 FAULTS

No failures occurred in the Power Conditioning Electronics in over six years of life testing. However, two failures were detected during the pretest performance testing. These failures may have existed when the equipment arrived at Boeing or may have been caused during the test set-up; this could not be determined.

The first failure was detected on 17 December 1969 during the pretest check of the 400 Hz inverter output frequency waveform and was traced to a faulty diode in the power synchronizer module 4A12, which caused the inverter frequency to go to 600 Hz. A copy of the failure report which was submitted to JPL subsequent to the fault investigation and analysis is included as Appendix I to this report.

The second failure was noted on February 6, 1970, when the pretesting was resumed after repair of the first fault. The battery voltage telemetry channel failed to provide the expected voltage and the fault was traced to two defective diodes, type IN459A, which were found to have a low reverse voltage breakdown. Coincidently these diodes were of the same type as the diode that had failed previously in the power synchronizer module. However, there was no apparent correlation between the failures as the circuit operating conditions were entirely different in each case. The full report on the failure investigation is given in Appendix II.

Examination of the diodes at JPL indicated that the diodes appeared to have been overstressed at some time but the cause of the failure could not be pinpointed. As indicated earlier, there were no further diode failures during the life testing.

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4.0 REDUNDANCY

The redundant functions in the Power Conditioning Electronics are provided by the capability to switch the maneuver booster regulator to substitute for the main booster regulator and by the automatic switching of the 2400 Hz maneuver inverter to replace the main 2400 Hz inverter in the case of failure of the latter. The long life test results indicate that redundancy may be considered for high reliability since no failures occurred during the long life testing under space environmental conditions. It must therefore be concluded that the redundancy provided in the MV'67 Power Conditioning Electronics was quite satisfactory for the requirements of that mission and, in fact, proved quite adequate for a simulated mission in excess of six years duration since the conservative design allowed the subsystem to perform satisfactorily well beyond its intended life, even without dependence upon its redundant features.

Since the design and development of MV'67 PCE, there have been significant advances in microelectronics. It is thus possible to reduce the volume and weight of the PCE by using the newest components and latest packaging techniques. This could permit additional redundancies for very long missions where extremely high reliability is required. However, such designs would have to be proven to determine whether the added complexity was warranted.

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5.0 CONCLUSIONS

The successful completion of over six years of life testing under simulated space environmental conditions has demonstrated that a simple, conservatively designed, electronics subsystem with sufficient stress margins is capable of operating without degradation or failure well beyond its original design life. This exceptional performance can be attributed to several factors: the use of high reliability components; simplicity of design; adequate derating of components; a good thermal design; and successful completion of a comprehensive qualification program.

There was no evidence of cold-welding of the electrical connector contacts and screw rings after six years in the space environment (vacuum and temperature).

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6.0 RECOMMENDATIONS

Since the PCE would be redesigned using up-to-date components in any new application, it would be a significant factor to determine whether the latest equipment could match the tested equipment in a long life test. Some of the components in the Venus '67 PCE are no longer available in the aerospace industry since they have been superceded by improved technology. Also, the advancements in microelectronics and microprocessors could permit advanced designs which may be able to outperform older equipment.

Available PCE from near-term space programs such as the Mariner Jupiter Saturn could be candidates for a long term evaluation while the spacecraft is enroute to the planets. The testing could be started as soon as the equipment is available, which might even be prior to the launch date.

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7.0 SIGNIFICANCE OF THE WORK

The performance of the Mariner-Venus '67 Power Conditioning Electronics during this life test, in which the equipment was operated continuously, 24 hours a day, for over six years, in a simulated space environment, provides confidence that design lives of six years or more are attainable. It also confirms that with adequate derating to limit voltage and thermal stresses to levels which are well within the limits of the electronic components used in the equipment design it is possible to operate the equipment on a continuous basis at elevated internal temperatures without failures or degradation in performance. That the equipment continued to operate within acceptable performance limits throughout the duration of the long life test also indicates that component design tolerances used in the design of the equipment were adequate for the desired design life and that the effect of ageing on parameters such as transistor gain, zener voltage, capacitance, etc., even over a six year period, can be successfully accommodated. With conservative designs as used in the MV'67 PCE, lifetimes of even 10 to 30 years might be achievable.

Although some outgassing was indicated in the early stages of the test, transformer and inductor insulations did not break down and relay and connector contact materials did not form films causing conductivity problems. It was also noted that at the conclusion of the test when the electrical connectors were separated that there was no evidence of cold welding. Until spacecraft which have been in space for many years are recovered by shuttle-era spacecraft and tested, this is the only evidence that cold welding does not occur between the particular metals used in the connectors after long exposure to the space environment.

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JPL Contract 952600

APPENDIX I

LONG TERM LIFE TEST OF SPARE MARINER VENUS '67 HARDWARE (P.C.E.)

FAILURE REPORT ON FIRST MALFUNCTION IN FLIGHT HARDWARE

January 16, 1970
Revised January 27, 1970

INVESTIGATION OF FAILURE OF POWER SYNCHRONIZER MODULE 4A12 From Spare Mariner Venus '67 Hardware

INTRODUCTION

The subject investigation concerns the failure of the inverter system of equipment case 1, serial number 5, of the Spare Mariner Venus '67 Hardware. Line-to-line phase outputs in the malfunctioning condition are shown in Figure 1. The output frequency of each of these waveforms is 600 Hz. The design frequency is 400 Hz. The output frequencies of the power synchronizer module were also found to be 600 Hz. The cause of this failure was traced and the results are reported herein.

REFERENCE

J4400483 Rev. J, Power Synchronizer Schematic Diagram, Module 4A12, Jet Propulsion Laboratory, California Institute of Technology.

CONCLUSION

Faulty operation of power synchronizer module 4A12, serial number 6, resulted from failure of component CR13. This component is a 1N459A diode manufactured by Fairchild Semiconductor with JPL serialization number A00092. The diode exhibited a 550 ohm resistive characteristic in the reverse and forward bias conditions until normal forward conduction voltage was reached. The device was forwarded to JPL for failure analysis.

Failure of this diode to block in the reverse direction allowed extraneous triggering pulses to be passed from the base of Q10-6 to the collector of Q9-7 and double triggering of F/F-1-7 resulted.

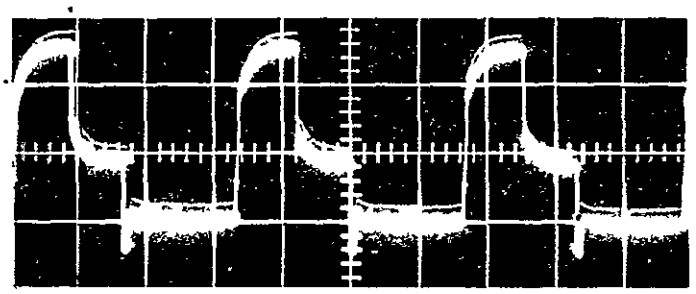
PROCEDURE

Power synchronizer module 4A12, serial number 6, was removed from the equipment rack and operated with laboratory power supplies. Output waveforms were observed for flip-flops F/F-1-5, 6, and 7, and for both electrode terminals of diode CR13. Reference to the test points for coordination with the waveform pictures is provided in Figure 2.

The outputs of flip-flops F/F-1-5, 6, and 7 are contained in Figures 3a, 3b, and 3c, respectively. The output of F/F-1-7 is the inverting output (collector of Q9-7) used in the reset feedback loop involving diode CR13. Although not shown, the correct inverted relationship between the two outputs of F/F-1-7 was observed indicating that the two sections of this flip, integral within itself, were operative. The waveforms for FF-1-5 and 6 are the non-inverted collector outputs of Q10-5 and 6. The A-phase output was used as an oscilloscope trigger to maintain the proper time relationship between all pictures.

Phase A-B Waveform

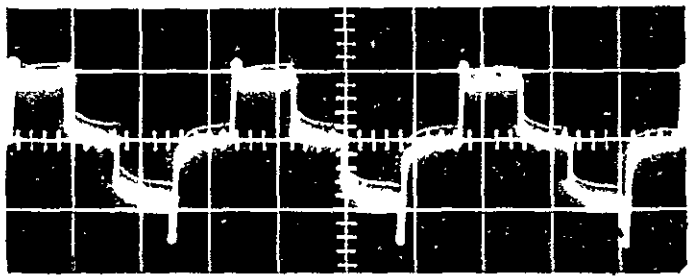
20 volts/div



0.5 msec/div

Phase B-C Waveform

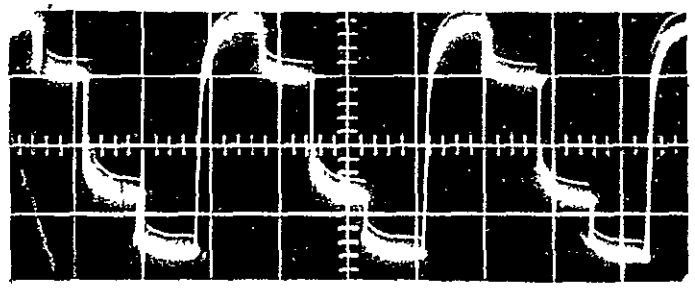
20 volts/div



0.5 msec/div

Phase A-C Waveform

20 volts/div



0.5 msec/div

Figure 1: 400 Hz, 3 Phase Inverter Waveforms (Malfunction Condition)

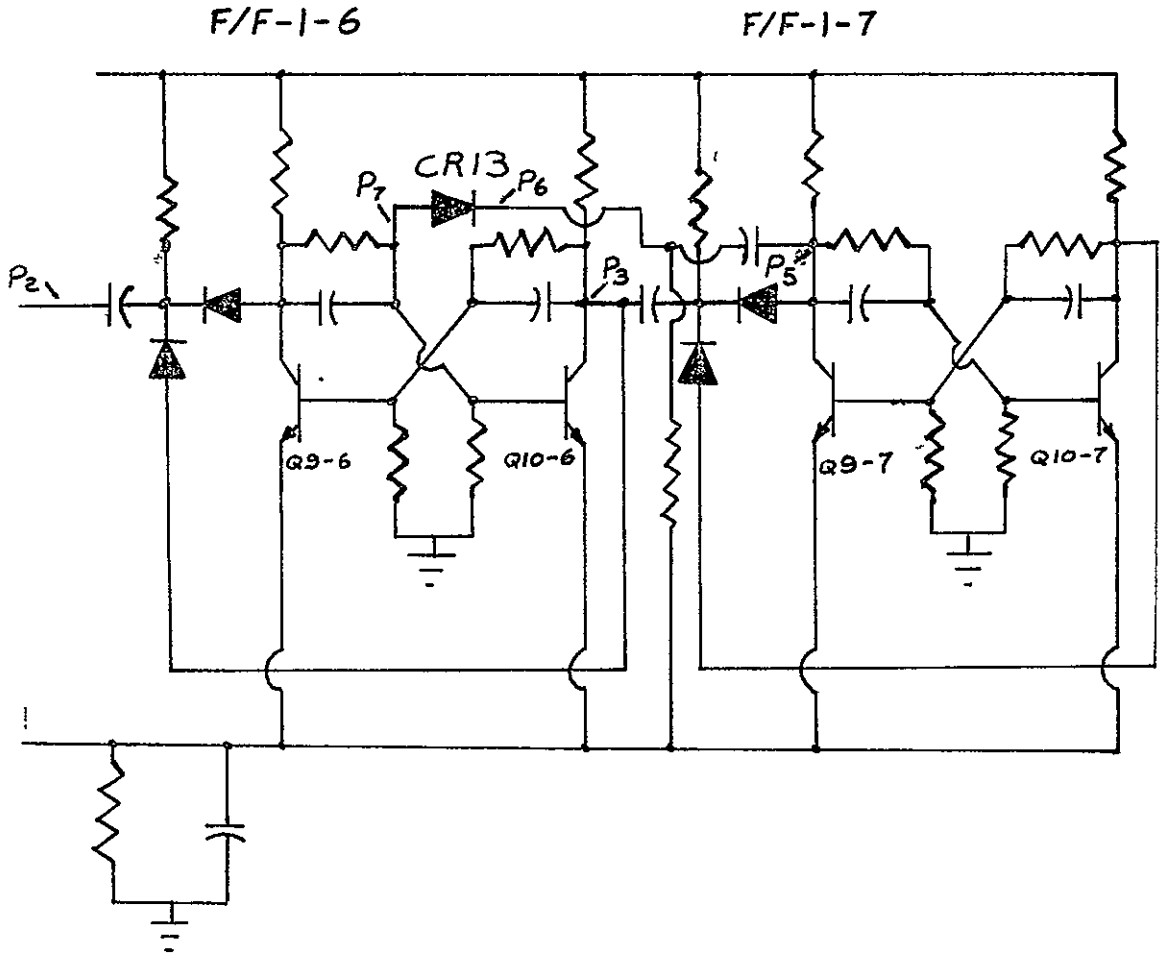
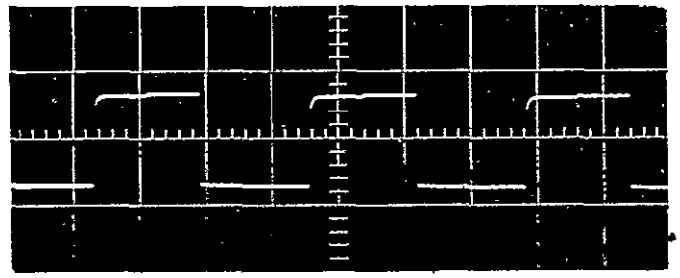
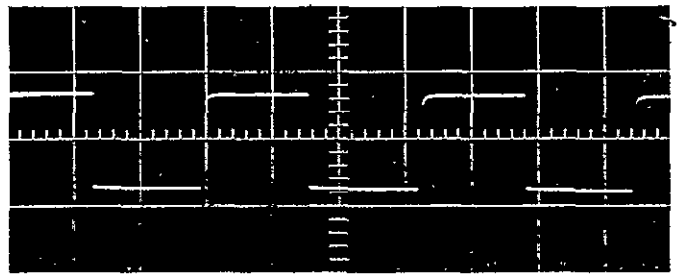


Figure 2: Schematic Diagram and Test Point Locations of F/F-1-6 and F/F-1-7

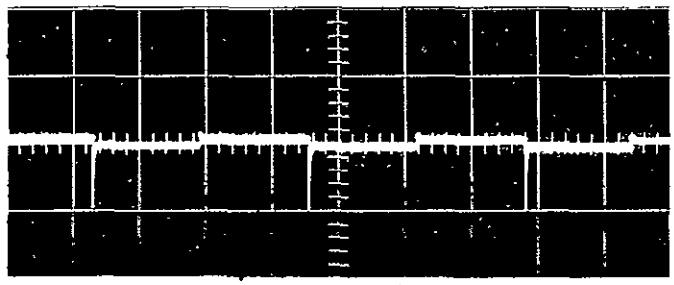
a) F/F-1-5 Output (P_2)



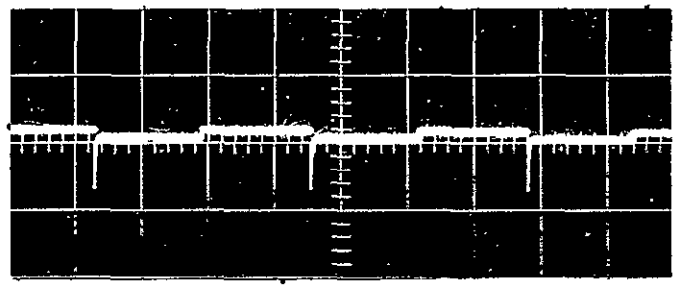
b) F/F-1-6 Output (P_3)



c) F/F-1-7 Inverting Output (P_5)



d) CR13 Cathode Waveform (P_6)



e) CR13 Anode Waveform (P_7)

Scale Factors (all waveforms)

10 volts/div (vertical
0.5 msec/div (horizontal)

Figure 3: F/F-1-5, 6 and Output and Diode CR13 Cathode and Anode Waveforms (Malfunction Condition)

Flip-flop 5 was found to operate satisfactorily at 1.2 KHz. Flip-flops 6 and 7, however, were both operating at 600 Hz rather than at 400 Hz as required. The cause appeared to be double triggering of F/F-1-7. This circuit was found to regenerate at both the leading and trailing edges of its input waveform. Triggering only on the negative going edge is intended.

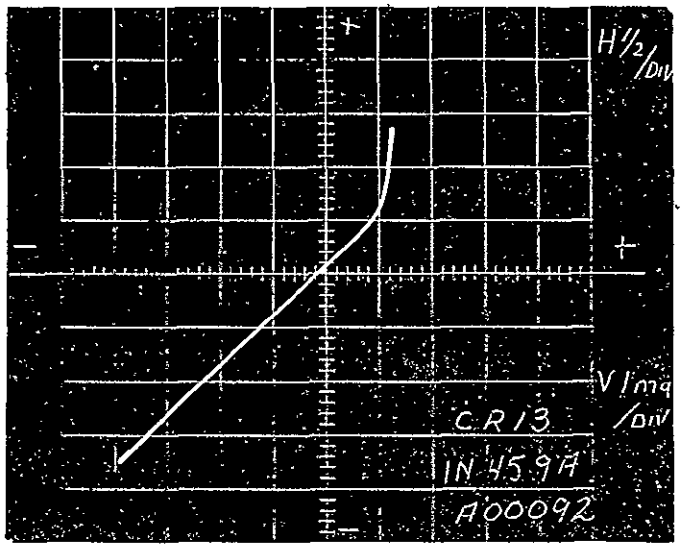
Cause of the triggering malfunction was investigated using a Tektronix Type 575 Curve Tracer with adequate series limiting resistance to prevent component damage. The input coupling capacitor and both steering diodes of F/F-1-7 were checked and no anomalies noted. Tracing across diode CR13 revealed a resistive characteristic of approximately 550 ohms until normal forward conduction voltage was reached. One end of this diode was lifted and the identical characteristic observed, thereby sourcing the short to the diode itself. The diode is a type 1N459A manufactured by Fairchild Semiconductor with JPL serial number A00092. The diode characteristic is exhibited in Figure 4.

Diode CR13 was temporarily replaced with a comparable unit. Proper operation was then achieved. The resulting three phase outputs are shown in Figure 5. The outputs were 400 Hz, 45 volt peak-to-peak square waves achieved with a 50 volt driver supply. The B and C phase outputs were found to lag the A phase by 120° and 60°, as is proper.

MALFUNCTION ANALYSIS

The extraneous triggering of F/F-1-7 was caused by failure of diode CR13 to block the negative pulse spike present as Q10-6 of F/F-1-6 is driven from saturation into cutoff. This occurs as Q10-6 is regenerating from a low to a high voltage state (Figure 3b) and Q9-7 is not conductive (Figure 3c). A negative spike passed through CR13 to the collector of Q9-7 causes F/F-1-7 to regenerate. As the collector voltage of Q9-7 drops, a negative spike is passed back through CR13 in the proper direction to the base of Q10-6. This spike does not reset F/F-1-6 since it reinforces the current digital state of that flip-flop.

Waveforms observed at the cathode and anode of CR13 are shown in Figures 3d and 3e. The spike magnitude is greater at the cathode indicating that the observed spike is the reset pulse passing from F/F-1-7 to F/F-1-6. Since it is hypothesized that an extraneous trigger was passed through CR13 in the opposite direction, and replacement of the failed diode resulted in proper operation, it appears that the faulty triggering spike is masked by the reset pulse in Figure 3. Occurrence of these two spikes would be essentially simultaneous.



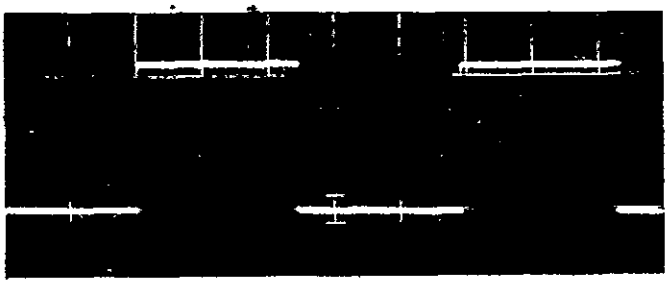
1 mA/div

0.5 volts/div

Figure 4: I-V Characteristic of Failed 1N459A Diode,
Serial Number A00092,
Configuration Position CR13

Phase A Output

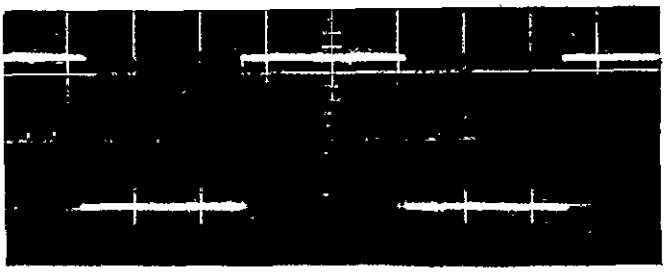
20 volts/div



0.5 msec/div

Phase B Output

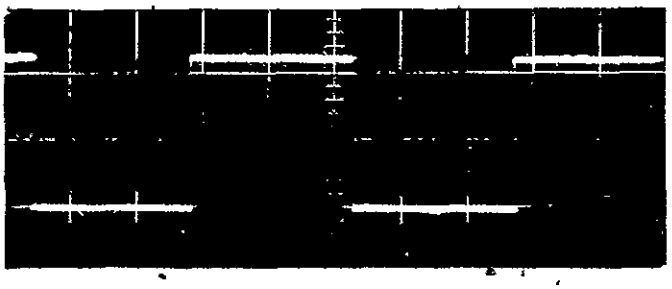
20 volts/div



0.5 msec/div

Phase C Output

20 volts/div



0.5 msec/div

Figure 5: Power Synchronizer Output Waveforms Resulting from Temporary Replacement of CR13

CIRCUIT ANALYSIS

This analysis concerns flip-flops F/F-1-6 and 7 associated with the reset diode CR13 with which the recent failure was experienced. Since a total of seven such flip-flops are used in the synchronizer module 4A12, this analysis actually covers all seven vibrators. F/F-1-6 and 7 are distinguished in that they contain the only reset feedback loop of all pairs, and along with F/F-1-5, drive the logic mesh circuits used to furnish the three phase output of the module. These gate loads are considered in the analysis.

The basic circuit considered is shown in Figure 6a. The initial effort was to calculate the range of emitter back bias voltage, labeled V_E, which could exist since high voltages could limit the capabilities of the base drive circuitry to saturate the "on" transistor. This voltage results from the collector and base current drainage of seven flip-flop circuits through the single emitter resistor R_E. Since one transistor of each circuit is conducting, this bias current was taken to be seven times the emitter current of a single transistor.

The expression used for I_E and its relationship to V_E is given in Equation 1. Since terms involving V_E appear in the expression (resulting from feedback), the equation was manipulated to form an expression for V_E which appears in Equation 4. The terms R_{Thb} and E_{Thb} which appear in these equations are Thevenin equivalent impedance and voltage as seen at the base of the driven transistor. Equations 2 and 3 express these values in terms of the other circuit parameters.

A worst case tolerance of $\pm$ 5% was assumed for all resistors involved. The symbol R_G is used to designate the loading of the gate logic on a high state "off" collector. The worst case (82.5K $\pm$ 5%) occurs when a "Z" input is driven which is disabled by the "R" input. R_G' represents the load occurring when a low state transistor drives the "R" input of one of the logic gates. Ranges assumed for all of these resistors is given in Table 1.

Table 1

Assumed Range of Resistors

	Max.	Nom.	Min.
R_B	3.49K	3.32K	3.15K
R_L	7.15K	6.81K	6.46K
R_K	23.21K	22.1K	20.9K
R_G	∞	82.5K	74.6K
R_G'	∞	82.5K	74.6K
$7R_E$	162.4	154.7	146.8

Circuit Equations

$$(1) \quad I_E = I_C + I_B = [V_{CC} - V_E - V_{CE(SAT)}] \left[\frac{R_L + R_G}{R_L R_G}\right] - [V_E + V_{CE(SAT)} - I_{EBX} R_B] \left[\frac{1}{R_K + R_B}\right] + [E_{Th} - V_E - V_{BE(SAT)}] \frac{1}{R_{Thb}} = \frac{V_E}{7R_E}$$

(2) $$R_{Thb} = \frac{R_B\,(R_L R_G' + R_K R_L + R_K R_G')}{R_L R_G' + R_B R_L + R_K R_L + R_G' R_B + R_G' R_K}$$

(3) $$E_{Thb} = \left[\frac{R_B R_G'}{R_B R_L + R_K R_L + R_B R_G' + R_K R_G' + R_L R_G'}\right]\left[V_{CC} + (I_{RDS} - I_{CEX})\,R_L\right]$$

(4) $$V_E\left[\frac{1}{R_E} + \frac{R_L + R_G}{R_L R_G} + \frac{1}{R_K + R_B} + \frac{1}{R_{Thb}}\right] = \left[V_{CC} - V_{CE(SAT)}\right]\left[\frac{R_L + R_G}{R_L R_G}\right]$$
$$- \left[V_{CE(SAT)} - I_{EBX}\,R_B\right]\left[\frac{1}{R_K + R_B}\right] + \left[E_{Thb} - V_{BE(SAT)}\right]\frac{1}{R_{Thb}}$$

(5) $$I_B = \frac{E_{Thb} - V_E - V_{BE}}{R_{Thb}}$$

(6) $$\left[E_{Th(min)} - V_{E(max)}\right] = 5.16 \times 10^{-2}\,V_{CC}$$

(7) $$h_{FE(min)} = \frac{I_{C(max)}}{I_{B(min)}}$$

(8) $$I_{C(max)} = \frac{V_{CC(max)}}{R_L(min)}$$

The 5% tolerance allowed for the resistors is probably rather severe in view of the temp. coeff. of -0.03%/°C quoted by the manufacturer. With the 1% nominal value allowance, the tolerance assumed will allow for temperature extremes in excess of 130C° for a non-defective resistor. In view of mission criticality, the 5% range was adhered to, however.

The range of Thevenin base parameters and emitter bias voltages were caluclated for power supply voltages of 20 ± 2 volts. One volt of the drift was allowed for zener regulator CR3 (1N1358A). The additional volt deviation from power supply nominal was added to cover to assumed .075%/°C drift of the regulator. A 67°C temperature change would produce this deviation. The base drive Thevenin parameters and emitter bias voltages appear in Table 2.

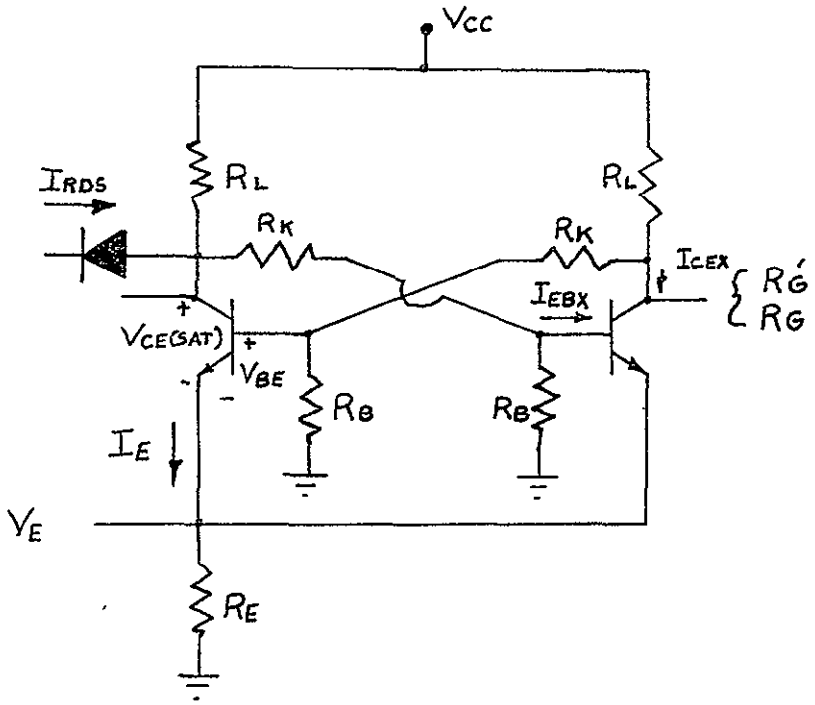


Figure 6a Circuit Defining Parameters Used in Worst Case Analysis

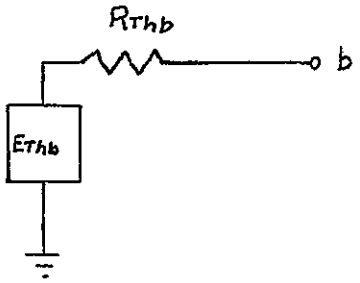


Figure 6b Base Circuit Thevenin Equivalent

Table 2

Emitter Bias Voltage and Base Drive Thevenin

Extremes for $V_{CC} = 20 \pm 2$ Volts

	Min.	Nom.	Max.
R_{Th}	2.45K	2.97K	3.50K
E_{Th}	1.56V ($V_{CC} = 18$)	2.00V ($V_{CC} = 20$)	2.52V ($V_{CC} = 22$)
V_E	.326V ($V_{CC} = 18$)	0.470V ($V_{CC} = 20$)	.772V ($V_{CC} = 22$)
V_E			.632V ($V_{CC} = 18$)

For the calculations of Table 2, one volt nominal saturation levels were assumed with 1.2 volt maximum. Terms involving diode leakages were ignored since their effort is greater than one order of magnitude less than the levels considered.

Concern is expressed for minimum differential which can exist between the minimum thevenin base voltage and the maximum V_E which can exist for a given supply voltage. As this differential diminishes, current gain requirements of the saturating transistor may be inordinately increased since the resulting base drive decreases with the relationship given in Equation 5. For an 18 volt power supply, this differential could be as low as 0.93 volts. If 0.7 volts is allowed for base-emitter conduction bias, transistor current gains in excess of 46 could be required to ensure saturation (Equations 5, 6, and 8). More than 0.7 volts base-emitter base should be allowed in a worse case analysis resulting in even greater current gain requirements.

An expression for the minimum differential between Thevenin base drive and emitter bias voltages was developed as given in Figure 6. At nominal power supply voltage, this differential could be as low as 1.03 volts. Since it is felt that at least 1 volt should be allowed for V_{BE}, although statistically improbable, this condition would result in circuit failure.

A current gain requirement was calculated for the nominal voltage differential and maximum R_{THb}. This gain requirement was $h_{FE} = 35$ and should be held as an absolute minimum gain requirement at $I_C = 3.0 - 3.5$ mA. This value of gain was calculated using an assumed worst case V_{BE} of 1.2 volts.

PART APPLICATION

All resistors involved are assumed to be precision, carbon film resistors of 125 milliwatt rating per MIL-R-10509D characteristic G. Worst case dissipation for all resistors, with the exception of R29, was calculated assuming a direct DC connection across the power supply. For this consideration, the highest dissipation would occur in the lowest value resistor. Specifically, the dissipation would be 120 milliwatts occurring in the 3.32K base resistors with 20 volts applied. In application, this resistor would not experience

a DC voltage application exceeding 12% of the actual power supply voltage. In view of this, the actual worst case dissipation would occur in the 6.81K load resistors. Voltage across these resistors is switched from approximately 100% to 26% of the supply voltage with a 50% duty cycle. Under these conditions, the resistor would dissipate 32 milliwatts, assuming 5% resistor tolerances, with a nominal 20 volt supply, and would exceed the 1/8 watt rating at a 39 volt supply level. Under nominal supply conditions, this resistor would be adequately derated for ambient temperatures up to 140°C per MIL-R-10509D, Characteristic G.

Peak transistor dissipation occurs during the switching transient when the collector is at approximately one-half of the supply voltage. For a 30 volt assumed supply, this dissipation would be about 33 milliwatts per section or 66 milliwatts for the total device. In view of the short switching duty cycles, actual worst case dissipation would be closer to twice the transistor saturation power or about 10.5 milliwatts occurring for a 30 volt supply and 1.2 volt collector saturation voltages. If this estimate is increased to 20 milliwatts, this application is safe for application in 165°C ambient by manufacturer ratings.

The voltage rating of all diodes is believed conservative for this application. The only concern in application of these diodes concerns the peak recurrent surge current which may be experienced by diode CR13 when passing the reset pulse during which the cathode of this diode may instantaneously drop 10-14 volts below ground level. Functionally, this spike is intended to cut off the base drive to Q10-6. Such a spike may cause breakdown of the emitter base of Q10-6 at as little as -7 volts, thereby clamping, during the short transient, a high forward bias across CR1e. In the monitored conditions of Figures 3d and 3e, this forward bias was estimated at 2.5 volts. Since the diode conductance is rated at better than 100mA at one volt, it is almost certain that the manufacturer's rating of 125mA peak recurrent forward current is being exceeded. No series limiting resistance is included in the diode circuit.

CONCLUSIONS

The statistically remote possibility exists that adequate base drive to insure saturation of a driven transistor is not available. The result would be functional failure of the entire synchronizer module.

Possible transient forward voltages in excess of 2.5 volts may be experienced by diode CR13. Although the duty cycle of such transients is small, the manufacturer's peak repetitive forward current rating of 125mA would certainly be exceeded. Whether the recent failure of this diode was precipitated by this potential abuse or a defective diode remains conjectural until the results of the failure analysis of the part are obtained.

RECOMMENDATIONS

It is recommended that a design modification concerning all components affecting base drive strength be performed. Possible modifications include raising the value of the base resistors R34 and R35 and/or decreasing the emitter bias resistor R29. To limit the surge current of diode CR1e, it is recommended that a limiting resistance on the order of 60 ohms be included in series with the anode at that diode.

EFFECT OF THIS TYPE OF MALFUNCTION ON THE MISSION

Loss of the correct three phase, 400 Hz signals from the Power Synchronizer (4A12) will cause the three phase, 400 Hz inverter (4A18) to run at a different frequency, in this case approximately 600 Hz, and the output to be distorted as shown in Figure 1. Due to the lower than normal line to line voltages, the gyro motors would not attain the synchronous speed of 36,000 r.p.m. but would tend to fluctuate in speed in some region between 24,000 r.p.m. and 36,000 r.p.m. The fluctuations could be small or as much as $\pm$ 1000 r.p.m. This would, of course, cause fluctuations in the gyro scale factor which may or may not be tolerable. Up to one hour operation at the higher speed should not cause serious damage to the motor bearings or damage the rotor.

The total effect on the mission would be to inhibit the use of the gyros, if the fluctuations in the gyro scale factor are intolerable, thus making it impossible to do any maneuvering of the spacecraft for, say, velocity changes.

APPENDIX II

LONG LIFE TESTING OF SPARE MARINER VENUS '67 HARDWARE

FAILURE REPORT EVALUATION
#2

JPL Contract 952600

March 2, 1970

Aerospace Group
Spacecraft Branch
The Boeing Company
Seattle, Washington

FAILURE REPORT EVALUATION #2

INTRODUCTION

A failure was noted on February 6, 1970, during checkout of the Power Regulator Electronic Assembly (4A8), Case VIII, S/N 06. Fault isolation steps were initiated following a failure of the Battery Voltage telemetry channel to provide the expected output voltage. The maximum voltage measured at the output of the channel was 0.4 VDC with 30 VDC or more applied to the ground power input terminals, whereas the voltage should have been at least 1.16 V (see Table 1, page 2). Proper performance of the telemetry channel, the circuit of which is shown in Figure 1, was restored after the faulty parts were isolated and replaced.

Two diodes, type 1N459A's, were found to have defective reverse voltage characteristics. One would break down at approximately five volts reverse bias and the other would break down with ten to fifteen volts reverse voltage applied; reverse voltage capability is 175 volts. These diodes were in circuit positions CR62 and CR63.

Fuse F1 was blown during the initial troubleshooting effort. The cause of this blown fuse was not determined.

A wiring error was discovered during the initial ohmmeter measurements in the Battery Voltage telemetry channel. This error resulted in Q40 being bypassed by the battery signal input to the telemetry circuit. This wiring error was corrected after the rest of the circuit had been restored to normal operation.

The faulty diodes and the blown fuse were forwarded to JPL for failure analysis.

REFERENCE

Power Regulator Electronic Assembly Schematic Diagram, JPL Drawing J4120171, Rev. C.

FAILURE DETERMINATION

The Power Regulator Electronic Assembly was removed from the equipment rack so that it could be operated with laboratory power supplies and probed for observation of waveforms in the malfunctioning telemetry channel.

Ohmmeter measurements were made of the telemetry circuit prior to applying power to the ground power input terminals. The ohmmeter checks revealed a wiring error which connected the base of Q39 to the base of Q40. The base of Q39 should be connected to the emitter of Q40. Figures 2 and 3 are photographs of the installation. This wiring error would cause a minor degradation of calibration accuracy (0.6V to 0.7V) and temperature stability compared to the correctly wired circuit. Normal ohmmeter readings were obtained throughout the rest of the battery voltage telemetry circuit except for a relatively low indication of 6,000 ohms reverse resistance for CR62.

Power was applied to the Power Regulator Electronic Assembly through the ground power connections. A current-limited laboratory power supply was used with the current limit set at five amperes. The +52VDC booster regulator output (reference JPL drawing J4120171, Revision C) was loaded with fifty ohms across pins X and V and a jumper was provided across the telemetry oscillator current monitor loop pins J and F on the connector P2 (reference drawing J4120171, Revision C).

The terminals of R41 and R42 were probed to observe the telemetry oscillator waveform at the input to the modulator. No waveform could be seen and fuse F1 (reference JPL drawing J4120171, Revision C) was found to be open. A specific cause for this open fuse was not found. It may have been opened while probing for the telemetry oscillator signal. A laboratory power supply, set to 52 volts and current limited to less than 0.5 amperes output, was connected to the telemetry circuit input in place of the jumper closing the current monitor loop. This provided a safe power source for continued troubleshooting in the telemetry circuitry. No further evidence of overloading was observed on the power supply current meter during subsequent troubleshooting and operation of this equipment.

A satisfactory square wave was observed at the input end of the modulator circuit resistors, R41 and R42. The waveforms at the anodes of CR62 and CR63 were both incorrect. The waveforms at the anodes of CR62 and CR63 should each approach zero volts during alternate half-cycle periods when the input waveforms are near zero volts. An examination was made of the modulator circuit diode characteristics with a Tektronix Type 575 Curve Tracer. A 20K ohm series limiting resistance was employed to prevent component damage. This observation revealed that both CR62 and CR63 were breaking down in the reverse direction at very low voltage levels. These diodes were then removed from the modulator circuit and the characteristic curves were checked again. Figures 4 and 5 illustrate the results. Proper operation of the battery voltage telemetry channel was obtained when these two diodes were replaced. The fuse F1 was then replaced, the 52 volt laboratory power supply removed, and the jumper replaced across the telemetry oscillator current monitor loop pins in the connector. Power was applied to the unit through the ground power connections and proper performance of the battery voltage telemetry circuit was verified again.

The wiring error noted earlier was corrected according to the referenced diagram. Table 1 contains calibration data obtained during the checkout which followed this circuit correction.

TABLE 1
Calibration Data, Battery Voltage Telemetry

Input Voltage	T/M Output Voltage
22.0 volts	0.00 volts
25.0	0.30
28.0	0.80
30.4	1.23
33.0	1.69
36.3	2.27

FAILURE ANALYSIS

The wiring error which connected the base of Q39 to the base of Q40 resulted in Q40 being bypassed and Q39 being driven directly by the battery voltage input through CR102. The most significant effect of this wiring error upon the performance of the telemetering channel would be a minor degradation of calibration accuracy and temperature stability. The magnitude of this error would be approximately equal to V_{BE} for Q40, typically 0.6V to 0.7V. The three diodes, CR99 through CR101, normally compensate for the voltage drop through CR102, V_{BE} Q40, and V_{BE} Q39, when the circuit is wired according to the diagram. However, with Q40 bypassed the voltage at the cathodes of CR62 and CR63 would be higher than the battery voltage by approximately one diode drop.

The two diodes, CR62 and CR63, are part of a modulator circuit which develops a square wave across the primary transformer T8. The peak-to-peak amplitude of this square wave, developed between each side of the primary and the center tap, should be approximately twice the difference between the voltage at the cathodes of CR62 and CR63 and the reference voltage at the center tap. The very low reverse voltage breakdown characteristics of the two diodes, CR62 and CR63 (ref. Figures 4 and 5), kept the low voltage portion of each half cycle of the reference waveforms at the anodes of CR62 and CR63 from approaching zero volts as they should. This severely restricted the maximum amplitude of the square wave that could be generated across the primary winding of T8, which in turn limited the magnitude of the output voltage to the battery voltage telemetry channel.

PARTS APPLICATION

Normal operation of this modulator circuit will apply a reverse voltage stress alternately across diodes CR62 and CR63 which is approximately equal to the voltage level being monitored. This would normally be less than 40 volts and vendor data sheets indicate a reverse voltage capability of 175 volts for the type 1N459A diode. Resistors R41 and R42 would limit the forward current in diodes CR62 and CR63 to a maximum of 3 ma. peak even with zero volts applied to the input of the battery voltage telemetry channel. These maximum stress levels provide ample derating for the type 1N459A diodes used in this application.

POSSIBLE EFFECT OF THE FAILURE ON A FLIGHT MISSION

The loss of the battery voltage telemetry should have a minimal effect on the mission. Not knowing the battery voltage would decrease the confidence in the state of the battery. However, during periods of battery discharge, a good indication of battery performance and state of health can be determined from the primary system voltage telemetry and the battery current drain telemetry.

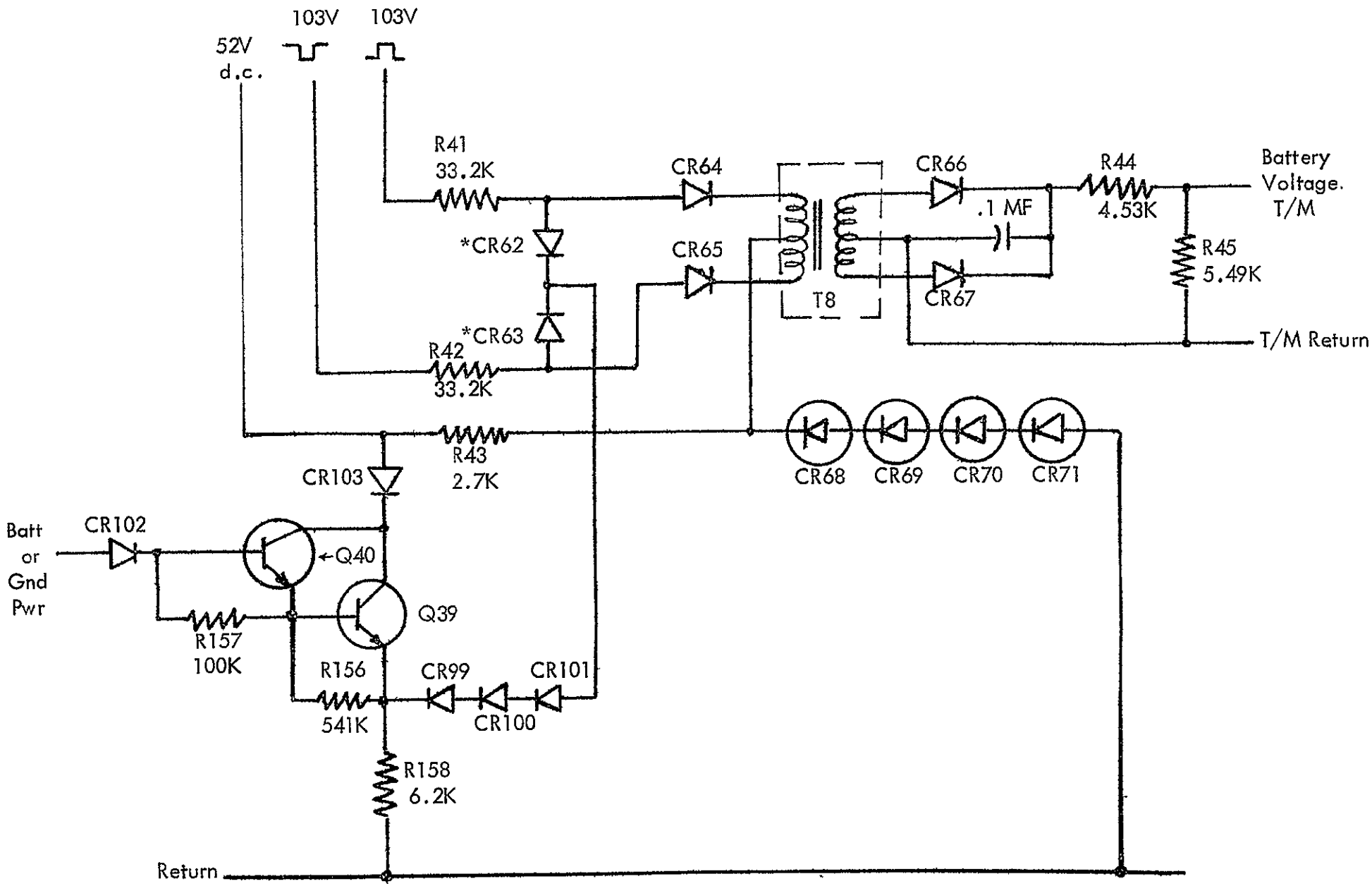
RECOMMENDATIONS FOR CHANGES OR IMPROVEMENTS IN THE CIRCUIT

The wiring error associated with transistors Q39 and Q40 suggested a circuit change which would reduce the parts count and improve the reliability in direct relation to the number of parts removed. This change would remove R156, R157, Q39, Q40, CR100, CR101, and CR103. The anode of CR99 would be connected to the cathodes of CR62 and CR63. The

cathode of CR102 would be connected to the junction of R158 and the cathode of CR99. With this change the current required to drive R158 would come directly from the battery input instead of the +52V regulated supply, and CR102 would be compensated for by CR99.

CONCLUSIONS

It is not apparent at this time how the failure of one of the diodes, CR62 and CR63, would create a stress on the other diode sufficient to damage a good part. The diodes are derated sufficiently for the application and are protected by R41 and R42 which limit the forward current to less than 3 ma. For this reason, coincidence is the only explanation offered for the failure of two identical parts in adjacent positions in the same circuit. It should be noted that the first malfunction reported in the Power Synchronizer Module also involved the failure of a type 1N459A diode. A review of the results of the failure analysis by JPL of the two diodes may suggest a direction for further investigation into the possible causes of these failures, such as evaluation of stock diodes for manufacturing defects or damage due to screening or burn in of the parts.



BATTERY VOLTAGE TELEMETRY CIRCUIT OF
POWER REGULATOR ELECTRONIC ASSEMBLY SCHEMATIC DIAGRAM
JPL DRAWING ., J4120171, REVISION C

*Failed Diodes

FIGURE 1

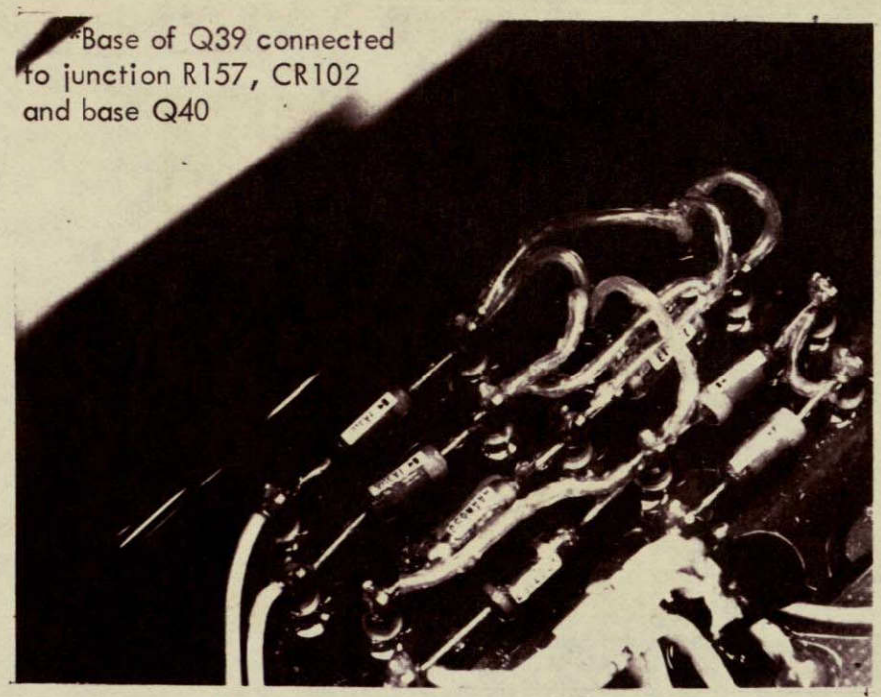


Figure 2: Circuit Board TB12 in Power Regulator Electronic Assembly (4A8) Case VIII, S/N 06

*Circuit wired improperly. See Figure 1 for correct wiring.

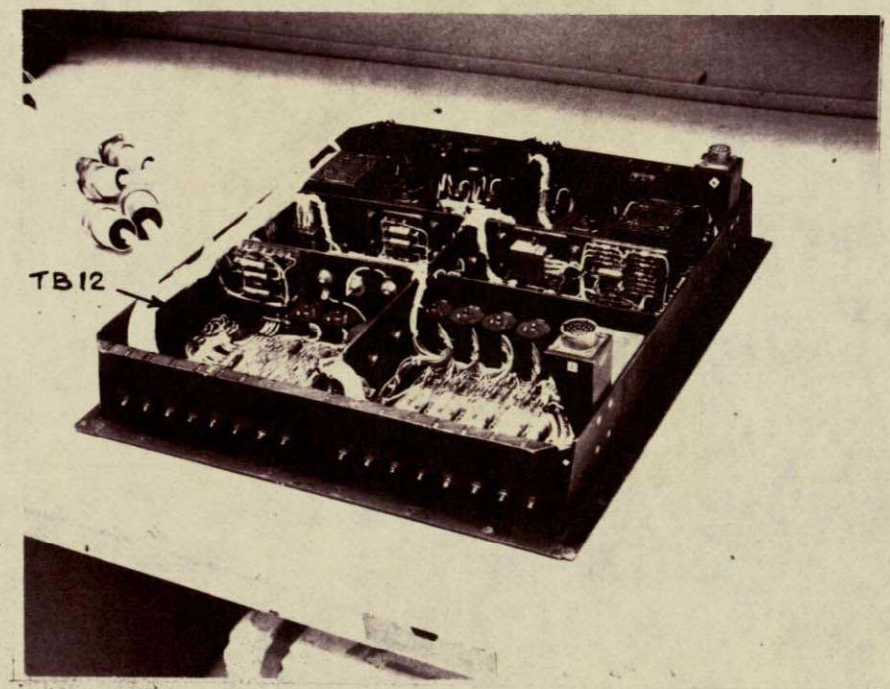
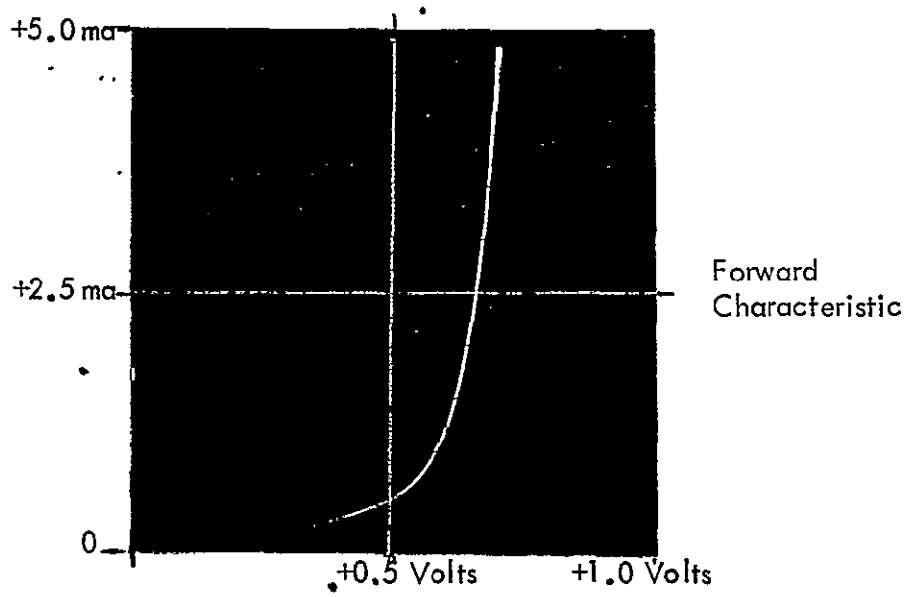


Figure 3: Power Regulator Electronic Assembly (4A8) Case VIII S/N 06



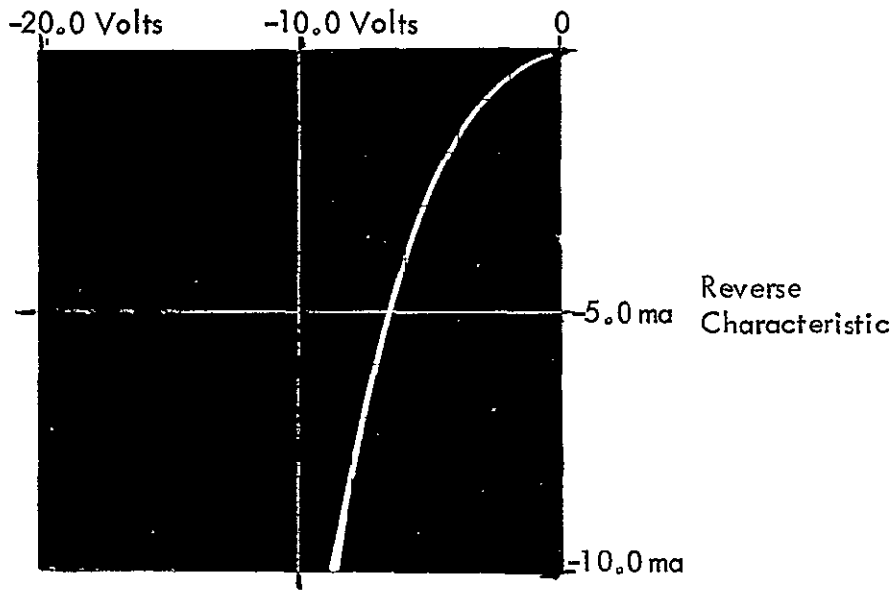


Figure 4 : Characteristic of Failed IN459A Diode,

Serial Number A00620,

Configuration Position CR62

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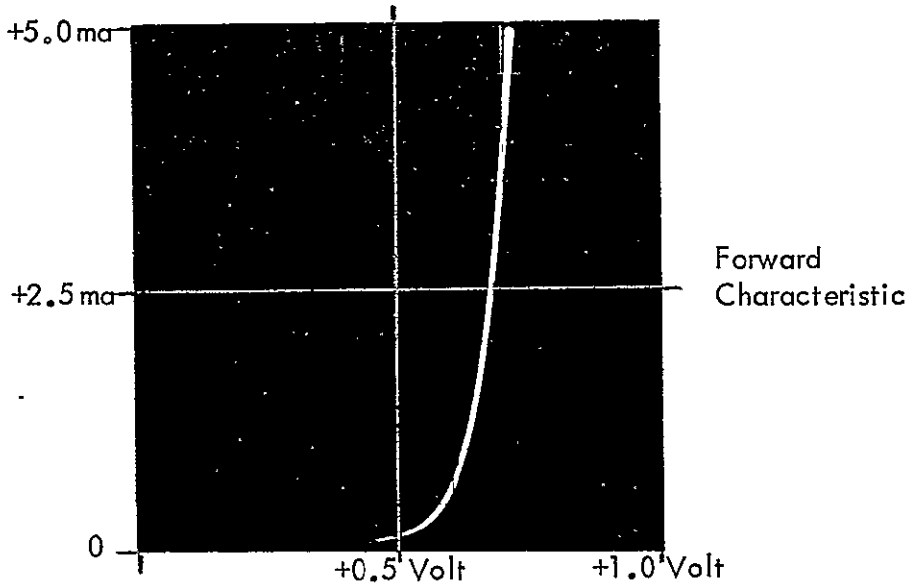

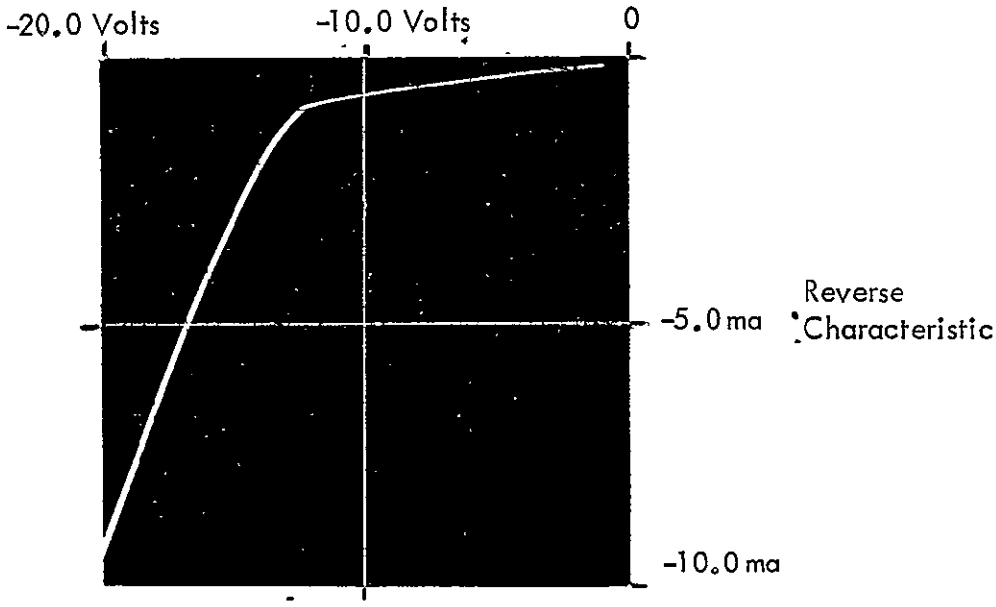

Figure 5 : Characteristic of Failed 1N459A Diode,

Serial Number A00905,

Configuration Position CR63

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