RESEARCH, DEVELOPMENT AND PILOT PRODUCTION

OF HIGH OUTPUT THIN SILICON SOLAR CELLS

JPL Contract No. 954197

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ABSTRACT

This report summarizes work performed to define and apply processes which could lead to high output from thin (2-8 mils) silicon solar cells.

The overall problems are outlined, and two satisfactory process sequences were developed. These sequences led to good output cells in the thickness range to just below 4 mils; although the initial contract scope was reduced, one of these sequences proved capable of operating beyond a pilot line level, to yield good quality 4-6 mil cells of high output.

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1.0 INTRODUCTION

1.1 Contract Purpose

The contract purpose was to investigate the solar cell process parameters needed to provide high output from thin (< 8 mils or 0.2 mm) silicon cells, and to select the best combination of these parameters to operate a pilot run of two thousand (2000) cells.

Most of the tests were aimed at developing methods for the cells in the lower thickness range, mostly around 4 mils. In the first six months of the contract, technical difficulties in combining the process steps for these thin cells resulted in relatively few shippable cells. As a result, excessive effort was diverted to solving what were planned as preliminary evaluation tests. This led to a re-definition of the contract performance whereby only 450 cells would be shipped to JPL. This redefinition relaxed the necessity to ship cells thicker than 6 mils. (The original plan called for delivery of 1400 cells in this thickness range.) Despite this relaxation, some assessment of the ability of the processes to be completed in pilot operation was obtained, because the last shipments comprising 250 cells in the range 3.5 to 6.0 mils, was fabricated mostly using manufacturing personnel and equipment.

2.0 ADVANTAGES AND DIFFICULTIES ASSOCIATED WITH THIN CELLS

2.1 Background

Production capability for silicon cells has been extended to run with slices as thin as 8 mils, (200μm). There are two difficulties in making cells thinner than 8 mils. First, there is increased breakage in handling slices during the process sequence. Second, the fabrication steps and their sequence, must be altered to maintain high electrical output; this process alteration involves some major differences in the process used.

2.2 Possible Advantages of Thin Cells

(a) Thinner cells can have higher power-to-weight ratio; ratios as high as 570 W/lb have been obtained prior to this contract.
(b) Thin cells have shown higher radiation resistance.
(c) Because of (a) and (b), thin cells should be useful for

large arrays, of the foldout or rollout variety, especially for use with electric propulsion schemes where very large area arrays are planned.

In order for these advantages to be realized, several other aspects must be met.

(i) The overall design of the arrays (including interconnections, covers, choice of mounting substrates, and deployment and other structural features) must be capable of exploiting the reduced weight available from thin cells.

(ii) The methods used to form arrays from the thin cells must be compatible with these cells; clearly if the complexity of interconnecting, covering and mounting of such cells becomes too great, there will be resistance to acceptance of thin cells, despite the advantages described above.

2.3 Possible Difficulties With Thin Cells

These difficulties fall into the two areas given in 2.1, namely mechanical and electrical difficulties. However, there is interaction between the two, in that some of the processes needed to enhance electrical output may provide added mechanical difficulties. To explore this in more detail it is useful to review the process sequence used to form normal thickness cells, and then to list some of the mechanical problems which accompany the fabrication sequence.

2.3.1 Normal Process Sequence

The conventional process sequence used is:

1. Grow single crystal of silicon, doped to give P- or N-type conductivity and to include a required resistivity range, and having a selected crystal orientation.

2. Cut and slice these ingots to form regular shape slices within the required resistivity range.

3. Process the surfaces of these slices; usually this involves polishing of at least one major face of the slice.

4. Using impurity diffusion form a shallow surface layer of opposite conductivity type from the original slice; in this way a shallow PN junction is formed below the front surface.

5. Remove the diffused layer from the back surface of the slice, and clean the slice carefully of diffusion-produced glass layers, and any other contaminants.

6. Using vacuum evaporation, apply contacts to the major faces. The contact to the front surface is of open construction, allowing as much sunlight as possible to enter the cells: to minimize the resistive losses in the shallow diffused layer, the open contact has thin grid fingers arranged to pervade the front surface as thoroughly as possible. The contact to the back surface is arranged to cover at least 90% of that surface.

7. An antireflecting coating is applied.

8. Usually a heat-treatment step is included to decrease the contact resistances and perhaps to improve the AR coating properties; this heating also improves the adhesion of contacts and coating to the silicon.

9. Finally in some cases the faces of the cell are masked, and the edges are etched to remove metals and damaged silicon, to decrease the edge leakage, and thereby to improve the PN junction performance.

2.3.2 Mechanical Considerations in the Process Sequence

The sequence outlined above requires mechanical handling of the slices at and between the various process steps. Comments will be made with the same sequence order as above.

2. During slicing, there is chance of slice breakage, particularly as the slices are made thinner; this breakage can occur during slicing or in removal from the holding jig, or during post-slicing cleaning.

3. As in 2, there is chance of breaking slices during surface treatment; if this treatment includes mechanical polishing the greatest chance of breakage occurs in removal of slices from the polishing plate, and in cleaning.

4. There is pre-diffusion chemical etching and cleaning, which involves loading and holding in fixtures; the slice must then be loaded and unloaded from quartz diffusion boats.

5. The post-diffusion cleaning again involves the same fixture problems as in step 4. In addition, if the diffused layer must be removed from the back surface, this involves masking

of the front surface followed by removal from the masking means. For thin slices this removal step has proved to be a constant means of breakage.

6. To hold the samples for contact deposition, especially when forming the thin grid lines, carefully designed fixtures are needed, wherein the silicon slices must be firmly held in location; there is chance of breakage in loading and unloading these fixtures.

7. As for 6, the slices must be held in, and loaded to/from special fixtures.

8. The heat-treatment step has the same breakage problems as those discussed for the diffusion step above in 4.

9. The methods used to protect and then unmask the slice faces during edge clean-up have proved to be a likely means for breaking thin slices.

Below we will discuss in more detail the mechanical problems during processing of thin slices.

2.3.3 Electrical Considerations for Thin Cells

This section describes the electrical difficulties expected with thin cells, and shows the remedies available. There are possible losses in the three main photovoltaic parameters, Isc, Voc and CFF.

(a) Isc Losses - These can be caused by:

(i) Decreased absorption in the thinner silicon layer,
(ii) reduced active area,
(iii) inefficient carrier collection,
(iv) stresses in the silicon, and
(v) surface reflectivity.

Possible remedies for these losses are respectively:

(i) Add surface texturing to change absorption path, and also to reduce reflectivity; enhance reflection of unabsorbed wavelengths for second pass.
(ii) Apply grid pattern in finer lines; this is possible even when very shallow PN junctions are used.
(iii) For greater carrier collection near the surface, very shallow PN junctions can be used; for better collection in the bulk silicon, a retarding electric

field can be provided near the back surface. This field, often called a Back Surface Field (BSF) is provided by a transition such as P/P+ at the back surface of an N/P cell.

(iv) Stresses in the silicon can be reduced by reducing thermal strains, and also by etching surfaces to relieve stresses, and

(v) Surface reflectivity can be reduced by better AR coatings, and surface texturing.

(b) Voc Losses - These can be caused by:

(i) Decreased Isc,
(ii) use of higher resistivity silicon,
(iii) increased "saturation current," (I_o), and
(iv) stresses.

Possible remedies are respectively:

(i) Increase Isc by means shown in (a) above,
(ii) use lower resistivities,
(iii) add a BSF to higher resistivity silicon, and
(iv) as for (a) (iv) above.

(c) CFF Losses - These can be caused by:

(i) Increased saturation current I_o
(ii) increased sheet resistance,
(iii) increased bulk resistance,
(iv) increased contact resistance, and
(v) decreased shunt resistance.

Possible remedies are:

(i) Use higher resistivity silicon +BSF,
(ii) use more pervading grid pattern,
(iii) use lower resistivity silicon,
(iv) P+ layer reduces back surface contact resistance,
(v) the processing must remove damaged surface layers or excess metal around the perimeter of the PN junction. In addition, the contact metals must not penetrate the PN junction; this becomes a more severe problem when very shallow PN junctions are used.

3.0 PROCESS SEQUENCE CONSIDERATIONS FOR THIN CELLS

3.1 Requirements of Process Sequence

The previous section outlined the remedies available to give improved output from solar cells made from thin slices. The most promising combination would include:

A low stress thin slice, with surface texturing. The choice of resistivity and orientation must be made according to the matching of the overall steps.

These thin slices must have a very shallow PN junction, necessarily accompanied by good surface coverage by a many fine-line grid pattern, using metals which have good conductivity and which do not degrade the shallow PN junction.

In addition the slices must have an effective back surface field, and perhaps a back surface which enhances reflection of longer wavelengths.

Finally, an improved AR coating must be applied with high transmission in the near ultra-violet, the region where enhanced response is obtained by the shallow junction; in addition, these AR coatings can show increased cell output when a cover is applied to the cell.

Clearly, many of these desirable process steps are those which modern space cell technology has developed. The present work sought to determine the best process sequences which included as many as possible of these steps, and applied them successfully to thin slices.

3.2 Possible Conflict in Process Steps

On examination of the optimum combination of process steps, several conflicts can be seen in the requirements for the separate steps.

(a) The method used to thin slices must result in low-stress conditions. If etch thinning is used, it may be affected by both the resistivity and the orientation of the slices. To minimize breakage, or to obtain more effective combinations of process requirements, there is a possibility of completing some of the process steps on thick slices, and then thinning the slice before completing the full process sequence.

(b) Effective surface texturing is very dependent on the slice orientation; to date (100) - oriented slices have been textured most effectively. This orientation is favorable for good shallow PN junction properties, but may be less effective than the (111) - orientation if a planar alloy front is required, when alloying is used to form the BSF. In addition, an effectively textured slice may add to the difficulties in providing a satisfactory fine grid line pattern (see below).

(c) For textured surfaces (and even for highly polished surfaces) a continuing problem in this work has been the formation of a satisfactory fine-line pattern. In principle, two methods are available to form the pattern. One method is an extension of the normal manufacturing method, where a mask with very fine etched slots is held close to the slice surface during contact evaporation. It has proved difficult to find a supplier of masks with sufficiently fine slots, which can allow an adequate build up of contact metal without lateral spreading. The other method forms fine lines using a combination of photomasks and photoresist. The mask has the required fine line pattern.

Two general photoresist methods are possible:

(i) Where the contacts are applied all over the slices, and then the photoresist is deposited on these contacts, exposed through a mask to allow the resist to remain in the contact pattern, and then the metals are etched away from the required open areas.

(ii) The resist is applied to the slice, and exposed to a mask, to allow resist to be removed in the contact pattern. The contacts are then applied to the open areas in the resist.

For normal cells, the active area (not covered by grid lines and other contact area) can be between 87 and 90% of the total slice area. Using the above methods can result in active area fractions $\approx$90% for a metal mask where the lines are $\sim$30 um wide because the combination of the mask lines, and the degree of registration are not optimum. Any slice warpage or the use of a non-flat surface finish are not favorable for increased active area fractions. Using the photoresist methods, active area fractions obtained have ranged from 90% to around 96%, the latter case for highly polished thick slices.

(d) There is increased chance of metal leakage through the shallow PN juction when depositing metals onto textured surfaces, or when the slices are warped, giving leakage under the mask defining the contact pattern.

(e) The other continuing problem has been the formation of an effective BSF. These fields are not completely understood in their action; earlier work showed that the like-doped layer (P+ for the N/P cells) must penetrate about 1 μm into the P-silicon, and that usually the minority carrier lifetime in the bulk silicon must exceed a certain minimum value. The manifestations of an effective BSF are an increased Voc (cells made from 10 and 100 ohm-cm had Voc increases of 50 and 100 mV respectively) to 590-600 mV and enhanced long wavelength current response. For silicon in the lower resistivity ranges (~3 ohm-cm) the Voc-values are around 590-600 mV, and thus the effects of the BSF are more difficult to confirm in these lower resistivities.

Two methods have been used to provide effective BS fields in P-silicon: These methods involve the alloying of aluminum, or the diffusion of boron.

The alloy processes typically use temperatures in the range 650° - 850°C for up to several hours; these temperature cycles allow reasonable lifetimes to be maintained. The problems in the alloy methods lie in the chance of formation of globules of aluminum during the alloy cycle; these globules introduce local stresses in the slices and are a frequent cause of breakage when slices are held in various fixtures. There is another problem, in that to retain a very shallow PN junction, the N+ diffusion should be performed after the alloy process; in this case the phosphorus diffusant may have adverse interaction with the BSF.

Some tests were quite successful when the N+ layer was in place during the alloying. The reduction in cell output because of the deeper PN junction, was somewhat offset by the more effective BSF, and the slight relaxation in the need to have so many fine grid lines.

The boron diffusion process involves higher temperature (~1050°C) for ½ - 1 hour: this temperature exceeds the N+ diffusion range, requiring that the P+ diffusion be performed before the N+ step. At the higher temperature of formation of the P+ layer there is greater chance for obtaining reduced carrier lifetime.

For either method there is the added possibility of applying protective films to one face of the slice while forming the BSF, or the N+ layer. Such films must be impervious to the various materials which must not contact the surface, and must in turn be easily removed without reducing the cell performance (or increasing the chance of breakage).

(f) Finally care is needed to ensure the best heat treatment to enhance the required cell properties without degradation of the junction, the carrier lifetime or the BSF.

3.3 Difficulties in Evolving the Best Process Sequence

Many of the tests were made to check how to reduce conflict between the several requirements to be met for making high output thin cells. Most of the early tests which produced cells of inferior output (or broken cells) were carried out deliberately in the lower end of the thickness range (<4 mils) with the initial assumption that when the problems were solved for fabricating these thin cells satisfactorily, the methods developed would be readily adaptable to the thicker slices. This plan gave rise to very poor overall yields. Compounding these problems were attempts to combine various texturing methods with these fabrication processes for the thinnest slices.

Illustrative of the interactions which led to severe yield losses are the following:

(a) Slices were thinned by combination of slicing to around 10 mils, and chemically etch-thinning to below 4 mils; in some cases, a texture-etch was used for the last 1-2 mils of thinning. These slices had some residual strain.

(b) These residual strains led to increased breakage in the various handling steps.

(c) In addition the photoresist process was not easily adaptable to the textured surface, requiring additional processing, with even more breakage.

In other cases as mentioned above, the methods used to develop the BSF gave separate problems, increasing both the chance of breakage and also reducing the electrical output of the cells. Some of the boron diffusion methods left the thin slices severely stressed; the aluminum alloy method often led to globules of aluminum, with increased local stress around the globules, and a high chance of breakage when the slices were pressed firmly in the various fixtures. As a result of this concentration on the problems of the very thin cells, the hoped-for isolation of the problems associated with the various

steps, their interaction, and their solution, was not completely achieved. However, several conclusions were possible, and as a result, two usable process sequences which gave good quality cells were finalized. In these sequences, the only process missing from the optimum sequence (as discussed in section 3.1 above) was the provision of complete texturing. It was possible to apply partial surface texturing however, as discussed in the description of some of the cells shipped in groups 3, 4, and 5.

3.4 Conclusions Drawn From Process Tests

These conclusions are the result of the various tests, and are discussed in the following process sequence order:

(a) Silicon selection
(b) Slice thinning
(c) BSF formation
(d) N+ diffusion
(e) Grid pattern formation
(f) AR coating
(g) Overall handling characteristics

(a) Silicon Selection. Many tests were run with (111) oriented slices, because in early tests, they showed slight advantages in electrical output, especially in Voc. However, (111) slices proved difficult to texture effectively, and with a matte surface finish this orientation was difficult to combine with photoresist operations. Unexpectedly, for a given chemical etch, and a given slice thickness, the breakage rate was much higher for (111) oriented slices than for the (100) orientation. Therefore for the third and later shipments, (100) - oriented slices were used.

The electrical output of cells was comparable for the 2 ohm-cm and 10 ohm-cm resistivity ranges used, with a proviso that for the 10 ohm-cm range, a more effective BSF was essential. This meant that the upper limit on output for a given thickness range and process sequence was similar for the two resistivity ranges, but that more 10 ohm-cm cells had low output if the BSF was not adequately formed. For this reason, the larger runs (#4 and 5) used only the lower resistivity.

(b) Slice Thinning. Three broad methods were used:

(i) Slices were lapped and polished (chemical-mechanically) to around 10 mils, and were thinned further by etching, usually with a polish-etch. These samples often revealed stresses, and in particular for slices thinner than 3 mils, holes were often seen in the slice, showing the preferential attack of the etchant on these regions of localized stress. In addition these slices often warped more, particularly after contacts were applied.

(ii) Slices were cut 8-10 mils thick, and then polish-etched to 4 mils; these slices had the same disadvantages as those in (i).

(iii) Slices were cut 8-10 mils thick, and with or without slight lapping, were etched down using a non-polish etch, usually with KOH solutions. This etch left a matte surface, and the resulting slices had less stress, as shown by lower breakage rates, and minimum warpage.

NOTE There were other attempts made to process either the front surface (diffused with contacts and perhaps coating) or the back surface (BSF plus contact) before protecting this surface and thinning the slice, and then completing the appropriate surface. These tests were not successful, mainly because the full requirements could not be met for the various surface processes e.g. the BSF heat treatment had adverse effects on the diffusion and front contacts.

Along the same lines, tests of various masking layers which could protect one completed surface while the other surface was processed were generally unsatisfactory. One exception to this is described below in 3.4 (g).

(c) BSF Formation. As described above there were problems associated with both general methods tried, namely boron-diffusion and aluminum-alloying. Both processes were best performed before N+ diffusion. The best method overall in this work used aluminum alloying, often with a surface layer (sprayed on glass or SiO_2) applied to minimize balling up; this surface layer was removed after the alloy cycle (or after N+ diffusion) to allow a good back contact to be applied. The alloy cycle most used was 750°C for 2 or 4 hours.

In all tests, it was more difficult to demonstrate the inclusion of an effective BSF for low resistivity silicon. The reason was that Voc was already near the range expected with the BSF (i.e. $\gtrsim$580 mV), and it was often difficult to ascribe increased long wavelength response to the BSF rather than to the increased active area, or the improved antireflective properties of the coated slices. For 10 ohm-cm slices, an effective BSF could be observed easily. As can be seen by the shipment summary, equivalent cells (at a given thickness) could be produced with a good BSF on both resistivity ranges: however, the chance of lower output cells was less for 2 ohm-cm silicon, and thus was selected for shipments 4 and 5. The generated current observed on the shipped cells indicated that some increased current resulted from bulk reflection of unabsorbed sunlight at the silicon-aluminum interface.

(d) N+ - Diffusion. Both $POCl_3$ and PH_3 were used satisfactorily as diffusants. The system finally chosen used $POCl_3$, and an intermediate sheet resistance range (60 to 150 ohm/square) which still gave good short wavelength response (see analysis of shipped cells, section 4.0).

(e) Grid - Pattern Formation. As described above two methods were used, namely evaporation through a metal shadow mask with fine slots to give the grid pattern,or evaporation through slots formed in photoresist by a photomask. Most of the tests on slices thinner than 4 mils used the shadow mask, but as mentioned, the high breakage rate (especially with warped slices) did not yield good cells. In the shipped cells mostly grids were applied with the photoresist method, and with some difficulty, this method was compatible with thin slices and matte surfaces, as shown by the results on the last two shipments, #4 and 5. (See section 4.0.)

(f) AR Coating. Ta_2O_5 was used in all tests; this coating has advantages in good short wavelength transmission, and in high refractive index, giving a "cover gain" when the cell is covered. Provision of a good AR coating was the least problematic step in this work.

(g) Overall Handling. Experience led to improved fixtures for the critical steps described in2.3.2 above, or for any additional steps such as the photoresist exposure; in addition, extra operator care reduced mechanical losses.

The improved etch-thinning methods relieved strain on some of the mechanical steps.

A major advantage was gained in removing the need for "back etching" to remove the N+ layer from the back surface. This was achieved by applying a protective layer to the back surface (either metal or dielectric) before diffusion, to prevent an N+ layer being formed on the back surface. When the aluminum-alloy method was used, the aluminum provided a diffusant-barrier. Removal of the need for masking and back etching reduced breakage considerably.

The other process step which had caused severe breakage was the masking of the major faces of the cell, to allow edge clean-up by etching . As the stresses in the slices and warpage were reduced, this step was completed with reasonable effectiveness.

Similarly, the testing under a simulator was eased for similar reasons, as for the other steps, and better electrical contact could be provided without need for severe pressures from the holding jigs.

This section has discussed the main considerations which led to the final process sequences. The next section discusses the shipped cells, summarizing and analyzing their performance.

4.0 CELL SHIPMENTS

4.1 Details of Cell Shipments

A description of the cell shipments is given in Table 1.

(i) Shipping Lot #1

This lot provided baseline performance for 8 mil cells. Although there were internal comparisons [(100) vs (111), shallow vs medium depth junction, 2 hr. vs 4 hr. alloy cycles] these internal variables did not appear to have pronounced impact. Therefore the whole group is compared in Figure 1 where histogram plots are given of the main I-V parameters namely, Isc, Voc and Pmax. The overall performance was typical of good quality 8 mil cells.

(ii) Shipping Lot #2

2(a) comprised 26 cells extending the 8 mil 2 ohm-cm baseline cells to include a shallow PN junction. Again the differences between the two major orientations and two different alloy cycles were not pronounced. Therefore the performance of the overall group is plotted in Figures 2 and 3. Figure 2 gives histogram data on Isc, Voc and Pmax; Figure 3 plots Pmax vs thickness. These cells are seen to be slightly improved over Lot #1.

2(b) comprised 27 cells made from 10 ohm-cm silicon mostly between 4 and 6 mils. The output of this group was slightly lower than that of 2(a); although Isc was larger, the curve fill factors CFF were lower for 2(b). Both alloy cycles used gave effective BSF fields; in this group the (111) oriented cells gave slightly higher Voc values.

(iii) Shipping Lot #3

3(a) comprised 10 thin (4.2-5.2 mils) violet cells, with a matte surface; the power output was in the mid 60-mW region, very satisfactory for uncovered cells.

3(b) comprised 20 violet cells, 9.3-12.2 mils thick polished surface and with powers in the low 70-mW region, again without a cover.

3(c) included 30 thin cells in the range 4.8-6.5 mils; 10 ohm-cm with polished front surface. As for group 2(b), the Isc values were higher, but the power output (uncovered) was in the mid 60-mW range. The performance of these groups is summarized in Figures 4 and 5. Groups 3(a) and 3(c) used shadow masks to form the grid patterns, resulting in lower active area.

(iv) Shipping Lots #4 and 5

These were 150 and 100 cells respectively 4-6 mils thick, made from 2 ohm-cm silicon with a matte finish. Their performance is summarized in Figures 6 through 9. The cells were screened to reject those with output below 64 mW. The overall performance of these cells is very satisfactory and shows the level of output capable in this thickness range.

Details of the overall yield (for the most pessimistic estimates) was 45%; the mechanical yield to electrical screening was 62%, the electrical yield (cells $>$ 54 mW) was 89%, and the good electrical performance can be seen by the fact that 87% of the cells checked were $>$60 mW, and 70% exceeded 65 mW, all these figures for uncovered cells.

Of the cells screened for shipping, 18% were rejected for visual reasons. Considering that these cells were made mostly in a manufacturing environment, these yield figures are quite promising. Figure 10 shows a tracing of the bounds of the I-V curves (measured for the simulator set with a conventional cell) for the cells in shipping lots #4 and 5.

4.2 Comment on Shipping Lots

The figures summarize the overall performance. The most notable conclusions are that it is possible to achieve good power output from cells down to below 4 mils thick; no severe fall-off in performance with thickness was observed, indicating the process sequences used were achieving many of the conditions listed earlier as optimum. This was particularly interesting for lots #4 and 5, which made use mainly of manufacturing personnel and equipment.

Some additional comments are given in the next three sections.

4.3 Thickness Measurements

The thicknesses quoted in the figures and tables were measured with dial gauges on the finished cells; in most cases, the probe was placed between grid lines, and where possible to avoid any metal lumps. However, the silicon thickness was less than the quoted values; in early tests differences 0.3 to 0.5 mils were estimated. Figure 11 shows the measured mass versus thickness curve; also plotted is the curve for silicon alone, showing that approximately the contacts accounted for about 10 mgm of the weight.

4.4 Cell Area

Measurements on typical cells shipped in lots 4 and 5 showed that the thinning and edge-etching resulted in a slice 3.92 cm^2, i.e. about 2% below the 4cm^2.

Also because of the difficulty in achieving close registration of masks, the active area (not covered by metal) was measured to be around 3.6cm^2; the technology used is capable of achieving active areas around 3.76 to 3.84 cm^2, while maintaining good electrical output.

4.5 Simulator Setting

The cells in shipping lots 1 and 2 were measured using a balloon-flown conventional cell to set the simulator light levels, and with cells at 28°C. For the other three lots, the simulator was set with a balloon-flown violet cell, and the cells were held at 25°C. Direct comparisons showed that the difference in Isc was ~3-3.5 mA, with the second setting being higher.

4.6 Cover Gains

Several separate measurements, using a fused silica cover, with 350 nm cut-on filter, and amyl alcohol to wet the cover to the cells while illuminated by the simulator, gave the cover gain noted in Table 3. These cover gains are appreciable (2.9 to 6% for Isc, 2.7 to 7% for Pmax). Most of these cover gains (as for typical thickness cells) were in the long wavelength response. Thin cells are usually considered to have reduced long wavelength response. These cover gains show that for the cells cited in Table 3, the long wave response was satisfactorily high, because without adequate response, the reduced reflectivity caused by the cover application cannot give appreciable cover gain.

4.7 Speculation

After consideration of the above factors, it is illustrative to estimate the maximum power expected from the cells; it is possible to justify the linear addition of these correction factors. Applying these correction factors to include cover gain (4% increase), full 4cm^2 total area (add 2%), plausible active area (add 4%), we can estimate that the 64-72 mW range for shipped uncovered cells could be 10% higher, namely 70 to 79 mW. Using the same correction factors, a 4.2 mil thick cell which gave 71.5 mW output as shipped could perhaps give 78mW output if the cell had optimum properties.

5.0 CONCLUSIONS

The data presented above gives a good summary of the electrical performance achievable from thin cells (8 down to less than 4 mils) when much of the modern space solar cell technology is applied to these cells; the only technology not included was the addition of complete texturing to the surfaces.

Preliminary measurements at JPL indicate increased radiation resistance for these thinner cells.

A most encouraging feature was the sign that these techniques are already capable of being performed beyond the pilot-line stage, much more towards the manufacturing level.

This work, and other JPL - sponsored work along these lines shows continual approach toward thin cells of high output, for possible use on large space arrays for solar electric propulsion or for orbiting space stations; thus if the overall array system can be suitably designed, cells of this type can make a significant contribution toward possible realization of these large scale schemes.

On a more basic level, the good performance confirms some of the recent theoretical estimates that the design of thin cell structures can maintain much of the output seen for normal thickness cells.

6.0 NEW TECHNOLOGY

The technical results achieved in this work were the result of the application and combination of already existing technology. No specific items of New Technology could be identified.

TABLE 1

DESCRIPTION OF SHIPPED LOTS

Shipping Lot No.	# Cells. (Quantity)	Thickness (t)[e] (mils)	Resistivity (ρ) (ohm-cm)	Orient.	Sheet Resistance ($R_\square$)	BSF_a (^oC-hrs.)	Simulator Setting	Other
#1	43	8	2±1	100 or 111	70-90	750-2 or 4	I*	b, c
#2	(a) 26	8-10	2±1	100 or 111	150	750-2 or 850-1/3	I	b, c
	(b) 27	4-6	10±3	100 or 111	90 or 150	750-2 or 750-4	I	b, c
#3	(a) 10	4-5	2±1	100	60-120	875-1/4	II*	b, d
	(b) 20	9-12	2±1	100	60-120	875-1/4	II	b, c
	(c) 30	4.8-6.5	10±3	100	60-120	750-4	II	b, c
#4	150	4-6	2±1	100	60-120	875-1/4	II	b, d
#5	100	3.8-5.6	2±1	100	60-120	875-1/4	II	b, d

NOTES

* I - Solar simulator set with conventional balloon flight cell, cells at 28°C.
  II - Solar simulator set with violet balloon flight cell, cells at 25°C.

(a) Numbers refer to Al-alloy cycle details, °C-hours.
(b) 2x2 cm, Ta_2O_5 AR coating. Contact grids 10 lines/cm.
(c) Front surface polished.
(d) Front surface matte.
(e) Thickness includes back contact metals; silicon 0.2-0.5 mils thinner.

TABLE 2

OVERALL YIELD FOR SHIPPING LOTS 4 AND 5

A	B	C	D	E	F	$\frac{F}{A}$ %	G	H	I
698	80	18	144	22	434	62	48	80	306

LEGEND

A - number of slices started.
B - number lost in thinning.
C - number lost in evaporation.
D - number lost in front contact formation.
E - other losses.
F - number to electrical test.
G - number <54mW output.
H - visual rejects
I - number electrically and visually satisfactory.

TABLE 3

COVER[a] GAINS FOR TYPICAL CELLS

Shipping Lot	Cell #	Cover	Voc (mV)	Isc (mA)	% Gain	Pm (mW)	% Gain	Simulator Setting[b]
3(a)	97	B	587	153.1		67.6		II
		A	589	159.7	4.3	71.6	5.9	
	98	B	579	143.4		62.7		
		A	581	151.0	5.2	66.5	6.0	
	102	B	580	144.3		63.6		
		A	583	152.4	5.6	67.6	6.3	
	1876-2	B	585	151.2		67.0		
		A	589	158.3	4.7	71.3	6.4	
3(b)	111	B	604	156.5		72.6		II
		A	607	162.5	3.8	75.7	4.2	
	118	B	609	156.8		74.6		
		A	612	161.6	3.0	77.5	3.9	
	122	B	603	156.3		72.7		
		A	606	160.5	2.7	75.0	3.1	
3(c)	132	B	597	151.5		66.9		II
		A	598	157.6	4.0	70.2	4.9	
	136	B	593	154.0		65.8		
		A	595	160.0	3.9	69.0	4.8	
	1903-5	B	585	154.6		65.6		
		A	588	159.7	3.3	68.5	4.4	
	1904-3	B	585	150.0		65.3		
		A	588	159.1	6.0	69.6	6.6	
4	0002-4	B	598	150.9		(c)		II
		A	601	159.0	5.3	↓	7.0	
	0002-6	B	598	155.8				
		A	600	161.8	3.8		4.7	
	0002-10	B	595	154.6				
		A	597	160.4	3.7		4.4	

(continued)

NOTES

B, A, refer to readings before and after cover applied.

(a) Cover - 6 mils fused silica, 350 nm cut-on filter wet-test using amyl alcohol.

(b) I - simulator set with conventional balloon flight cell, Cells at 28°C.

II - simulator set with violet balloon flight cell, cells at 25°C.

(c) Pm - incorrectly read, gain still applicable.

TABLE 3 (Cont'd)

Shipping Lot	Cell #	Cover	Voc (mV)	Isc (mA)	% Gain	Pm (mW)	% Gain	Simulator Setting[b]
4	0002-12	B	595	151.7		(c)		II
		A	596	158.2	4.2		3.6	
	0002-19	B	594	150.3				
		A	596	157.1	4.5		5.8	
	0002-13	B	599	153.7				
		A	600	160.0	4.1		3.5	
	0002-35	B	601	153.7				
		A	602	159.3	3.6		4.0	
	0002-37	B	596	156.2				
		A	598	161.3	3.2		3.3	
	0002-52	B	588	151.2				
		A	589	156.0	3.1		2.7	
	0002-62	B	591	154.7				
		A	591	159.7	3.2		3.3	
	0002-84	B	593	148.6				
		A	595	156.8	5.5		6.5	
	0011-7	B	594	150.2		70		I
		A	597	155.1	3.2	72.9	4.1	
	0011-10	B	591	146.2		67.8		
		A	597	152.2	4.1	71.6	5.6	
	0011-13	B	592	151.3		68.5		
		A	595	155.8	2.9	71.4	4.2	
	0011-14	B	594	148.8		69.4		
		A	597	154.1	3.5	72.1	3.9	
	0011-16	B	595	152.6		68.4		
		A	598	157.1	2.9	72.0	3.9	
	0012-2	B	586	143.8		64.9		
		A	589	148.7	3.4	68.3	5.2	
	0012-5	B	591	146.4		67.5		
		A	595	151.3	3.3	70.5	4.4	

FIGURE 1

HISTOGRAM PLOTS FOR SHIPPING LOT #1

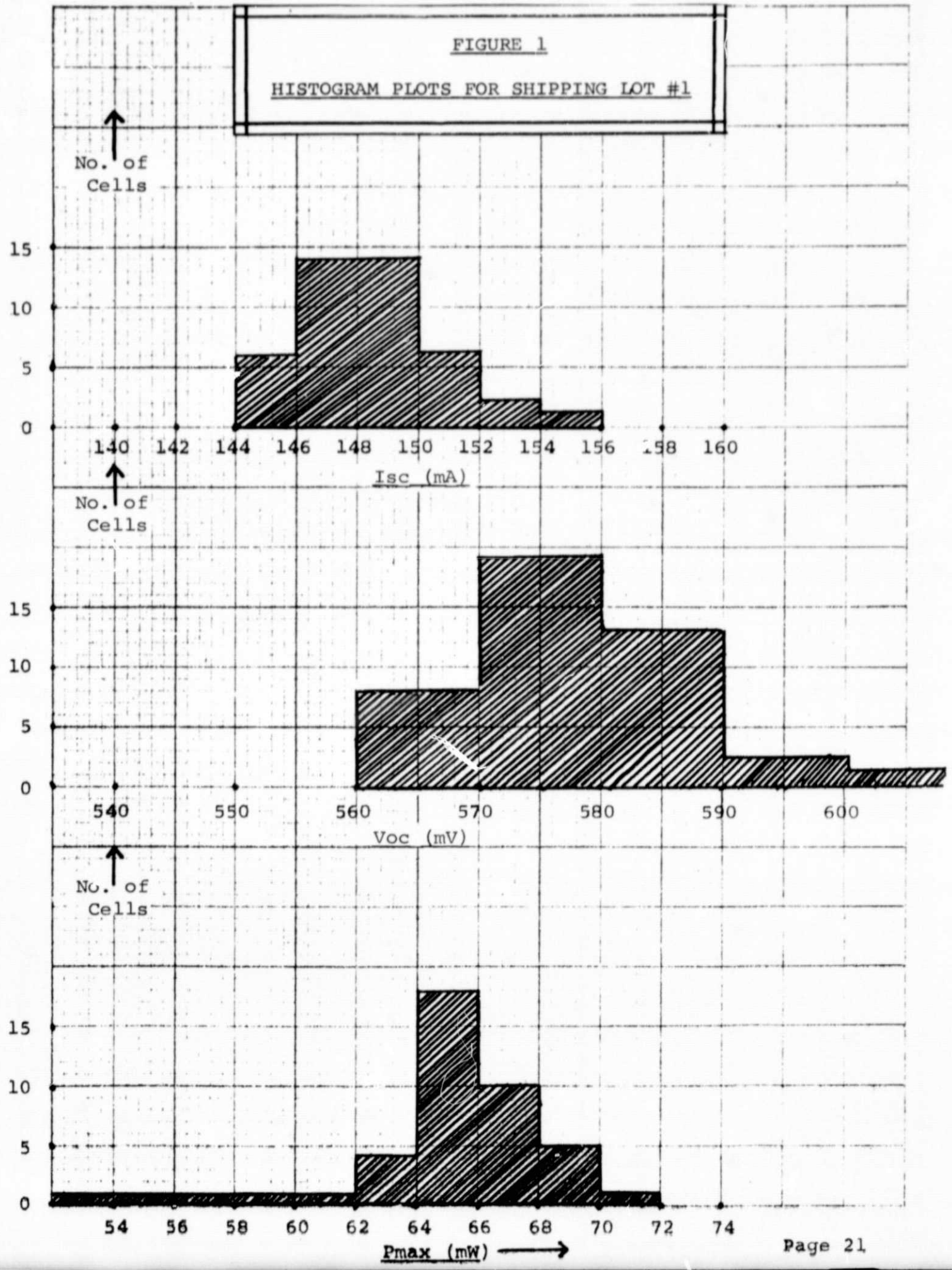


FIGURE 2(a)

HISTOGRAM PLOTS FOR SHIPPING LOT #2(a)

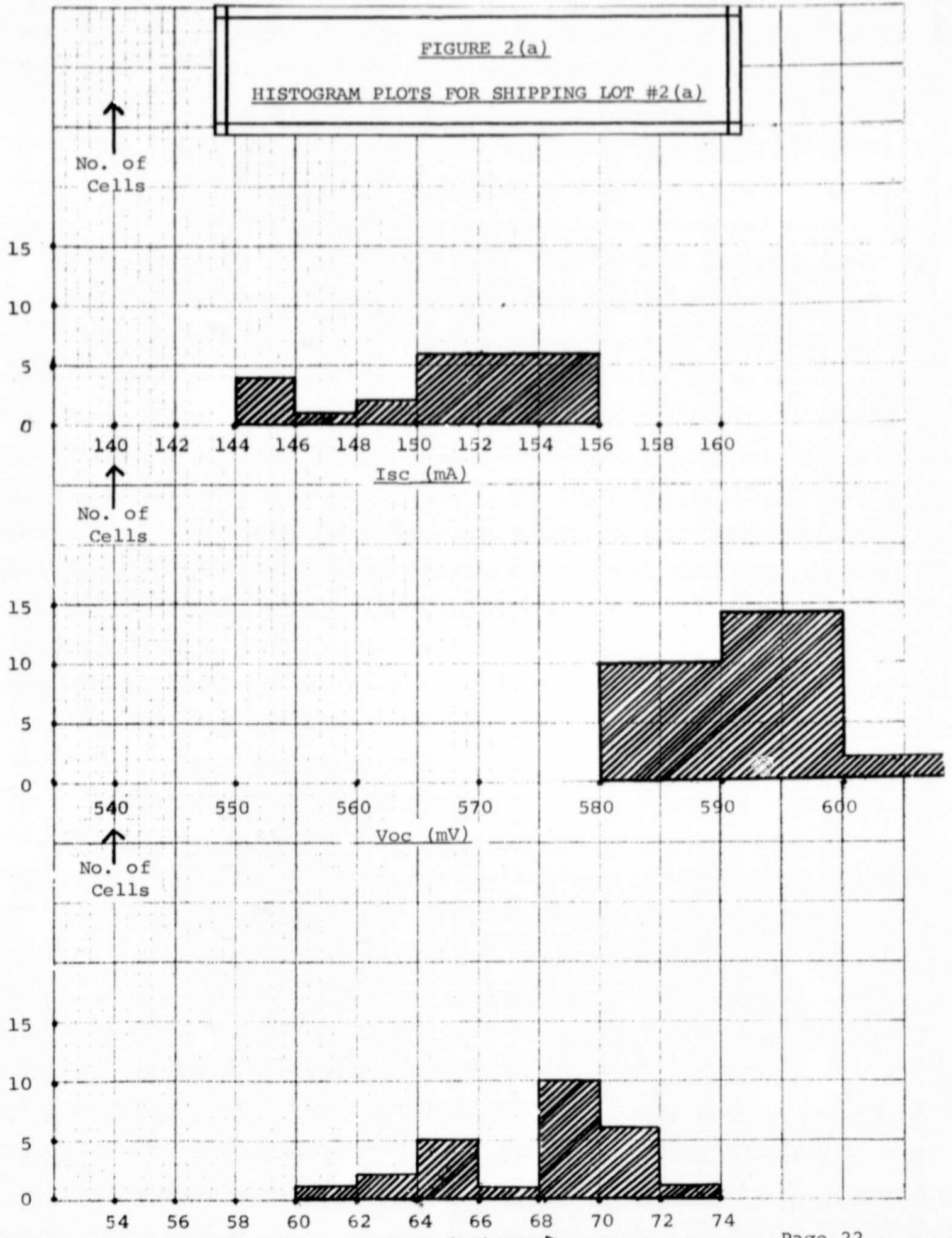


FIGURE 2(b)

HISTOGRAM PLOTS FOR SHIPPING LOT #2(b)

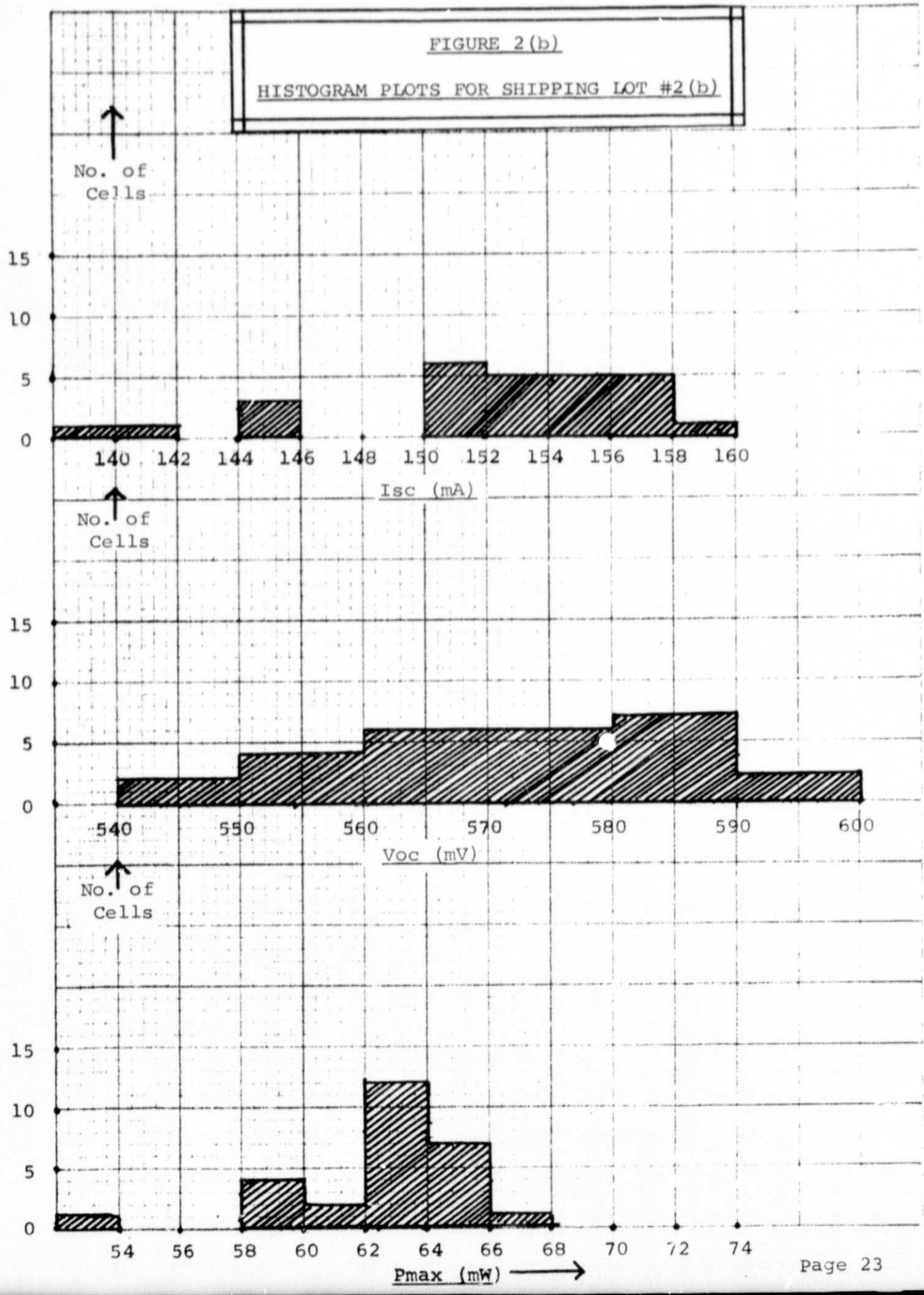


FIGURE 3

PMAX VS. CELL THICKNESS FOR SHIPPING LOTS 2(a), 2(b)

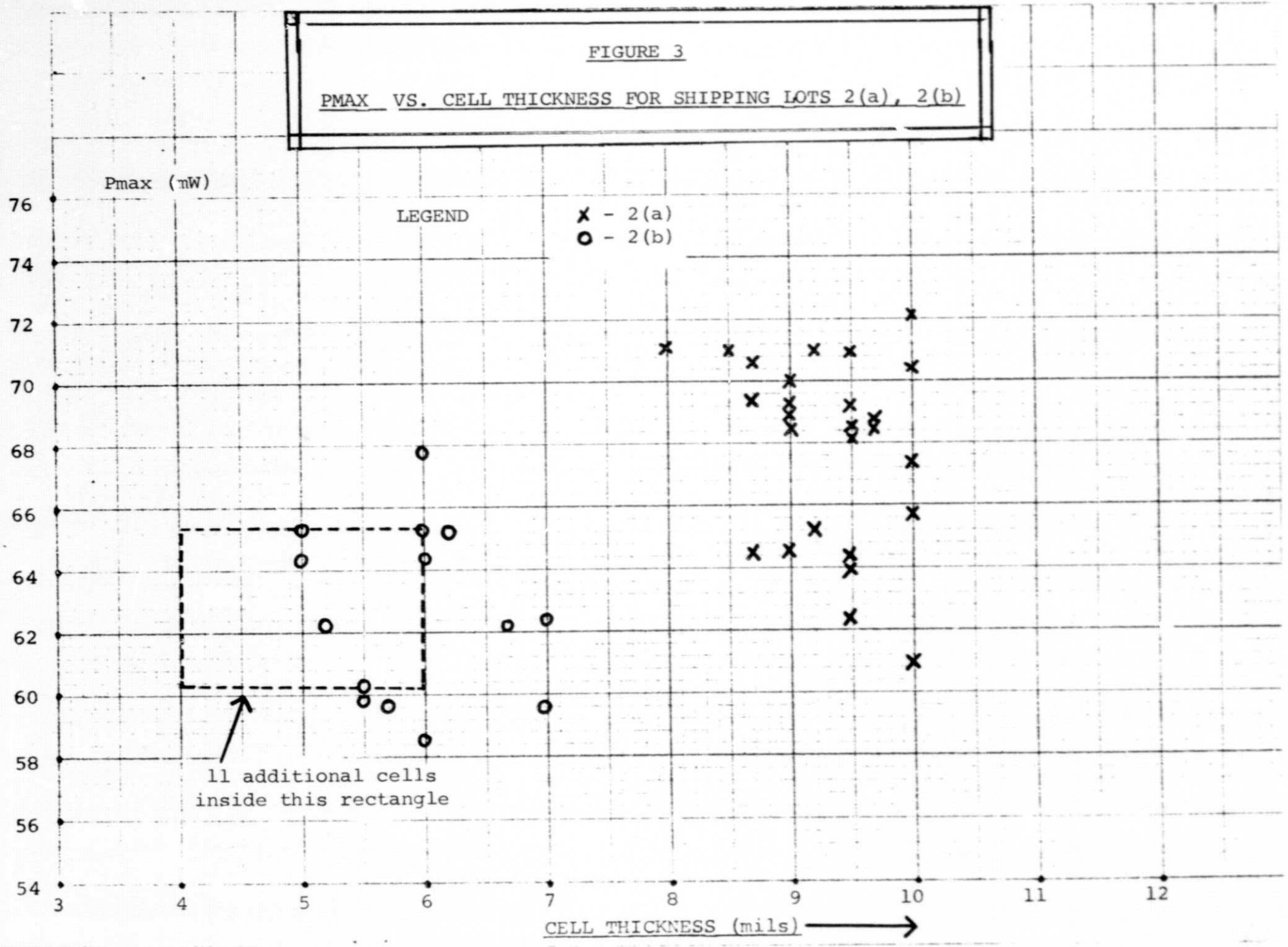


FIGURE 4(a)

HISTOGRAM PLOTS FOR SHIPPING LOT #3(a)

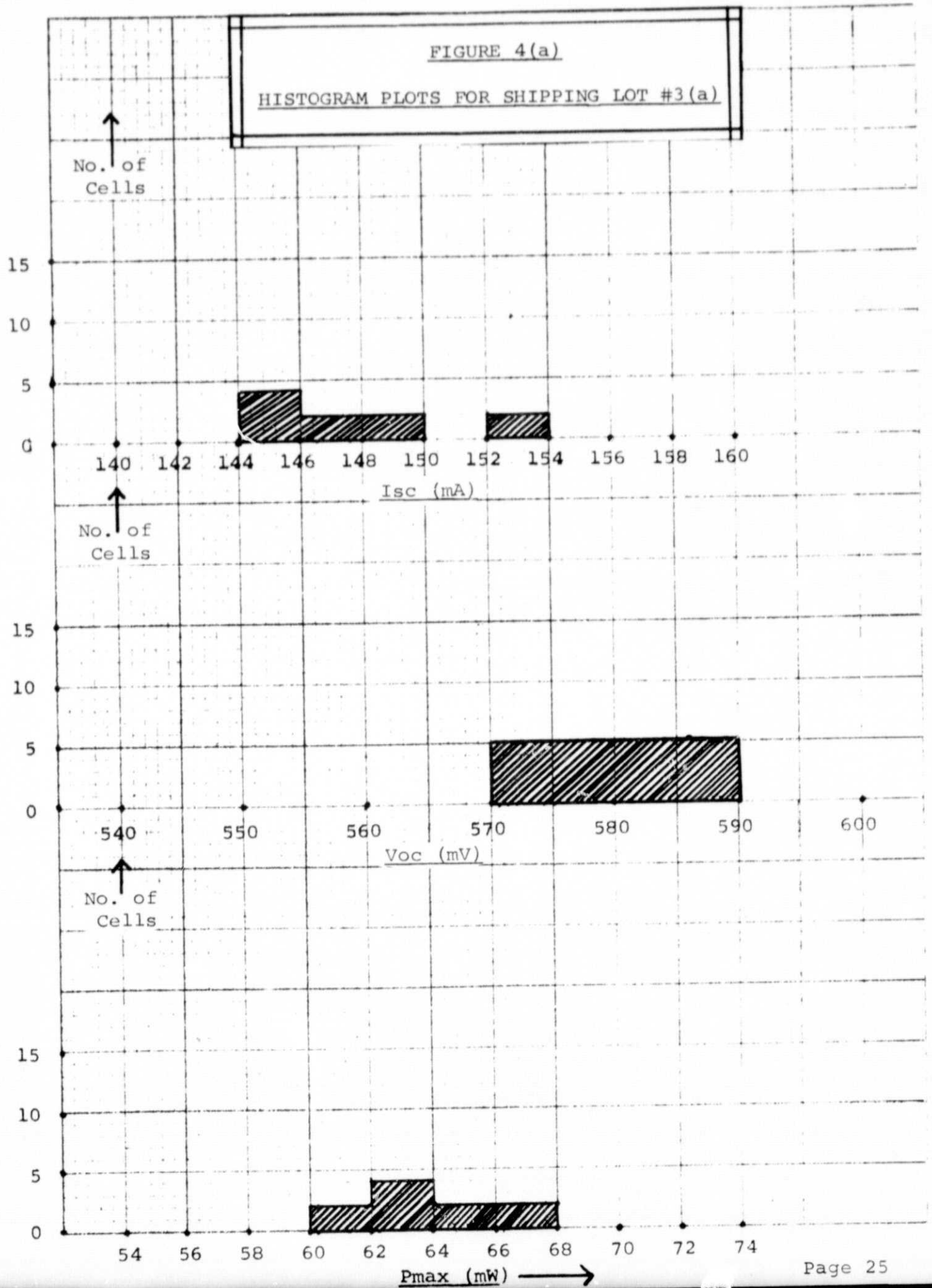


FIGURE 4(b)

HISTOGRAM PLOTS FOR SHIPPING LOT #3(b)

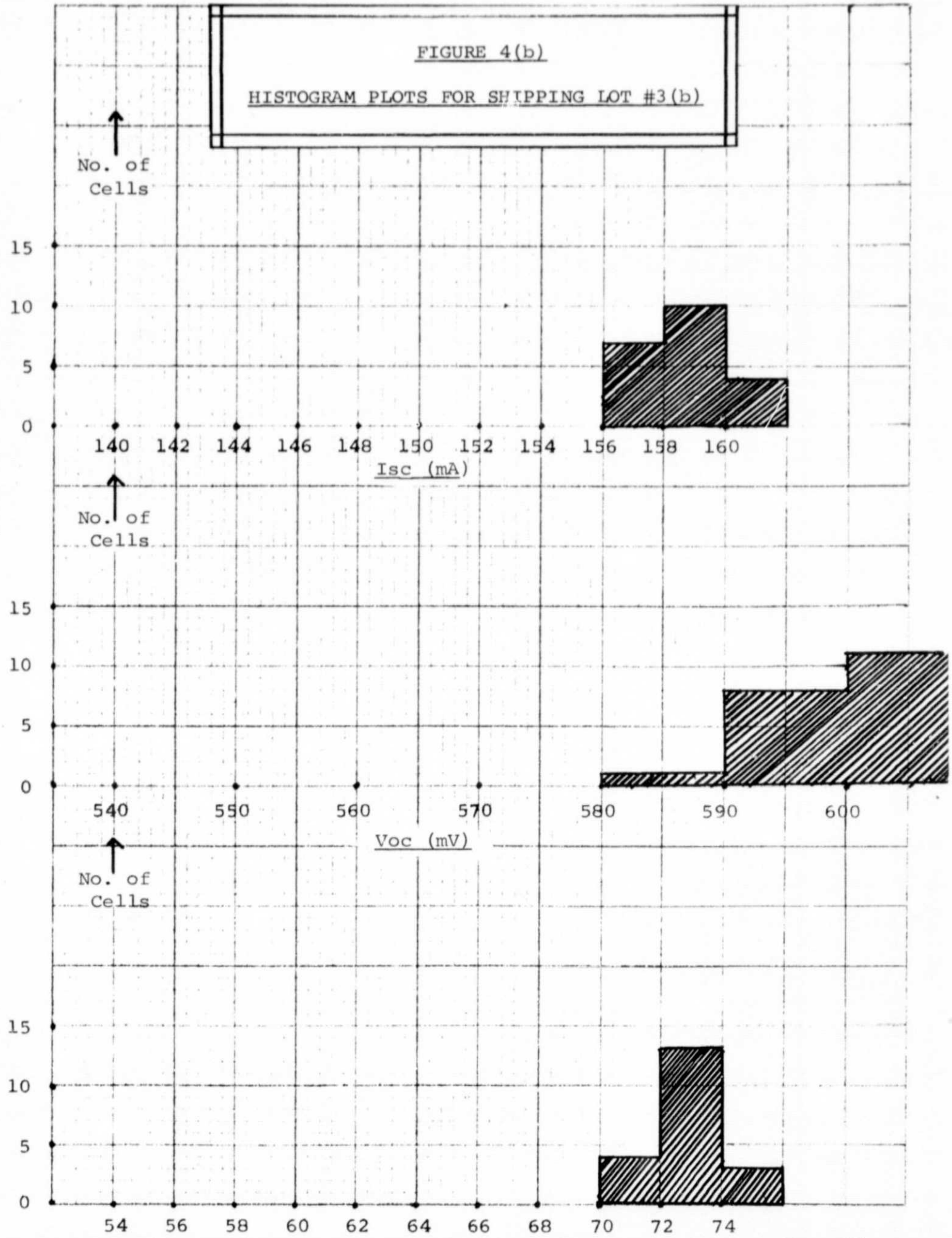


FIGURE 4(c)

HISTOGRAM PLOTS FOR SHIPPING LOT #3(c)

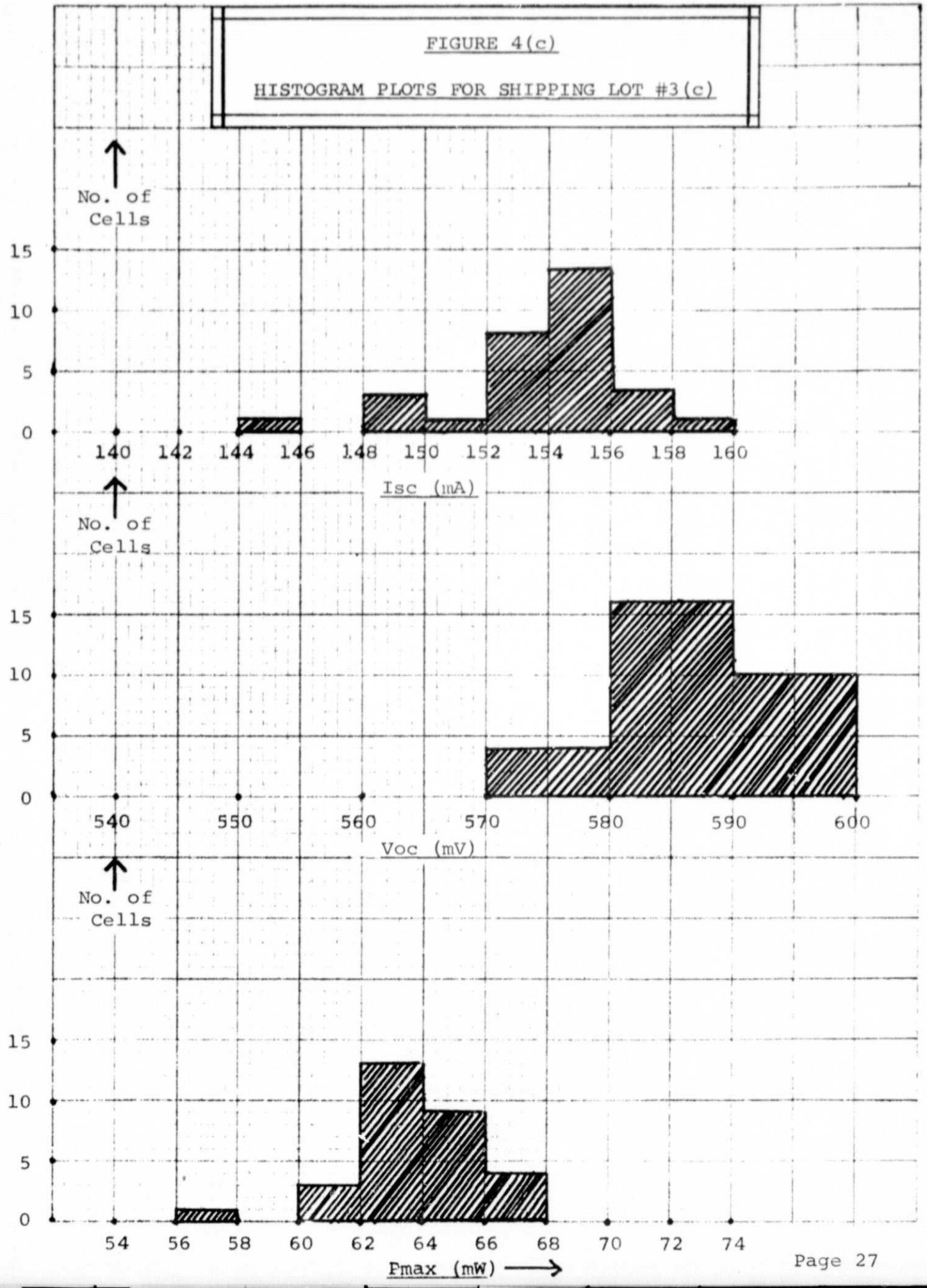


FIGURE 5

PMAX VS. CELL THICKNESS FOR SHIPPING LOT #3

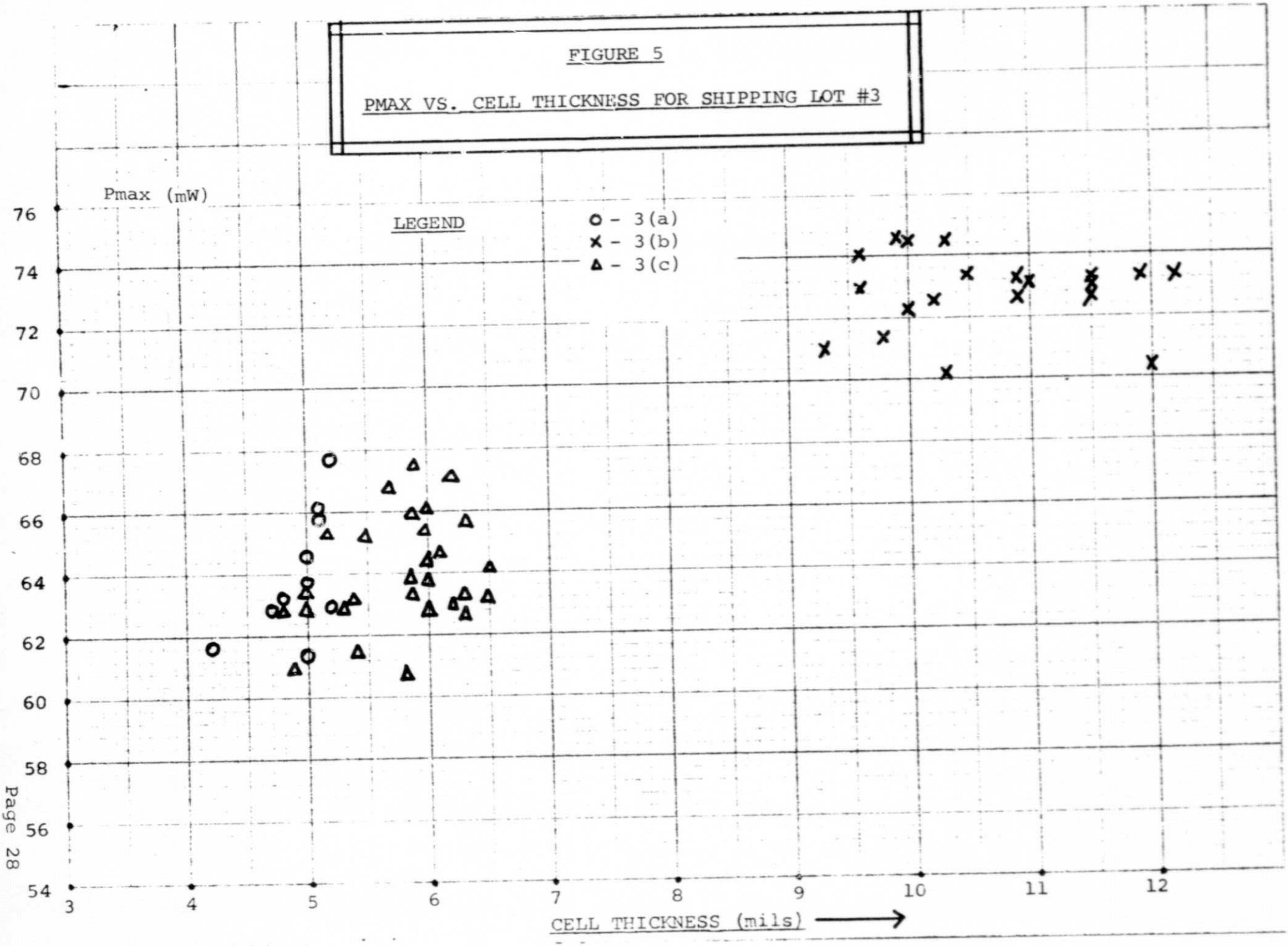


FIGURE 6

HISTOGRAM PLOTS FOR SHIPPING LOT #4

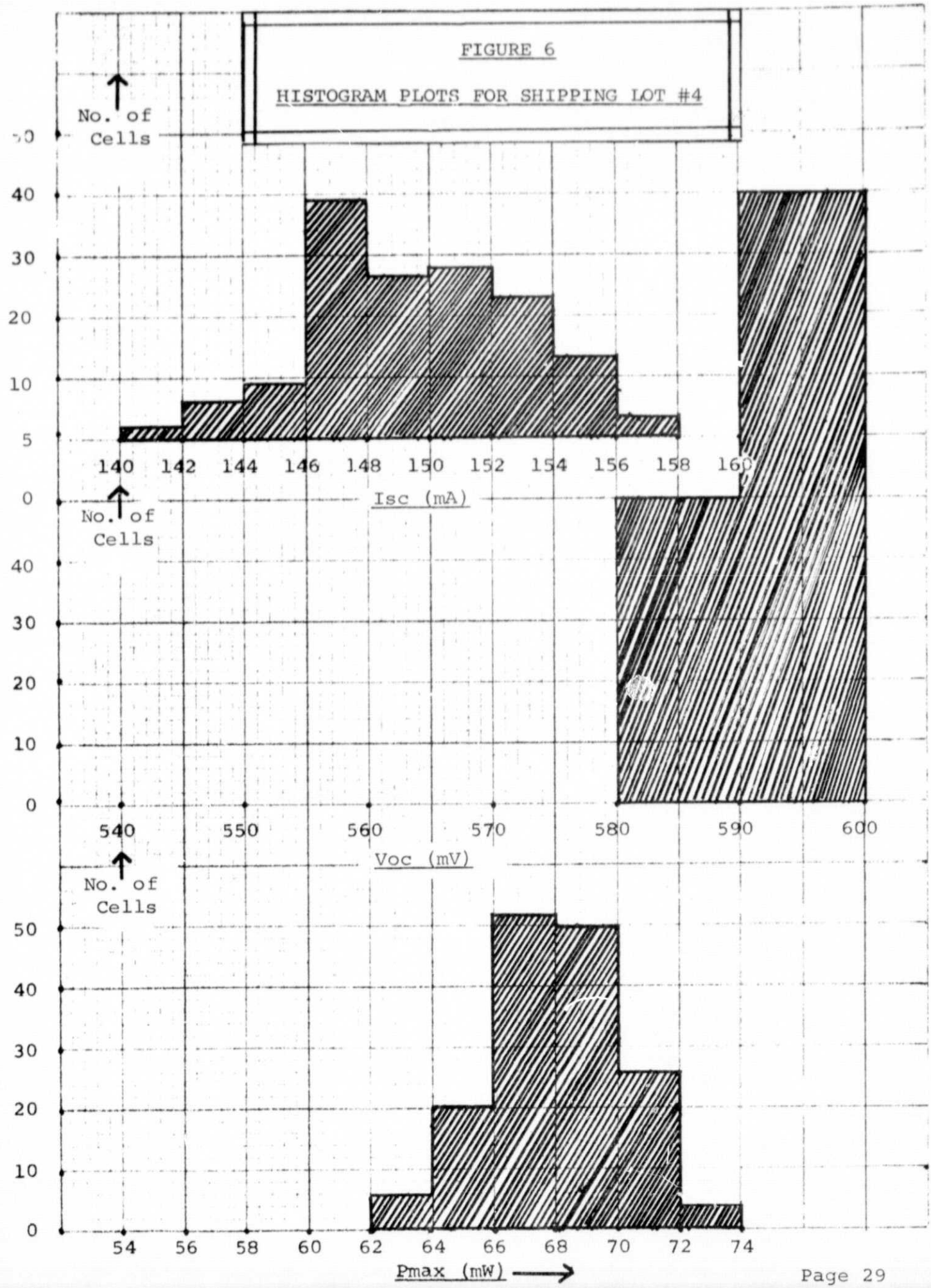


FIGURE 7

PMAX VS. CELL THICKNESS FOR SHIPPING LOT #4

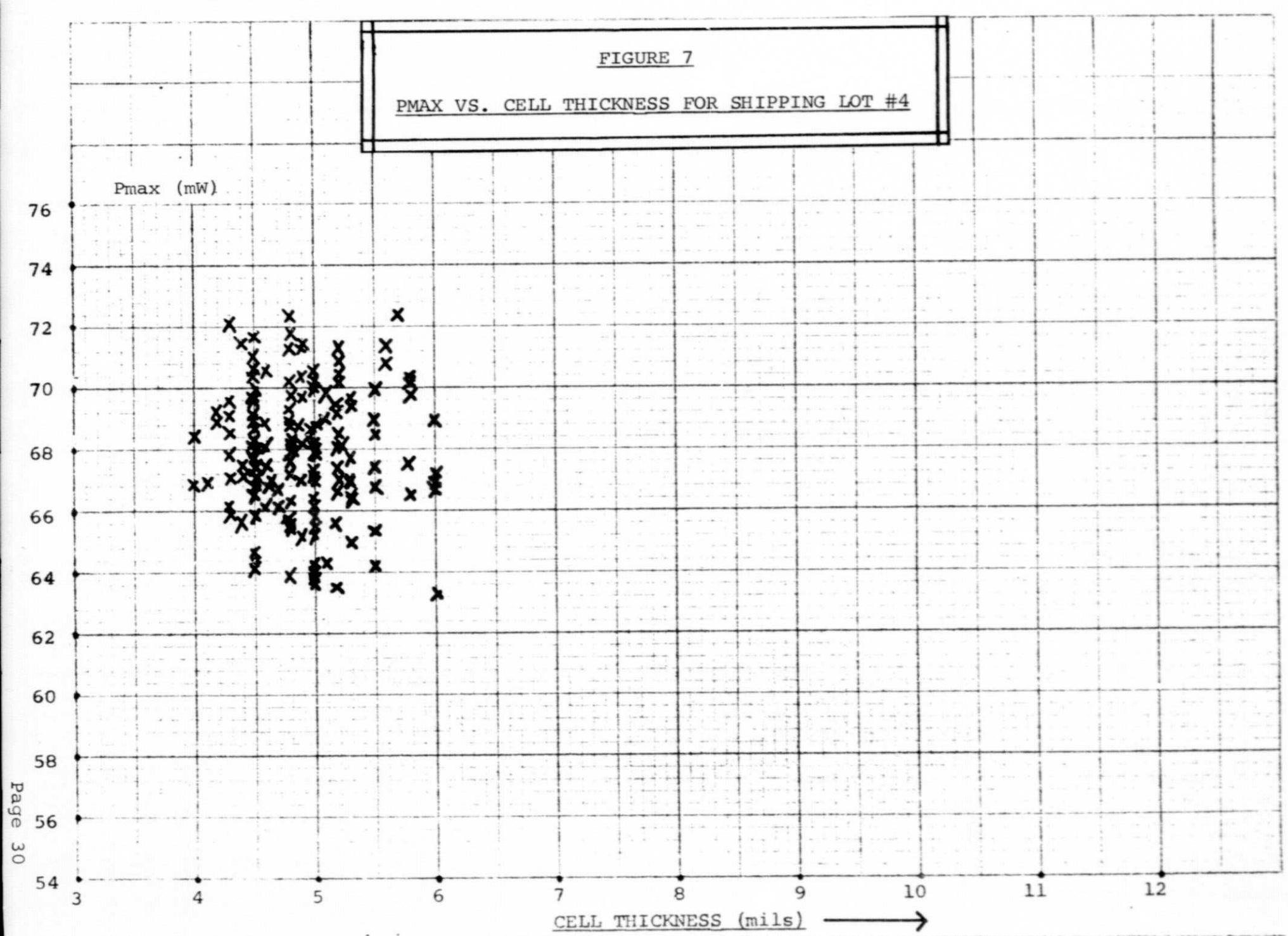


FIGURE 8

HISTOGRAM PLOTS FOR SHIPPING LOT #5

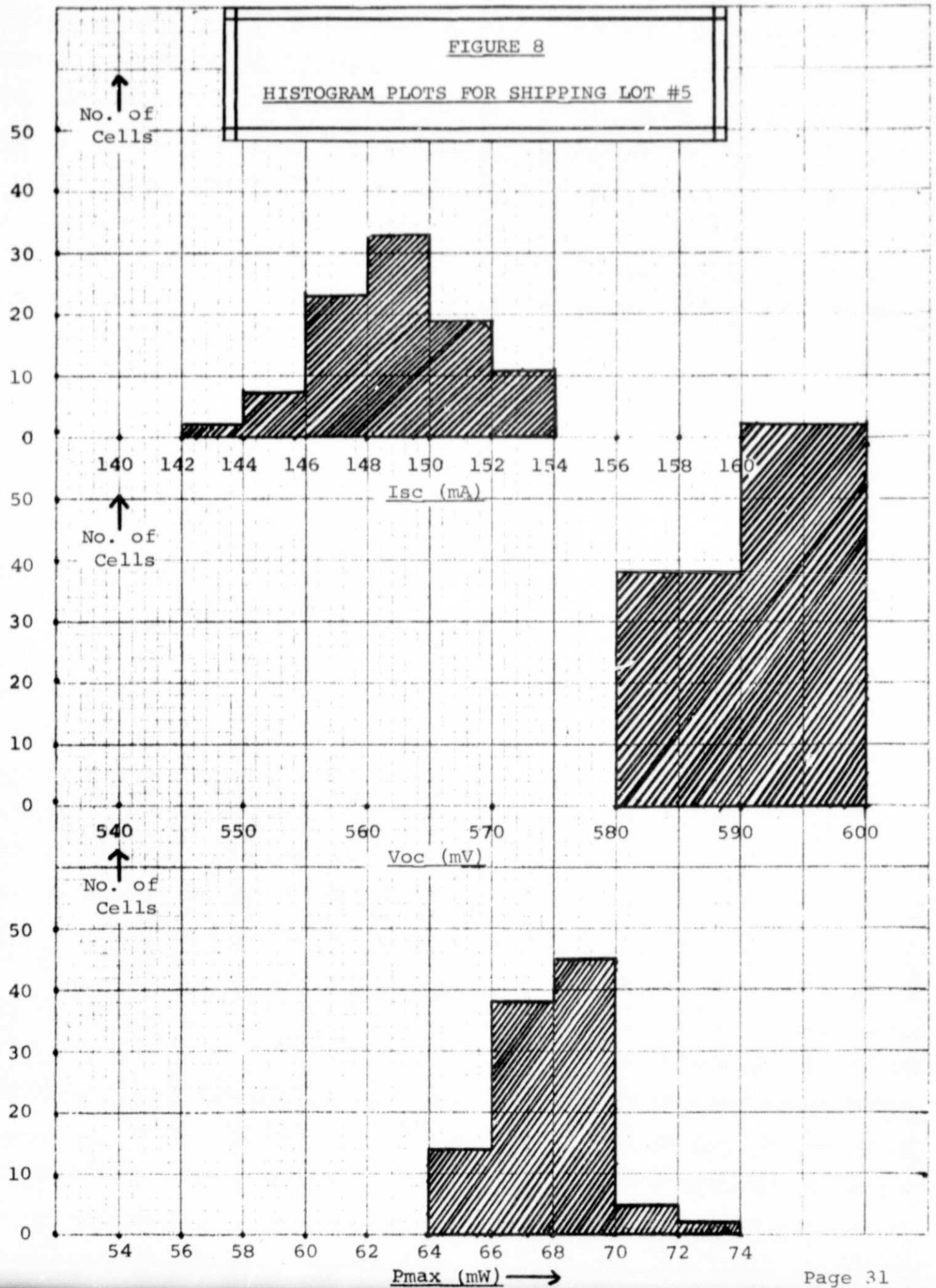


FIGURE 9

PMAX VS. CELL THICKNESS FOR SHIPPING LOT #5

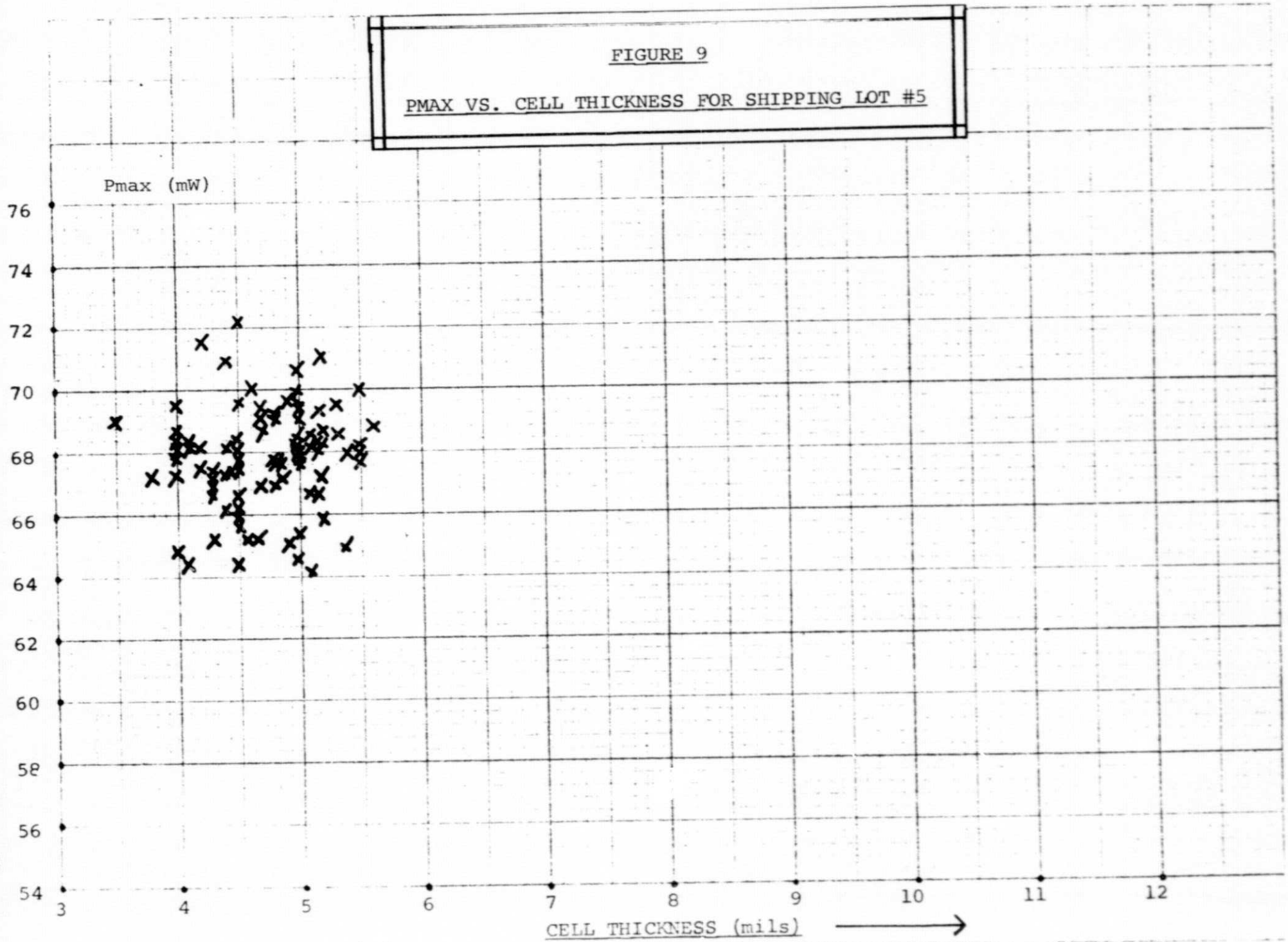
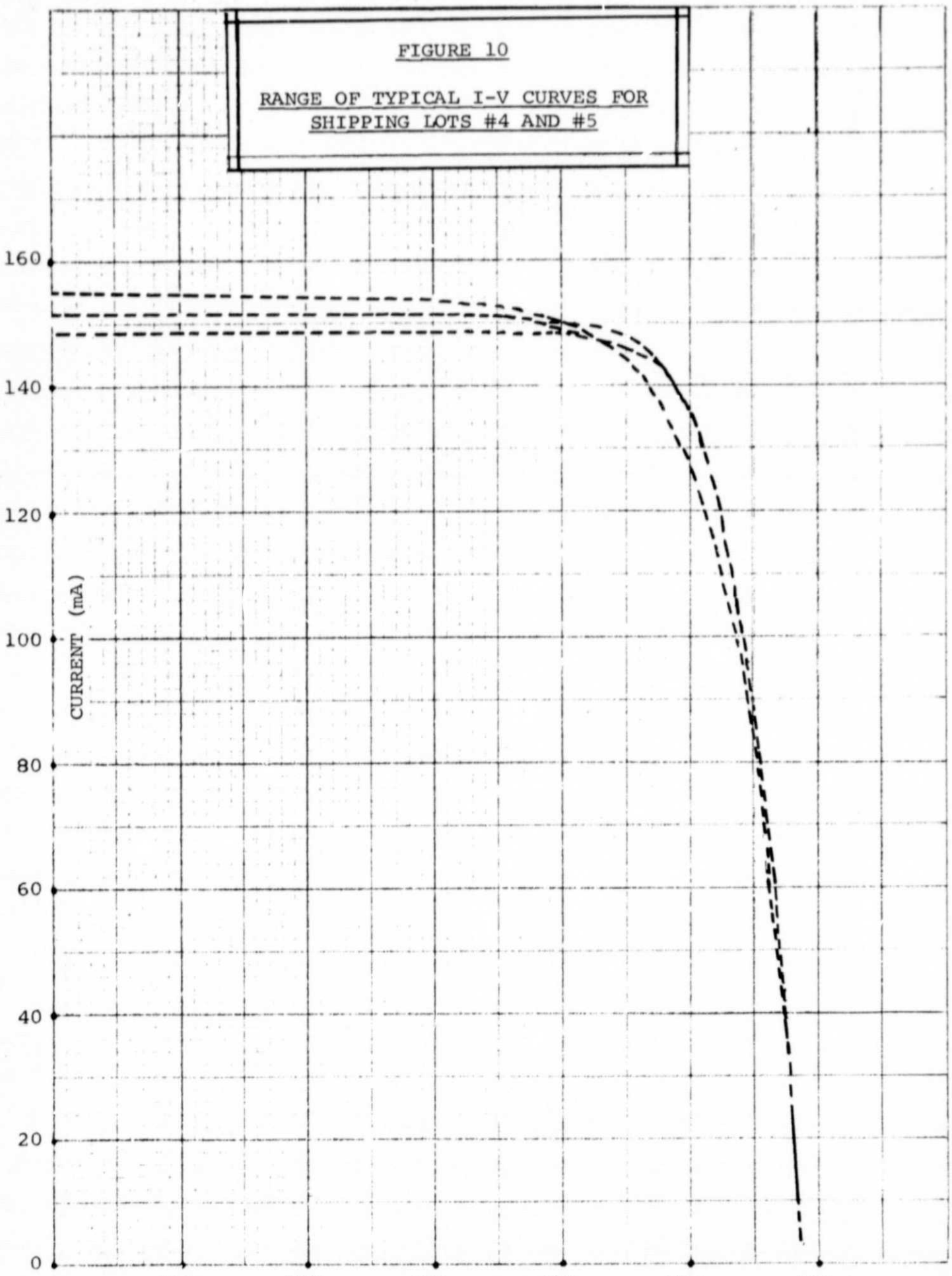


FIGURE 10

RANGE OF TYPICAL I-V CURVES FOR SHIPPING LOTS #4 AND #5



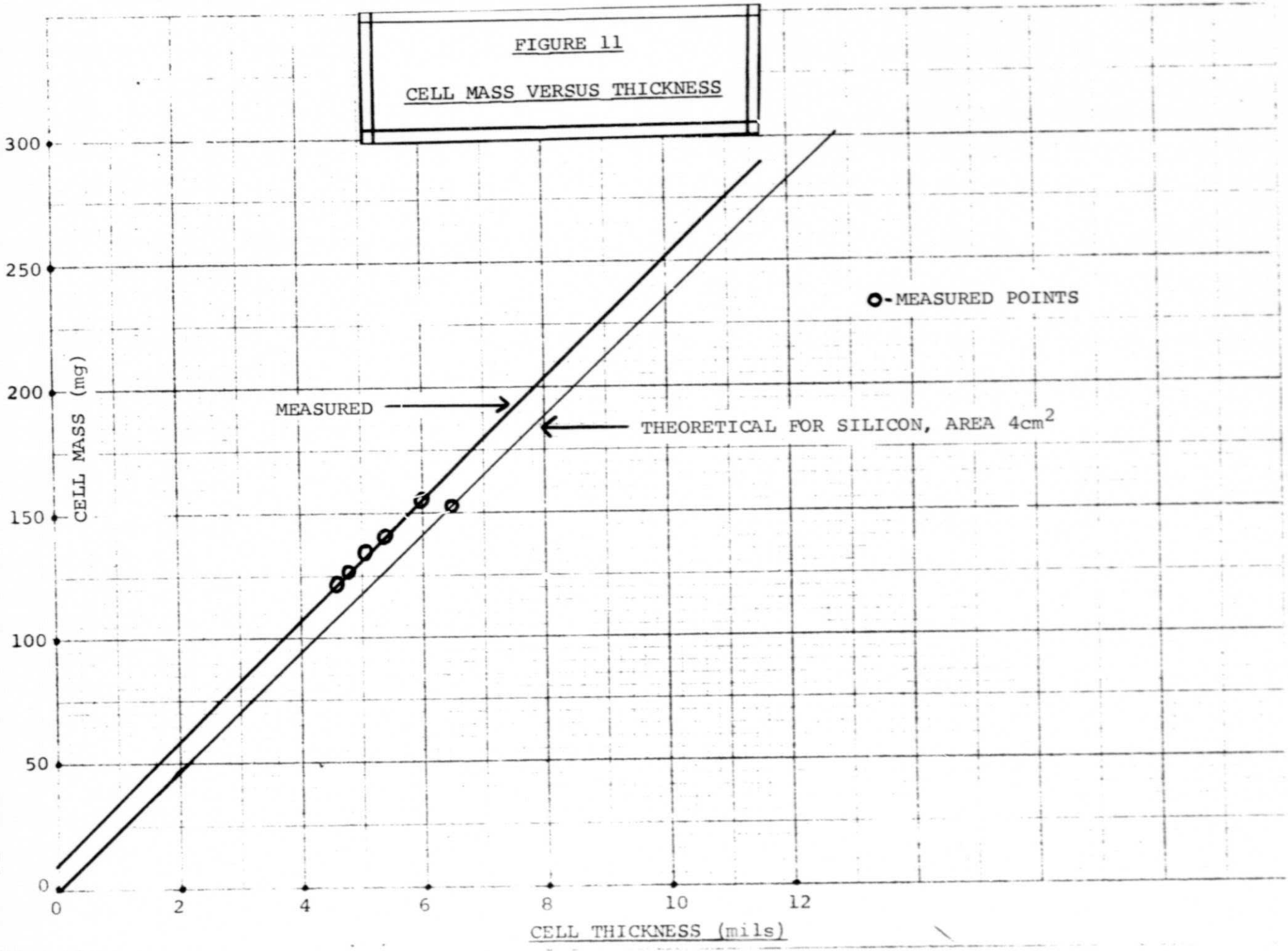


FIGURE 11
CELL MASS VERSUS THICKNESS
300
250
200
150
100
50
0
CELL MASS (mg)
MEASURED
O-MEASURED POINTS
THEORETICAL FOR SILICON, AREA 4cm2
0
2
4
6
8
10
12
CELL THICKNESS (mils)