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DAILY WEATHER DIRECT READOUT MICROPROCESSOR STUDY

FINAL REPORT

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16. Abstract

This report reviews the work performed under NASA contract NAS5-22476. The work completed included a study of the requirements and hardware and software implementation techniques for NIMBUS ESMR and TWERLE direct readout applications using microprocessors. Many microprocessors were studied for this application. Because of the available Interdata development capabilities at Goddard Space Flight Center, it was concluded that future implementations be on an Interdata microprocessor which was found adequate for the task. After that, a conversion to other microprocessors could be considered.

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PREFACE

The purpose of this contract was to develop methods of data handling, information storage, information retrieval, and display to facilitate the use of NIMBUS ESMR and TWERLE direct readout data. During the contract period, the contract objectives were completed through several phases. First a study was performed to determine the data format and data handling requirements for the ESMR and TWERLE applications. Real time software was developed for the handling of the data on the Interdata machine. Finally, a study was performed of the available microprocessor capabilities with emphasis on the use of the Interdata microprocessor capability in light of the available technology at GSFC. It was concluded that real time implementation of a direct readout daily weather data system is feasible using microprocessors and that, in particular, it is feasible using the available Interdata hardware and software.

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I. Introduction

Recent rapid developments in large scale integrated (LSI) circuit technology have resulted in inexpensive microprocessors, sometimes called "computers on a chip," which provide design engineers with a new design tool for a wide range of system, communication, control, and other applications. These programmable microprocessors are universal enough in operation set and I/O capability for broad useage. They can be reprogrammed rapidly to a new configuration. Furthermore, because of their size, they add only a small weight, power, and heat burden to a system.

This contract was for the study and development of microprocessor techniques as applied to low cost direct readout applications, in particular for applications to daily weather data as produced by the NIMBUS spacecraft. Governing considerations in such an application are ultimate microprocessor cost, data quality relative to data user requirements, and ease of change of input data format and data display. A wide variety of microprocessors are commercially available for consideration. An additional consideration for this contract was the availability of Interdata hardware and software packages for the contract study.

Microprocessors make possible significant system improvements and flexibilities for a wide variety of applications due to their low cost, speed, computing power and programming capability. From the beginnings of the industry in 1971 to the present, an explosion in product availability and capability has occured with over twenty five different microprocessors on the market. As a result, a hard task is the selection of a best processor for a given job. Almost any microprocessor can satisfy a given requirement as long as speed is not important. However, speed is usually an important factor, as in this contract study, where real time application is involved. A throughput of 4000 bits per second or 250 microseconds per bit must be maintained including all input, processing, and display operations. Additional factors to consider in processor selection relative to a given application include software design considerations such as word size, address capacity, number of registers, and addressing modes, hardware design considerations such as clock rate, voltages required, power dissipation, size, and compatibility with the interfaced hardware, and overall microprocessor system considerations such as price, availability, product longevity, software support, documentation, and direct memory access (DMA) ability. As a result of the wide variety of considerations, a large sample of available microprocessors was evaluated during the contract period.

II. NIMBUS Data System

The NIMBUS direct readout data is obtained by the on board versatile information processor (VIP) which samples approximately 1000 outputs from spacecraft systems. The sensor data are digitized, time-multiplexed, and formatted into a 4000 bits per second serial stream. The serial bit stream is transmitted over the pulse code modulation 136.5 MHz beacon transmission link. Data transmitted in the VIP mode include spacecraft subsystem and experiment housekeeping telemetry such as temperature of components, calibration signals and voltages plus the outputs of four experiments: NEMS, ESMR, ITPR, and SCR. VIP output has a normal mode, two verification modes, and a counter mode. All modes are 4000 bits per second, ten bits per word, least significant bit first. The normal mode is the one of interest for the direct readout application.

In the normal mode, three types of data are telemetered:

1.) Analog housekeeping data (including analog experiment data)

2.) Digital housekeeping data (digital B)

3.) Digital experiment data (digital A).

Although the VIP subsystem has the capability to generate many different telemetry matrices, only a single matrix of 80 minor frames, each containing 80 ten bit words is utilized. A major frame of 80 rows by 80 columns is generated every 16 seconds. Each minor frame has two synch words (words 0 and 1), a minor frame identification (bits 0 through 6 of word 41), format identification (bits 8 and 9 of word 41), a clock word (word 76) plus data words. 28 of the data words are digital A data where the ESMR data appears.

The electrically scanned microwave radiometer (ESMR) consists of four major components:

1.) A phased array microwave antenna consisting of 103 electrically phase shifted waveguide elements.

2.) A beam steering computer which adjusts the phase shift for each beam position.

3.) A microwave receiver.

4.) Timing, control, and power circuits.

The unit is arranged to scan perpendicularly to the spacecraft velocity vector. Brightness temperatures are measured at each scan position which, when properly displayed, will produce a microwave image of the portion of the earth near the satellite track.

The main data stream appears in digital A on the VIP. It is a serial bit stream which consists of the radiometer outputs multiplexed with the AGC step number and all the thermistor data necessary for data reduction. The data rate is 200 bits per second. The total data cycle is two VIP major frames or 32 seconds. The format is:

Scan	Word	Contents	Scan	Word	Contents
1	1	Beam position 1	3	1	Beam position 1
1	2	Beam position 2	3	2	Beam position 2
.	.	....	.	.	......
.	.	....	.	.	......
1	78	Beam position 78	3	78	Beam position 78
1	79	Hot reference	3	79	Hot reference
1	80	Avg. Antenna Temp.	3	80	Ferrite SW. Temp.
2	1	Beam position 1	4	1	Beam position 1
.	.	.....	.	.	......
.	.	......	.	.	......
2	78	Beam position 78	4	78	Beam position 78
2	79	Cold reference	4	79	Cold reference
2	80	Avg. Phase Shifter Temp.	4	80	Ambient load temp.

Scan	Word	Contents	Scan	Word	Contents
5	1	Beam position 1	7	1	Beam position 1
5	2	Beam position 2	7	2	Beam position 2
.	.	......	.	.	......
.	.	......	.	.	......
5	78	Beam position 78	7	78	Beam position 78
5	79	Hot reference	7	79	Hot reference
5	80	Dicke load temp.	7	80	Multiplex calibrate
6	1	Beam position 1	8	1	Beam position 1
.	.	......	.	.	......
.	.	......	.	.	......
6	78	Beam position 78	8	78	Beam position 78
6	79	Cold reference	8	79	Cold reference
6	80	AGC Count	8	80	Frame ID

Digital B on the VIP is a set of one bit status words to indicate the position of each of the command relays and one to identify the VIP major frame of the digital A cycle. They are sampled once per major frame or every 16 seconds.

The following is a summary of the calibration algorithm used to reduce the data for direct readout applications:

1.) Read two VIP major frames to get the 8 scans listed above.

2.) Using the de-multiplexed data,calculate the calibration temperatures from known calibration curves.

3.) Average the four ambient and the four cold calibration numbers.

4.) Convert all the data for the 78 beam positions for all 8 scans to brightness temperatures at the radiometer input.

5.) Using the measured antenna thermodynamic temperature and the tabulated antenna losses as a function of beam position as corrected for phase shifter temperature, calculate the gain function for average brightness temperatures.

6.) Correct each scan for the sidelobe contribution by an appropriate matrix operation.

III. Microprocessors Studied

As a part of the contract effort, an exhaustive study of available microprocessors was made. Three major areas of investigation were considered in this study:

1.) Software design of the microprocessor, which covers features as seen by the programmer and includes word size, type and number of registers, address capacity, execution time.

2.) Hardware design of the microprocessor, including such factors as clock,power and voltage required, size, etc.

3.) System design of the microprocessor, which affects the interface conventions between hardware and software design and includes important factors such as vendor support, product longevity, interrupts, DMA ability, and documentation.

Some of the microprocessors evaluated are:

Fairchild F-8

The Fairchild F-8 has a unique feature in that the CPU has no program location counter. Much more logic is packed on the CPU chip itself than other micros and some important registers are duplicated on each and every memory chip in the set.

The F-8 family consists of a CPU chip, a mask-programmed ROM chip, and a general memory interface chip. The RAM and ROM chips also provide I/O paths at the chip's edge. The 1024 x 8 bit ROM provides two bi-directional eight-bit channels and the 256 x 8 bit RAM has one. The addresses are programmed into ROM I/O ports when the mask is cut.

Each memory chip accepts one interrupt signal (therefore, to have a number of different interrupts there must be an equal number of chips) and each chip connects to two neighbors to chain interrupt priorities. Each chip also has a clock-driven interrupt capability.

The most important feature of the memory chips is that they have two program locators and a data address counter, with the same information stored on each chip. There are two program location counters on each chip so that interrupts can be performed quickly.

One major disadvantage of the F-8 storage addressing scheme is the required use of the data counter. There are no instructions that explicitely refer to storage addresses, so that the global data counter must be loaded before referring to any data in ROM or RAM.

INTEL 8080

The INTEL 8080 has been a very popular microprocessor. The 8080 has a three register sixteen bit file and an accumulator. Many instructions treat these as seven separate eight bit registers. The 16 bit stack pointer is used to place all return addresses in the RAM. This means that the program has to be assigned a unique on-chip register.

The 8080 has two potential disadvantages: from a software point of view, the lack of indexed addresses is serious in some applications; from a hardware standpoint, the need for three power supplies must be considered.

Motorola 6800

Programming of the Motorola 6800 is relatively easy. There are some areas where special precautions need to be taken, however. For example, there is no direct path from the two accumulators to the index register. To compute an index requires storing the sixteen bit value into the RAM and then loading it into the index register. The choices of various addressing modes are somewhat arbitrary because only certain instructions admit certain modes; it is the programmer's responsibility to remember which addressing forms are valid for each instruction.

An advantage of the 6800 is the provision for four levels of interrupts.

The CPU itself is organized as a conventional computer with an eight bit data/instruction path. Instructions execute in from two to twelve microseconds. There are two accumulators and a sixteen-bit index register.

Interdata Microprocessors

Because of the available software and hardware at GSFC, and because of the contract requirement for programming on the Interdata Model 4, special attention was given to the study of the Interdata microprocessor structure. Microprocessing for all models in the Interdata line is similar, although not directly compatible. Therefore the discussion in this report will be confined to the Interdata Model 4. Extensive study and programming was also devoted to the Model 8/32.

The Interdata Model 4 is controlled by a ROM. A series of programs are wired into the ROM which controls the flow of information within the registers and core storage of the machine. The machine is similar to the IBM 360 family of machines and has a very powerful instruction set. A block diagram appears in figure 1.

The Model 4 has ten basic micro-instructions:

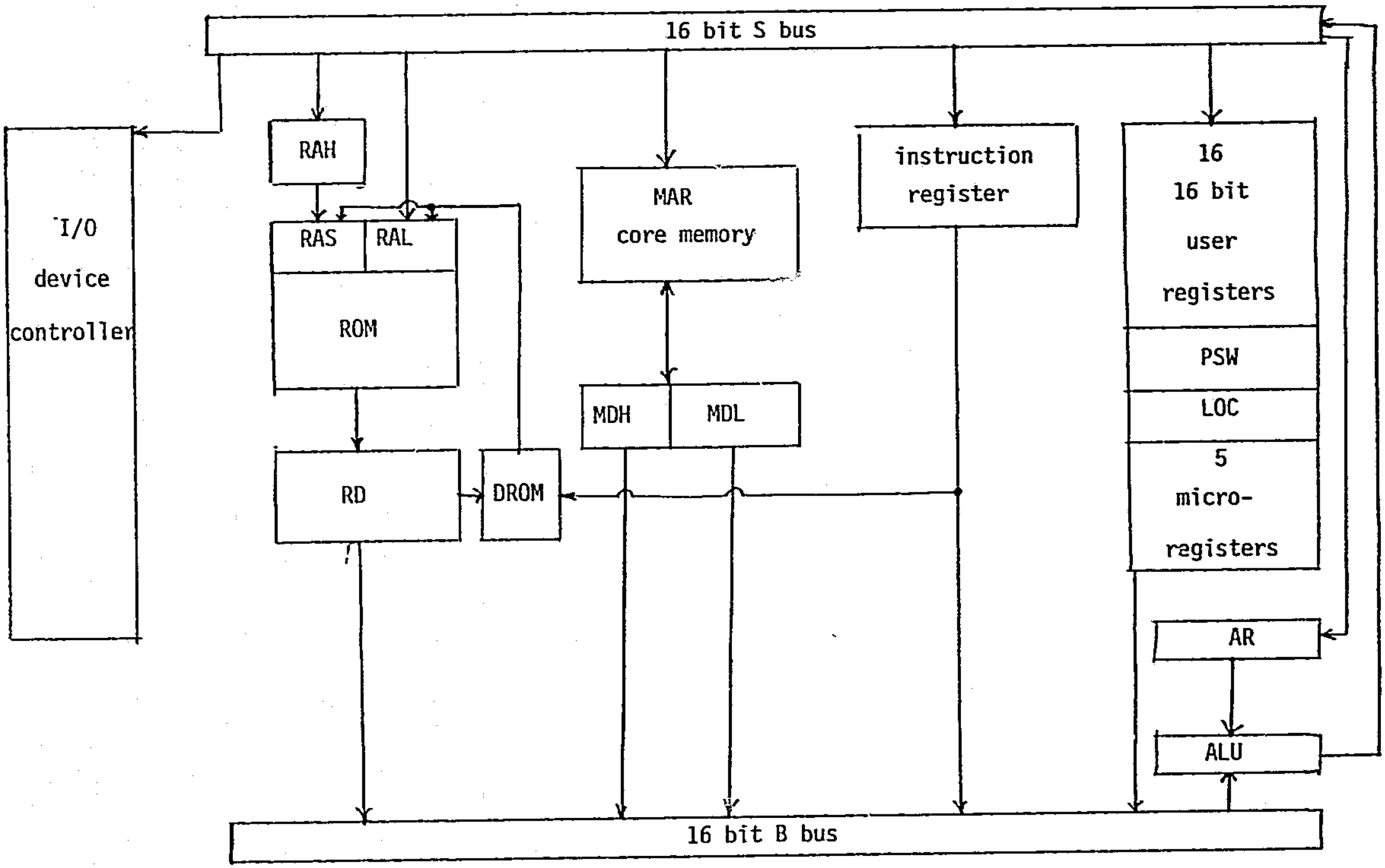

Figure 1. Interdata Model 4 Microprocessor

Symbol	Definition
A	add
S	subtract
X	exclusive OR
N	AND
O	OR
L	load
C	command
T	test
B	branch
D	decode

All data paths are sixteen bits wide. All arithmetic and logical operations work between the A register (AR) and the B bus. The arithmetic logic unit (ALU) performs the micro-instruction read from the ROM and contained in the ROM data register (RD). The RD is reloaded from the ROM at the completion of each micro-instruction. The RAS and RAL registers form a 12 bit address for the ROM. The RAL is incremented by one at the completion of each micro-instruction. The RAL is an eight bit micro-instruction location counter and RD is a 16 bit micro-instruction register. The RAS is a four bit page register which is loadedfrom the RAH whenever the RAL is loaded from the S bus.

The register stack consists of 24 16 bit registers, 16 of which are user general registers, 5 of which are general purpose micro-registers, 2 of which are the program status word (PSW) and location counter (LOC) and one of which is the memory address register (MAR) which is used to address core memory locations. The MAR appears twice with duplicate contents. It is duplicated because the address register on the memory interface can not be unloaded to the B bus.

The Interdata micro-instruction can have any one of four machine language formats, depending on the operation specified by the Op-code:

1.) Add,subtract, exclusive OR, AND, inclusive OR, and load

0 3	4 7	8 11	12 15
OP-CODE	D	S	E

Bit 3 in this format is always zero.

D = destination field: the result of the operation is placed into the register whose address is in this field

S = source field: the address of the register containing the second operand is in this field. The first operand comes from the AR.

E = extended operation field: specifies options

2.) Add immediate, subtract immediate, exclusive OR immediate, AND immediate, inclusive OR immediate, and load immediate

0 3	4 7	8 15
OP-CODE	D	DATA

Bit 3 in this format is always one.

D = destination field: the result of the operation is placed into the register whose address is in this field

DATA = the second operand is in this field. The first operand comes from the AR

3.) Test and command

0 3	4 15
OP-CODE	TC CODE

TC code = test or command code. Specifies the signal to be tested, or specifies the command to be performed.

4.) Branch on condition

0 3	4	5	6	7	8 15
OP-CODE	C	V	G	L	ADDRESS

C = carry

V= overflow

G = greater than zero

L = less than zero

ADDRESS = if specified condition on C, V, G, L is met, branch to this address

Through the availability of micro-programming, the power, speed, and full flexibility of the Interdata processor becomes attainable. The architecture can be extended to perform high speed algorithms and specialized application functions to a system without hardware involvement. The combination of minicomputer and microprocessor make it ideal for studies of ultimate microprocessor dedicated applications such as in the direct readout study performed in this contract. Algorithms can be quickly implemented at the assembly and FORTRAN level and modified. Then improvements can be gained by converting portions on an incremental basis to firmware microprogrammed in operations.

Experience With the Interdata family and investigations under this contract have led to the conclusion that the direct readout data handling system can be feasibly implemented on the Interdata microprocessor.

IV. New Technology

There are no reportable new technology items resulting from the work under this contract. The following review activities were performed to determine any reportable items:

1. The key technological concepts and ideas studied under the contract were identified. These consisted of the application of microprocessors to the direct readout. system and the specific microprograms and algorithms developed for the data reduction and display. The extent to which these ideas represented new techniques as versus an application of known techniques was reviewed.

2. A review of appropriate published literature to determine the uniqueness of the ideas developed under the contract was performed.

3. A meeting with the technical officer to discuss the results of the contract study effort and points (1) and (2) in connection with efforts performed at GSFC and under contract with other contractors was held.

As a result of the review activities, it was concluded that there were no ideas, discoveries, or improvements or reportable items which were first discovered, conceived or reduced to practice under the contract.

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