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FINAL REPORT

TVC ACTUATOR MODEL

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Prepared for:

George C. Marshall Space Flight Center
NASA
Marshall Space Flight Center, Alabama

M&S COMPUTING, INC.

TABLE OF CONTENTS

LIST OF FIGURES

PREFACE

The assembly of a Space Shuttle Main Engine (SSME) Thrust Vector Control (TVC) Actuator model by M&S Computing has progressed from trade studies to determine the most cost effective components with which to build the model, through the preparation of detailed software and hardware specifications, to the actual construction of the five PC Boards which make up the model. The contract ends with their successful checkout and operation.

This report outlines these activities and forms a final synopsis of the effort expended to develop this prototype TVC actuator model.

Prepared by:

R. W. Baslock

Approved by:

R W Baslock for W Ross

W. F. Ross, Jr.

1. SUMMARY

The contract to construct a prototype Space Shuttle Main Engine (SSME) Thrust Vector Control (TVC) Actuator analog model has been successfully completed. The prototype, mounted on five printed circuit (PC) boards has been delivered to NASA, checked out and tested using a modular replacement technique on an analog computer. In all cases, the prototype model performed within the recording techniques of the analog computer which is well within the tolerances of the specifications.

2. INTRODUCTION

The end product for the SSME TVC Actuator contract is a working prototype constructed of electronic components such as operational amplifiers, analog multipliers, dividers and switches. This end was obtained by first performing a trade study of the market place to determine the most cost effective devices with which to build the model. Next, the math model supplied by NASA was reduced to a circuit schematic which included those components selected in the trade study. These circuits were then built on five PC boards using plated through holes on double sided boards. In parallel with the construction of the PC boards, a digital simulation of the circuitry was generated to give assurance that the prototype would have the desired performance characteristics.

After the prototype was constructed, it was tested at NASA by incorporating portions of the model into an analog computer simulation and comparing the results. In all cases, the operation of the prototype was comparable to the analog program and completely satisfactory.

3. DESCRIPTION

The first effort that was required in performing the TVC actuator contract was a thorough study of the market place. This study was necessitated by the rapid advance in recent months in the technology base of analog operational amplifiers and function generators. These fourth generation devices have only been available for a short period of time and offer performance characteristics vastly superior to devices of two or three years ago.

In addition to studying the analog circuitry market place, the trade study also encompassed the field of microprocessors. Two devices were included in this trade off, the Motorola MC6800 microprocessor and the Texas Instruments TMS-9900 microprocessor and their families of supporting devices.

The entire trade study report is attached in the appendices for reference. However, the major conclusions are given in the following paragraphs.

The operational amplifiers which were capable of performing adequately in the TVC model formed a list of seven. These were:

RCA	CA 31400	$0.69 per 100
National Semiconductor	LF156	7.50 per 100
National Semiconductor	LF356	2.18 per 100
Burr Brown	3521	17.80 per 100
Burr Brown	3523	25.00 per 100
Analog Devices	146	61.00 per 100
Analog Devices	AD540	8.95 per 100

Of course, the most cost effective were the two that are least expensive: the CA3140 and the LF356. Based solely on price, the CA3140 was chosen and has since proven to be a good selection. The device can be handled almost with impunity with no deteriation of performance. The performance of the operational amplifier is very adequate in the completed model as predicted in the original trade study.

The selection of the analog switches was based almost entirely on price since all that were found performed adequately. The device chosen was Analog Device's AD7512 series costing $5.80 in 100 lot quantities.

he interface devices between the digital microprocessor and the analog amplifiers, i.e., the digital to analog and analog to digital converters were chosen to be the Burr Brown DAC 80 and the ADC 80, respectively. In addition to adequate electrical performance, these devices were relatively inexpensive, plus their physical size was among the smallest found. This was attractive due to the limited packaging area allotted to the interface board in the model package.

The microprocessor selection was based on sixteen factors. Each of these criteria were carefully weighed with the final selection being the MC6800 over the TI9900.

NASA and M&S Computing jointly agreed that the packaging of the TVC Actuator model should be accomplished using the Digital Equipment Corporation (DEC) back panels and cabinets. The most desireable approach would be to have one TVC actuator model per back panel with each back panel capable of holding nine PC boards; these nine boards being spaced 1/2 inch apart. Since some of the components necessary for building model were over 1/2 inch thick, it was decided to use five PC boards in the same back panel which allows 1 inch spacing between the boards. In keeping with the desire to have the model modular and interchangable with the other models, the allocation of board slots became the microprocessor-one slot; an interface board - one slot; the model power spool - one slot and finally, the model's 4-channel inputs to the power spool were divided into one PC board each and each PC board 1/2 slot. Therefore, the final two slots of the back panel contain four PC boards which constitute the 4 input channels of the TVC actuator model.

The next process in the development of the prototype consisted of two steps; one the designing of the analog circuitry based on the components selected in the trade study and the analog math model supplied by NASA, and, the second, the writing of specifications for the microprocessor hardware and software. These specifications were based on documents written by NASA which described the performance requirements of the TVC actuator models and knowledge of the capabilities of the MC6800 microprocessor system. These schematics and specifications are included in the Appendices.

The remainder of the project was used in the process of designing the microprocessor and interface board schematics (see the Appendices) and ordering parts, and, building the actuator model.

During the time when parts were on order and PC boards were being constructed, there was time to study the schematics of the analog model to insure proper operation of the circuitry once constructed.

This analysis was two pronged in that several of the actual circuits of the model were bread boarded using the trade study selected components and, a digital simulation of the overall actuator model based on input/output transfer functions was written. The circuitry that was bread boarded gave confidence that the individual circuits of the model were inherently stable and responsive to input stimuli such as would be encountered in actual practice. Further, time dependent drift and temperature drift proved not to be factor based on tests of the circuitry.

The digital simulation was based on a continuous systems simulation algorithm. The circuitry was described by explicitly programming equations which mathematically defined every node in the simulation. Integrators were emulated by a fourth order Runce Kutta Integration algorithm whose bandpass was explicitly defined. This approach has a distinct advantage over packaged simulation programs since there is a substantial savings in computer time. However, it does require a more through understanding of controls, numerical analysis, and FORTRAN, as well as the electronics of the circuit.

4. CONCLUSIONS

The requirements of the TVC actuator model program have been accomplished. The prototype is built and the microprocessor design is complete. In addition to these two accomplishments, M&S Computing has assisted NASA in the testing of the prototype model. This testing has been accomplished by a modular substitution technique into an analog computer at NASA which contained the same math model of the TVC actuator as was built by M&S Computing. Thus, one channel of the computer simulation could be removed and the prototype PC board channel substituted into the computer simulation. A comparison of computer responses before substitution and after substitution gives a graphic example of how well the ptototype functions. In performing these tests, no difference could be discerned between the computer responses and the prototype responses.

APPENDIX A

1. SUMMARY

Two trade studies have been conducted to define the best performing, most cost effective circuit components for use in the TVC actuator model. The first study encompassed the microprocessor that will be used to interface between the analog model and the simulation computer. The record analysis investigated integrated circuit operational amps, analog to digital converters, digital to analog converters, and analog switches that are to be used to actually construct the model.

The results of the microprocessor trade study is the selection of the MC6800. This device contains the best combination of individual circuit modules, interface characteristics, and software requirements.

The integrated circuit study resulted in the selection of the RCA CA 3140 operational amplifier, the Burr Brown DAC-80 digital to analog converter, a Burr Brown ADC80 analog to digital converter, and an Analog Devices AD7512 analog switch.

2. INTRODUCTION

The two trade studies contained in this report were conducted to determine what circuit components would provide the best performance and most cost effective integrated circuits for the TVC actuator model being designed by the Marshall Space Flight Center for use in the Marshall Mated Element Simulator, MMES. This analog model will contain from one hundred to one hundred fifty operational amplifiers interfaced to and controlled by a microprocessor. The microprocessor will in turn be interfaced with a simulation computer. The purpose of the studies was to choose the best microprocessor, operation amplifier, Digital to Analog (DAC) and Analog to Digital (ADC) converter and analog switches for use in the first brassboard prototype of the model. If these components perform properly in this prototype model, ten more models will be built to fullfill the requirements of the MMES. This means that at least 1000 operational amplifiers, 40 ADC's and DAC's and 250 analog switches would be required for the 10 models. Before making this large a committment to a circuit component, a market survey was in order. This report is the result of that survey.

The study approach used was to survey the market place and determine who made components which met the requirements of the TVC actuator model. These components specifications were then studied in detail. Factory engineers and representatives were contacted for reliability data, and firms using the devices were contacted for first hand information on the individual parts. The results of this data gathering is given in the following paragraphs.

3. DESCRIPTION

3.1 Microprocessor Trade Study

The MC6800 microprocessor is a bi-direction, bus-oriented, 8-bit parallel machine with 16 bits of address. The processor is capable of directly interfacing with eight peripheral devices and one TTL load on the same bus at a MHZ one clock rate. The key features of the MC6800 are:

- o 8-bit parallel processor
- o 65K bytes of memory
- o N-channel MOS technology
- o All input and outputs, except the clock, are TTL compatible
- o 72 basic instructions
- o Seven addressing modes
- o 2 microsecond instruction execution
- o Common I/O and memory bus

The Texas Instrument TMS-9900 microprocessor is a single-chip 16-bit central processing unit (CPU) which uses a N-channel silicon-gate MOS technology. The instruction set of the TMS-9900 includes the capabilities offered by full minicomputers. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort. Texas Instruments provides a compatible set of MOS and TTL memory and logic function circuits to be used with a TMS-9900 system. The system is fully supported by software and a complete prototyping system. The key features of the TMS-9900 are:

- o 16- Bit Instruction Word
- o Full Minicomputer Instruction Set Capability including Multiply and Divide
- o Up to 65,536 Bytes of Memory
- o 3-MHz Speed
- o Advanced Memory-to-Memory Architecture
- o Separate Memory, I/O, and Interrupt Bus Structures

- o 16 General Registers
- o 16 Prioritized Interrupts
- o Programmed and Direct Memory Access (DMA) I/O Capability
- o N-Channel Silicon-Gate Technology

3.1.1 Motorola MC6800

- o Advantages
  - The MC6800 system is attractive to the system user because the peripheral parts appear to the microprocessor as simply memory locations on the address and data bus. This bus architecture simplifies the interface between memory and peripheral devices and eliminates the use for dedicated I/O instructions.
  - A versatile peripheral interface adapter (MC 6820) simplifies MC6800 interfacing requirements with the TVC actuator model and Sigma-Type Multiplexer Input/Output Processor.
  - Comprehensive MC6800 supporting parts available including memory options, and communications devices.
  - The MC6800 is TTL compatible on all inputs and output, except for clock. A single power supply is required (+5v). The TMS-9900 requires +15V and +12V. (However, use of EPROM such as the Intel 2708 in a MC6800 system negates this advantage, since the 2708 requires +12V and +5V).
  - Despite only two accumulators and one index register, an efficient instruction set and addressing modes make the MC6800 a program execution benchmark leader in comparison to other 8-bit, single chip microprocessors. The address modes are as follows:
    1. Immediate
    2. Direct
    3. Index
    4. Extended
    5. Implied

6. Relative

7. Accumulator (ACCX)

- The MC6800, being the second most popular microprocessor in a field of approximately 50 commercially available types, attests to its performance and user satisfaction. The MC6800 is multi-second-sourced. (The TMS-9900 is not)

- Familarity with the MC6800 instruction set should be easily learned by DEC PDP-11 users, since many of the instructions (for example, the branch instructions) were copied from the PDP-11 as closely as possible with a shorter word-length machine. (However, it does not include the PDP-11 two-operand, source/destination- type instructions)

- Software cross assemblers for the MC6800 are available for PDP-11, Nova, IBM 360, HP 2100, and Sigma 9 computers.

- A non-overlapping two-phase clock in DIP form is available for the MC6800. (There is no similar four-phase clock available for the TMS-9900)

- Physically, the MC6800 is more than an inch shorter than the TMS-9900.

o Disadvantages

- In comparison to the 16-bit TMS-9900, the 8-bit MC6800 is at a disadvantage in communicating with the 12-bit resolution, DAC and ADC converters used on the TVC actuator model interface. This would impact hardware as well as software to some degree.

- All other things being equal, a 16-bit machine should be inherently more powerful than its 8-bit counterpart, particularly in memory addressing capabilities.

- The MC6800 has only two vectored interrupts, one maskable and one unmaskable. This limitation would require some software interrupt polling in most applications.

o Cost (not including software development)

- MC MC6800 Microprocessor	$35.00 each

-	MC 6871A Crystal OSC	$15.00 each
-	Intel 2708 EPROM (unprogrammed)	$99.00 each
-	Intel 2102 Static Ram (32EA)	$160.00 each
-	MC6820 Peripheral Adapter (2EA)	$30.00 each
-	MC6850 Async Communication Inf (ACIA)	$15.00 each
-	Miscellaneous parts including decoupling capacitors, resistors, IC's, etc.	$150.00 (est.)
-	MC6800/PDP-11 Cross Assembler	$1250.00 each (non-recurring)
	TOTAL: Approximately	$1650.00

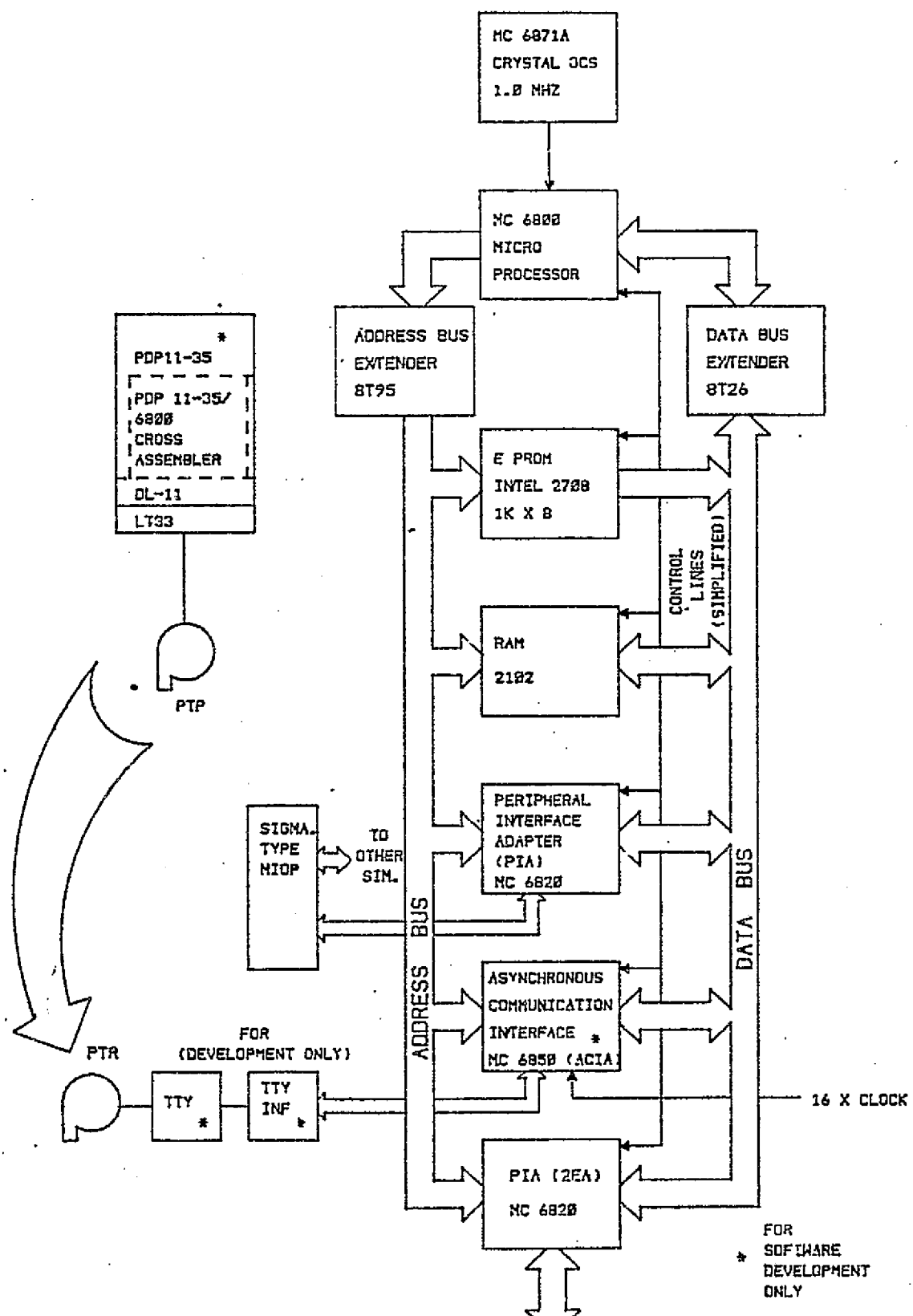
o Delivery Times

- Microprocessor and supporting chips are off-the-shelf.

o Design Considerations

- Three interfaces are required. (See Figure 3.1). They are (1) microprocessor to simulator, (2) microprocessor to a Sigma-type Multiplexer Input/Output Processor, and (3) microprocessor to teletype (TTY) (for software development only). Interfaces 1 and 2 could be accomplished with the use of peripheral interface adapters (PIA). Teletype interfacing could be accomplished through the use of an asynchrous communication interface and, external from the board, a TTY interface.

- Programming requirements include, writing a bootstrap loader to be resident in EPROM so that developmental software could be entered into the target microprocessor via a teletype interface. Software could be developed in a PDP-11 with a Motorola PDP-11/MC6800 cross assembler through a DL-11 interface to a TTY unit (LT 33). After software development is complete, the E Prom would be updated to its final configuration.



PRELIMINARY DESIGN CONCEPT
MC6800 MICROPROCESSOR
FIGURE 3.1

- An alternative software development approach would be to use the 6800/Sigma 9 instead of the 6800/PDP11 Cross Assembler. Assuming the 6800/Sigma 9 Cross Assembler could run on the simulation computer (or modified to do so), the target microprocessor software development programs could be loaded through the MIOP interface without the necessity of development of a special hardware serial interface.

Whichever approach is finally adopted, a significant microprocessor software development task can be anticipated.

3.1.2 Texas Instruments TMS-9900

o Advantages

- Most TMS-9900 instructions use a two-address format, specifying both operand source and destination, which is notably efficient in conserving instruction space and reducing program storage. The MC6800 utilizes single operand instruction only.

- The TMS-9900 provides up to 16 hardware vectored interrupts. The vectored interrupts, along with the work space register concept (all general purpose registers are resident in programmable slots in memory), permits the microprocessor to handle high interrupt rates. This means that the TMS-9900 can handle high speed I/O (which on some machines would normally be tied down by high overhead software) without necessarily resorting to expensive autonomous (DMA-type) controllers. The MC6800 has limited vector interrupt capabilities.

- The TMS-9900 employs a communications register unit (CRU) which is a general purpose, command-driven I/O. The novel feature of this device is that it can provide up to 4096 directly addressable input bits and 4096 directly addressable output bits. Both input and output bits can be addressed individually or in fields of from 1 to 16 bits. The CRU facilates interfacing variable word length device as would be required in process control applications.

- The TMS-9900 has hardware multiply and divide instruction.

- The TMS-9900 is software compatible with the Texas Instrument (TI) 990/4 and 990/10 minicomputer. Motorola does not have a family of

MC6800 like computers. Availability of a 990/10 minicomputer could simplify software to a target TMS-9900 microprocessor.

o Disadvantages

- The TMS-9900 I/O commands are relatively slow due to the I/O address incrementing and shifting. For a sixteen bit interface, the output command (LDCR) has a best case execution time of 17 microseconds and the input command (STCR) has a best case execution time of 20 microseconds.

- A four phase non-overlapping clock circuit would have to be designed.

- The MC6800 can read 8 bits of data into an accumulator (with a load accumulator (LDA)) from a peripheral device and store it into memory (with a store accumulator (STA)) faster than the TMS-9900 can read 8 bits from peripheral device and store it in memory (with a store communication register (STCR) instruction).

o Cost (not including software development)

		Quantity	Cost
1.	TMS TMS-9900 microprocessor	1	$99.65
2.	Intel 2708 EPROM (1K x 16 array)	2	$198.00
3.	Intel 2102 Static Ram (2K x 16 array)	32	$160.00
4.	Addressable Latch 74LS259	6	$12.00 (est.)
5.	1 of 8 multiplexer 74LS251	4	$10.00 (est.)
6.	Miscellaneous parts including decoupling capacitors, resistor, IC's, etc.	AR	$200.00 (est.)
7.	Motorola K1091 3MHz XTAL OSC		$35.00
8.	TMS-9900 IBM 3XO Cross Assembler		*$1250.00
9.	TMS-9900 Simulator Software		*$950.00

TOTAL: Approximately $3000.00

* Non-recurring costs

- o Delivery Times
  - Six weeks delivery time is quoted on the TMS-9900.
- o Design Considerations
  - Three interfaces are required. (See Figure 3.2). They are (1) microprocessor to simulator, (2) microprocessor to sigma-type MIOP, and (3) microprocessor to teletype (for software development only). Since LSI programmable interface adapters do not exist for the TMS-9900, the interface design between the microprocessor and the device would have to be built up from 74XX series (or equivalent) MSI and SSI parts. For data out and control functions, the device must latch Communications Register Unit (CRU) output data as the I/O bit address is being incremented. This can be accomplished by the use of addressable latches such as the 74LS259. Since the TMS-9900 is a "bit picking" machine, control functions (such as start conversion) can be initiated by issuing a single bit without affecting other bits in the status and control registers of the device.

    Data to the microprocessor can be channeled to the TMS-9900's CRU by the use of 1 of 8 tri-state output multiplexers. The 741S251 1 of 8 MUX and the incrementing I/O bit address effectively selects and then converts the user parallel data to serial data for the CRU input line.

    Device interrupt capability can be implemented by hard wiring interrupt request to a couple of 74148 encoders, which will generate the interrupt request and provide interrupt vector address to the TMS-9900.

    To provide software support, a link must be established to the outside world. One approach would be to bring the I/O bit address, CRU out, CRU in, CRU clock, an interrupt line, and other signals to an edge connector. Using these signals, an external TTY interface to TMS-9900 microprocessor could be designed.

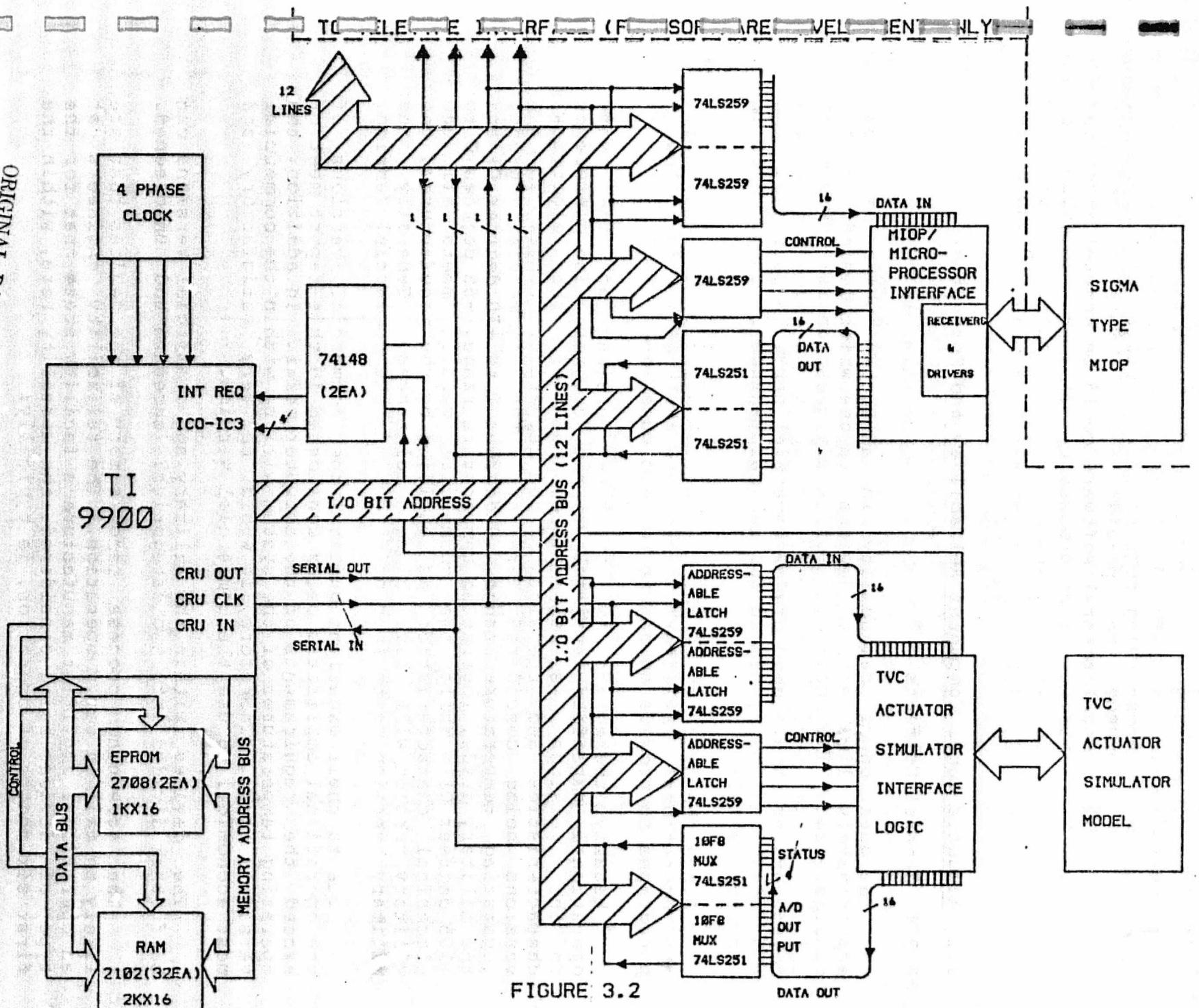


FIGURE 3.2

PRELIMINARY DESIGN CONCEPT

TI 9900 MICRO PROCESSOR

- Programming requirements dictate the need for EPROM to provide for a bootstrap so that developmental software could be entered into the target microprocessor via a teletype or equivalent interface. Software could be developed in a IBM 360/9900 cross assembler and TMS-9900 simulator.

3.2 Actuator Model Component Reliability and Cost Study

3.2.1 General Comments

The question of reliability in a system which will use approximately 1500 active devices is one which demands serious consideration. The basic trade-off study question is: Should an initial large amount of money be spent on high reliability components or should good grade commercial parts be purchased and the additional money needed for the maintenance be spent on an as required basis?

Since the majority of the 1500 active devices in the model are operational amplifiers, they are analyzed in the following paragraphs to provide an answer to this question.

Usually there are two or more versions of the same operational amplifier available to the designer. The difference in the versions is the tolerances of the electrical characteristics and the width of the temperature range. The two versions being considered here are the commercial grade, (operating temperature range, 0 degrees C to +70 degrees C) and the military grade, (operating temperature range, -55 degrees C to +125 degrees C). While the commercial version meets all the electrical characteristics as specified by the manufacturer, the military version will have closer tolerances. Generally, the military version costs four or five times the commercial version.

Due to their excellent quality, the commercial versions of the operational amplifiers being considered in this report meet or exceed the requirements of the actuator model. In addition, the operating temperatures of the system will be within the commercial version's range. Therefore, it would be very satisfactory and most economical to use the commercial version.

The devices within the military and commercial versions can be further divided into two categories: screened and unscreened.

The screening process removes many of the devices that are likely to fail in early operation. The reliability engineers at an operational amplifier manufacture's facility state that for the type of devices being considered, the mortality rate, within the first six months of operation, is typically:

0.02% per 1000 hours of operation for screened devices.

0.05% per 1000 hours of operation for unscreened devices.

These figures are true for both the military and commercial versions.

The failures that occur during this period are due to such things as scratched or cracked dies, marginal wiring contacts, imperfect packaging, and other events that are hard to detect during the manufacturing process. When these devices are tested at the end of the process they appear good, but after a few hours of operation at high temperatures and working voltages the weak points fail under stress.

An operational amplifier that is screened undergoes a process in which it experiences high temperatures and full operating voltages for many hours in the manufacturers facility, hence most of the weak devices are forced to fail and rejected before reaching the user. The unscreened device does not undergo this screening process, and it may take from a few to many hours of operation by the purchaser before it fails.

A worst case cost analysis can be made to compare the screened and unscreened devices. Assuming that one-thousand devices will be operated for eight hours each working day for six months (1040 hours) and the mortality rate is as previously given, the number of failures expected is:

Screened: (1000 units) x (1040 hours) x (0.02%/1000 hours) = 0.208 failed units.

Unscreened: (1000 units) x (1040 hours) x (0.05%/1000 hours) = 0.520 failed units.

Thus, in six months there should be expected one failure in each group, with the probability of failure 2.5 times greater in the unscreened group than in the screened group.

Considering that 1000 units is a relatively small sample and to ensure worst case, as is often done when calculating failures, the number of expected failures will be multiplied by a factor of five. Therefore, considering a failure of three amplifiers in the unscreened group and one in the screened group, the differential cost between the groups can be calculated.

The manufacturers screening costs are approximately $3000.00. Assuming eight hours to find and replace each failure at a cost of $20.00 per hour, the relative costs are as follows:

	Unscreened	Screened
Screening cost	$ 0	$3000.00
Replacement cost*	3.00	4.00

Labor cost	480.00	20.00
	$483.00	$3024.00

* Assuming a cost of $1.00 each for the unscreened device and $4.00 for the screened device.

Thus, there is a substantial cost to go from a situation of three expected failures when using unscreened parts to one expected failure after screening.

Another factor to consider is the downtime each group would cause. The unscreened group would be down for 24 man hours (2.3% of the first six months), while the screened group would be down for 8 man hours (0.8% of the first six months).

It should be emphasized that as the number of operational hours increase the likelihood of failure decreases. After approximately 1000 hours the unscreened devices that are still functioning are no more likely to fail than those of the screened group. This cost analysis represents the worst situation likely to exist. Also, it is quite possible that a failure can be found and replaced in much less time than the eight hours used in the calculations.

Considering the results of this study, it is recommended that the unscreened commercial operational amplifiers be used.

Now that is has been determined that the most cost effective approach is to purchase good commercial grade operational amplifiers, several other subjects should be addressed before the selection of specific devices is undertaken.

In order to facilitate model maintainability it is recommended that all integrated circuits be mounted in sockets with sufficient test points identified around the sockets. This approach is particularly important if a multilayer printed circuit board is used. When components must be unsoldered for replacement, the integrity of the boards will be jeopardized due to the difficulty of reusing the plated through holes.

Troubleshooting to detect failed components is difficult if a multilayer board is used. Since the middle layers of the PC board are inaccessable, input/output testing of suspect components is nearly impossible if these points are not given access to the outside world. Therefore, it is recommended that specific points within the circuitry be made available for testing.

3.2.2 Operational Amplifiers

3.2.1.1 Performance Analysis

A detailed study has been conducted to choose the "best" operational amplifier for the actuator model implementation. This

investigation was based on thorough study of data sheets, personal interviews with distributors and local company field engineers, and numerous calls to factory applications engineers.

The initial results of this investigation quickly indicated several peculiarities of the operational amplifier field.

The first was the very limited data available on the reliability of operational amplifiers. For instance, the official MSFC qualified parts list, Micro circuits, High Reliability, Qualified Circuits List contains only the record generation LM108 and LM741 operational amplifiers. The Military Standard Parts List for Flight and Mission Essential Ground Support Equipment, M11-STD- 975 also lists these two devices and none of the newer, higher performance operational amplifiers. An inquiry to the RAC, Reliability Analysis Center, Griffiss ARB NY indicates that: the most recent reliability data on operational amplifiers in their files includes the LM108, but no later devices.

The operational amplifiers field is supplied by several manufacturers with the most dominate being National Semiconducter, Motorola, RCA, and Burr Brown. Each of these companies offer a wide range of devices capable of performing the functions of operational amplifiers.

The operational amplifiers considered in this trade study analysis all have the following characteristics:

- Power supply voltages of at least $\pm$10 volts
- Input Bias current less than 1 micro ampere
- Input Resistance greater than 1 megaohm
- Gain band width 1 megahertz
- Common mode rejection greater than 70 dB.

Table 3.1 presents the individual operational amplifiers and their general usage category.

MOTOROLA		
	MC1556	High Performance
	MLF 156	J-FET Input
	MLM 108A	Precision
RCA		
	CA3140	MOS/FET Input
National Semiconductor		
	LF 156	JFET Input
	LF 356	JFET Input
	LM 108A	Precision
	LM 741	General Purpose
Burr Brown		
	3521	Low Drift FET
	3523	Low Bias Current
Analog Devices		
	AD540	General Purpose FET
	146J	Low Drift FET
	AD301	High Accuracy

Table 3-1

Operational Amplifiers Used for Analysis

Figure 3.3 shows the more basic operational amplifiers characteristics and how they apply to each of the amplifiers listed in Table 3.1. The second generation operational amplifiers, LM741 and MC1556, can be immediately eliminated from further consideration due to their high values of input bias currents and low input impedances. Even though the price of the LM741 is a relatively low $1.45 each, there are other devices in the list that are more cost effective. The MC1556, at $12.00 each in 100 quantity lots, is also relatively high priced and can be eliminated.

Now that a reasonable list of candidate devices has been established, additional selection criteria will be defined followed by discussions of their application to the specific op amps.

The most critical parameters for the TVC actuator model are output voltage drift with temperature, power supply variance rejection, input bias voltage and current, and cost. The areas of least interest are slew rates, common mode rejection ratios, gain bandwidth products, and power consumption. This is not to imply that these areas can be ignored, rather their significance is minimal. That is why the first filter process contained several of these criteria. For instance, all signals within the model are under 2500 hertz. Therefore, an amplifier need only have a full power bandwidth of ten times this amount (as a rule of thumb) or 25 kilohertz to be adequate.

The definitions and significance of the critical parameters are:

- Input Offset Voltage and Current

  All operational amplifiers register a small temperature dependent voltage and current, called offset, between their two input terminals. If these offsets are relatively constant and small, they can usually be ignored. However, if due to large temperature excursions or other circuit design parameters, the variations of the offsets become a significant portion of the input signal. This error will appear at the amplifier output.

- Power Supply Variance Rejection

  This parameter is an indication of how well the output of an operational amplifier is isolated from the power supply inputs. All amplifiers considered in this report have adequate rejection ratios for the short term, however, if inadequate poorly regulated supplies are used which tend to drift over a long period of time, problems could be encountered. For this reason, well regulated, good quality power supplies are recommended.

	POWER SUPPLY (VDCMAX)	OUTPUT BINS CURRENT	INPUT RESIST -ANCE	FULL POWER FRE- QUENCY (KHZ)	COMMON MODE REJECT -ION	GAIN BRID WIDTH PRODUCT (MHZ)
MC1556	$\pm$22	15NA	$10^{6}\Omega$		——	1
MLF356A	$\pm$18	50PA	$10^{11}\Omega$	——	——	5
MLM108A	$\pm$20	2NA	70MΩ	——	——	1
CA3140	$\pm$18	2PA	$10^{12}\Omega$	——	100DB	4.5
LF156	$\pm$22	30PA	$10^{12}\Omega$	——	100DB	5
LF356	$\pm$22	30PA	$10^{12}\Omega$	——	100DB	5
LM108A	$\pm$18	1.5NA	$40X10^{6}\Omega$	——	100DB	——
LM741	$\pm$22	200NA	$10^{6}\Omega$	——	90DB	——
3521	$\pm$15	20PA	$10^{11}\Omega$	10	90DB	1
3523	$\pm$15	0.5PA	$10^{12}\Omega$	10	80DB	1
AD540	$\pm$15	25PA	$10^{10}\Omega$	100	80DB	1
146	$\pm$15	15PA	$10^{11}\Omega$	150	80DB	5
AD301	$\pm$15	30NA	$4X10^{6}\Omega$	150	100DB	5

FIGURE 3.3 OPERATIONAL AMPLIFIER BASIC CHARACTERISTICS

o Output Voltage Drift

Drift is the gradually developing change in the input offset voltage and current. This change in offsets corresponds, in most operational amplifier applications, to a change in the null setting of the circuit and, therefore, appears as part of the signal at the output of the circuit. One of the factors that contributes the most to operational amplifier drift is external temperature variations. This should not be too much of a problem for the actuator model if the temperature within the computer room is held to variations of one or two degrees around ambient as is expected.

Figure 3.4 compares the individual devices in these important criteria. Notice that the input bias current column is repeated from Figure 3.3 for ease of reference. A study of this figure shows that the AD301 can be eliminated due to its high input noise voltage; the MLM108A and LM108A have relatively high input bias currents in relation to the rest of those in the list; and the MLF356A is not yet released by Motorola, therefore, these three devices can be removed from consideration.

Any of these remaining operational amplifiers can perform adequately in the TVC actuator model in that all of their electrical parameters meet its performed consideration. There is one remaining consideration, however, that still must be evaluated and that is cost.

The advantage in buying commercial products was stated earlier.

The following list gives the cost per hundred for each of the candidate devices.

CA 3140	$ 0.69
LF 156	$ 7.50
LF 356	$ 2.18
3521	$17.80
3523	$25.00
146	$61.00
AD540	$ 8.95

The two standouts in terms of cost are the RCA CA 3140 and the National Semiconductor LF356. The availability of these two parts according to the local technical engineers is 2 weeks for the LF 356 and off the shelf for the CA 3140. Therefore, the

	INPUT VOLTAGE DRIFT (MV/°C)	INPUT CURRENT DRIFT (PA/°C)	POWER SUPPLY REJECT -ION RATIO	INPUT BIAS CURRENT (PA)	INPUT OFFSET VOLTAGE (MV)	INPUT NOISE CURRENT (PA/$\sqrt{HZ}$)	INPUT NOISE VOLTAGE (NV/$\sqrt{HZ}$)	SETTLING TIME (μSEC)	PACKAGE SIZE
MLF 356A	5	———	———	50	———	———	———	———	———
MLM 108A	———	10	96 DB	2000	2	———	———	15	TO-99*
CA 3140	10	———	80 DB	2	5	———	40	1.4	TO-99*
LF 156	5	17	100 DB	30	3	0.01	15	1.5	TO-99*
LF 356	5	17	100 DB	30	3	0.01	15	1.5	TO-99*
LM 108A	1	0.5	110 DB	1500	1	———	———	20	TO-99*
3521	10	———	———	20	± 0.5	0.3	4	———	TO-99*
3523	25	———	———	0.5	± 1	0.01	5	———	TO-99*
AD301	± 5	———	———	30	± 0.5	———	400	———	TO-99*
146	±5	———	———	15	± 0.7	———	10	———	1.5"X1.5"
AD540	±25	———	———	25	± 20	———	10	———	TO-99*

* TO-99 IS A METAL CAN 0.4" IN DIAMETER AND 0.2" HIGH

FIGURE 3.4 OPERATIONAL AMPLIFIER CRITICAL PARAMETERS

results of this study yields these two operational amplifiers each capable of adequate operation in the actuator model.

There is one note of caution necessary for the CA 3140 and that is the fact that it uses MOSFET inputs guarded by bipolar diodes. In some cases, due to the extremely high input impedance, static electricity can cause circuit damage in spite of the guard diodes. The LM 356 has almost the same input resistance, but it is obtained by using JFET input devices which are not as susceptable to static electricity. It is felt that this one precaution does not decrease the desireability of the CA 3140 for use in the actuator model.

A search for reliability information on the two devices disclosed that the CA 3140 has passed a series of manufacturer reliability tests while the LF 356 has not yet been evaluated. The test for the CA 3140 subjected 20 devices operating as amplifiers with ±15 volt power supplies to 125 degrees C temperatures for 2000 hours. There were no failures during this test.

3.2.3 Analog Switches

There were three different sets of analog switches considered for the actuator model as shown in Figure 3.5. Since a total of 27 or more of these switches will be required to switch test voltages, ADC and DAC converters and monitor points in and out of the model, the switches should be carefully considered. Again, like the operational amplifiers, two families of technologies exist for the switches. These are the C-MOS and JFET. The C-MOS devices require special handling due to their high input impedances and possible susceptability to static electricity. They have the advantages of higher-off resistances than the JFETS. The Analog Devices AD 7512 does have zener diode protected inputs and outputs which reduces their susceptibility to static charges while the AH0019C does not have this protection.

There is no reliability data on these relatively new devices. However, since they use the same technology, their failure rates should be comparable to those given for the operational amplifiers, i.e. a 0.05% infant mortality rate for the first 6 months and then no failures attributable to the device itself thereafter.

3.2.4 Digital to Analog Converters

The choice of manufacturers for the DAC can be quickly narrowed to two, Burr Brown, Inc, and Analog Devices, Inc., based on the requirements of small size, 12 bit, I/O volt operation, and military grade quality.

The Burr Brown Company makes three devices which meet these requirements. These are the DAC80, DAC85C, and the DAC12QZ. The Analog Devices Company makes three devices which also meet these

	TYPE	ANALOG INPUT SIGNALS (VOLTS)	SWITCH ON RESIST-ANCE (Ω)	MAXIMUM FRE-QUENCY (MHZ)	SWITCH OFF RESIST-ANCE (Ω)	SWITCH-ING TIME (μSEC)	CASE	COST QTY=100
NATIONAL SEMICONDUCTOR AH0140C	JFET	±10	10	1	$500X10^6$	t_{ON} =.4 t_{OFF}=1.0	14 LEAD DIP	$14.95
AH0120C	JFET	±10	10	1	$500X10^6$	t_{ON}=0.4 t_{OFF}=1.0	14 LEAD DIP	$14.25
AH0019C	MOS	±10	200	1	$500X10^8$	t_{ON}=.4 t_{OFF}=.5	14 LEAD DIP	$7.80
ANALOG DEVICES								
AD7512	C-MOS	±10	70	1	10^9	1.2	14LEAD DIP	$5.80

FIGURE 3.5 ANALOG SWITCH CHARACTERISTICS

criteria: DAC1118, AD 562, and DAC12QZ. Note that both companies make the DAC12QZ, which is somewhat of an industry wide standard.

Figure 3.6 presents the specifications for these DAC's. Notice that the AD 562 has an output current rather than a voltage. This particular device requires an external operational amplifier to convert the output current to voltage levels. If the specifications of this operational amplifier were included in Figure 3.6, the specifications of the DAC would be in line with the rest of the list, plus, the price would be that much higher.

It should be noted that the prices listed in Figure 3.6 are for good commercial grade DAC's, not military grade as outlined in the scope of work. Since the operational amplifier that will be used in the actuator model will not be military versions, the DAC's need not be either. The only difference between the commercial grade and military grade devices is their allowable temperature excursions. The commercial temperature range being 0 degrees C to 70 degrees C and the military -25 degrees C to +85 degrees C. Since these devices will be operating in a controlled environment, the wider temperature range is excessive. The military trade device costs about one-half again the cost of the commercial grade.

The DAC's can be purchased from the manufacturer after they have been screened to military standards. But like the operational amplifiers, the failure rates would not warrant the very high costs of devices so tested.

3.2.5 Analog to Digital Converters

The ADC market place is similar to that of the DAC's; there are few manufacturers making 12 bit, $\pm$ 10 volt, military grade DAC's. Even by ignoring the military temperature range as was done for the DAC's, the field quickly narrows down to the Burr Brown model ADC 85 and ADC 80 and the Analog Device AD7550 and ADC-12QZ. The specifications for these devices is given in Figure 3.7.

The AD7550, while inexpensive and small in size, uses a "quad slope" technique for converting the analog signal to digital data. As can be seen, this process takes a relatively long time to complete, 40msec, compared to the higher priced units that use the more common "successive approximation" approach.

	LINE-ARITY ERROR	OUTPUT VOLTAGE (V)	SETTLING TIME TO 0.01% OF FULL SCALE (MSEC)	TEMPERA-TURE COEFFI-CIENT	POWER REQUIRE.	CASE SIZE	PRICE
BURR BROWN DAC80	±0.012%	±10	3	±30PPM/°C	±15V@25MA +5V@20MA	0.8"X1.4" X0.25"	$18.50/100
DAC85C	±0.012%	±10	3	±20PPM/°C	±15V@25MA +5V@20MA	0.8"X1.4" X0.25"	$56.00/100
DAC12QZ	±0.012%	±10	3	±30PPM/°C	±15V@25MA +5V@20MA	2"X2"X.4"	$39.00/100
ANALOG DEVICES DAC12QZ	±0.0125%	±10	5	±30PPM/°C	± 15V, +5V @ 30MA, 35MA	2"X2"X.4"	$47/100
DAC1118	±0.0125%	±10	5	±20PPM/°C	± 15V, +5V 30MA, 35MA	2"X2"X.4"	$80/100
AD562	±0.006%	±1MA	1.5	±3PMM/°C	± 15V, +5V	24 PIN DIP	$39/100

	ANALOG INPUTS (VOLTS)	INPUT IMPEDANCE (Ω)	LINEARITY ERROR (% OF FULL SCALE)	OFFSET DRIFT (PPM)	CONVERSION TIME / CLOCK FREQUENCY	POWER SUPPLY REQUIRE -MENTS	CASE SIZE	PRICE
ADC80	±10	10K	± 0.012	± 15	21 MSEC / 500KHZ	+15V@ 20MA -15V@ 20MA +5V@ 70MA	1.75"X1.2" X0.25"	1-25 UNITS $77.50
ADC85	±10	10^8	± 0.012	± 12	10 MSEC / 1.35MHZ	+15V@ 45MA -15V@ 35MA +5V@ 120MA	1.75"X1.2" X0.25"	10-24 UNITS $199.00
AD7550	±10	10^6	± 0.012	± 1	40 MSEC / 1.0 MHZ	+15V@0.6MA -15V@0.3MA +5V@0.06MA	40 PIN DIP 2"X0.5"	1-50 UNITS $35.00
ADC-12QZ	±10	10^9	± 0.0125	± 30	40 MSEC	+15V@ 20MA -15V@ 30MA +5V@ 210MA	2"X4" X0.4"	1-10 UNITS $149.00

FIGURE 3.7 ANALOG TO DIGITAL CONVERTER PARAMETERS

4. CONCLUSIONS AND RECOMMENDATIONS

4.1 Microprocessors

- The decision of which microprocessor to use for the Actuator model is based on careful consideration of the following factors:

  1. Ease of interfacing
  2. Interrupt handling capability
  3. Instruction set power
  4. Peripheral support devices availability
  5. Hardware and software development AIDS.
  6. Hardware development time
  7. Software development time
  8. Hardware costs
  9. Delivery time of parts
  10. Throughput requirements
  11. Unique design requirements
  12. Value of development expertise for possible future applications
  13. In-house computer cross assembler or directly compatability software for target microprocessor
  14. Second source availability of microprocessor and peripheral devices.
  15. Instruction execution times
  16. User acceptance (reliability)

- Preliminary designs for both the MC6800 and the TMS-9900 have been made to determine which device is most suitable for use in the Actuator model based on the above criteria. It is recommended that the MC6800 be chosen for the model as a result of this design effort.

4.2 Actuator Model Functional Components

4.2.1 General Comments

As was shown in Section 3, it is not cost effective to purchase either military grade components nor manufacturer screened commercial grade devices. The small number of failures expected over the first six month period do not warrent the additional cost of the high reliability military grade parts.

The one area where a cost savings can be generated is the use of sockets for the integrated circuits. The prototype board should definitely use sockets and after experience is gained in component failure occurrance and location, a decision be made for the use of rockets in the follow-on actuator model boards.

The configurations in which the operational amplifiers will be used in the actuator model are standard analog computer circuits such as integrators, summers, invertors, limiters, etc. As previously stated, any of the operational amplifiers in Table 3.2 will perform adequately in these circuits, although some are more cost effective than others. There are two circuits configurations where these amplifiers should not be used. These are the two output integrators of the model which supply gimbal rates and position. For these two applications, it will be necessary to preset their outputs to desired values, and to hold their output at some point in time. Therefore, it is recommended that two analog function integrators be purchased from the Develcor Corporation, Denver, Colorado. These devices have three inputs in addition to the normal analog input. These are:

- IC - This input voltage sets the output of the integrator to any given value. That is, it biases the output to a given DC level from which the normal output signal may deviate.

- Reset - This input signal removes the input signal to the integrator and sets the output voltage either to zero volts if the IC input is zero, or to the preset voltage established by the IC if IC is non-zero.

- Hold - Clamps the integrator output voltage at whatever value voltage was present when the Hold signal was issued.

The cost of these integrators is $135.00 each.

4.2.2 Operational Amplifiers

There are two operational amplifiers whose electrical parameters, availabilities, and costs make them attractive for the actuator model circuitry. These are the RCA CA 3140 at $0.69 per hundred and the National Semiconductor LF 356 at $2.18 per hundred. The rest of the amplifiers considered in this study,

while having suitable electrical parameters, are expensive and not cost effective.

The choice between these two devices based on their specification sheets is a draw. The CA 3140 has two times the drift and 2.5 times the input noise voltage as the LF 356. The LF 356, however, has 15 times the input bias current as the CA 3140. As previously noted, some precautions must be used when handling the CA 3140 due to its MOS input devices. However, the more rugged LF 356 costs three times as much as the CA 3140. This means that two CA 3140's could be mishandled and destroyed before inserting it in the PC board for every one LF 356 installed and the costs would be the same. Therefore, it is recommended that a suitable sample of each operational amplifier be purchased and inserted in a breadboard circuit of an integrator or summer and an electrical evaluation be conducted to see if either one has a clear superiority. This task is made particularly simple by each having the same connector pin configuration so one can be removed from a circuit socket and the other inserted. If again there is no clear winner in this evaluation, the cheaper CA 3140 should be used throughout the actuator model program.

4.2.3 Analog Switches

The selection of which analog switch to choose for the actuator model is relatively easy. Here price is the deciding factor with the Analog Devices Corporation, AD 7512 C-MOS switch being the most inexpensive at $5.80 each per 100 units, having a moderate 70 ohms of resistance and a gigaohm off resistance.

4.2.4 Digital to Analog Converters

The DAC that is the most cost effective is the Burr Brown, DAC80. This device has electrical characteristics comparable to the others that were considered, and contains all voltage references and output amplifiers. The physical size is also smaller than the others at 0.08" x 1.4" x 0.25". When these characteristics are considered along with its costs, it becomes the recommended choice.

4.2.5 Analog to Digital Converters

In comparison to the rest of the integrated circuits contained in the actuator model, the ADC converters are the most expensive. The one which is relatively inexpensive, the AD 7550 at $35.00, uses a process to convert analog to digital data, that requires 40 milliseconds. Therefore it was not considered. One of the goals during during the design of the actuator model is to keep the number of ADC's and DAC's to a minimum due to their high costs and large physical size. Therefore, some of the outputs of the model will be multiplexed through these devices. A conversion time of 40 msec does not allow a rapid enough cycle time for the actuator model and large errors could result.

Thus, the recommended choice for the ADC is the Burr Brown ADC 80 at $77.50 with conversion times of 21 microseconds.

5. APPENDICES

Not applicable.

6. REFERENCES

Not applicable.

7. APPROVALS

R. W. Baslock

W. F. Ross

APPENDIX B

1. SCOPE

This specification describes the software design requirements for the TVC Actuator Microprocessor which will be used to initialize, monitor, and test the TVC actuator model while it performs in the MSFC Mated Elements Simulator.

2. APPLICABLE DOCUMENTS

MSFC-20A82000	MMES Requirements Definition
76-0055	TVC Actuator Model Microprocessor Hardware Specification

3. REQUIREMENTS

3.1 General Description

For compatibility with Motorola's resident M6800 monitor MIDBUG/MINIBUG, and thus retain the ability to control the microprocessor with either a terminal or a host computer (Sigma), the software for the TVC actuator microprocessor will be based on the MIKBUG/MINIBUG utility command structure. An extended version of MIKBUG/MINIBUG CALLED MUDBUG acquired from Arizona State University will be used for this purpose. The modified version will be called M&SBUG.

The TVC actuator microprocessor control software will be designed to be executable under the direction of a high level interpreter. This interpreter will accept a variety of commands from the host computer or from a prestored list in microprocessor memory. The host will be able to load interpreter directive sequences into microprocessor memory, to request their execution, or transmit individual directives to the microprocessor at the time they are to be executed.

3.2 M&SBUG

3.2.1 System Configuration

M&SBUG will reside in the 1K EPROM from addressed $C000 through $C3FF and will use 128 words of RAM for variable storage. The utility commands in M&SBUG are single ASCII letters followed by zero to four hex parameters (sent as two ASCII characters per hex byte). The parameters are called PARM1 PARM2, PARM3, and PARM4.

3.2.2 MUDBUG Commands

Figure 3.1 lists the MUDBUG utility commands which will be supported. Hex numbers must be terminated with a period, comma, asterisk, or slash. A slash terminator aborts the command. Commands with no parameters require a carriage return terminator.

3.3 Interpreter

3.3.1 Purpose

The interpreter approach to performing the TVC Actuator project is intended to avoid including D/A and A/D settings in the microprocessor object code, since this would require reassembly to change the settings. Rather a high level list of directives will be interpreted by the microprocessor software at execution time.

M&S BUG COMMANDS

Command	Number of Parameters	Description
A	0	Display the current A register and accept a new value.
B	0	Display the current B register and accept a new value.
C	1	Display the current contents of location PARM1 and accept a new value. If the new value is terminated with a comma, display the contents of PARM1+1; if an asterisk terminator, display the contents of PARM1-1. Return to M&S BUG after a period or slash terminator.
E	1	Execute interpreter sequence number PARM1 from the resident Master Interpreter Table (MIT).
G	1	Load the registers from the pseudo registers and go to location PARM1.
H	0	Halt return. Load the registers from the pseudo registers and go to the location following the one from which the last halt (SWI) was executed.

Figure 3.1

M&S BUG COMMANDS
(Continued)

Command	Number of Parameters	Description
I	3	Initialize locations PARM1 thru PARM2 with the value PARM3.
J	0	Job command (JOBT or JOBN) to confirm reset.
K	0	Display the current condition codes and accept a new value.
L	0	Load the M6800 object tape into memory (checksum).
M	2	Memory dump locations PARM1 thru PARM2.
T	2	Trace from locations PARM1 to PARM2. When PARM2 is reached, print registers and return to M&S BUG.
U	1	Execute interpreter sequence that follows, PARM1 = byte count.
X	0	Display the current XR and accept a new value for the XR.
Y	2	Enter following interpreter sequence number PARM1 into Master Interpreter Table (MIT). PARM2 = byte count.
Z	0	Zero the AR, BR, and XR.

Figure 3.1

3.3.2 Interpreter Description

The interpreter will accept directions from within the microprocessor memory or from the host computer across the serial lines. M&SBUG utility commands are provided to allow the host to load directive sequences into microprocessor memory (Y), to call for execution or resident sequences (E), or for execution of directives as they are received by the microprocessor from the host (U).

The interpreter will be a table driven module. Each sequence to be resident in microprocessor memory will have an entry in the Master Interpreter Table (MIT). Entries can be made at object code load time (i.e., assembled along with the resident interpreter module) or under M&SBUG utility directive Y.

Each entry in the MIT is an address which points to an associated Control Interpreter List (CIL) and each entry has a sequence number which is its relative location in the table (i.e., the first MIT entry represents sequence number 1, etc.). Therefore the sequence number can be used by the interpreter as an index to the correct MIT entry, thus avoiding a memory search to find the address of the associated CIL entry.

The CIL contains a list of directive addresses for each sequence. Each entry points to a variable length directive in a given sequence. When a jump directive is encountered by the interpreter, the CIL will be used to locate the destination directive. The jump will specify the directive number and the interpreter will use this number as an index into the CIL, and thus acquire the address of the directive directly.

Interpreter sequences which are not resident in the microprocessor but are sent by the host using the U command will not have MIT entries. These sequences will not be saved by the microprocessor but must be sent dynamically by the host at the time of execution.

Figure 3.2 lists the interpreter directives which will be used. Each directive has a code which will be used by the interpreter as an index into a list of subroutine address to process the respective directive.

3.3 Host Communications

3.3.1 General

All communications between the microprocessor and host (terminal) will be via the ACIA serial link using seven bit ASCII characters with even parity and one stop bit (i.e., RS232). All M&SBUG utility commands sent by the host (terminal) will be echoed

INTERPRETER DIRECTIVES

CODE	PARM1	PARM2	PARM3	Description
00				Initialize interpreter
01	XXXX			Set MDO register with hex value XXXX
02	S	DDD		Set D/A register S with value DDD
03	TT	LL		Read test point TT of A/D1 into location LL (relative) & LL+1
04	TT	LL		Read test point TT of A/D2 into location LL (relative) & LL+1
05	LL			Read TVSDIS (upper 4 bits of 2PB) into LL
06	XX			Load counter with value XX
07				Increment counter
08				Decrement counter
09	NN			Unconditional-jump to directive number NN in this sequence
0A	NN	XX		Jump to directive NN in this sequence if counter .EQ. value XX
0B	NN	XXXX	LL	Jump to directive NN if the value in location LL and LL+.1 .EQ. XXXX
0C	NN	XXXX	LL	Jump to directive NN if the value in location LL and LL+.1 .LT. XXXX

Figure 3.2

INTERPRETER DIRECTIVES
(Continued)

CODE	PARM1	PARM2	PARM3	Description
0D	NN	XXXX	LL	Jump to directive NN if the value in location LL and LL+.1 .GT. XXXX
0E	XXXX			Delay XXXX miliseconds.
0F	LL			Send contents of LL and LL+1 to host
10	LL	MM		Send contents of LL thru MM+1 to host
11				Send start sequence message to host
12				Send complete sequence message to host
13	EE			Send error message to host (EE = error code)

Note: Each character in the directives shown represents one 4 bit hex digit.

Figure 3.2
(Continued)

back to the sender who is responsible for verification and retransmission when necessary. All object code to be loaded into microprocessors memory using the L command must be in M6800 object tape format including checksum (see Figure 3.3). The SCIA will always be enable for interrupt on input so that the host may get its attention at any time. It will be connected to the non-maskable interrupt line on the M6800.

3.3.2 M6800 Reset

When the M6800 reset occurs (power on or switch), the M&SBUG monitor is initialized. It will send a carriage return (CR), line feed (LF), escape (ESC, and esclamation mark (!) to the host (terminal). The microprocessor will ignore all subsequent messages until a JOBH (host) or JOBT (Terminal) is received from the sender to confirm recognition of the reset. The microprocessor will respond with a CR, LF, $ to indicate acceptance. It is the sender's responsibility to timeout and send this command followed by a reload of the interpreter commands cannot be insured since the interpreter resides in RAM which would have been erased by power on reset.

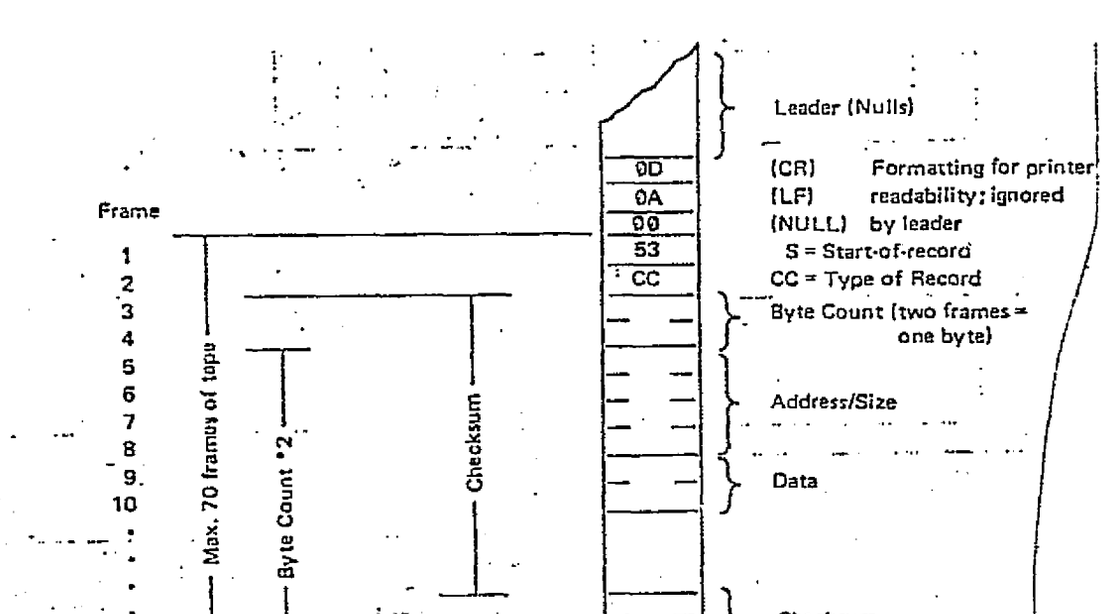
3.3.3 Message Formats

M&SBUG utility commands formats will be retained with some extensions. Each single character command will be echoed back to the host (terminal. The parameters will be separated or terminated with a period, comma, asterisk, or slash, where slash will abort the command. Each character will be echoed back to the host (sender). Completion of the command will be followed by a CR-LF-* to the host (terminal). If an error occurs, a backslash (\) followed by one character error code will be sent and then a CR-LF-*.

The interpreter sequence which is sent by the host (terminal) following the Y command will include a two character ones complete checksum (similar to Figure 3.3).

Messages sent to the host (terminal) in response to interpreter directives will be of the format shown in Figure 3.4. Refer to Figure 3.2 for the codes. Each byte will be encoded as two ASCII characters (similar to Figure 3.3).

TAPE FORMAT



Frames 3 through N are hexadecimal digits (in 7-bit ASCII) which are converted to BCD. Two BCD digits are combined to make one 8-bit byte.

The checksum is the one's complement of the summation of 8-bit bytes.

Frame	CC = 30 Header Record		CC = 31 Data Record		CC = 39 End-of-File Record	
1. Start-of-Record	53	S	53	S	53	S
2. Type of Record	30	0	31	1	39	9
3. Byte Count	31	12	31	16	30	03
4. Byte Count	32		36		33	
5.	30		31		30	
6. Address/Size	30	0000	31	1100	30	0000
7.	30		30		30	
8.	30		30		30	
9. Data	34	48-H	39	98	46	FC
10. Data	38		38		43	
•	34	44-D	30	32		(Checksum)
•	34		32			
•	35	52-R				
•	32		41	A8 (Checksum)		
•			48			
N. Checksum	39	9E				
	45					

Figure 3.3

INTERPRETER MESSAGE FORMAT

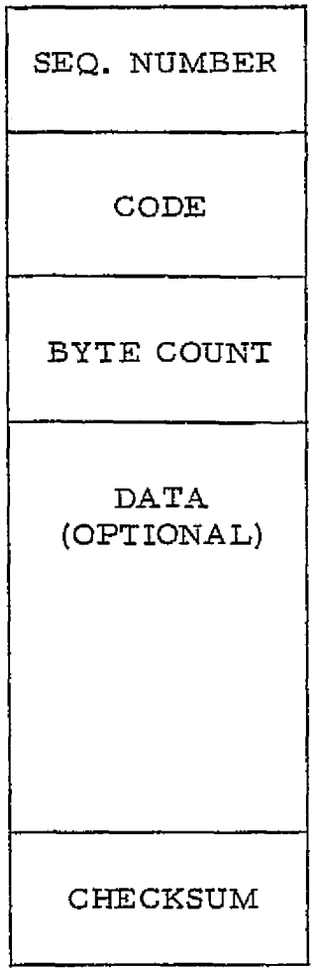


Figure 3.4

4. OPERATION

4.1 Philosophy

The TVC actuator microprocessor software will be designed such that the host is always in a position to exercise control over the microprocessors. The microprocessors will always act as slaves and will never be in a state where the host cannot get their attention. This approach will facilitate software recovery without the need for microprocessor manual reset.

4.2 Method

All M&SBUG and interpreter directives will originate in the host. The microprocessor will not generate unsolicited responses to the host except at power-on restart. The link between the microprocessor and the host will generate a non-maskable interrupt in the microprocessor whenever a character is sent by the host. This provides the mechanism whereby the host may restart the microprocessor at any time (i.e., JOB command).

5. HOST REQUIREMENTS

This section isolates the requirements placed upon the host computer to control the TVC microprocessors. The normal microprocessor operation requires three procedures by the host: initialize, load object, and load sequence. Special procedures are required when abnormal operation occurs.

5.1 Normal Operation

5.1.1 Initialize

When the microprocessor is first powered up, it will send four characters to the host: CR-LF-ESC-! The host must send four specific characters in response. The microprocessor will accept no others until it receives the characters JOBH (JOBT for terminal). Each character will be echoed (as will all subsequent utility commands) so that the host can verify them. If any character is incorrect, the microprocessor will start over looking for the first characters again (J). When the microprocessor has received the JOBH, it will send three characters to indicate AD (CR-LF-$) plus three characters to indicate it is ready to receive another utility command (CR-LF-*). These last three characters will always indicate that the microprocessor is back at the top of its monitor loop waiting for another utility command (see Figure 3.1).

5.1.2 Load Object

After successful initialization (JOBH), the host must load the object code of the interpreter into the microprocessor memory before it will accept any interpreter directives. The L utility command should be used for this purpose.

The host should send the character L, which will be echoed. This should be followed by the M6800 object code in the format shown in Figure 3.3. This is the format generated by the M6800 cross assembler. If the microprocessor takes the entire object without error, it will send three characters to the host (CR-LF-*). Error handling is described in Section 5.2.

5.1.3 Load Sequences

Next, the host must load the interpreter sequences into the microprocessor memory before the microprocessor can be used with the TVC actuator to change status or enter faults as described in Reference 76-0055. The Y utility should be used for this purpose.

The host should send the character Y, which will be echoed. This should be followed by the directives which make up the sequence (see Figure 3.2). If the microprocessor takes the entire

sequence without error, it will send these characters to the host (CR-LF-*). The host should then repeat this procedure for each sequence which must be loaded into the microprocessor memory. (Note: all sequences could be back to back on a single file and sent together at one time).

The microprocessor is now able to receive interpreter utility commands to execute sequences (E command in Figure 3.1).

5.2 Abnormal Operation

5.2.1 Error Messages

If at any time the microprocessor detects an error condition, it will sent two characters. The first character will always be a backslash (\). The second will indicate the error (see Figure 5.1). Three characters will then usually follow, indicating that the microprocessor is back at the top of its monitor loop (CR-LF-*), ready to accept another command.

5.2.2 JOB Command

If a power reset occurs at any time, the microprocessor will send CR-LF-ESC-! to the host. The host must then send JOBH as described in Section 5.1.1.

The JOBH may also be sent by the host to reinitialize the microprocessor. In fact, this is the only command that will be accepted by the host if it is processing a directive (i.e., - possibly hung in a loop).

5.2.3 Interpreter Initialization

An interpreter directive (code 0) is supplied (see Figure 3.2) to reinitialize the interpreter tables. A reload of sequences is then required.

APPENDIX C

1. SCOPE

This specification describes the hardware design requirements for the TVC Actuator microprocessor which will be used to initialize, monitor, and test the TVC Actuator model while it performs in the MSFC Mated Elements Simulator. This digital microprocessor shall interface with the analog model through digital to analog converters (DAC) and analog to digital converters (ADC) and will be controlled by stored programs in the MES simulation computer.

2. APPLICABLE DOCUMENTS

The following documents are applicable to the information presented herein to the extent specified.

MSFC-30A82000	MMES Requirements Definition Document
JSC-10658	SAIL/MMES Requirement Document
MSFC-30A82001	MMES Preliminary Design Document

3. REQUIREMENTS

3.1 General Requirements

The purpose of the TVC Actuator Simulators is to represent the TVC actuator hardware in the Shuttle Avionics Integration Laboratory (SAIL). These simulators will represent four SRB TVC actuators and six mainstage propulsion system SSME TVC Actuators.

The models will consist of analog operational amplifier and microprocessor circuitry mounted on printed circuit boards and will perform the simulation of the SSME and SRB actuators as commanded by the host Sigma computer through the resident microprocessor computers.

The microprocessor driven analog circ itry used for each actuator shall provide the capability of redundant input charmed monitoring, and providing actuator positions and feedback to the Orbiter TVC drivers. The actuator bypass feature in each of the four redundant input channels shall be included and used to "vote out" a failed channel based on monitoring of simulated servo valve secondary hydraulic pressure. The actuator simulators shall also provide SSME gimbal positions, rates, and accelerations to the SAIL.

An interface will be provided between the analog circuitry and the digital microprocessor which will consist of analog to digital converters, digital to analog converters, and necessary solid state switches. These drives shall all be controlled by the microprocessor.

3.2 Interfaces

3.2.1 Digital to Analog

The Digital to Analog interface shall employ eight 12-bit resolution Burr Brown Model digital to analog converters (DAC) 80-CBI-V digital to analog converters. The output shall be bipolar ($\pm$10V) and provide both gain and offset adjustments on each device.

The Burr Brown DAC 80 shall accept externally-latched data from the microprocessor/DAC interface in complementary offset binary format. This format shall be as follows:

000000000000	+ Full Scale
011111111111	Zero
100000000000	-1 LSB

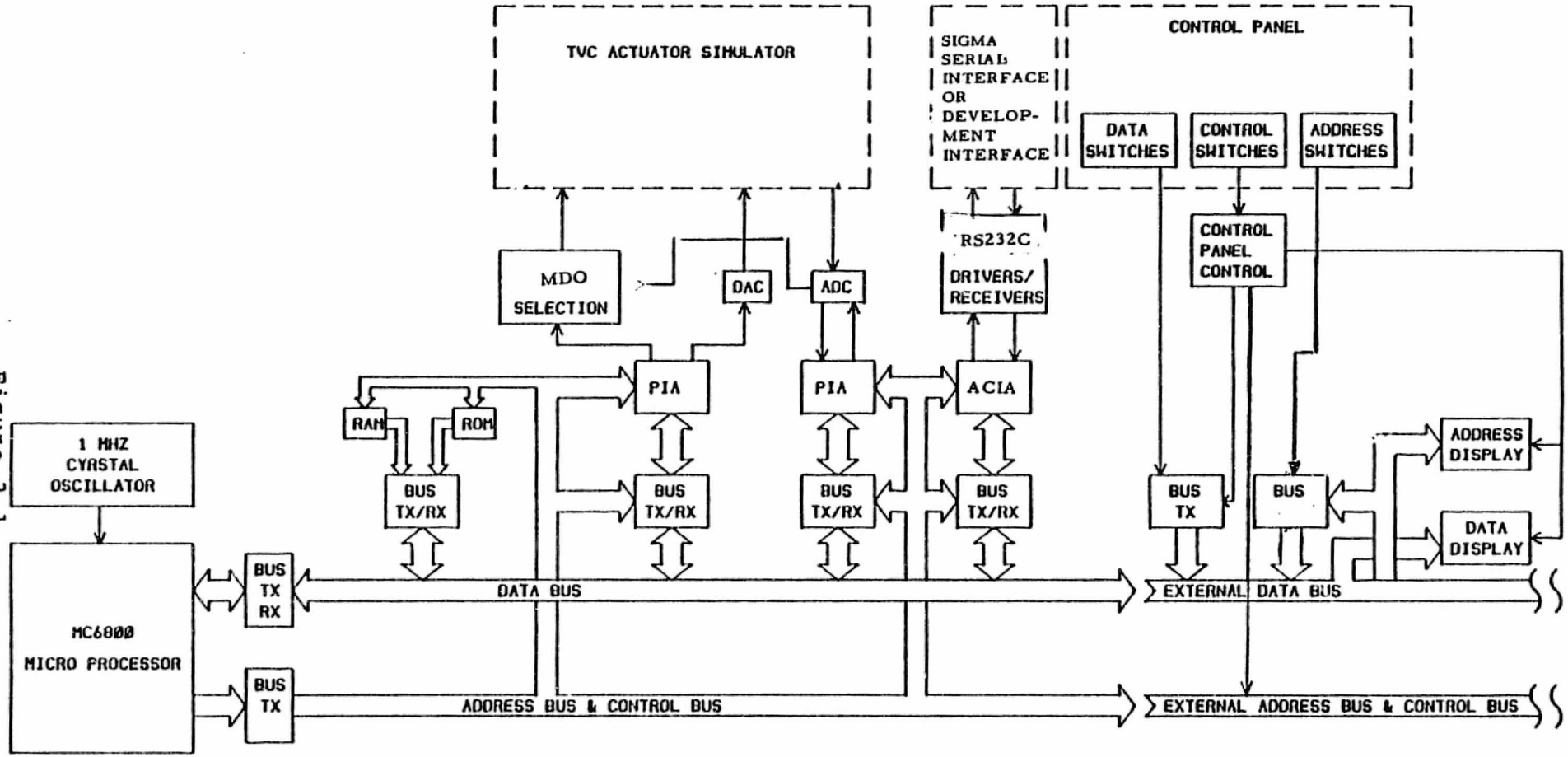
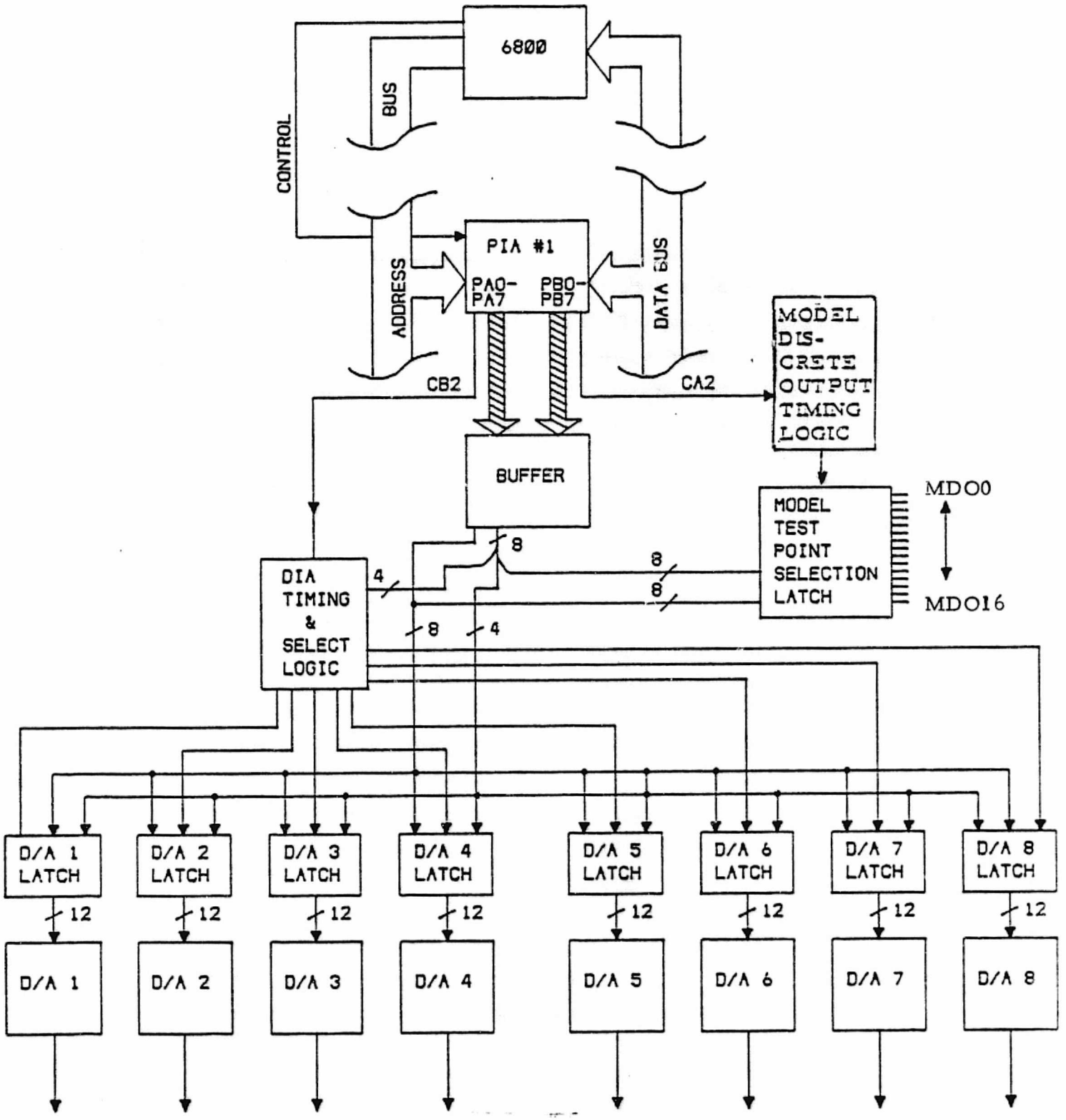


Figure 3.1 C-8

TVC ACTUATOR SIMULATOR MICRO PROCESSOR
FUNCTIONAL BLOCK DIAGRAM



D/A OUTPUTS TO MODEL AND MODEL INTERFACE

MICRO PROCESSOR TO D/A AND MICRO PROCESSOR TO MODEL DISCRETE OUTPUT INTERFACE

Figure 3.2

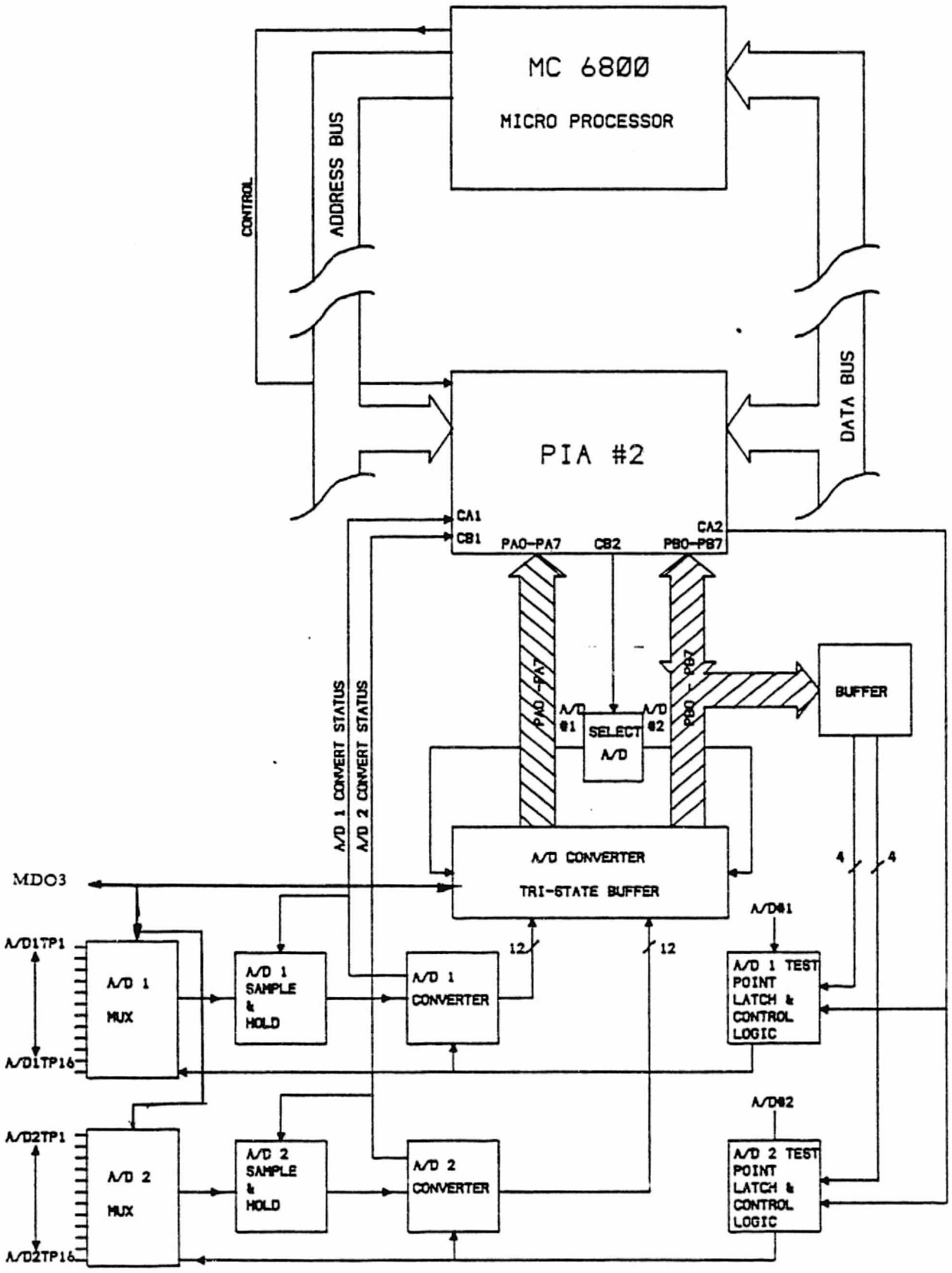


FIG. 3.3 MICROPROCESSOR TO A/D INTERFACE

111111111111 -Full Scale

The outputs of the DAC's shall be distributed to the model via the model interface for simulation and shall be switched to an analog to digital converter (ADC) test point for self-test.

3.2.2 Analog to Digital

The Analog to Digital interface shall employ two Burr Brown model ADC 80 AG-12, 12-bit successive approximation ADC's. These ADC's perform conversion in 25 microseconds.

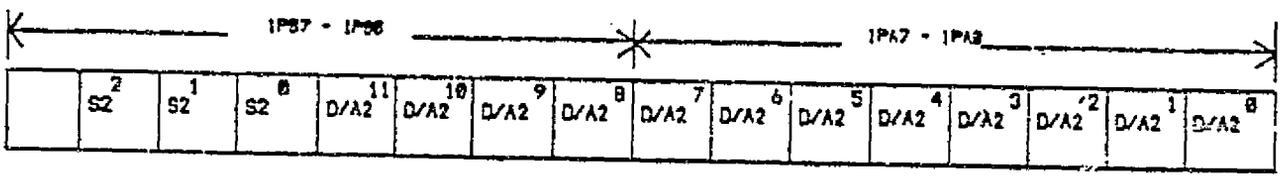
Through the use of two MPC 16 analog multiplexers, up to 16 test points shall be provided to each ADC. Conversions shall occur concurrently on the two converters, but the digital data is read separately under the microprocessor control through the use of tri-state buffers.

Conversion shall be initiated by the 2CA2 signal from the microprocessor/ADC interface. After a 10-microsecond delay to allow the multiplexer to settle, a start convert command shall be provided to the Burr Brown ADC 80. When the converter is converting, the status signal from the Burr Brown ADC 80 goes high and shall be used to make sample and hold amplifier to go into the hold state. After approximately 25 microseconds, the status signal from the ADC shall go low, indicating the end of the conversion. This event shall generate an interrupt request to notify the microprocessor that the new data may be read.

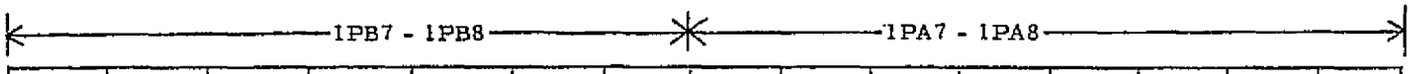
3.2.3 Microprocessor to Model Model Discrete Output, ADC, and DAC Interfaces

The microprocessor to model test point, ADC, and DAC interfaces shall be accomplished through the use of two programmable interface adapters (PIA's) (see Figure 3.1). One of these PIA's shall be shared by the model discrete output (MDO) and the DAC interfaces (see Figure 3.2), while the second shall be dedicated to the ADC converter (see Figure 3.3).

The DAC output value and DAC address shall be set up by first loading the PIA peripheral data registers (PA0-PA7 and PB0-PB7) with the DAC values and the selected DAC, and then strobing this data with the CB2 signal from the microprocessor. The format for this word is:



Similarly, the model discrete output(s) (MDO's) shall be enabled by loading the PIA peripheral data registers with the desired test point(s) using logical "1" is a test point ON and logical "0" is a test point OFF. This data shall be strobed with the 1CA2 signal from the microprocessor. The format for the test point word shall be:

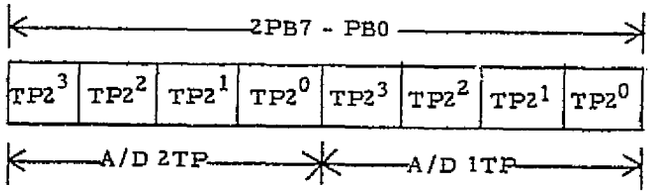


MDO15	MDO14	MDO13	MDO12	MDO11	MDO9	MDO8	MDO7	MDO6	MDO5	MDO4	MDO3	MDO2	MDO1	MDO0

where:

MTP0-MTP15 are model test points.

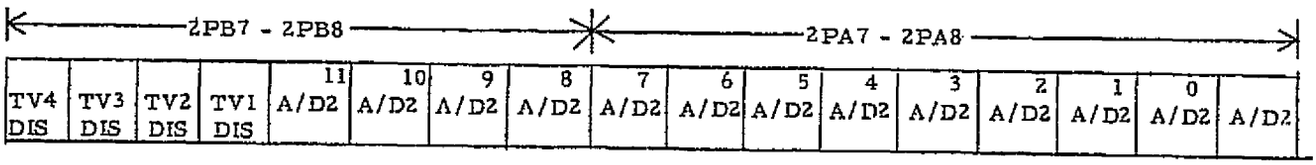
The ADC converter operation requires the selection of either ADC1 or ADC2. Selection shall be determined by the 2CB2 signal, that is, ADC1 is selected when 2CB2 is a logical "0", and ADC2 is selected when 2CB2 is a logical "1". The analog test points shall be set up by programming the PIA #2 peripheral data register "B" in the following format:



$TP2^3$	$TP2^2$	$TP2^1$	$TP2^0$	$TP2^3$	$TP2^2$	$TP2^1$	$TP2^0$

Conversion in the selected ADC commences when 2CA2 is ON. Conversion in the second converter may run concurrently with the first by inverting 2CB2 and reissuing 2CA2. When the conversions are completed, interrupts shall occur for ADC1 and ADC2 on the trailing edge of 2CA1 and 2CB, respectively.

The converted values shall be read by setting model discrete output 3 (MDO 03) on, selecting the ADC, changing the peripheral direction register, and reading the appropriate PIA data register. Reading the peripheral register shall reset the associated interrupt. The ADC format shall be as follows:



The most significant four bits (2PB4-2PB1) are not associated with the ADC conversion. TV1 Discrete through TV4 are T+C level, channel disables from ATVC signal conditioner. These signals may be read whenever MDO 03 is set without performing an analog conversion.

3.2.4 Microprocessor to Sigma Interface

The interface between the TVC Actuator Simulator and the Sigma shall be via a RS 2325 compatible asynchronous serial interface available transfer rates (at the microprocessor) are 9600, 4800, 2400, 1200, 600, and 300 baud. The serial communication link is accomplished on the microprocessor board through the use of an asynchronous communication interface adapter (ACIA).

3.2.5 Model Interface Switch and DAC and ADC Loop Test

The model and model interface shall contain analog switches (Analog Devices model AD7511 and AD7512). The function of these switches shall be two fold: 1) Provide a method of placing initial conditions or testing stimuli from the DAC to the model and 2) Provide a DAC and ADC loop test capability.

All inputs on the AD7511 and AD7512 are TTL compatible. Maximum switch current is 50MA (Is continous) or 150MA (Is surge, 1 MS duration 10% duty cycle). Input current to the AD7512 is 10NA.

3.3 Microprocessor

3.3.1 MPU

The Microprocessing Unit (MPU) utilized for each TVC actuator simulator shall be the Motorola MC 6800. The MC 6800 is a monolithic eight-bit microprocessor, the central function of the Motorola M 6800 family which includes the MC 6820 Peripheral Interface Adapter (PIA) and the MC6850, a synchronous communication adapter (ACIA). The MPU operating characteristics are delineated on the MC 6800 specification sheets.

3.3.2 Microprocessor Memory

The microprocessor random access memory (RAM) shall be up to a 4K x 8 memory array made AMD's AM9140 EDC, 4K x 1 RAM. These RAM's are static storage, dynamic control devices.

The microprocessor shall also contain one 1 K x 8-bit Erasable Programmable Read Only Memory (EPROM). The EPROM shall be Intel 2708, which shall be installed on a 24-pin IC socket for ease of reprogramming. This EPROM requires power supplies of +12V, -5V, and +5V. +5V.

Since the MC 6800 does not utilize separate I/O instructions, all I/O device addressing shall be accomplished as though it were memory addresses, see Figure 3.1.

To read memory, the microprocessor (or control panel) shall place the address on the address bus, causing the selection of ROM or one of two groups of RAM. If the address is valid (VMA), data corresponding to the address location shall be strobed onto the data bus by the control bus enable (DBE) signal.

The WRITE operation is similar to the READ operation except that the CBR/W signal is low to enable the selected data to be written into memory at CBE time.

3.3.3 Microprocessor Bus

Due to limitation in the drive capability of the MC 6800 family of LSI components (1 TTL load and 130PF), the TVC actuator simulator microprocessor's address bus, data bus, and control bus shall utilize TTL tri-state bus drivers. The drivers, which shall be used, shall be selected from the Signetic's 8TXX family. These high impedance PNP input devices have 40MA sinking drive capability thus are well suited for microprocessor bus applications.

3.3.4 Microprocessor Control Panel

Integral to the microprocessor system shall be an external pluggable control panel which will provide an off-line hardware

and software development aid. The control panel shall have the following capabilities:

1. Single step operation.

2. Read or write direct memory access capability when the MPU is in the HALT state.

3. Jump to non-maskable interrupt vector location.

4. Control panel control shall provide RESET, GO/HALT, READ, WRITE, JUMP, 16 address and eight data switches.

5. Led indicators for the 16 address bits, and 8 data bits shall be used. HALT and BUS AVAILABLE status shall be indicated by LED's.

Single step operation is accomplished by removing HALT for one memory clock cycle (leading edge of 1 to the leading edge of the next 01). The address of the executed instruction shall be strobed at the appropriate time and latched on the control panel address and data display.

Reading from or writing to memory from the control panel can only be accomplished when the MPU is in the HALT state. During the HALT state, the address bus, data bus, and the R/W line are all in the high impedance state which will allow the external control panel to gain access to these bus lines. The control panel logic simulates the MPU timing by placing the address and data switch data, and the R/W on the line as required.

Depressing the JUMP push button generates a non-maskable priority interrupt. Upon recognition of this interrupt, the MPU reads a 16-bit pre-settable address and, under program control, jumps to this address.

Depressing the RESET push button resets the microprocessor system and the memory to location FFFE.

The GO/HALT switch provides an external control of the MPU. In the HALT mode, the MPU's HALT line is taken low forcing all MPU operations to stop and to make the buses available for external control panel operations. In the GO mode, the MPU proceeds executing of instructions at the present program counter location.

3.4 Miscellaneous

3.4.1 Power Requirements

The TVC actuator simulator microprocessor requires the following estimated power:

+5V @ 4 AMP (MAX)

+12V @ TBD MA

-5V @ TBD MA

+15V @ TBD MA

-15V @ TBD MA

3.4.2 Mechanical Housing

The TVC simulator microprocessor PC board is to be mounted in standard *DEC backplane. The number of modules and size are to be determined.

The microprocessor address bus (AB), Data Bus (DB), and Control Bus (CB) signals shall be accessible via 40-pin Scotch flex edge connector conveniently located to plug in an external control panel.

3.4.3 Temperature and Humidity

The TVC actuator simulator shall operate in a range of TBD F to TBD F at a relative humidity of TBD percent.

3.4.4 Noise Considerations

The Vcc voltage (+5V) shall be decoupled with approximately 0.01uF for each 20 gates, preferably distributed over a wide area. These capacitors shall be ceramic type. In addition, 10uF to 50uF tantalum capacitors shall be distributed across the boards;

The DAC's and ADC's should be bypassed with tantalum capacitors as close to the device as possible. In addition, the tantalums shall be bypassed with 0.01uF ceramic capacitors for improved high frequency performance.

* Digital Equipment Corporation

4. QUALITY ASSURANCE

Not applicable.

5. PREPARATION FOR DELIVERY

Not applicable.

6. NOTES

The following schematics form a part of this specification by delineating the layout and interpin connections of the 6800 microprocessor, associated memories, and ADC and DAC interfaces.

APPENDIX D

1. SCOPE

This design and performance specification delineates the software required to interface the TVC actuator model microprocessors to a Sigma class digital computer.

2. APPLICABLE DOCUMENTS

The following documents are applicable to the information presented herein to the extent specified.

MSFC-30A82000	MMES Requirements Definition Document
JSC-10658	SAIL/MMES Requirement Document
MSFC-30A92001	MMES Preliminary Design Document

3. REQUIREMENTS

3.1 General

Each of the ten Actuator models in the Marshall Mated Element System (MMES) shall be controlled by a MCMC6800 class microprocessor. The interface between the digital microprocessor and the analog model shall be eight input digital to analog converters (DAC) and two analog multiplexed input analog to digital converters (ADC). The microprocessor will be interfaced with the Sigma computer in the MMES or a serial input/output (I/O) for testing and checkout prior to the Sigma being available.

It is the function of the software resident in the Sigma computer and the MC6800 microprocessor to tie the Sigma and MC6800 together to provide initialization, self-test and the operational states necessary for the TVC actuator models. The software in the Sigma computer shall operate under the control of the MES EXECUTIVE. The microprocessor software shall be established in the memories of the microprocessor as program steps capable of responding to commands from either the Sigma computer, or the serial I/O device.

3.2 Simulation State Software Requirements

The overall software program of the microprocessor and Sigma computer shall perform those operational functions shown in Figure 3.1.

3.2.1 Sigma Computer Software

3.2.1.1

The Sigma software shall establish the operability conditions of the TVC Actuator Model, format this data into suitable form and transmit the information to the microprocessor.

3.2.1.2

The Sigma computer shall not interface with the TVC Actuator Model once the model has been initialized and a normal run began, except for the insertion of predetermined faults or the initiation of a stop or freeze mode as shown in Figure 3.1.

Faults shall be sent in digital form from the Sigma computer software to the MC6800 for forwarding to the normal inputs of each of the four input channels. The faults shall be: "plus hardover," "negative hardover" or "zero" input. These faults shall be entered either singularly or in pairs.

3.2.1.3

Once the MMES is placed in the run mode by an operator, the Sigma software shall not communicate with the TVC Actuator Model microprocessors except when the operator initiates either a stop mode or a freeze mode.

The stop mode shall cease operation of the TVC Actuator Model.

The freeze mode shall be conducted in a manner similar to the stop mode except that the Sigma software shall query the microprocessor to determine the exact analog signal condition that exists at the time of the freeze. The digitized analog data shall be gathered by the microprocessor and transmitted to the Sigma computer for subsequent storage. The Sigma shall then retransmit this stored data back to the microprocessor to be used as the initial conditions at the end of the freeze.

3.3 Microprocessor Software

3.3.1

The microprocessor software and its interactions with the Sigma computer are shown in detail in Figure 3.2. This flow chart depicts the steps which must be taken to load the input registers of the microprocessor and prepare it to execute the steps required by the Sigma.

3.3.2

The microprocessor shall act only on the instructions of the Sigma computer. The functions of the microprocessor shall include data acquisition and transmittal to the Sigma, control of the digital to analog converts (DAC), control of the analog to digital converter (ADC) and control of the electronic switching functions.

3.3.2.1

The TVC Actuator model DAC and ADC flowcharts are shown in Figure 3.3 and 3.4, respectively.

3.3.3

The functions that the microprocessor must perform are listed in the following paragraphs.

3.3.3.1

The TVC actuator model shall be capable of being initialized at any point within its normal range of operation.

MICROPROCESSOR/SIGMA-TYPE INTERFACE
FLOW DIAGRAM

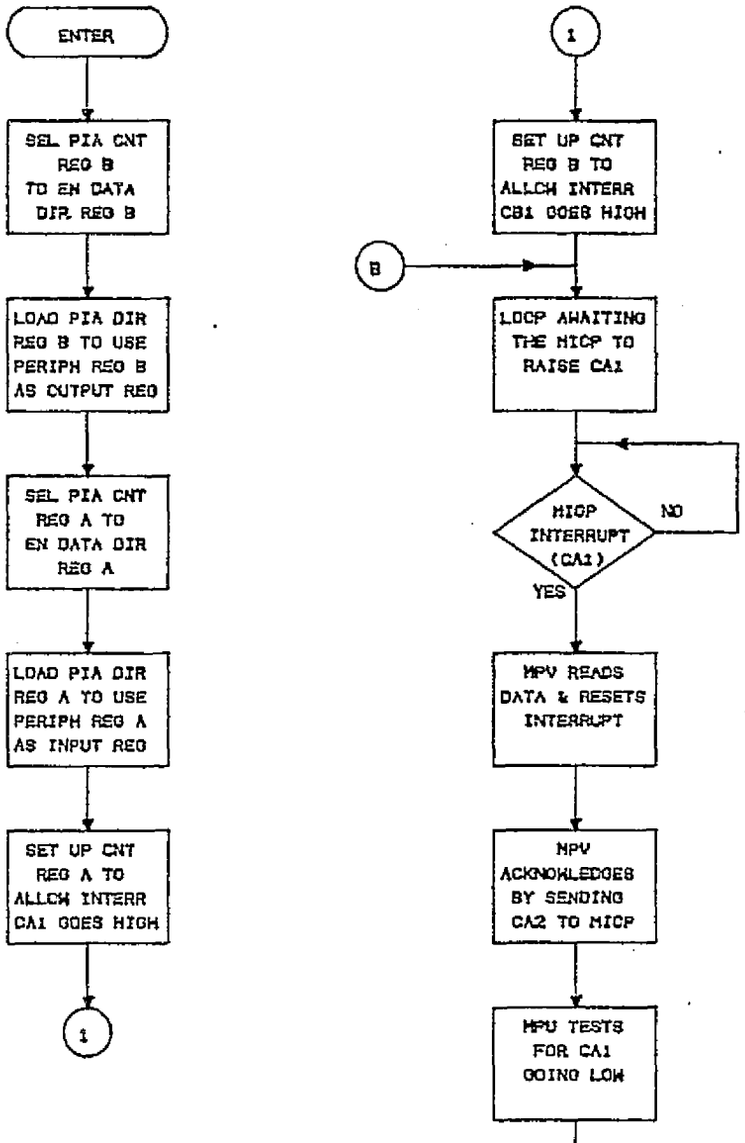


Figure 3.2

OPERATIONAL SIMULATION PROGRAM
FOR EACH TVC ACTUATOR MODEL

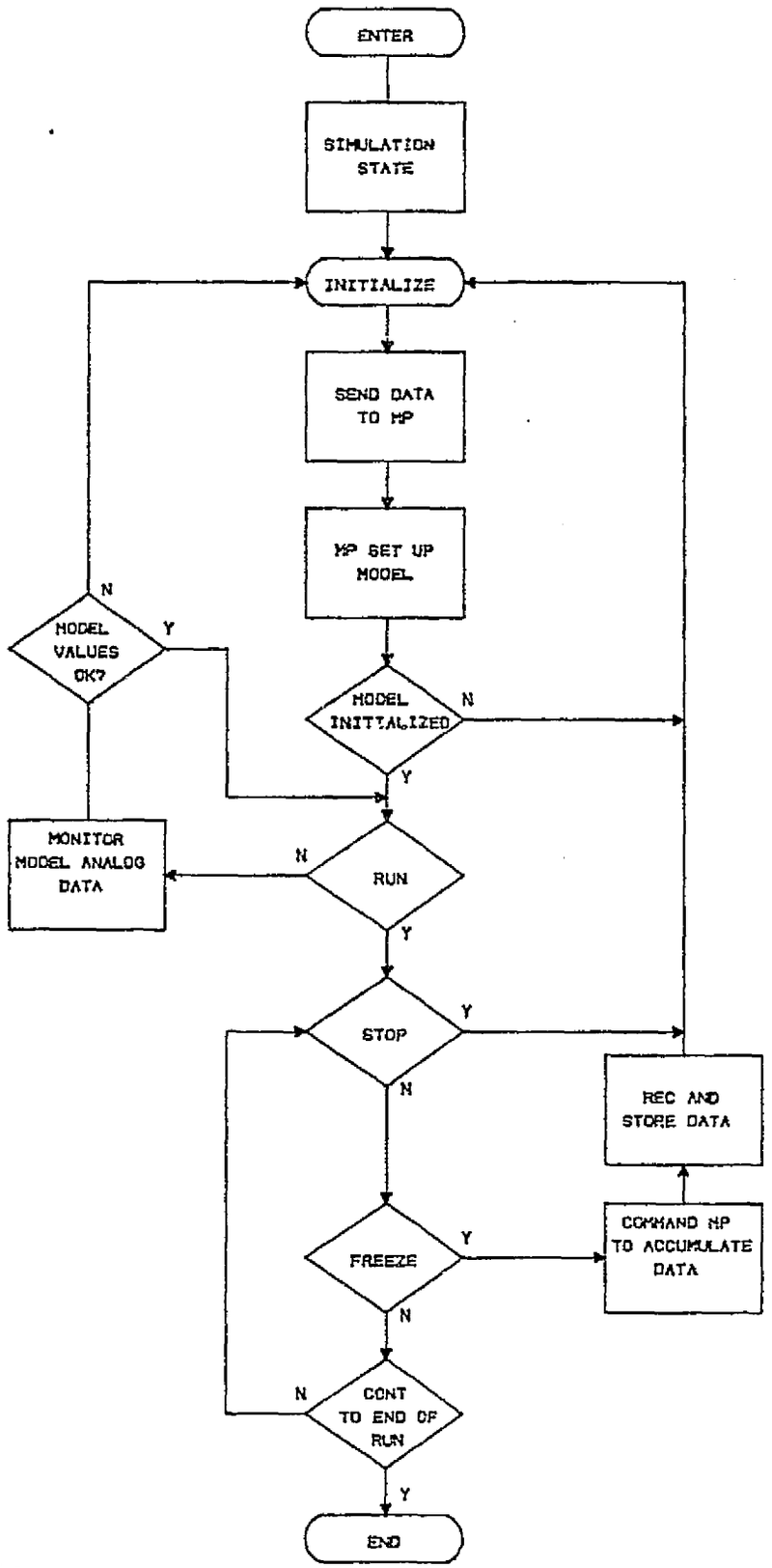


Figure 3.1

MICROPROCESSOR/SIGMA-TYPE INTERFACE
FLOW DIAGRAM
(Continued)

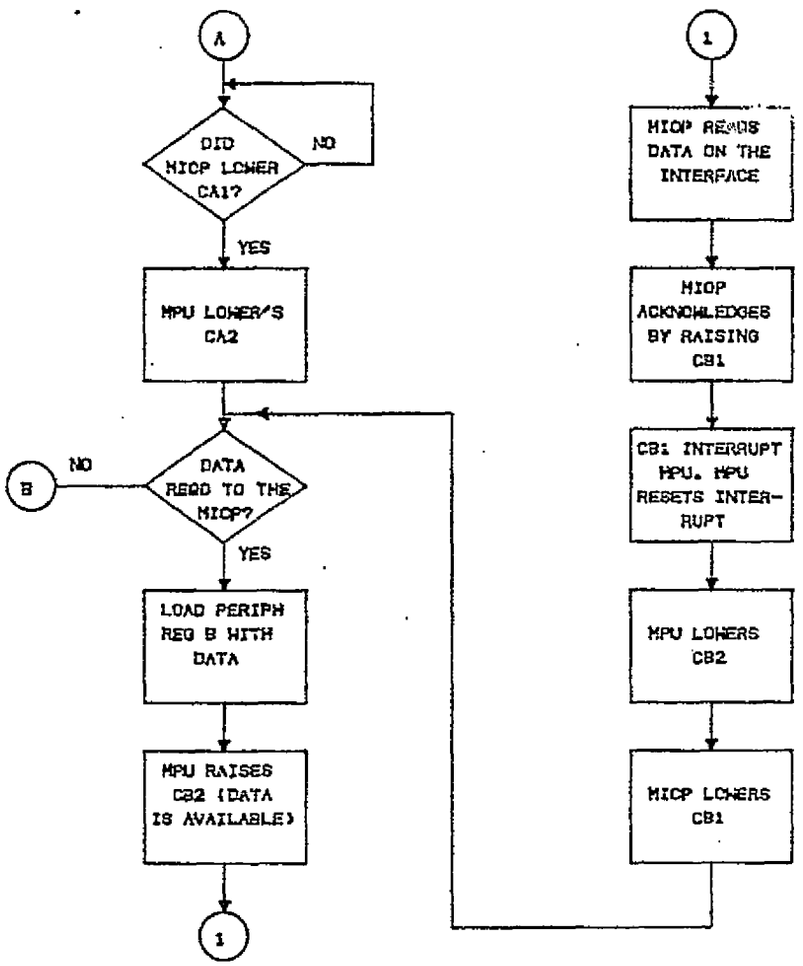


Figure 3.2
(Continued)

D/A PROGRAMMING FLOW CHART

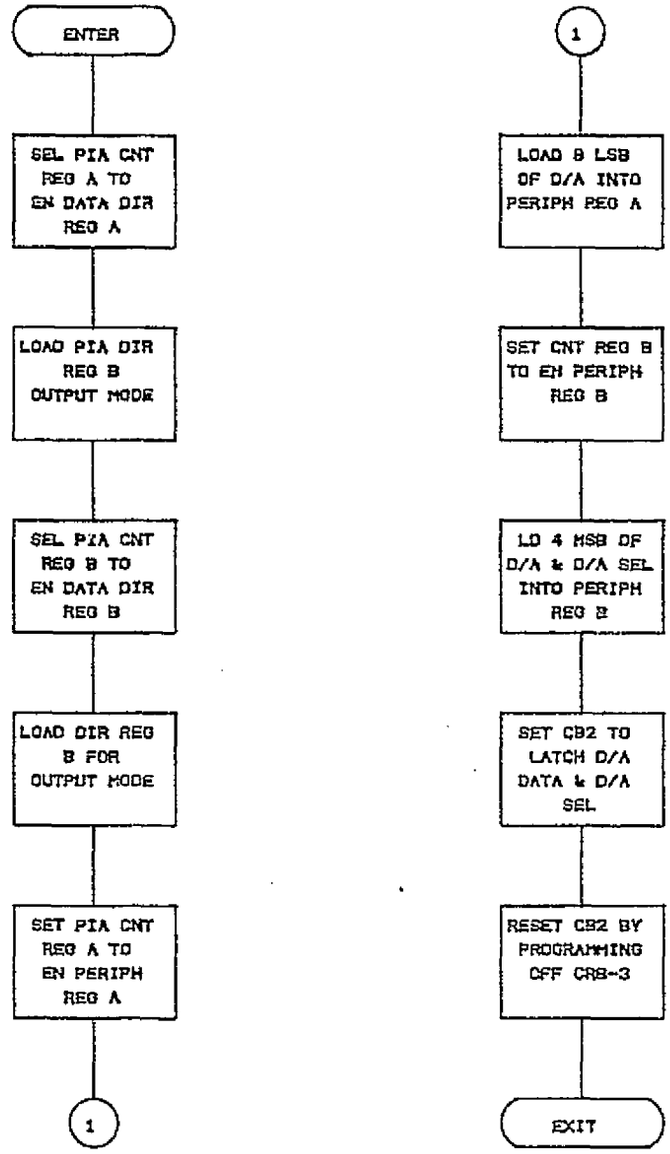


Figure 3.3

A/D PROGRAMMING FLOW CHART

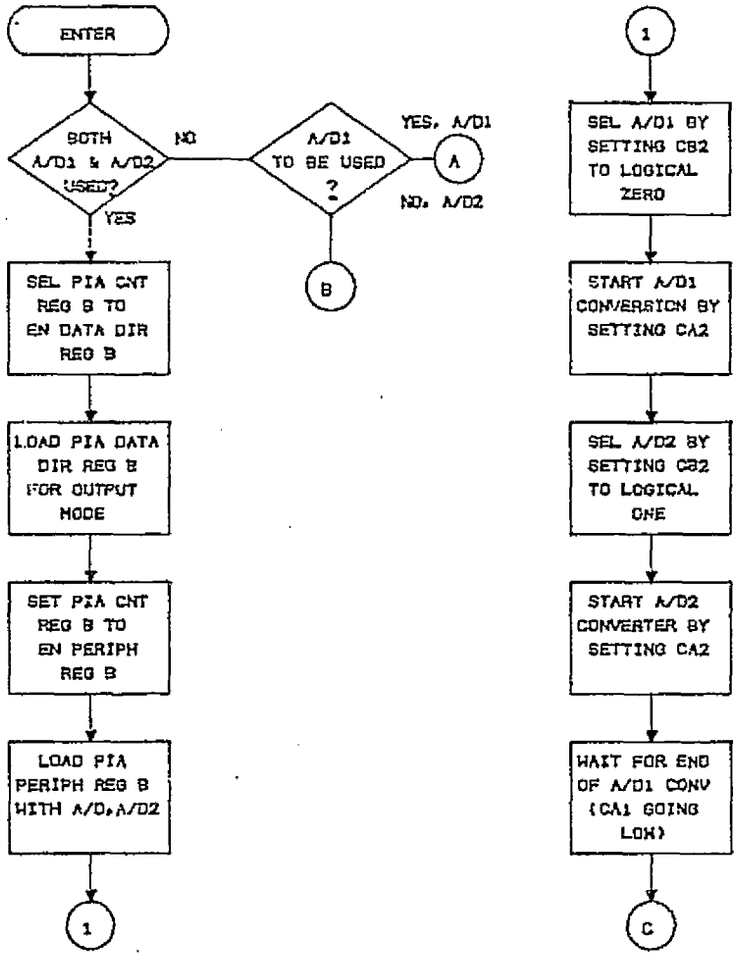


Figure 3.4

A/D PROGRAMMING FLOW CHART
(Continued)

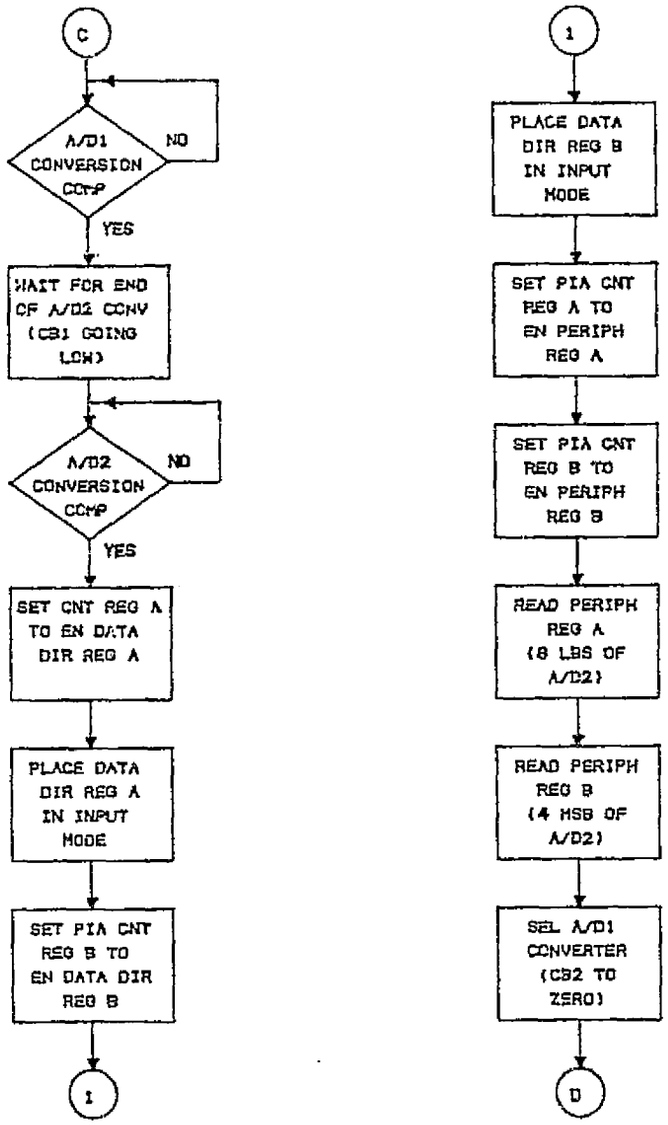


Figure 3.4
(Continued)

A/D PROGRAMMING FLOW CHART
(Continued)

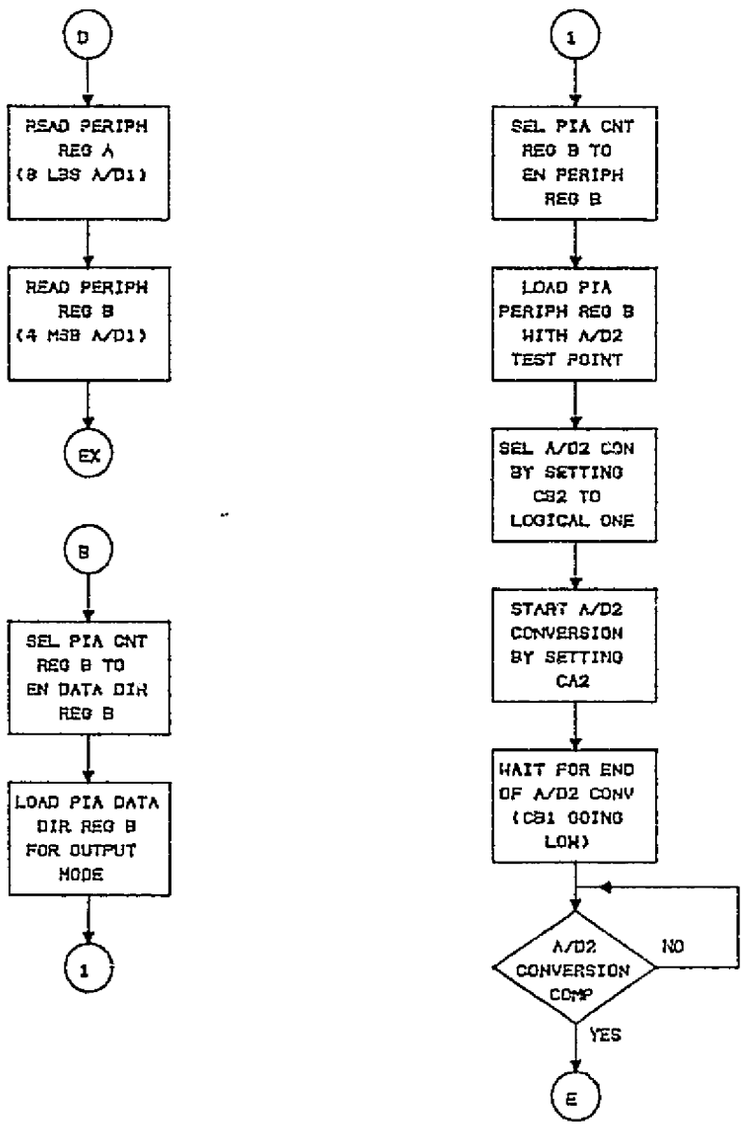


Figure 3.4
(Continued)

A/D PROGRAMMING FLOW CHART
(Continued)

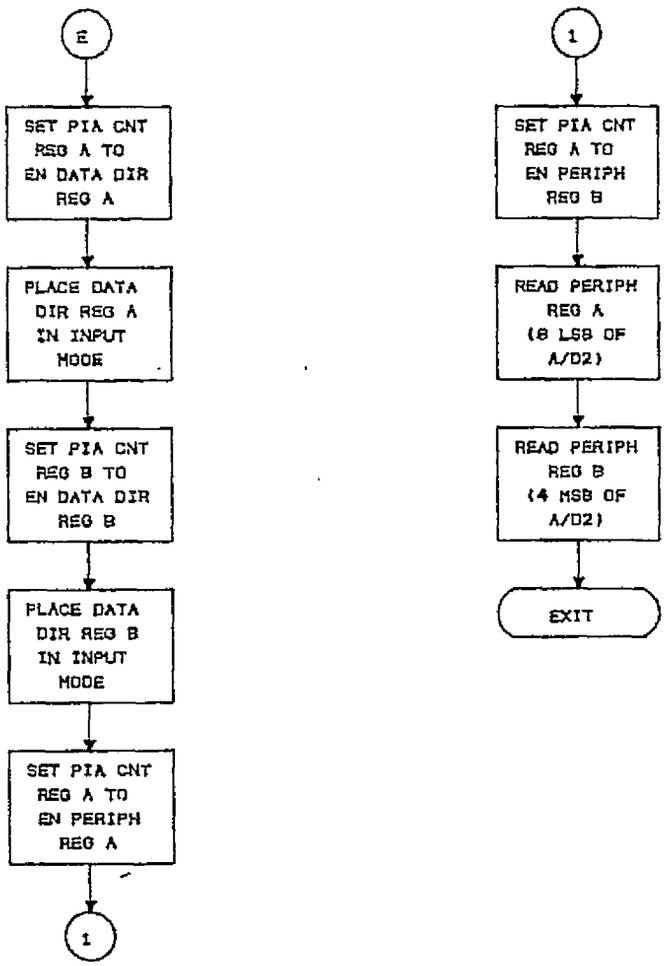


Figure 3.4
(Continued)

A/D PROGRAMMING FLOW CHART
(Continued)

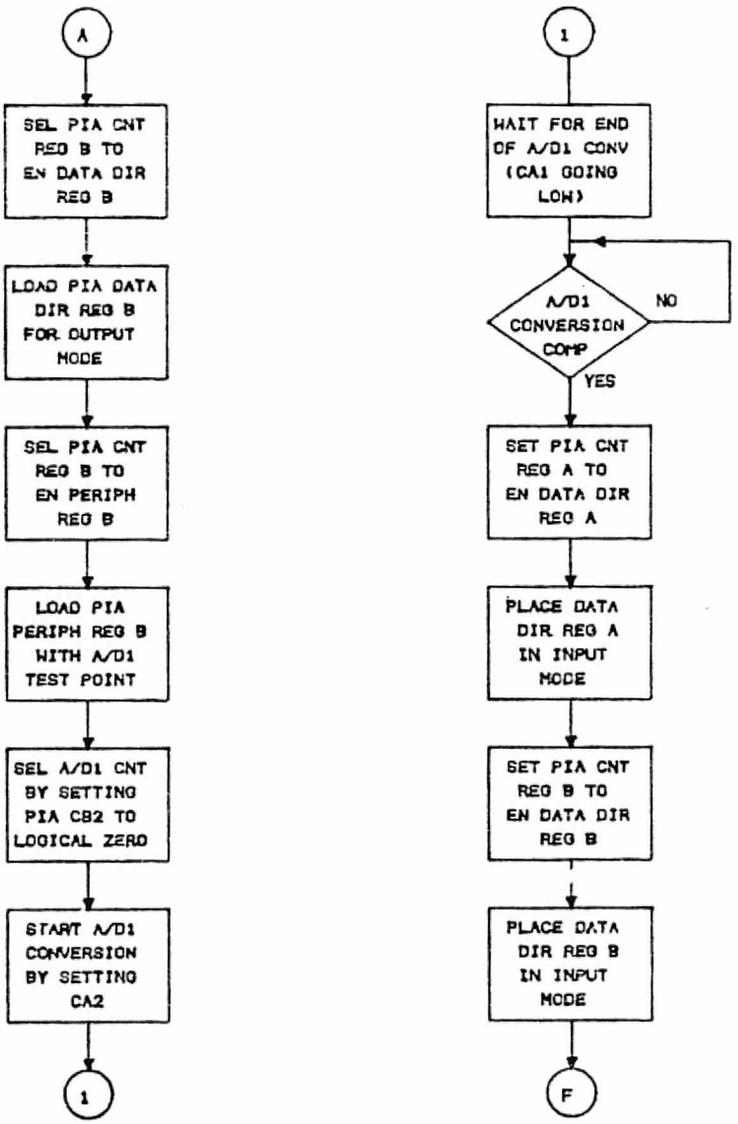


Figure 3.4
(Continued)

A/D PROGRAMMING FLOW CHART
(Continued)

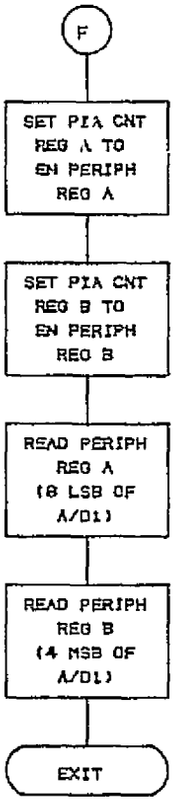


Figure 3.4
(Continued)

This will be accomplished by obtaining from the Sigma the command to initialize and the point to which the model should be initialized. The microprocessor shall then input, through the DAC, the value obtained from the Sigma to the four input servovalve channels of the model. In addition, the desired output of the model shall be established on the SDS outputs of the model by placing the initial conditions on the output integrators and holding this value until a run instruction is received.

3.3.3.2

Fault insertion shall be in accordance with Paragraph 3.2.1.2.

3.3.3.3

The freeze mode shall be initiated by the Sigma software. At the initiation of the freeze, the outputs of the TVC actuator model shall be read by the ADC and these values sent to the Sigma computer for storage to be used as the initialization values of the model at the end of the freeze period.

4. QUALITY ASSURANCE PROVISIONS

4.1 TVC Model Test Software

4.1.1 Description

The testing of the microprocessor and TVC actuator model will consist of two test phases. First, the microprocessor will be tested by itself, followed by an overall test of the TVC actuator under the control of the microprocessor.

4.1.2 Microprocessor Test

The test flowchart shown in Figure 4,1 depicts the tests that shall be performed on the microprocessor. These tests shall be initiated, controlled, and analyzed by either a serial I/O device driving the microprocessor, or the Sigma computer.

4.1.3 TVC Actuator Model Test

This test shall exercise the model electronics by energizing various input conditions, both static and dynamic, from the Sigma computer through the DAC to the servovalve inputs. The microprocessor shall configure the output ADC such that various points within the model are queried. This data is then acquired by the microprocessor and transmitted to the serial I/O device, which will normally be the Sigma computers for error checking and analysis.

MICROPROCESSOR TESTING

TEST-FLOW CHART	FUNCTIONAL TEST DESCRIPTION
RESET	Verify that MPU vectors to FFFF after power up or reset.
PROGRAM COUNTER TEST	Increment program counter through its full range.
MEMORY TEST	Perform data equal-to address test for all 4K locations. Perform all ones test, all zeroes test and checker board tests for all 4K RAM locations. Perform sum check on EPROM.
STACK POINTER TEST	Verify that the stack pointer can increment and decrement through its full range.
ALU	Verify that the ALU will add, subtract, detect a "0", a positive value and a negative value; perform a carry and perform all logical instructions.
ACCUMULATOR	Verify load, readback, rotate and transfer operations with multiple pattern combination.
TIMING AND CONTROL	Exercise all external stimulae and verify their correct action.
INSTRUCTION DECODER	Perform all instructions that have not been previously exercised.

Figure 4.1

5. PREPARATION FOR DELIVERY

Not applicable.

6. NOTES

Not applicable.

APPENDIX E

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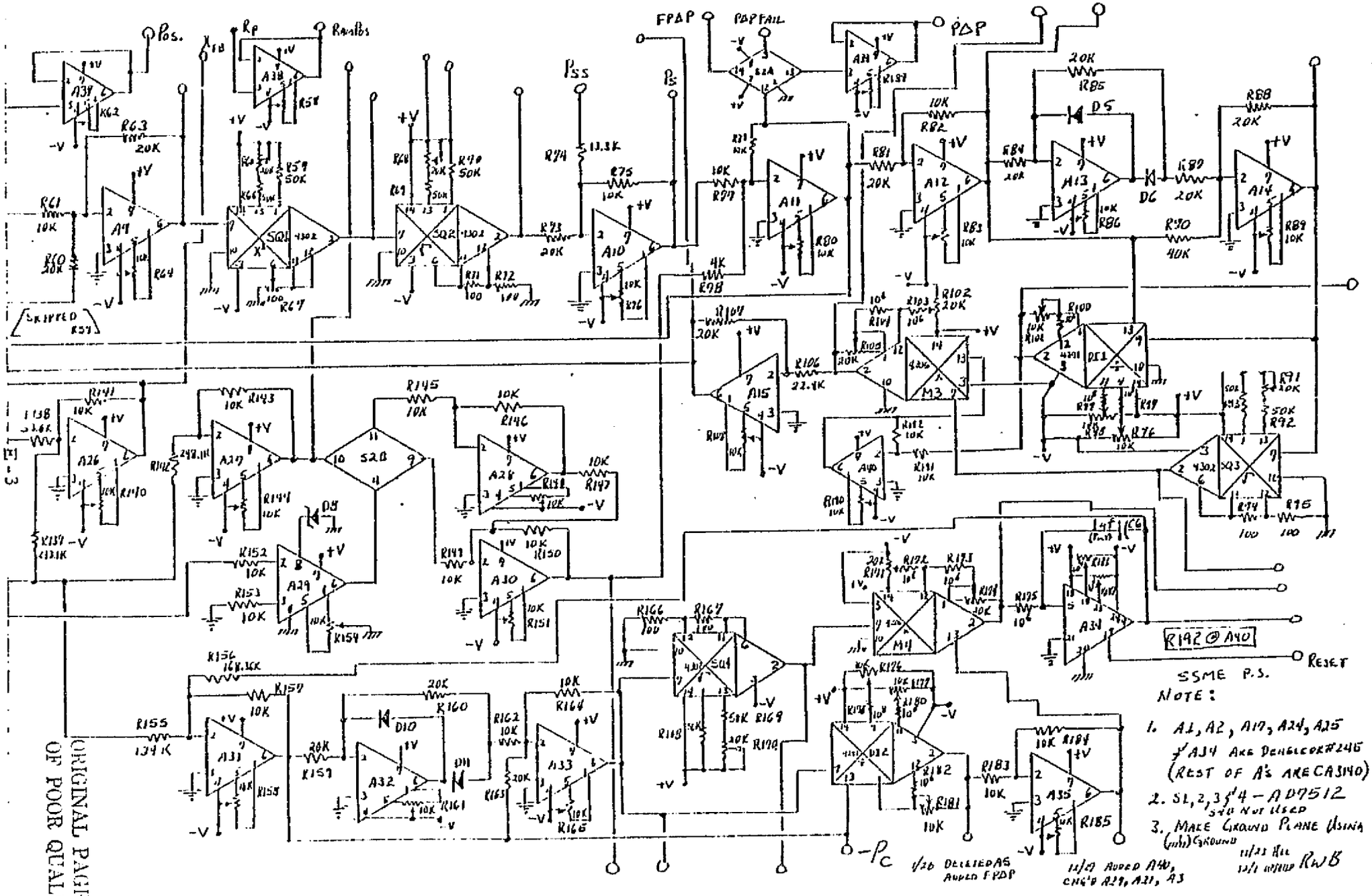

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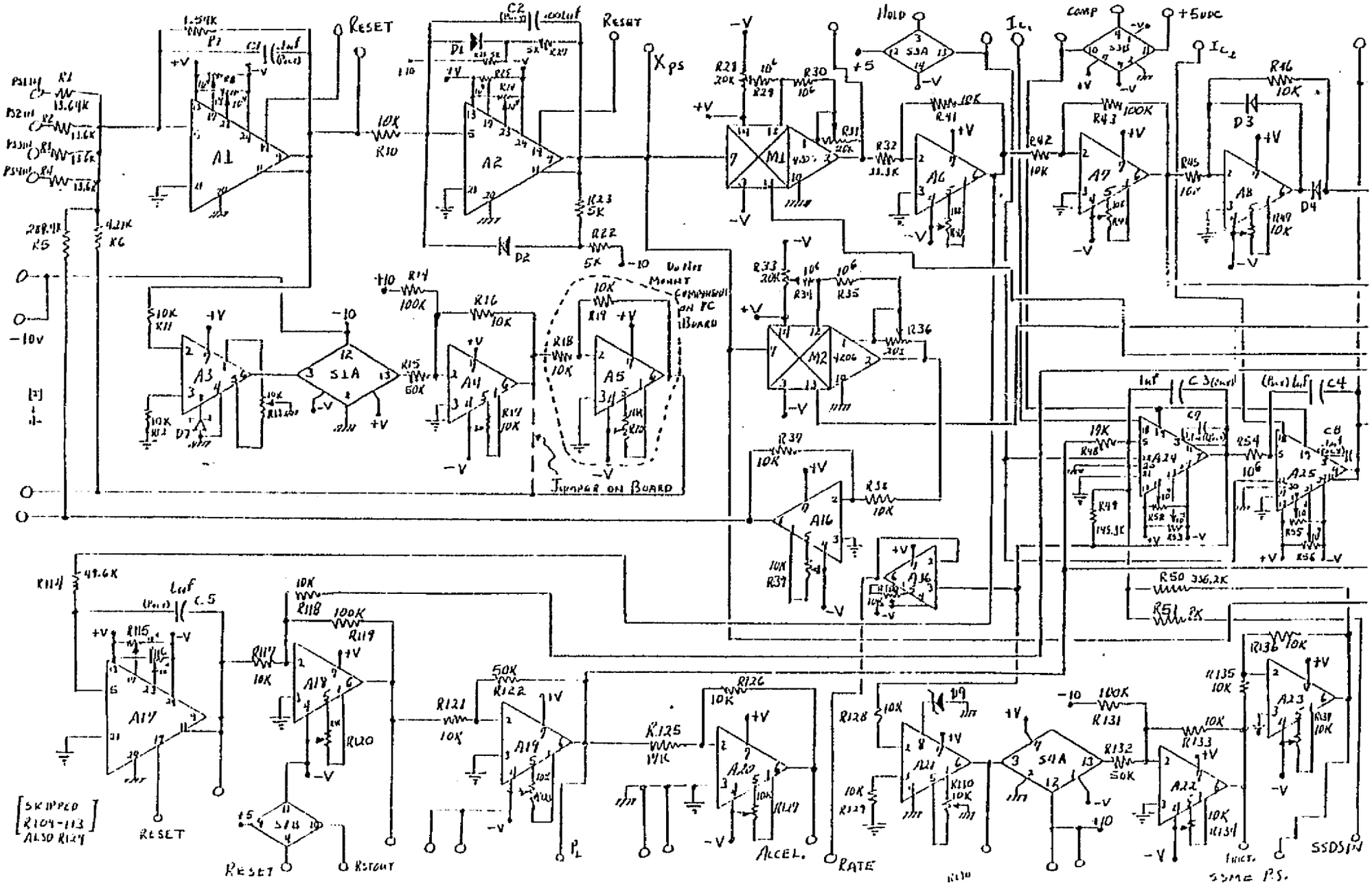
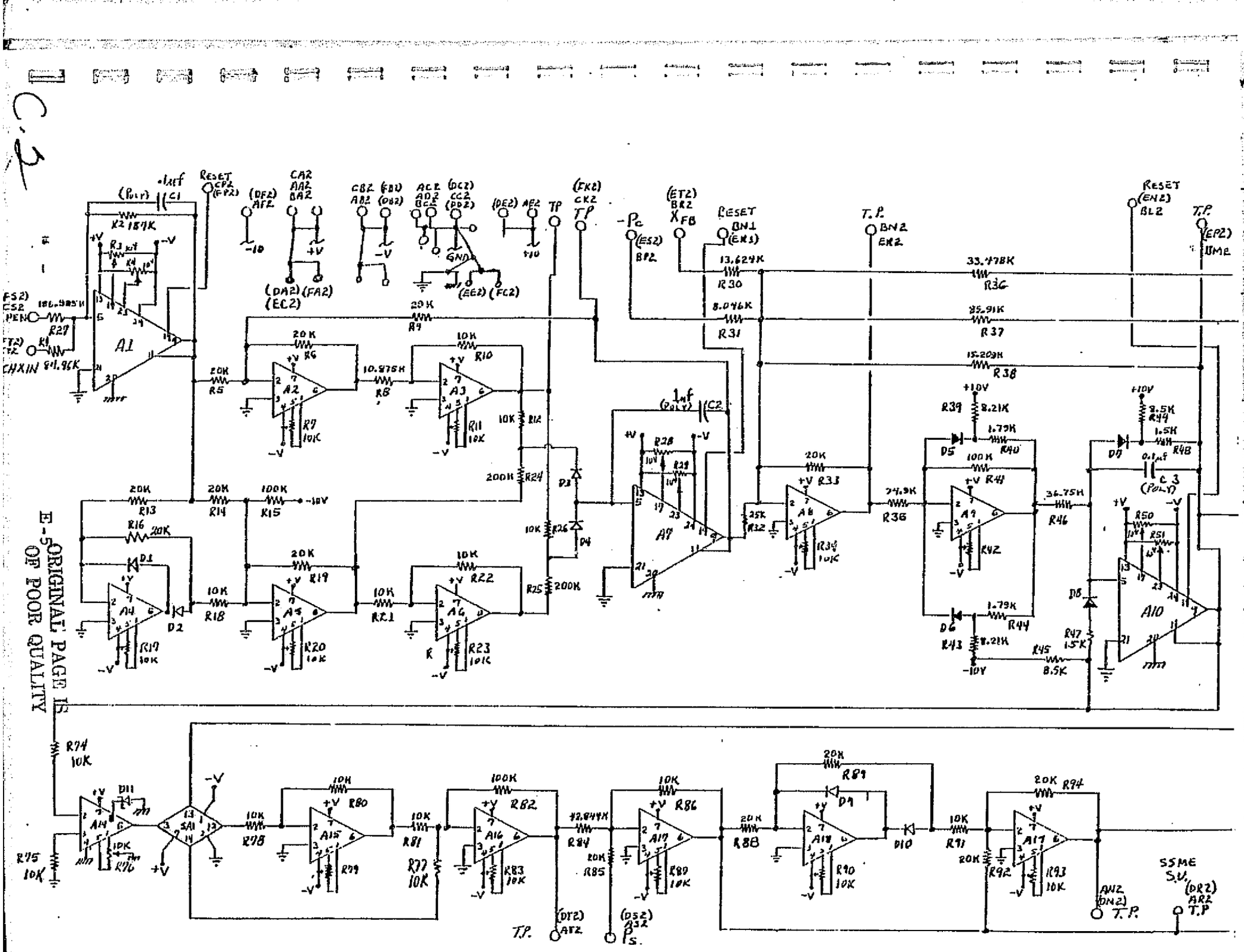

RESET
Xps
HOLD
COMP
+5VDC
IL1
IL2
JUMPER ON BOARD
RESET
RESET
RSTOUT
ACCEL.
RATE
SSDSIN
SSMC P.S.

C-2



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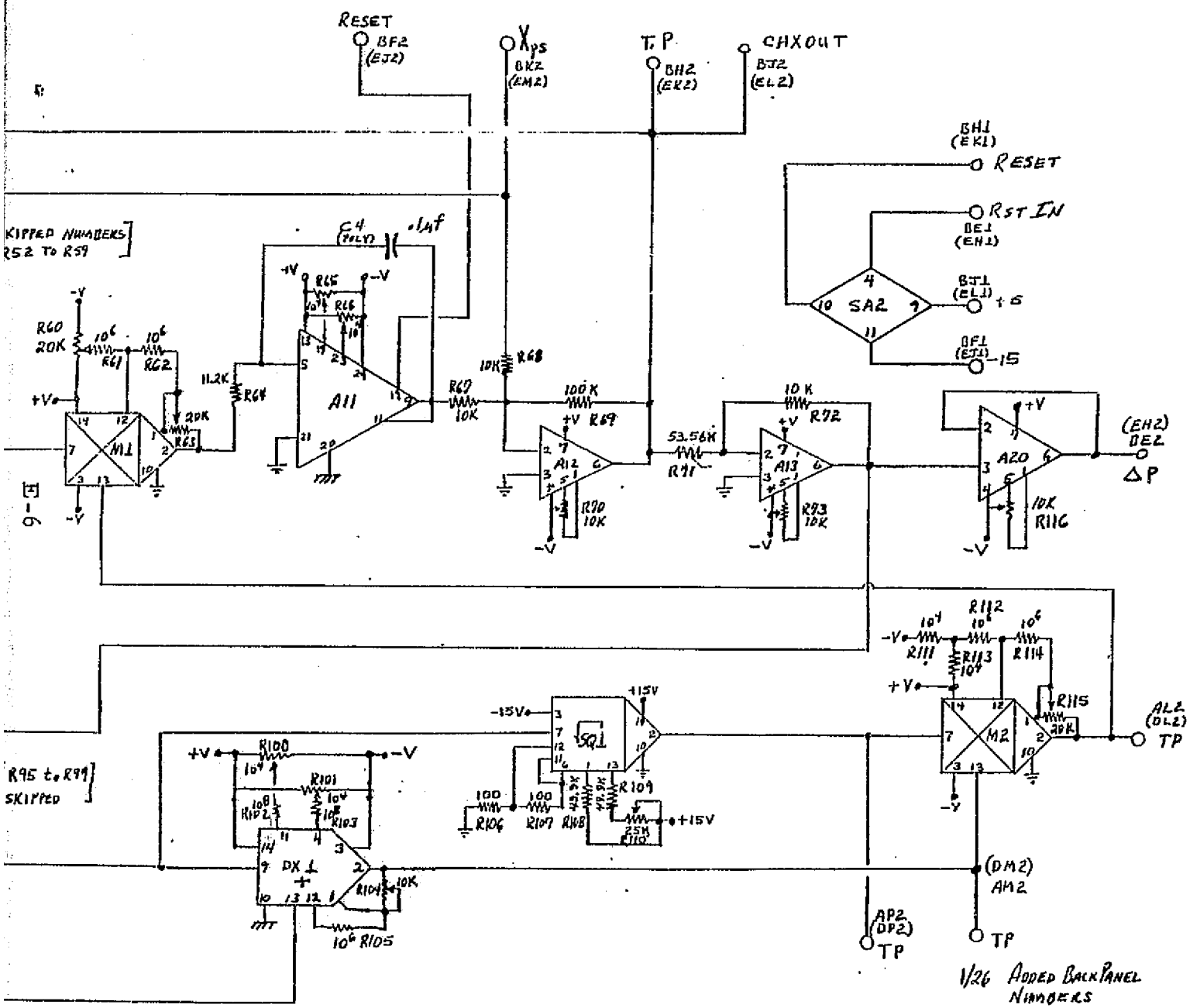


NOTES:

1. DEVICES:

   A's - Op Amps - CA3140

   A1, A9, A10 & A11 ARE PENELCOR #245 24 PIN DEVICES

   SA - SWITCH - AD7512

   M1 & M2 - MULTIPLIER - 4206

   DX1 - DIVIDER - 4291

   SQ1 - MULTIFUNCTION - 4302

2. AD7512 14 PIN DEVICE

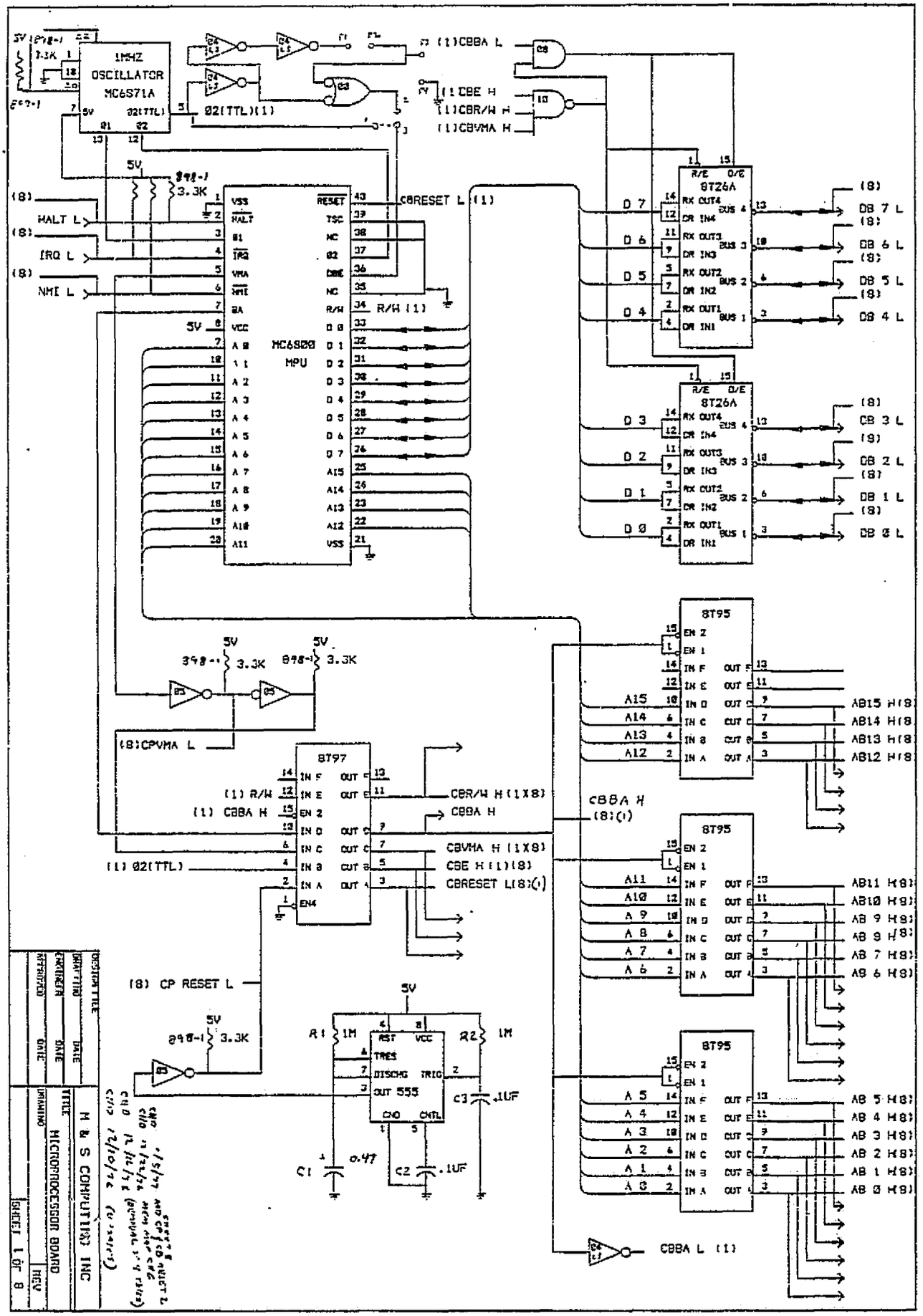
3. PLACE CAPS FROM +V, & -V TO GROUND NEAR ALL S, M, R & DX DEVICES.

4. KEEP ALL SUMMING JUNCTION RESISTORS NEAR AMPLIFIER

SSME
S.V.

10/21 RELEASED
11/1 ADDED SWITCHES
11/18 ADDED PENELCOR #245's REMOVED SWITCHES
1/26 ADDED BACK PANEL NUMBERS
11/23 ADDED A20 ISO. AMP
12/27 CHANGED A14 CONFIG.

RWB



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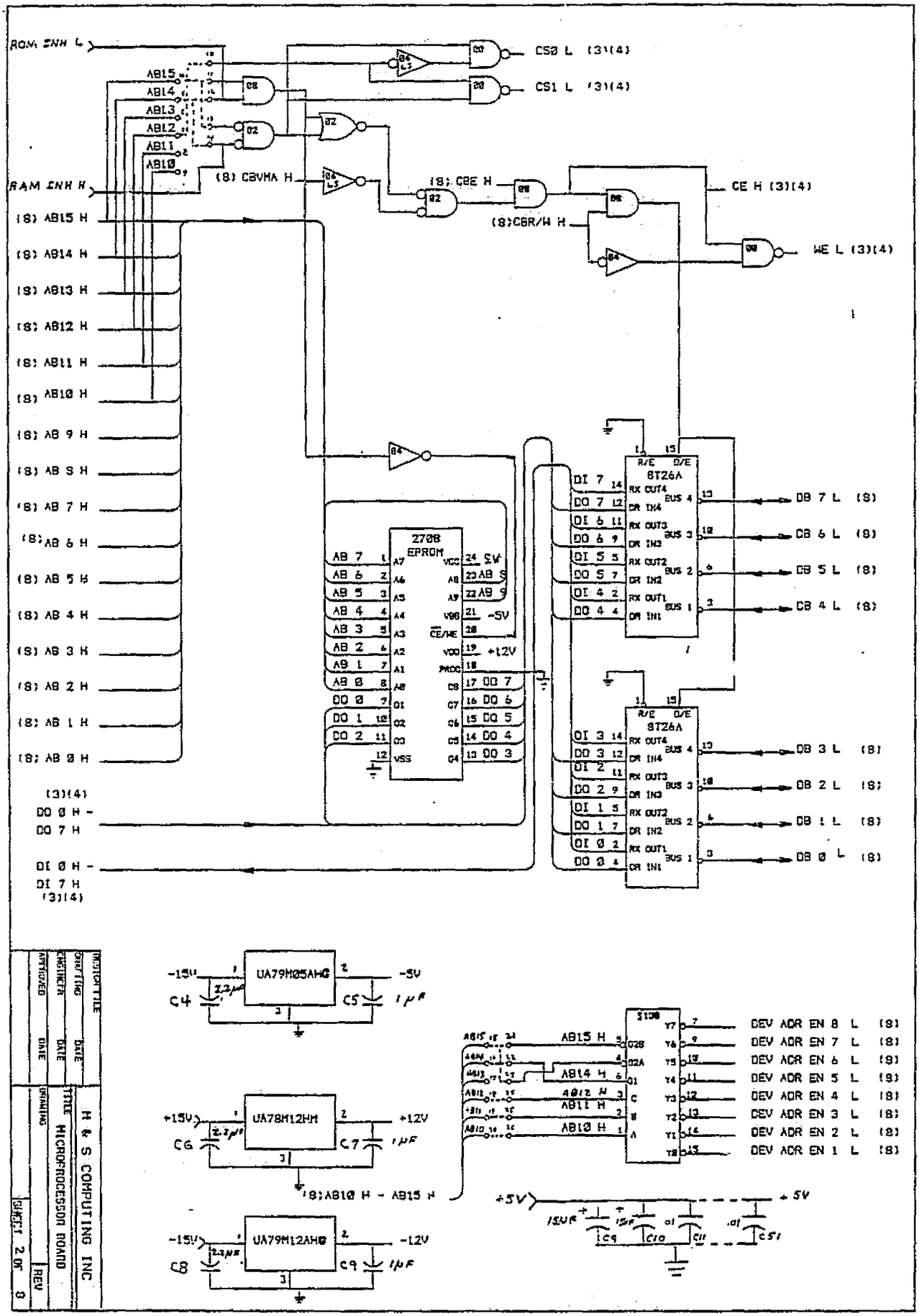
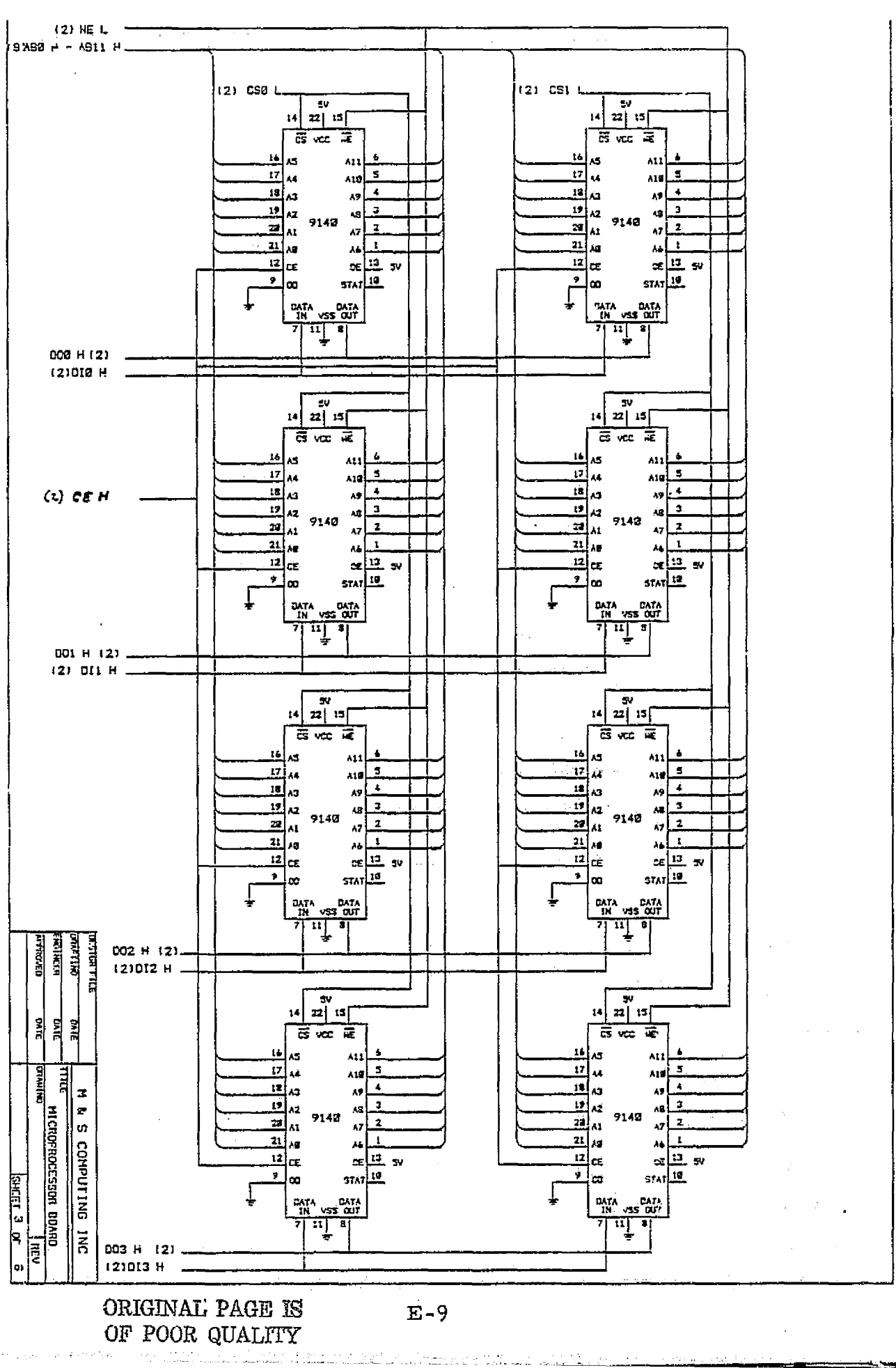
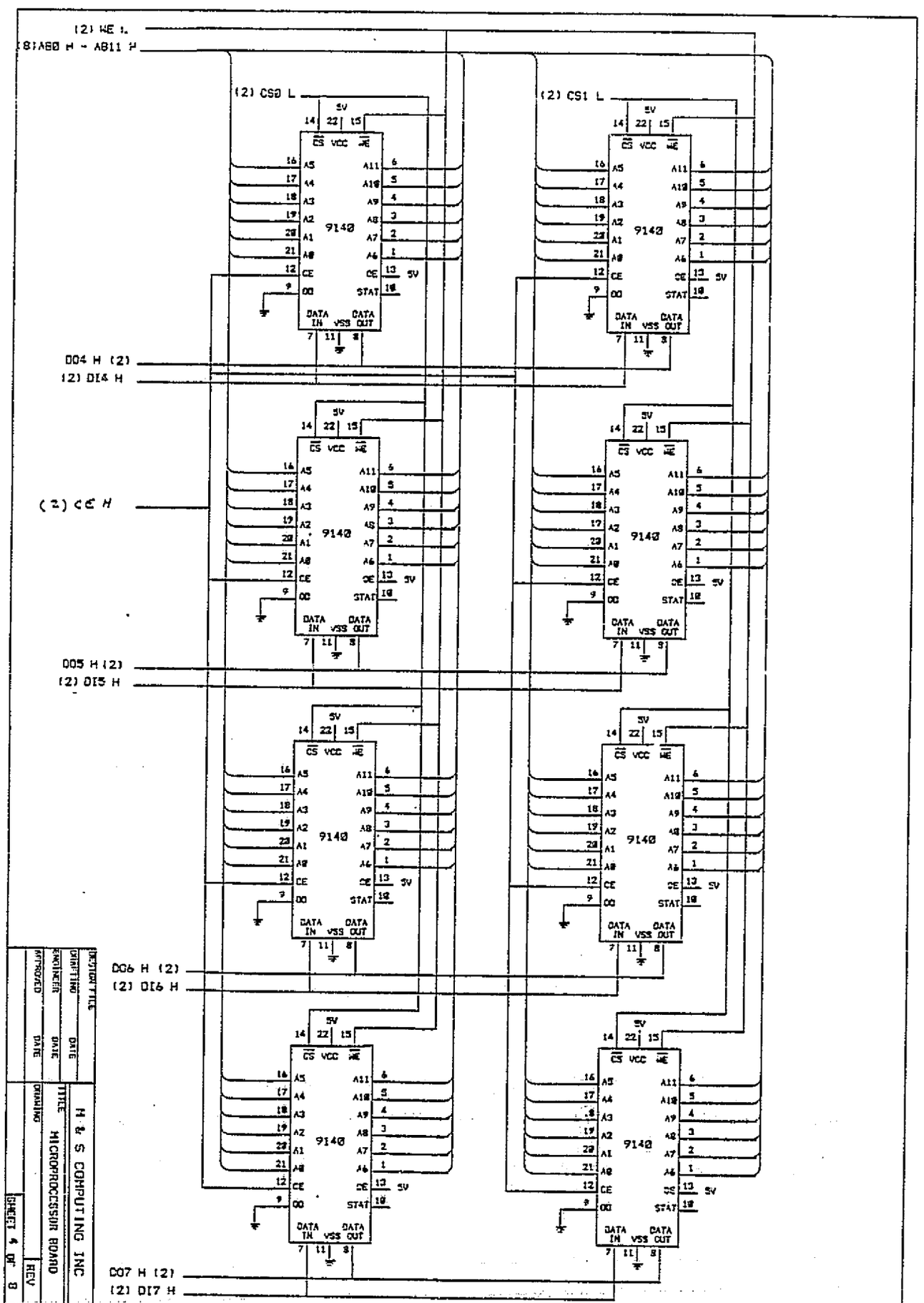
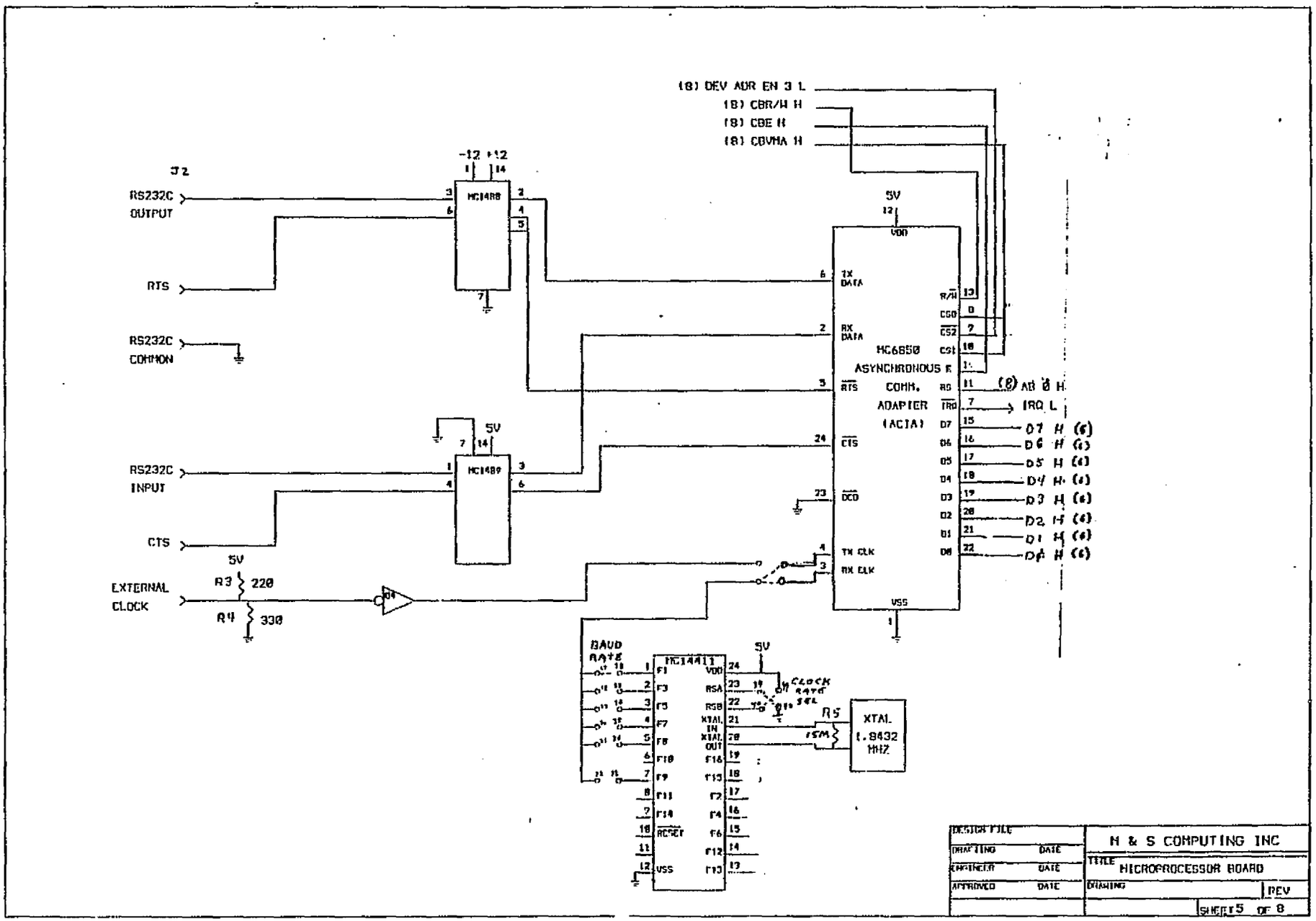

ROM ENH L
RAM ENH H
AB15
AB14
AB13
AB12
AB11
AB10
(8) CBVMA H
(8) CBE H
(8) CBR/W H
CS0 L (3)(4)
CS1 L (3)(4)
CE H (3)(4)
WE L (3)(4)
(8) AB15 H
(8) AB14 H
(8) AB13 H
(8) AB12 H
(8) AB11 H
(8) AB10 H
(8) AB 9 H
(8) AB 8 H
(8) AB 7 H
(8) AB 6 H
(8) AB 5 H
(8) AB 4 H
(8) AB 3 H
(8) AB 2 H
(8) AB 1 H
(8) AB 0 H
2708 EPROM
8T26A
DB 7 L (8)
DB 6 L (8)
DB 5 L (8)
DB 4 L (8)
DB 3 L (8)
DB 2 L (8)
DB 1 L (8)
DB 0 L (8)
(3)(4) DO 0 H - DO 7 H
DI 0 H - DI 7 H (3)(4)
UA79M05AHC
UA78M12HM
UA79M12AHC
-15V
+15V
-5V
+12V
-12V
C4
C5
C6
C7
C8
C9
C10
C11
C51
(8)AB10 H - AB15 H
S138
DEV ADR EN 8 L (8)
DEV ADR EN 7 L (8)
DEV ADR EN 6 L (8)
DEV ADR EN 5 L (8)
DEV ADR EN 4 L (8)
DEV ADR EN 3 L (8)
DEV ADR EN 2 L (8)
DEV ADR EN 1 L (8)
+5V
M & S COMPUTING INC
MICROPROCESSOR BOARD
SHEET 2 OF 8




(2) WE L
(8)A00 H - A011 H
(2) CS0 L
(2) CS1 L
9140
5V
DATA IN
VSS
DATA OUT
D04 H (2)
(2) DI4 H
(2) CE H
D05 H (2)
(2) DI5 H
D06 H (2)
(2) DI6 H
D07 H (2)
(2) DI7 H
H & S COMPUTING INC
MICROPROCESSOR BOARD
DRAWING
REV
SHEET 4 OF 8



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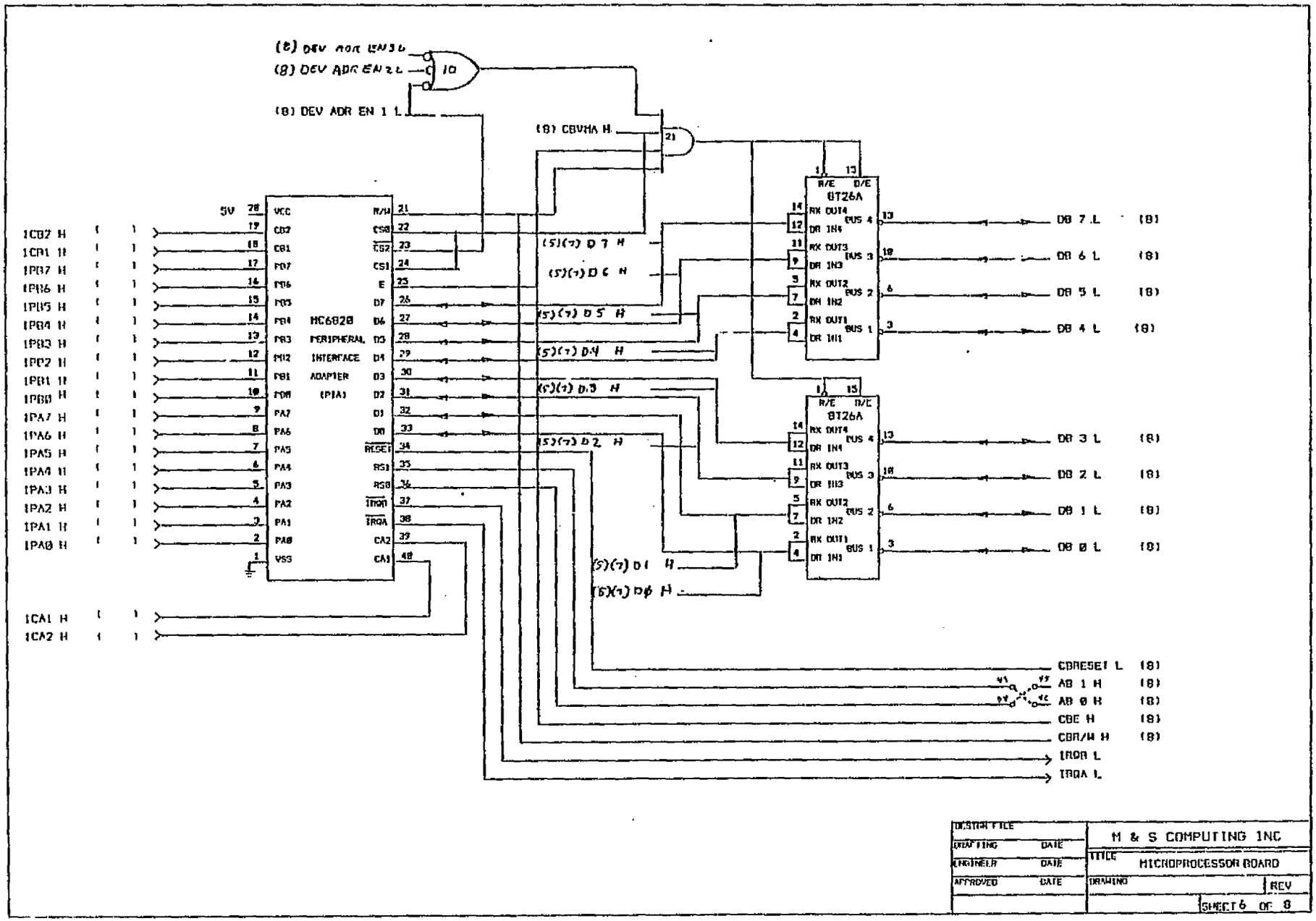
ENGINEER	DATE	DRAWING REV
APPROVED	DATE	SHEET 5 OF 8



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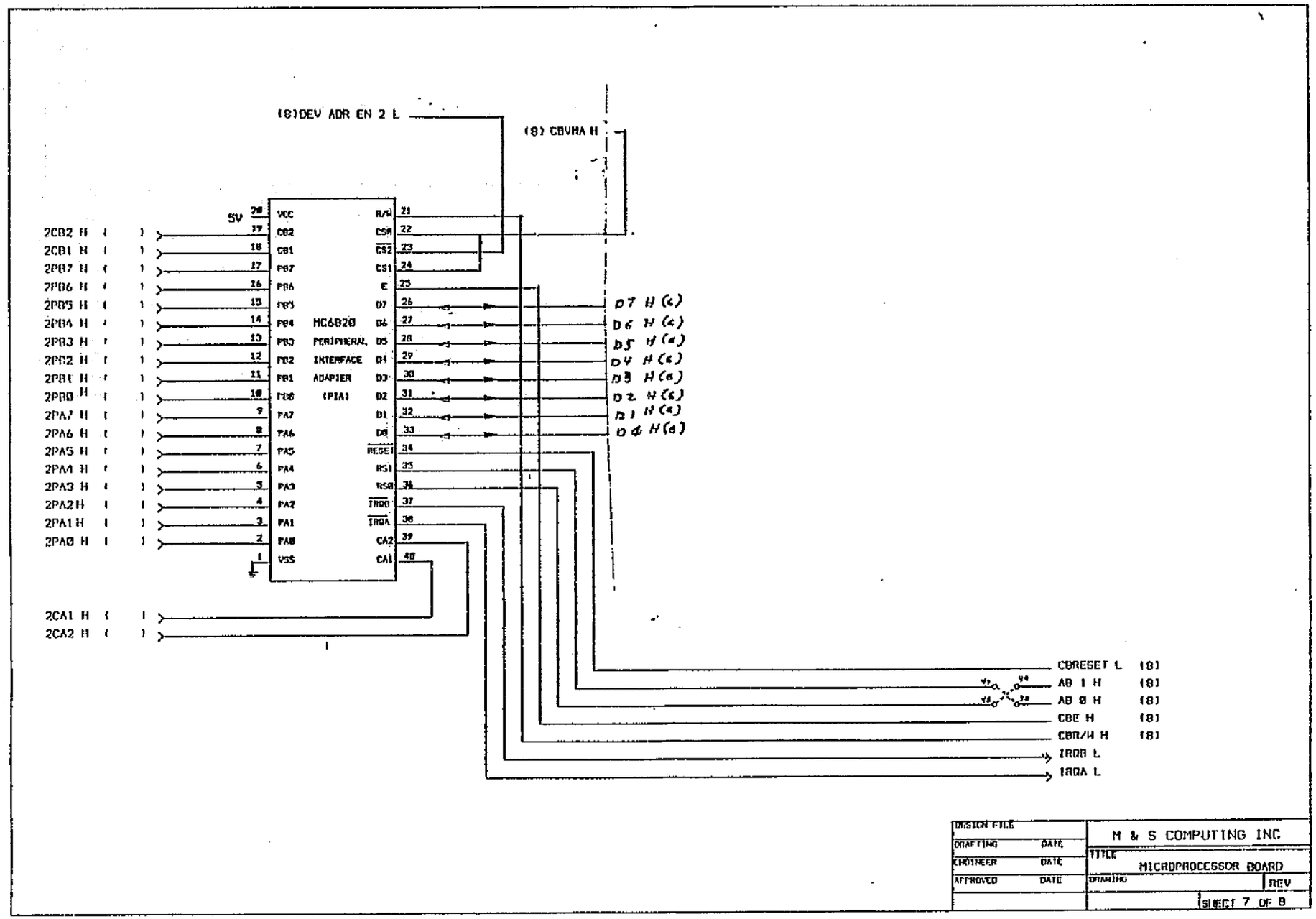
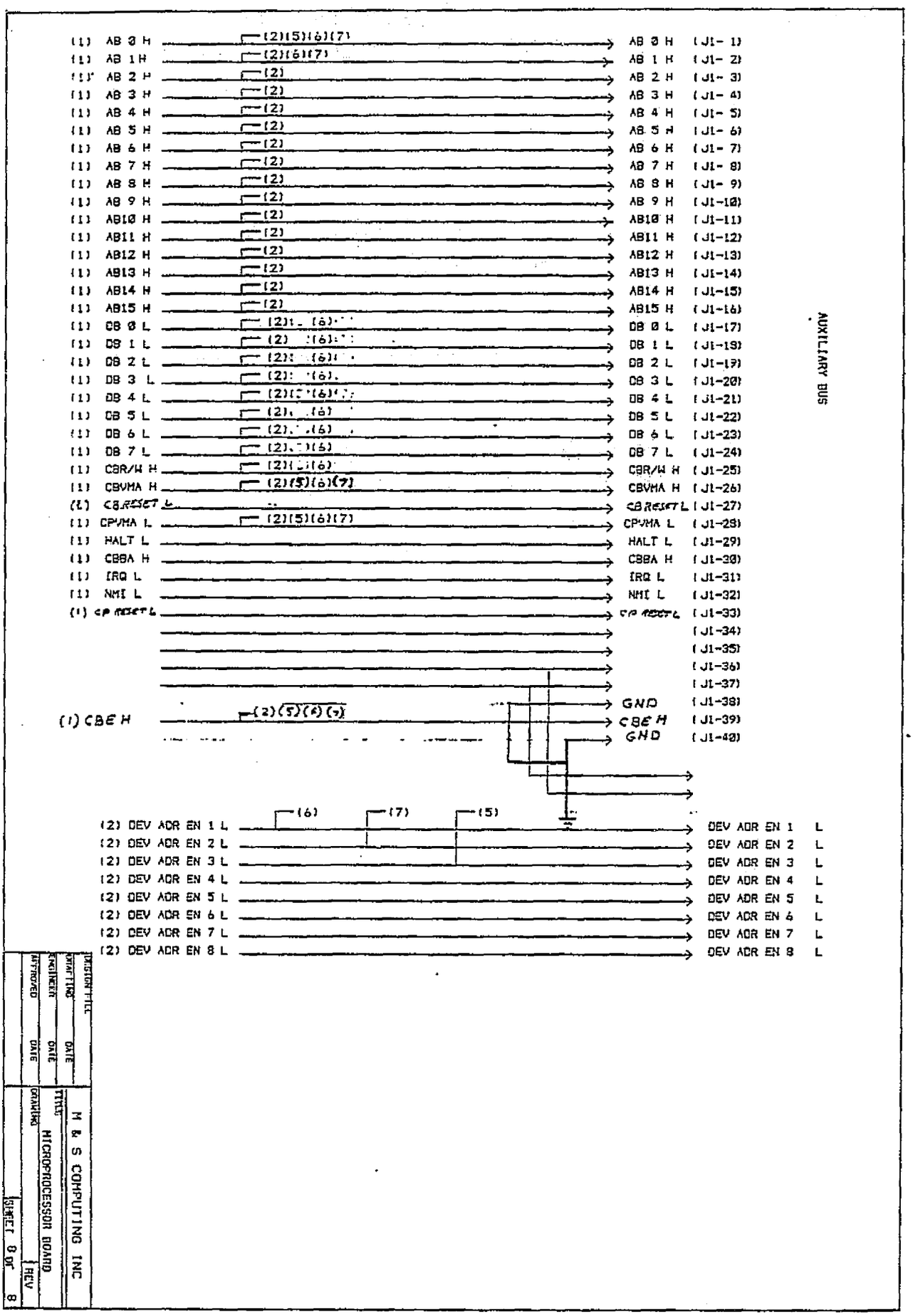
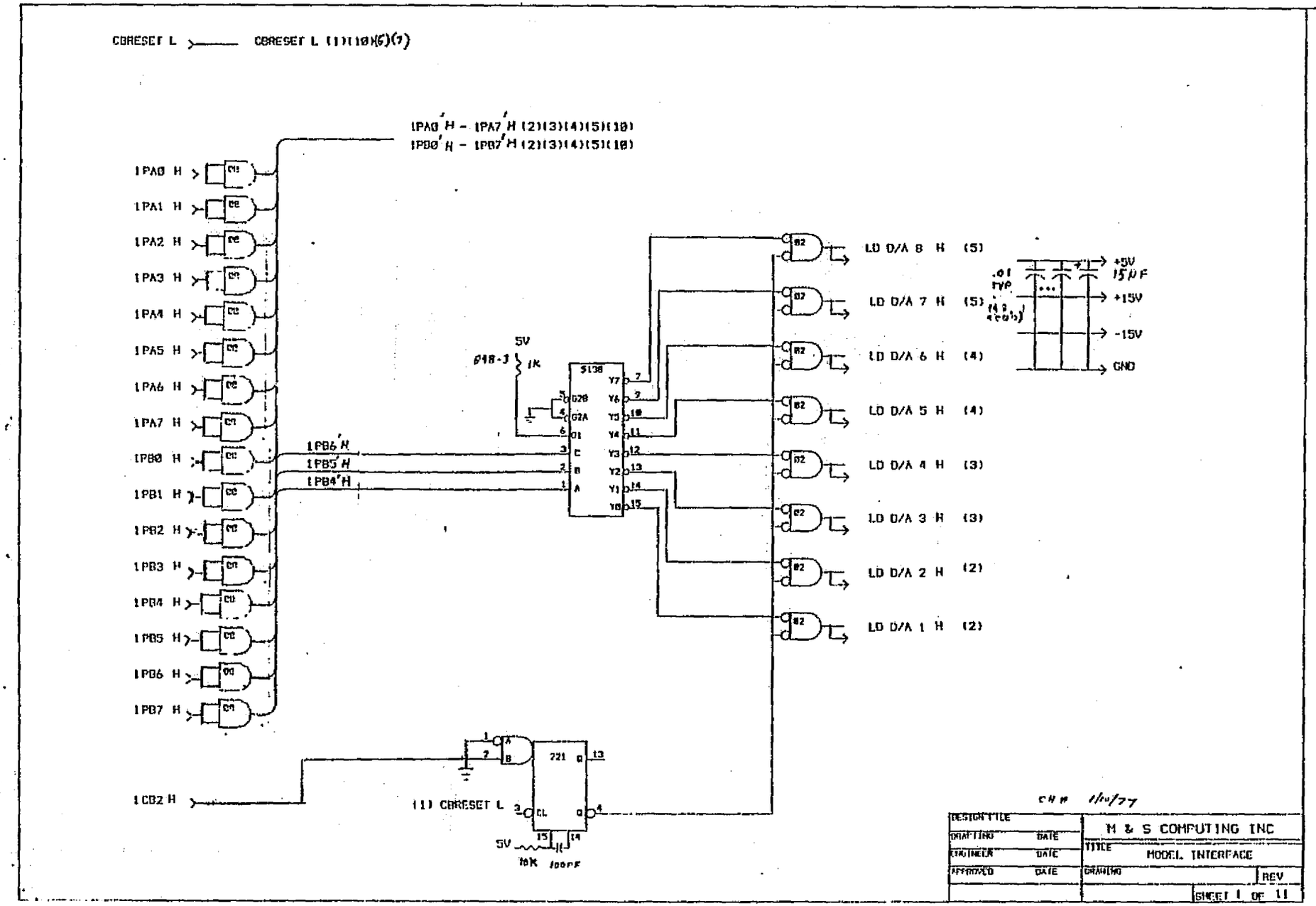
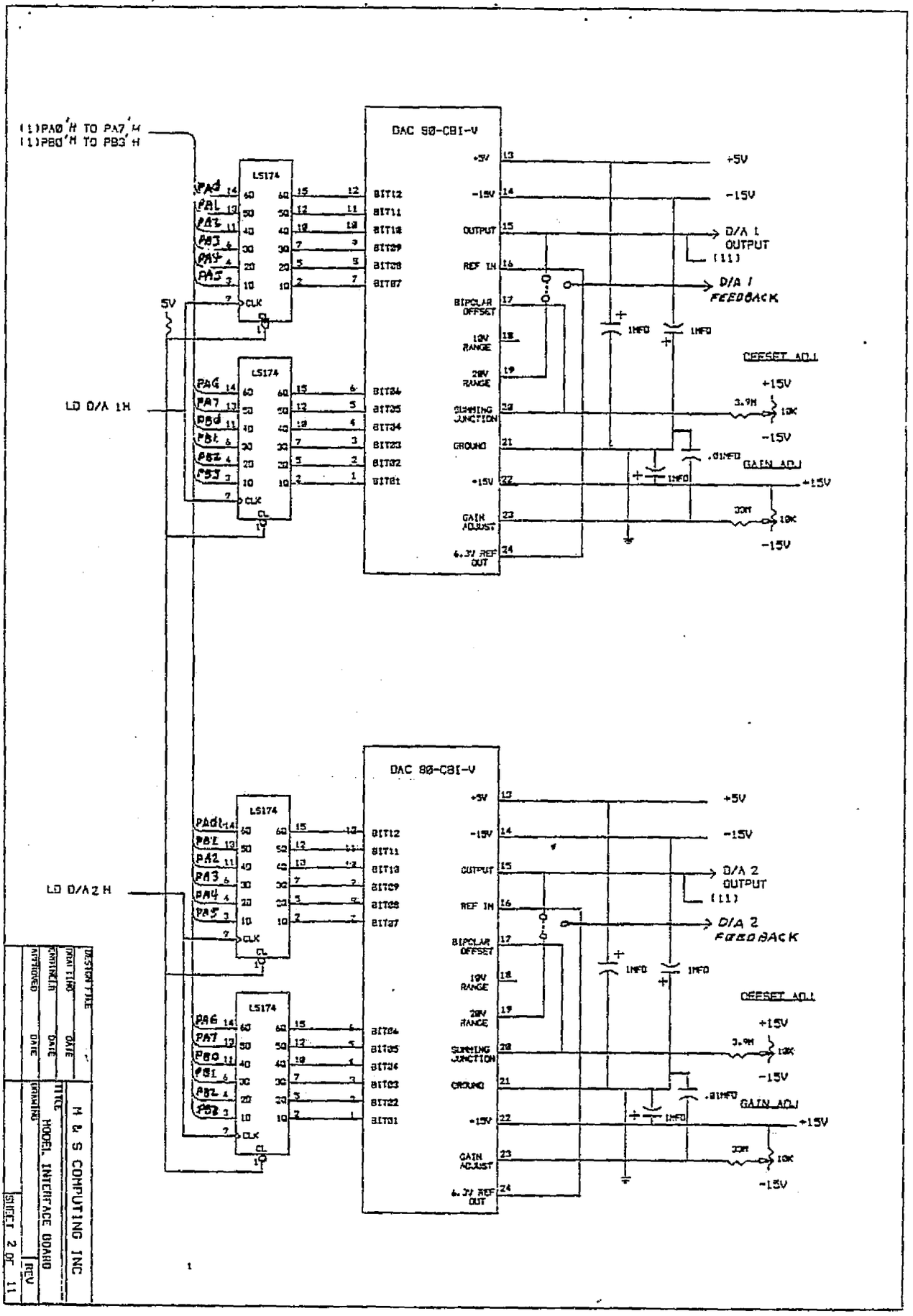
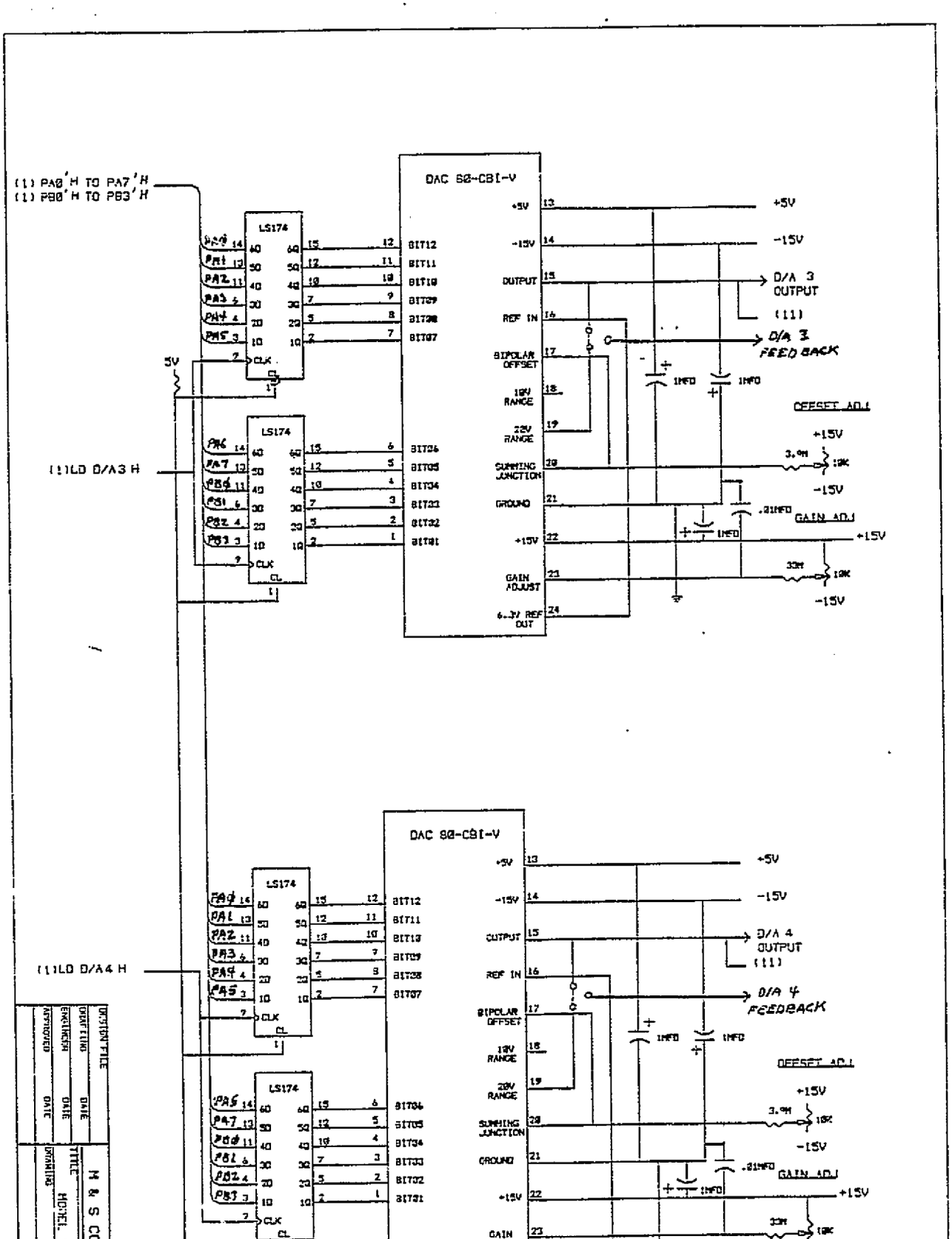
ENGINEER	DATE	DRAWING REV
APPROVED	DATE	SHEET 6 OF 8

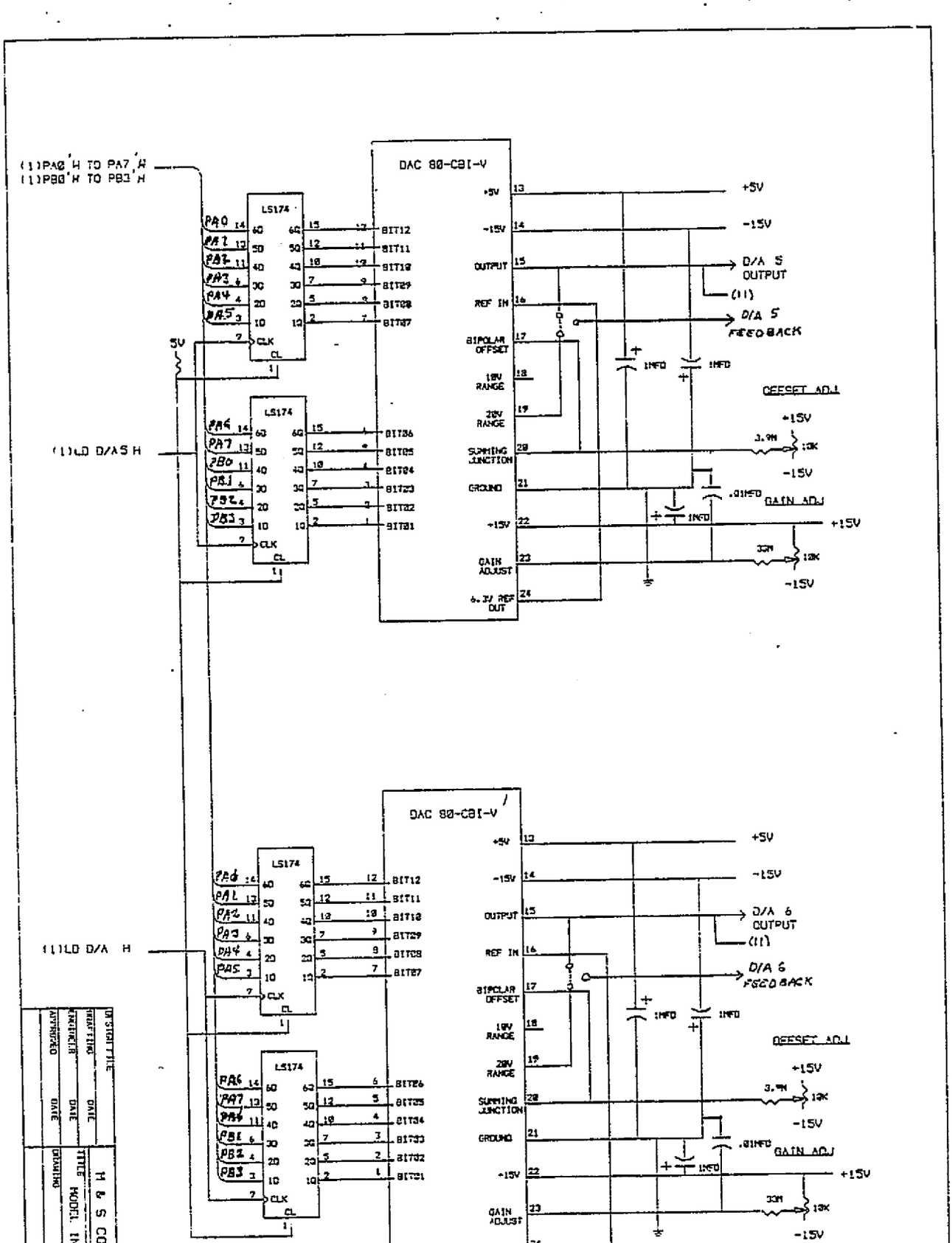


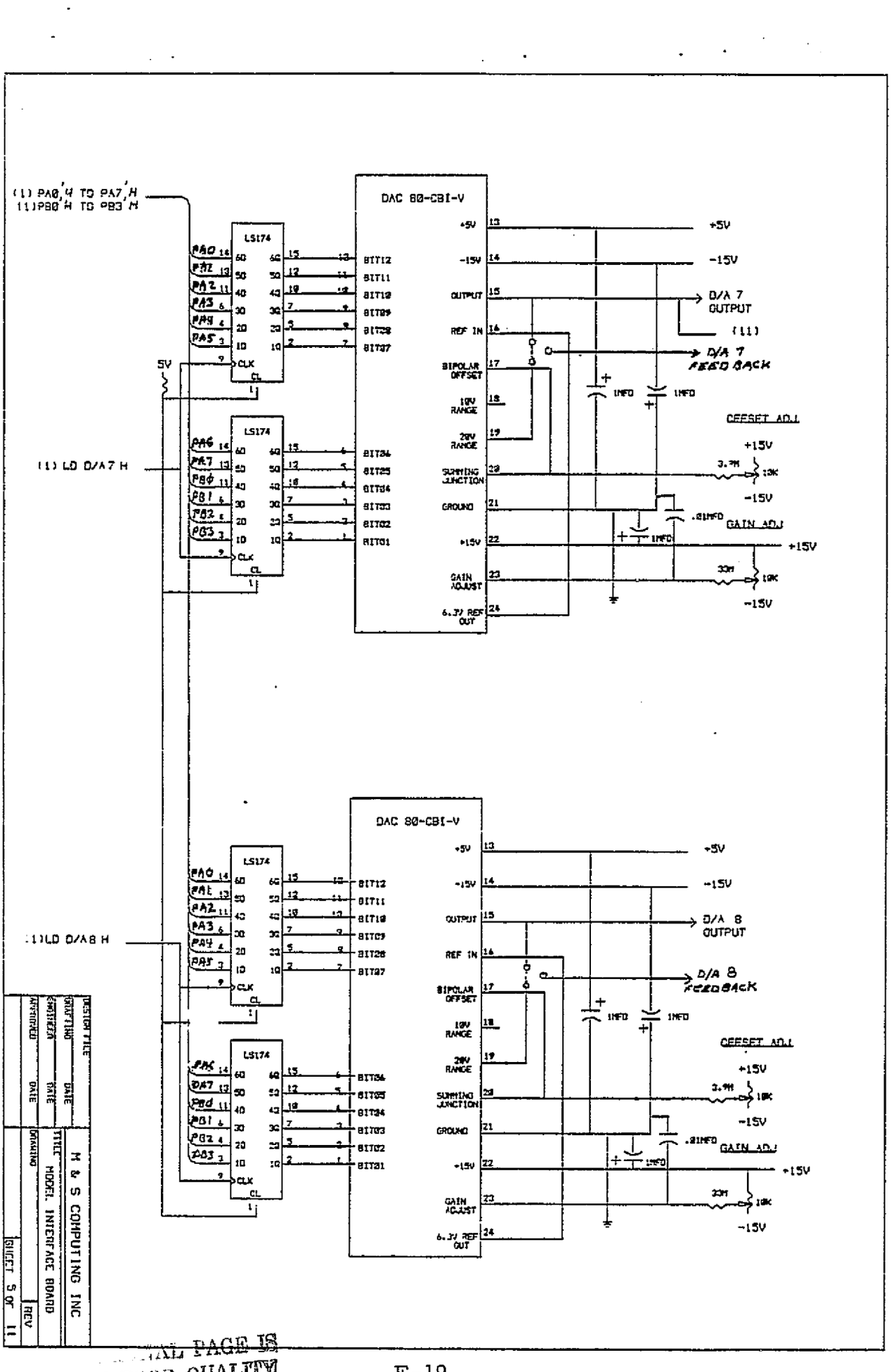

AUXILIARY BUS
(1) AB 0 H
(1) AB 1 H
(1) AB 2 H
(1) AB 3 H
(1) AB 4 H
(1) AB 5 H
(1) AB 6 H
(1) AB 7 H
(1) AB 8 H
(1) AB 9 H
(1) AB10 H
(1) AB11 H
(1) AB12 H
(1) AB13 H
(1) AB14 H
(1) AB15 H
(1) DB 0 L
(1) DB 1 L
(1) DB 2 L
(1) DB 3 L
(1) DB 4 L
(1) DB 5 L
(1) DB 6 L
(1) DB 7 L
(1) CBR/W H
(1) CBVMA H
(1) CBRESET L
(1) CPVMA L
(1) HALT L
(1) CBBA H
(1) IRQ L
(1) NMI L
(1) CP RESET L
(1) CBE H
(2) DEV ADR EN 1 L
(2) DEV ADR EN 2 L
(2) DEV ADR EN 3 L
(2) DEV ADR EN 4 L
(2) DEV ADR EN 5 L
(2) DEV ADR EN 6 L
(2) DEV ADR EN 7 L
(2) DEV ADR EN 8 L
(2)(5)(6)(7)
(2)(6)(7)
(2)
(6)
(5)
GND
J1-1
J1-2
J1-3
J1-4
J1-5
J1-6
J1-7
J1-8
J1-9
J1-10
J1-11
J1-12
J1-13
J1-14
J1-15
J1-16
J1-17
J1-18
J1-19
J1-20
J1-21
J1-22
J1-23
J1-24
J1-25
J1-26
J1-27
J1-28
J1-29
J1-30
J1-31
J1-32
J1-33
J1-34
J1-35
J1-36
J1-37
J1-38
J1-39
J1-40
DESIGN FILE
DRAFTING
DATE
ENGINEER
DATE
APPROVED
DATE
M & S COMPUTING INC
TITLE
MICROPROCESSOR BOARD
DRAWING
REV
SHEET 8 OF 8

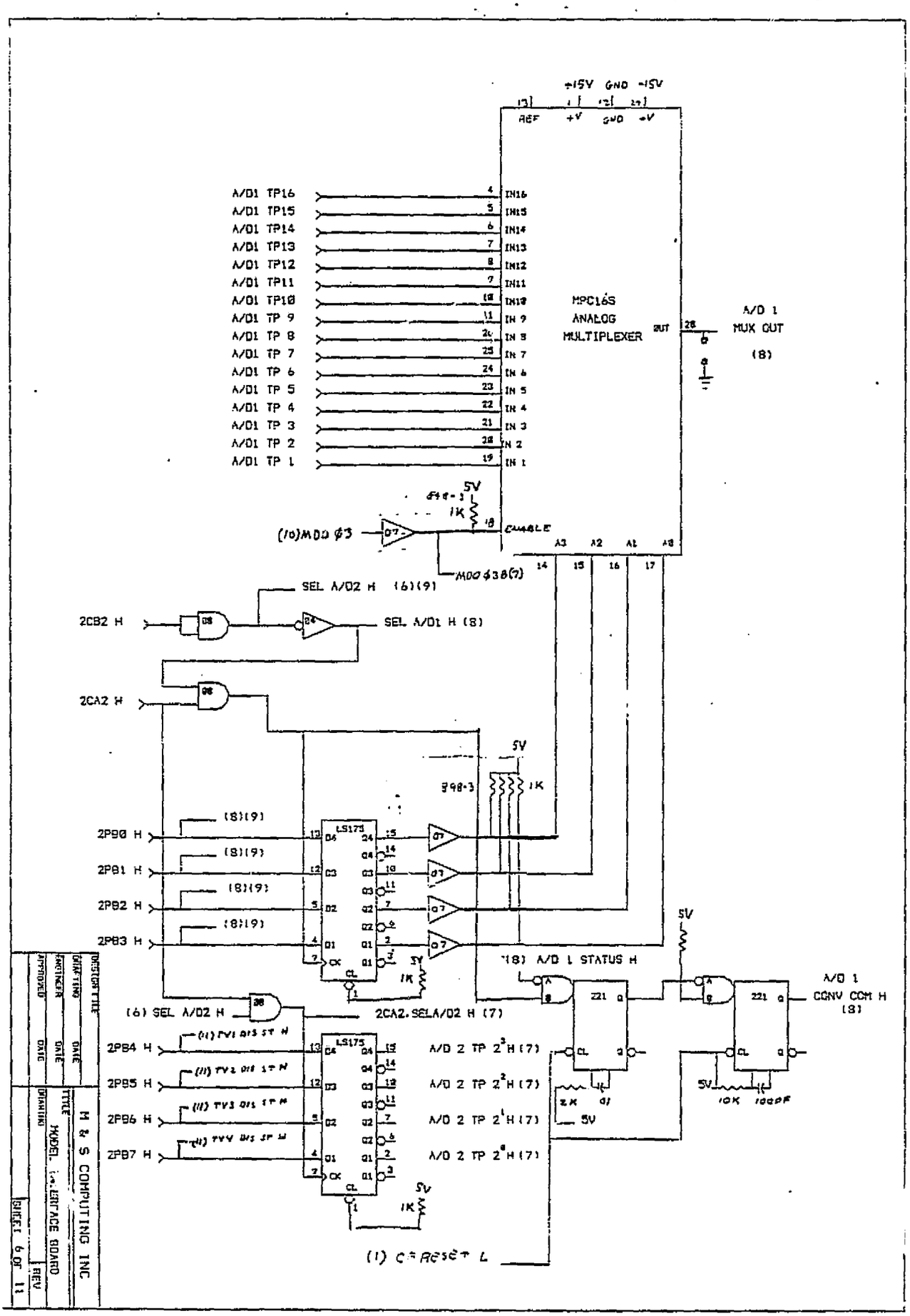

CBRESET L
CBRESET L (1)(10)(6)(7)
1PA0'H - 1PA7'H (2)(3)(4)(5)(10)
1PB0'H - 1PB7'H (2)(3)(4)(5)(10)
1PA0 H
1PA1 H
1PA2 H
1PA3 H
1PA4 H
1PA5 H
1PA6 H
1PA7 H
1PB0 H
1PB1 H
1PB2 H
1PB3 H
1PB4 H
1PB5 H
1PB6 H
1PB7 H
1CB2 H
1PB6'H
1PB5'H
1PB4'H
5V
DIP-3
1K
S138
G2B
G2A
G1
C
B
A
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
LD D/A 8 H (5)
LD D/A 7 H (5)
LD D/A 6 H (4)
LD D/A 5 H (4)
LD D/A 4 H (3)
LD D/A 3 H (3)
LD D/A 2 H (2)
LD D/A 1 H (2)
.01 TYP
+5V
15UF
+15V
-15V
GND
221
CL
(1) CBRESET L
5V
10K
100PF
DESIGN TITLE
DRAFTING DATE
ENGINEER DATE
APPROVED DATE
M & S COMPUTING INC
TITLE MODEL INTERFACE
DRAWING
REV
SHEET 1 OF 11

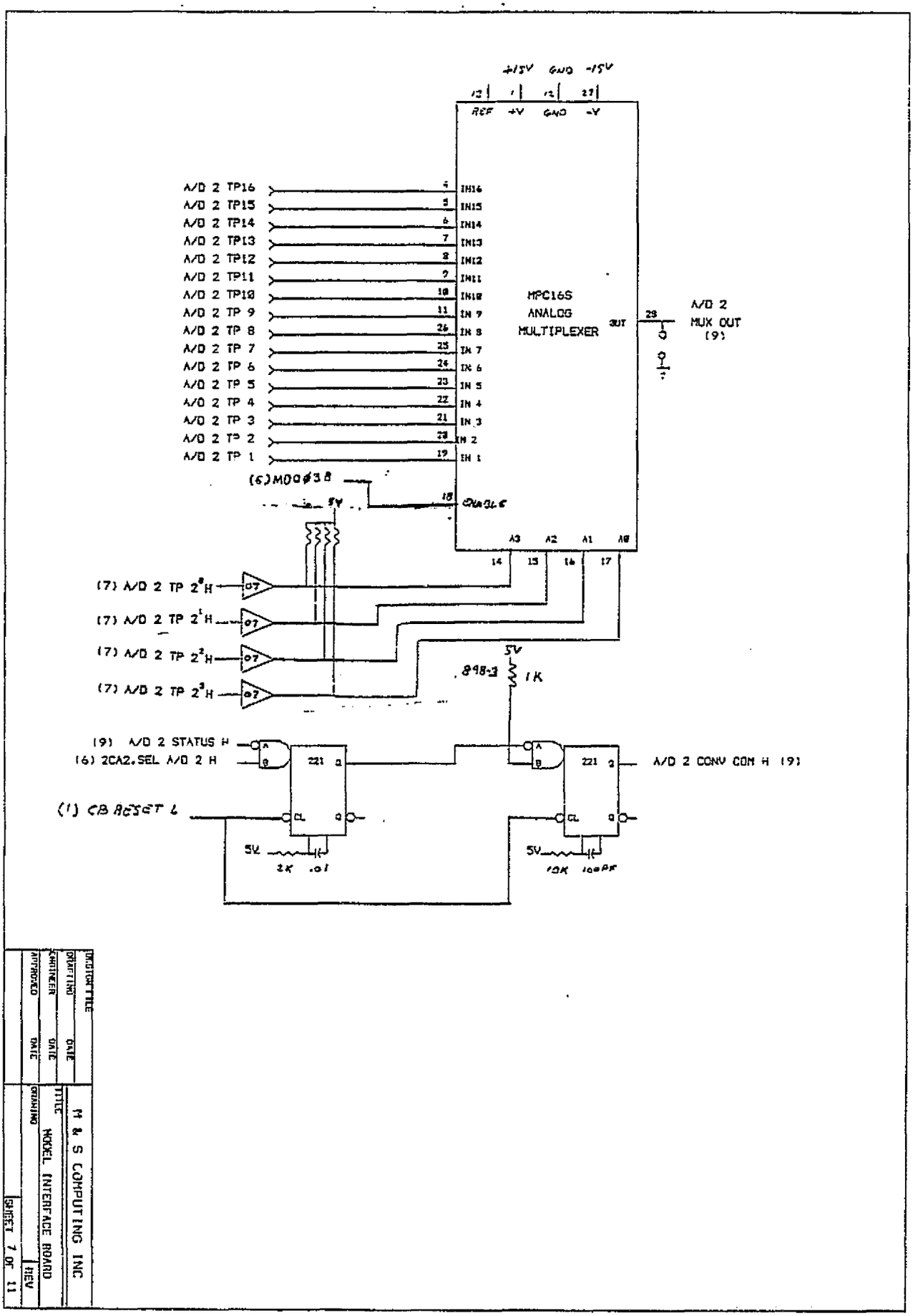

(1)PA0 H TO PA7 H
(1)PB0 H TO PB3 H
LD D/A 1H
LD D/A 2 H
5V
LS174
DAC 80-CBI-V
BIT12
BIT11
BIT10
BIT09
BIT08
BIT07
BIT04
BIT05
BIT04
BIT03
BIT02
BIT01
+5V
-15V
OUTPUT
REF IN
BIPOLAR OFFSET
10V RANGE
20V RANGE
SUMMING JUNCTION
GROUND
+15V
GAIN ADJUST
6.3V REF OUT
D/A 1 OUTPUT (11)
D/A 1 FEEDBACK
D/A 2 OUTPUT (11)
D/A 2 FEEDBACK
OFFSET ADJ
GAIN ADJ
1MFD
.01MFD
3.9M
10K
20M
CLK
M & S COMPUTING INC
MODEL INTERFACE BOARD
SHEET 2 OF 11

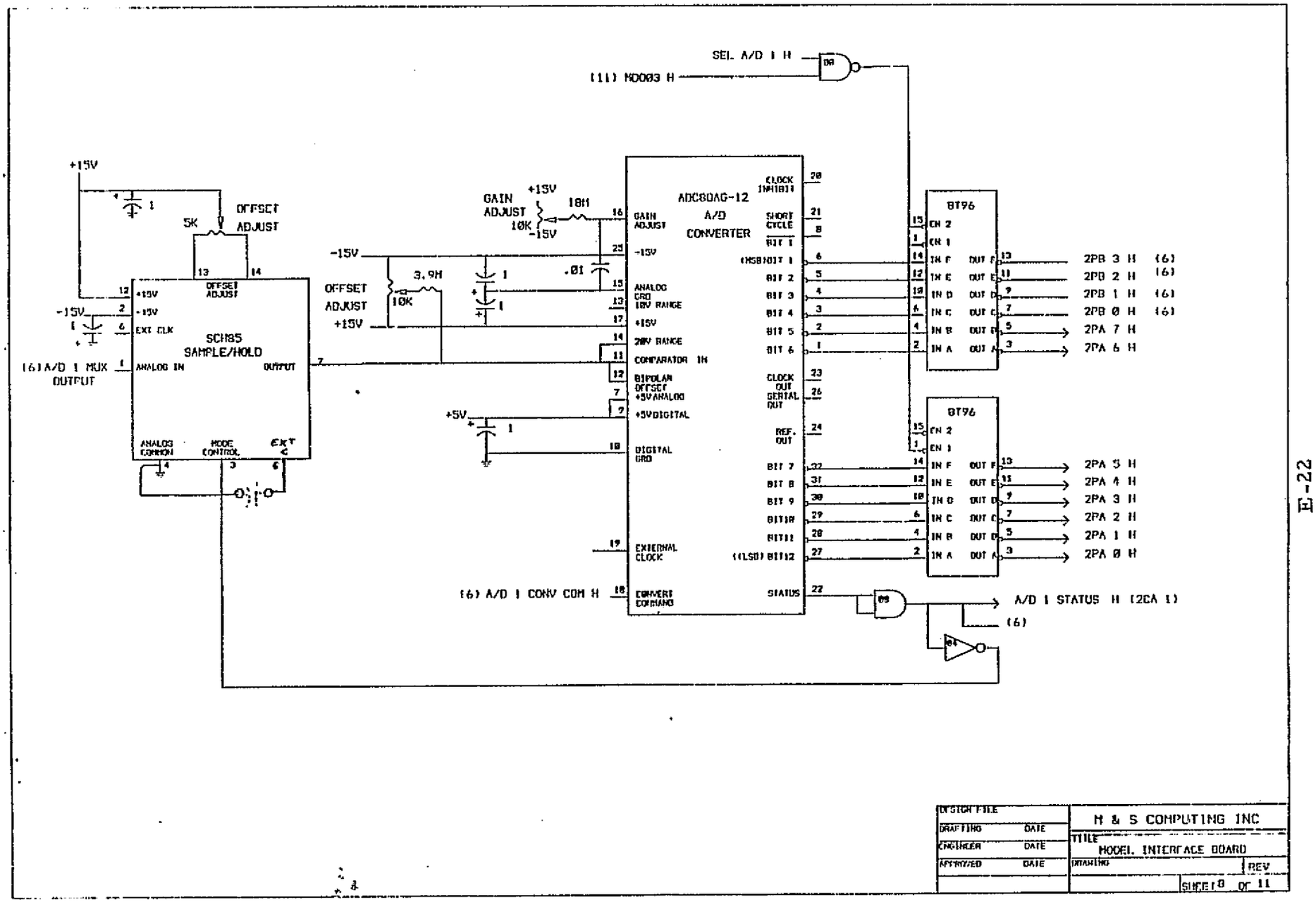



(11)PA0 H TO PA7 H
(11)PB0 H TO PB3 H
(11)LD D/A S H
(11)LD D/A 6 H
LS174
CLK
CL
BIT12
BIT11
BIT10
BIT09
BIT08
BIT07
BIT06
BIT05
BIT04
BIT03
BIT02
BIT01
DAC 80-CBI-V
+5V
-15V
OUTPUT
REF IN
BIPOLAR OFFSET
10V RANGE
20V RANGE
SUMMING JUNCTION
GROUND
GAIN ADJUST
6.3V REF OUT
D/A 5 OUTPUT
(11)
D/A 5 FEEDBACK
D/A 6 OUTPUT
D/A 6 FEEDBACK
.1MFD
OFFSET ADJ
GAIN ADJ
3.9M
10K
33M
H & S COMPUTING INC
TITLE MODEL INTERFACE BOARD
SHEET 4 OF 11
REV




+15V GND -15V
REF +V GND -V
A/D1 TP16
A/D1 TP15
A/D1 TP14
A/D1 TP13
A/D1 TP12
A/D1 TP11
A/D1 TP10
A/D1 TP 9
A/D1 TP 8
A/D1 TP 7
A/D1 TP 6
A/D1 TP 5
A/D1 TP 4
A/D1 TP 3
A/D1 TP 2
A/D1 TP 1
IN16
IN15
IN14
IN13
IN12
IN11
IN10
IN 9
IN 8
IN 7
IN 6
IN 5
IN 4
IN 3
IN 2
IN 1
MPC16S
ANALOG
MULTIPLEXER
OUT
A/D 1
MUX OUT
(8)
5V
1K
ENABLE
(10)MDD #3
MDD #38(7)
A3 A2 A1 A0
SEL A/D2 H (6)(9)
SEL A/D1 H (8)
2CB2 H
2CA2 H
(8)(9)
2PB0 H
2PB1 H
2PB2 H
2PB3 H
LS175
(6) SEL A/D2 H
2CA2.SELA/D2 H (7)
2PB4 H
2PB5 H
2PB6 H
2PB7 H
A/D 2 TP 2^3 H (7)
A/D 2 TP 2^2 H (7)
A/D 2 TP 2^1 H (7)
A/D 2 TP 2^0 H (7)
(8) A/D 1 STATUS H
221
2K
10K
100PF
A/D 1
CONV COM H
(8)
(1) C=RESET L
M & S COMPUTING INC
INTERFACE BOARD
SHEET 6 OF 11


+15V GND -15V
REF +V GND -V
MPC16S
ANALOG
MULTIPLEXER
A/D 2 TP16
A/D 2 TP15
A/D 2 TP14
A/D 2 TP13
A/D 2 TP12
A/D 2 TP11
A/D 2 TP10
A/D 2 TP 9
A/D 2 TP 8
A/D 2 TP 7
A/D 2 TP 6
A/D 2 TP 5
A/D 2 TP 4
A/D 2 TP 3
A/D 2 TP 2
A/D 2 TP 1
IN16
IN15
IN14
IN13
IN12
IN11
IN10
IN 9
IN 8
IN 7
IN 6
IN 5
IN 4
IN 3
IN 2
IN 1
OUT
A/D 2
MUX OUT
(9)
(6)M00838
GNDLE
A3 A2 A1 A0
(7) A/D 2 TP 2⁰H
(7) A/D 2 TP 2¹H
(7) A/D 2 TP 2²H
(7) A/D 2 TP 2³H
5V
898-3
1K
(9) A/D 2 STATUS H
(6) 2CA2.SEL A/D 2 H
221
A/D 2 CONV CON H (9)
(1) CB RESET L
CL
5V
2K .01
10K 10PF
M & S COMPUTING INC
DRAWING TITLE
MODEL INTERFACE BOARD
SHEET 7 OF 11
REV



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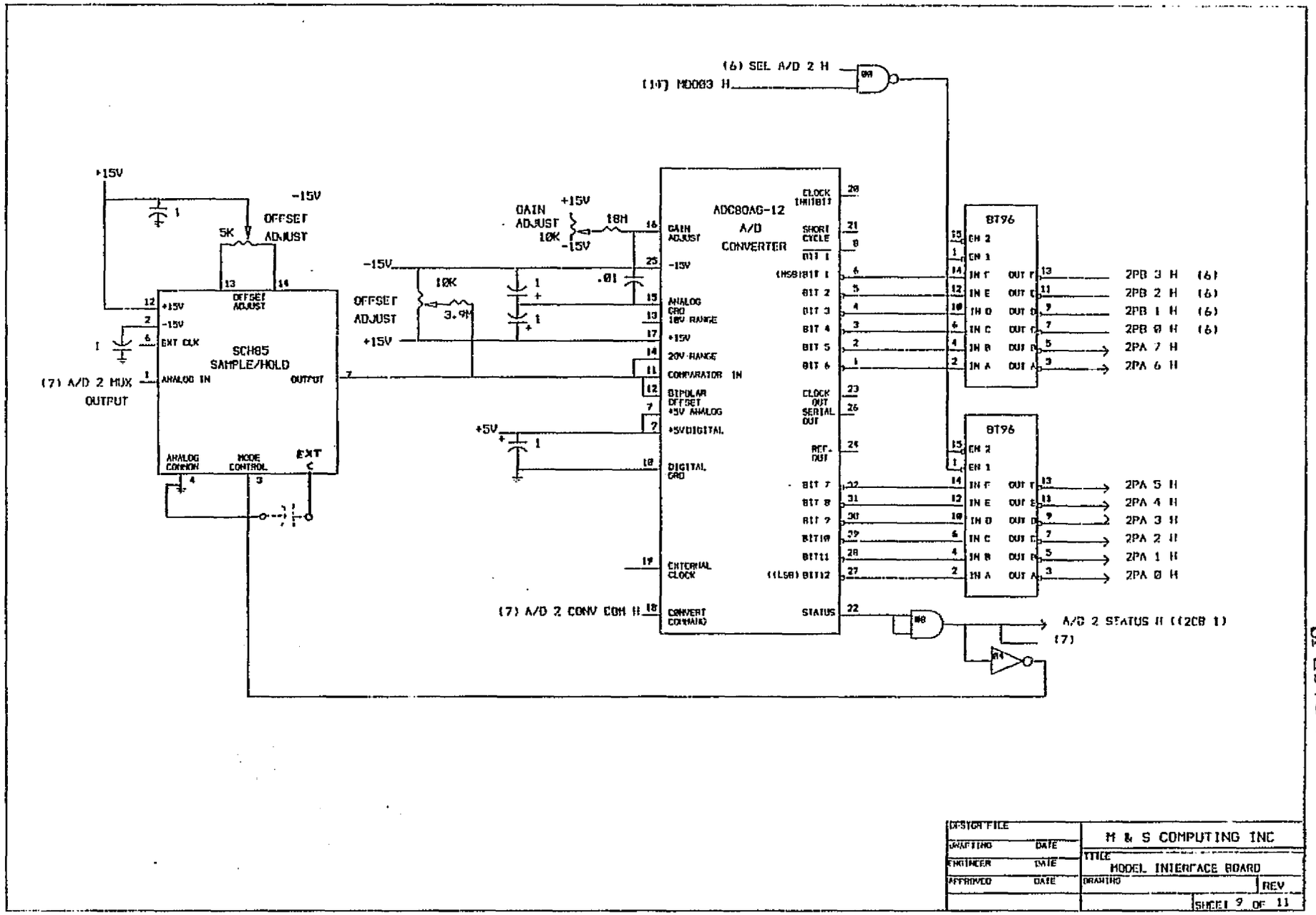
ENGINEER	DATE	DRAWING REV
APPROVED	DATE	SHEET 8 OF 11



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ENGINEER DATE	DRAWING REV
APPROVED DATE	SHEET 9 OF 11

E-23

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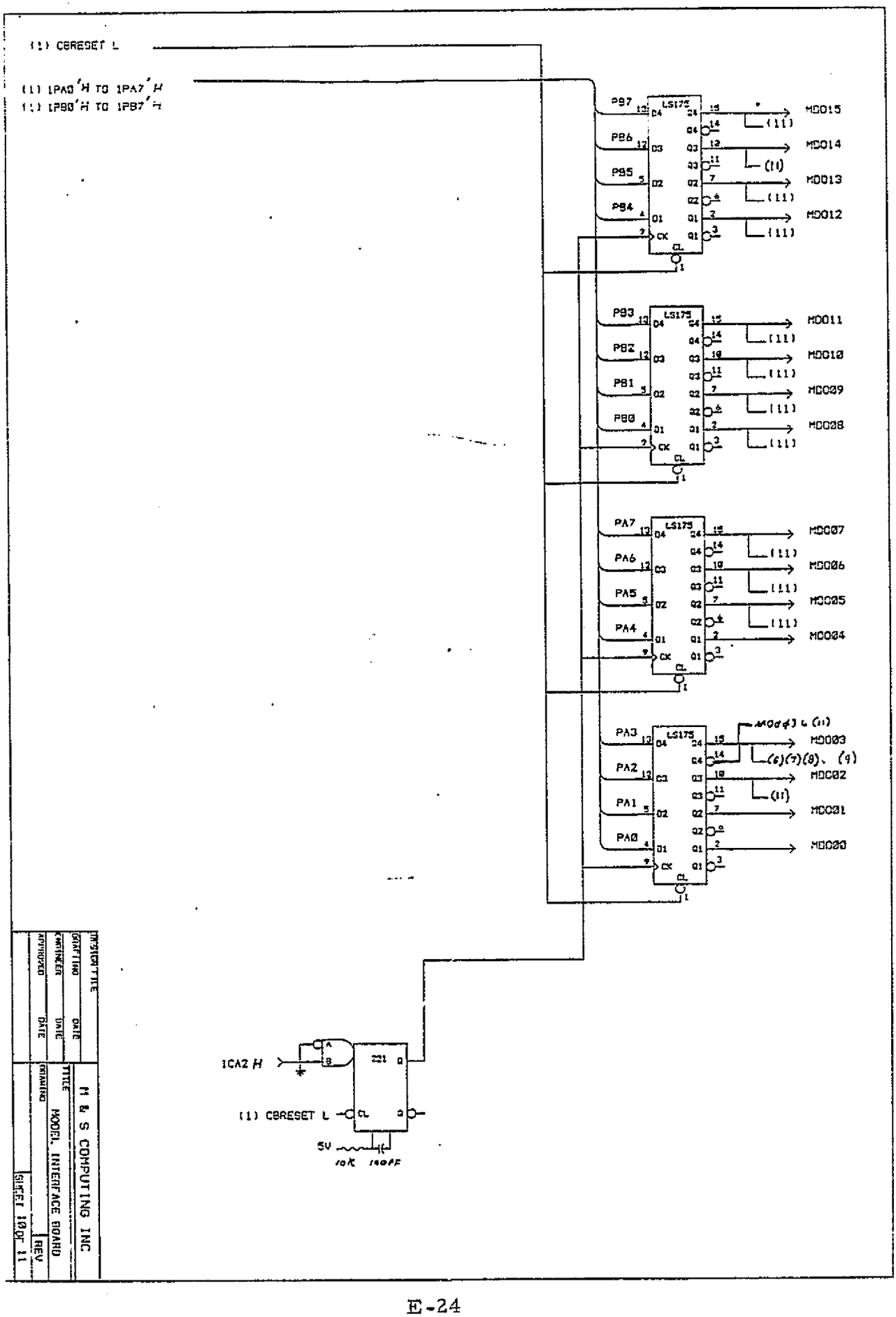
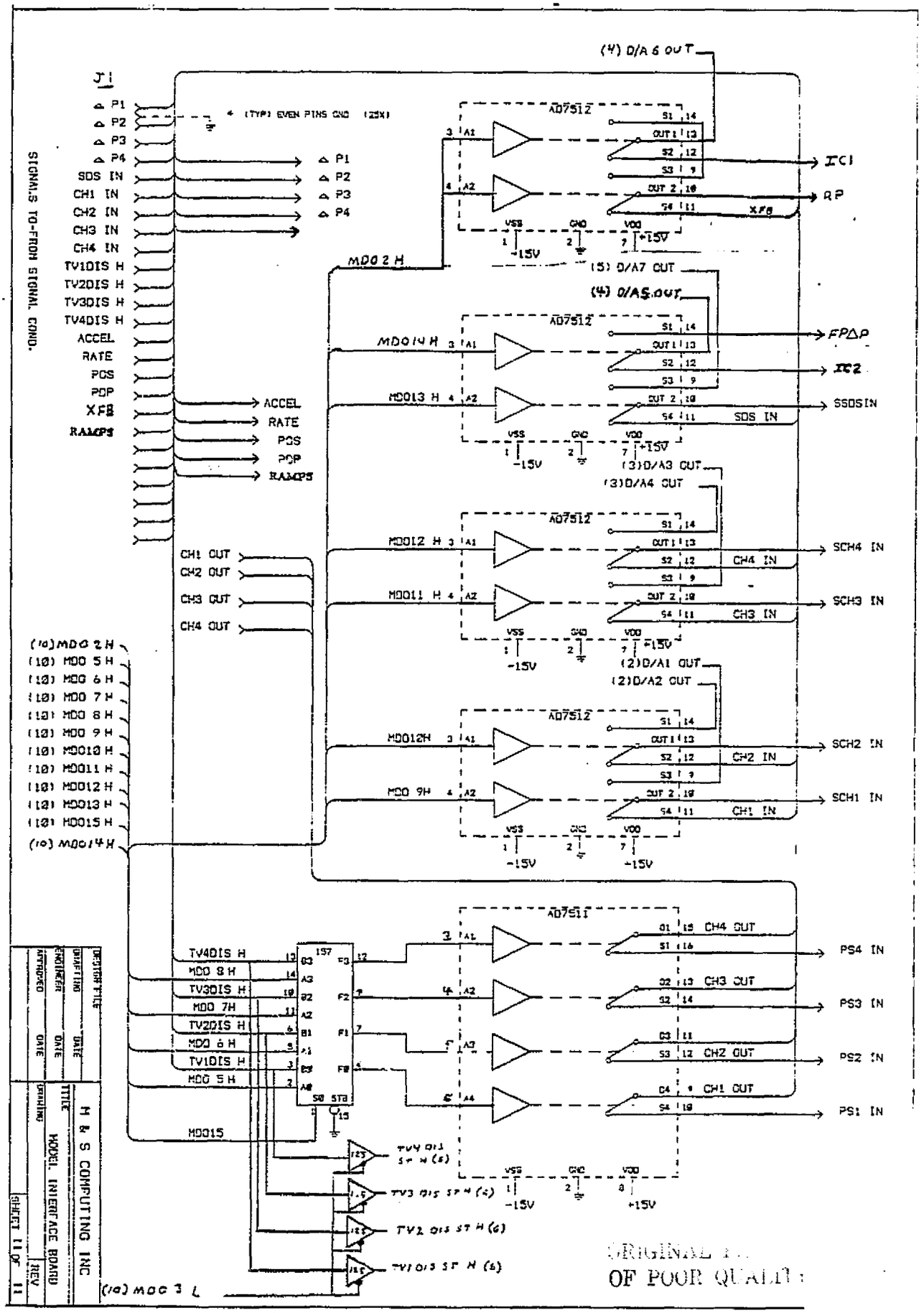

(1) CBRESET L
(1) IPA0 'H TO IPA7 'H
(1) IPB0 'H TO IPB7 'H
PB7
PB6
PB5
PB4
PB3
PB2
PB1
PB0
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
LS175
CK
CL
MD015
MD014
MD013
MD012
MD011
MD010
MD009
MD008
MD007
MD006
MD005
MD004
MD003
MD002
MD001
MD000
ICA2 H
(1) CBRESET L
5V
10K
100PF
M & S COMPUTING INC
MODEL INTERFACE BOARD



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