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AUTOMATED ARRAY ASSEMBLY TASK
PHASE I

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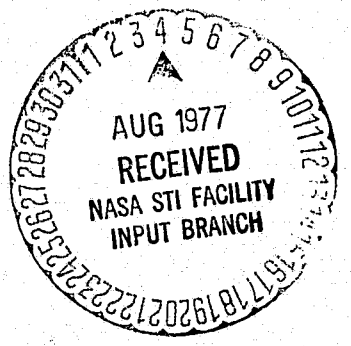
Annual Report

Bernard G. Carbajal

March 1977



JPL Contract No. 954405

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This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, under NASA Contract NAS7-100 for the U.S. Energy Research and Development Administration, Division of Solar Energy.

The JPL Low-Cost Silicon Solar Array Project is funded by ERDA and forms part of the ERDA Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays.

ABSTRACT

This contract, a subtask of Task 4 of the LSSA Project, consists of an assessment of state-of-the-art technologies that are applicable to silicon solar cell and solar cell module fabrication. The assessment consists of a technical feasibility evaluation and a cost projection for high-volume production of silicon solar cell modules.

The cost projection was approached from two directions, a design-to-cost analysis assigned cost goals to each major process element in the fabrication scheme and a cost analysis built up projected costs for alternate technologies for each process element. A technical evaluation was used in combination with the cost analysis to identify a baseline low-cost process. Since some of the technologies called for in the baseline process are still in a feasibility stage for solar cell fabrication, two alternates to the baseline process were also identified.

A novel approach to metal pattern design based on minimum power loss was developed. These design equations were used as a tool in the evaluation of metallization technologies. The quantitative nature of the design equations provided a solid technical basis for the choice of a metallization technology.

A hermetic module was proposed that has a high probability of meeting the 20-year life goal. Solar cell processing and module fabrication cost projections exceed the 1985 cost goal by only a factor of ≈ 3.

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SECTION I
INTRODUCTION

This is the 1976 Annual Report under JPL contract number 954405, a subtask of Task 4 of the Low-Cost Silicon Solar-Cell Array (LSSA) Project. The goal of this study is an assessment of existing process technologies and encapsulation technologies as applied to solar cell module manufacture. From this assessment, low-cost solar cell processes and module configurations shall be proposed.

During this investigation several quantitative and semiquantitative evaluation methods were developed. These evaluation methods were used as tools in the evaluation and choice of process step technologies. The metal pattern design equations developed to minimize power loss in the cell were particularly useful in the evaluation of various options available for front surface metallization.

A large number of solar cell process step alternatives were evaluated from a technical acceptability viewpoint and detailed costing was calculated on technically promising steps assuming a reasonable degree of automation. Using technical and cost criteria, a baseline low-cost solar cell process was proposed. The assessment assumes only evolutionary changes in process technology and does not depend on any technical breakthroughs.

A similar approach to module fabrication led to a technically weighted choice of a higher cost module. The choice was made on the basis of a high probability of meeting the 20-year life goal.

Comparison of projected process and module costs against design-to-cost goals, based on a 1985 price of $0.50 per watt, shows that a cost gap still exists. The gap has been reduced from a factor of 30-50 based on the existing terrestrial solar cell market to a factor of ≈ 3. Improvements in module efficiency coupled with selected cost improvements should allow this gap to be closed.

SECTION II
TECHNICAL DISCUSSION

A. DESIGN-TO-COST CONCEPT

One of the key uses of the design-to-cost concept is to allocate portions of the total cost to the various process elements so that each process element can be tested against its individual cost goal. In this fashion, key cost barriers can be identified for individual consideration. This evaluation then points the way to the required technical innovation for cost reduction.

The allocation of the total cost to the individual process elements is not an exact science and must be weighted by known factors and engineering judgment. The cost allocations for solar cell module fabrication used in this analysis were arrived at in this fashion. Since solar cell manufacture is a material intensive process, up to 50% of the total cost is allocated to silicon sheet fabrication. Junction formation, metallization, and antireflection (AR) coating are each allocated 10% of the total cost. Module substrate, assembly, and encapsulation are allocated 20% of the total cost. Testing costs must be included with the process element where testing is used and does not represent a separate cost element in this analysis.

The cost goal of the LSSA project is $500/kW peak power in 1985. An intermediate goal of $2000/kW peak power can be assigned to the 1980-81 time period.

Manufacturing costs for solar cell modules are a function of the number of units and the area of modules processed and can be related to a cost per watt as shown in equation (1):

$$\text{cost/meter}^2 = (\text{cost/watt})\,(\text{solar flux})\,(\text{conversion efficiency}) \qquad (1)$$

where conversion efficiency = η_M = conversion efficiency of the module. The cost/watt is the project goal of $500/watt and the solar flux at the earth's surface is taken as 1.00 kW/m^2. Figure 1 is a plot of cost/meters^2 versus conversion efficiency. The left ordinate is scaled to a cost/watt goal of $500/watt and the right ordinate is scaled to the intermediate cost/watt goal of $2000/watt.

The allowed cost/meters^2 can be easily read for any given module efficiency, e.g., at $\eta_M = 0.10$ cost/meter^2 = $50 in 1985. Using the above allocated percentages of the total cost, the data in Table 1 is obtained.

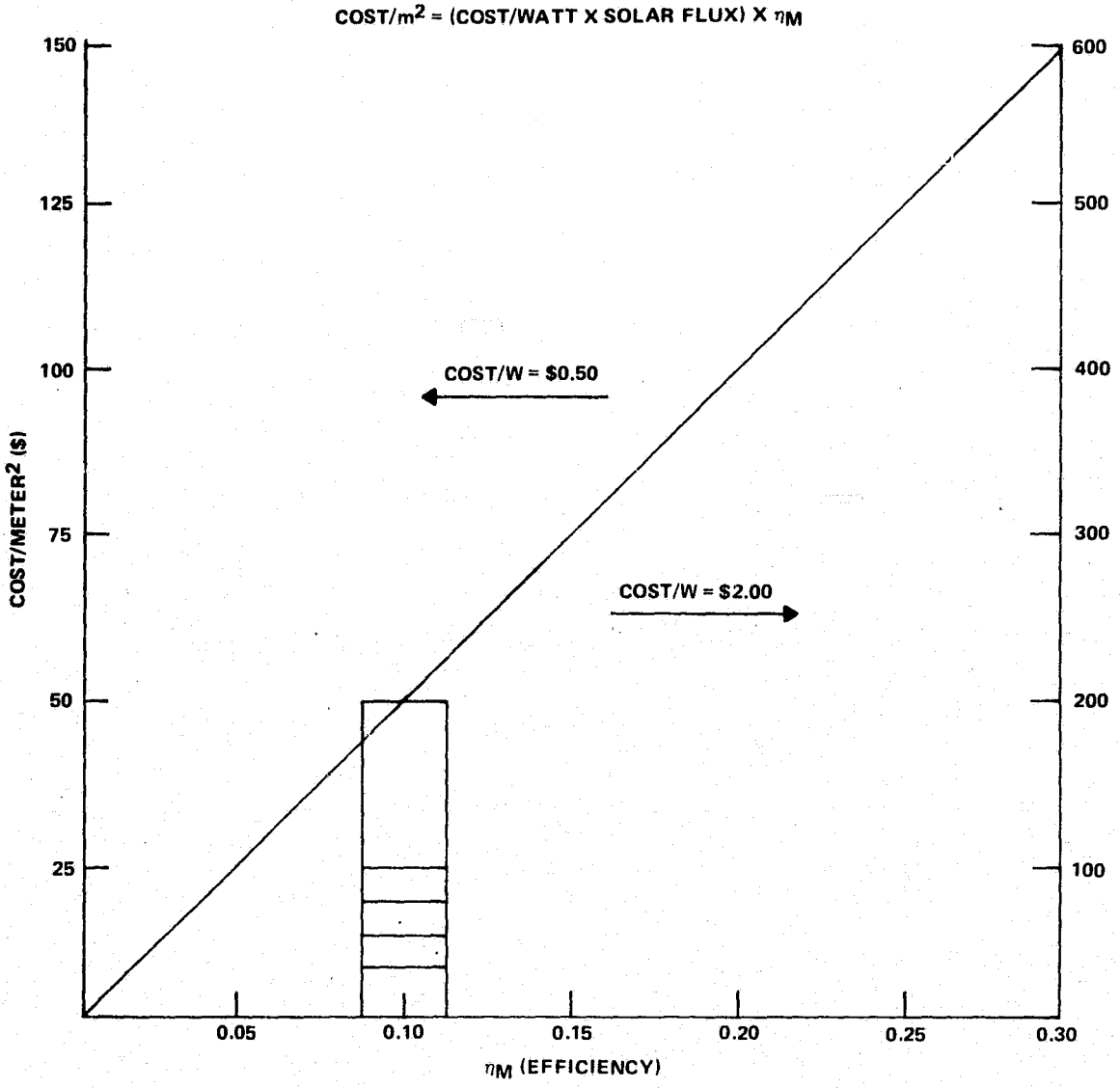


Figure 1. Cost/Unit Area versus Module Efficiency

Table 1. Design-To-Cost Allocation
Cost/Meter^2 (Module)

Si sheet		$25
Junction formation		$ 5
Metallization		$ 5
AR coating		$ 5
Module assembly and encapsulation		$10
	Total	$50

The cost of the solar cell manufacture is related to module cost allocation by using the board utilization factor shown graphically in Figure 2. Using a utilization factor of 0.85 for circles or hexagons, the process element costs for cell manufacture given in Table 2 are obtained. The process element costs are for solar cells with a cell efficiency (η) of 11.8% obtained by dividing the module efficiency by the board utilization as in equation (2):

$$\eta = \frac{\eta_M}{B.U.} \tag{2}$$

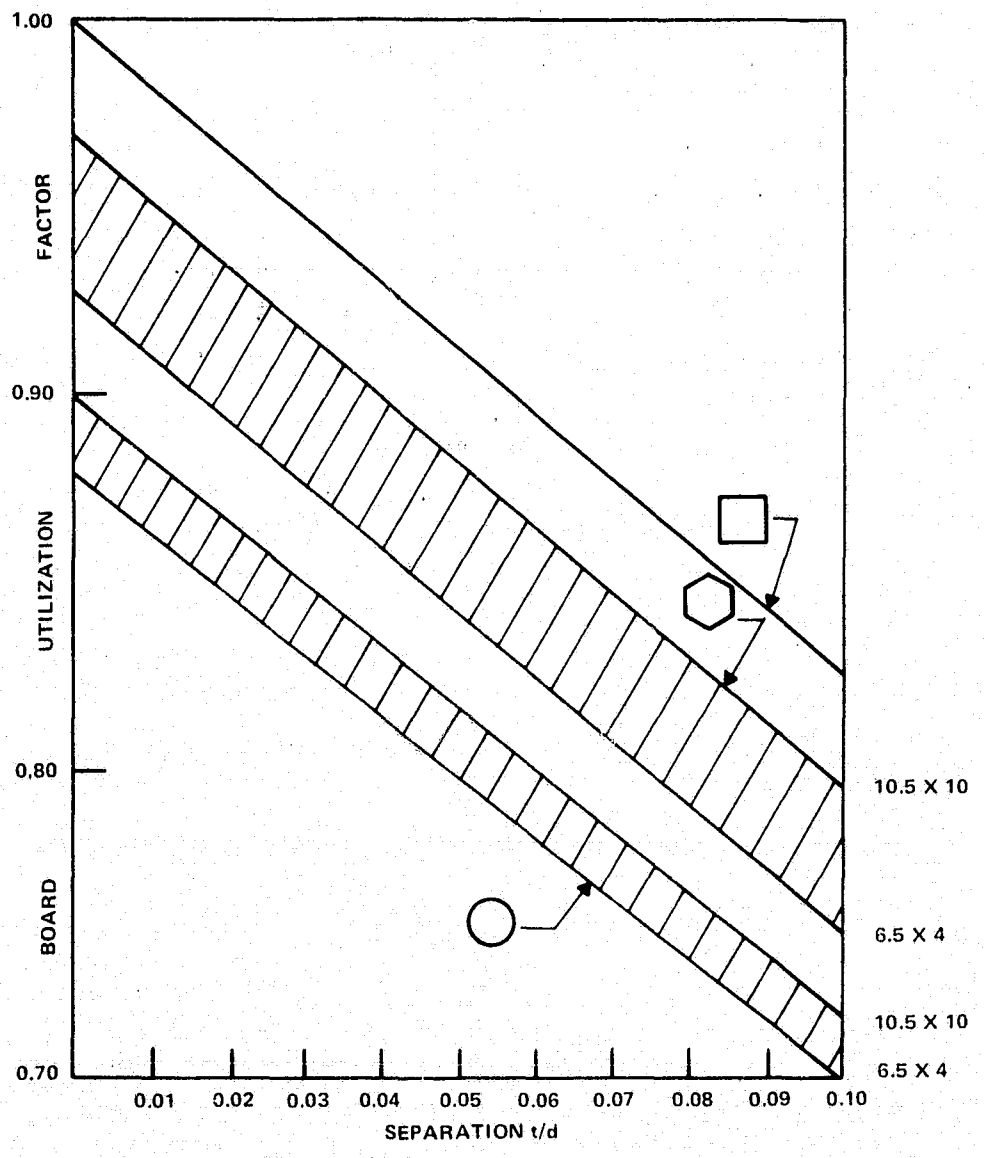


Figure 2. Board Utilization as a Function of Cell Separation

Table 2. Design-To-Cost Goals for Solar Cell Manufacture Cost/Meter^2 (Cell)

Si sheet	$29.41
Junction formation	5.88
Metallization	5.88
AR coating	5.88
Total	$47.05

Solar cell efficiencies greater than 11.8% would allow corresponding larger cost/meter allocations than those shown in Tables 1 and 2. Single crystal silicon solar cell efficiencies of 15% to 18% in the early 1980s appear to be a reasonable extrapolation from existing technology. Using board utilization of 0.85, this gives an allowable module manufacturing cost per square meter of $64 to $76 to meet the 1985 cost goal of $500/watt peak power.

This analysis can now be used to assess the compatibility of various approaches for each of the module fabrication process elements to the overall cost goal and initial technical confidence (or risk) factors can be assigned. For example, the Si sheet cost goal of $29.41/m^2 for a 10% efficient module compares favorably with the $30/m^2 projection for a semicontinuous Czochralski process.[1] A cell efficiency of 11.8% should be readily achieved leading to a high confidence factor (0.9) that this Si sheet process is compatible with the overall module goal. Other Si sheet processes that had comparable cost projections but lower confidence factors would be higher risk options.

This analysis can also be used to define some limiting criteria (keeping in mind the assumptions included in the analysis). Each process element has a lower limiting value that is finite at any point in time. If it is assumed that the allocated costs for junction formation, metallization, AR coating, and module assembly and encapsulation shown in Table 1 are at the limiting value for 1985, then the cost of the Si sheet is the only cost that varies with module efficiency. Inspection of Figure 1 shows that at $\eta_M = 0.05$, the allowed cost allocation for Si sheet is zero. Therefore, Si sheet processes that inherently yield modules of less than 5% efficiency are unacceptable, and for module efficiencies greater than 5%, a cost allowance derived from Figure 1 must be met, e.g., at $\eta_M = 0.08$, the allowed cost for Si sheet = $15/m^2 (module) or with a board utilization of 0.85, allowed cost for Si sheet = $17.65/m^2(cell).

Another trend that can be derived from this analysis is that cost per area is a function of module efficiency, therefore higher conversion efficiency processes allow higher cost processing. For example, a solar cell fabrication process that yields a value for $\eta = 0.18$ at a board utilization of 0.85 gives $\eta_M = 0.18 \times 0.85 = 0.153$, this gives an allowable module fabrication cost of $76.50.

In summary, the analysis of module efficiency (η_M), cell efficiency (η), board utilization, cost per watt and allowable cost per unit area allow one to test each of the module fabrication process elements, prioritize various options for each process element, and evaluate overall module fabrication processes. As more data and projections become available, optimum processes can be identified.

B. LABOR AND CAPITAL COST MODELING

Direct labor and capital cost for any operation can be calculated from the following parameters:

Operator Hours/Year = OHPY = (work hours/day) (work days/week) (work weeks/year)

Annual Throughput/Machine = ATPM = (machine throughput/hour) (work hours/day) (work days/week) X (work weeks/year) (utilization factor)

$$\text{Annual Capital Recovery} = \text{ACR} = (\text{capital cost})(\text{interest rate}) \times \left[1 + \frac{1}{(1+R)^N - 1} \right]$$

where

R = interest rate

N = number of years

$$\text{Capital Recovery Factor} = \text{CRF} = (\text{interest rate}) \left[1 + \frac{1}{(1+R)^N - 1} \right]$$

Solar cells will be manufactured in units that will then be assembled into modules. The labor cost per unit (cell, for direct labor, is given in equation (3).

$$\text{Labor Cost/Unit} = \text{LCPU} = \frac{\text{OHPY}}{\text{ATPM}} \times (\text{operator pay/hour}) \times \text{OPM} \qquad (3)$$

where

OPM = (number of operators/machine)

Labor cost per unit is independent of the number of hours worked per year.

Depreciation cost per unit is given in equation (4).

$$\text{Depreciation Cost/Unit} = \text{DCPU} = \frac{\text{ACR}}{\text{ATPM}} \tag{4}$$

Combining equations (3) and (4), an allowable capital cost as a function of DCPU and LCPU [equation (5)] can be derived:

$$\text{Capital Cost} = \text{CC} = \frac{\text{DCPU}}{\text{LCPU}} \text{ X } \frac{\text{OHPY X OPPH}}{\text{CRF}} \text{ X OPM} \tag{5}$$

where OPPH = operator pay/ hour.

CRF, OHPY, and operator pay/hour are definable terms that can be evaluated as follows:

CRF (7 yr life, 9% interest) = 0.1987/year

OHPY = (24 hour/day) (7 day/week) (50 week/year)

= 8400 hour/year

Operator pay/hour = $3.50/hour

Then:

$$\text{Capital Cost} = 147962 \text{ X } \frac{\text{DCPU}}{\text{LCPU}} \text{ X OPM}$$

or

$$\text{Capital Cost/OPM} = 147962 \text{ X } \frac{\text{DCPU}}{\text{LCPU}} \tag{6}$$

Using these relationships and the design-to-cost goals in Table 2, a set of boundary conditions for a solar cell factory that meets the $500/kW peak power goal can be described.

OPM can be defined as the equipment run by one operator, i.e., OPM = 1, and one square meter of solar cells, independent of the shape or size of the individual cells, is a unit and the utilization factor is 0.80 (allowing 20% of the time for equipment down time, R&M, etc.) (Table 3).

The cost associated with processing one unit is the sum of material, labor, overhead, and depreciation in equation (7).

$$\text{CPU} = \text{MPU} + \text{LCPU} + \text{OH} + \text{DCPU} \tag{7}$$

where

CPU = cost per unit

MPU = material consumed per unit

OH = overhead associated with LCPU

If OH = LCPU, where 50% of the OH is labor associated and 50% is allocated to cover supervisory wages, management costs, building cleaning and maintenance, then equation (7) reduces to:

$$CPU = MPU + LCPU + LCPU + DCPU$$

$$= MPU + 2\ LCPU + DCPU$$

Using the design-to-cost goals in Table 2 and assigning a value of 25% of CPU to MPU, total allowable labor and depreciation costs to a process element in solar cell manufacture, such as metallization, can be defined.

$$\$5.88 = 0.25\ (\$5.88) + 2\ LCPU + DCPU$$

$$\$4.41 = 2\ LCPU + DCPU$$

Substituting this into equation (6)

$$\text{Capital Cost} = \frac{147962 \times 4.41}{LCPU} - 295924 \qquad (8)$$

Table 3. ATPM and LCPU as a Function of Machine Throughput/Hour

Machine Throughput/Hour m^2/hour	ATPM m^2/year	LCPU \$/m^2
1.00	6,720	4.375
2.00	13,440	2.188
3.00	20,160	1.458
4.00	26,880	1.094
5.00	33,660	0.875
6.00	40,320	0.729
7.00	47,040	0.625
8.00	53,760	0.547
9.00	60,480	0.486
10.00	67,200	0.4375

or

$$\text{Capital Cost} = \frac{147962 \text{ X } 2 \text{ X DCPU}}{4.41 - \text{DCPU}} \tag{9}$$

or

$$\text{Capital Cost} = \frac{147962 \text{ X } 4.41}{4.375} \text{ MTPH} - 295924 \tag{10}$$

These equations are plotted in Figures 3, 4, and 5. One interesting observation that is shown in Figure 5 is that for a given set of assumptions, there is a threshold throughput rate below which no capital expenditure will meet the cost goal. Above this threshold, the allowed capital cost is a linear function of the machine throughput rate. For the set of assumptions used in this analysis, the threshold limit for machine throughput is 2 square meters per hour.

The allowed DCPU as a function of MTPH can also be derived from equation (4). This relationship is given in equation (11).

$$\text{DCPU} = \frac{\text{ACR}}{\text{MTPH (work hours/day) (work days/week) (work weeks/year) (utilization factor)}} \tag{11}$$

$$= \frac{\text{ACR}}{\text{MTPH X } 6720}$$

for 7-year depreciation and 9% interest rate ACR = 0.19869 X Capital Cost

$$\text{DCPU} = \frac{\text{Capital Cost}}{\text{MTPH}} \text{ X } \frac{0.19869}{6720}$$

and substituting equation (10):

$$\text{DCPU} = \frac{149145.69 \text{ MTPH} \quad 295924}{\text{MTPH}} \text{ X } \left(\frac{0.19869}{6720}\right)$$

$$= 4.4098 - \frac{8.7496}{\text{MTPH}}$$

DCPU versus MTPH is plotted in Figure 6.

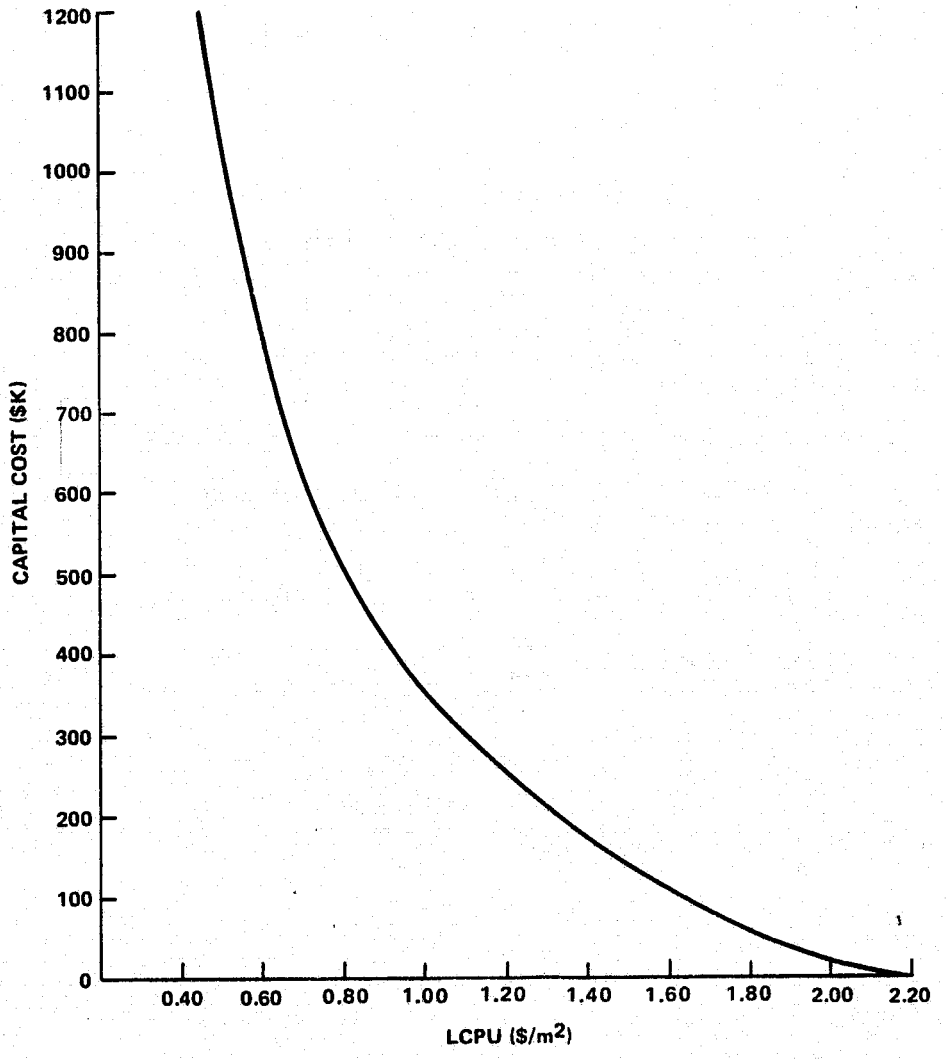


Figure 3. Capital Cost versus LCPU

Similarly, the allowed LCPU can be expressed as a function of MTPH, equation (12) and given in Table 3.

$$\text{LCPU} = \frac{\text{OPPH X OPM}}{\text{MTPH X Utilization Factor}} \qquad (12)$$

$$= \frac{4.375}{\text{MTPH}}$$

Equation (12) is plotted in Figure 7.

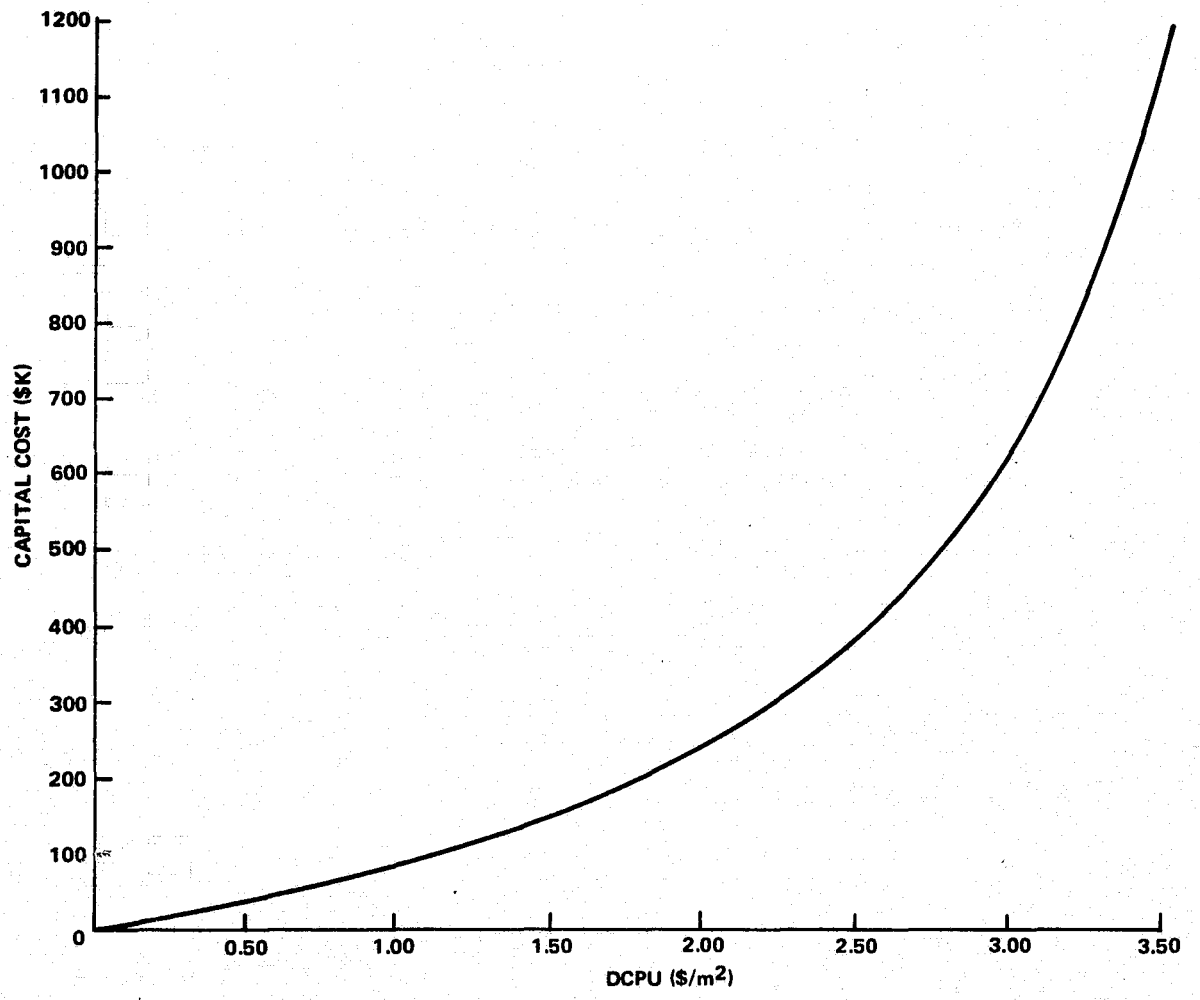


Figure 4. Capital Cost versus DCPU

The key parameter in this analysis is MTPH. For the values used in this design-to-cost simulation, a MTPH threshold of 2 m^2 per hour exists before any capital or depreciation cost can be tolerated. This leads to a description of a model metallization system that will meet the program goals. Table 4 describes this model system.

Any of the parameters in a design-to-cost model can be varied according to engineering judgment within the constraint of the total cost. The most impactive change would be to improve the module efficiency and thereby generate more available cost dollars per square meter.

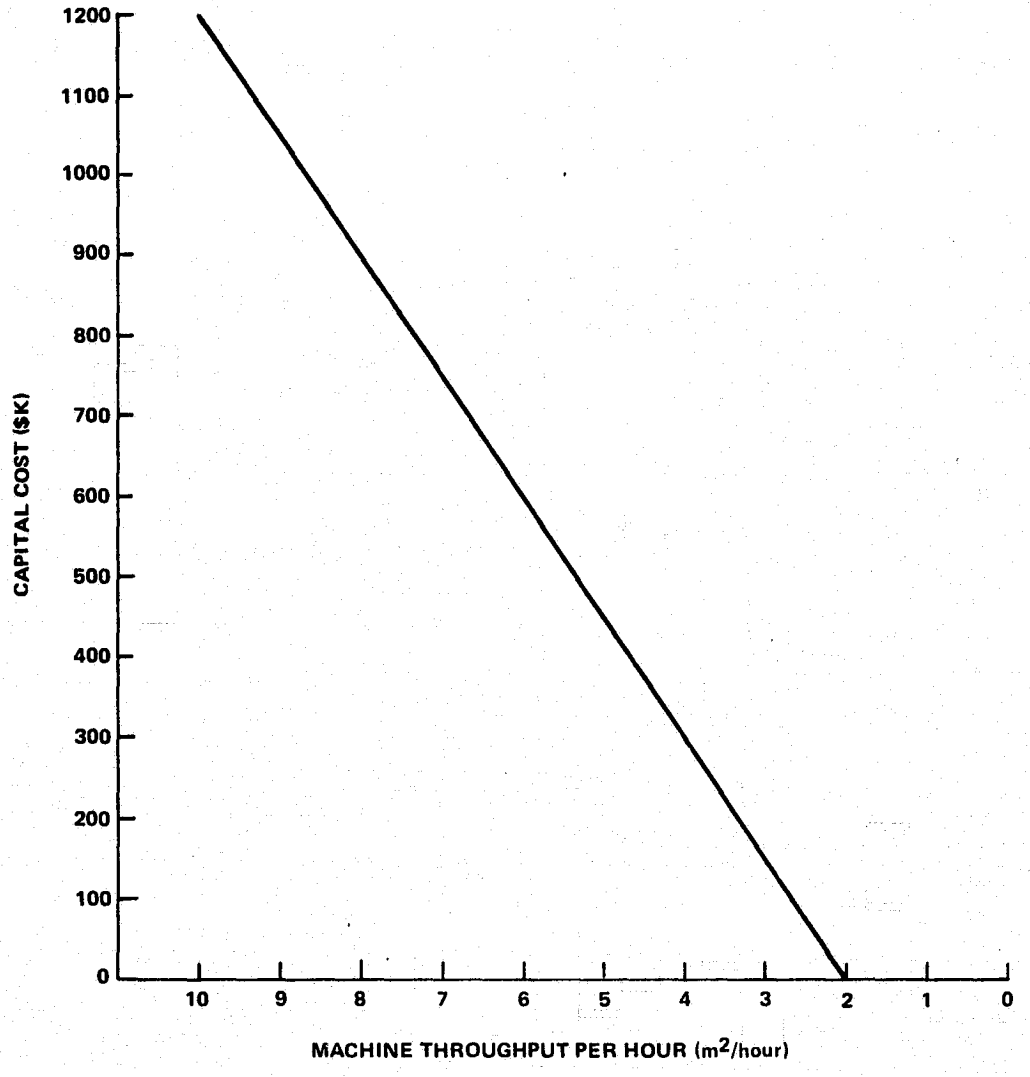


Figure 5. Capital Cost versus Machine Throughput

For purposes of comparison, one can relate square meters of cell to 10.16-cm (4.00 inch) diameter round cells. The area of a 10.16 cm diameter round cell is 81.07 cm^2. This corresponds to 123.4 cells/m^2. Therefore the threshold value of 2 m^2/hour is equivalent to a throughput of 246.7 round cells (10.16-cm diameter) per hour. Table 5 gives the CC, LCPU and DCPU for a metallization module as a function of slice (10.16-cm diameter round cells) throughput per hour.

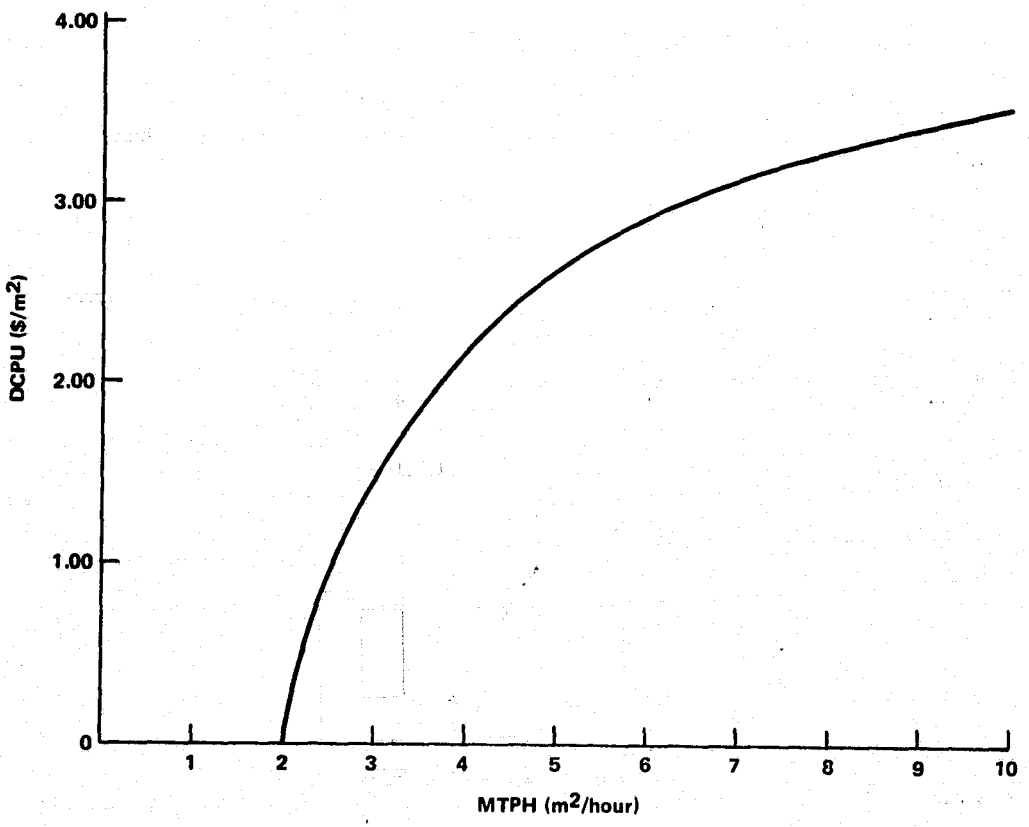


Figure 6. DCPU as a Function of MTPH

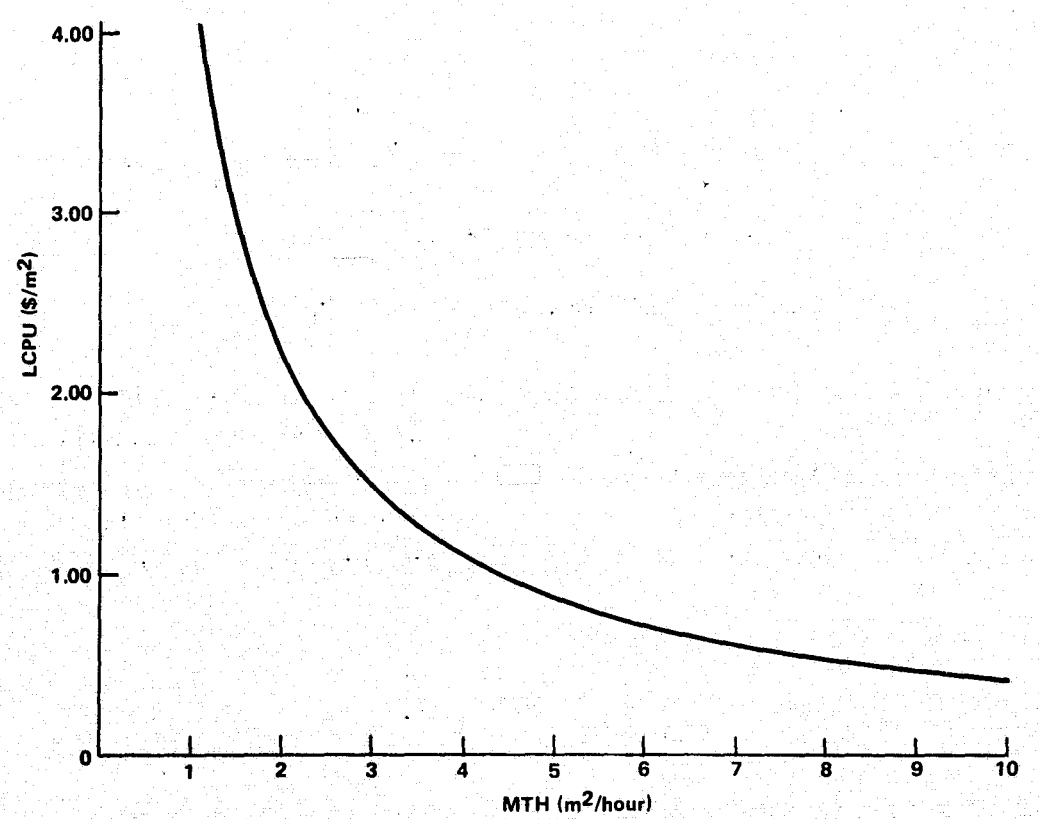


Figure 7. LCPU versus MTH

Table 4. Model Metallization System

OPM	1 technician
OPPH	$3.50/hour
OH	100% of OPPH
CPU	$5.88/$m^2$
MPU	$1.47/$m^2$
MTPH	>2 m^2/hour
LCPU	See Figure 7
DCPU	See Figure 6
CC	See Figure 5
Work Year	50 weeks 7 days/week 24 hours/day

Table 5. LCPU, DCPU and CC as a Function of Machine Throughput (10.16 cm diameter slices/hour)

Machine Throughput/Hour (10.16 cm diameter slices)	LCPU $/slice	DCPU $/slice	CC $K
200	.0219	(Below Threshold)	
250	.0175	.0005	2
300	.0146	.0064	65
350	.0125	.0106	125
400	.0109	.0137	185
450	.0097	.0161	245
500	.0088	.0180	305

C. SOLAR CELL DEVICE AND MODULE MODELING

Modeling was used in this study as a tool to define the impact of various parameters on output of solar cells and modules. A simple solar cell model consisting of a current generating source with a diode and a resistor in parallel and a resistor in series was found to be inadequate to describe actual solar cell I-V characteristics. Module modeling was done using a 4 X 4 cell array as a basic unit.

1. Solar Cell Modeling

A solar cell model was developed that includes a light generated current source with two diodes and a resistor in parallel with the current source and a resistor in series with the current source. The two diodes represent an ideal and a nonideal diode. The nonideal diode represents deviations from ideal diode behavior due to various defects or junction edge leakage. The two resistors represent series and shunt resistance in the solar cell. The values of the various components

in the equivalent circuit were varied to attain a "best fit" with actual solar cell characteristics. Figure 8 is a schematic of the equivalent circuit with observed values for the various components of the equivalent circuit for a solar cell with significant deviation from ideal diode behavior.

Families of I-V characteristic curves were generated by fixing the "best fit" model parameters and varying only one parameter. Figure 9 is the family of I-V characteristic curves generated by varying only the series resistance. From this family of curves, a quantitative assessment of the impact of series resistance can be gained. Figure 10 is a plot of maximum power versus series resistance (R_S) for this model. It is evident from an inspection of Figure 10 that series resistance at any level is a source of power loss in a solar cell. The design of an improved solar cell must therefore minimize series resistance in order to minimize power loss.

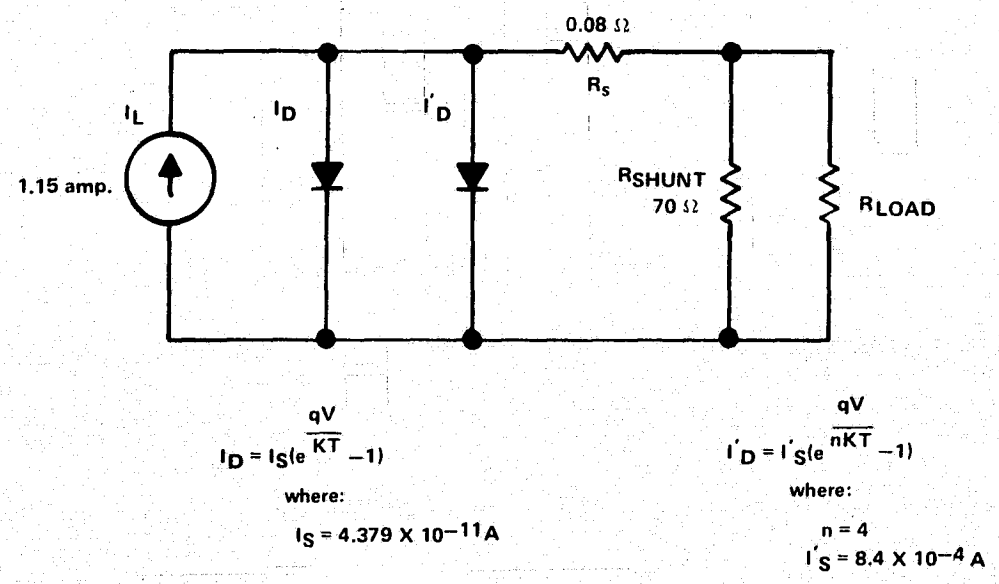


Figure 8. "Best Fit" Model of Actual Solar Cell Characteristics

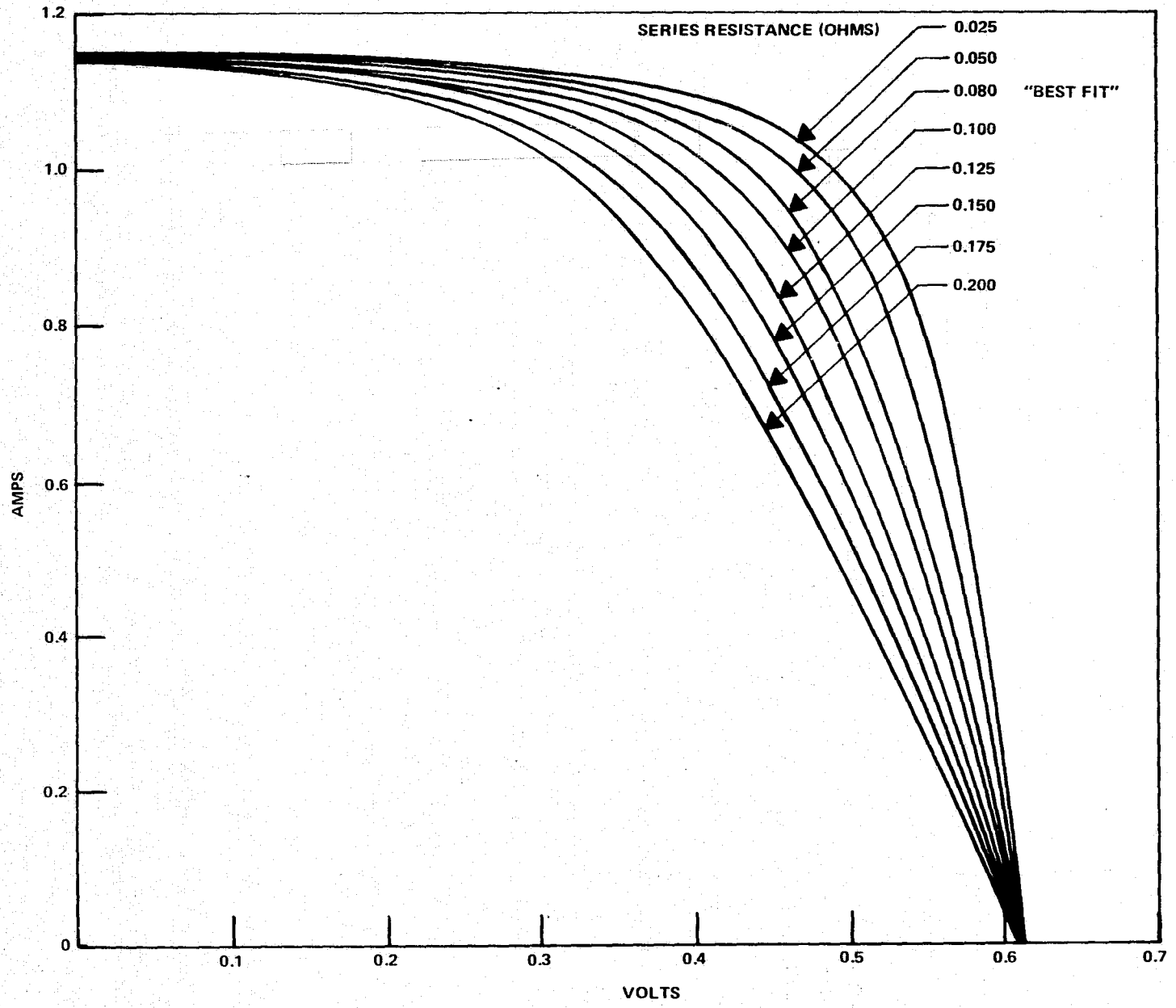


Figure 9. "Best Fit" Model I-V Characteristics with R_S as a Variable

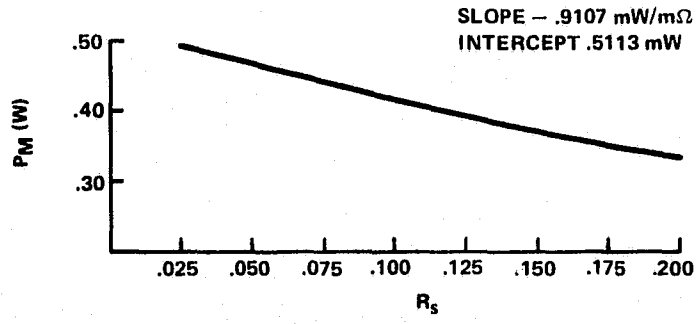


Figure 10. "Best Fit" Model Maximum Power as a Function of Series Resistance

Figure 11 is the family of I-V characteristic curves generated from the "best fit" model by varying only the excess component of current, I_S'. As I_S' increases, the impact on the solar cell performance is very severe. Decreasing values of I_S' give a marked increase in cell efficiency with maximum power going from 0.4373 W at $I_S' = 8.4 \times 10^{-4}$ ampere to 0.4869 at $I_S' = 1.05 \times 10^{-4}$ ampere. Figure 12 is a plot of maximum power (P_M) versus the log of I_S'. From an inspection of Figure 12, it is obvious that excess component of current can cause a very severe degradation in output current. This model data shows the importance of good diode characteristics on solar cell performance. Changes in I_S' over the life of a solar cell caused by improperly passivated junctions can lead to severe degradation of output power. Cell design, cell fabrication, and module fabrication processes must all be optimized to provide stable diode characteristics over the life of a solar cell module. It is also obvious from Figure 12 that improvement in I_S' (to lower values) is only beneficial to a point. For this model, values of I_S' below 10^{-5} ampere give no improvement in output power.

Variations of shunt resistance (R_{SH}) and the value of "n" in the "best fit" model confirm that series resistance (R_S) and nonideal diode characteristics are the key parameters affecting cell efficiency. For 7.6-cm cells, shunt resistance values $\geq$ 70 ohms cause no degradation in cell efficiency – below 70 ohms power output decays.

2. Module Modeling

A model of a 16-cell module was developed using the simple solar cell model shown in Figure 13. The solar cell characteristics are $V_{OC} = 0.55$ V and $I_{SC} = 1.272$ A with an internal resistance of 0.015 Ω. With an optimum load of 0.38 ohm, the series-parallel module would deliver 8.79 W at 4.81 A and 1.83 V if all cells are identical. Figure 14 is a schematic of the balanced array module. The I-V curve for the balanced array module is shown in Figure 15. A computer run with cell 11 generating no photocurrent, $R_L = 0.38$ ohm predicts that the module should deliver 5.52 W at 3.81 A and 1.27 V. With 25% of the module inoperative (one series leg of the 4 X 4 cell module),

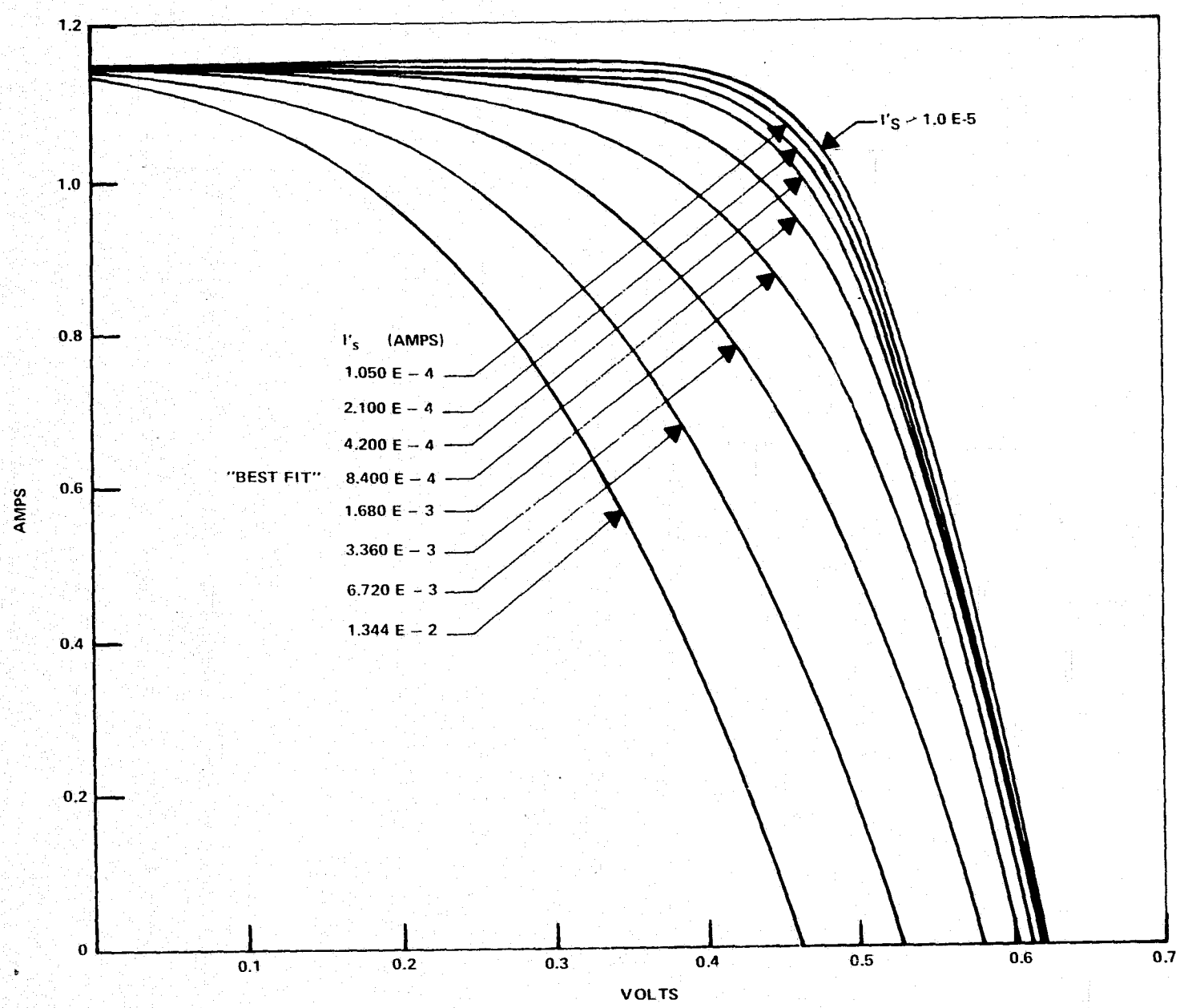


Figure 11. "Best Fit" Model I-V Characteristics with I_S' as the Variable

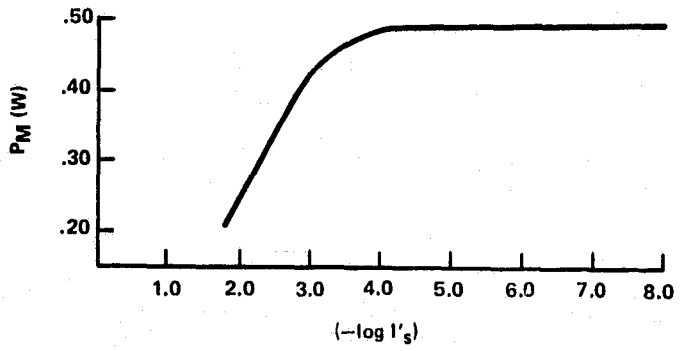


Figure 12. "Best Fit" Model Maximum Power as a Function of Excess Component of Current (I_S')

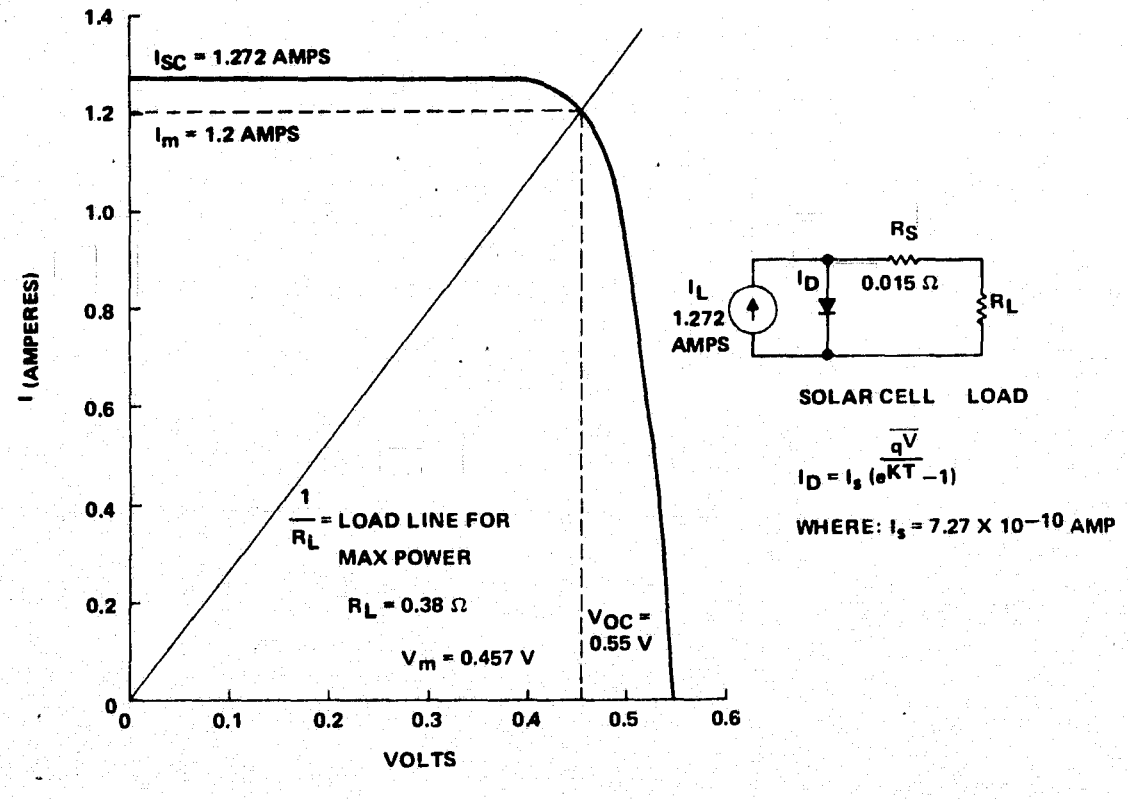


Figure 13. I-V Curve of Computer Modeled 7.6-cm Solar Cell

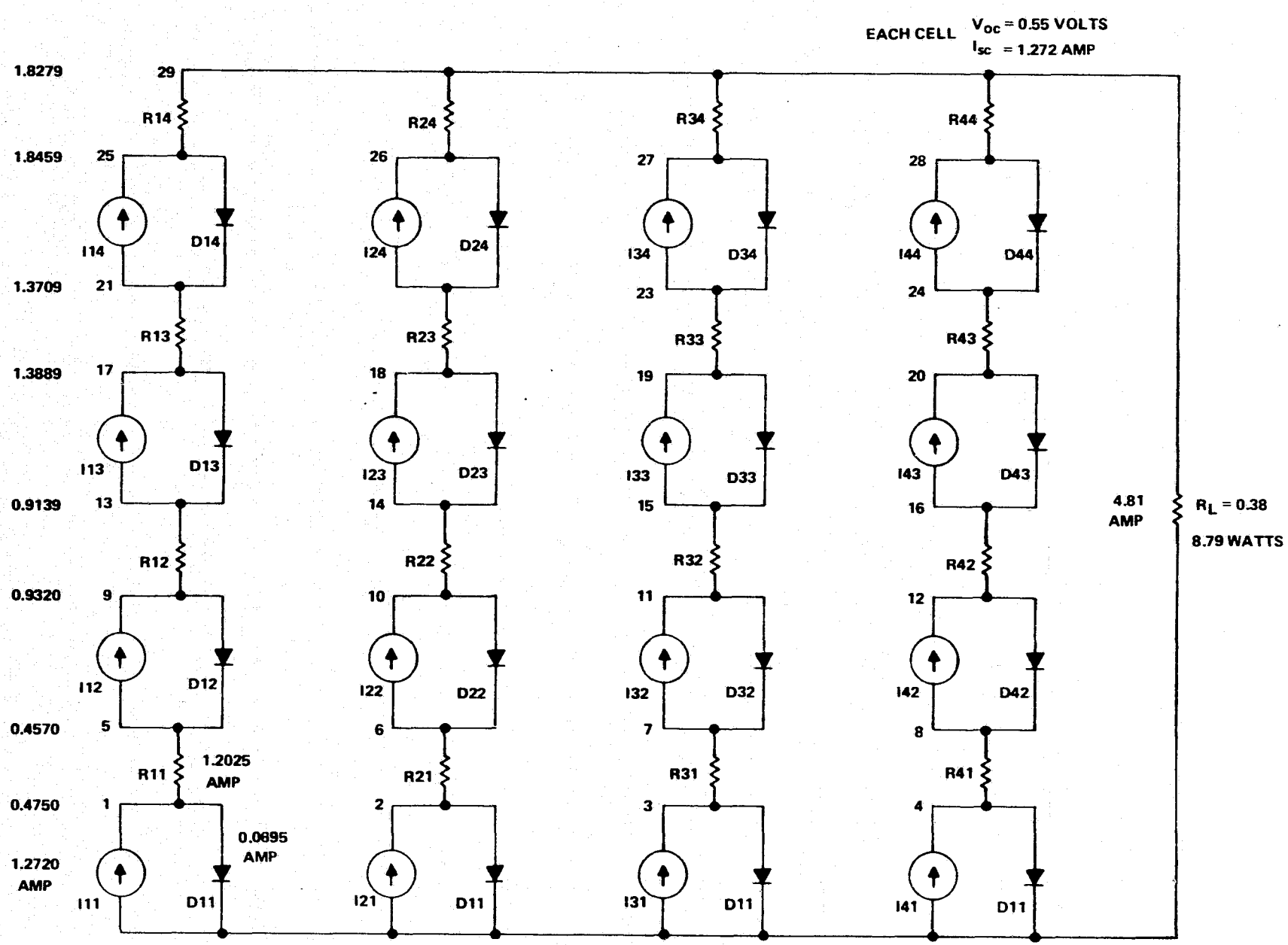


Figure 14. Solar Cell Module Model with Balanced Cells

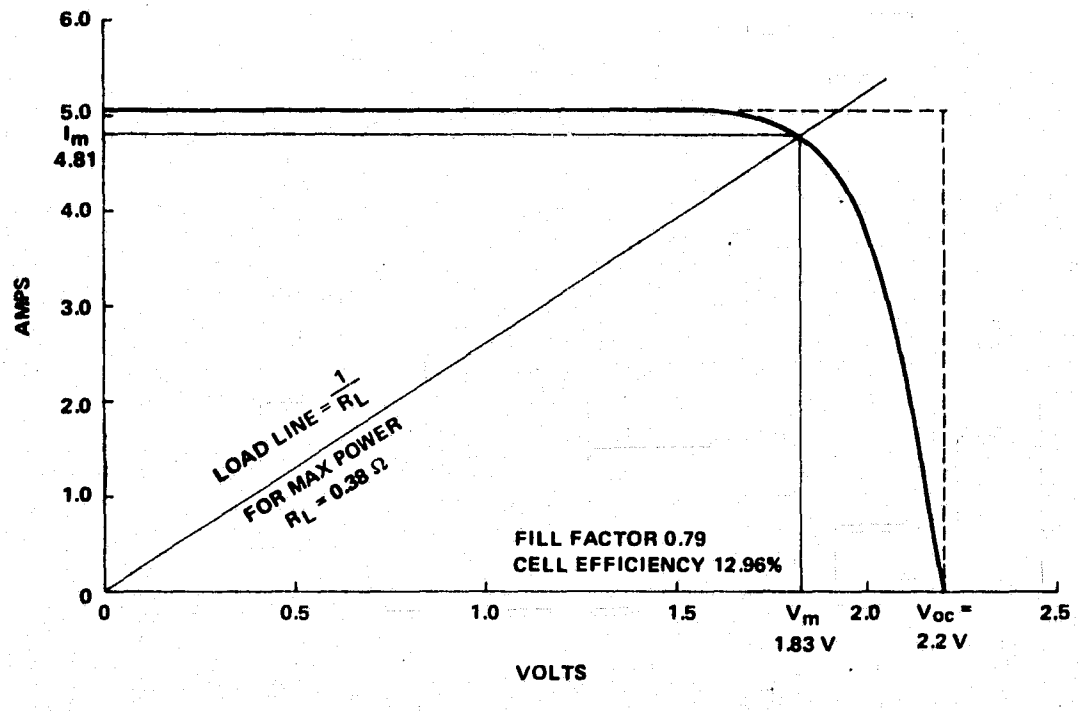


Figure 15. Solar Cell Module I-V Curve from Computer Model

the 3 X 4 portion of the module delivers only 63% of the original power. The 37% power loss due to a 25% loss of active cells is caused by the nonoptimum load conditions for the effective 3 X 4 module. The optimum load resistance for the damaged module would be 0.51 ohm. Figure 16 shows the model schematic for the array with cell 11 inoperative.

Two failure mechanisms have been investigated to date. One cell of the 4 X 4 module model was selected as the failing cell and one of its parameters varied from 0 to 120% nominal value.

The first parameter varied was light generated current. A graph of normalized power output versus I_L of one cell is shown in Figure 17.

The second parameter varied was open circuit voltage. A graph of normalized power output as V_{OC} is varied as shown in Figure 18. A module schematic is shown in Figures 14 and 16. From Figures 17 and 18, a variation of ±10% in V_{OC} or I_{SC} of one cell of a 16-cell module would cause less than a 2% variation in module output power. A variation of ±20% in one cell would cause less than a 5% variation in module output.

Analysis of the 4 X 4 array connected in a parallel-series arrangement instead of a series-parallel gives essentially the same result.

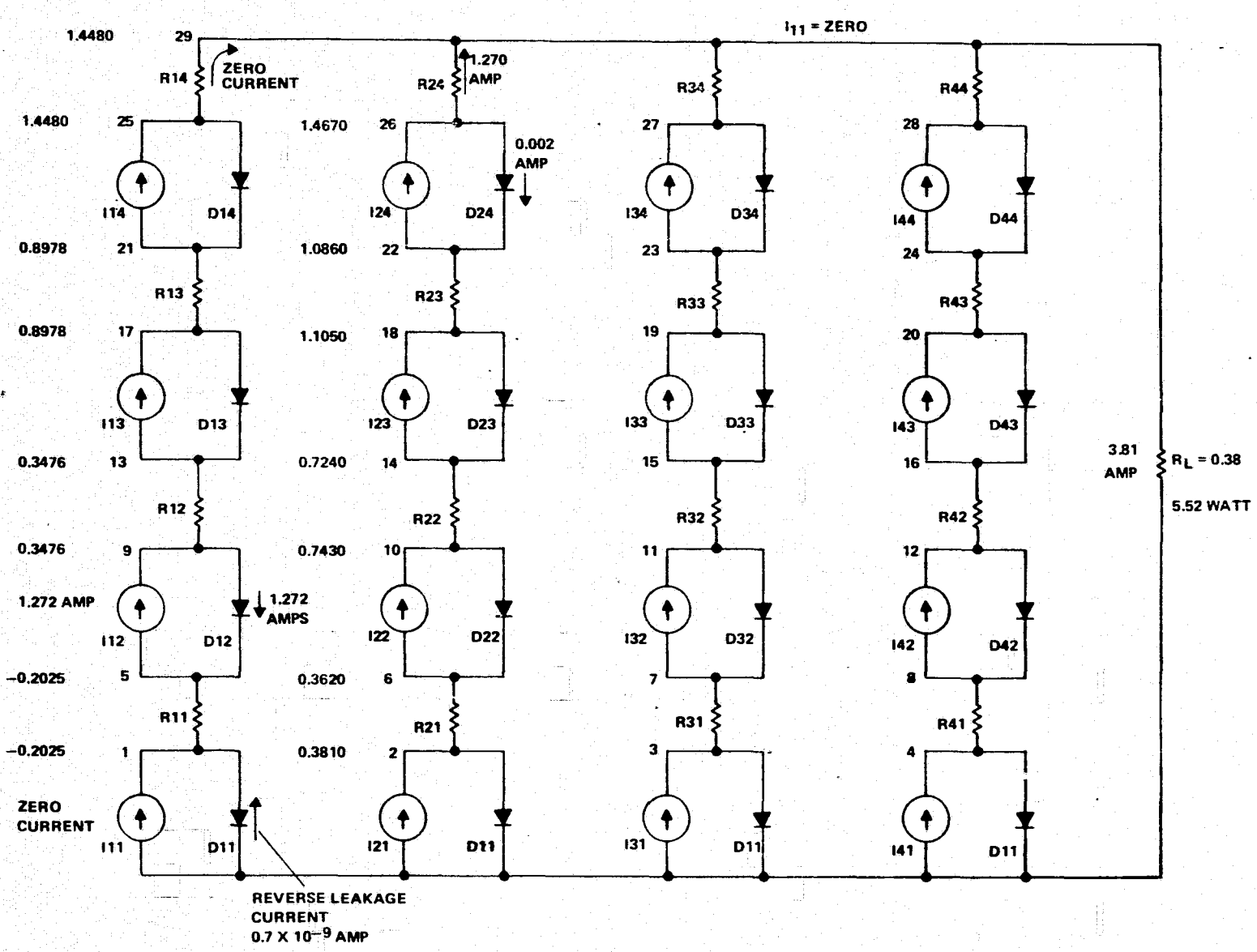


Figure 16. Solar Cell Module Model with One Inoperative Cell

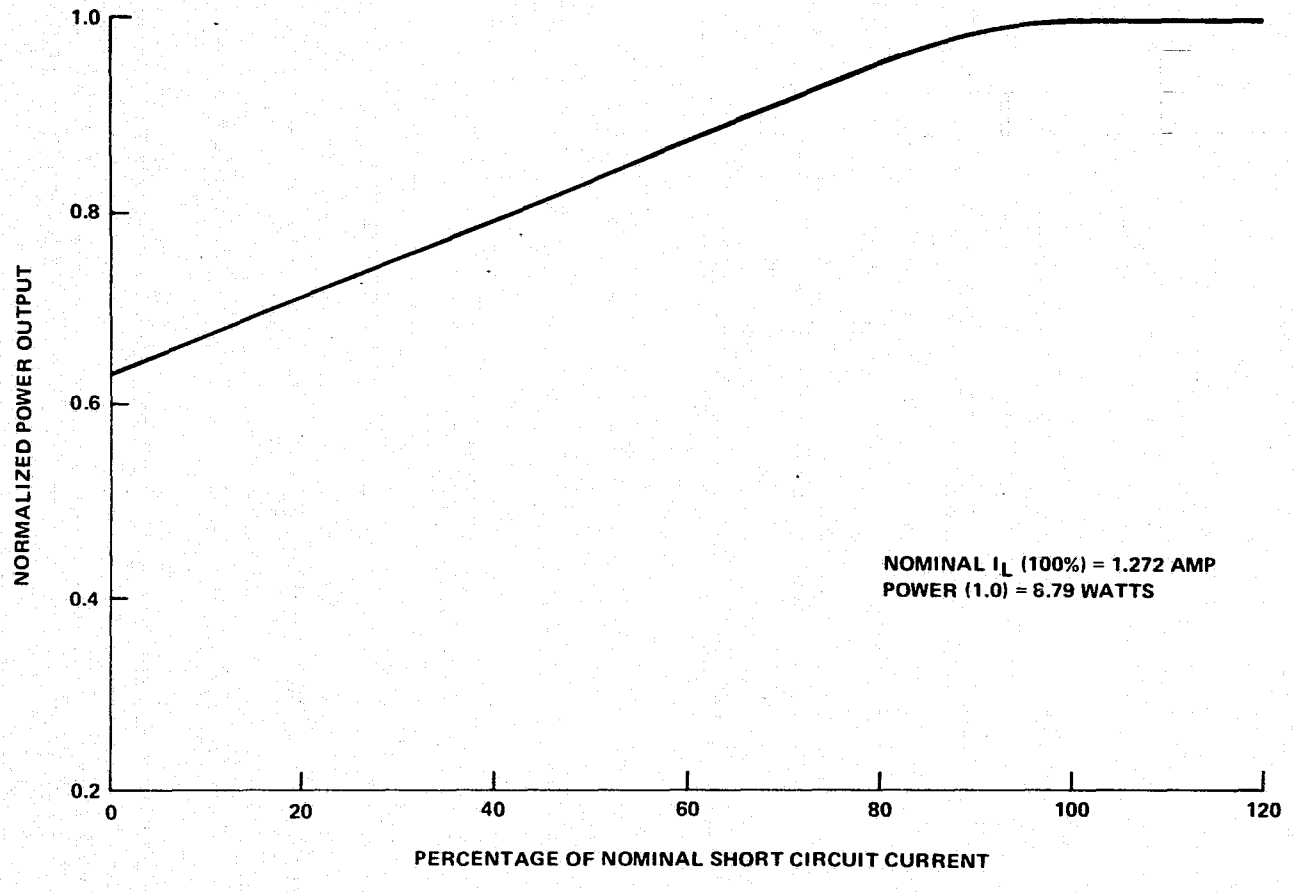


Figure 17. Normalized Power Output of 16-Cell Module as I_L of One Cell Varies

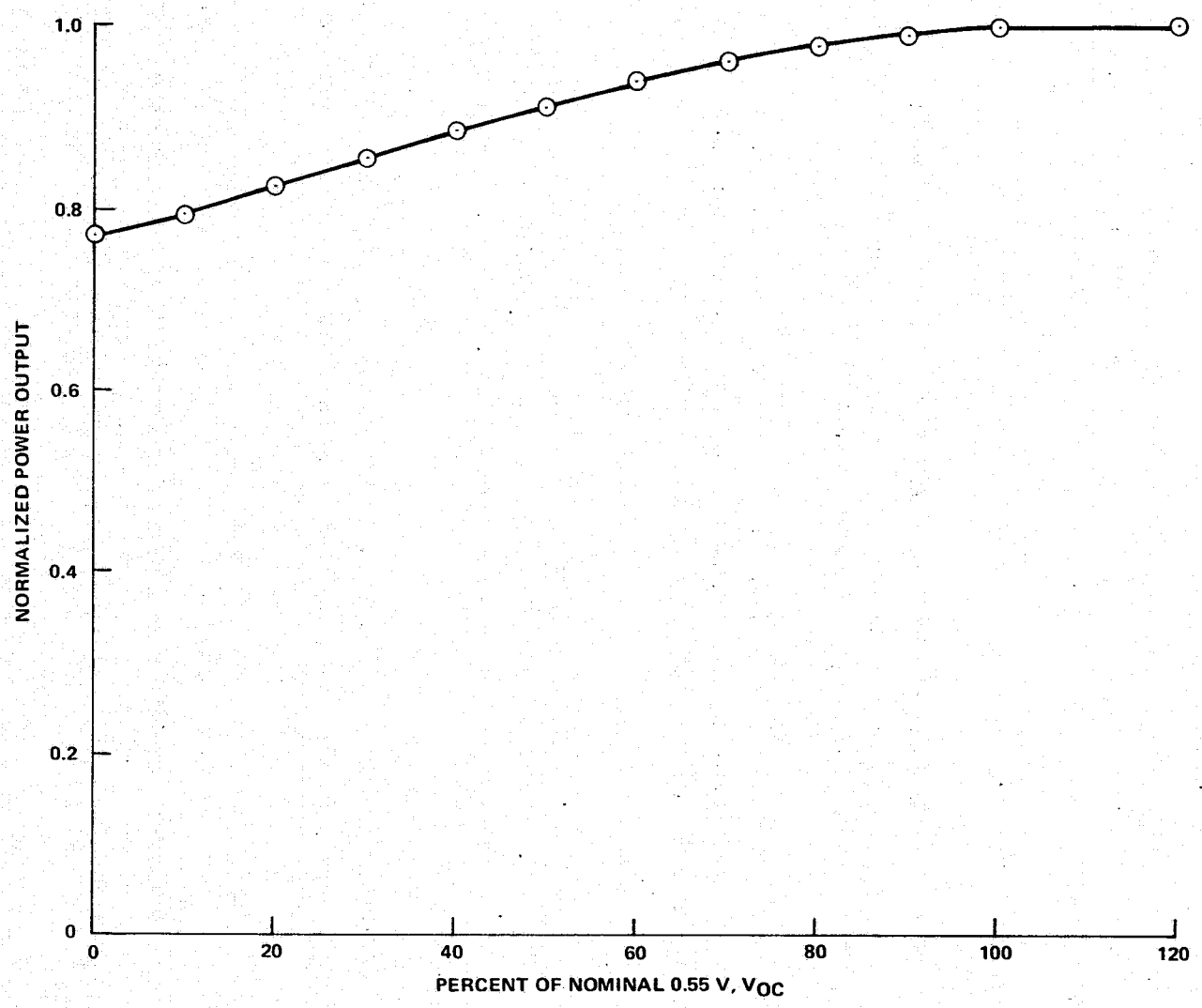


Figure 18. Sixteen-Cell Module V_{OC} of One Cell Varying

D. COMPUTER OPTIMIZATION OF METALLIZATION PATTERN

The LSSA project goal of $500/W for silicon solar cell modules is obviously dependent upon module and cell efficiency. Cost per watt is inversely proportional to efficiency. Therefore a metallization pattern design study was undertaken to define a technique for optimizing the front-side metal pattern as a function of design constraints and as a quantitative tool in the evaluation of metallization process technologies. For example, what is the efficiency impact of using a metallization process technology that can form a metal pattern with a minimum line width of 100 μm? or 10 μm?

1. Scope

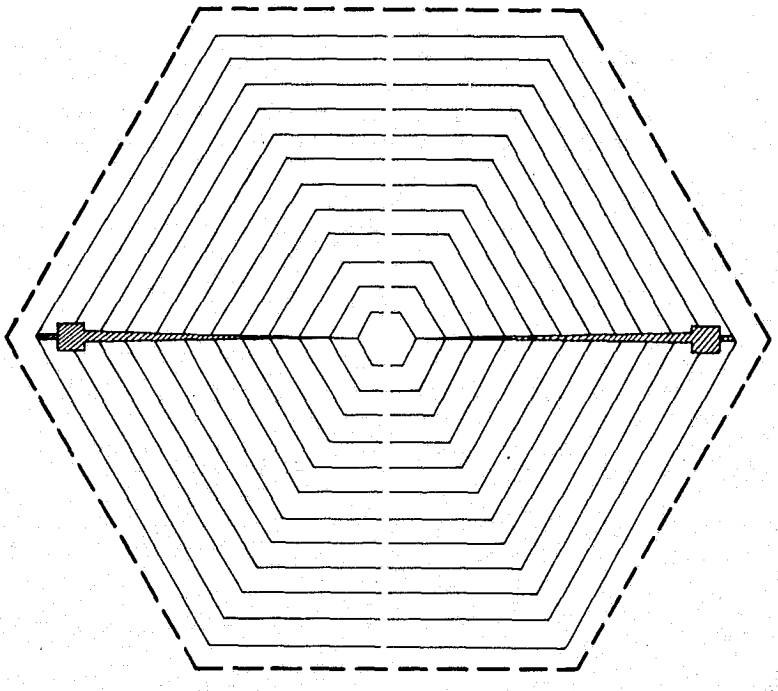
Design of the front surface metallization pattern for solar cells requires a trade-off between resistive power losses and metal shadowing loss. The objective of this part of the program was to provide design data for minimizing the sum of these losses.

The analysis presented here applies primarily to large-area silicon solar cells for terrestrial solar panels. Design constraints have been imposed which are consistent with this application. For example, bond pads are at the cell edge; the number of pads is restricted for compatibility with panel assembly.

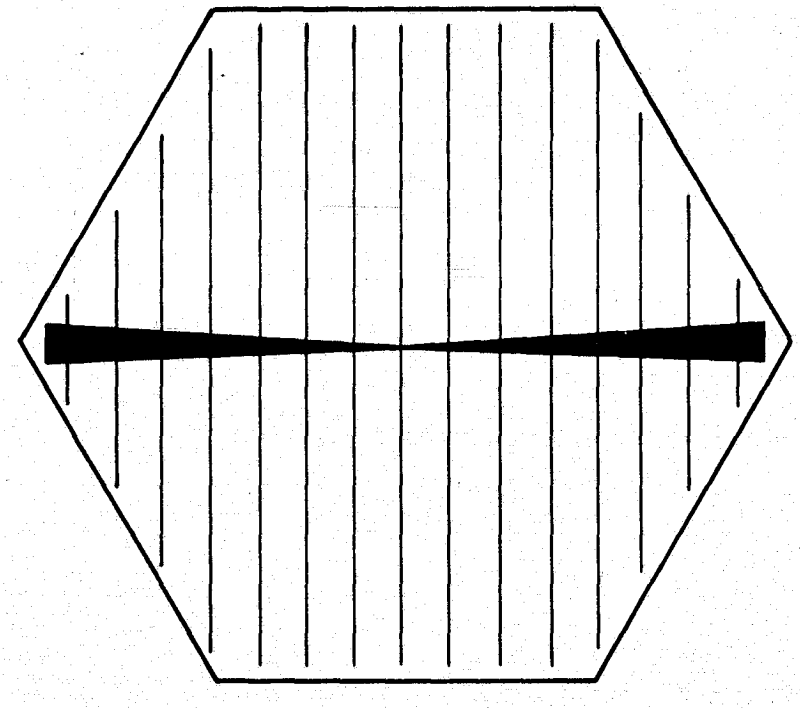
Cell configurations analyzed include hexagonal and rectangular shapes. A computer program was developed to calculate spacing of metal fingers which minimizes the sum of resistive and shadowing losses. Optimum spacing and cell efficiency were calculated for a range of cell sizes and metal finger widths.

The analysis was carried out using representative values of process parameters, assuming AM1 illumination and uniform current density over the cell. Resistive loss in the homogeneous base (1.0 ohm-cm) and contact resistance have been neglected.

Details of the computer program are illustrated first for a hexagonal cell with concentric metal fingers, shown in Figure 19(a). The analysis was also carried out for a hexagonal cell with a "fishbone" pattern and for a rectangular cell. These configurations are shown in Figures 19(b) and 26(a). For the latter two cases, program modifications are discussed and results are shown for comparison to the concentric hexagon.



a. CONCENTRIC HEXAGONAL PATTERN



b. FISHBONE HEXAGONAL PATTERN

Figure 19. Hexagonal Solar Cell Metallization Patterns

2. Concentric Hexagonal Pattern

The concentric metal pattern for the hexagonal cell is shown in Figure 19(a). Current is collected by concentric metal fingers which are connected to the bond pads by tapered metal trunk lines. The metal fingers are parallel and of constant width for a given cell.

Losses associated with the metal fingers are illustrated by the cell segment shown in Figure 20(a). The segment is bounded by the center lines of two metal fingers of width, T, length, L, and spacing, S.

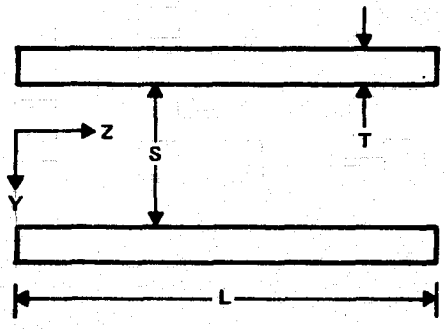
The components of power loss associated with the cell segment are:

1) Resistive loss due to current in the diffused layer

2) Resistive loss in the metal fingers

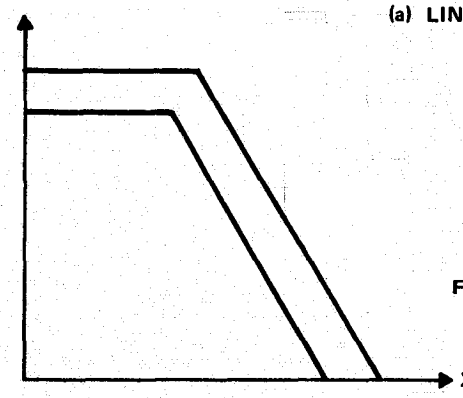
3) Shadowing loss from the metal fingers.

If the finger width, T, is held constant and the spacing, S, is varied, there is a value of S for which the total power loss per unit area of the cell segment is minimized.



LOSS COMPONENT	FRACTIONAL LOSS (POWER LOSS/POWER AVAILABLE)
DIFFUSED RESISTANCE	$a\frac{S^3}{S+T}$
METAL RESISTANCE	$b\frac{L^2S^2}{T(S+T)}$
METAL SHADOWING	$\frac{T}{S+T}$

(a) LINEAR SEGMENT



$$F = a'\frac{S^3}{(S+T)} + b'\frac{X^2S^2}{T(S+T)} + \frac{T}{S+T}$$

(b) HEXAGONAL SEGMENT

Figure 20. Loss Components for Solar Cell

Power loss per unit area is evaluated in terms of fractional loss components. The fractional loss component is defined as

$$F = P_{loss}/P_S \tag{13}$$

where P_{loss} is a power loss component and

$$P_S = (j)\,(V_m)\,(A_S)$$

is the maximum power which can be delivered to the load, assuming no shadowing or resistive losses. In the above expressions, j and V_m are current density and voltage, respectively, at the load for maximum power, and

$$A_S = L\,(S + T)$$

is the area of the cell segment.

Resistive losses in the diffused region and the metal fingers are calculated using a technique similar to other reported work.[2] The interpretation is different, in that power loss is considered rather than voltage drop.

The power loss due to transverse current flow through the diffused region is

$$P_D = 2\int_{y\,0}^{S/2} [i(y)]^2\, dR_D \tag{14}$$

where

$$i(y) = jLy$$

is current flow through the diffused region,

$$dR_D = \rho\,\frac{dy}{L}$$

is the incremental transverse resistance of the diffused region, and ρ is the sheet resistivity of the diffused region. The fractional loss for the diffused region resistance is

$$F_D = \frac{P_D}{P_S} = \frac{1}{12} \frac{j\rho}{V_m} \frac{S^3}{(S+T)} \tag{15}$$

For the resistive loss in the fingers, the fractional loss is

$$F_F = \frac{P_F}{P_S} = \frac{1}{P_S} \int_{Z=0}^{L} [i(Z)]^2 \, d\, R_F \tag{16}$$

where

$$i(Z) = j\, S\, Z$$

is the current in each of the metal fingers and

$$dR_F = \frac{M}{T} d\, Z$$

is the incremental resistance of a metal finger. The sheet resistance of the metal finger is M. In terms of the above equations, the fractional resistive loss in the metal fingers is

$$F_F = \frac{j\, M\, L^2\, S^2}{3\, V_m\, T\, (S+T)} \tag{17}$$

The fractional loss component due to coverage by the metal fingers is

$$F_c = \frac{T}{S+T} \tag{18}$$

A segment for the hexagonal cell is shown in Figure 20(b). The length of the segment is $L = 1.5\, X$ where X is the distance along a major diagonal from the center of the hexagon. The sum of the loss factors for the hexagonal segment is

$$F_S = \frac{a'\, S^3}{S+T} + \frac{b'}{(S+T)} \frac{X^2\, S^2}{T} + \frac{T}{S+T} \tag{19}$$

where

$$a' = \frac{1}{12}\,\frac{j\rho}{V_m}$$

and

$$b' = \frac{3}{4}\,\frac{jM}{V_m}$$

It is seen from the above equation that F_S will have a minimum which depends upon the values of S, X, and T. For a constant value of T, the optimum value of S will vary with X.

The optimum value of S might be determined analytically by differentiating F_S with respect to S and solving a cubic equation for S as a function of T and X. The alternative approach taken here was to use a computer program to calculate and minimize the sum of the fractional loss components for each cell segment.

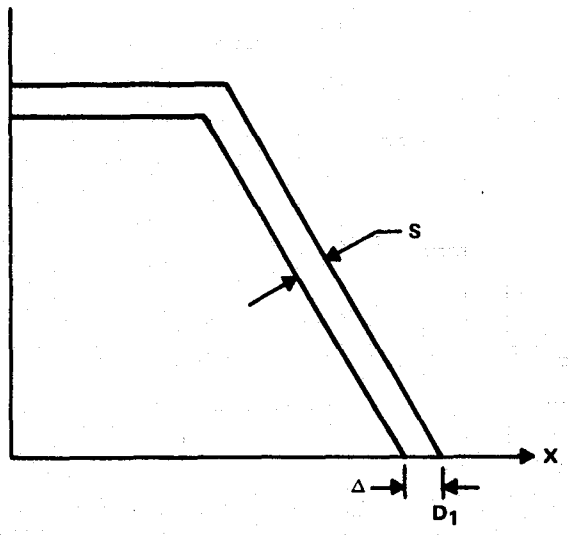
A computer program was developed which determines optimum spacing of metal fingers of a hexagonal cell as a function of distance from the center and finger width. Additionally, the program calculates power loss components for this optimized spacing from which metal-shadowing efficiency and series-resistance efficiency are determined.

The technique used for the computer analysis is illustrated in Figure 21(a). Fractional loss components are calculated for a segment at the cell periphery. The width S of the segment is varied by incrementing Δ along the x-axis. Losses are calculated initially for a small value of Δ; calculations are repeated for successive values of Δ, as Δ is increased by small increments. The first value of Δ which causes the sum of the three fractional loss components to increase is selected as the optimum value, Δ_{opt}, for the initial value of $X(X = D_1)$; i.e., the optimum spacing is given by

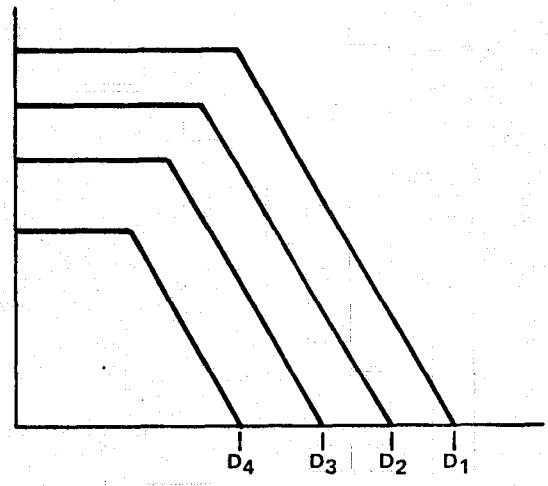
$$S + T = \Delta_{opt}\,(\cos 30^\circ) \tag{20}$$

As shown in Figure 21(b), the first hexagonal segment is then defined by D_1 and D_2 where

$$D_2 = D_1 - \Delta_{opt} \tag{21}$$



(a) INITIAL SEGMENT



(b) SUCCESSION OF SEGMENTS

Figure 21. Hexagonal Segments Used in Computer Analysis

Successive hexagonal segments are determined by repeating the procedure until $D_n \leqslant 0$. The metal fingers in each case are located midway between the values of D_n and D_{n-1}.

The above procedure was used to determine optimum spacing as a function of distance from the center of a hexagon. This data is shown in Figure 22 for a range of values of metal finger width.

Losses for the trunk line were also calculated by the computer program. The configuration of the trunk lines is shown in Figure 19(a). Current from the fingers is carried by the trunk lines to the bond pads located at the outer edge of the trunk lines. The trunk configuration was designed to minimize the sum of resistive and shadowing losses.

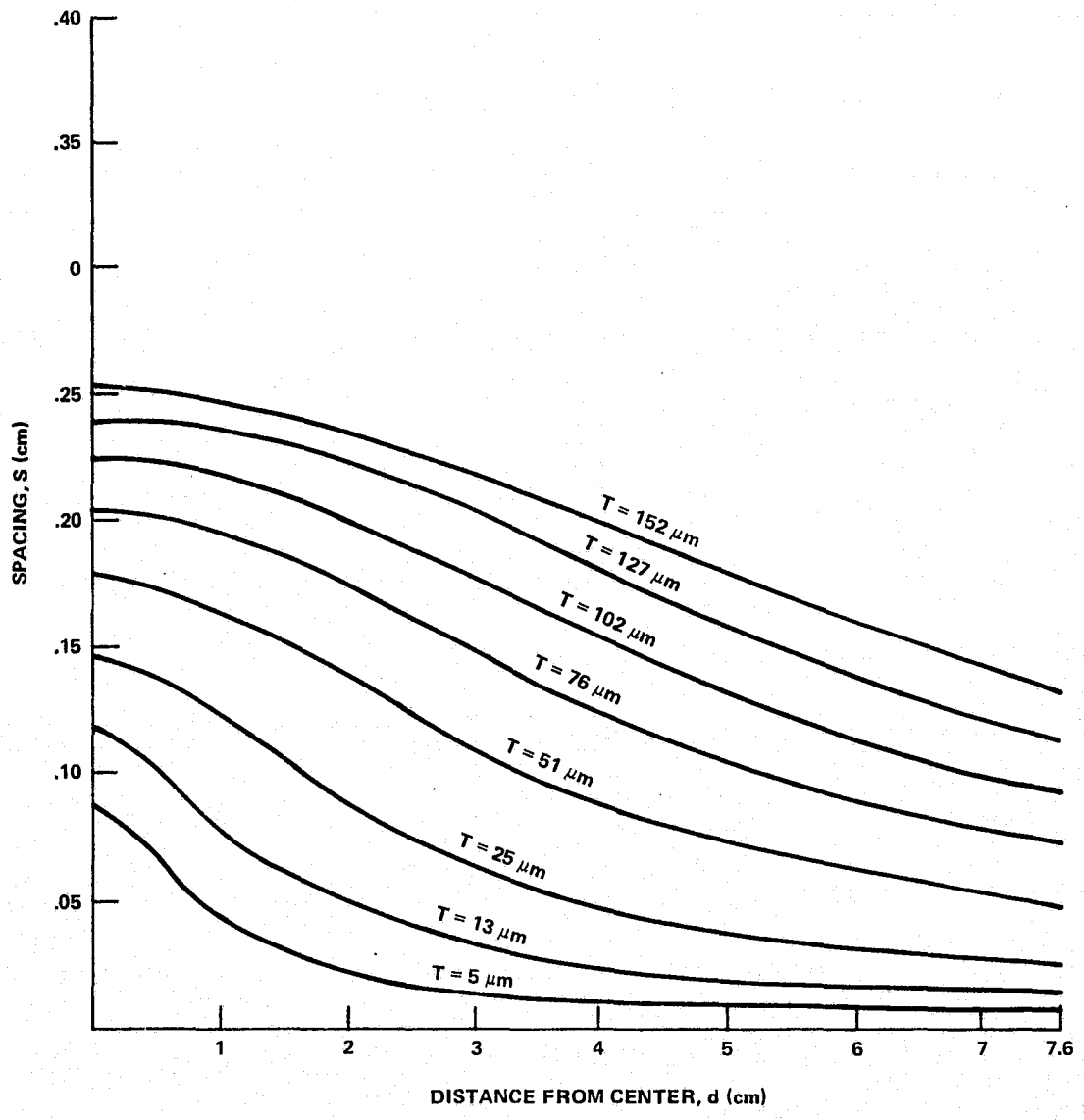


Figure 22. Optimum Metal Line Spacing versus Distance from Center as a Function of Metal Line Width for Hexagonal Solar Cells

The current in each trunk line as a function of distance, X, from the center of the hexagon is

$$i(x) = \frac{3\sqrt{3}}{4} X^2 j \qquad (22)$$

where j is the current density. The incremental resistance of the trunk line is

$$d R = \frac{M}{T_T (x)} d x \qquad (23)$$

where M is the sheet resistance of the metal, and the width of the trunk line is assumed to increase with X according to the relationship

$$T_T(x) = K X^n.$$

The resistive power loss in each trunkline is

$$P_{RT} = \int_o^D [i(x)]^2 \, dR \qquad (24)$$

$$= \frac{27}{16} \frac{M}{K} j^2 \frac{D^{(S-n)}}{(5-n)}$$

where $D = (DIAG)/2$

and (DIAG) is the major diagonal.

The power loss due to metal coverage for each trunk line is

$$P_{CT} = \int_o^D K x^n \, dx \qquad (25)$$

$$= \frac{KD^{(n+1)}}{n+1}$$

The fractional resistive loss component is

$$F_{RT} = \frac{2 P_{RT}}{P_A} \qquad (26)$$

where P_A, the total available power is

$$P_A = A_T \cdot V_m \cdot j \qquad (27)$$

and

$$A_T = \frac{3\sqrt{3}}{8} (DIAG)^2 \qquad (28)$$

is the area of the hexagon. From the above equations

$$F_{RT} = \frac{3\sqrt{3}}{4\,(5-n)} \frac{Mj}{K} \frac{D^{(3-n)}}{V_m} \tag{29}$$

The fractional loss due to metal coverage is

$$F_{cT} = \frac{2\,P_{cT}}{A_T} \tag{30}$$

$$= \frac{4}{3\sqrt{3}} \frac{K\,D^{(n-1)}}{(n+1)}$$

The sum of the fractional loss components for the trunk,

$$F_{RT} + F_{cT} = \frac{3\sqrt{3}}{4\,(5-n)} \frac{Mj}{K} \frac{D^{(3-n)}}{V_m} + \frac{4}{3\sqrt{3}} \frac{K\,D^{(n-1)}}{(n+1)} \tag{31}$$

is minimized when

$$K^2 = \frac{27}{16} \frac{(n+1)}{(5-n)} \frac{(Mj)\,D^{(4-2n)}}{(VM)}$$

Hence

$$F_{RT} = F_{cT} = \frac{D}{\sqrt{n+1}\,\sqrt{5-n}} \sqrt{\frac{Mj}{V_m}} \tag{32}$$

These losses will be minimized when

$$n = 2.$$

For this case

$$F_{RT} = F_{cT} = \frac{D}{3} \sqrt{\frac{Mj}{V_m}} \tag{33}$$

$$= \frac{DIAG}{6} \sqrt{\frac{Mj}{V_m}}$$

Note that for n = 2, the current density in the trunk line is constant. Intuitively, we would expect this condition to minimize the losses. For an optimized linear taper, used in the first design, losses are higher by a factor of 1.06.

When the optimum spacing has been determined for a segment, the power loss components are computed for that segment; e.g., the power loss components for the j^{th} segment are

$P_{D(j)}$ diffused resistive power loss

$P_{F(j)}$ finger resistive power loss

$P_{C(j)}$ finger coverage power loss

These power loss components are summed to give total power loss components for the n segments of the cell; i.e.,

$$S_D = \sum_{j-1}^{n} P_{D(j)}$$

$$S_F = \sum_{j=1}^{n} P_{F(j)}$$

$$S_C = \sum_{j=1}^{n} P_{C(j)}$$

Loss factors for the cell are defined as

$F_{DR} = S_D/P_A$ diffused resistive loss factor

$F_{FR} = S_F/P_A$ finger resistive loss factor

$F_{FC} = S_C/P_A$ finger coverage loss factor

where

$$P_T = A_T \cdot j \cdot V_m$$

is the total power available at the maximum power point, A_T is the total cell area, and j and Vm are current density and voltage for maximum available power.

The total loss factor for metal coverage is

$$F_{TC} = F_{FC} + F_{CT} \tag{34}$$

where F_{CT} is the trunk coverage factor.

Total resistive loss factor is defined as

$$F_{TR} = F_{DR} + F_{FR} + F_{RT} \tag{35}$$

where F_{RT} is the trunk resistive loss factor.

Efficiency for metal coverage is

$$E_C = (1 - F_{TC})\,100 \tag{36}$$

and efficiency for resistive loss is

$$E_R = \left(1 - \frac{F_{TR}}{(1 - F_{TC})}\right) 100 \tag{37}$$

The efficiency product for metal coverage and series resistance is

$$E_P = \frac{(E_C)(E_R)}{100} \tag{38}$$

Constants used for calculation of optimum spacing, loss components, and efficiencies are shown in Table 6.

Optimized fractional loss components for the total cell were calculated as a function of finger width for a hexagonal cell of 7.6 cm diagonal. As shown in Figure 23, finger resistance loss and finger coverage loss are of comparable importance for small finger widths. However, finger coverage loss dominates for wide fingers.

Table 6. Design Assumptions for Improved Solar Cells

- 2 Contact pads on opposite points
- AM1 (no concentrator)
- Diffused layer sheet resistance, r ≅ 80 Ω/□
- 6 μm Ag, m = 0.00333 Ω/□
- Design equations based on minimized power loss (based on minimizing the sum of resistance loss and metal shadowing loss)
- Contact resistance and bulk resistance assumed negligible
- Voltage output for maximum power = 0.50 V
- Current density for maximum power = 32.5 mA/cm^2

The product of series-resistance efficiency and metal-coverage efficiency was calculated for a range of values of finger width and for a range of diameters of hexagonal cells. This data is plotted in Figure 24. It is noted that for large cells, the product is not significantly improved by use of very narrow finger widths.

3. "Fishbone" Pattern

The "fishbone" configuration, shown in Figure 19(b), consists of trunk lines along a major diagonal of the hexagon with perpendicular metal fingers on each side of the trunk. Optimum spacing for the metal fingers is calculated from the sum of the fractional losses

$$F = a'' \frac{S^3}{S+T} + b'' \frac{S^2}{S+T} + \frac{T}{S+T} \tag{39}$$

where S is the spacing between fingers, T is the finger width, and a″ and b″ depend upon fabrication parameters. The length, L, of the fingers is related to distance, X, from the center of the hexagon by the relationships

$$L = \frac{\sqrt{3}\,D}{2} \qquad 0 < X < \frac{D}{2}$$

$$L = \sqrt{3}\,(D - X) \qquad \frac{D}{2} < X < D$$

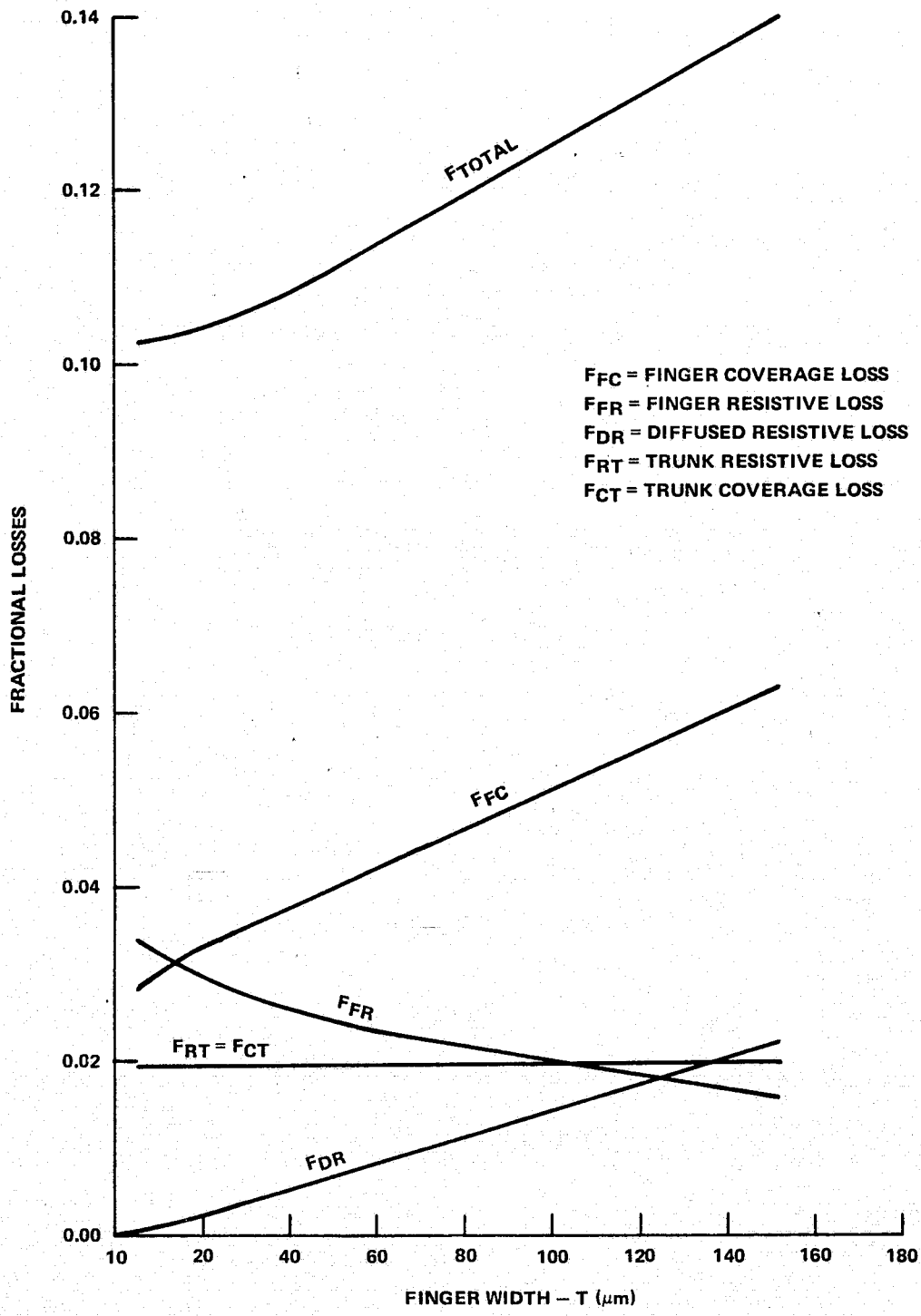


Figure 23. Fractional Loss Components for 7.6-cm Hexagonal Solar Cell as a Function of Metal Finger Width

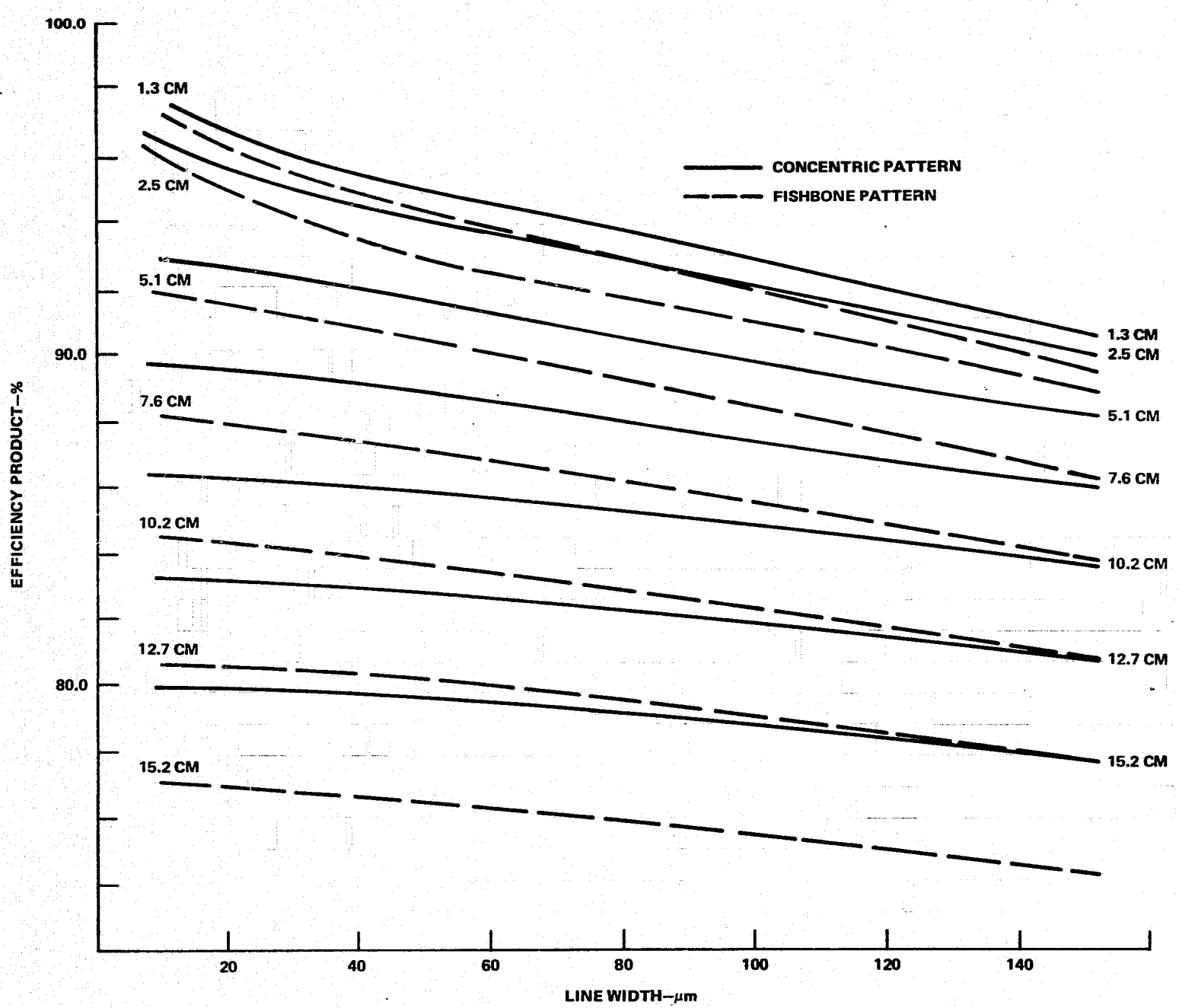


Figure 24. Efficiency Product for Metal Coverage and Series Resistance versus Metal Finger Width as a Function of Cell Diagonal for Hexagonal Cells

As for the concentric hexagonal pattern, the computer program determines optimum spacing as a function of X, computes power loss components and increments to the next segment.

The trunkline is tapered such that current density is the same for all values of X. For $X \leq \frac{D}{2}$,

$$i(X) = \sqrt{3}\, j\, D\, X$$

In this region, the width of the trunk line is

$$T_T(X) = K\, X.$$

Current density for the trunk line is

$$j_T = \frac{2\,(X)}{T_T\,(X)} = \sqrt{3}\,\frac{jD}{K} \tag{40}$$

For the region $D/2 < X < D$, current in the trunk line is

$$i\,(X) = j\sqrt{3}\,(2\,D\,X - D^2/4 - X^2)$$

For constant current density, trunk width in this region is

$$T_T\,(X) = \frac{i\,(X)}{\sqrt{3}\; j\, D/K}$$

trunk resistive and coverage loss factors are calculated as

$$F_{RT} = \frac{2}{P_A}\int_o^D [i(X)]^2\,\frac{M}{T_T(X)}\,dx \tag{41}$$

and

$$F_{CT} = \frac{2}{A_T}\int_o^D T_T\,(X)\,dx \tag{42}$$

where P_A and A_T are total available power and total area as defined before. The sum of these losses is minimum when

$$F_{RT} = F_{CT} \tag{43}$$

For this condition

$$K^2 = \frac{3}{4}(DIAG)^2 \frac{jM}{V_m}$$

and

$$F_{RT} = F_{CT} = \frac{11}{36}(DIAG)\sqrt{\frac{jM}{V_m}}$$

The product of metal-coverage efficiency and series-resistance efficiency is plotted in Figure 24 vs metal line width, as a function of cell diagonal for hexagonal cells. Efficiency products for both the fishbone metal pattern and the concentric metal pattern are shown for comparison. In Figure 25, efficiency products are plotted versus cell diagonal for the concentric and fishbone hexagonal patterns with 100 μm metal line width.

In both Figures 24 and 25, we note that the efficiency product for the concentric pattern is always higher than for the fishbone pattern with the same diagonal and line width.

4. Rectangular Pattern

The basic rectangular pattern, shown in Figure 26(a), consists of parallel metal fingers connected to one edge of a trunk. The trunk is a tapered line with a bond pad at the larger end. As shown later, efficiencies for other rectangular configurations can be deduced from combinations of this pattern.

For one segment of the cell, the sum of fractional losses due to diffused region resistive loss, finger resistive loss, and finger shadowing loss, is

$$F = a\frac{S^3}{S+T} + 6\frac{W^2S^2}{(S+T)T} + \frac{T}{S+T}. \tag{44}$$

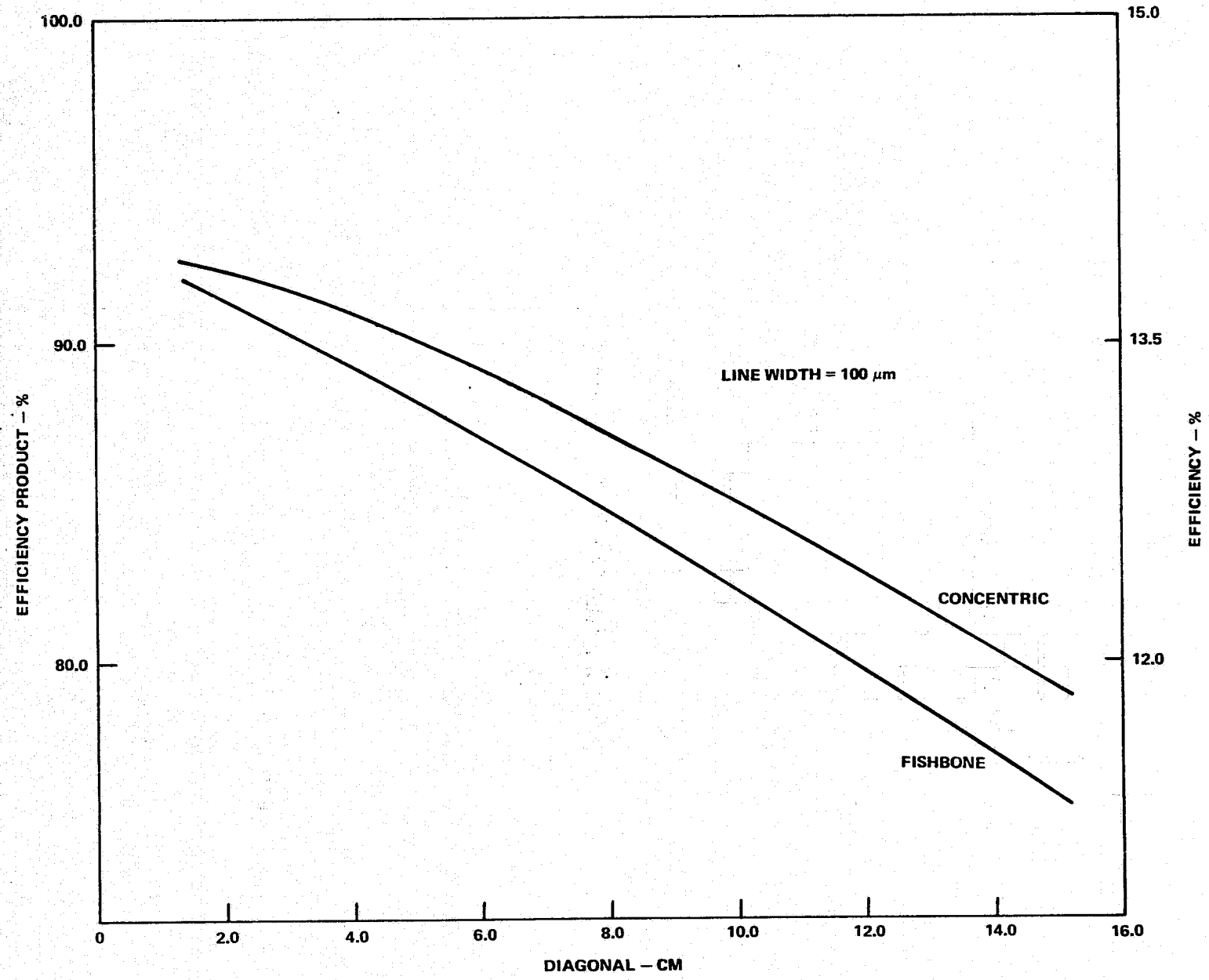
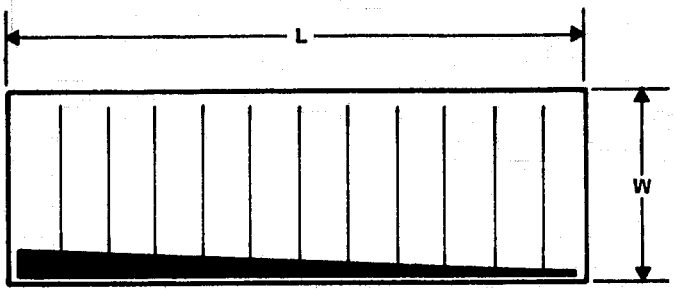
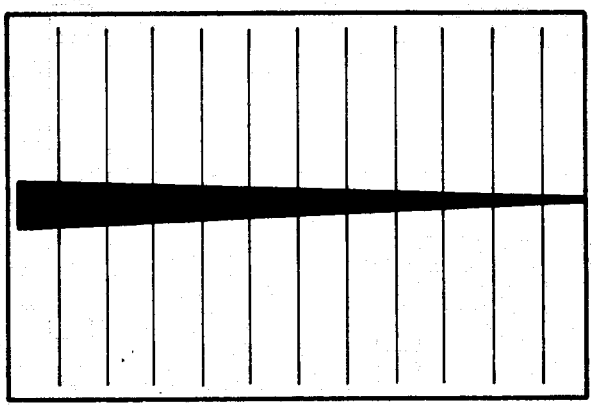


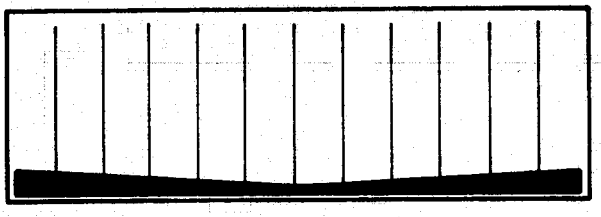
Figure 25. Efficiency Product and Efficiency as a Function of Cell Diagonal



a. RECTANGULAR COMB PATTERN



b. RECTANGULAR FISHBONE PATTERN



c. RECTANGULAR BOW-TIE PATTERN

Figure 26. Rectangular Solar Cell Metal Patterns

The computer program determines the value of spacing, S, which minimizes F and computes the values of F and efficiency product for that spacing. It is assumed that the length, H, of the cell is much larger than S so that all segments are of optimum width. Hence, the efficiency product for the cell is the same as for a segment. The efficiency product, Ep, for diffused region loss and finger loss is plotted in Figure 27 versus finger width, T, as a function of cell width, W.

Resistive loss for the trunk line is

$$P_{RT} = \int_0^H [i(X)]^2 \, d\,R \tag{45}$$

where X is the distance along the length, H, of the cell, j is the current density, M is sheet resistance of the metal,

$$i(X) = j\,W\,X$$

and

$$d\,R = \frac{M}{T(X)}\,dX$$

Width of the trunk line is assumed to vary as

$$T_T(X) = K\,X^n$$

From these relationships, the resistive loss factor for the trunk is

$$F_{RT} = \frac{P_{RT}}{H\,W\,V_m\,j} \tag{46}$$

$$= \frac{j\,W\,M\,H^{(2-n)}}{V_m\,K^{(3-n)}}$$

The shadowing loss for the trunk is

$$P_{CT} = \int_0^H T(X)\,dx \tag{47}$$

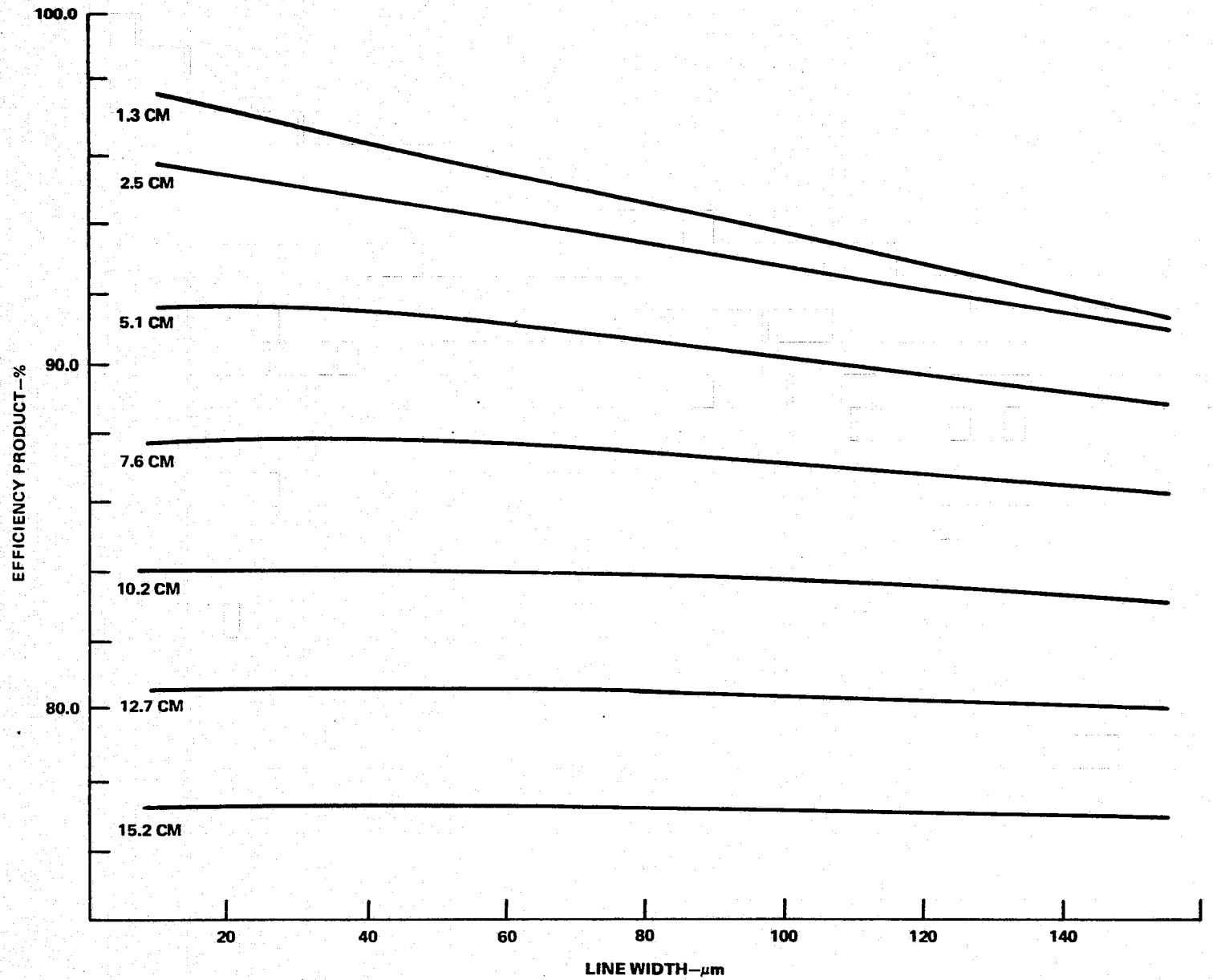


Figure 27. Efficiency Product for Metal Coverage and Series Resistance vs. Metal Finger Width as a Function of Cell Width for Rectangular Cells, Excluding Trunk Losses

and the shadowing loss factor is

$$F_{CT} = \frac{P_{CT}}{HW} \tag{48}$$

$$= \frac{K H^n}{W^{(n+1)}}$$

The sum of these losses is minimum for

$$K^2 = \frac{n+1}{3-n} \frac{H^{(2-n)}}{H^n} W^2 \frac{jM}{V_m}$$

So that

$$F_{RT} = F_{CT} = \frac{H}{\sqrt{(n+1)(3-n)}} \sqrt{\frac{jM}{V_m}} \tag{49}$$

These loss factors will have their lowest value for n = 1 (i.e., a linear taper). In this case

$$F_{RT} = F_{CT} = \frac{H}{2} \sqrt{\frac{jM}{V_m}} \tag{50}$$

The trunk loss factor ($F_{RT} - F_{CT}$) is plotted in Figure 28 as a function of cell length, H.

In terms of the efficiency product, E_P (Figure 27) for diffused region and finger losses of the cell and the loss factor for the trunk ($F_{RT} = F_{CT}$), the overall efficiency product E_{PT} for the rectangular cell is

$$E_{PT} = E_P - 2 F_{RT} (100) \tag{51}$$

5. Improved Designs

Several alternate metallization pattern designs can be used to improve the efficiency product of rectangular solar cells, providing that the array bonding is compatible. Two examples are discussed below.

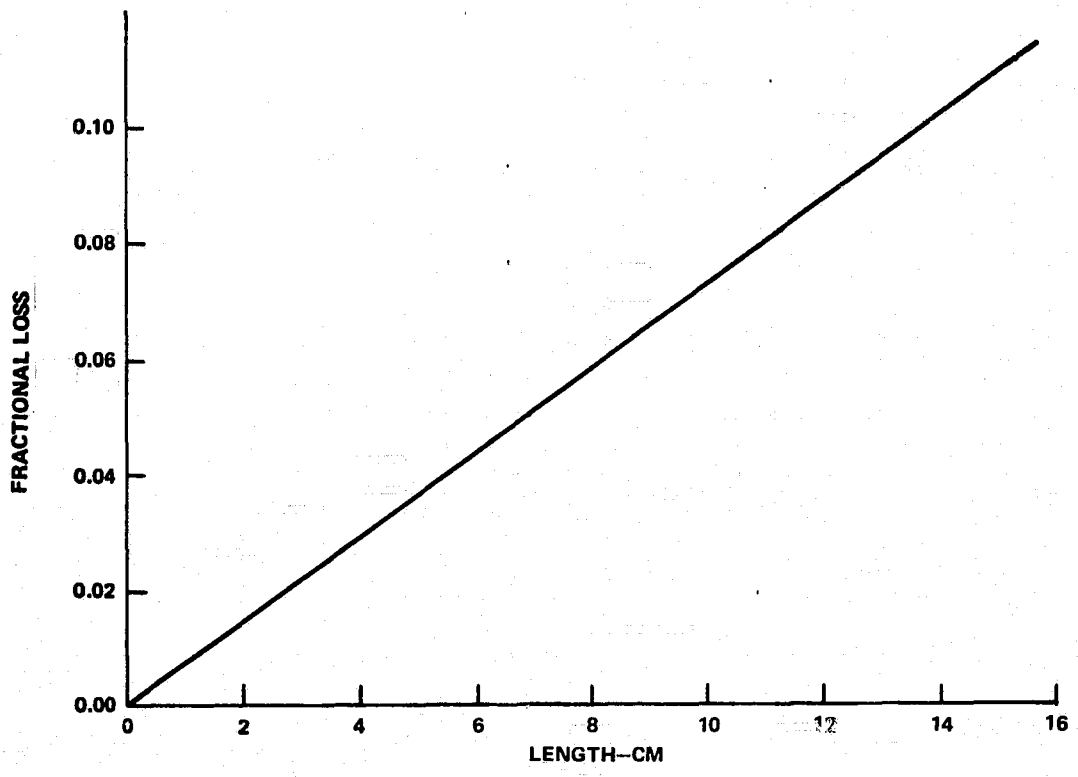


Figure 28. Fractional Trunk Loss due to Resistance or Shadowing as a Function of Length for Rectangular Cell

1) For a wide rectangle, the efficiency product is lower than for a narrow rectangle. From Figure 27, a 15.2-cm wide rectangular cell with 100-μm finger widths has an efficiency product of 0.772, while a 7.6-cm wide rectangle with 100-μm finger widths has an efficiency product of 0.872. By using the rectangular fishbone pattern shown in Figure 26(b), one can achieve the effect of two comb patterns back-to-back and thus achieve the higher efficiency product of the half width cell, 0.872, on the full 15.2 cm width. Of course, one could use two comb patterns front-to-front if it was desirable to keep the bonding areas on the cell edges.

2) For a long rectangle, the trunk line losses can become excessive. If one imagines two rectangular comb patterns end-to-end, we arrive at the rectangular bow-tie pattern shown in Figure 26(c). Now the effective length of a cell is one half the total length and the trunk losses are similarly halved, yielding higher efficiency for the bow-tie pattern.

In a fashion similar to the above examples, the basic patterns can be iterated on wide or long rectangles to achieve the effect of higher efficiency small rectangles. It must be kept in mind however that each subcell unit must be attached to the outside world to achieve large arrays, and in practice, the number of subcell iterations that can be used will depend on the allowed interconnect scheme.

As a general rule for large-area rectangular solar cells, the fishbone pattern will be the most efficient configuration when one bonding site is allowed and a bow-tie-fishbone (two fishbone patterns head-to-head) will be the most efficient configuration when two bonding sites are allowed. A brief study of Figure 26 will show that many more variations of the basic comb pattern are possible.

The structures described were selected as practical configurations for fabrication of cells and arrays. There may be other design variations which give higher efficiencies, e.g., the width of a finger might be decreased with distance from a trunk line. A specific example is calculated here to illustrate the potential improvement and limitations of tapered fingers.

A rectangular cell segment of width, W and spacing, S, is illustrated in Figure 29. The current as a function of distance, Z, along the finger is

$$i(Z) = j S Z \tag{52}$$

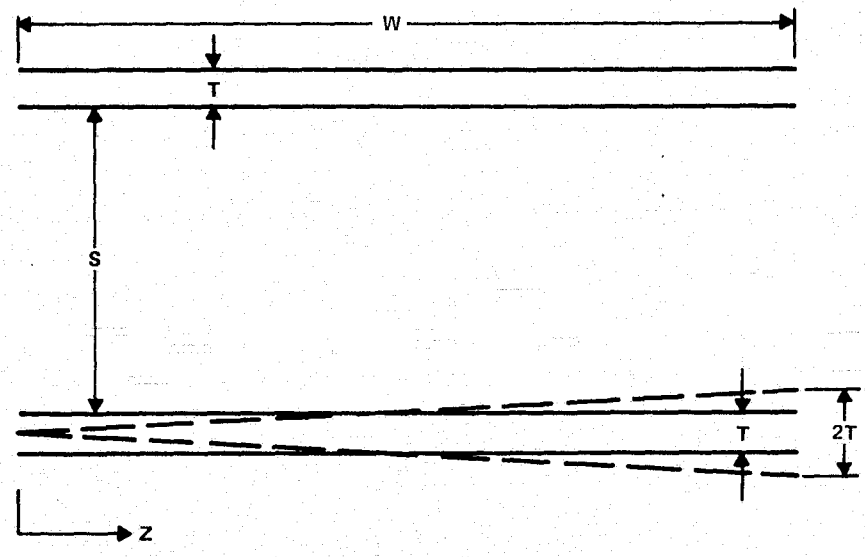


Figure 29. Cell Segment for Comparison of Constant-Width and Tapered Fingers

A triangular shaped finger having the same area is shown by the dotted line. Width of the end connected to the trunk is 2T and thickness as a function of distance from the small end is

$$T(Z) = \frac{2T}{W} Z$$

For the tapered finger, the resistive power loss is

$$P_F' = \frac{j^2 M S^2 W^3}{4T} \tag{53}$$

The resistive finger loss is reduced 25% by tapering the fingers, without changing metal coverage loss or diffused region resistive loss. However, in practice, photolithographic processes would be required to fabricate the triangular shaped fingers due to the fine geometry incurred at the narrow end of the finger.

6. Conclusion

Computer analysis of solar cell front surface metallization design equations provides a powerful tool for optimization of process alternatives. Significant comparisons can be made without resorting to the time consuming and costly process of cell fabrication. Optimum efficiency as a function of metal line width and cell diameter can be predicted.

Equally important, a quantitative assessment can be made of the impact of various process technology choices. This quantitative assessment is a key factor in the evaluation of alternatives for low-cost high-efficiency solar cell fabrication.

While this calculation covers only a hexagonal and rectangular solar cells, it can be extended to cover other pattern geometries and other cell geometries. The quantitative assessment of competing geometries can be used to identify the optimum pattern geometry that matches a given cell geometry.

Finally, a fractional loss calculation can be used as one of the parameters in establishing the maximum practical sheet area for various large area silicon sheet processes.

E. SILICON SHEET CONSIDERATIONS

The choice of a low-cost silicon solar cell process for a 1985 high-volume production goal is dependent on a number of factors. One important factor, silicon sheet form and quality, is not covered in depth in this study. A few comments on the impact of silicon sheet form and quality are in order at this point.

1. Shape

Semiconductor industry experience is based on round single crystal silicon wafers. Existing mechanical handling equipment is designed to operate with round wafers. Simple geometric shapes other than round, e.g., hexagons, squares, and rectangles, can be accommodated by straightforward mechanical redesign. Caution must be observed to prevent breakage at the pointed corners. Process techniques, such as spin-on coating, can be adapted using spray, dip, or screen-on techniques, as appropriate. Long continuous ribbons of silicon will present much more complex problems if processing is envisioned as a continuous process. Although many semiconductor processes can be adapted to continuous processing, it is not practical to fabricate very large-area solar cells. Solar cells are high-current, low-voltage power supplies and if solar cells become too large, the I^2R power losses become excessive. Therefore at this time, it is envisioned that continuous ribbons of silicon would be cut into rectangles for processing.

2. Crystallinity

Silicon sheet can be obtained in different degrees of crystallinity. For purposes of this discussion, three forms are considered: single-crystal, two-dimensional polycrystalline and three-dimensional polycrystalline silicon sheet material. Amorphous silicon will not be included at this time. The behavior of single-crystal silicon is well known and all other things, e.g., cost, performance, etc., being equal, this is the material of choice. Within the realm of polycrystalline material, one can distinguish between two-dimensional polycrystalline material where the typical crystal dimension in the vertical (front to back) direction is greater than the sheet thickness, therefore, grain boundaries exist primarily in the vertical direction and three-dimensional polycrystalline material where the typical crystal dimension is less than the sheet thickness and grain boundaries exist in all dimensions.

Processes that are accelerated along grain boundaries, such as impurity diffusion, will have to be modified for use with polycrystalline silicon sheet. For example, in the case of impurity introduction, ion implantation would undoubtedly be more desirable than standard diffusion techniques. Front and backside contact techniques would also have to be altered to accommodate polycrystalline material.

Two dimensional polycrystalline silicon sheet has been shown to yield solar cells of reasonable efficiency, $\approx$ 10%, and must be considered as a viable alternate for solar cell applications. Three-dimensional polycrystalline silicon sheet is still in the speculative stage at this time.

Silicon sheet in the form of polycrystalline silicon on a substrate is not considered a viable alternate at this time. Access to the back side for back-side contact imposes added process complexity and cost that does not appear to be performance cost effective in the near future. No further consideration of this form of silicon sheet is planned at this time.

3. Surface

Although most of the existing solar cell technology has been developed on chemically polished surfaces, surface roughness is not envisioned as a problem area. Low-cost solar cell processes will probably utilize junction formation technologies and thick-film metallization technologies, e.g., screen print or electroless plate, that are very tolerant of surface irregularities. A preferred surface on ⟨100⟩ single-crystal silicon sheet is a texture etched surface that has chemically formed surface pyramids of approximately 5-μm height. Highly polished surfaces are undesirable because of their loss of incident light by reflection.

Processing techniques must be optimized if textured or roughened surfaces are used. The main cause for concern is mechanical damage such as chipping on the wafer surface.

4. Thickness

Silicon sheet thickness will impact solar cell cost and performance. Cost will be directly impacted by the quantity of silicon used per unit area. The more silicon volume that is used, the more raw silicon cost that must be included.

Balanced against raw silicon cost will be solar cell performance and wafer processing yield. Thicknesses below 250 μm appear to exert a negative effect on cell efficiency. A quantitative relationship is not available. Semiconductor manufacturing experience indicates that with increasing wafer size, thicker wafers are required to minimize wafer warpage and breakage. The breakage is related to mechanical handling and to a degree can be controlled by proper design of automated handling equipment. Warpage may be more of an intrinsic problem that may impose a lower limit on wafer thickness. This will be a factor of silicon sheet formation technology and absolute limits cannot be predicted at this time.

F. SOLAR CELL PROCESS STEPS

The manufacture of silicon solar cells involves a number of process operations or steps. The choice of a preferred process will be dependent on many factors. The key factors used in this analysis are process step cost, ultimate cost potential, ease of automation, technical feasibility, and process compatibility. A number of process step alternatives have been evaluated. The process step alternatives have been grouped into surface preparation and cleaning, junction formation, metallization and optical coating groups for comparison and evaluation. Each group is discussed below. Costing is discussed in the following section.

1. Surface Preparation and Cleaning

Masking operations have been downgraded as nonproductive and costly operations. Photoresists are material intensive and other methods can be used to define patterns. Mask stencils are costly and can only be used in a low-cost process if no buildup or deposit accumulates. Mask stencil cleaning is too expensive. Mask stencils might be useful in plasma etching operations.

Surface cleaning techniques can be divided into chemical and mechanical. The chemical cleaning techniques can be subdivided into water based (including acids and bases), organic solvent based and gaseous (plasma). Water-based cleaning techniques are best suited for the removal of inorganic residues, such as metals, metallic ions, and water soluble anions. Organic solvent-based cleaning techniques are best suited for removal of organic residues, such as waxes, greases and polymeric materials. In general, organic solvents do not remove inorganic residues. Gaseous cleaning techniques, such as oxygen plasma and reverse sputtering are excellent for removing organic residues that do not leave ash residues (inorganic oxides). Plasma cleaning is easily automated and has a low-cost potential.

Mechanical cleaning is particularly suited to removal of particulate matter and is easily automated. Ultrasonic agitation can be used to augment any of the chemical cleaning techniques.

The ideal process would require no cleaning operations at all. However, in the real world, cleaning will be required and the choice of a cleaning process will depend on the type of contaminant to be removed.

Surface texturing can have a beneficial effect on solar cell performance. Textured surfaces produced on ⟨100⟩ silicon surfaces substantially reduce light reflection and improve metal adhesion. Two methods are known to produce uniform texture on ⟨100⟩ silicon surfaces, NaOH and hydrazine etching. The NaOH technique is preferred on the basis of lower material cost, ease of control and safer conventional chemical handling. On sawed single-crystal material, the NaOH etch can be used

both for removal of surface damage and texture etching. Feasibility evaluation at Texas Instruments has shown that this combined damage removal and texture etching is possible. With a suitable choice of processing conditions, it is also feasible to polish one side of a wafer while texturing the other side. The process includes an acetic acid rinse so that no subsequent cleaning operation is necessary.

2. Junction Formation

The characteristics of the front-side (collecting) junction are very critical in the fabrication of high-efficiency solar cells. Sheet resistance, surface concentration, juntion depth and diode characteristics must be carefully controlled to achieve optimum performance. The minority carrier lifetime of the base region should not be degraded during the junction formation process. A back-side contact region and back surface field are also required.

An ideal process for the N^+PP^+ solar cell structure would introduce both N^+ and P^+ regions at the same time and leave no detrimental surface residue. Two processes approach this ideal: ion implantation and polymer dopant technologies. Both allow the introduction of opposite conductivity type impurities on opposing wafer faces and simultaneous thermal treatment (diffusion). Both offer good control of sheet resistivity, surface concentration and junction depth. Although diode characteristic data and base minority carrier lifetime data are not complete at this time, both processes are excellent candidates for a solar cell process. Ion implantation would probably be preferred for polycrystalline material due to the lower temperature thermal treatment and probable smaller effect at grain boundaries. On the basis of projected cost, we favor polymer dopant at this time.

Open-tube diffusion using a gaseous source, e.g., $POCl_3$ or PH_3, has been used to make solar cells for many years. Excellent results have been achieved. The primary disadvantage of this technique is that the gaseous diffusion source dopes all exposed surfaces with one conductivity type impurity. Separate steps with attendant masking are required to produce both the N^+ and P^+ regions. Operations such as depositing and alloying Al through the N^+ diffusion on the back side have been used. The extra processing steps make this technique a poor third choice.

Other technologies such as epitaxy, alloying, doped oxides, and solid source diffusion do not offer good enough control or low enough cost to merit further study for this application.

3. Metallization

The front-side contact metallization plays an important role in the collection and transmission of photo-generated current in solar cells. Metal resistivity, thickness, adhesion, contact resistivity and bondability must be carefully controlled to achieve optimum performance.

Metallization technologies can be broadly categorized into two groups, vacuum and nonvacuum processes. The vacuum processes include evaporation and sputtering technologies. Vacuum deposition of metal is wasteful of material since not all of the evaporant stream can be directed onto the substrate and on the front side only a small portion, <5%, of the metal that condenses on the surface is used in the metallization pattern. Vacuum equipment is costly, difficult to maintain and throughput is low. Very good metal properties can be attained with the exception of metal thickness. Thickness buildup can be achieved with a subsequent plating or solder coating operation. Vacuum deposition through a mask stencil is preferred, to avoid the extra processing steps involved in photomask and etching operations. The problem of mask cleaning and fixturing remains, however. Although vacuum deposition has been used to fabricate solar cells for many years and the metal properties are good, vacuum deposition is not a preferred choice for a low-cost process.

Among nonvacuum metallization processes, two candidates appear most promising, thick-film screen printed metallization and electroless plating of metals. Both of these technologies have considerable industry experience but not in the application on silicon solar cells.

Thick-film screen printed metallization has been used extensively in the metallization of ceramics. The majority of commercial pastes or inks contain precious metals, Au, Pt, Pd or Ag and are fired at high temperatures, >800°C in air. The pastes also contain significant amounts of glass frit, 5 - 15%, whose function is to promote bonding to a ceramic substrate. Experimental pastes are becoming available that contain base metals, Cu, Ni, and Al. The screened printing process prints a paste pattern on the substrate through a mask stencil (screen). Little or no paste is wasted since the paste that is left on the screen can be used on subsequent substrates. Patterns as narrow as 100 μm can be printed. The glass frit found in commercial pastes presents a problem in contact printing on silicon. The glass is not conductive and can inhibit contact to the silicon solar cell. The high firing temperatures used with commercial pastes are not readily compatible with solar cell processing. Screen printed metal is typically 15 to 25 μm thick and does not require subsequent plating or solder dipping to improve conductivity.

Experimental work at Texas Instruments on this contract with Cu and Ni inks demonstrated that these commercial pastes show promise but are not ready for implementation in a manufacturing process. The commercial Cu paste alloyed into the silicon surface and penetrated the shallow N^+P junction on the front side of the solar cell. Commercial Ni paste could be fired on solar cells without shorting the junction.

This technology holds much promise as a low-cost readily automated metallization technology for silicon solar cells and should be pursued as a development program. Silicon solar cells are being fabricated using specially formulated Ag pastes.[3]

Electroless plating of nonprecious metals is the alternate metallization technology of choice. Electroless Ni plating has been used for many years in the semiconductor industry on deep junction devices. Typical Ni plates contain significant amounts of P or B depending on the plating solution. The plated metal must be sintered to enhance contact resistivity and adhesion.

Unless the metal plate can be patterned as part of the plating operation, masking techniques must be used. The requirement for separate masking would be a serious cost impediment in the incorporation of electroless plating into a low-cost silicon solar cell process. A low-cost patterning process that did not add material cost would be very desirable.

A patterned electroless plating process called PIMDEP, photo impeded metal deposition, has been used on plastic and ceramic substrates. The process uses a sensitizer, $SnCl_2$, that can be desensitized by light, followed by an activator, $PdCl_2$, that activates the nonexposed regions, followed by electroless plating. A photomask is required to expose the sensitizer but the photomask is not consumed and does not accumulate deposits that require subsequent removal. The process has been used to form patterns on Kapton, a polyimide plastic, and ceramics. Pattern geometries as small as 100 μm have been plated. The process has not been demonstrated on silicon devices but there does not seem to be any inherent reason why it would not work on silicon solar cells. The sensitizer and activator steps are also required in conventional electroless plating so these operations do not add significant extraneous cost elements. The PIMDEP process offers the most attractive approach to electroless plated contact metallization.

The problem of making reproducible ohmic contact to shallow junction devices remains a question for electroless plated metals, as it does for all metallization schemes. The shallow front junction, required for efficient collection of photons, presents a delicate structure for low resistivity ohmic contacts. The problem should be solvable and electroless plating, particularly the PIMDEP process, is a good candidate process element for a low-cost silicon solar cell process.

In summary, vacuum metallization processes, while technically good, are not attractive process elements for a low-cost solar cell process. Thick-film screen printed metallization and electroless metal plating, PIMDEP, are good choices for a low-cost process. Significant further development is needed for each of these nonvacuum metallization options.

4. Optical Coating

The optical coating on the front of a silicon solar cell plays an important role in efficiency at which a cell will operate by reducing reflection losses and providing a degree of surface passivation. Since reflection is a function of surface smoothness, roughened or textured surfaces reduce the requirement for good optical matching in the antireflection coating. A good optical coating should provide refractive index matching between the silicon surface and air, have very low absorption (high transmittance) and provide surface passivation for the silicon solar cell.

Several materials have been used in the solar cell industry, evaporated silicon monoxide, tantalum pentoxide and silicon oxide-titanium oxide mixtures. Silicon nitride represents another good optical material. Optical films can be applied by evaporation, sputtering, spin-on or spray-on techniques. Assuming good control of the basic material properties, the key parameter is optical thickness control. Thickness control provides an optimum response at a predetermined wave length with less than optimum response at other wavelengths in the spectrum. Since a terrestrial (or space) solar cell will be operated over a broad spectrum, very tight control over the thickness is not required. Slight deviations in thickness will only shift the point in the spectrum where maximum response occurs. All of the above optical coating techniques are acceptable. Low-temperature silicon nitride deposition and spin-on or spray-on techniques for silicon oxide-titanium oxide films offer the most favorable approaches to an automated process.

For use on rough or textured surfaces, the spin-on or spray-on approach or the low-temperature silicon nitride processes are the most favored. Vacuum techniques could suffer from shadowing if surface roughness interferes with line-of-sight deposition.

5. Interconnection

Metal-to-metal bonding, soldering, welding or ultrasonic bonding offer the most attractive approaches to cell interconnection. Thermal compression bonding requires high pressure per unit bond area and is not considered a viable candidate. Conductive epoxies can introduce series resistance and have not demonstrated long life history. Conductive epoxies are not considered as viable candidates.

Since interconnect of cells is such a key area of module fabrication, it is discussed under module fabrication in a subsequent section of this report.

6. Encapsulation

The main purpose of solar cell encapsulation is to protect the cell and interconnect system from environmental hazards. Data collected in Task 3 of the LSSA Project indicates that plastic encapsulants provide only partial protection from the environment. Complete protection can be provided only by using impermeable encapsulants. Plastics are also expensive and thick layers of plastic required for environmental protection add significantly to module cost.

Glass provides a reasonable cost nonpermeable cover for solar cell modules. The substrate must also be low-cost and provide environmental protection. Several materials have been proposed bot porcelainized steel appears to offer the best balance of cost and material properties.

A more complete discussion of a long life module is found in the discussion of module fabrication.

7. Test

A discussion of final testing of completed solar cells and solar cell modules is found in the section on Solar Cell Testing. Test requirements and a proposed design for test equipment is included.

In-line testing as a process control technique is another aspect of testing. The function of in-line testing is to provide rapid feedback for process control and early detection of possible reject material. The process control function is related to each process step and provides the positive control necessary to optimize each operation. The frequency and extent of the testing must be balanced against the need and cost. For example, if diffused layer resistivity is routinely controlled to ± 10% and the sensitivity analysis shows that diffused layer resistivity does not significantly impact cell efficiency until the variation exceeds ± 30% of nominal value, then frequent in-line testing of diffused layer resistivity is a nonaffordable luxury. If, on the other hand, ± 10% of nominal value is the limit before cell efficiency is impacted, then in-line testing is a necessity.

By definition, a well controlled process will have reproducible process variations and in-line testing will only be required at a few key points in the process. These key points have not been defined for solar cell processes at this time. A sensitivity analysis is the next logical step in the definition of a well controlled automated solar cell process. In-line test costs must be very low so that they do not adversely affect manufacturing cost.

8. Process Uniformity

Two lots (AAAP-16 and 17) of 7.6-cm hexagonal solar cells, 25 slices per lot, were processed using our standard open-tube P diffusion process with sintered Al for back-side contact. These N^+PP^+ cells have Ti-Pd-Ag front-side metallization and were laser scribed into hexagons after processing. Parameter uniformity was very good within a lot and between lots. A total of 45 cells out of 50 slice starts was achieved. At AM0, $I_{SC} = 1.0 \pm 0.1$ ampere and $V_{SC} = 0.59 \pm 0.02$ V. Figures 30 and 31 give the total distribution of I_{SC} and V_{OC} for these lots. The overall yield of 90% is probably greater than one would expect in a production facility but it is indicative of the good process and test yields that might be expected from a properly controlled solar cell process. These cells were used for experiments on module assembly.

G. SOLAR CELL TESTING

A key link in the manufacture of low-cost solar cells is the final test procedure for cells and for modules. Testing rates must be compatible with overall factory throughput rates to minimize costs. Testing should have a low labor content and a reasonable capital cost.

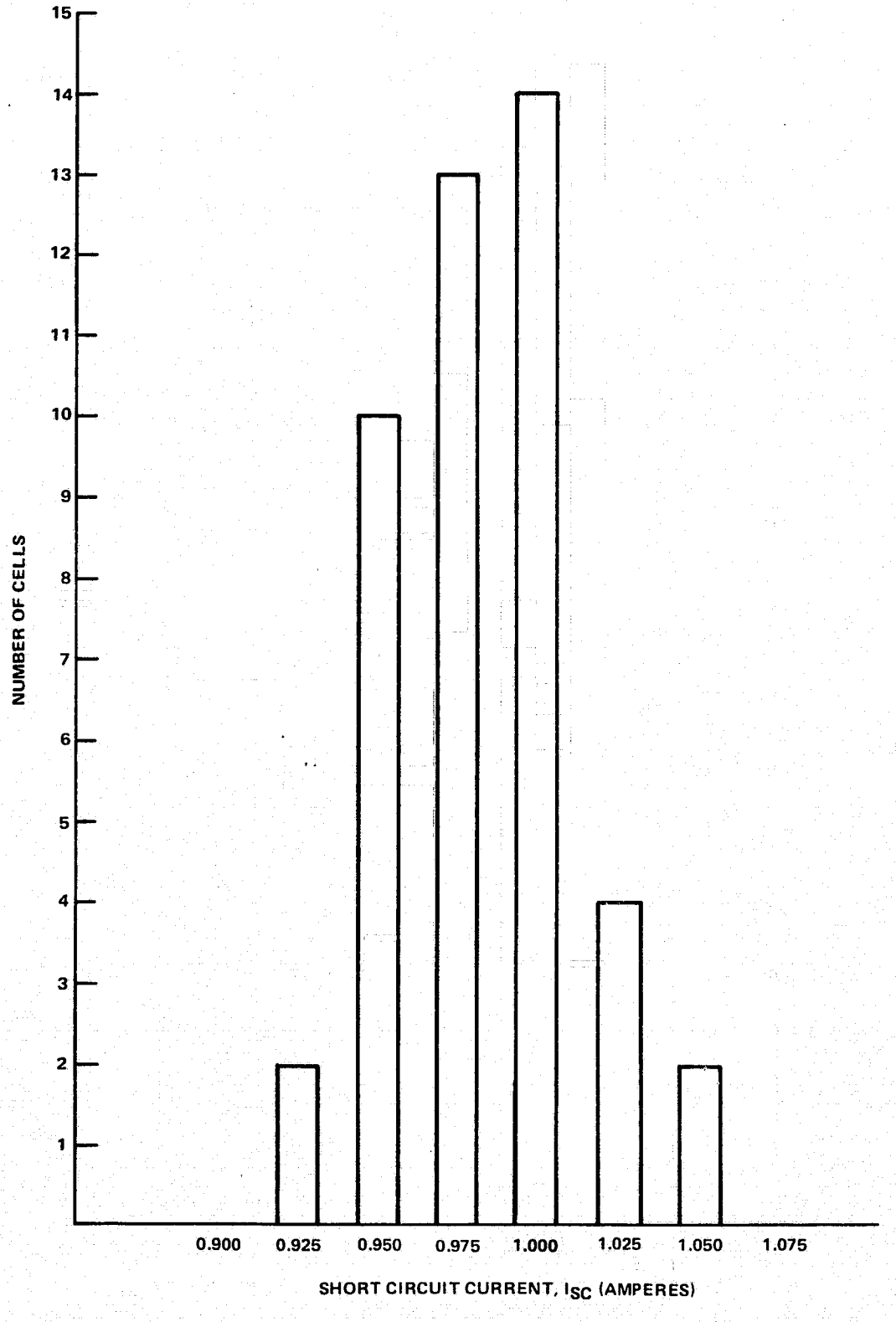


Figure 30. Distribution of Solar Cell Lots AAAP-16 and AAAP-17 as a Function of I_{SC}

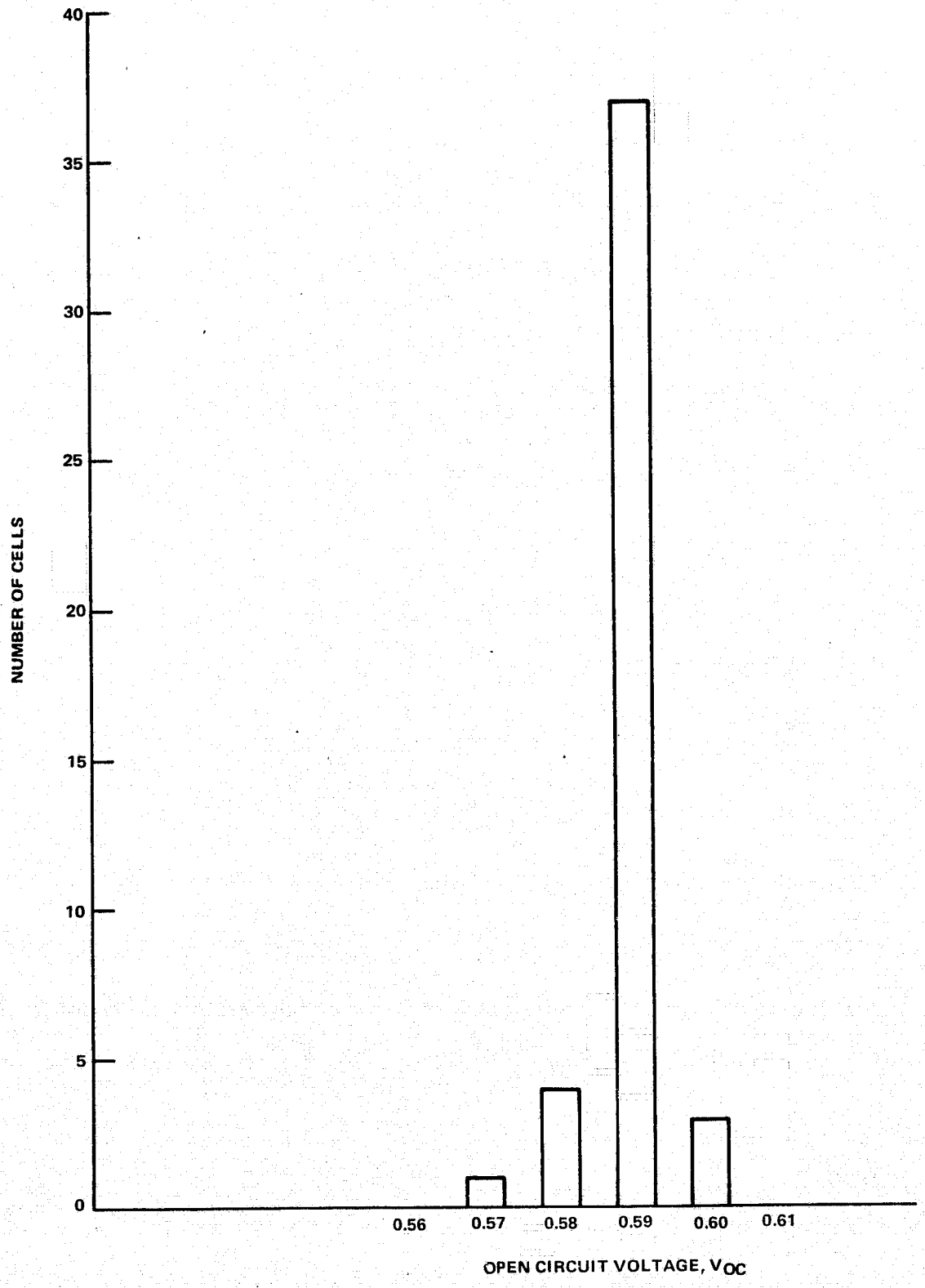


Figure 31. Distribution of Solar Cell Lots AAAP-16 and AAAP-17 as a Function of V_{OC}

A conceptual design of a solar cell test station for a unit factory has been developed. By definition, a unit factory will have an annual output of 3-6 MW (peak power) with a target output of 5 MW. Testing will be done on an individual cell basis to provide "good" cells for module fabrication. A second different test station will be required for module testing.

The solar cell test station is designed to accommodate the parameters in Table 7. All of the specific tests that will be required are not defined at this time but the test station must be versatile enough to accommodate any anticipated electrical tests. Table 8 lists the key known electrical tests, forward and reverse diode characteristics and illuminated I-V characteristics. Two versions of the test station are conceived, the basic version that assumes good process control and tight parameter control so that all good cells are grouped together in one category and a refined version that assumes good cells will be produced with a spread of usable outputs and this distribution of good cells must be grouped into bins of matched cells. The refined test station will require extra unload stations to correspond to the number of good categories or bins and the ability to sort "good-1," "good-2," etc., solar cells.

Table 7. Solar Cell Test Station Parameters

Cell Dimension	12 cm or 10 cm
Shape	Hexagon, round, or rectangle
Positioning in θ	Mechanical index from the flat edge (hexagon, rectangle or round with a flat) – Automatic optical alignment if no flat
Illumination	AM1 (100 mW/cm^2)
Temperature	Room (nominal 25°C)
Electrical Output	V_{OC} – 0.6 V I_{SC} – 2.5 A V_M – I_M 0.5 V, 2.0 A
Throughput	Nominal 1000/hour
Work Year	8400 hour
Down Time	20%
Yield	85%

Table 8. Solar Cell Tests

Dark	
Forward voltage	0.4 – 0.7 V @ 2 A
Reverse voltage	< 10 mA @ 1 V
Illuminated (AM1)	
I-V	Measure several points on I-V curve and software to calculate equation of curve, fill factor, maximum power, etc.

As a basic working premise, the basic test machine is the more desirable choice. The advantages are obvious, lower cost, a simple single "good cell" inventory and reduced record keeping. Module fabrication is also simplified if a tightly controlled cell inventory is available. In a well controlled process, it should be possible to maintain a high yield of a reproducible narrow distribution product. Therefore one of the goals of process and equipment development should be achievement of this well-controlled process using uniform silicon sheet material.

The test rate or throughput in Table 7 is based on the assumption that the factory output will be solar cells with a nominal 1-watt output per cell, with an electrical test yield of 85% and a utilization factor of 80%. Thus, at a throughput rate of 1000 cells per hour, the annual output of good tested cells would be (1000 cells/hour) X (8400 hours/year) X 0.80 X 0.85 = 5,712,000 good cells.

The basic solar cell test machine must contain the following stations in sequence, load, orient, test, sort/unload. To meet the 1000 cells tested per hour throughput rate, the machine must handle and test each cell in 3.6 seconds. Evaluation of the mechanical handling and test requirements indicates that a multitrack approach is the most desirable.

Figure 32 is a schematic of a four-track machine with provision for a single unload-good station. The machine would be fed from a four-carrier carousel using a standard "common carrier" cell holder. The common carrier cell holder concept would be used in the unit factory to interface from one cell fabrication machine to the next where machine boundaries exist. If the machine were built in modular stations which could be bolted together, extra unload stations could be added for sorting good cells into matched categories. Also, an extra load station could be added on the front so that the carousel change would not have to occur at a specific time.

The machine operation would be in a series-parallel-series mode where the cells would advance into the load station in a series fashion loading tracks 1, 2, 3, and 4. Then in a parallel fashion, all four tracks would adrance to the orient station to orient the cells to the test head in the next station. During the orient period, the load station would reload tracks 1 through 4. Depending on the availability of a mechanical asymmetry in the cell, mechanical and/or optical means would be used to position the contact pads on the cell for test. In a parallel fashion, all four tracks transfer to the test station. The test station would be computer controlled for test sequencing and pass/fail. After test, all four tracks would advance to the unload-good or unload-bad station. Then in a series fashion, tracks 4 through 1 would unload into another common carrier carousel. A timing diagram is shown in Figure 33.

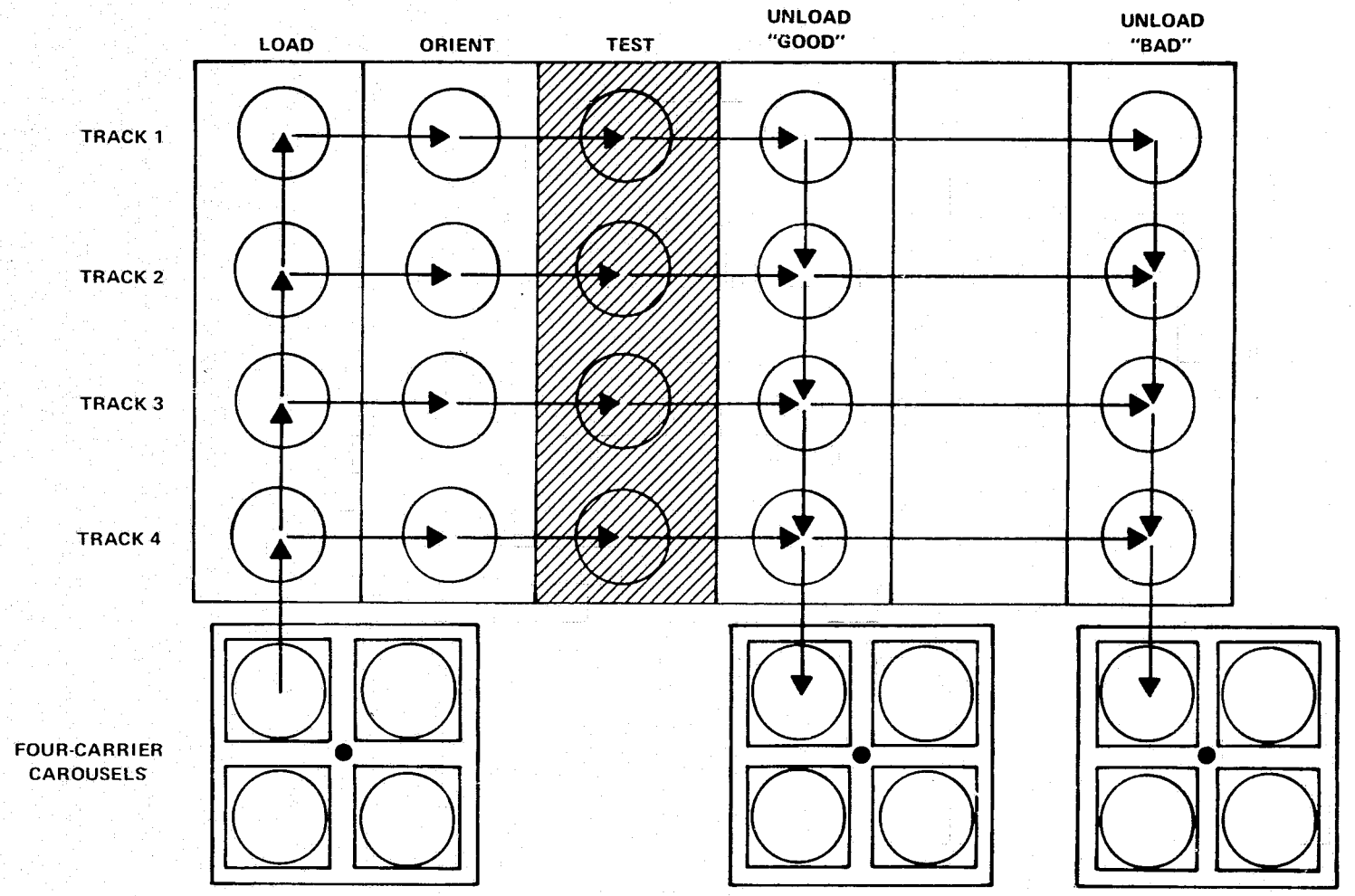


Figure 32. Solar Cell Test Machine

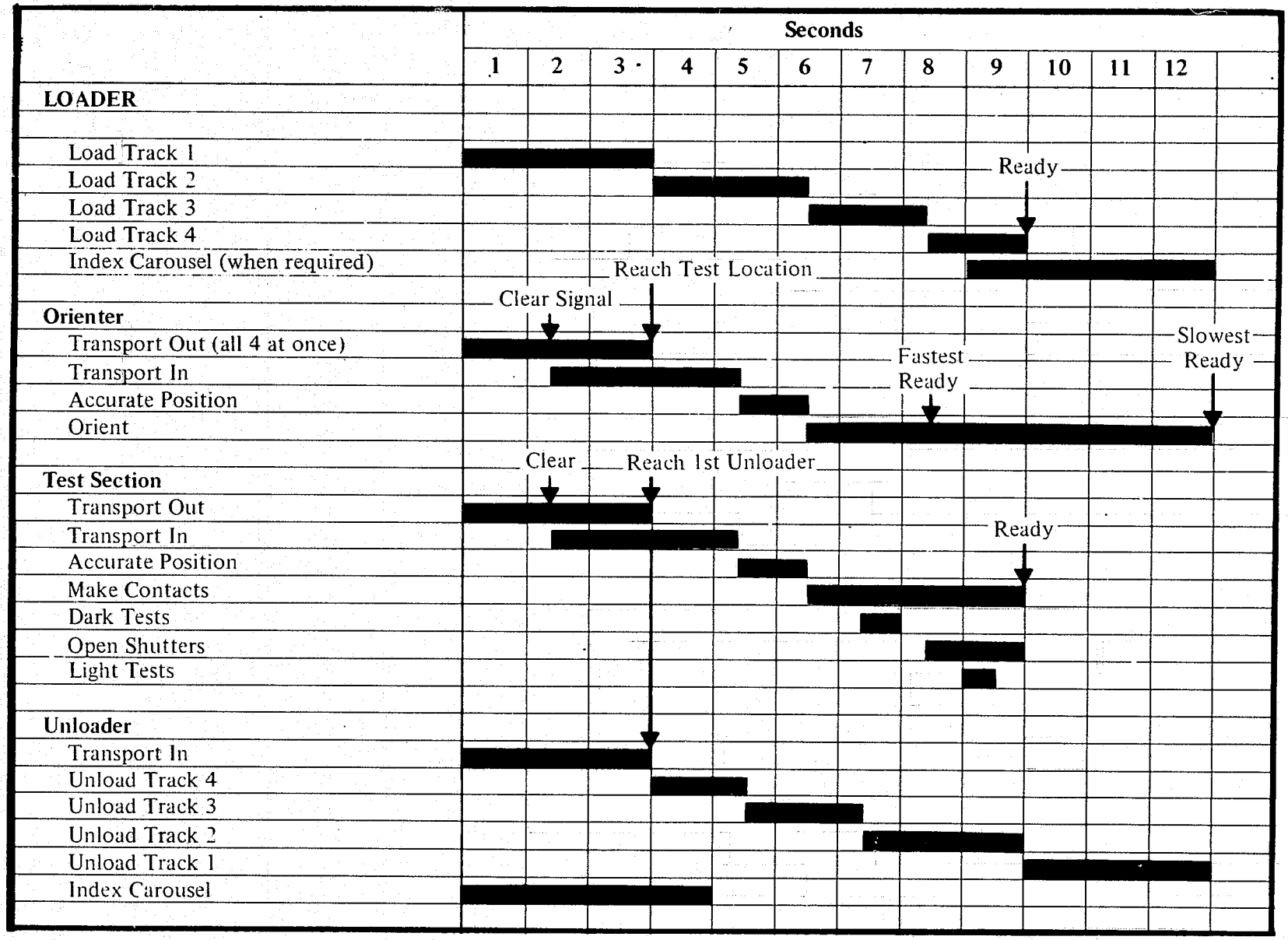


Figure 33. Solar Cell Tester – Timing Diagram

The test station, orient station, and unload stations would be controlled from a central computer or a remote minicomputer. The software in the control system would use curve fitting programs to determine the critical dark and illuminated parameters of the tested solar cells. Critical parameters such as shunt resistance, I_{SC}, V_{OC}, maximum power, voltage and current, and series resistance would be stored in memory and used as process control data to keep the fabrication process in control. This data could be displayed on a CRT or printed in hard copy. Figure 34 is an artist's rendition of a solar cell test machine with a control console at the test site. After design and after production begins, a test machine of this type is estimated to cost $100K-150K.

H. PHOTOVOLTAIC MODULE TESTING

Testing rates for a photovoltaic module test machine are dependent on the size of the module and the number of unit factories (nominal 5 MW/year output) served. A module tester for a single unit factory producing a standard 20 W module would have to test at a rate of 40 panels per hour. Test rates in this range are readily handled by single track testing. A test and mechanical handling time schedule for a photovoltaic module tester is shown in Table 9. The test rate derived from this time schedule is $\approx$ 200 modules/hour. A module tester with this capability would service 4 or 5 unit factories or operate on a one-shift rather than three-shift schedule.

The design of a module tester would be similar in concept to a solar cell tester, incorporating load, lock and contact, test, and unload-good – unload-bad stations. The module test machine would be larger than the cell test machine but software and control requirements would be similar. Estimated machine costs would be $\approx$ $100K each after development.

The main area of concern in the design of a module tester would be the availability of a large area, uniform AM1 illumination source. The module area is likely to be in the range 0.25 to 1.0 m^2. One possible solution is the adaptation of photographic enlargement equipment. No further development of the module test machine is planned in this phase of the program.

I. AUTOMATED MODULE FABRICATION

In order to evaluate potential high-volume module fabrication costs, four module configurations have been evaluated. Three of the module configurations feature very low-cost nonhermetic structures and the fourth is a "hermetic" structure that has a very high probability of meeting or exceeding the 20-year life goal.

The three low-cost nonhermetic structures use plastic encapsulants or sealants. The expected lifetime and barrier properties of the plastic encapsulants or sealants cannot be predicted with high degree of accuracy at this time. It is expected that the studies in Task III of the LSSA project will answer these questions.

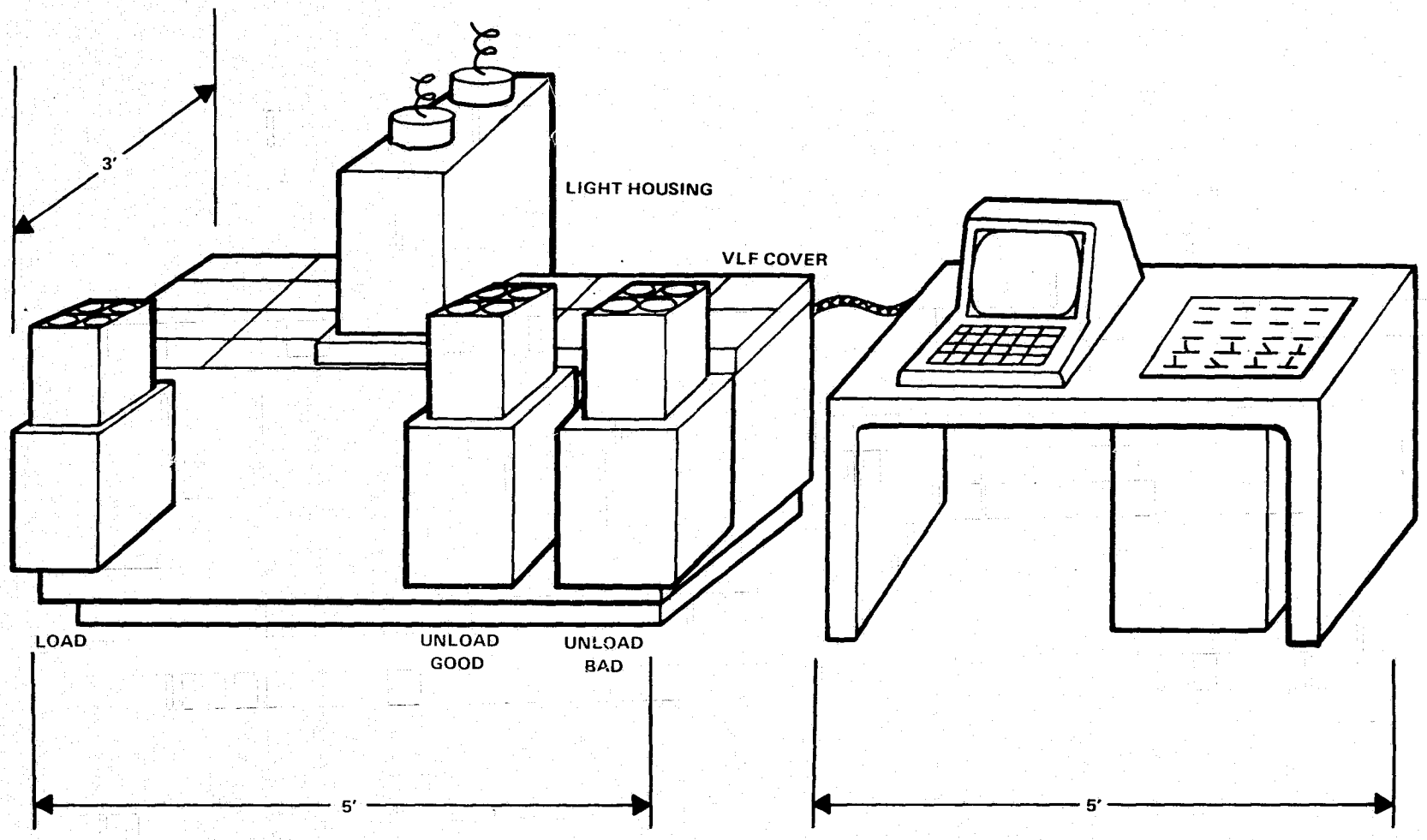


Figure 34. Artist's Rendition of Solar Cell Test Machine and Control Console

Table 9. Photovoltaic Module Test and Handling Time Schedule

Load module onto test tray		5 seconds
Lock and contact		2 seconds
Open shutter, test, close shutter		3 seconds
Eject module		3 seconds
Unload tested module to shipping		5 seconds
	Total	18 seconds

The three structures are: (1) substrate with plastic overcoat, (2) substrate with rigid superstrate, and (3) superstrate with plastic undercoat. Options 1 and 2 were evaluated assuming both N^+ and P^+ contacts are on the back of the cell and can be simultaneously bonded to an interconnect pattern on the substrate. Option 3 assumes a tab or ribbon interconnect is used for electrical connection. Tables 10, 11, and 12 give the estimated material cost per m^2 of module and the labor, overhead (at 100% of labor) and depreciation cost per m^2 of module assuming a throughput rate of 2 m^2 per hour for options 1, 2, and 3. Also, included are capital equipment cost estimates for each option.

Table 10. Option 1 Cost and Capital

COST

Material	**$/m²**
Porcelainized Steel	2.93
Solder Paste	1.20
Encapsulant @ 0.04 mm	.37
Subtotal	**4.50**
Labor	1.75
Overhead	1.75
Depreciation	2.29
TOTAL	**10.31**

CAPITAL – PORCELAIN SUBSTRATE

	$K
Solder Screener	20
Magazine Unloader	10
Magazine	3
Cell Mounter	40
Fixture (holds cells in place)	10
Soldering Oven	20
Clean-up Hood	10
Encapsulate/Cure	40
TOTAL	**153**

Table 11. Option 2 Cost and Capital

COST

Material	$/m^2
Porcelainized Steel	2.93
Solder Paste	1.20
Gasket	0.11
Glass Cover – 32 mm	2.63
Subtotal	**6.87**
Labor	1.75
Overhead	1.75
Depreciation	2.29
TOTAL	**12.66**

CAPITAL – PORCELAIN-GLASS SANDWICH

	$K
Solder Screener	20
Magazine Unloader	10
Magazine	3
Cell Mounter	40
Fixture (holds cells in place)	10
Soldering Oven	20
Clean-up Hood	10
Gasket Applier	10
Glass Mounter	10
Cure Oven	20
TOTAL	**153**

For each of these options, the material cost was kept to a minimum value in an attempt to see if the \$10 per m^2 design-to-cost goal could possibly be projected. The lower cost plastics, not the best optical choices, were used. No judgment is or can be drawn at this time regarding the ability of any of these options to meet the 20-year life goal.

It appears that all three of these options have the potential to meet the cost objective when minimum cost and minimum amounts of material are used. While it is doubtful that minimum costs or amounts of material would be optimum, it is encouraging that preliminary costing is this favorable. Of these three options, Option 2 using a glass superstrate and a porcelainized steel substrate is the most attractive technically. Option 2 provides mechanical rigidity, a cleanable hard surface and some protection from mechanical abrasion. Protection from ambient atmosphere is dependent on a plastic adhesive gasket-seal between the glass and the porcelainized steel. In all likelihood this adhesive seal would be the module weak point.

Table 12. Option 3 Cost and Capital

COST

Material	**$/m²**
Precoated 3.2 mm Glass	3.50
Tabs	1.77
Aluminum wire 0.25 mm dia.	1.24
Encapsulant	0.06
Subtotal	**6.57**
Labor	1.75
Overhead	1.75
Depreciation	2.42
TOTAL	**12.49**

CAPITAL – GLASS SUPERSTRATE

	$K
Magazine Unloader	10
Magazines	3
Tab Applier	25
Tab Bonder	15
Cell Mounter	40
Curing Oven	10
Wire Bonder	40
Encapsulate/Cure	20
TOTAL	**163**

1. LSSA Module

The fourth configuration studied was the "hermetic" module. Because of the high probability that this option could meet the 20-year life goal a more detailed analysis was performed. The major objective for initial design of this module was to obtain lowest cost per exposed m^2 of silicon. The second objective was to have a design which would be suitable for large-scale, high-speed manufacturing, and the third objective was to have a module with long projected lifetime.

The first objective can be achieved by selecting low cost materials and by maximizing the packing density of the solar cells per module.

A design was selected in which the silicon solar cells are directly mounted on the substrate and separate glass cover is used for protection from environment. This design, which is a modification of common flat plate solar-thermal collector requires a positive spacing between the substrate and the cover and separate spacer ring is used for this purpose. Studies with solar-thermal flat plate collectors have shown that decreasing spacing between the transparent cover and the collector plate enhances the thermal losses, therefore, in this case, the spacing was kept as small as possible, however, retaining sufficient spacing for convectional flow between the transparent cover and the front bus bars. Small air volume is also preferred to reduce the elastic deformation of the collector enclosure due to pressure changes caused by temperature fluctuations.

Despite the pressure fluctuation it is desirable to seal the collector cavity as well as possible to prevent the atmospheric corrosion of the interconnection junctions of the solar cell matrix.

To meet the low $/W cost goal, all module designs must have high packing density and generally only low-cost materials are used to reduce the material cost.

High packing density and suitability for mass manufacturing set special requirements for the interconnection arrangement. The hexagonal cells can be packed with minimum spacing, however, this also makes any front to back, P to N, interconnection between the individual cells more difficult. A simple parallel-series arrangement was selected in which the parallel interconnections were made across the cell surfaces with conductor bus bars. The P to N series interconnections are made outside of the parallel connected rows. The assembly of this type of design is easy to automate, and as an added advantage the external conductors reduce the current carrying requirements set for the metallization of the collector pattern trunk lines on the solar cell.

The dimensions of the module were selected to obtain practical size for automated or semiautomated manufacturing and for easy LSSA array assembly and maintenance. With 0.76-mm spacing between the hexagonal cells, 8 cells X 20 cells array can be mounted into 61 X 122 cm^2 substrate and provide sufficient space for series interconnections, external contacts and seal rings. Figure 35 shows the exploded view of proposed LSSA collector module, Design I and Figure 36 shows a cross section of the frame and seal assembly. Figure 37 shows a detail of the back conductor arrangement of Design II.

a. STRUCTURAL MATERIALS

The selected module design dictates some specific requirements for the substrate. The glass cover reduces the thermal dissipation by convection and conduction and blocks the thermal dissipation by infrared radiation through the front cover. To prevent excessive temperature rise in the solar cells, the thermal dissipation through the substrate has to be maximized. Therefore, metallic materials were preferred for this purpose.

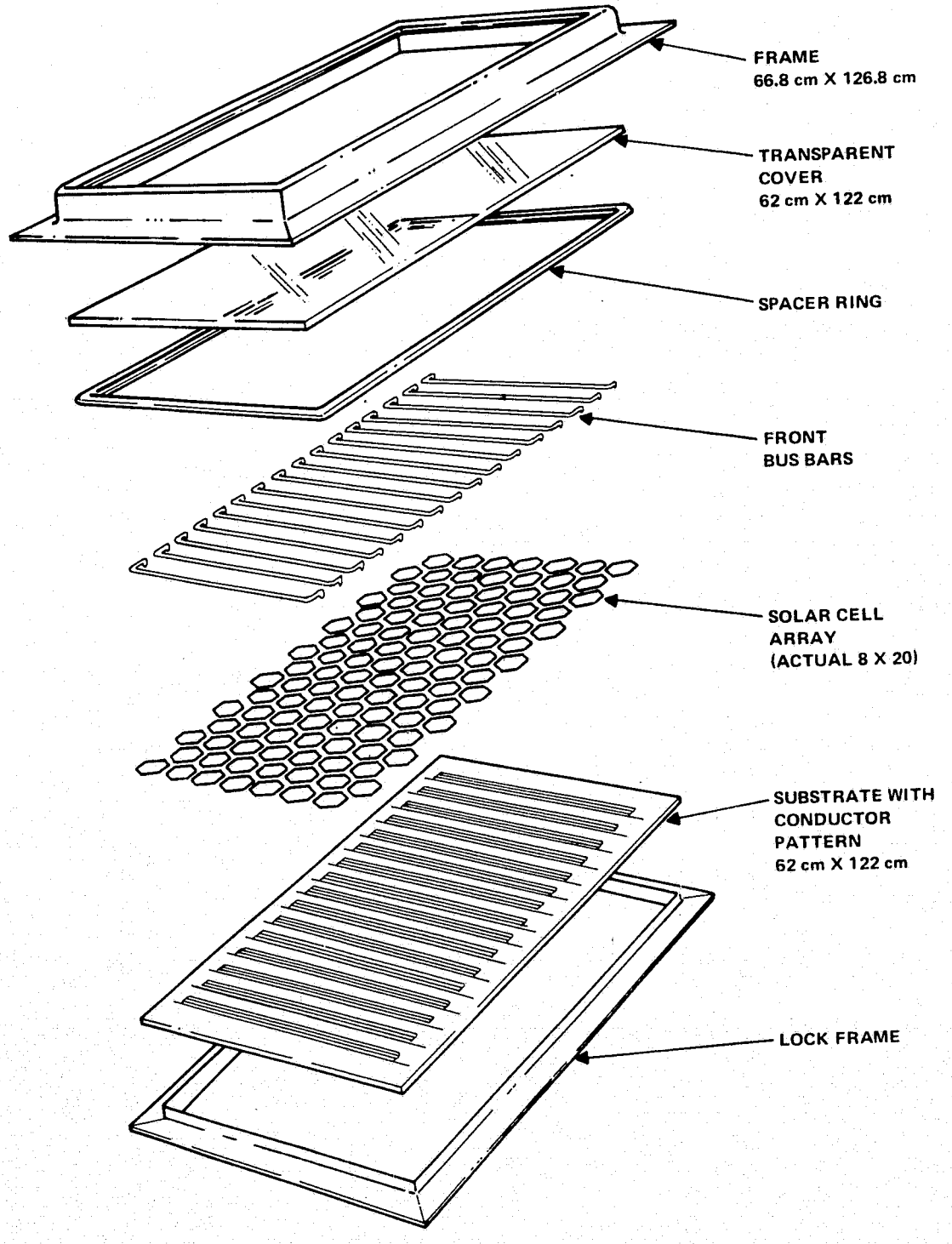


Figure 35. Exploded View of Proposed LSSA Module

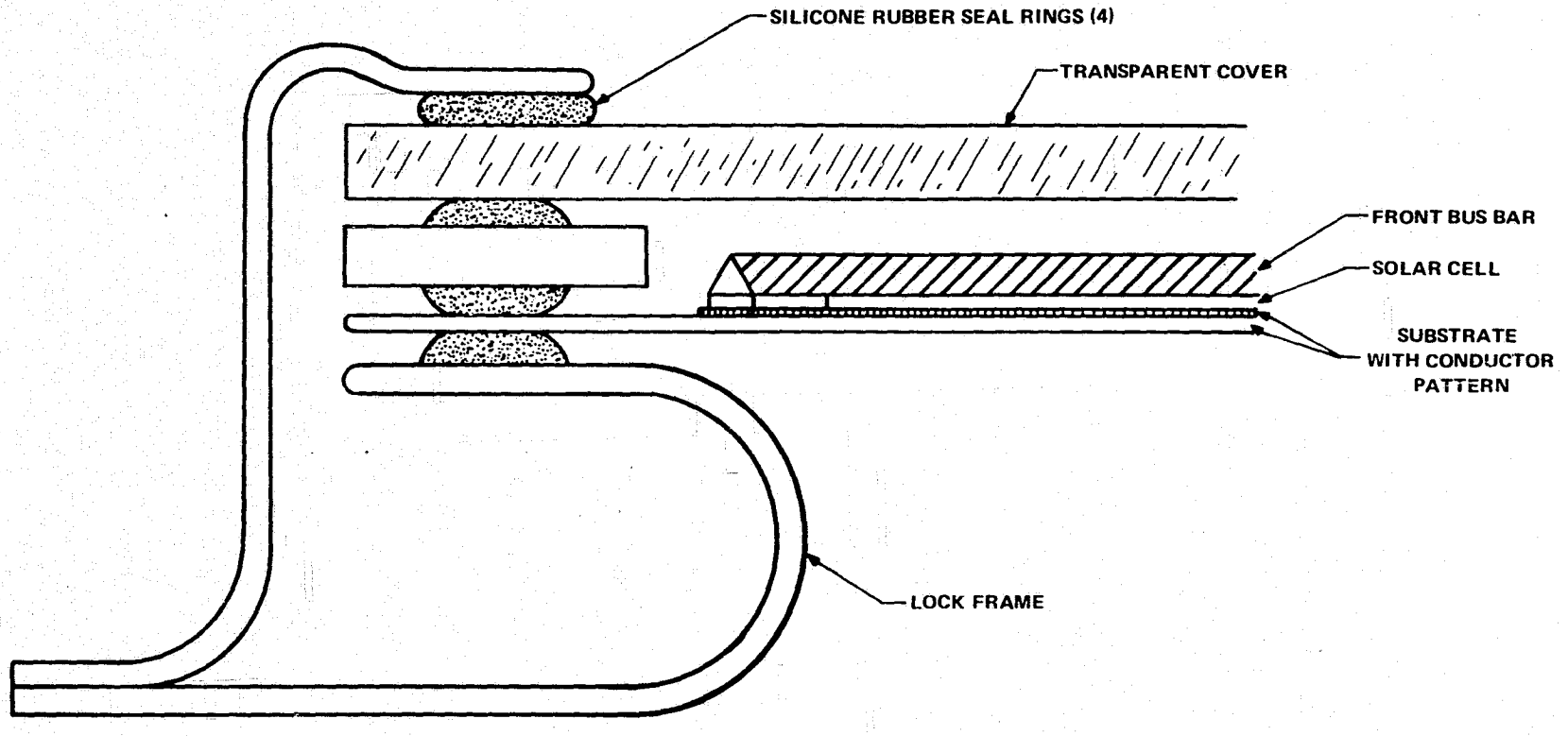


Figure 36. Cross Section of Proposed LSSA Module Frame

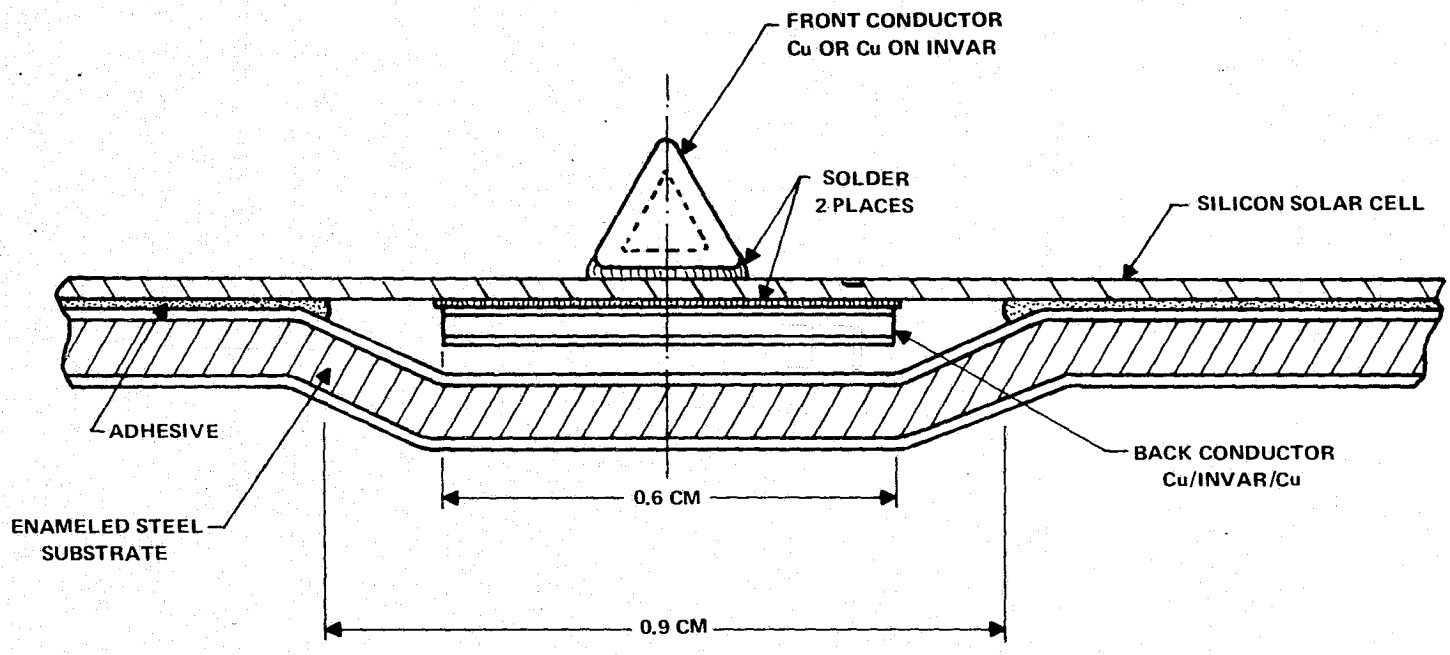


Figure 37. Back Conductor Arrangement of Proposed LSSA Module

Porcelain enameled steel was selected for all structural parts including the substrate. It has a good demonstrated durability in outdoor environment, low per square meter material cost, good thermal conductivity as substrate material and the raw materials are available in large quantities. The good dielectric properties of the porcelain enamel permit direct mounting of the silicon solar cells on the substrate, assuring good thermal contact with the substrate and consequently good thermal dissipation through the substrate.

By having only one material system for all the structural parts offers definite advantages in the module assembly. Notably the same manufacturing equipment and processes can be used for all the structural components and also inventories are reduced.

b. TRANSPARENT COVER

As was pointed out before, glass was selected as cover material, again, because of its demonstrated durability against atmosphere deterioration, good availability and relatively low cost. The fragility of glass is of concern and, therefore, both tempered and untempered glasses are considered in the cost estimation. Regular window glass has a transmittance of 85%. If iron content is reduced as in so-called "Water Clear Crystal #76" transmittance is increased to 91%. Both glasses are considered in cost calculations and the difference in the transmittance is accounted for the $/W values.

c. SEALER STRIPS

Silicone rubber sealer strips, applied to and cured directly on the frame, spacer ring and lock frame, are used to seal the collector from ambient atmosphere. Contacts through the substrate are also sealed using silicone rubber washers.

d. FRONT AND BACK CONDUCTORS

The conductors are soldered or welded directly across the front and the back of the silicon solar cells. In both cases a good electrical conductivity is required to minimize the I^2R losses and the coefficient of thermal expansion of the conductor cannot differ too significantly from that of silicon, $\alpha_{Si} = 2.33 \times 10^{-6}$ cm/cm/°C. Conductor material should be easy to solder. None of the monolithic metals or alloy meet these requirements. However, composite metal technology can be used to manufacture material systems to meet the requirements. For this application the best choice, from the standpoint of manufacturability and cost, is copper-clad Invar.

The coefficient of the thermal expansion of two layer composite metal, parallel to the layers can be calculated from the approximate equation

$$\alpha_c = \alpha_1 + \frac{A_2 E_2}{A_1 E_1} \times \alpha_2 \qquad (54)$$

in which

α_1 = coefficient of thermal expansion of the material with lower α

α_2 = coefficient of thermal expansion of the material with higher α

A_1 and A_2 are cross sectional areas of the component layers

E_1 and E_2 are moduli of elasticity of component metals.

Similarly the resistance per unit of length of the composite metal conductors can be calculated parallel to the layers from the parallel circuit equation.

$$\frac{1}{R_c} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \cdots\cdots\cdots \qquad (55)$$

Where R_1, R_2 and R_3 are the respective resistance of the composite metal layers per unit length.

The conductors were dimensioned by permitting a certain I^2R loss per row. For the calculations it was assumed that current pickup was constant per unit length of the conductor, Figure 38. For the length l_1 the I^2R losses can be calculated from equation

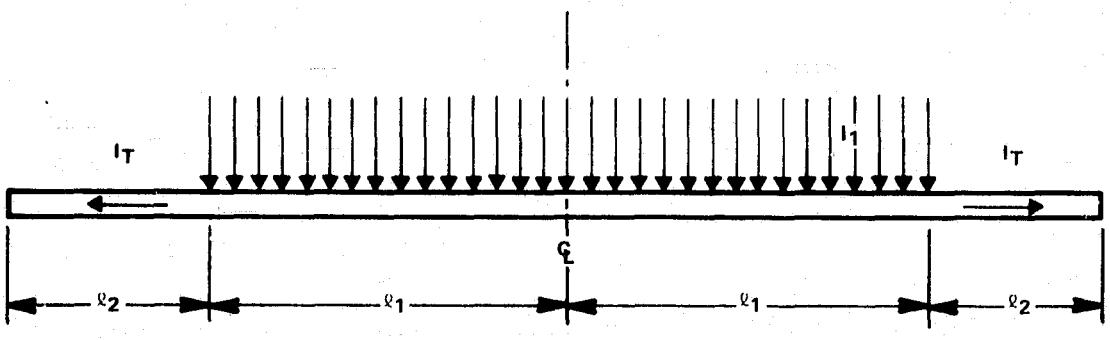
$$\Delta P = \int_0^L (I_L x)^2 R_c \, dx$$

$$\Delta P = \frac{1}{3} I_L^2 R_c L_1^3$$

The total I^2R losses are then

$$\Delta P_T = \frac{1}{3} I_L^2 R_c L_1^3 + I_T^2 R_c L_2 \qquad (56)$$

Assigning specific values for the loss component ΔP, the necessary cross sections of the conductors can be calculated.



ℓ_1 = LENGTH TO WHICH SILICON SOLAR CELLS ARE SOLDERED

ℓ_2 = AVERAGE TERMINATION LENGTH OUTSIDE OF THE CELLS

I_1 = CURRENT PICKUP A/CM

I_T = TOTAL CURRENT FOR HALF LENGTH OF CONDUCTION = ℓ_1 X I_1

Figure 38. Schematic of Module Interconnects

1. Front Conductor

Assuming transmittance for the front cover, 13.5% cell efficiency and permitting 2% I^2R loss at peak output, we obtain $R_c = 0.0001757\ \Omega/cm$ from equation (56). Twenty-five percent of the cross section of the conductor is assumed to be copper and 75% Invar. From equation (55) we obtain

$$\frac{1}{R_c} = \frac{A_1}{\rho_1} + \frac{A_2}{\rho_2} + \ldots\ldots \qquad (57)$$

in which

$A_1 = 0.25 \cdot A$ for copper

$A_2 = 0.75 \cdot A$ for Invar

$\rho_1 = 1.7 \text{ X } 10^{-6}\ \Omega$-cm for copper

$\rho_2 = 50 \text{ X } 10^{-6}\ \Omega$ -cm for Invar

The required cross section of the composite metal conduction

$$A = 0.0408 \text{ cm}^2$$

The front conductor should cause a minimum shadowing of the solar cell and offer a flat surface for soldering to the metallization pattern on the silicon solar cell. An equilateral triangle was selected because some of the incident radiation, blocked by the base of the triangular conductor can be recovered by reflection from the sides of the conductor to the cell surface.

For $A = 0.0409 \text{ cm}^2$, the side of the triangular conductor will be $s = 0.3$ cm.

The apparent coefficient of thermal expansion of the composite metal conductor is calculated from equation (54),

$$\alpha_c = \alpha_1 + k\,\alpha_2$$

in which $k = A_2E_2/A_1E_1$ and

$$\alpha_1 = \alpha_{Invar} = 1.5 \times 10^{-6} \text{ cm/cm/°C}$$

$$\alpha_2 = \alpha_{Cu} - 16.5 \times 10^{-6} \text{ cm/cm/°C}$$

$$E_1 = E_{Invar} = 21.4 \times 10^6 \text{ lb/in}^2$$

$$E_2 = E_{Cu} = 16.0 \times 10^6 \text{ lb/in}^2$$

$$A_1 = 0.75\ A$$

$$A_2 = 0.25\ A$$

$$\alpha_c = 5.7 \times 10^{-6} \text{ cm/cm/°C}$$

2. Back Conductor

Two different mounting techniques are considered. In the first one, tin-lead solder is used to bond the silicon solar cells to the porcelain enameled substrate and the tin-lead pattern is at the same time used as the conductive path. The second design uses a separate composite metal conductor rail which is tin-lead soldered to the back sides of the silicon solar cells. The cells are adhesively bonded to the porcelain enameled steel substrate.

Design I

The conductor-bonding pattern is silk screened to the porcelain enamel surface using copper or silver ink. The tin-lead-(silver) bonding and conduction layer is wave soldered to the printed pattern. For the back conductors it would be desirable if the I^2R losses would not exceed 1.5%. However, the solder stripes become too wide for the 1.5% I^2R losses. Therefore, for Design I, 2% I^2R loss in back conductor is used in calculations, and also the conductivity of the silk screened copper pattern has to be included in the calculation. Using equation (57) we obtain

$$\frac{1}{R_c} = \frac{w \cdot t_1}{\rho_1} = \frac{w \cdot t_2}{\rho_2} \tag{58}$$

$t_1 = 0.0125$ cm for tin-lead solder

$t_2 = 0.00125$ cm for silk screened pattern

$\rho_1 = 14.5 \times 10^{-6}$ Ω-cm for Sn-40 Pb solder

$\rho_2 = 2 \times 10^{-6}$ Ω-cm for silk screened copper

$R_c = 0.000252$ Ω-cm for 2% I^2R loss

Above calculation gives w = 2.6 cm or four 0.65 cm wide parallel stripes of tin-lead solder for each cell row.

Design II

The width of the back conductor was selected to be 0.6 cm. The conductivity of the 60% Sn-40% Pb solder, which is used to solder the conductor to the back metallization of the silicon solar cell is taken into consideration, however, the contribution of the back metallization of the silicon solar cell is disregarded as in the previous calculations

$$\frac{1}{R} = \frac{w \cdot t}{\rho_1} + \frac{w \cdot t_2}{\rho_2} + \frac{w \cdot t_3}{\rho_3} \tag{59}$$

$t_1 = 0.25\ t$ = total thickness of copper layers

$t_2 = 0.75\ t$ = thickness of Invar layer

$t_3 = 0.0125$ cm = thickness of tin-lead solder

$\rho_3 = 14.5 \times 10^{-6}\ \Omega$-cm for tin-lead solder

$R_c = 0.000189\ \Omega$/cm for 1.5% I^2R loss

The back conductor thickness from the above equation becomes:

$$t = 0.06 \text{ cm}$$

The coefficient of the thermal expansion is the same $\alpha_c = 5.7 \times 10^{-6}$ cm/cm/°C as for the triangular front conductor, because the area ratio between the copper and Invar are the same.

e. LOCK FRAME

Lock frame is designed so that it is elastically formed in the assembly providing necessary spring action to compensate for possible relaxation of the silicone rubber seals. It is pressed to the frame, simultaneously tensioning it, and riveted to the place using hollow rivets.

f. COMPONENT MANUFACTURING

For the following components, labor and overhead cost are included in Tables 13 and 14 as a fraction of the material cost.

1. Frame and Lock Frame

Starting materials: enameling steel strip

porcelain enamel frit

silicone rubber sealant

Slit to width

Stamp fastener holes

Roll form

Cut to length

Weld corners

Table 13. Estimated Material and Component Cost of Proposed LSSA Module, Design I

	Item	Low $/mod	Low $/W	Probable $/mod	Probable $/W	High $/mod	High $/W
1.	Frame						
	Enameled Steel	1.35	0.020	1.72	0.026	2.45	0.034
2.	Glass Cover						
	Ann. window	2.66	0.040				
	Temp. window			3.84	0.057		
	Temp. low iron					9.28	0.130
3.	Spacer Ring						
	Enameled Steel	0.66	0.010	0.88	0.013	1.27	0.018
4.	Sealants 4 places	1.56	0.023	1.88	0.028	2.19	0.031
5.	Substrate						
	Enameled Steel	3.84	0.057	5.04	0.075	8.00	0.112
6.	Front conductor	0.60	0.009	0.75	0.011	1.00	0.014
7.	Substrate conductor						
	a. Screen print						
	Pattern						
	Copper ink	3.59	0.054				
	Average			5.60	0.084		
	Silver ink					7.63	0.107
	b. Tin-lead conductor	2.24	0.034	3.12	0.047	4.01	0.056
8.	Connectors	0.75	0.011	1.00	0.015	1.50	0.021
9.	Lock Frame						
	Enameled Steel	1.60	0.024	2.06	0.031	2.94	0.041
10.	Lock frame fasteners	0.36	0.005	0.72	0.011	1.08	0.015
	Subtotal	18.85	0.282	25.89	0.387	41.35	0.579
	Assembly L + OH	2.37	0.035	3.16	0.047	4.74	0.066
	TOTAL M + L + OH	21.22	0.317	29.05	0.434	46.09	0.645

Table 14. Estimated Material and Component Cost of Proposed LSSA Module, Design II

	Item	Low $/mod	Low $/W	Probable $/mod	Probable $/W	High $/mod	High $/W
1.	Frame						
	Enameled Steel	1.35	0.020	1.72	0.026	2.45	0.034
2.	Glass Cover						
	Ann. window	2.66	0.040				
	Temp. window			3.84	0.057		
	Temp. low iron					9.28	0.130
3.	Spacer ring						
	Enameled steel	0.66	0.010	0.88	0.013	1.27	0.018
4.	Sealants 4 places	1.56	0.023	1.88	0.028	2.19	0.031
5.	Substrate						
	Enameled steel	3.84	0.057	5.04	0.075	8.00	0.112
6.	Front conductor	0.60	0.009	0.75	0.011	1.00	0.014
7.	Back conductor	2.01	0.030	2.41	0.036	2.82	0.039
8.	Adhesive	0.81	0.012	1.22	0.018	1.62	0.023
9.	Connectors	0.75	0.011	1.00	0.015	1.50	0.021
10.	Lock frame						
	Enameled steel	1.60	0.024	2.06	0.031	2.94	0.041
11.	Lock frame fasteners	0.36	0.005	0.72	0.011	1.08	0.015
	Subtotal	16.20	0.241	21.52	0.321	34.15	0.478
	Assembly L + OH	3.64	0.054	4.85	0.073	7.28	0.102
	TOTAL M + L + OH	19.84	0.295	26.37	0.394	41.43	0.580

Clean

Prepare surface for enameling

Apply enamel frit

Fire

Inspect

Apply sealant bead

Cure

→ To the assembly line

2. Spacer Ring

Starting materials: cold drawn carbon steel rod

porcelain enamel frit

silicone rubber sealant

Cut to length

Weld corners

Clean

Prepare surface for enameling

Apply enamel frit

Fire

Inspect

Apply sealant beads

Cure

→ To the assembly line

3. Substrate

Starting materials: enameling steel strip

porcelain enamel frit

Cut in length

Punch connector holes

Draw back conductor grooves (optional)

Clean

Prepare surface for enameling

Apply enamel frit

Fire

Inspect

→ To the substrate assembly area

4. Front Conductor

Starting materials: Invar cored copper 75/25 area ratio

Tin

Draw into profile

Clean

Tin electroplate

Reflow

Draw to mirror finish

Clean

→ To the cell row manufacturing area

5. **Back Conductor (Design II)**

Starting materials: copper clad Invar strip 25/75

area ratio

tin

Tin electroplate

Slit

Clean

→ To the cell row manufacturing area

6. **Connector Lugs, Silicon Gaskets for connectors and Fastening Rivets purchased from outside vendors.**

7. **Cover Glass**

Cut

Clean

→ To the assembly line

g. CELL ROW MANUFACTURING, DESIGN II

Cell rows are soldered and formed in automated manufacturing line. For further process steps, rows are supported by reusable carriers.

	Rate per labor hour				L + OH $7/hr
	Cell	Rows	Modules	Hrs/mod	$/mod
Solder cell rows	720	90	4.5	0.222	1.55
Cut					
Bond ends					
Trim to length					
Clean		600	30	0.033	0.23
Test		360	18	0.056	0.39
Subtotal					2.17

h. SUBSTRATE ASSEMBLY

1. Design I

The manufacturing of back conductor pattern on substrate is included in the assembly operation.

	Rate per labor hour				L + OH $7/hr
	Cell	Rows	Modules	Hrs/mod	$/mod
Clean substrate			360	0.003	0.02
Silk screen pattern			240	0.004	0.03
Dry + fire			240	0.004	0.03
Wave solder conductors			240	0.004	0.03
Clean + inspect			60	0.017	0.12
Solder cell rows	960	120	6	0.167	1.17
Bond front bus bars		240	12	0.083	0.58
Solder interconnect		500	25	0.040	0.28
Clean ultrasonically			60	0.017	0.12
Assemble connector lugs			120	0.008	0.06
Test			360	0.003	0.02
Subtotal					2.46

2. Design II

	Rate per labor hour				L + OH $7/hr
	Cell	Rows	Modules	Hrs/mod	$/mod
Apply adhesive to cells	3600	450	22.5	0.044	0.31
Bond to substrate		120	6	0.167	1.17
Solder interconnect. (weld)		500	25	0.040	0.28
Clean ultrasonically			60	0.017	0.12
Assemble connector lugs			120	0.008	0.06
Test			360	0.003	0.02
Subtotal					1.96

i. MODULE ASSEMBLY , DESIGNS I AND II

Module assembly is done in a continuous assembly line.

	Modules/ labor hr	Hrs/mod	L + OH $7/hr $/mod
Assemble	10	0.1	0.70
Place frame			
Insert glass			
Insert collector plate			
Insert spacer ring			
Apply tensioning load			
Rivet			
Remove from assembly tool and line			
Test	360	0.003	0.02
Subtotal			0.72

j. MODULE ASSEMBLY COST

Tables 13 and 14 give the estimated total material, labor and overhead cost, excluding the silicon solar cells and depreciation. Cost will be shown $/module and $/watt output. Effective peak output of cell per unit area is

$$P_T = \eta_g \cdot \eta_{tb} \cdot \eta_{bb} \cdot \eta_c \cdot I_o \qquad (60)$$

η_g = transmittance of the glass

η_{fb} = 1-front conductor losses

η_{bb} = 1-back conductor losses

η_c = efficiency of Si solar cell, includes shadowing by metallization pattern and front conductor

η_g = 0.85 window glass

η_g = 0.91 Water White Crystal #76

$\eta_{fb} = 1 - 0.02 = 0.98$

$\eta_{bb} = 1 - 0.015 = 0.985$

$\eta_c = 0.135$

$I_o = 0.1$ W/cm^2

For Window glass $P_T = 0.01108$ W/cm^2

For W.W.C #76 $P_t = 0.01186$ W/cm^2

In calculating the module output, the total cell area is considered, because the shadowing losses of the metallization and the front bus bar are accounted for in the cell efficiency.

$$P_M = n \cdot A_c P_T \tag{61}$$

n = number of cells in module = 160

A_c = area of cell cm^2 = 37.71 cm^2

P_T = effective cell output W/cm^2

For window glass P_M = 66.85 W/module

For Water White Crystal #76 P_M = 71.56 W/module

J. SOLAR CELL PROCESS STEP COSTS

Processing cost data has been generated on a large number of potentially useful process steps. These data are useful for comparing costs for various solar cell process alternatives. These data are calculated on the basis of processing 10.2-cm single-crystal wafers. All costs are based on 1976 dollars with processes projected to be available in the 1981-1982 time period for the implementation into a 1985 500 MW per year factory. Some of the processes require development

but no major technical innovations are assumed. Not all process steps have been experimentally verified at Texas Instruments, but all processes are available in the industry and are either in use in a simplified form or under active investigation.

Material costs include all materials and supplies consumed in the operation. No distinction is made for materials that appear in the final product versus those that are discarded. No allowances are made for material recovery except in places where a chemical may be reused several times, such as a refluxing solvent or an etch bath that is used many times. In general, reclamation costs are considered to be too expensive to be cost effective.

Labor costs are based on a production operator pay rate of $3.50 per hour with no allowance for overtime or shift premium. The overhead (OH) rate of 100% is intended to cover all direct overhead costs such as F.I.C.A., insurance, etc., supervisory and clerical costs and allow for a slight fraction to cover overtime or shift premiums. Labor costs are calculated on the basis of the hourly throughput rate times 0.8. The 20% reduction in throughput rate covers meal and rest breaks plus an allowance for equipment repair and maintenance.

Depreciation is calculated on a straight line 7-year depreciation at 9% annual interest. The depreciation in the first year is the same as the depreciation in the seventh year. Depreciation is based on a 50-week, 7-day, 24-hour operating year. No other allowance is made for vacation or holiday shutdown.

Process yield is the physical yield at the particular process step and no functional or parametric yield is taken before the cell test step. Typical process step yields are 98% or better.

Cell efficiency, in general, is not a function of the individual process step but rather is a function of the composite solar cell process. In most cases, a solar cell process capable of yielding cells of 13.5% efficiency (AM1) is assumed. Higher cell efficiencies would, of course, yield lower cost per watt.

Table 15 is a compilation of the process step cost breakdown. The subsections of Table 15 are cleaning and surface preparation, junction formation, metallization, AR coating, encapsulation and test. A brief discussion of each subsection follows.

1. Cleaning and Surface Preparation

As a general rule, acid cleanup and etching operations are more expensive than equivalent nonacid operations. With the exception of texture etching, all operations assume a polished single-crystal surface. Texture etch costs include a preliminary etch polish operation to remove saw damage.

Table 15. Solar Cell Process Step Cost Breakdown

Process Step		$/W					Process (%) Yield	Investment Cap.	Cell Eff. (%)	Thruput W/hr	Thruput MW/yr	$K Capital Cost
		Mat'l	Labor	O.H.	Dep.	Total						
Cleaning and Surface Preparation												
Scrubbing (Detergent)		.0001	.0088	.0088	.0033	.0210	98	.0167	13.5	4x125	3.36	56
Scrubbing (Alcohol)		.0125	.0088	.0088	.0033	.0334	98	.0167	13.5	4x125	3.36	56
Cleanup — Acid — H_2O		.0043	.0029	.0029	.0015	.0116	98	.0074	13.5	1500	10.0	75
Cleanup Solvent — Acid — Solvent		.0092	.0088	.0088	.0044	.0312	98	.0223	13.5	500	3.36	75
Degrease — Refluxing Solvent		.0001	.0044	.0044	.0035	.0124	99	.0179	13.5	500	3.36	60
Ultrasonic Clean — Solvent		.0002	.0044	.0044	.0030	.0118	99	.0149	13.5	500	3.36	50
Reverse Sputter (50 Å)		.0002	.0023	.0023	.0054	.0102	99	.0271	13.5	1920	12.9	350
Etch Polish — Acid		.050	.0088	.0088	.0044	.0720	98	.0223	13.5	500	3.36	75
Etch Polish — NaOH		.0010	.0088	.0088	.0030	.0216	98	.0149	13.5	500	3.36	50
Oxide Etch — Acid		.0031	.0088	.0088	.0044	.0251	99	.0223	13.5	500	3.36	75
Oxide Etch — Plasma		.0002	.0088	.0088	.0039	.0217	99	.0194	13.5	500	12.9	250
Texture — H_2NNH_2		.0178	.0088	.0088	.0044	.0398	98	.0223	13.5	500	3.36	75
Texture — N_aOH		.0014	.0088	.0088	.0030	.0220	98	.0149	13.5	500	3.36	50
Junction Formation												
Spin-on — Polymer	2 sides	.0023	.0146	.0146	.0059	.0374	99	.0297	13.5	300	2.02	60
Spray-on — Polymer	2 sides	.0023	.0146	.0146	.0059	.0374	99	.0297	13.5	300	2.02	60
Drive-in (diffusion)		.0010	.0073	.0073	.0017	.0173	99	.0087	13.5	600	4.04	35
Silicon Source		.090	.0073	.0073	.0017	.1063	99	.0087	13.5	600	4.04	35
Gas Depositing & Diffusion		.030	.0073	.0073	.0022	.0468	99	.0111	13.5	600	4.04	45
Ion Implant	1 side	.010	.0182	.0182	.0185	.0649	99	.093	13.5	240	1.61	150
Ion Implant (advanced)	1 side	.010	.0088	.0088	.0178	.0454	99	.089	13.5	500	3.36	300
Spin-on Polymer	1 side	.0012	.0073	.0073	.0030	.0188	99	.0149	13.5	600	4.04	30
Metallization												
Vacuum Deposition Ti/Cu	1 side	.035	.0194	.0194	.0513	.1251	98	.265	13.5	225	1.51	400
Vacuum Deposition Ti/pd/Ag	Front	.060	.0194	.0194	.0513	.1501	98	.265	13.5	225	1.51	400
Vacuum Deposition Ti/Pd/Ag	Back	.060	.0194	.0194	.0513	.1501	98	.265	13.5	225	1.51	400
Thick Film, Ag	Front	.0024	.0036	.0036	.0012	.0108	98	.0062	13.5	1200	8.06	50
Thick Film, Ag	Front	.0024	.0036	.0036	.0012	.0324	98	.0062	13.5	1200	8.06	50
Thick Film, Base Metal	Front	.0015	.0036	.0036	.0012	.0099	98	.0062	13.5	1200	8.06	50
Thick Film, Base Metal	Back	.0150	.0036	.0036	.0012	.0234	98	.0062	13.5	1200	8.06	50

Table 15. Solar Cell Process Step Cost Breakdown (Continued)

Process Step	$/W					Process (%) Yield	Investment Cap.	Cell Eff.(%)	Thruput W/hr	Thruput MW/yr	$K Capital Cost
	Mat'l	Labor	O.H.	Dep.	Total						
AR Coating											
Oxide Growth	.0005	.0073	.0073	.0017	.0168	99	.0087	12.0	600	4.03	35
Spin-on	.0023	.0073	.0073	.0030	.0199	99	.0148	13.5	600	4.03	60
Evaporate	.004	.0109	.0145	.0145	.0403	99	.0744	13.5	400	2.69	200
Sputtering	.004	.0109	.0109	.0145	.0403	99	.0074	13.5	400	2.69	200
Bake (Spin-on)	0.0	.0073	.0073	.0015	.0161	99	.0074	13.5	600	4.03	30
Encapsulant											
Glass Superstrate	.066	.0219	.0219	.0241	.1339	96	.1213	13.5	200	1.34	163
Glass with Substrate	.069	.0219	.0219	.0226	.1354	96	.1138	13.5	200	1.34	153
Substrate with Coating	.045	.0219	.0219	.0226	.1114	96	.1138	13.5	200	1.34	153
Hermetic	.247										
Test											
Cells	0.0	.0044	.0044	.0030	.0118	85	.0149	13.5	1000	6.72	100
Modules 80W	0.0	.0003	.0003	.0006	.0012	98	.0010	13.5			

2. Junction Formation

Junction formation represents one of the most critical operations in the solar cell process sequence. Diffused layer resistivity, junction depth, profile, and surface condition are all critical parameters in the control of a high efficiency solar cell process. Both an N^+ and a P^+ layer must be formed in an N^+PP^+ solar cell structure. The P^+ layer forms a region for ohmic contact to the P base region and forms the back surface field. The N^+ layer must form a good diode for efficient solar cell operation.

Processes that allow independent introduction of the N^+ and P^+ layers are desirable. From this standpoint, polymer dopant and ion implantation processes would be favored, assuming equivalent junction parameters. Integrated circuit open tube gas deposition-diffusion techniques, introduce impurity atoms on all exposed surfaces and are not cost effective unless special processes are used, e.g., oxide mask the back side during front-side diffusion or impurity compensation such as Al alloying through an N^+ layer.

Ion implant and polymer dopant processes must be followed by a drive-in diffusion or thermal activation step. Both of these techniques allow one to independently introduce N-type and P-type impurities on opposite surfaces followed by a single drive-in diffusion step.

Ion implantation is well advanced in the semiconductor industry and has found wide acceptance in certain low-dose applications. High-dose applications, such as solar cells, suffer from a low throughput per capital dollar and significant advances in beam current and wafer handling techniques must occur before this technique will become cost effective for low cost operations.

Polymer dopant or paint-on techniques have been used in the semiconductor industry for well over 10 years as a low technology process. In recent years, commercial formulations and proprietary formulations have been developed for specific applications such as diffusion under exitaxial films. Process control is good ($< \pm$ 10%) within the range of interest for solar cells, 30-100 $\Omega/\square$ diffused layer resistivity. Existing formulations suffer from a shelf life problem with typical shelf lives from one month to six months. In a solar cell factory using polymer dopant, the dopant formulation should be included in the factory to ensure good control over product quality.

Techniques such as epitaxy and alloying are too expensive to be considered for low-cost solar cell manufacture. Back side alloying, e.g., Al may have a place in low-cost solar cell manufacture.

3. Metallization

Vacuum deposition, either evaporation or sputtering is too expensive for low-cost solar cell manufacture. Vacuum deposition is wasteful of material, low in throughput, and high in depreciation when compared to thick film or electroless deposition techniques. Mask stencils are more cost effective than photolithography and etching but mask costs and mask cleaning are costly.

Thick-film technology is well developed for hybrid circuit applications. This technology requires further development, however, before it can be readily applied to direct metal-silicon contacts. Present commercial ink or paste formulations typically contain precious metals, Ag, Au, or Pt, and a glassy matrix for adhesion to a ceramic surface. Low-cost inks for solar cell application should ideally contain cheaper base metals and probably no glassy matrix. A small amount of development is in progress to develop inks for solar cell applications. More work needs to be done in this area. High throughputs and low capital investments are typical in this field.

Electroless plating is another low-cost metallization process alternate. Electroless plating techniques are well known in the semiconductor industry. Capital costs are low and throughput is generally high. Typical applications of electroless Ni in the semiconductor industry has been on deep junction devices. Application on shallow junction solar cells will require some development. The key area of concern in the application of electroless plating in low-cost processing schemes is the ability to deposit a metal pattern directly without resorting to masking or etching techniques. Further development should be encouraged in the area of patterned electroless depositions. A technique known as Photo-Impeded-Metal Deposition, PIMDEP, appears to offer a fruitful area for future development.

4. AR Coating

Both spin-on (or spray) and vacuum deposition techniques appear to offer attractive process alternatives. Oxide growth is low cost but suffers from the restriction that the only convenient oxide that can be grown on Si is SiO_2, a relatively low index material. Low index SiO_2 on a textured surface may be acceptable in light of the low cost for oxide growth.

Attractive AR coating will feature high index films ($\approx$ 2.0) and in general, single layers will be more cost effective than multiple layers.

5. Encapsulation

Array encapsulation presents a major cost and reliability barrier. Low-cost approaches using conformal coating do not appear to offer a high probability of achieving the 20-year life goal. Conformal coatings are material intensive in cost, and thick coatings do not appear to offer significant improvement in life time.

The highest probability of achieving a 20-year life module appears to require a costly hermetic encapsulation. This approach is very material intensive and does not, at this time, meet the cost goals. Further investigation is required to find an acceptable compromise between the low-cost high-risk and the high-cost low-risk approaches.

At this time, the closest approximation to an acceptable encapsulation scheme is the glass with substrate (porcelainized steel) approach using a plastic seal at the edges.

6. Test

Solar cell and module test concepts appear to be cost effective and well within existing technology capabilities. Solar cell test yields projected at 85% should be improvable with a well controlled process and good silicon sheet material. Cell test yields in excess of 90% should be possible with a well engineered solar cell process and good process control.

The goal of the solar cell process and the cell test should be to produce a single class of high-quality solar cells. One should avoid the trap of a "cheap" process that produces a distribution. A "cheap" process should not be confused with a low-cost process.

K. LOW COST SILICON SOLAR CELL MODULE COSTING

The design of a low-cost silicon solar cell process requires a number of choices that must be made within the context of some set of constraints. The constraints are not invariant but will change with time and advances in the various process technologies, design windows, and material technologies. Task 4 of the LSSA Project calls for an assessment of existing technologies and an extrapolation into the near future for a guideline to a 1985 high-volume production base. Within these constraints a further set of boundary conditions or philosophies can be imposed. These are:

1) High cell efficiency is a must
2) All process steps must be demonstrated no later than 1982
3) All process steps should be additive
4) The process should yield a tight distribution
5) All process steps that are in a feasibility stage must have an alternate fall-back that is process compatible.

While these conditions are mostly self-evident, a few explanatory comments are in order.

Cell efficiency and module efficiency are key factors driving cost. While some processes may yield cheap solar cells, the module costs and system costs are area related and drive the module and system costs to unacceptable levels. This cost analysis assumes a minimum cell efficiency of 13.5% at AM1.

In order to impact a 1985 high-volume production goal, all process steps must be operating production processes by 1985. The scale-up to a 500 MW annual run rate will require a 2 to 3-year lead time. As a practical corollary, any factory must be capable of absorbing new advances in technology or technical obsolescence will occur.

For minimum cost to be achieved, no extraneous operations should be allowed. Additive processes are those that lead in a direct path to the final product. Process steps such as a deposition followed by partial removal are to be avoided, if possible. An alternate process that would deposit a patterned material is preferred.

A well-controlled process should yield a product with a narrow distribution of parameters. Testing and sorting at the end of the process is a poor substitute for proper process design and control. A factory that relies on the sale of "seconds" to be economically viable is a poorly designed factory.

Some process steps that are included will still be in a feasibility stage. These process steps must have an alternate available so that process development does not depend totally on the success of one or more critical steps. This provides a redundancy that allows rapid advancement of technology with minimum risk.

From the process step cost analysis, one can construct a series of solar cell processes that will work. On the basis of minimum cost and minimum technical risk, the following baseline process sequence was chosen. The process flow and individual process step costs are shown in Figure 39. Yield numbers given for each process step are basically mechanical yield with all electrical yield accounted for at the cell test operation. The column on the far right is the cost per watt yielded through each process operation. The cumulative yielded process and test cost is given at the bottom of the column. The yielded cost of $0.2559 per watt is the cost for cell processing and cell testing and does not include the cost of silicon sheet or module test and assembly. The totals across the bottom are the unyielded material, labor, overhead and depreciation costs.

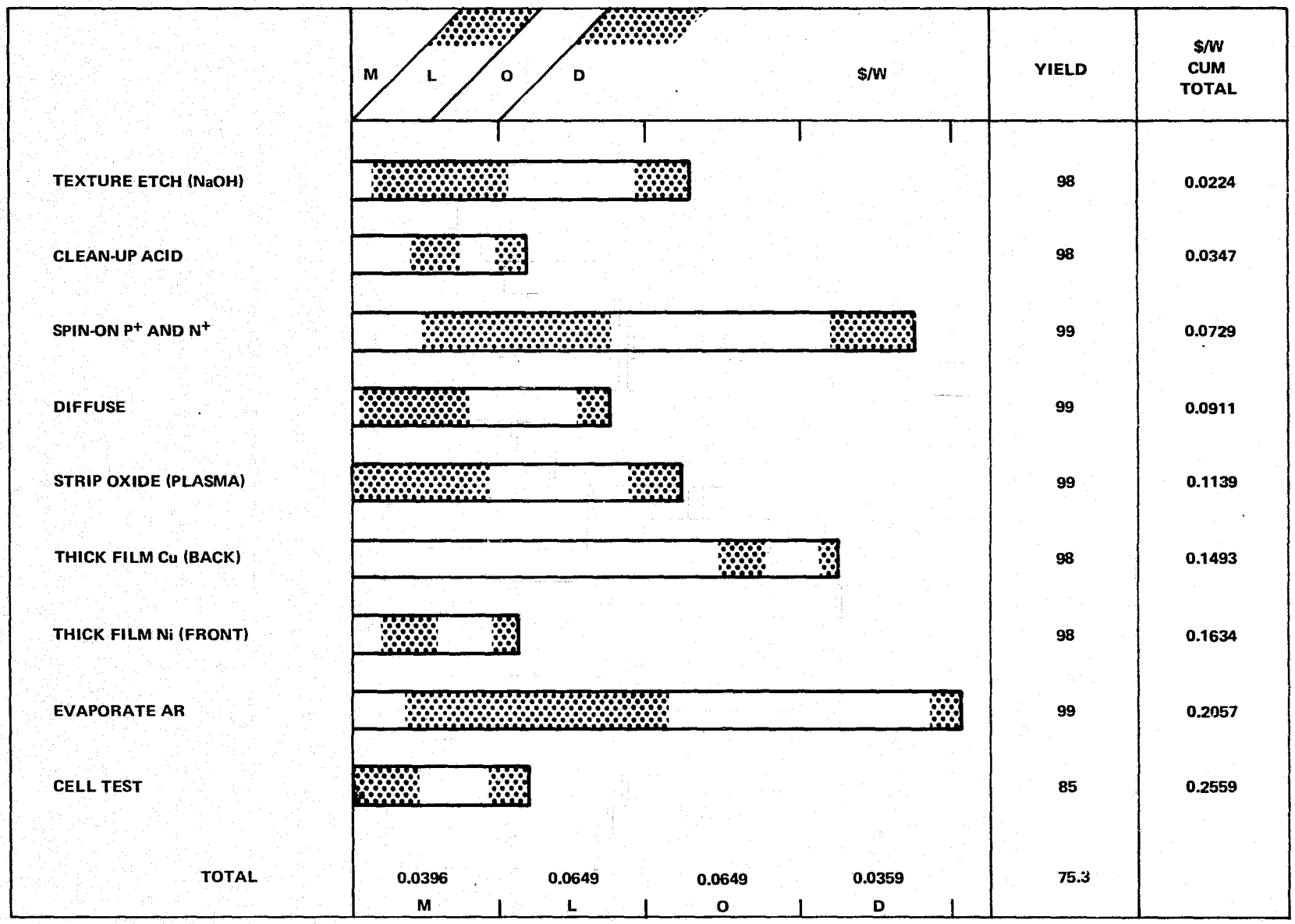


Figure 39. Baseline Low-Cost Cell Process

Several interesting points are evident from inspection of Figure 39. Almost two-thirds of the total material cost is due to the back-side metallization step alone. Since the material cost is directly related to the area printed, a reduction in the area of the back-side metallization should be investigated. The use of spin-on (or spray-on or paint-on) polymer dopant to form the N^+P junction and the P^+ back-side field in one operation is a significant cost reduction.

The two process steps that require alternate backup processes are junction formation and metallization. Figures 40 and 41 give the process flow, process step yield, cumulative yielded cell process and test cost, and unyielded totals for material, labor, overhead and depreciation for Baseline Process – Alternate 1 (Junction), Figure 40, and Baseline Process – Alternate 2 (Metallization), Figure 41. Process steps that differ from the Baseline Process are italicized. All process costs are sensitive to process step and test yields. Improvements in any of these yields will favorably impact cost.

The baseline process and alternates 1 and 2 represent solar cell processes that can be achieved by extensions of today's technology. They do not meet the design-to-cost goals for the LSSA Project goal by more than a factor of two. Labor costs could be impacted by full automation with the ultimate low-cost potential for each process approaching the material cost for that process as a minimum (at infinite throughput labor cost approaches zero and depreciation approaches zero). Material costs will not decrease unless cell efficiency increases. The factor-of-two discrepancy between design-to-cost goals and projected process costs can be overcome by improved throughput and by improved cell efficiency.

Module assembly and test costs present a more serious but not intractable cost barrier. Two module configurations were chosen from the modules discussed in an earlier section of this report. The primary module considered is called the hermetic or LSSA module. This design represents an approach based on a 20-year life requirement. All construction materials are designed to withstand outdoor weathering with minimum degradation. The solar cells are protected from weathering by the module enclosure. All cell interconnects are part of the module fabrication process. Two primary construction materials were chosen, glass, and procelainized steel. These choices are based on cost and durability.

The second option consists of a minimum cost design with no provision made to assure 20-year life. This low-cost option consists of a porcelainized steel substrate and an overcoat of low-cost silicone plastic. Minimum overcoat thickness is used to minimize cost. Studies under Tasks 3 and 5 of the LSSA Project indicate that silicone or plastic overcoats will not provide protection from weathering over long periods of time. The difference in cost between these two options represents the cost incurred to assure weatherability. Further detailed investigation of module construction is necessary.

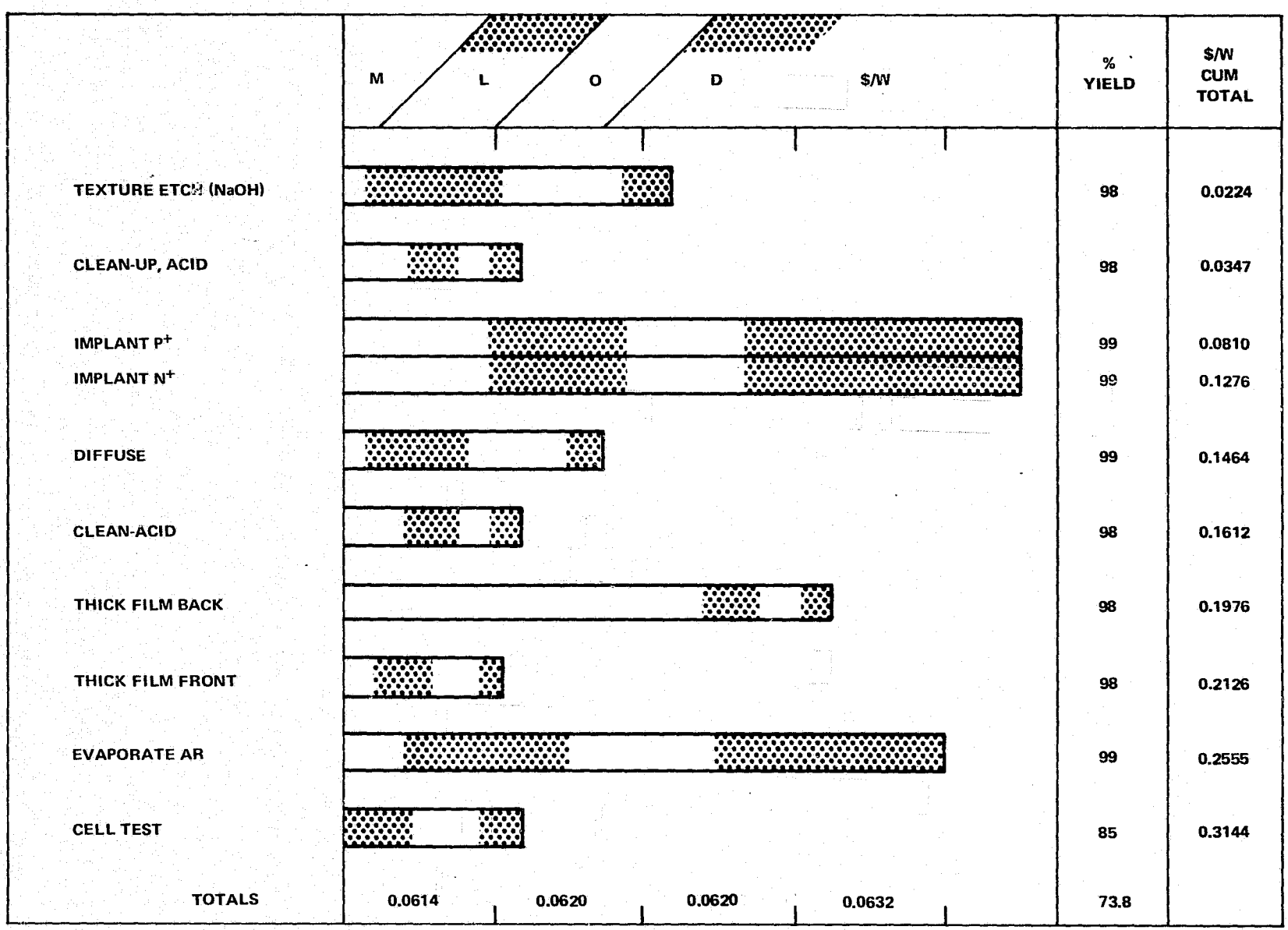


Figure 40. Baseline Low-Cost Solar Cell Process – Alternate 1 (Junction)

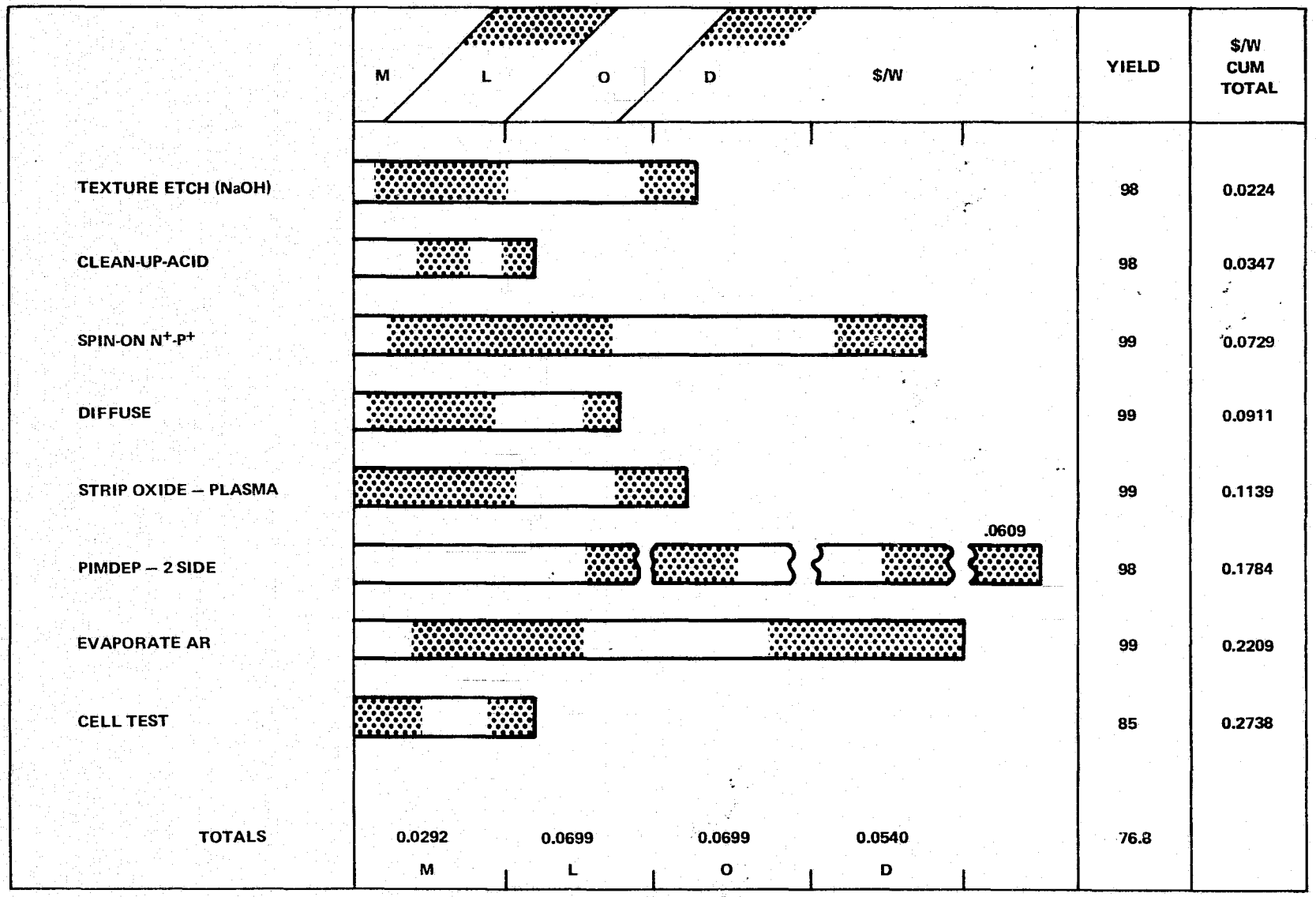


Figure 41. Baseline Low-Cost Cell Process – Alternate 2 (Metal)

In this assessment, all piece parts that go into module construction are treated as purchased material. Some economies could be achieved by fabricating the piece parts in the solar cell module factory. Module add-on costs are given below.

	$/(W)				
	M	**L**	**O**	**Dep.**	**Total**
Hermetic Module	0.247	0.0101	0.0101	0.0048	0.272
Low-Cost Module	0.069	0.0219	0.0219	0.0226	0.1354

The above module add-on costs exceed the design-to-cost goals by a factor of two or three. Since these costs are very sensitive to cell and module efficiency and the final design is still preliminary, this difference from 1985 cost goals is not considered serious.

Overall solar cell process, test, module fabrication and test costs are summarized below for the baseline low-cost solar cell process and alternates 1 and 2 coupled with the hermetic module and the low-cost module.

	$/W (Excluding Si Sheet)	
	Hermetic Module	**Low-Cost Module**
Baseline Low-Cost Cell Process	0.5442	0.4076
Alternate 1	0.6045	0.4685
Alternate 2	0.5627	0.4263

All cost assessments in this report exclude the cost of silicon sheet and are not dependent on the form of the silicon sheet. All costs do assume a minimum cell efficiency of 13.5% at AM1. Silicon sheet costs would have to be yielded through the process.

SECTION III
CONCLUSIONS

A number of detailed conclusions were reached during the course of this investigation. The generalized conclusions at this stage of the study are summarized in this section of the report.

1. **The design-to-cost concept** has been applied to the LSSA Project 1985 cost goal to allocate costs to the various elements in the fabrication of silicon solar cell modules. In order for the program to be 100% successful, the total manufacturing cost must be less than the selling price goal to allow a satisfactory profit margin, return on assets and cash flow. The exact differential depends on external factors, such as tax credits or government subsidies, available at the time of investment. The general principle is valid and useful even without an exact knowledge of these external factors.

2. **Solar cell and module modeling** is a useful tool in the evaluation of solar cell processes and module configurations. An understanding of the effects exerted by various device parameters on cell and module performance allows one to make more quantitative technical judgments.

3. **A new approach to solar cell metal pattern design** using minimum power losses has proven to be an extremely valuable tool in the design of optimized metallization patterns and in the evaluation of front-side metallization technologies. It has been shown that on large-area solar cells, fine-line (12-μm) definition offers very little performance advantage over coarse-line ($> 100\ \mu$m) definition. This conclusion was a significant factor in the choice of screen-printed metal for the baseline low-cost process.

4. **For rectangular solar cells,** limits can be established for maximum cell length and width. The limits are a function of allowable power loss and metal pattern configuration.

5. **For low-cost solar cell processing,** each process step must be capable of high throughput to minimize labor cost and depreciation, and materials costs must be kept to a minimum. Process steps that do not contribute in an additive fashion to the final product, such as cleaning or metal etching, should be avoided whenever possible.

6. **Metallization** is the most expensive of the cell process steps. Metallization costs are a key to cell process cost. Low cost options are screen printed metal and a patterned electroless plating technique, PIMDEP.

7. **Module fabrication** has been identified as a significant cost barrier in meeting the 1985 LSSA Project cost goal. The cost impact of the 20-year life goal is difficult to assess due to the limited data base on terrestrial operating systems. Over-design is probably required in this area. A "hermetic" module configuration has been proposed utilizing a glass superstrate and a porcelainized steel substrate.

8. **A baseline low-cost silicon solar cell process** is proposed along with two alternate versions. Two module configurations are proposed. All of the above use evolution of existing technology and do not require technology breakthroughs.

9. **This contract and other parallel contracts** under the LSSA Project have defined a number of areas that need immediate attention to maintain the thrust of the LSSA Project toward the 1985 cost and performance goals. Key areas related to Automated Array Assembly are contained in the following section of this report.

10. **Assuming silicon sheet costs** $\leq$ 0.25 per watt and resulting cell efficiency $\geq$ 13.5% AM1, automation of existing evolving technology can drive solar cell module factory costs to $<$ \$1.00 per watt, provided a market exists to absorb the factory output.

SECTION IV
RECOMMENDATIONS

The assessment of technology required to fabricate silicon solar cells for a low-cost high-volume factory leads to several key areas requiring more detailed investigation. These areas are outlined below.

A. HIGH EFFICIENCY CELL DEVELOPMENT

All cell and module costs are directly tied to cell and module efficiency. Significant improvement in module costs can be achieved by improvements in cell efficiency. Improvements in cell structure or better control of material and cell parameters can pay major dividends in lower cost per watt. A realistic goal would be AM1 cell efficiency of 20% for a low-cost process.

B. SENSITIVITY ANALYSIS

A sensitivity analysis is required to identify key parameters that affect solar cell performance. These parameters can be related to various process steps and a sensitivity analysis can identify the parameters and the process steps that require close control and monitoring. The sensitivity analysis can also be used to identify process steps that may require particular attention in further process development.

C. LOW COST PROCESS DEVELOPMENT

Some of the process steps included in the Low-Cost Baseline Process or in Alternates 1 and 2 need further development before the full process can be optimized. Individual process steps that need further development are printed metallization, photo impeded metal deposition (PIMDJP) and spin-on polymer dopant diffusion. The process step development needs to be part of an overall low-cost process development.

D. THIN CELL DEVELOPMENT

A substantial cost savings can be achieved if the silicon sheet thickness can be reduced. The cost saving would be in the silicon sheet cost. Thin cell development must be consistent with high cell efficiency and low-cost cell processing to achieve maximum cost benefit. Thin cells should not be developed if the cell efficiency is $< 13.5\%$ AM1.

E. ALL BACK SIDE CONTACT METALLIZATION

Current solar cell technology resembles the state-of-the-art mesa diodes of the 1960 time frame with one contact on the top and the second contact on the bottom. Significant improvement in diode performance was achieved with the advent of planar diodes in the early 1960s. Similar technology applied to solar cells with the contacts on the nonilluminated back side could yield substantial benefits in cost and performance. Module assembly would be simplified with the use of existing high-speed automatic bonding equipment, photocurrent generation would increase due to the elimination of shadowing losses and back side recombination and the surface dead layer could be reduced or eliminated. To achieve maximum benefits, so-called wraparound contacts are not acceptable, rather an entirely new structure is required. This area could yield a step function improvement in cost per watt at the module level and bring projected cost into line with design-to-cost goals.

F. LONG LIFE MODULE DEVELOPMENT

Present solar cell modules featuring printed circuit board substrates and silicone or epoxy encapsulant do not appear to offer a high probability of achieving the 20-year life goal of the LSSA Project. A program is needed to develop and qualify a long-life module similar to the module proposed in this report.

These areas are recommended for further investigation in the immediate future as fruitful avenues of pursuit in the attainment of the LSSA Project goal.

SECTION V
REFERENCES

1. S. N. Rea, *Large Area Czochralski Silicon* (Dallas, Texas: Texas Instruments Incorporated), JPL Contract 954475, Quarterly Technical Report (June 1976), ERDA/JPL – 954475-76/1.

2. *Terrestrial Photovoltaic Power Systems with Sunlight Concentration,* Report NSF/RANN/SE/GE-41894/PR/74/4, College of Engineering Sciences, Arizona State University and Spectrolab (January 31, 1975).

3. J. W. Thornhill and W. E. Taylor, *Demonstration of the Feasibility of Automated Silicon Solar Cell Fabrication,* NASA Final Report CR-135095, Spectrolab, Inc. (August 1976).

SECTION VI
NEW TECHNOLOGY

This contract was directed to an assessment of existing solar cell process technologies and module fabrication schemes. No new technology was developed under this contract.