DEVELOPMENT OF A 1000 V, 200 A, LOW-LOSS, FAST-SWITCHING, GATE-ASSISTED TURN-OFF THYRISTOR

E. S. Schlegel, L. R. Lowry and D. L. Moore

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Project Manager: Gale R. Sundberg
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Project Manager, Gale R. Sundberg
NASA Lewis Research Center
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16. Abstract

This final report gives the results of a program to develop a fast high-power thyristor that can operate in switching circuits at frequencies of ten to twenty kHz with very low power loss. Feasibility was demonstrated for a thyristor that blocks 1000V forward and reverse, conducts 200A, turns on in little more than 2 μsec with only 2A of gate drive, turns off in 3 μsec with 2A of gate assist current and has an energy dissipation of only 12 mJ per pulse for a 20 μsec half sine wave 200A pulse. Data was generated that clearly showed the tradeoffs that can be made between the turn off time and forward drop. The understanding of this tradeoff relationship enabled NASA to select deliverable thyristors with turn off times up to 7 μsec to give improved efficiency in a series resonant DC to DC inverter application.

The physical understanding of gate assisted turn off was improved and this provided the basis for bringing the usual advantages of cathode shunting to gate assisted turn off thyristors.

In order to combine the advantages of gate amplification and gate-assisted turn off three types of bypass diodes were developed and evaluated. Practical feasibility was demonstrated, late in the program, for the device to be made with an integrated bypass diode.

A new light weight package was developed.

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1. SUMMARY

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2. INTRODUCTION

The objective of this program is to design and develop a fast high-power thyristor that can operate at frequencies in the range of ten to twenty kilohertz with a very low power loss. Low power loss has always been important for aerospace applications, and it is becoming increasingly important for energy conservation in non-space applications. Operation at high frequencies is important for aerospace applications because higher frequency components are smaller in size and lighter in weight. However, it is important to consider all of the ramifications of choosing a higher operating frequency because, unfortunately, component efficiencies tend to be lower as the frequency is increased. The reduced efficiency in turn increases the weight required (1) for the larger power generation equipment to provide the extra power and (2) for the vehicle-cooling system which must dissipate the added power. Therefore, for any system, there is a frequency that will minimize the total weight. By improving the efficiency of any component at higher frequencies, the frequency-weight trade-off is improved towards higher frequency and/or lower system weight.

The frequency capability of a thyristor is primarily limited by its turn-off time (τ_q). The turn-off time is the waiting time required, after the thyristor has been commutated out of conduction, before a forward voltage can be reapplied without refiring the thyristor. The device designer has a variety of ways by which he can decrease the turn-off time. Unfortunately, they all involve decreasing the current gains of one or both of the transistors that make up the two transistor analog of the thyristor. Consequently, all the design changes that decrease this turn-off time, that is that make the turn-off faster, make turn-on and conduction more lossy. Thus there is an unavoidable tradeoff between the turn-off time and the turn-on and conduction losses. At the beginning

of this program there was only one known way to significantly relax the stringency of this tradeoff. This way consists of applying a reverse voltage to the gate of the thyristor during the time at which voltage is to be reapplied to the anode. By this means, the current gain of the thyristor can be temporarily decreased during the time that the thyristor is to be turned off without degrading the gain during the turn-on and conduction parts of the cycle. Such a device is known as a gate-assisted turn-off thyristor (GATT).

The target specifications of the contract are given in Table I. The turn-off time specified therein is 3 μsec. This was consistent with the objectives of two preceeding GATT development contracts, NAS12-2198 and NAS3-14394, which were reported in NASA Reports No. CR-120832 and No. CR-121161. This 3 μsec turn-off time was based on an initial objective to operate at frequencies up to 50 kHz. While the capability to achieve 3 μsec turn-off times was demonstrated in all three contracts, work performed during the period of this third contract provided a basis for changing the emphasis on short turn-off times. This change was based on a study, by Westinghouse on this contract, of the tradeoff that could be made between turn-off time and the forward voltage drop. The change incorporated the results of a study by TRW Inc. that showed that increased inverter efficiencies could be attained with GATT's with somewhat longer turn-off times with lower forward drops. Therefore, the later stages of this effort were performed with the understanding that the 3 μsec turn-off time should be relaxed to about 7 microseconds to obtain the best performance from circuit application.

The background that lead to the work on this contract was described in NASA Reports No. CR-120832 and No. CR-121161, which are the Final Reports for the two preceding GATT development contracts. The device is to be used in a series inverter circuit for the conversion of dc power from one voltage level to another. Regulation is provided to maintain the output voltage constant independent of changes in the input

TABLE I

Target Specifications

Symbol	Description	Specifications
V_{RRM}	Minimum reverse blocking voltage.	1000V
V_{DRM}	Minimum forward blocking voltage.	1000V
$I_{T(rms)}$	Maximum rms forward current.	200A
V_{TM}	Maximum steady state forward voltage drop for conduction of 200A.	2.5V
t_{on}	Time required to reach V_{TM} after initiation of current conduction with a rate of rise of 100A per microsecond and application of a gate signal of 2.0A for ten (10) microseconds.	2 µsec
I_{RRM}	Maximum reverse leakage current at 1000V.	10 mA
I_{DRM}	Maximum forward leakage current at 1000V.	10 mA
I_G	Maximum gate current to fire at V_{DRM} = 30V.	200 mA
V_G	Maximum gate voltage to fire at V_{DRM} = 30V.	4V
I_h	Minimum holding current.	200 mA
t_q	Maximum time after anode current has reached zero before anode voltage can be reapplied @ the maximum rate of rise of voltage (dV/dt) as stipulated below and a maximum gate signal of 2.0A for 3 µsec.	3 µsec
dV/dt	Maximum rate of rise of anode voltage.	400V/µsec
E pulse	Allowed dissipation per pulse (20 µsec half sine wave with a 200A peak).	12 mJ
dI/dt	Maximum rate of rise of current concurrent with and after a gate signal of not more than 3.0A.	100A/µsec

voltage or output loading. The use of natural commutation minimizes the current and voltage transients thereby increasing the efficiency and reliability of the circuit; it also minimizes electromagnetic interference problems.

Other work on GATT devices includes an experimental 600V, 100A, GATT, with a t_q of 2 μsec made by the Westinghouse Brake and Signal (type D1171),[1] and a 1200V, 400A GATT with a t_q of 6 μsec made by the Mitsubishi Electric Corporation.[2,3]

The scope of the present work included:

1. A broad review of the possibilities by which the turn-off time and energy loss per pulse might be decreased.
2. An experimental study of the electrical behavior of fast turn-off thyristors.
3. The development of a better model for gate-assisted turn-off.
4. The design and fabrication of a new family of GATT devices based on the improvement in understanding of thyristor turn-off.
5. The evaluation of devices in this new design.

The information reported herein provides both a theoretical understanding, and an empirical measure, of the present state-of-the-art of high-voltage, high-current GATT's. This information can be used by those involved in the design of low-loss, high-power, high frequency circuits of the type described by Schwarz.[4] The devices made on this contract are being used in a thyristor power processor for a 30 cm mercury electric propulsion ion engine as described by Beiss et al.[5]

The work was done by investigators of the Research and Development Center of the Westinghouse Electric Corporation, Pittsburgh, Pennsylvania, in cooperation with the Westinghouse Semiconductor Division, Youngwood, Pennsylvania. Thyristors were fabricated in the production facilities of the Semiconductor Division using modifications of standard production processes. Special modifications and all device testing and behavioral studies were conducted at the Research Laboratories.

The value of the work done was significantly enhanced by direct interaction, encouraged by NASA, with those at TRW who are involved in the development of a circuit in which these thyristors are to be used.

3. DEVICE DESIGN

3.1 Background

The preceding work, performed by Westinghouse Electric Corporation and supported by NASA,[6,7] can be summarized as follows.

The first GATT development program, from the middle of 1969 to the middle of 1970, resulted in the demonstration that devices could be made that blocked 600V, and carried 50A of average anode current with a V_{TM} of no more than 2V. They had a turn-off time, tq, of 2 μsec tested with a gate-assist gate bias of -10V in series with 10 ohms, all measured at 100°C. The cathode-emitter was of mesa construction and, therefore, had widely varying leakage currents between individual emitter fingers. To produce usable devices with this process, it was necessary to test each emitter finger individually and to weld a raised contact to each individual good finger so that the device could be packaged without contacting the leaky fingers. This was clearly not a good manufacturable design.

The second GATT development program, from about September 1971 to November 1972, yielded devices that blocked 1000V and carried 100A of average anode current with a V_{TM} of no more than 2V. The turn-off time was less than 2 μsec, tested with a gate-assist bias of -20V through a gate-assist source impedance of no more than 1 ohm. The measurements were taken at 100°C. This device was planar and manufacturable, but it had five disadvantages:

1. To achieve the desired turn-on speed, the gate turn-on current had to be $\geq$ 15A.
2. To achieve the desired turn-off time, the gate assist current had to be > 10A.

3. If this high level of gate-assist current were applied before the anode current had been commutated to zero, the thyristor was likely to be permanently damaged.

4. The energy loss per pulse was quite high, e.g., $\sim$ 30 mJ.

5. A constant gate bias was necessary to prevent firing of the device by an applied dV/dt. Without a gate bias, the dV/dt rating was much lower than the specified 400V/μsec.

It was the objective of this contract (GATT III) to create a thyristor in which these five disadvantages are overcome.

3.2 Design of GATT III

3.2.1 Turn-on

3.2.1.1 Gate Amplification

In the previous GATT's a gate turn-on drive current of > 15A was required to achieve fast low-loss turn-on. In GATT III, gate amplification was incorporated into the device so that it could be fired well with only 2A of externally applied gate drive current.

3.2.1.2 Cathode Edge Length

At the beginning of this contract there was no definitive information on how the length of the cathode edge (the boundary between the cathode and the gate) affects the speed and losses of the turn on. It was not known whether an increase in the length of this periphery, for a given set of operating conditions, would:

1. Increase the energy loss because the gate drive per unit length is reduced, thereby causing a slower turn on;

2. Decrease the energy loss because the current density and therefore the forward drop are at a lower level; or

3. Cause no change because the effects of (1) and (2) cancel out.

An extensive amount of effort was expended to answer this question. First, turn-on voltage and current waveforms were measured on the circuit shown in Fig. 1 for a large number of variations in device design and operating conditions. These measurements indicated that the cathode peripheral length has little influence on the turn on energy loss.

There was considerable uncertainty about whether this was a definitive result because:

a. There is always uncertainty in the accuracy of a small ($\sim$ 3V) voltage being measured within a few tenths of a microsecond after a much higher voltage ($\sim$ 200V) was present on, and saturating, the amplifier of the oscilloscope.

b. It is difficult to be certain that no emf's are developed in the voltage probe leads in the vicinity of the line in which a dI/dt of the order of 10^8A/sec exists.

c. Other variables such as the shunt patterns and the spacing between the shunt and the edge of the cathode were different. Also the diffusion profiles may have been different.

d. The sample size was small, one device for each cathode edge length, because of the limited amount of time for such work.

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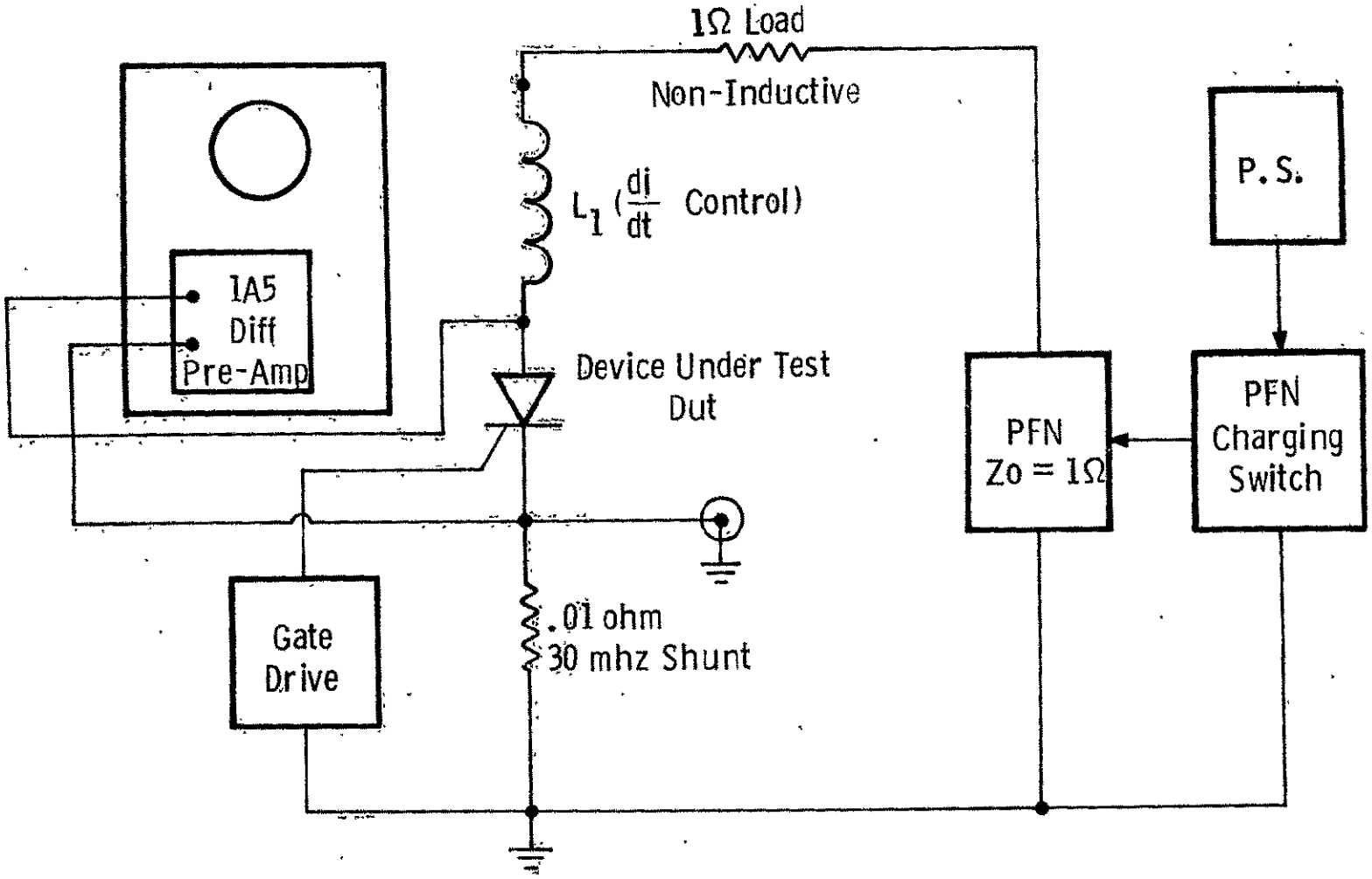


Fig. 1 — Turn-on test circuit

To minimize the effects of uncontrolled variables, the following technique was developed by which the effects of varying the cathode edge length were simulated on a single device. To understand this approach, consider the following thought experiment. Take two identical thyristors and compare how one of them would behave while being turned on in a given circuit with a given set of conditions with how both would behave, perfectly paralleled, in the same circuit with the same conditions.

The device would see the following differences:

a. In the parallel case, both the gate-drive-current and the anode-current densities per unit of cathode edge length would be half their values in the single-device case.

b. The losses in the parallel case occur over twice the cathode edge length of that of the single device case.

Note that, if the loss per unit of edge length were the same in both cases, the total loss in the second case would be twice that of the first case. Based on this, one should be able to test a single device under two proportionate sets of gate current drive and circuit-limited-anode dI/dt to simulate differences in cathode edge length. The losses measured under the two sets of currents must be scaled in proportion to the simulated difference in cathode edge length. Turn-on losses were measured using this technique, and again there appeared to be no significant effect of the edge length.

There still was the question of whether the voltage waveforms might be significantly in error and so an apparatus was built in which the thyristor could be operated under typical conditions on a heat sink while the dissipated energy losses were measured with a calorimeter. Details of this are given in Section 4.3.

In summary, a strong effort was made in three different ways to determine how to design the cathode peripheral length and the results have shown no significant effect of the cathode edge length on the turn-on losses. Given this result, the device was designed to have a fairly long cathode periphery because after the initial turn-on transient, it is known [8,9] that the spreading velocity increases more slowly than linearly with the current density. Therefore, once the device has turned on at the emitter edge its conducting area is larger at any point in time during the plasma spreading phase if the edge being initially fired is longer. A similar conclusion appears to have been found by Shimizu, et al.[3]

3.2.1.3 Diffusion Profile

A third effect on turn-on speed and losses is the current gain designed into the axial distribution of the impurity density and the thickness of the layers in the four layer structure. To the degree that one can, consistent with the requirements for a fast turn-off time and for the required blocking voltages, one should design for a high current gain. This was also a difficult area to know how to design the device. One cannot know theoretically whether the tradeoff between turn-on losses, conduction losses, and the turn-off time is improved or degraded by a design change that increases the current gain. One knows that a diffusion layer change that increases the current gain will improve the turn-on speed and loss but will degrade the turn-off time. One knows that such a design change would require a somewhat different but unknown carrier lifetime level for the optimum tradeoff of V_{TM} and t_q. Thus, it was not possible to know at the outset of this program how to design the thicknesses and impurity profile of the device for an optimum trade-off.

An extensive experiment involving three impurity density profiles and stepped lifetime control provided the means for improving this tradeoff. The details of this were published in the paper that constitutes Appendix A of this report.

This experiment shows that the effects of a change in the diffusion profile and base thickness that increases the current gain improves the $t_q - V_{TM}$ tradeoff at the fast turn-off, low lifetime part of the curve and degrades it at the more conventional higher lifetime end of the curve. A possible explanation of this is that in a device with high lattice-defect-determined lifetime, the turn-off speed is sensitive to this lifetime, while the conduction losses are mainly dependent on Auger recombination which is hardly sensitive to the lattice-defect-determined lifetime. On the other hand, in a device with a low lattice-defect-determined lifetime, Auger recombination is less significant and the losses are sensitive to the lattice-defect-determined lifetime. In this case, the turn-off speed becomes insensitive to lifetime because it becomes limited by the reverse recovery time.

3.2.2 Turn-off

3.2.2.1 Cathode Shunts

In the early years of GATT development, it was believed that the effectiveness of gate assist current was due to a sweep out of excess carriers that decreased the reapplied-forward-voltage-induced displacement current. An experimental investigation during the early part of this program yielded the finding that this was not the reason for the effectiveness of gate assist current. Instead, it was found that the effect of gate assist and its driving voltage is to prevent a forward voltage from being created on the cathode junction. The details of this have been published in References (10) and (11) which constitute appendices B and C of this report.

Once it is understood that the effect of the gate assist signal is to prevent the formation of forward voltage rather than to sweep out charge, the design of a GATT takes a different course. First, one can use cathode

shunting. Shunts would degrade the sweep-out of excess carriers but they strengthen the opposition to forward voltage on the cathode junction. Thus, one need not give up the valuable and well-recognized advantages of shunts that are used in nearly all thyristors today. (Even at the time of the writing of this report, there is no other known GATT design that has shunts.) First, shunts give the GATT a high dV/dt rating without the need for a continuous negative gate signal to protect the device against firing by spurious transient voltages. Second, shunts help to decrease the turn-off time by decreasing the current gains at the low current levels at which a dV/dt would refire the thyristor. Third, and perhaps most important, shunts prevent the cathode current from being pinched in to the middle of the emitter fingers in the manner similar to second breakdown in which transistors or non-shunted thyristors are very subject to failure. The fact that shunts prevent current pinch failures makes it possible for significantly lower gate voltages (that is, 1-3V instead of 10-20V) to be used to prevent the development of forward voltage on the cathode junction.

The optimum sheet resistivity for the p-base is dependent on whether the cathode is shunted. In the case of no shunting, a relatively low sheet resistivity is necessary to allow the negative gate voltage to "reach" to the central portion of the cathode junction without requiring a large voltage (approaching the avalanche voltage) at the edge of the junction.

On the other hand, if there are cathode shunts, the cathode cannot be forward biassed in the central region and a negative gate current through the lateral resistance of the p-base causes IR drops that oppose forward voltages from appearing on the rest of the cathode junction. In this case, high sheet resistivities in the p-base make the gate assist current more effective for opposing the forward voltage.

One should ask the question here whether an increase in the sheet resistivity produces a greater improvement in the effectiveness of gate assist current than the degradation that it causes in the non-gate assisted turn off time. This was another important question that could

not be answered theoretically and had to be answered experimentally. The answer depends on the operating conditions of the device. For operating conditions in which two amperes of gate assist current were used, a net gain was achieved by increasing the lateral sheet resistivity of the p-base. At higher gate-assist currents, the advantage would be even greater.

3.2.2.2 Lifetime Control

In the early stages of the program several attempts were made to compare the lifetime killing properties of gold diffusion with those of electron irradiation to determine which would yield the best $V_{TM} - t_q$ tradeoff. It quickly became apparent that this investigation would require an effort that was beyond the resources of this program. It is a very complex area because it is difficult to compare one type of lifetime control with another unless an extensive effort is made to optimize both processes. In the final month of this program a published paper [12] has shown that gold diffusion may have an advantage over electron irradiation for optimizing the tradeoff between the turn-off time and turn-on and conduction losses. While there is reason to hope that such an advantage might be found due to differences in the level in the energy gap and in the capture cross section, it is still very difficult to compare the two. It is well known that gold can exist both interstitially and substitutionally in the silicon lattice and that the final state is very sensitive to how it was diffused and annealed. Also, gold is gettered by the phosphorus on the cathode side and its distribution is therefore non-uniform; this non-uniformity also depends on the heat treatment. Furthermore, gold cannot be put into finished fusions in precise steps to optimize and tailor the device. Finally, when one uses gold instead of electron irradiation there is a greater probability that compensation of the dopant density will be significant. Therefore, one must be careful not to confuse an effect on impurity density with one on lifetime.

3.2.3 Bypass Diode

The combination, in a single thyristor, of gate amplification and gate-assisted turn-off or gate turn-off (GTO or GCS) confronts one with a problem. In order for a low gate current, of say 50 mA, to turn a thyristor on, the resistance in the p-base under the auxiliary cathode must be at least 0.7V/0.05A = 14Ω. (The 0.7V is the voltage needed to cause the cathode to start emitting.) On the other hand, when a thyristor is to be turned off with a gate-assist current of 2A, as called for in the contract, this 2A through 14 ohms of resistance produces an IR drop of 28V. (The need for a much larger gate current at turn off than at turn on is because only the turn on current can be amplified.) This 28V is higher than the avalanche voltage of the cathode junction. The high energy density in this avalanche is enough to melt silicon and degrade the auxiliary cathode junction. To overcome this problem, it is necessary to bypass the resistance of the p-base under its auxiliary cathode when gate-assist current is drawn. On this contract, this has been achieved by three different approaches.

3.2.3.1 Diode Mounted in Package

In one approach, which was developed on a separate Westinghouse program, a small diode is soldered in the package as shown in Fig. 2. This diode contacts to the main gate and the floating gate as shown. This diode carries a negligible amount of forward current when turn-on current is applied to the main gate. On the other hand, when gate assist current is drawn from the main gate lead, this current passes through the forward biased bypass diode and prevents the occurrence of avalanche in the auxiliary cathode junction. This approach was demonstrated on devices similar to those of this contract on a parallel Westinghouse program, and later in 35 thyristors that were purchased by NASA on Contract No. NAS 3-19097 and finally in the first twenty devices that were delivered on this contract. This approach appeared to be practical initially but it was found to suffer from a long term reliability problem. The diode contact to the floating gate became erratic

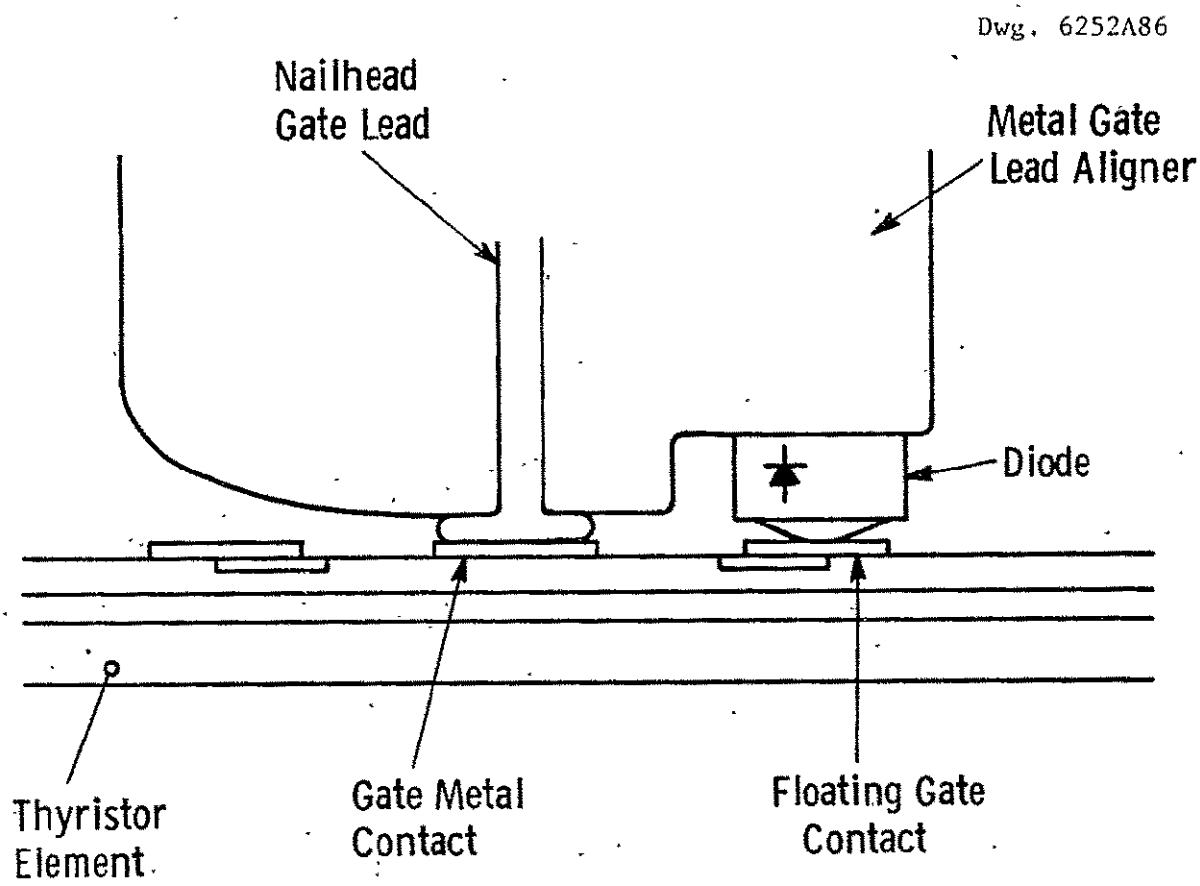


Fig. 2 —Sketch of package modification with bypass diode

and in some cases opened. An investigation revealed that the mound of solder on the diode, which was necessary to provide a raised area to contact the floating gate contact, was subject to cold flow and the pressure of the contact diminished with time until eventually effective contact was lost. (This is discussed further on page 59.) Another problem with this approach was that when the supply of diodes that were used in the beginning was consumed, no supplier of similar rugged diodes could be found.

3.2.3.2 Diode Built into the Thyristor Fusion

Ultimately the best approach will be to build the bypass diode into the silicon slice. This structure is shown in Figs. 3 and 4. As shown in Fig. 4 the diffused auxiliary cathode is segmented into two parts, A1 and A2. These parts function just like the standard amplifying gate. Two bypass-diode diffused regions, B1 and B2, are formed at the same time as the diffusion of the main and auxiliary cathodes.

There are three features to be noted about the construction of this bypass diode. First, note that the metal overlaps the opposite side of the diffused region from that of the auxiliary cathodes. This clearly creates a diode polarity opposite to that of the auxiliary cathode. Second, there are small etch pits, E, between the segmented circular diffused regions. These etch pits prevent gate current from bypassing the auxiliary cathode during turn-on. Current that bypasses the auxiliary cathode is wasted and is not effective for fast, low loss turn on. Third, there is an additional diffused layer or lip, which helps to prevent the bypass diode from refiring the device during the gate-assisted turn off. This is sketched in Fig. 5. The function of this lip fusion is to cause the injection from the bypass diode to occur in an area in which the npn current gain is low so that it does not fire the thyristor. To understand the need for this, consider what would happen if this npn current gain were not low. In this case, when current is drawn out the main gate, most of this current involves electrons being injected into the p-base. Many of these

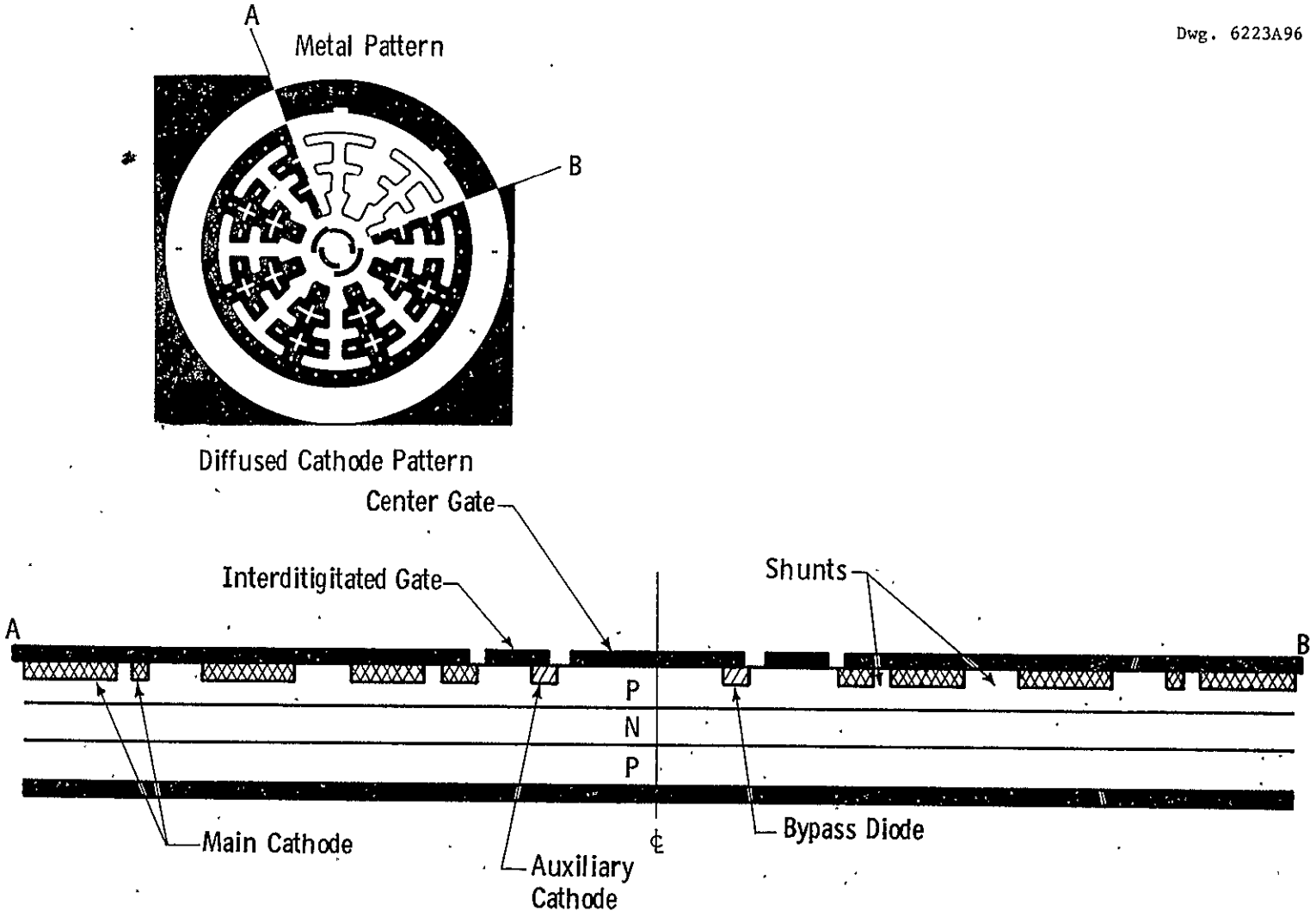


Fig. 3 — Thyristor structure with an integrated bypass diode

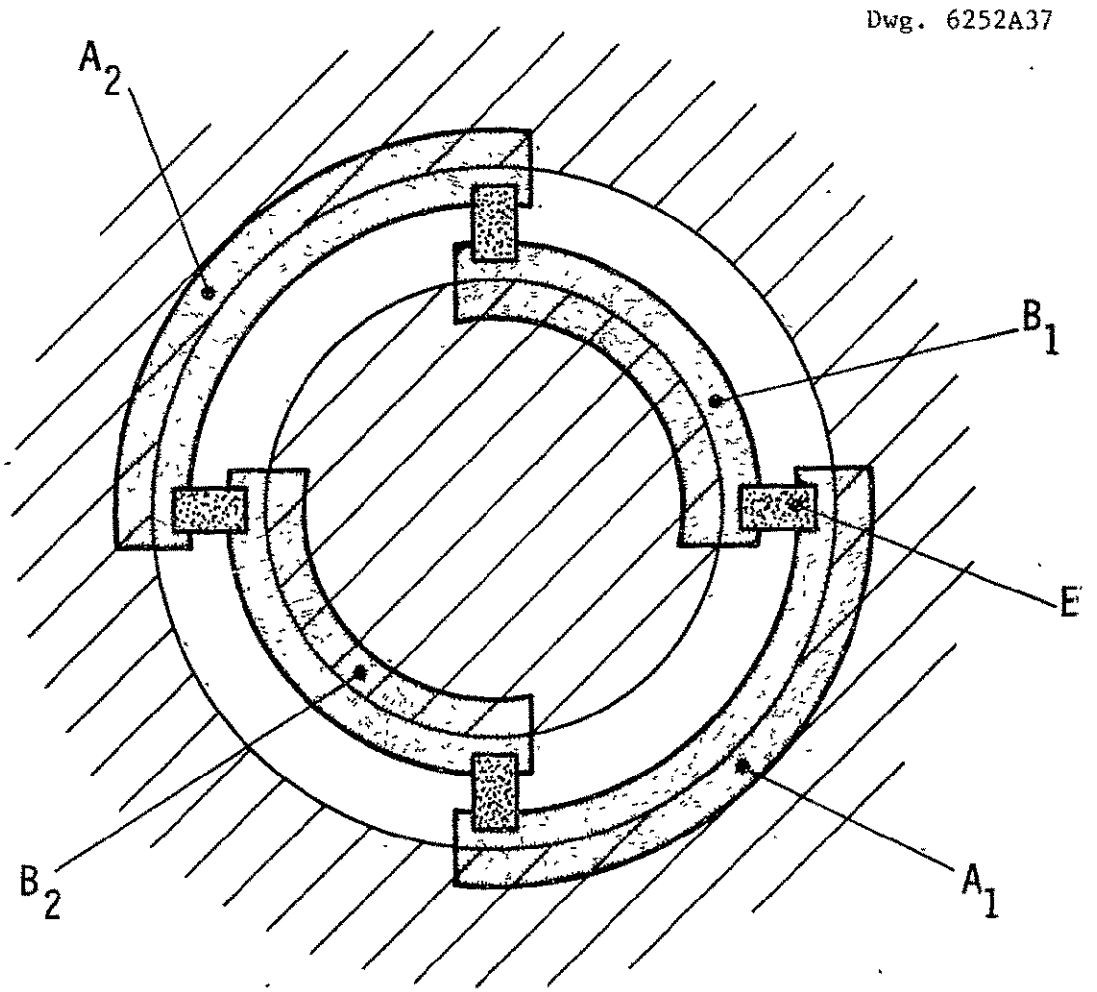


Fig. 4 —Top view of gate having both gate amplification and a bypass diode

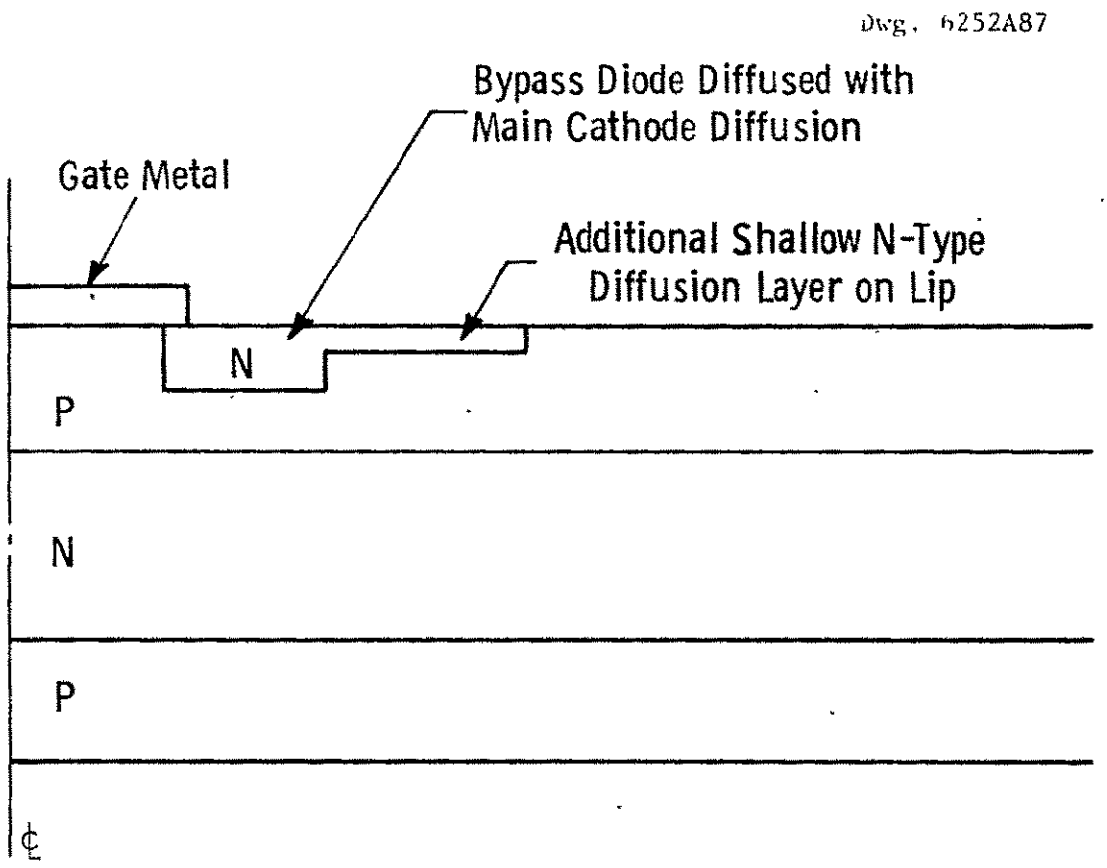


Fig. 5 —Sketch of modification of integrated bypass diode to prevent injected electrons from firing the thyristor

electrons reach the forward blocking junction and drift to the n-base. These electrons are base current to the pnp transistor and partially turn it on. The impedance of the cathode circuit which is designed to carry several hundred amperes is lower than that of the gate circuit which was only designed to carry a few amperes. Therefore, the anode voltage of several hundred volts drives the current being carried by the pnp transistor mostly through the cathode. This current has the polarity to forward bias the cathode junction and fire the thyristor.

To prevent the gate-assist current from firing the thyristor in this manner, a means had to be developed for minimizing the proportion of gate-assist-current-induced electrons that reach the forward blocking junction. This was done by building the bypass diode in the form shown in Fig. 5. This design forces the injection of electrons from the bypass diode to occur over a larger area and in a region where the p-base width is wider. Such widening of the p-base decreases the transport factor for electrons through the p-base and decreases the injection efficiency for electrons into the p-base.[13] The increase in the emitter area increases the amount of recombination that occurs in the space charge region of this bypass diode emitter-thereby further decreasing the injection efficiency for electrons. The injection efficiency and transport factor are both further reduced by area-selectively decreasing the lifetime under the extended bypass diode region by means of a masked electron irradiation.

3.2.3.3 Diode Soldered to the Thyristor

The third approach for making the bypass diode was to solder the diode to the thyristor fusion. In this case two diodes were soldered to the floating gate metal and then a silver jumper that had been photolithographically etched out of a 0.15 mm thick silver sheet was soldered to these diodes and to the center or main gate. Photographs of this construction are shown in Fig. 6. This design became the design of choice near the end of the program for direct application in a dc-dc inverter design because it combined reliability with the ability to use devices similar to those made in production.

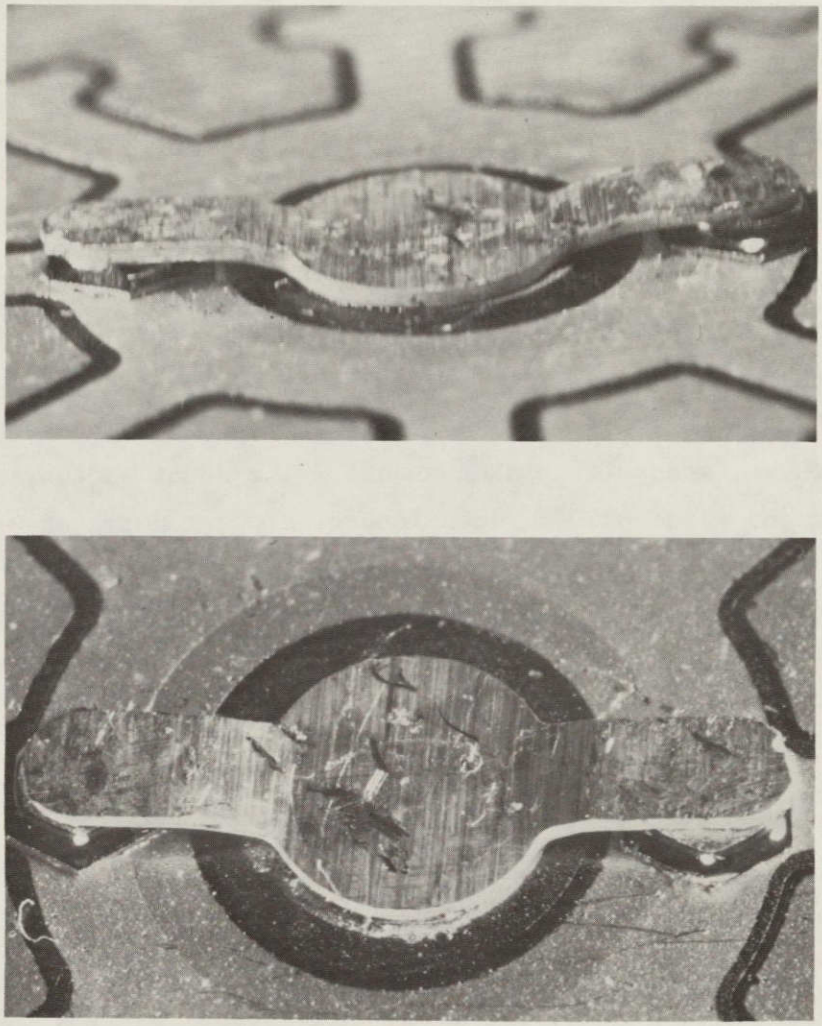


Fig. 6 Two views of the bypass diodes and jumper contact bonded to the thyristor.

3.2.4 Cathode Shape

Among the design implications of the physical model for turn off which is described in Appendix B are:

1. Minimize the ratio of gate area to the peripheral length of the edge of the cathode.
2. Minimize the cathode line width.
3. Make shunts continuous lines with a minimum of corners.

Based on these implications a new mask set was designed. The phosphorus diffusion mask is shown in Fig. 7. As shown the gate area is made as small as practical. The cathode lines were only 0.25 mm wide and are continuous without corners or broken shunts. The shunt widths are 0.25 mm on the mask and about 0.20 mm when lateral diffusion is taken into account. The gate metal lines are 0.30 mm wide.

4. TEST CIRCUIT DEVELOPMENT

4.1 Introduction

Most of the test circuits used in this program were described with detailed circuit drawings on pages 29-60 of the final report of Contract NA53-14394, i.e., NASA report number CR-121161.

4.2 Turn-on Circuit

The turn-on circuit is shown in Fig. 1 herein and in more detail on pages 42 to 48 of NASA Report CR-121161. It consists of a pulse forming network that is charged and then discharged through the thyristor under test. The anode voltage and anode current waveform are observed on an oscilloscope. Turn-on switching losses can be calculated from these waveforms.

Unfortunately, it seems to be a universal problem with this approach that one can never be sure that the voltage waveform is accurate because of the following:

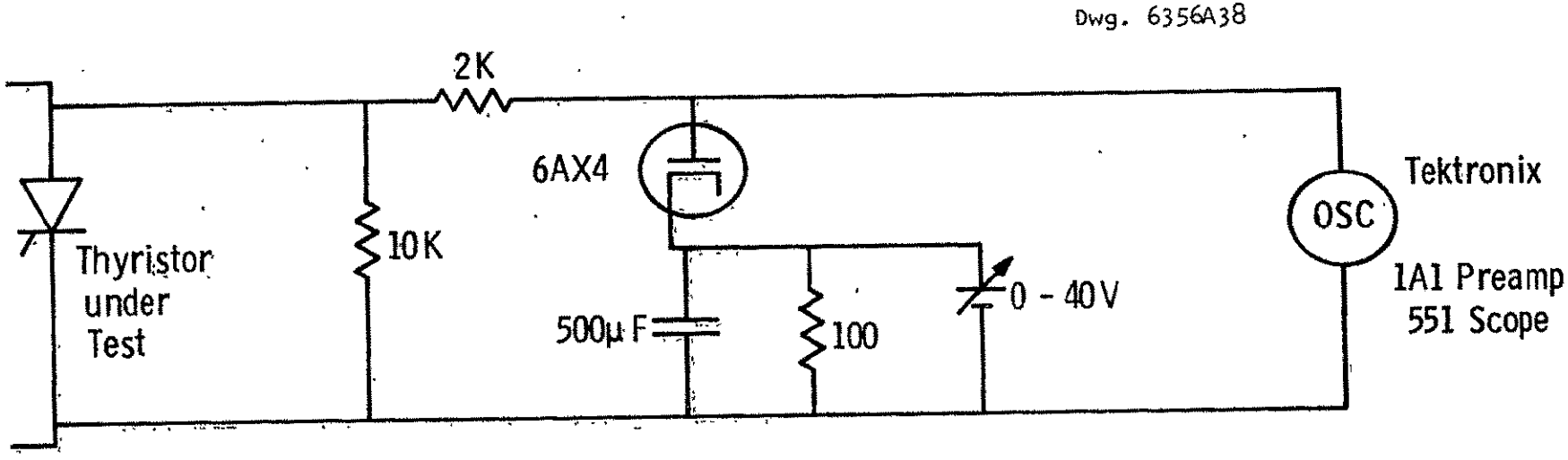
1. If the anode voltage being switched from is as high as the normal operating voltage, the preamplifier of the oscilloscope must be overdriven and saturated so that, at turn-on, voltages of 0-5 volts can be read. This saturation of the preamplifier can produce erroneous readings. Sometimes this source of error is minimized by switching the thyristor on from a much lower voltage, say 30V. In this case, while the voltage waveform may be correctly measured, it may be significantly different from the one that occurs when the thyristor is switched on from a higher voltage.

2. The environment of the device under test includes very high dI/dt and dV/dt levels. It is very difficult to be sure that neither capacitive nor inductive coupling has influenced the voltage waveform that is measured.

To avoid possible errors due to overloading of the preamplifier a second piece of equipment was built to improve the accuracy of the voltage measurement during turn-on of the thyristor. This consisted of a voltage clipping circuit to limit the voltage applied to the oscilloscope preamplifier. Figure 8 is a schematic diagram of the clipper circuit. The quality of the data from this circuit was checked by determining that the part of the waveform to be measured is independent of the voltage level at which the waveform is clipped. The key component of the clipper circuit is the fast recovery diode. Several solid state diodes were examined and rejected as being too slow, and satisfactory results were finally obtained with a 6AX4 vacuum tube diode. There was good agreement between the data from the calorimeter and that from the turn-on circuit with the clipper.

4.3 Calorimeter Set-Up

In order to measure the losses more directly a circuit was built to be used with a calorimeter. The heart of this equipment is a calorimeter that measures the heat generated in the thyristor while it is being operated under conditions similar to those of the circuit in which it is to be used. Figure 9 is a schematic diagram of the circuit that powers the thyristors for the calorimetric loss measurements. Figures 10 through 12 are photographs of this equipment which measures the sum of the turn-on and conduction losses of a half sine wave of 20 μsec pulse width. Reverse recovery losses are negligible because the reverse voltage on the device under test is limited to less than a volt. Forward recovery losses are negligible because the interval between pulses is long. The pulse height can be selected using three sets of inductors and capacitors that provide for either 50, 100, or 200 A when the device is switched on from 400 V.



Clipper circuit for measuring dynamic forward drop

Fig. 8

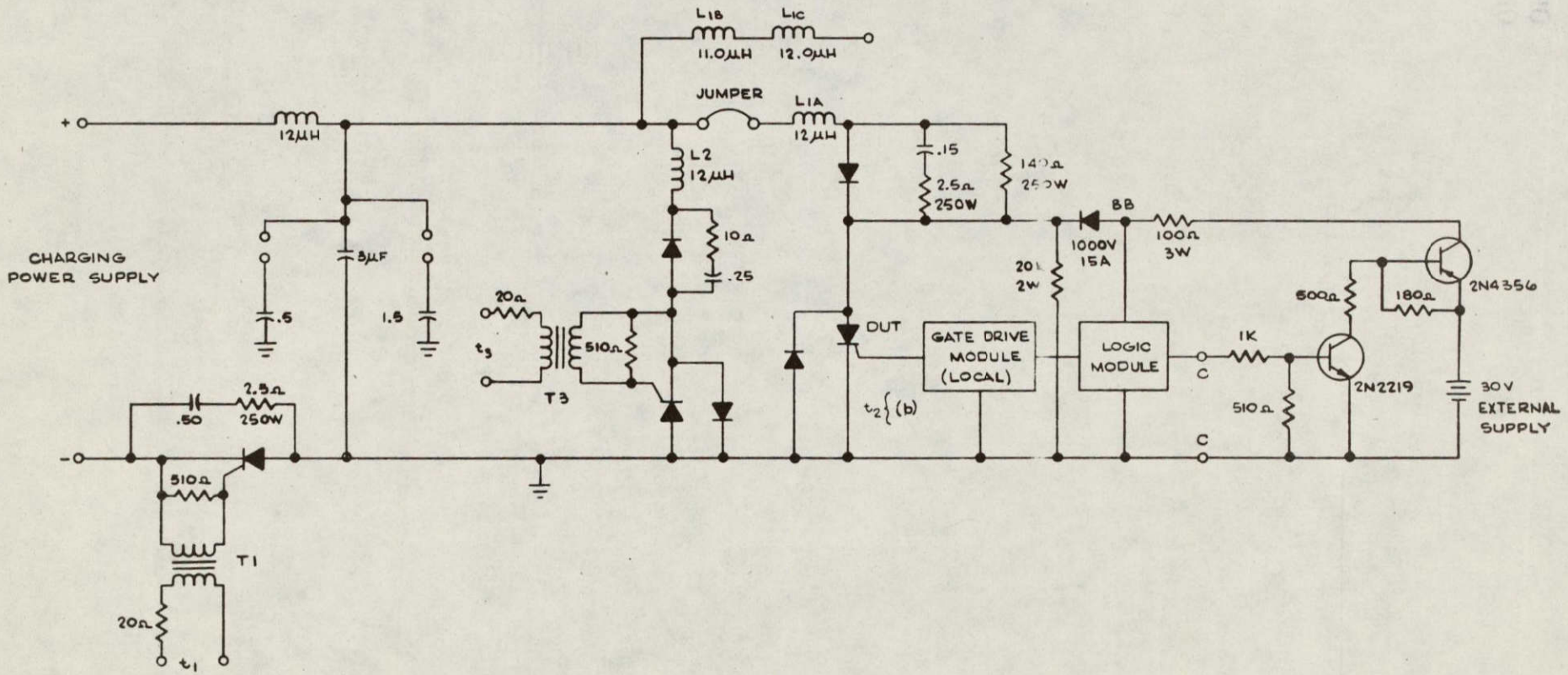


Fig. 9 - Circuit for Powering Thyristors for Calorimeter Measurements.

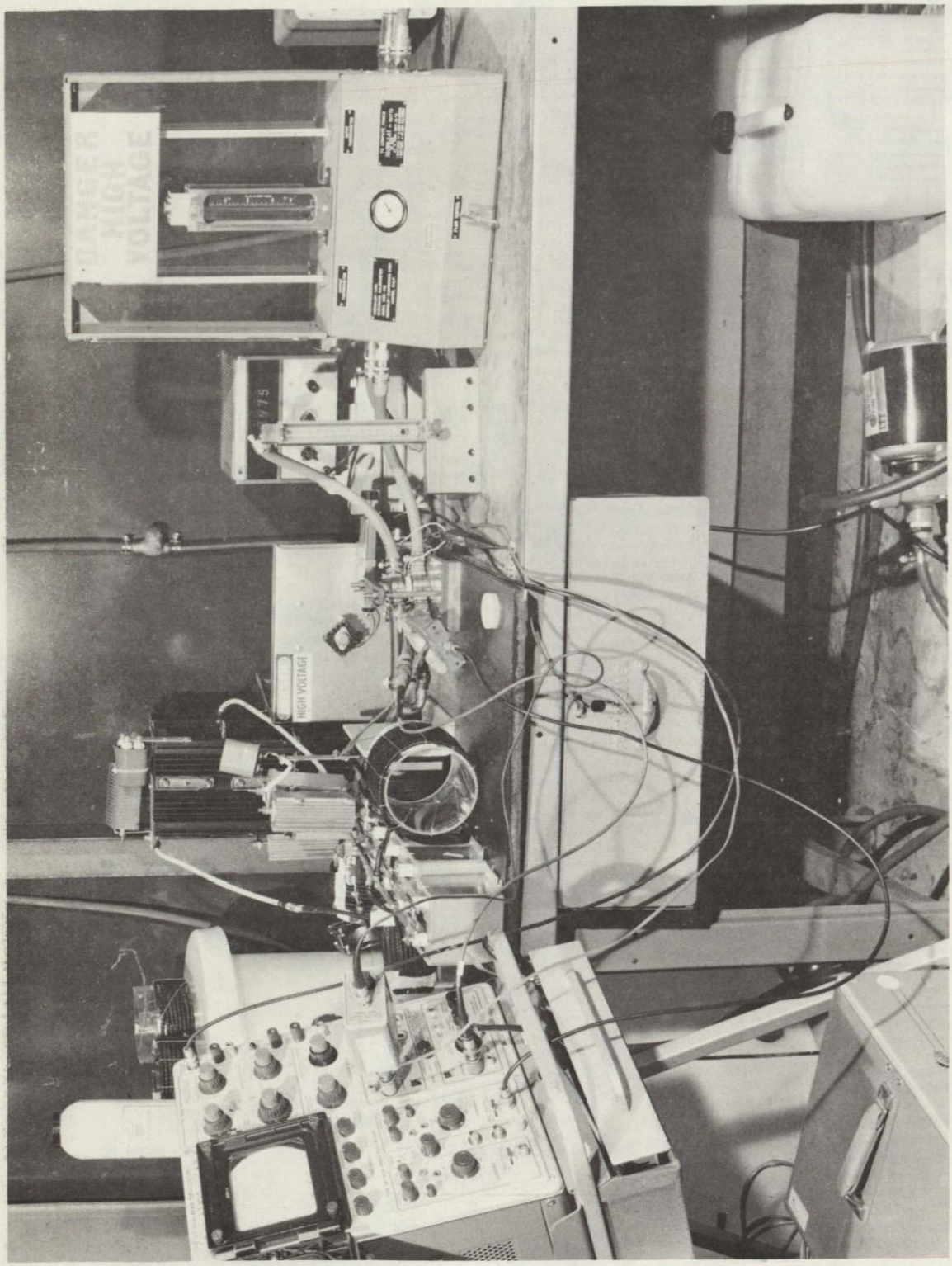


Fig. 10 Overall View of Calorimeter Set-up.

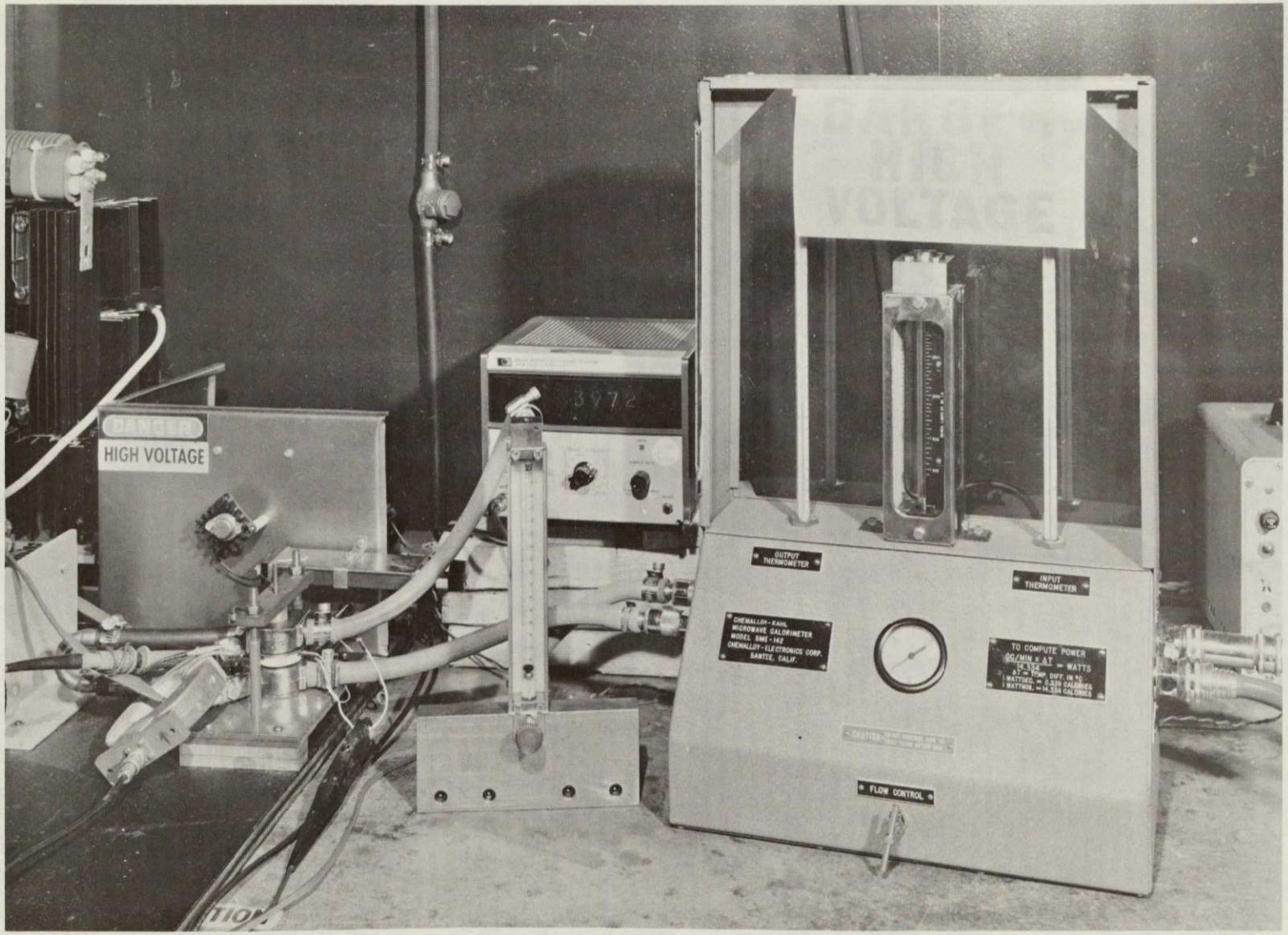


Fig. 11 View of Sample Mounting and Calorimeter.

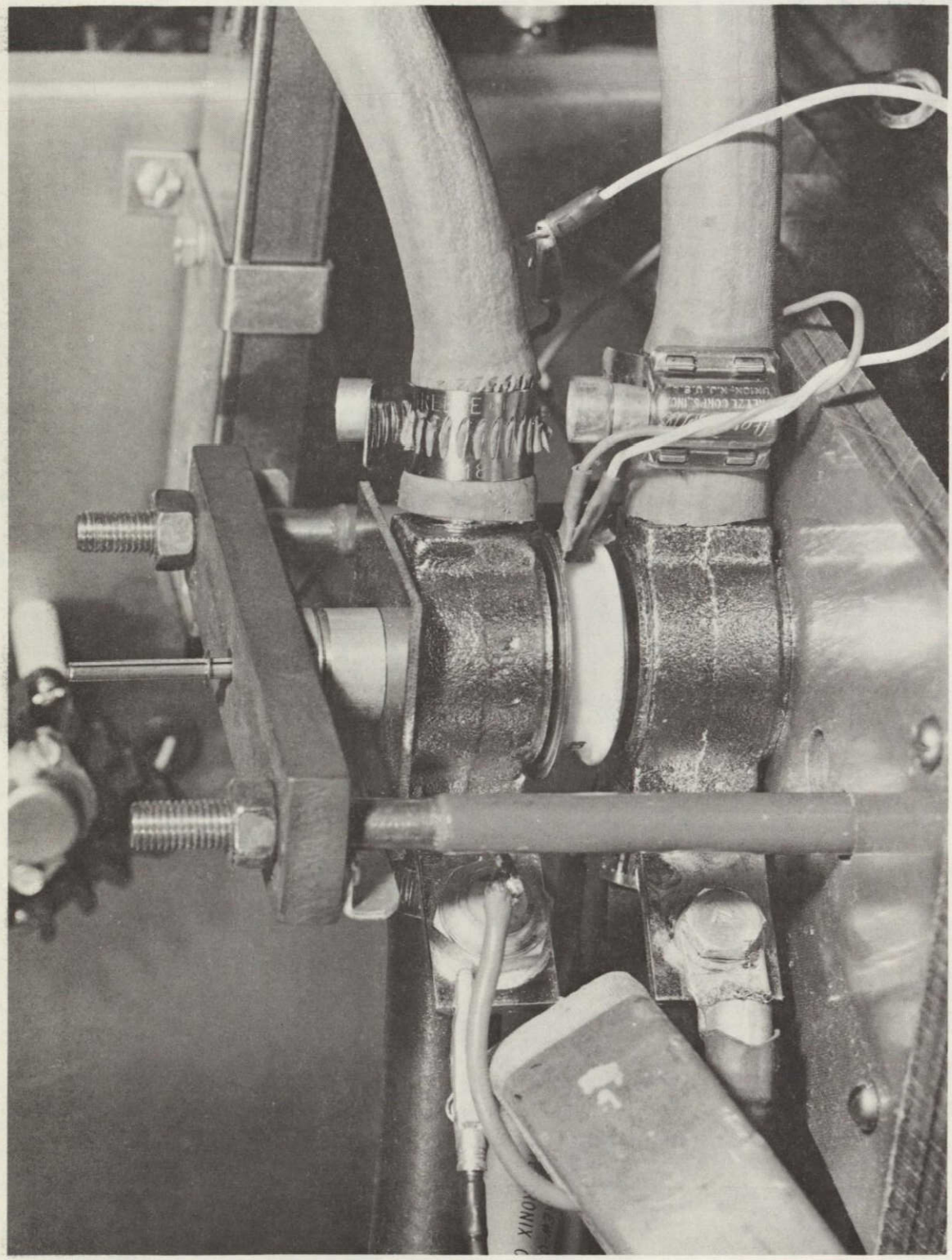


Fig. 12 Close-up View of Sample Mounted in Heat Sink.

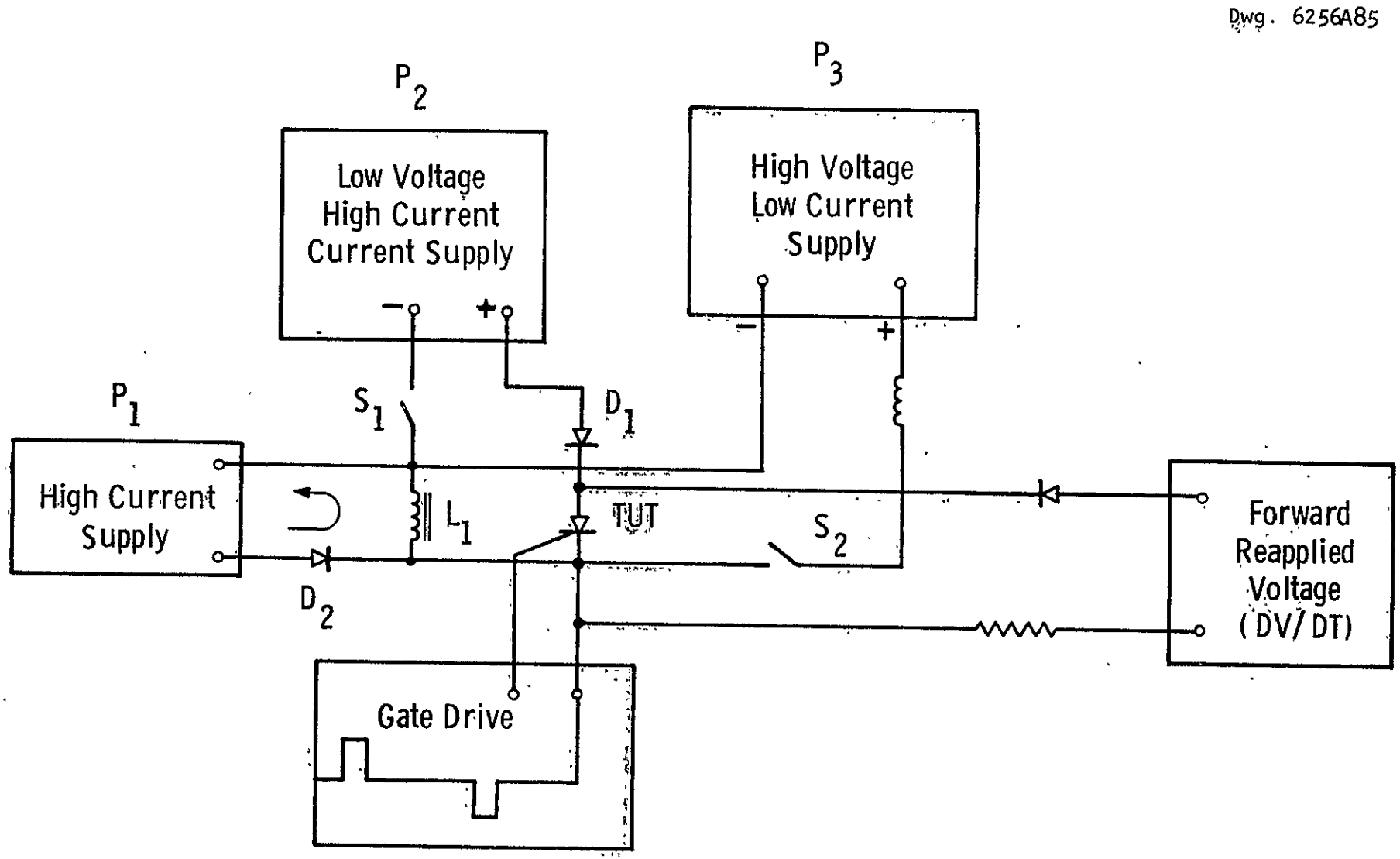


Fig. 13 —Turn-off time tester

The gate drive circuit creates a forward gate pulse to turn the TUT on and at an adjustable time later a reverse gate current can be applied to the gate. This reverse current is the gate assist current. The time of initiation and the pulse height and width of this reverse gate current are adjustable.

The recovery times of diodes and/or thyristors in the test circuit must match the recovery time of the thyristor under test. If a component in the test circuit has reverse recovery too early, that component will interrupt the sweep out of the excess charge from the device under test. On the other hand, if it takes the component of the test circuit too long to recover, the test circuit cannot reapply a forward voltage on the device under test as soon as it is capable of supporting a reapplied forward voltage. In the first case, the device under test is not permitted to turn off as fast as it might if more excess charge were swept out. In the second case, the circuit will not be able to measure the true turn-off time.

During the course of the program a continual effort was made to ensure that the turn-off time was being measured as realistically as practical. This involves the following considerations:

1. The impedance of the gate circuit can influence the actual gate current during the switching transient period.
2. The limiting resistance in the part of the test circuit that generates the dV/dt ramp can limit the forward recovery current and thereby influence the measured turn-off time.
3. Inductance in the leads of an anti-parallel diode can force a forward current into the thyristor under test during the turn-off time interval. Such an unwanted forward pulse is diverted into the device under test when reverse recovery occurs in the diode that isolates the lower impedance current

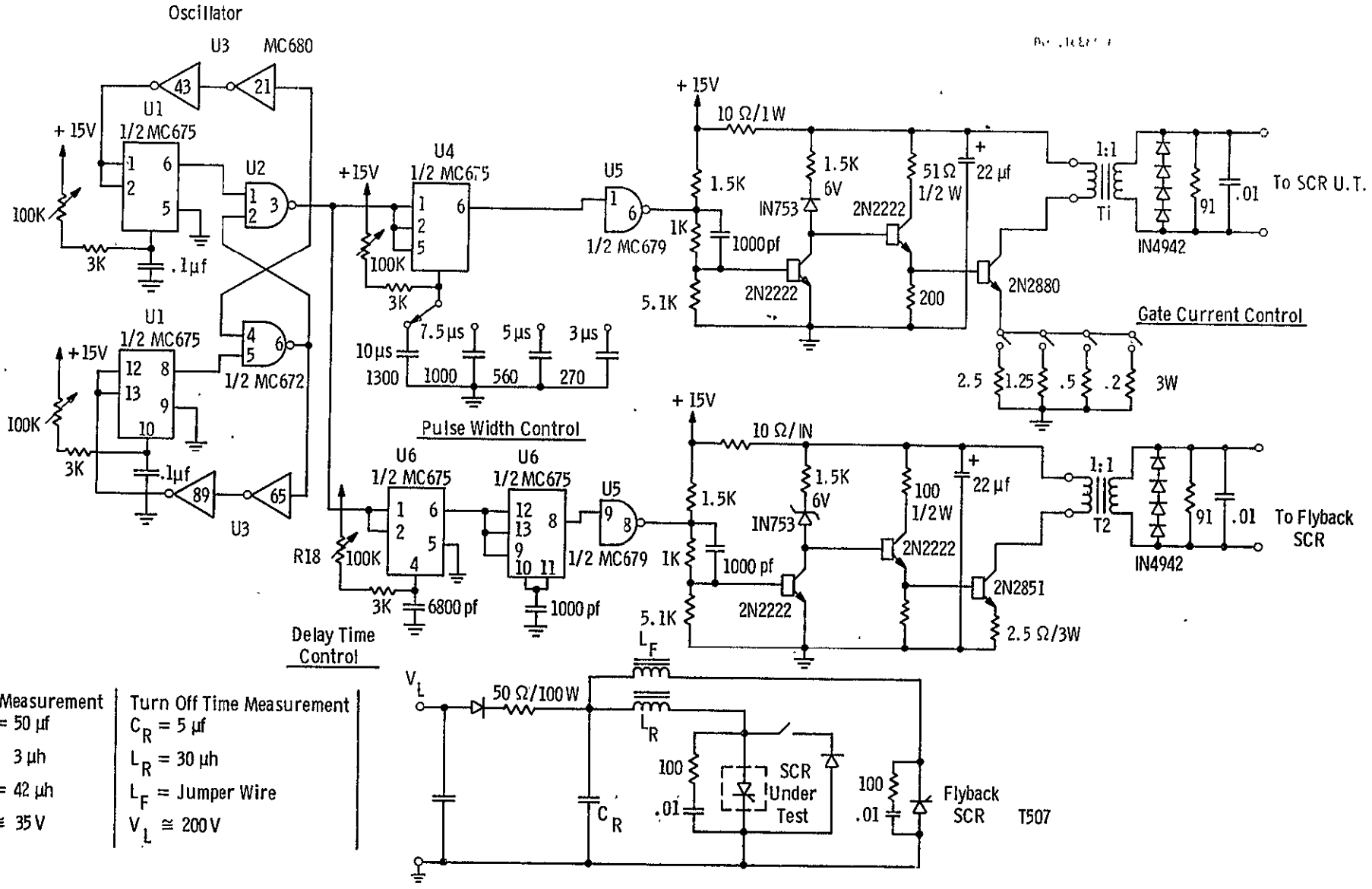
generating circuitry from the high impedance voltage generating circuitry.

4. The width and shape of the anode current pulse can determine whether the device is carrying the current uniformly over its area.

5. The shape of the reverse voltage waveform can influence the amount of charge that is swept out of the device in the reverse recovery phase. The rate of application of this voltage is believed to be more important than the ultimate voltage reached.

4.5 Simulated Application Circuit

In August of 1974, the team at TRW that developed a circuit in which these thyristors were used provided Westinghouse with a breadboard set-up. This set-up, shown in Fig. 14, permits the thyristors to be evaluated in a circuit that simulates the ion-engine power supply application. Both t_q and V_{TM} are measurable on this circuit.



Vtm Measurement	Turn Off Time Measurement
C_R = 50 µf	C_R = 5 µf
L_R = 3 µh	L_R = 30 µh
L_F = 42 µh	L_F = Jumper Wire
V_L ≅ 35 V	V_L ≅ 200 V

Fig. 14 — Simulated application circuit

5. DEVICE FABRICATION AND TESTING

5.1 Introduction

This part of the report will present the significant approaches problems, and results of the device fabrication and testing effort.

5.2 Study of New Design Features

When the program started in July 1973, there were several areas in which it was unclear how the device should be designed. These were the slice diameter, the cathode edge length, whether the emitter could successfully be shunted to achieve good GATT performance, and whether gate amplification and good GATT performance could be combined in a device. The first two runs were made with 23 mm diameter slices with an existing amplifying gate snowflake mask design shown in Fig. 15. The third run was made with an existing 33 mm diameter snowflake design.

The data taken on these early devices yielded the important findings that:

1. The snowflake design with its shunted cathode can perform well in the GATT mode.
2. The high resistance in the p-base under the auxiliary cathode of the gate amplification structure must be bypassed by the gate assist current to avoid degradation, and perhaps failure, of the device.
3. The gate assist pulse must be present during the reapplication of the forward anode voltage if it to be effective for decreasing the turn-off time.

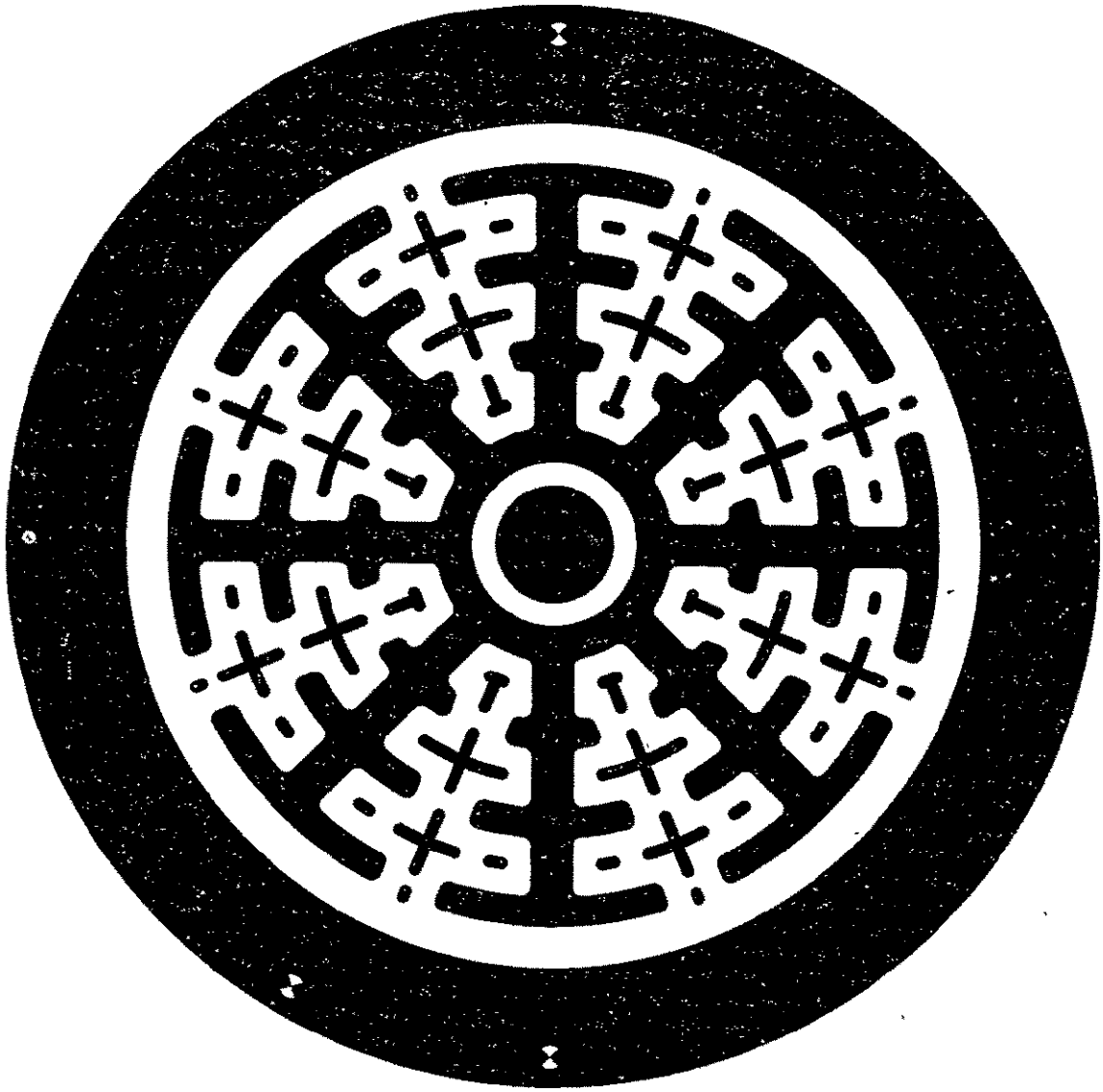


Fig. 15 PHOTOGRAPH OF THE CATHODE DIFFUSION MASK-SNOWFLAKE DESIGN

5.3 Improved Understanding of the Effect of Gate Assist Current

Early in the experimental studies of the program it became clear that the existing understanding of the physics of gate assisted turn-off was in error. In contrast to the then-existing belief that the gate assist bias sweeps the excess carriers out before anode voltage is reapplied, our finding was that the fundamental effect of the gate assist bias is to oppose the development of a forward bias on the cathode. This forward bias is caused by the dV/dt induced displacement current; and if unopposed, this bias will cause the cathode to inject a sufficient number of electrons into the p-base to refire the device. The effects of the gate assist current is described in detail in Appendices B and C.

5.4 Switching Loss Measurements

There was an experimental phase early in the program in which extensive efforts were made to measure the turn-on transient energy losses per pulse on the circuit shown in Fig. 1. Current and voltage transient waveforms were photographed and the product of the anode voltage and current was calculated and numerically integrated. These calculated energy losses per pulse were in the range of 2 to 5 mJ. While this was a good acceptable level of loss, there was significant skepticism about whether the voltage and current waveforms might be in error due to an overloading of amplifiers, an influence of a clipper circuit or to capacitive or inductive effects in the environment of the high dI/dt and dV/dt circuitry. To measure the energy dissipation in a more straightforward manner with fewer uncertainties, a calorimeter was set up as described on pages 27 to 33 and loss measurements were taken as described on pages 52 to 55. The results from the two different approaches were in good agreement.

The behavior of the forward recovery current and its associated losses were studied, and the results were published [14] as given in Appendix D.

5.5 Determination of t_q - V_{TM} Tradeoff Curve

Another experimental effort was undertaken to determine a forward drop, turn-off time trade off curve by stepwise varying the amount of lifetime reduction by means of high energy electron irradiation. The advantage of using electrons to control the lifetime permits one to vary the lifetime in individual devices and thereby to precisely determine an optimum lifetime level.

In May of 1974, a review meeting was held at NASA Lewis Research Center with representatives of TRW who were developing an efficient circuit that could use the GATT thyristors, present. Eight sample thyristors from a Westinghouse internal program, packaged with the bypass mounted inside of the package, and with the characteristics given in Table 2 were loaned to NASA.

At this meeting, the graph of Fig. 16 was shown which illustrates the V_{TM} - t_q tradeoff for a sample of devices from five process runs. The data in this figure gave NASA and TRW a significantly improved understanding of the Westinghouse ability to trade t_q for V_{TM}. It became evident to everyone that, if one were to relax the specification of a 3 μsec t_q, one could very substantially decrease the forward drop, V_{TM}, and therefore the conduction losses.

5.6 Devices Made on a Separate Contract

Based on the t_q - V_{TM} tradeoff curve, a decision was made for Westinghouse to make additional devices on a separate contract (NAS3-19097). They were similar to those represented by Table 2 except that the t_q - V_{TM} tradeoff was shifted to a higher t_q and lower V_{TM} by giving them less electron irradiation. The characteristics of these devices are summarized in Table 3.

TABLE 2. CHARACTERISTICS OF THE EIGHT DEVICES LOANED TO NASA IN MAY OF 1974

	t_{off}			V_{TM}	V_{DRM}	V_{RRM}	I_{GT}	V_{GT}	I_H	I_{LX}	dV/dt	Energy Pulse	Units
Devices													
	µsec	µsec	µsec	V	V	V	mA	V	mA	A	V/µsec	mJ	
21-2	5.5	3.0	5.5	2.9	1180	1040	130	1.25	65	0.5	> 500	12	
21-19	6.0	3.5	6.0	2.3	1080	940	100	1.10	55	0.4	> 500		
21-26	6.5	3.0	6.5	2.1	1100	1080	90	1.10	50	0.4	> 500	11	
21-49	6.5	5.0	6.5	2.1	920	920	120	1.10	55	0.5	> 500		
21-55	5.5	4.5	5.5	2.2	740	680	100	1.00	55	0.4	> 500		
21-4	8.0	4.0	8.0	2.4	720	680	85	1.10	40	0.4	> 500		
21-42	5.0	5.0	5.0	2.5	890	840	100	1.10	70	0.8	> 500		
21-30	5.0	4.5	5.0	2.2	830	760	130	0.95	65	0.4	> 500		
Conditions													
temp	100	100	100	100	100	100	25	25	25	25	100		°C
I_{TM}	200	200	200	200									A
-diR/dt	25	25	25										A/µsec
dV/dt	400	400	400										V/µsec
V_{Rev}	yes	yes	yes										V
Gate I	2	2	0							2			A
Gate PW	3	10								3			usec
I_A					0.01	0.01							A
V_A							30	30	30	30			V

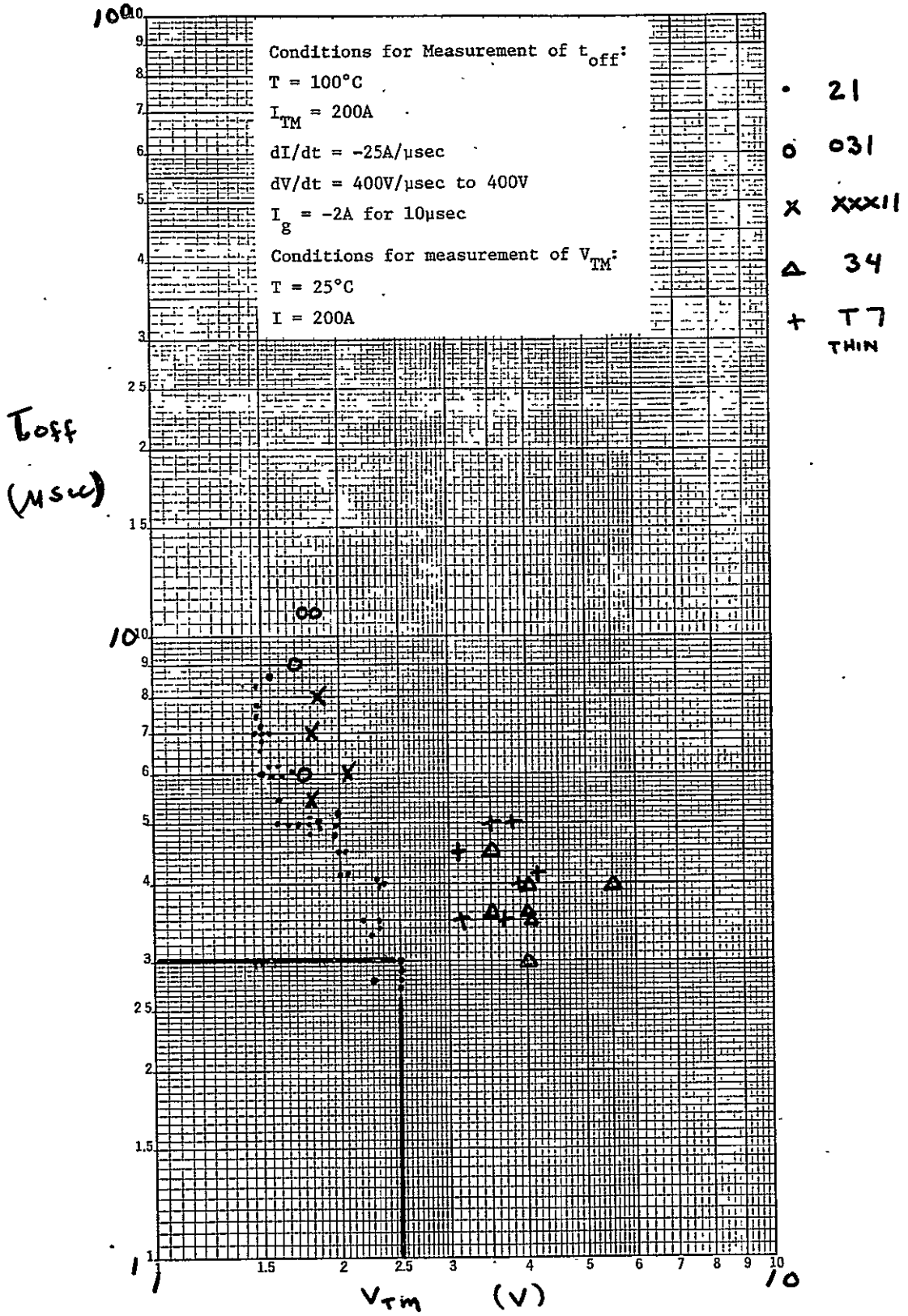


Fig. 16 t_q - V_{TM} tradeoff curve

TABLE 3

Characteristics of Thyristors Delivered on NASA Contract No. NAS3-19097

	T_{off}			V_{TM}		V_{DRM}	V_{RRM}	I_{GT}	V_{GT}	I_{LX}	I_H
Conditions											
	µsec	µsec	µsec	V	V	V	V	mA	V	mA	mA
Temp., °C	100	100	100	100	100	25-100	25-100	25	25	25	25
I_{TM}, A	80	200	200	80	200						
$-dI_R/dt$, A/µsec	10	50	25								
dV/dt, V/µsec	50	400	400								
Gate: I, A	2	2	2								
PW, µsec	10	10	10					10	10	10	
Device Nos.											
54	4.2	7.9		1.50	1.85	1000	960	120	1.4	870	168
55	4.1	8.0		1.98	1.96	1100	1080	150	1.5	1350	200
56	4.0	9		1.96	2.07	1280	1120	120	1.2	900	150
57	5.0	8.4		1.75	2.05	1120	1030	300	2.0	1900	190
63	5.0	9		2.00	1.98	1260	1120	180	1.6	1500	320
64	4.0	7		1.74	2.01	960	960	120	1.2	700	180
65	4.0	7.2		1.80	1.97	1000	1000	125	1.4	1050	170
66	4.0	8.4		1.41	1.75	940	930	160	1.5	1200	300
70	6.4	11	11	1.86	2.05	990	960	150	1.3	790	260
71	3.5	5.8	5.0	1.57	1.89	1200	1120	160	1.5	1300	280
74	4.1	8.2		1.72	2.16	1100	1000	170	1.7	2200	340
77	4.0	16	9	1.43	1.77	900	920	120	1.2	1300	320
78	3.8	13	7	1.49	1.90	1200	1000	120	1.2	750	200
82	< 3.0	5.8		1.79	2.14	1010	1020	200	1.6	1500	320
86	4.0	9		1.40	1.75	1200	1040	120	1.2	1000	190

TABLE 3 (Continued)

	T_{off}			V_{TM}		V_{DRM}	V_{RRM}	I_{GT}	V_{GT}	I_{LX}	I_H
Device Nos.											
108	4.1	1.5		1.45	1.84	900	800	150	1.3	1150	220
110	4.0	12		1.35	1.63	1080	1090	120	1.2	850	180
120	4.2	12	8.2	1.43	1.70	1260	1120	130	1.6	1000	170
124	3.2	8		1.49	1.95	880	890	130	1.2	1150	320
128	3.2	7.2		1.45	1.67	1000	960	160	1.2	1500	230
132	3.0	7.6		1.69	2.13	1000	1000	160	1.4	1600	280
135	4.4	9.8		1.70	1.89	1080	1080	150	1.6	1600	250
137	4.0	6.4		1.45	1.80	1120	920	130	1.4	1300	210
138	4.2	10	9	1.43	1.75	1020	1040	120	1.4	1160	210
139	4.0	7		1.54	1.96	1220	880	160	1.6	1200	210
140	4.5	7.5		1.52	1.77	980	990	140	1.2	900	200
141	5.0	8		1.88	2.18	1200	1200	210	1.6	2000	400
122	12.	V. high		1.17	1.47	920	960	100	1.0	380	160
143	4.2	7.2		1.60	2.11	1160	1080	180	1.6	2200	210
144	3.6	7.8		1.68	1.96	880	880	140	1.6	1350	250
145	4.2	10.2	9.8	1.47	1.77	960	960	150	1.7	1250	240
131	12.	32	19	1.22	1.44	830	840	80	1.0	450	120
148	4.5	14	8	1.34	1.62	760	720	150	1.2	1200	210
149	5.0	17	13	1.65	1.89	960	880	150	1.4	1200	230
152	4.0	6.4	6	1.51	1.86	1120	1080	120	1.3	720	150
153	4.2	9		1.37	1.69	1020	1020	100	1.2	700	150
154	7.0	11.2	10.4	1.50	1.79	1000	920	120	1.4	1180	160

5.7 Fineline Thyristors and the Results Obtained from Them

Thyristors were fabricated with the mask design shown in Fig. 7. A photograph of a finished device is shown in Fig. 17. These devices were found to have very short turn-on and turn-off times without electron irradiation. A surprising characteristic of these devices was that they did not respond well to gate assist current. This unexpected result was subsequently explained as follows. It is not sufficient to merely provide gate assist current to counteract the dV/dt induced displacement current. The gate assist current must create an IR drop in the p-base that substantially counteracts the roughly 0.7 volts in this p-base that is present when a dV/dt induced displacement current fires the thyristor. Thus, if one has chosen to use a gate assist current of .2 amperes one must have a lateral base resistance under the cathode of roughly 0.35 ohms. In hindsight, a change in design to a long-periphery narrow-line cathode must be accompanied by a change in the diffusion layer design to maintain this resistance if effectiveness of gate assist current is to be maintained.

5.8 Change in Directions

At this point in the program it was decided that the effort should be focused on the 23 mm diameter snowflake design which was much closer to meeting the specifications than the new 33 mm diameter design. An additional reason for choosing this route was that the development of a new package of the type desired by TRW and NASA would be significantly less time consuming and less costly for the 23 mm diameter unit.

At the end of 1974, the contract was amended to include three additional areas of work:

1. An experimental study was to be made of the effects of the diffusion profile on the V_{TM} - t_q tradeoff so that a better tradeoff could be obtained at low lifetime levels.

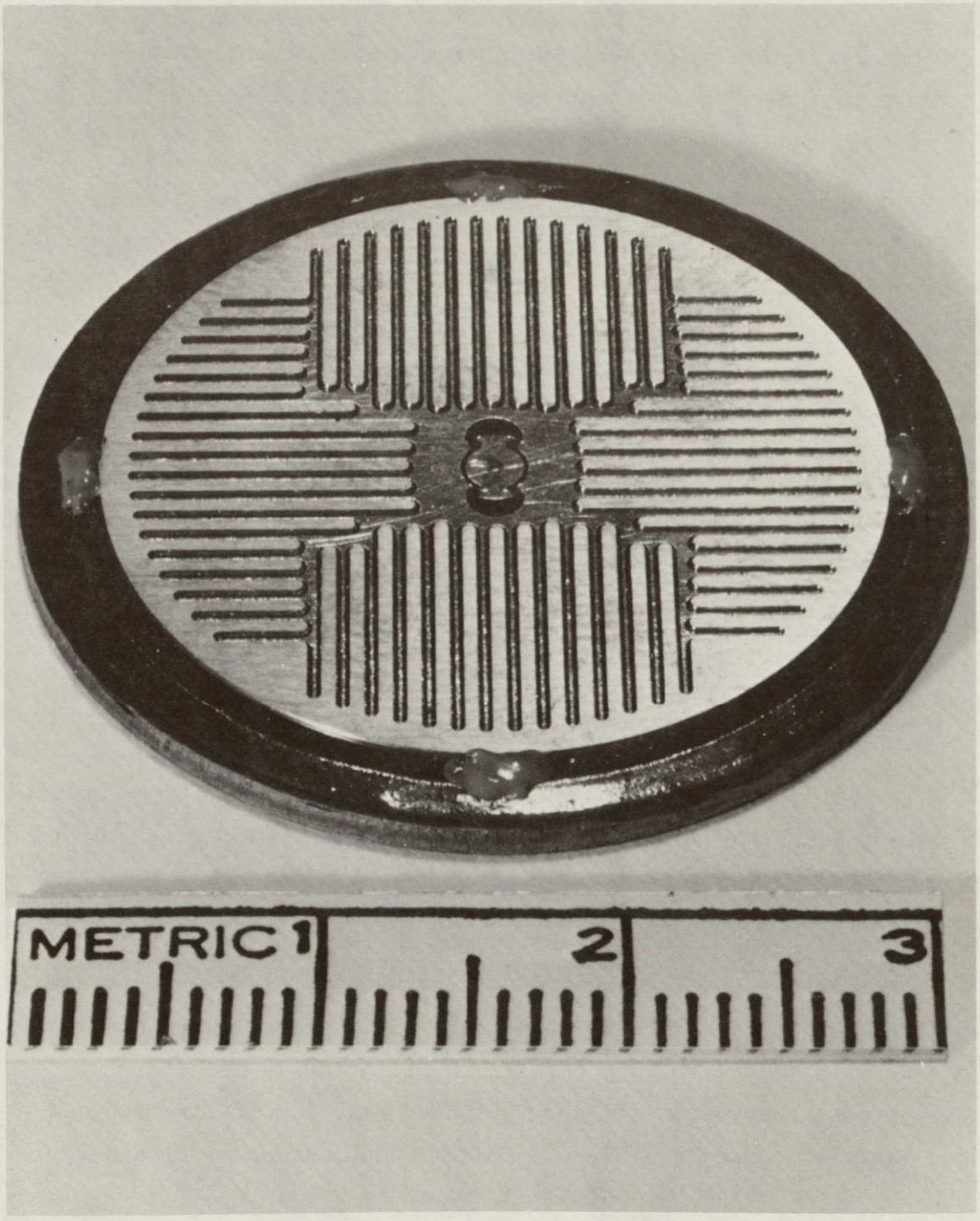


Fig. 17 Photograph of a fineline thyristor.

2. The effect of the cathode peripheral length on the energy loss per pulse was to be better defined by means of loss measurements with a calorimeter.

3. Westinghouse was to develop and fabricate an improved light-weight package.

5.9 Effect of Diffusion Profile on t_q - V_{TM} Tradeoff Curve

The study of the effect of the diffusion profile on the t_q - V_{TM} tradeoff showed clearly that the t_q - V_{TM} tradeoff can be improved by changes in the diffusion profile. Further, it showed that a change that gives an improvement at high lifetime levels degrades the tradeoff at low lifetime levels and vice versa. This type of a study was practical because of the Westinghouse use of electron irradiation to control the lifetime. It would not have been practical to do this with gold. The details of this study and a physical explanation for the findings are given in Appendix A.

The data in Appendix A were taken without gate assist current. Similar data taken with two amperes of gate assist current are given in Figs. 18 and 19. The letters A, B and C designate the same diffusion profiles in Figs. 18 and 19 as in Appendix A. All of these data show that, at low lifetime levels, the tradeoff between t_q and V_{TM} is improved if the diffusion layer profile is changed to yield higher current gains. The opposite is observed in each case if the lifetime is high. This technique permits one to clearly show which combination of lifetime and diffusion profile to use to achieve a desired combination of t_q and V_{TM}.

5.10 Devices Delivered in May of 1975

In May of 1975, a group of eight thyristors were delivered to NASA-Lewis. These devices were packaged in non-magnetic flat packs. A summary of the data taken on these devices is given in Table 4.

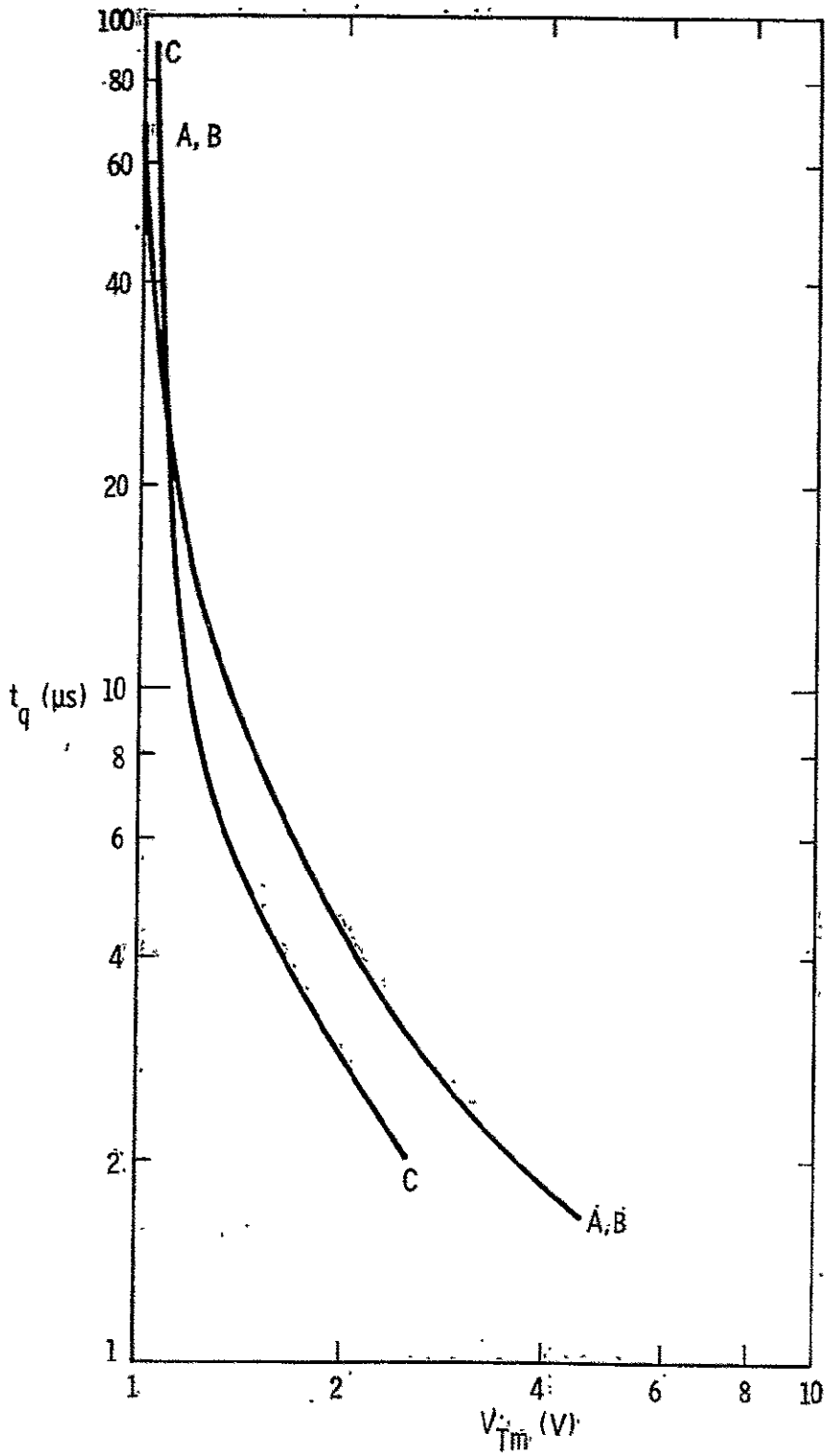


Fig. 19 – t_q (2A gate assist) – V_{Tm} (80A)
V_{Tm} Conditions - 80 A, 25°C
t_q Conditions - 200 A, 25 A/µsec, 400 V/µsec, 100°C

TABLE 4

SUMMARY OF DATA TAKEN ON DEVICES DELIVERED IN MAY 1975

	V_{TM}		t_q				V_{DRM}	V_{RRM}	I_{GT}	V_{GT}	I_L	I_H	To NASA
Temp.	25°C	25°C	100°C	100°C	100°C	100°C	25& 100°C	25& 100°C	25°C	25°C	25°C	25°C	
I_{TM}	80A	200A	80A	80A	200A	200A			12.5A	12.5A			
dI/dt			10A/μs	10A/μs	25A/μs	25A/μs							
dV/dt			50V/μs	50A/μs	500V/μs	400V/μs							
V_A									50V	50V	50V		
Gate Current													
(turn-off)			0A	2A	0A	2A							
(turn-on)											0.5A		
Devices	V	V	μs	μs	μs	μs	V	V	mA	V	mA	mA	
34-17	1.17	1.32	17	10	14	8	1000	1050	75	1.00	340	80	X
18	1.49	1.64					1000	1000	118	1.00	650	180	X
19	1.27	1.39	14	9	10	7	1150	1100	108	1.05	480	140	X
20	1.32	1.42	14	9	11	7.2	1000	1000	110	1.05	380	90	
22	1.32	1.49	11	11	10.5	10.0	1100	800	80	1.05	540	160	
23	1.32	1.42	10	8.5	8	7	1150	1050	108	1.00	440	160	X
24	1.36	1.47	20	10	15	8	900	900	70	0.90	310	90	
25	1.27	1.39	13	9	10	7	1050	1050	105	1.10	500	160	X
26	1.50	1.61	10.5	7.5	10	6.5	1100	1100	140	1.20	720	240	
27	1.36	1.52	13	7	10	6	900	900	108	1.10	540	160	X
28	1.31	1.46	14	8	11	6.5	1100	1100	108	1.05	540	160	X
29	1.40	1.52	11.5	8	8	6	1100	1100	125	1.10	640	200	X
30	1.51	1.67	8	8	8	6	1100	950	110	1.05	665	170	
31	1.64	1.80	15	9	10	6	900	900	90	1.05	380	130	

5.11 Calorimetric Measurements

In June and July of 1975, the calorimeter apparatus described in Section 4 was used to measure turn-on and conduction losses. The resulting data are given in Table 5.

The thyristor under test is described by giving the cathode geometry, the main cathode edge length in cm, the device diameter in mm and a numerical value that is in linear proportion to the amount of electron irradiation used to decrease the carrier lifetime. (E.g., snowflake, 23, 23, 4 means the pattern is the snowflake design, which has a main cathode perimeter of 23 cm, is in a silicon slice 23 mm in diameter and had four units of irradiation to control the carrier lifetime.) In some cases, the same device type and test conditions are represented by data from more than one sample. In this case, the energy per pulse value in Table 4 is followed by an asterisk and a sample distinguishing number. The gate energy is not completely negligible and in some cases is as high as 0.5 mJ/pulse.

Significant conclusions that can be drawn from these data include:

1. The desired 12 mJ per pulse is attainable for the conditions specified by the contract.
2. The part of the loss that is sensitive to gate drive current without amplification is nearly negligible when this current is as large as that to be expected with gate amplification. Thus with gate amplification the turn-on switching loss is a small part of the total loss.
3. The cathode edge length has little noticeable effect on the loss as long as a threshold gate drive current has been exceeded.
4. The radiation level has a strong influence on the loss (a well recognized fact that deserves to be re-emphasized).

TABLE 5

Calorimetric Data

Device	Gate Drive	Voltage Switching From	Peak Current	Energy Per Pulse
Std 627, 1.6, 23, 4	1A, ampl.	400V	200A	19.3 mJ
	2A, ampl.	400	200	19.3
	1A, not ampl.	400	200	19.5
	4A, not ampl.	400	200	19.0
Std 627, 1.6, 23, 0	2A, ampl.	400	200	13.0
	2A, ampl.	200	100	4.4
	2A, ampl.	100	50	1.8
	2A, ampl.	200	50	2.6
	2A, ampl.	400	50	4.4
Dual ring, 8.2, 23, 4	1A, ampl.	400	200	13.8*20
	2A, ampl.	400	200	13.0*20
	1A, not ampl.	400	200	17.1*20
	4A, not ampl.	400	200	13.6*20
	2A, ampl.	200	100	4.9*20
	1A, ampl.	400	200	10.8*17
	2A, ampl.	400	200	10.7*17
	1A, not ampl.	400	200	13.1*17
	2A, not ampl.	400	200	12.5*17
	4A, not ampl.	400	200	12.2*17
Snowflake, 23, 23, 4	1A, ampl.	400	200	13.1
	2A, ampl.	400	200	13.0
	1A, not ampl.	400	200	17.7
	4A, not ampl.	400	200	13.6
Snowflake, 23, 23, 5.5	4A, not ampl.	400	200	11.6*80
(Like the devices	3A, not ampl.	400	200	16.2*146
delivered on NAS3-	6A, not ampl.	400	200	12.3*146
19097)	7.8A, not ampl.	400	200	10.8*146
	2A, ampl.	400	200	9.2*146
	2A, ampl.	400	200	11.3*62
	2A, ampl.	400	50	4.0*80
	2A, ampl.	200	50	3.0*80
Snowflake, 23, 23, 3	2A, ampl.	400	200	9.1*22
(Like the devices	2A, ampl.	400	200	9.3*18
delivered on NAS3-	2A, ampl.	200	100	3.6*22
16801)	2A, ampl.	100	50	2.1*22
Snowflake, 23, 23, 24	1A, not ampl.	400	200	21.3*21
(Devices on Fig. 1	2A, not ampl.	400	200	21.3*21
of Monthly Status	4A, not ampl.	400	200	20.7*21
Report No. 22)	6A, not ampl.	400	200	19.6*21
	3A, not ampl.	400	200	22.2*24
	6A, not ampl.	400	200	19.0*24
	2A, ampl.	400	200	15.2*28
	2A, ampl.	400	200	16.5*9

TABLE 5 (cont'd)

Calorimetric Data

Device	Gate Drive	Voltage Switching From	Peak Current	Energy Per Pulse
(Devices on Fig. 3 of Monthly Status Report No. 22)	2A, ampl.	400V	200A	15.3*15
	2A, ampl.	400	200	11.9*16
Fineline, 97, 33, 0	1A, ampl.	400	200	9.8*A
	4A, ampl.	400	200	10.3*A
	1A, ampl.	400	200	9.1*B
	2A, ampl.	400	200	9.1*B
	2A, ampl.	400	200	10.4*C
	2A, ampl.	200	100	4.1*C
	2A, ampl.	400	50	4.0*C
	2A, ampl.	200	50	1.9*C
Fineline, 97, 33, 5	2A, ampl.	400	200	16.7
	2A, ampl.	200	100	7.7

Calorimeter data were also used to determine that for a 400V, 200A, half sine wave 20 μsec wide, changing the flat pack package from a magnetic to a non-magnetic package decreased the losses from 12.1 to 11.3 mJ/pulse. The sample was like one of those delivered on Contract No. NAS3 -19097. D. Balenovich and W. Karstaedt of the Westinghouse Semiconductor Division have independently found a similar improvement in studies with nonmagnetic packages. On this program this improvement is not worth the added cost that it would require to prepare a nonmagnetic lightweight package.

5.12 Delivery of Devices in the New Package

During 1975 an improved package was developed as described in Section 6.

In December of 1975, it was apparent that devices with the integrated bypass diodes would not be ready at the desired time. In order to provide NASA with devices that they needed, a decision was made to, prepare additional devices on a separate contract like those delivered in May of 1975 but in the new package. The bypass diodes were mounted in the package as described in Fig. 2.

Table 6 gives a summary of the data taken on these devices. Figure 20 is a photograph of a packaged device. Three similar devices were shipped in July of 1976 as summarized in Table 7.

TABLE 6

SUMMARY OF DATA TAKEN ON DEVICES DELIVERED IN JANUARY 1976

	V_{DRM}	V_{RPM}	VTM		t_q		I_{GT}	V_{GT}	I_L	I_H	Leak Rate
Temp, °C	25-125	25-125	100	100	100	100	25	25	25	25	
I_{TM}, A			80	200	200	200					
V_A, V							50	50	50		
-dI/dt, A/μs					25	25					
dV/dt, V/μs					400	400					
Gate Assist I,A					0	2					
I_G, A							0.5	0.5	0.5		
Units	V	V	V	V	μs	μs	mA	V	mA	mA	
34-2	1140	1080	1.15	1.35	11	8	130	1.1	380	144	$<10^{-6}$
34-3	840	880	1.15	1.35	10	6	110	1.0	320	140	10^{-7}
34-13	820	880	1.15	1.35	12	8	100	1.0	300	140	$<10^{-6}$
34-15	1140	1140	1.45	1.51	11	7.5	120	1.1	450	160	$<10^{-6}$
34-B5	960	880	1.15	1,35	12	6.5	110	1.05	400	140	$<10^{-6}$
34-B6	1190	1000	1.3	1.5	13	7	115	1.1	440	172	10^{-7}
34-B7	1000	980	1.45	1.75	10	5	115	1.2	540	184	10^{-8}
34-B12	1020	790	1.25	1.55	15	8	110	1.0	510	148	10^{-7}
34-B13	1200	1190	1.3	1.55	13	7	100	1.0	370	126	10^{-8}
34-B15	1180	1100	1.2	1.4	15	7.5	125	1.15	410	170	$<10^{-6}$

Fig. 20 Photograph of a packaged device

TABLE 7

SUMMARY OF DATA TAKEN ON DEVICES DELIVERED IN JULY 1977

	V_{TM}		t_q				V_{DRM}		V_{RRM}		I_{GT}	V_{GT}	I_L	I_N
Temp.	100°C	100°C	100°C	100°C	100°C	100°C	25°C	100°C	25°C	100°C	25°C	25°C	25°C	25°C
I_{TM}	80A	200A	80A	80A	200A	200A					12.5A	12.5A		
dI/dt			10A/µs	10A/µs	25A/µs	25A/µs								
dV/dt			50V/µs	50V/µs	400V/µs	400V/µs								
VA											50V	50V	50V	
I_G (On)														
I_G (Off)			0A	2A	0A	2A							0.5A	
Devices	V	V	µs	µs	µs	µs	V	V	V	V	mA	V	mA	mA
34-1	1.15	1.35	11.0	8.0	14.0	9.0	1240	1150	1200	1150	110	1.1	300	140
34-9	1.10	1.30	12.0	7.5	13.5	9.0	1100	1100	1050	1050	100	1.0	300	100
34-B10	1.25	1.54	9.0	7.5	14.0	8.0	1200	1200	1200	1150	140	1.1	600	180

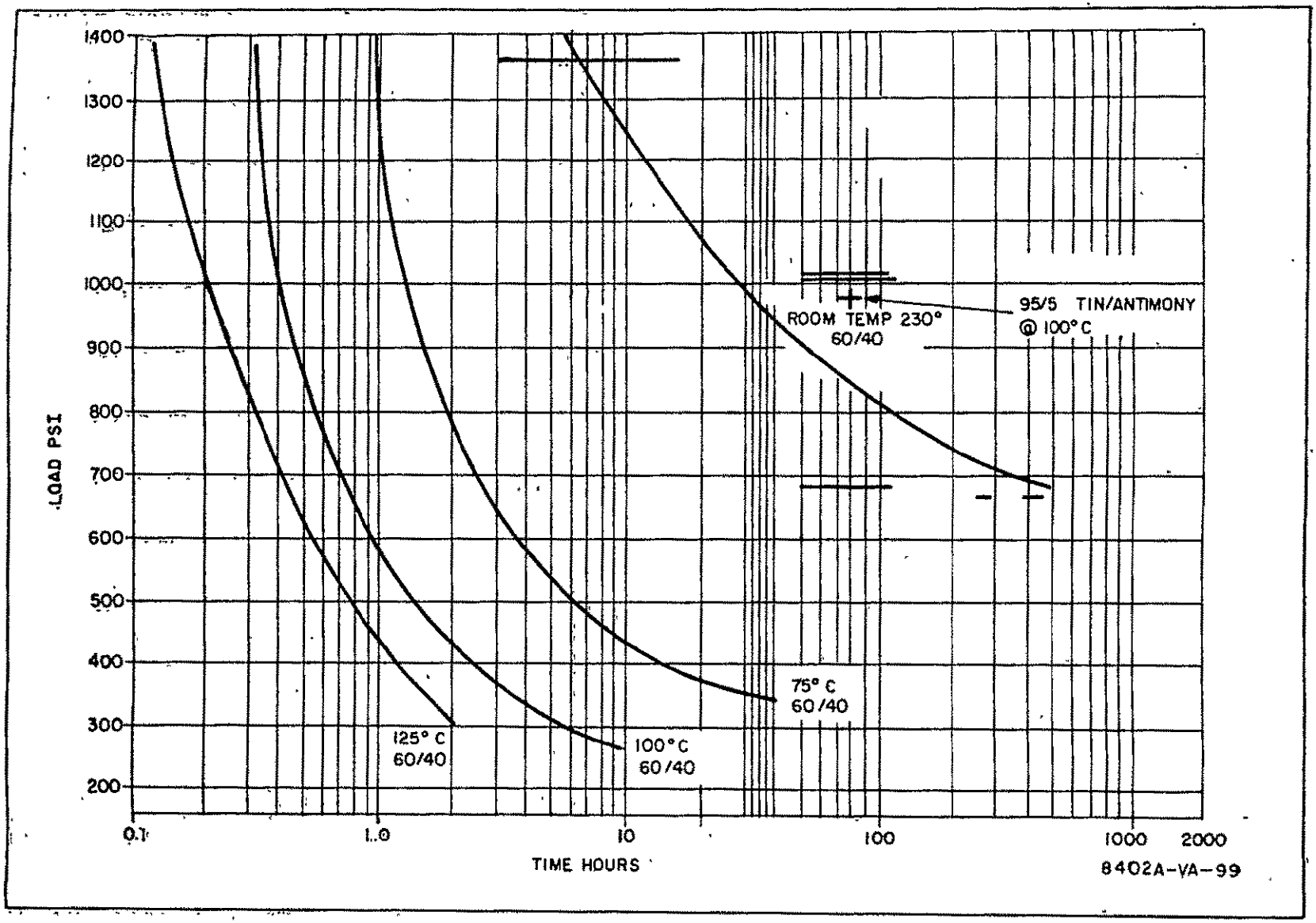


Fig. 21 Creep-Rupture Properties of Some Solders

TABLE 8

SUMMARY OF DATA TAKEN ON DEVICES WITH INTEGRATED BYPASS DIODES DELIVERED IN MARCH 1977

	V_{DRM}	V_{RRM}	V_{TM} 2μs	80A 10μs	V_{TM} 2μs	200A 10μs	t_{q1}	t_{q2}	t_{q3}	t_{q4}	t_{q5}	t_{q6}	I_{GT}/V_{GT}	I_L/I_H
Units	V	V	V	V	V	V	μs	μs	μs	μs	μs	μs	mA/V	mA/mA
44-24	1150	1200	3.5	2.0	4.2	2.6	14	9	11	7	14	8.5	$400_{0.6}$	320_{8}
45-17	750	1200	2.3	1.5	3.4	2.2	12	8	9	6	12.5	7	$130_{1.8}$	290_{2}
48-6	>600	1200	2.9	1.7	4.2	2.3		7.5	18	6	>23	7.5	$55_{1.6}$	150_{2}
48-9	1150	1300	3.0	1.9	4.2	2.5	21	8	15	5	19	6.5	$90_{1.8}$	260_{4}
48-11	300	1150	2.2	1.6	3.4	2.2	14	8	10	5	17	5	$78_{1.7}$	300_{2}
48-13	~150	~600	2.2	1.5	3.0	1.9	13	9					$85_{1.7}$	240_{4}
48-16	~400	1240	2.2	1.5	3.2	2.1	14	8.5	11	4			$95_{0.6}$	190_{2}
53-2	1000	680	3.0	2.0	4.2	2.7			18	6	>23	7	$95_{1.6}$	180_{2}
57-1	900	900	4.0	1.6	4.2	2.0	14	10	11	9	13.5	11	$660_{2.5}$	500_{6}
57-3	1000	1090	2.1	1.4	3.3	1.9	15	9	13	7	15	8.5	$460_{2.5}$	620_{7}
57-5	1020	1020	2.0	1.4	3.0	2.0	22	7	16	6	22	7	$210_{1.6}$	400_{8}
57-6	780	780	1.9	1.3	2.6	1.7	21	7.5	16	6			$290_{2.0}$	480_{6}
57-7	1000	950	2.2	1.4	3.6	1.7	14	10	11	8	14	10.5	$700_{2.6}$	760_{6}
57-9	120	750	2.0	1.3	2.8	1.8	148	7	20	6.5	>23	11	$160_{1.8}$	330_{6}
57-10	1100	880	1.9	1.3	2.9	1.8	28	6	20	6.5	>23	12	$135_{1.7}$	300_{7}
57-11	950	900	1.9	1.3	2.9	1.6	28	7	18	6	>23	7.5	$120_{1.7}$	280_{6}
57-12	1000	1000	1.9	1.3	2.6	1.5	38	8	24	7	>23	10	$40_{1.1}$	270_{6}
57-13	1150	1150	1.9	1.3	2.8	1.6	22	7	18	6	>23	8	$120_{1.7}$	280_{5}
57-14	950	920	2.0	1.3	2.6	1.7	31	8	21	7	>23	13	$170_{1.7}$	340_{8}
57-15	860	840	2.1	1.4	3.0	1.8	15	8	12	6.5	15	8	$350_{2.2}$	540_{6}
57-16	970	980	2.1	1.4	3.1	1.8	22	12.5	16	10	18	12	$145_{1.2}$	600_{4}
57-17	950	950	1.9	1.3	2.9	1.6	23	7.5	17	6	>23	7.5	$120_{1.7}$	300_{4}
57-19	980	1000	2.0	1.3	3.1	1.8	21	8	13.5	6.5	20	8.5	$220_{1.4}$	480_{4}

TABLE 8 (Cont'd.)

MEASUREMENT CONDITIONS

V_{DRM}	100°C		
V_{RRM}	100°C		
V_{TM}	25°C		TRW circuit, half sine wave, 80A peak, 20 µs wide Measured at 2 and at 10 µs after gate current reached 2A.
t_{q1}	100°C		200A, 25A/µs, 400V/µs no gate assist
t_{q2}	100°C		200A, 25A/µs, 400V/µs 2A gate assist
t_{q3}	100°C		80A, 20 µs half sine TRW circuit no gate assist
t_{q4}	100°C		80A, 20 µs half sine TRW circuit 2A gate assist
t_{q5}	Same as t_{q3} but with antiparallel diode.		
t_{q6}	Same as t_{q4} but with antiparallel diode.		
V_{GT} I_{GT}	V_A 50V	25°C	
I_L	V_A 50V	25°C	I_G 2A
I_H		25°C	

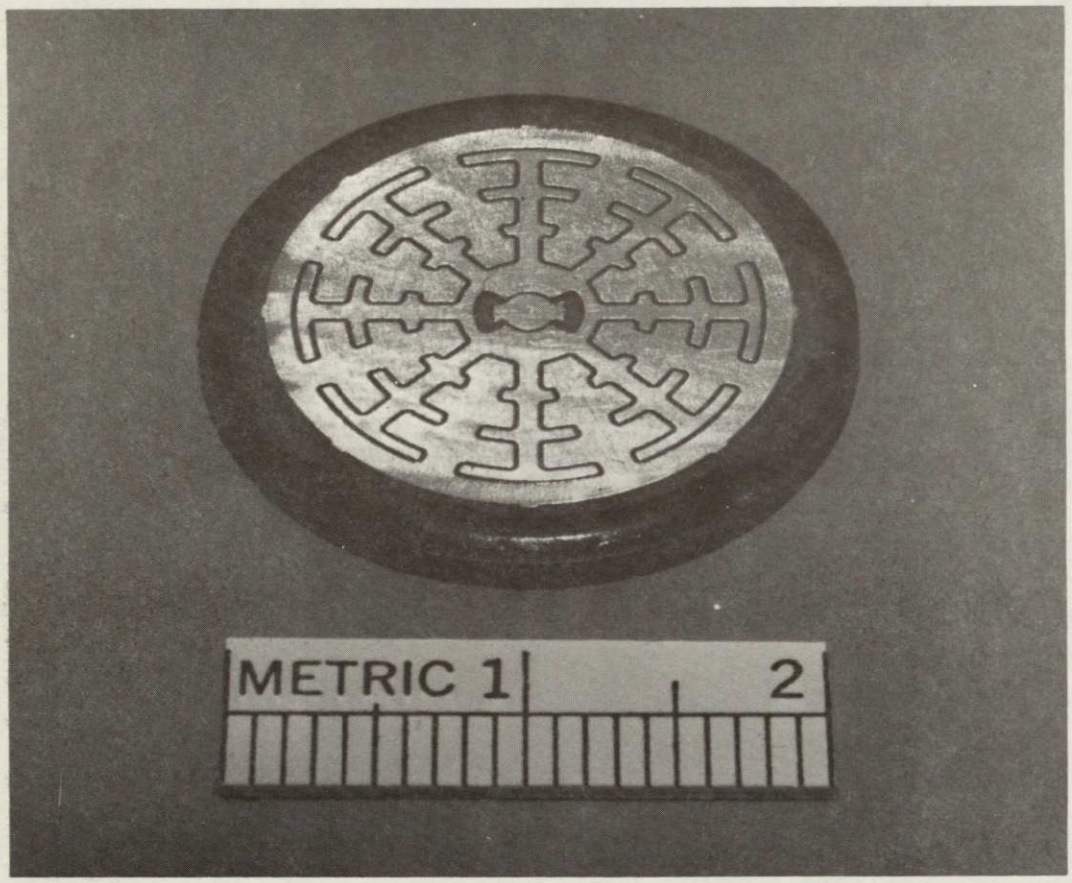


Fig. 22 Photograph of thyristor fusion with integrated bypass diode.

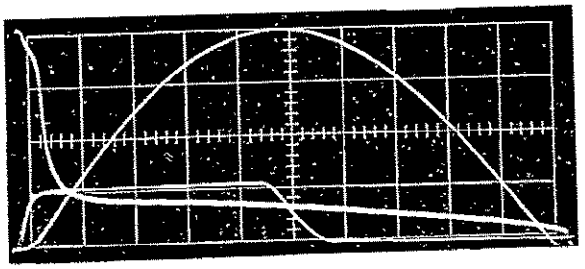
A photograph of one of these fusions is given in Fig. 22. Typical oscillograms that were taken on these devices are given in Figs. 23-29. Blocking voltage waveforms, at 100°C, are shown in Fig. 23. Figure 24 shows dynamic forward drop waveforms for an 80A, 20 μs half sine wave of current. Figure 25 shows dynamic forward drop waveforms for 200A current waveforms. Turn off time waveforms, both with an without gate assist current are given in Figs. 26-28. In Fig. 26, the current waveform was a 200A, 20 μs half sine wave. In Fig. 27, the current waveform was an 80A, 20 μs half sine wave. In Fig. 28, the same current waveform was used as in Fig. 27, with the difference being that in Fig. 28 an anti-parallel diode was used. Figure 29 shows that the devices can be operated at a di/dt level of 100A/μs.

5.16 Discussion of the Measured Performance of these Thyristors

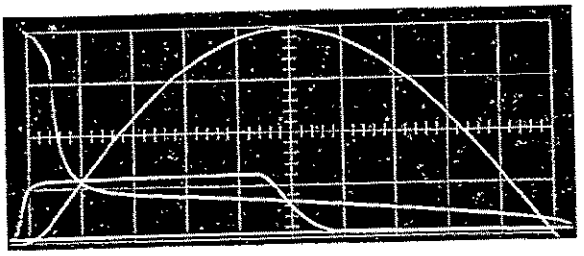
The data in Table 2 show that the target specifications of Table 1 are feasible (except that no t_{on} data was shown because at that stage of the program, there was doubt about our ability to make accurate t_{on} measurements).

Given the V_{TM} - t_q tradeoff curve of Fig.16, devices as represented by Table 3 were made to have a higher carrier lifetime. The average V_{TM} at 200A (which in Tables 2 and 3 were measured in the middle of a 60 Hz half sine wave) was thus decreased by 20%. This decreases the conduction losses by 20% and the circuit designer tolerated the longer t_q.

Using an improved slice thickness and diffusion schedule design, devices were made and delivered as represented in Table 4. Without sacrificing blocking voltage and with even a faster t_q than that in Table 3, the V_{TM} was again decreased. (2.34 V in Table 1, 1.87V in Table 2 and 1.51 V in Table 3). At this stage of the program, we added another test of t_q (80A, 10A/μs, 50V/μsec) with conditions similar to those of the circuit application.



57-6



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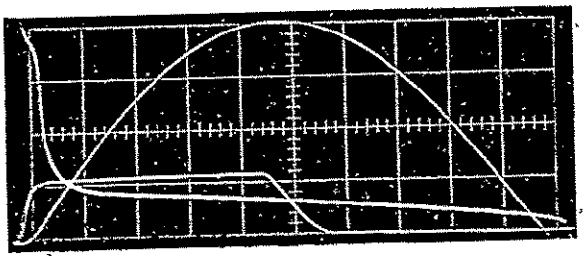


57-11

Figure 24

Typical Dynamic Forward Drop
25°C Half Sine Wave 80A, 20 µs
I_A 20A/div, V_A 2V/div, I_G 2A/div
time 2 µs/div

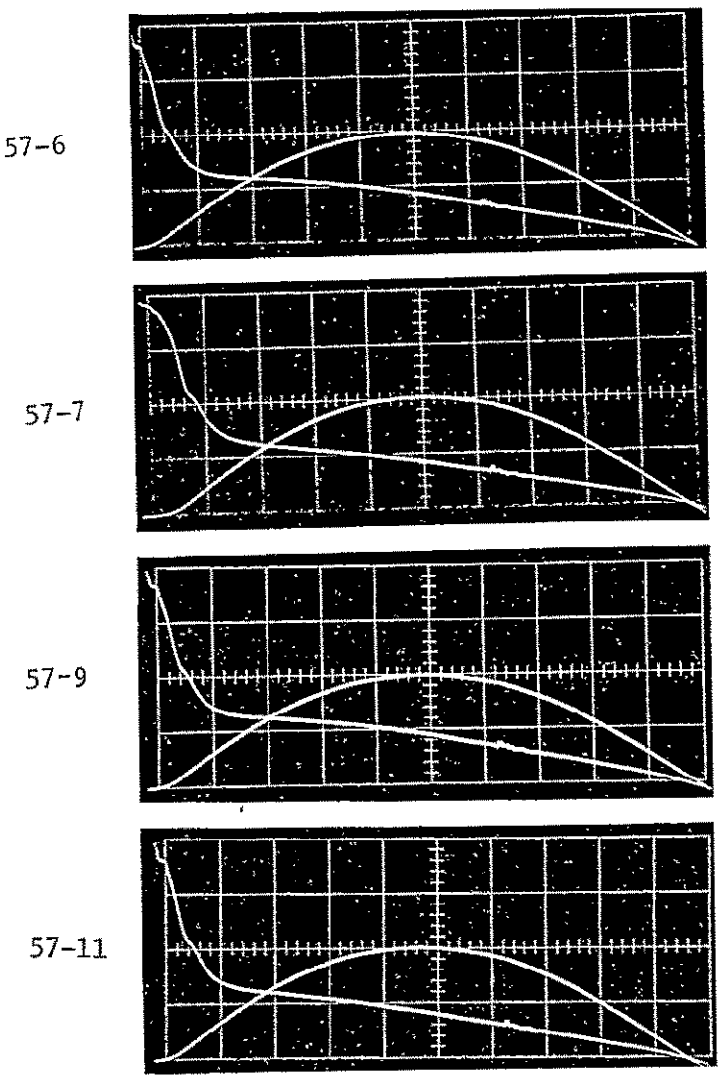
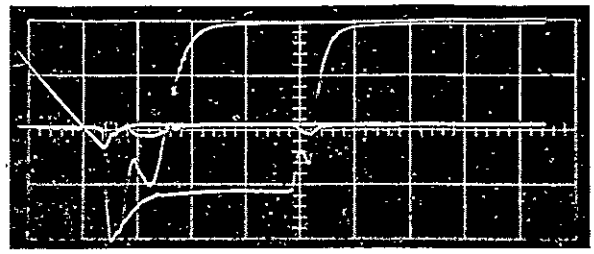


Figure 25

Typical Dynamic Forward Drop
25°C Half Sine Wave 200A, 20 μs
I_A 100A/div, V_A 2V/div
time 2 μs/div



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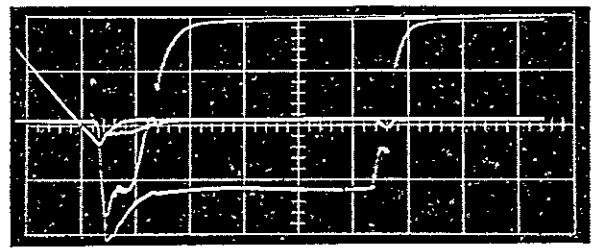

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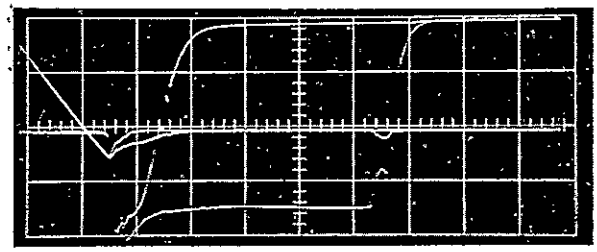
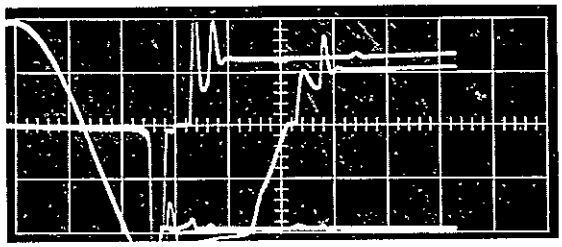


57-11

Figure 26

Typical Turn-Off Time Waveforms (t_{q_1}, t_{q_2})
100°C I_A 100A/div, V_A 200V/div
time 5 μs/div, Gate assist 0 and 2A



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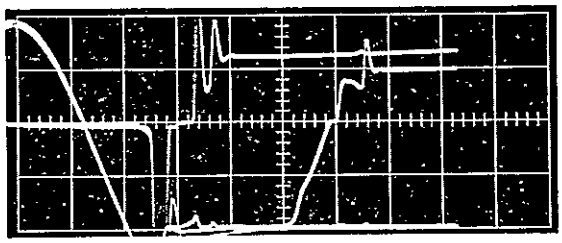

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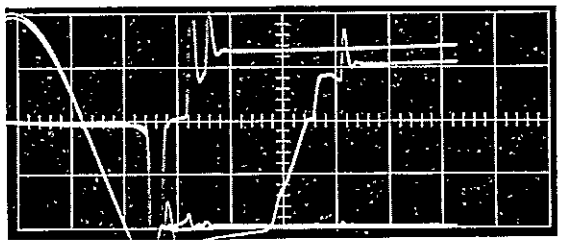
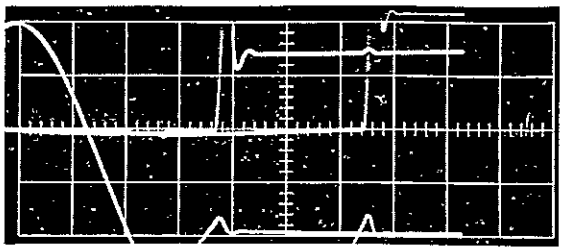


57-11

Figure 27

Typical Turn-off Time Waveforms (t_{q_3}, t_{q_4})
100°C I_A 20A/div, V_A 50V/div
time 5 µs/div Gate Assist 0 and 2A



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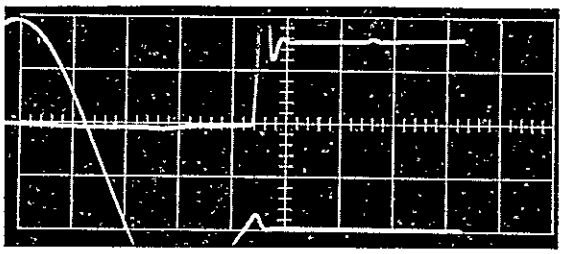

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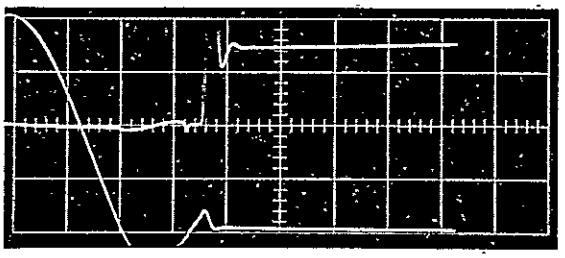
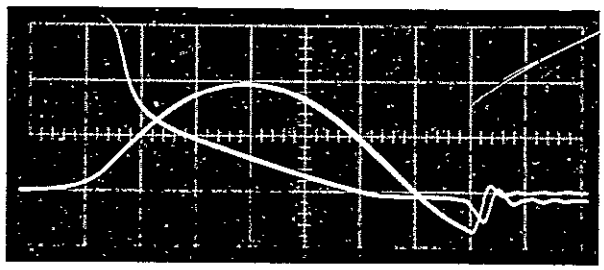


57-11

Figure 28

Typical Turn-Off Time Waveforms (t_{q_5}, t_{q_6})
100°C I_A 20A/div, V_A 50V/div
time 5 µs/div Gate Assist .0 and .2A



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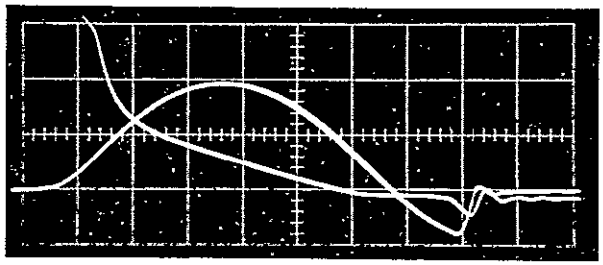

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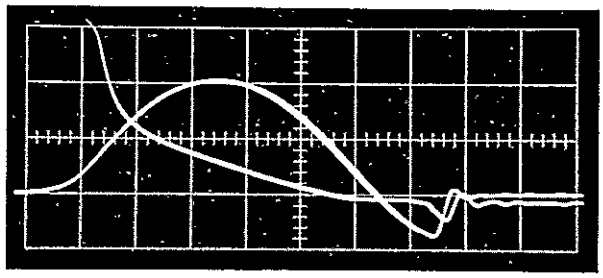

57-17

Figure 29

Demonstration of 100A/μs Capability
25°C I_G 2A, 10 μs
I_A 100A/div, V_A 5 V/div
time 1 μs/div

The devices described in Tables 6 and 7, were packaged in the newly developed package. They showed similar characteristics to those shown in Table 4.

The data in Table 8, Figures 23-29, and the above described calorimetric measurements show that the device can be made with an integrated bypass diode to perform well with good device-to-device uniformity. The difficulties that prevented us from building these devices earlier in the program were of a nature that had nothing to do with the novel features of this device design.

6. PACKAGE DEVELOPMENT

The package development effort proceeded as follows. Three package types were considered, as shown by the drawings in Figs. 30, 31 and 32. Their characteristics were analyzed by Westinghouse, NASA and TRW.

The package dimensions are shown in the drawings. The estimated weight of the flat square base style device, Sketch #A348779, with the dimensions shown and the required mounting hardware, including four BeO washers is ∿ 459 grams. By selectively thinning the square base and trimming the hardware this weight can be reduced by ∿ 88 grams to ∿ 371 grams. The weight of the flat hex base style device utilizing a leaf spring and single BeO disc, Sketch #A348780, is estimated at ∿ 308 grams. The weight of the flat pack style device utilizing the "cage type" clamp and single BeO disc, Sketch #A34871, is estimated at ∿ 345 grams.

Calculations for two distinct mounting techniques were made for device A348779, the "Flat Square-Base Device". For the first technique it was assumed that a 1.0 inch diameter BeO disc 0.10 inches thick would be used under the center of the device to conduct the heat from the square base to the heat sink and provide the electrical isolation. Epoxy heat transfer compound would be used on both sides of the BeO disc to assure that there will be no voids under vacuum environment conditions. For these conditions the calculated thermal resistance from device junction to heat sink is ∿ 0.403°C/Watt.

The second technique utilizes four (4) BeO washers around the mounting holes to provide the thermal conduction path from the device to the heat sink and also to provide the electrical isolation. In this case the washers are 0.75 inches outside diameter by 0.265 inches inside diameter by 0.10 inches thick. Epoxy heat transfer compound would be

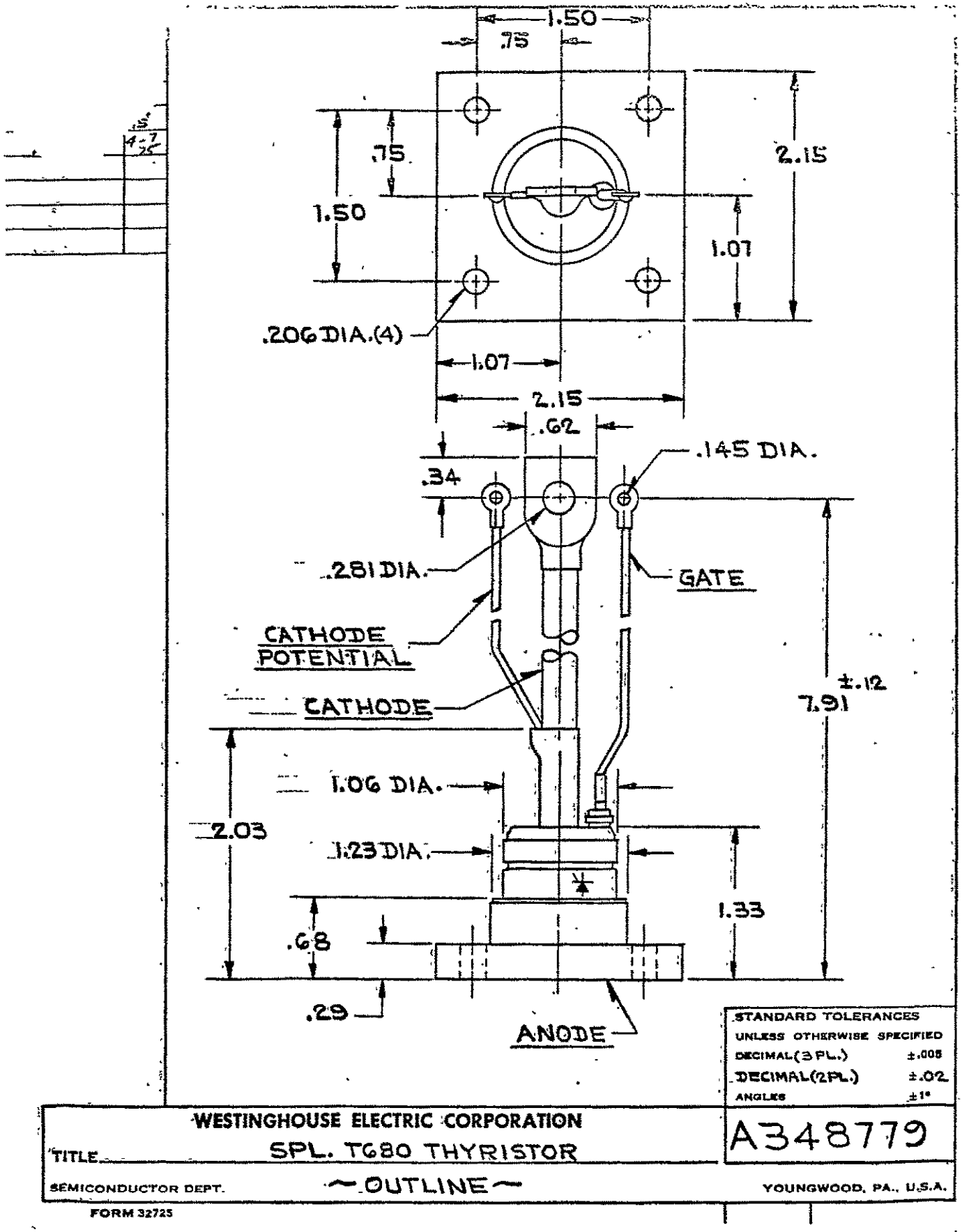
1.50
.75
.75
2.15
1.50
1.07
.206 DIA. (4)
1.07
2.15
.62
.145 DIA.
.34
.281 DIA.
GATE
CATHODE POTENTIAL
CATHODE
±.12
7.91
1.06 DIA.
2.03
1.23 DIA.
1.33
.68
.29
ANODE
STANDARD TOLERANCES
UNLESS OTHERWISE SPECIFIED
DECIMAL (3 PL.) ±.005
DECIMAL (2 PL.) ±.02
ANGLES ±1°
WESTINGHOUSE ELECTRIC CORPORATION
TITLE SPL. T680 THYRISTOR
A348779
SEMICONDUCTOR DEPT.
OUTLINE
YOUNGWOOD, PA., U.S.A.
FORM 32725

Fig. 30

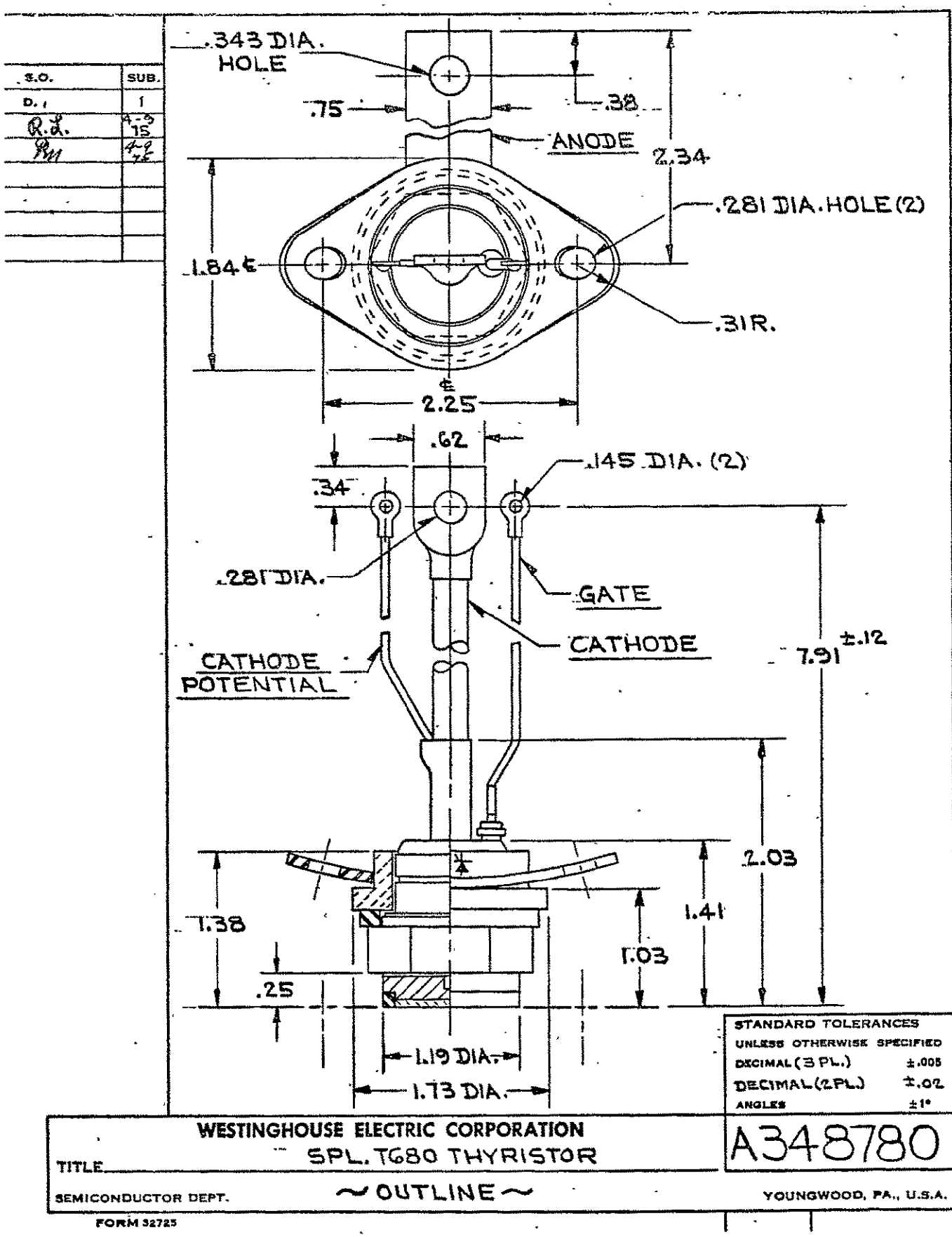
S.O.
SUB.
D.I
1
R.L.
15
RM
.343 DIA. HOLE
.75
.38
ANODE
2.34
.281 DIA. HOLE (2)
1.84
.31R.
2.25
.62
.145 DIA. (2)
.34
.281 DIA.
GATE
CATHODE
CATHODE POTENTIAL
7.91 ±.12
2.03
1.38
1.41
1.03
.25
1.19 DIA.
1.73 DIA.
STANDARD TOLERANCES
UNLESS OTHERWISE SPECIFIED
DECIMAL (3 PL.) ±.005
DECIMAL (2 PL.) ±.02
ANGLES ±1°
WESTINGHOUSE ELECTRIC CORPORATION
TITLE SPL. TG80 THYRISTOR
A348780
SEMICONDUCTOR DEPT.
~ OUTLINE ~
YOUNGWOOD, PA., U.S.A.
FORM 32725

Fig. 31

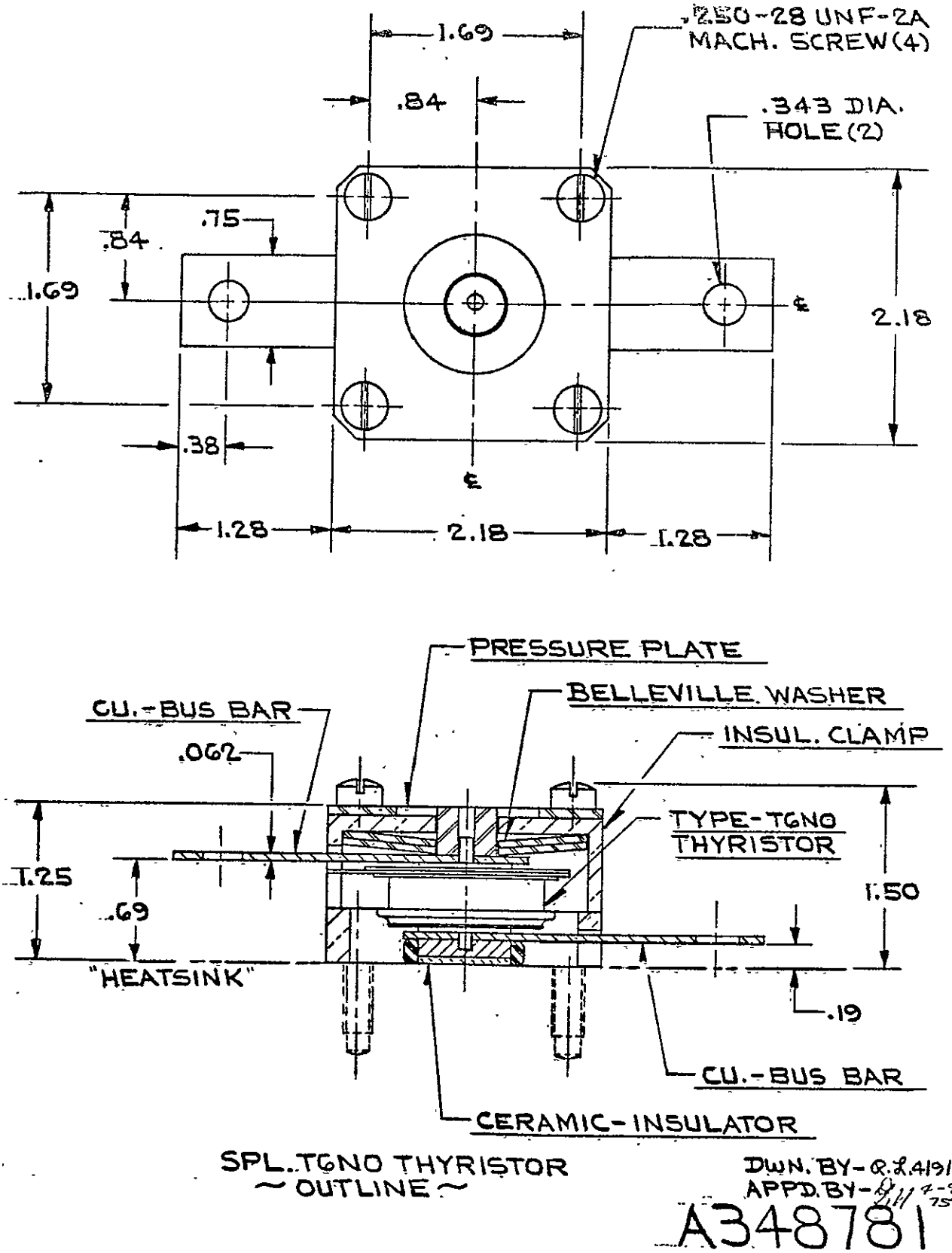
1.69
.84
.250-28 UNF-2A
MACH. SCREW(4)
.343 DIA.
HOLE(2)
.75
.84
1.69
2.18
.38
1.28
2.18
1.28
PRESSURE PLATE
BELLEVILLE WASHER
CU.-BUS BAR
.062
INSUL. CLAMP
TYPE-TGNO
THYRISTOR
1.25
.69
1.50
"HEATSINK"
.19
CU.-BUS BAR
CERAMIC-INSULATOR
SPL. TGNO THYRISTOR
~ OUTLINE ~
DWN. BY- R.L. 4/9/75
APPD. BY- 4/11 4-9 75
A348781

Fig. 32

used on both sides of the BeO washers to assure that there are no voids in the joints. In this case the calculated thermal impedance, junction to heat sink, is ∿ 0.428°C/Watt.

For calculating the thermal impedance of device A348781, the flat pack with the "cage-type" clamp assembly, it is assumed that the joint between the flat pack and the copper bus bar terminal can be made using a Sn-Pb solder alloy -- thereby eliminating the external "dry" joint. In this case a BeO disc 0.75 inches in diameter and 0.10 inches thick would be used to provide electrical isolation and thermal conduction. Epoxy heat transfer compound would be used on both faces of the BeO disc. For this case the calculated thermal impedance is ∿ 0.462°C/Watt. As has been mentioned previously, this value could be reduced by building a larger contact into the flat pack housing. Such a modification consitutes a rather major redesign, however, and would require several months to accomplish.

For calculating the thermal impedance of device A348780, the Flat Hex Base design, it is also assumed that the anode terminal would be attached to the device using a Sn-Pb alloy and a soldering process to eliminate the external "dry" joints. A BeO disc 1.0 inches in diameter by 0.10 inches thick would be used to provide electrical isolation and thermal conduction. Both surfaces of the BeO disc would be coated with epoxy thermal conductive compound to eliminate voids in thermal path. In this case, the calculated thermal impedance is ∿ 0.37°C/Watt.

The final decision was to use the design A348779. The main reason for this choice was that this package design would be least likely to distort the light weight heat sink to which the package must be mated.

In order to decrease the weight below the value given above, the cathode lead weight was decreased and an anode bus connector was not included. The final package weighed 230 gms plus 77 gms for the mounting washers, bolts, sleeves and nuts or 307 gms total.

Figure 20 showed a photograph of the new package.

7. CONCLUSIONS

A gate-assisted turn-off thyristor has been developed that is useful in efficient lightweight circuits such as those used in power processors for ion engines.

The device blocks 800-1000V forward and reverse, has a 2.6V forward drop at 2 μs and 1.6V at 10 μs into a 200A, 20 μs wide half sine wave. The turn-off time is 6-7μs at 100°C with a dV/dt of 400V/μs, making 20 kHz operation practical. Fast low loss turn-on was achieved by adding gate amplification to the GATT. Turn-off time can be lowered to 3μs or below at the expense of a higher forward drop.

It was found and demonstrated that the effectiveness of gate assist current is not, as previously thought, due to carrier sweep out but is primarily due to its opposition to the dV/dt induced forward voltage on the cathode junction. Based on this finding, it was demonstrated that cathode shunting, which imparts good performance and reliability to nearly all other types of modern thyristors, can also be used to advantage in GATT's.

It was found that the resistance in the p-base, under the cathode, significantly influences the effectiveness of gate assist current on the turn-off time.

A useful design curve was developed that shows the possible tradeoffs between t_q and V_{TM}. The generation of this type of curve is possible when electron irradiation is used to kill lifetime because electron irradiation can be used in stepped increments to decrease the lifetime of otherwise finished devices. The generation of such a curve would not be practical if gold were used to kill the lifetime. A physical understanding of the nature of this tradeoff curve was developed. This curve made it possible for the user of the devices to select,

after the program was well underway, a better point on this tradeoff curve for the device to be built to give the most efficient performance in the circuit.

It was found that in order to use gate amplification in a GATT, one must introduce a diode so that the gate assist current bypasses the resistance in the p-base under the auxiliary cathode. Three configurations of bypass diodes were used in this effort and problems with each were defined.

A new lightweight package was designed and built for the device because of the significance of weight in NASA's applications.

Overall, the efforts have significantly improved the understanding of the behavior of, and provided an improved basis for designing, gate assisted turn-off thyristors of a type that can be, and are being, used by NASA in the construction of circuits with improved efficiency for deep space missions.

ACKNOWLEDGEMENTS

The authors acknowledge the support of the personnel of the Westinghouse Semiconductor Division in the fabrication of the devices and of J. B. Brewster in the testing. L. E. Hohn and L. V. Rohall also made contributions to the program.

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APPENDIX A

A Technique for Optimizing the Design of Power Semiconductor Devices

EARL S. SCHLEGEL, SENIOR MEMBER, IEEE

Abstract—**A technique is described that provides a basis for predicting whether any device design change will improve or degrade the unavoidable trade-off that must be made between the conduction loss and the turn-off speed of fast-switching high-power thyristors. The technique makes use of a previously reported method by which, for a given design, this trade-off was determined for a wide range of carrier lifetimes. It is shown that by extending this technique, one can predict how other design variables affect this trade-off. The results show that for relatively slow devices the design can be changed to decrease the current gains to improve the turn-off time without significantly degrading the losses. On the other hand, for devices having fast turn-off times design changes can be made to increase the current gain to decrease the losses without a proportionate increase in the turn-off time. Physical explanations for these results are proposed.**

I. INTRODUCTION

THE SIZE, weight, and cost of high-power electronic equipment can be reduced if the circuitry can be designed to operate at higher frequencies. This is due to the smaller size and weight of high-frequency components. For this reason, and the desire to use solid-state components in applications requiring higher and higher frequencies, development efforts are currently being directed toward improving fast-switching semiconductor devices.

The focus of these development efforts is on improving the trade-off between the device dissipated losses and the turn-off speed. The importance of this trade-off can be briefly described as follows. The turn-off time limits the duty cycle and frequency capability of a thyristor. Energy losses dissipated in the thyristor degrade the efficiency of the circuit and increase the operating temperature of the thyristor. The increased temperature decreases the power handling capability of the thyristor and, because it degrades the turn-off time [1]–[4], decreases its frequency capability. Hence the need to design for the best combination of losses and turn-off speed.

Unfortunately, design changes always affect the loss and speed in opposite directions and one is forced to find the best compromise. For a number of reasons, the effect of a design change on this compromise is difficult to determine. It is fairly simple to predict how a design change will affect the losses or the turn-off speed individually—any change that increases the current gains of the transistors in the two-transistor analog will decrease the losses and degrade the turn-off speed. On the other hand, a prediction of whether a given design change will improve or degrade the

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The author is with the Research and Development Center, Westinghouse Electric Corporation, Pittsburgh, PA 15235.

trade-off between these parameters is very difficult. This difficulty arises from the following:

1) The complexities of the three-dimensional, and temperature-sensitive, nature of thyristor physics makes quantitative calculations very difficult. There are many design variables and their interactions are complex. The list of design variables includes the shape, size, spacing, and pattern of the cathode shunts; the shape, effective line width, and perimeter length of the cathode; the width and dopant profile both of the p-base and the n-base; the dopant diffusion profiles of both the cathode and the anode; and the carrier lifetime and its spatial variations.

2) For any set of device-design and operating-condition variables it is difficult to determine the optimum carrier lifetime level.

3) The conditions that influence those current gains that determine the conduction losses are different from those that determine the turn-off speed. The current gains that determine the conduction losses are the result of high current densities, of a forward-biased collector junction, and are an average for a large conducting area. On the other hand, the current gains that affect the turn-off speed involve much lower current densities, a reverse-biased collector junction and, perhaps, a small local area.

4) A design change that seemingly affects the current gain of only one transistor in the two-transistor analog causes changes in the current densities and voltages, and therefore in the current gains, of both transistors. For these reasons it has been impractical to use theoretical analyses for determining the effects of design changes on the trade-off between the losses and turn-off speed.

Experimental studies have also been impeded by a number of practical problems. Typically, because a single device fills an entire 23 to 50-mm-diameter slice, one is limited to a relatively small number of test samples. There are many possible sources of sample-to-sample variability. The starting slice can have variability in the resistivity, lifetime, defect density, surface conditions, and thickness. Additional variability can be added at any or all of the diffusion steps (often as many as five), the oxidation steps (often two), and intermediate lapping or etching steps. A systematic empirical study is therefore costly and subject to variables in parameters that are difficult to control.

Thus the ability to study the effects of individual design variables in large expensive power thyristors would be improved if the sample-to-sample variability, and therefore the necessary sample size, could be decreased.

This paper describes a technique by which this can be accomplished.

II. Approach to The Problem

In generalized terms, the above-described difficulties can be decreased if a way can be found by which a relatively large amount of information can be extracted from relatively small number of samples. Fortunately, a technique is already developed and is in use routinely on production quantities of high-power semiconductor devices that provides this capability [5]. By this technique, high energy

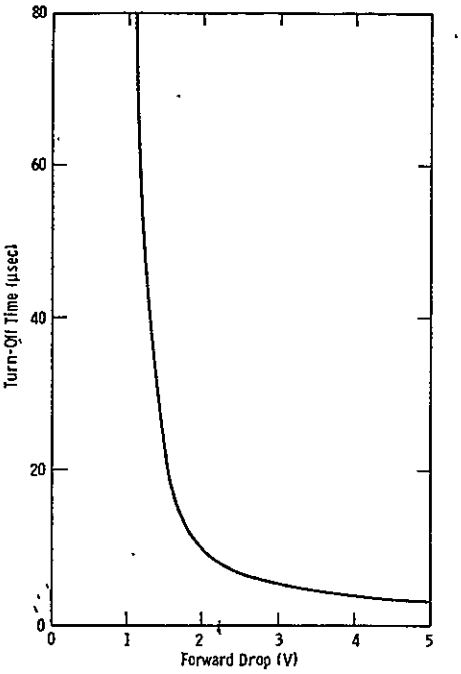

Fig. 1. Typical trade-off relationship between forward drop and turn-off time of power thyristors.

electron irradiation is used in small incremental steps to produce, in individual devices, well controlled incrementally stepped changes in carrier lifetime. For example, Chu, Bartko, and Felice [5] have measured the forward drop and the turn-off time between the irradiation steps and generated trade-off curves of the type shown in Fig. 1. From these curves they have been able to precisely determine the exact amount of irradiation that will yield the best-trade off in forward drop and turn-off time for a given application.

The subject of this paper is an extension of the capability represented by Fig. 1. Fig. 1 shows only how the carrier lifetime affects the trade-off for a given device design. In the following it is shown how the many other design variables affect this trade-off. It is qualitatively well understood how any design variable, say the p-base width or the cathode geometry, affects the current gains in the two-transistor analog. It is also understood that an increase in these current gains decreases the losses and increases the turn-off time. The difficult problem is to predict whether a given design change will improve or degrade the trade-off between these parameters.

The trade-off curve given in Fig. 1 shows that when the samples are heavily irradiated, the forward drop V_{TM} is sensitive and the turn-off time t_q is insensitive to the carrier lifetime, and that when the samples are only slightly irradiated, the opposite is true. One might infer from this that other design changes that increase the current gains will improve the V_{TM} faster than they degrade the t_q in heavily irradiated samples and that the converse would occur in lightly irradiated samples. An experiment described in the next section shows that this does indeed happen. A-2

Fig. 2. Photograph of the cathode diffusion mask.

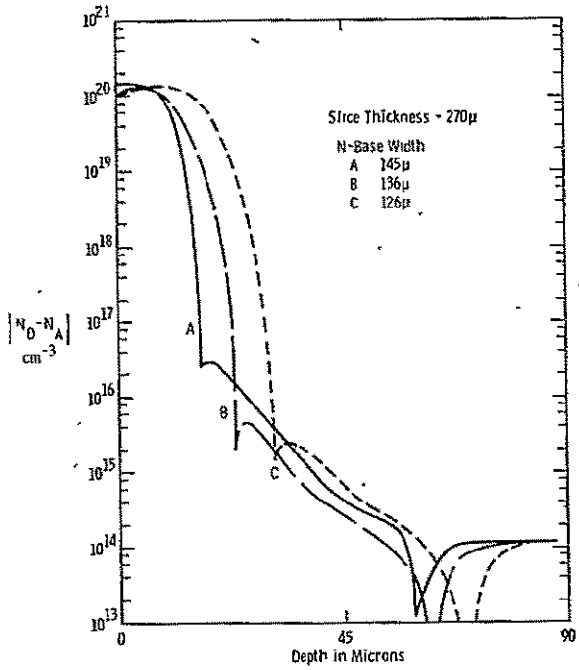

Fig. 3. Impurity density profiles measured by spreading resistance [6].

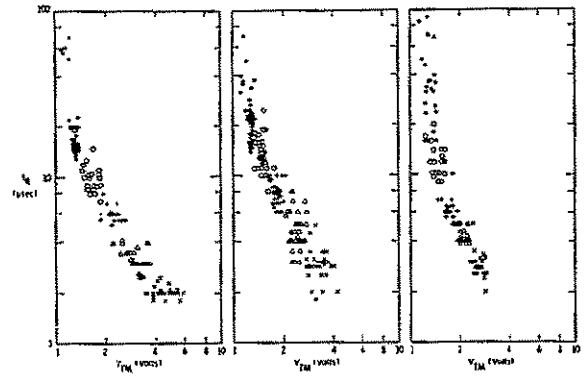

Fig. 4. Measured turn-off time t_q and forward drop V_{TM}. The different point styles indicate different irradiation doses. (Conditions: t_q, I_{TM} = 200 A, di/dt = −25 A/μs. dv/dt = 400 V/μs to 400 V, 100°C; V_{TM}, I_{TM} = 200 A, 25°C.)

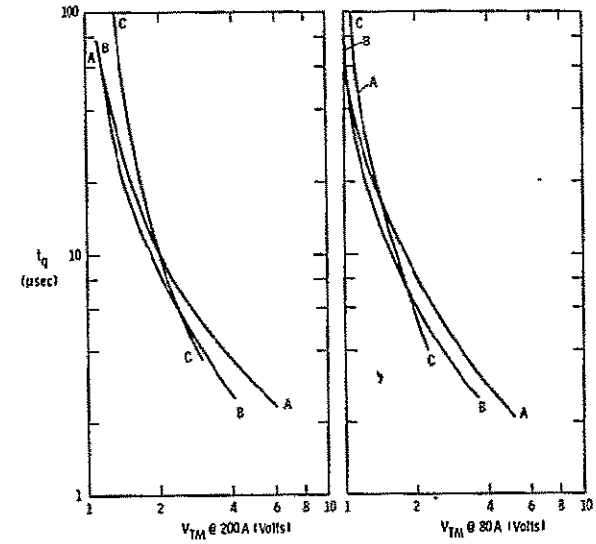

Fig. 5. Comparisons of $t_q - V_{TM}$ curves for the three impurity density profiles.

III. Experimental Details

To evaluate the validity of the inference made above, the following experiment was performed. The test structure used was a developmental thyristor that is similar to commercially available, high-speed high-power thyristors.

Fig. 2 is a photograph of the cathode diffusion mask. The samples were made from a single processing run, in which three sublots were created by varying the length of the phosphorus diffusion time to produce the measured [6] impurity profiles given in Fig. 3. Following the phosphorus diffusion, the three sublots were finished without any additional difference in the processing. The completed thyristors were then tested for t_q and V_{TM} after each of five steps in which the carrier lifetime was progressively and incrementally decreased by means of high energy irradiation.

The measured t_q and V_{TM} were plotted as given in Fig. 4. To facilitate comparisons, single-line curves were fitted to the data and superimposed as given in Fig. 5. Fig. 5 also summarizes similar data for which the V_{TM} was measured at 80 A. The differences between profiles C and A in Fig. 4 are such that C gives the higher current gain. That is, diffusion profile C has a narrower n-base, a narrower p-base, and a lower density of acceptor atoms in the p-base.

As predicted, the data in Figs. 4 and 5 show that a change that is known to increase the current gains has improved the trade-off between V_{TM} and t_q at the low-carrier-lifetime end of the trade-off curve and degraded it at the high-carrier-lifetime end of the curve.

IV. Discussion

Physically, this finding can be explained as follows. The current gains that determine t_q are different from those that determine V_{TM}. The current gains are very sensitive to current density, which is much higher under the conditions of forward conduction than for turn-off. They are also sensitive to the voltage on the central junction, which is the collector junction for both transistors in the two transistor analog. This junction is forward biased for V_{TM} and reverse biased for t_q. Furthermore, the current gains

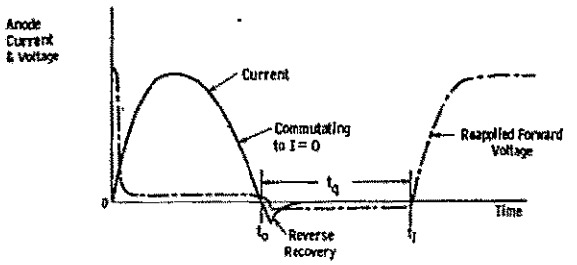

Fig. 6. Definition of turn-off time t_q of a thyristor.

that establish the V_{TM} are averaged for the entire device area while those that influence the t_q are determined only by the first small area to become regenerative.

Because of these differences, a change in any design parameter can change the V_{TM}—and the t_q—determining current gains differently.

A conducting thyristor with high carrier lifetimes has high excess carrier densities [7]–[9] with recombination rates that may be dominated by Auger recombination. When this same thyristor is in the turn-off mode, the carrier densities are much lower and the recombination is lattice-defect determined. In this case, a decrease in the lifetime due to an electron irradiation has a much larger effect on t_q than on V_{TM}.

If the lifetime is progressively decreased, the effect of Auger recombination becomes less significant and changes in lifetime have an increasing effect on V_{TM}.

When the lifetimes are decreased to much lower levels, the effect of lifetime on t_q appears to be decreasing. This is probably due to the manner in which t_q has been defined. The definition [10] of t_q includes, as shown in Fig. 6, the reverse recovery time. Reverse recovery times are much less sensitive than turn-off times to changes in the carrier lifetime.

Therefore, when the t_q is decreased to the level where it approaches the reverse recovery time, it becomes relatively insensitive to the carrier lifetime. These arguments explain the shape of the curve in Fig. 1.

Other device design changes similarly have a greater effect on one set of current gains than on the other as demonstrated in Fig. 5. Thus design changes should be made to improve whichever parameter is most sensitive to a change in current gain. That is, when t_q is high, one should decrease the current gain because this decreases the t_q with little detriment to V_{TM}. On the other hand, when V_{TM} is high, the current gain should be increased to decrease V_{TM} with little detriment to t_q.

By this technique, a device designer can, with a relatively small number of devices, improve and optimize the trade-off between forward drop and turn-off time. Further, the technique provides the means for determining where the cross-over point between the two extremes is.

V. Conclusions

A technique has been described and demonstrated that provides a basis for predicting whether a given device design change will improve or degrade the unavoidable trade-off between the conduction loss and the turn-off speed of fast-switching high-power thyristors.

Data are given that show that, at high-carrier-lifetime levels, a design change that decreases the current gains in the two-transistor analog will improve the turn-off time more significantly than it will increase the conduction loss. On the other hand, the data show that, at low-carrier-lifetime levels, a design change that increases the current gains will improve the losses more significantly than it will degrade the turn-off time. Since a device designer knows how to design for a change in the current gains this technique gives him a basis for designing for a better trade-off between V_{TM} and t_q.

Explanations are given for these results. It is proposed that in a device with a high lattice-defect-determined lifetime, the turn-off speed is sensitive to this lifetime, while the conduction losses are mainly dependent on Auger recombination which is hardly sensitive to the lattice-defect determined lifetime. On the other hand, in a device with a low lattice-defect-determined lifetime, Auger recombination is less significant and the losses are sensitive to the lattice-defect-determined lifetime. In this case, the turn-off speed becomes insensitive to lifetime because it becomes limited by the reverse recovery time.

Acknowledgment

The author is pleased to give recognition to J. Bartko, C. K. Chu, P. E. Felice, and K. S. Tarneja who developed the capability for using electron irradiation for tailoring the performance of power semiconductor devices. He is indebted to J. B. Brewster for his support in the taking of the electrical measurements and to E. Dombrowski for his part in the preparation of the samples. The author thanks M. H. Hanes, D. J. Page, and D. K. Schroder for their critical reading of the manuscript.

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Gate-Assisted Turnoff Thyristors

APPENDIX B

EARL S. SCHLEGEL, SENIOR MEMBER, IEEE

Abstract—**A study of the turnoff physics in gate-assisted turnoff thyristors (GATT's) leads to a proposed mechanism involving the gate bias acting to prevent a forward voltage from appearing on the cathode rather than, as was previously thought, to sweep out excess carriers.**

It is shown that cathode shunting can be used in GATT's to virtually eliminate an important failure mode and to decrease the gate voltage needed to produce the desired improvement in turnoff time. Implications for designing GATT's are given, one being that a change in the lateral resistance of the p-base will have opposite effects depending on whether the cathode is shunted or not.

I. Introduction

THE SIZE, weight, and cost of high-power electronic circuitry can be decreased if the circuit can be designed to operate at higher frequencies. This is due to the fact that the components of higher frequency circuits are smaller in size and lighter in weight. With the increasing usage of thyristors in higher frequency power electronic circuits, it becomes necessary to determine more clearly how the frequency capability of a thyristor is limited and to explore possibilities for increasing the high-frequency capabilities of thyristors.

The frequency capability of thyristors is limited by the turnoff time of the thyristors. This turnoff time t_q is defined [1] as the time, after the anode current of the thyristor has been commutated to zero, that is necessary for the excess carrier density distribution to decay to a level at which forward voltage can be reapplied without refiring the thyristor. Extensive efforts are being made to design and build thyristors with short turnoff times.

The thyristor designer wants both fast turnoff time and low losses. He recognizes that this calls for high current gains while the device is in its conducting state and for low current gains when the device is to be turned off. Since this is difficult to achieve by device design alone, efforts [2]–[4] have been made to design thyristors that can be operated in a manner in which the current gains can be significantly changed by the operating conditions of the conducting and the turnoff periods. Thyristors designed to operate in this manner have been called gate-assisted turnoff thyristors (GATT's) [2]–[4].

The objective of the work of this paper is to provide a physical understanding of gate-assisted turnoff and to discuss the implications of this understanding for the design of thyristors for which gate assist is to be effective.

II. Definition of Gate-Assisted Turnoff

Gate-assisted turnoff is the name given to the method for turning off a thyristor with the usual commutation of the anode current but with the addition of a negative pulse applied to the gate during the time when forward anode voltage is being reapplied. This negative gate pulse decreases the turnoff time; that is, it allows one to reapply the forward voltage earlier without refiring the thyristor. (GATT's must not be confused with devices usually called gate-turnoff thyristors (GTO's) or gate-controlled switches (GCS's), that can be turned off with a gate signal without commutating the anode current.)

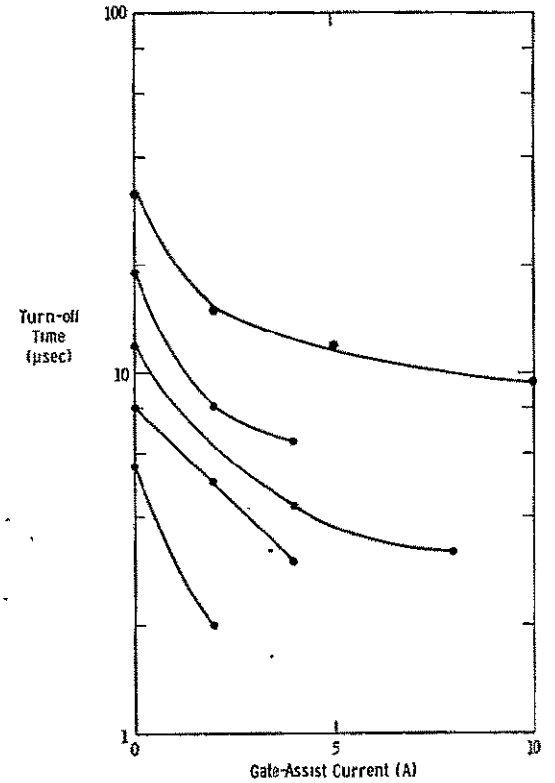

Fig. 1. Dependence of measured turnoff time on gate-assist current. (Conditions: 100°C, 25 A/μs, 400 V/μs.) Each curve represents a device having a different carrier lifetime level created by different doses of high-energy electron irradiation.

Fig. 1 gives typical data that show how the turnoff time is decreased by the negative gate current pulse (gate-assist current). The cathode diffusion mask, which is shown in Fig. 2, was the same for all of the devices represented in Fig. 1. The difference between devices represented in Fig. 1 was the value of the carrier lifetime. The devices represented in Fig. 1 have forward and reverse blocking voltages of 1000 V, and a device that has a turnoff time of 6 μs with 2 A of gate-assist current has a V_{TM} of 1.5 V at 200 A. The slice diameter is 23 mm. Fig. 2 shows that the cathode design contains shunts down the middle of the cathode fingers. All previous designs for GATT's have not used emitter shunts [2]–[4]. As is shown in this paper, shunts can be used to advantage both to gain a better understanding of and to improve the performance and reliability of GATT's.

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The author is with the Westinghouse Research Laboratories, Pittsburgh, PA 15235.

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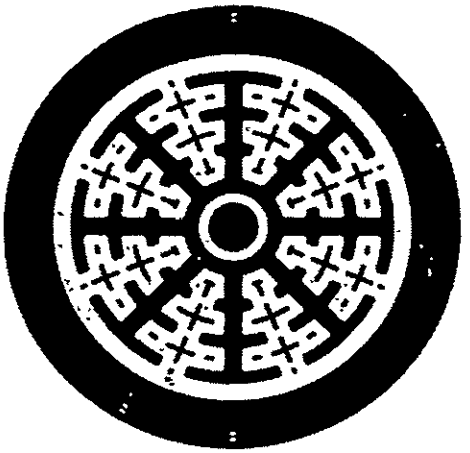

Fig. 2. Photograph of the cathode diffusion mask.

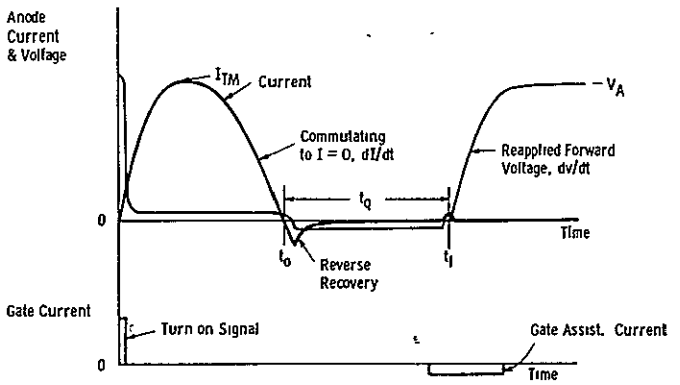

Fig. 3. Typical anode current and voltage of a thyristor.

III. Physics of Thyristor Turnoff

A. Outline Description of the Model

Fig. 3 shows typical waveforms of the voltage and current of a thyristor during one cycle of its operation. The turnoff time t_q is the minimum time interval between the time t_0 at which the anode current has been commutated to zero, and the time t_1 at which a forward voltage can be reapplied to the thyristor without refiring the thyristor. In this section, the physics of turning off a thyristor is briefly reviewed so as to provide the basis for describing the physics of gate-assisted turnoff.

The description of the model will be best understood if the reader understands how all thyristors involved in commutated turnoff go through the following sequential steps:

1) conduction;
2) current commutation;
3) current polarity reversal;
4) reverse recovery;
5) dV/dt-induced displacement current creation of forward bias on the cathode junction.

The thyristor will fail to turn off if this IR drop causes sufficient injection from the cathode to refire the thyristor.

Two models for the effectiveness of gate-assist current will be described: 1) earlier model—carrier sweep out; 2) this model—decreased forward bias on cathode junction.

B. Thyristors in General

The anode emitter of a thyristor in the conducting state injects holes uniformly from its entire area. This creates an excess hole density and, because the region is space-charge neutral, an excess electron density that is fairly uniform over the entire area of the n-base. At the initiation of turnoff, the anode current is commutated and the emitters stop injection. Excess charge densities decrease in the n-base both because of carrier flow across the boundaries of the n-base and because of recombination within the n-base. At this time the anode-to-cathode voltage has not yet reversed.

Later, when the *excess* charge densities have decreased to zero at the anode junction, the current-carrying capability of the anode junction drops abruptly and the device "blocks." The anode-to-cathode voltage is reversed at this point and the device becomes capable of supporting a high reverse voltage. This is reverse recovery. At this stage of turnoff, the anode junction limits the current to a sharply reduced value. The voltage polarity on this junction prevents electrons from leaving the n-base through the anode junction. On the other side of the n-base, at the central junction, the dopant density distributions are such that this junction emits holes from the p-base in much greater number than it emits electrons from the n-base. Therefore, only a small proportion of the already small anode-junction-limited current consists of electrons flowing from the n-base to the p-base. Clearly, after reverse recovery, the flow of excess electrons from the n-base is nearly stopped at both junctions. An equal number of excess holes are present to neutralize the charge of these electrons to maintain space-charge neutrality. At this stage of turnoff, even though the anode junction has undergone reverse recovery, there is a substantial amount of excess charge "blocked" in the n-base of the thyristor. This charge plays an important role in determining the turnoff time. Since it is blocked from flowing out, the lifetime of these carriers in the n-base strongly influences the turnoff time. Assalit and Studtman [5] have suggested taking this charge out via an electrode attached to the n-base but the use of an n-base lead is undesirable because it complicates both the manufacturing process and the circuit design.

When forward anode voltage is reapplied, the anode junction again becomes forward biased and electrons can flow out the anode junction. As electrons flow out to the anode, holes can, because of space-charge neutrality, flow out to the p-base and on out through the cathode. This current continues until the excess charge at the central junction is reduced to zero, and then forward recovery [6] occurs at the central junction in a manner very similar to that of reverse recovery.

The forward-recovery (dV/dt-induced displacement) current plays a very important role in the physics of turnoff of a thyristor, and a good understanding of the behavior of forward-recovery current is necessary if one is to understand the behavior of turnoff time.

A study [6] of forward-recovery current shows that it:

1) Decreases exponentially with increasing time after the anode current reversal, as shown by the superimposed waveforms given in Fig. 4 and the curves in Fig. 5.

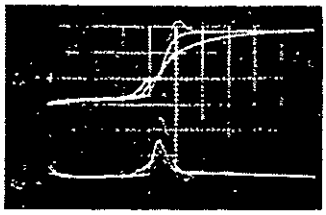

Fig. 9. Top: anode voltage (200 V/div). Bottom: anode current (2 A/div), time (1 μs/div), temp. 100°C. The effect of the dV/dt on the forward-recovery current pulse height and pulse sharpness. Each set of curves was photographed just at the point at which a shorter turnoff time interval would refire the thyristor. The time axis was shifted to superimpose the start of the dV/dt ramps to facilitate the comparisons of the waveforms The actual turnoff time increased with the increasing dV/dt.

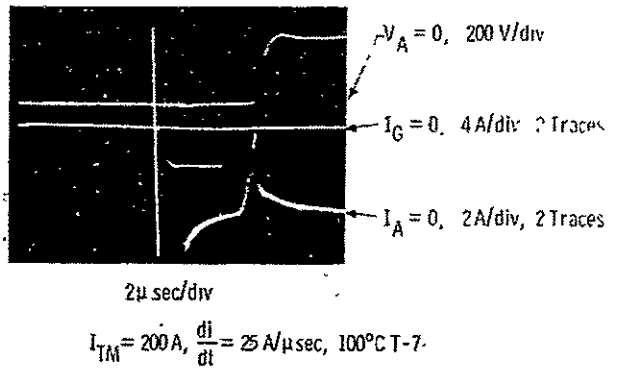

Fig. 10. Photograph of forward-recovery current both with and without 4 A of gate-assist current.

the onset of forward-voltage-induced displacement and the forward-recovery point (at the recovery current peak) decreases with increasing dV/dt. It is this leading portion of the forward-recovery pulse that determines whether the device refires.

Of course, the diffusion layer profiles and the n-base width and resistivity, the carrier lifetime, and the junction temperature all influence the current gains of the n-p-n and the p-n-p transistors that constitute the thyristor. These design variables, therefore, all influence the magnitude of the forward-recovery-current-induced IR drop that is necessary to cause a refiring of the device.

C. Gate Assisted TurnOff

Carrier Sweep Out Model: Previous investigators [2], [4] had proposed that the function of gate-assist bias, in decreasing the turnoff time, is to sweep out excess carriers through the gate so as to decrease the excess carrier density more rapidly than by recombination alone. However, there is a difficulty with this model in that it does not explain why gate-assist current, drawn before the forward voltage is reapplied, does not significantly improve the turnoff time. That is, the gate-assist current is helpful only if it is present during the interval when the forward voltage is being reapplied. As Fig. 10 shows, the forward-recovery current is also insensitive to gate-assist current drawn before dV/dt is reapplied.

D. Cathode-Voltage Prevention Model

In the preceding model for the turnoff of thyristors, the voltage developed on the cathode junction plays a key role

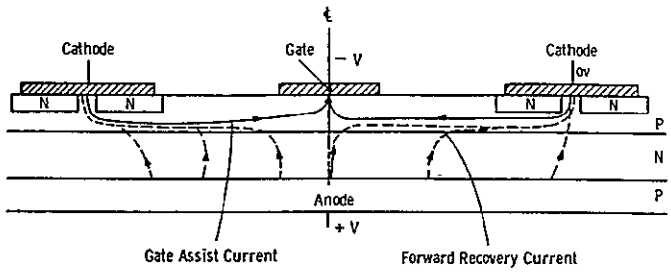

Fig. 11. Improved model for gate assist. Gate assist is effective because it provides an IR drop that opposes the IR drop generated by the forward-recovery current

in determining whether the thyristor will turnoff, that is, whether it will support reapplied forward voltage or refire. In the cathode-voltage prevention model for gate-assisted turnoff the effect of gate-assist bias is to prevent the development of a forward voltage on the cathode junction. In GATT's which have no cathode shunting, the gate-assist bias diverts the forward-recovery current from the cathode to the gate. Because of this diversion of the current, the cathode junction becomes less forward biased and injects a lower density of electrons into the p-base. Therefore, the thyristor is less likely to refire. In this case, it is desirable to have low lateral resistance in the p-base under the cathode so that the forward-recovery current can easily be conducted to the gate without producing an IR drop that would forward bias the central part of the cathode.

In GATT's with properly designed cathode shunts, the gate-assist bias causes current to flow from the cathode shunts to the gate. This current produces a lateral IR drop in the p-base that, along with the centrally located shunt, prevents a forward drop from appearing on the cathode junction. This is depicted in Fig. 11. In this case, a greater counteracting effect for a given gate-assist current level can be achieved if the lateral resistance in the p-base is higher. Alternatively, for a given gate-assist voltage an increase in this lateral resistance will decrease the gate-assist current and power.

Cathode shunts can be used in GATT's to improve both the device reliability and performance.

The nature of gate-assist current is that it is most effective at the edge of the cathode. In an unshunted cathode it is very possible for the initial refiring to occur in the middle of the cathode. Once firing occurs centrally in an unshunted cathode, gate-assist current pinches the conducting area and thereby confines the fired area to the middle of the cathode causing overheating and oftentimes failure of the device. On the other hand, a central shunt forces the initial firing to occur at the cathode edge where gate-assist current is more effective, and this eliminates the failure mode.

Shunts can also improve the reliability of GATT's because they increase the certainty that the auxiliary thyristor will fire before the main thyristor when gate amplification is used. While a discussion of gate amplification is beyond the scope of this paper, it can be used to good advantage in GATT's. To do this it is necessary to have an antiparallel bypass diode across the auxiliary cathode. Without this diode, when gate-assist bias is applied, the

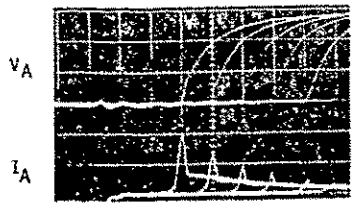

Fig. 4. Forward-recovery current dependence on time of application reapplied forward voltage. $I_{TM} = 50$ A, $(di_R/dt) = -25$ A/μs, $V_A = 200$ V/div, $I_A = 2$ A/div, time = 2 μs/div, temp = 100°C.

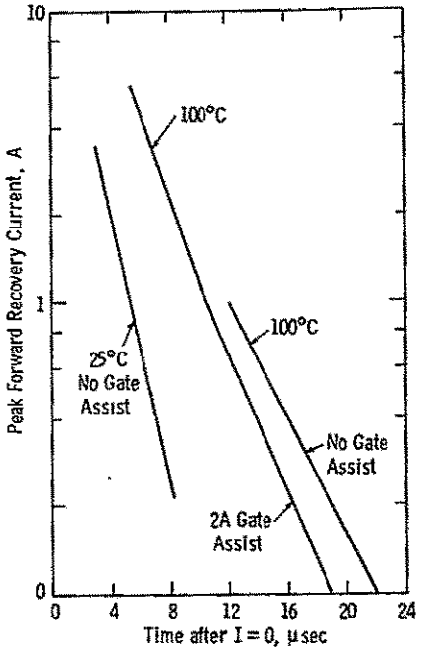

Fig. 5. The dependence of the forward-recovery current on the time of the application of forward voltage.

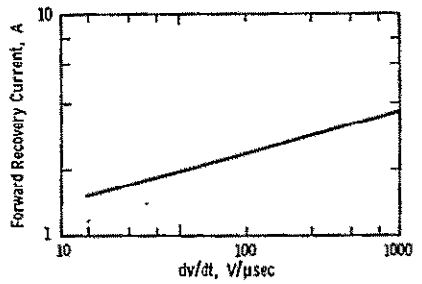

Fig. 6. Effect of dv/dt on forward-recovery current. $I_{TM} = 150$ A, $(di_R/dt) = -25$ A/μs, 100°C, $t_q = 8$ μs.

2) Increases with dV/dt as shown in Fig. 6.

3) Increases with junction temperature as shown in Figs. 5 and 7.

4) Increases with increasing di_R/dt, the rate of commutation of the anode current.

5) Increases with increasing carrier lifetime.

The turnoff time and the dV/dt rating depend on the forward-recovery current as follows. The forward-recovery current enters the p-base over the entire area of the middle junction and flows to, and out through, the cathode. If the cathode is unshunted, a forward bias is developed on the cathode junction to the degree necessary to carry the forward-recovery current. If it is shunted, the forward-recovery current flows to and out the shunts. This current creates a voltage drop in the p-base as shown in Fig. 8. This

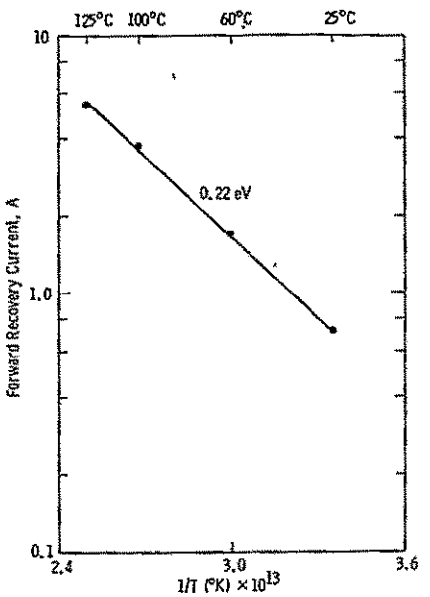

Fig. 7. Effect of temperature on forward-recovery current $I_{TM} = 150$ A, $(dI_R/dt) = -25$ A/μs, $(dv/dt) = 400$ V/μs, $t_q = 8$ μs

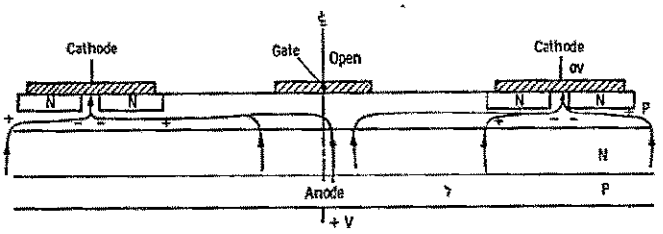

Fig. 8. Forward-recovery-current-induced IR drops in p-base. Forward-recovery current creates an IR drop in p-base under the cathodes that forward bias the cathode emitters.

voltage drop depends on:

1) The magnitude of the forward-recovery current.

2) The lateral resistance in the p-base to this current. This depends both on the sheet resistivity of the p-base under the cathode and on device geometrical factors that determine the current path distribution in the p-base.

Since the lateral resistance is different for different areas of the thyristor structure, it is important that the area being examined be that in which the dV/dt is most likely to refire the device. For example, if there is an auxiliary cathode one must know whether the dV/dt fires the main or the auxiliary cathode first.

If the IR drop in the p-base due to the forward-recovery current is greater than about 0.7 V, it will forward bias the cathode emitter and causes injection from the cathode. If this cathode injection continues long enough, the injected carriers diffuse through the thyristor bases and build up a distribution of excess carriers that is sufficient to refire the thyristor.

Because the time it takes to build up the carrier distribution (about 1 μs) depends on the injected carrier density, the IR drop that is capable of refiring the thyristor depends on the duration of the forward-recovery current pulse. This forward-recovery current pulsewidth, in turn, depends on the dV/dt applied to the anode. This is illustrated in Fig. 9, which shows how the peak forward-recovery current increases with increasing dV/dt. The time interval between

resistance of the auxiliary cathode degrades the effectiveness of the gate-assist bias on the turnoff time. Furthermore, depending on the gate-assist current drawn through this resistance, it can heat up the auxiliary region of the thyristor to the point of degradation or failure.

Shunts prevent the forward-recovery current from firing the thyristor centrally in the cathode, and therefore the gate-assist bias voltage can be lower. Gate voltages of only 1–3 V were needed to produce the data of Fig. 1. On the other hand, unshunted GATT's require 10–20 V of gate-assist bias [2]–[4].

E. Design Guidelines

Based on this understanding, the following is a set of guidelines for designing thyristors for which gate-assist current is effective.

1) Interdigitate the gate and cathode.

2) Minimize the gate area to minimize forward-recovery current from gate areas.

3) If the cathode is not shunted, design for low lateral resistance in the p-base.

4) Shunts can be used in GATT's to virtually eliminate an important failure mode, to decrease the gate-assist voltage, and to insure proper performance of an amplifying gate.

5) If the cathode is shunted, the lateral resistance of the p-base under the cathode must be high enough that the gate-assist current develops an IR drop greater than 0.7 V.

6) The shunts must be designed so that the gate-assist current is uniformly effective over the entire cathode area.

IV. Conclusions

A study of the effectiveness of a negative gate bias for shortening the turnoff time of thyristors has resulted in a new hypothesis for the turnoff mechanism of GATT's. The results indicate that the effect of gate-assist bias is one of preventing forward voltage from appearing on the cathode junction rather than one of sweeping out excess carriers. GATT's can be made with cathode shunts to virtually eliminate an important failure mode and to decrease the gate voltage necessary to significantly decrease the turnoff time.

Design guidelines for improved GATT performance and reliability are given. It is shown that varying the lateral resistance of the p-base will have opposite effects depending on whether or not the cathode is shunted.

Acknowledgment

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Appendix C

GATE ASSISTED TURN-OFF THYRISTOR WITH CATHODE SHUNTS AND DYNAMIC GATE

Earl S. Schlegel and Derrick J. Page

Westinghouse Research Laboratories

Pittsburgh, PA 15235

ABSTRACT

A 1000V, 200A gate-assisted turn-off thyristor (GATT) is described that was developed for, and is being used in, circuitry for space applications requiring high efficiency and reliability as well as small size and weight. The design features include an interdigitated shunted cathode, a dynamic gate, a means for optimizing the carrier lifetime level, and a bypass diode. The bypass diode is necessary to permit the combination of both dynamic turn-on and gate-assisted turn-off in the same device. Two versions of this diode are described.

The device physics of gate-assisted turn-off will be reviewed. Based on this, improvements in the design will be described. It is shown that a prime failure mode can be eliminated and that the gate-assist signal voltage can be substantially decreased by employing a shunted cathode emitter.

The test data show excellent turn-on characteristics due to the dynamic gate and the long perimeter of the edge of the main cathode. Turn-off times as short as 3 μsec are obtained. The effect of the gate-assist current on the turn-off time is described.

The combination of controlling the carrier lifetime with a precisely controlled and easily variable irradiation dose of high energy electrons with gate assist current provides for simple, precision tailoring of the device characteristics to the intended application.

INTRODUCTION

The weight and efficiency of the electric propulsion power processing equipment will be very important for the design of spacecraft being planned for the exploration of deep space in the 1980's. The size and weight of solid state power conditioning equipment can be reduced if the operating frequencies can be increased because smaller circuit components can be employed. High efficiency, so important in the high-power circuitry in spacecraft, requires that the switching losses in the thyristors be held to a minimum. This paper describes a thyristor development part of a program sponsored by NASA Lewis Research Center to develop a reliable and efficient power processor for an electric propulsion engine.[1]

The requirements for both fast switching and low switching losses are difficult to achieve in a single device. Any change in a device design that increases the current gain decreases the turn-on switching loss and conduction loss but increases the turn-off time. This unavoidable trade-off between turn-off speed and device losses can be relaxed if the device is operated in a manner in which the current gain is degraded during turn-off period but not during the rest of the cycle of operation. This can be done by applying a negative pulse to the gate during the turn-off time period. Devices designed for good performance in this operating mode are called gate-assisted turn-off thyristors or GATT's.

Gate-assisted turn-off thyristors have been produced by several groups[2,3,4,5] during the last few years. The name is given to the method for turning off a thyristor with the usual commutation of the anode current but with the addition of a negative pulse applied to the gate during the time when forward anode voltage is being reapplied. This negative gate pulse decreases the turn-off time; that is, it allows one to reapply the forward voltage earlier without refiring the thyristor. (GATT's must not be confused with devices usually called gate-turn-off thyristors (GTO's) or gate-controlled switches (GCS's), that can be turned off with a gate signal without commutating the anode current.)

GATT DEVELOPMENT

The early devices were designed to have digitated cathode geometries without dynamic gating or cathode shunting. Shunting was not used because it was believed that the effect of the gate-assist pulse was to sweep out excess carriers and that the inclusion of cathode shunts would only add parasitic gate current. Dynamic gating was not used, because without shunts to direct the current through well defined resistance paths, dynamic

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gating can pose difficult problems both in the design and manufacturability of the device. Furthermore, the usual construction of a dynamic gate interposes a high resistance between the main cathode and the gate so that the effect of negative pulses on the gate is severely reduced. Further, the voltage drops developed in this resistance can avalanche the auxiliary cathode junction and cause locallized heating and degradation of the device.

Unfortunately, a digitated cathode without gate amplification requires high gate currents (~ 20A) to turn the device on with low switching losses. In addition, there are two other important weaknesses in GATT's with unshunted cathodes. First the dV/dt capability is very low unless the gate assist bias is maintained continually. Second, if the device conducts anode current and it fails to turn off while there is gate assist bias present the high current is crowded to the middle of the unshunted emitter fingers and the device can fail in a mode very similar to that of transistors and gate turn-off thyristors (GTO's).

PHYSICS OF GATE-ASSISTED TURN-OFF

With these problems in mind, an effort was undertaken to develop a more complete understanding of the physics of gate-assisted turn-off. The effort resulted in the finding that the effect of the gate-assist bias is not primarily to sweep out excess charge but to prevent a sufficient forward bias from developing on the cathode junction to cause injection and a sufficient current gain to create regenerative thyristor action. The details of this are given in Reference 6. Summarizing the findings on which this understanding is based:

1. Gate-assist bias is only effective if it is present during the application of reapplied forward voltage.

2. Gate-assist current that flows before the application of reapplied forward voltage has little effect on either the turn-off time or the displacement current induced by the reapplied forward voltage.

3. An increase in the lateral resistance in the base under the cathode makes a given gate-assist current more effective for decreasing the turn-off time.

A NEW GATT DESIGN

Based on this new understanding, we developed a GATT with the following design features:

1. The cathode was digitated. This is necessary both for good, fast, low loss turn-on and for effective gate-assisted turn-off behavior.

2. The cathode was shunted. This provides for a high dV/dt capability whether there is a gate-assist bias present or not. Further, it appears to eliminate failure due to current crowding of the type that causes transistor and GTO failure. In addition, shunts direct the current paths in such a manner that the effect of the gate-assist bias is more reliable, and requires a lower drive voltage. Shunts make the device more tolerant of process induced nonuniformities and thereby make the device more manufacturable.

3. A bypass diode was necessary to combine the advantages of dynamic gating and gate assisted turn-off. There are several ways of incorporating bypass diodes. The package can be modified to contact the floating gate with a diode. Our most successful way to date was to solder the diode directly to the floating gate with a lead connecting the diode cathode to the main gate. The most reliable way is to build the diode into the thyristor itself as shown in Figure 1. In the sectional cut from G_L to A the structure is simply that of the familiar amplifying gate. This structure exists in two opposing quadrants of the central region. In the other two quadrants the structure is as shown in the section G_L to B. When forward bias is applied to the gate, it causes current to flow through the auxiliary cathode and little current flows through the high resistance under the bypass diode. When a reverse (gate-assist) bias is applied to the gate, most of the current flows through the bypass diode and little through the high resistance under the auxiliary cathode. To prevent electrons emitted by the bypass diode from firing the thyristor, the carrier lifetime is decreased in this local area by masked electron irradiation. The cathode geometry can also be shaped to decrease the

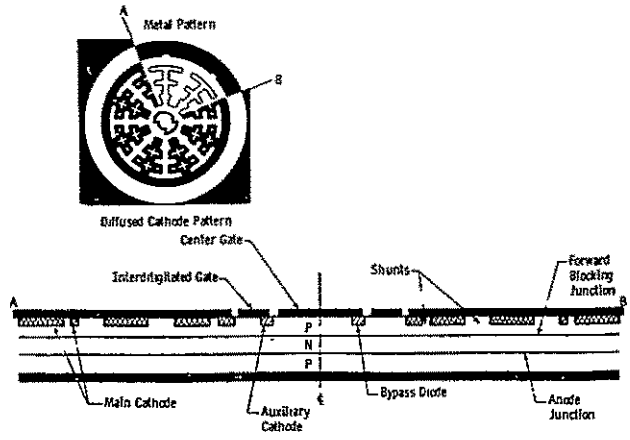

Fig. 1 Thyristor structure with an integrated bypass diode.

emitter efficiency and to widen the p-base width under the bypass diode so that the current through the bypass diode produces few electrons that reach the central depletion layer. Etch pits between the ends of the auxiliary cathodes and the ends of the bypass diode diffusion regions substantially decrease the flow of useless current through the gaps between these n-regions when the device is to be turned on. Another version of the integrated bypass diode is described in Reference 5.

4. The effect[7] of the diffusion profiles was studied to see how the effectiveness of the gate-assist current is influenced by profile changes. In this area, it was found that a change in the sheet resistivity in the p-base has opposite effects on the effectiveness of gate assist current for shunted and unshunted GATT's.

5. Electron irradiation was used to control the carrier lifetime. The ability, with electron irradiation, to easily and quickly measure the same devices with different stepped doses of irradiation provides a valuable capability for studying how to optimize the diffusion profiles and for tailoring a device to a specific application.

PERFORMANCE ACHIEVED

GATT's have been constructed with the geometry shown in Figure 2 and the typical characteristics shown in Table 1 have been demonstrated. Measured turn-off times were found to depend on the magnitude of the gate-assist current as shown in Figure 3. Here the various curves represent different levels of carrier lifetime which were produced by various levels of electron irradiation.[7] Figure 4 shows the trade-off between the turn-off time and the forward drop which was varied by stepping the dose of electron irradiation used to control the lifetime.

TABLE 1

Measured Characteristics

Forward Blocking Voltage	1000 V
Reverse Blocking Voltage	1000 V
Gate Trigger Current	< 200 mA
Gate Trigger Voltage	< 2 V
Latching Current	< 1.0 A
Holding Current	< 200 mA
dV/dt	> 1000 V/μs

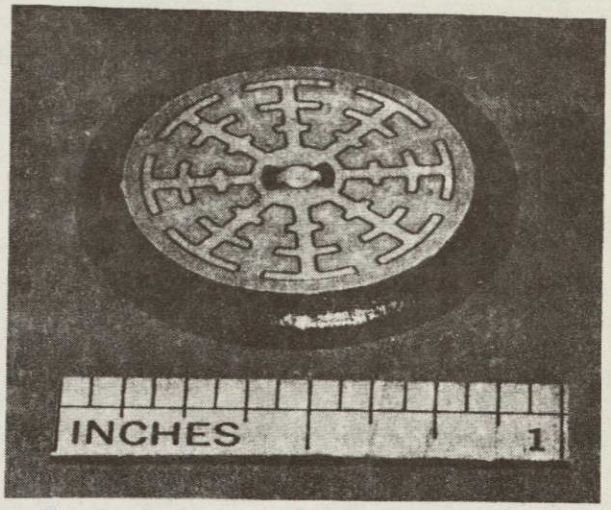

Fig. 2 Photograph of a gate-assisted turn-off thyristor having both cathode shunts and a dynamic gate.

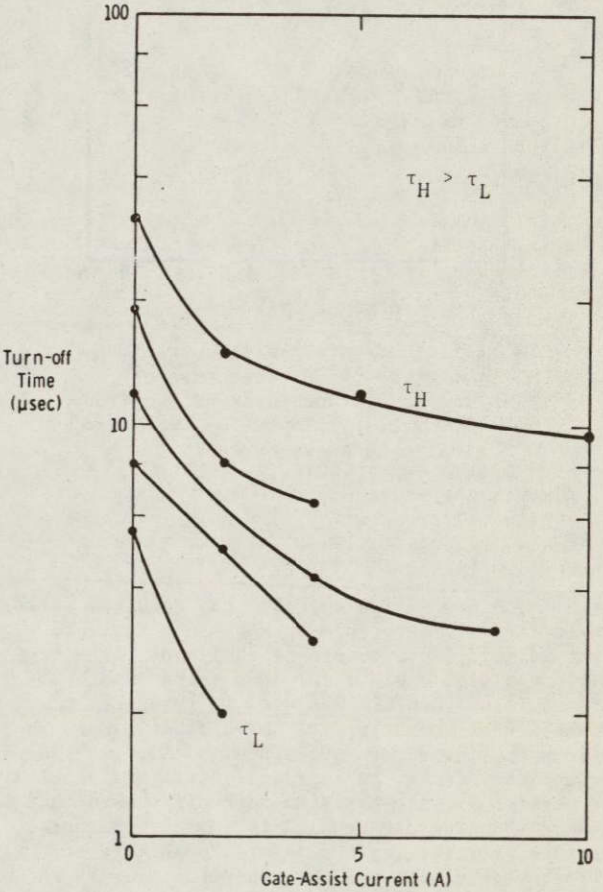

Fig. 3 Dependence of measured turn-off time on gate-assist current. (Conditions: 100°C, 25 A/μs, 400 V/μs.) Each curve represents a device having a different carrier lifetime level created by different doses of high-energy electron irradiation.

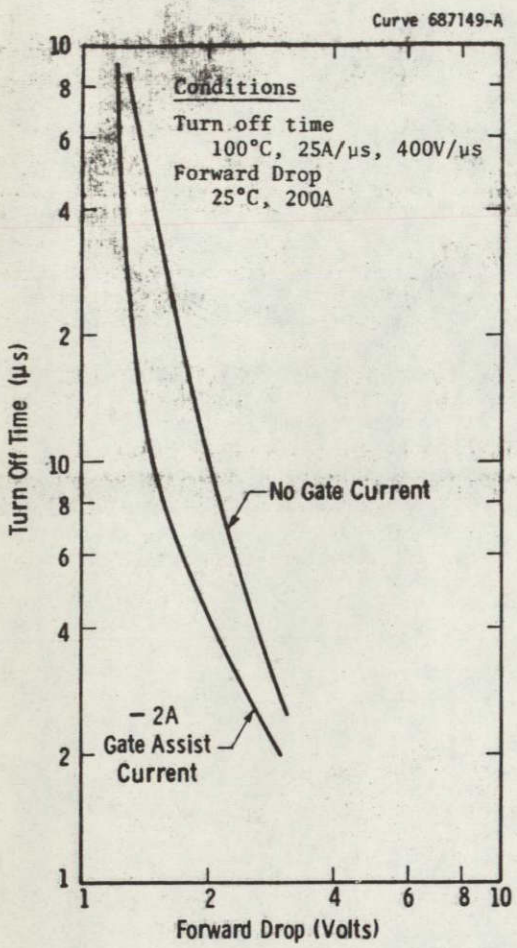

Fig. 4 Effect of gate-assist current on the trade-off between turn-off time and forward drop of a GATT. The carrier lifetime was varied along each curve by means of electron irradiation.

CONCLUSION

A new design approach has resulted in improved thyristors for use by NASA in efficient, light weight power processing equipment for electric propulsion engines for deep space missions. Gate-assisted turn-off was used to relax the stringency of the otherwise unavoidable compromise between thyristor turn-off speed and turn-on and conduction losses. An improved understanding of the physics of gate-assisted turn-off showed that cathode shunting can be used to improve the performance, reliability and manufacturability of GATT's. Techniques are described that permit the combination of both dynamic gating and gate-assisted turn-off in single devices. The ability to easily vary the gate-assist current level and the carrier lifetime level extends greatly ones ability to find optimum diffusion profiles and to tailor devices for specific applications.

ACKNOWLEDGEMENTS

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(6) E. S. Schlegel, "Gate-Assisted Turn-Off Thyristors," IEEE Trans. Electron Devices, Vol. ED-23, 888-892 (1976).

(7) E. S. Schlegel, "A Technique for Optimizing the Design of Power Semiconductor Devices," IEEE Trans. Electron Devices," Vol. ED-23, 924-927 (1976).

into reverse recovery faster there is less time for carriers to recombine and therefore more carriers remain to contribute to the forward recovery and excess leakage currents.

Effect of dV/dt

Figure 8 shows the effect of dV/dt. An increasing dV/dt is shown to increase both the forward recovery and the excess leakage currents. The increase in forward recovery current with increasing dV/dt is primarily due to the fact that a slower rising voltage. sweeps out more charge before the device becomes capable of supporting forward voltage. Therefore, forward recovery occurs at a lower anode voltage and current for a lower dV/dt.

Effect of Slice Diameter

Figures 5b and 5c show that for devices having the same turn-off time the forward recovery current is fairly independent of slice diameter.

Effect of Turn-Off Time

Figures 5a and 5b show that the forward recovery current is smaller, for a given interval between $I_A = 0$ to the onset of the dV/dt ramp, the lower the device-limited turn-off time.

Effect of Reapplied Voltage Level

The forward recovery current has ended before the dV/dt ramp has ended and is, therefore, independent of the reapplied forward voltage level. The excess leakage current tail shows no change in slope when the dV/dt ramp ends and it can be inferred, therefore, that it is not sensitive to differences in the reapplied forward voltage level.

Effect of Reverse Voltage

Neither the peak or excess leakage currents were found to depend on variations in the reverse voltage level.

Effects of Gate Assist Current Variables

The level of gate assist current had little effect on the peak or excess leakage currents. The gate assist pulse affects the forward recovery current only when it is present during the dV/dt ramp. A gate assist current before the dV/dt ramp has no significant effect.

Model

The physical model of a thyristor in its turn-off sequence can be described in simple terms as follows.

Starting with a simple rectifier, it is well understood that in its conducting state the injection of charge carriers produces an excess charge plasma on the low conductivity side of the junction. When a reverse voltage is applied, the rectifier remains conductive because of this excess mobile charge until it is removed by recombination and/or sweep out. This is simple reverse recovery.

Turning to a thyristor, the phenomenon described above occurs at the reverse blocking junction (the anode junction) when the thyristor is switched from the forward conducting to the reverse blocking state.

Consider now some differences between a rectifier and a thyristor. In the rectifier in the reverse conducting state there are no barriers to the flow of excess carriers from the device. On the other hand in the thyristor, when the reverse blocking junction blocks current, current continuity must be maintained and the current through the middle junction must be small. Then, because the injection efficiency of this middle junction is low for electrons leaving the n-base, the excess electrons are blocked in the n-base and cannot flow out. They must reach their equilibrium density mainly by recombination. To the extent that these blocked carriers are excess minority carriers, they contribute to an excess leakage current and are the cause of the tail current when the junction blocks voltage.

If a forward voltage is applied to the thyristor within a few microseconds after reverse recovery has occurred, much of this blocked charge must be swept out before the forward blocking junction can block. This produces a forward recovery current quite similar in nature to the reverse recovery current.

For thyristors with turn-off times of tens of microseconds, this blocked charge mostly recombines in the base of the thyristor and contributes little to the forward recovery current and loss. As the turn-off times reach levels below ten microseconds, this current and loss become more and more significant.

The data in Figure 5 show that the effectiveness of gate assist current for decreasing the turn-off time is not to decrease the forward recovery current but it instead raises the level of forward recovery current that fires the thyristor.

Just as the carriers are not all swept out by the reverse recovery current, the presence of the excess leakage current after the forward recovery shows that there are still blocked excess carriers left in the n-base after forward recovery.

The effects of variations in device design can be broadly understood to fall into three categories:

1. The rate of decay of the carriers responsible for the forward recovery, and its excess leakage current, is inversely proportional to the carrier lifetime.

2. The p-base sheet resistivity and the cathode and shunt pattern design determine when the dV/dt displacement current will forward bias the cathode.

3. The design of the impurity density distribution, layer thicknesses, carrier lifetimes, and emitter shunting determines the degree to which the emitter must be forward biased to fire the thyristor.

GATE ASSISTED TURN-OFF THYRISTOR

FAST VOLTAGE BLOCKING RECOVERY BY APPLYING NEGATIVE GATE CURRENT AT ANODE CURRENT ZERO

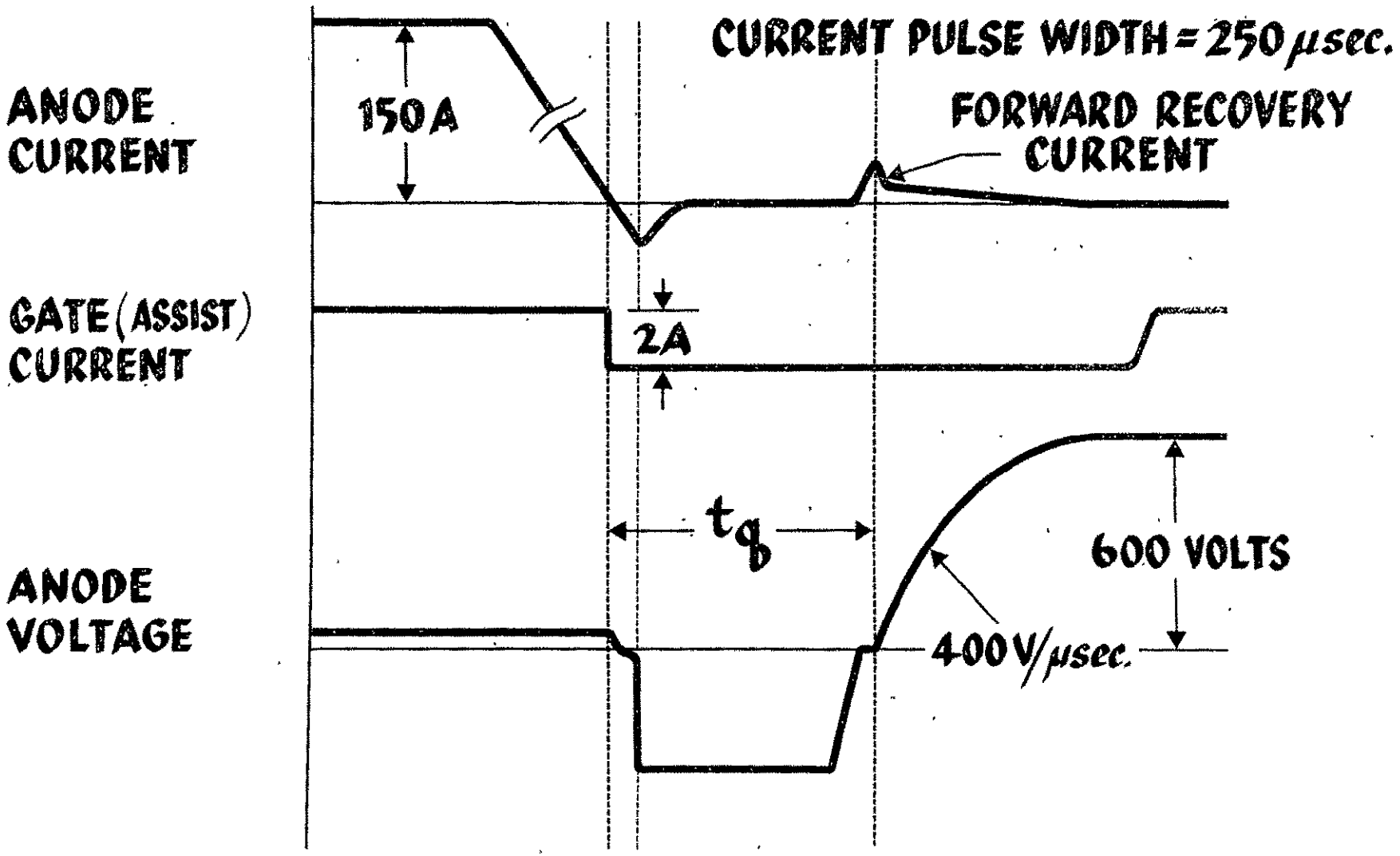


Fig. 1

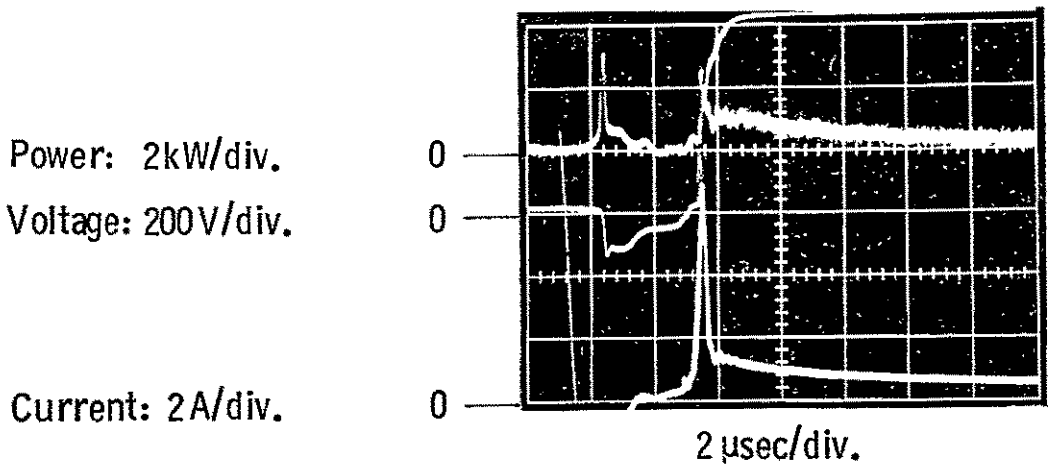
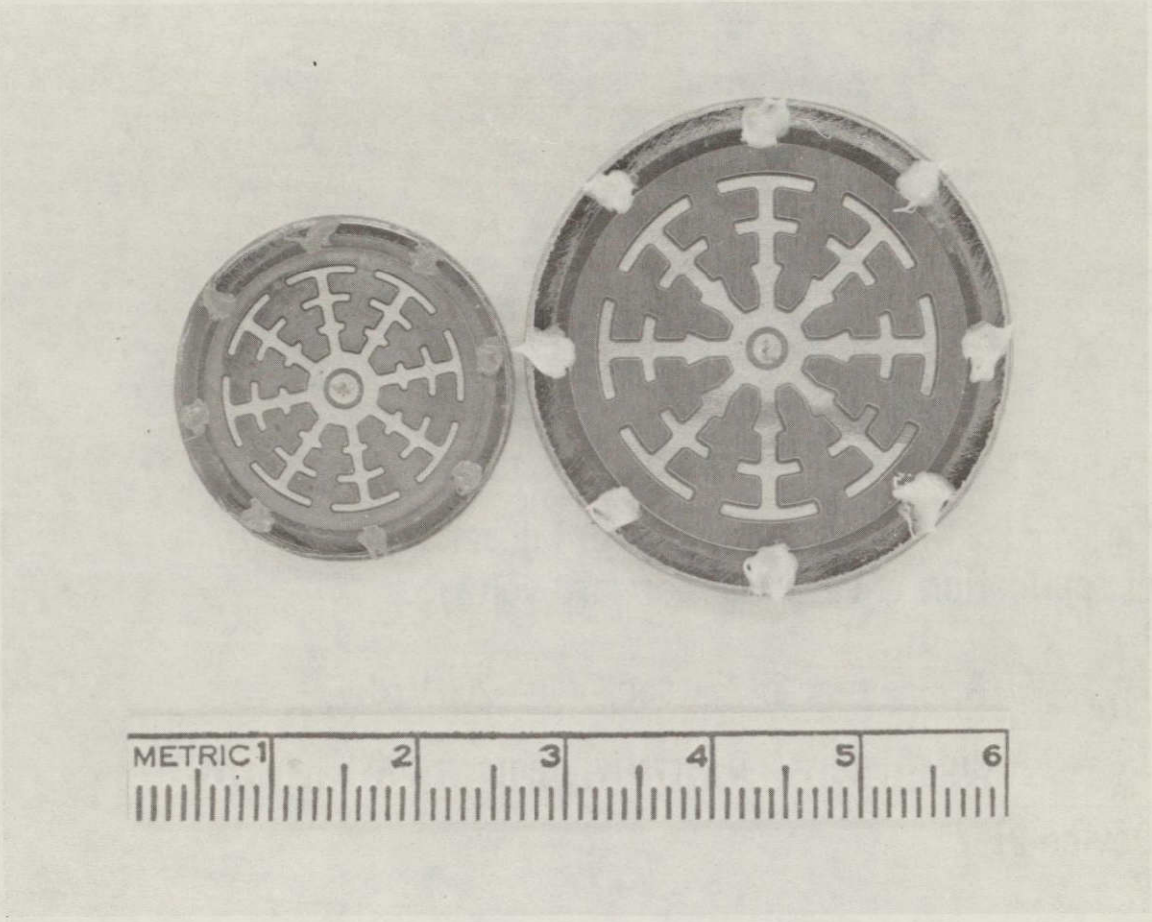


Fig. 2— Anode current, voltage and power demonstrating relative energy losses for reverse and forward recovery. $I_{TM} = 150$ A, $\frac{di_R}{dt} = -25$ A/μsec, 100°C, device 21-19



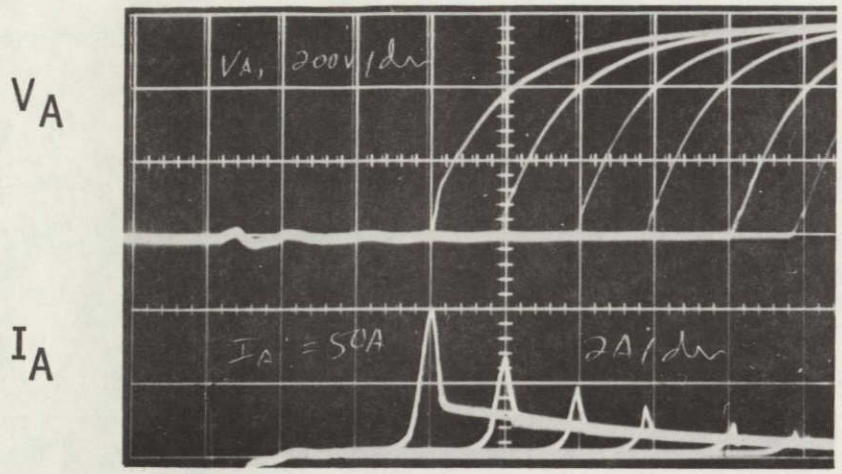


Fig. 4—Forward recovery current dependence on time of application of reapplied forward voltage.

$I_{TM} = 50\,A$, $\frac{di_R}{dt} = -25\,A/\mu sec$, $V_A = 200\,V/div$,
$I_A = 2\,A/div$, time = $2\,\mu sec/div$, temp = 100°C,
Device 21-7

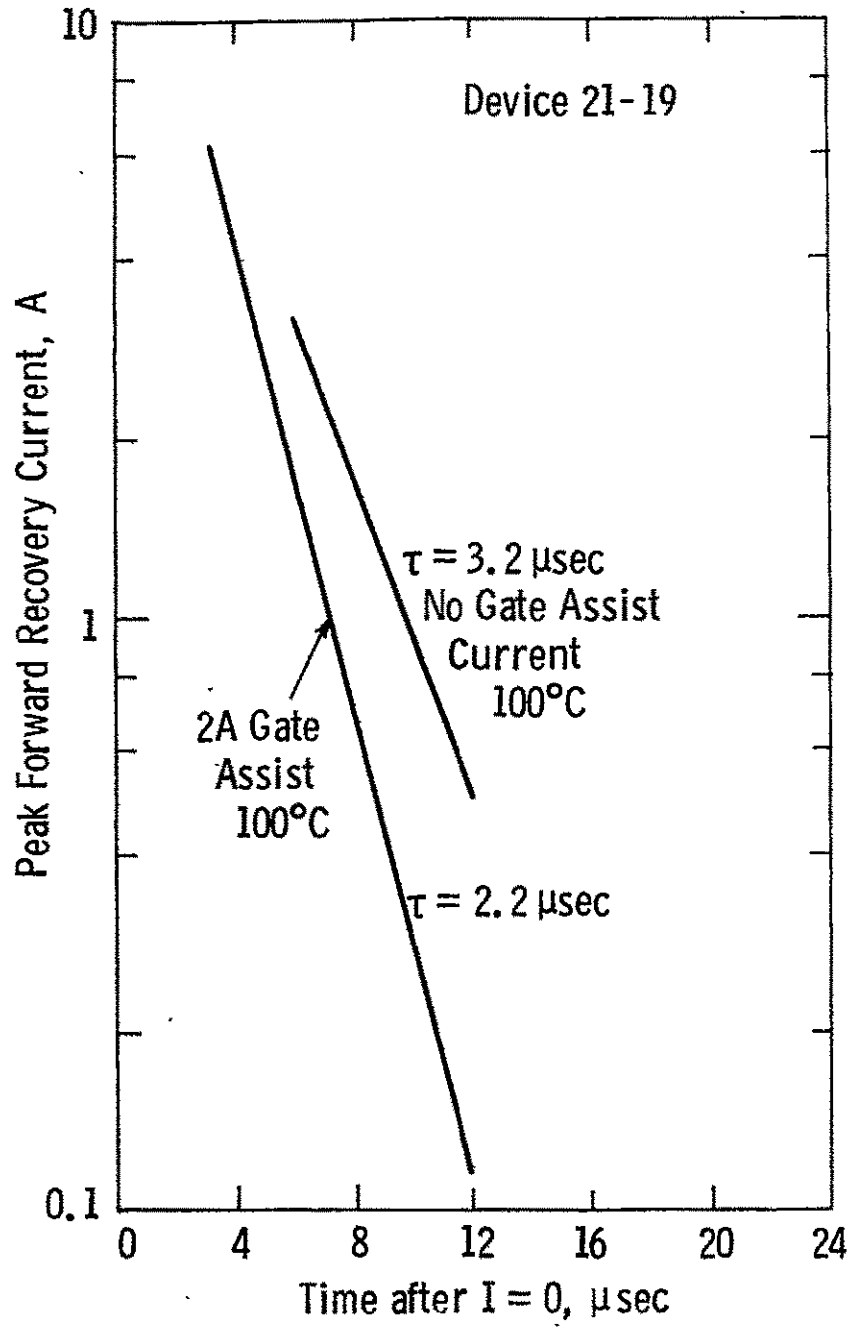

10
1
0.1
Device 21-19
τ = 3.2 μsec
No Gate Assist
Current
100°C
2A Gate
Assist
100°C
τ = 2.2 μsec
Peak Forward Recovery Current, A
0
4
8
12
16
20
24
Time after I = 0, μsec

Fig. 5b

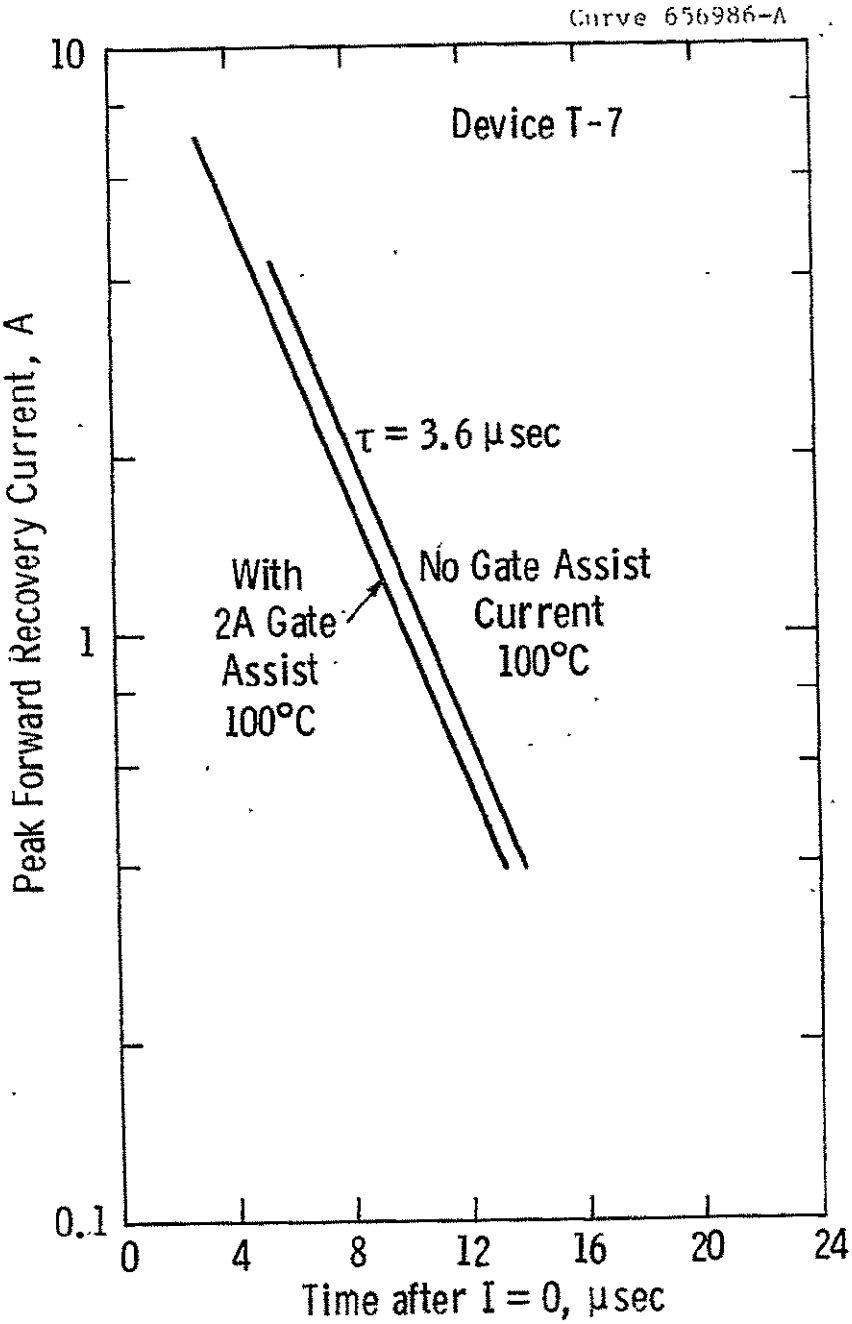


Fig. 5c

Fig. 5a-5b-5c—Forward recovery current dependence on time of application of reapplied voltage with and without gate assist current. I_{TM}=150 A, $\frac{di_R}{dt}$ = −25 A/μsec $\frac{dv}{dt}$ = 400 v/μsec

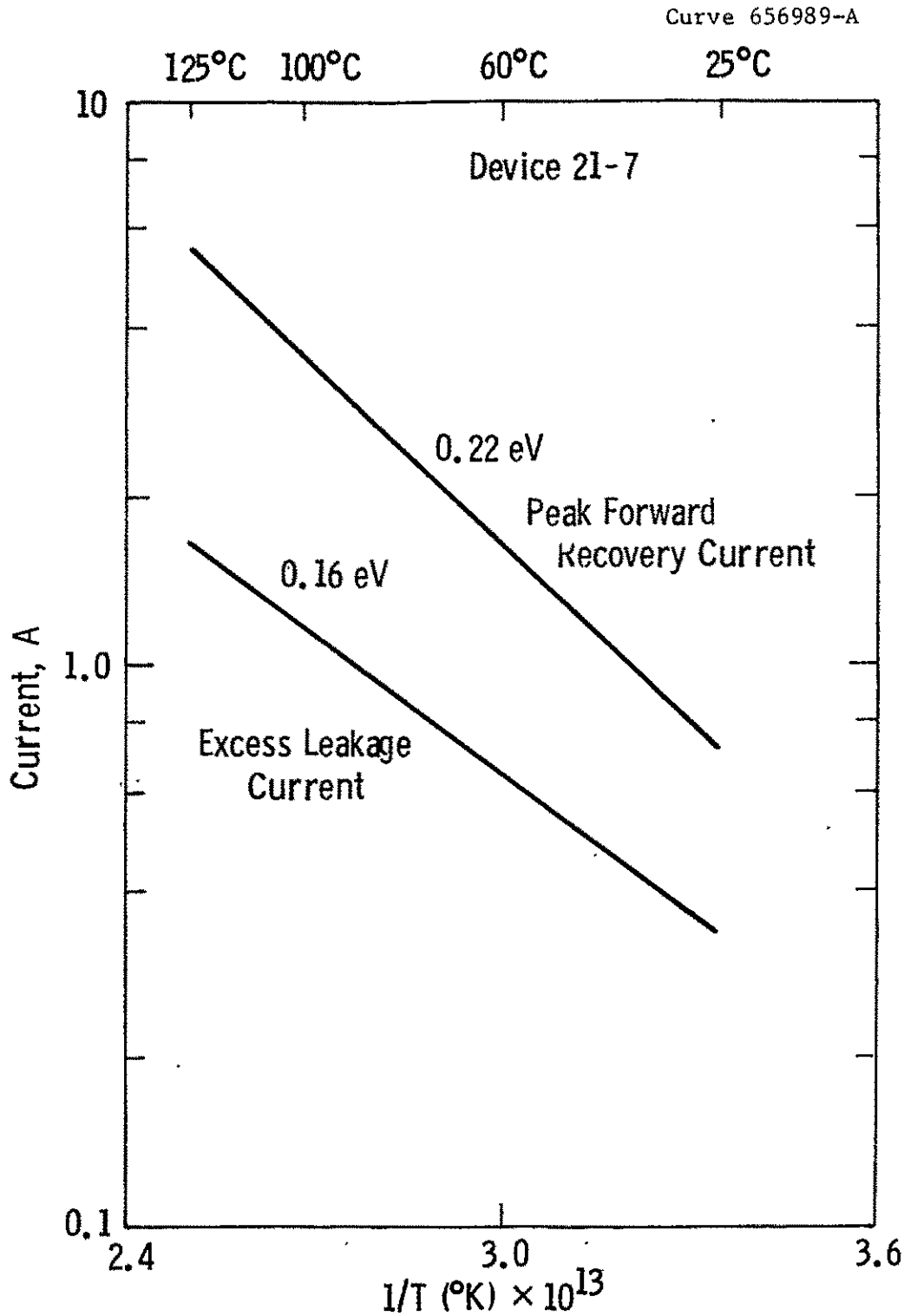


Fig. 6—Effect of temperature on forward recovery current and its excess leakage current, $I_{TM} = 150\,A$, $\frac{dI_R}{dt} = -25\,A/\mu sec$ $\frac{dv}{dt} = 400\,V/\mu sec$, $t_q = 8\,\mu sec$

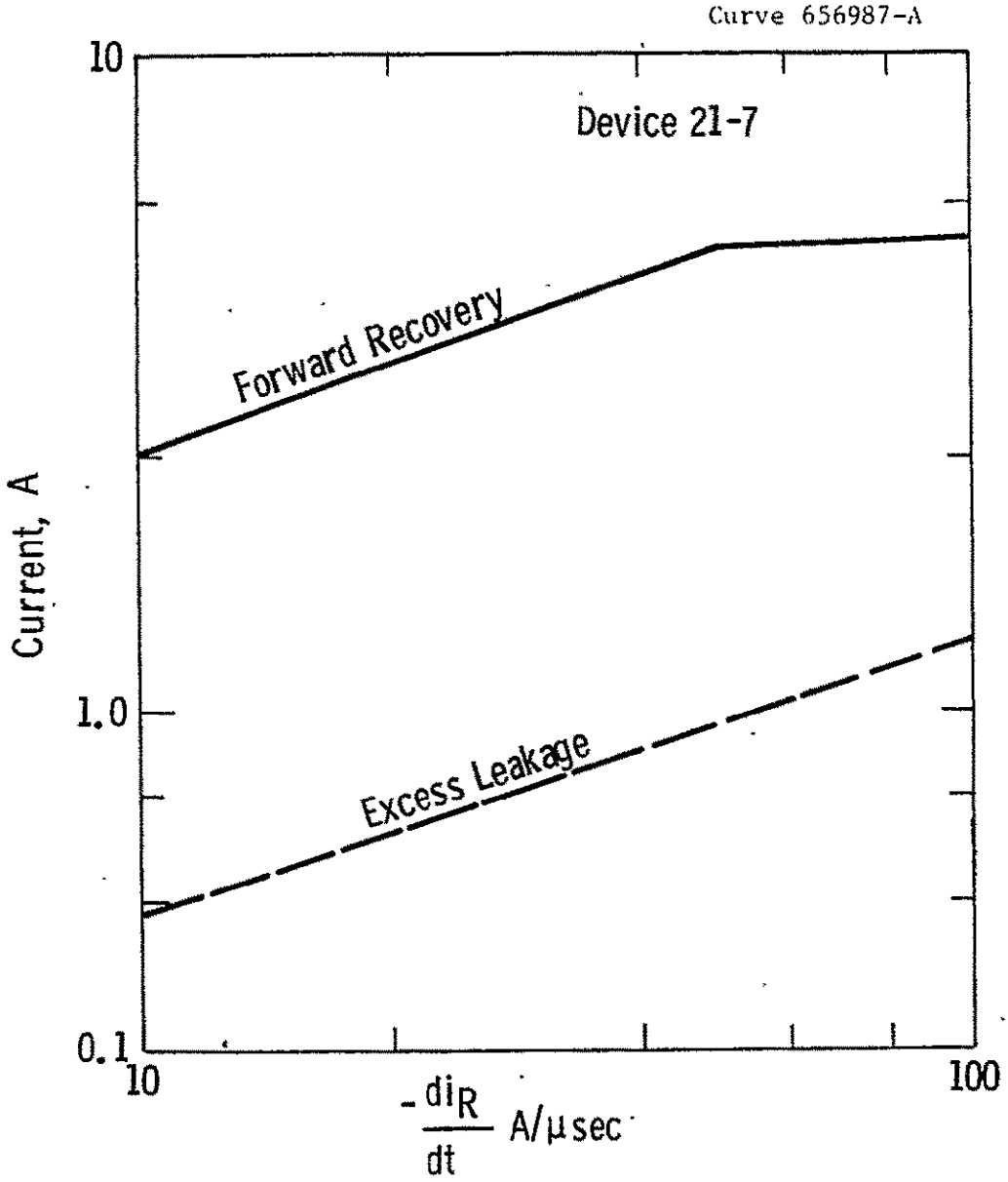


Fig. 7—Effect of $\frac{-di_R}{dt}$ on forward recovery current and its excess leakage currents $I_{TM} = 150$ A,

$\frac{dv}{dt} = 400$ V/μsec, $t_q = 8$ μsec, 100°C

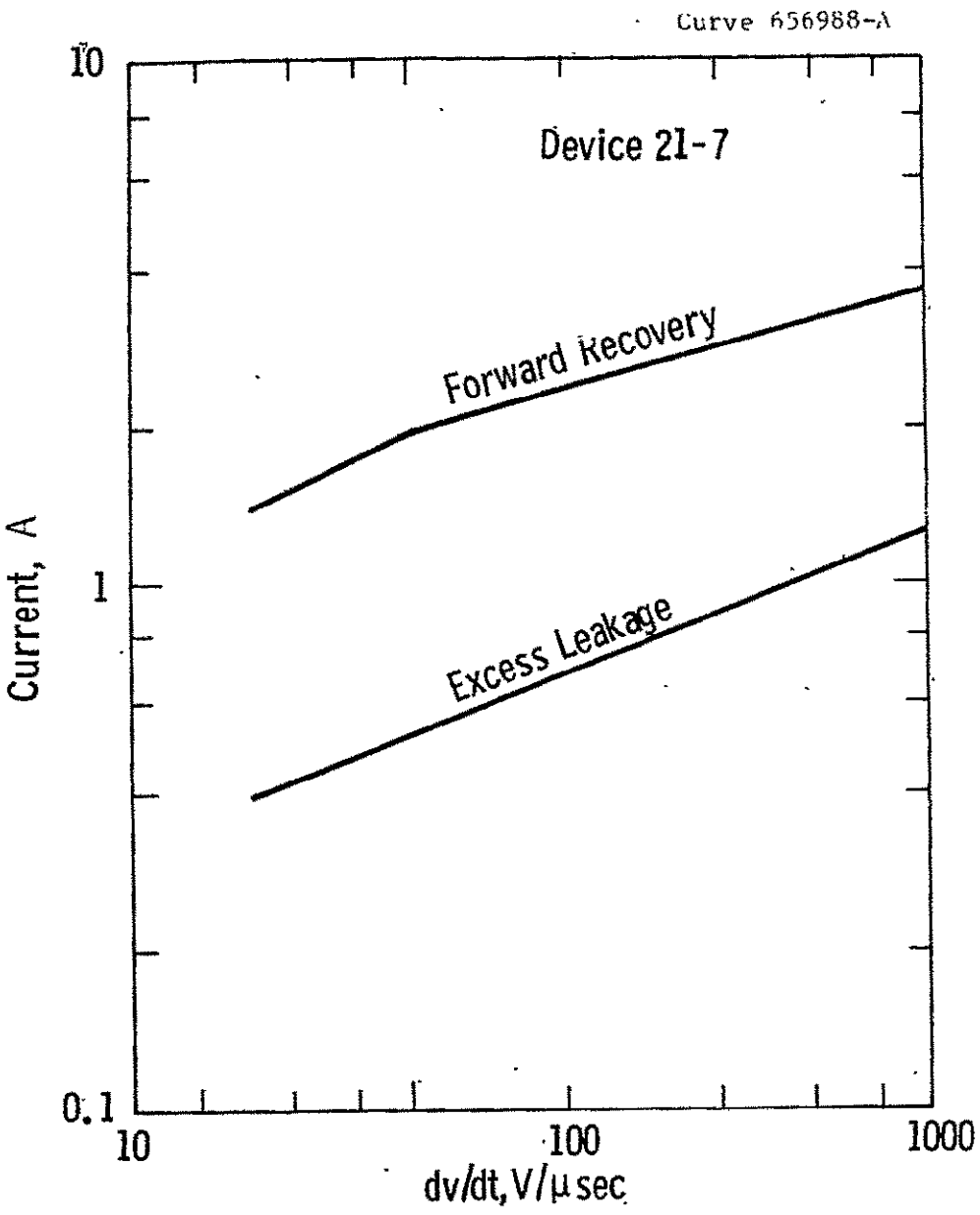


Fig. 8—Effect of dv/dt on forward recovery and excess leakage currents. $I_{TM} = 150$ A, $\frac{di_R}{dt} = -25$ A/μsec, $t_q = 8$ μsec 100°C