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OPTICAL SCANNING TESTS OF COMPLEX CMOS MICROCIRCUITS

FINAL REPORT – MAY 1976 THROUGH APRIL 1977

M. E. LEVY
J. J. ERICKSON

OCTOBER 1977

Prepared under Contract No. NAS8-31239 by

Advanced Technology Laboratory
Technology Support Division

AEROSPACE GROUPS

HUGHES
HUGHES AIRCRAFT COMPANY
CULVER CITY, CALIFORNIA

for

GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
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1.0 FOREWORD

This report is a summary of work performed on NASA Contract NAS8-31239 during the period of 1 May 1976 to 30 April 1977. The investigation was conducted for the George C. Marshall Space Flight Center, Huntsville, Alabama. The Contracting Officer's Technical Representatives were Mr. William R. Barlow and Mr. Leon Hamiter.

The work was performed within the Advanced Technology Laboratory of the Technology Support Division of Hughes Aircraft Company. Dr. Miguel E. Levy was principal investigator and program manager. Mr. James J. Erickson contributed significantly to the experimental work. Mr. Ronald V. De Long's help with equipment design and maintenance was also a valuable contribution.

A substantial portion of the work reported here was presented at the 1977 Reliability Physics Symposium in Las Vegas; an account of the work will appear in the printed Symposium Proceedings, to be published by IEEE Press.

2.0 SUMMARY

The work described in this report was the second phase of a project to develop and evaluate a new nondestructive inspection and test method for microcircuits. The basis of the new method is the use of a raster-scanned optical stimulus in combination with special electrical test procedures. The raster-scanned optical stimulus is provided by an Optical Spot Scanner, an instrument that combines a scanning optical microscope with electronic instrumentation to process and display the electrical photoresponse signal induced in a Device Under Test (DUT).

The Optical Spot Scanner itself is not a novel idea: Its ability to detect and image flaws in semiconductor devices and to check the static logic states of internal stages of microcircuits is well known. The overall purpose of this project was to devise methods by which an Optical Spot Scanner could be used for 100% screening inspection of microcircuits. Because of the time necessary to scan a raster frame and because of the number of data points (picture elements) contained in a photoresponse image of a DUT, an important prerequisite for this application is that the DUT must be adequately characterized by a single photoresponse image for the accept/reject decision. A method by which this special photoresponse image can be generated was developed in the first phase of this project. The new method was named the State Superposition Technique because of the way in which it generates the photoresponse image. The work done in the first phase was described in the final report "Imaging LSI Microcircuits with Optical Spot Scanners," dated January 1976.

The work in this second phase involved the application of the State Superposition Technique to CMOS microcircuits that had been subjected to a 1000 hour life-test at 125°C. Twenty specimens of each of two part types were examined. In each set of twenty devices there was a group of ten failed specimens and a control group of ten good specimens. The failure criteria were the results of various current consumption and leakage tests. With one possible exception, all the test devices were functional.

For various reasons that made this approach more productive, emphasis in the laboratory work was placed on one of the two part types. In addition to a survey of State Superposition photoresponse images under conditions of normal operation, experiments were planned and carried out on this part type to detect effects whose presence was implied by results of electrical tests. Tests at high clock frequencies showed the Optical Spot Scanner's ability to localize the stages that malfunctioned at high frequency. These tests also disclosed the unexpected activation of parasitic bipolar structures that amplified the optically injected photocurrents. Experiments were also done to measure a length parameter describing the dependence of a junction's photocurrent on the distance from the junction to the focused optical spot. While not entirely conclusive, the experimental results strongly suggest that large values of the length parameter are a necessary condition for low leakage currents in the test specimens.

The laboratory work on the second part type was restricted to State Superposition image surveys at two values of power supply voltage. At the lower voltage the test specimens were operated near their upper frequency limits. A fairly consistent pattern of bipolar parasitics was detected in all the specimens. The parasitics appeared to involve diffused conductors and diodes, and also p-channel FET's in transmission gates. Some major differences between photoresponse images for different test specimens were noted, but they could not be readily correlated to the electrical test data for these specimens.

In brief, the results of this program showed that the Optical Spot Scanner operated in combination with the State Superposition Technique can detect effects in microcircuits that are correlated with their electrical

behavior. Since the effects are localized on particular portions of the microcircuit chips, the resulting information may be of value not only for screening inspection but also for engineering studies of CMOS microcircuits.

3.0 INTRODUCTION

In recent years the growing complexity and density of microcircuits has greatly increased the difficulty of inspecting and testing them. Since the reliability requirements of space and airborne systems can be met only by 100 percent inspection and testing procedures, more efficient and effective testing and inspection methods are necessary. One prospective technique for fulfilling this need is inspection with an Optical Spot Scanner.

The Optical Spot Scanner (OSS) is an instrument that scans a focused spot of light in a raster pattern over a specimen. The electrical photoresponse signal and the reflected light signal are displayed on CRT displays. In fact, the OSS can be thought of as a Scanning Optical Microscope that is closely analogous to the Scanning Electron Microscope (SEM) operated in the Electron Beam Induced Current (EBIC) and secondary electron emission modes. However, unlike the SEM, the OSS is completely nondestructive, does not require a vacuum chamber for the test specimen, and can provide a significantly higher beam-induced signal level (by several orders of magnitude, if necessary). Research experience with the optical scanner has already established that it can detect certain important types of flaws in simple semiconductor devices. Some of these flaws cannot be detected by visual inspection or by conventional electrical tests. In microcircuits, the OSS generates a photoresponse pattern or image that depends on the circuit's digital state. In effect, the OSS can thereby monitor directly the internal operation of microcircuits. Because of the buffering effect of each succeeding stage on the preceding stages of a digital microcircuit, direct monitoring of the internal operation of the circuit cannot be done by conventional electrical measurements at the external terminals.

These potential capabilities - to nondestructively monitor the internal operation of digital microcircuits and to detect and localize otherwise undetectable flaws - would make the OSS a very effective inspection instrument for 100 percent screening inspection and also for engineering studies of microcircuits. Unfortunately, its use is made difficult by the complexity of the digital microcircuits themselves. For screening inspection it must be assumed that the photoresponse image data will be converted to digital form, processed, and compared to a reference image to make the accept/reject decision. The large amount of data contained in a single image can be handled rapidly enough by a modern computer, but a screening procedure that required scanning and processing several images per test device would not be practical. The use of the OSS for screening inspection therefore requires a method for generating a single photoresponse image that adequately characterizes the Device Under Test (DUT). This image then could be used as a "characteristic signature" for making the accept/reject decision. One obvious requirement for the image is that it should contain images of all photoresponsive circuit elements in it.

The difficulties with using a conventionally generated photoresponse image can be stated in several, essentially equivalent ways. One version is as follows: when the photoresponse image of a DUT is generated, the photoresponse signals from some of the circuit elements may not be accessible at the device's external terminals. The photoresponses may be shorted out by conductive paths in parallel with the circuit elements in question, or they may be prevented from reaching the external terminals by blocking series elements. Whatever the reason, these circuit elements will appear dark in the photoresponse image.

The work in the first phase of this contract addressed the problem of generating the required photoresponse image on the basis of the above statement of the problem. One promising approach was selected for further development after several possibilities had been investigated. The successful implementation of a method based on this approach was mainly the result of an improved understanding of the problem. As stated above, the difficulty is that the photoresponses from some of the circuit elements are externally

inaccessible, so these circuit elements do not appear in the photoresponse image. However, which circuit elements appear and which do not is determined by the DUT's digital state. Indeed, it is the pattern of light and dark circuit elements in the photoresponse image that characterizes the DUT's digital state. By analyzing this pattern it is possible to determine the state of internal circuit stages that are not accessible to measurement via the device's external terminals. The difficulty of imaging all circuit elements in one photoresponse image is not that the photoresponses from some elements are inaccessible, but that the DUT is being examined in a single digital state. It can be assumed that if the set of photoresponse images of all possible states of the DUT were examined, any given circuit element would appear at least once in the set. In fact, for a complex microcircuit, a set of images containing each circuit element in at least one image would be a small subset of the set of all possible images. Disregarding the problems of implementation, one possible approach for generating the required "characteristic signature" image is to form an appropriately weighted superposition or average of a subset of images having each circuit element in at least one image. The method that was developed in the first phase of this work is an implementation of this approach. Because of the way in which it generates the "characteristic signature" image, the new method was named the State Superposition Technique.

Following a demonstration of the State Superposition Technique in the first phase of this effort, the work reported here was undertaken in order to investigate the effectiveness of the new technique in detecting flaws in microcircuit specimens. Since the initial demonstration had shown that the Optical Spot Scanner was particularly well suited to CMOS microcircuit inspection, this second phase consisted of a project to examine good and failed CMOS microcircuits with the State Superposition Technique and to correlate the photoresponse images with the electrical behavior. Twenty specimens of each of two CMOS part types were supplied by NASA MSFC. The specimens had undergone a 1000 hour 125°C life-test; after which they had been tested according to tentative MIL-M-38510 specifications for the part types. The twenty specimens of each type included a group of ten reject

microcircuits that had failed power supply current tests and a control group of ten good microcircuits.

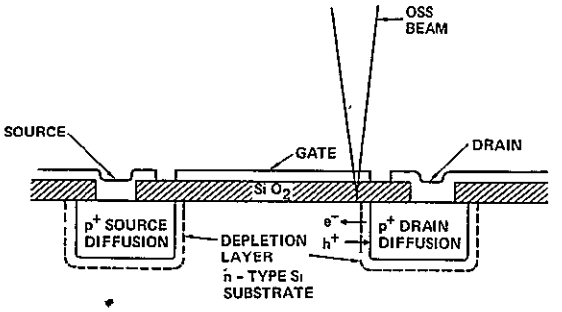
Briefly, the tasks for this program consisted of developing the electrical test program for use with each part type for the State Superposition Technique, hermeticity tests, internal visual inspection of the uncapped test specimens, Optical Spot Scanner examinations, and interpretation of the data. The two microcircuit types examined were the CD4028A BCD-to-decimal decoder and the CD4034A eight stage bus register.

Although the State Superposition Technique was described in the final report of the first phase, it is reviewed in this section in the light of added experience. The mechanism of photoresponse image generation for a CMOS inverter is also included for completeness. The improved optical scanner used for this work, which significantly outperforms the one used in the first phase, is also described. The laboratory work, results, and conclusions are covered in subsequent sections.

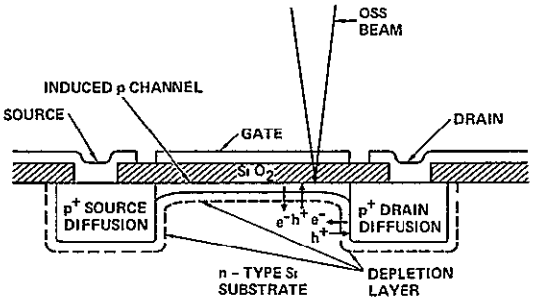
3.1 PHOTORESPONSE IMAGE FORMATION ANALYSIS FOR A CMOS INVERTER

CMOS microcircuits are conventionally made with enhancement mode, p-channel and n-channel MOSFET's. The p-channel transistors are fabricated on the n-type substrate; the n-channel transistors are fabricated on p-wells diffused into the substrate. The photoresponse from these elements is generated in the space-charge regions associated with diffused and field-induced p-n junctions. During normal circuit operation, these junctions are not forward biased, and the photoresponse can be qualitatively understood in terms of photodiode action. The excess hole-electron pairs generated at or near the junction's space-charge region (the depletion layer) are separated in a direction that tends to forward-bias the junction: holes drift to the p side of the junction, electrons to the n side.

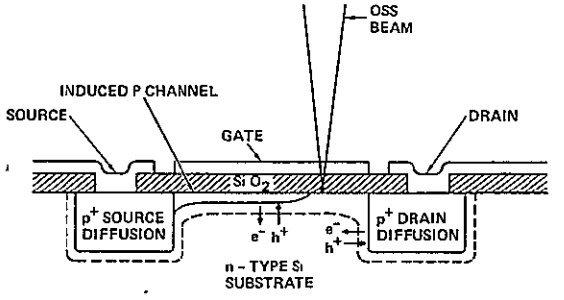
Three operating points of a MOSFET are of interest: the "off" state, the "on" state in the nonsaturating region, and the "on" state in saturation or pinch-off. Figure 3-1a illustrates the "off" state of a p-channel MOSFET. The photoresponse arises from the source and drain diffusions only. Figure 3-1b illustrates the nonsaturated "on" state. The photoresponse is



a. "Off" state



b. Nonsaturated "on" state



c. Pinched-off "on" state

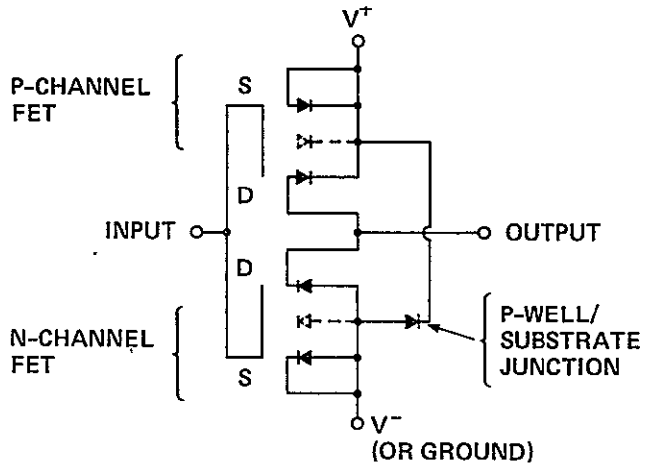
Figure 3-1. P-channel MOSFET.

generated by the field-induced junction as well as by the source and drain diffusions, all of which act together as a single, extended junction. The field-induced channel extends from the source to the drain and acts as a low impedance conduction path. Figure 3-1c illustrates the saturated or pinched-off "on" state. The source junction plus the field-induced junction now act as a single junction, which is separated by the depleted pinched-off region from the drain junction. The pinched-off channel acts as a high impedance conduction path. An n-channel MOSFET's behavior is similar with the photoresponse polarity reversed.

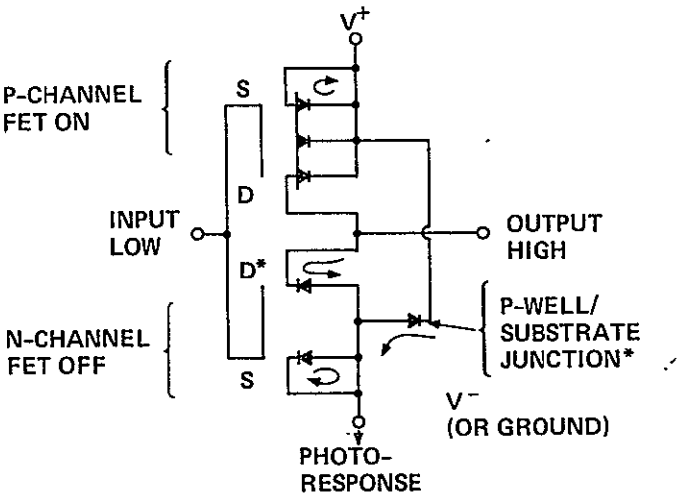
The manner in which individual MOSFET's photoresponses combine to form the photoresponse image of a digital circuit stage (such as inverter, gate, or flip-flop) depends on the particular interconnections between the various elements. The kinds of factors that enter into the analysis of any particular stage's image are well exemplified by the following interpretation of a CMOS inverter's image under various conditions.

Figure 3-2a shows the circuit diagram of a CMOS inverter with the diffused junctions and the field-induced junctions denoted explicitly by diode symbols. The field-induced junctions are depicted by dotted symbols, the diffused junctions by solid symbols. The sources of the p- and n-channel transistors are connected to the n-substrate and p-well respectively, which effectively places a short-circuit across the source junction.

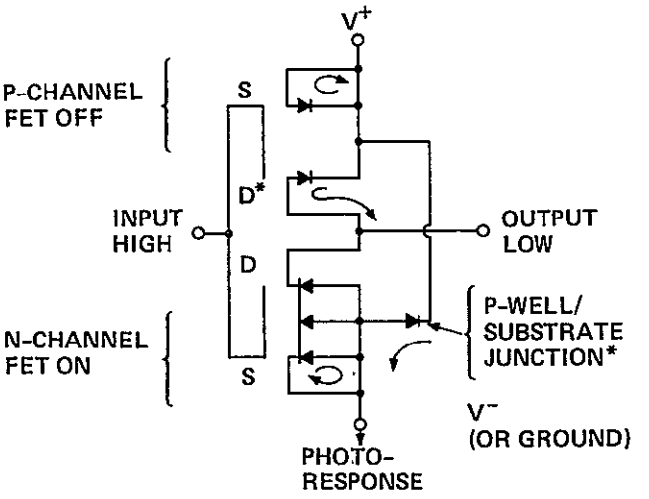
Figure 3-2b shows how photoresponse currents flow in a CMOS inverter operating normally with a low input ($\sim V^-$). The p-channel FET is in the nonsaturated "on" state, with the field-induced junction joining the source junction to the drain junction. (The field-induced junction is shown as a solid diode in this figure.) Because of the source-to-substrate connection, the photoresponse of the entire extended junction is shorted out, and the p-channel FET is dark in the photoresponse image of the inverter. The n-channel FET is "off." Its source photoresponse is also shorted out by the source/p-well connection. (In the figure, both of these shorted photoresponses are shown as circulating currents.) The drain's photoresponse is conducted to the V^+ and V^- terminals via the "on" FET and the p-well, respectively. The p-well/substrate junction photoresponse is conducted through the



a. Circuit diagram



b. Pr currents with a low input



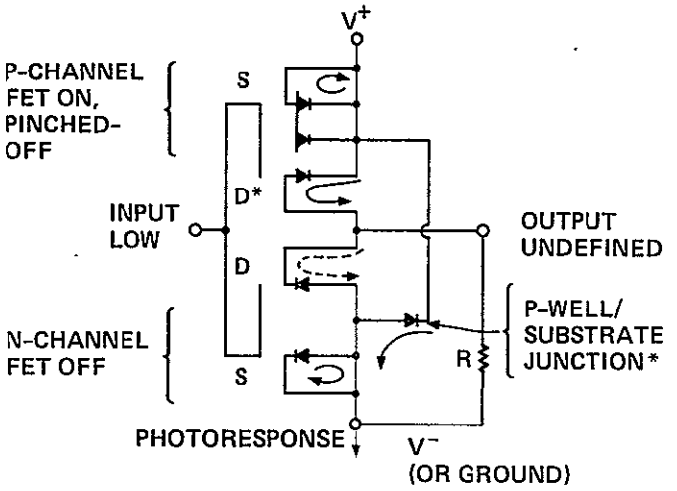
c. Pr currents with a high input

Figure 3-2. CMOS Inverter.

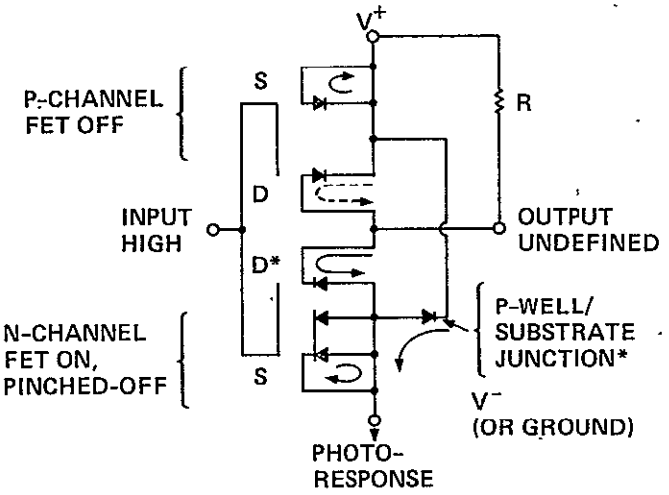
V^+/substrate and V^-/p-well connections. Thus, in this state of the inverter, the imaged elements are the p-well and the n-channel FET's drain.

Figure 3-2c shows the inverter circuit with a high input ($\sim V^+$). The n-channel FET is "on," and its photoresponse is shorted out by the source/p-well connection. The p-channel FET is "off," and its source photoresponse is shorted out by the source/substrate connection. The drain photoresponse is conducted to the V^- and V^+ terminals via the "on" FET and the V^+/substrate connection, respectively. The p-well/substrate junction photoresponse is conducted out as before. The imaged elements are the p-well and the p-channel FET's drain. Thus, the rule of thumb for a correctly operating inverter is that the "off" transistor's drain and the p-well/substrate junction are the elements imaged in either one of the two digital states. This analysis can be extended readily to NAND and NOR gates, in which FET's of one type are stacked in series while the complementary FET's are connected in parallel. In these circuits, only the end transistor in the series stack has its source photoresponse shorted out by a source/substrate or source/p-well connection. Analysis of static operation of other types of circuits is equally straightforward.

During static operation, CMOS circuit stages have the "on" FET's in the nonsaturated state when operating properly because succeeding stages are very high impedance loads. However, if due to an internal anomaly, such as a leakage path or a resistive short, a stage in a CMOS microcircuit were required to supply a relatively high current, the "on" FET would be pinched-off. The photoresponse image would be altered in such a way that the presence of the anomaly could be inferred. This situation is illustrated in Figure 3-3a for a conductive path to V^- (ground or p-well) and in Figure 3-3b for a conductive path to V^+ (n-substrate). The analysis proceeds in the same way for both situations, so only the conductance to V^- (Figure 3-3a) will be considered. With a high ($\sim V^+$) input, the inverter's output is low, and the anomalous load has no effect on the photoresponse image. The p-well junction and the drain of the "off" p-channel FET are imaged by their photoresponses. The "on" n-channel FET is dark. With a low ($\sim V^-$) input, the output tries to go high, but it ends up at some voltage between "0" and "1". The "on"



a. With a low input and an anomalous output load to ground (or V^-).



b. With a high input and an anomalous output load to V^+.

Figure 3-3. CMOS inverter Pr currents.

p-channel FET is pinched off (as in Figure 3-1c), and the n-channel FET is "off." In the pinched-off transistor, the source/substrate connection shorts out the source and field-induced junction photoresponses. The drain is separated from the source and the inverted channel by a high impedance depleted region, so its photoresponse is not shorted out. As shown in Figure 3-3a it is conducted out to the V^+ and V^- terminals via the n-substrate and the anomalous load, respectively. The "off" n-channel FET has its source photoresponse shorted out by the source/p-well connection, as usual. The drain photoresponse is shunted by the anomalous load at the inverter's output. The pinched-off p-channel FET presents a high impedance to the conduction of this photoresponse to external terminals, so the "off" transistor is dark in the photoresponse image. The effect of the anomalous load at the output of the inverter is to make the inverter's photoresponse image the same with a low or a high input. If the anomalous output load conductance goes to V^-, the photoresponse image is the same as for a correctly operating inverter with a high input; if it goes to V^+, the image is as expected with a low input.

The image obtained when the load conductance has no voltage across it appears normal, so detection of the anomaly requires inspection of two photoresponse images: One with and one without voltage across the load conductance. Since the inverter's output state with voltage across the load conductance is logically undefined, the next stage may or may not change logic state when the inverter's input state changes.

To summarize this discussion, a simple analysis has shown that the (static) logical states of correctly operating stages in a CMOS microcircuit can be determined from the photoresponse image displayed by the optical scanner. The conceptually simple but realistic example of an anomalous high conductance at an inverter's output demonstrates that the presence and location of such a flaw can be deduced from photoresponse image data. Reliable detection of the flaw requires inspection of <u>two</u> images: in one image, the inverter would look "normal"; in the image with the complementary input, the inverter would appear not to have changed state. Throughout this analysis the implicit assumption was made that the photoresponse signal would be sensed at the V^+ or V^- power supply terminal.

3.2 THE BASIC IDEA OF THE STATE SUPERPOSITION TECHNIQUE

As discussed previously, the objective in developing the State Superposition Technique was to generate a "characteristic signature" photoresponse image that could be used for microcircuit screening inspection. The approach would be to form an appropriately weighted superposition or average of a set of images having each circuit element in at least one image.

In principle the required superposition can be effected as follows: first, a set of digital states is selected such that each circuit element appears in at least one photoresponse image corresponding to a digital state in the set. Next, a test circuit or program is devised to rapidly clock the device under test through the set of selected digital states. Then, the required superposition of images is generated by scanning the DUT with the optical scanner as it is being clocked repeatedly through the set of selected digital states.

The application of this approach to a CMOS inverter may clarify this rather abstract description. The analysis of how the CMOS inverter's photoresponse image is formed showed that the imaged element is the drain of the "off" transistor. With a low input, the drain of the n-channel FET is imaged; with a high input, the drain of the p-channel FET is imaged. Clearly the superposition of these two images would be an image showing the drains of both FET's in the inverter. The inverter has only two states. The program that will repeatedly clock the inverter through this set of two states is an input square wave. Thus the required State Superposition image of the inverter can be obtained by scanning the DUT as it is being switched rapidly by a square-wave signal applied to the input.

This simple example of the inverter can be extended to more complex circuits, which are made by interconnecting circuit stages not much more complicated than the inverter. Instead of two possible states, a complex circuit can have a very large number of states. The problem is to choose a set of digital states that provides the desired characteristic signature image. For a given circuit this set of digital states is not unique, nor is the order in which the states occur. The criteria for selecting an optimum sequence of digital states have not been determined. At a minimum, the digital state

sequence should be such that every active element appears in the photoresponse image. This will happen if each active element appears in at least one of the photoresponse images that would be obtained statically for each state in the sequence. Although a reliable, formal procedure has not yet been devised for determining a state sequence that satisfies even this minimal criterion for the most general type of circuit, some guidelines for finding a satisfactory sequence for certain types of circuits have been found through experience. This matter is discussed further in Subsection 3.3.

For digital microcircuits the photoresponse is sensed at the power supply or ground terminal, where it appears superimposed on the current normally flowing through the circuit. If an attempt is made to obtain a photoresponse image of a microcircuit as it is being clocked rapidly through some sequence of states, the photoresponse signal is found to be masked by switching transients. This difficulty can be surmounted by using a light beam whose intensity is modulated at a high frequency. The photoresponse then can be separated from the switching transients by a highly frequency-selective demodulator.

The problem of separating an optical signal from noise is well known in optical spectroscopy, where it is solved by the use of a lock-in amplifier. The basic element of the lock-in amplifier is a phase-sensitive detector in which the signal voltage is multiplied by a reference square or sine wave signal, producing sum and difference frequencies. The detector's reference signal can be externally supplied, or it can be derived from an internal reference oscillator. A low-pass RC filter at the detector's output rejects the high frequency components and passes the difference frequencies of sidebands within the passband. Difference frequencies that are removed from the reference frequency by more than the low-pass filter's cut-off frequency are attenuated. Thus, the filter's output is due to that portion of the signal's spectrum that lies about the reference frequency within a passband determined by the low-pass filter.

A lock-in amplifier can be used to extract the photoresponse signal from the switching transients in an operating microcircuit's power supply current provided that certain requirements are met. The most obvious

requirement is that the switching noise spectrum must contain no frequency components within the band extending from the reference modulation frequency f_m to $f_m - \Delta f$, where Δf is the width of the photoresponse sideband spectrum. A sufficient (but not necessary) condition for meeting this requirement is that the switching noise spectrum should contain only frequencies higher than f_m. In practice this condition is usually met.

The sideband spectrum width Δf is closely related to the sharpness or fineness of detail in the photoresponse image and to the raster line-scan time. If the maximum number of spatial frequency periods (i.e., the number of pixels) in one line-scan is n and the line scan period is T_L, then $\Delta f = n/T_L$. The upper limit on n for any microcircuit is set by the diffraction-limited spot diameter d that the optical scanner can deliver. If the line-scan over the microcircuit has length ℓ, the maximum n is approximately $n \approx \ell/d$. A typical value is $n \leq 10^3$ for an optical scanner that uses a conventional microscope objective with visible light.

The manner in which the image information is impressed on the modulated photoresponse places certain restrictions on the choice of f_m, the light modulation frequency. If the photoresponse image is to contain the maximum amount of information, the beam dwell time on each pixel T_L/n is required to equal at least one modulation period $1/f_m$. Then $f_m > n/T_L = \Delta f$. In practice it is convenient to make $f_m \gg \Delta f$.

If a square raster is assumed, the number of scan lines should at least equal n. The frame scan time then is $T_F \geq nT_L$.

The assumption that the diffraction-limited spot size determines the number of pixels n in a line-scan of the photoresponse image leads to an overestimate of n. In fact, carrier diffusion limits the photoresponse image sharpness. This "diffusion blurring" allows somewhat shorter line-scan and frame scan times than the above estimates would indicate.

The two ideas presented here - that of rapidly clocking a microcircuit through a specially selected sequence of digital states, and then using a modulated optical beam in the optical scanner to generate a photoresponse that can be separated from the switching transients - comprise the State Superposition Technique. The photoresponse image so generated will be referred to as a

State Superposition image. The sequence of digital signals applied to the microcircuit's external terminals to cause it to go through the selected sequence of digital states will be referred to as the State Superposition program.

3.3 SOME PRACTICAL CONSIDERATIONS CONCERNING THE STATE SUPERPOSITION TECHNIQUE

In the above explanation of the State Superposition Technique, the program required to operate the DUT during the optical scanner examination was described in abstract terms. Somehow a sequence of digital states must be found such that each active element in the DUT appears in the photo-response image (taken statically) of at least one state. The absence of a formal procedure for generating the sequence for the most general case was noted. In practice, with MSI microcircuits of moderate complexity, it is found that a good approach is to choose a set of input signals that is likely to exercise all of the data signal paths in the circuit. Then this set of signals is applied to the data inputs while all possible combinations of control signals are being applied to the control inputs. The resulting sequence of states is not the minimum necessary, but it is adequate and usually easily generated. Some examples that have proven this approach will serve as illustrations. With simple shift registers, it is only necessary to input a sequence of alternating ones and zeros into the DUT. With up/down counters the circuit is made to count up, then down. Multiplexers with channel-select circuitry are made to select each channel sequentially. If only a part of the circuitry needs to be examined (e.g., if the test is being done for engineering studies and not as a screening inspection), the State Superposition program can be simplified considerably. For example, if testing the operation of parallel jam-inputs in a counter is not required, then the parallel data inputs and the parallel-input-enable circuitry can remain inactive.

For very complex or dense microcircuits, the test circuit that implements the State Superposition program may have to be controlled by the raster generator. This could substantially decrease the time required to scan the DUT, since only the circuit elements being irradiated by the OSS

beam at any given moment would be exercised by the test circuit. For example, the State Superposition program for a memory would alternately write and read ones and zeros in the memory cells. The memory cell addresses would be controlled by the position of the beam so that only the irradiated cell would be addressed and exercised.

4.0 OPTICAL SPOT SCANNER INSTRUMENTATION

The development and application of the State Superposition Technique were done on an optical scanner constructed according to design concepts published by Sawyer and Berning.* Conventional long-working-distance, flat-field, metallographic microscope objectives are used in combination with two photographic lenses. A 50 mm f/1.4 lens is used instead of a microscope eyepiece. A pair of commercial galvanometer mirror scanners separated by a 50 mm f/1.0 field lens comprise a two-axis scanner assembly. A beam splitter between the microscope objective and the 50 mm f/1.4 lens is used to direct the light reflected back from the specimen to a photodetector. The reflected light signal yields an image that is essentially identical to that obtained with a conventional bright-field, reflected light microscope. A diagram of the optical arrangement is shown in Figure 4-1.

Each galvanometer mirror scanner is driven with a sawtooth waveform whose period is independently adjustable. A wide range of combinations of frame scan time and number of scan lines per frame is available. For the work reported here, a frame scan time of 50 sec and a line scan time of 0.1 sec was used, resulting in a 500 line raster with nearly invisible scan lines and very good reflected light image quality. The use of such a slow frame scan was required primarily to overcome a CRT writing speed limitation in a false-color photography method that is described further on.

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*D. E. Sawyer, D. W. Berning, "A Laser Scanner for Semiconductor Devices," NBS Special Publication 400-24.

The equipment required specifically for implementing the State Superposition Technique included a Metrologic ML-669 0.5 mW modulatable He-Ne red laser and a Princeton Applied Research HR-8 Lock-in Amplifier with a Type C Preamplifier. The Metrologic laser is a current-modulated laser with a usable modulation frequency band of 50 Hz - 500 kHz and a

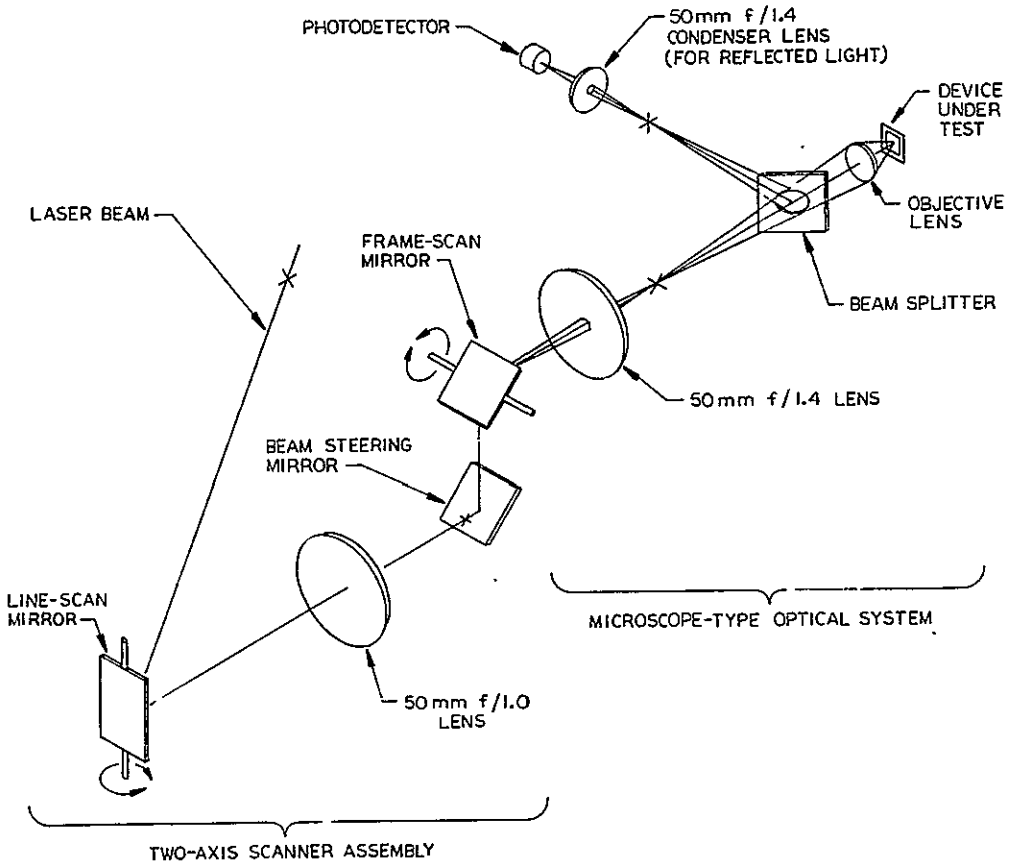


Figure 4-1. Diagram of optical arrangement of the optical spot scanner.

maximum modulation index of 0.15. For the experiments reported here the laser's output was attenuated by a neutral density filter of ~25% transmissivity. The power delivered at the focal point on the DUT's surface probably was less than 0.1 mW. (Though normally unnecessary with digital CMOS specimens, the ND filter is used to limit the photocurrent injected into linear bipolar microcircuits (e.g., op-amps, comparators) and also to prevent latch-up in some CMOS devices after removal of the passivation. It is routinely left in the beam path and removed only when the photoresponse signal is too weak.)

The P.A.R. HR-8 lock-in amplifier is capable of operating with a reference oscillator frequency $f_m \leq 160$ kHz, which is well within the laser's modulation bandwidth.

The photoresponse signal is sensed by a small (100Ω) resistor in series with the V^- or ground terminal of the Device Under Test (DUT). The voltage drop across the sensing resistor is amplified by a Tektronix 1A7A oscilloscope plug-in amplifier connected ahead of the lock-in amplifier. To diminish the switching noise entering the lock-in amplifier, the adjustable low and high pass filters in the 1A7A plug-in are set for a bandpass of 10 kHz - 100 kHz. The use of a modulation frequency $f_m \simeq 130$-140 kHz, slightly outside this passband, results in a negligible loss of signal strength after the phase control on the lock-in amplifier's demodulator has been adjusted for maximum demodulated signal output.

An important advantage of using the modulated laser and lock-in amplifier demodulator is that the zero reference level of the photoresponse signal is independent of the static power supply current consumption of the DUT. This is not true when an unmodulated laser is used, and the CRT's intensity control must be continually readjusted when the DUT's current changes (i.e., as a result of changing the DUT's digital state, temperature, or the DUT itself).

The way in which the lock-in amplifier and the modulatable laser are incorporated in the optical scanner is shown diagrammatically in Figure 4-2.

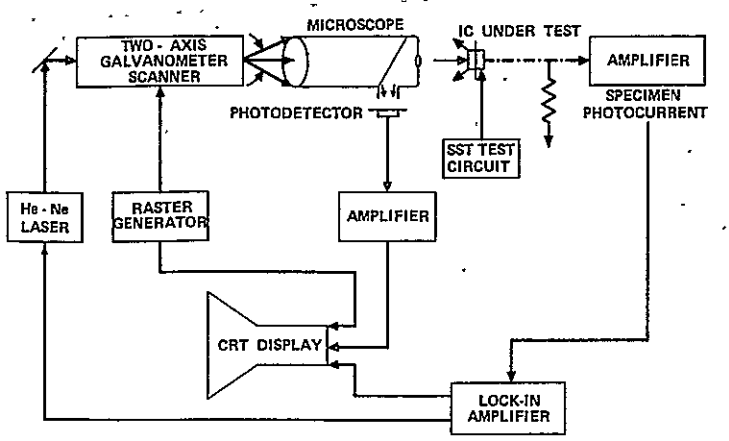


Figure 4-2. Block diagram of optical spot scanner set up for the State Superposition Technique.

A flat-face, electromagnetically-deflected CRT display with a 4" x 5" screen is used for photographic recording. This display can resolve at least 500 lines in the vertical (4") dimension. Its broad-band P-4 phosphor was chosen so that false-color images could be made on color film by multiple exposures through additive primary-color filters. This method is very effective for localizing features in the photoresponse image with respect to features of the reflected light image. The reflected light image is photographed through a green filter or without a filter; the photoresponse image is photographed through a red filter. Multiple-exposures through different colored filters are also extremely valuable for comparing the photoresponse images obtained under different conditions. For example, the relative effectiveness of two State Superposition Programs in imaging all active elements can be evaluated by this method. The identification and localization of the point of malfunction under special conditions can also be done in this way. The photoresponse images with and without the malfunction are superimposed by a double exposure through a green and a red filter, respectively. FET's that stop switching (remain "on") when the circuit malfunctions appear red. This method was used to localize CMOS microcircuit stages that malfunction at high frequency, as reported in the next section. Unfortunately, the color photographs cannot be reproduced in these printed proceedings.

A CRT display with P-7 long-persistence phosphor is used as a visual display. An X-Y oscilloscope is used as a waveform monitor for displaying either the reflected light or the photoresponse signal: the raster generator's line-scan signal is connected to the X input, and the monitored signal is connected to the Y input.

4.1 ILLUSTRATIVE RESULTS WITH A CMOS INVERTER

Experimental verification of the analysis of the CMOS inverter's photoresponse behavior was obtained with a type 4049 hex inverting buffer. The reflected light image of one inverter on the 4049 chip is shown in Figure 4-3. The n-channel FET appears below the p-channel FET, just as in the circuit diagram in Figure 3-2a. (Unlike most CMOS microcircuits, the type 4049 has the n-channel FET larger than the p-channel FET because it is intended to interface with TTL microcircuits, an application in which it must act as a current sink. The input protection circuit is also different. These differences do not affect the validity of the results presented here.)

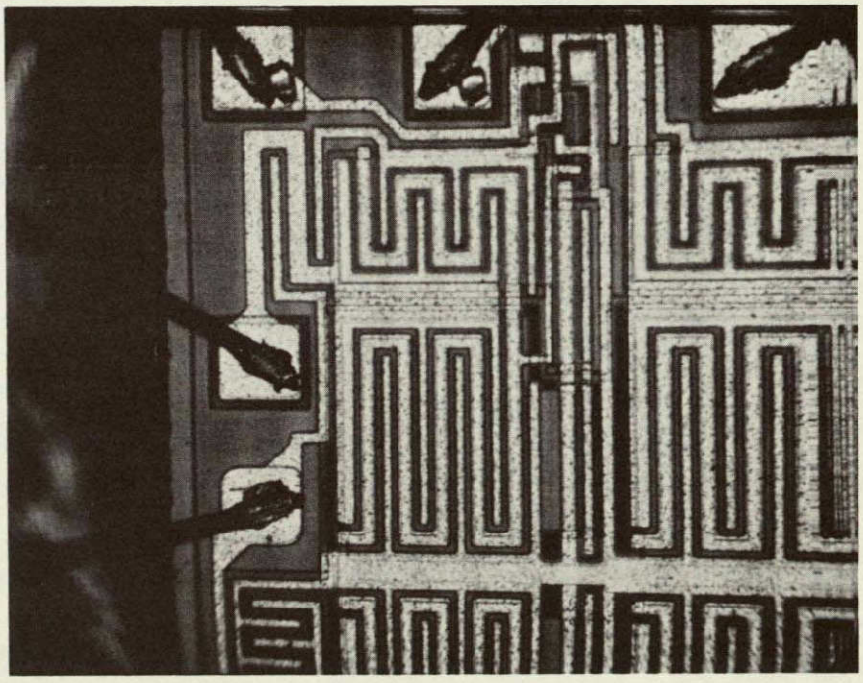
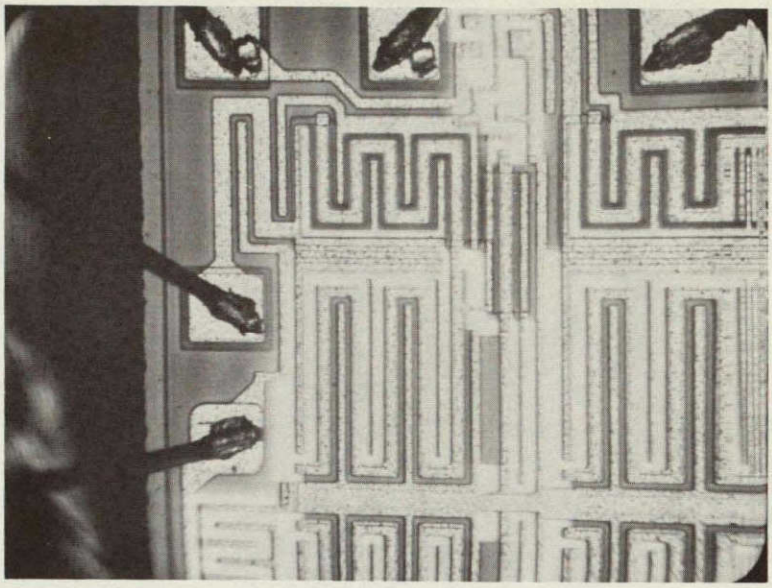


Figure 4-3. Reflected light image of a CMOS inverter on a MC14049B hex inverter/converter chip.

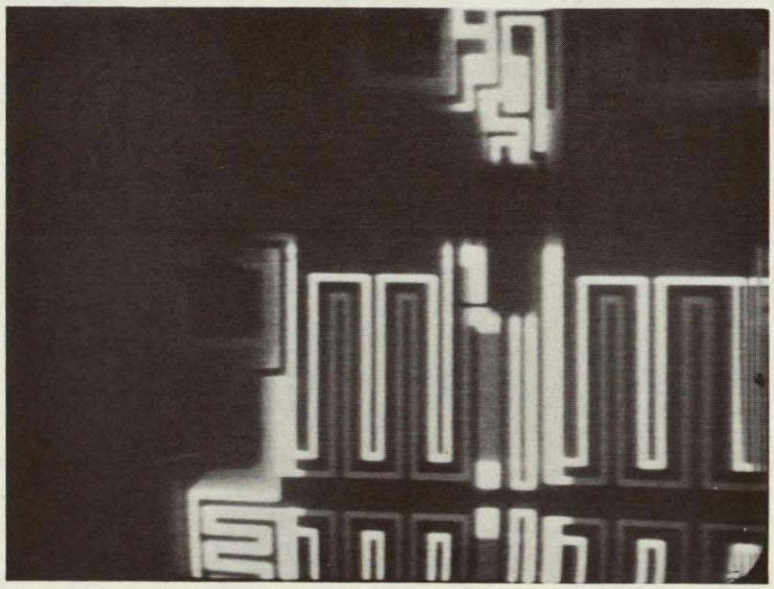
Photoresponse images of the inverter were made with 10V power supply voltage; the modulated laser was used with $f_m \simeq 130$ kHz. The photoresponse image with a low (~0V) input is shown superimposed on the reflected light image in Figure 4-4a and by itself in Figure 4-4b. The imaged features are the drain of the "off" n-channel FET and the p-well/substrate junction, as predicted in Figure 3-2b. The corresponding images for a high (~10V) input are shown in Figures 4-5a and 4-5b. As predicted in Figure 3-2c, the imaged features are the drain of the "off" p-channel FET and the p-well/substrate junction.

The case of the inverter with the anomalous load with a high conductance to ground was simulated by a 100Ω load resistor at the output of the inverter test specimen. The resulting photoresponse image, shown in Figure 4-6, is as predicted in Figure 3-3a: the imaged features are the drain of the "on" p-channel FET and the p-well/substrate junction. The "off" n-channel FET appears dark.

The State Superposition image of the inverter was obtained as the inverter was being driven with a 3.0 MHz, 10V symmetrical square-wave. As shown in Figure 4-7, the drains of both the n-channel and the p-channel FET's are imaged together with the p-well/substrate junction. Figure 4-7 is essentially a superposition of Figures 4-4b and 4-5b, as expected from the way in which it was generated.

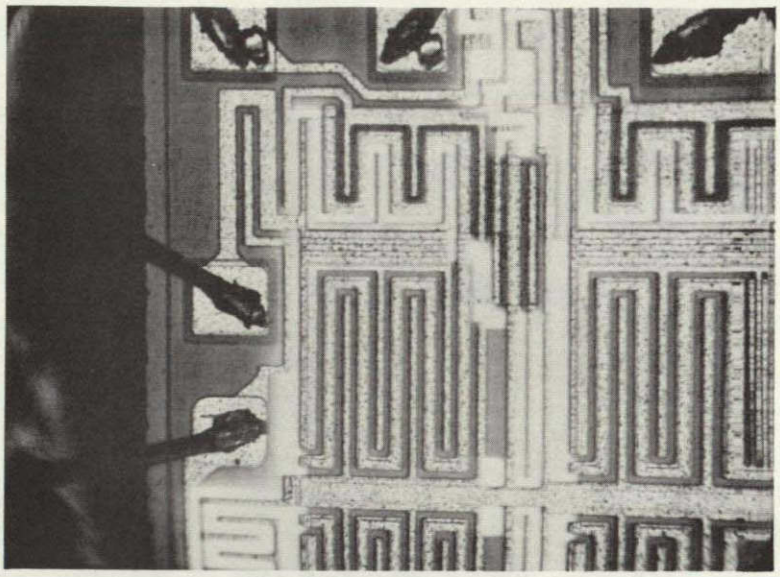


a. Superimposed on the reflected light image

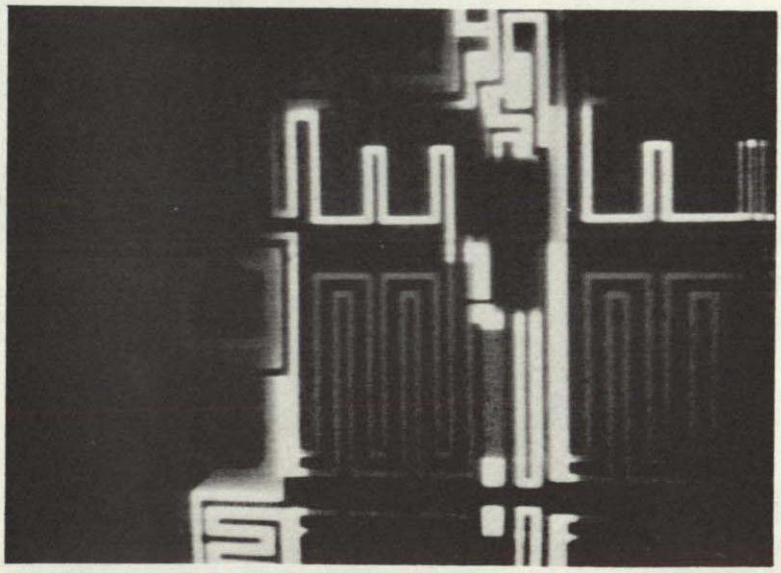


b. Photoresponse image (alone)

Figure 4-4. Photoresponse image of a CMOS inverter. (Low input).



a. Superimposed on the reflected light image



b. Photoresponse image (alone)

Figure 4-5. Photoresponse image of a CMOS inverter. (High input).

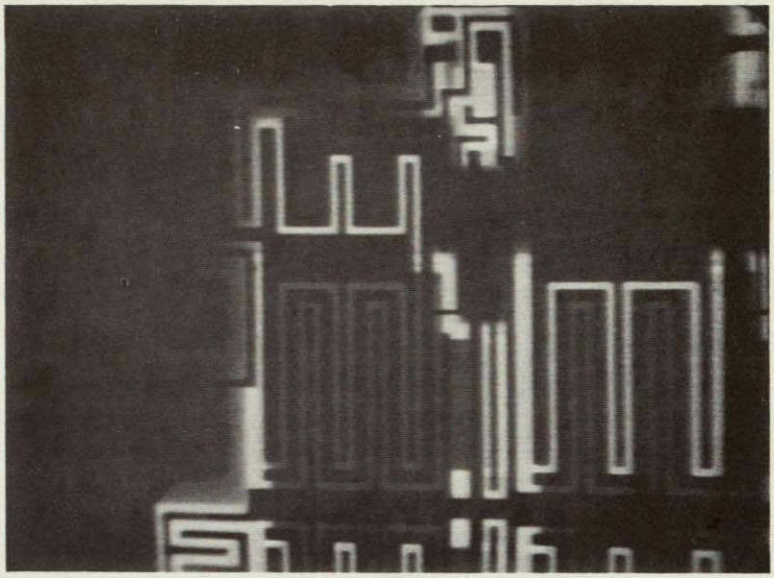


Figure 4-6. Photoresponse image of CMOS inverter with low input and a 100Ω load resistor to V^-.

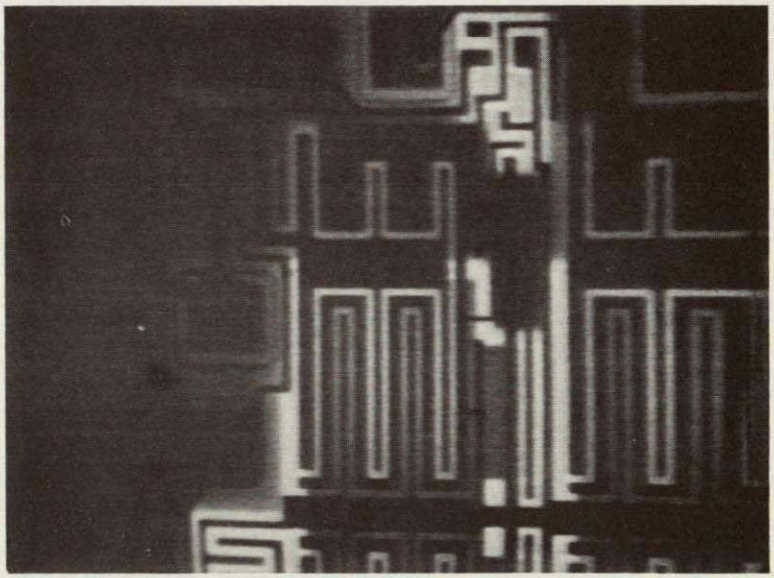


Figure 4-7. State superposition image of inverter being driven by a 3.0 MHz square-wave.

5.0 TEST OF THE CD4028A BCD-TO-DECIMAL DECODER

5.1 CIRCUIT DESCRIPTION

The CD4028A is a fully static BCD-to-decimal decoder. A positive-true logic input BCD number (0-9) applied to the inputs DCBA causes the corresponding decimal output to go high while the other outputs remain low. The logic diagram of this microcircuit is shown in Figure 5-1. The circuit diagram is shown in Figure 5-2 with the individual MOSFET's labelled by numbers 1 to 120. Although not shown explicitly, the p-well is connected to the V^- terminal, and the n-substrate is connected to the V^+ terminal. The p-well/substrate junction is also omitted from the diagram.

Figure 5-3 is a micrograph of the CD4028A chip with the MOSFET's labelled on the gate electrodes.

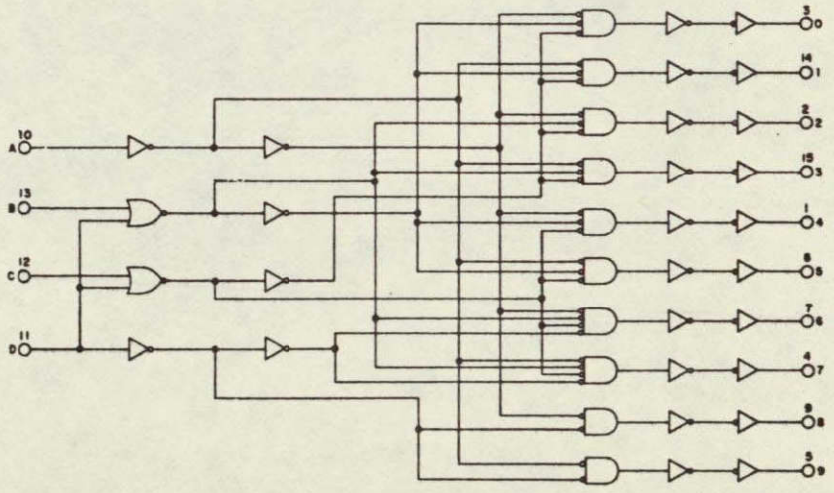


Figure 5-1. Logic diagram of the CD4028A microcircuit.

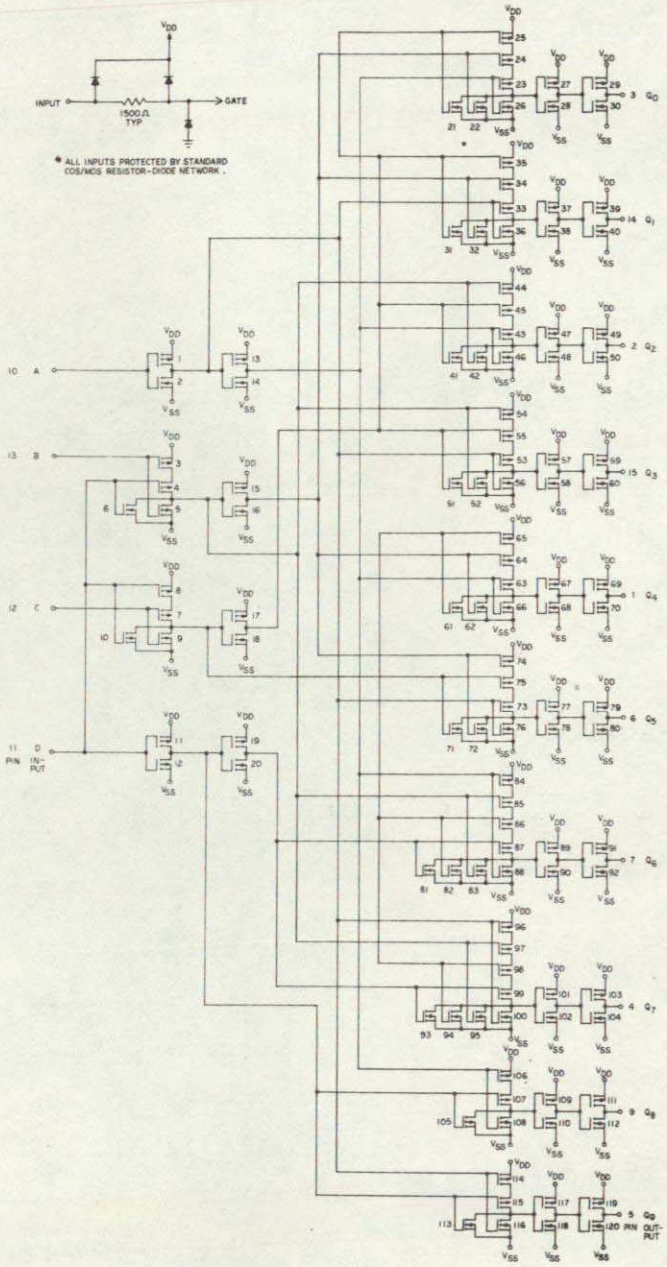


Figure 5-2. Circuit diagram of the CD4028A microcircuit.

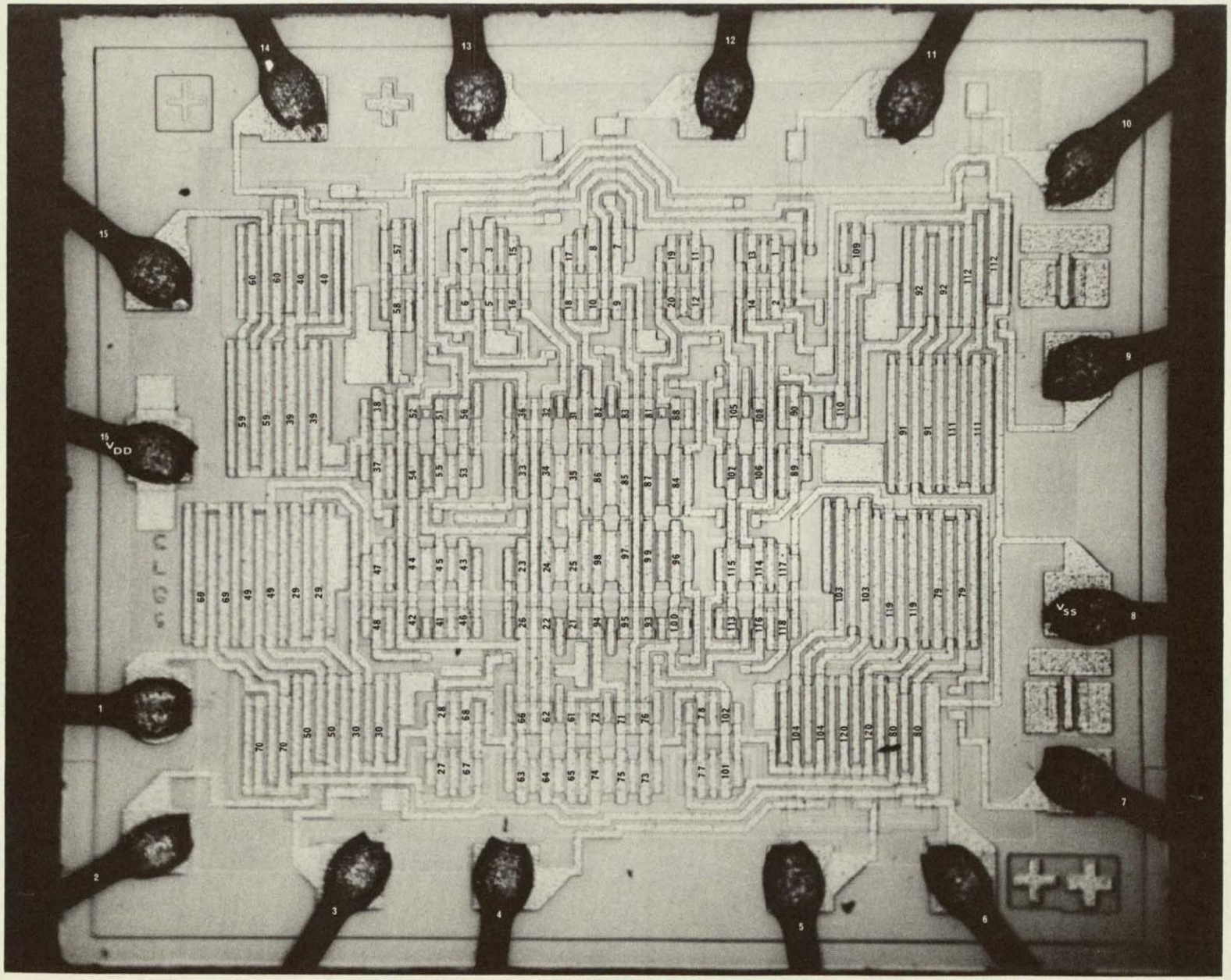


Figure 5-3. Micrograph of the CD4028A microcircuit chip. (1.70 mm x 1.50 mm)

5.2 STATE SUPERPOSITION PROGRAM DEVELOPMENT

Although its internal complexity qualifies the CD4028A as a MSI microcircuit, it is a relatively simple device for which to develop a State Superposition program. It has four parallel digital inputs to which a BCD number is applied, so that there are at most 16 possible input data words. There are no control inputs of any kind. The State Superposition program must therefore consist of a sequence of four bit input words that causes all circuit elements to appear in the photoresponse image. As a first step, the photoresponse images of a good device were recorded with each of the binary input numbers 0 to 15. The results showed that each circuit element appeared in at least one image for the numbers 0 through 9. The FET's associated with the final decode gates (in Figure 5-1) appeared in several images. Each p-channel FET in an output inverter driver was imaged only when its corresponding output was high (i.e., when the p-channel FET was off). The State Superposition program that images all circuit elements must therefore include all BCD input numbers 0 through 9. The duration of each input number in the program must be approximately the same if each output inverter driver is to be imaged with the same intensity. While the BCD input numbers 0 through 9 could occur in any sequence, they can be generated most conveniently with a decade or binary counter. A conventionally clocked decade counter does not generate the BCD numbers with equal duration: the interval required to reset the counter in the transition from 9 to 0 can shorten the duration of one or both of these numbers. However, this duty cycle nonuniformity has only a minor effect on the appearance of the affected circuit elements in the photoresponse image.

Preliminary tests of this program were carried out with a test circuit in which a CD4029A binary/decade presettable up/down counter was used to drive the CD4028A test device directly. A pulse generator was used to clock the CD4029A at 3.3 MHz in the upcount mode, both as a decade and a binary counter. Results showed that the basic idea for this State Superposition program was a sound one, but that some improvements were necessary. The output inverter driver's p-channel FET's were not imaged

at all. A check of the signals at the test specimen's input terminals showed that, due to inadequate drive capability, the CD4029A counter was delivering triangular pulses with rounded-off tops to the CD4028A test device input terminals. Even with good, square-top pulses, the "off" duty cycle of each p-channel FET would be only about 10 percent, so that only a faint image would be expected under the best of circumstances. The degraded pulses resulted in a shorter "off" duty cycle and consequently, an inadequate level of photoresponse signal from these circuit elements.

Comparisons of photoresponse images made with the counter operated in the binary mode and the decade mode disclosed only small differences in the photoresponse levels for various circuit elements.

The test circuit that was developed for subsequent tests of the CD4028A specimens is shown in Figure 5-4. The CD4029A counter was clocked with a 1-10 MHz square-wave generator (a Hewlett-Packard 220A) via level-shifting circuitry. A fixed 15 V supply was used to power the CD4029A, whose outputs were level-shifted down to the test device's (variable) V^+ power supply voltage by a CD4050B non-inverting buffer/converter. With a test device power supply voltage of 5 V, this test circuit delivered good, clean pulses at the test specimen's input terminals up to a clock frequency of ~7.1 MHz, beyond which the CD4029A counter began to malfunction. A Hewlett-Packard 5301 six-digit frequency counter was used to monitor the clock frequency.

5.3 SUMMARY OF ELECTRICAL TEST RESULTS

The set of twenty CD4028A test specimens was supplied by NASA MSFC with electrical test print-outs. The test specimens had been subjected to a 1000 hour, 125°C life-test and then tested to a tentative 38510 specification by DCA Reliability Laboratory. A group of ten reject specimens had been chosen on the basis of static current consumption tests. The other ten specimens constituted a control group of good devices. All specimens, both good and reject, were fully functional, although many devices in each group had failed one or more propagation time or transition

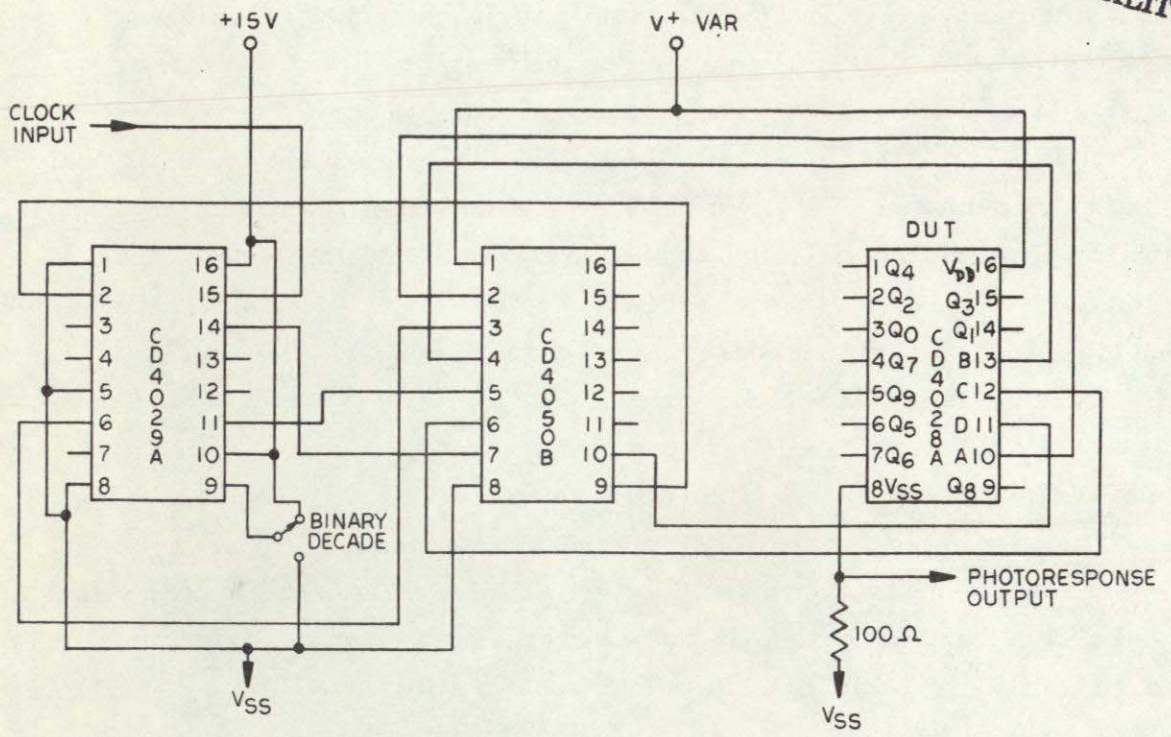


Figure 5-4. State superposition test circuit for the CD4028A microcircuit.

time tests. For all specimens the low-to-high propagation time was greater for the odd-numbered tests than for the even-numbered tests, with the tests whose number ended in seven always yielding the longest times. The relationship between test number and input BCD number is uncertain, but it is believed that the tests were conducted with BCD numbers increasing in order from 0 to 9. The test number ending with digit n then should correspond to BCD input n-1. If so, the tests showed that propagation times to even-numbered outputs were consistently longer than to odd-numbered outputs, with the propagation time to output No. 6 always being the longest for any given specimen.

5.4 HERMETICITY TESTS AND VISUAL EXAMINATION

Hermeticity tests were performed on all the CD4028A specimens in accordance with MIL-STD-883, Method 1014, Condition A (fine leak) and Condition C (gross leak). The results are shown in Table 5-1. All specimens

TABLE 5-1. HERMETICITY TEST RESULTS
FOR THE CD4028A SPECIMENS

	Pressure: 75 psi; Time: 1+hrs.		
Parameter	Fine Leak	Elapsed Time	Gross Leak
Conditions	MIL-STD-883, Met. 1014 Condition A	Pressure Vessel to Spectrometer	MIL-STD-883, Met. 1014 Condition C
Requirement	5.0×10^{-8} max	30 minutes max	No bubbles observed
Unit of Measurement	atm-cc/sec	minutes	Check mark indicates no bubbles observed

Specimen			125°C
*2721	2.0×10^{-7}	< 30 min.	✓
*2724	1.0×10^{-7}		
2735	3.0×10^{-8}		
2737	5.0×10^{-8}		
*2738	1.5×10^{-7}		
2750	2.0×10^{-8}		
2753	1.6×10^{-8}		
2765	5.0×10^{-8}		
2770	4.5×10^{-8}		
2772	5.0×10^{-8}		
*2722	8.0×10^{-8}		
2733	1.2×10^{-8}		
2734	3.5×10^{-8}		
2749	1.5×10^{-8}		
2756	1.0×10^{-8}		
2766	4.0×10^{-8}		
2768	3.6×10^{-8}		
2773	1.0×10^{-8}		
2779	3.0×10^{-8}		
2780	1.0×10^{-8}	< 30 min.	✓

*Specimen failed fine leak test

Date: 8-31-76
Mass Spectrometer: NRC925

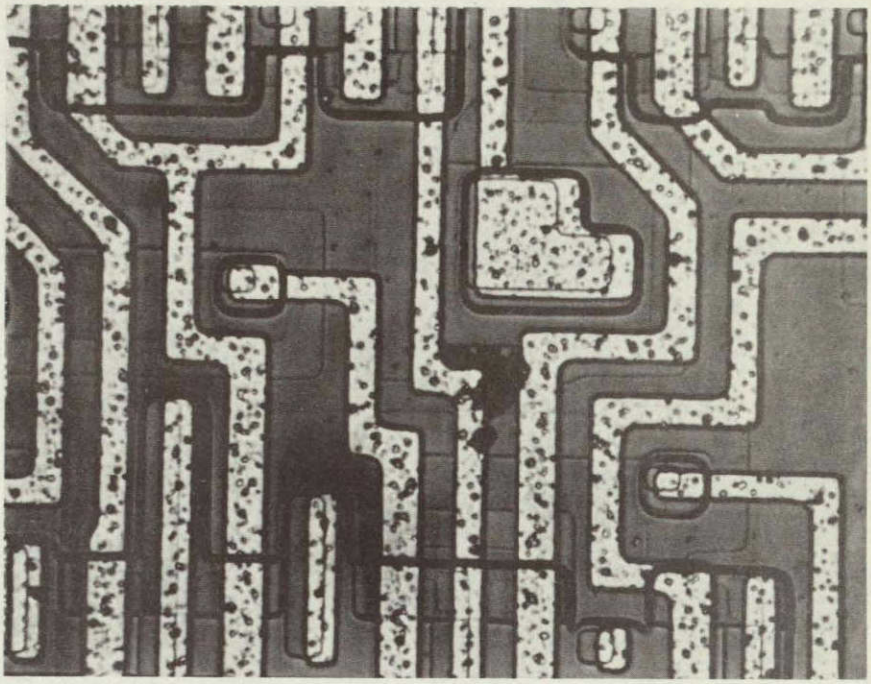
Date: 8-31-76

passed the gross leak test; two reject and two good specimens failed the fine leak test. No correlation was found between the hermeticity test failures and the electrical test results.

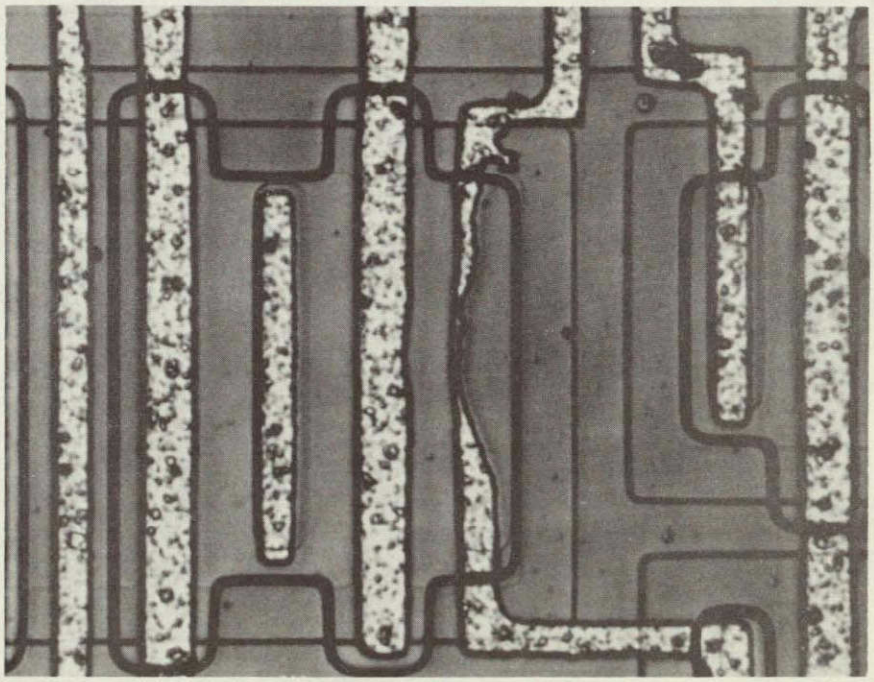
The microcircuit packages were given an external visual examination with a low power stereomicroscope; no anomalies were noted. The packages were uncapped, and the exposed chips were carefully examined with a Reichert Zetopan microscope. All apparent anomalies or defects were noted and photographed. These defects included: photoresist residues adhering to metallization, thin or irregular metal resulting from photolithographic flaws, scratched silicon, localized cracks in the passivation, and metallization misalignment. Except for the metallization misalignment, these defects were distributed more or less evenly among the good and reject specimens. Most of the specimens having metallization misalignment were found to have only one of two identified patterns of electrical behavior. One characteristic of this behavior pattern was a high value of current consumption that was nearly independent of the input BCD data. In CMOS microcircuits the static current consumption is essentially a leakage current, which could increase if incomplete gate coverage by misaligned metallization led to ionic contamination of the gate oxide. Examples of these defects are shown in Figures 5-5a through 5-5h.

5.5 ELECTRICAL TESTS USING THE STATE SUPERPOSITION TEST CIRCUIT

The electrical tests performed by DCA on a computerized tester identified excessive leakage current and limited frequency of operation as the two characteristics that could result from effects detectable by the optical scanner. In order to plan the optical scanner experiments, the twenty specimens were tested with the State Superposition test circuit described previously (Figure 5-4). With the test device power supply set at 5 V, the frequency of the square wave generator clocking the CD4029A counter was gradually increased in small increments. The counter was operated in the decade upcount mode. Every output of the test device was checked with an oscilloscope after each frequency increase. As the

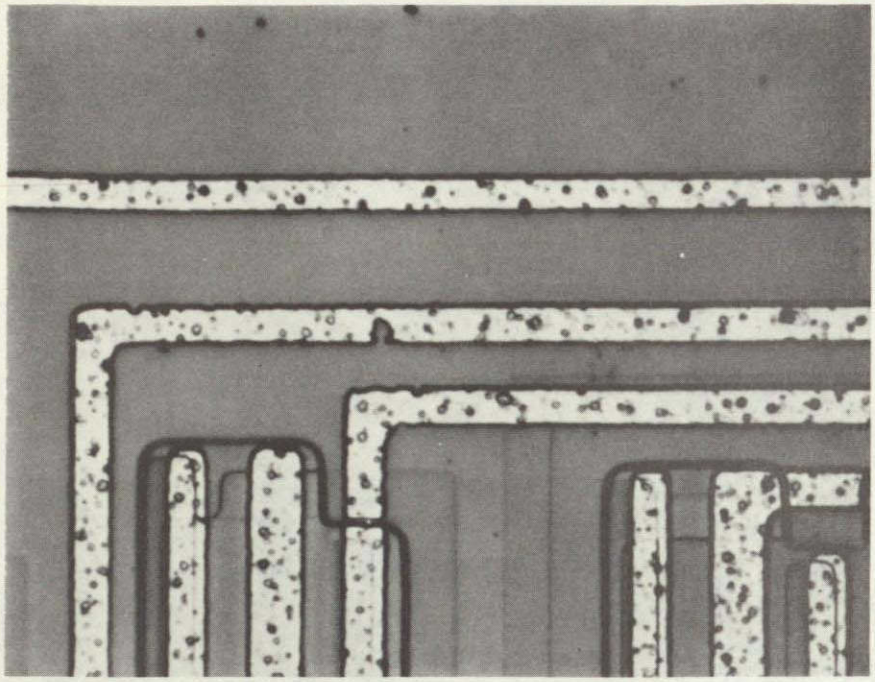


a. Photoresist residues adhering to metallization Specimen 2735. (490X).

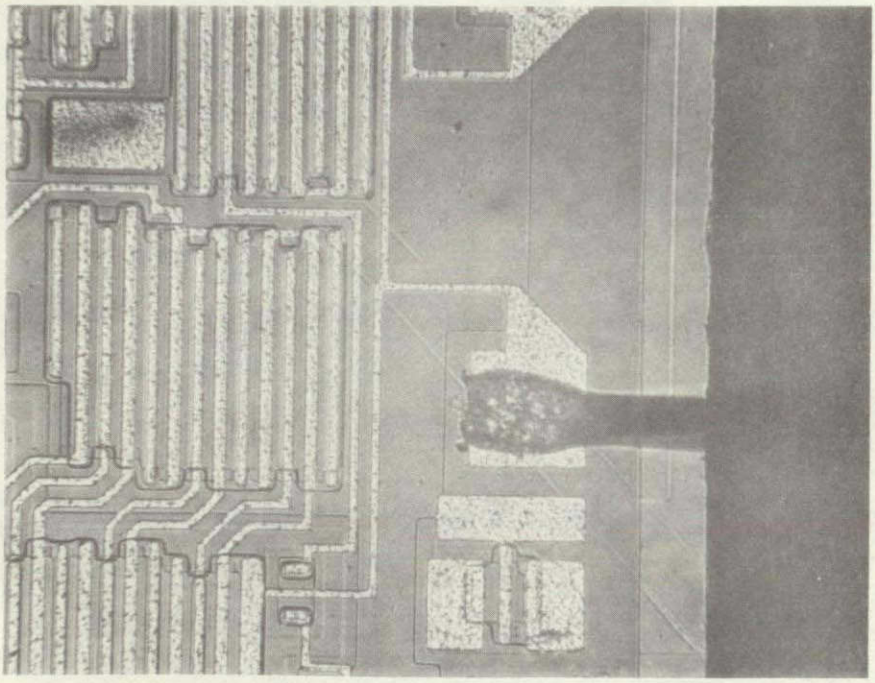


b. Necked-down metallization. Specimen 2737. (670X)

Figure 5-5. Examples of defects found in CD4028A specimens by visual inspection. (Sheet 1 of 4)

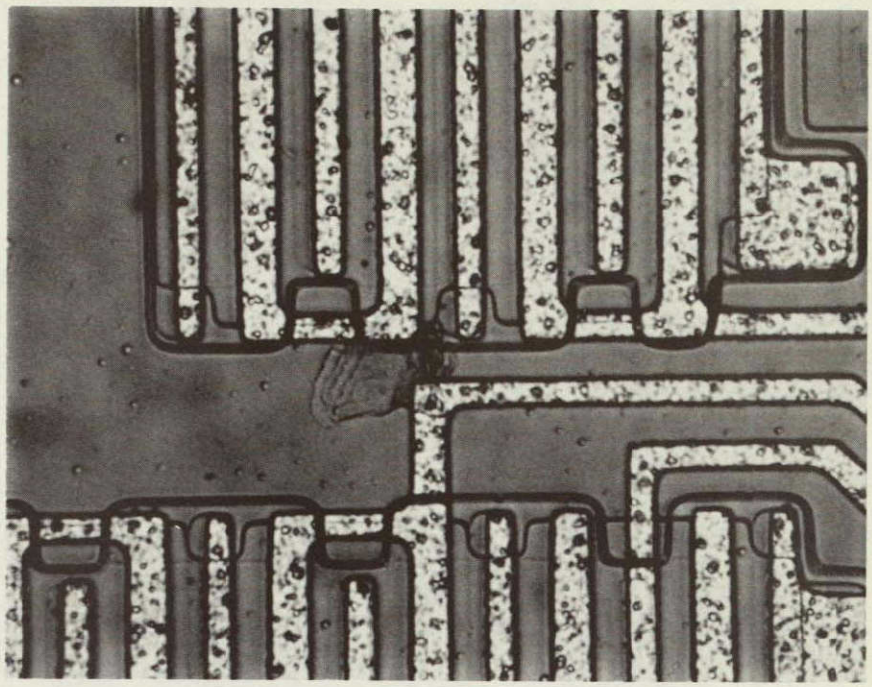


c. Necked-down metallization
Specimen 2773. (630X)

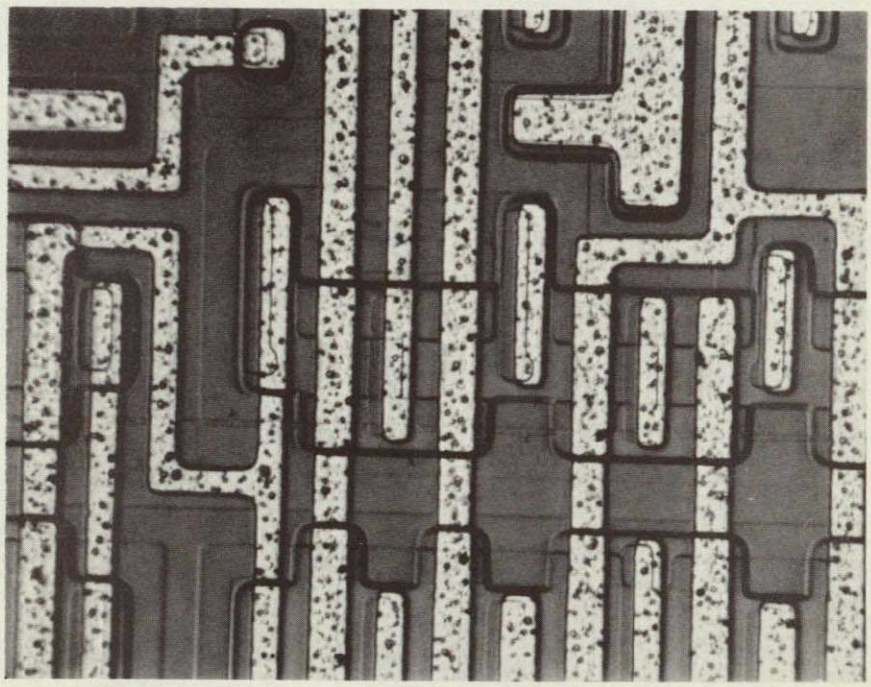


d. Scratch in the silicon substrate
Specimen 2766. (120X)

Figure 5-5. Examples of defects found in CD4028A specimens by visual inspection. (Sheet 2 of 4)

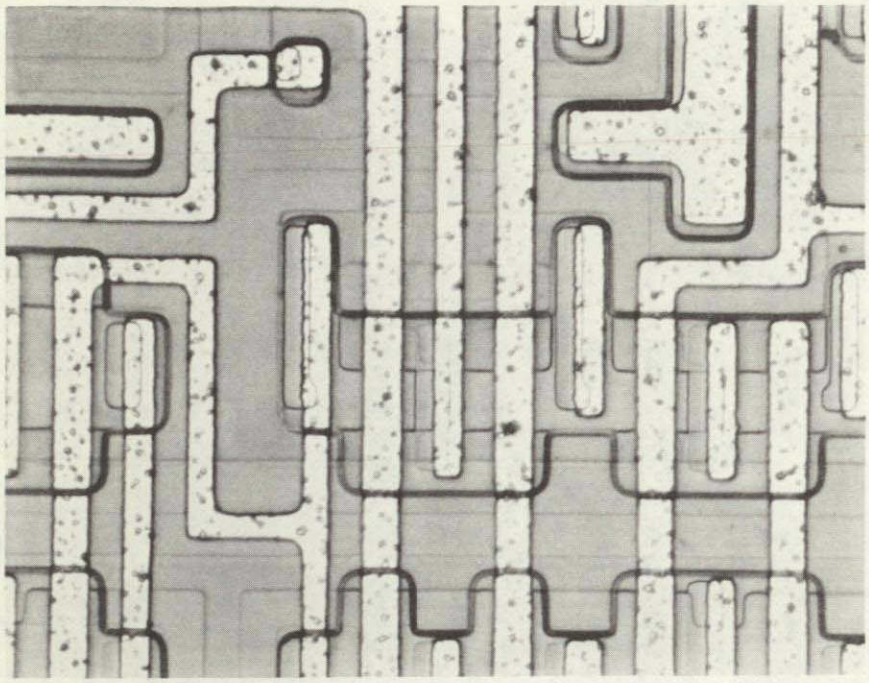


e. Cracked passivation.
Specimen 2734. (510X)

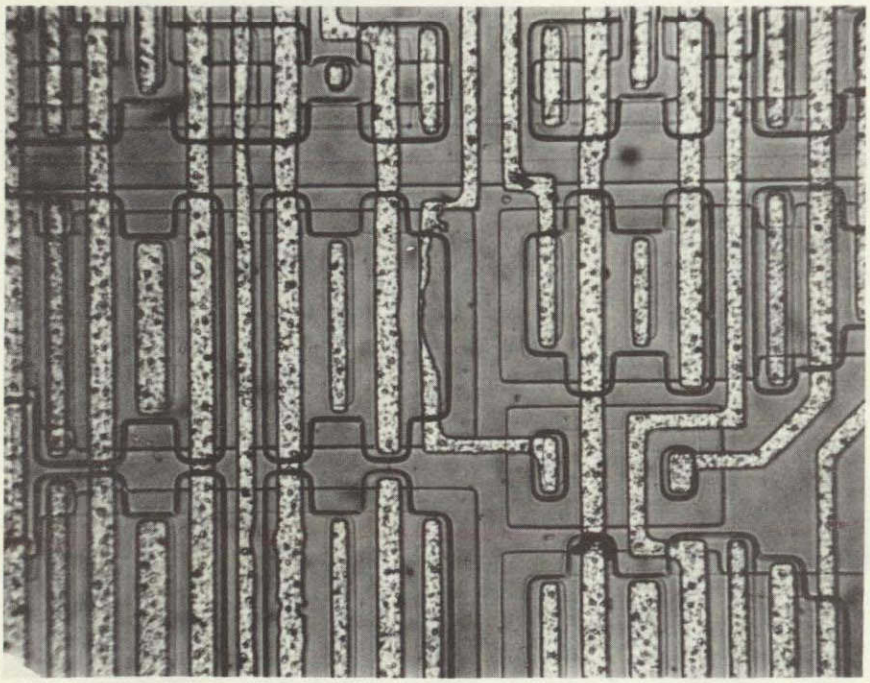


f. Metallization misalignment
Specimen 2773. (430X)

Figure 5-5. Examples of defects found in CD4028A specimens by visual inspection. (Sheet 3 of 4)



g. Metallization misalignment
Specimen 2780. (440X)



h. Metallization misalignment
Specimen 2737. (320X)

Figure 5-5. Examples of defects found in CD4028A specimens by visual inspection. (Sheet 4 of 4)

maximum operating frequency of the test device was passed, some of the output pulses began to decrease in amplitude until they merged with the baseline switching noise. The frequency at which each output dropped out completely in this way was recorded for each specimen up to the maximum clock frequency (7.1 MHz) at which the test circuit could be operated. The output drop-out frequencies are listed in Table 5-2. It can be seen from these data that the twenty specimens can be divided into two categories: one for which the odd-numbered outputs drop out first (Type 1), and one for which the even-numbered outputs drop out first (Type 2). The table also lists the current consumption measurements for BCD input numbers 0 - 9. These results are well correlated with the high frequency behavior: the Type 2 circuits all have a high level of static current consumption that is nearly independent of the input data; the current consumption of the Type 1 circuits is highly dependent on the input data. For each Type 1 circuit there is at least one input number that results in a very low current reading (<0.7 nA). In the tables the specimens that were found to have misaligned metallization are denoted by an asterisk. All but one of these specimens are Type 2. The amount of misalignment in the Type 1 specimen was less than in the Type 2 specimens.

5.6 OPTICAL SCANNER EXPERIMENTS

5.6.1 Photoresponse Image Survey

Photoresponse images of all twenty specimens were recorded with the State Superposition test circuit described previously. With specimen power supply voltages of 10 V and 5 V the CD4028A counter was operated in the decade upcount mode with a clock frequency of 2.50 MHz. All circuits were fully operational under these conditions.

Figure 5-6 shows the reflected light image of a CD4028A specimen as recorded on the optical scanner's CRT display during these experiments. The photoresponse image obtained with $V^+ = 0$ V, shown in Figure 5-7, is an image of the p-well/substrate junctions.

TABLE 5-2. OUTPUT DROP-OUT FREQUENCIES AND I_{ss} DATA FOR THE CD4028A SPECIMENS

Specimen	2721(G)		2724(G)		2735(G)		2737(G)		2738(G)	
Output No.	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$
0	700pA		1050pA		9.035μA	5.31	1035pA		250pA	
1	350pA	5.21	700pA	5.12	9.030μA		1100pA	6.30	500pA	6.20
2	550pA		850pA		9.075μA	5.38	650pA		1050pA	
3	350pA	5.58	650pA	5.46	9.040μA		1150pA	6.56	550pA	6.38
4	700pA		950pA		9.040μA	5.31	950pA		950pA	
5	150pA	5.89	500pA	5.71	9.045μA		1050pA	6.79	850pA	6.74
6	1050pA		1350pA		9.055μA	5.23	1350pA		1000pA	
7	-50pA	6.01	350pA	5.98	9.050μA		900pA	6.92	1350pA	≥ 7
8	1000pA		1350pA		9.065μA	5.50	1250pA		600pA	
9	-100pA	6.22	250pA	6.26	9.055μA		450pA	6.63	1300pA	6.70
Specimen	2722(R)		2733(R)		2734(R)		2749(R)		2756(R)	
Output No.	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$
0	150pA		20.85μA	5.38	44.60μA		19.75μA	5.70	12.50μA	5.64
1	150pA	5.47	20.85μA		44.10μA	5.23	19.75μA		12.50μA	
2	1050pA		20.90μA	5.49	43.95μA		19.80μA	5.85	12.55μA	5.80
3	1.095μA	5.79	20.85μA		650pA	5.49	19.75μA		12.50μA	
4	271.5μA		20.85μA	5.38	44.10μA		19.75μA	5.71	12.50μA	5.72
5	800pA	5.89	20.85μA		43.80μA	5.76	19.75μA		12.50μA	
6	950pA		20.85μA	5.33	43.95μA		19.75μA	5.78	12.50μA	5.56
7	500pA	6.28	20.85μA		43.75μA	5.87	19.75μA		12.50μA	
8	1050pA		20.85μA	5.63	43.85μA		19.75μA	5.96	12.55μA	5.91
9	250pA	6.48	20.85μA		43.75μA	5.99	19.75μA		12.50μA	

(Table 5-2, concluded)

Specimen	2750(G)		2753(G)		2765(G)		2770(G)		2772(G)	
Output No.	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$
0	8.91μA	5.36	6.995μA	4.24	950pA		1050pA		2550pA	
1	8.920μA		6.960μA	7.03	650pA	5.81	900pA	5.61	2900pA	5.31
2	8.955μA	5.49	6.990μA	4.43	450pA		1750pA		1650pA	
3	8.920μA		6.965μA		600pA	6.09	850pA	5.94	2650pA	5.56
4	8.920μA	5.43	6.970μA	4.37	700pA		1950pA		1950pA	
5	8.920μA		6.965μA		400pA	6.29	1000pA	6.23	2750pA	5.93
6	8.930μA	5.45	6.975μA	4.37	1050pA		2000pA		2450pA	
7	8.920μA		6.970μA		150pA	6.54	1350pA	6.67	2600pA	6.24
8	8.935μA	5.52	6.980μA	4.43	1150pA		1550pA		2400pA	
9	8.925μA		6.975μA		150pA	6.18	1250pA	7.05	1700pA	6.00

Specimen	2766(R)		2768(R)		2773(R)		2779(R)		2780(R)	
Output No.	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$	I_{ss}	$f_{d.o}$
0	106.0μA		50pA		10.35μA	5.58	103nA		12.55μA	5.43
1	106.0μA	5.57	350pA	5.14	10.35μA		102.5nA	4.63	12.55μA	
2	950pA		450pA		10.40μA	5.74	94.1μA		12.60μA	5.55
3	150pA	5.89	1050pA	5.45	10.35μA		124.5nA	4.90	12.55μA	
4	105.0μA		50pA		10.35μA	5.65	103nA		12.55μA	5.49
5	104.5μA	6.02	181.5μA	5.65	10.35μA		1300pA	5.28	12.55μA	
6	150pA		550pA		10.35μA	5.57	123.5nA		12.55μA	5.46
7	1100pA	6.35	500pA	5.98	10.35μA		124nA	5.50	12.55μA	
8	300pA		1150pA		10.35μA	5.92	104.5nA		12.55μA	5.66
9	950pA	6.60	200pA	5.90	10.35μA		103nA	5.68	12.55μA	

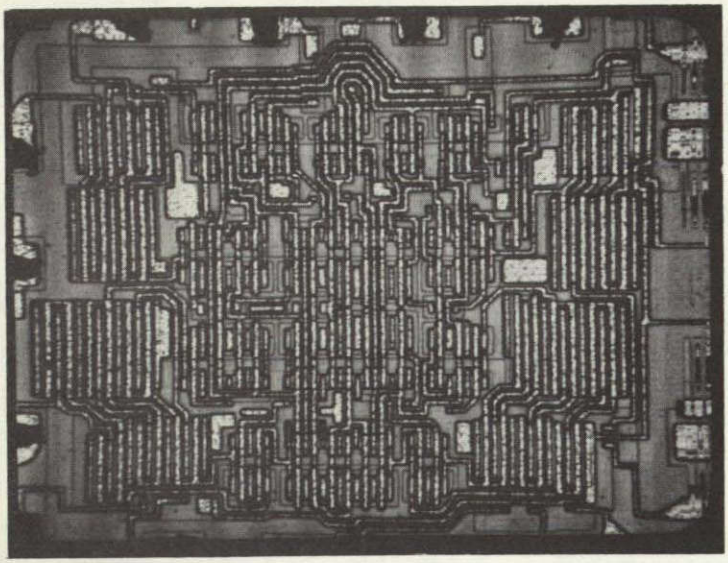


Figure 5-6. Reflected light image of a CD4028A microcircuit recorded on OSS CRT display.

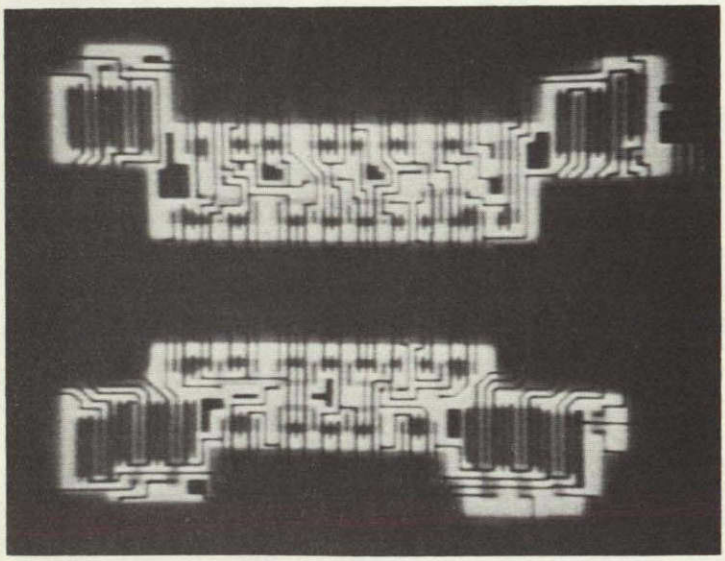


Figure 5-7. Photoresponse image of a CD4028A microcircuit obtained with V^{+}=0 V, showing the p-well/substrate junctions.

Figure 5-8 shows a representative photoresponse image obtained with V^+ = 10 V with a specimen from the reference control group. A visual comparison of photographs of these images for all the specimens, both good and reject, disclosed only subtle differences among them. The overall photoresponse level appeared to vary from specimen to specimen; however, the variations could have been caused by drift in the CRT display settings and/or the laser power output. Similarly, small differences could be seen in the grey level with which individual circuit elements had been imaged, but these differences also could have been the result of instrumental drifts.

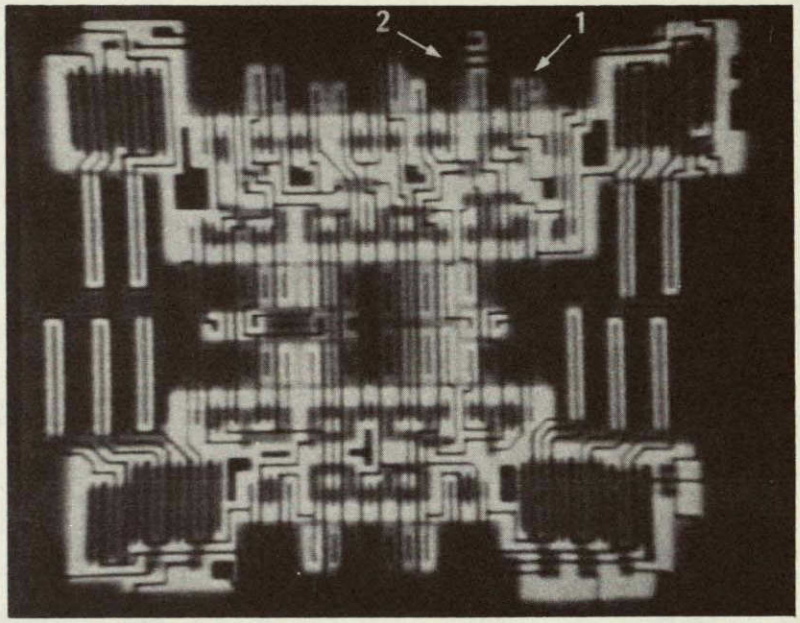
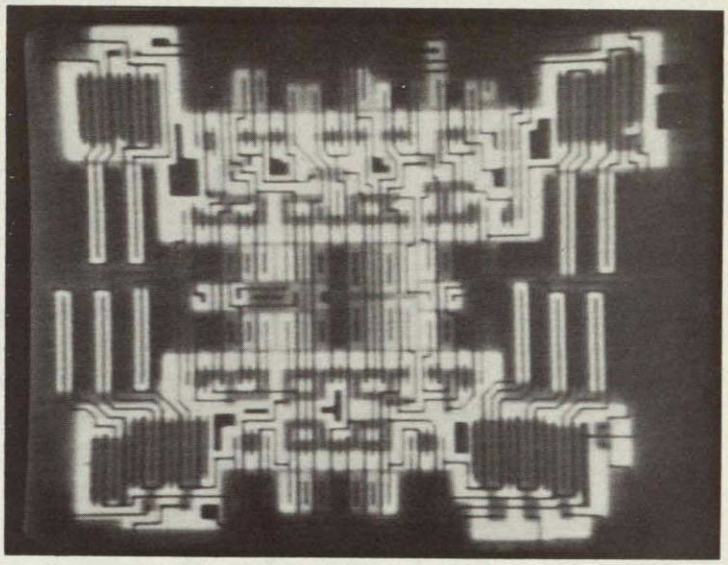


Figure 5-8. Representative state superposition photoresponse image obtained with V^+=10 V and 2.5 MHz test circuit clock frequency. The arrows labelled 1 and 2 indicate features CU-1 and CU-2 in the photoresponse image that were found to change for different specimens and for different values of V^+.

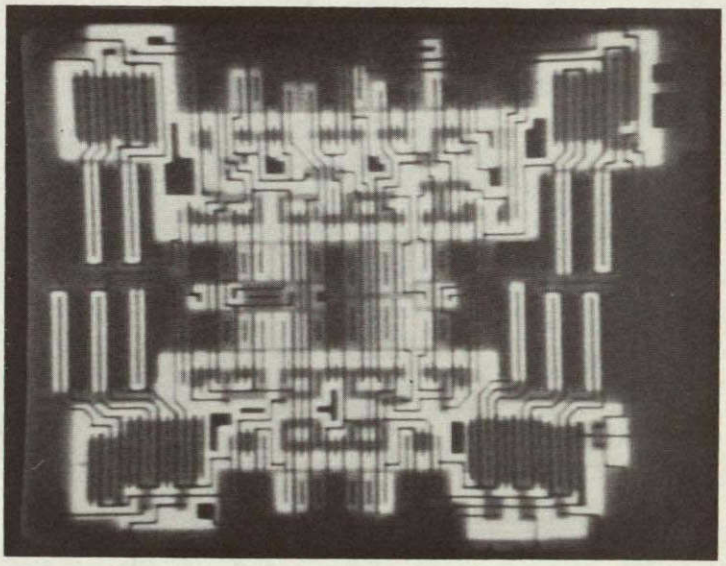
The photoresponse images recorded with V^+ = 5 V showed significant differences between specimens; comparison between 5 and 10 V photoresponse images also disclosed significant differences. Two image features that were found to vary with changes in V^+ and also between specimens are indicated by numbered arrows in Figure 5-8. (The photoresponse image in this figure was recorded with V^+ = 10 V). These two features are p diffusions in the n-substrate that are used as cross-unders, i.e., isolated conduction paths that allow one circuit conductor to cross under another. For convenience, they will be referred to as CU-1 and CU-2, in accordance with the arrow labels in Figure 5-8. CU-1 connects the outputs (i.e. drains) of FET's 1 and 2 to the gates of 56 and 53, and 36 and 33. CU-2 connects the outputs (i.e. drains) of FET's 13 and 14 to the gates of 46 and 43, 26 and 23, and 66 and 63.

One pattern of photoresponse behavior observed for CU-1 and CU-2 for several samples is as follows: for V^+ = 10 V, both CU-1 and CU-2 are imaged at about the same intensity, but for V^+ = 5 V, CU-1 becomes very dim or completely dark, while CU-2 becomes distinctly brighter. This pattern occurred only with Type 1 specimens (in which odd-numbered outputs drop out first at high frequency); it is illustrated in Figures 5-9 a and b.

In another photoresponse behavior pattern, CU-1 and CU-2 are imaged with approximately the same intensity for V^+ = 5 V and 10 V. This is illustrated in Figures 5-10 a and b. The five Type 2 specimens that had been found to have misaligned metallization all displayed this behavior, as did one Type 1 specimen that showed evidence of poorly controlled metallization delineation (see Figure 5-5b). In the third observed behavior pattern, CU-1 remains approximately the same in the transition from V^+ = 10 V to 5 V while CU-2 appears distinctly brighter. One Type 2 and four Type 1 specimens showed this behavior, which is illustrated in Figures 5-11 a and b.

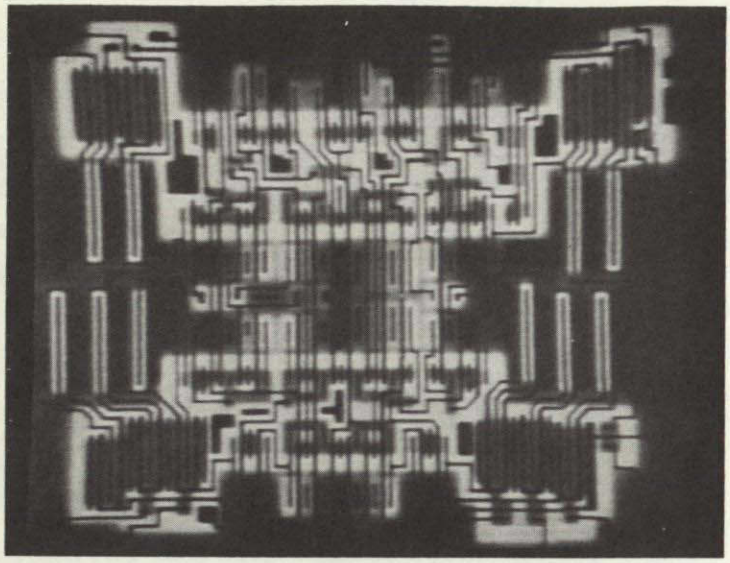


a.

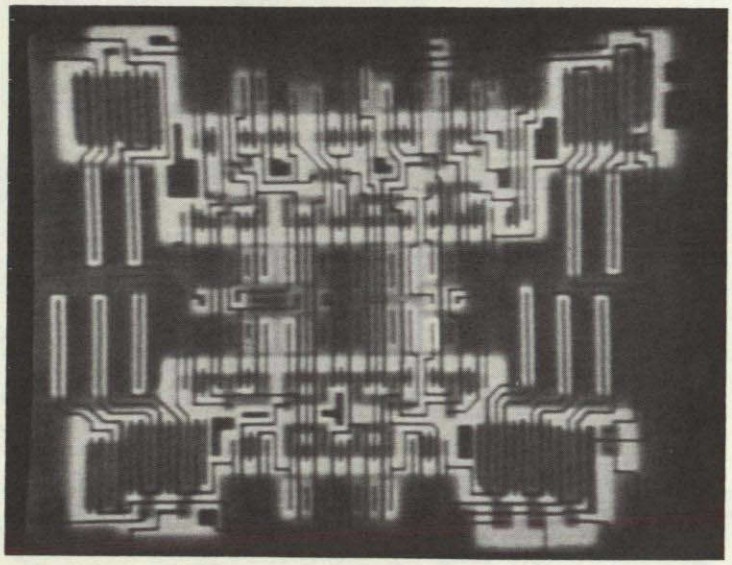


b.

Figure 5-9. Comparison of photoresponse images for $V^+ = 10$ V (a) and $V^+ = 5$ V (b), showing darkening of CU-1 and brightening of CU-2 at the lower voltage

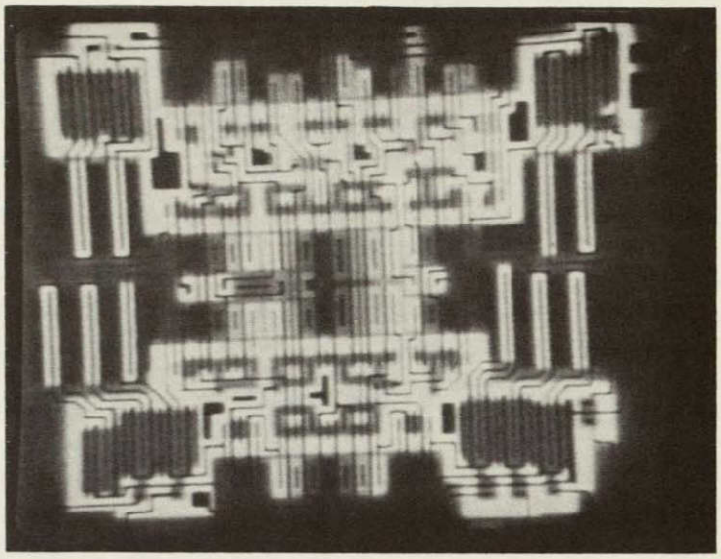


(a)

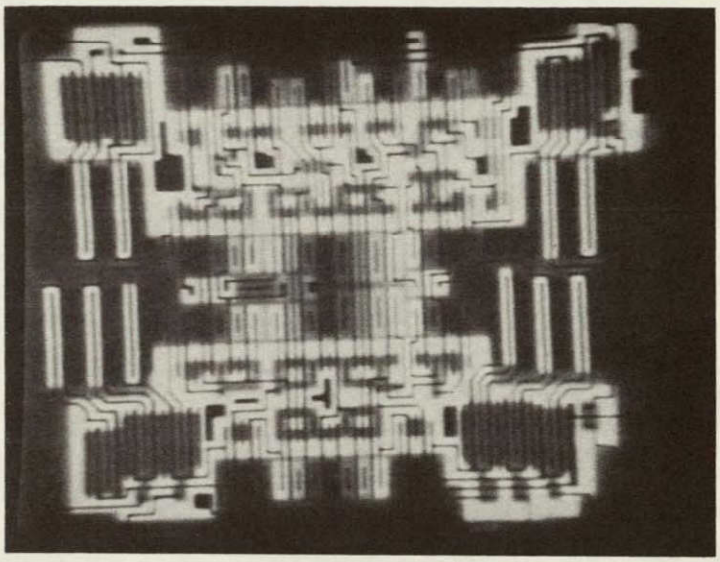


(b)

Figure 5-10. Comparison of photoresponse images for $V^+ = 10$ V (a) and $V^+ = 5$ V (b), showing CU-1 and CU-2 imaged at approximately the same intensity for the two values of V^+.



(a)



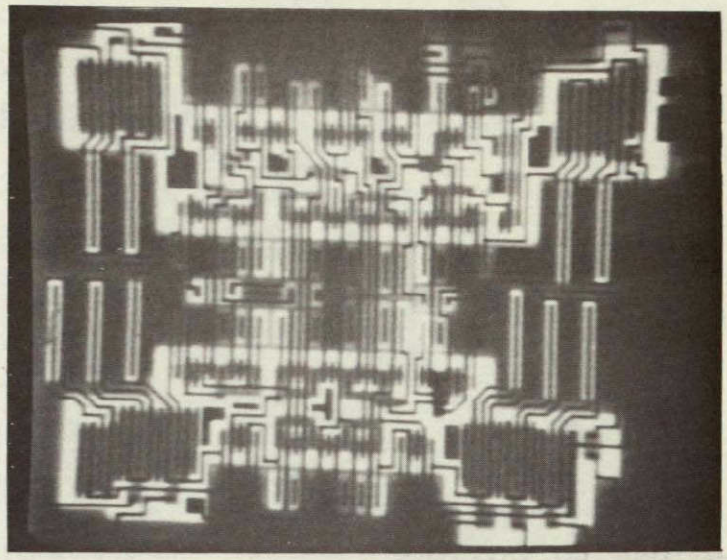
(b)

Figure 5-11. Comparison of photoresponse images for $V^+ = 10$ V (a) and $V^+ = 5$ V (b), showing CU-1 at approximately the same intensity and CU-2 brighter when V^+ is changed from 10 V to 5 V.

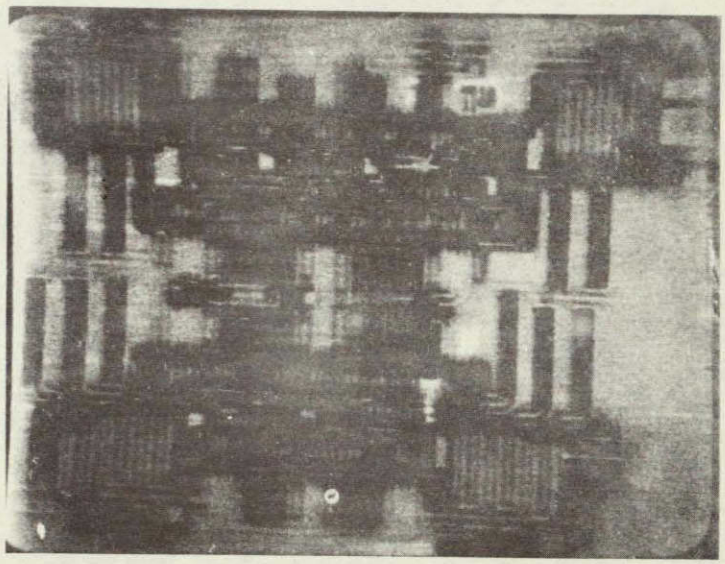
A check of the photoresponse images obtained statically with BCD input numbers 0 through 9 showed that CU-1 is imaged with odd input numbers while CU-2 is imaged with even input numbers. The appearance of a photoresponse from CU-1 with odd input numbers is explained by noting that FET 2 must be "on" to conduct the photoresponse to the external terminals. This occurs when the A input is high, i.e., when the BCD input number is odd.

The appearance of a photoresponse from CU-2 with even input numbers is explained by noting that FET 14 must be "on" to conduct the photoresponse to the external terminals. This occurs when the A input is low, i.e., when the BCD input number is even. In addition to these three behavior patterns, each of which was manifested by several specimens, other peculiarities were also evident in the photoresponse images of a few specimens. In two Type 2 specimens - one good and one reject - cross-under CU-1 appeared surrounded by a dark halo. Dark areas also appeared in these specimens at or near the drains of FET's No. 11, 116, 117, and at a cross-under connecting the drains of FET's No. 13 and 14 to the gates of 88 and 84. With the CRT video input inverted, some of these regions appeared slightly brighter than the zero signal background. These peculiarities are illustrated in Figures 5-12 a and b.

The photoresponse images of four Type 2 specimens had certain areas that appeared unusually bright. These are not very obvious in the photoresponse image photographs made with the standard settings; however, with the lock-in amplifier gain decreased by half, the bright areas are very apparent, as shown in Figures 5-13 a and b, and 5-14 a and b. The bright areas in Figure 5-13 are the source of FET No. 114 and the drain of No. 115 in the lower half of the picture, and a cross-under at the outputs (drains) of FET's No. 1 and 2 in the top half of the picture. In Figure 5-14 the bright area is the drain of FET No. 115.

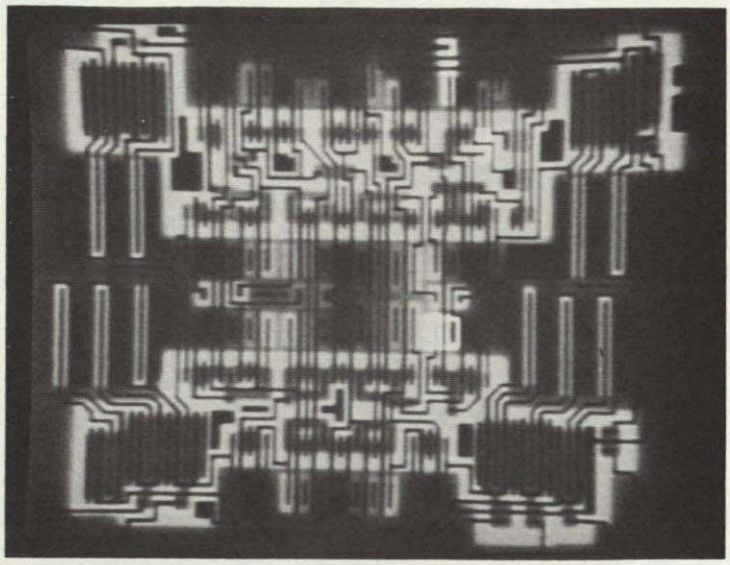


(a)

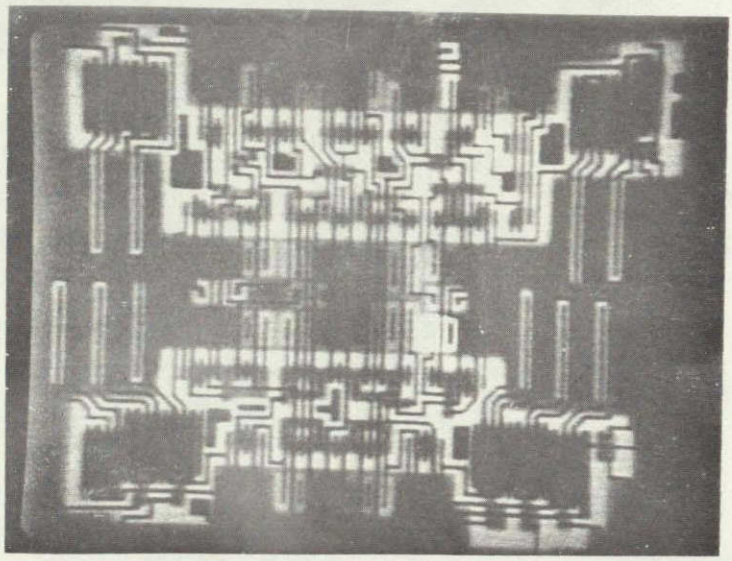


(b)

Figure 5-12. Photoresponse image of a Type 2 specimen (with $V^+ = 5$ V) with a dark halo surrounding CU-1; (a) with normal video polarity and (b) with inverted video polarity.

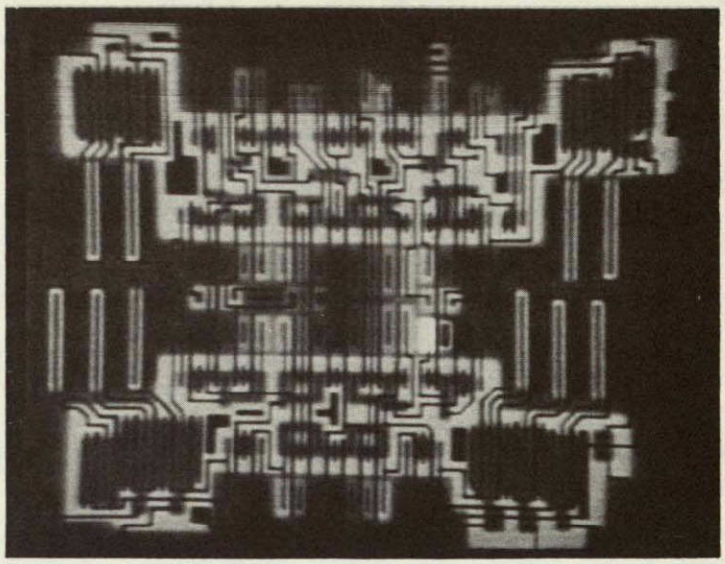


(a)

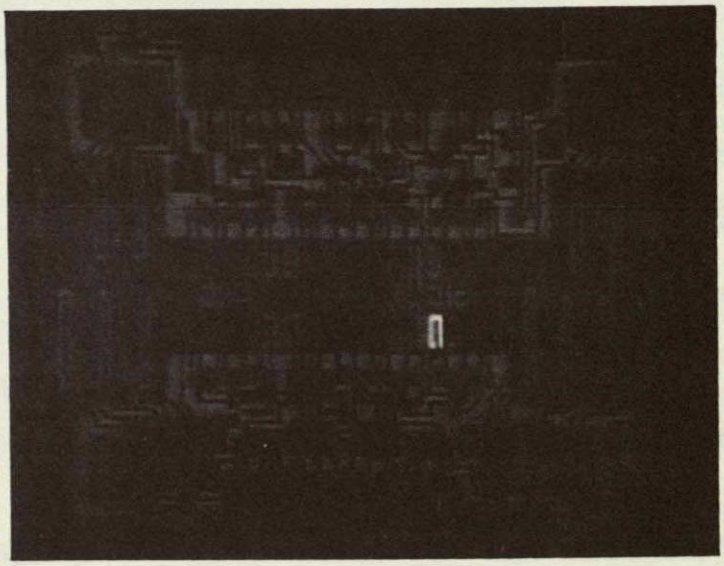


(b)

Figure 5-13. Photoresponse image of a Type 2 specimen (with $V^+ = 5$ V) having unusual, bright areas (a) with the standard video settings, (b) with the lock-in amplifier gain decreased by half.



(a)



(b)

Figure 5-14. Another example of a photoresponse image of a Type 2 specimen with areas having a high photoresponse level, (a) with standard video settings, (b) with the lock-in amplifier gain decreased by half.

As Figures 5-13b and 5-14b clearly illustrate, the abnormally bright features in the photoresponse images have a photoresponse signal level that is considerably greater than that of the p-well/substrate junction. While the photocurrent collection efficiency of the p-well/substrate junction is not 100%, the photoresponse from this function is typical of what can be expected from a CMOS microcircuit with the laser power and wavelength used for the experiments. Increased carrier collection efficiency is not an adequate explanation for the increased photoresponse level.

The occurrence of a substantially higher photoresponse suggests that certain elements in the microcircuit can amplify the photocurrent injected by the optical scanner beam. The discussion in Section 4 demonstrated that the photoresponse from a CMOS circuit stage is expected to have one polarity. The appearance of regions with photoresponse polarity opposite to that expected also suggests that the photocurrents are being amplified, but with negative gain. These types of phenomena were made much more evident in the optical scanner experiments performed at higher clock frequencies, as described below.

The results of the photoresponse image survey are summarized in Table 5-3, where the correlations among high frequency behavior, leakage current, metallization misalignment, and photoresponse image features are quite apparent.

5.6.2 Optical Scanner Examination of Dynamically Malfunctioning Microcircuits

A series of experiments was conducted to evaluate the optical scanner's ability to localize malfunctioning stages in CMOS microcircuits. As discussed in the Introduction, a malfunction in a stage of a digital microcircuit should result in a readily apparent qualitative change in the photoresponse image.

If the malfunction occurs under static conditions of operation, it can be localized without the use of the State Superposition Technique. However, if the malfunction occurs only during dynamic operation, then the State Superposition Technique is essential for localizing the malfunctioning stage.

TABLE 5-3. RESULTS OF THE PHOTORESPONSE IMAGE SURVEY (AT 2.5 MHz CLOCK FREQUENCY) FOR THE CD4028A SPECIMENS

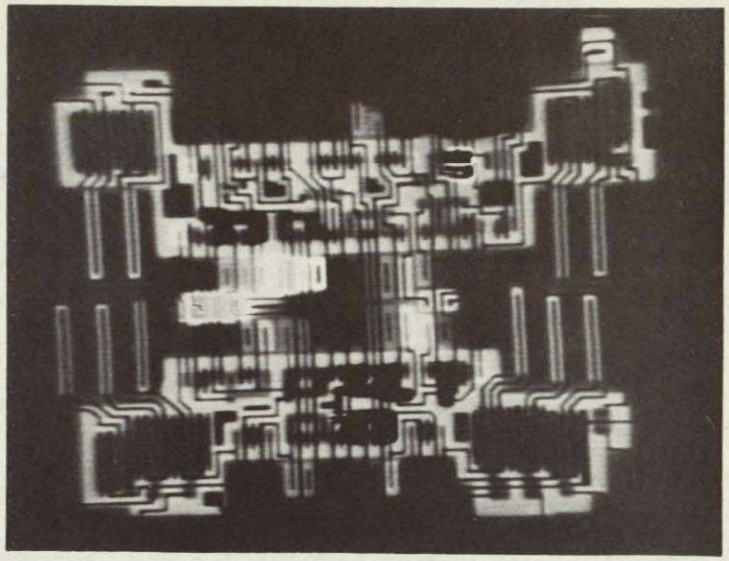
	V^+:		10 V		5 V		
	Circuit Element:		CU-1	CU-2	CU-1	CU-2	Other
Specimen Number	Type	Misaligned Metallization					
2721(G)	1		OK	OK	dK	OK+	
2724(G)	1		OK	OK	OK	OK+	
2735(G)	2	X	OK	OK	OK	OK	
2737(G)	1	X	OK	OK	OK	OK	
2738(G)	1		OK	OK	OK	OK+	
2750(G)	2		OK	OK	OK	OK+	-p region around CU-1; -p drain of FET's = 11, 117, CU near #116; +p between drains of #96 and #115
2753(G)	2		OK	OK	OK	OK+	+p at source of #114 and drain of #115; +p at CU at output of #1/2 inverter
2765(G)	1		OK	OK	V WK	OK+	
2770(G)	1		OK	OK	dK	OK+	
2772(G)	1		OK	OK	dK	OK	
2722(R)	1		OK	OK	dK	OK+	
2733(R)	2	X	OK	OK	OK	OK	
2734(R)	2		OK	OK	OK-	OK+	
2749(R)	2		OK-	OK-	OK-	OK+	-p region around CU-1; V WK -p at #11 drain; #116 and 117 drains dK; dK CU from output of #113 and 14 to gates of #84 and 88
2756(R)	2	X	OK	OK	OK	OK +	+p at drain of #115
2766(R)	1		OK	OK	V WK	OK+	
2768(R)	1		OK	OK	V WK	OK+	
2773(R)	2	X	OK	OK	OK	OK +	
2779(R)	1		OK-	OK-	OK+	OK+	
2780(R)	2	X	OK	OK	OK	OK +	+p at drain of #115

Abbreviations: "V WK" = very weak; "p" = parasitic (with ± sign indicating polarity); "OK" = light grey (in photograph, with sign indicating slightly brighter or dimmer image); CU = cross under; dK = dark.

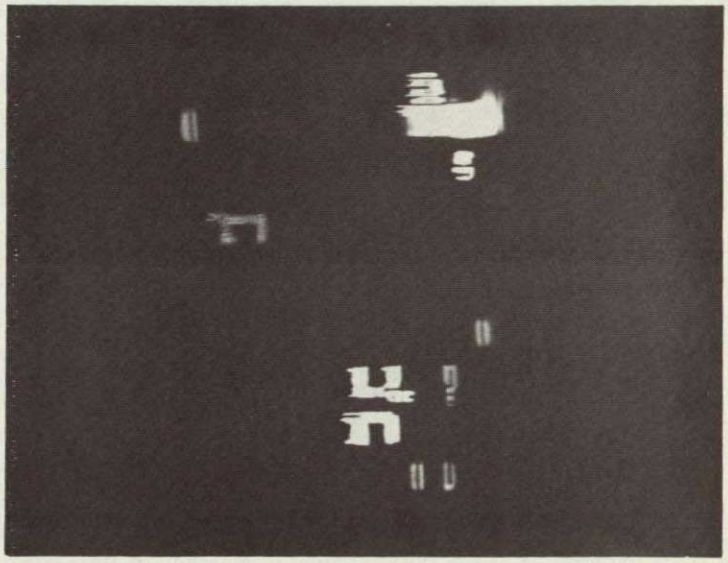
As the data in Table 5-2 indicates, dynamic malfunction could be induced in every microcircuit specimen by raising the test circuit's clock frequency to a high enough value. With an upper frequency limit of ~7.1 MHz for the test circuit itself, either all the odd or all the even outputs could be made to stop operating in every specimen. Therefore, a series of optical scanner examinations was planned that would localize the stages that stopped switching at high frequencies. The basic idea was to record a photoresponse image at each clock frequency for which an output or group of outputs of the microcircuit ceased to operate. Because of the large number of images involved, the tests were done with eight selected specimens: two good and two reject specimens for each of the two categories.

Preliminary examinations of photoresponse images at high clock frequencies showed that many regions on the microcircuits had abnormally high photoresponses of either normal or inverted polarity. The photoresponse images recorded at each output drop-out frequency were photographed separately in black and white with normal and inverted video polarity, and also superimposed by the false-color method described in the Introduction. Two kinds of false-color photographs were made. In one kind, the normal and inverted polarity images were photographed by double exposures through a green and a blue filter, respectively. In the other kind, these two color-coded, high frequency photoresponse image exposures were superimposed on the low frequency (2.5 MHz) image, which was exposed through a red filter. In effect, the low frequency images were used as references to which the high frequency images were compared in these triple-exposure photographs.

Photoresponse images were recorded in the manner just described at each of five output drop-out frequencies for the four selected Type 1 specimens. For the Type 2 specimens the frequencies at which certain outputs dropped out were so closely spaced that it was not practical to record images for each frequency. The photoresponse images were therefore recorded at only three frequencies for these specimens. A representative set of black and white photoresponse images for a Type 1 specimen is shown in Figures 5-15a through 5-15j. The corresponding set for a Type 2 specimen is shown in Figures 5-16a through 5-16f.

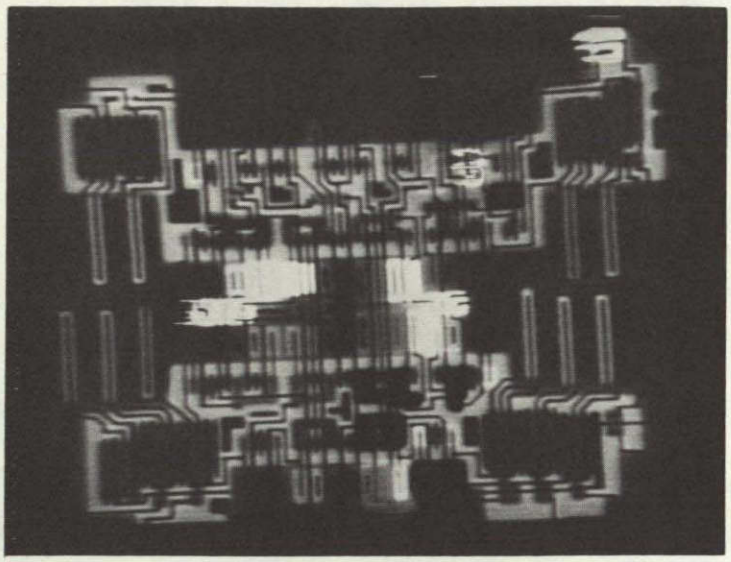


a. 5.12 MHz, Q_1 drop-out, normal video polarity

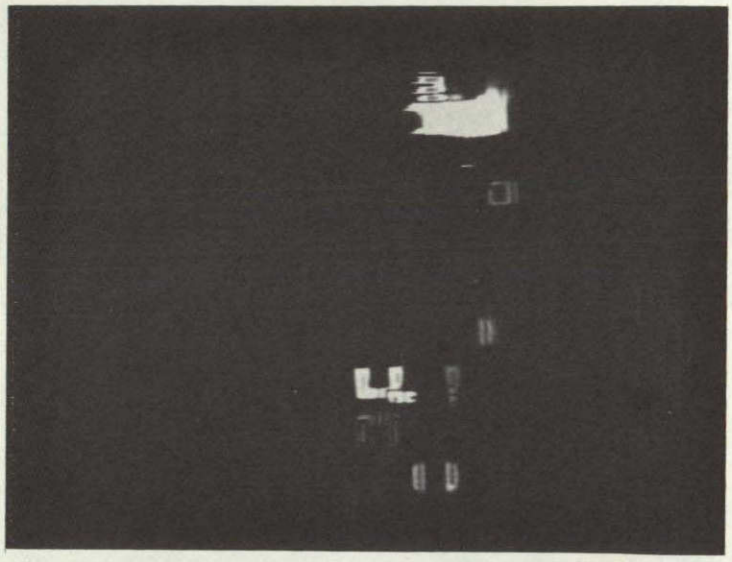


b. 5.12 MHz, Q_1 drop-out, with video polarity inverted

Figure 5-15. Photoresponse images of a (good) Type 1 specimen at the output drop-out frequencies.
(Sheet 1 of 5)

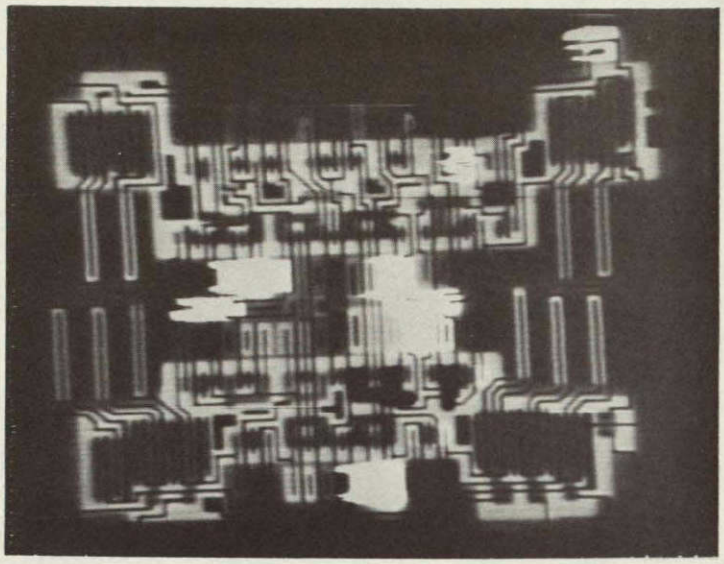


c. 5.46 MHz, Q_3 drop-out, normal video polarity

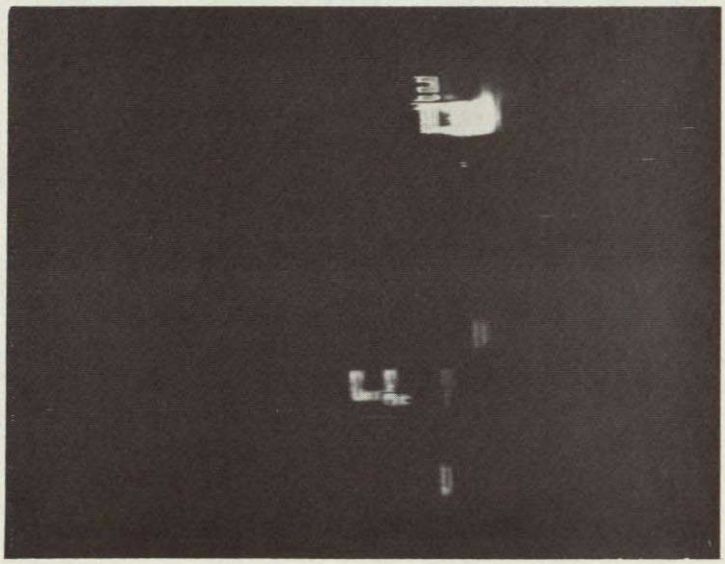


d. 5.46 MHz, Q_3 drop-out, with video polarity inverted

Figure 5-15. Photoresponse images of a (good) Type 1 specimen at the output drop-out frequencies. (Sheet 2 of 5)

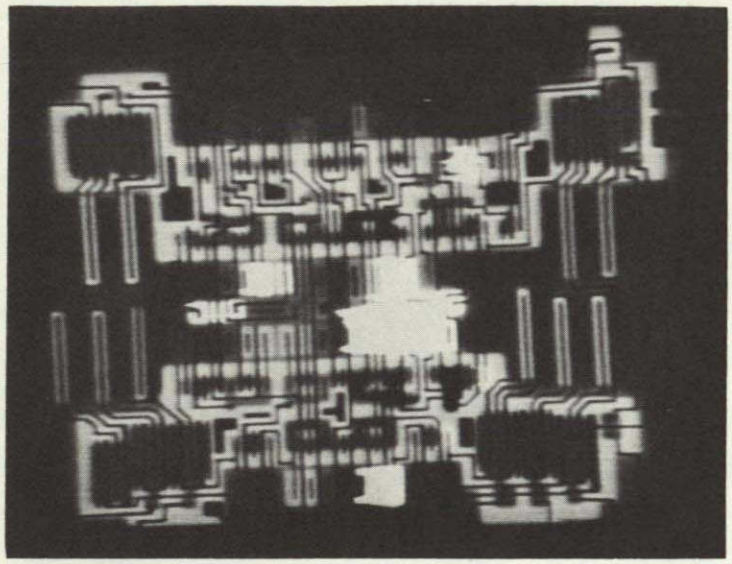


e. 5.71 MHz, Q_5 drop-out, normal video polarity

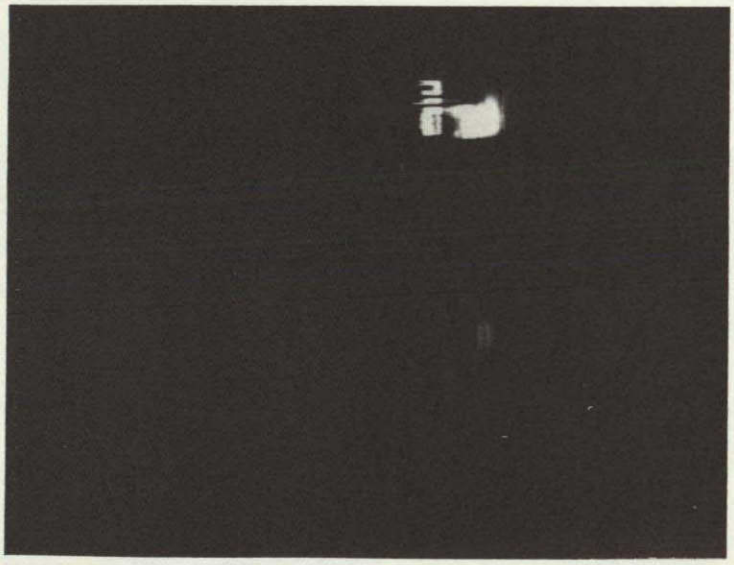


f. 5.71 MHz, Q_5 drop-out, with video polarity inverted

Figure 5-15. Photoresponse images of a (good) Type 1 specimen at the output drop-out frequencies. (Sheet 3 of 5)

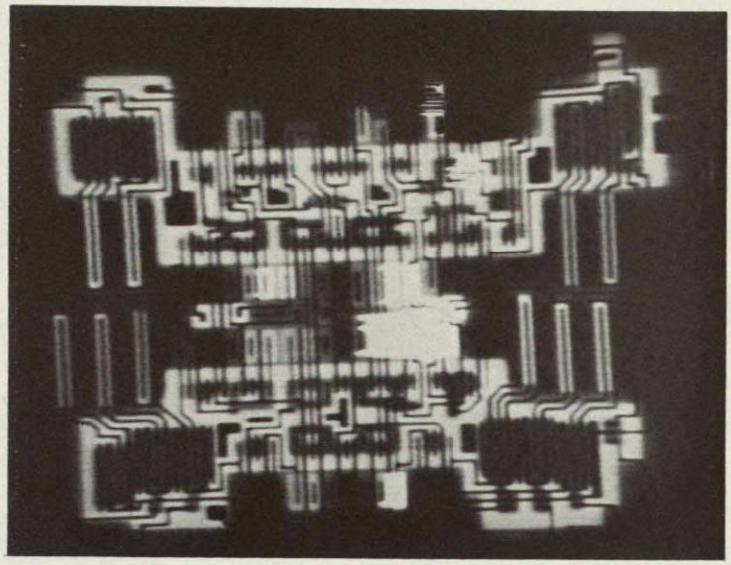


g. 5.98 MHz, Q_7 drop-out, normal video polarity

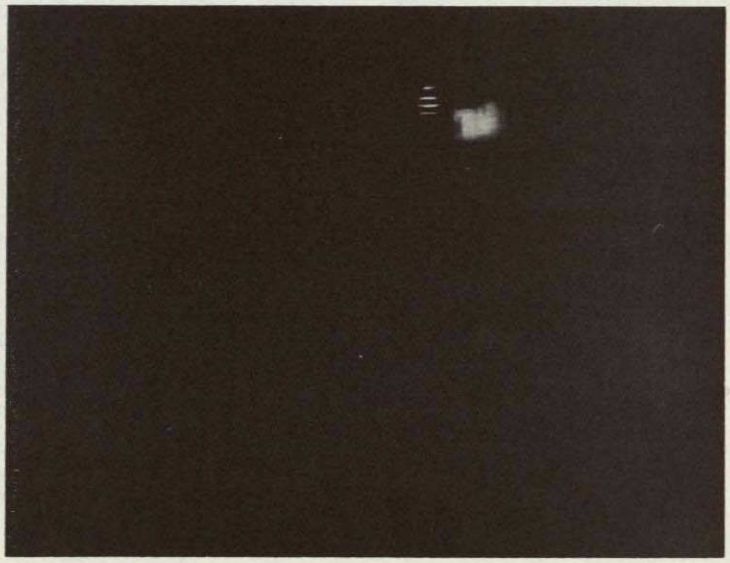


h. 5.98 MHz, Q_7 drop-out, with video polarity inverted

Figure 5-15. Photoresponse images of a (good) Type 1 specimen at the output drop-out frequencies. (Sheet 4 of 5)

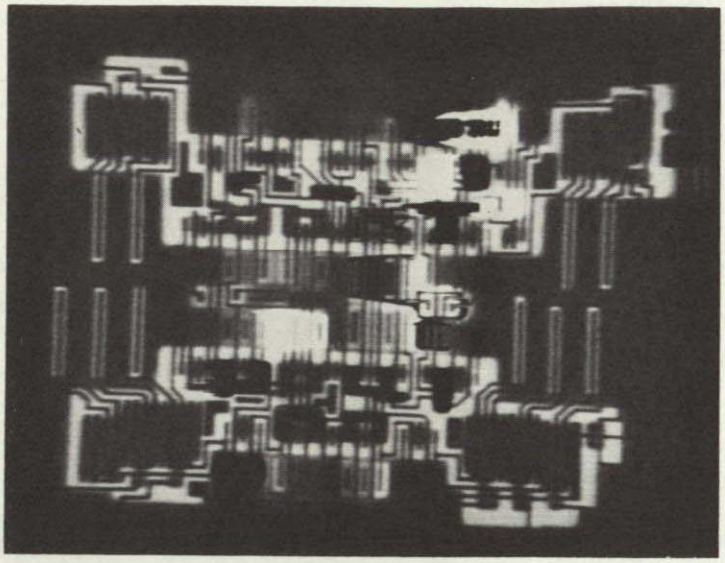


i. 6.26 MHz, Q_9 drop-out, normal video polarity

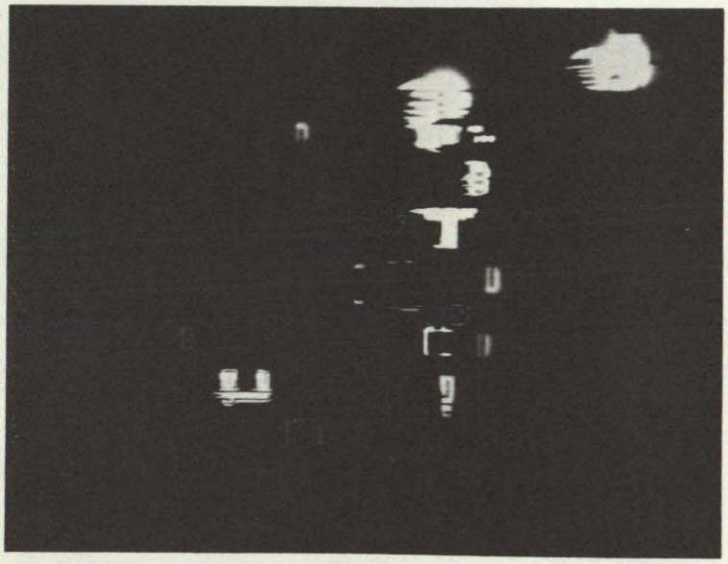


j. 6.26 MHz, Q_9 drop-out, with video polarity inverted

Figure 5-15. Photoresponse images of a (good) Type 1 specimen at the output drop-out frequencies.
(Sheet 5 of 5)

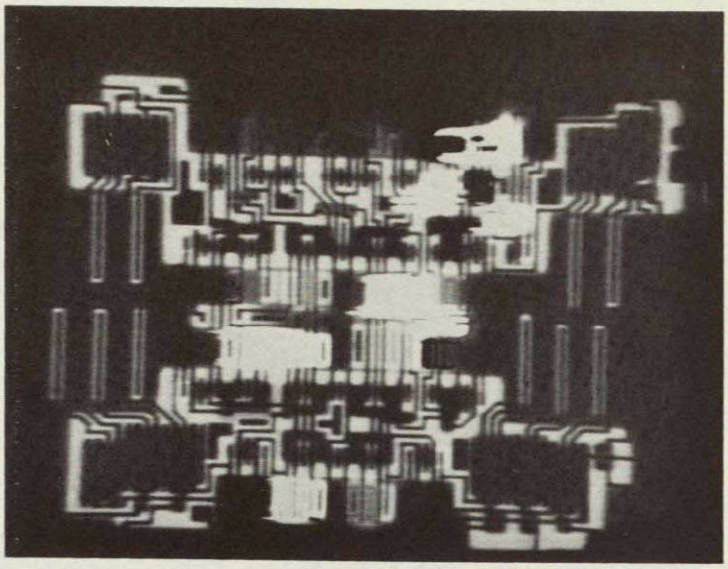


a. 5.36 MHz, Q_0 drop-out, normal video polarity

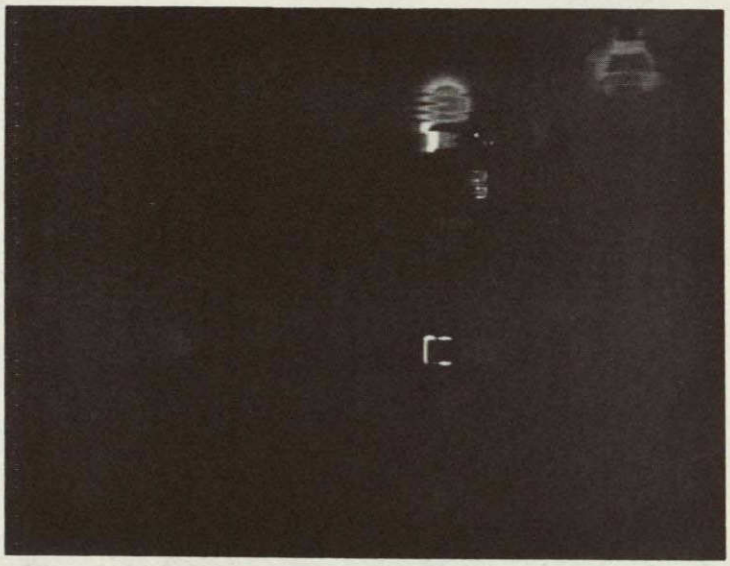


b. 5.36 MHz, Q_0 drop-out, with inverted video polarity

Figure 5-16. Photoresponse images of a (good) Type 2 specimen at the output drop-out frequencies.
(Sheet 1 of 3)

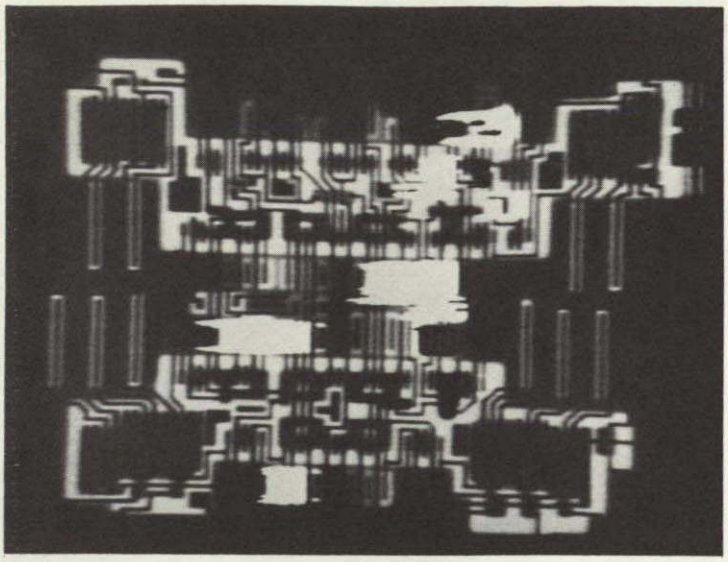


c. 5.49 MHz, Q_4 and Q_6 drop-out, normal video polarity

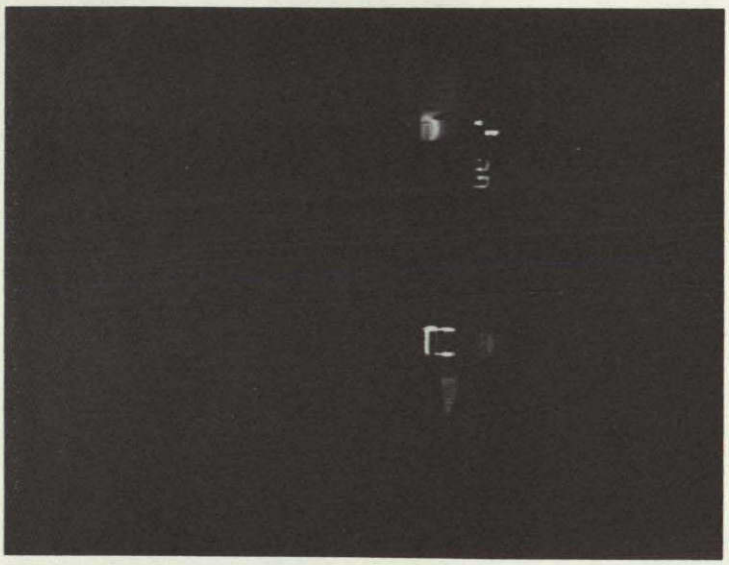


d. 5.49 MHz, Q_4 and Q_6 drop-out, with inverted video polarity

Figure 5-16. Photoresponse images of a (good) Type 2 specimen at the output drop-out frequencies. (Sheet 2 of 3)



e. 5.56 MHz, Q_2 and Q_8 drop-out, normal video polarity



f. 5.56 MHz, Q_2 and Q_8 drop-out with inverted video polarity

Figure 5-16. Photoresponse images of a (good) Type 2 specimen at the output drop-out frequencies. (Sheet 3 of 3)

The most striking features in these photoresponse images are the regions of abnormally high photoresponse of both normal and inverted polarity. The "smearing" that appears to occur in these regions in the photographs is due to the slow recovery from overload of the lock-in amplifier. The fact that the injected photocurrent is apparently amplified in the high photoresponse areas suggests that some sort of bipolar parasitic structure is doing the amplifying. If these bipolar parasitics are transistor-like, the normal polarity photoresponses result from p-n-p parasitics, and the inverted polarity photoresponses result from n-p-n parasitics. Both n-p-n and p-n-p parasitics are known to occur in CMOS microcircuits under various unusual conditions during static or quasi-static operation. For example, the latch-up that occasionally destroys transmission gates and improperly designed input circuitry is known to result from activation of parasitic bipolar transistors that interact so as to emulate a SCR. The parasitics that appear in these photoresponse images do not involve any kind of latch-up behavior. Since they are absent during static or low frequency operation, they must be due to some unidentified transient or dynamic condition that somehow activates the parasitic bipolar structures. Attempts were made to induce similar effects in a simple CMOS inverter (a MC14049B inverter/converter) by various means. It was hypothesized that the transient parasitics might be activated in inverters during the transition interval when both complementary FET's are turned on simultaneously. This idea was tested by operating the inverter with triangular and sinusoidal input waveforms with frequencies in the range of 200 kHz to 2 MHz and with $V^+ = 5$ V and 10 V. Operation with high frequency (up to 8 MHz) square waves was also tried. In no case was the parasitic behavior observed.

A careful examination was made of all the high frequency photoresponse images in order to discern some pattern in the appearance and disappearance of the parasitic amplification of the photocurrent. At the same time the images were analyzed to identify the internal stages that stopped operating when the pulses from an output or group of outputs dropped to zero. In general this identification turned out to be less obvious

than had been anticipated. Because of the presence of parasitics, a stage that stopped switching properly did not just appear the way it would have if it had been in only one static digital state. Instead it presented a totally unexpected appearance. Nevertheless by carefully correlating the electrical output behavior with the photoresponse appearance of the various circuit stages, it was possible to identify the stages that malfunctioned. It was particularly helpful that in each specimen there was a set of outputs (odd or even) with a corresponding set of internal data paths that remained fully functional throughout the range of clock frequencies covered by these tests. Thus there were images of properly operating stages available for comparison that had been photographed under exactly the same conditions as the malfunctioning stages. This minimized or eliminated such variables as CRT intensity variations, film sensitivity and color balance shifts, laser output variations, etc.

The circuits that were identified as the frequency-limiting stages are the multiple-input NOR gates that decode the individual decimal outputs. These final decode gates have two, three, or four inputs, depending on which output they decode. In the circuit's logic diagram in Figure 5-1, they appear as AND gates with inverting inputs; in the microcircuit they are implemented as conventional CMOS NOR gates as shown in the circuit diagram in Figure 5-2, with the n-channel transistors in parallel clusters and the p-channel transistors in series strings. The location of the parallel n-channel FET clusters is shown in the photoresponse image in Figure 5-17, in which the decoded decimal output numbers are used as labels. The p-channel series strings are adjacent in the n-substrate. The individual FET's can be identified by referring to the circuit diagram in Figure 5-2 and the labeled chip micrograph in Figure 5-3.

The photoresponse behavior of the decode gates in all eight test specimens is summarized in Tables 5-4 through 5-11, which also list the output pulse peak voltage for each decimal output at each test frequency. For either the output peak voltage or the photoresponse, an "OK" entry means that the observed behavior was as expected for a properly

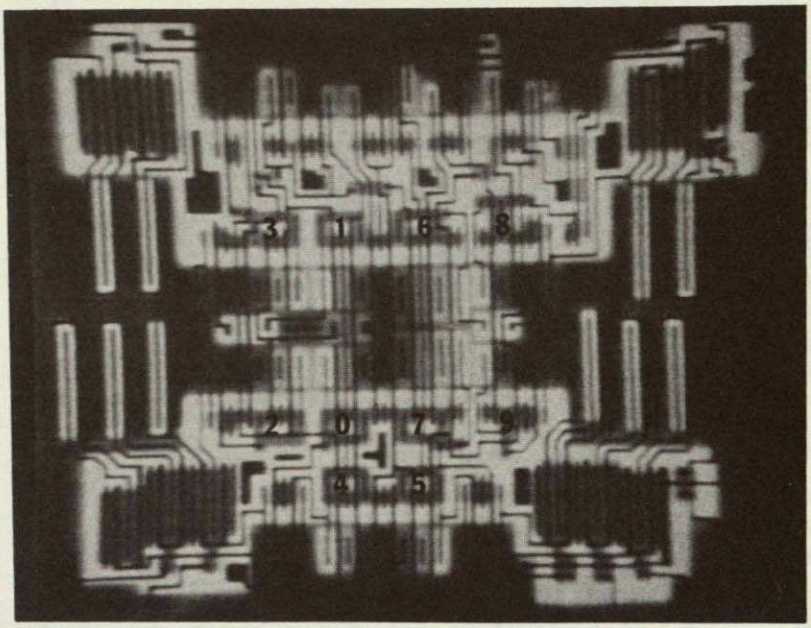


Figure 5-17. Photoresponse image of a CD4028A specimen showing the locations of the parallel n-channel FET clusters in the final decode gates.

operating circuit. (The low frequency (2.5 MHz) behavior was taken as the standard of comparison in most cases. For the photoresponse behavior, the appearance of circuitry on the test specimen known to be operating properly was also used as a reference). The photoresponse columns in the tables list the n-channel photoresponse appearance on the left of a slash ("/"), the p-channel appearance on the right. The entry "OK" with a plus or minus indicates a somewhat brighter or dimmer appearance, respectively, than the reference. The entries "+p" and "-p" indicate a parasitically amplified photoresponse of normal or inverted polarity, respectively. The appearance of parasitic amplification in the n-channel FET's in a gate always affects all the n-channel devices in the gate. A "p" was entered for parasitic behavior of the p-channel devices even when only one of the devices in the gate was involved. The following abbreviations were also used: "dk" = dark, "wk" = weak, "v wk" = very weak, and "dbl p" = double pulse. This last abbreviation refers to an abnormal double pulse observed at output #9 of three of the four Type 2 specimens. This anomaly or "glitch" occurred not only at high frequencies, for which the microcircuits malfunctioned in other ways, but also at low frequencies, for which they were otherwise fully functional.

TABLE 5-4. PHOTORESPONSE BEHAVIOR OF DECODE GATES AT OUTPUT DROP-OUT FREQUENCIES. SPECIMEN 2721

Freq. (MHz):	5.20		5.58		5.89		6.01		6.22	
Gate/Out	Out V_p	PR	Out V_p	PR	Out V_p	PR	Out V_p	PR	Out V_p	PR
0	OK	OK/OK	OK	OK/OK	OK	OK/OK	OK	OK/OK	OK	OK/OK
1	0	dk/+p	0	dk/+p	0	dk/+p	0	dk/OK	0	dk/OK
2	OK	OK/OK	OK	OK/OK	OK	OK/OK	OK	OK/OK	OK	OK/OK
3	4.0	-p/OK+	0	-p /+p (wk)	0	dk/+p	0	dk/OK	0	dk/p+
4	OK	OK/OK	OK	OK-/OK+	OK	OK/OK	OK	OK/OK	OK	OK/OK
5	OK	-p/OK	3.4	-p/OK+	0	dk/+p	0	OK-/+p	0	OK/+p
6	OK	OK/OK	OK	OK/+p	OK	dk/+p	OK	dk/+p	OK	dk/+p
7	4.0	-p/OK	2.4	-p/+p	~1.8	-p/+p	0	dk/+p	0	dk/+p
8	OK	OK/OK	OK	OK-/OK-	OK	OK/OK	OK	OK/OK	OK	OK/OK-
9	3.6	-p/-p	2	-p/+p	~1.8	-p/+p	~1.6	-p/+p	0	-p/+p
CU-1		-p		-p		-p		-p		-p
CU-2		-p		-p		-p		-p		-p (wk)
CU-3		+p (wk)		+p		+p		+p		+p (wk)

(Explanation of table entries in text)

TABLE 5-6. PHOTORESPONSE BEHAVIOR OF DECODE GATES AT OUTPUT DROP-OUT FREQUENCIES. SPECIMEN 2722

Freq. (MHz):	5.52		5.80		5.96		6.36		6.56	
Gate/Out	Out V_p	PR	Out V_p	PR	Out V_p	PR	Out V_p	PR	Out V_p	PR
0	OK	OK-/OK	OK	OK/OK	OK	OK/OK	OK	OK/OK	OK	OK/OK
1	0	dk/+p	0	dk/+p	0	dk/+p	0	dk/OK	0	dk/OK
2	OK	OK/OK	OK	OK/OK	OK	OK+/OK	OK	OK/OK	OK	OK/OK
3	2.8	-p/+p	0	-p /+p (v wk)	0	dk/+p	0	dk/+p	0	dk/+p
4	OK	OK-/OK	OK	OK/OK	OK	OK/OK+	OK	OK-/OK+	OK	OK/OK+
5	4.4 (narrow pulse)	-p/OK-	1.6	-p /+p (v wk)	0	dk/+p	0	OK/+p	0	OK/+p
6	OK	OK/OK	OK	OK/+p	OK	dk/+p	OK	dk/+p	OK	OK-/+p
7	4.4 (very narrow pulse)	-p/OK	3.8	-p/OK	3.2	-p/OK+	0	dk/+p	0	dk/+p
8	OK	OK/OK	OK	OK-/OK-	OK	OK-/OK+	OK	OK/OK-	OK	OK/dk
9	3.6	-p/+p	2	-p/+p	1.6	-p /+p (wk)	~1.2	-p /+p (v wk)	0	-p /+p (v wk)
CU-1		-p		-p		-p		-p		-p (wk)
CU-2		-p		-p		-p		±p (wk)		+p (wk)
CU-3		+p		+p		+p		+p (wk)		+p (wk)

(Explanation of table entries in text)

TABLE 5-7. PHOTORESPONSE BEHAVIOR OF DECODE GATES AT OUTPUT DROP-OUT FREQUENCIES. SPECIMEN 2734

Freq. (MHz):	5.26		5.49		5.77		5.89		6.02	
Gate/Out	Out V_p	PR	Out V_p	PR	Out V_p	PR	Out V_p	PR	Out V_p	PR
0	OK	dk/OK-	OK	OK/OK-	OK	OK/OK-	OK	OK/OK	OK	OK/OK
1	0	dk/+p	0	dk/+p	0	dk/+p	0	dk/+p	0	dk/OK
2	OK	OK/OK	OK	OK/OK-	OK	OK/OK	OK	OK/OK	OK	OK/OK
3	1.6	-p /+p (v wk)	0	dk/+p	0	dk/+p	0	dk/+p	0	dk/+p
4	OK	OK-/OK+	OK	OK-/OK+	OK	OK/OK+	OK	OK/OK+	OK	OK/OK+
5	OK	-p/OK	3.8	-p/+p (wk)/(wk)	0.4	dk/+p	0	dk/+p	0	OK-/+p
6	4.9 (narrow pulse)	OK+/OK+	OK	OK/+p	OK	dk/+p	OK	dk/+p	OK	dk/+p
7	3.2	-p/OK+	2	-p/OK (wk)/+	1.8	-p /+p (v wk)	0	dk/+p	0	dk/+p
8	OK	OK/OK	OK	OK/OK-	OK	OK/OK-	OK	OK/OK	OK	OK/OK-
9	2	-p/+p (wk)/(wk)	2	-p /+p (wk)	1.6	-p /+p (v wk)	$\lesssim$1.2	-p /+p (v wk)	0	-p /+p (v wk)
CU-1		-p		-p		-p		-p		-p
CU-2		-p		-p		-p(wk)		-p(wk)		-p(wk)
CU-3		+p		+p		+p		+p		+p(wk)

(Explanation of table entries in text)

TABLE 5-8. PHOTORESPONSE BEHAVIOR OF DECODE GATES AT OUTPUT DROP-OUT FREQUENCIES. SPECIMEN 2750

Freq. (MHz):	5.36		5.49		5.56	
Gate/Out	Out V_p	PR	Out V_p	PR	Out V_p	PR
0	0	dk/+p	0	dk/+p	0	dk/+p
1	OK	OK-/OK	OK	OK-/OK	OK	OK-/OK
2	3.6	-p/OK	2	OK-/+p	0	OK-/+p
3	OK	OK-/OK	OK	OK-/OK	OK	OK-/OK
4	2.4	-p(wk)/OK	0.5	dk/+p	0	OK-/+p
5	OK	-p(vwk)/OK	OK	OK-/+p(wk)	OK	OK-/OK
6	1.8	-p(vwk)/-p(vwk)	≤0.8	OK-/+p	0	OK-/+p
7	OK	-p(wk)/+p(wk)	~3.4	dk/+p(wk)	OK	dk/OK
8	3.6	-p/+p(wk)	3.2	dk/+p(wk)	0	OK/+p
9	(dbl p)	-p/-p	(dbl p)	dk/-p	(dbl p)	-p/-p
CU-1		+p		+p		+p
CU-2		-p		-p(wk)		-p(wk)
CU-3		-p		-p(wk)		dk

(Explanation of table entries in text)

TABLE 5-9. PHOTORESPONSE BEHAVIOR OF DECODE GATES AT OUTPUT DROP-OUT FREQUENCIES. SPECIMEN 2753

Freq. (MHz):	4.25		4.43		4.52	
Gate/Out	Out V_p	PR	Out V_p	PR	Out V_p	PR
0	0	OK-/+p	0	dk/+p	0	OK-/+p
1	OK	OK-/OK	OK	OK-/OK	OK	OK-/OK
2	4	-p/OK	<1.6	OK-/+p	0	OK-/+p
3	OK	OK/OK	OK	OK-/OK	OK	OK-/OK
4	3.2	-p/OK	0	OK-/+p	0	OK-/+p
5	OK	OK-/OK	OK	OK-/OK	OK	OK-/OK
6	2.8	-p(vwk)/+p(vwk)	0	OK-/+p	0	OK-/+p
7	OK	dk/OK	OK	dk/OK	OK	dk/OK
8	4	-p/OK	2	OK/+p	0	OK-/+p
9	(dbl p)	-p/-p	(dbl p)	dk/-p	(dbl p)	-p(wk)/-p
CU-1		+p		+p		+p
CU-2		-p		-p(vwk)		-p(vwk)
CU-3		-p		-p(vwk)		-p(vwk)

(Explanation of table entries in text)

TABLE 5-10. PHOTORESPONSE BEHAVIOR OF DECODE GATES AT OUTPUT DROP-OUT FREQUENCIES. SPECIMEN 2749

Freq. (MHz):	5.69		5.78		5.94	
Gate/Out	Out V_p	PR	Out V_p	PR	Out V_p	PR
0	0	OK-/+p	0	OK-/+p	0	OK/+p
1	OK	OK-/OK	OK	OK-/OK+	OK	OK-/OK
2	2.6	-p(vwk)/OK+	0	OK-/+p	O	OK/+p
3	OK	OK-/OK	OK	OK-/OK	OK	OK-/OK
4	0	OK-/+p	0	OK-/+p	0	OK/+p
5	OK	OK-/OK	OK	OK-/OK+	OK	OK/OK
6	1.6	OK-/-p(vwk)	0	OK-/+p	0	OK/+p
7	OK	dk/OK	OK	OK-/OK+	OK	dk/OK
8	3.8	-p/+p	$\lesssim$ 1.2	dk/+p	0	OK/+p
9	(dbl p)	-p(vwk)/-p(wk)	(dbl p)	dk/-p	(dbl p)	dk/-p
CU-1		+p		+p		+p
CU-2		-p		-p(wk)		-p(vwk)
CU-3		-p		-p(vwk)		dk

(Explanation of table entries in text)

TABLE 5-11. PHOTORESPONSE BEHAVIOR OF DECODE GATES AT OUTPUT DROP-OUT FREQUENCIES. SPECIMEN 2780

Freq. (MHz):	5.50		5.58		5.68	
Gate/Out	Out V_p	PR	Out V_p	PR	Out V_p	PR
0	0	OK-/+p	0	OK/+p	0	OK/+p
1	OK	OK-/OK	OK	OK-/OK	OK	OK-/OK
2	3.6	-p(vwk)/+p	0	OK/+p	0	OK/+p
3	OK	OK-/OK	OK	OK-/OK	OK	OK-/OK
4	1.2	OK/+p	0	OK/+p	0	OK/+p
5	OK	OK/OK	OK	OK/OK	OK	OK/OK
6	< 1	OK/+p	0	OK/+p	0	OK/+p
7	OK	dk/+p	OK	OK/OK	OK	dk/OK
8	4.6	-p/+p	4	OK-/+p	0	OK/+p
9	OK	OK/+p	OK	OK-/-p(vwk)	OK	OK/±p
CU-1		+p		+p		+p
CU-2		-p		-p(wk)		-p(vwk)
CU-3		-p		-p(vwk)		dk

(Explanation of table entries in text)

In addition to photoresponse information on the decode gate FET's, the tables also list the photoresponse behavior of three diffused cross-unders. CU-1 and CU-2 were identified previously in Figure 5-8. CU-3 is the diffused resistor that forms part of the pin 10 (input A) protection network.

The most general statement that can be made concerning the incidence of parasitic amplification of the photocurrent is that it occurs as the maximum operating frequency of the circuitry is approached and passed. Each of the specimens had one set of outputs (even for Type 1 specimens, odd for Type 2 specimens) that remained fully functional while the other set of outputs dropped out with increasing frequency. No parasitics were observed in the final decode gates for these outputs. The parasitics that were observed in the decode gates and other circuitry associated with failing outputs did not suddenly appear just as the output pulse height began to decrease with increasing frequency. Though not shown in the set of images being considered here, many parasitics appeared at frequencies well below those at which the outputs began to drop out. Some of these parasitics first began to appear in the photoresponse images recorded with 2.5 MHz clock frequency, approximately half the frequency at which the outputs typically dropped out.

As shown in Tables 5-4 through 5-7, the odd-numbered outputs of the Type 1 specimens failed in increasing numerical order with increasing clock frequency. The general trend in the photoresponse behavior, followed in the majority of cases, was as follows: as the output drop-out frequency was approached, the decode gates' n-channel FET cluster manifested an amplified photoresponse of inverted polarity while the p-channel FET's appeared normal. When the output drop-out frequency was reached, the n-channel FET's appeared dark, indicating that one or more of them was always "on"; at the same time, the p-channel FET's had an amplified photoresponse of normal polarity. Further increase in the operation frequency eventually led to a photoresponse image with the n-channel FET's dark and the p-channel FET's imaged with a non-amplified (i.e., normal)

brightness level - exactly as expected for a nonfunctioning NOR gate. The two main exceptions to the trend involved the decode gates for outputs 6 and 9. The decode gate for output 6 presented the appearance of a gate with a failing output (n-channel FET's dark, p-channel FET's with amplified photoresponse) although the output pulses appeared normal. This behavior may be related to the electrical test result that consistently showed the propagation time to output #6 to be the longest for all specimens. The trend for the output #9 decode gate was for the n-channel FET's to have an amplified photoresponse of inverted polarity and for the p-channel FET's to have an amplified photoresponse of normal polarity. Unlike the other decode gates, the #9 gate has a diffused cross-under within it that connects the output to the gates of FET's #118 and 119. Diffused diodes, resistors, and cross-unders elsewhere in the chip manifested parasitic amplification of both polarities; the presence of the cross-under in the #9 gate therefore can be expected to make this gate's high frequency photoresponse atypical.

The results for the Type 2 specimens, listed in Tables 5-8 through 5-11, showed similar trends. The images of the n-channel FET's in the final decode gates are considerably dimmer than for the Type 1 specimens even when these gates are functioning normally. The darkening of the n-channel FET's images when the gates stopped functioning therefore was not as obvious as with the Type 1 specimens. The entries in the photoresponse columns of the tables accordingly denote the photoresponses of the (presumably) nonfunctioning n-channel FET's as "OK-" instead of "dk". The output pulses from all of the outputs of the Type 2 specimens were of somewhat shorter duration than for the Type 1 specimens, and they had more of a triangular than a rectangular shape. The darker appearance of the n-channel decode gate FET's could reflect an internal duty cycle difference that would also result in the different pulse shape for the Type 2 specimens.

The tables show that three of the four Type 2 specimens had an anomalous double pulse "glitch" in the #9 output. The photoresponse behavior of the #9 decode gate is similar for these three specimens, but

differs from that observed in the Type 1 specimens. In the Type 2 specimen without the double pulse anomaly (#2780), the #9 decode gate's photoresponse behavior differed from that of the other seven specimens. Although these results do not establish a causal relationship, they do show that the double pulse output and the different photoresponse appearance are correlated.

The photoresponse behavior pattern of the three diffused cross-unders listed in the tables is quite consistent within each category (Type 1 or Type 2), but it differs for the two categories. Cross-under CU-2's photoresponse behavior was essentially the same for all eight specimens: its photoresponse has inverted polarity, and it becomes weaker at higher frequency. In one Type 1 specimen (#2722) the photoresponse polarity reversed at high frequency. The photoresponse polarity for CU-1 was consistently inverted in the Type 1 specimens and normal in the Type 2 specimens. For CU-3 the photoresponse polarity was inverted in the Type 2 specimens and normal in the Type 1 specimens. The behavior of CU-3 is particularly interesting in that this cross-under connects input A to the rest of the circuitry. Input A is the least significant digit for the BCD input number. A is high for odd numbers and low for even numbers. Any frequency-dependent phenomenon that would diminish this input signal in some specimens but not others could account for the Type 1 and Type 2 categories of electrical behavior. Since the mechanism that produces the parasitic amplification of photocurrent is not understood, a causal relationship cannot be established. However, the results do show that the photoresponse behavior of the diffused cross-unders is well correlated with the specimens' electrical behavior.

5.7 EVALUATION OF THE SILICON-DIELECTRIC INTERFACE BY A PHOTOCURRENT TRANSPORT METHOD

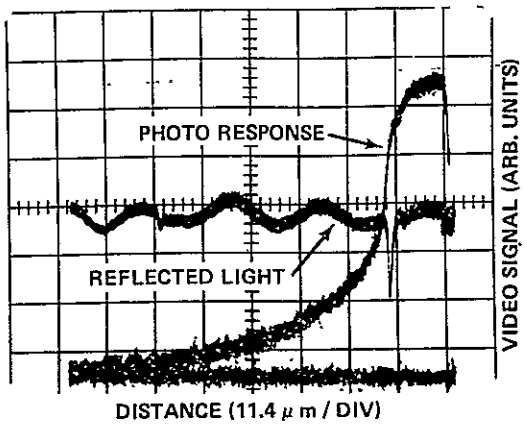
The power supply current of a CMOS device in a static digital state is essentially a leakage current. One component of the total leakage current is a surface current, and it is precisely this component that tends to increase when the microcircuit is powered and sometimes leads to parametric failure. The changes in surface conditions that accompany

surface current changes can be expected to affect the transport along the surface of optically injected carriers. In particular, the rate at which the photoresponse drops off as the optical spot moves away from a p-n junction will be significantly affected by surface conditions. Experiments were performed on eleven CD4028A specimens to observe and quantify such effects and to correlate the results with leakage current measurements.

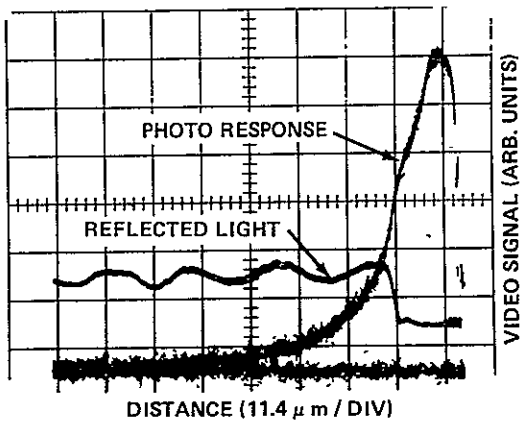
Individual photoresponse line-scans were made across a portion of the p-well/substrate junction in the vicinity of FET No. 60. A 40 x long-working-distance objective with a numerical aperture of 0.55 was used. Both the photoresponse and the reflected light line scan traces were photographed together on the waveform monitor oscilloscope. A step in the oxide that probably resulted from fabrication of the p-well could be seen as a notch or step in the reflected light scan. This was used to approximate the location of the metallurgical junction. Due to lateral diffusion of the p-well dopant, the actual location of the junction is probably displaced from the step by a couple of micrometers. A line scan with the laser beam blocked was also photographed to indicate the zero of the photoresponse scale. The horizontal scale on the waveform monitor was calibrated using the 0.02 mm lines on an AO stage micrometer. A scale factor of 11.4 μm per horizontal division was obtained. The length of the scan on the specimen was 95 μm, which was traversed in 0.1 sec by the focused spot of light.

The photoresponse line scans were recorded for four good and two reject Type 1 specimens and three good and two reject Type 2 specimens. Quantitative data on the n (substrate) side of the junction were obtained by direct measurements on the oscilloscope photographs. At least four points were measured for each specimen and fitted with an expression of the form $I(x) = I(o)\, e^{-x/L}$. The parameter L is essentially an effective diffusion length for transport along the silicon-dielectric interface.

A photoresponse line-scan for a good Type 1 specimen is shown in Figure 5-18a; the fitted value of L is 23.1 μm. The corresponding photograph for a Type 2 specimen is shown in Figure 5-18b; the fitted value



a. For a good type 1 specimen; fitted value of L = 23.1 μm



b. For a good type 2 specimen; fitted value of L = 14.0 μm

Figure 5-18. Photoresponse line-scans.

of L is 14.0 μm. The complete set of fitted L values and of static current consumption measurements is listed in Table 5-12. Two of the Type 2 specimens listed in the table had misaligned metallization; they are designated by an asterisk.

TABLE 5-12. EFFECTIVE DIFFUSION LENGTHS FITTED TO PHOTORESPONSE LINE SCANS

	Specimen Number	I_o, (div)	L (μm)	I_{ss}	2	3	4	5	6	7	8	9	10
Type 1	2721G	2.93	19.75	700pA	350pA	550pA	350pA	700pA	150pA	1050pA	-50pA	1000pA	-100pA
	2724G	3.30	20.53	1050pA	700pA	850pA	650pA	950pA	500pA	1350pA	350pA	1350pA	250pA
	2737G	2.74	23.10	1035pA	1100pA	650pA	1150pA	950pA	1050pA	1350pA	900pA	1250pA	450pA
	2738G	2.40	19.07	250pA	500pA	1050pA	550pA	950pA	850pA	1000pA	1350pA	600pA	1300pA
	2722R	3.80	25.98	150pA	150pA	1050pA	1.095μA	271.5μA	800pA	950pA	500pA	1050pA	250pA
	2734R	2.95	23.90	44.60μA	44.10μA	43.95μA	650pA	44.10μA	43.80μA	43.95μA	43.75μA	43.85μA	43.75μA
			$\langle L \rangle = 22.1$, $\sigma = 2.46$										
Type 2	2735G*	2.94	15.10	9.035μA	9.030μA	9.075μA	9.040μA	9.040μA	9.045μA	9.055μA	9.050μA	9.065μA	9.055μA
	2750G	2.53	13.99	8.910μA	8.920μA	8.955μA	8.920μA	8.920μA	8.920μA	8.930μA	8.920μA	8.935μA	8.925μA
	2753G	2.77	22.78	6.995μA	6.960μA	6.990μA	6.965μA	6.970μA	6.965μA	6.975μA	6.970μA	6.980μA	6.975μA
	2749R	3.08	16.95	19.75μA	19.75μA	19.80μA	19.75μA	19.75μA	19.75μA	19.75μA	19.75μA	19.75μA	19.75μA
	2780R*	2.24	21.15	12.55μA	12.55μA	12.60μA	12.55μA	12.55μA	12.55μA	12.55μA	12.55μA	12.55μA	12.55μA
			$\langle L \rangle = 18.0$, $\sigma = 3.41$										

*These samples had misaligned metallization.

The values of L listed in the table are not well correlated with the measured current values. However, it should be noted that for every Type 1 specimen there is at least one input BCD number that results in a current reading $\lesssim 0.7$ nA. This would not occur if the surface leakage component were large and fairly uniformly distributed over the surface of the microcircuit. The implication is that in Type 1 specimens with high leakage currents, the excess leakage is a localized phenomenon and most of the microcircuit has a low level of leakage current. Conversely, the high value of leakage current of Type 2 microcircuits varies little with the BCD input data. Presumably the surface leakage in these microcircuits is widely distributed over the chip. The periphery of the p-well/substrate junction is a likely location for surface leakage. In specimens with misaligned metallization the leakage could occur through the FET channels. However, in specimens for which a substantial fraction of the leakage occurs across the p-well/substrate junction periphery, it was anticipated that a substantially different value of L would be measured.

The results listed in Table 5-12 show that the Type 1 specimens had an average L = 22.1 μm with a mean deviation $\sigma = 2.46$ μm. For the Type 2 specimens the average L is 18.0 μm, with a mean deviation $\sigma = 3.41$ μm. These results have been interpreted as showing that, for the leakage processes occurring in these specimens, a longer value of L is a necessary but not sufficient condition for low leakage. This interpretation is consistent with the idea that a high surface recombination velocity would both shorten the observed value of L and increase the surface leakage. The data presented here apply only to conditions over the n-substrate. Substantial differences in the shape of the photoresponse line-scan traces could be seen over the p-well (see Figures 5-18a and b), but no attempt was made either to measure them or to interpret them qualitatively.

5.8 SUMMARY OF RESULTS FOR THE CD4028A MICROCIRCUITS

The results of the optical scanner examinations were found to correlate significantly with results of automated and manual electrical tests. The automated tests indicated that both the good and reject test specimens could be placed in one of two categories - Type 1 and Type 2 - depending on the input BCD number's influence on the static current consumption. The specimens' behavior at high clock frequencies in the State Superposition test circuit was well correlated with this separation into two categories. In the Type 1 circuits the odd-numbered outputs' signals dropped out in increasing numerical order as the clock frequency was increased, while the even-numbered outputs remained unaffected. In the Type 2 circuits it was the even-numbered outputs that failed with increasing clock frequency.

The visual examination of the microcircuit chips disclosed only one kind of anomaly - misaligned metallization - that could partly account for the observed electrical behavior. Misaligned metallization could cause increased leakage current by allowing ionic contamination of the gate oxide. This anomaly occurred primarily in Type 2 specimens.

The photoresponse images had many features that were correlated with the electrical behavior pattern. With a 2.5 MHz clock frequency (for which all devices were fully functional), it was found that the absence of a photoresponse from one diffused cross-under at $V^+ = 5$ V occurred in Type 1 specimens only. At the high clock frequencies for which the specimens malfunctioned, the photoresponse images manifested parasitic amplification of the photocurrent in many locations; moreover, it was possible to determine which circuit stages caused the output signals to disappear or drop out. In general, it was observed that the appearance of parasitic behavior in the n-channel FET's of NOR gates was a precursor of high frequency malfunction. The pattern of parasitic behavior and high frequency failure of NOR gates was quite consistent within each of the two categories of microcircuits.

Several diffused cross-unders and diodes were found to exhibit parasitic photocurrent amplification. In the case of the cross-under connecting the A input to external terminals, the photoresponse amplification polarity was well correlated with the electrical behavior pattern.

In summary, it is clear that many of the features of the photoresponse images of the CD4028A microcircuits were correlated with electrical behavior. If properly interpreted, such images should provide otherwise unobtainable information on the internal operation of microcircuits. The observed parasitic photocurrent amplification that occurs at high frequencies is an unexplained phenomenon. The simple model for photoresponse image generation given in the Introduction, though inadequate for explaining such parasitic effects, does suffice for understanding a correctly functioning circuit's image at low frequencies and also a completely nonfunctional stage's image at high frequency.

Although the data from photoresponse line scans was not well correlated with the leakage current data for the Type 2 circuits, the results for the Type 1 circuits did indicate that such data, taken over both n- and p-type regions of the circuit, might provide useful information about the silicon-dielectric interface.

6.0 TESTS OF THE CD4034A EIGHT STAGE BUS REGISTER

6.1 CIRCUIT DESCRIPTION

The CD4034A is a fully static eight-stage parallel/serial bilateral bus register. It is a very versatile microcircuit that can be operated in any one of several modes. Depending on inputs to the control terminals, it can operate as a serial-input shift register, a data-recirculating register, or as a parallel-load register. The parallel load can be performed either asynchronously or synchronously (i.e., controlled by the clock input). Each stage has two parallel input/output data lines, which are labelled A and B, whose functions are selected by two control inputs: A/B and A-enable. The A/B control selects either the A or the B data lines as inputs; the non-selected lines then serve as outputs. The A-enable control must be high to enable the A data lines. A low input on the A-enable control and a high input on the A/B control puts the microcircuit in the data-recirculating mode.

The logic diagram for the CD4034A microcircuit is shown in Figure 6-1. The circuit diagram is shown in Figure 6-2 with the individual MOSFET's labelled. The connections of the p-well to the V^- terminal and of the n-substrate to the V^+ terminal are not shown explicitly. Also omitted from this diagram is the p-well/substrate junction. A micrograph of the CD4034A chip is shown in Figure 6-3 with the MOSFET labels on the gate metallization.

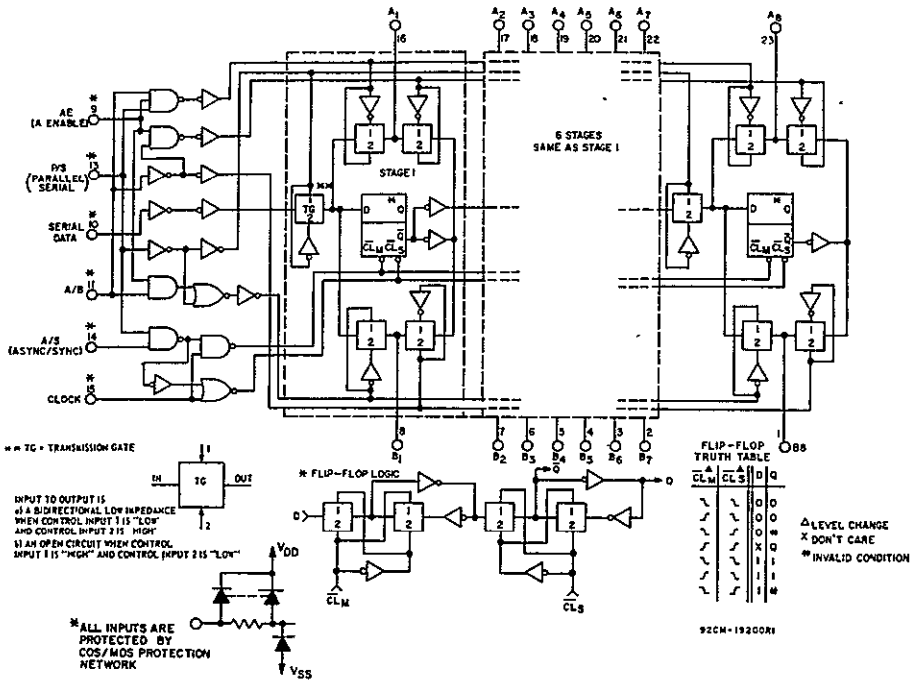


Figure 6-1. Logic diagram of the CD4034A microcircuit.

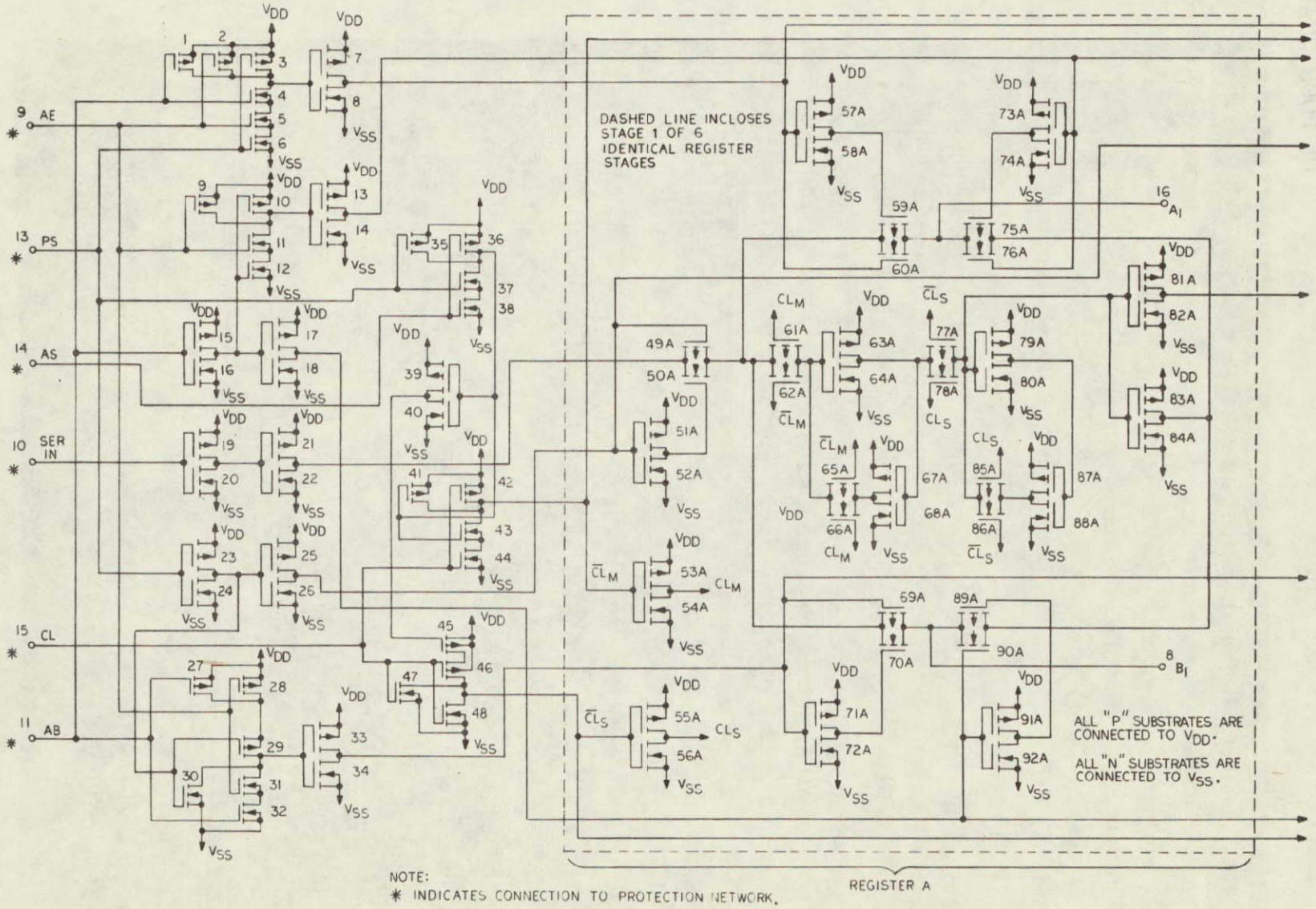


Figure 6-2. Circuit diagram of the CD4034A microcircuit.

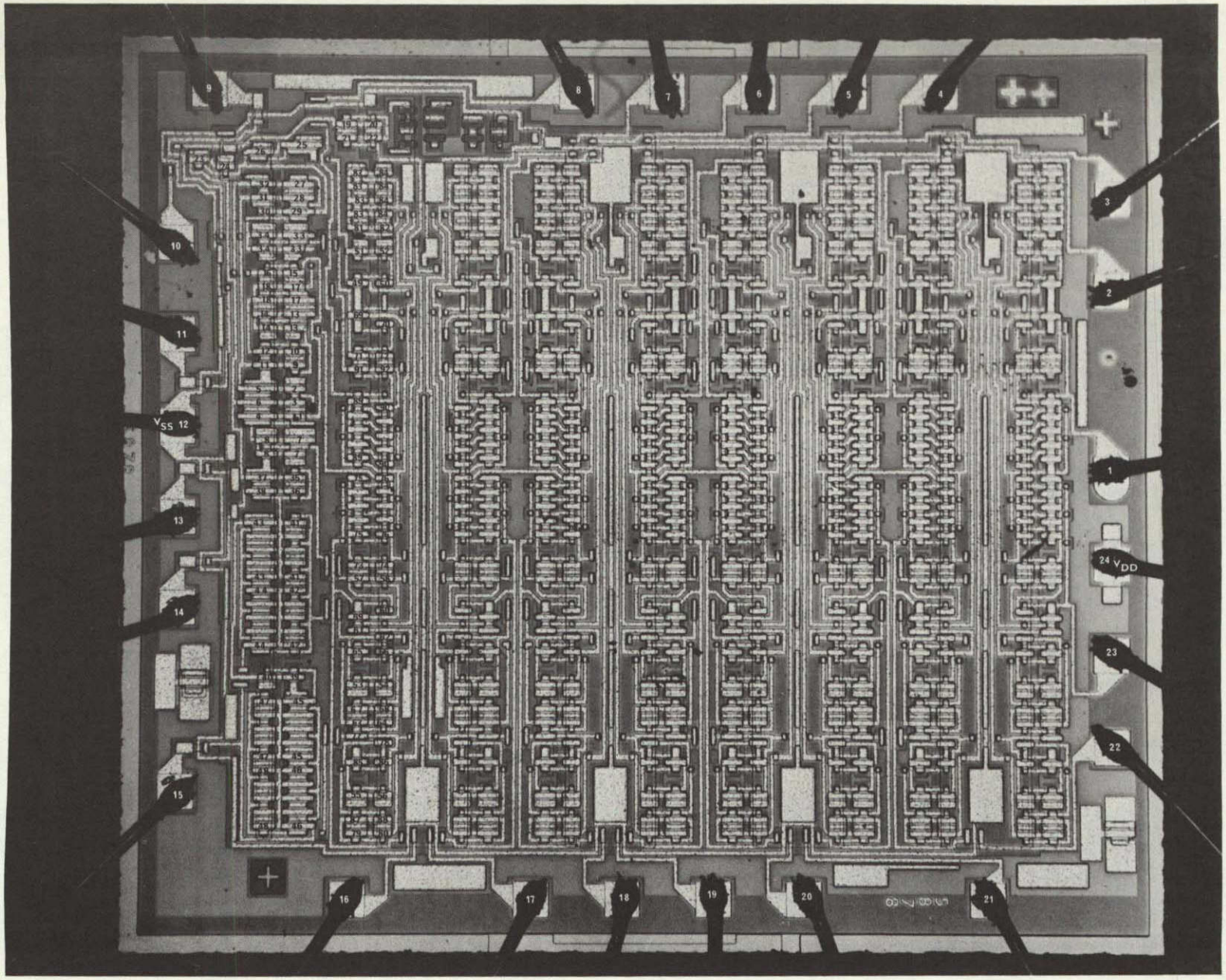


Figure 6-3. Micrograph of the CD4034A microcircuit chip.
(2.80 mm x 2.55 mm)

6.2 STATE SUPERPOSITION PROGRAM DEVELOPMENT

The CD4034A is basically a simple type of circuit, an eight-stage register, which is complicated by an elaborate set of control functions. The approach used to devise a State Superposition program is stated in Subsection 3.3: a set of input signals is chosen that is likely to exercise all data signal paths; then these input signals are applied to the data inputs while all possible combinations of control signals are applied to the control inputs.

Each stage in the register can be either in a high or low state. The data flow into a register stage proceeds along three paths: through one of the two selectable parallel inputs, or through the serial transfer input from the previous stage. These paths can be exercised by using them to alternately load ones and zeros into each stage. The sequence of operations chosen for the State Superposition program is as follows:

1. Do an asynchronous parallel load of ones into the even-numbered A inputs and zeros into the odd-numbered A inputs.
2. Do above operation with complemented input data.
3. Do operations 1 and 2 synchronously (i.e., under control of clock input).
4. Do operations 1, 2 and 3 into the B inputs.
5. Do a serial input load of alternating ones and zeros for eight cycles of the clock.

The input and control signals required to carry out this sequence of operations can be derived from a clock square wave signal divided down by a four-stage counter or frequency divider. A timing diagram of the input and control signals to be applied to the DUT is shown in Figure 6-4.

In addition to generating the signals in the timing diagram, the State Superposition test circuit must perform two additional functions: it must generate a clock signal that lags the input data so that the data signals are properly set up when the clock pulse loads them in (during synchronous loading operations), and it must disconnect the A or B terminals from the

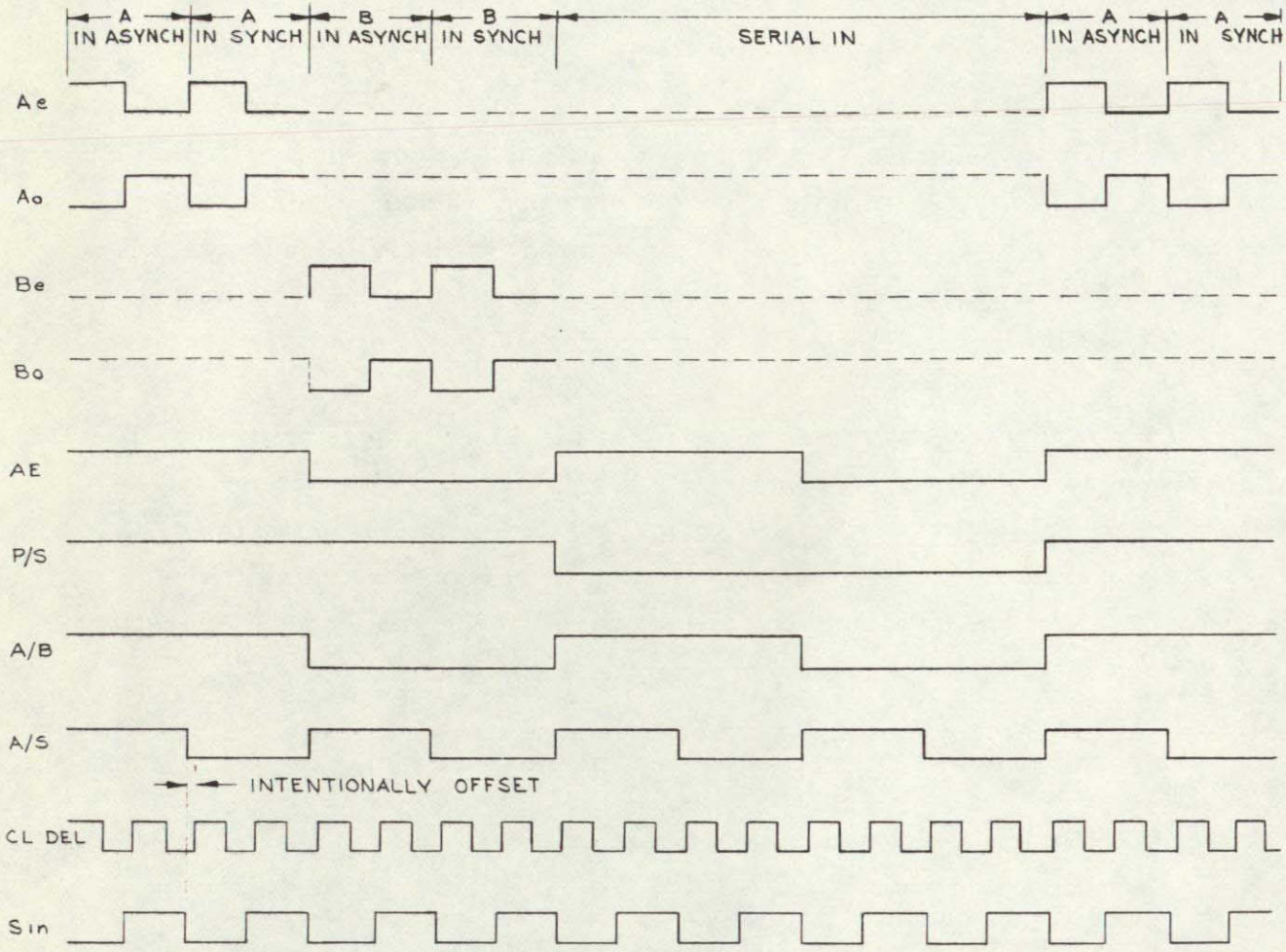


Figure 6-4. Timing diagram of signals applied to the CD4034A by the state superposition test circuit.

data sources when these terminals are selected as outputs. This latter function is implemented with transmission gates that are turned on only when the terminals to which they are connected are selected as inputs. The State Superposition test circuit that performs all these functions is shown in Figure 6-5. The following CMOS microcircuits are used in it:

CD4016 - quad transmission gate
CD4024 - seven stage binary counter (only four stages employed)
CD4011 - quad two input NAND gate
CD4049 - hex inverting buffer/converter
CD4050 - hex non-inverting buffer/converter

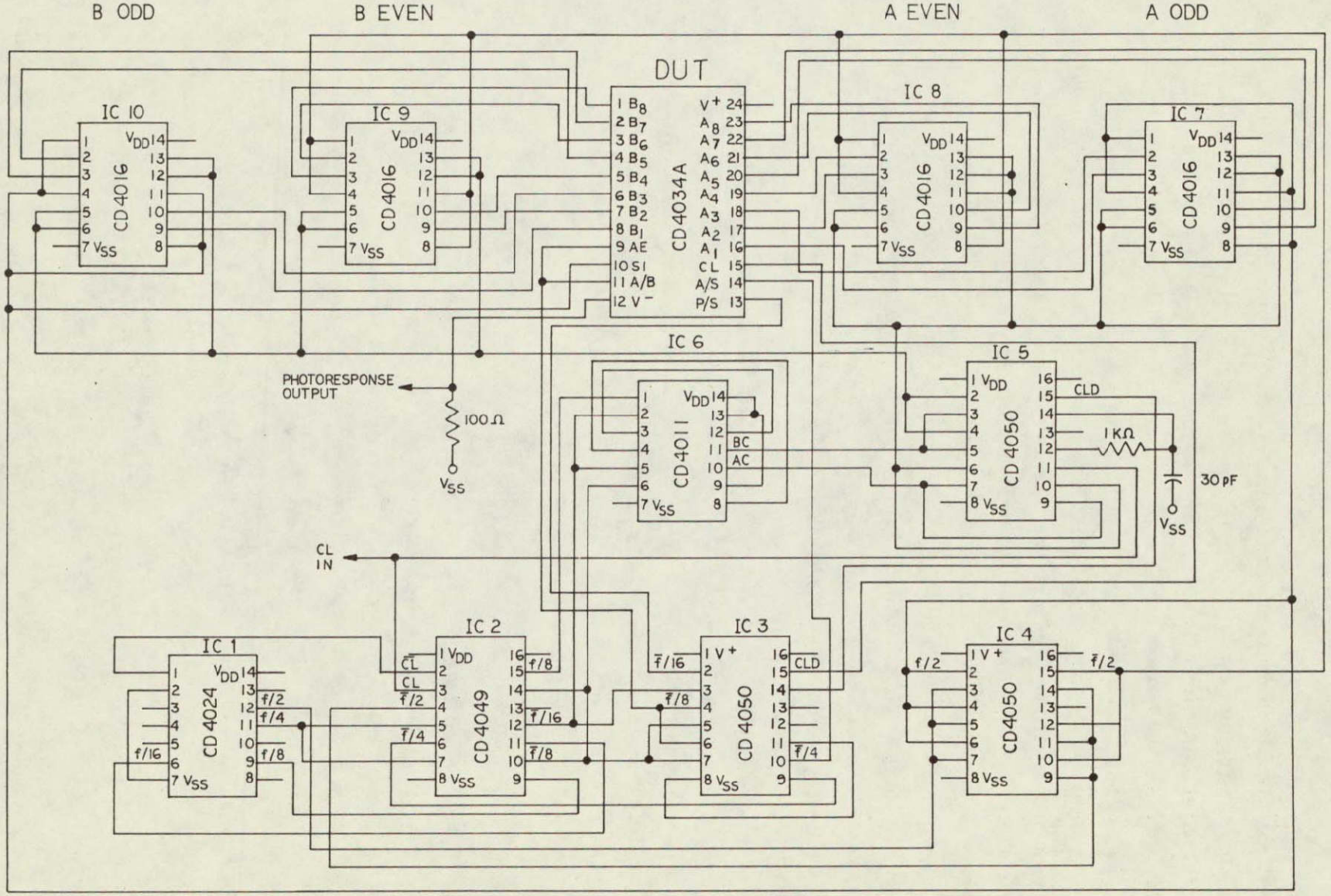


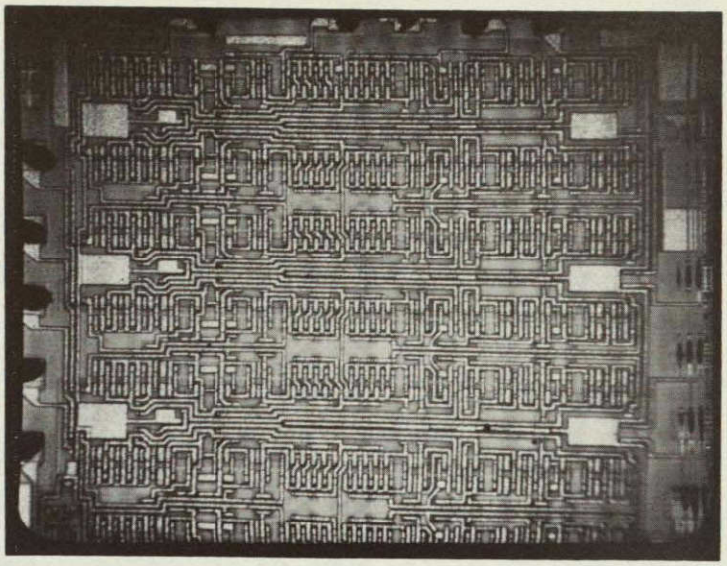
Figure 6-5. Circuit diagram of the state superposition test circuit for the CD4034A microcircuits.

This test circuit is driven by the same combination of square wave generator (HP-220A), frequency counter (HP-5301), and level-shifting circuit used for the CD4028A test circuit. A fixed 15 V power supply is used to operate most of the test circuit, with the DUT and level-shifting buffers being powered by a continuously variable V^+ supply.

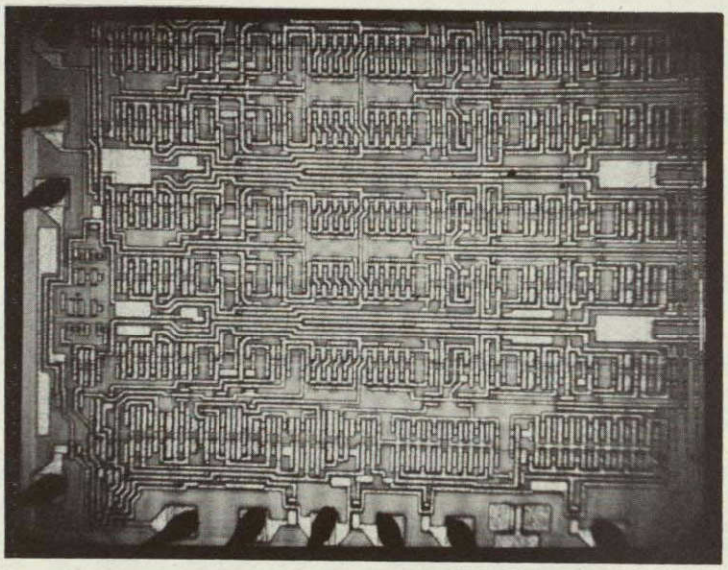
Because of the size of the CD4034A chip, it was not found possible to fully cover it with the optical scanner in a single raster frame scan. By using a 3.5 X 40 objective, it was possible to cover the chip in two frame scans with a considerable amount of overlap between the two frame scans, as shown in Figure 6-6a ("top" of chip) and 6-6b ("bottom" of chip). The photoresponse images obtained with $V^+ = 0$ V show only the p-well/substrate junctions; they are shown in Figures 6-6c and d. Figure 6-6a, the "top" of the chip, includes the circuitry for registers three through eight. Figure 6-6d, the "bottom" of the chip, includes the control circuitry (FET's No. 1 through 48) as well as the circuitry for registers one through five. Figures 6-7a and 6-7b show the photoresponse image obtained for a good test specimen with $V^+ = 10$ V and a 2.5 MHz clock frequency. A check of these pictures shows that all circuit elements expected to appear in them do appear. Many of the imaged features are diffused conductors (cross-unders, and protection circuit elements).

6.3 SUMMARY OF ELECTRICAL TEST RESULTS

The set of twenty CD4034A test specimens had essentially the same history as the CD4028A microcircuits. After a 1000 hour, 125°C life test, they had been tested according to a tentative 38510 specification by DCA Reliability Laboratory. The automated tester print-outs (supplied by NASA MSFC with the test specimens) included results for all the 38510 specification tests, but for all tests involving measurements at the A or B data lines, the relationship between the test number and the data line number was not known. A group of ten reject specimens included devices that had failed one or more current consumption (I_{SS}) or input current leakage tests. Three specimens (Nos. 226, 257, and 263) had failed several I_{SS} tests. Four other specimens (Nos. 220, 241, 258, and 260)

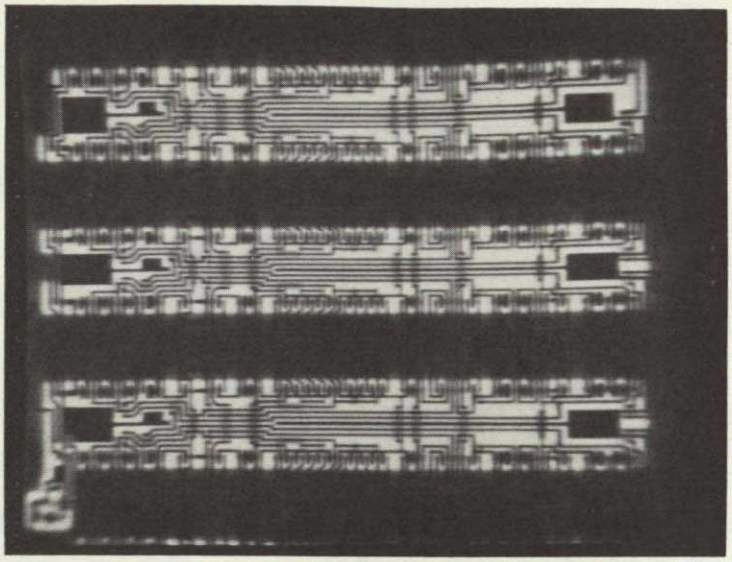


a. Reflected light image of "top" of chip

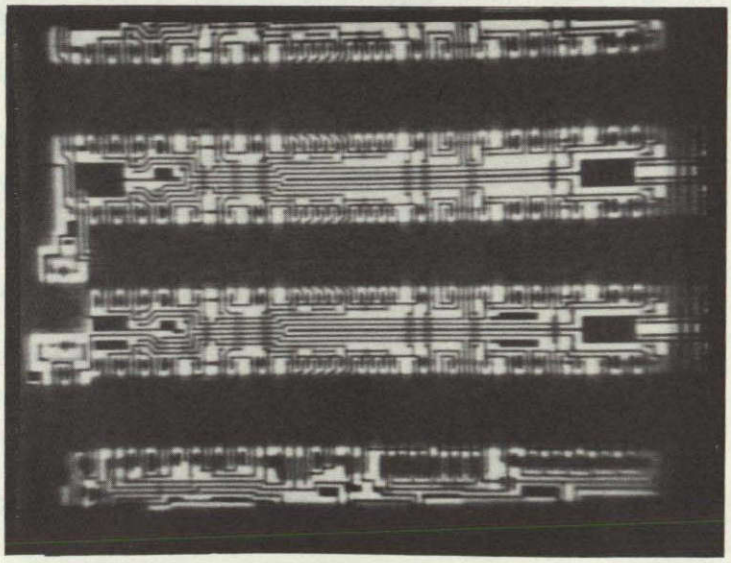


b. Reflected light image of "bottom" of chip

Figure 6-6. Images of a CD4034A specimen showing frame scans required to cover chip. (Sheet 1 of 2)

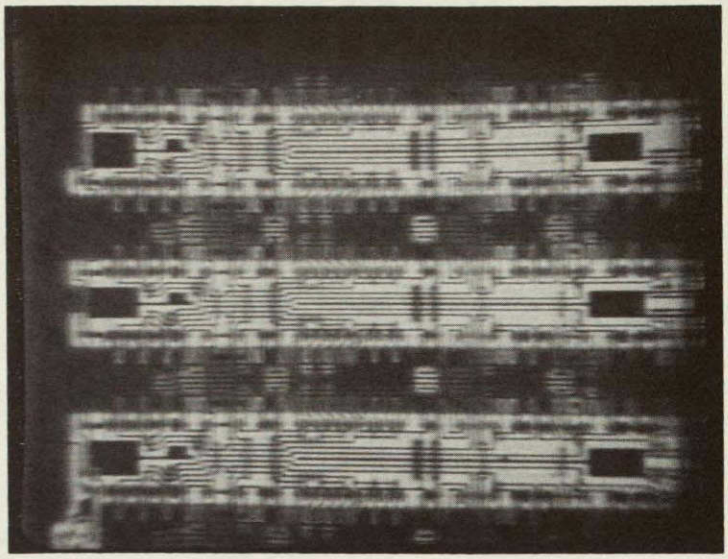


c. Photoresponse with $V^+ = 0$ V showing diffused p-wells on "top" of chip

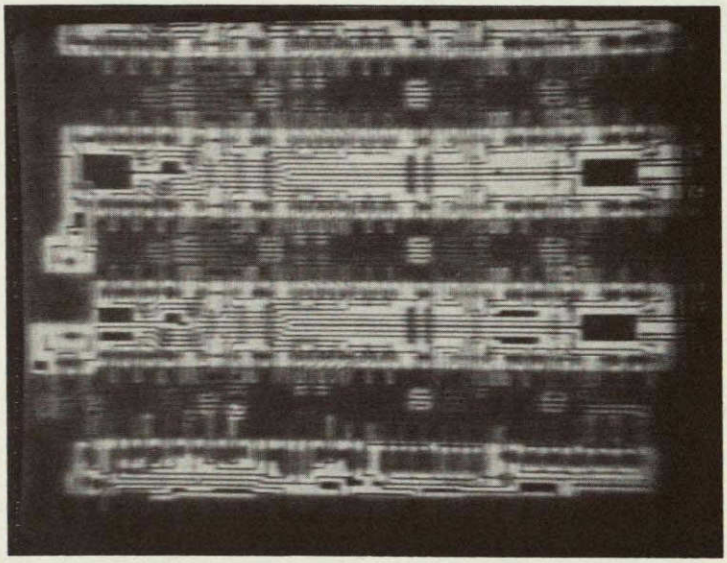


d. Photoresponse with $V^+ = 0$ V showing diffused p-wells on "bottom" of chip

Figure 6-6. Images of a CD4034A specimen showing frame scans required to cover chip. (Sheet 2 of 2)



a. "Top" of chip



b. "Bottom" of chip

Figure 6-7. State superposition photoresponse image of a good CD4034A microcircuit obtained with V^+ = 10 V and 2.5 MHz clock frequency.

had failed an input current leakage test into an unspecified set of inputs. One specimen (No. 263) that had failed three I_{SS} tests also had failed an input current leakage test. The anomalous results on output voltage and propagation time tests for one specimen (No. 262) indicated that it was only partly functional. Results for two of the reject specimens (Nos. 242 and 246) were omitted from the print-outs.

A group of ten specimens constituted the control group of good specimens. One of these specimens (No. 252) had failed one transition time test; another (No. 256) had failed many propagation and transition time tests and was obviously a very slow circuit. One specimen (No. 222) had failed two I_{SS} tests.

Unlike the CD4028A specimens, the CD4034A microcircuits were evidently a mixed lot that could not be divided into groups of devices with a common pattern of electrical behavior. For this reason, no extensive tests of each specimen were made with the State Superposition test circuit.

6.4 HERMETICITY TESTS AND VISUAL EXAMINATION

All CD4034A specimens were subjected to hermeticity tests according to MIL-STD-883, Method 1014, Condition A (fine leak) and Condition C (gross leak). The results in Table 6-1 show that all specimens passed the gross leak test. One specimen (No. 219) failed the fine leak test.

An external visual examination of all the microcircuit packages was done with a low power stereo microscope. No anomalies were noted.

The microcircuit packages were flat-packs of a type that does not have a metal lead frame. Instead, the electrical connections from the inner cavity to the package exterior are made by means of a conductor pattern screened onto the ceramic by a thick film process. The external leads are individually fastened to the thick film conductors only. When the microcircuit packages were uncapped to expose the chips, three of these fragile leads were broken off two of the specimens. Replacement leads were attached with a high conductivity silver paste.

TABLE 6-1. HERMETICITY TEST RESULTS FOR THE CD4034A SPECIMENS

	Pressure: 75 psi; Time: 1+ hrs.		
Parameter	Fine Leak	Elapsed Time	Gross Leak
Conditions	MIL-STD-883, Met. 1014 Condition A	Pressure Vessel to Spectrometer	MIL-STD-883, Met. 1014, Condition C
Requirement	5.0×10^{-8} max	30 minutes max	No bubbles observed
Unit of Measurement	atm-cc/sec	minutes	Check mark indicates no bubbles observed
Specimen			125°C
*219	1.5×10^{-7}	< 30 min.	✓
222	4.8×10^{-8}		
223	5.0×10^{-8}		
225	5.0×10^{-8}		
239	2.4×10^{-8}		
249	1.8×10^{-8}		
250	2.0×10^{-8}		
252	2.2×10^{-8}		
256	2.0×10^{-8}		
259	1.4×10^{-8}		
226	3.2×10^{-8}		
241	1.5×10^{-8}		
242	1.0×10^{-8}		
246	1.0×10^{-8}		
257	1.0×10^{-8}		
220	1.2×10^{-8}		
258	1.0×10^{-8}		
260	1.5×10^{-8}		
262	1.2×10^{-8}		
263	1.0×10^{-8}	< 30 min.	✓

Date: 8-31-76 Date: 8-31-76

Mass Spectrometer: NRC925

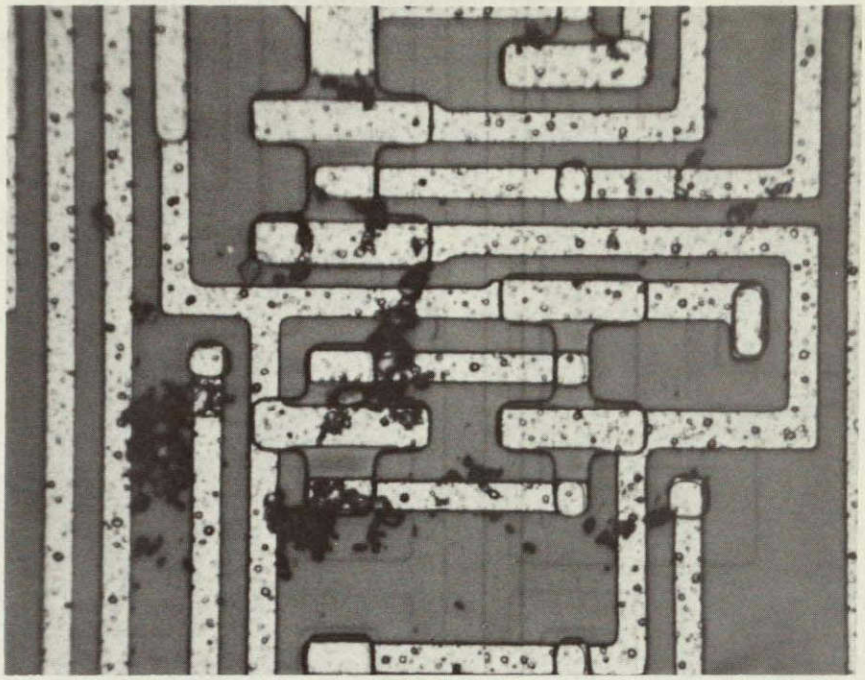
*Specimen failed fine leak test.

The exposed chips were carefully examined with a Reichert Zetopan microscope; all visible anomalies were noted and photographed. The apparent quality of the CD4034A chips was somewhat better than that of the CD4028A chips. The visible anomalies included process residues and other debris under the passivation, photolithographic flaws, and narrowed or necked-down metallization stripes. These defects were distributed fairly evenly among the good and reject specimens. They are illustrated in Figures 6-8a through d. None of the specimens had the misaligned metallization noted in some of the CD4028A microcircuits. The only anomaly noted in a reject microcircuit that obviously could account for its electrical failure (high values of I_{SS}) was a line of scratches apparently caused by a pointed instrument that was dragged across the silicon wafer. Diffused junctions fabricated on this path of damaged material would be expected to be electrically very leaky. This anomaly is shown in Figures 6-8e and f.

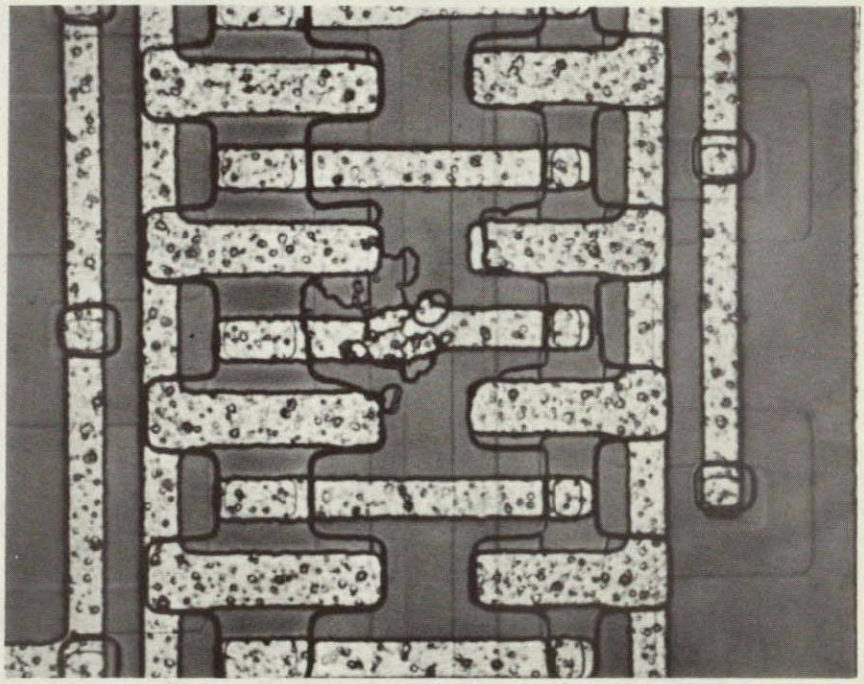
6.5 OPTICAL SCANNER EXAMINATIONS

Since the CD4034A specimens did not show any common patterns of electrical behavior that would suggest specific effects detectable with the optical scanner, the examinations of these specimens were restricted to a survey of photoresponse images. With a clock frequency of 2.5 MHz operating the test circuit shown in Figure 6-5, photoresponse images were photographed with $V^+ = 0$ V (showing only the p-well/substrate junction), 5 V, and 10 V. With $V^+ = 5$ V, the photoresponse images were photographed with the video polarity both normal and inverted to properly record parasitic behavior. An inverted polarity image was photographed for $V^+ = 10$ V for a specimen that showed parasitic behavior at that voltage.

The 161 photographs that resulted from the optical scanner examinations had to be compared visually among themselves, a formidable task that could not be carried out at the circuit element level within the available time. Instead, the images were examined for differences involving groups of circuit elements. (Since the malfunction of one element would be evident in the images of all elements dependent on it for a drive signal, this is not an unreasonable approach).

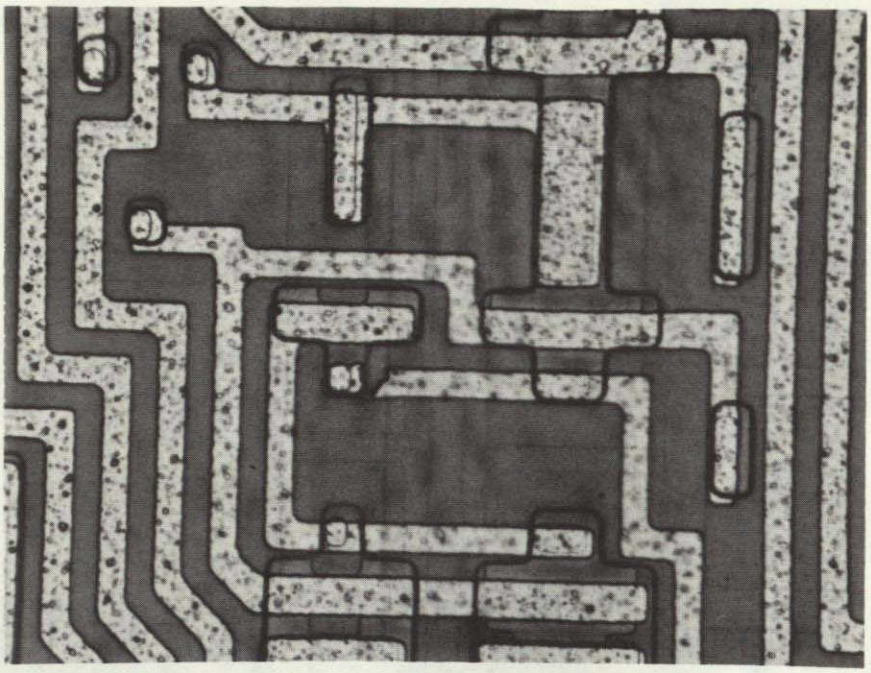


a. Process residues under passivation
Specimen 220. (440X)

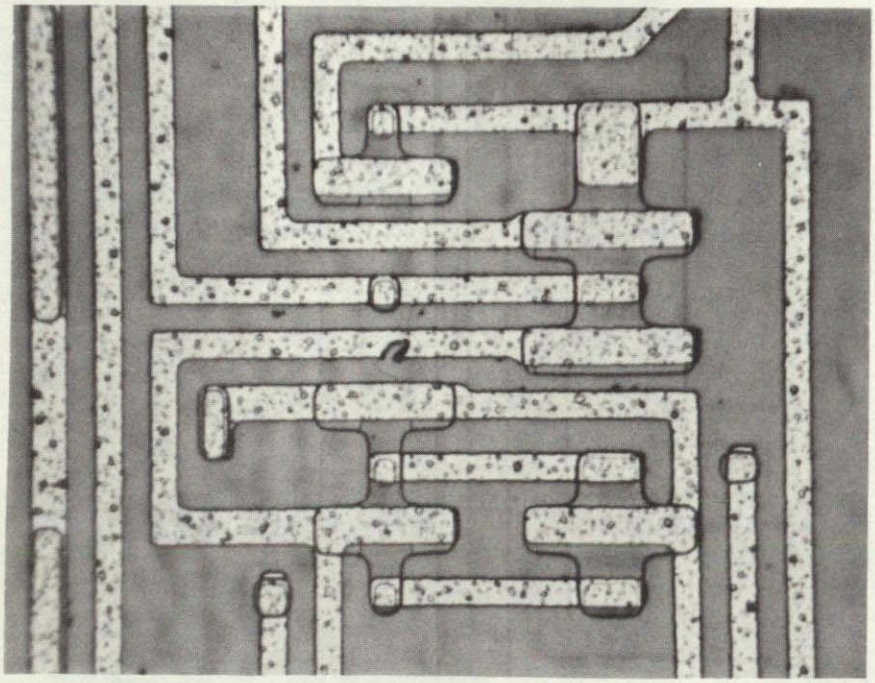


b. Photolithographic flaw
Specimen 225. (590X)

Figure 6-8. Examples of defects found in the CD4034A specimens by visual inspection. (Sheet 1 of 3)

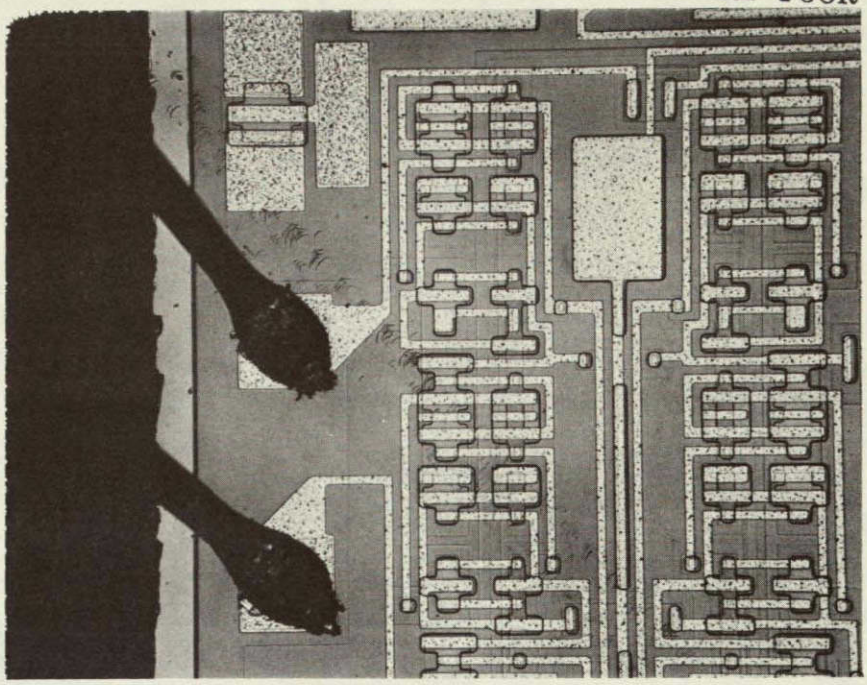


c. Necked-down metallization stripe
Specimen 256. (440X)

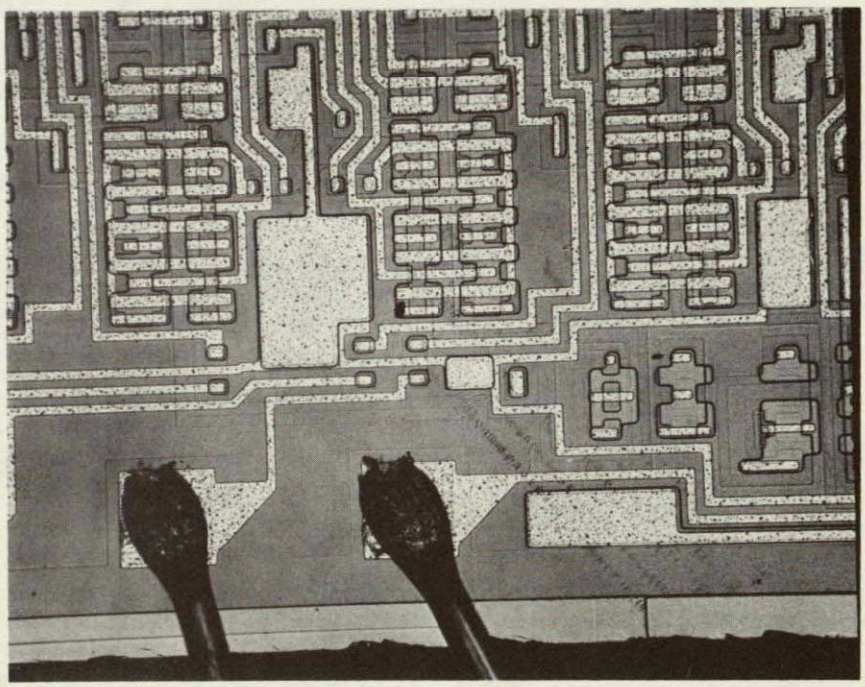


d. Necked-down metallization stripe
Specimen 246. (440X)

Figure 6-8. Examples of defects found in the CD4034A specimens by visual inspection. (Sheet 2 of 3)



e. Scratches in silicon substrate
Specimen 257. (130X)



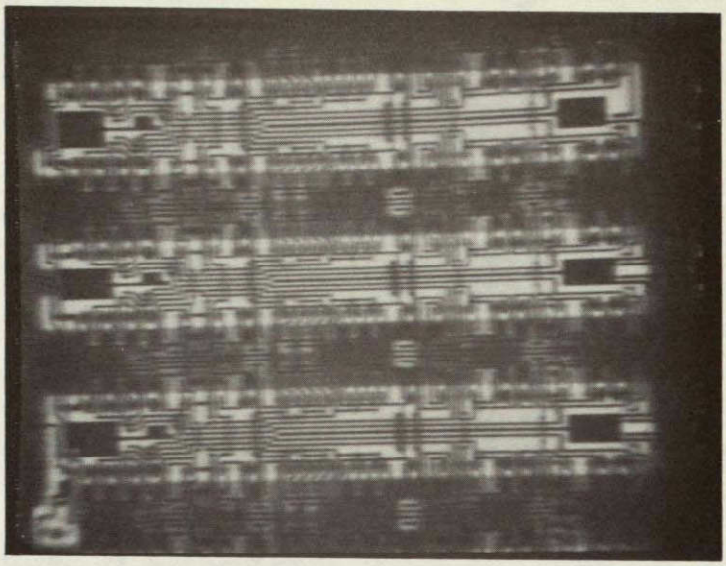
f. Scratches in silicon substrate
Specimen 257. (130X)

Figure 6-8. Examples of defects found in the CD4034A specimens by visual inspection. (Sheet 3 of 3)

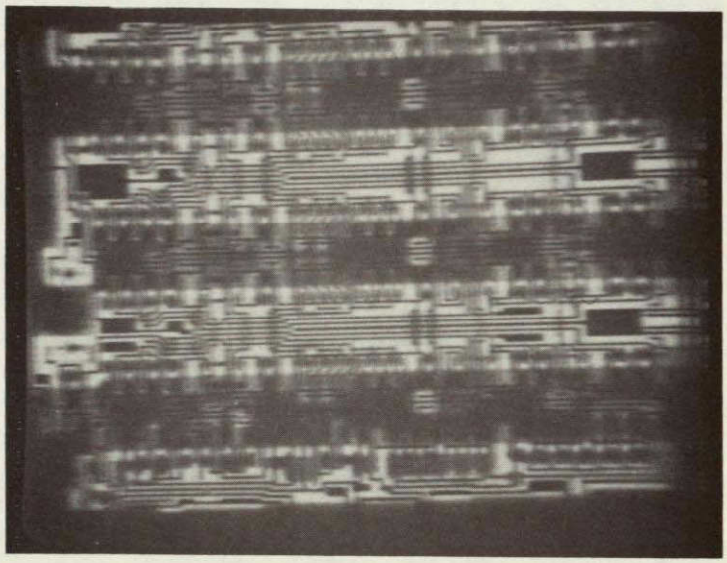
The photoresponse images made with $V^+ = 0$ V did not show any obvious differences between specimens. With these and other specimens it has been noticed that certain features (diffused junctions) in the n-substrate are imaged very faintly with $V^+ = 0$ V if they are near the p-well/substrate junction (otherwise they are not imaged at all). The weak photoresponse intensity from these features appears to vary from specimen to specimen. Such variations probably reflect conditions at the surface or in the bulk silicon that affect diffusion by optically generated carriers. They may accordingly be useful for device evaluation. These effects could not be adequately documented with the images produced by these optical scanner tests.

The images made with $V^+ = 10$ V, exemplified by Figures 6-9a and b, were very similar to each other, with two exceptions. For one good specimen (No. 256) and one reject specimen (No. 242), parasitic photocurrent amplification was observed in the p-channel circuitry of register 8. The images showing this phenomenon appear in Figures 6-10a and b and 6-11. The FET's involved are all p-channel devices in transmission gates that control the data flow from the serial input. The good specimen (No. 256) was one previously pointed out as having failed several propagation and transition time tests. No test data were available on the reject specimen.

The images made with $V^+ = 5$ V all exhibited parasitic amplification of the photocurrent in a pattern that was fairly consistent among all specimens. Since the experiments with the CD4028A microcircuits had shown that the photoresponse polarity and intensity from the parasitics can be strongly influenced by the frequency of operation, the wide variations that were observed could be expected for different specimens operated at the same frequency. The locations of the parasitics, however, did not vary greatly. In most cases the parasitics involved diffused conductors or cross-unders in the p-well or the n-substrate, although instances of FET's manifesting this behavior could also be found.

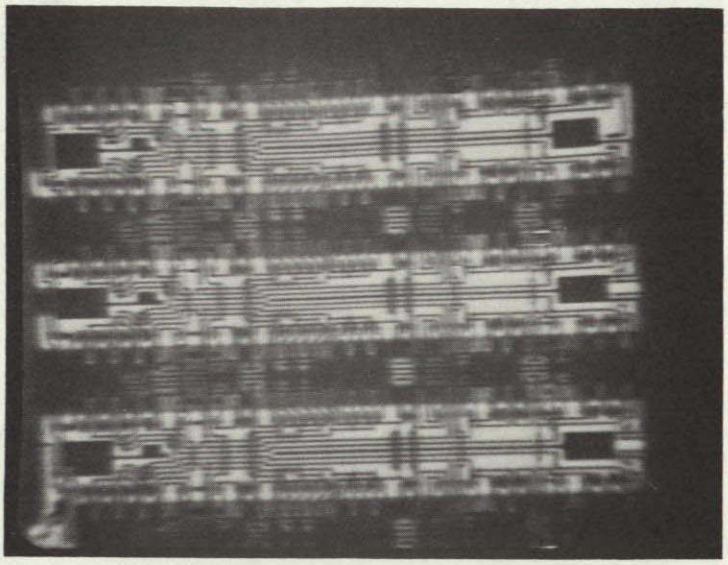


a. "Top" of chip

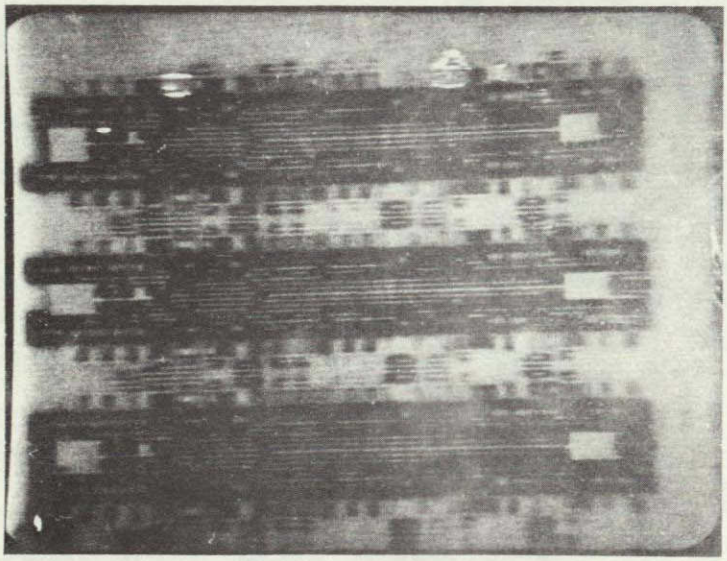


b. "Bottom" of chip

Figure 6-9. Representative photoresponse images of a CD4034A microcircuit specimen with $V^+ = 10$ V.



a. With normal video polarity



b. With inverted video polarity.

Figure 6-10. Photoresponse image of good specimen (No. 256) with parasitic photocurrent amplification in the circuitry of register 8. ($V^+ = 10V$)

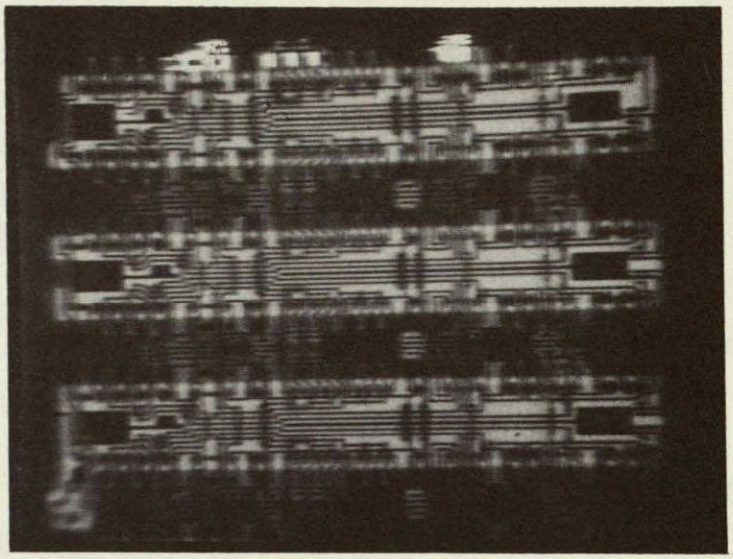


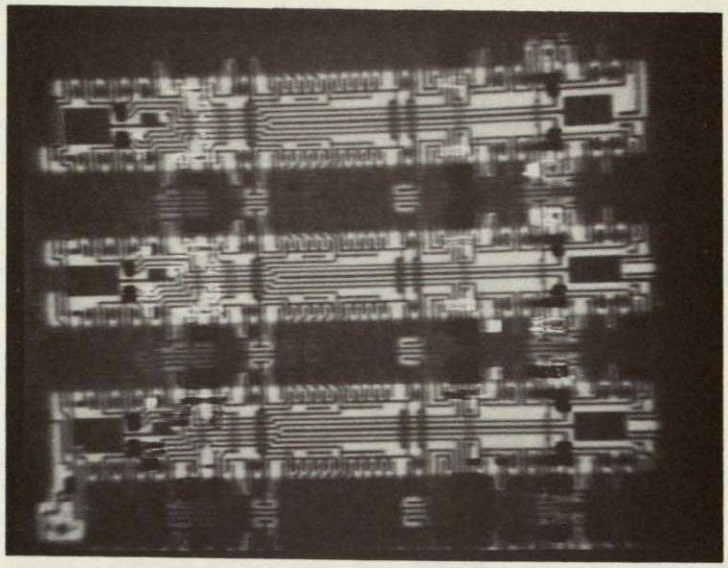
Figure 6-11. Photoresponse image of reject specimen (No. 242) with parasitic behavior in the circuitry of register 8. (normal video polarity) $V^+ = 10$ V.

One readily apparent difference between the images made at $V^+ = 5$ V for the various specimens involves the photoresponse intensity from the p-channel FET's. For many of the specimens the p-channel FET's appeared dark; this would imply that the circuits were not functional during substantial portions of the operation sequence that makes up the State Superposition program. The State Superposition test circuit produced rather complicated output waveforms from the DUT. These were not checked for all outputs of all specimens, but spot checks did seem to show that all specimens were functional. In many cases the output pulses were rounded off or otherwise degraded. Five of the specimens - three good devices and two reject devices - did have at least parts of the circuitry with distinctly imaged p-channel FET's. The results for these specimens are as follows:

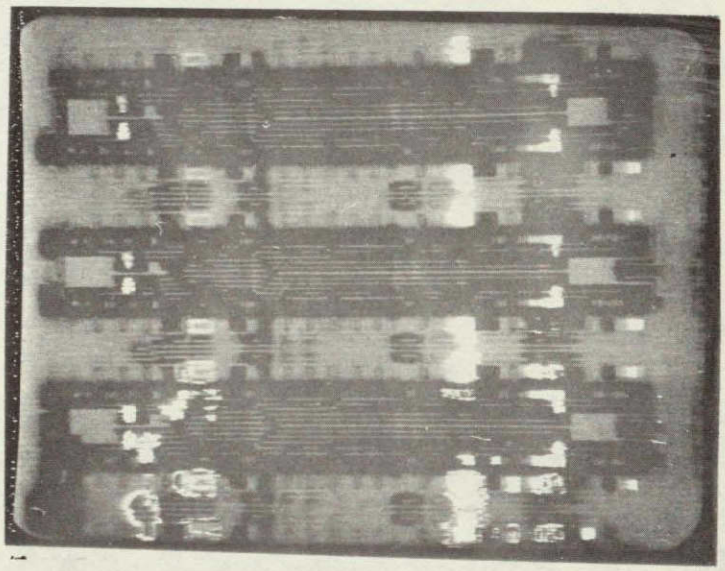
No. 219(G): All p-channel circuitry imaged
No. 223(G): P-channel circuitry dark in registers 7 and 8
No. 256(G): P-channel circuitry dark in registers 6, 7, and 8
No. 257(R): P-channel circuitry rather dim; many parasitics with intense photoresponse
No. 262(R): All p-channel circuitry imaged.

Examples of photoresponse images illustrating the behavior with $V^+ = 5$ V are shown in Figures 6-12a through d, 6-13a and b, and 6-14a and b. Figures 6-12a through d show typical images with dark p-channel circuitry. Figures 6-13a and b show images obtained with a specimen (No. 219) having all p-channel circuitry imaged. Figures 6-14a and b show images for a specimen (No. 256) in which part of the p-channel circuitry appeared dark.

The overall appearance of the photoresponse images made with $V^+ = 5$ V did not correlate well with the automated tester electrical test results. However, the fact that observed differences did affect all the circuitry for individual register stages does imply that the optical scanner was detecting real operational differences. The occurrence of parasitic amplification of the photocurrent at high clock frequencies in these circuits as well as in the CD4028A's shows that this is probably a phenomenon common to many CMOS microcircuits. The detailed mechanism of the parasitics is not known.

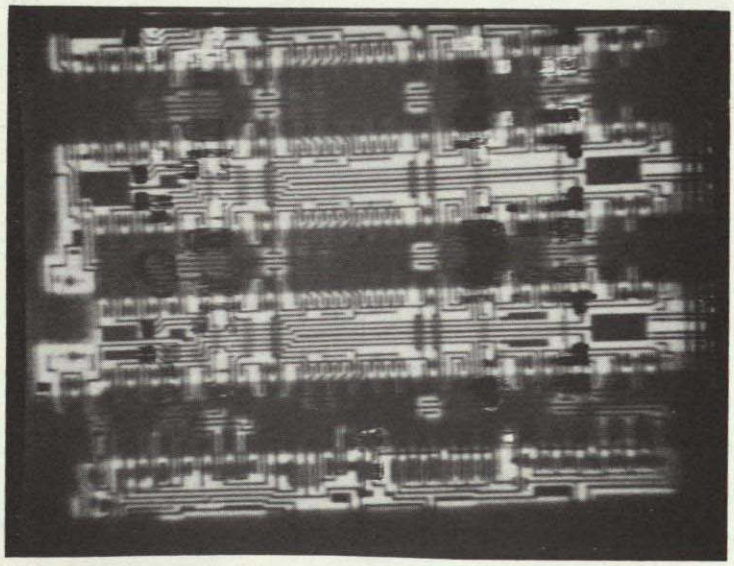


a. "Top" of chip, normal video polarity

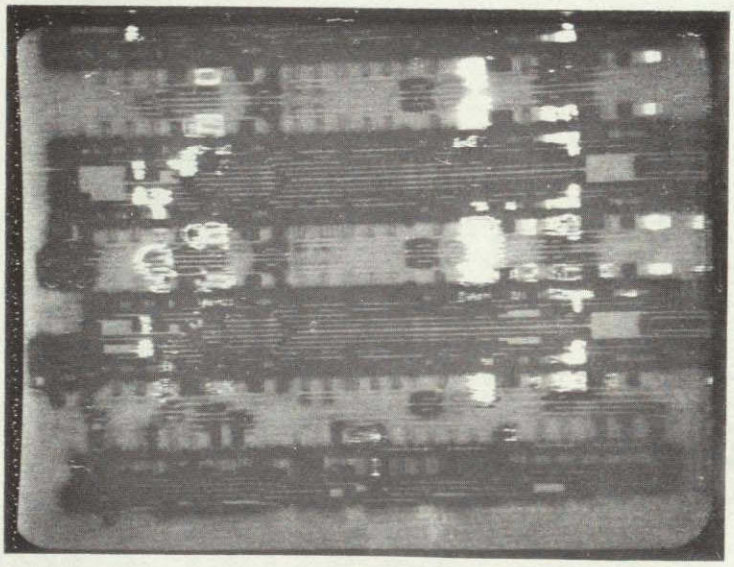


b. Same, inverted video polarity

Figure 6-12. Photoresponse image for $V^+ = 5$ V of a specimen (No. 250) with all the p-channel circuitry dark. (Sheet 1 of 2)

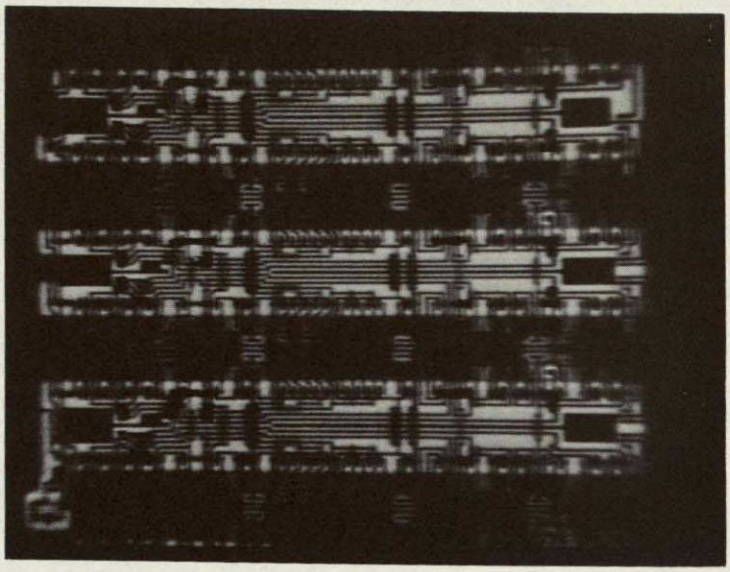


c. "Bottom" of chip, normal video polarity

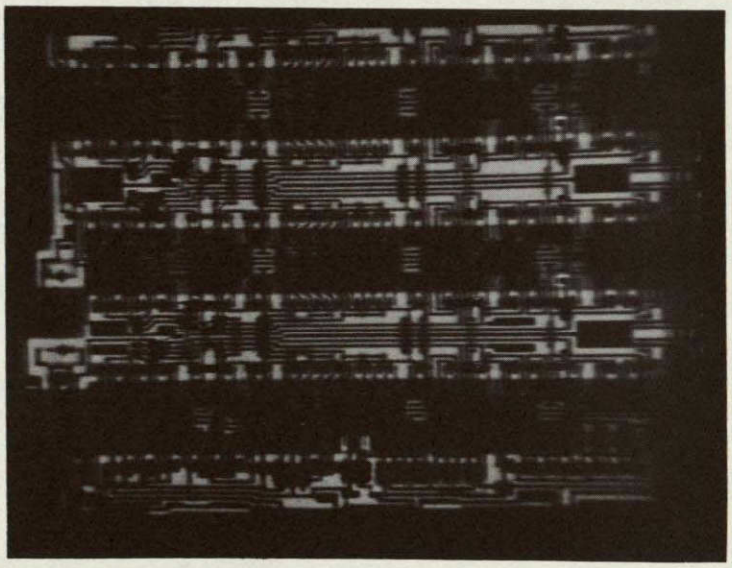


d. Same, inverted video polarity

Figure 6-12. Photoresponse image for $V^+ = 5$ V of a specimen (No. 250) with all the p-channel circuitry dark. (Sheet 2 of 2)

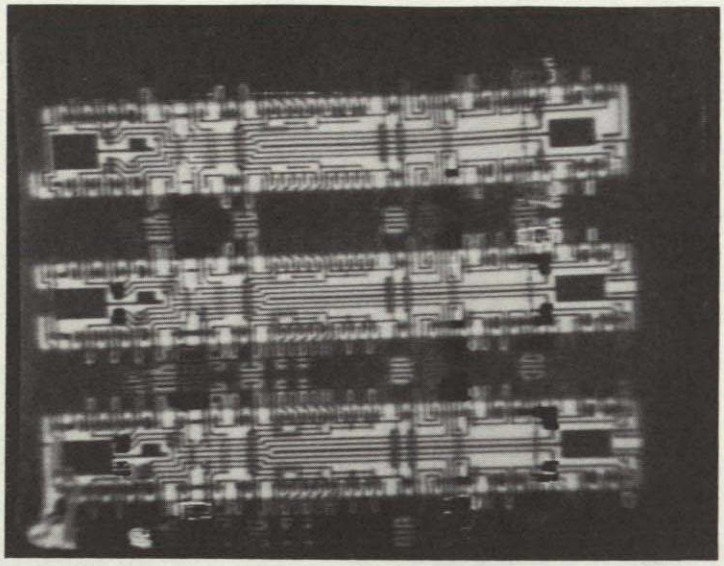


a. "Top" of chip

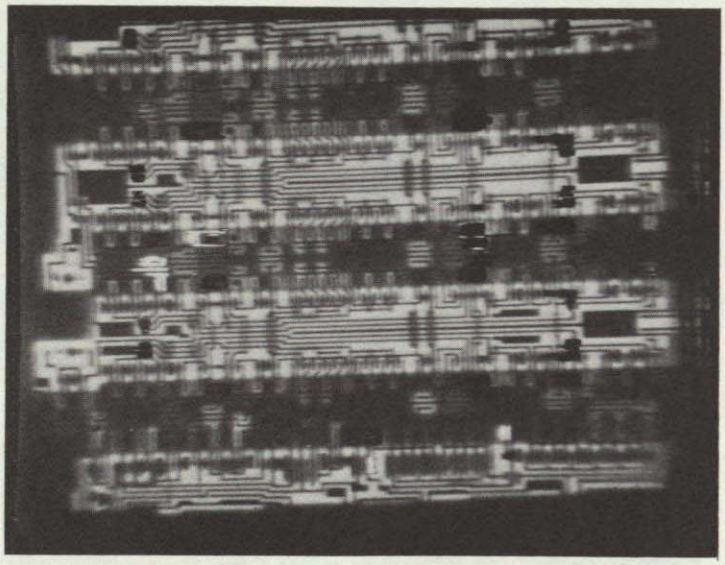


b. "Bottom" of chip

Figure 6-13. Photoresponse image for $V^+ = 5$ V of a specimen (No. 219) with all p-channel circuitry imaged (normal video polarity).



a. "Top" of chip



b. "Bottom" of chip

Figure 6-14. Photoresponse image for V^+ = 5 V of a specimen (No. 256) with the p-channel circuitry dark in registers 6, 7 and 8 (normal video polarity).

The Optical Spot Scanner test plan for the CD4028A microcircuits included tests specifically intended to look for effects related to high frequency malfunction and to current leakage mechanisms. The high frequency tests were intended to illustrate the Optical Spot Scanner's ability to localize the circuit stages that malfunctioned at high frequency. Although this objective was met, the localization of malfunctioning stages was neither as definite nor as dramatic as had been anticipated. One reason for this may be that the high frequency failure is not as definitely localized as had been hypothesized. The model that had been implicitly assumed was that of a single stage that ceased to operate at high frequency in spite of having adequate drive signals at its inputs. In fact, the high frequency malfunction of the microcircuit may involve several marginally functioning stages that successively attenuate the signal pulses. Nevertheless, the results of the Optical Spot Scanner examination did identify certain stages as being the principal cause of high frequency malfunction. This information cannot be obtained directly by any other nondestructive test.

The activation at high frequency of bipolar parasitics that amplified the photocurrent was an unanticipated phenomenon. Although the mechanism that causes the parasitic behavior is not understood, the appearance of the phenomenon at NOR gate FET clusters and at input protection diodes was very well correlated with the high frequency and leakage current behavior patterns of the microcircuits. The appearance of parasitic behavior must reflect the local occurrence of electrical bias conditions that are not explained by simple models of CMOS circuitry. In the case of NOR gate FET's, the parasitic behavior was a precursor of malfunction at high frequency. In addition to posing an obvious, puzzling question about their origin and cause, these parasitics would seem to have some important practical consequences. It should be kept in mind that the parasitics are observed at frequencies for which the microcircuits are fully functional. Therefore, a system using conventional CMOS microcircuits at high operating frequencies in a radiation environment could be predicted (on the basis of these findings) to manifest an abnormally high current consumption as well as occasional data errors.

An attempt was made to detect current leakage processes by measuring a parameter that describes carrier diffusion along the silicon - dielectric interface. The measurements characterized only the surface of the n-type substrate, so leakage effects on the p-well material could have gone undetected. The results obtained on a limited number of specimens were more indicative than definitive. The finding that a large value of the decay length parameter may be a necessary but not sufficient condition for low leakage is consistent with the idea that a high surface recombination velocity would cause high surface leakage currents.

The results for the second part type, the CD4034A eight stage bus register, were obtained only from a photoresponse image survey at two values of power supply voltage. The appearance at high frequency of parasitic photocurrent amplification in these specimens indicates that the phenomenon occurs in various types of conventional CMOS microcircuits. It is not just a peculiarity of the CD4028A decoder chip. The photoresponse images for $V^+ = 5$ V also displayed substantial differences among the specimens, which must reflect differences in their internal electrical operation.

The State Superposition program for the CD4034A microcircuits was considerably more complex than for the CD4028A's. The fact that a successful program and a test circuit to implement it were devised in the first attempt shows that the semi-intuitive approach (described in Section 3) does work.

Taken as a whole, the results of this development project show that the Optical Spot Scanner, used in combination with the State Superposition Technique, can generate a single photoresponse image that contains a substantial amount of useful information about the device under test. This information is well correlated with the measured electrical parameters that are used for acceptance testing. However, the photoresponse image data are much more specific in terms of determining the locations of malfunctions. Such data are therefore significant not only for screening inspection but also for engineering studies.

During the course of this work, a number of problems were discovered that will have to be addressed in future work. It was clear from the beginning that phenomena resulting in small changes in photoresponse signal would not be detected by a visual comparison of CRT photographs; quantitative data processing would be required. The effects that were looked for were those resulting in obvious, qualitative changes in the photoresponse image. The results of the project showed that such effects do occur. However, experience with the CD4034A specimens, which are quite complex, showed that even qualitative changes can be very difficult to keep track of by visual comparisons alone. It is evident that future development of the Optical Spot Scanner as an inspection instrument can best be carried out by recording, processing and comparing the photoresponse data in digital form. While digital data processing will eventually be required for a practical implementation, the complexity and quantity of the data appear to require data processing even in the developmental effort.