

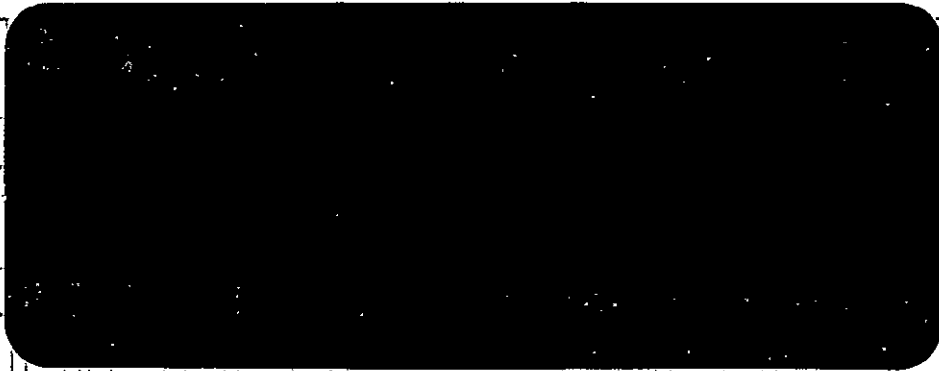
TRW

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SYNCHRONIZER Final Report (TRW Defense and
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100 MSPS SYMBOL SYNCHRONIZER

FINAL REPORT

December 21, 1977

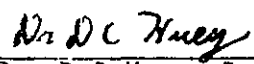
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1.0 INTRODUCTION

This final report describes the functional characteristics and design of the 100 MSPS symbol synchronizer and presents test data obtained from the brassboard. This brassboard constitutes one of the deliverables under the contract.

The successful completion of this contract represents a significant increase in the maximum symbol rate at which a heavily noise corrupted signal can be acquired and tracked with near optimum performance. The work reported herein shows that symbol rates to 100 MSPS can be properly synchronized and detected at signal to noise ratios down to -2 dB with detection degradation less than 1.5 dB.

The basic system approach remains as described in the original proposal and is as follows:

1. Matched filter : 8-tap transversal filter
2. Baseline restoration : Maintaining equal average amplitude of detected symbol types
3. Output normalization : Combination of manual gain control (>35dB) and automatic gain control (6dB)
4. Clock recovery : Data Transition Tracking Loop (DTTL) with window width equal to one symbol period
5. Acquisition : Acquisition is normally dependent on the action of clock recovery loop. A manually activated sweep function is available.

The hardware implementation utilizes both analog and digital circuits to take advantage of the simplicity of the analog circuits and the precision of the digital circuits. As shown in Figure 1-1 the same tapped-delay line is used both as a matched-filter for data detection and as a correlation filter (with integration centered about the transition) for the DTTL phase detector. A TRW LSI 3 bit A/D converter (designated the "3BQ") is used to sample and to perform the digital conversion on the transversal filter output at twice the symbol rate. Alternate samples go to the data detector and phase detector circuits in which these digital circuits perform the appropriate processing to (1) encode soft-decision output, (2) cross-multiply phase error with data

1.1 100 MSPS SYMBOL SYNCHRONIZER SPECIFICATION SUMMARY

Required Data Rates	: 20, 30, 60 and 100 MSPS $\pm 0.01\%$ *
Input Data Code	: NRZ-L
Input Signal Level	: 400 mV rms ± 20 dB
Input Baseline Variation	: $\pm 100\%$ of peak signal from dc to 1 KHz
Output	: 3 bit soft decision
Format	: Sign and magnitude binary coding
Threshold Spacing	: Nominal at 0.51 times noise free bit and continuously variable from 0.18 to 0.70
Normalization	: AGC response to the total input signal plus noise power
Threshold	: $E_s/N_o = -2$ dB
Acquisition Time	: ≤ 0.1 sec at $E_s/N_o = 7$ dB ≤ 1.0 sec at $E_s/N_o = -2$ dB
Input Jitter	: $\leq 1.0\%$ of bit period in the frequency range of 1.0 Hz to 10% of bit rate
RMS Output Jitter	: $\leq 2.5\%$ of bit period
BER Performance Degradation:	≤ 1.5 dB for -2 dB $\leq E_s/N_o \leq 7$ dB

*Other rates in the range 10 to 100 MSPS are possible with slight modifications to the basic design.

transition sense per the DTTL algorithm, and (3) sense baseline error. The latter two functions are converted to analog for processing by their respective loop filters. For the clock recovery loop, an LC VCO is used as a reference for a digital frequency synthesizer. The output of this synthesizer is the desired coherent clock that is used to sample the matched filter and to clock the digital logic.

The brassboard is as shown in Figure 1-2 and is a rack mountable chassis 10.5" high. Power is provided via a standard 110V AC source. Circuit construction techniques used include printed circuit boards and circuit boards with arbitrary wiring where semi-rigid cable used on most of the signal paths.

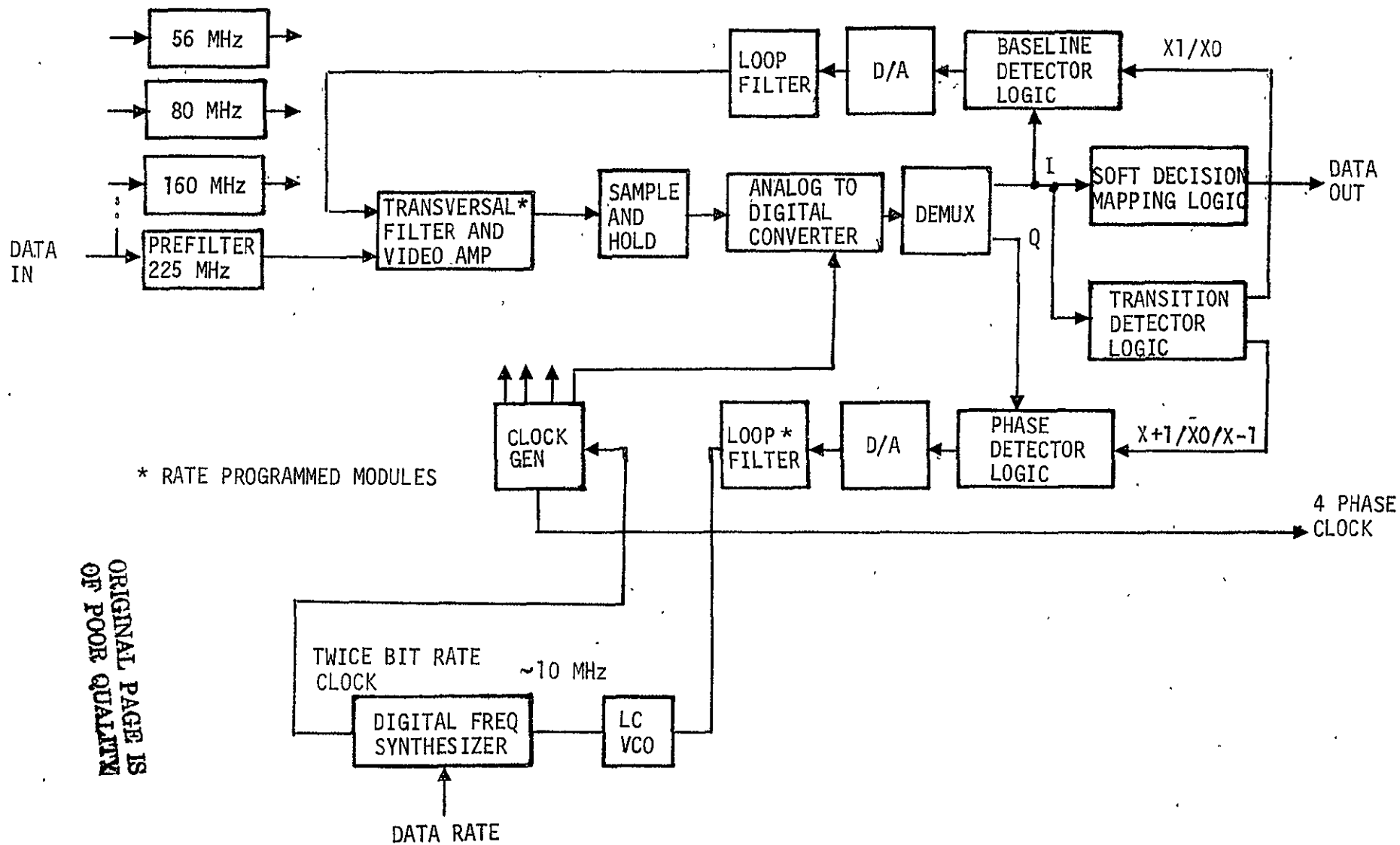


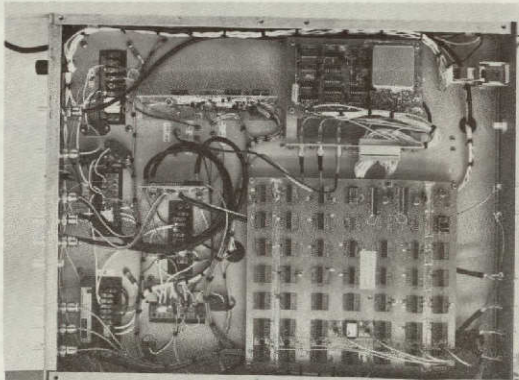
Figure 1-1. 100 Msps Symbol Synchronizer Block Diagram

FOLDOUT FRAME 1

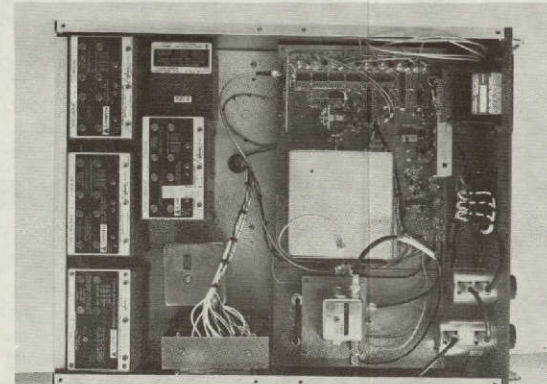
FOLDOUT FRAME 2



(a) Front View



(b) Top View



(c) Bottom View

Figure 1-2. 100 MSPS SYMBOL SYNCHRONIZER

2.0 SYSTEM CONFIGURATION DESIGN

In this section is presented a detailed description of the functional design of the 100 MSPS symbol synchronizer.

2.1 INPUT CIRCUITS

The input circuits include a set of lowpass pre-filters, a variable gain control attenuator, and a matched filter. The lowpass pre-filters may be selected or bypassed by connection of appropriate coaxial cable jumpers (RG58C/U with BNC connectors). In fact they may be used independent of the symbol synchronizer. At symbol rates (f_s) below 100 Msps, the input bandwidth must be reduced to avoid aliasing as the effective matched filter sample rate ($8 f_s$ for eight taps) drops. Seven filters (one of which is shown in Figure 2-1) are required to cover the full 10 MHz to 100 MHz range (Table 2-1). However, the four required rates of 20, 30, 60 and 100 Msps only utilize four of these filters and hence these are the four that are included in the hardware. The filter and attenuator are designed to maintain 50 ohm impedances and are dc coupled.

Input signal levels of 400 mv RMS $\pm$ 20 dB are normalized to the minimum signal end of this range by the variable gain control attenuator; this requires 40 dB attenuation range.

In addition, operation at lower bit rates with a given input prefilter bandwidth results in reduced total input SNR and consequent suppression of signal level for constant total signal-plus-noise. This requires 1.5 dB for half-octave filters. Thus, the total input dynamic range is 41.5 dB and is obtained using a combination of manual attenuators (mounted on the front panel) and an AGC circuit having 6 dB dynamic range.

In order to obtain the required 6 dB dynamic range AGC, a circuit based on the concept shown in Figure 2-2 is used. The differential amplifier and the push-pull output driver stage are optimized for broad bandwidth as is the circuit layout. The gain control is achieved by varying the (negative) feedback ratio according to the power detected at the output. The actual voltage at the AGC output is 75 mv RMS while the control voltage varies from -1.0V to -8.0V.

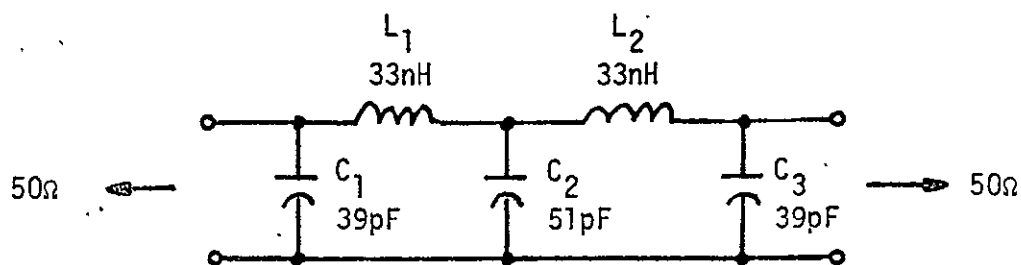


Figure 2-1. 225 MHz Prefilter

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Table 2-1. Half-Octave Input Prefilter Set

SYMBOL RATE (MS/S)	FILTER CUTOFF (MHz)	L_1, L_2 nH	C_1, C_3 pf	C_2 pf
70 - 100	225 *	33	39	51
50 - 70	160 *	47	56	68
35 - 50	112	68	82	100
25 - 35	80 *	91	110	150
18 - 25	56 *	130	160	220
13 - 18	40	180	220	300
10 - 13	28	270	330	430

*Included in hardware

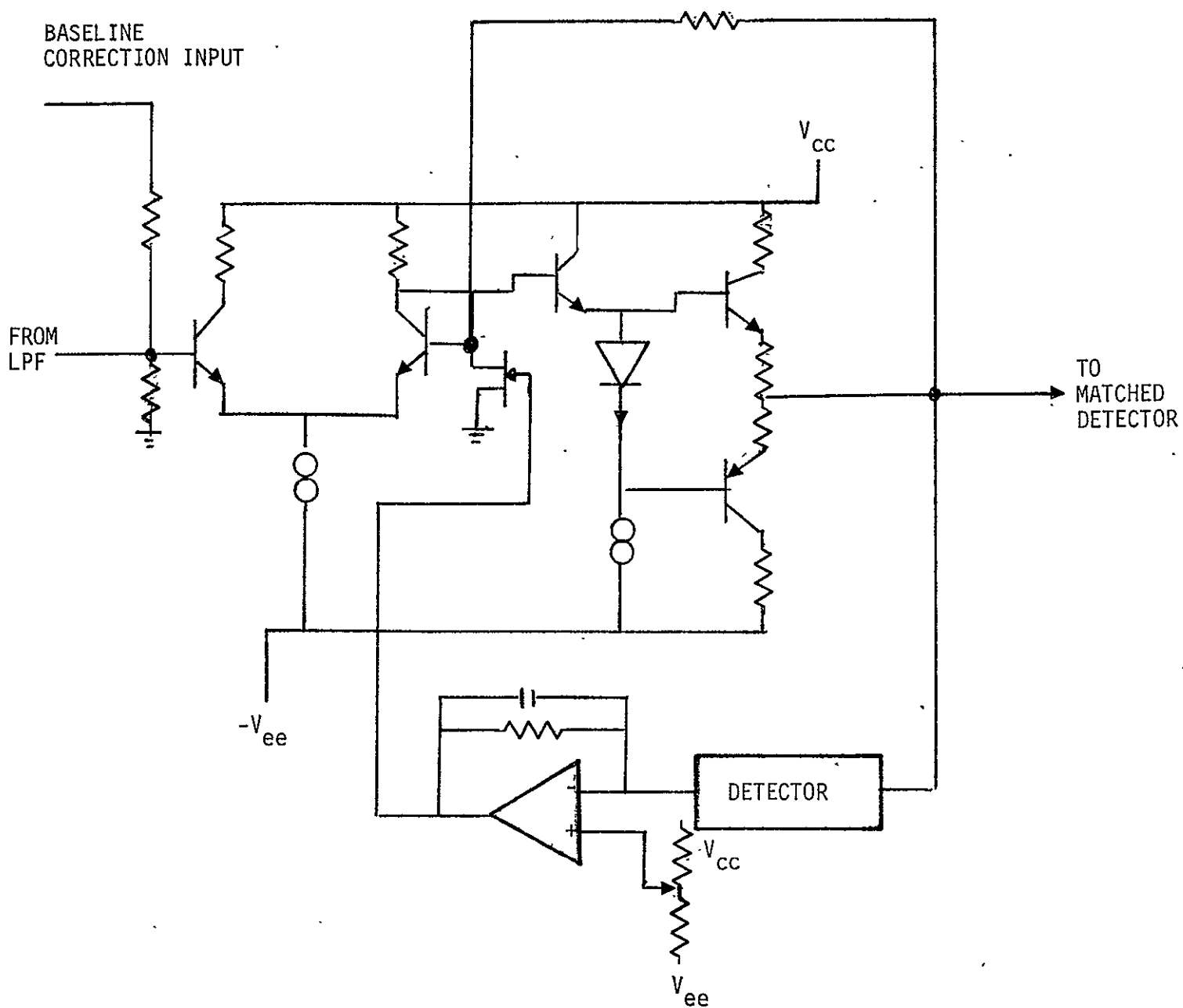


Figure 2-2. Basic AGC Approach

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Input signal baseline variation is specified as equal to 100% of the peak signal level, and thus is a maximum of 75 mv at the AGC input. Accordingly, a dc offset correction term (with sufficient dynamic range to correct this offset as well as internal circuit offsets) is added at this point. The correction signal is generated in the coherent baseline offset detector which is described later.

2.2 MATCHED FILTER

The matched filter, implemented as a tapped delay line, is used both for data and phase detection simply by sampling its output at times spaced one-half a symbol period apart (Figure 2-3). Thus, when a single received data bit is just entering the tapped delay line (and its predecessor is just exiting the far end) the analog voltage at the output of the matched filter corresponds to the integral over a bit time. This is exactly as required for a "matched to NRZ" data detector. On the other hand, if the transition between two bits is in the exact middle of the delay line, then the matched filter output corresponds to the estimate of phase error. Thus, it is only necessary to uniformly sample the matched filter twice per symbol time and alternately use every other sample as data and phase information.

Symbol rate programming is effected by selection of a unique matched filter assembly for 100 Msps operation and a second assembly for data rates below 60 Msps. This unit is tuned to the particular data rate by connection of a set of seven matched lengths of coaxial cable. The appropriate cable lengths are as shown in Table 2-2. The use of eight taps over a symbol interval is equivalent to sampling at eight times the symbol rate ($8 f_s$) and thus avoids aliasing since the $2.25 f_s$ predetection filter provides attenuation in excess of 15 dB at $4 f_s$ and above.

Wideband amplifiers using matched high frequency transistors serve as buffers to the sampled signals at the tap points. The diagram of the transversal filters, which includes the delay lines, the wideband buffers and the video amplifiers, is shown in Figure 2-4.

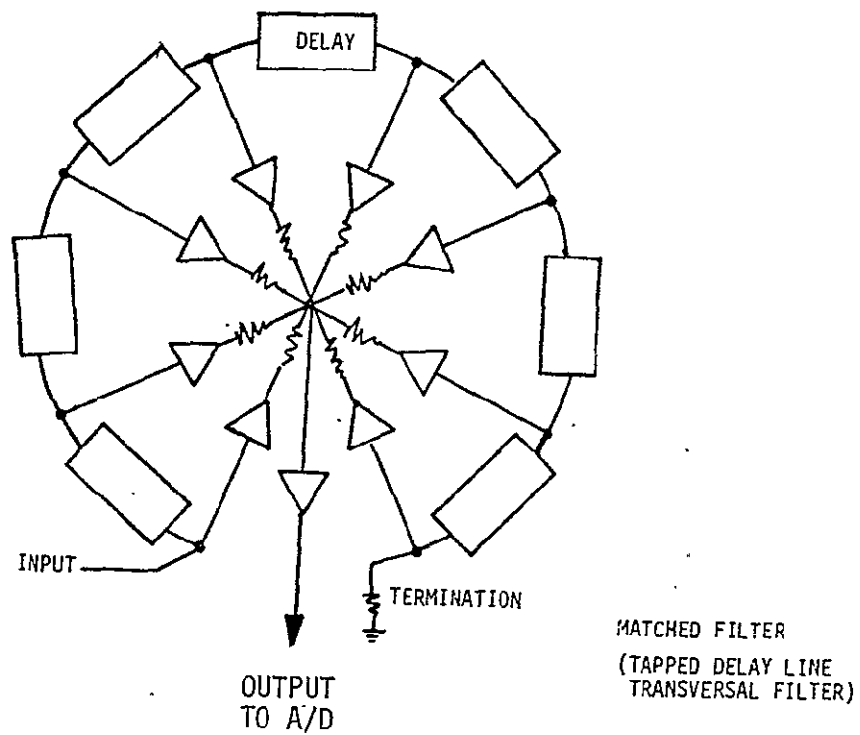


Figure 2-3. Matched Filter (Tapped Delay Line Transversal Filter)

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Table 2.2. Matched Filter Delay Line Lengths

SYMBOL RATE	DELAY ELEMENT LENGTH (INCHES)	EXTERNAL DELAY ELEMENT LENGTH (INCHES)
100 MSPS	10.25	--
60	17.09	9.59
30	34.18	26.68
20	51.27	43.77
SR ($10 \leq \text{SR} \leq 60$ MSPS)	$\frac{1.025 \cdot 10^9}{F_s}$	$\frac{1.025 \cdot 10^9}{F_s} - 7.5$

Note: For Symbol Rates below 60 MSPS, use 0.141 Dia Solid teflon semi-rigid with length as noted in the right hand column. Connect to the matched filter module with SMA 3mm connectors.

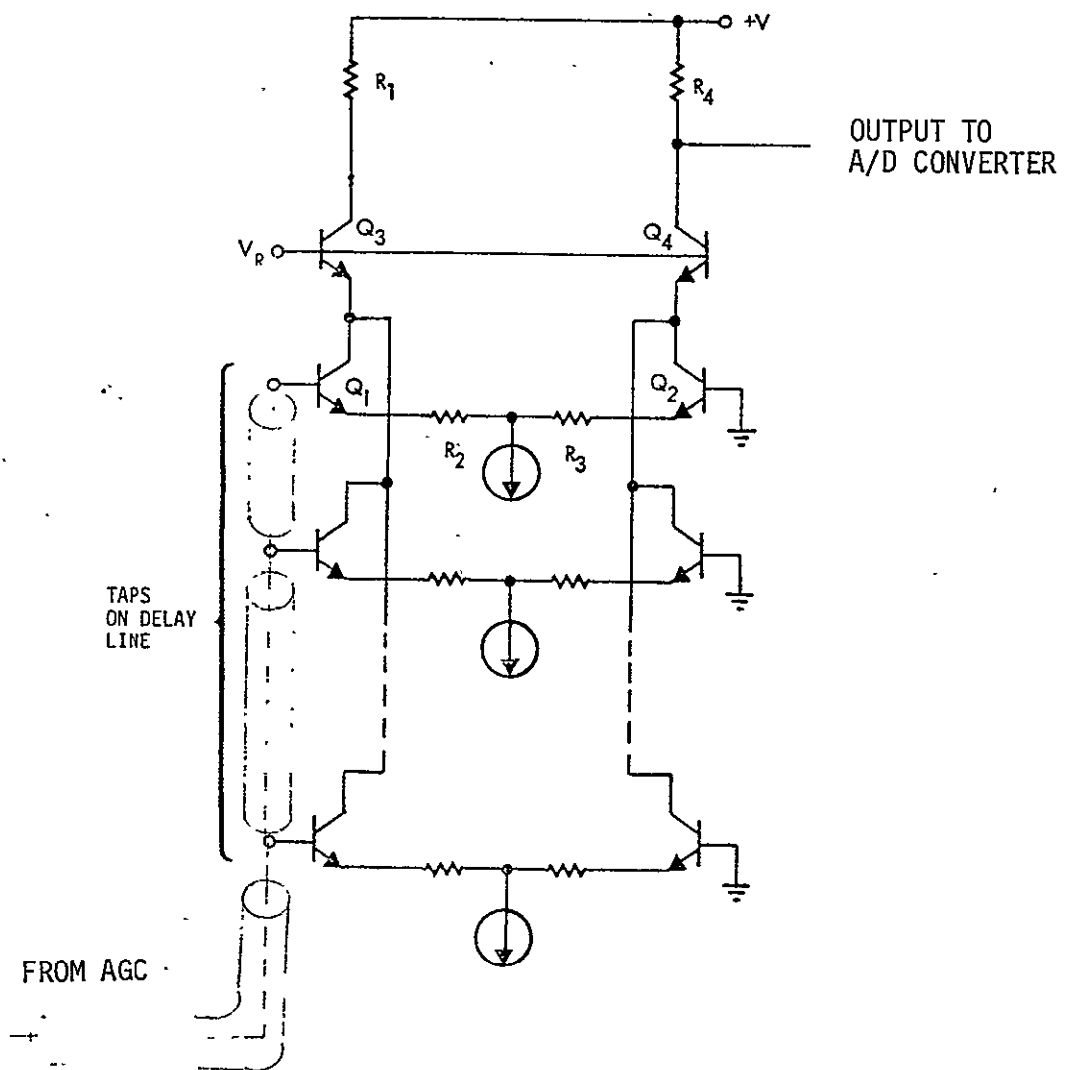


Figure 2-4. Transversal Filter Amplifiers

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The wideband buffer amplifiers serve the following four purposes:

- 1) To provide high impedance at the delay line tap points, thus minimizing reflections due to the delay impedance mismatch.
- 2) To provide low impedance drive to the summing network.
- 3) To convert the single-ended video input into differential signals for the summation process, thus minimizing even-harmonic distortion.

As shown in Figure 2-4, each wideband buffer consists of an emitter-degenerated differential pair. The pairs are biased identically. The gain of the wideband buffer amplifiers is determined by the ratio $(R_1 + R_4)/(R_2 + R_3)$. The resistor values are selected so that the gain is equal to 0.4. This selection allows frequency roll-off at 225 MHz due to the parasitic RC time-constants to be less than 0.1 dB.

2.3 ANALOG-TO-DIGITAL CONVERSION

Existing TRW designs from recent advanced development projects for microelectronic A/D conversion building blocks have been applied to the synchronizer design. Specifically a three-bit parallel A/D converter on a single monolithic silicon LSI chip "3 BQ," has been used. Due to the short aperture time of the 3 BQ, 100 ps, it is not necessary to include a sample and hold.

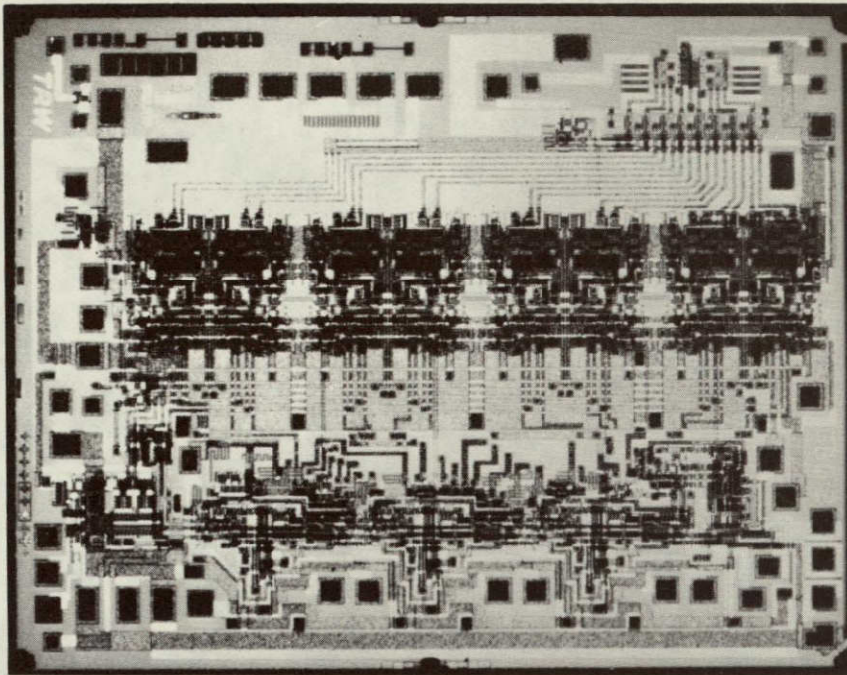
Functionally, the monolithic 3-bit quantizer array consists of the following blocks:

- Input buffer
- Resistor networks
- Comparators
- Linear-to-binary decoder.

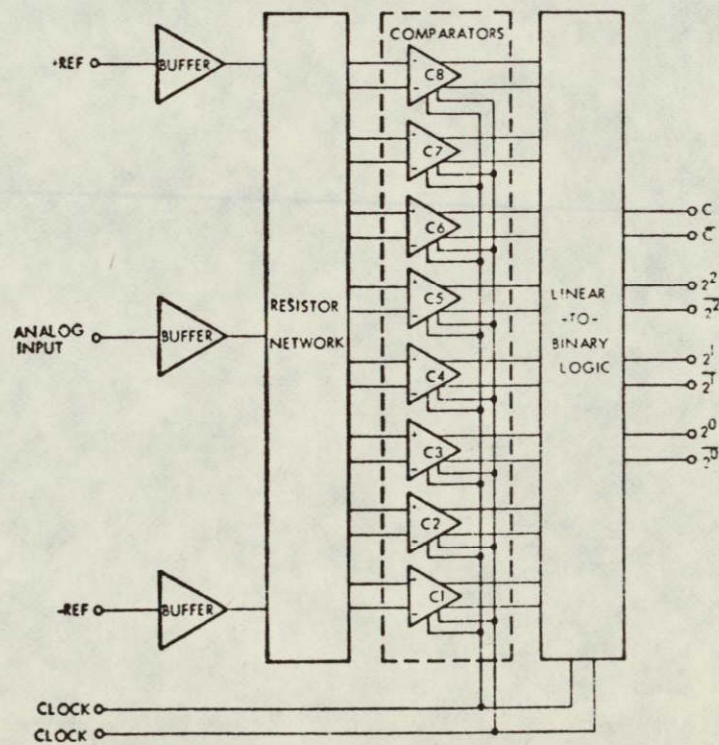
The block diagram and a photograph of the 3 BQ are shown in Figure 2-5.

The reference resistor ladder network is included on the LSI chip to minimize external interfaces and off-the-chip parts. The analog input terminals are tied to a similar resistor network to equalize the source impedance of each comparator, thereby reducing current input dc errors. Both ends of this network are tied together and driven by an emitter follower, T2. This reduces the input capacitance by more than a factor of 8, to 0.15 pf plus pad and wiring capacitance, or about 0.40 pf. Without this buffering emitter follower, the input capacitance would be 1.12 pf plus the parasitic capacitance of the resistor network plus wiring and pad capacitance, or about 3.4 to 5.4 pf depending on resistor network area, which would be prohibitive.

There are eight comparators in the 3 BQ. Seven of the eight comparators makes the decision as to whether the input signal lies in one of the eight quantization regions. The eighth comparator indicates over-range. The digital outputs of these comparators are then registered and binary-coded for external usage.



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Figure 2-5. 3BQ Monolithic Circuit

2.4 DATA AND PHASE DETECTORS

The threshold spacing of the data detector's A/D is variable by manual control over the range from 0.18 to 0.70 times the noise-free symbol amplitude (75 mv). This relationship is illustrated in Figure 2-6. The A/D's offset binary output is mapped into a sign-and-magnitude format as indicated in Table 2-3. This word is presented as the soft-decision output. The output word is buffered by MECL III differential drivers. A separate pair of output connectors duplicates the most significant bit, providing the hard-decision serial NRZ-L output signal.

The hard-decision NRZ-L is also processed by transition detection logic to determine the presence and polarity of transitions. The results are used to multiply the properly delayed phase detector A/D output by +1, 0, or -1 according to the Data Transition Tracking Loop (DTTL) principle. Table 2-4 indicates the mapping. The resulting three bit word is D/A converted and then provided as input to the loop filter.

The logic circuits which functionally implement the data and phase detector functions described above are depicted in Figure 2-7. Approximately 40 MECL III type devices suffice for these operations.

The 3-bit D/A converters are implemented as R-2R ladders being driven from MECL III gates. The resistance selected for R is 50 ohm which reduces the mismatched termination problem. A characteristic of an R-2R ladder D/A converter which is driven by logic levels is that a dc offset will exist on its output. This is cancelled by the addition of an equivalent offset generated as the negative of the average voltage of a logic "1" and "0" (Figure 2-8). Thus, temperature induced changes in the offset will track if both the reference logic IC and the D/A driver IC's are at the same temperature.

2.5 LOOP FILTER

The loop filter (Figure 2-9) is designed such that a classical second order phase locked loop response is obtained. The loop filter is as shown in Figure 2-9 where two additional circuits are also indicated. The first is a clamp circuit which does not allow the loop stress voltage to exceed some

NOMINAL CASE T = 0.36S			LOW T CASE T = 0.18S			HIGH T CASE T = 0.70S		
MV	CODE	"T"	MV	CODE	"T"	MV	CODE	"T"
81	<u>011</u>	3T				159MV	<u>011</u>	3T
54	<u>010</u>	2T					010	
27	<u>001</u>	T	41	<u>011</u>	3T	106MV	<u> </u>	2T
	<u>000</u>		27	<u>010</u>	2T		001	
-27	<u>100</u>	-T	14	<u>001</u>	T	53MV	<u> </u>	T
-54	<u>101</u>	-2T		<u>000</u>			000	
-81	<u>110</u>	-3T	-14	<u>100</u>	-T		<u> </u>	
	111		-27	<u>101</u>	-2T		100	
			-41	<u>110</u>	-3T	-53MV	<u> </u>	-T
				111			101	
						-106MV	<u> </u>	-2T
							110	
						-159MV	<u> </u>	-3T
							111	

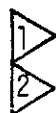
Figure 2-6. Threshold Spacing

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Table 2-3. Soft Decision Data Coding

DATA DET. A/D OUTPUT	ROUNDED VALUE		DATA OUTPUT			
	BINARY	DECIMAL	HARD	MSB	SOFT 2SB	LSB
0 1 1	011.1	3.5	1	0	1	1
0 1 0	010.1	2.5	1	0	1	0
0 0 1	001.1	1.5	1	0	0	1
0 0 0	000.1	0.5	1	0	0	0
1 1 1	111.1	-0.5	0	1	0	0
1 1 0	110.1	-1.5	0	1	0	1
1 0 1	101.1	-2.5	0	1	1	0
1 0 0	100.1	-3.5	0	1	1	1

NOTES



A/D CENTRAL THRESHOLD AT ZERO VOLTS DC

APPENDING AN LSB $(0.1)_2 = (0.5)_{10}$ FOR SYMMETRY

Table 2-4. Data Polarity Cross Multiplier Function

PHASE DETECTOR A/D OUTPUT	D/A INPUT		
	TIMES +1	TIMES 0	TIMES -1
0 1 1	0 1 1.1	0 0 0.0	1 0 0.1
0 1 0	0 1 0.1	0 0 0.0	1 0 1.1
0 0 1	0 0 1.1	0 0 0.0	1 1 0.1
0 0 0	0 0 0.1	0 0 0.0	1 1 1.1
1 1 1	1 1 1.1	0 0 0.0	0 0 0.1
1 1 0	1 1 0.1	0 0 0.0	0 0 1.1
1 0 1	1 0 1.1	0 0 0.0	0 1 0.1
1 0 0	1 0 0.1	0 0 0.0	0 1 1.1

NOTES:



A/D CENTRAL THRESHOLD AT ZERO VOLTS DC

NOTE 000.1 ROUNDING ADDED FOR SYMMETRY,
GATED OFF FOR X(0)

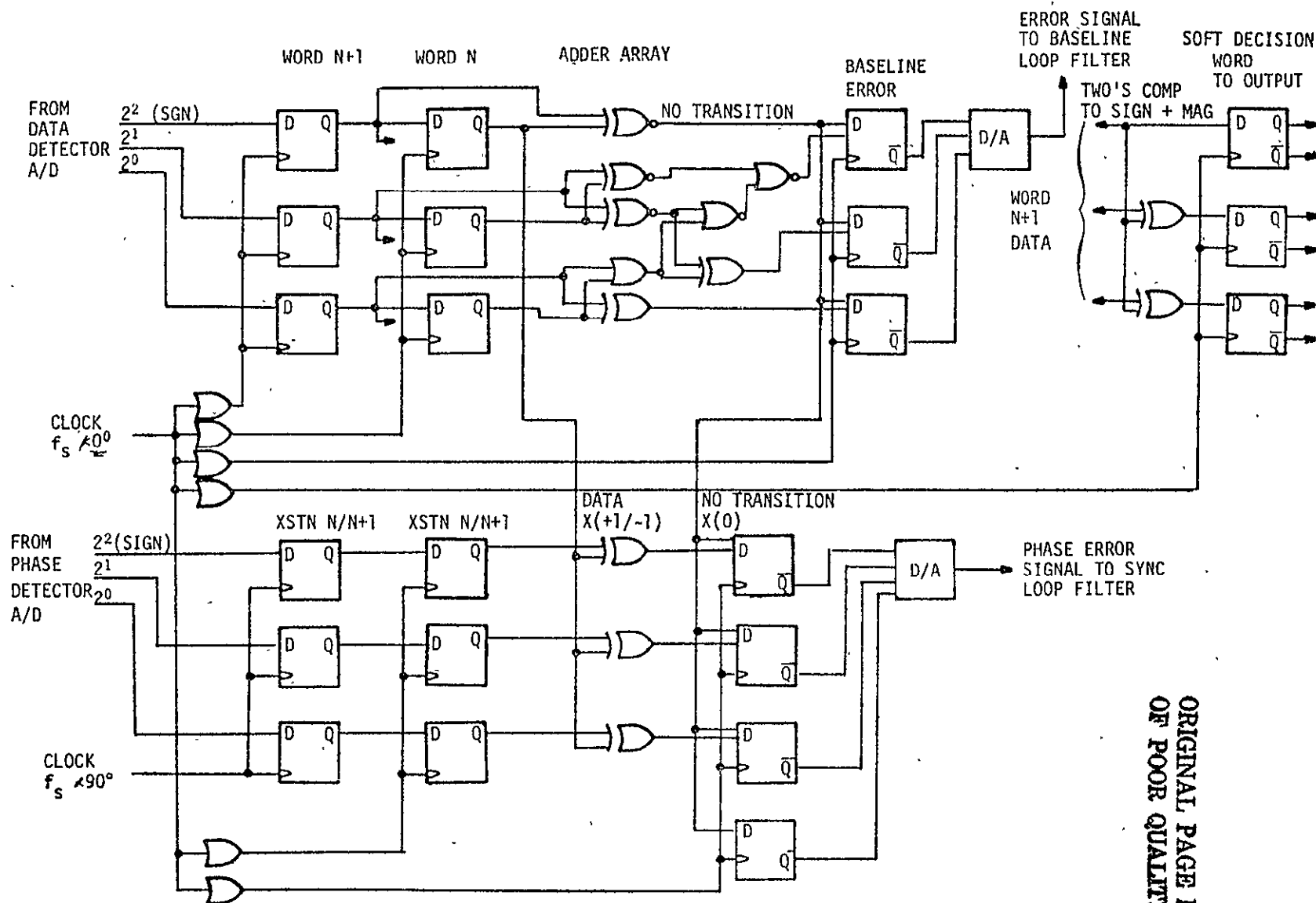


Figure 2-7. Data/Phase Detector Logic

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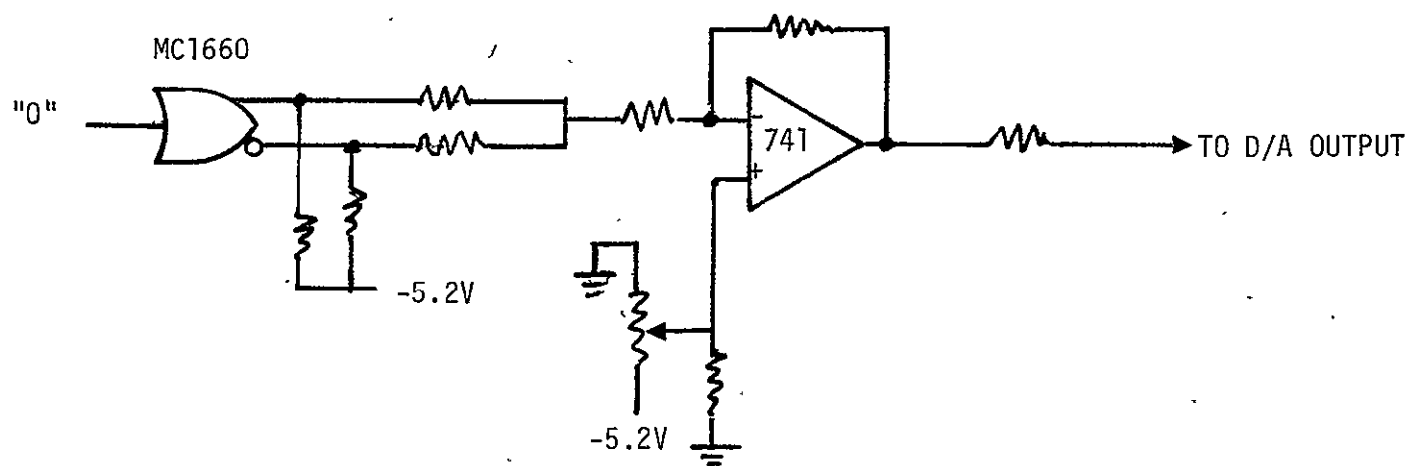


Figure 2-8. Baseline and Phase Error
D/A Converter Offset Cancellation

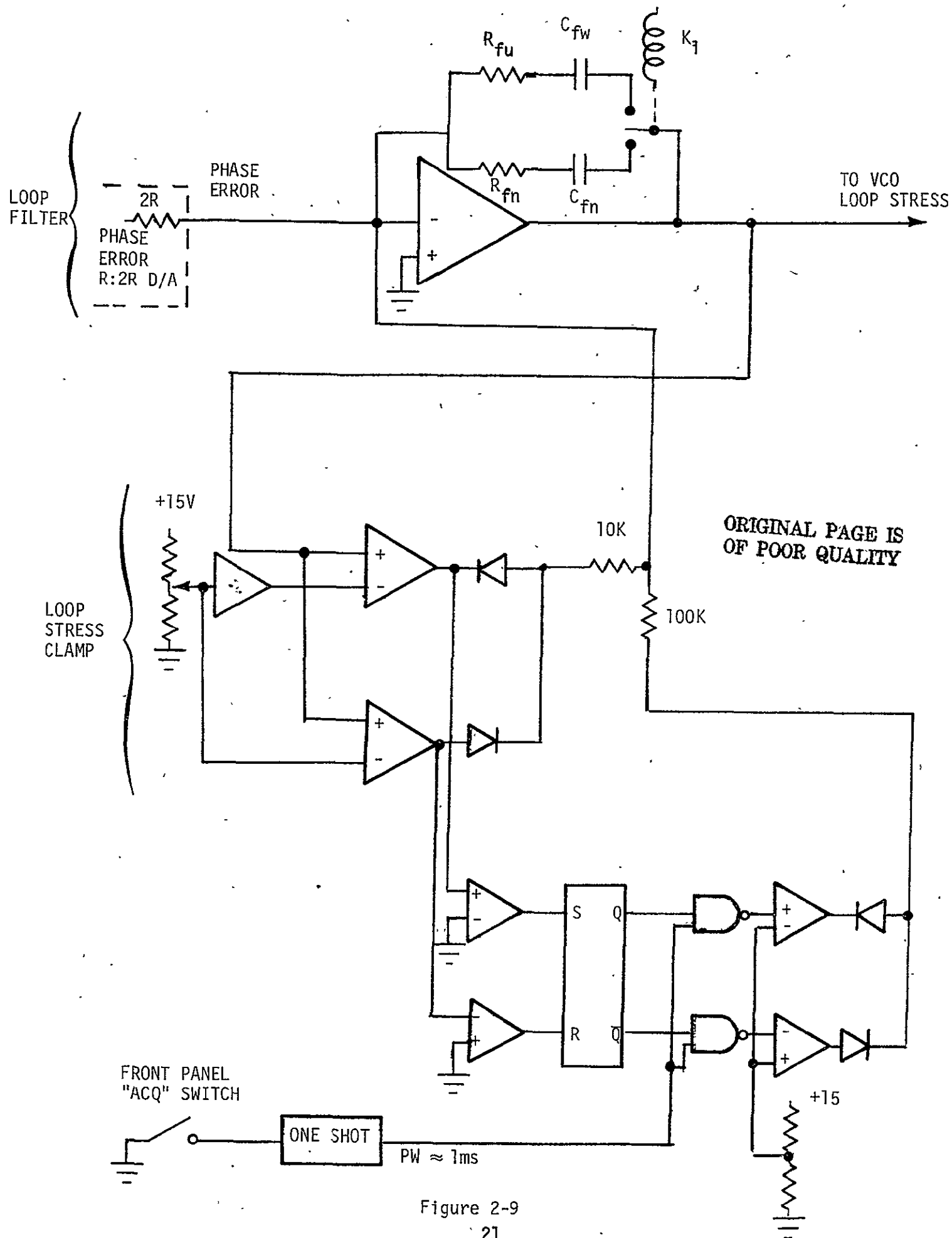


Figure 2-9

positive or negative limit. This limit controls the maximum frequency offset that the VCO can be forced to undergo. It is set at approximately 3.3V and allows the VCO to be at most 0.01% from the nominal bit rate. The second additional circuit is a front panel initiated sweep circuit which, if the synchronizer is out of lock, will force the frequency estimate out of the loop filter to sweep through all possible values for approximately 1 ms. This capability is not generally required but under low SNR and low transition density signal conditions, it may prove to be necessary.

2.6 VCO

The VCO function is obtained in a two-step process whereby the loop stress voltage first proportionally changes the output frequency of an ovenized LC VCO (whose nominal output frequency is 10 MHz). The specification for this device, as purchased from FEI, is shown in Table 2-5. The second stage of the VCO function is a frequency synthesizer which when augmented with a divide by 2^k circuit provides a signal nominally at twice the selected bit rate and which uses the LC VCO output as its reference. A functional block diagram is shown in Figure 2-10.

2.6.1 Frequency Synthesizer

A two-loop approach is used in the frequency synthesizer. (Figure 2-11) where the select loop module provides a 1 MHz step size and the sum loop provides the wide loop bandwidth ($f_n = 300$ KHz) needed for this application. These functions cannot be implemented simultaneously in the same loop because the loop natural frequency, f_n , must be much less than the step size, or sample frequency, f_s , of the loop. Note that the select and sum loops are almost identical except that the select loop does not employ the mixer and comparator stages of the basic module, and the sum loop does not use the divider stages. The sum loop required an additional interface stage (VCO driver) between the loop filter and the VCO, which was built on a small PCB and bolted to the main board. This stage performs the functions of impedance buffering (between the coarse tune sum point and the VCO) and VCO linearization. The buffering is needed to maintain a wide modulation bandwidth for the high f_n . Photographs of the two boards are shown in Figure 2-12 and 2-13, while the specifications are shown in Table 2-6.

Table 2-5. LC VCO Specification

A. ELECTRICAL REQUIREMENTS

1. Center Frequency: 10 MHz
2. Center Frequency Adjustment Range: 9.5 MHz to 10.5 MHz
3. Adjustment Accuracy: Within 5 kHz of center frequency
4. Frequency Stability:
 - a) Long Term (Per Day): 0.02% maximum (2 kHz)
 - b) Long Term (Per Year): 2% maximum (200 kHz)
 - c) Over Temperature: ± 10 PPM per $^{\circ}\text{C}$ maximum (100 Hz)
 - d) Power Supply ($\pm 15\text{V}$): ± 20 kHz per volt maximum
 - e) Stabilization after Power Turn-on: 1 hour
5. VCO Characteristics:
 - a) Pull Range: $\geq \pm 50$ kHz
 - b) Modulation Rate: ≥ 200 kHz (3 dB points)
 - c) Modulation Input Voltage: ± 8 Vdc
 - d) Modulation Sensitivity: 6 kHz ± 600 Hz per volt
 - e) Modulation Linearity: $\pm 2\%$ of full bandwidth (100 kHz)
 - f) Modulation Input Impedance: 500 ohms minimum shunted by 50 pf maximum
6. Output:
 - a) Level: 0dBm ± 1 dB into 50 ohms
 - b) Waveform: Sine wave
 - c) Phase Noise: $\leq 1^{\circ}$ rms in a 1 MHz bandwidth, excluding ± 1 kHz, centered on the carrier
 - d) Harmonic Suppression: -15 dB minimum
 - e) Spurious Outputs: -40 dB minimum

Table 2-5. Continued

7. Temperature:

- a) Operating: 0°C to 70°C
- b) Non-Operating (storage): -20°C to $+80^{\circ}\text{C}$

8. Power Requirement:

- a) VCO: ± 15 Vdc @ 20 ma nominal
- b) Oven: +28 Vdc @ 0.5 amp. maximum

B. MECHANICAL REQUIREMENTS

- 1. Mechanical Tuning: Screwdriver adjust for setting frequency
- 2. Connector Type (output): SMA (3mm)
- 3. "Connector Type" (power input): Feed-thru capacitors
- 4. "Connector Type" (modulation input): Feed-thru terminal
- 5. Size: $3\text{-}1/16"$ x $3\text{-}1/16"$ x $5"$
- 6. Weight: 36 oz.

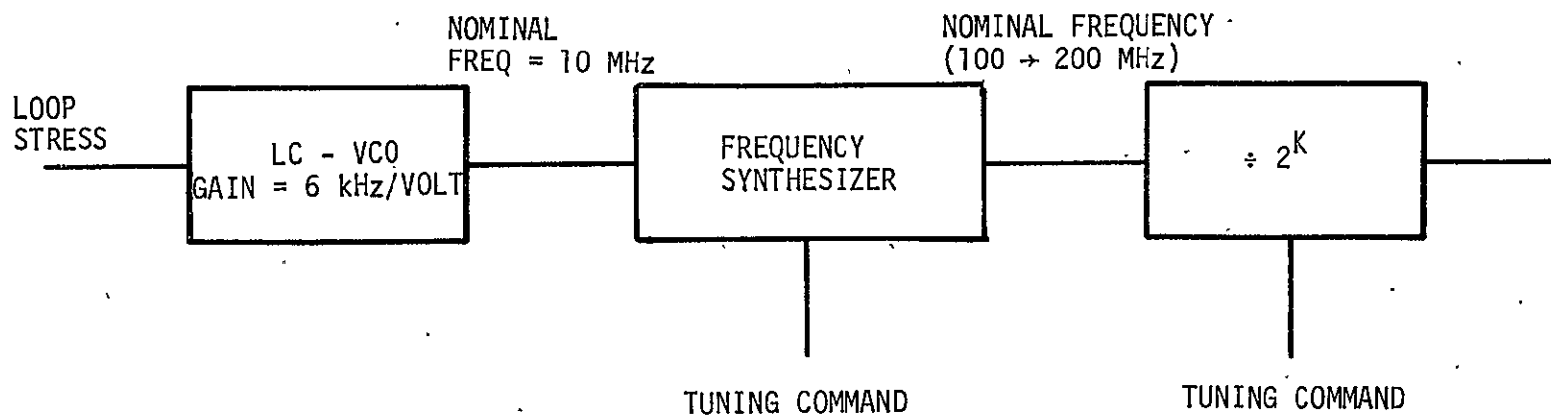


FIGURE 2-10. VCO FUNCTION

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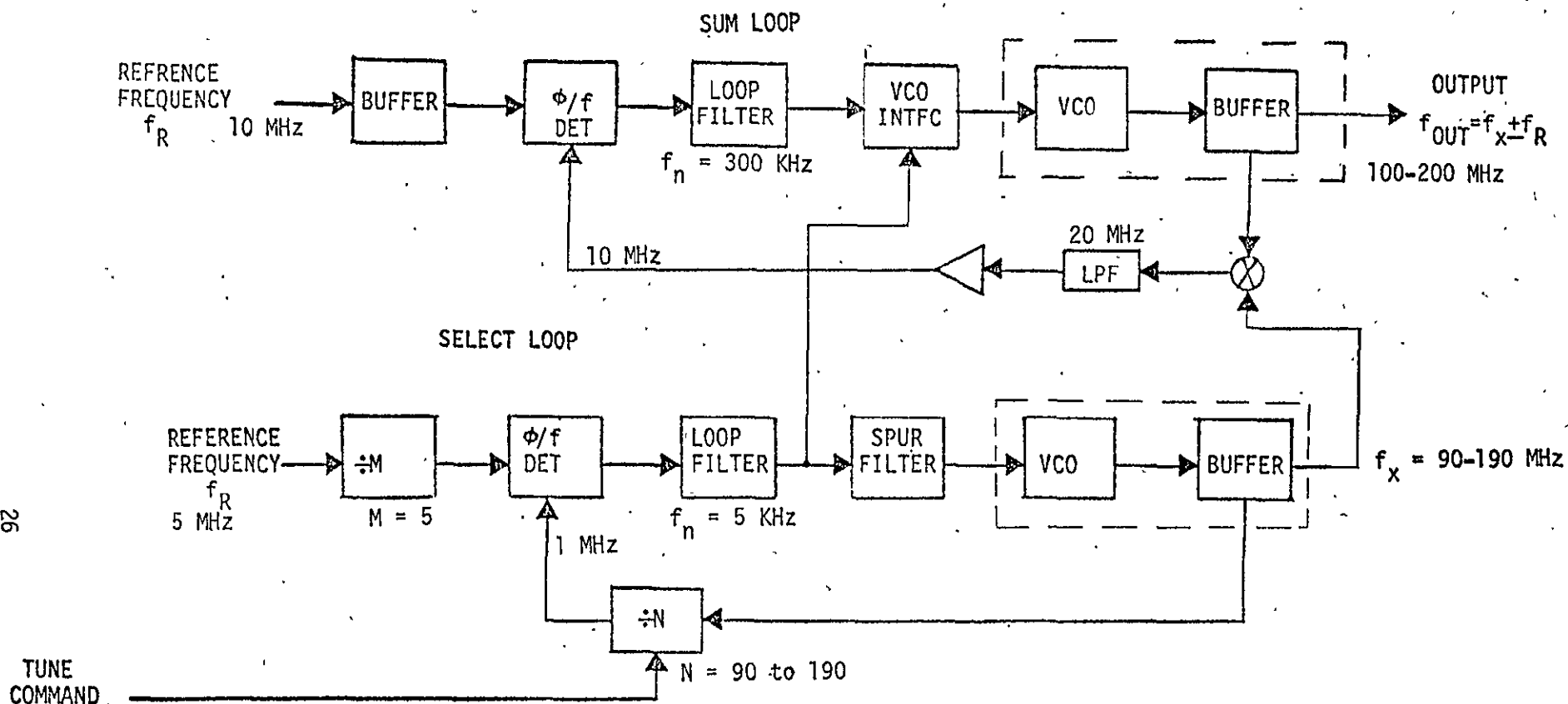


FIGURE 2-11. TWO LOOP VHF SYNTHESIZER USING THE VHF MODULES

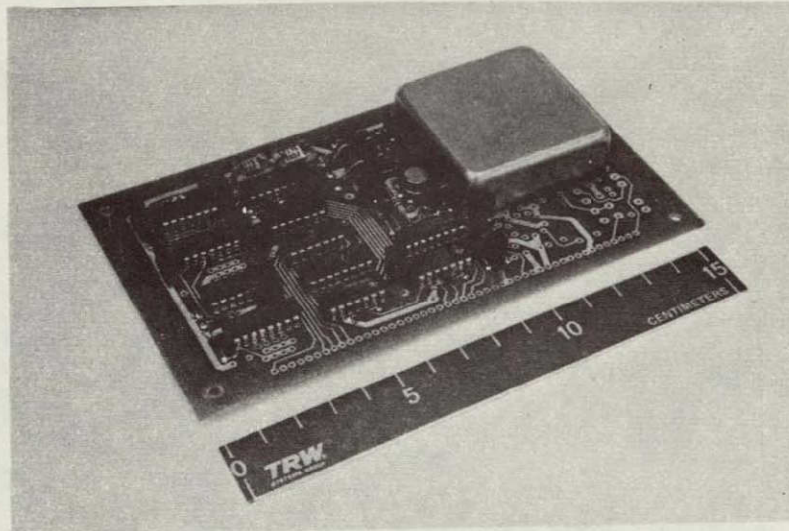


FIGURE 2-12
SELECT LOOP VERSION OF THE VHF SYNTHESIZER MODULE

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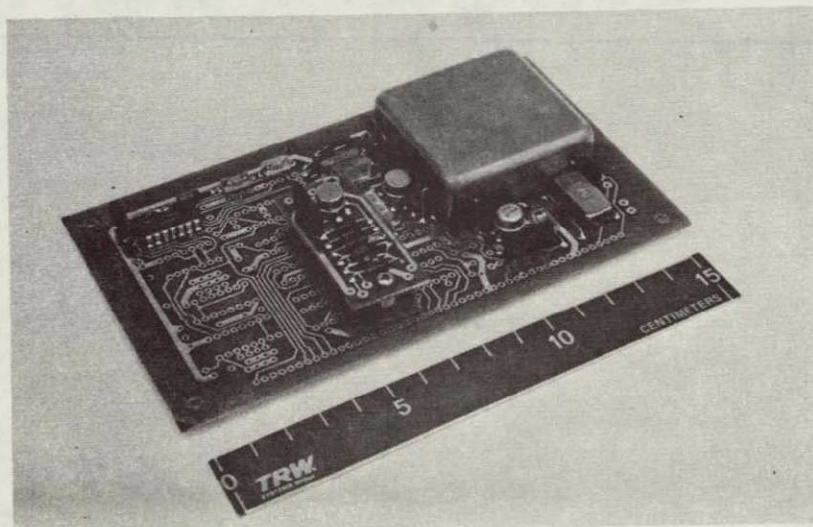


FIGURE 2-13
SUM LOOP VERSION OF THE VHF SYNTHESIZER MODULE

TABLE 2-6
VHF SYNTHESIZER MODULE SPECIFICATIONS

PARAMETER	MODULE CAPABILITY	SELECT MODE	SUM MODULE
<u>OUTPUT</u>			
Frequency	10 - 200 MHz	90 - 190 MHz	100 - 200 MHz
Bandwidth	Octave	100 MHz	100 MHz
Level	ECL	ECL	ECL
Spurs			
Harmonic	-20 dBc	-20 dBc	-20 dBc
Non-Harmonic	-40 to -70 dBc	-40 dBc	-40 dBc
Residual Phase Noise	Depends on VCO, f_n		1.5° RMS
<u>N DIVIDER</u>			
Range	90 - 999	90 - 190	
Frequency	30 - 350 MHz	90 - 190 MHz	
Format	BCD 9's Comp $N = 10 N_p + N_s$ $N_p = 99 - P, N_s = 9 - S$		
<u>M DIVIDER</u>			
Range	2 - 256	M = 5	
Frequency	0 - 13 MHz	5 MHz	
Format	Binary 2's Comp. $M = 256 - M_s$		
<u>PHASE DETECTOR</u>			
Frequency (f_s)	0 - 10 MHz	1 MHz	10 MHz
Output Level	2.1 v/cycle		
<u>LOOP BW (f_n)</u>	$< f_s / 30$ Depends on spur level	5 KHz	300 KHz
<u>MIXER (WJ M6E)</u>			
Offset Frequency	5 to 500 MHz		90 - 190 MHz
I-port Frequency	DC to 500 MHz		10 MHz
<u>COMPARATOR (SE 529)</u>			
Input Frequency	DC to 50 MHz		10 MHz
Input Power (50Ω)	-35 dBm		

2.6.2 Symbol Rate Tuning.

The commands necessary to tune the synthesizer are generated on the front panel via two sets of thumbwheel switches. The first set is coded such that binary multiple of twice the symbol rate (in MHz) is entered. The second set (actually a single thumbwheel switch) is the power of two corresponding to the binary multiple used in the first set. The pertinent information for the four symbol rates of interest are shown in Table 2-7.

2.7 BASELINE OFFSET DETECTOR

The proper function for baseline error sensing is the average sum of detected data values straddling a transition; i.e., if the amplitude of a ONE is 1.0 and of a ZERO is -1.0, the sum is 0.0; for ONE = 1.5 and ZERO = -0.5, the sum is 1.0; and this error signal can be applied through a suitable loop filter to cancel the input offset. Note that to avoid bias due to data statistics (ONE/ZERO balance), it is important to be sure that an equal number of ONE and ZERO levels are used. Thus the sum is gated into the baseline loop filter if and only if their signs differed, (i.e., a transition was present).

With two's complement coding, the problem can be simplified slightly: ignore the two MSBs (signs) and add a single fixed ONE in this position (for they must be different to be used), and add an LSB ONE rather than the two NLSB 0.1_2 which were appended (conceptually) for rounding. Also, to thus add two two-bit words plus a 101_2 constant, direct logic mapping using gates is chosen in lieu of an adder since they are too slow. Figure 2-14 depicts the derivation of this gate network.

Having derived the error signal in digital form, it remains to utilize it to drive a control loop filter. Digital and analog methods were considered, and the analog technique selected in the interest of lower cost for the development of the brassboard. Digital loop filters to handle the 100 Msps rate are complex but use of custom LSI could solve this problem.

The baseline loop filter is similar to that of the sync loop in that it is driven from an R-2R D/A converter. It is shown in Figure 2-15. The component values were chosen to allow at most the tracking of baseline variation rates of 5 KHz. This limitation is imposed by the selection of what in fact

Table 2-7. Symbol Rate VCO Control

SYMBOL RATE	TWICE SYMBOL RATE	BINARY MULTIPLE OF TWICE THE SYMBOL RATE	
		VALUE ($L-2^n$)	POWER OF 2 (n)
100	200	1	0
60	120	1	0
30	120	2	1
20	160	4	2

		WORD N+1							
		+3.5	+2.5	+1.5	+0.5	-0.5	-1.5	-2.5	-3.5
WORD N	+3.5	7	6	5	4	3	2	1	0
	+2.5	6	5	4	3	2	1	0	-1
	+1.5	5	4	3	2	1	0	-1	-2
	+0.5	4	3	2	1	0	-1	-2	-3
	-0.5	3	2	1	0	-1	-2	-3	-4
	-1.5	2	1	0	-1	-2	-3	-4	-5
	-2.5	1	0	-1	-2	-3	-4	-5	-6
	-3.5	0	-1	-2	-3	-4	-5	-6	-7

(a)

ONLY THE PAIRS N, N+1 WITH CHANGED SIGN ARE USED. NOTE THE 32 RESULTING STATES MAP INTO SIXTEEN STATES WHEN THE SIGN AND ROUNDING BITS ARE ADDED SEPARATELY, AS IN (b)

		WORD N+1*			
		11	10	01	00
WORD N*	11	011	010	001	000
	10	010	001	000	111
	01	001	000	111	110
	00	000	111	110	101

* STRIPPED OF SIGN AND ROUNDING BITS

(b)

Figure 2-14. Successive-Symbol Adder Logic Derivation

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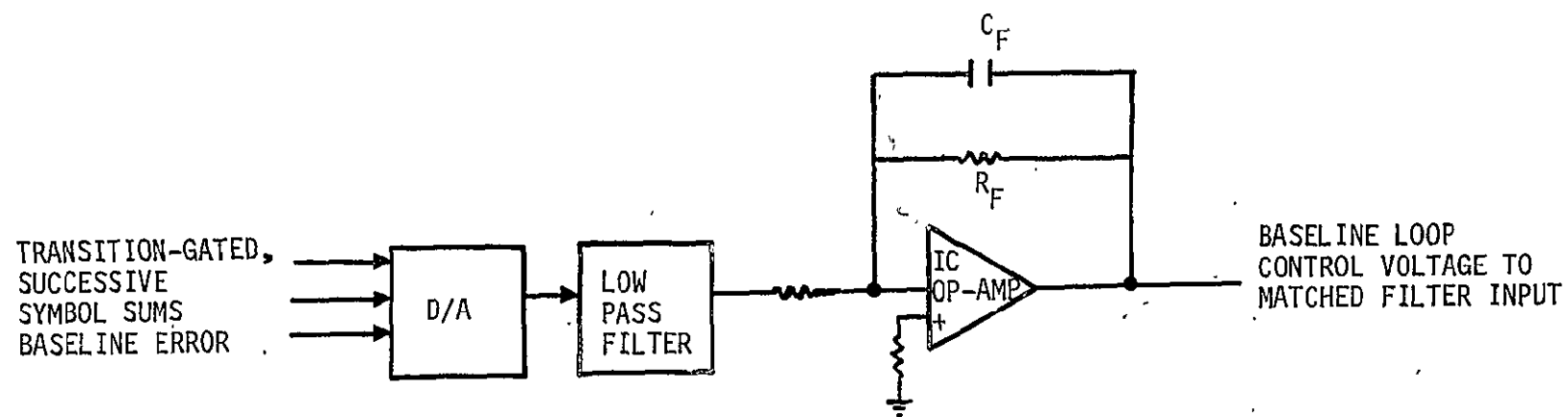


FIGURE 2-15. BASELINE LOOP FILTER

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is a relatively low gain D/A converter and an operational amplifier having only 20 MHz of unity gain bandwidth. Other combinations could be used to obtain tracking at higher baseline variation rates. However, it is felt that in most cases it is unnecessary since sources of baseline variation generally are either related to power-supply ripple (60 - 400 Hz) or to thermal drift (~ 1 Hz) and a 5 KHz capability can certainly track these.

2.8 LOOP DYNAMICS

The symbol synchronizers' phase locked loop behaves as a classic second order phase locked loop with damping and noise bandwidth determined by the selection of the time constants in the loop filter. The unit provides for the front panel selection of two bandwidths, wide and narrow, which switch a different set of components (via a relay) into the feedback path of the loop filter's operational amplifier. The selected values of these components is as shown in Table 2-8.

Table 2-8

Symbol Rate	Bandwidth	R_f	C_f
100 Msps	Wide	20K	0.012 μ f
	Narrow	10	0.048
60 Msps	Wide	20	0.02
	Narrow	10	0.08
30 Msps	Wide	20	0.04
	Narrow	10	0.16
20 Msps	Wide	20	0.06
	Narrow	10	0.24

3.0 TEST RESULTS

The tests data obtained on the 100 MSPS symbol synchronizer falls into two categories, that of evaluation of individual functions within the synchronizer and that of evaluation of the performance of the unit as a symbol synchronizer. With respect to the first category, the items to be presented include the AGC, Transversal Filter, A/D Converter, Phase Detector and the VCO's Frequency Synthesizer. The latter includes BER performance and a brief discussion of acquisition time.

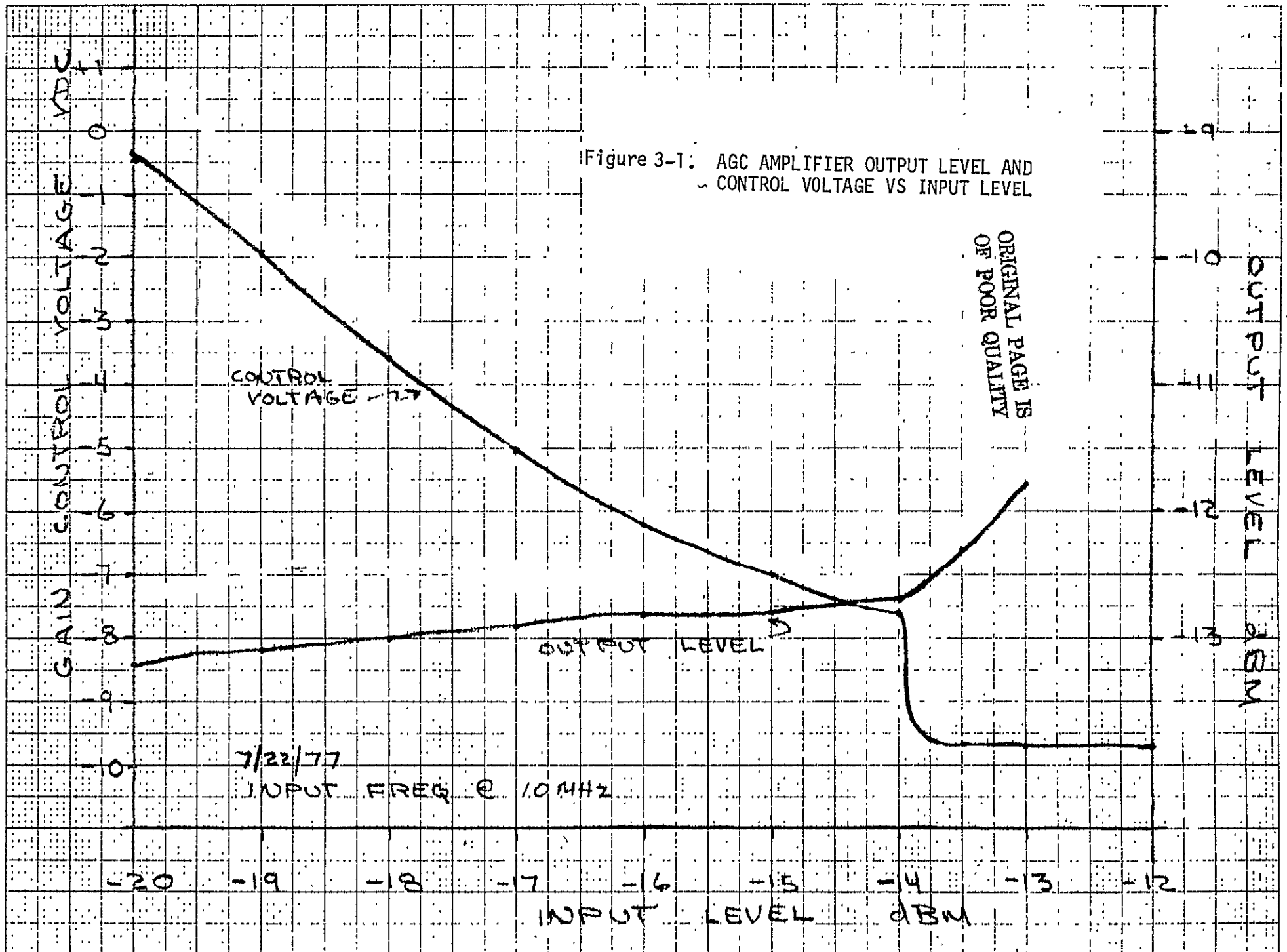
3.1 FUNCTIONAL TESTS

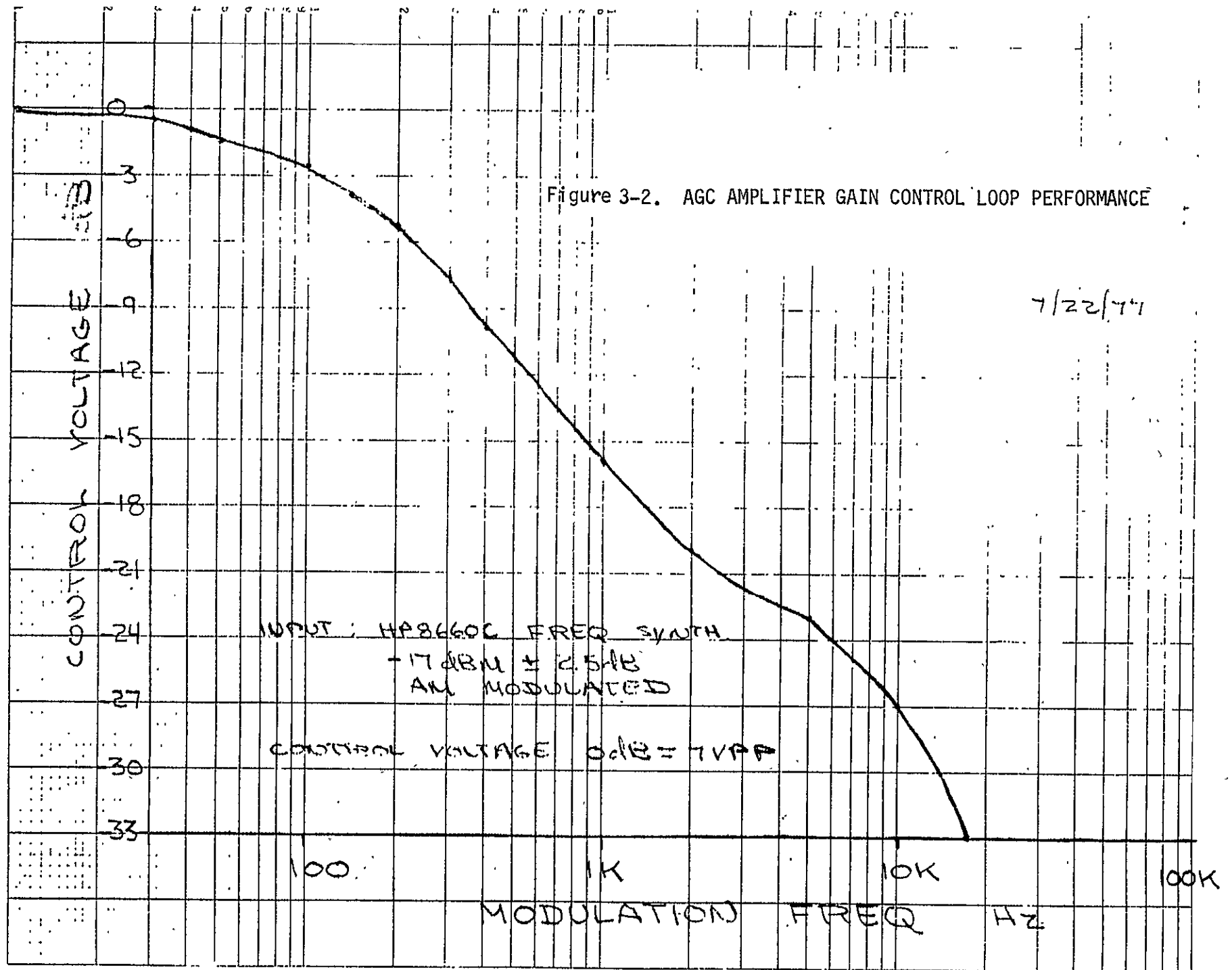
3.1.1 AGC Evaluation

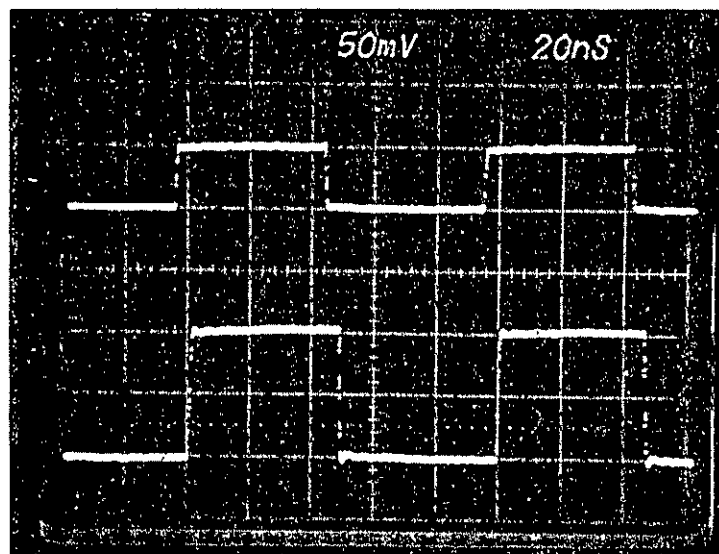
The ability of the AGC amplifier to control the drive level on its output is shown in Figure 3-1 where the input is varied over an 8 dB range and the output remains constant (to within a ± 0.25 dB) for 6 dB of that range. The operating range of the control voltage is shown to be between -0.5 and -8.5 volts. This quantity is displayable on the front panel's DVM and as such is useful in determining if the manual AGC is properly set.

AM modulation of the input signal yields the plot of control voltage vs modulating frequency shown in Figure 3-2. A rough estimate of the -3 dB corner of the AGC control characteristic can be obtained as the frequency at which the ac component control voltage (at the modulating frequency) is 3 dB down from its low frequency value. This can be seen to occur at approximately 100 Hz. Thus the AGC can be expected to track out any amplitude variations which change at a rate of approximately 100 Hz or less.

A second evaluation tool for the AGC is to examine its transient response. Of necessity this must be done in both the maximum and minimum gain configuration since a difference exists. Figures 3-3 to 3-6 show this data for the two signal level conditions and for two extreme signal patterns, one an alternation NRZ "10" pattern at 20 MSPS (Figures 3-3 and 3-4) and second the same pattern at 200 MSPS, (Figures 3-5 and 3-6) a factor of 2 higher than necessary. As can be seen, there is significant ringing for the minimum gain signal level and that this is more pronounced at the higher symbol rates. Some degradation may result at maximum symbol rate and maximum signal level. However keep in mind that the NRZ symbols of Figures 3-4 and 3-6 are twice as narrow as will occur at the maximum symbol rate of 100 MSPS and thus the effect will not be as pronounced as the figures seem to indicate.





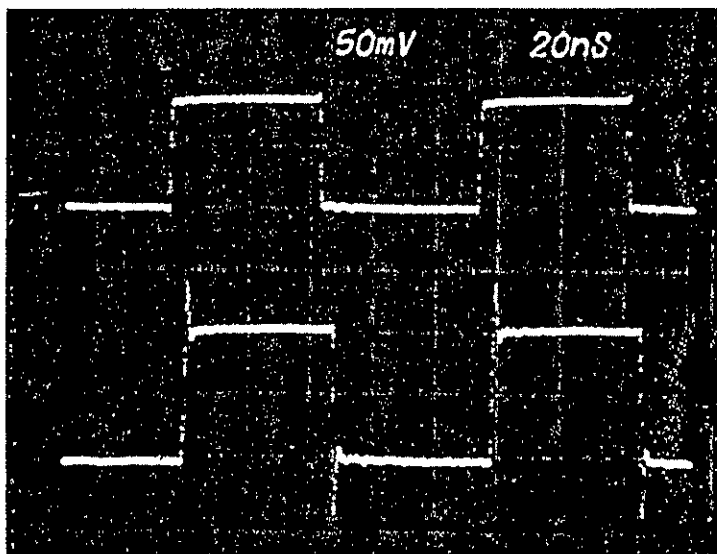


TOP - INPUT
10 MHz SQ. WAVE

BOTTOM - OUTPUT

37" OUTPUT CABLE
S6A SAMPLING HEAD

Figure 3-3. PULSE RESPONSE, MAXIMUM GAIN 50 ns PULSE

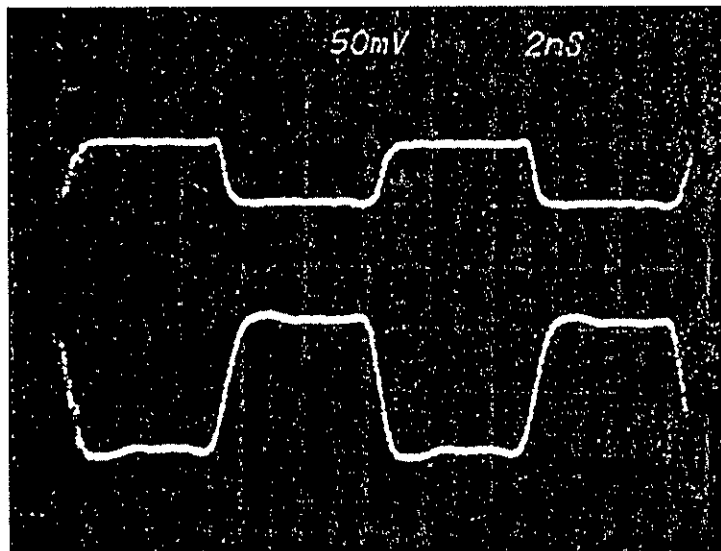


TOP - INPUT
10 MHz SQ. WAVE

BOTTOM - OUTPUT

37" OUTPUT CABLE
S6A SAMPLING HEAD

Figure 3-4. PULSE RESPONSE, MINIMUM GAIN 50 ns PULSE

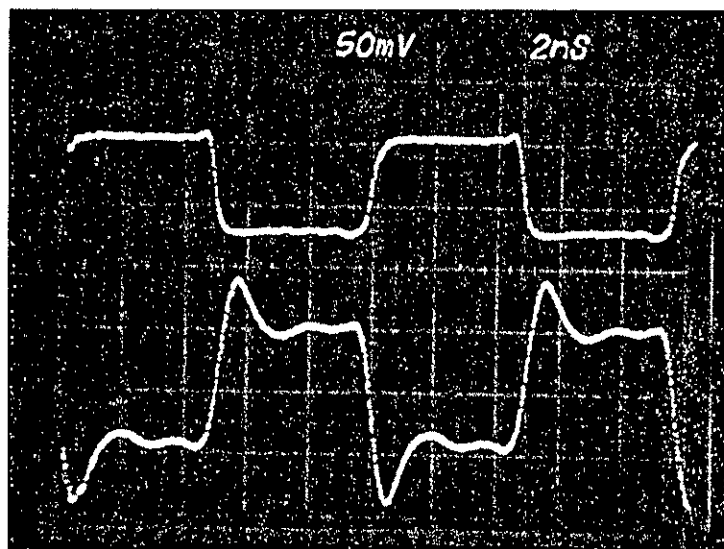


TOP - INPUT
100 MHz SQ WAVE

BOTTOM - OUTPUT

37" OUTPUT CABLE
S6A SAMPLING HEAD

Figure 3-5. PULSE RESPONSE, MAXIMUM GAIN (5 ns PULSE)



TOP- INPUT

100 MHZ SQ WAVE

BOTTOM - OUTPUT

37" OUTPUT CABLE
S6A SAMPLING HEAD

Figure 3-6. PULSE RESPONSE, MINIMUM GAIN (5 ns PULSE)

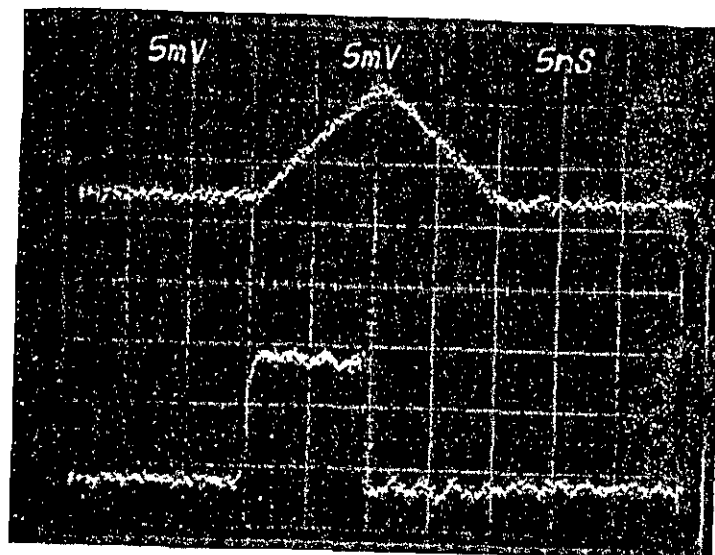
3.1.2 Transversal Filter

Techniques used to evaluate the transversal filter include the transient and frequency response of the 100 MSPS filter and the frequency response of the 20, 30, or 60 MSPS filter.

The transient response input conditions and corresponding filter outputs are: 1) a single 10 ns NRZ "1" preceded and followed by "0"'s (Figure 3-7); 2) a sequence of 8 "1"'s followed by 8 "0"'s (Figure 3-8); and 3) the same pattern as in 2 except that just the rising edge of the filter's output is displayed (Figure 3-9). Interesting observations of Figure 3-8 include the fact that the output is triangular as expected and that it is symmetrical about its midpoint indicating all 8 gains of the 8 tap filter are matched. Figure 3-9 shows that there is a slight decrease in detected signal level whenever there is a transition but that it is less than 5%. Figure 3-10, by virtue of its extremely linear response, indicates that all taps are, indeed, uniformly weighted.

The frequency response plots at all 4 symbol rates is shown in Figures 3-11, -12, -13, and -14. As the symbol rate decreases, the tuning becomes more accurate in that the first null is progressively closer to the designed symbol rate. However, even at 100 MSPS (Figure 3-11) the deviation is only 3% while the equivalent noise bandwidth was found to be 13% low. Additional iterations in the cutting of the delay lines could reduce the deviations.

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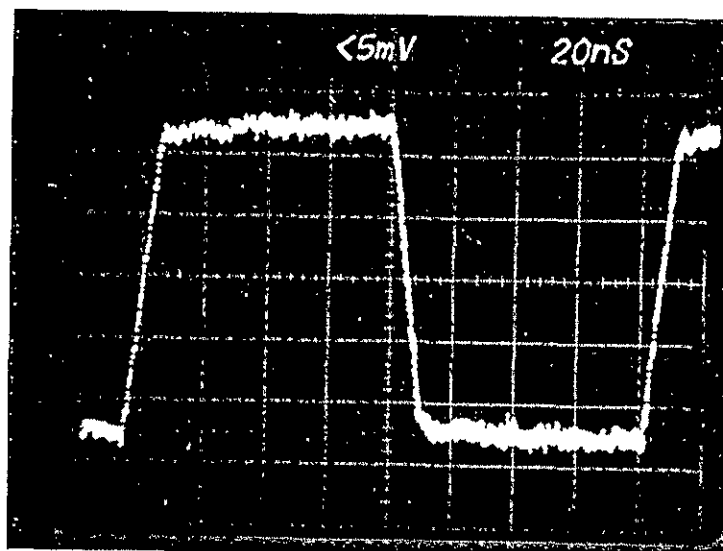


TOP - OUTPUT
 5 mv x 34/CM
 S6 SAMPLING HEAD

BOTTOM - INPUT
 5 mv x 25/CM
 S4 SAMPLING HEAD
 EH 129 Pulse Generator
 INPUT 10 ns PW

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FIGURE 3-8. TRANSVERSAL FILTER IMPULSE RESPONSE

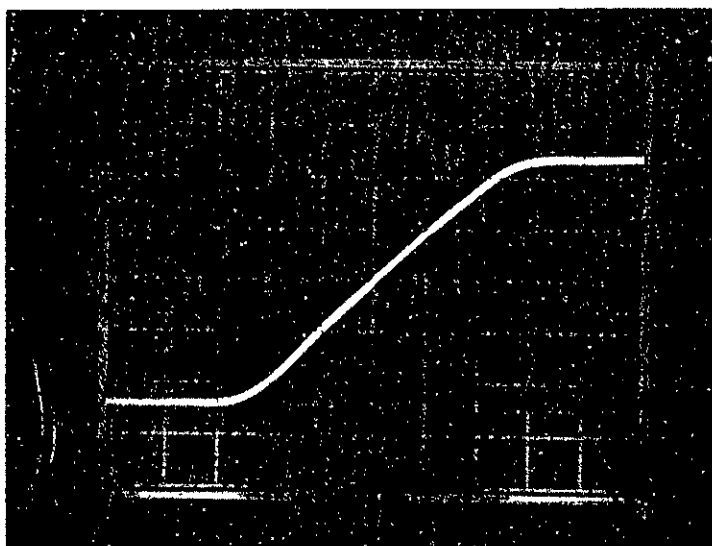


..... 100%

OUTPUT
 $\approx 5 \text{ mv} \times 34/\text{CM}$

..... 0% S6 SAMPLING HEAD
 EH 129 INPUT

FIGURE 3-9. TRANSVERSAL FILTER SQUARE WAVE RESPONSE



.... 100%

OUTPUT

2 mv x 34/CM

2 ns/CM

TEK 475 SCOPE

..... 0%

-4-

FIGURE 3-10. TRANSVERSAL FILTER STEP RESPONSE

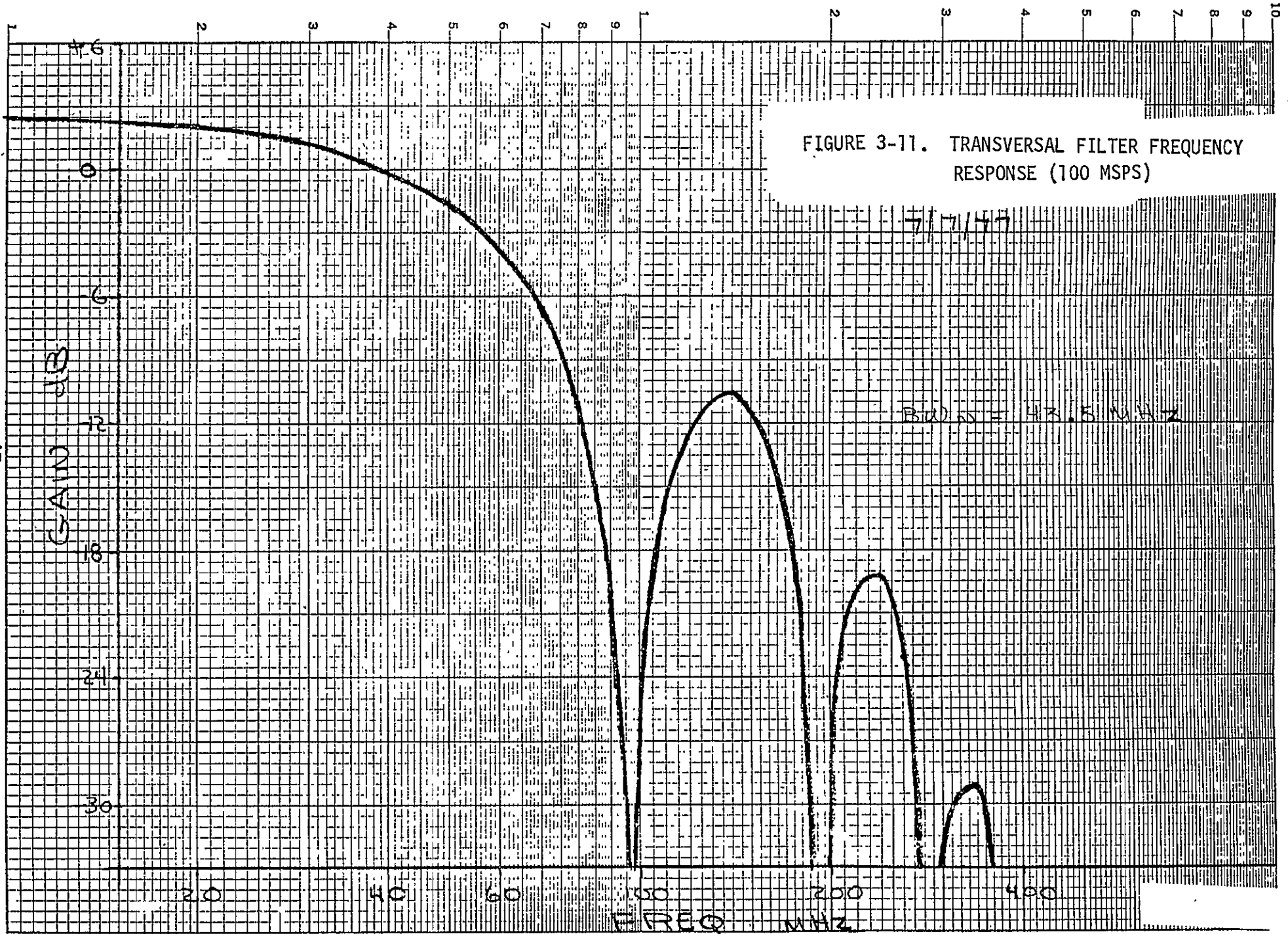


FIGURE 3-11. TRANSVERSAL FILTER FREQUENCY
 RESPONSE (100 MSPS)

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BW = 43.8 MHz

47

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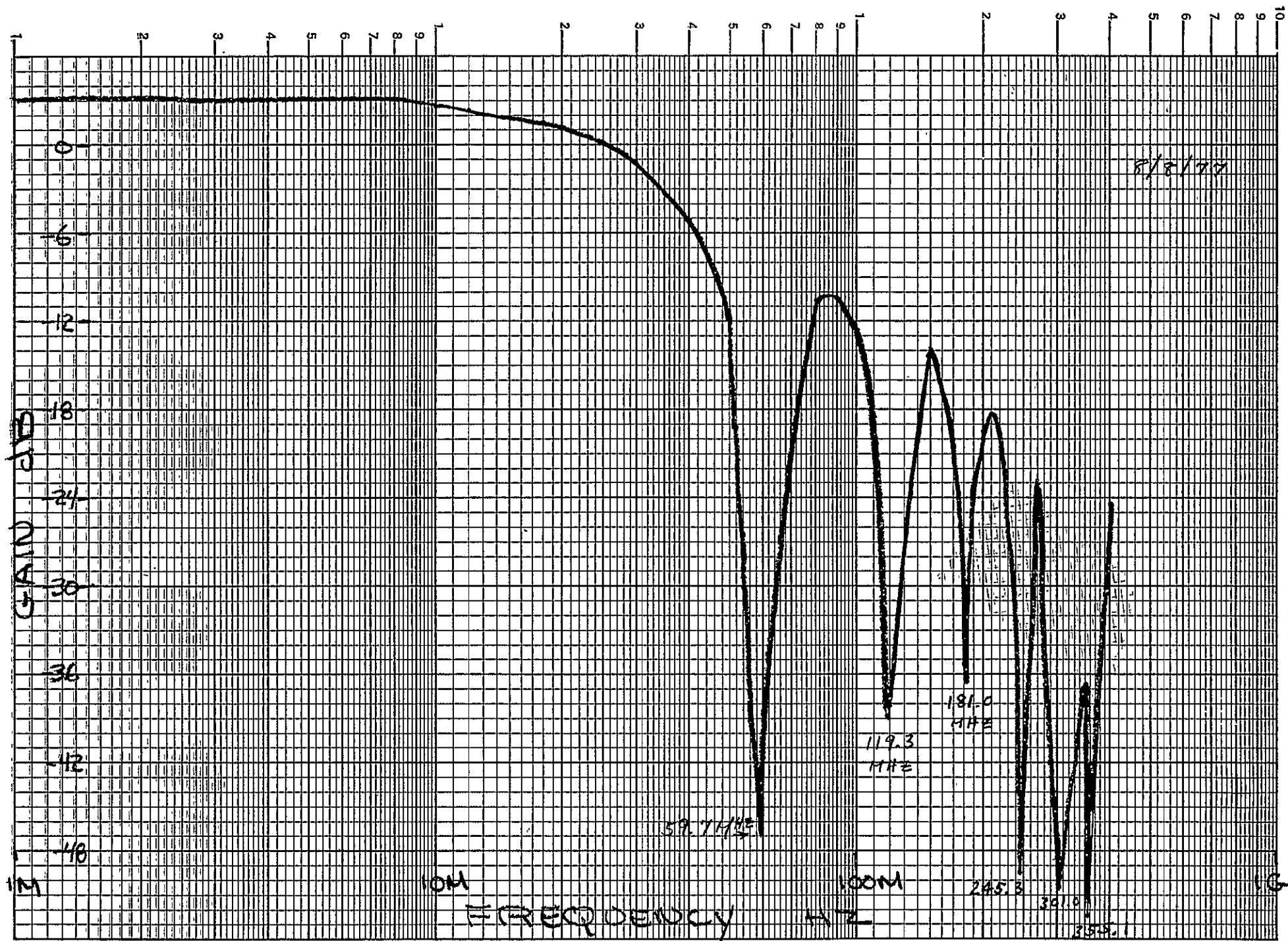


FIGURE 3-12. TRANSVERSAL FILTER FREQUENCY RESPONSE (60 MSPS)

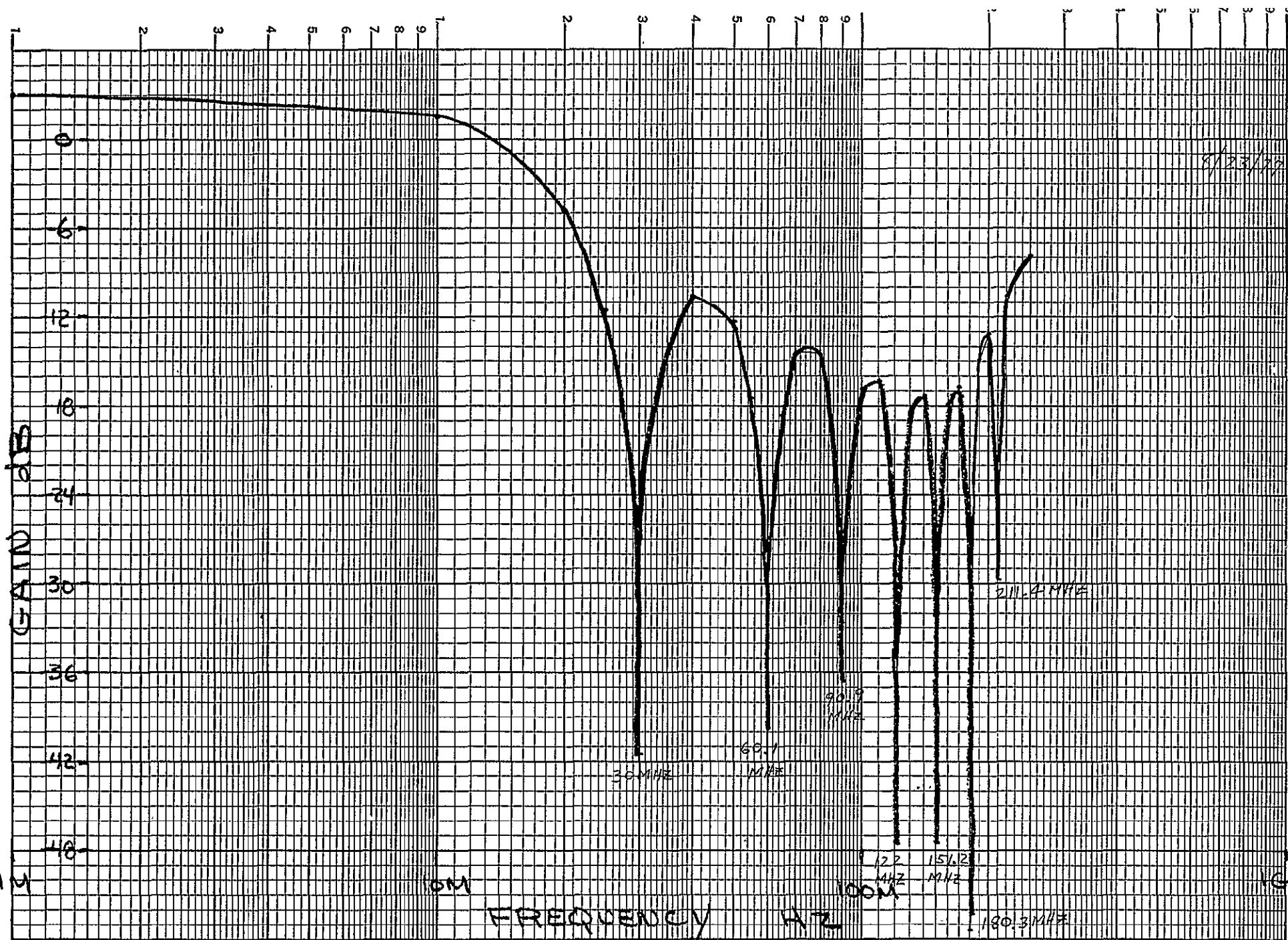


FIGURE 3-13. TRANSVERSAL FILTER FREQUENCY RESPONSE (30 MSPS)

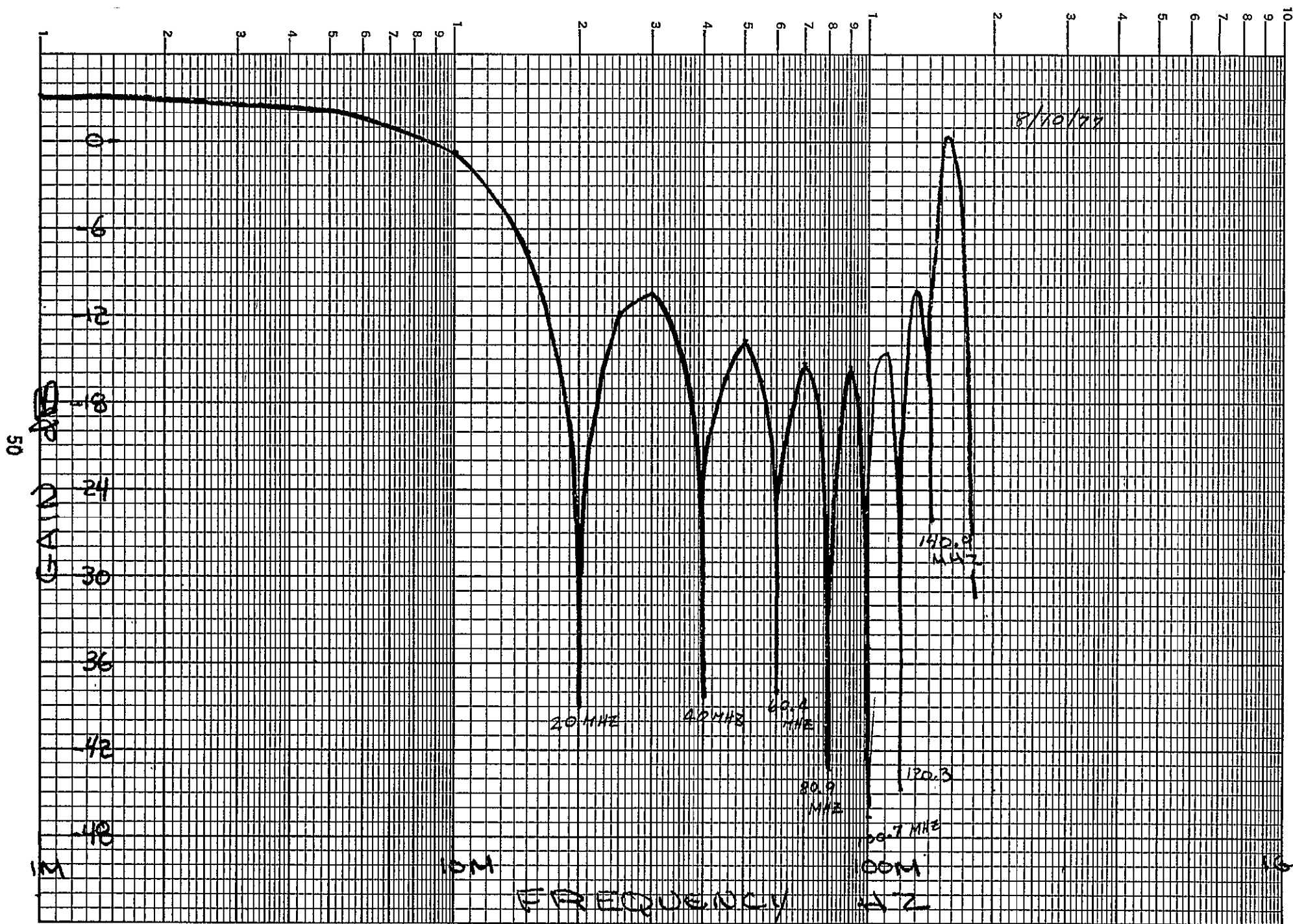


FIGURE 3-14. TRANSVERSAL FILTER FREQUENCY RESPONSE (20 MSPS)

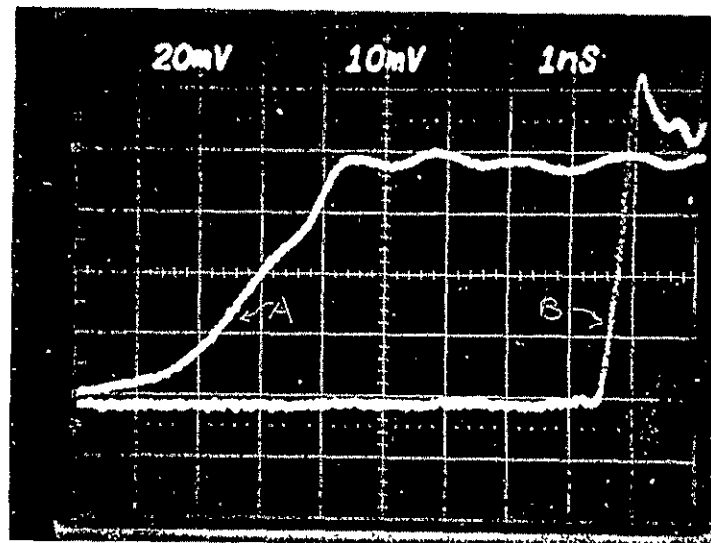
3.1.3 A/D Converter

Critical issues in the design of the A/D converter function are that the device is properly clocked with an extremely fast rising edge and that the device yield a linear response to an analog input.

Clock edge conditions were tested and as shown in Figure 3-15a and 3-15b are quite adequate. The rising edge can be seen to be less than 0.5 ns and the data can be observed to be stable 3 ns after the clock rises. Thus the latches which follow have a 2 ns window in which to be clocked and store the data. This timing relationship is obtained by appropriate asynchronous delays of the various clocks.

A/D linearity is tested as defined in Figure 3-16a and the results are shown in Figure 3-16b. When the uniformity of the quantization levels can be observed. More detailed testing has yielded the data in Figure 3-17 under static conditions and two extreme A/D loading situations. The nominal A/D loading is at approximately $T = 40$ mV and the maximum deviation (as a percent of a step size) is on the order of 10%. This is a negligible source of error and in fact shows the ability of the A/D to operate with a 50% threshold error at step sizes down to approximately 5 mV if a linear relationship is assumed.

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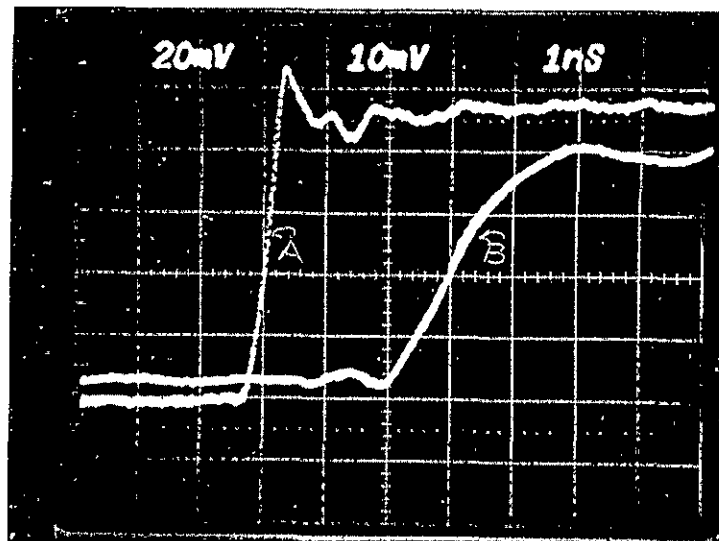
A - 2BR Clock Input

B - 3BQ Clock

20 MHz Input Clock

X10 Probes

FIGURE 3-15a. A/D TIMING: CLOCK GENERATOR



A - 3 BQ Clock

B - Buffered
3BQ 2⁰ Data

20 MHz Input Clock

X10 Probes

10 MHz Analog Input (Sq. wave)

FIGURE 3-15b. A/D TIMING: CLOCK TO DATA DELAY

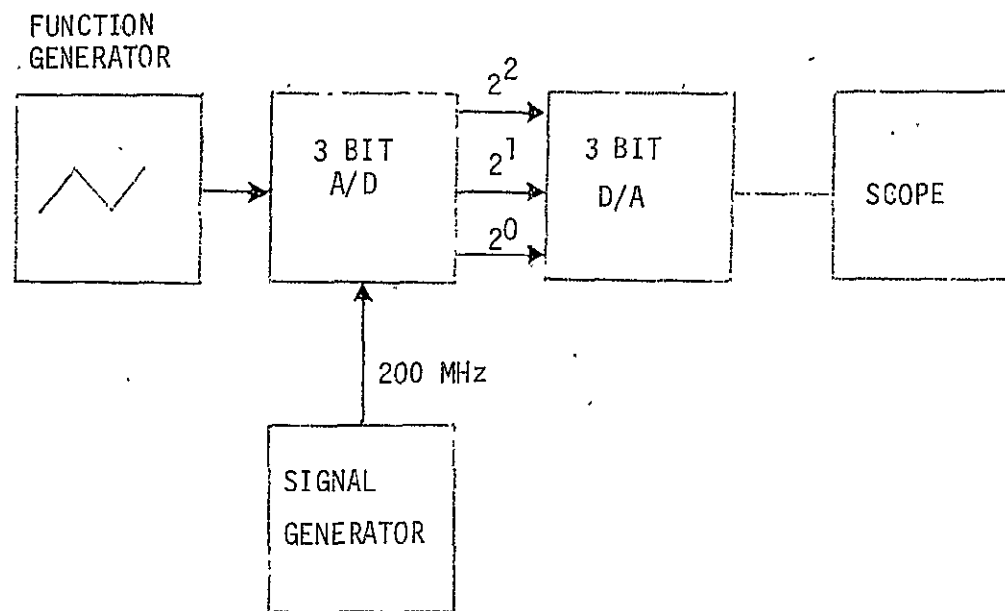
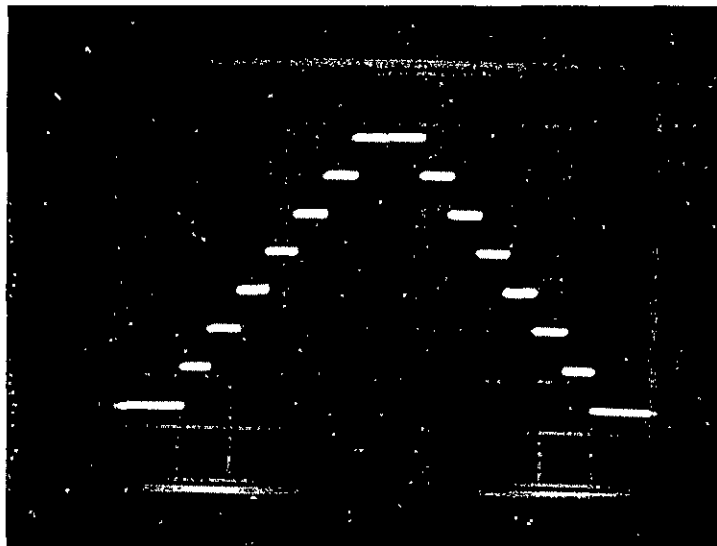


FIGURE 3-16a. A/D DYNAMIC LINEARITY TEST SETUP

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3 BIT A/D
80 mv Q Steps

$+V_{REF} = 240 \text{ mv}$

$-V_{REF} = 400 \text{ mv}$

FIGURE 3-16b. A/D DYNAMIC LINEARITY TEST RESULTS

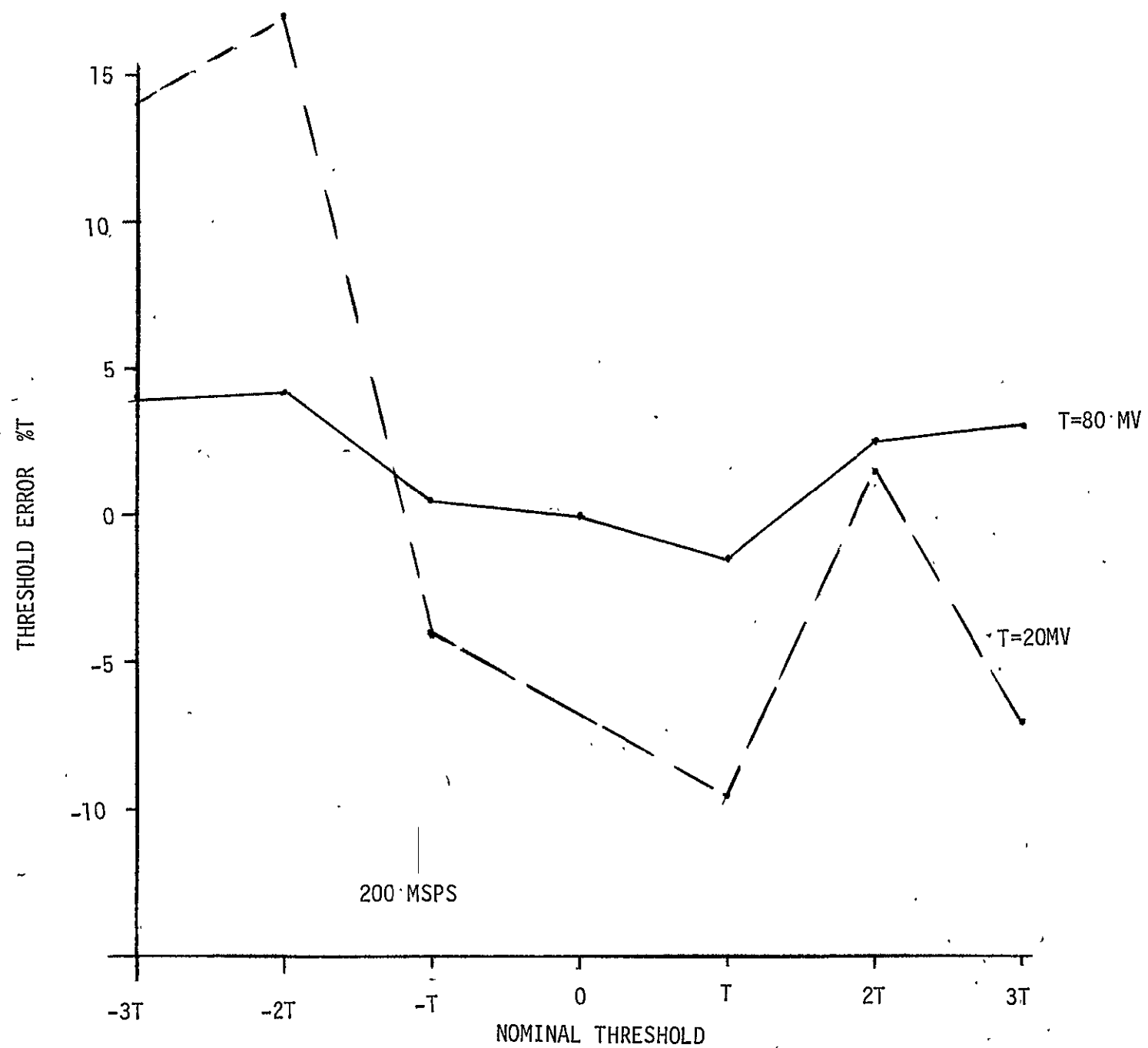
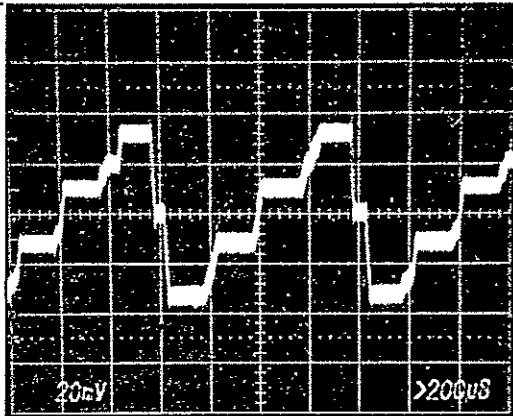


FIGURE 3-17. A/D STATIC LINEARITY TEST RESULTS

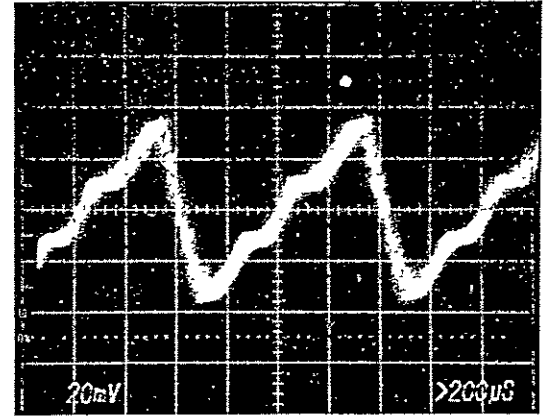
3.1.4 Phase Detector

A valuable means of characterizing the phase detector is to drive the data source (with NRZ "10" data pattern) and the symbol synchronizer from separate frequency synthesizers having a known frequency difference. The resulting beat note at the phase detector output displays the amplitude vs phase offset. The eventual lock point for the synchronizer is where the amplitude of the phase detector output is zero and the slope is positive. The 180° out of lock points are where the magnitude is again zero but the slope is negative. A set of such curves is shown in Figure 3-18 at four SNR's of interest. Notice that at high SNR the beat note is quite non linear but as noise is added, the curve is linearized.

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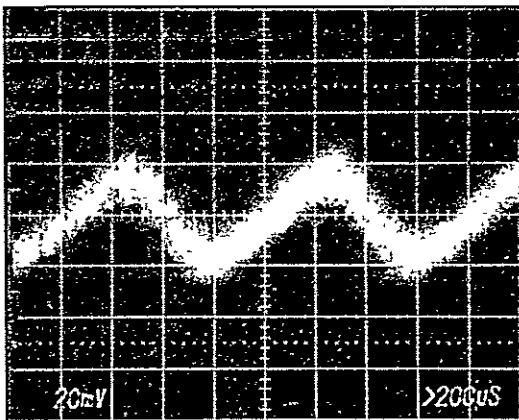


SNR $\approx \infty$

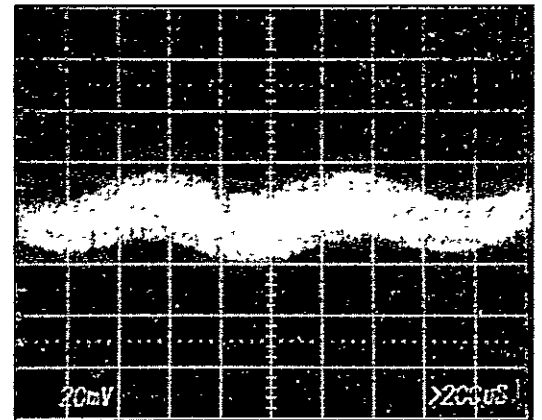


SNR ≈ 17 dB

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SNR ≈ 7 dB



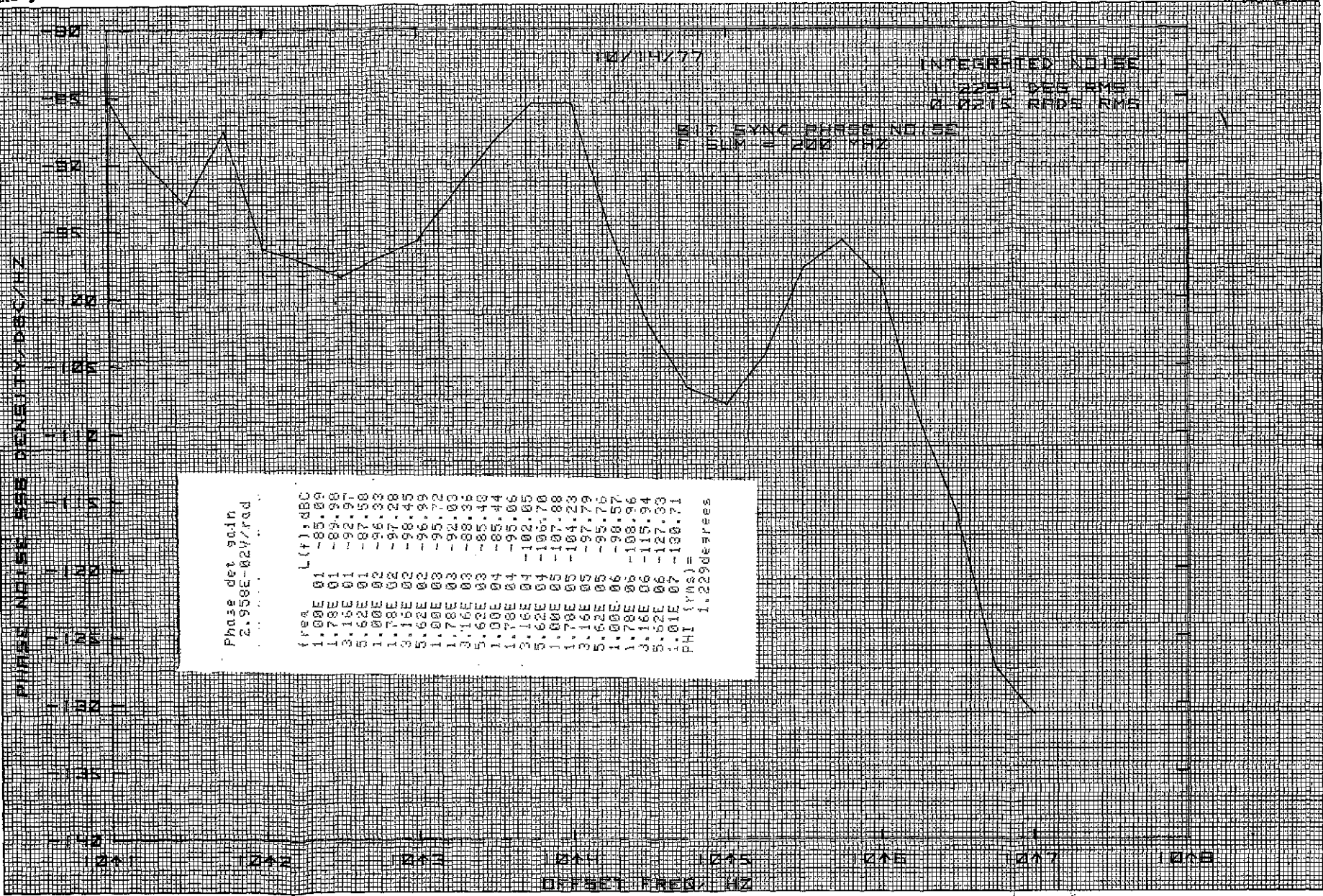
SNR ≈ -2 dB

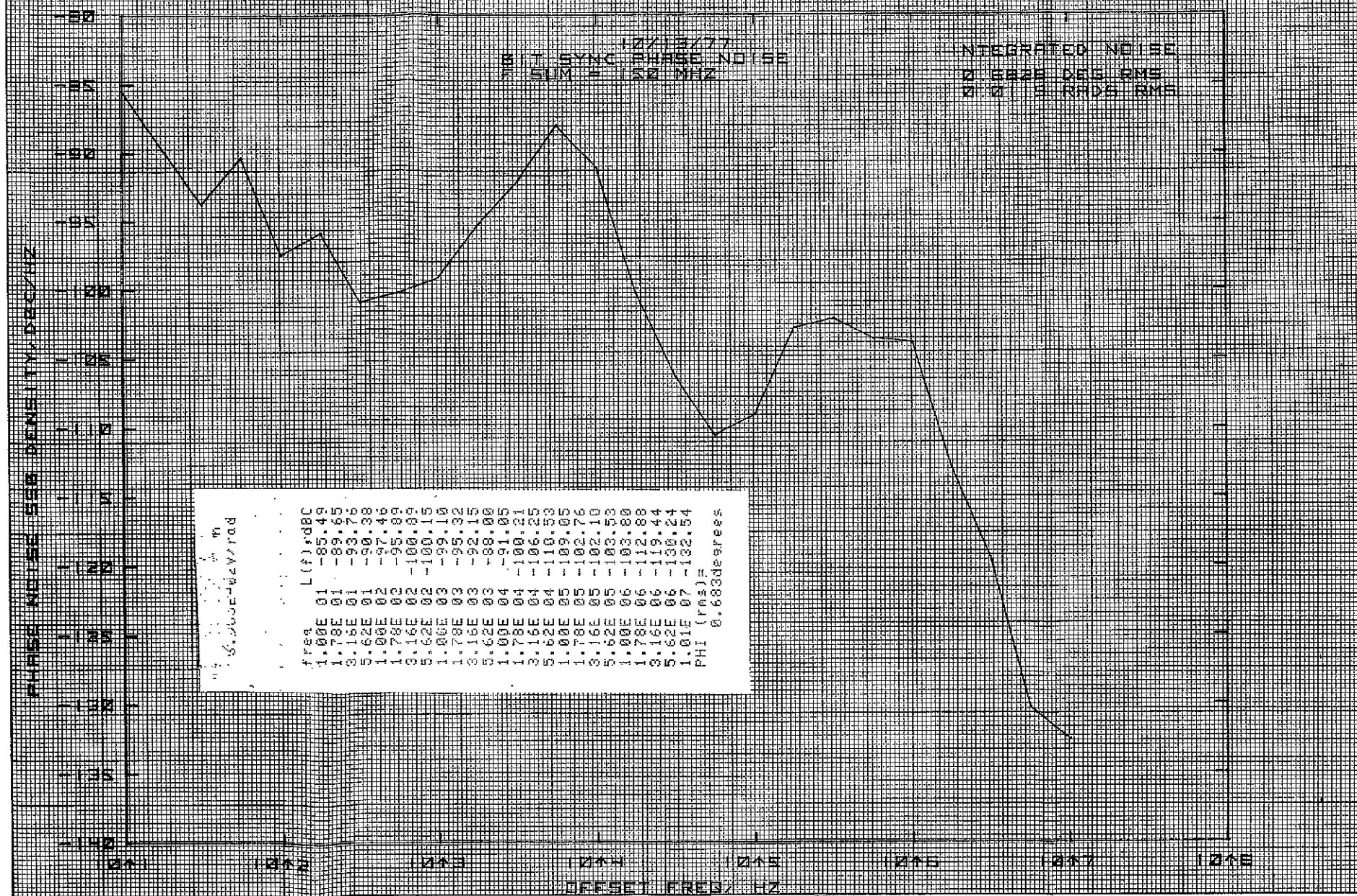
FIGURE 3-18. PHASE DETECTOR CORRELATION CURVES

3.1.5 VCO Frequency Synthesizer

Phase noise data was taken on the two loop VHF Synthesizer for sum VCO frequencies of 100 MHz, 150 MHz, and 200 MHz shown in Figures 3-19, -20, and -21. The graphs display two broadband noise peaks, the first being due to the select loop noise and the second to the sum loop. At 100 MHz, the noise peaks occur at frequencies higher than the design loop natural frequencies due to the large VCO gain at that point. (The single breakpoint linearizer allows a 6 dB variation in VCO gain.) The integrated residual phase noise results in an rms phase jitter of less than 1.5 degrees for all measured frequencies.

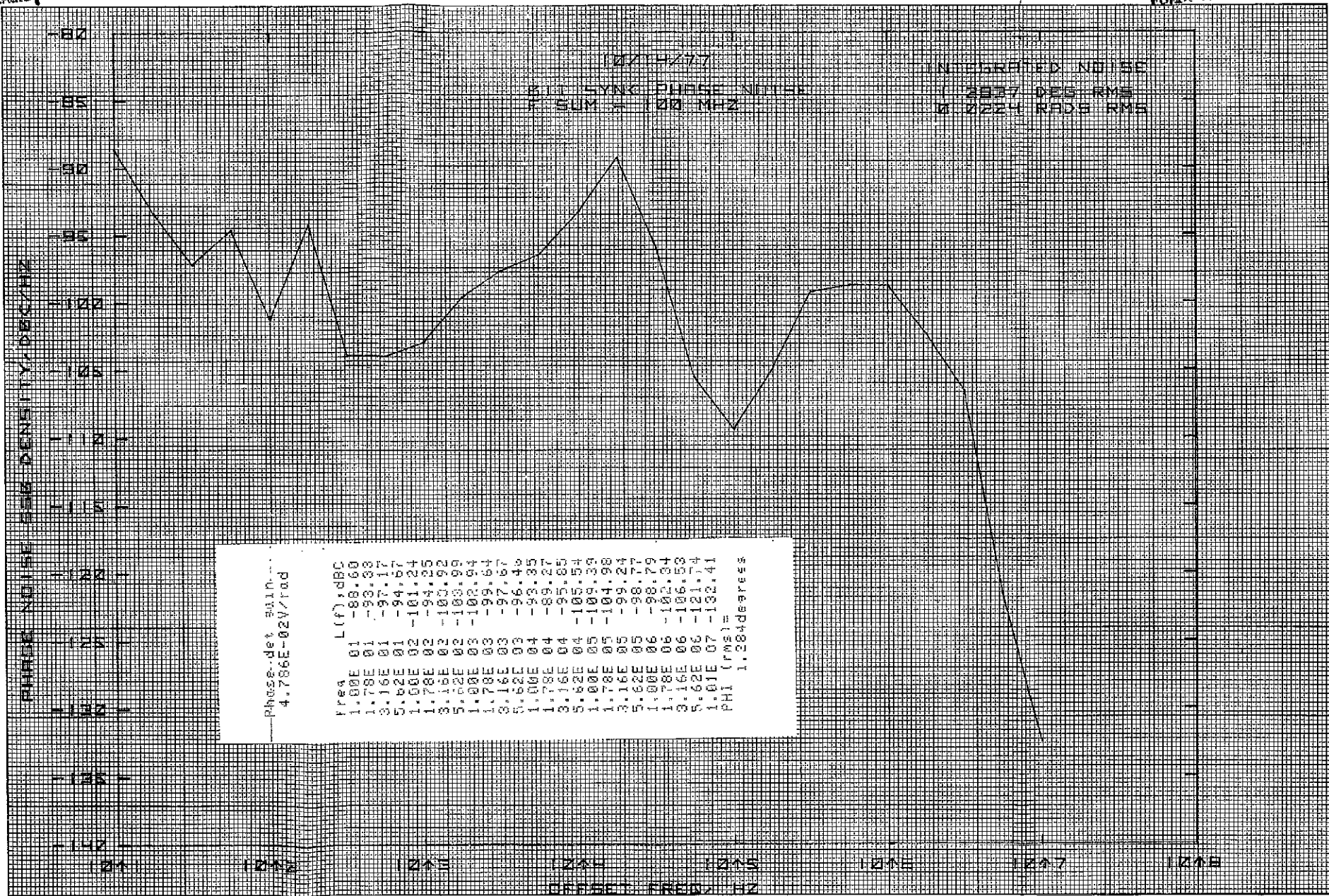
The bandwidth of the upper loop was measured using the test setup of Figure 3-22. A GR 1062 is phase modulated by an HP 3330 automatic synthesizer, and is used as the reference for the synthesizer. The output is then phase detected and the resulting modulation measured with the HP 3571A tracking analyzer (driven by the 3330B). The resulting phase modulation responses are shown in Figures 3-23, 3-24, and 3-25. The phase modulation bandwidth of the GR 1062 alone was measured using a similar setup, and is shown in Figure 3-26. The plots show a modulation bandwidth of about 300 kHz, with the exception of Figure 3-25, which has an added peak in the response at about 680 kHz. This is probably due to insufficient phase margin.





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Figure 3-20. Phase Noise Output at 150 MHz



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Figure 3-21. Phase Noise Output at 200 MHz

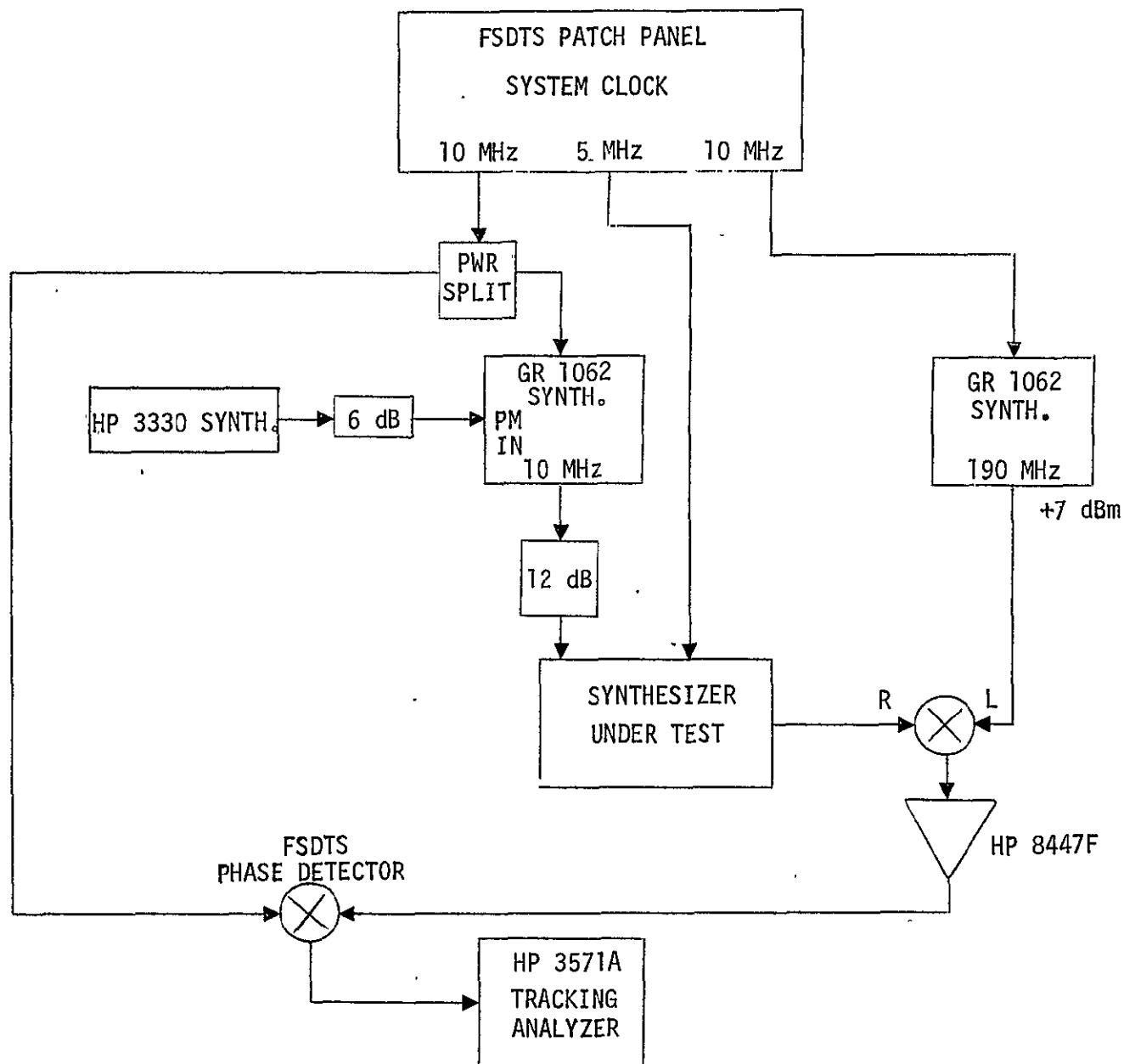


Figure 3-22. SETUP FOR MEASURING LOOP BANDWIDTH

10/13/77

PHASE MOD RESPONSE OF BIT SYNCH

SETUP #2

FSUM = 100 MHZ

0 DBM IN

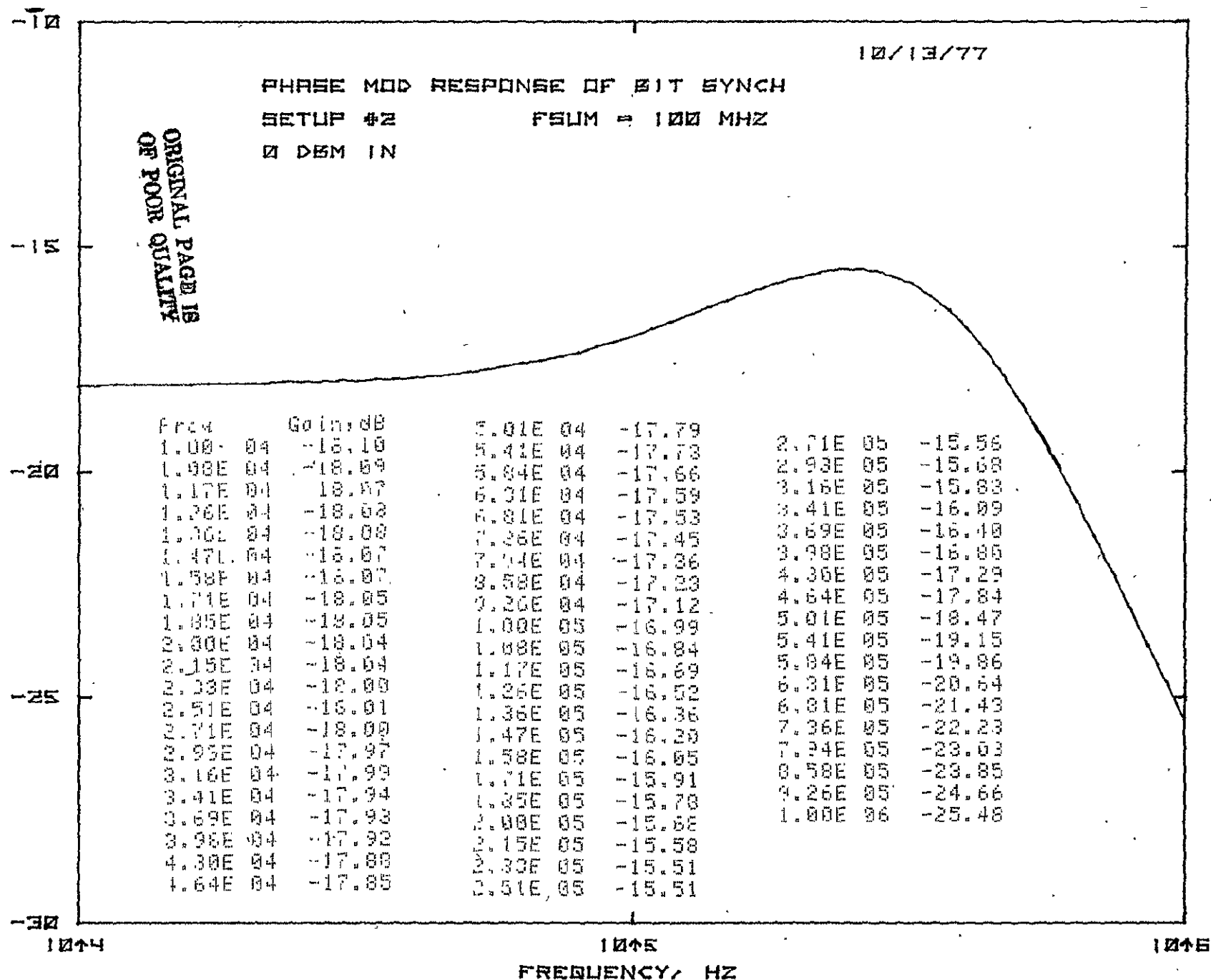
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Figure 3-23. Loop Bandwidth, Output at 100 MHz

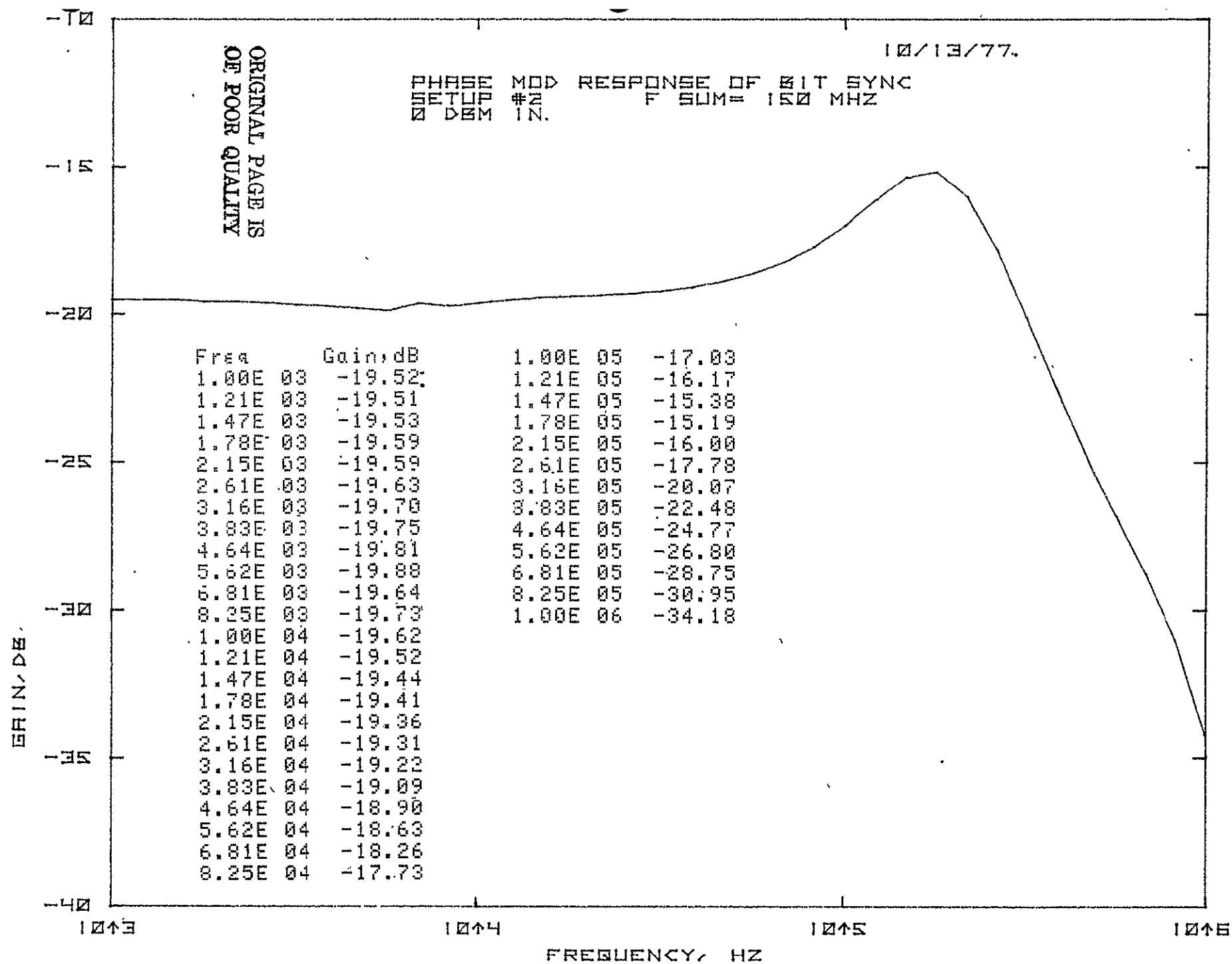


Figure 3-24. Loop Bandwidth, Output at 150 MHz

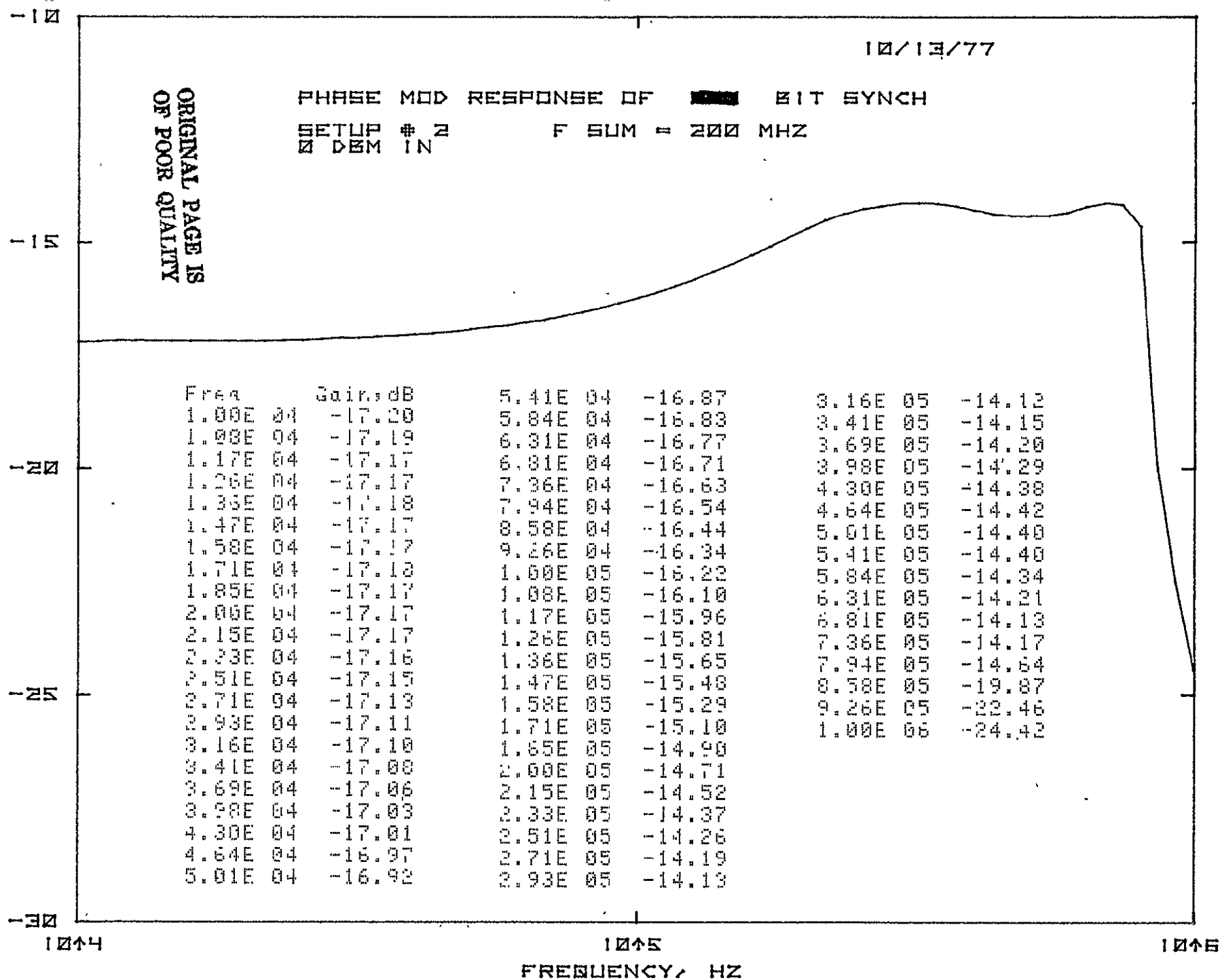


Figure 3-25. Loop Bandwidth, Output at 200 MHz

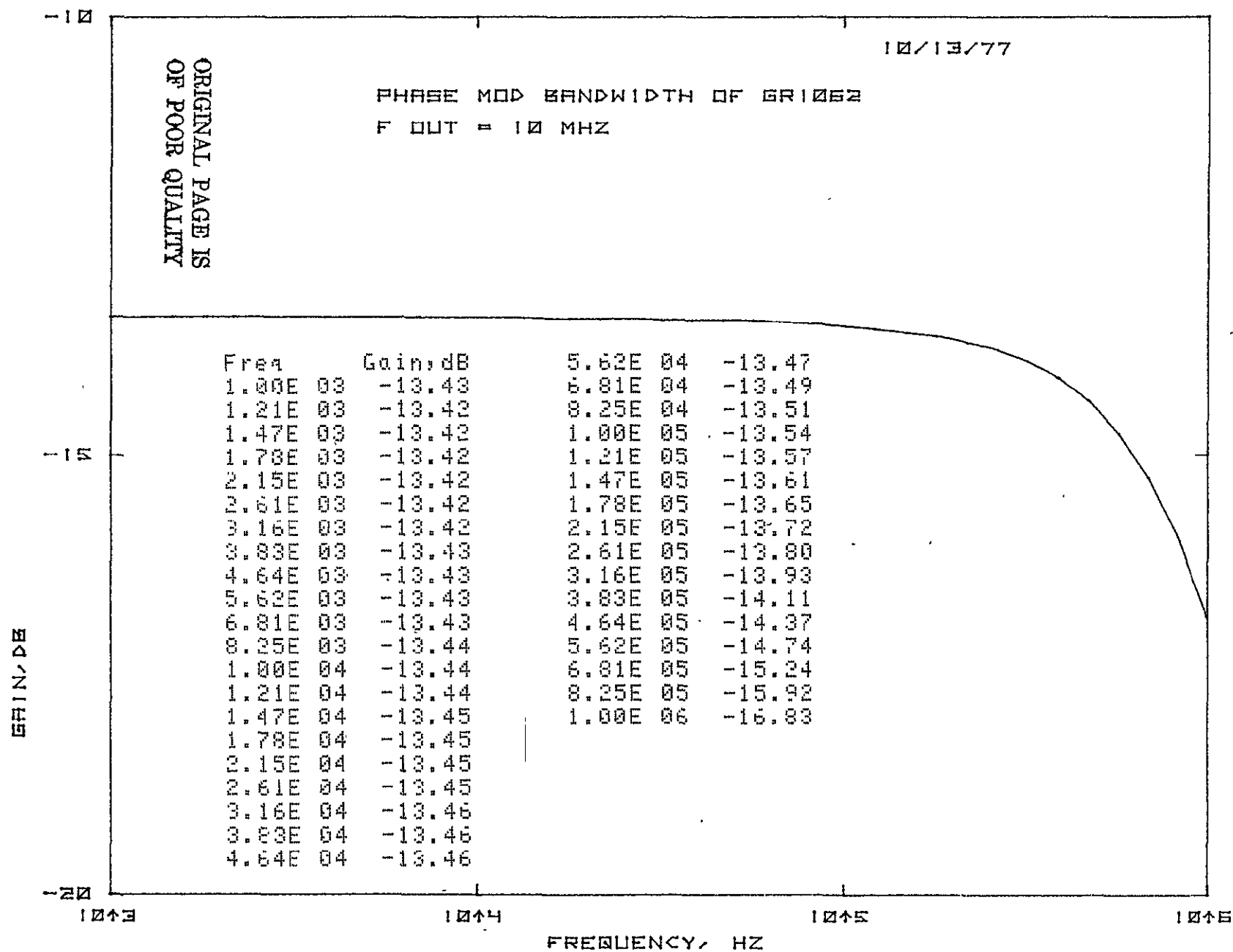


Figure 3-26. Test Setup Limitations

3.2 PERFORMANCE OF SYMBOL SYNCHRONIZER

The 100 MSPS Symbol synchronizer was tested according to the acceptance test procedure (IOC 7333.21-07). A discussion follows for two subjects of interest, i.e., Bit Error Rate degradation and acquisition time.

3.2.1 BER Degradation

The BER degradation data is plotted in Figure 3-27a and 3-27b for the 2 pairs of data rates 20, 30 MSPS and 60, 100 MSPS. Due to equipment limitations, phase jitter excitation was not provided. However a separate test, at 25°C was performed for various values of phase jitter at various frequencies. This data is shown in Figure 3-28.

The temperatures selected for the tests were 25°C and 40°C. It is expected that this temperature range is similar to that which the unit would experience when mounted in a blower equipped instrumentation rack and thus meets the intent of the specification. The unit was not tested at higher temperatures due to the self heating provided by the internal dc power supplies. In fact, the power supplies raise the internal temperature by as much as 30°C.

The BER performance is plotted in Figure 3-27A for the 20 and 30 MSPS case. Notice that at 25°C the performance is between 0.5 and 1 dB from the theoretical values. However at 40°C an additional degradation of approximately 0.2 dB is experienced at the low SNR's, but not as SNR approaches +7 dB. Figure 1B shows the same parameter (BER degradation) but at symbol rates of 60 and 100 MSPS. In these cases there is a degradation that increases with SNR and which, for the 100 MSPS case, leads to an out of spec condition for SNR's greater than +5 dB. At 40°C, this limit becomes +2 dB. This phenomena of increasing degradation with SNR is thought to be due to the frequency synthesizer based VCO function but the exact cause has not been isolated. However, the purpose of this symbol synchronizer is to acquire and maintain sync with low degradation at SNR's in the range of 0 dB where coded systems operate with significant coding gain. The contention is made that at SNR's greater than 2 to 5 dB, the error rate after decoding is so negligible that the additional degradation of between 0 and 0.5 (at SNR = 7 dB) will not be detrimental to the overall system.

A dominant source of BER degradation is that of predetection filtering. In particular, Figure 3-28 shows BER degradation vs transition density. As

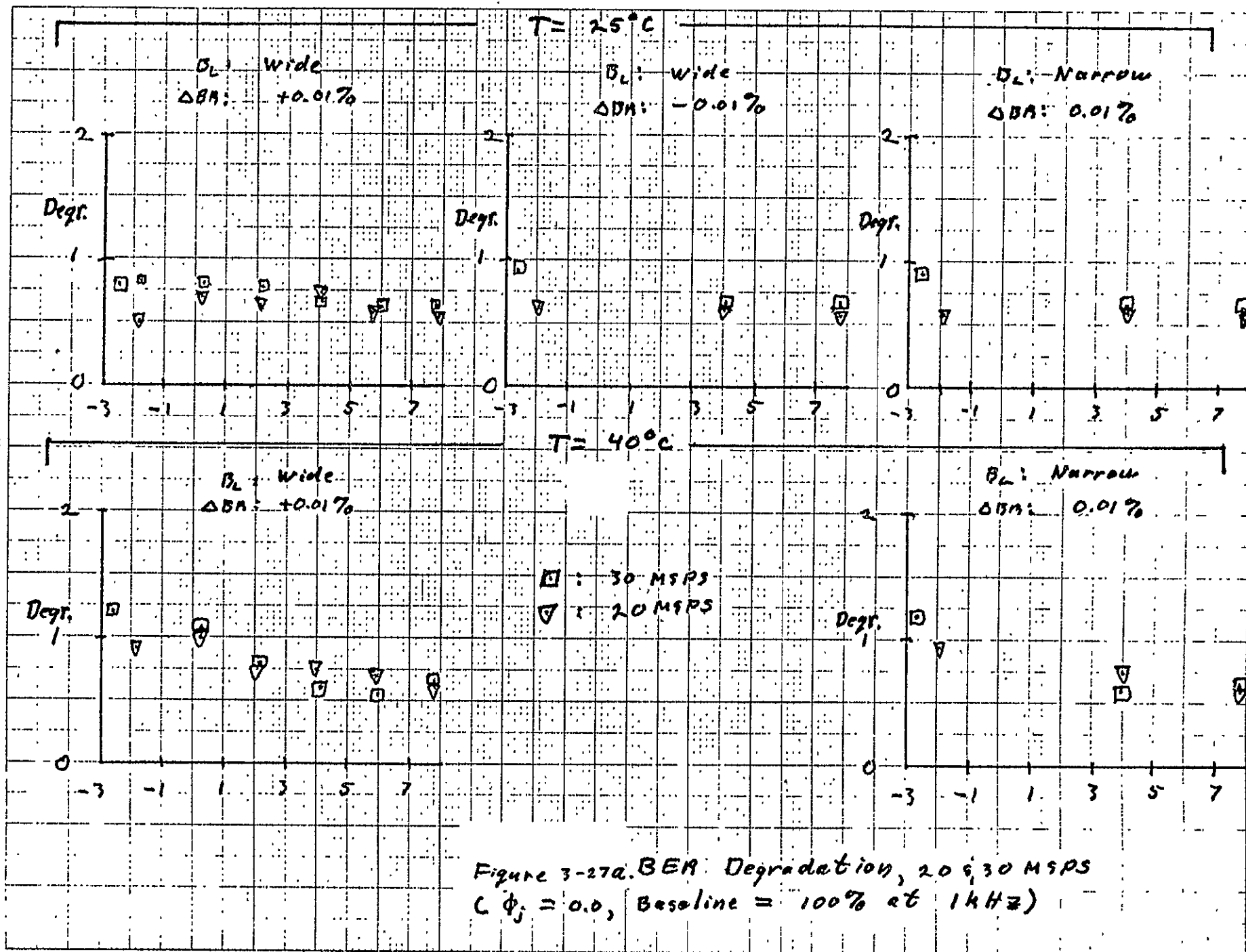
transition density increases, the frequency spectrum shifts such that more energy is in the higher frequencies and the effects of band limiting are more severe. A limiting case is that of 100% where the data pattern is "1010 ..." and the spectrum of the signal is that of a square wave at half of the bit rate. In this case, a 2.25 bit rate filter suppresses all but the first 2 harmonics yielding a 0.5 dB BER degradation. In addition intersymbol interference contributes an additional degradation of approximately 0.1 dB. For lower transition densities (20-50%) both of these factors decrease but phase jitter in the loop increases. This degradation increase has been experimentally observed to be 0.3 dB. Thus the claim that the unit as tested meets the specification of less than 1.5 dB degradation is justified on the basis that more than 0.3 dB would not be present if the signal were not so severely band-limited. This degradation can be reduced to a negligible amount if bandlimiting on the order of 4 to 6 times symbol rate is used instead of the factor 2.25.

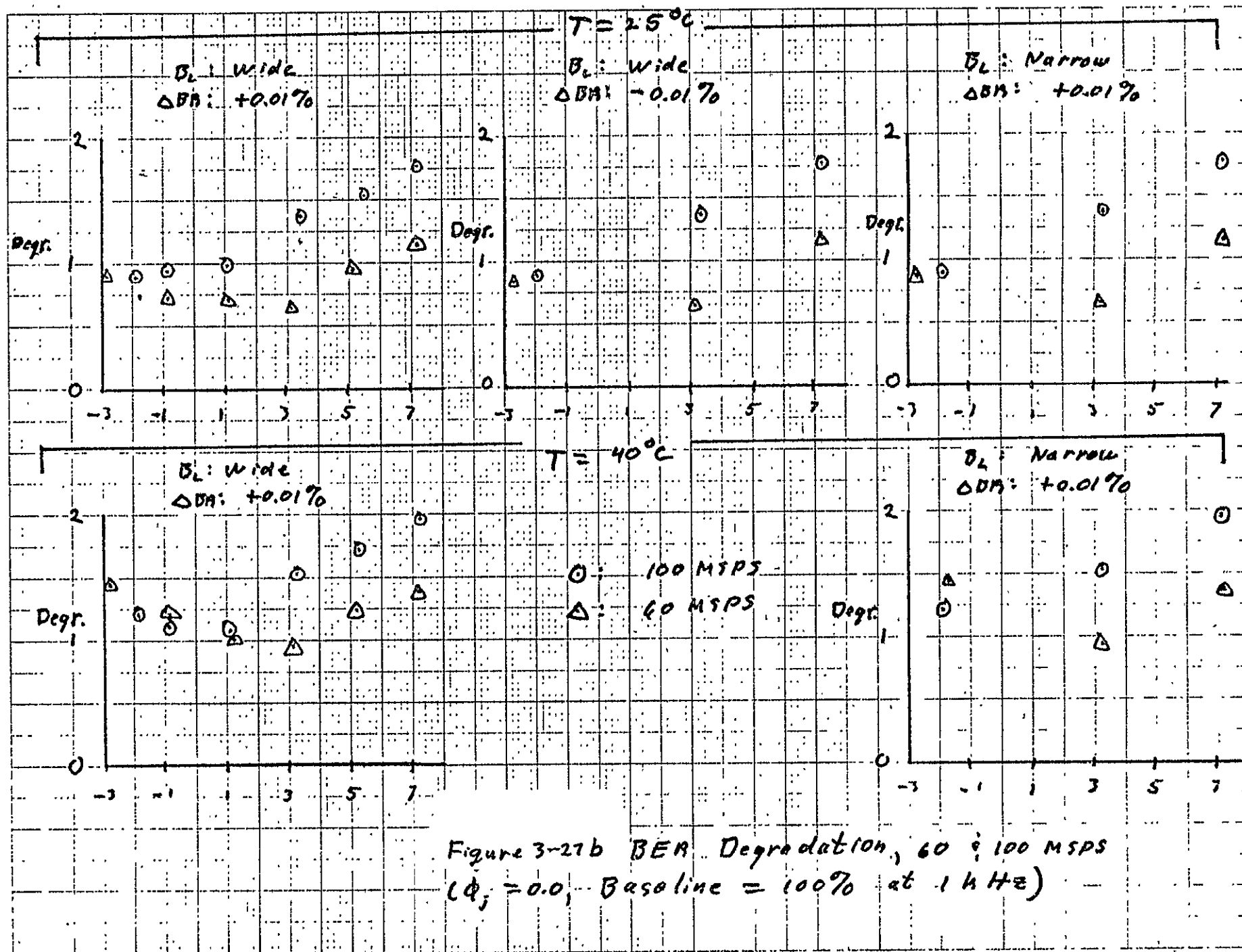
The effect of input phase jitter on BER degradation is shown in Figure 3-29. Notice that phase jitters at 1% of the Bit Rate in excess of 8° (peak) lead to little discernible BER degradation (0.08 dB for 8°). Also notice that there is negligible degradation for 1° jitter over the frequency range of 0.003% to 3% of the bit rate.

3.2.2 Acquisition Time

The acquisition specification of 0.1 second ($\text{SNR} > 7 \text{ dB}$) and 1.0 second ($\text{SNR} > -2 \text{ dB}$) are easily met by the symbol synchronizer by observation of its locking characteristics on the oscilloscope. Since there is no lock detector included in the unit, it is extremely difficult to measure the actual acquisition time. In as much as the acquisition time spec appears to be present only to guarantee lock, it appears to be unnecessary to calibrate the rather elaborate instrumentation that is required for acquisition time measurements.

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BER Degradation
vs
Transition Density

BR 20MHz

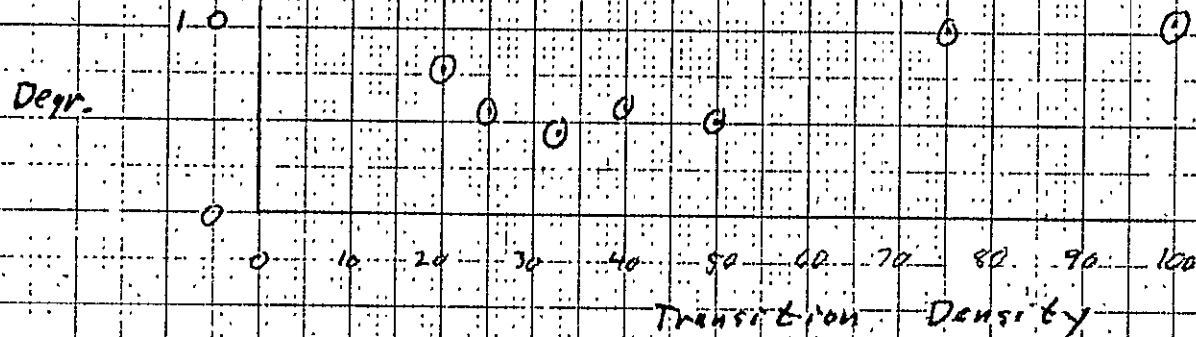


Figure 3-28 BER Degradation
vs
Transition Density

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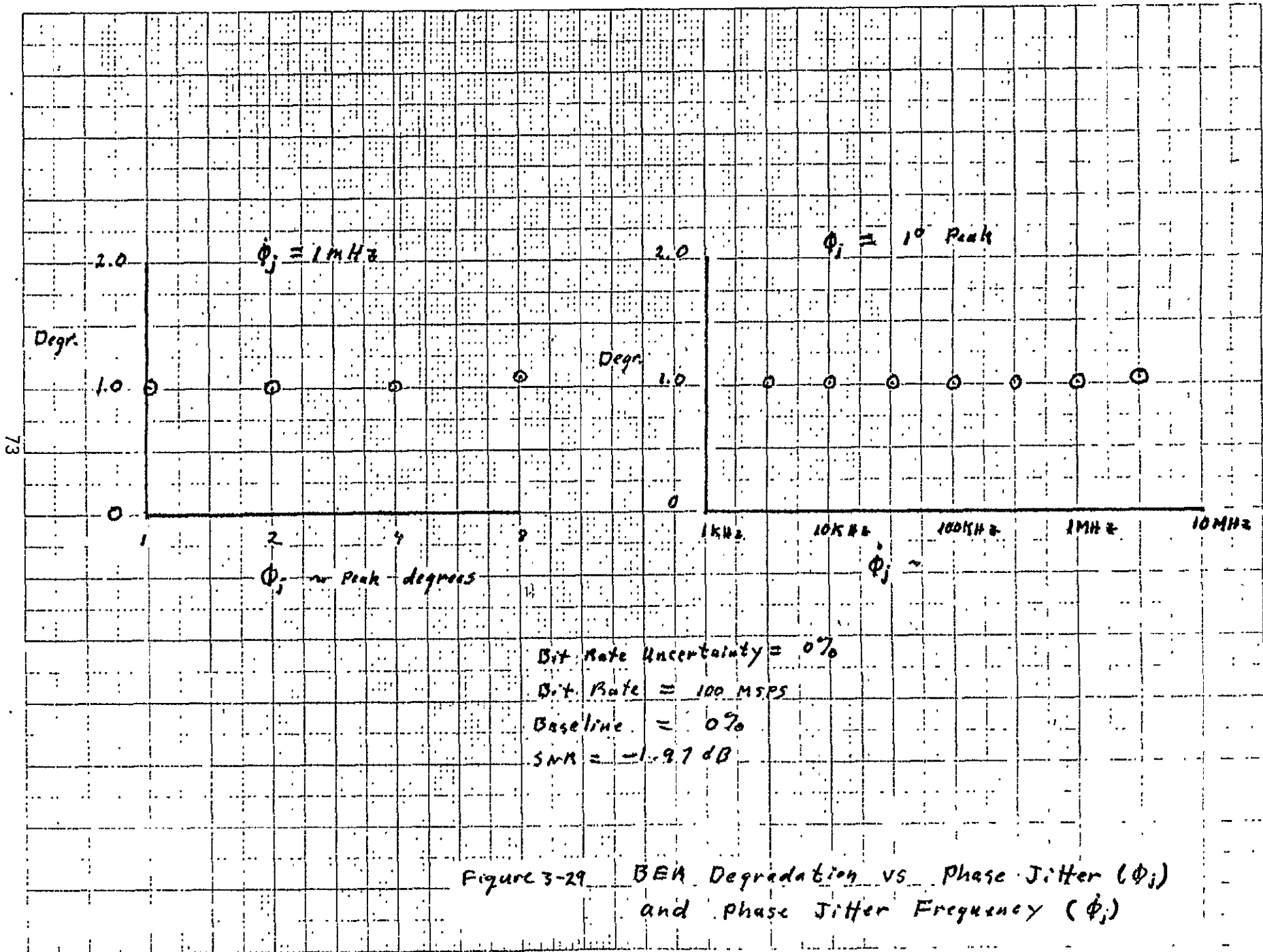


Figure 3-29 BEA Degradation vs. Phase Jitter (ϕ_j) and Phase Jitter Frequency (ϕ_j)