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Technical Report

DATA SYSTEMS ELEMENTS TECHNOLOGY ASSESSMENT AND SYSTEM SPECIFICATIONS (ISSUE NO. 1)

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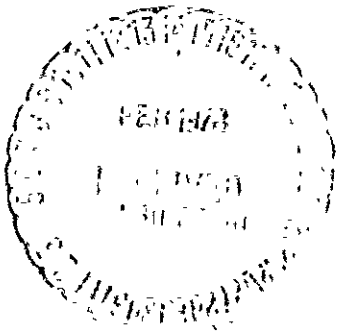

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TECHNICAL REPORT
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DATA SYSTEMS ELEMENTS TECHNOLOGY ASSESSMENT AND SYSTEM SPECIFICATIONS (ISSUE NO. 1)

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Prepared For

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ABSTRACT

The ability to satisfy the objectives of future NASA Office of Applications Programs is dependent on technology advances in a number of areas of data systems This report examines the technology of end-to-end data systems (space generator elements through ground processing, dissemination, and presentation) in terms of state of the art, trends, and projected developments in the 1980 to 1985 timeframe. Capability is considered in terms of elements that are either commercially available or that can be implemented from commercially available components with minimal development.

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ACKNOWLEDGEMENT

Many authorities in the field of data systems responded to requests for information in support of this report via the mails, telecom, and visits. Significant parts of the forecasts are the result of their contributions. Many of the respondents generously gave permission to use their names as sources of the information provided. However, the sponsoring agency (NASA) requested that specific references be made only to published literature to eliminate the possibility of embarassment to either individuals or organizations. Individuals and organizations that contributed are listed alphabetically at the end of the report Their contributions are gratefully acknowledged.

EXECUTIVE SUMMARY

INTRODUCTION

The ability to satisfy the objectives of future NASA Office of Applications (OA) programs depends on technology advances in all areas of data systems. This report examines the technology of end-to-end data systems (space generator elements through ground processing, dissemination, and presentation) in terms of state of the art, trends, and projected developments in the 1980 to 1985 timeframe. Subsequent efforts will use this initial effort as a basis for extending the projections to 1990. Capability is considered in terms of elements that are either commercially available or can be implemented from commercially available components with minimal development. The following paragraphs of this Executive Summary highlight the trends and projected developments in some of the more important areas of data systems as far as NASA's future programs are concerned. The summary and report itself begin with space data storage elements. Space data generator elements and space data processing elements were not covered in this first phase of the study. Coverage will be provided in subsequent editions of the report.

Data systems technology is advancing at an unprecedented rate. Announcements of new products that outperform existing systems are made daily. The majority of advances are primarily the result of improvements in integrated circuit technology. Products are becoming faster, smaller, less expensive, more efficient, more flexible, and more reliable, to name a few areas of improvement. Although the major advances are occurring at the chip level, these advances are being implemented at the system level almost as rapidly as they occur. This report presents the technology status at both the chip level and the system level, with emphasis on the latter area since this is where the effects of NASA's programs will be most heavily felt

The major emphasis throughout the report is on hardware technology. Software for data base management is addressed in Section 8. Subsequent reports should assess software technology in greater detail since this

area is expected to represent an increasingly larger percentage of the NASA budget for data systems. Of course this is the case only because of the significant advances that are occurring in hardware technology

The Executive Summary is presented in the same sequence as the report. The emphasis throughout this summary is on trends and projected development in lieu of the state of the art.

SPACE DATA STORAGE ELEMENTS

Space data storage has typically been performed with magnetic tape recorders that are limited in capacity, reliability, and lifetime. Although magnetic tape recorders will still be used extensively in space into the mid 1980's and possibly beyond, new technologies that are potentially more reliable are beginning to emerge. The most promising technology for replacing tape recorders across a broad front in space is magnetic bubbles.

NASA is currently developing a prototype 10^8-bit bubble memory system that will be ready for flight by 1978. Although this system will not be competitive with existing magnetic tape recorders in terms of volume, weight, power, and storage capacity, it will provide for an early flight demonstration of a bubble memory recorder. Additionally, it will provide a mechanism for demonstrating the alleged higher reliability of bubble memory storage systems.

The potential for bubble memory spaceborne data recorders lies in the expected chip storage capacity increase from the currently available 10^5-bit chips to 10^8-bit chips by 1985. The larger-capacity bubble chips will make the performance of bubble memory systems competitive with tape data recorders for storage capacities of up to 10^{10} bits by 1985.

High-density airborne digital tape recorders can be generally classified as rotary-head recorders and fixed-head recorders. The fixed-head recorders currently offer the highest data transfer rates. RCA is developing a 240-Mbps fixed-head data recorder for GSFC that records 120 active data channels on a 2-in.-wide tape

Authorities are predicting that the rotary-head tape recorders will be used extensively in future data systems that either require very high storage capacities or must interface with onboard digital computers that store and access data in blocks, rather than continuously as is currently done in most aerospace recorder systems.

Technology projections for 1985 are for aerospace data recorders with storage densities of up to 10^7 bits/in^2 and data transfer rates of up to 10^9 bps.

SPACE DATA HANDLING ELEMENTS

Future general-purpose data systems will provide increased flexibility, reliability, and data throughput capacity. Microcomputers will be incorporated into future remote terminal unit designs to provide remote programming and processing capabilities that will significantly increase the overall data system throughput capacity by eliminating much of the nonessential data bus traffic and reducing the central computer processing load. Space-qualified 64-kbit RAM chips and 1-Mbit bubble memory chips should be available by 1980. These devices will make it feasible to package microcomputers with upwards of 10^6 bytes of memory by 1980 without increasing the current size of the remote unit. Improvements in analog and digital circuit integration levels will more than offset the additional size and power required for the remote unit processor and memory functions.

By 1980, low-cost, low-power, monolithic analog-to-digital converters and digital-to-analog converters should be available from a number of different sources.

Technology projections for 1985 that will impact the ultra-high data rate and high-speed digital data handling systems of the future include the following

- Space-qualified GaAs MESFET logic with propagation delays of less than 100 psec and clock rates in excess of 5 GHz will be available.
- All monolithic analog-to-digital series-parallel converters will be available with a conversion speed of 10 nsec for 8 bits.

- Hybrid analog-to-digital parallel converters will be available with a conversion speed of 2 nsec for 8 bits.
- Short-channel MOS analog switches will be available with switching speeds less than 500 psec.

These developments will provide the technology necessary to build data systems having analog sample rates of up to 400 MHz for 8-bit resolution and output PCM data rates of up to 5 GHz for a single output serial data stream. This technology will support the development of real-time imaging systems similar to the Thematic Mapper with resolutions of less than 5 m.

Projected power consumption per gate for the high-power 5-GHz GaAs MESFET logic is 10 mW per gate. At this power level, only medium-scale integration can be used. For applications that require logic speeds less than 1 GHz, low-power GaAs MESFET logic with power dissipations of only 0.3 mW per gate can be used to provide highly reliable LSI designs with integration levels in excess of 1,000 gates per chip.

These developments in high-speed, relatively low-power logic, coupled with the developments in bubble memories discussed in Section 3 2 and semiconductor memories discussed in Section 7.2.1, will make high-rate data handling much easier by 1985.

Another development that is likely to have a significant impact on data handling system designs by 1980 is the optical data bus. Both the Air Force and the Navy are actively pursuing the development of optical transmission lines in an operational airborne environment. Advantages claimed include transmitting higher serial data rates (up to 100 Mbps), reduced weight, and less susceptibility to RFI/EMI/EMP.

SPACE TO GROUND COMMUNICATION

Both solid-state and tube-type power sources for space-to-ground communication systems are currently experiencing improvements in power output, efficiency, and size over a wide range of frequency bands, and the current trends are expected to continue through the 1980 to 1985 time

period. Transmitters will be using a variety of devices for different frequency bands between now and 1985. Below 6 GHz, bipolar devices will be competing with TWTs for size, power, and efficiency. FETs should be equivalent to the IMPATTs of today in the 6- to 50-GHz band by the mid-1980's, whereas IMPATTs should improve in power and efficiency to provide approximately 1 to 2 W at 100 GHz Efficiency in FETs should increase significantly by 1985, approaching 80% of the theoretical maximum. In spite of these advances, TWTs will continue to either equal or outperform solid-state devices in terms of efficiency, gain, and power output in most frequency bands.

The major areas of research in communications are going on at frequencies above 30 GHz, including the optical band Improvements in these frequency bands are likely to be reflected in the lower frequency bands also.

Reflector-type antennas will be prevalent in all bands through 1985 These will be folding types below 10 GHz, and will be deployable at all frequencies. Prime focus and offset reflectors with cluster array feeds will be common. Phased-array antenna systems will be capable of competing with reflector types in performance, weight, and volume. However, they will be more expensive by a factor of 1.5 to 2. Phased arrays will handle much higher power without experiencing multipactor Array feeds of low-loss air-stripline or microstrip networks using high-permittivity substrates will allow designs with sidelobes that are down more than 30 dB.

Relay satellites employing laser technology are likely to be feasible by 1985. Whether such a system will be implemented is unknown. Such systems will be capable of data rates in excess of 1 Gbps.

As a result of developments in super components, receiver size in all frequency bands will decrease to somewhere in the range of 25 to 50% of their present size by 1985, while performance will improve. Power consumption will continue to decrease to approximately 50% of the present consumption by 1985, especially for the higher-frequency receivers.

Solid-state devices will be capable of operating at higher frequencies with sufficiently low noise figures and high enough gains to replace TWTs in most systems.

The analog portion of the receiver of the future will shrink as more and more digital circuitry is used. The trend is to have digital circuitry from the conversion to baseband to the output of the receiver. When short (<512-bit) PN Codes are used, it is likely that CCD transversal filters will be employed.

PREPROCESSING ELEMENTS

Preprocessing elements include those hardware and software elements that take the outputs from the ground communications system (ground station receivers) and perform the functions necessary to input the data into the ground processing system. Functions performed by the preprocessing elements include data detection and synchronization, demultiplexing, reformatting, data buffering, decoding, error correction, and calibration.

The TDRSS ground station, currently under development, represents the state of the art in operational ground stations. When operational in 1980, the TDRSS ground station will handle data rates to 300 Mbps and will employ Viterbi decoders that are capable of data rates to 20 Mbps. Development hardware for future system applications is currently being tested in the laboratory with bit synchronizers that operate at 500 Mbps and demultiplexers capable of handling rates to 1 Gbps.

In general, the trends in preprocessing elements are toward higher data rates and more real-time processing and data handling, including real-time data reformatting, retransmission, and distribution.

Tape recorders currently used for ground data storage are mostly the fixed-head, high-density digital instrumentation type. Trends in high-density digital instrumentation recorders are toward wider tapes, more heads per inch of tape, and higher data rates. Several companies are currently developing fixed-head instrumentation recorders with data recording rates in excess of 200 Mbps.

Some authorities predict the increased use of rotary-head type data recorders because of the higher data packing densities and faster start-stop times that can be achieved with the rotary-head systems.

Flexible high-rate instrumentation recorders should be available by 1985 that record and play back at data rates up to 1 Gbps with data storage densities of 10^7 bits/in^2.

DATA PROCESSING ELEMENTS

Data processing elements covered in this report include minicomputers, large-scale computers, super-scale computers, bipolar memory systems, MOS memory systems, electron-beam memory systems, and disks. Subsequent reports will cover additional areas of hardware and software.

The rapid growth in the capabilities of minicomputers experienced during the past decade will continue during the 1980 to 1985 timeframe. By taking advantage of the predicted improvements in LSI logic circuits and semiconductor memories, the most powerful minicomputers of 1980 and 1985 should be capable of achieving instruction rates of 2 million and 5 million instructions per second (MIPS), respectively, at costs in the vicinity of $50,000. Mean time between failure for these systems is expected to approach 10,000 hr, and software offered with the machines is going to become much more sophisticated, rivaling that of medium-scale computers of today.

The historic 12 to 15% annual price/performance improvement in large-scale computers will continue during the 1980 to 1985 timeframe as a result of achievements in logic circuits, main memories, and mass storage. The desire for ever greater speed will force the continued growth of multilevel hierarchical storage systems. In particular, the use of buffer memories will expand. More emphasis will be placed on system reliability, with improvements achieved through the use of error-correcting codes in memory systems, fault-tolerant design, and hardware redundancy. The most powerful large-scale computers of 1980 will be

capable of 45 MIPS, with increases to 100 MIPS by 1985. Expanded use of distributed data processing systems will occur in conjunction with, rather than instead of, the growth of large-scale computers. Many of the large-scale computers of the next decade will be geared to large data base management operations.

Super-scale computers of the next decade will continue to have a very limited market, addressing problems that throughput large amounts of data and in which computations are highly parallel in nature. Their characteristics will continue to improve, with emphasis placed on larger memories and faster execution times since the quality of the solution to the problems addressed depends on the number of data points considered and on the number of computations performed. Both vector and parallel designs will be used to build systems

Vector super-scale computers are expected to achieve 100 to 150 MIPS by the early 1980's, with increases to 200 to 300 MIPS by the mid-1980's. Parallel super-scale computers will be capable of achieving instruction rates as high as 1,000 MIPS by 1985. One limiting factor in achieving these rates is the extent to which the parallel or vector capabilities are utilized, which depends primarily on software advances. Since software development is slower than hardware development, it will be the limiting factor, preventing the more optimistic projections made by some experts from being achieved. Only very limited software support is available on most state-of-the-art super-scale computers. Major advances in software support are needed so that systems can be more fully utilized. For this reason, emphasis will be placed on software development during the next decade.

Bipolar memory systems, which are built using TTL, ECL, or I^2L technology, will experience major improvements in all performance categories during the 1980 to 1985 timeframe. By 1980, chip densities will double, access and cycle times will improve by 20%, and power consumption and cost per bit will improve by 50% over current values. By 1985, chip densities will quadruple, access and cycle times will improve by 40%,

and power consumption and cost per bit will improve by 75% over current values. By 1985, cycle times of 20 to 40 nsec should be common for ECL memory systems with costs on the order of 0.45 to 0.2 ¢/bit. Costs for I^2L memory will be on the order of 0.2 to 0.06 ¢/bit, but cycle times will run between 80 and 140 nsec.

MOS technology, particularly NMOS, will continue to be the dominant processor memory technology during the 1980 to 1985 timeframe. Major improvements will occur in all performance categories of NMOS and CMOS memory systems during this time period. By 1980, chip densities will quadruple, access and cycle times will improve by 40%, and power consumption and cost per bit will improve by 75% over current values. By 1985, chip densities will increase by a factor of 16, access and cycle times will improve by 60%, and power consumption and cost per bit will improve by 90% over current values.

Electron beam memories offer great potential in terms of performance, cost per bit, and total system capacity. However, for major advances to occur, the following three problems areas must be overcome:

- MOS target life must be improved.
- Electron optics must be upgraded to accomplish submicron beam diameters in production.
- Cathode development must occur to accomplish increased beam brightness with decreased beam size.

If sufficient progress is made in these areas, electron beam memories should be commercially available in 1980 with capacities to 2×10^9 bits for two-stage deflection units with access times of 3.3 nsec (no operation changes involved) and costs on the order of 0 01 to 0.02 ¢/bit. By 1985, similar units should have capacities to 8×10^9 bits, with access times of 2.5 nsec and costs of 0.001 to 0.005 ¢/bit.

The initial use of electron beam memories will be as a replacement for the fast-access auxiliary storage devices. Eventually these systems will be cost-competitive with all on-line random access peripheral

memories. They have the potential not only of bridging the memory access gap but also of eliminating it and thus allowing a dramatic reduction in operating system software complexity and cost. In addition, these systems are dark-horse candidates for onboard data storage if the lifetime characteristics of the target can be improved.

Moving-head disk storage technology is still evolving and viable. By 1980, spindle capacities, maximum system capacities, and cost per bit will improve by 50%, and transfer rates will improve by 25% over current values. By 1985, spindle capacities and maximum system capacities will improve by 150%, cost per bit will improve by 80%, and transfer rates will improve by 275% over current values. However, access time will not experience major advances.

Fixed-disk packs will become common once again to achieve the tighter mechanical tolerances needed to accomplish higher densities at the least cost

DATA BASE SYSTEMS ELEMENTS

Data Base Management System (DBMS) software and/or techniques are receiving wide attention for managing the large data bases of the future. Some of the key issues associated with DBMSs are data independence (loosely defined as the immunity of applications programs to the data base structure), data base security, data models, and data base machines.

Data independence is gradually becoming a reality with certain limitations. It is expected that existing applications programs will essentially be immune to data item changes, as well as to changes that add a relationship, by no later than 1982. At the same time, changing relationships will still be a problem under many circumstances for the foreseeable future.

Present DBMSs provide security at the data base and file level. Projections call for security at the record level to be widely available

by 1980, security at the data aggregate level to be standard by 1983, and the individual data item to be protected by 1984. These features will be implemented primarily in software prior to the mid-1980's, when such features will be available in hardware, probably as an option.

Data models are receiving the attention of a number of software and hardware vendors. Current DBMS software is primarily oriented toward hierarchical models. The current trend is away from hierarchical data models toward relational and network models. Although there is very high interest in relational models, the network model is expected to be the primary data model available and in use through 1985. In this respect, a high-level language capable of translating a data base from a hierarchical model to a network model is expected to be available by 1983.

Many authorities are of the opinion that the major mainframe manufacturers will orient their next generation of computers toward data base management, and thus create the so-called data base machine. Such a machine will exhibit a hierarchical memory structure, sophisticated data clustering capabilities, and a full complement of subsidiary DMBS processors capable of performing functions such as searching, sorting, security checking, etc. Projections are that a machine with capabilities such as these is expected to be available by 1982.

INFORMATION DISTRIBUTION ELEMENTS

Terrestrial networks will continue to provide the dominant method of interconnection for data communications in the early to mid-1980's, although long-haul links will tend to use more and more satellite channels. The average user, however, will interface to the satellite via a telephone line in lieu of having a satellite terminal. At the same time, the use of small satellite terminals, particularly for reception of wideband data, will grow at a rapid rate.

Terrestrial networks will still be predominantly analog, and thus require modems, into the mid-1980's, with a continued strong trend toward an all-digital network. By 1985, the major long-haul networks will probably be digital, with a continued dominance of analog circuits to subscribers. Optical fibers will be used extensively in future networks.

Data rates over voice-grade lines are expected to increase to 9,600 bps on multi-point lines, including switched voice-grade lines, and to approach 14 to 15 kbps on point-to-point lines The improvements will be primarily the result of improvements in software techniques and modem hardware. However, the use of digital links between switches will also play an important role in increasing the data rates.

Packet switched networks will continue to increase and will play a major role in computer communications of the future. Small satellite terminals will see increased use (particularly receiving terminals) and will likely prove to be feasible for distribution of wideband NASA data that require fast turnaround.

INFORMATION PRESENTATION ELEMENTS

Information presentation elements include both the dynamic or real-time systems (terminals, graphic display systems, and image presentation systems) and hardcopy systems (COM, printer/plotters, etc.) for presenting data in a viewable form. Advances in capability in all areas of information presentation will result from research in the specific technology areas as well as research in related areas of data processing and memory systems.

The capability, flexibility, and throughput of all types of information presentation systems will increase as the individual devices become more intelligent and thus more independent of the host processor. Flexibility of both dynamic and hardcopy systems will increase as a result of internal processing and memory capacity. In general, prices are likely either to remain constant or to increase as a result of the added capability.

The cathode ray tube (CRT) will remain the dominant display medium for most applications where size is not a limiting factor. (The size of CRTs is not expected to exceed 25 in.). Plasma panels will be feasible and will replace CRTs for selected applications, but their impact is not

expected to be major since they will not be cost competitive with the CRT. Thin-film transistor panels, possibly in conjunction with electroluminescent powder technology, are likely to see limited use.

In the hardcopy area, there will be continued improvement in the area of COM technology, primarily as a result of the use of front-end processors.

CONCLUDING REMARKS

In summary, all areas of data systems technology are advancing at unprecedented rates. Although technology is advancing rapidly and there is a high probability of satisfying NASA's future requirements, technological capability does not imply availability, and developments at the system level may be required in a number of areas. In view of this, a continuing assessment of technology at the component and the system level is required to establish where such developments are needed and how to best accomplish the desired result.

INTRODUCTION

OVERVIEW

Future NASA Office of Applications (OA) programs require the collection and subsequent dissemination of unprecedented volumes of data on a timely basis over widespread geographic areas. Users of the data range from large Government departments (Interior, Agriculture, etc.) to the individual (college professor, researcher, etc.) with a common limitation: budget.

The OA foresaw the technical, logistical, and integration problems associated with such a complex undertaking and implemented the Data Management Program to review and input to those functions that affect NASA's participation in the objectives, including requirements, capabilities, integration, and budget assessment. This report covers one aspect of the capabilities function: i.e., technology assessment. Also, because technology assessment covers cost as well as performance, inputs to budget will result.

The scope of a technology assessment for end-to-end data systems is so massive that it was impossible to provide the breadth and depth of coverage that is desirable within a limited resources program. Selected areas of technology that were considered as critical to NASA's future programs have been given the broadest and most in-depth coverage. Subsequent work will increase both the breadth and the depth of coverage in all areas, including software.

Technology assessment as defined herein is directed toward establishing the state of the art, trends, and future capabilities (1980-1985, with eventual extrapolation to 1990) for end-to-end data systems Data systems elements making up end-to-end data systems were defined by the NASA Data Systems Laboratory and are as follows.

- Data Generation - Sensing of physical parameters that characterize the phenomena to be investigated and translation of these parameters into electrical signals acceptable to a data system.

- Data Processing (Space) - Processing of data, usually but not exclusively in the digital mode, to change them to a form more acceptable for data transmission, storage, or use on board

- Data Storage (Space) - Storage of data for delayed transmission, for delayed processing, display, or other use onboard; or for physical return of the storage media

- Data Handling (Space) - The acquisition and/or distribution of data for data processing, display, storage, or other use onboard. The combining of data streams from several sources or the modification of single data streams to a format suitable for storage and/or transmission

- Communication (Space to Ground) - All functional elements necessary to transfer data to or from a spacecraft to the ground. Includes the functions performed by modulator, transmitter, airborne antennas, relay systems, ground antennas, receivers, and demodulators

- Preprocessing Elements (Ground) - The data processing elements (hardware and software) that take either predetection or postdetection data and detect (as necessary), demultiplex, and reformat the data into a parallel, digital format with calibration

- Processing Elements (Ground) - The hardware and software components that take parallel formatted digital data (either raw or semiprocessed) and produce end products suitable for either further processing, display, or storage within a data base

- Data Base System Elements (Ground) - The hardware and software components that enable the creation of an integrated data base from logical files and the subsequent retrieval of information from the data base using either specified keys and/or relationships

- Information Distribution Elements (Ground) - The manual and electronic means (hardware, software, and protocol) for requesting and distributing processed and preprocessed data in response to a user request

- Information Presentation Elements (Ground) - The hardware and software elements necessary to provide hardcopy and dynamic visual presentations of image, alphanumeric, and graphic data.

In the following sections, current and future data systems technologies are discussed within the context of the above definitions. The report is organized into the 10 sections that are consistent with the above data systems elements, and the elements are discussed in terms of the subelements or levels that make up the parent element For example, data processing elements comprise hardware (processors, data storage, etc), software (operating systems, compilers, assemblers, etc), and firmware (memory and microcode). The subelements are then discussed in terms of state of the art (performance capabilities of typically top-of-the-line or high-performance devices), trends (uses, effects on cost and performance, historical extrapolations, etc.), and projected developments (forecasted capabilities for some future time period -- 1980 to 1985 for this report).

PURPOSE AND USE OF REPORT

The report is intended as the beginning of a data bank that can be used by designers, analysts, and planners of NASA data systems. When completed, the data bank will project the technological potential for the key characteristics of the individual data systems and components that make up the 10 data systems elements defined in the preceding paragraph. Future reports will update the tabular and graphical presentations of the key characteristics for the individual data systems components provided herein. The technological capabilities will be maintained current in terms of state of the art, projected technology in 1980, projected technology in 1985, and eventually the projected technology for 1990 In addition, trends in the basic technology area will be provided and updated to establish a basis for the projections and to enable the designers to assess particular aspects of the technology that may not be immediately obvious from the projected specifications.

Use of the report and the data bank may be accomplished by reference to an index. (The report index serves that purpose herein A separate,

more detailed cross reference index will be provided with the data bank). An individual data component or subcomponent will frequently have application in several data systems element areas. For example, semiconductor memories could conceivably be used in any of the 10 data systems areas. To minimize repetition of data within the report, discussions relating to a specific data system element or component are presented within the parent element section where its application is expected to most heavily affect NASA data systems. In the above example of semiconductor memories, the subject is covered under Data Processing Systems Elements (Section 7) and is referenced in other sections where applicable.

Finally, an important consideration concerning the technology forecasts is that a forecast does not necessarily imply availability Further, a list of specifications does not imply that all specifications within a given list will be feasible within the same system. For example, speed and power consumption are usually opposing considerations (i.e., as the propagation delay within a circuit decreases, the power increases) and the specification for low power consumption per bit may not correspond to the best projections for access and cycle times. To clarify limiting factors such as these, verbal discussions that attempt to identify pertinent considerations are presented within the report. Thus the user must interpret data herein within the intended context for it to be meaningful.

APPROACH

The approach to developing the assessment was based on a combination of analysis of literature in the different technology areas and a sampling of opinions of experts and authorities currently working the areas

Many authorities in the data systems field responded to requests for information via the mail, telecons, and visits, and significant parts of the forecasts are the result of their contributions. Many of the respondents generously gave permission to use their names as the source of the information. However, the sponsoring agency (NASA) requested that specific references be made only to published literature to eliminate the possibility of embarrassment to either the individual or the organization Individuals

and organizations that contributed are listed alphabetically at the end of the report. Many of these individuals are outstanding in their fields Their contributions are gratefully acknowledged.

As with literature, the responses of individuals regarding future capabilities varied rather widely. These responses had to be weighted based on some criteria. Frequently, the criteria used were in favor of the majority of responses. Another criterion was the availability of prototype hardware that appears to have potential as production equipment in the timeframe of interest. Finally, the past experience of the individual within a given area was weighted heavily. For example, if an individual or his organization has been dominant in a given field for a reasonable length of time, then the opinions of that individual were rated heavily

SPECIAL CONSIDERATIONS

A number of traps exist in any report of this type, even when reporting state of the art One of the first traps is to distinguish in the literature and in replies to questions between what is feasible on a production basis versus what is available on a custom-design (higher-cost) basis. Beyond this, one must distinguish between what is available on a custom-design basis and what is available only in the laboratory, and finally, for space applications, there must be a distinction between what is available for terrestrial applications versus space applications. The literature is usually vague on these distinctions.

Another very important consideration is that just because technology will support a capability, this does not mean that the capability will be available. The availability in many instances is a function of market demand or emphasis in the area of concern. Microprocessors, semiconductor memories, and other integrated circuit devices, for example, provide the capability for building tremendous flexibilities into data system elements, but the capability does not imply availability Similarly, various elements of data systems comprise several underlying technologies: i e., RF technology and integrated circuits. Thus developments in one technology -- e.g.,

IC speed -- that would permit an advance in a data system element capability is not necessarily reflected on a one-for-one basis because of either the limitations or lack of emphasis in another area. Attempts are made to account for this in the discussions where possible.

In summary, an attempt was made to distinguish between what is likely to be available commercially and what is feasible in terms of technology. Projections are based on the use of commercially available components; thus developments at the component level will not be required. Developments at the system level (above the IC level) may be required.

REPORT CONTENT

The report is organized along the lines of the 10 data system elements identified by NASA. Inputs to Sections 1 and 2 will be provided by the Government and were not available for this version of the report Also, inputs to Paragraph 7.1.1 (microprocessors), to be provided by the Government, were not ready for this report These remaining items will be provided in subsequent versions, along with updated information that comes from scheduled activities.

REPORT FORMAT

The report is formatted to comply with NASA's data bank organization and to facilitate update. As a result, a large number of pages are only partially filled.

1. DATA GENERATOR ELEMENTS

(To be provided later)

2. SPACE DATA PROCESSING ELEMENTS

(To be provided later)

3. SPACE DATA STORAGE ELEMENTS

Space data storage elements discussed in this section pertain to the devices and techniques used to store space data for either delayed transmission, delayed processing and display onboard, or physical return of the storage media. Figure 3-1 identifies the subelements that were considered as potential candidates for such storage The majority of the subelements identified in the referenced figure have been ruled out as likely candidates for space data storage either because certain features of these subelements are undesirable for a space data storage system or because they have not been used previously, and there are no known developments going on to make them more attractive to space applications.

The most likely candidates for space data storage between 1977 and 1985 appear to be tape recorders (currently the primary means of data storage for subsequent playback to Earth), magnetic bubbles, and film (for return to Earth physically). A dark-horse candidate that deserves periodic evaluation to assess its potential is Electron Beam Addressable (EBA) memories, also referred to as Beam Addressable MOS (BEAMOS). Although the technology appears to have undesirable features for space applications (relatively low tube lifetime and relatively high power consumption), it has great potential in terms of storage capacity and access time. Subsection 7 2.2 discusses this technology in more detail. Tape recorders are addressed in Subsection 3 1; bubble memories are addressed in Subsection 3.2, and film will be addressed in Subsection 3.3 in future updates of this report.

The approaches that have been ruled out as being likely candidates for space data storage and the rationale for their elimination are:

- Disks - Disks had been ruled out previously in favor of tape recorders, and the technology improvements occurring in both areas do not tend to give disks any more favorable consideration than in the past

- Semiconductors - Semiconductors have been ruled out primarily on the basis of the volatility. However, certain semiconductor devices (CCDs for example) have a

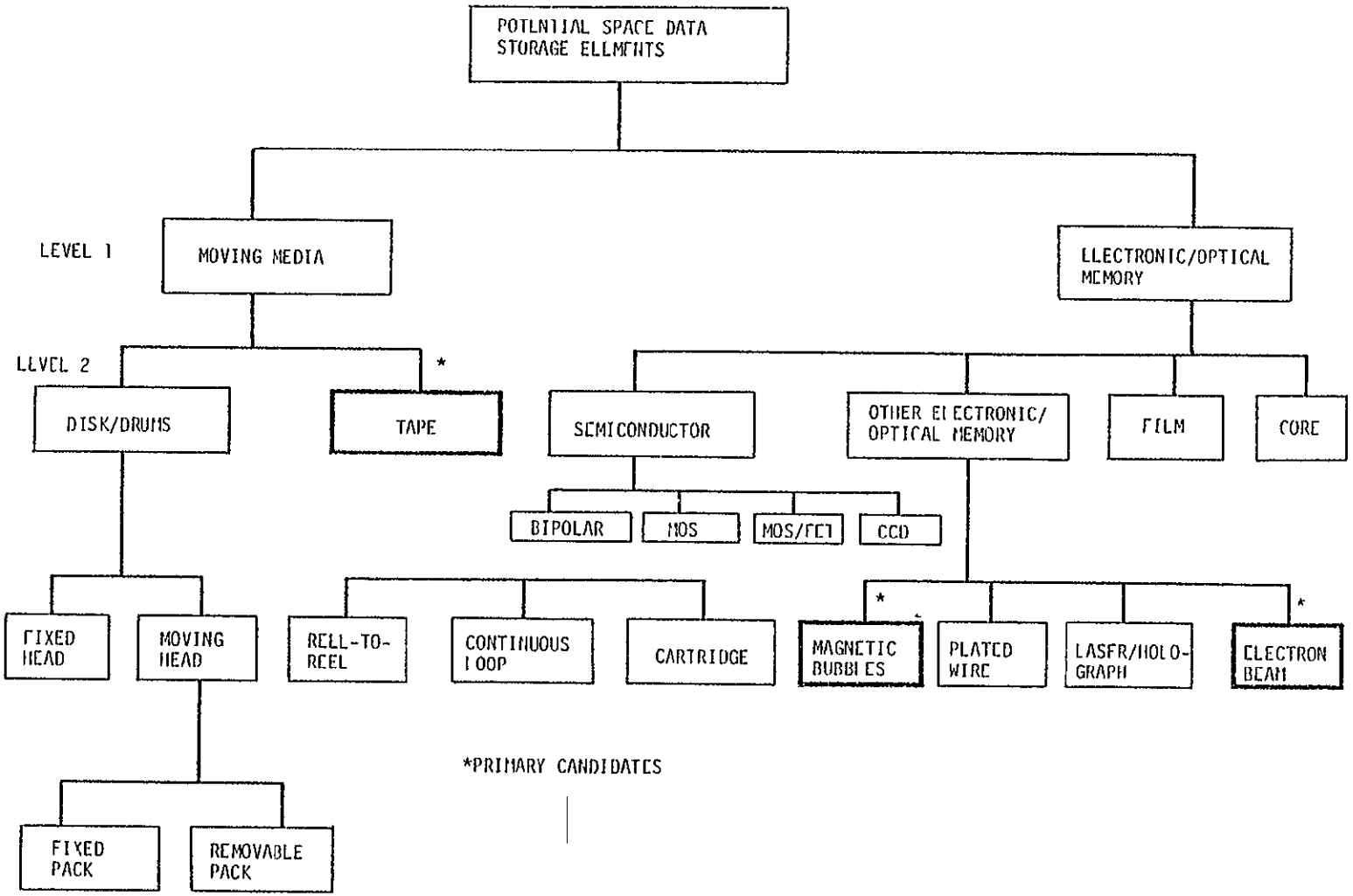

FIGURE 3-1. POTENTIAL SPACE DATA STORAGE ELEMENTS

number of desirable features that could make them contenders for future use as space data storage devices. Also, certain types of semiconductors (MNOS) do not exhibit the characteristic of volatility Semiconductor memory technology is discussed in Section 7.2.1.

- Core - Core was eliminated from contention on the basis of cost, speed, and size

- Plated Wire - Plated wire was not considered a likely candidate on the basis of storage capacity and cost.

- Optical Systems - Optical systems were eliminated on the basis of technology status, which is primarily limited to laboratory type systems at present

3.1 AEROSPACE MAGNETIC TAPE RECORDERS

Tape recorders have provided the primary means for aerospace mass data storage in the past. High-performance magnetic tape recorders are generally classified as either digital recorders, instrumentation type recorders, or video recorders.

Digital tape recorders are used mostly to support data processing applications and are characterized by the need for start-stop operation to permit real-time access and readout of individual records within the tape file. The instrumentation type recorder is generally higher performance in terms of storage density and throughput than the data processing tape recorders Instrumentation recorders are also characterized by continuous rather than incremental operation. Most spacecraft onboard tape recorders are classified as instrumentation recorders. Video recorders are extremely wideband recorders designed for recording and replaying video signals such as those associated with broadcast television. The video recorders achieve extremely wide bandwidth by utilizing rotating heads to effectively increase the speed at which the tape moves across the head. Video recording techniques are currently being applied to the design of both instrumentation and digital tape recorders to achieve higher storage capacities and higher data transfer rates.

This section addresses digital and instrumentation recorders for onboard spacecraft applications Ground instrumentation tape recorders are discussed in Section 6, and data processing tape recorders will be discussed in Section 7 for future versions/updates of this report.

3 1.1 State of the Art in Aerospace Magnetic Tape Recorders

Aerospace magnetic tape recorders generally use one of three basic methods for recording signals on magnetic tape direct recording, fm recording, and digital high-density recording Digital high-density instrumentation recorders are discussed in this section since they represent the recorders with the highest technology and performance that have been built or are currently in development for NASA and DoD applications.

The major improvements in aerospace tape recorder designs in recent years have centered around increased data transfer rates and increased storage capacity. In both cases this has been achieved primarily by increasing the number of tracks per inch either by using higher-density longitudinal heads or by employing rotating-head video recording techniques. The ERTS (Landsat), Skylab Airlock, and Apollo/Soyuz recorders were all rotary-head types that recorded at densities of approximately 6.25×10^5 bits/in^2. The NASA 240-Mbps recorder, currently under development, has a storage density of 1.2×10^6 bits/in^2 using longitudinal (fixed-head) magnetic recording. The U.S. Navy currently has a variable-data-rate, rotary-head recorder under development with a storage density of 2.7×10^6 bits/in^2 Although the Navy recorder is not an aerospace type, it illustrates what can currently be achieved in terms of storage density. Specifications for some of the various aerospace instrumentation recorders under development are presented in Table 3.1.1-1

Recent advances in magnetic tape recording technology that will have an impact on the flexibility and performance of future spaceborne high-density digital recorder designs include the following:

- Read-write head fabrication and materials
- Automatic scan tracking
- Continuously variable data rate recording
- Tape improvements
- Channel coding improvements.

Several companies have reported improvements in head materials, fabrication, and design techniques. These include the multi-turn, thin-film head design recently reported by Applied Magnetics, Inc., and improvements in rotary-head designs, such as IBM's 3850 helical-scan digital

TABLE 3.1.1-1. EXAMPLES OF NASA AEROSPACE TAPE RECORDERS CURRENTLY UNDER DEVELOPMENT

MANUFACTURER	ODETICS	ODETICS	RCA
Model/Name	SCS 1001 (NASA 10^9)	DDS 6000 (Spacelab HDRR)	240 MBS
Year Operational	1978	1978	1979-80
Volume	1,648 in^3	3,393 in^3	5 3 ft^3
Weight	TBD	8.516 in.	200 lb
Max. Input Rate	8.192 Mbps	32 Mbps	240 Mbps
Max. Record Speed	120 in/sec	92 in/sec	100 in/sec
No. of Tracks	8 or 16	22 data + 2 servo	120 data + 22 other
Tape Capacity	2,442 ft	9,200 ft	6,200 ft
Tape Size	0.5 in. by 1 mil	1.0 in. by 1 mil	2 in. by TBD
Storage Capacity	4×10^9 (16 Tracks)	1.7×10^9	1.8×10^{11}
BER	5×10^{-7}	1×10^{-6}	1×10^{-6}
Head Type	Fixed	Fixed	Fixed
Configuration	Coaxial	Coaxial	Coplanar
Max. Power	31W (serial)	161W	270W

recorder in which the heads "fly" at a nominal 10 μin. Because rotating-head recorders have tape-head speeds of 1,000 to 1,500 in./sec, head life of about 1,000 hr in considered normal with "in-contact" heads. The "flying" head should provide virtually unlimited head life.

Automatic scan tracking was developed to allow the reproduce head in video tape recorders (VTRs) to follow the written track more accurately and thus allow closer track spacings. State-of-the-art VTRs achieve tracking errors of less than 1 mil by servo control of the tape speed, drum speed, and mechanical guidance of the tape. Similar techniques are being developed for high-density, fixed-head recorders Automatic scan tracking also makes possible continuously variable data rate changing.

Continuously variable data rate recording provides a high degree of adaptability for data systems with variable data rates. These types of recorders should find increased application in future spacecraft with multiple observation systems that operate asynchronously.

The development of dc-free modulation codes for recording is an important improvement in digital instrumentation recorder design because it provides a significant improvement in BER without an increase in bandwidth. Typically, repetition of a worst-case pattern with large dc content in a conventional digital recorder causes a dc buildup that results in a distorted output waveform and increased BER. The new codes are adaptive such that a code itself changes to eliminate dc buildup, depending on the input data, whenever a pattern with the potential of dc buildup occurs.

3.1.2 Trends in Aerospace Magnetic Tape

The trends in aerospace magnetic tape recorders are toward more tracks per inch of tape width, use of wider (2-in.) tapes, higher data transfer rates, faster start/stop times, variable data rates, higher performance tapes, and use of more sophisticated coding for error control. Other trends include lower cost per bit of storage, greater use of integrated circuitry, and increasing use of rotary-head techniques.

The trend toward more tracks per inch of tapewidth is driven by efforts to achieve greater packing densities (i.e., higher bits per square inch and higher bits per cubic inch) and higher data rates. The reason for increasing tracks per inch (tpi) rather than bits per inch (bpi) is that for a moderately high-bpi system, a bpi versus tpi tradeoff favors tpi increase and bpi decrease. The reason for this is that a 2.1 increase in bpi packing density costs 18 dB of S/N margin, whereas increasing the tpi by 2:1 only costs 3 dB. Difficulties in multi-channel head fabrication and with multi-channel electronics have so far prevented widespread adoption of fixed-head machines with track densities exceeding 42 tpi.

Rotary-head digital recording is emerging as probably the most viable magnetic tape recording technique for future spacecraft onboard storage applications. Rotary-head recorders have already been used for at least three different spacecraft data recording applications and are finding increased application as ground-base instrumentation recorders This trend, plus the need to provide both digital recording with fast start-stop operation and onboard mass storage capability on board future spacecraft, assures the increased use of rotary-head recorders in space One of the main advantages of the rotary-head recorder is its ability to provide fast start/stop operation with minimum tape motion. It should be noted, however, that with current and near-future technology, both the very-high-data-rate recorder (>100 Mbps) and low-data-capacity recorder applications will be dominated by longitudinal fixed-head type recorders

3.1 3 Projected Developments in Aerospace Magnetic Tape Recorders

The rapid increase in packing density and data transfer rates will continue for both the commercially available and custom aerospace recorders. Authorities in the field predict that both rotary-head and fixed-head machines will be available by the early 1980's with transfer rates of 600 Mbps using 2-in. tapes. A projection of data transfer rates through 1985 is given in Figure 3.1.3-1. As seen in Figure 3.1.3-1, the data transfer rate is projected to increase to 1 Gbps on 2-in. tape by 1985.

Figure 3.1.3-2 projects how the number of tracks per inch is expected to increase through 1985 for both fixed-head and rotary-head recorders As previously explained, the increase in track density will be made possible by a combination of head fabrication techniques and automatic tape track following using servo techniques.

Figure 3.1.3-3 illustrates the projected increase in areal storage density for both aerospace recorders and ground recorders. Although there are no technical reasons, other than power and weight requirements, for the aerospace recorders to lag the ground-type recorders in areal storage density, most of the current developments in state-of-the-art recorders are for either ground-based or shipboard applications. For example, RCA is developing a 2.7-Mbit/in^2 recorder for the Navy. Bell & Howell has a contract with Northrop to develop a 270-Mbps recorder for the Air Force One source indicated that NSA is currently looking for a 600-Mbps recorder.

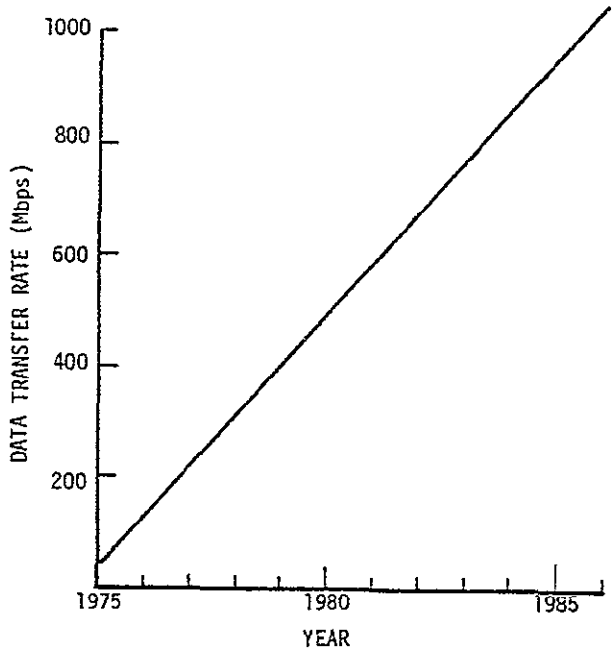

FIGURE 3.1.3-1. MAGNETIC TAPE DATA TRANSFER RATES (2-in.-wide tape)

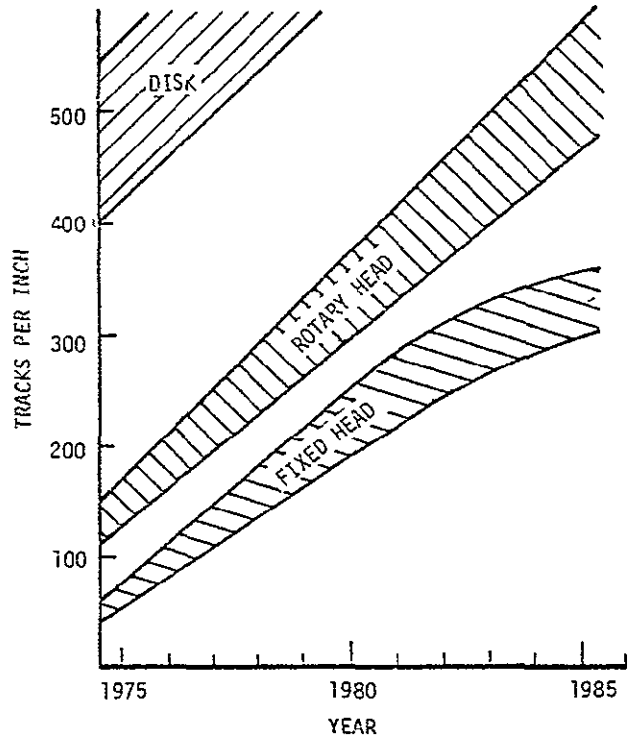

FIGURE 3 1.3-2. OPERATIONAL MAGNETIC TAPE DENSITY

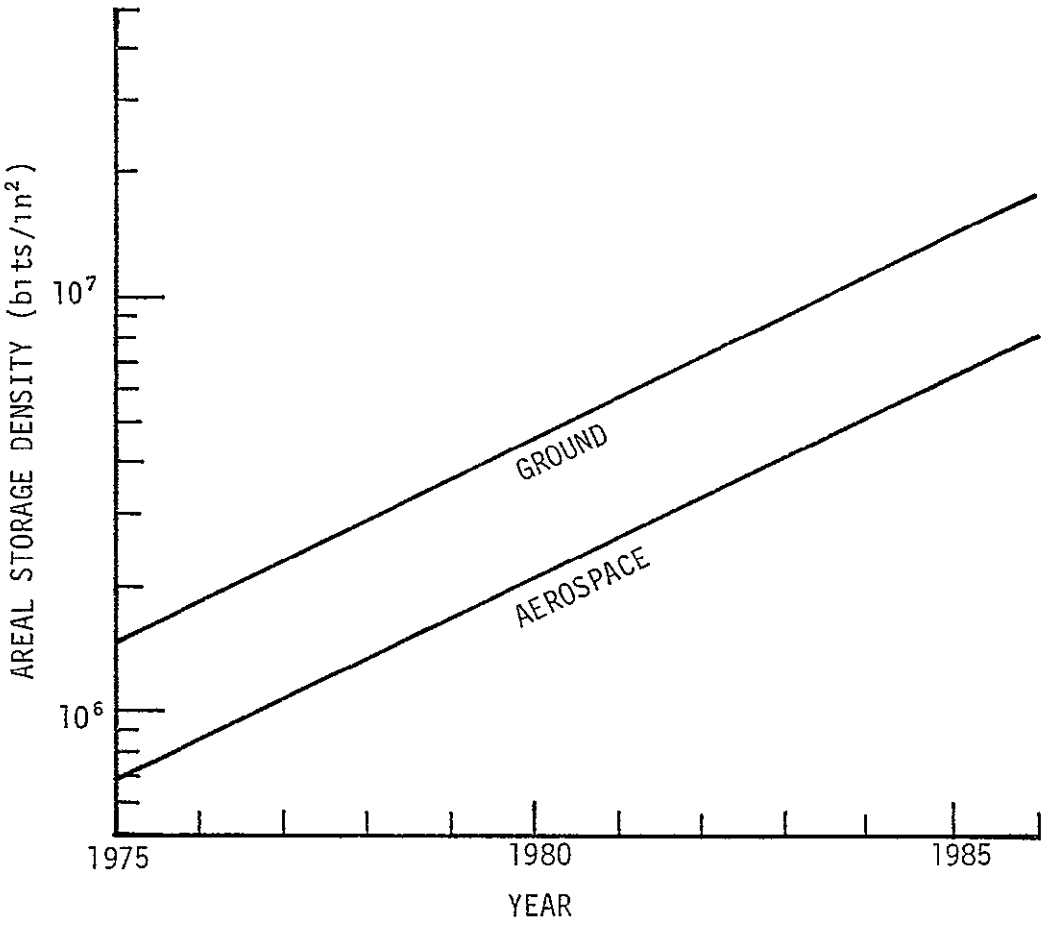

FIGURE 3 1 3-3 MAGNETIC TAPE STORAGE DENSITY

3 2 MAGNETIC BUBBLE MEMORIES

Magnetic bubbles exhibit very favorable characteristics for space storage applications, including high storage densities and capacity, relatively low power consumption per bit of storage, high reliability, and nonvolatility NASA is currently sponsoring development work on magnetic bubbles for mass data storage purposes. This development work, combined with the rapid developments elsewhere in the area of bubble technology, makes magnetic bubble memory a primary contender for future use as a mass storage device in spacecraft.

Magnetic bubbles are mobile cylindrical magnetic domains that can be generated in a thin flat magnetic film material and moved about in the medium by the application of an external magnetic field The bubbles are guided within the film layer by interaction with propagate paths that are processed into the layer and magnetized by the external magnetic field

Bubble memories are normally implemented as conventional linear shift registers in which the minimum spacing between adjacent bubbles is defined as the propagate period. Some geometric features of various bubble structures are defined in the following subsection.

Significant progress in bubble memory development has been made since 1967, when magnetic bubbles were first invented at Bell Laboratories and 100-μm bubbles were being discussed, to the present day, when 4-μm-diameter bubbles are currently used in production devices. Impressive as this past work has been, future work may be even more so as bubble diameters tend toward the theoretical limit, which is estimated to be 0.01 μm (Ref. 3-1)

3.2.1 State of the Art in Magnetic Bubbles

Magnetic bubble technology is to the point where developmental prototypes and limited production of chips in the 65- to 100-kbit range is fairly widespread (Ref. 3-2). Rockwell has built prototypes of 1-Mbit bubble chips on a 400-by-400-mil die with 2-μm bubbles and an 8-μm period Western Electric is currently producing a 272-kbit bubble memory package that contains four 68-kbit serial shift register chips. The unit is used to store 12 sec of speech in the 13A Voice Announcement System. Several other companies are currently testing the commercial market with complete bubble memory subsystems having storage capacities that range from 800 kbits to 8 Mbits.

Access times for current bubble memory devices depend on the individual bubble chip architecture and range from 0.1 msec to 0.5 sec. Many different ways have been developed to organize a bubble memory chip The simplest organization is a single-loop shift register. A 100-kbit single-loop chip operated at a 100-kHz shift rate has an access time of 0.5 sec. For applications requiring improved performance, the major/minor-loop organization is most frequently used. The access time for the 100-kbit chip is reduced to less than 4 msec if a major/minor-loop organization is used. This improvement in performance is obtained with an attendant increase in bubble chip complexity, interface electronics, and control logic. Since total access time is a combination of the minor-loop access time plus the major-loop access time, replacing the major loop with a decoder circuit further decreases access time. Rockwell has reported success (Ref. 3-3) in decreasing access time through the use of hybrid systems involving a combination of major/minor loops and decoder organizations. Although decoders decrease access time, they are considered complex, they dissipate relatively high power, and a reliable decoder is difficult to achieve. Near-future applications for bubble memories as onboard spacecraft storage devices are for high-reliability tape recorder replacements; hence access time is not the major design consideration. The 10^8-bit bubble memory recorder currently being developed for NASA by Rockwell has an access time of 0 5 sec.

Data transfer rates for a bubble memory system are a function of drive frequency, chip density, chip organization, and system organization Typical drive frequencies range from 50 Hz to 300 kHz, with several companies reporting chips capable of operation to 500 kHz. The maximum drive frequency is limited by the maximum bubble velocity and the repetitive circuit period, λ. For a bubble memory with an 8-μm period fabricated from garnet film with a maximum bubble velocity of approximately 1,000 cm/sec, the practical upper frequency limit is approximately 600 kHz In systems such as the 10^8-bit NASA bubble memory, data rates much higher than the chip drive frequency are achieved by parallel reading or writing of multiple chips within the memory system.

Increases in chip density are a major goal for designers of bubble memory systems. Most bubble memory devices to date, including the 100-kbit Rockwell chip and the 92-kbit TI chip, have utilized the T-bar propagate structure. The T-bar with two gaps per propagate period has been recently replaced in most laboratories by more efficient single-gap structures such as shown in Figure 3.2.1-1. The asymmetric half disk, which was invented at Bell Laboratories, provides a four-fold increase in density over the T-bar using the same wafer processing capability. Rockwell has utilized the asymmetric disk structure with 2-μm bubbles and an 8-μm period to construct a 1-Mbit chip with a storage density of 1.5×10^6 bits/cm^2. The asymmetric chevron, which was also invented at Bell Laboratories, provides an additional factor of two improvement in chip density over the asymmetric half disk. The asymmetric chevron structure enables chip densities approaching 4 Mbits/cm^2 using current wafer-processing techniques.

There has been a continued evolution in bubble memory cell packaging design to make construction more reliable, smaller, and simpler to manufacture. The 272-kbit memory cell, designed by Bell Laboratories and manufactured by Western Electric, is packaged as a four-chip configuration on a single plane in a 32-pin dual-in-line package (DIP). The package is approximately 1.2 in wide, 2.2 in. long, and 0.6 in. high and contains a circuit board, rotation field coils, a bias field coil, a permanent magnet

1. T-BAR

- 1/16 PERIOD MINIMUM FEATURES
- DEFECT SENSITIVE BARS

2 ASYMMETRIC HALF DISK

- 1/8 PERIOD MINIMUM FEATURES
- NO BARS
- NO CHANNEL-TO-CHANNEL INTERCONNECTS

3 ASYMMETRIC CHEVRON

- GAP TOLERANT
- INTERMESHED ADJACENT CHANNELS

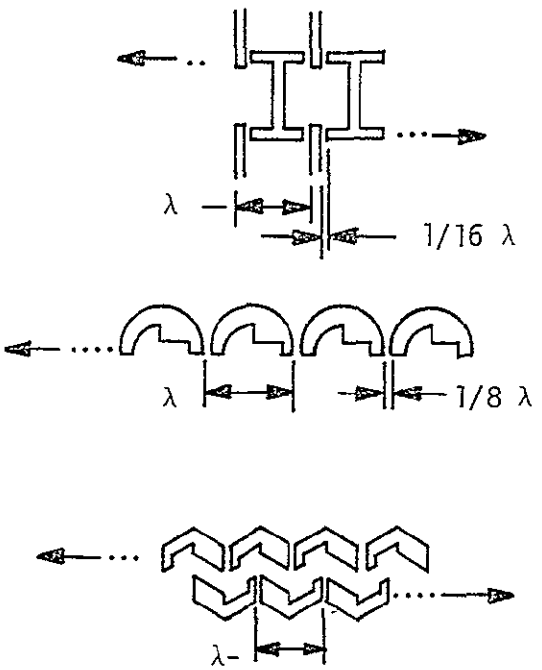

FIGURE 3.2.1-1. EVOLUTION OF PROPAGATE STRUCTURES

structure consisting of a permanent magnet and a high permeability ferrite plate, and a mu-metal can that serves as a shield against external magnetic fields. Bubble memory packages of this type have been successfully operated from 0°C to 80°C. The bubble cell for the NASA 10^8-bit Data Recorder contains a pair of printed circuit boards, each with eight 102-kbit bubble chips The cell, which includes magnetics, measures 1 5 by 3.0 by 0.5 in. The TI TBM 0103 packages a single 92-kbit chip and associated magnetics in a 1.02 -by 1.1- by 0.4-in. 14-pin DIP.

Cost per bit of storage was in the range of 0.05 to 0.10¢ in 1976 according to a number of reports. At this cost, it was competitive with head-per-track disks and floppy disks and was generally lower than semiconductor memories.

Chip yields on the order of 20 to 30% have been reported. The application of improved propagate structures such as the asymmetric chevron proposed by Bell Laboratories with only one permalloy feature and only one gap per propagate period should further improve chip yield by lowering the statistical probability of processing defects causing problems.

Rockwell International's Autonetics Group is currently developing a 10^8-bit bubble memory system for NASA/Langley. The purpose of the program is to determine the applicability of bubble technology to spacecraft data recording applications by development, design, fabrication, and test of a flight-qualifiable, solid-state data recorder. This program is representative of the current state of the art in bubble technology for spaceborne applications. Table 3 2.1-1 presents a comparison of the NASA 10^8-bit solid-state (bubble memory) data recorder with the NASA 10^8-bit standard recorder and the NASA 10^9-bit standard recorder.

TABLE 3 2.1-1. COMPARISON OF NASA 10^8-BIT SOLID STATE RECORDER WITH STANDARD 10^8-BIT AND STANDARD 10^9-BIT RECORDERS

	NASA 10^8-BIT BUBBLE MEMORY	NASA 10^8-BIT STANDARD RECORDER	NASA 10^9-BIT STANDARD RECORDER
Manufacturer	Rockwell	RCA	Odetics
Year Operational	1978	1976	1978
Volume	616 in^3	363 in^3	1,648 in^3
Weight	40 lb	14 lb	TBD
Storage Capacity	1×10^8 bits	4.5×10^8 bits	4×10^9 bits
Data Rate	1.2 Mbps (serial) 2 4 Mbps (parallel)	2 kbps to 2.56 Mbps	6.25 kbps to 8 19 Mbps
Power Min/Max	13.5 W/103 W	7 W/17 W	18 W/46 W
Standby	TBD	2.3 W	1 W
BER	1×10^{-8}	1×10^{-6}(EOL)	1×10^{-6}(EOL)
MTBF	40,000 hr	30,000 hr	TBD

3.2.2 Trends in Bubble Memories

Research in bubble memories is proceeding on many fronts, including materials, lithography, propagating structure design, chip organization and configuration, fabrication processes, and packaging. The results are enabling improvements in a number of important areas such as storage density and capacity per chip, higher yields on larger chips, improved temperature and bit error performance, improved packaging that enables bubble chips to be used with integrated circuit chips, improved fabrication techniques leading to one-step fabrication, lower cost, and increases in potential applications.

Currently, bubble memory chip designs are evolving in two directions corresponding to identified market areas. One type of chip is configured for maximum storage density and is intended for applications where access time is not critical, such as airborne tape recorder replacement. The other type of chip design is intended for disk replacement applications that require access times that are less than 1.0 msec. Future storage capacity projections for both types of chips are presented in Section 3.2.3. Chip capacities are currently increasing by a factor of four per year. This trend should continue through 1980. By 1985, commercially available chips will have at least 1,000 times the storage capacity of currently available chips (approximately 100 kbits). However, smaller-capacity chips (2 to 8 Mbits) with faster access times will most likely dominate the bubble memory market. The larger-capacity bubble memory chip designs will incorporate on-the-chip fault tolerant circuit arrangement to maximize the processing yield for the large-capacity devices.

The use of electron-beam fabrication and X-ray lithography will enable much larger capacity chips to be fabricated by increasing both storage density and chip size. Chips fabricated using photolithography are currently limited in size to approximately 1 cm^2 with 1-μm minimum features. Using electron beam fabrication and X-ray lithography, the resolution limit can be reduced to 0.2 μm or less. Electron-beam fabrication also makes possible much larger chips; however, it is not believed that chips much larger than 1 cm^2 will be economically practical.

In addition to improved fabrication techniques, several experimental bubble devices have the potential for additional fugure increases in chip densities. These devices are known as the contiguous disk and bubble lattice The contiguous disk currently appears to offer the most promise as the next-generation bubble memory. The contiguous disk device uses propagating structures consisting of connected elements shaped like disks or diamonds. Because of the absence of gaps which have to be resolved photographically, the density can be increased by approximately a factor of four times the density of the asymmetric chevron. The bubble lattice is fundamentally different from the other devices. It packs bubbles closely together in a hexagonal lattice and stores information in two kinds of bubbles with different magnetization. According to Ho and Chang of IBM's T. J. Watson Research Center (Ref 3-4), the bubble lattice will necessitate more complicated structures than discrete bubble devices when implemented in functionally complete chips. Other authorities, including Bonyhard of Bell Laboratories, do not believe that the bubble lattice is a practical approach for achieving higher-density devices.

3.2.3 Projected Developments in Bubble Memories

The rapidly changing state of the technology in magnetic bubbles assures significant improvements over the existing state of the art. The projections presented in the following paragraphs are based on trends in bubble technology during the last 3 to 4 years and on an assessment of the statements of a number of authorities in the field. It should also be noted that there is a gap between laboratory accomplishments and commercially available technology. The following discussion concerns projections of commercially available technology rather than laboratory accomplishments.

The trends identified in Subsection 3.2.2 will result in the introduction of a number of products employing magnetic bubbles during 1977, with substantial increases in such products during the coming years. Applications that will employ bubble memories extensively by 1980 include microprocessors, minicomputers, smart terminals, desktop computers, point-of-sale terminals, and replacements for fixed-head disks and drums. Other potential applications for 1980 include military systems, aircraft and spacecraft recorders, data collection terminals, and special signal processing devices. Applications projected for 1985 include all the above applications on a larger scale including replacements for head-per-track disks and mass storage systems in general.

Several authorities have projected that chips with storage capacities of 10^8-bits/chip will be commercially available by 1985. This can be achieved either by fabricating larger chips or by utilizing smaller device structures. Figure 3.2.3-1 gives a projection of commercially available bubble chip storage capacities through 1985.

The cost of commercially available memory systems is currently about 80 millicents per bit, as shown in Figure 3.2.3-2. As seen in the figure, the system cost should drop to 1 to 3 millicents per bit by 1985, depending on memory size, access times, etc These cost figures are based on the opinions of various experts for fast access bubble memories as represented by curves A and B of Figure 3.2.3-1.

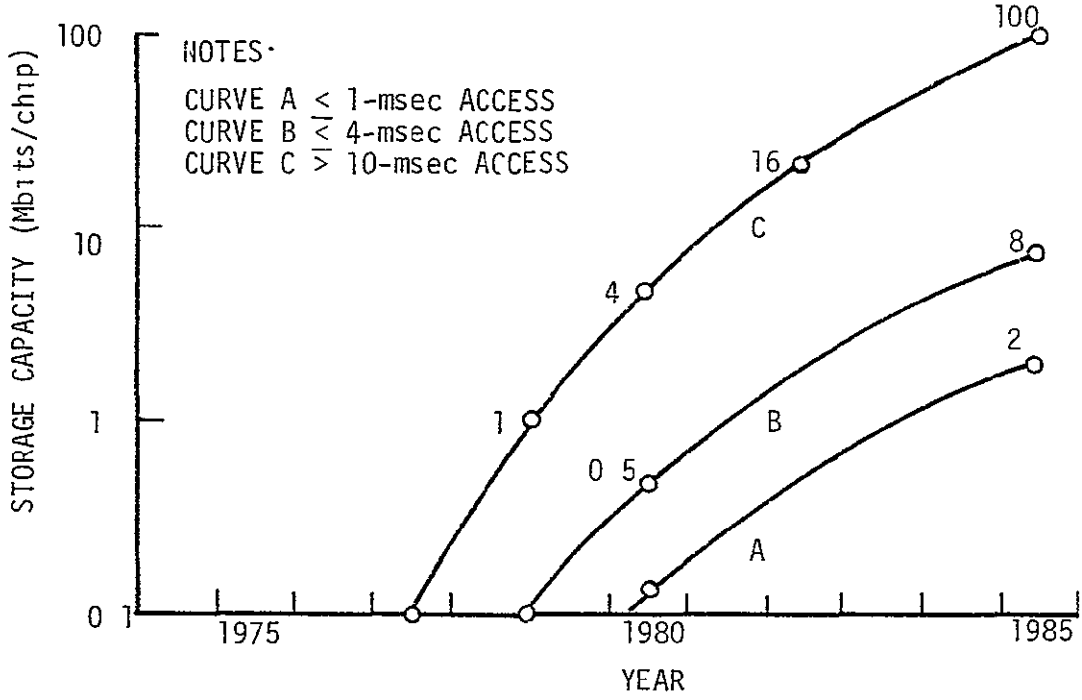

FIGURE 3 2.3-1. STORAGE CAPACITY PROJECTION - PRODUCTION BUBBLE MEMORY CHIPS

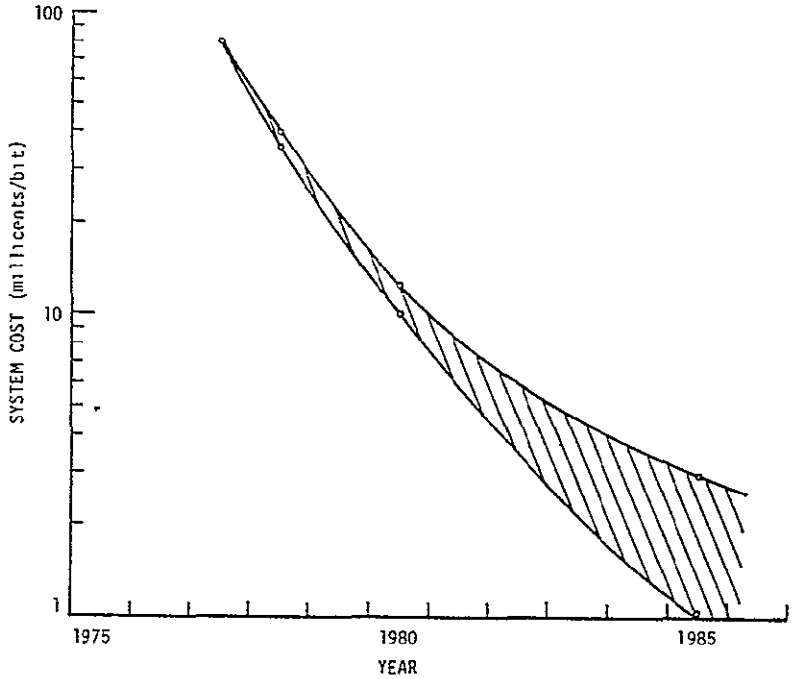

FIGURE 3.2.3-2. BUBBLE MEMORY SYSTEM COST PROJECTION (COMMERCIAL)

Although most authorities believe that bubble applications will be limited to storage requirements of 10^9 bits or less, Rockwell currently has an Air Force contract to study the feasibility of building an airborne 10^{12}-bit bubble memory system. Rockwell claims that this system could be operational before 1985 and the system goals represent a reasonable estimate of projected spaceborne bubble memory technology for that time period. The conclusion after completing the first year of the study is that most of the system design goals, with the exception of volume and power, can be achieved with current bubble technology and it is reasonable to assume that a system that meets all the system goals can be built in the early 1980's. Table 3.2.3-1 compares the system goals for the Air Force 10^{12}-bit bubble memory system and NASA 10^8-bit bubble memory data recorder currently under development.

TABLE 3.2 3-1 COMPARISON OF NASA 10^8-BIT BUBBLE MEMORY DATA RECORDER AND AIR FORCE 10^{12}-BIT MEMORY SYSTEM GOALS

	NASA 10^8-BIT BUBBLE MEMORY	AIR FORCE 10^{12}-BIT BUBBLE MEMORY SYSTEM GOALS
Year Operational	1978	1985 (est.)
Volume	616 in^3	3,456 in^3
Weight	40 lb	120 lb
Storage Capacity	10^8 bits	10^{12} bits
Power (Max)	103 W	200 W
Data Rate (Max)	2.4 MHz	50 MHz

NASA's Langley Research Center is also developing a standard 10^7-bit bubble memory (SBM) for relatively low-storage-capacity applications The SBM will weigh 15 lb and occupy a volume of 275 in^3. The SBM will have the capability for recording or playback of asynchronous data from dc to 1,024 Mbps. The SBM will also provide the capability to simultaneously record and play back.

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4. SPACE DATA HANDLING ELEMENTS

Space data handling is defined herein as encompassing the functions that take place between the output of the data source (instrumentation outputs, computer outputs, imaging system outputs, etc.) and the input to the modulator for the downlink. Figure 4-1 presents the areas of coverage in terms of the various methods that are commonly used to combine and format the data for input to the communications system. Figure 4-1 subdivides data handling into analog systems and digital systems The breakdown for the analog systems is more or less self-explanatory; however, the breakdown for the digital systems is somewhat arbitrary. The digital systems are subdivided into general-purpose digital data systems, unique/dedicated data systems, and high-rate digital data systems. The major emphasis in this section is on digital systems, since the majority of the data systems of the future will be digital and this is the area that will be most heavily impacted by technology advances.

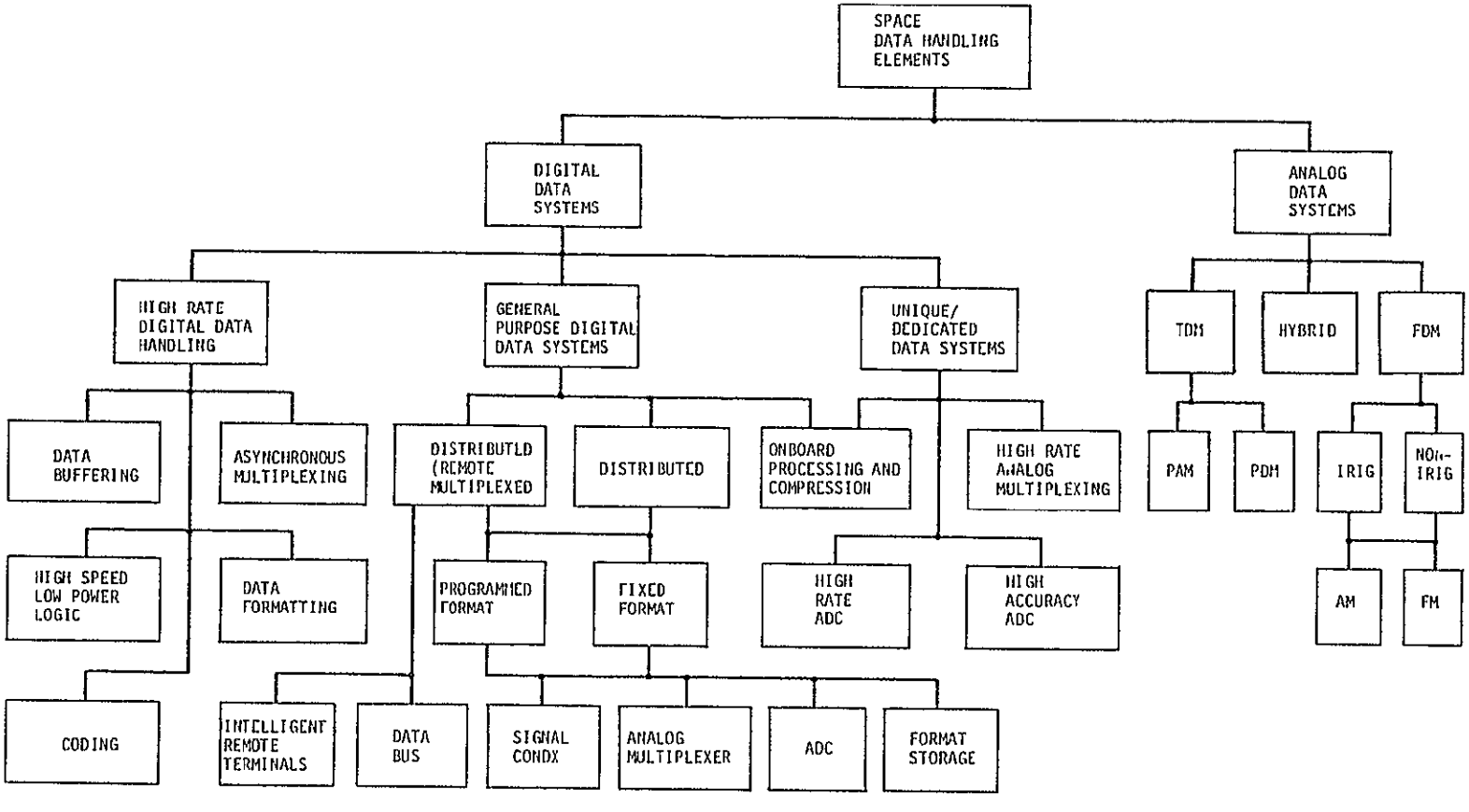

FIGURE 4-1. SPACE DATA HANDLING ELEMENTS

4.1 DIGITAL DATA HANDLING SYSTEMS

Space digital data handling system elements are subdivided into general-purpose, unique/dedicated, and high-rate data systems Although most of the digital data system elements can be classified in this manner, some tend to contradict this division. The division between unique/dedicated and high-rate data handling is somewhat arbitrary in that most of the high-data-rate systems are also unique/dedicated systems. In general, the high-rate digital data handling discussion includes both very-high-rate (>50 Mbps) dedicated systems and also applications in which several general-purpose or unique/dedicated system outputs are combined to form a single high-rate (>10 Mbps) output.

The trend during recent years has been toward the increased use of flexible general-purpose digital data systems for onboard spacecraft data handling applications. As the speed of data systems increases, the flexibilities that are provided become more difficult to implement. In addition, the very-high-speed data sources tend to be unique in that they are designed to have only a limited number of output channels that feed a dedicated communication link.

The need for high-rate digital data handling is twofold. First, large space systems, such as Spacelab, will simultaneously operate a number of experimental data systems with a combined output data rate that approaches 50 Mbps. The second application of high-rate digital data systems is for high-resolution imaging sensors such as the Thematic Mapper on Landsat-D which has an 83-Mbps output data rate. Future systems will require data rates in excess of 500 Mbps. Systems that operate above 100 Mbps are of particular concern because of the large amounts of power consumed to operate conventional logic designs at these speeds.

4.1.1 General-Purpose Digital Data Systems

General-purpose digital data systems include the various types of general-purpose PCM telemetry and instrumentation systems ranging in size from small PCM multiplexer/encoders to very large, remote, multiplexed instrumentation systems that can accommodate several hundred input channels. Typical systems that are available for space applications operate at rates ranging from 50 Kbps to 2 Mbps. Such systems are available from a number of companies, including: Aydin Vector, Base Ten Systems, Gulton, SCI Systems, and Teledyne Telemetry. These systems are flexible in that they are capable of accepting various combinations of high-level and low-level analog signals and discrete (bilevel) signals. Additionally, most offer some flexibility in selection of sample rates, word length, bit rate, and synchronization codes via both programmable and hardware options. Systems in this classification are generally available as off-the-shelf hardware. These systems normally provide PCM outputs that are IRIG-compatible.

Not all general-purpose data systems are characterized by a PCM output to a data collection ground station. Some data systems, such as those used in advanced military aircraft, communicate via a data bus to a central computer that provides the data monitoring, display, and control functions in real time. These systems often use general-purpose remote terminals that are very similar to the remote terminals used in space applications (such as the Shuttle MDM). The Department of Defense has recently adopted MIL-STD-1553A as a data bus standard for airborne military systems applications. NASA does not currently have a similar data bus standard that is recognized and used for all new system developments, however, NASA is developing a set of standards that define interfaces and operational characteristics for both the internal and external interfaces of Multiplex Serial Data Acquisition and Distribution Systems (MSDADS).

4.1.1.1 State of the Art in General-Purpose Digital Data Systems - A number of companies build general-purpose PCM systems and distributed instrumentation systems capable of handling 1 Mbps and below, and 2-Mbps systems are readily available in either single units or in combinations of multiple lower-rate units. Data rates to 10 Mbps for space-qualified systems are within the state of the art, but such systems are custom-built to the customers' specifications. During recent years, the trend in large instrumentation systems has been toward greater system flexibility and modularity. Several companies offer systems that feature remote multiplexers/demultiplexers that can be reconfigured simply by changing interface cards or modules to provide various combinations of system input/output capability.

Examples of standard system interface modules include:

- Analog multiplexers
- Discrete multiplexers
- Serial multiplexers
- Frequency converters
- Digital-to-analog converters
- Discrete Outputs
- Serial outputs.

Features that are available in state-of-the-art large data acquisition systems include:

- Programmable format selection
- Programmable channel selection
- Programmable analog channel gain
- Programmable analog channel offset.

Programmable gain and programmable offset increase system flexibility by allowing a single input channel to function either as a high-level channel or as a low-level channel simply by reprogramming the format controller. Programmable gain ranges that are available go from less than 1 to greater than 500 Another advantage of programmable gain and offset is that it allows the system to interface directly with transducers with minimum signal conditioning.

Another system design feature that is included in most state-of-the-art data systems is Built-In-Test (BIT) capability. Most current data systems provide the capability for either automatically testing or testing on command upwards of 90% of the circuitry within each unit of the system.

At the component level, current state-of-the-art circuitry includes hybrid analog-to-digital converters and 16-channel random-access multiplexer chips. The use of LSI circuitry for analog multiplexer applications is usually limited by system design constraints that include requirements that do not allow a multiplexer circuit failure to affect multiple channels. The Analog Devices AD572 12-bit successive approximation analog-to-digital is representative of state-of-the-art circuitry for general-purpose data system applications. The converter is packaged in a 1.74- by 1.14-in. hybrid module and features low power consumption (900 mW) and a conversion time of 25 μsec. Datel Systems manufactures a similar hybrid analog-to-digital converter (Model ADC-HX12 BGC) that performs a 12-bit conversion in 20 μsec.

4.1 1.2 Trends in General-Purpose Digital Data Systems - Trends in the development of general-purpose digital data systems are affected both by technology advances as well as trends in the other system hardware that interfaces with the data system. Most authorities predict the continued demise of sensors and subsystems that output analog signals to the data system. Although this trend has already eliminated most of the analog type outputs from the larger spacecraft subsystems such as inertial platforms and experiments, there are a number of types of onboard sensors (e.g., temperature and pressure) that most likely will continue to provide analog inputs to the data system.

Generally, the trends in general-purpose digital data systems are toward increased capability and flexibility, smaller size, and lower power consumption. Flexibility will continue to be enhanced in future systems as microprocessors and memories with greater capacities are incorporated into the designs. Bubble memories (Subsection 3.2) will probably replace plated wire memories and E-PROMS for nonvolatile program storage in future system format controller designs.

Future general-purpose data systems will utilize microprocessors within the remote terminals to perform functions such as data queueing, data compression, and buffer storage. These intelligent remote terminals will significantly reduce the amount of traffic on the data bus by eliminating much of the nonessential data transmitted on the bus.

In addition to advances in MSI and LSI logic complexity, improvements in linear circuit devices and hybrid circuit packaging techniques are evolving to improve system performance, size, and cost. In general, the degree to which LSI can be employed in linear circuitry is limited compared with digital technology because linear circuits must withstand higher voltages, typically 30 to 40 V. Therefore, oxides in linear devices must be five to ten times thicker than for digital circuitry; hence the resulting device geometries are much larger. Some experts expect to see increased use of MOS/CMOS linear devices on future data systems as the performance and the costs of these devices challenge their bipolar counterparts.

The Department of Defense currently has two programs to demonstrate fiber optic data transmission in an operational airborne environment. One program is being managed by the Naval Electronics Laboratory and the other program by the Air Force Avionics Laboratory. The outcome of these programs should significantly affect the role of fiber optics for future data bus applications in general-purpose data handling systems Fiber optics offers the advantages of light weight, high data handling capacity, high security from jamming, and a high immunity to EMI/EMP effects. Both the Navy and the Air Force are engaged in developing components and modules as well as systems. The Navy is working on devices for second-generation 10-Mbps systems. The Air Force is concentrating on the development of low-cost electrical-to-optical and optical-to-electrical interface circuits.

Hybrid circuit packaging techniques are used to achieve small package size in many state-of-the-art data system designs According to various authorities, there have been no radical changes in hybrid circuit packaging technology during the last 5 years. The packaging of hybrid circuits has been evolving slowly during the past 5 years and should continue to do so in the immediate future.

4.1.1.3 Projected Developments in General-Purpose Digital Data Systems - Projected developments in general-purpose digital data systems are toward flexibilities and capabilities heretofore unavailable. The most significant development will be the ability by 1985 to package a powerful computer with a large memory (on the order of 10-Mbits) on a single small PC board, thus making it possible to perform complex processing functions within each remote data terminal.

Another projected development is an increased requirement for asynchronous multiplexing and associated data buffering. Low-cost bubble memories and/or CCD memories will be used to provide buffer storage for asynchronous data interleavers and temporary data buffers.

The cost of analog-to-digital converters should be significantly less by 1985. Figure 4.1.1 3-1 projects integrated circuit analog-to-digital converter costs for the 1980-1985 timeframe. The performance of these devices should be significantly better than currently available low-cost units. The projected speed for the 1985 integrated circuit devices shown in Figure 4.1.1.3-1 is 60 nsec for 8 bits and 150 nsec for 12 bits By 1985, faster integrated circuit converters will be available, but not in mass production.

Table 4.1.1.3-2 compares some typical characteristics of current gneral-purpose data systems and general-purpose data systems that will be in general use by 1985.

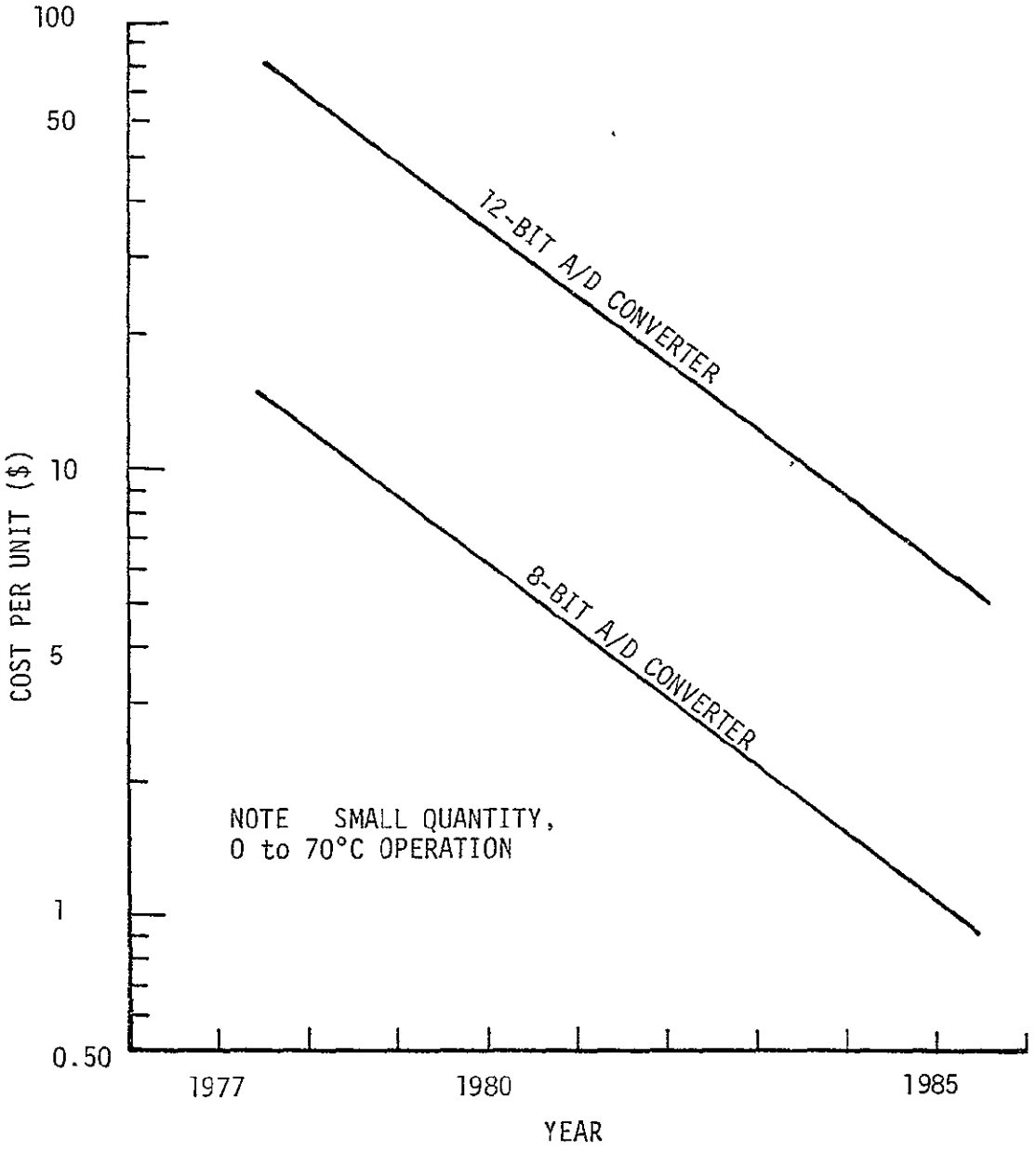

FIGURE 4.1 1.3-1. ANALOG-TO-DIGITAL CONVERTER COST PROJECTION FOR PRODUCTION HYBRID/ INTEGRATED UNITS

TABLE 4.1.1 3-1. COMPARISON OF TYPICAL CURRENT AND FUTURE GENERAL-PURPOSE DIGITAL DATA SYSTEMS

CHARACTERISTIC	CURRENT (1977)	1985
System Type	Modular, stored program, party line	Modular, stored program, party line
Data Output Rate	500 kbps	5 Mbps
Party Line Construction	Twisted shielded pair	Fiber optics
Party Line Rate	1 Mbps	10 Mbps
Party Line Operation	Command-response	Asynchronous demand
Remote Unit Capacity	32	32
Central Unit Processing Capability	Sample format, gain offset	Remote unit parity, data queueing, security encoding, correlative analysis, etc
Remote Unit Programming Capability	Remote unit address	Channel (sample rate), offset, data distribution, data compression, self-test, limited analysis, etc.

4.1.2 Unique/Dedicated Data Systems

The unique/dedicated digital data systems are defined to include those systems that are either dedicated to a single high-data-rate sensor or require unusual data-handling capabilities that are not practical to implement with a general-purpose data system. Examples of unique/dedicated data systems are the various types of IR and visible imaging systems that will be used on future Earth resources missions. The unique/dedicated data systems applications include the Multispectral Scanner and Return Beam Vidicon data systems on Landsat 1 and 2 and the Thematic Mapper and Return Beam Vidicon systems on Landsat-D. The analog circuit and system aspects of the unique/dedicated data systems are discussed in this subsection. The associated digital circuit technology is discussed in Subsection 4.1.3.

4.1.2.1 State of the Art in Unique/Dedicated Data Systems - The "Multimegabit Operation Multiplexer System" (MOMS, Ref. 4-1), developed by Harris Corporation for the Goddard Space Flight Center, represents the current state of the art in unique/dedicated data systems. The system was developed to prove the feasibility of implementing a high-rate data system for the Landsat-D Thematic Mapper application. MOMS consists of two 140-Mbps subsystems from which the outputs are interleaved to produce a combined system output data rate of 280 Mbps. Each of the 140-Mbps subsystems consists of a multiplexer with 30 radiometer channels and 2 vidicon channels, sample-and-hold circuits, and a 20-Msample/sec by 7-bit analog-to-digital converter. Although MOMS was only implemented as a breadboard, the system has a projected volume of 625 in^3 and a power requirement of 30 W.

The MOMS multiplexer uses a two-level gating arrangement that employs a sophisticated bipolar analog switch with a 12-nsec settling time. The sample-and-hold circuits are used only for the two vidicon channels.

The MOMS analog-to-digital converter is a series-parallel type that consists of two series stages, each of which contains 16 parallel comparators. The first stage encodes the four most significant bits. These four bits are then reencoded by a digital-to-analog converter and subtracted from the input signal. The second stage encodes the subtracted difference. Since completing the MOMS contract, Harris has redesigned the analog-to-digital converter to provide 8-bit resolution at 30 Msamples/sec.

In addition to the series-parallel type of analog-to-digital converter used in MOMS, two other types of ultra-high-speed analog-to-digital converter designs are frequently used in high-rate data systems. These are the cyclic converter and the parallel converter.

The parallel converter is a "brute force" approach that utilizes 2^N-1 comparators to implement an N-bit converter. Although the parallel type converter is very fast (<20 nsec), except for use in low-resolution applications, most designs to date are too large and require too much power to be used in aerospace data systems.

The cyclic analog-to-digital converter consists of a series string of nonlinear amplifier stages each with a transfer function as shown in Figure 4.1.2.1-1. The converter is named cyclic because the voltage at the outputs of each stage cycles up and down as the input voltage varies linearly. The cyclic converter has the advantage of high speed with minimum circuitry The main disadvantage of the cyclic converter is accuracy, since accuracies in excess of 7 bits are difficult to achieve. The cyclic converter binary representation is inherently generated in Grey code. For applications requiring binary, Grey-code-to-binary converters are used.

The Computer Labs MATV series of analog-to-digital converters overcomes the accuracy limitation of the cyclic converter by using a cyclic scheme to encode the six most significant bits and a parallel encoder for the two least significant bits. The MATV converters provide 8-bit accuracy and are packaged in a configuration suitable for aerospace applications. Other specifications include a conversion time of 50 nsec, power consumption of 8 W, and size of 5.5 by 4.8 by 0.85 in.

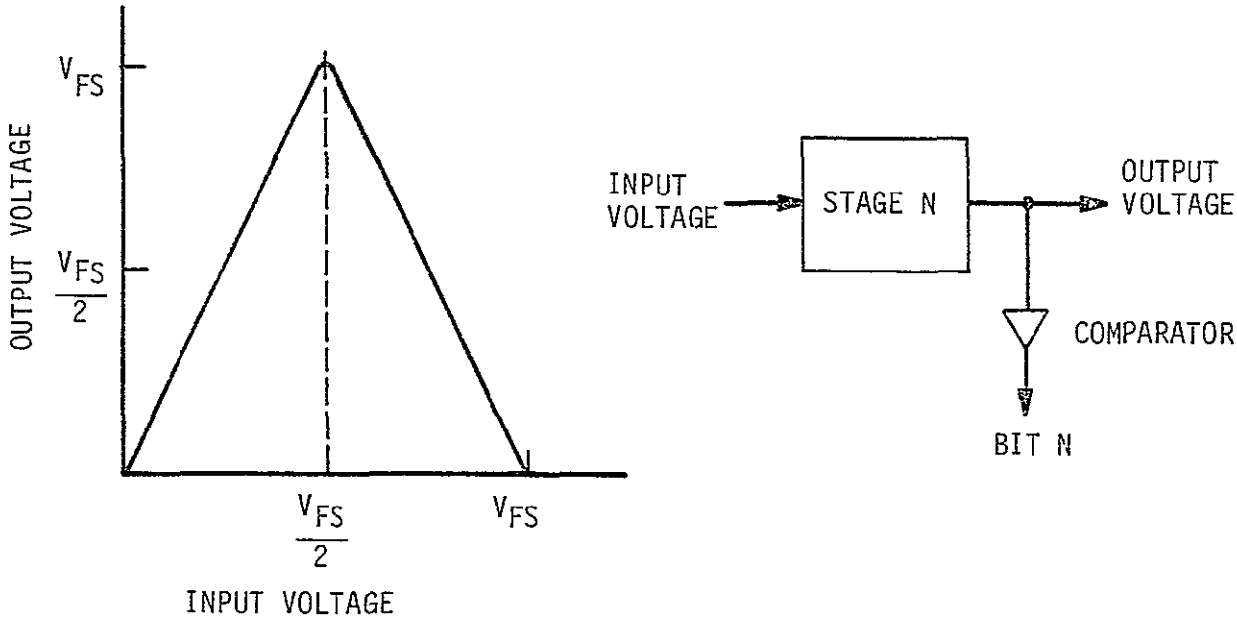

FIGURE 4.1.2.1-1 CYCLIC ANALOG-TO-DIGITAL CONVERTER STAGE TRANSFER FUNCTION

Advanced Micro Devices, Inc., is currently developing a 4-bit quantizer with 8-bit accuracy. Each 4-bit quantizer contains 16 high-speed comparators with an associated resistor divider network and logic packaged as a single LSI integrated circuit. Using two of these devices plus some additional circuitry, a series-parallel 8-bit converter with a 20-Msample/sec word rate can be built. Sixteen of these ICs can be used to build a parallel 8-bit converter with a 100-Msample/sec (800-Mbps) word rate. These 4-bit quantizers make it feasible to build relatively small, medium accuracy parallel type converters for use in aerospace systems.

Another example of current state-of-the-art technology that can be used to implement data systems in the near future is the family of ultra-high-speed analog-to-digital converters recently announced by TRW that employ LSI circuit technology. This family includes an 8-bit converter with a 50-nsec conversion time and a 10-bit converter with a 100-nsec conversion time.

TRW is also developing a 4-channel, 5-bit, accurate, 400-Msample/sec data system for the Air Force Avionics Laboratory. The system contains a parallel type analog-to-digital converter packaged as a single hybrid module that uses four 3-bit quantizer chips and an emitter-follower differential logic family that has gate delays of 250 to 350 psec per gate.

4 1.2.2 Trends in Unique/Dedicated Data Systems - The major current trend in unique/dedicated data systems is toward higher data rates. For example, the Landsat-D Thematic Mapper data rate will be almost six times the rate of the Landsat-C Multispectral Scanner. Other trends are the increased use of onboard processing to control selective sampling, control sensors, perform data compression, and provide real-time data analysis.

The technology currently exists to build data systems having 8-bit resolution with output data rates up to 1 Gbps. Current developments in LSI analog-to-digital converter technology, GaAs metal-semiconductor field-effect transistor logic technology, and short-channel NMOS technology for analog switches should make possible the construction of even much faster data systems by 1985. The main problem in building faster data systems is that ultra-high-rate space-to-ground data links do not currently exist, and none are planned that will accommodate in excess of 600 Mbps. It will therefore become necessary beyond Landsat-D for onboard data systems to include a significant amount of data processing to selectively sample and/or perform data compression.

Current trends related to unique/dedicated data systems technology are being driven by radar processing and electronic countermeasures applications. This includes both ultra-high-speed analog-to-digital conversion and onboard real-time processing. Several companies, including Harris, IBM, Motorola, TRW, and others, are developing high-rate data systems for radar processing. JPL has a 5-year program to develop a synthetic aperture radar (SAR) processor. Possible applications for the SAR processor include SEASAT-C, Spacelab, and Venus Orbiter.

Another trend is for the increased use of MOS/CMOS linear devices in future high-speed multiplexer and analog-to-digital converter applications as the performance and cost of these devices challenge their bipolar counterparts It has been known for many years that majority carrier devices (such as NMOS) should be faster than minority carrier devices (such as bipolar transistors) However, only recently have short-channel MOS devices that were faster than bipolar devices actually been fabricated.

4.1.2.3 Projected Developments in Unique/Dedicated Data Systems - The data system for the Thematic Mapper is probably the most advanced 8-bit data-handling system currently under development for advanced NASA program. Currently, NASA has no exploratory data system development work for data systems beyond Landsat-D. The Air Force system previously discussed in Subsection 4.1.2.1 represents the highest-data-rate (2 Gbps) system currently under development employing a single analog-to-digital converter. High-speed GaAs MESFET logic currently achieves 100-psec propagation delays in laboratory tests, and frequency dividers have been operated with actual counting rates of 4 GHz. Projections of current device technology trends to 1985 result in the high-rate unique/dedicated data system characteristics presented in Table 4.1.2.3-1.

TABLE 4.1.2.3-1. HIGH-RATE DATA SYSTEM TECHNOLOGY PROJECTIONS FOR 1985

Analog Multiplexer Switch	Short-channel NMOS
Analog Switching Speed	<400 psec
Analog-to-Digital Converter	All parallel for 4 to 8 bits Series-parallel for 8 to 12 bits
Conversion Speed	2 nsec for parallel converter 10 nsec for series-parallel converter
Serial Output Data Rate	To 5 Gbps
Ultra-High-Speed Logic	GaAs MESFET

4.1.3 High-Rate Digital Data Handling Systems (HRDDHS)

High-rate digital data handling has received considerable attention in recent years as the complexity and data speeds of airborne and spaceborne digital systems have increased and onboard spacecraft requirements have evolved for multiplexing, processing, correlating, compressing, interleaving, synchronizing, coding, and buffering of high-rate digital data.

One of the major problems in high-rate digital data handling is power consumption. One technique used to reduce power in aerospace data systems is to operate parallel subsystems constructed from components with lower speed-power products and combine these subsystems outputs using a minimum of high power logic to produce the high-speed system output. Another method for reducing power is to attack the basic physics of the power consumption problem, which is the amount of energy required to charge device capacitances The power can be reduced either by reducing voltage swings or device capacitances. Harris used custom-designed, large-scale ECL logic in MOMS to reduce both the internal logic voltage swings and also the intergate capacitances Typical speed-power products achieved were an order of magnitude less than MECL III for 200-MHz operation.

4.1.3.1 State of the Art in HRDDHS - Reported developments in high-rate digital data handling systems (particularly multiplexers) tend to cover two distinct categories of equipment

- The very-high-data-rate systems used by the military and built from custom-designed IC components
- The relatively high-data-rate (10- to 500-Mbps systems built from commercially available IC components.

A further distinction has to be made within each of the two categories to establish the difference between laboratory models of developed systems and production models, with particular emphasis on determining the applicability of production models for space applications, considering reliability, power consumption, size, weight, and similar factors.

Successful operation of digital multiplexers using custom-designed ICs has been reported (Ref. 4-2) to 1 Gbps as far back as 1972, and recent reports have discussed systems to 4 Gbps. The sensitive nature of the projects does not enable a determination as to the operational status of these systems for space applications, but it is evident that such systems use specially designed circuitry that is very expensive and not commercially available. The majority of work in this area has apparently taken place at Harris, Motorola, TRW Systems, and Dynatronics.

One example of a system utilizing custom-designed ICs is a high-rate digital multiplexer developed by TRW Systems for the Air Force Avionics Laboratory. The multiplexer has six input channels. Each channel multiplexes 8 bits of parallel data at a 20-MHz word rate. The system adds synchronization and converts the data to a 1-GHz serial data stream. The logic technology employed in the system is TRW's emitter-follower differential logic with oxide-lined transistors and junction isolation. Typical gate delays are 250 to 350 psec.

Subsection 9.1.1.2 reports on a 274-Mbps multiplexer (AT&T's D34 multiplexer) that has been in operation on a test basis between New

York City and Newark, New Jersey, since early 1975. The D34 system accepts three 44.736-Mbps pulse streams into each of two 137-Mbps multiplexers and interleaves the two 137-Mbps bit streams at the last instant to minimize the requirement for high-speed (≈1-nsec) logic. By definition, this system is a unique/dedicated system in lieu of a general-purpose system. Also, the system is not restricted in power consumption, weight, size, etc., as in a spaceborne system. However, as reported in Section 9, the same types of ICs were used in this system as in the system discussed below, which is being built for space data-handling purposes.

Systems being designed and/or tested for space application and which use commercially available components include a 200-Mbps simulator built by Martin Marietta in 1974 (Ref. 4-2). Work is being performed on a 500-Mbps system that uses faster components than were available when the 200-Mbps system was built.

The 200-Mbps system was designed with Motorola MECL 10,000 and MECL III components and was successfully operated at 230 Mbps under varying signal conditions. MECL III components were used where speed was a primary consideration and either MECL 10,000, TTL, or CMOS components were used where possible to minimize power consumption. The engineer responsible for the program was contacted to determine the power consumption and the feasibility of this high-data-rate system for space applications. The actual power consumption was not established, but the opinion was that the consumption of power was too high for space applications.

At the time the 200-Mbps system was built, the state of the art in available flip-flop components permitted a toggle rate to approximately 350 MHz using the Motorola MC 1670 flip-flop from the MECL III series. Presently, Fairchild semiconductors offer flip-flop components capable of toggle rates to approximately 720 MHz. Thus improvements in speed by a factor of two over previous systems are reasonable to expect

As stated earlier, there is still a significant distinction between what is available in the laboratory and what is feasible in terms of usable hardware for space applications where a major emphasis is placed on reliability, power consumption, size, environmental considerations, etc. The most advanced spacecraft development reported using commercially available components is a 50-Mbps general-purpose asynchronous multiplexer being developed for NASA by Martin Marietta. This system has 16 multiplexer inputs that will each accept up to 16 Mbps for a combined total system data rate of up to 48 Mbps. The system is coded in NRZ-L format with separate clock links to each input. The system is designed to use technology capable of being space-qualified; however, the system being delivered has not been subjected to a full qualification test.

Current designs for high-rate asynchronous data systems do not attempt to buffer blocks of data for formatting purposes. Data are output and multiplexed a word at a time in a manner similar to conventional data systems in the past. Fill bits are output when data are not available from asynchronous systems.

4.1 3.2 Trends in HRDDHS - A number of advances have occurred in high-rate digital data-handling systems, including both performance and cost. Although the advances have occurred primarily independent of the needs for space data-handling equipment, data rates from space in excess of a few tens of megabits would not have been feasible without these advances.

Increases in speed of integrated circuits, decreases in power consumption, and decreases in cost for complex chips can be expected to continue for the foreseeable future (Subsection 7.2.1), and the effects on space data handling systems will continue to be felt. However, there is a feeling on the part of some authorities that the emphasis is not sufficient to produce really significant advances in data-handling systems from commercially available components. Advances in custom-designed systems will continue, however, but the costs will be significant.

Newer systems will tend to be asynchronous and will use memories (possibly shift registers) that permit a wide flexibility in formatting data, controlling data rates, and prioritizing data, if the user elects to specify these functions.

Gallium Arsenide is currently emerging as the high-speed logic technology of the future. Tuyl and Liechti (Ref. 4-3) project high-power GaAs MESFET logic with propagation delays as low as 50 psec resulting in counting rates of .8 to 10 GHz. However, because of data link limitations, data systems employing these data rates probably will not be implemented by 1985 unless additional emphasis is put on optical data link developments

There appears to be a trend toward optical technologies for Earth-based telecommunications data handling. Several experts predict that optical technology will significantly impact high-rate data handling on spacecraft by 1985. This aspect of data handling should be investigated for space applications during follow-on phases of the program Subsection 9.1.1.2 discusses the impact of the technology for telecommunications.

4.1 3.3 Projected Developments in HRDDHS - The response from authorities and the results of in-house analysis indicate that progress in commercially available high-rate data handling systems will continue, but possibly at a somewhat slower rate than has occurred over the past 5 years. The lack of more rapid progress over the next decade is based on a lack of emphasis in the area more than on a slowdown in the supporting technologies. What will happen in high-cost militarized systems cannot be established because of security reasons.

Some authorities predict that the highest-rate space-qualified multiplexers that will be available as off-the-shelf components in the 1980-1985 timeframe will operate on the order of 100 to 125 Mbps. One company stated that they can build a 600-Mbps system today, but would not elaborate on the technology used. Motorola has been producing shift-registers in the MECL III series that operate in the 300-MHz range for the past 3 to 4 years. The device is based on circuitry with propagation delays on the order of 1 nsec. Subsection 7 2.1 reports the state of the art in ECL components as 0 5 nsec at present and projects improvements to approximately 0.2 nsec by 1980 and 0.1 nsec by 1985. As reported in Subsection 4.1.3.1, TRW is currently building custom logic with propagation delays as low as 0.25 nsec that operates at 1 GHz. The Air Force Avionics Laboratory projects (Ref. 4-4) that by 1981, reasonably complex GaAs ICs will be available to operate at 5 GHz, with power levels of 5 to 10 mW per gate. In view of these projections, development of a 600-Mbps data system in the immediate future appears feasible.

Reference 4-2 by John Goodwin emphasizes the importance of RF design techniques for these high bit rates. Others in the area also emphasize the same points. Thus for data rates beyond 500 MHz, attention must be given to such other aspects of the system design as low-capacity printed circuit board materials such as Teflon and R T. Duroid.

4.2 ANALOG DATA SYSTEMS

Analog data systems are discussed in terms of time-division-multiplexed (TDM) systems, frequency-division-multiplexed (FDM) systems, and hybrid systems that employ a combination of time and frequency multiplexing Except for instrumenting development vehicles to obtain vibration and acoustic data, analog data handling systems have been replaced almost completely by digital data systems

In general, other than minor packaging innovations, no major new developments have been made in analog data systems during the past 15 years. Since the state of the art in analog data systems is not changing as fast as it is for the digital data systems, this report emphasizes the digital system technology.

4.2.1 Frequency Division Multiplexing (FDM)

Most of the current FDM systems utilize IRIG-compatible FM subcarrier oscillators that are packaged as microminiature pluggable assemblies. The microminiature subcarrier oscillator package configuration that is most popular was first introduced by Vector (now Aydin Vector) in 1963 Several other companies, including Microcom and Omnitek, have developed somewhat smaller (submicrominiature) subcarrier oscillator designs The Omnitek series 30 subcarrier oscillators are packaged in a standard 14-pin integrated circuit DIP configuration. These units are mounted by soldering to a PC board rather than plugging into a socket.

Future analog channel bandwidths will be increased significantly by the latest change in the IRIG Standards that are scheduled to be published later this year The IRIG STD 106-77 expands the bandwidths of the baseband and increases the number and the bandwidth of the available channels. For example, the number of proportional channels will be increased from 21 to 25 and the highest center frequency changed from 165 kHz to 560 kHz.

4.2.2 Time Division Multiplexing (TMD)

Analog time-division multiplexing data systems used in the past have included pulse-amplitude modulation (PAM) and pulse-duration modulation (PDM) techniques. During the past 15 years, PAM systems have been replaced by PCM systems except for some small missile test applications that continue to use PAM. The IRIG STD 106-1975 deleted PDM because of a lack of usage. It is not anticipated that any spaceborne systems of the future will employ either PAM on PDM Technology projections are therefore not given for these types of data systems. The analog multiplexers used in the digital data systems are basically identical to the multiplexers used in the PAM. However, since practically all PAM systems in use conform to these IRIG standards, it is anticipated that technology advances will only be incorporated in these types of systems to reduce hardware costs

4.2.3 Hybrid Systems

Space data systems in the past have employed hybrid systems that included various combinations of frequency-division and time-division multiplexing in a single system. For example, one of the FM subcarrier channels on the Saturn V was modulated by a PAM time-division multiplexer.

It is not anticipated that hybrid PAM/FM analog systems will ever be employed in operational spaceborne systems; however, hybrid PCM/FM systems may be used in future booster/spacecraft test programs. The PCM/FM configuration would consist of an FDM system with one or more of the wideband FM channels modulated by a PCM wavetrain. The FM subcarrier channels would handle wideband (2-kHz) acoustic data, and the PCM system would handle low-frequency (50-Hz) vibration data. For this type of hybrid configuration, the technology discussions already presented in Subsections 4.1.1 and 4.2.1 apply.

REFERENCES - SECTION 4

4-1. W. T. Burton et al., "Multimegabit Operation Multiplexer System", Final Report, NASA Contract NAS5-21690, Harris, Electronics Systems Division, September 1973

4-2. J. E. Goodwin , "A 200 Megabit per Second Data Handling/Data Link Simulator", Proceedings of 1975 International Telemetering Conference, Volume XI, sponsored by International Telemetry Conference, pp. 102-111

4-3 C Liechti et al., "Gallium Arsenide Spawns Speed", IEEE Spectrum, pp. 41-47, March 1977

4-4. "Military Integrated Circuits-Microcircuits Status and Trends-Technology Trends", Countermeasures, pp. 44-46, 59-60, May 1977

4-5. B. Abrahamsen et al., "A 560 Mbit/s Digital Transmission System Over Coaxial Cable", Proceedings of 1976 International Zurich Seminar on Digital Communications, sponsored by IEEE, pp. A4.1-A4.6

4-6. H. I. Maunsell et al., "The M13 and M34 Digital Multiplexers", Proceedings of 1976 International Conference on Communications, sponsored by IEEE, pp. 48-5, 48-9

4-7. B. Elson, "Fiber Optics' Aerospace Role Studied", Aviation Week and Space Technology, pp. 56-57, February 9, 1976

5. SPACE-TO-GROUND COMMUNICATION ELEMENTS

Space-to-ground communication elements include the Level 2 hardware elements and signal design techniques illustrated in Figure 5-1 Discussions of state of the art, trends, and projected developments are presented in terms of these Level 2 elements. The major emphasis throughout the discussions is on digital communication links because the trends and the major developments in communication are toward digital links. Future reports will look at developments for handling analog data.

This section addresses relay satellites from the standpoint of relaying data from orbiting satellites to the Earth. Point-to-point transfer of data for telecommunications purposes on the Earth will be addressed in Section 9.2. Also, detection hardware and techniques have been arbitrarily placed in Section 6, where preprocessing elements are discussed.

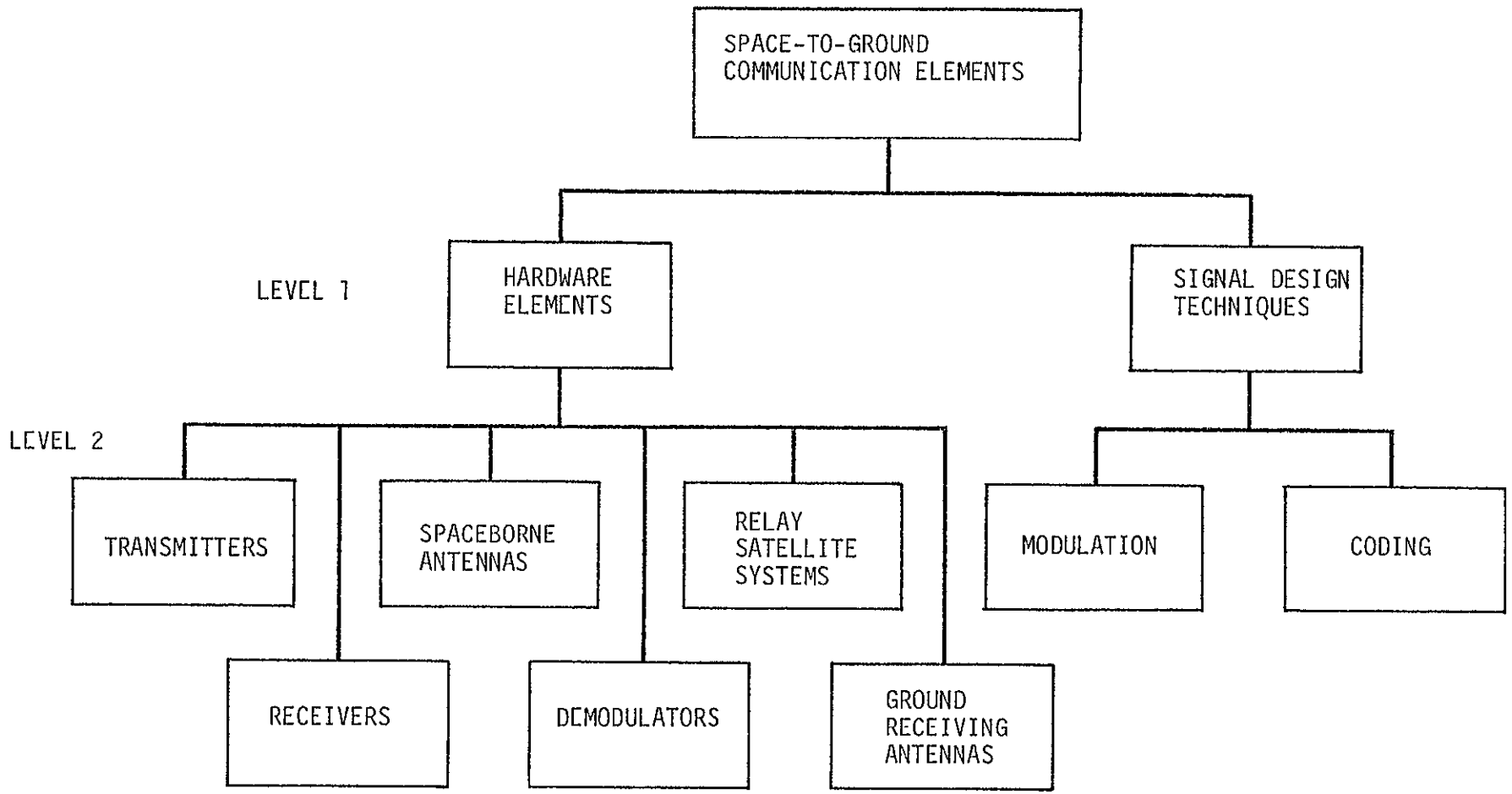

FIGURE 5-1. SPACE-TO-GROUND COMMUNICATION ELEMENTS

5.1 SPACEBORNE TRANSMITTERS

5.1.1 State of the Art in Spaceborne Transmitters

Spaceborne transmitter frequency ranges and characteristics of interest are shown in Figure 5.1.1-1 for clarification. The characteristics of most interest are power, efficiency, and gain, especially in the area of solid-state devices

5 1.1.1 Solid-State Devices - Tables 5.1.1.1-1 through 5.1.1.1-5 (Ref. 5-1) list the current state-of-the art specifications for various solid-state devices, some of which are in production and some of which have been achieved only in the laboratory. Figures 5 1 1.1-1 through 5.1.1.1-3 present profiles of power efficiency, and gain as functions of frequency for state-of-the art devices. Projected profiles for the 1980-1985 timeframe are also presented in this figure for comparison.

The major developments in the 1976-1977 period are those in the gallium arsenide (GaAs) FETs. The efficiencies of the lower frequency devices shown in Table 5.1.1.1-1 should be noted, particularly RCA's 4-GHz, 68% efficient GaAs FET. GaAs FETs are high-efficiency, high-gain, medium-power devices that are approaching the effectiveness of bipolar devices in the 4-GHz frequency range. The advantages of GaAs FETs are even more pronounced in the 6- to 13-GHz range. Above this point, IMPATT diodes promise high power, reasonable gain, and reasonable efficiency.

5.1.1.2 Microwave Tubes - Traveling Wave Tubes (TWTs) have undergone significant improvements in efficiency in the 11- to 12-GHz and 14-GHz satellite communication bands. The SATCOM 12-GHz, 50% efficient, 200-W TWT developed by NASA is the basis for NASA's development on 100- and 200-W TWTs for operation on the 41- to 43-GHz and 84- to 86-GHz bands for space-qualified operation. Efficiencies of 25 to 30% in TWTs are achieved now in satellite TWTs in the 10- to 12-GHz band. The European Space Research Organization (ESRO) TWT (TH3525), operating at 10.95 to 11 7 GHz, has 40% efficiency at a 20-W, 60-dB gain.

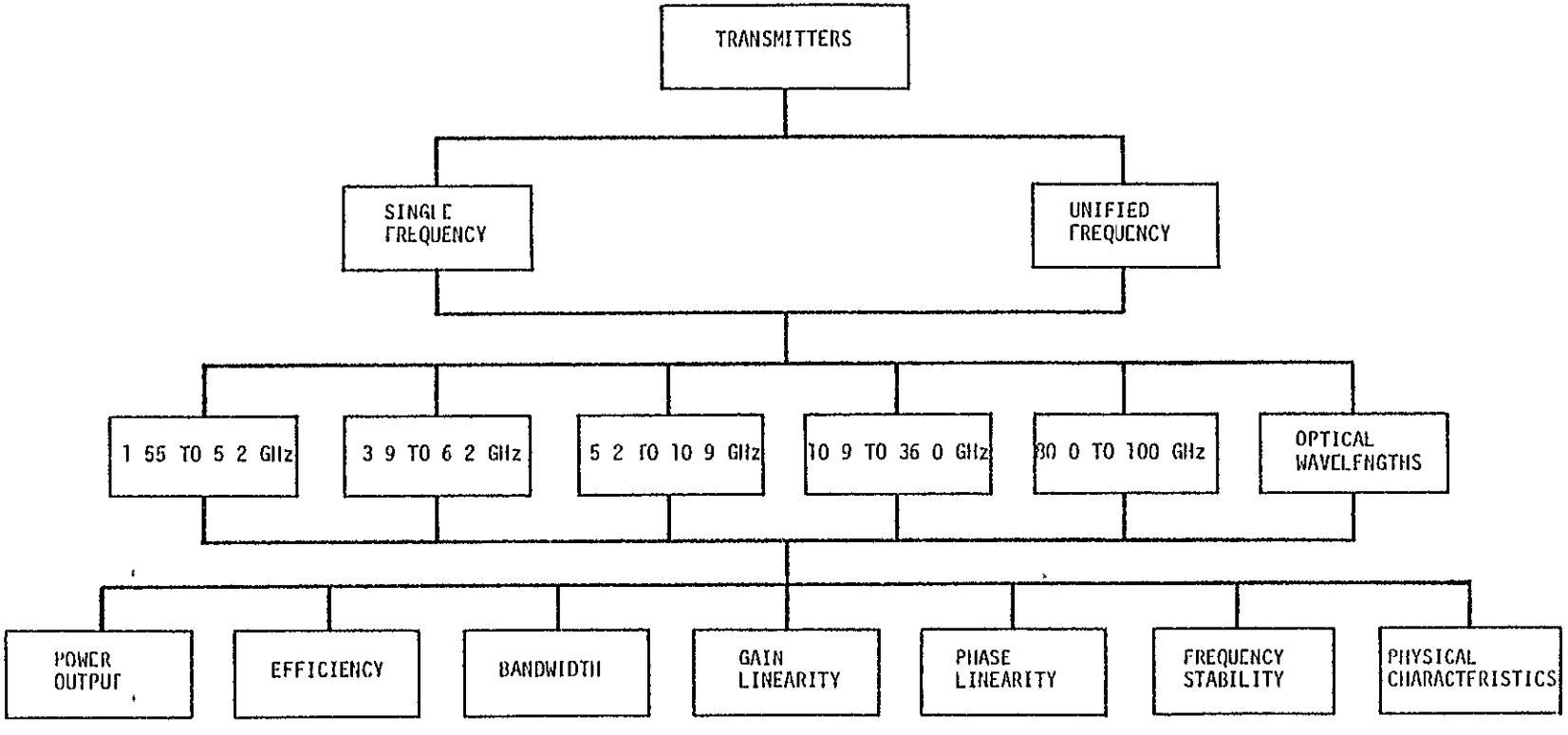

FIGURE 5.1 1-1. SPACEBORNE TRANSMITTER PARAMETERS

TABLE 5 1 1 1-1 STATE OF THE ART IN FET DEVICES

FREQUENCY (GHz)	POWER (W)	POWER GAIN (dB)	EFFICIENCY (%)	MATERIAL	SOURCE
4	0 26	9.6	68	GaAs	RCA
4	3	6	47	GaAs	Fujitsu
5	0.25	12	22	GaAs	Plessey
6	2.4	5	34	GaAs	Fujitsu
8	-	20	-	GaAs	Plessey
8	4.1	4	31	GaAs	Texas Instruments
8 to 10	0.7	6	46	GaAs	Texas Instruments
10	-	10	-	GaAs	Plessey
12	0.5	6	15	GaAs	RCA
15	0.45	5	12.5	GaAs	RCA
22	0.14	4.8	9	GaAs	RCA
47	0.1	-	2 2	InP	Plessey

TABLE 5.1.1.1-2 STATE OF THE ART IN BIPOLAR DEVICES

FREQUENCY (GHz)	POWER (W)	POWER GAIN (dB)	EFFICIENCY (%)	SOURCE
1	40	9	65	Typical
2	24	7	45	Typical
2	40	8	50	TRW
3	8	7	45	Typical
4	7	-	-	Texas Instruments
6	1.5	4	36	Hewlett-Packard
8	1.5	-	-	Texas Instruments
10	1	4.5	20	Texas Instruments

TABLE 5.1 1.1-3. STATE OF THE ART IN 3- TO 4-GHz MICROWAVE POWER DEVICES

DEVICE	PEAK P_o (W)	PW (usec)	DUTY CYCLE (%)	1 dB BW (%)	POWER GAIN (dB)	EFFICIENCY (%)	SOURCE
TRAPATTS	240*	0 2	0 1	8 3	4 8	29	Hughes
	195	Narrow	-	Narrow	6 3	20	RCA
	98	0 2	0 1	8 3	6	30	Hughes
	82	10	?	8	4 9	15	RCA
	55	50	1	5	5	24	Hughes/NRL
	45	50	0 001	10	7	21	Sperry
	3	CW	100	Oscillator	-	20	BTL
IMPATTS	21 (3 diodes)	CW	100	Narrow	Locked Oscillator Locking Power = 3 5 W	12 to 13	BTL
	12 1	CW	100	Oscillator	-	21	Lincoln Laboratories
	3 4	CW	100	Oscillator	-	37	Lincoln Laboratories

*Two devices hybrid combined

TABLE 5.1.1.1-4. STATE OF THE ART IN 8- TO 10-GHz MICROWAVE POWER DEVICES

DEVICE	MATERIAL AND TUBE DEVICE	PEAK P_o (W)	PW (µsec)	DUTY CYCLE (%)	BW (%)	POWER GAIN (dB)	EFFICIENCY (%)	SOURCE
TRAPATTS		27	1	0 1	Oscillator	-	42 5	Hugnes
		10	0 25	0 1	10	6	12	Sperry
		6	CW	100	Oscillator	-	24	Hughes
		5	CW	100	5 5	5	16 4	Hughes
IMPATTS	SiDD	16	0 8	25	Oscillator	-	12 3	Hewlett-Packard
	GaAs HI-LO	12 8	0 8	25	Oscillator	-	25	Varian
	GaAs SB Read	8	CW	100	Oscillator	-	35	Raytheon
	GaAs Flat Profile	5	CW	100	7	25 (4 Stages)	10	Typical
	CaAs SB Read	4 5	CW	100	6 5	4 5	22	Raytheon
	GaAs HI-LO	2 9	CW	100	Oscillator	-	18 8	Varian

TABLE 5 1 1 1-5. STATE OF THE ART IN IMPATT DEVICES ABOVE 12 GHz

MATERIAL	TYPE*	FREQUENCY (GHz)	PEAK P_o (W)	PW (μsec)	BW (%)	POWER GAIN (dB)	EFFICIENCY (%)	SOURCE
Silicon	DD	16 5	11 0	0 8	Oscillator	-	14	Hewlett-Packard
	DD	29 39	1 2	CW	Oscillator	-	10	Hughes
	DD	39	11 0	0 35	Oscillator	-	10	Hughes
	DD	55	1 6	CW	Oscillator	-	11 5	Fujitsu
	DD	60	1 0	CW	Up to 6 GHz	9 (2 Stages)	2	Hughes
	DD	66	0 7	CW	Oscillator	-	6	Hughes
	DD	92	0 38	CW	Oscillator	-	12 5	BTI
	SD	94	0 1	CW	2 GHz	4	2	Hughes
	DD	140	0 72	0 3	Oscillator	-	4	Hughes
	DD	170	0 03	CW	Oscillator	-	2	Hughes
	SD	185	0 08	CW	Oscillator	-	2 3	Nippon T&T
	SD	202	0 05	CW	Oscillator	-	1 3	Nippon T&T
	DD	212	0 209	0 05	Oscillator	-	1 5	Hughes
	SD	285	0 008	CW	Oscillator	-	0 35	Nippon T&T
	SD	301	0 0012	CW	Oscillator	-	-	Nippon T&T
GaAs	SB Read	13 7	3 2	CW	Oscillator	-	24	Raytheon
	DD	21	1 2	CW	Oscillator	-	15 6	Hitachi
	SD	34 8	0 7	CW	Oscillator	-	12 4	RCA
	SD Ion Imp	37.5	0 5	CW	Oscillator	-	9 6	Lincoln Laboratories
	SB	51	0 2	CW	Oscillator	-	11 0	Hitachi
	SB	53	0 4	CW	Oscillator	-	5 2	Hitachi

*DD - Double Drift, SD - Single Drift, SB - Schottky Barrier

Helix-type TWTs are being used in the 35- to 45-GHz range. Watkins-Johnson has achieved 20% efficiency at 12 W, 35 to 40 GHz, with a gain of 28 $\pm$1 dB in their high-CW-power-level TWT designed for satellite and airborne communications.

Crossed-field tubes are very efficient (80%) at low frequencies (2 to 6 GHz) and high power (hundreds of watts at 6 GHz), but excess noise plagues them. They provide efficient Earth-terminal transmitters but are limited in usefulness in satellite transmission.

TWTs are undergoing significant improvement in efficiency and size for the 5- to 200-W power range. Their main advantage over solid-state devices is higher efficiency (40 to 50%) in the lower frequency ranges (up to 12 GHz). Recent work (Ref. 5-2) shows that 50% efficiency may be common shortly after 1980, with up to 84% efficiency possible in four-stage designs.

A summary of the key characteristics for state-of-the-art TWTs and solid-state devices is presented in Tables 5.1.1.2-1 through 5.1.1.2-4. The summary information is extracted from Tables 5.1.1.1-1 through 5.1.1.1-5.

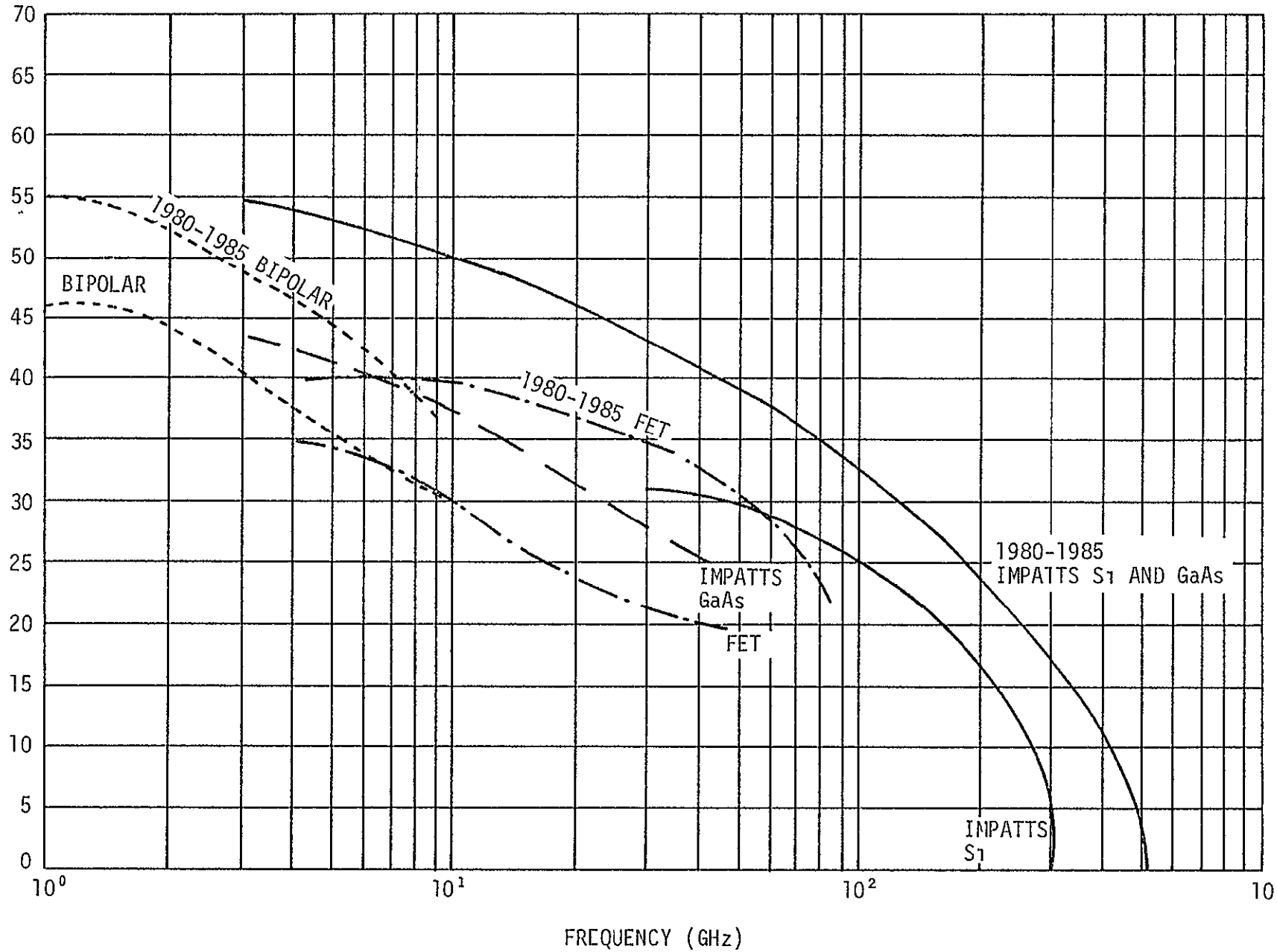

FIGURE 5.1.1 1-1. POWER AS A FUNCTION OF FREQUENCY FOR SOLID-STATE DEVICES

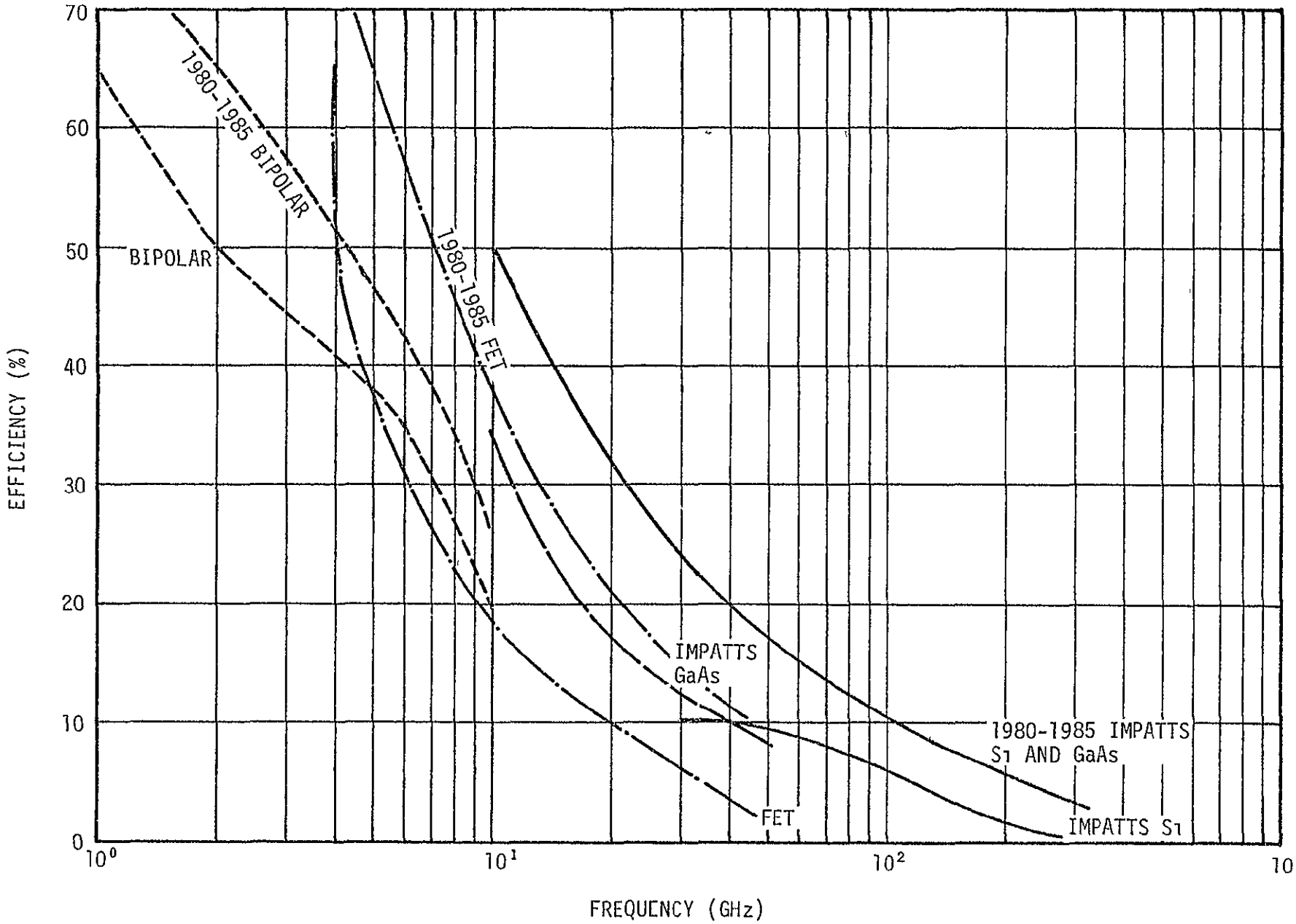

FIGURE 5 1.1.1-2. EFFICIENCY AS A FUNCTION OF FREQUENCY FOR SOLID-STATE DEVICES

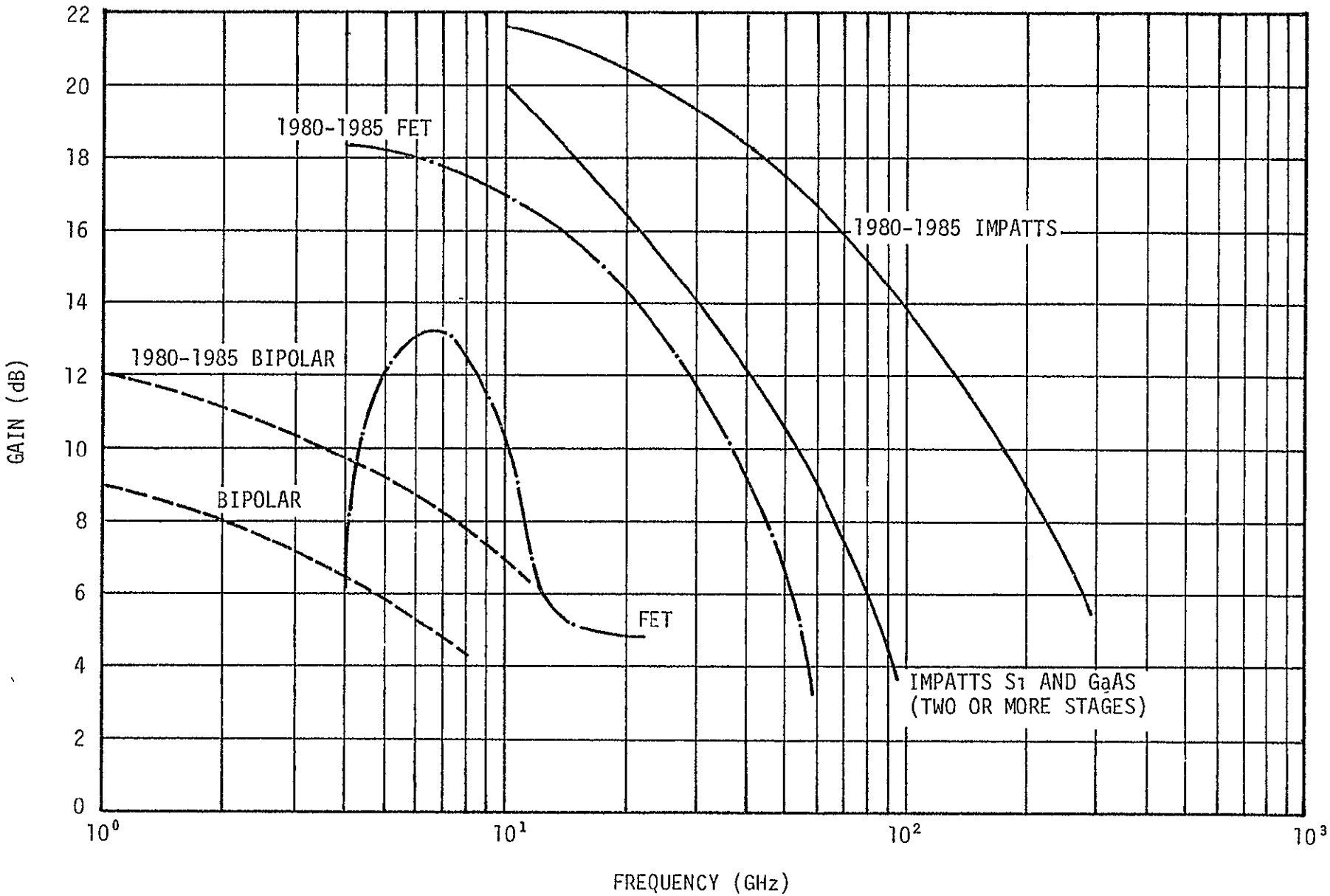

FIGURE 5.1.1.1-3. GAIN AS A FUNCTION OF FREQUENCY FOR SOLID-STATE DEVICES

TABLE 5.1.1.2-1 SUMMARY OF KEY CHARACTERISTICS FOR STATE-OF-THE-ART TWTs

CHARACTERISTIC	FREQUENCY (GHz)				
	1 TO 4	4 TO 6	6 TO 10	10 TO 40	40 TO 100
Power Output (W)	50	100	100	20	8
Gain (dB)	55	40	40	50	20
Efficiency (%)	80	75	65	50	45
Relative Size (%)	100	100	100	100	100
Relative Cost (%)	100	100	100	100	100

TABLE 5.1.1.2-2 SUMMARY OF KEY CHARACTERISTICS FOR STATE-OF-THE-ART BIPOLAR TRANSISTORS

CHARACTERISTIC	FREQUENCY (GHz)		
	1 TO 4	4 TO 6	6 TO 10
Power Output (W)	40	7	1 5
Gain (dB)	9	6.5	5.5
Efficiency (%)	65	40	35
Relative Size (%)	100	100	100
Relative Cost (%)	100	100	100

TABLE 5.1.1 2-3 SUMMARY OF KEY CHARACTERISTICS FOR STATE-OF-THE-ART GaAs FET DEVICES

CHARACTERISTIC	FREQUENCY (GHz)			
	4 TO 6	6 TO 10	10 TO 40	40 TO 100
Power Output (W)	3	1.5	1	0.1
Gain (dB)	13	13	10	2
Efficiency (%)	65	30	18	1
Relative Size (%)	100	100	100	100
Relative Cost (%)	100	100	100	100

TABLE 5.1.1 2-4 1977 STATE-OF-THE-ART FOR IMPATT DEVICES

CHARACTERISTIC	FREQUENCY (GHz)		
	6 TO 10	10 TO 40	40 TO 100
Power Output (W)	10	5	1
Gain (dB)	22	20	12
Efficiency (%)	40	30	10
Relative Size (%)	100	100	100
Relative Cost (%)	100	100	100

5 1 2 Trends and Projected Developments in Spaceborne Transmitters

Improvements in substrate technology are enabling higher power outputs in FETs and IMPATTs, and at the same time are providing a fair gain of efficiency also. Reproducible high-quality devices operating with state-of-the-art specifications are being pursued by all major manufacturers. As in the past, the trend is for smaller package size, which should be about 70 to 75% of present size by 1980 and 45 to 55% in 1985. Efficiency should increase significantly by 1980 to 1985, approaching 80% in FETs. Figure 5.1.1.1-2 depicted the projected improvements in efficiency as a function of frequency for the 1980 to 1985 timeframe.

Transmitters will be using a variety of devices for different frequency bands. Below 6 GHz, bipolar devices will be competing against TWTs for size, power, and efficiency Power and efficiency projections for solid-state devices for 1980 to 1985 are shown in Figures 5 1.1.1-1 and 5.1.1.1-2, respectively Gain projections are shown in Figure 5.1.1.1-3. FETs should be equal to the IMPATTs of today by 1980 to 1985, i.e., 6 to 50 GHz, whereas IMPATTs should improve in power, and mainly efficiency, to about 1 W at 100 GHz

The advancement of these various devices depends on the demand and the research and development money that is funneled into these areas. The higher frequencies (30+ GHz) and the optical wavelengths are being pursued more deeply than some of the intermediate areas because of the allotment of higher frequencies to spacecraft communication. Any improvements in hardware at these frequencies should influence the performance of lower-frequency devices also.

Projected trends in available transmitter power at different frequencies are shown in Figures 5.1.2-1 through 5.1.2-4; trends in available transmitter gains at the same frequencies are shown in Figures 5.1.2-5 through 5.1.2-8; trends in transmitter efficiency are shown in Figures 5.1.2-9 through 5.1 2-12, trends in transmitter size are shown in Figures 5.1.2-13 through 5.1.2-15, and trends in transmitter cost are shown in Figures 5.1.2-16 through 5.1.2-18.

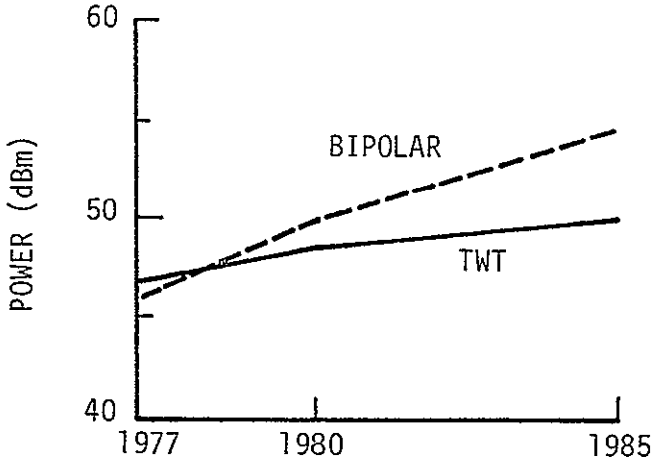

FIGURE 5.1.2-1. TRENDS IN 1- TO 4-GHz TRANSMITTER POWER

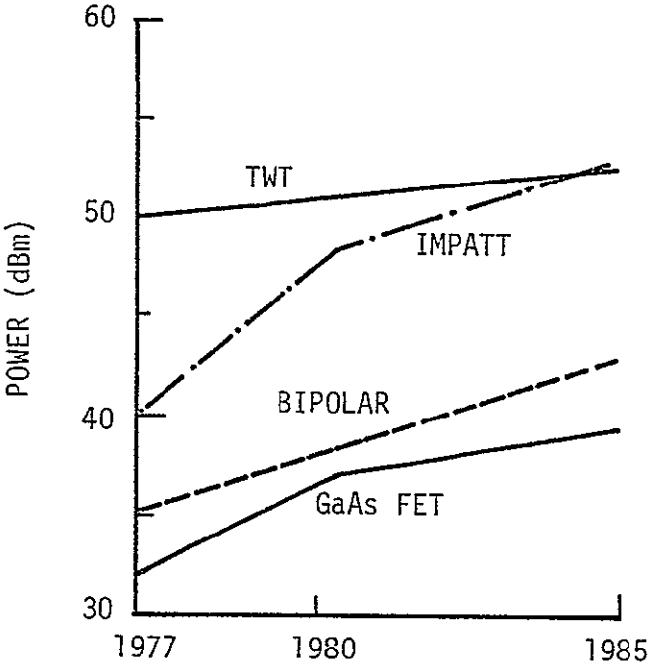

FIGURE 5.1 2-2. TRENDS IN 6- TO 10-GHz TRANSMITTER POWER

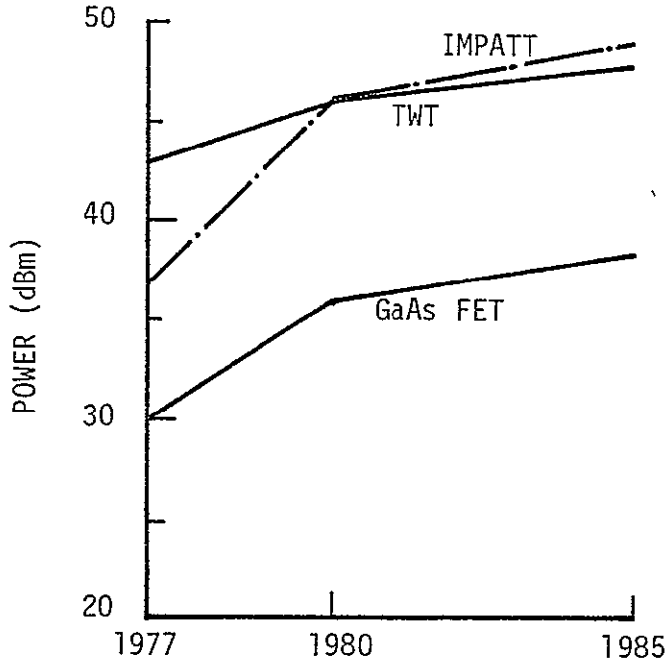

FIGURE 5.1.2-3. TRENDS IN 10- TO 40-GHz TRANSMITTER POWER

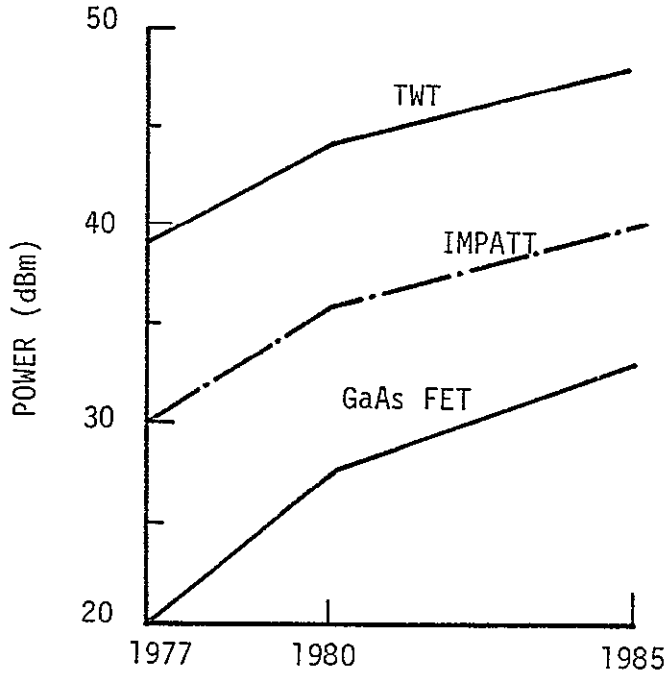

FIGURE 5.1.2-4. TRENDS IN 40- TO 100-GHz TRANSMITTER POWER

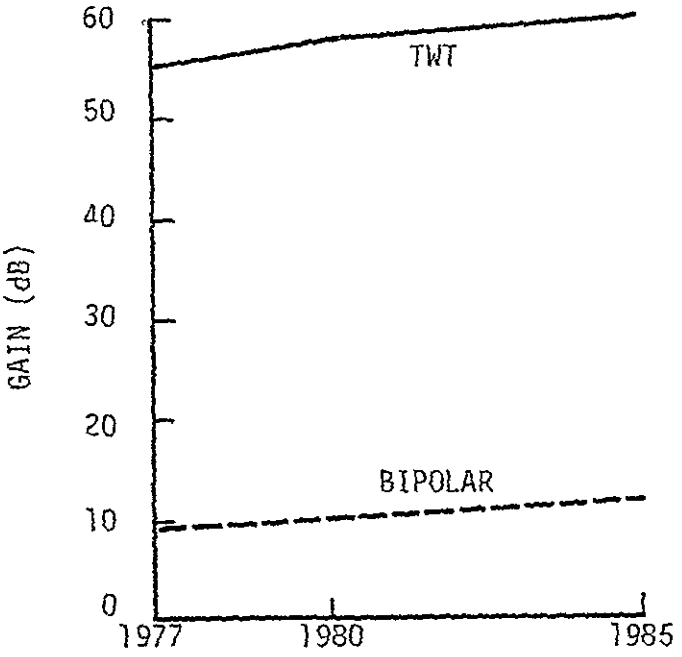

FIGURE 5.1.2-5. TRENDS IN 1- TO 4-GHz TRANSMITTER GAIN

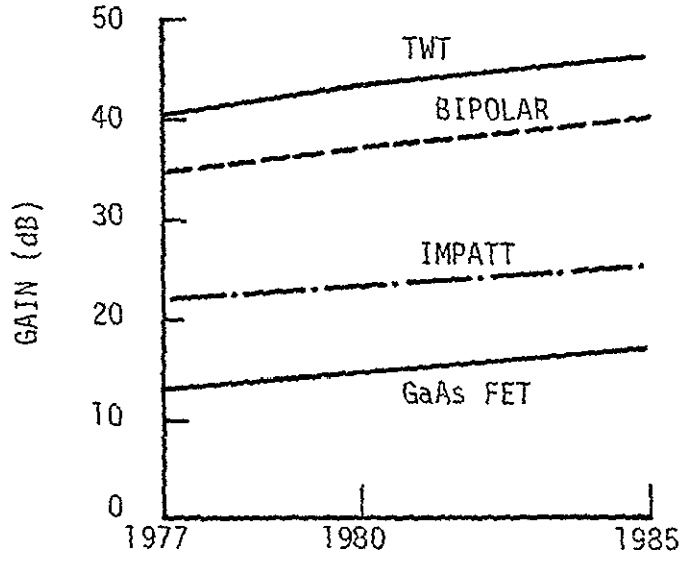

FIGURE 5.1.2-6. TRENDS IN 6- TO 10-GHz TRANSMITTER GAIN

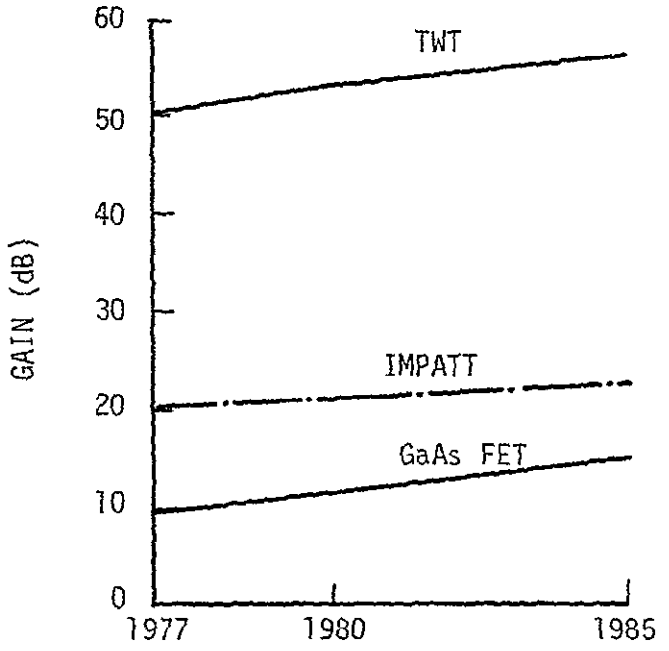

FIGURE 5 1.2-7. TRENDS IN 10- TO 40-GHz TRANSMITTER GAIN

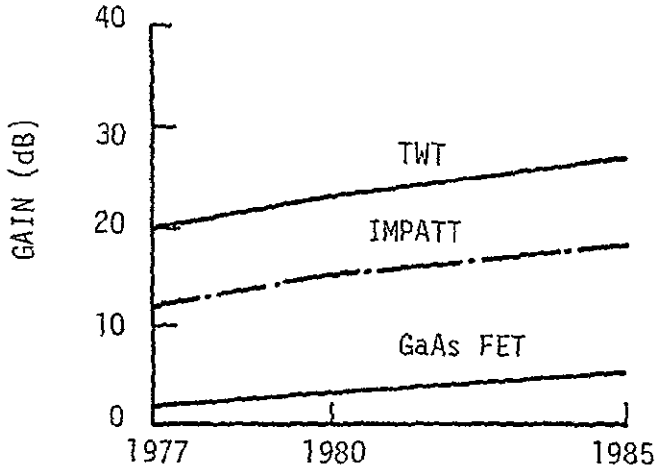

FIGURE 5.1.2-8 TRENDS in 40- TO 100-GHz TRANSMITTER GAIN

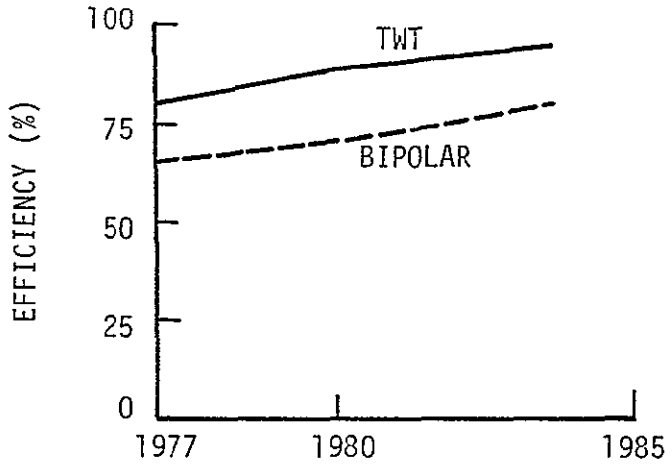

FIGURE 5.1.2-9. TRENDS IN 1- TO 4-GHz TRANSMITTER EFFICIENCY

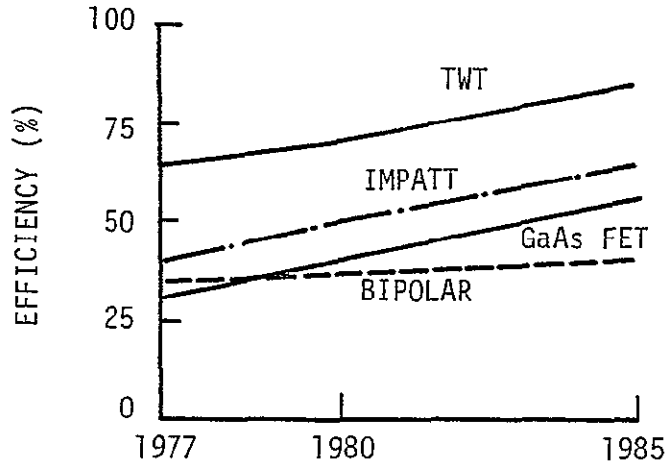

FIGURE 5.1.2-10. TRENDS IN 6- TO 10-GHz TRANSMITTER EFFICIENCY

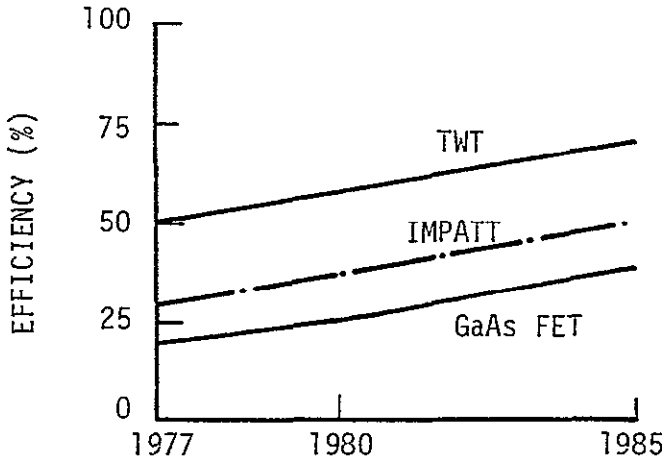

FIGURE 5.1.2-11. TRENDS IN 10- TO 40-GHz TRANSMITTER EFFICIENCY

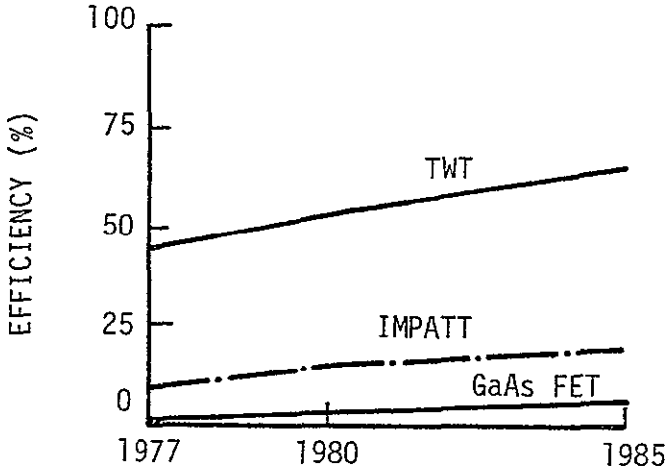

FIGURE 5.1.2-12. TRENDS IN 40- TO 100-GHz TRANSMITTER EFFICIENCY

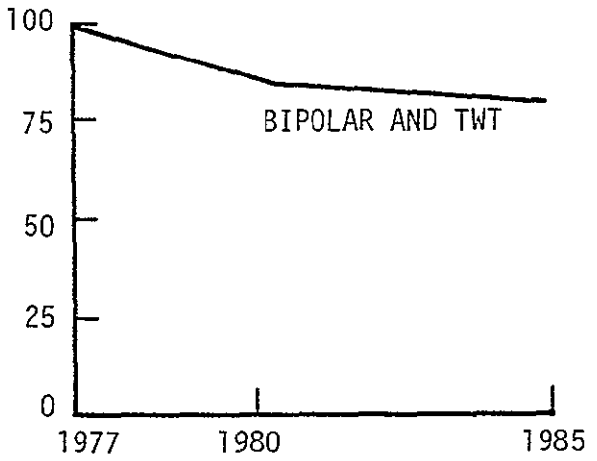

FIGURE 5.1.2-13. TRENDS IN 1- TO 4-GHz TRANSMITTER SIZE

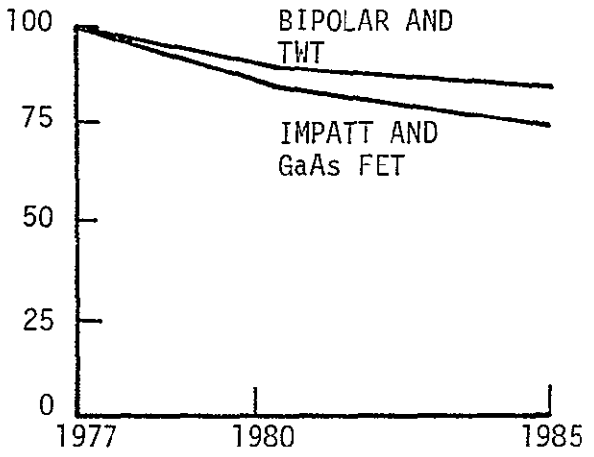

FIGURE 5.1.2-14. TRENDS IN A 6- TO 10-GHz TRANSMITTER SIZE

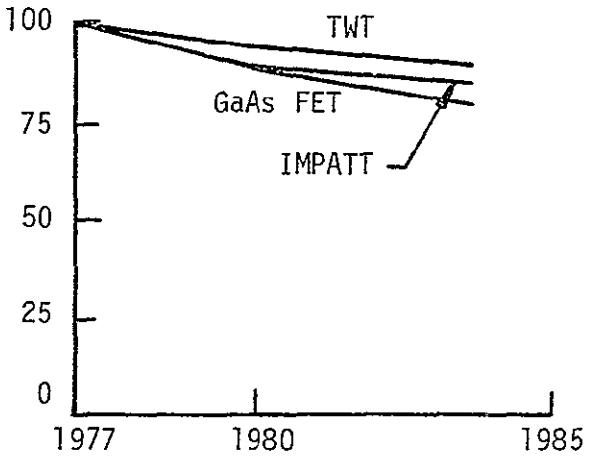

FIGURE 5.1.2-15. TRENDS IN 40- TO 100-GHz TRANSMITTER SIZE

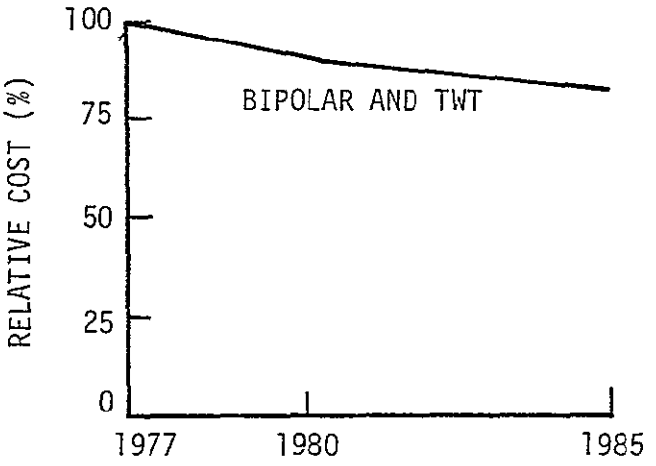

FIGURE 5.1 2-16. TRENDS IN 1- TO 4-GHz TRANSMITTER RELATIVE COST

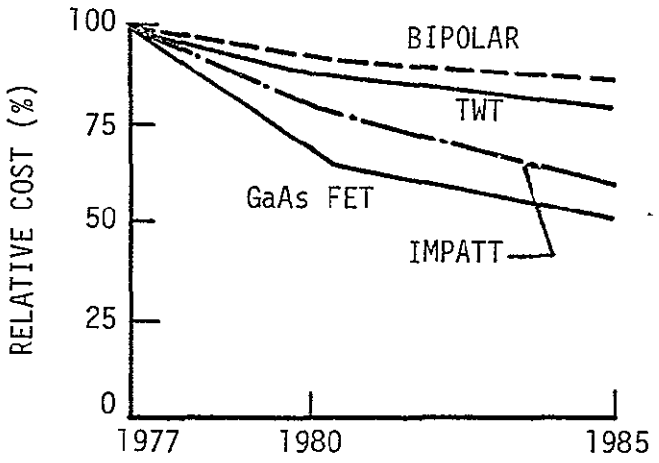

FIGURE 5.1.2-17. TRENDS IN 6- TO 10-GHz TRANSMITTER RELATIVE COST

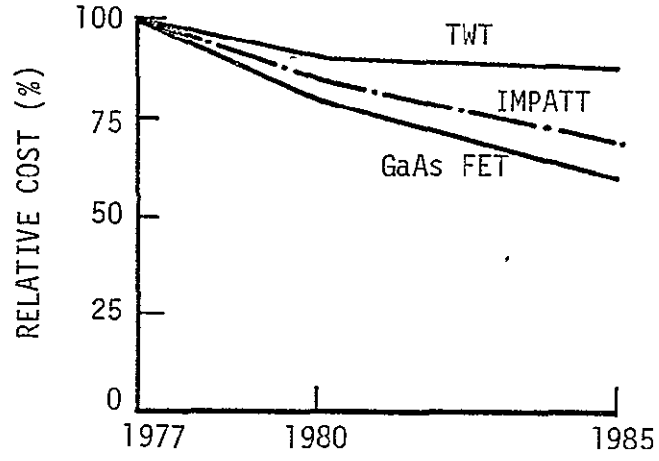

FIGURE 5 1.2-18. TRENDS IN 40- TO 100-GHz TRANSMITTER RELATIVE COST

Projections of key characteristics for TWT and solid-state transmitter devices are presented in Tables 5 1.2-1 through 5.1.2-4 Similar projections for the 1985 timeframe are presented in Tables 5 1.2.5 through 5.1.2-8.

TABLE 5 1.2-1. PROJECTIONS OF KEY CHARACTERISTICS FOR TWTs IN 1980

CHARACTERISTIC	FREQUENCY (GHz)				
	1 TO 4	4 TO 6	6 TO 10	10 TO 40	40 TO 100
Power Output (W)	70	120	130	40	25
Gain (dB)	58	43	43	53	23
Efficiency (%)	85	80	70	58	55
Relative Size (%)	-85	87	90	93	95
Relative Cost (%)	90	88	88	90	90

TABLE 5.1.2-2 PROJECTIONS OF KEY CHARACTERISTICS FOR BIPOLAR TRANSISTORS IN 1980

CHARACTERISTIC	FREQUENCY (GHz)		
	1 TO 4	4 TO 6	6 TO 10
Power Output (W)	110	20	7
Gain (dB)	10	7.5	6.5
Efficiency (%)	70	45	37
Relative Size (%)	87	88	89
Relative Cost (%)	89	91	93

TABLE 5 1.2-3. PROJECTIONS OF KEY CHARACTERISTICS FOR GaAs FET DEVICES IN 1980

CHARACTERISTIC	FREQUENCY (GHz)			
	4 TO 6	6 TO 10	10 TO 40	40 TO 100
Power Output (W)	6	5	4	0.7
Gain (dB)	15	14	12	3
Efficiency	70	40	25	2 5
Relative Size (%)	80	84	86	90
Relative Cost (%)	60	65	75	80

TABLE 5 1.2-4 PROJECTIONS OF KEY CHARACTERISTICS FOR IMPATT DEVICES IN 1980

CHARACTERISTIC	FREQUENCY (GHz)		
	6 TO 10	10 TO 40	40 TO 100
Power Output (W)	70	40	4
Gain (dB)	23	21	15
Efficiency (%)	50	35	15
Relative Size (%)	85	87	90
Relative Cost (%)	80	82	85

TABLE 5.1.2-5. PROJECTIONS OF KEY CHARACTERISTICS FOR TWTs IN 1985

CHARACTERISTIC	FREQUENCY (GHz)				
	1 TO 4	4 TO 6	6 TO 10	10 TO 40	40 TO 100
Power Output (W)	100	150	170	80	60
Gain (dB)	61	46	46	56	27
Efficiency (%)	90	87	85	70	65
Relative Size (%)	80	82	85	88	90
Relative Cost (%)	85	80	80	85	87

TABLE 5.1.2-6. PROJECTIONS OF KEY CHARACTERISTICS FOR BIPOLAR TRANSISTORS IN 1985

CHARACTERISTIC	FREQUENCY (GHz)		
	1 TO 4	4 TO 6	6 TO 10
Power Output (W)	290	40	20
Gain (dB)	12	9.5	8.5
Efficiency (%)	80	50	40
Relative Size (%)	80	83	83
Relative Cost (%)	82	84	87

TABLE 5.1.2-7. PROJECTIONS OF KEY CHARACTERISTICS FOR GaAs FET DEVICES IN 1985

CHARACTERISTIC	FREQUENCY (GHz)			
	4 TO 6	6 TO 10	10 TO 40	40 TO 100
Power Output (W)	10	9	7	2
Gain (dB)	19	17	15	5
Efficiency (%)	80	55	38	6
Relative Size (%)	70	73	77	80
Relative Cost (%)	50	52	57	60

TABLE 5.1.2-8. PROJECTIONS OF KEY CHARACTERISTICS FOR IMPATT DEVICES IN 1985

CHARACTERISTIC	FREQUENCY (GHz)		
	6 TO 10	10 TO 40	40 TO 100
Power Output (W)	190	90	10
Gain (dB)	25	22	18
Efficiency (%)	65	50	20
Relative Size (%)	75	80	85
Relative Cost (%)	60	65	70

5.2 SPACEBORNE ANTENNAS

5.2.1 State of the Art in Spaceborne Antennas

Most of the current spaceborne antennas operate at S-band with a few at UHF, L, and C bands. With few exceptions, the downlink data rate is modest (50 kbps or less) so that high-gain antennas are not required. These needs are met with helical, conical, cavity-backed, and reflector type antennas. A very common type is the S-band conical antenna, which is physically small, is easily deployable when necessary, has 0-dB gain, and is fairly isotropic in its pattern. Phased-array and multiple-feed reflector antennas are still in the development stage.

The Airborne Electronically Steerable Phased Array (AESPA) program conducted by Marshall Space Flight Center has resulted in an S-band antenna system 22 in. in diameter weighing 38 lb. The details of this antenna are contained in Table 5.2.1-1. An X-band steerable array was built recently for the Air Force, but information on the characteristics and performance capabilities is unavailable at this time. These units represent the state of the art in airborne phased-array antennas that have been built and tested. However, new device technology would probably enable as much as a 50% reduction in power consumption, but rejection of dissipated energy within the array would still be a problem.

TABLE 5.2.1-1. S-BAND PHASED-ARRAY CHARACTERISTICS*

Coverage	Conical, ±60 deg from boresight
3 dB Beam Width (deg)	16
Overall Size (in)	22 diameter by 4
Number of Elements	48
Polarization	RHCP
Weight (lb)	38.5
dc Power (W)	220
Transmitting Characteristics	
Frequency (MHz)	2,252 to 2,312
Gain (boresight) (dB)	31 8
Gain Loss at 60-deg Scan (dB)	4 4
RF Drive Required (W)	2.5
EIRP (dBW)	35.8
Scan Angle (deg)	Sidelobe Level (dB)
0	-16
20	-11
40	-13
60	-8
Receiving Characteristics	
Frequency (MHz)	2,071 to 2,131
Gain (Boresight) (dB)	31.3
Gain Loss at 60-deg Scan (dB)	4 0
Noise Figure (dB)	5 6
Scan Angle (deg)	Sidelobe Level (dB)
0	-15
20	-14
40	-12
60	-11

*This antenna system was developed under NASA's Airborne Electronically Steerable Phased Array (AESPA) program.

5 2.2 Trends in Spaceborne Antennas

In the past, data from low-Earth-orbiting unmanned spacecraft were transmitted directly to ground stations using low-gain, omnidirectional, helical or conical antennas. Depending on the mission, the satellite attitude was the major determinant of the location and number of antennas. Also, data rates were low (50 kbps or less) by today's standards, and with relatively short propagation distances to the ground stations, high EIRPs were not required. The requirements on low-Earth-orbiting spacecraft will change significantly by 1980. Operation of the TDRSS and the closing of all but three STDN ground stations will force spacecraft to relay data to the Earth via geosynchronous satellites. As a result, high-gain tracking antenna systems will be required. In some cases, depending on the mission attitude requirements, more than one antenna system will be required. Data from future low-Earth-orbiting missions will fall into two categories. low data rates (50 kbps or less) and high data rates (multi-megabit rates for imaging data). The low data rates will be handled by the multiple access (MA) service of the TDRSS, and the high data rate will be handled by the Ku-band single access (KSA) service of the TDRSS or by stations compatible with the TDRSS KSA service. Reflector type antennas for frequencies up to 6 GHz will be deployable and in many cases collapsible. Also in this frequency range, phased arrays will become more and more prevalent as the state of the art advances in microminiaturization. Switchable beam and multi-beam antennas will see increasing use. New materials will allow the reduction in weight of many antenna designs. Continuing improvements in feed systems will improve antenna performance in gain and sidelobe reduction.

5.2.3 Projected Developments in Spaceborne Antennas

Reflector type antennas will be prevalent in all bands through 1985. Tracking systems will be used with them (as for TDRSS use). They will be folding types below 10 GHz and will be deployed at all frequencies. Prime focus and offset reflectors with cluster array feeds will be common. Phased-array antenna systems will become competitive with reflector types in performance, weight, and volume. However, they will be more expensive by a factor of 1.5 or 2. Arrays will handle much higher power without experiencing multipactor. Array feeds of low-loss air-stripline or microstrip networks using high permittivity substrates will allow designs with sidelobes that are down more than 30 dB.

5.3 RELAY SATELLITE TECHNOLOGY FOR SPACE DATA TRANSFER

Relay satellite technology for point-to-point and multipoint transfer of data is addressed in Section 9.2 Transmitter, receiver, and antenna technologies for low-Earth-orbiting spacecraft and geosynchronous relay satellites are covered elsewhere in Section 5 In view of this, this subsection addresses the technology/capability for relaying data from an orbiting spacecraft to the Earth by means of a relay satellite and is more capability oriented than technology oriented. The capability is presented in terms of the orbiting spacecrafts' data throughput as a function of EIRP and other factors such as coding, single access by the spacecraft, and shared or multiple access with other users.

5.3.1 State of the Art in Space Data Transfer via Relay Satellite

Relay satellites capable of transferring wideband data from orbiting spacecraft on an operational basis are not currently available for use by civilian spacecraft. The Tracking and Data Relay Satellite System (TDRSS) is currently under development for this purpose and is scheduled to be launched on January 1, 1980. The operational date for the satellite is June 1, 1980, when all Space Tracking Data Network (STDN) stations will be closed down except for two or three stations that will remain with the capability for handling low-rate data.

The TDRSS network (to be provided by Western Union) will consist of two geostationary satellites located over the equator at approximately 41° and 171°W longitude and one Earth station located in the continental United States in New Mexico. The satellites are positioned so as to permit direct contact with low-Earth-orbiting satellites for approximately 85% of the time. The coverage exclusion zone, centered over the Indian Ocean, is a function of the user spacecraft orbit inclination and altitude. For example, an orbital altitude of 200 km permits coverage for at least 85% of the time.

TDRSS capabilities are covered in a number of documents, including a document entitled "Tracking and Data Relay Satellite System (TDRSS) Users' Guide" (Ref. 5-3) by the Goddard Space Flight Center, from which the technical specifications provided herein were extracted. No attempt will be made to repeat the information found elsewhere, other than to provide an overview of the primary technology parameters of bandwidth, sensitivity, power, etc., that affect the user interface with the spacecraft.

The Tracking and Data Relay Satellite (TDRS) will provide multiple services to user spacecraft on S- and Ku-bands. Multiple Access (MA) service may be shared by up to 20 users. All users operate on the same frequency and are discriminated by unique Pseudo-random Noise (PN) codes. Two single-access services are available. Single Access at

S-band (SSA) and Single Access at Ku-band (KSA). The available RF bandwidths are 5 MHz on MA, 10 MHz on SSA, and 225 MHz on KSA. Because of the coding requirements, the maximum return link data rates are 50 kbps on MA, 6 Mbps on SSA, and 300 Mbps on KSA.

The link calculations for the MA return link (orbiting spacecraft to relay satellite to ground), the SSA return link, and the KSA return link have been extracted from the TDRSS Users' Guide and are included herein as Tables 5 3.1-1 through 5.3.1-3.

A user currently receiving support by means of STDN is assumed to have the following equipment and capability:

- S-band receiver and transmitter
- S-band low-gain antenna
- Sufficient transmit EIRP and receiver sensitivity for operation with a 9-m ground antenna system.

MA users of the TDRSS must add equipment and capability as follows:

- A spread spectrum receiver with PN correlator and a Phase Locked Loop (PLL) capable of handling the frequency hop preamble used in acquisition
- A digital command decoder
- A spread spectrum transmitter
- Additional dc power for transmitter if continuous real-time operation is required
- A digital telemetry system capable of convolutional coding
- Increased EIRP. This may be accomplished with higher transmitter power, but most likely will be accomplished by a higher gain antenna. Higher antenna gains and narrower beamwidths mean that the user will have to provide an antenna pointing (tracking and/or steering) capability.

SA users of the TDRSS must also have the MA capability. Single access requires higher receiver gains than MA, as well as higher EIRP.

TABLE 5 3.1-1. SIGNAL CHARACTERISTICS FOR MA RETURN LINK, S-BAND

BER	10^{-5}
User EIRP (dBW)	EIRP
Space Loss (dB)	-192 2
Polarization Loss (dB)	-1 0
TDRS Antenna Gain at ±13 deg (dB)	28.0
P_S at Output of Antenna (dBW)	-165.2 + EIRP
T_S (Antenna Output Terminals) (K)	824
T_I (Due to Direct Other User Interference) (K)	255
$K(T_S + T_I)$ (dBW/Hz)	-198.3
$P_S/K(T_S + T_I)$ (dB-Hz)	+33.1 + EIRP
Transponder Loss (dB)	-2 0
Demodulation Loss (dB)	-1.5
PN Loss (dB)	-1.0
Antenna Beam Forming Loss (dB)	-0.5
System Margin (dB)	-3.0
Required E_b/N_0 (dB-Hz) (ΔPSK)	-9.9
Achievable Data Rate (dB)	+15.2 + EIRP
FEC Gain, R = 1/2, K = 7 (dB)	5.2
*Achievable Data Rate (dB)	+20.4 + EIRP

*This achievable data rate is the users' information rate It should not be confused with the channel symbol rate which is twice the information rate.

NOTE: Extracted from GSFC Document STDN No 101.2 - TDRSS Users' Guide

TABLE 5.3 1-2 SIGNAL CHARACTERISTICS FOR SSA RETURN LINK

BER	10^{-5}
User EIRP (dBW)	EIRP
Space Loss (dB)	-192.2
Pointing Loss (dB)	-0.5
Polarization Loss (dB)	-0.5
TDRS Antenna Gain (dB)	36.0 (50%)
P_S at Output of Antenna (dBW)	-157.2 + EIRP
T_S (Antenna Output Terminals) (K)	586
KT_S at Output of Antenna (dBW/Hz)	-200.9*
P_S/KT_S (dB-Hz)	43.7 + EIRP
Transponder Loss (dB)	-2.0
Demodulation Loss (dB)	-1.5
PN Loss (dB)	0.0**
System Margin (dB)	-3.0
Required E_b/N_O (dB-Hz) (ΔPSK)	-9.9
Achievable Data Rate (dB)	27.3 + EIRP
FEC Gain, R = 1/2, K = 7 (dB)	5.2
***Achievable Data Rate (dB)	32.5 + EIRP

*Does not apply when operated simultaneously with DG2

**-1 dB for DG1

***This achievable data rate is the users' information rate. It should not be confused with the channel symbol rate which is twice the information rate.

For more information, refer to TDRSS Users' Guide

NOTE: Extracted from GSFC Document STDN No. 101.2 - TDRSS Users' Guide

TABLE 5.3 1-3. SIGNAL CHARACTERISTICS FOR KSA RETURN LINK

BER	10^{-5}
User EIRP (dBW)	EIRP
Space Loss (dB)	-209.2
Pointing Loss (dB)	-0.5
Polarization Loss (dB)	-0 5
TDRS Antenna Gain (dB)	52.6 (55%)
P_S at Output of Antenna (dBW)	-157.6 + EIRP
T_S (Antenna Output Terminals) (K)	893
KT_S at Output of Antenna (dBW/Hz)	-199.1*
P_S/KT_S (dB-Hz)	41.5 + EIRP
Transponder Loss (dB)	-2.0
Demodulation Loss (dB)	-1.5
PN Loss (dB)	0**
System Margin (dB)	-3.0
Required E_b/N_0 (dB-Hz) (ΔPSK)	-9 9
Achievable Data Rate (dB)	25.1 + EIRP
FEC Gain, R = 1/2, K = 7 (dB)	5 2
***Achievable Data Rate (dB)	30.3 + EIRP

*Does not apply when generated simultaneously with DG2

**-1 dB for DG1

***This achievable data rate is the users' information rate. It should not be confused with the channel symbol rate which is twice the information rate.

For more information, refer to TDRSS Users' Guide

NOTE: Extracted from GSFC Document STDN No. 101.2 - TDRSS Users' Guide

The user interface on the ground will be at either the TDRSS ground station, the Goddard Space Flight Center, or the Johnson Space Center. Communication between these three ground centers will be implemented via the NASCOM network. The maximum bit rate between ground centers is planned to be 2.677 Mbps. No provisions are currently being made for multi-megabit data transfer between ground centers.

5.3.2 Trends in Space Data Transfer Via Relay Satellites

There are a number of trends in data relay satellites in general (migration to higher frequency bands, wider bandwidths, and higher data rates within these higher frequency bands, etc.) that could affect space data transfer by means of relay satellites. However, the present plans in the TDRSS program do not incorporate any of these into NASA's planning for the 1980-1985 timeframe. For a more detailed discussion of trends in data relay satellites in general, refer to Subsection 9.2.

For trends in relay satellite subsystems, refer to Subsections 5.1 and 5.2.

5.3.3 Projected Developments in Space Data Transfer Via Relay Satellites

Projections through 1985 call for continued use of the TDRSS for purposes of space data transfer by means of relay satellites. Although use of other frequency bands with added capabilities, as discussed in Subsection 9.2, would be technically feasible, this is not consistent with the present budget and planning for NASA missions.

In related areas, the Air Force Avionics Laboratory, Wright-Patterson AFB, is working on a laser satellite relay experiment to be operating in 1979. This system will use an Nd:YAG laser to transmit data at 1,000 Mbps from a synchronous satellite. NASA Goddard Space Flight Center is working on a laser data relay system called Advanced Tracking and Data Relay Satellites (ATDRS), which will be similar in operation to the TDRSS. Their developed hardware has demonstrated a 300-Mbps data rate and can track Doppler frequency variations over a $\pm$700-MHz range. The schedule for implementation of this system is unknown.

For projected developments in relay satellite subsystems, refer to Subsections 5.2 and 5.3.

5.4 GROUND STATION ANTENNAS

Ground station antennas represent a key link in communications satellite systems as evidenced by the fact that two of the important measures of ground station performance are directly influenced by the gain of the ground station antenna These measures of performance are 1) the EIRP and 2) the figure of merit of a receiving system. The EIRP is expressed in decibels above 1 W (dBW) and is obtained by adding the radiated power in dBW to the gain of the antenna (in decibels above an isotropic source) to which the power is delivered. The figure of merit of a receiving system is the ratio of the antenna gain to the system noise temperature expressed as dB/K and written as G/T.

Since many other antenna parameters (e.g., beamwidth, sidelobe level, efficiency) are related to the gain (G) and/or noise temperature (T_a) of the antenna, these two parameters generally describe the performance of a given antenna. When G and T_a are used in conjunction with the available power at the antenna or with the low noise amplifier (LNA) noise temperature, the resulting EIRP or G/T gives a very good indication of the performance of the ground station.

5.4.1 State of the Art in Ground Station Antennas

The majority of ground station antennas currently in use or planned for the near future are some form of parabolic reflector with diameters ranging from less than 3 m to more than 30 m. Over the past several years, ground station antennas of a given diameter have experienced significant improvement in gain and noise temperature. These improvements have resulted from the development of more efficient feed designs (including corrugated horns and beam waveguides), from the ability to maintain tighter surface tolerances during fabrication and assembly, and from the implementation of surface correcting systems to maintain these tolerances in the field. These improvements in antenna gains and noise temperature, when combined with the steadily increasing available transmitter power (see Subsection 5.1) and decreasing receiver front-end noise temperatures (see Subsection 5.5), have resulted in steadily increasing values for ground station EIRP and G/T. Furthermore, the availability of high-gain, low-noise antennas, higher-powered transmitters, and ultra-low-temperature receivers has opened the door to cost/configuration tradeoff studies relative to achieving a specified EIRP or G/T. The performance of meaningful tradeoff studies tends to minimize the overall cost (acquisition and ownership) of a ground station designed to achieve a given performance level.

Since it is now possible to achieve a given EIRP or G/T with various combinations of antennas and transmitters or LNAs, it is difficult to quantitize the state of the art of ground station antenna performance On the other hand, qualitative descriptions can be obtained by plotting representative values of EIRP and G/T as a function of antenna diameter for some existing systems in a given frequency band. Figure 5.4.1-1 shows such a plot for the 4- to 6-GHz band. As shown by this figure, the range of antenna diameters in use indicates that adequate antenna performance can be achieved with current designs. Thus future trends should be toward increasing the capacity of existing systems, increasing the number of systems, and reducing the overall cost of communications satellite systems.

These trends are discussed in more detail in the following paragraphs.

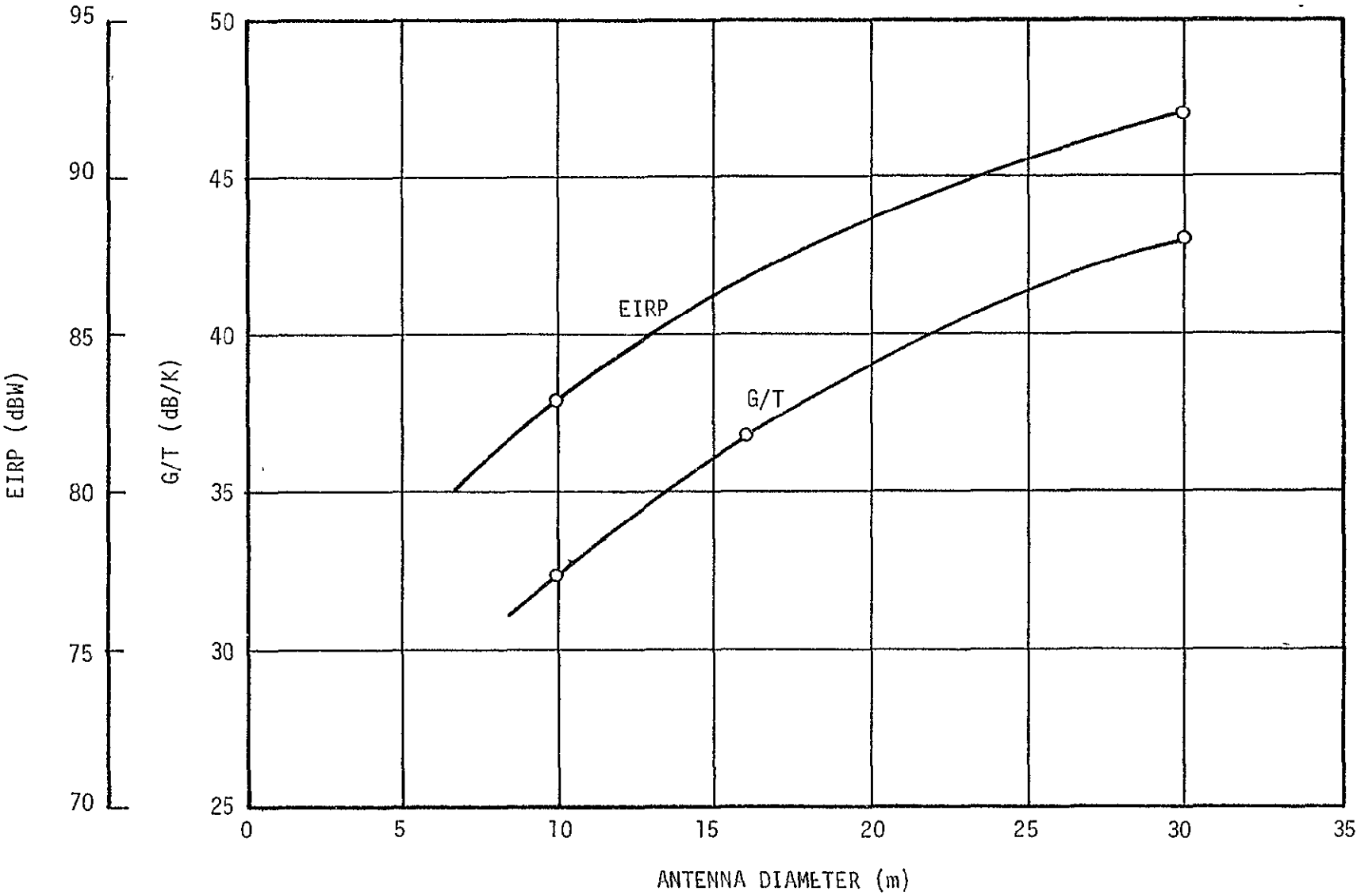

FIGURE 5 4 1-1. REPRESENTATIVE VALUES OF EIRP AND G/T FOR EXISTING GROUND STATIONS IN THE 4- TO 6-GHz BAND

5.4.2 Trends in Ground Station Antennas

Trends in ground station antenna design will be in the direction that permits increased capacity for existing systems and supports the proliferation of additional systems at lower overall costs.

With the continually increasing volume of traffic in the 4- to 6-GHz band, methods of increasing usage of the available spectrum are being and will continue to be developed. One approach relative to the antenna system is the "frequency-reuse" system, whereby the use of the available spectrum can be doubled. This technique can be implemented in existing ground station antennas by modifying the feed system to radiate/receive two orthogonal polarizations. Two operational, frequency-reuse satellite systems are being implemented, and development effort will continue to meet the required characteristics of frequency reuse feeds (e.g., maintain existing G/T and provide high polarization isolation).

Even with the increased capacity provided by frequency reuse and other techniques (see Subsection 5.6), the 4- to 6-GHz band will lack the capacity or capability to support the increasing demand for additional channels, including TV broadcasting and the high-speed digital communications that have been using terrestrial links.

The move to higher frequencies has already started with two experimental satellites in orbit and several more in the construction or planning stage in the 11- to 14-GHz (SATCOM) band. To support the use of the 11- to 14-GHz band, ground station antenna development will cover the entire range of antenna diameters from less than 1 m to greater than 100 m. The larger antennas (>80 m) will be used for radio astronomy and extraterrestrial research. Antennas in the 10- to 20-m range will be used to handle high-density, high-speed digital communication traffic, somewhat similar to the traffic in the 4- to 6-GHz band. Smaller antennas in the 3- to 6-m range will be used for television transmission and/or reception and for low-density FDM and single channel per carrier (SCPC) traffic. Antennas between 0.5 and 2 m in diameter will be used for television reception from satellites. The latter use will depend on achieving very high values of EIRP from the satellites.

Antenna designs based on the parabolic reflector will continue to be the dominant choice for ground station antennas. Some tradeoffs exist in the choice between prime focus (low sidelobes) and Cassegrainian (high gain) feeds, particularly with regard to the smaller antenna sizes. In addition, the need to reduce outages (caused by Sun transit, satellite failure, etc.) will require the continued development of multiple beam or steerable beam feeds for use with the larger reflectors. At higher frequencies, beam waveguide feeds will become more attractive and thus will become more common since they reduce the structural requirements on the antenna and its mount and offer the potential for low loss.

Cost reductions will be realized through the use of more reliable equipment including antenna steering and control systems; small, fixed-position receiving antennas used with geosynchronous satellites, and a trend toward standardized rather than one-of-a-kind ground stations.

5.4.3 Projected Developments in Ground Station Antennas

Future developments in ground station antennas will be related to the continued increase in frequency of the satellite communications systems. An increase to the 20- to 30-GHz band, where the International Telecommunications Union (ITU) has allocated contiguous bandwidths of up to 2,500 MHz, is inevitable. Ground station antennas will use the same design techniques that have been developed for the 4- to 6-GHz band and are being developed for the 11- to 14-GHz band.

5.5 MICROWAVE RECEIVERS

5.5.1 State of the Art in Microwave Receivers

Microwave receivers as discussed herein include that part of the overall receiving system between the antenna and the demodulator. Thus, the receiver as defined here provides gain, frequency conversion, and bandwidth limiting only. Demodulation is covered in Subsection 5.7.

Since receivers are designed to operate within a multiuser frequency spectrum, the permissible bandwidths are standardized by Inter Range Instrumentation Group (IRIG) regulations, and the restrictions imposed by these regulations preclude bandwidth from consideration as a technology item. The primary items of concern from a technology viewpoint then become receiver frequency, receiver noise figure as a function of frequency, local oscillator stability, frequency selection techniques, and physical considerations, including size, weight, power consumption, system configuration, and environmental limitations.

The availability of efficient and reliable hardware at frequencies above 10 GHz is of primary concern to designers of future systems because of frequency crowding at the lower bandwidths and because of the higher bandwidths associated with the frequencies. Significant improvements in both commercially available and developmental "front end" devices have occurred within the past 2 years, particularly in the area of gallium arsenide FET (GaAs FET), with some improvements in extending the upper frequency of cryo-cooled parametric amplifiers to include the 35- to 36-GHz band. Figure 5.5.1-1 presents curves of noise temperature as a function of frequency for the various devices being worked on in 1975 and 1977 without distinguishing between which devices are commercially available and which are developmental. Also, gain figures are not readily available, particularly at frequencies above 10 to 12 GHz. The February 1977 issue of Microwave Systems News published a listing ("FET Scoreboard", pages 70 and 71) (Ref. 5-4) of commercially available GaAs FETS, along with typical specifications. The listing is presented in Table 5.5.1-1,

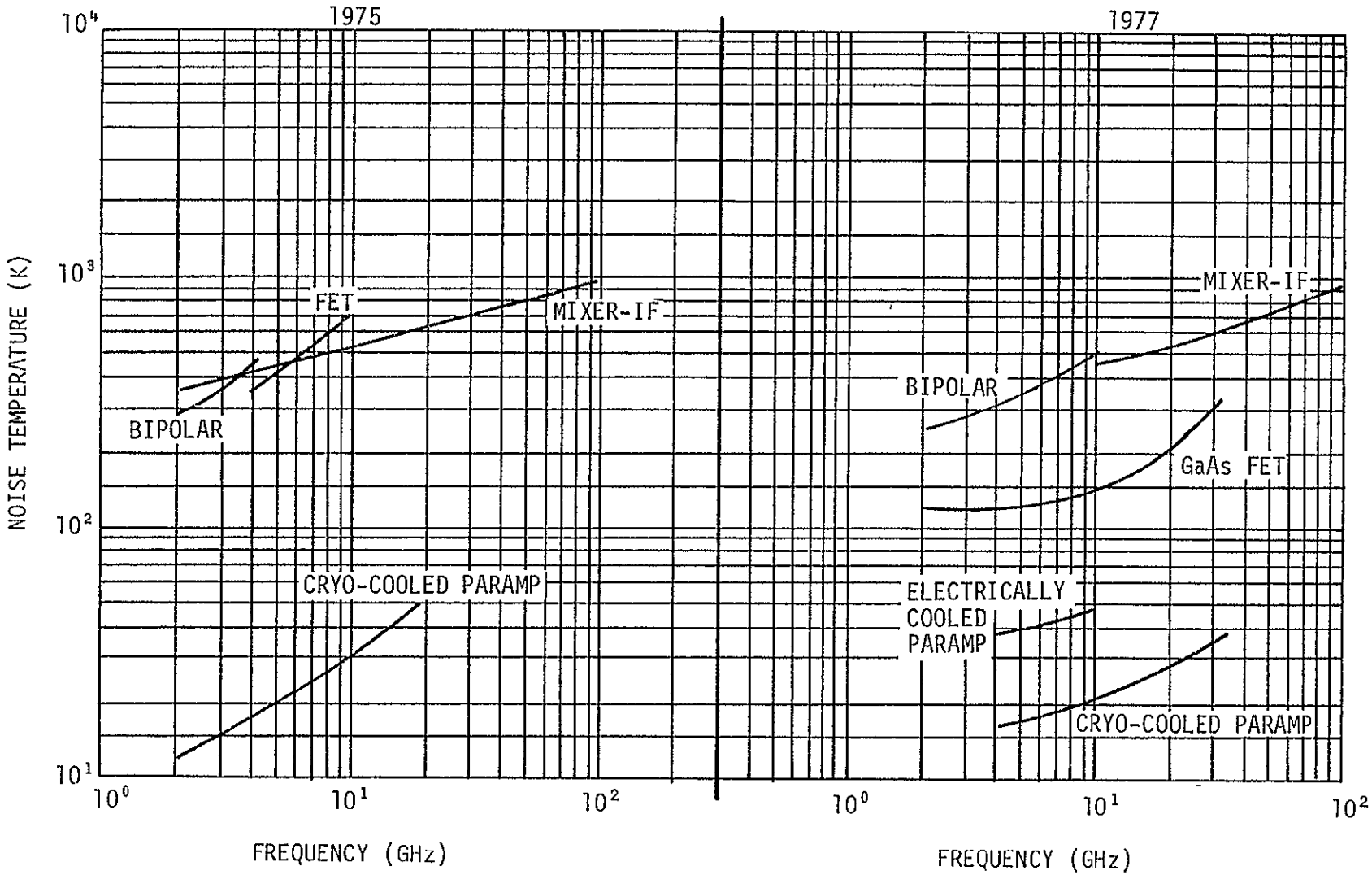

FIGURE 5.5 1-1. DEVICE NOISE TEMPERATURES AS A FUNCTION OF FREQUENCY

TABLE 5.5 1-1 SMALL SIGNAL FET CHARACTERISTICS AND COST
(EXTRACTED WITH MODIFICATIONS FROM REF. 5-4)

MANUFACTURER OR U S REP	MODEL	GATE LENGTH (μm)	NOISE FIGURE (dB min)	TEST FREQUENCY (GHz)	GAIN (dB)		RF POWER OUTPUT (dBm)	SMALL QUANTITY PRICE (1-9)
					ASSOC	MAG		
Aertech Industries 825 Stewart Dr Sunnyvale, CA 94086 (408) 732-0880	AFT2000	0 75	2.2	8	9 0	12.0	10 0	$ 60 (10-49)
Dexcel, Inc 2285-C Martin Ave Santa Clara, CA 95050 (408) 244-9833	DXL-502	0 50	2 5	7	7 0	9 0	10 0	$ 95 (1-24)
Fujitsu America, Inc 1135 E Janis St Carson, CA 90746 (213) 636-0858	FSC02	1 00	3 5	8	6 5	12 0	-	$250
Hewlett-Packard Company 1501 Page Mill Rd Palo Alto, CA 94304 (415) 493-1501	HFET-1000	1 00	3 6	10	6 9	11 0	14 5	$135
Hitachi-Denshi 58-25 Brooklyn/ Queens Expressway Woodside, NY 11377 (212) 898-1261	HCRL-85	1 00	3 0	8	-	11 0	10 0	$ 60
	HCRL-87	0 50	2 5	8	-	13 0	10 0	$160
NEC (Nippon Electric) Calif Eastern Labs One Edwards Ct Burlingame, CA 94010 (415) 342-7744	NE244	1 00	2 3	8	10 5	12 0	8 5	$ 75 (10-24)
	NE388	0 50	2 7	12	8 0	12 0	8 5	$125
	NE463	1 0/1 0 Dual	3 2	8	14 0	15 0	8 5	$ 90
	-	-	1 55	4	-	30	-	-
Plessey Optoelectronics and Microwave 1674 McGraw Ave Irvine, CA 92705 (714) 540-9945	GAT-5	0 80	2 5	8	10 0	12 0	13 0	$105
			3 0	10	8 0	10 0	10 0	
	GAT-3	-	3 5	12	-	5 8	-	-
	GAT-3	-	1 2	2	-	12	-	-

along with some additional listings that have been obtained elsewhere. Reference to the table shows that nothing is available commercially at frequencies above 12 GHz. Also, the information presented shows that the gain of the available devices at the higher frequencies is relatively low compared with the 20- to 30-dB gains that are achievable at frequencies below 4 GHz. Cost information is also provided, and that aspect of the program is particularly promising. Table 5.5.1-2 shows the state of the art of receiver noise temperature for several device types in the 4- to 36-GHz bands.

In general, data tend to indicate that receiver "front ends" at the higher frequencies do not use RF amplifiers but feed the signal directly from the preselector to the mixer.

The state of the art in local oscillator stability is presented in Table 5.5.1.3 for the three most commonly used sources. Because of cost considerations, quartz crystals are the most commonly used sources. Only those applications requiring extreme accuracy (e g., tracking receivers) can afford rubidium or cesium sources. Crystal oscillators with stabilities on the order of 1×10^{-6}/day are available in smaller packages at considerably less cost.

TABLE 5 5.1-2 1977 STATE OF THE ART IN RECEIVER NOISE TEMPERATURE

DEVICE	CHARACTERISTIC	
	NOISE TEMPERATURE (K)	FREQUENCY (GHz)
Bipolar	320	4
	500	10
FET	120	4
	150	10
	330	36
Paramp (Electrically Coded)	38	4
	48	10
Paramp (Cryo-Cooled)	16	4
	21	10
	38	36

TABLE 5 5.1-3. COMMERCIALLY AVAILABLE OSCILLATOR CHARACTERISTICS

CHARACTERISTIC	CESIUM	RUBIDIUM	QUARTZ
Accuracy	$\pm 1 \times 10^{-11}$	N/A	$\pm 2 \times 10^{-6}$
Long-Term Stability	$\pm 5 \times 10^{-12}$/life	$\pm 1 \times 10^{-11}$/month	$\pm 5 \times 10^{-10}$/day
Short-Term (1 sec) Stability	5.6×10^{-11}	5×10^{-12}	1×10^{-11}
Relative Cost	$20K	$9K	$600
Relative Size (in)	9 by 17 by 16	5 by 17 by 16	2.8 by 2 by 2 4

5.5.2 Trends in Microwave Receivers

Continuing pressure to reduce costs while improving performance has motivated manufacturers to find more cost-effective solutions for receivers. This has resulted in placing more functions per module and reducing the life-cycle costs of microwave systems The combining of a number of active and passive components that would normally be packaged separately has led to the "super component". An example is a Ka-Band front end that contains the preselector, amplifier, mixer, and IF filter in one small package. Super components eliminate some interconnections and packaging hardware. As a result, the size and weight of microwave systems are reduced, while the costs remain about the same. Development of gallium arsenide and indium phosphide FETs will allow replacement with solid-state components of TWTs in some receiver designs

Increased use of large-scale integrated circuits (LSI) will allow increased capability, improved reliability, reduced maintenance cost, lower power consumption, and a reduction in size. Devices such as surface acoustic wave (SAW) filters have the potential to provide further reductions in receiver size while providing very stable, maintenance-free bandwidth filtering. However, unless there is greater standardization of receiver IF bandwidths, SAW devices will not be very common because of their cost. (A system such as commercial television is a broad, standardized market where SAW devices will become common.)

Figure 5.5.2-1 presents the projected trends in GaAs FET noise figures from the present to 1985 Figures 5.5.2-2 and 5.5.2-3 project the trends in receiver size and power consumption for the same period.

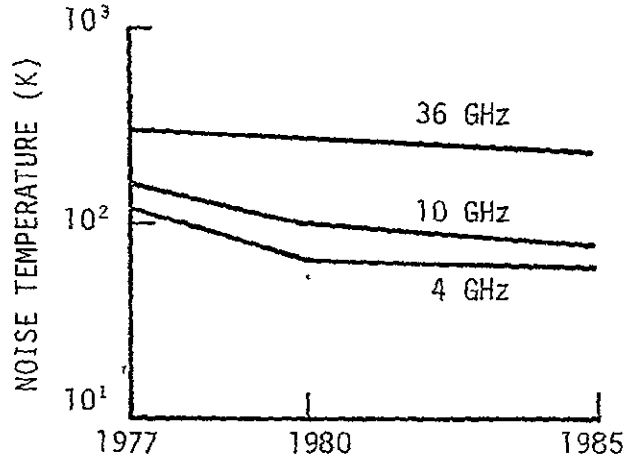

FIGURE 5.5 2-1. PROJECTED TRENDS IN GaAs FET NOISE TEMPERATURE

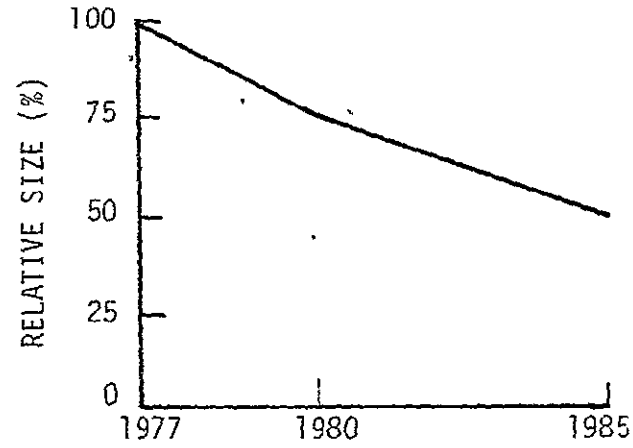

FIGURE 5 5.2-2. PROJECTED TRENDS IN RECEIVER RELATIVE SIZE

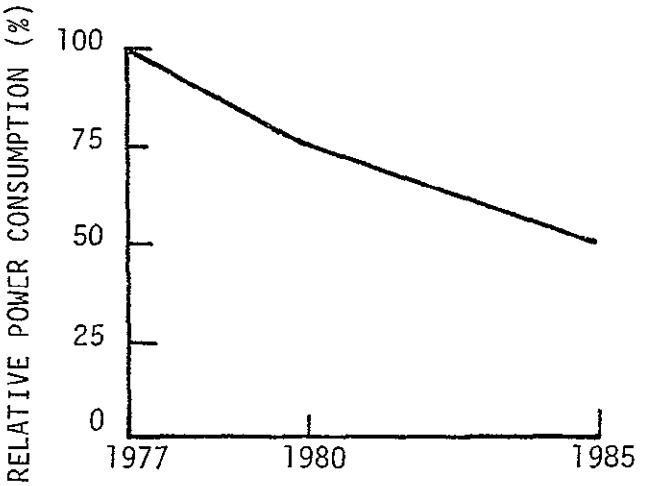

FIGURE 5.5.2-3 PROJECTED TRENDS IN RECEIVER POWER CONSUMPTION

5.5.3 Projected Developments in Microwave Receivers

As a result of developments in super components, receiver size will continue to decrease to somewhere in the range of 25 to 50% of their present size by 1985, while performance will improve. Power consumption will continue to decrease, especially for the higher frequency receivers. The decline in power consumption will not be at a constant rate but is expected to be approximately one-half the present consumption by 1985. Solid-state devices will be capable of operating at higher frequencies with sufficiently low noise figures and high enough gains to replace TWTs in existing systems. GaAs FETs will undoubtedly continue to show improvement in noise figure and gain. Tables 5.6.3-1 and 5 6.3-2 list projections of receiver noise temperature for 1980 and 1985, respectively

TABLE 5 5.3-1. 1980 PROJECTIONS OF
RECEIVER NOISE TEMPERATURE

DEVICE	CHARACTERISTIC	
	NOISE TEMPERATURE (K)	FREQUENCY (GHz)
Bipolar	N/A	4
	N/A	10
FET	85	4
	110	10
	350	36
Paramp (Electrically Cooled)	N/A	4
	N/A	10
Paramp (Cryo-Cooled)	N/A	4
	N/A	10
	N/A	36

TABLE 5.5.3-2. 1985 PROJECTIONS OF
RECEIVER NOISE TEMPERATURE

DEVICE	CHARACTERISTIC	
	NOISE TEMPERATURE (K)	FREQUENCY (GHz)
Bipolar	N/A	4
	N/A	10
FET	73	4
	75	10
	250	36
Paramp (Electrically Cooled)	N/A	4
	N/A	10
Paramp (Cryo-Cooled)	N/A	4
	N/A	10
	N/A	36

5.6 MODULATION AND CODING

5 6.1 State of the Art in Modulation and Coding Technology

Modulation and coding are the major areas of signal design and signal processing and are intimately related. Signal design can be defined as coding/decoding, modulation/demodulation, and bandwidth compression. Signal processing includes any transformation of signals into information sets that are useful and meaningful to the user.

5.6 1.1 Modulation - Modulator characteristics of interest are shown in Figure 5.6.1.1-1. The two major classes of modulation are angle and amplitude modulation. Angle modulation is further broken into phase modulation (PM) and frequency modulation (FM). The factors of bandwidth, linearity, physical characteristics, and cost apply to all forms of modulators. Amplitude modulation (AM) is now used mostly with optical band (laser) transmission systems. A few systems use a combination of AM and PM. Frequency modulation is used mostly in frequency division multiplexing (FDM)/FM systems where data rates are relatively low. The most common form of modulation is PM where it is used for the lowest to the highest data rates.

Binary-phase-shift-keyed (BPSK) modulation is a well-developed PM technology where the RF carrier is shifted between 0 and 180 deg according to the binary modulating data. Quadriphase-shift-keyed (QPSK) modulation is becoming increasingly popular because twice the data rate can be transmitted in the same RF bandwidth as the BPSK. Systems using 8-phase and 16-phase modulation, as well as AM-PM combinations, are being developed.

The need for transferring more and more data through a finite bandwidth has resulted in another measure of technology, bits-per-second per hertz (bps/Hz). Ordinary BPSK modulation results in 0.5 bps/Hz, QPSK doubles this to 1 bps/Hz Systems using 8- and 16-phase modulation schemes increase this number as shown in Table 5.6.1.1-1. Table 5.6.1.1-2 shows the bandwidth efficiency as a function of modulation technique for a number of operational and experimental systems currently in use (Ref. 5-5)

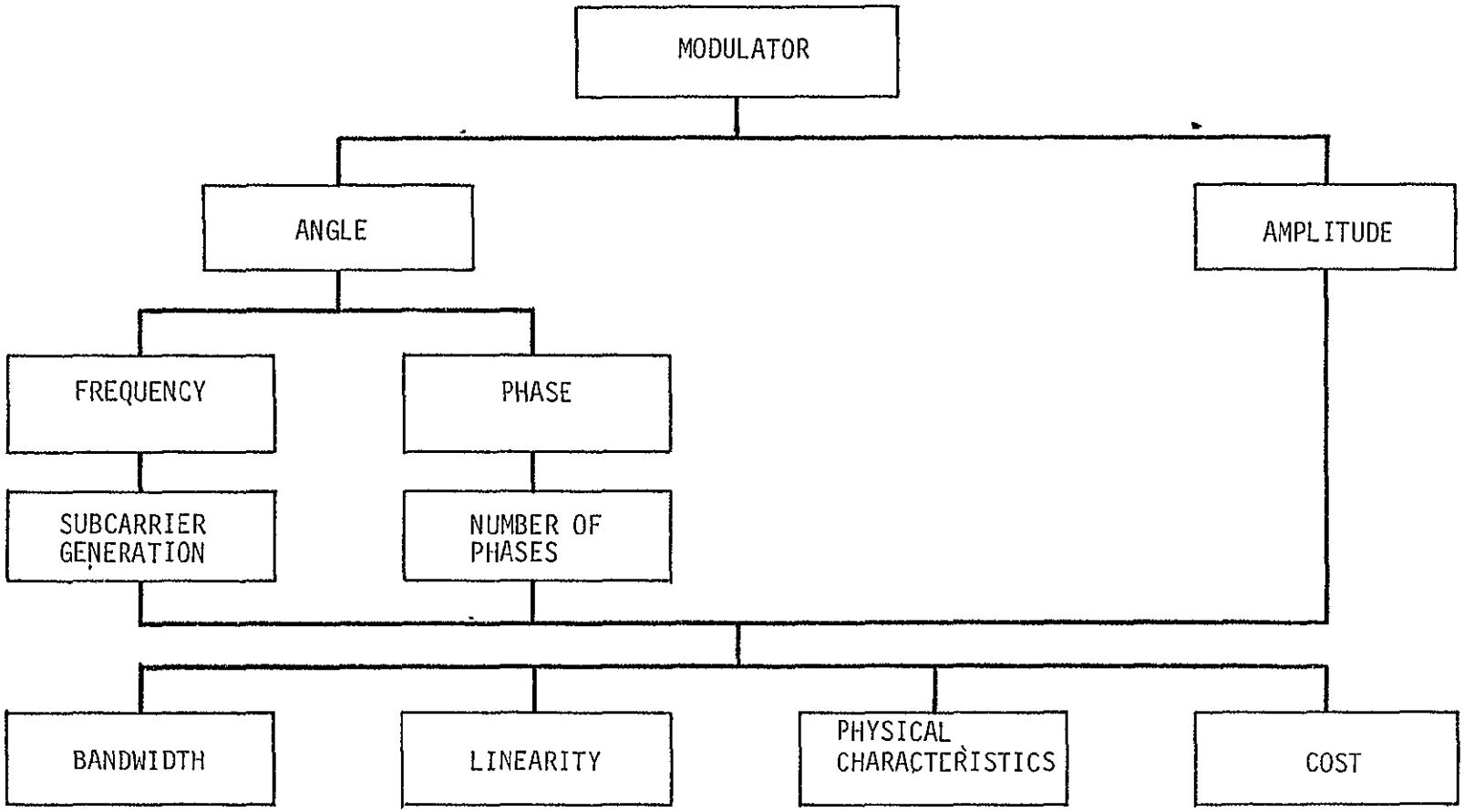

FIGURE 5 6.1.1-1 MODULATOR CHARACTERISTICS

TABLE 5 6.1.1-1. CHARACTERISTICS OF M-ARY-PHASE-SHIFT-KEYED MODULATION SCHEMES

MODULATION TYPE	EFFICIENCY (bps/Hz)	BANDWIDTH (BR)	REQUIRED E/No FOR BER = 10^{-6} (dB)
BPSK	0.5	2 0	10 6
QPSK	1.0	1 0	10.6
8 PSK	2.0	0.75	12.7
16·PSK	4.0	0 5	18 2

TABLE 5.6 1.1-2. BANDWIDTH EFFICIENCY AS A FUNCTION OF MODULATION TECHNIQUE (Ref 5-5)

LEVEL	TYPE MODULATION	BPS/Hz	WHERE USED
2	2 ϕ PSK (using M)	0.50	Canada Thin Route Norway Marisat TTY
4	QPSK	0.94	SBS
	QPSK	1.12	SPADE (Intelsat)
	QPSK	1.53	Telsat
	SQPSK	1.30	Bell System T3 transmission via 11 GHz radio
	QSPSK	1.80	Experimental (F. Chethik)
	FFSK	2.20 (2.5 capability)	CTS Canada Experiment (11/14 GHz through 85 MHz BW)
6	QPRK	2.25	Microwave Associates 11 GHz terrestrial radio
7	Zero-Memory Nyquist Correlative Coding: Modulating a PCM-FM System	4.00	Lenkurt system for transmitting 6.312 Mbps T2 over 3 MHz terrestrial radio channel
8	8 ϕ PSK	1.81	TDMS through Intelsat IV by Fujitsu Ltd
	8 ϕ PSK	2.20	NEC terrestrial radio for 11 GHz
16	16 ϕ PSK	4.00	Comsat Labs/Japan NTT/ECL
	16 APSK*	4 00	Japan NTT/ECL†
32	4-bit QASK**	4.00	JPL for Space Lab††
49	Hexagonal type signal format using superimposed modulation	4.00	Japan NTT/ECL† (experimental)

*Combined amplitude and phase shift keying
**Quadrature amplitude shift keying
†K. Myauchi, IEEE Trans Comm., February 1976
††J Smith, AIAA paper 76-230

As the required bandwidth decreases, the bit signal-to-noise ratio (E/N_o) increases to maintain the same bit error rate (BER). For example, for a BER of 10^{-6}, the required E/N_o goes from 10.6 dB for BPSK to 18 2 dB for 16-phase modulation. This places a restriction on a user satellite in radiated power (EIRP) such that 8- and 16-phase modulation schemes may not be feasible for data transfer from satellites.

QPSK can be accomplished with two bi-phase modulators connected either in series or parallel. The parallel method is used for low power and lower frequencies (X band and below). The series modulator adapts readily to waveguide circuits. This latter approach has demonstrated data rates to 1 Gbps. PIN diodes, Schottky diodes, and FETs can be used in the series modulator.

The Air Force Avionics Laboratory, Wright-Patterson AFB, is working on an experimental satellite-to-ground Nd.YAG laser communication system that will handle a 1-Gbps data rate. This experiment is scheduled to be flown in 1979. NASA Goddard has just completed a 5-year study of satellite-to-satellite laser communication systems. Using a CO_2 laser with a 0.95-W output, modulation capabilities of 300 Mbps with an NRZ-L binary code have been demonstrated. The modulator is a cadmium telluride rod that changes the polarization of the laser output.

5.6.1.2 Coding - Digital data can be encoded in many ways. Binary bit codes (e.g., NRZ, RZ, and bi-phase) were first used and were selected mainly on the basis of the different spectrums produced. Block codes (e.g., adding parity bits to a word or frame) were introduced as a means of detecting bit errors and thus increasing the reliability of the data. Continuous codes (e.g., convolutional and PN) were later used for improving data reliability, spectrum spreading, signal identification, and measuring satellite range and range rate. Coding allows almost 100% use of the data channel capacity in the presence of noise.

Certain communication links under development, such as the TDRSS, require the use of concatenated (multiple) codes. In this case, a 2^{18} bit PN code is used for spectrum spreading and user identification to allow up

to 20 users to operate on the same frequency. This same PN code will also be used to derive range and range-rate information. Additionally, a convolutional code of rate 1/2, constraint length 7, will be used to improve the data reliability since long transmission distances will be used.

In the past, the power limitation of the transmitted signal resulted in the additive noise being the predominant cause of random errors. This limitation on power no longer exists for a wide range of frequencies and the random errors have become less significant than the burst errors and slippage errors. Current convolutional codes are capable of correcting random errors but are not adaptable for correcting long burst errors and slippage errors However, block codes such as the BCH Code and Reed-Soloman Code exist that can correct all three types of errors.

5.6.2 Trends and Projected Developments in Modulation and Coding

The trend over the years has been to transfer information at ever-increasing rates. This trend will continue as shown in Figure 5.6.2-1. In the 1960's and even early 1970's, FDM of analog signals was quite common. Radio frequency bandwidths of 400 kHz or less were adequate. More and more, analog signals are being converted to digital signals for transmission. Once converted to digital signals, multiple-phase modulation schemes are being used extensively to increase the bps/Hz that are transmitted over available bandwidths. The major exception to this rule is optical systems, which almost exclusively use AM techniques.

In the area of coding, the trend is toward block codes for error detection and correction while continuous codes will continue to be used more for spectrum spreading purposes. Since coding schemes must be responsive to the error phenomenon, future systems that use higher frequencies will not necessarily use the same techniques as those that use lower frequencies. Techniques such as polarization and/or space diversity may allow systems to operate with sufficient reliability that the need for other coding methods will be minimized.

Modulation schemes for data transmission through 1985 will tend to divide into two types: low-data-rate, narrowband systems and high-data-rate, wideband systems. The latter systems will use M-ary phase modulation schemes for frequencies below the optical band. The optical band will continue to use AM. Data rates for both the optical and RF band will be in the 200- to 1,000-Mbps range.

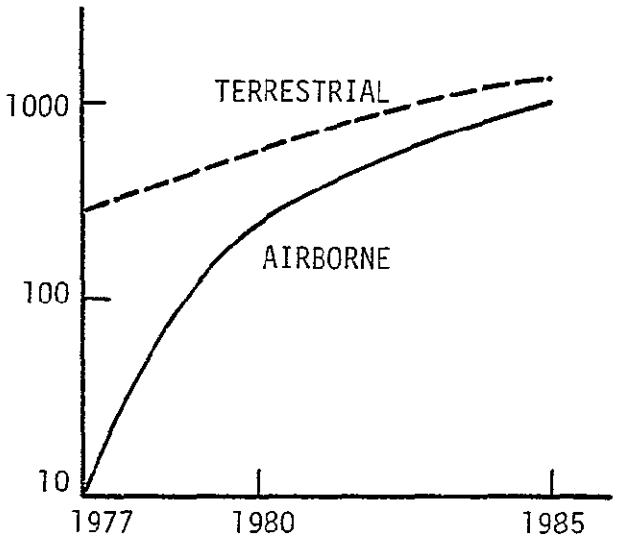

FIGURE 5.6.2-1. TRENDS IN MODULATION RATES

5.7 DEMODULATORS

5.7.1 State of the Art in Demodulators

Demodulators perform the function of converting the modulated RF signal to a baseband signal. Demodulators can be divided into two major categories, as shown in Figure 5.7.1-1. angle and amplitude. The angle demodulators are further divided into frequency (FM) and phase (PM) types. The characteristics of allowable modulation index, bandwidth, linearity, size, and cost are common to all demodulators. Amplitude demodulation (AM) for data transmission is now used almost exclusively in the optical band. (A combination AM-PM is used for some high-data-rate terrestrial cable systems.) FM demodulators have been the workhorse of missile telemetry systems. They are still used for FMD/FM signals of (now) relatively narrow bandwidth. The FDM baseband as defined in IRIG-106-75, "Telemetry Standards" (Ref. 5-6), is limited to about 200 kHz. This FDM system allows the user a maximum of 21 analog data channels with frequency response from 6 Hz to 2,475 Hz. PM demodulators have been used mainly for PCM/PM signals since the trend to digital coherent transmission signals has been so strong.

Bi-phase-shift-keyed (BPSK) modulation is very common for low to intermediate binary data rates. BPSK is a specific case of PCM/PM where the binary data modulates the RF carrier to 0- or 180-deg phases. Demodulation of BPSK requires a carrier reconstruction (i e., a carrier without phase modulation). This is accomplished by multiplying the received (intermediate frequency) signal by two and phase locking the local oscillator to it. The doubled signal modulation is modulus-360 and thus the doubled carrier appears to have no modulation. Quadriphase-shift-keyed (QPSK) modulation is also used where the carrier is modulated by one binary bit stream between 0 and 180 deg while also being modulated by a second binary bit stream of the same bit rate between 90 and 270 deg. Section 5.6 on modulation gives more information on this technique. In demodulating QPSK, the carrier must be reconstructed as with BPSK. This is accomplished by multiplying the received intermediate frequency signal by four to phase lock a local oscillator to it. The X4 multipliers use step recovery diodes, tapped delay line frequency multipliers, or FETs.

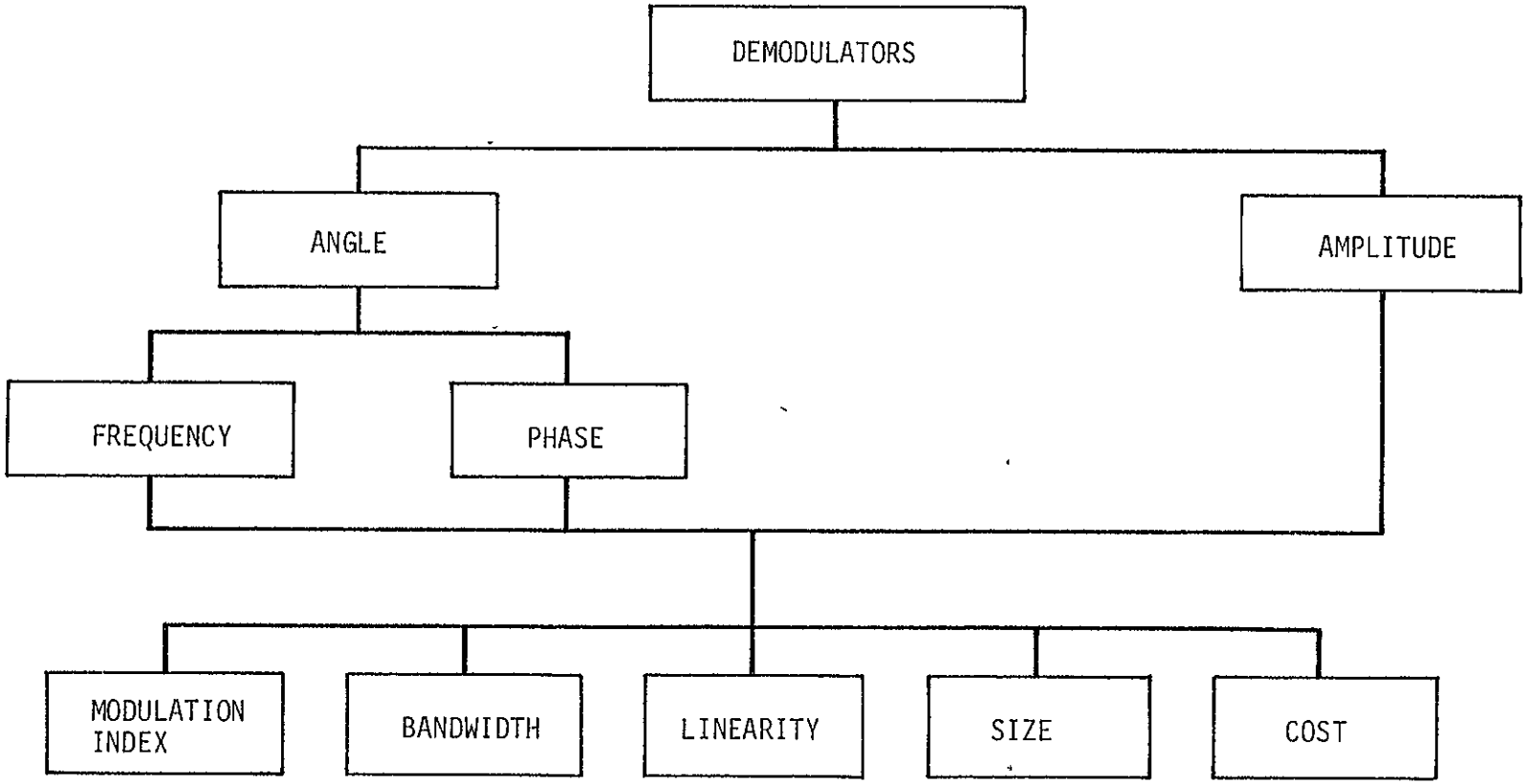

FIGURE 5.7.1-1. DEMODULATOR CHARACTERISTICS

5.7.2 Trends and Projected Developments in Demodulators

Improvements in integrated circuit technology will allow demodulators to operate at higher intermediate frequencies. The trend toward surface acoustic wave (SAW) devices for fixed-tuned bandpass filters and charge-coupled devices (CCDs) in transversal filters will allow demodulators to increase in complexity yet be physically smaller and consume less power. Both of these devices will also be used in decoding processes. The costs of these new devices will be offset by the reduction in parts count and reduced size of circuit boards and housings. Further, the analog portion of the receiver will shrink as more and more digital circuitry is used. The trend is to have digital circuitry from the conversion to baseband to the output of the receiver. When short ($\leq$512-bit) PN codes are used, it is likely that CCD transversal filters will be employed. Longer PN codes, such as required by TDRSS, will require delay lock loops. Figures 5.7.2-1 through 5.7.2-3 show the trends in demodulator complexity, size, and power consumption.

With the trend toward higher operating frequencies and all-digital systems, demodulators will shrink to about one-half their present size by 1985 Power consumption will be reduced to about one-third of current requirements in spite of more complex demodulator schemes. The cost should remain about the same.

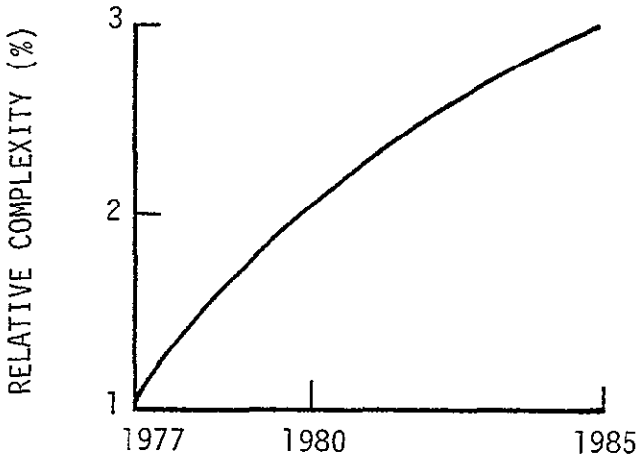

FIGURE 5 7 2-1. TRENDS IN DEMODULATOR COMPLEXITY

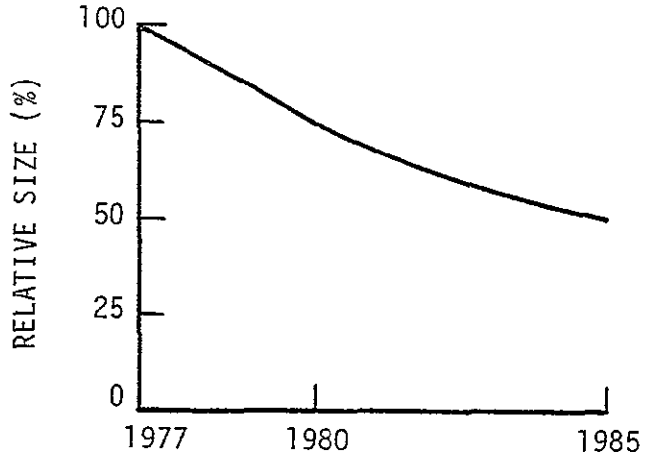

FIGURE 5 7 2-2. TRENDS IN DEMODULATOR SIZE

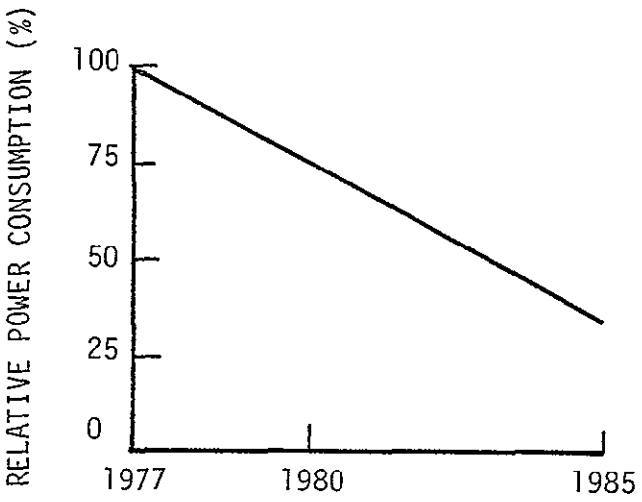

FIGURE 5.7.2-3. TRENDS IN DEMODULATOR POWER CONSUMPTION

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6. PREPROCESSING ELEMENTS

Preprocessing elements are defined herein to include the Level 1 elements identified in Figure 6-1 Thus, the preprocessing elements consist of the data storage and data manipulation (hardware and software) elements that take either the predetection or postdetection serial bit stream and detect (as necessary), buffer or store, demultiplex, and reformat into a parallel, digital format with calibrations. Detection, wideband recording, and decommutation/demultiplexing technologies are presented in this section. Processor elements, data storage elements, and software are reserved for Section 7, which discusses these aspects under the context of processing elements.

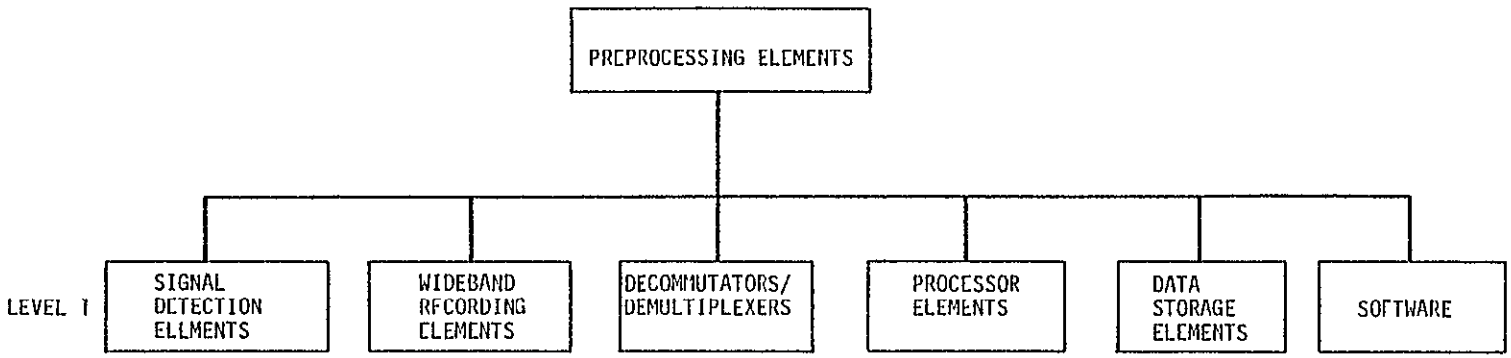

FIGURE 6-1. PREPROCESSING ELEMENTS

6 1 SIGNAL DETECTION ELEMENTS

(To be provided)

6.2 WIDEBAND RECORDING ELEMENTS

This subsection addresses the technology for instrumentation type tape recorders such as those found in telemetry ground receiving stations for recording wideband analog and digital (PCM) data. Subsection 3.1 addressed the technology for using magnetic tape recorders for spacecraft data storage, and Subsection 7.2.6 examines the technology for data processing magnetic tape recorders. Most of the discussion in Subsection 3.1 is applicable to ground instrumentation recorders, particularly the projections of Subsection 3.1.3

Magnetic tape recorders have been used in the instrumentation area for many years. During this time, major progress has been made in improving the performance through advances in the recording heads, the electronics, the drives, data encoding, and the media (i.e , the tape). Also, standards have evolved for tape speeds, tape widths, data bandwidths, etc.

Currently, most of the new developments in instrumentation recorders are directed toward achieving higher data rates and greater storage densities in high-rate digital recording systems.

6.2.1 State of the Art in Wideband Magnetic Tape Recorders

Today's instrumentation recorders are available in a wide variety of standard configurations as defined in Table 6.2.1-1. The recorders listed in this table are the fixed-head instrumentation type recorders such as those manufactured by Ampex and Bell & Howell. Fixed-head recorder designs have progressed from 14 tracks/in. in the 1960's to 42 tracks/in. at present. Frequency responses of 2 MHz are standard, and experimental systems are being tested with frequency responses of 4 MHz at 120 in/sec. Several companies are currently developing recorders that use 2-in.-wide tapes with up to 84 tracks; however, these recorders are not yet commercially available

According to Bessette (Ref. 6-1) fixed-head recorders currently achieve 50% of the theoretical potential number of bits per inch (80 kbpi) and 10% of the potential number of heads per inch (1,000/in.) This implies that fixed-head recorders achieve 5% (10% of 50%) of the theoretical data packing density (5×10^7 bits/in^2) using currently available media. These figures indicate that future improvements in recording density will be achieved by increasing track density rather than attempting to increase bit density.

Increasing the number of data tracks also increases the total input data rate for digital applications. However, for analog recorders, the bandwidth can only be increased by increasing in-track response either by increasing the data density or by moving the tape at higher speed. Factors that affect the response of a track are the tape magnetic particle size (12 µin. typical), the head gap, and the tape speed. The head gap is the most limiting component of response at this time. The small gaps required for higher-frequency response require shallower pole face depths, which are difficult to achieve and have shorter lives. New methods of tape lubrication are being developed to improve the head life. Developments in magnetic materials to allow smaller particle size and thinner oxide coating are also occurring.

TABLE 6 2.1-1. STANDARD INSTRUMENTATION RECORDER CONFIGURATION

Tape Speeds	15/16 to 240 in/sec
Tracks	7, 8, 14, 16, 28, 32, or 42
Tape Widths	1/2, 1 in.
Reel Size	8, 10 1/2, 12 1/2, 14, 15, and 16 in.
Record Methods	FM, direct, digital high density
Bandwidth/Data Rates (per track)	
FM	dc to 600 kHz (at 120 in/sec)
Direct	100 Hz to 2 MHz (at 120 in/sec)
Digital H D.	to 3.5 Mbps (at 120 in/sec)

In addition to the "standard" instrumentation recorder configurations, there are several other types of instrumentation recorders. One is the Newell drive type recorder manufactured by Emerson The other type is the rotary-head recorder manufactured by RCA, Ampex, and Echo Science.

The Emerson TITAN recorder features 42 tracks on a 1-in.-wide tape with tape speeds of up to 600 in/sec. The TITAN will record digital data at up to 10 Mbps/track.

Rotary-head recorders offer a number of advantages, including: higher data storage density, rapid start/stop, and high rate at low tape speed. Because of these advantages, a number of authorities believe that the rotary-head type recorder will find increased application for instrumentation recording in the future.

The RCA VERSABIT 200 is representative of the state of the art in rotary-head recorder designs. This system records 20 Mbps on a standard 2-in.-wide television tape at a tape speed of only 9.53 in/sec The VERSABIT 200 records at an in-track density of 10,000 bpi at 133 tpi. RCA is currently developing a double-density system with a track density of 266 tpi

6.2.2 Trends in Wideband Magnetic Tape Recorders

The trends in fixed-head instrumentation recording systems are toward wider tapes and more tracks per inch of tape This results in higher data rates for high-density digital recording and more channels for analog recording. As a result of the trend toward digital instrumentation and communication systems, most authorities question whether analog recording will still be in use in the 1980-1985 timeframe for ground-based data handling systems.

Bell & Howell is currently developing a recorder for Northrop that is to be incorporated into an Air Force system that has 84 tracks on a 2-in.-wide tape and records at an input data rate of 270 Mbps. RCA has recently demonstrated a laboratory model of a 240-Mbps recorder with 120 data tracks. These recorders are forerunners of the next-generation commercial fixed-head instrumentation tape systems.

Rotary-head recorders will find increased use in systems that utilize instrumentation recorders to provide temporary buffering as well as permanent data storage where frequent start/stop/replay operations are required such as on-line processing of satellite data.

Trends in rotary-head recorder designs are toward higher data rates using multiple heads, more tracks per inch of tape, and tape head designs that reduce head wear. As previously mentioned in Subsection 3.1, IBM's recently announced 3850 Mass Storage System employs a helical scan rotary-head system that "flys" a 2.7-in.-wide tape across the head at 10 μin. to minimize head wear.

6.2.3 Projected Developments in Wideband Magnetic Tape Recorders

A number of improvements in both analog and digital recorders are within current technological capabilities. Authorities predict improved tape handling through increased use of vacuum chambers and zero loop configurations by 1980 and improved maintenance and calibration through the use of microcomputer interfaces by 1985.

Several authorities predict that for analog recorders, 4-MHz bandwidth at 120 in/sec will become a standard option by 1980 with up to 48 tracks/in. on either 1-in. or 2-in.-wide tapes

Most authorities foresee the trend heavily toward digital recording by 1985 If analog recording is still in use, 6-MHz bandwidth capability will be available. On the digital side, very-high-density digital recorders with throughput rates of 1 Gbps at densities of 10^7 bits/in^2 will become available in the 1980-1985 timeframe. Thr projections presented in Figures 3.1.3-1, 3.1.3-2, and 3.1.3-3 for aerospace instrumentation recorders also apply to ground instrumentation recorders.

A number of other projections foreseen in the 1980-1985 timeframe include a move from longitudinal to rotary, helical, or transverse heads to permit the use of very narrow tracks without excessive costs; rapid start-stop capability along with continuously variable speeds, and improved reliability and head lifetimes through improved head designs, tape-lubrication, and other techniques.

Everyone agrees that magnetic tape will remain the low-cost medium for high capacity ($\approx 10^{12}$-bit) recording through 1985.

6.3 DEMULTIPLEXER/DECOMMUTATOR ELEMENTS

Demultiplexer/decommutator elements are divided into either analog or digital classifications, as shown in Figure 6.3-1. Analog demultiplexers are further subdivided into frequency-division multiplexing (FDM) and time-division multiplexing (TDM) systems Since analog TDM has been replaced by digital PCM for space data handling applications, advances in analog TDM decommutator technology are not reported.

In general, the technology for decommutators and demultiplexers is comparable, with the technology for multiplexers as reported in Sections 4 and 9, since the same system technology (e.g., data rates, bandwidths, and codes) applies in both areas. In fact, decommutator technology should be ahead of spacecraft multiplexer technology because of less restrictions on size, power consumption, weight, etc.

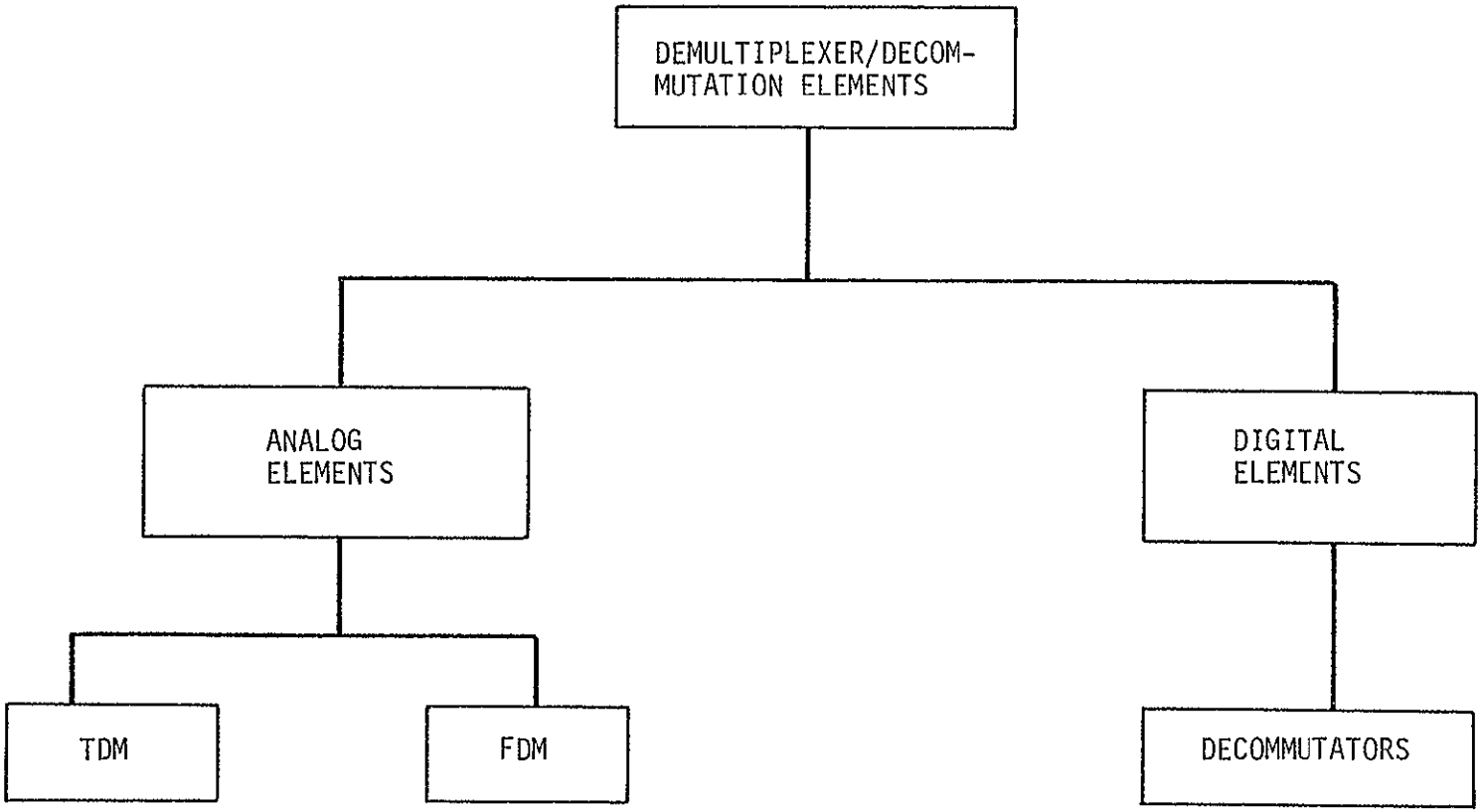

FIGURE 6.3-1. DEMULTIPLEXER/DECOMMUTATOR ELEMENTS

6.3 1 State of the Art in Demultiplexers/Decommutators

FDM signals are defined by IRIG 106-75 "Telemetry Standards". The development of FDM decommutators in recent years has been toward smaller, more universal, plug-in type discriminators with low power consumption However, until recently very little has been done toward increasing the number of data channels or data capacity As with other areas of communication electronics, the development of MSI and LSI circuits has done much to reduce the size and power consumption of these units. Because of the trend toward higher data rates and all-digital systems, there has been very little new development in FDM decommutators.

The new IRIG 106-77, which will be released later this year, will increase the number of available channels by the addition of wide-band channels above the already existing constant-bandwidth and proportional-bandwidth channels. Some authorities indicate that there is still a need for additional narrowband constant-bandwidth channels to increase the availability of channels to handle 50-Hz data. The Shuttle Solid Rocket Booster FDM system uses several nonstandard, constant-bandwidth channels to get more 50-Hz data channels

Digital demultiplexers represent the area of demultiplexing where the greatest changes resulting from technology improvements have been made in recent years. Demultiplexers available today on a commercial basis tend to be capable of handling data rates on the order of 2 to 5 Mbps, with some units available at 10 Mbps on a more-or-less custom basis Current technology permits decommutation hardware capable of handling hundreds of megabits; however, only a few systems are currently under development that will handle data rates in excess of 100 Mbps. The TDRS ground station, which is being built by Harris under a subcontract from TRW, will be capable of handling data rates up to 300 Mbps.

As discussed in Section 4, the Air Force has an operational laboratory model of a 1-Gbps digital data system that includes a 6-channel demultiplexer. This system uses custom-designed integrated circuits.

6.3.2 Trends in Demultiplexers

Improvements in LSI and standardization of high-data-rate systems will allow a reduction in size, power consumption, and increased capabilities. Already INTELSAT has developed a set of LSI circuits that are available to users to provide PCM encoding/decoding, convolutional coding/decoding, transmitter synchronization, and bit timing recovery for their system. Plessey now has programmable dividers that operate up to 1.2 GHz. In the United States and Canada, digital coaxial cable systems are operating at 274-Mbps rates. Because of the increase in data requirements by satellite imaging systems, data rates will accelerate through 1985. Motorola, under contract to McDonnell Douglas, is developing communications electronics for a 1-Gbps laser space-to-ground data link. Although the system does not include a demultiplexer as it only transmits two 500-Mbps PN codes to test the optical data link, it is representative of the trend toward higher-data-rate systems. The system is currently scheduled to be test flown (probably from synchronous orbit) in either 1980 or 1981.

Increased flexibilities in decommutators can be expected through 1985 as a result of the availability of low-cost memory and microprocessors. Authorities forecast that "Decom" boxes will contain more internal intelligence and will become multiported to accommodate distributed processing of high-data-rate signals. More digital signal processing will be employed in the signal detection and synchronization areas Improvements will be made in signal processing performance, and increased throughput (data rate) through the use of distributed processing and improved human factors of units can be expected. Increased development of Transfer Electron Devices (TEDs) and GaAs logic elements with their reduced propagation delay and low power consumption may have an effect on demultiplexers by 1985. Little, if any, development is expected in FDM equipment.

6.3.3 Projected Developments in Demultiplexers

The multiplexers used in future space-to-ground data links are expected to be digital. Two types of digital demultiplexers are foreseen general-purpose and unique/dedicated, with the general-purpose types being restricted to the lower data rates and the unique/dedicated types being built for special-purpose systems or experiments such as the Thematic Mapper.

As stated earlier, the technology will support hundreds of megabits, however, standard commercial products for 1980 will be of the general-purpose type and capable of handling 10 to 12 Mbps, with increases to 35 to 40 Mbps for 1985. At the higher data rates, custom demultiplexers will be built using either ECL, GaAs, or other high-speed logic technologies that become available.

Decommutators will have more output ports to accommodate distributed processing of high-data-rate signals. They will also be more adaptive in an attempt to overcome nonstationary noise and signal conditions. Concatenated coding will be implemented to correct errors from random noise, burst errors, and signal dropout. Some authorities also predict error probabilities within 1 dB of theoretical for data rates up to 5 Mbps, within 2 dB for 5 to 20 Mbps, and within 3 dB for 20- to 50-Mbps signals by 1985.

REFERENCES - SECTION 6

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7. PROCESSING ELEMENTS

Processing elements include the Level 1 hardware, software, and firmware elements and their corresponding Level 2 elements, as illustrated in Figure 7-1. The Level 1 hardware elements that are part of the Phase I effort are discussed in this section. The remaining hardware elements will be discussed in future updates of this report. Software elements, with the exception of the Data Base Management System (DBMS), and firmware elements are not included in this Phase I effort. The DBMS is covered in Section 8.

Figures 7-2 through 7-6 present the different hardware elements in terms of their Level 2 and higher elements. Subsequent subsections present the state of the art, trends, and projected development for the different levels.

7.1 PROCESSOR/COMPUTER ELEMENTS

Processor/computer elements are discussed in terms of four areas of processing capability that are considered to be representative of the processing technology in general. The four areas, illustrated in Figure 7-2, are microprocessors, minicomputers, large-scale computers (the upper end of the mainframe manufacturers' line), and super-scale computers. Microprocessor technology (Subsection 7.1.1) inputs will be provided in a later version of this report.

7.1.1 Microprocessors

(Not available for Phase I)

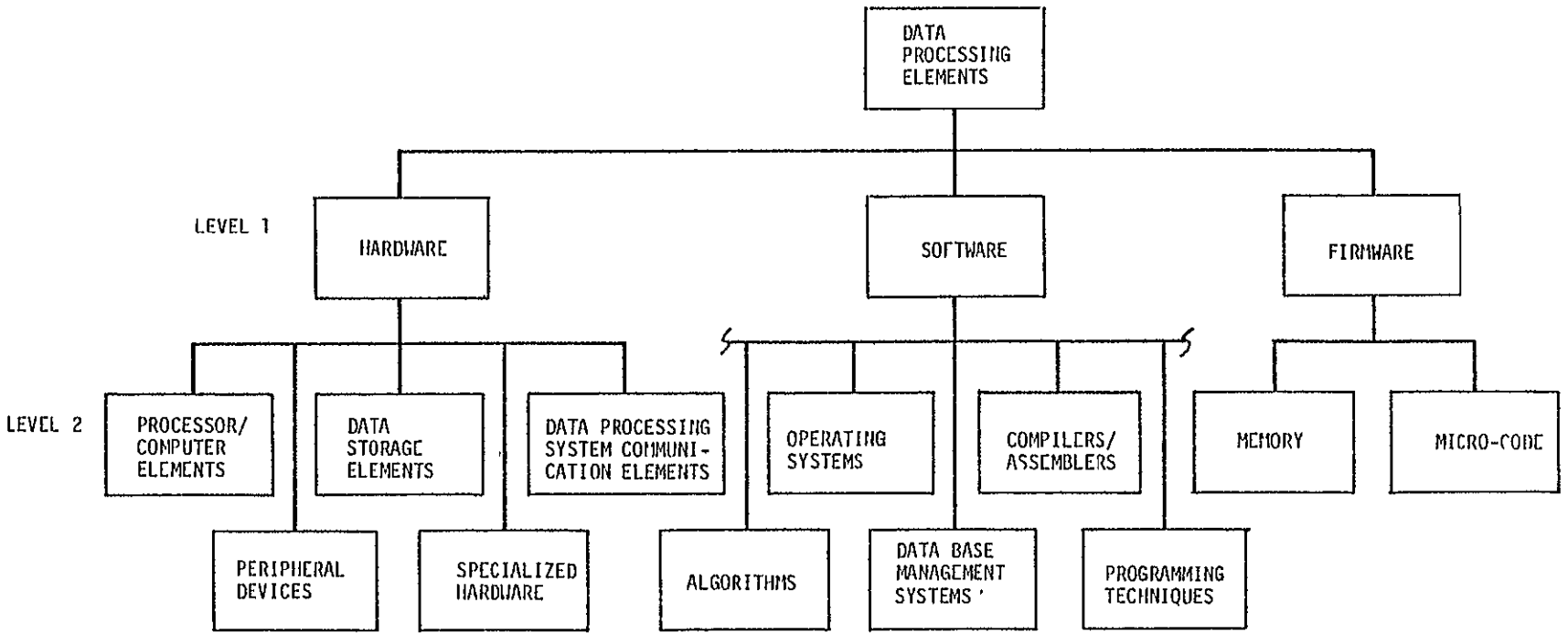

FIGURE 7-1. DATA PROCESSING ELEMENTS

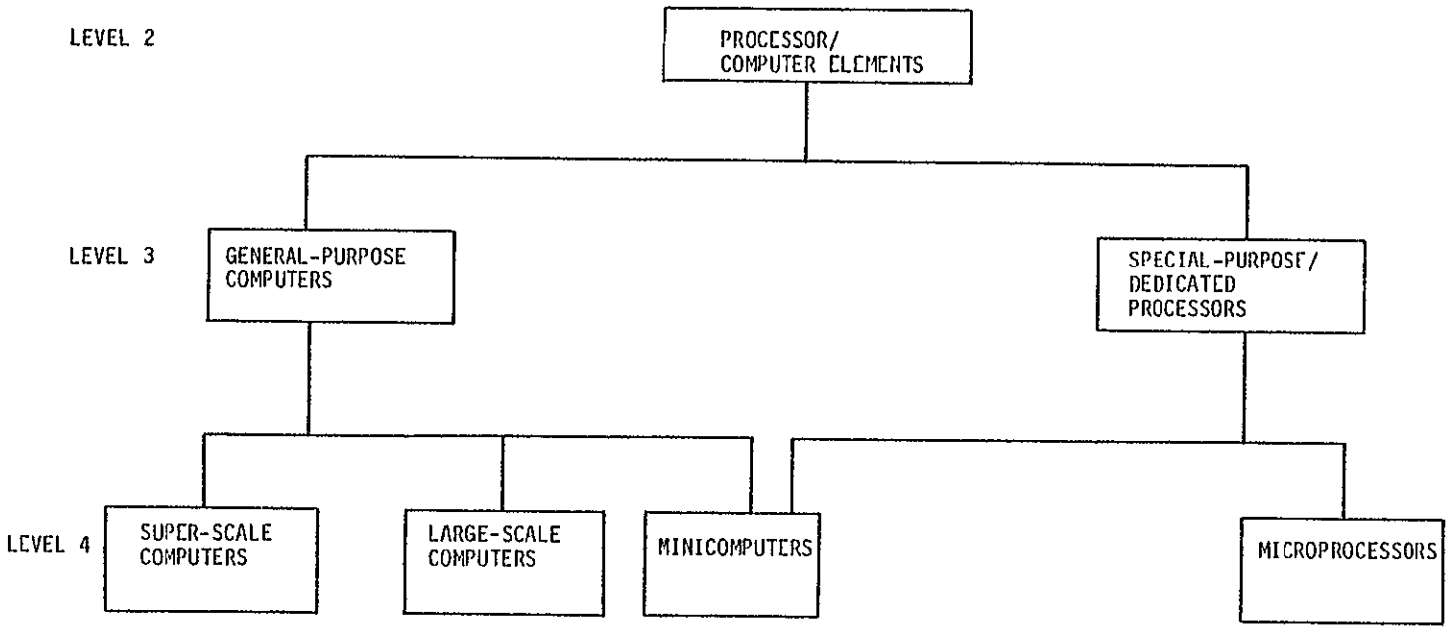

FIGURE 7-2 PROCESSOR/COMPUTER ELEMENTS

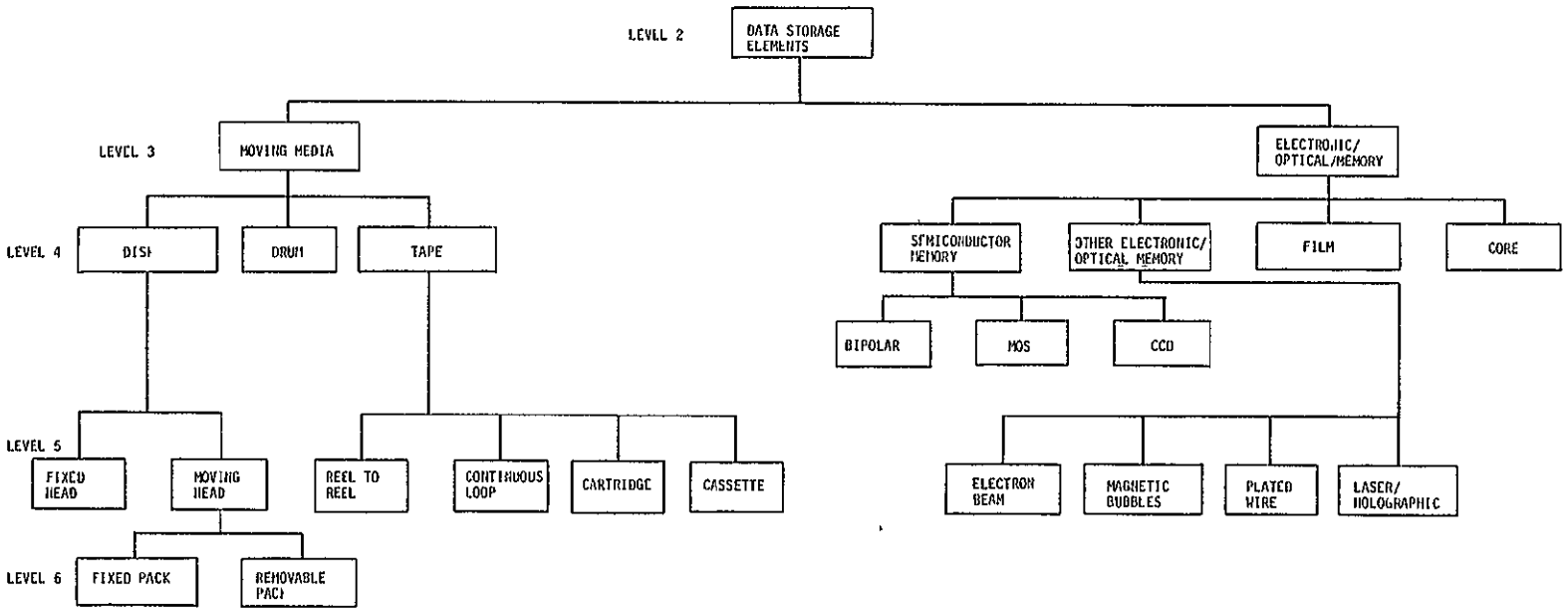

FIGURE 7-3. DATA STORAGE ELEMENTS

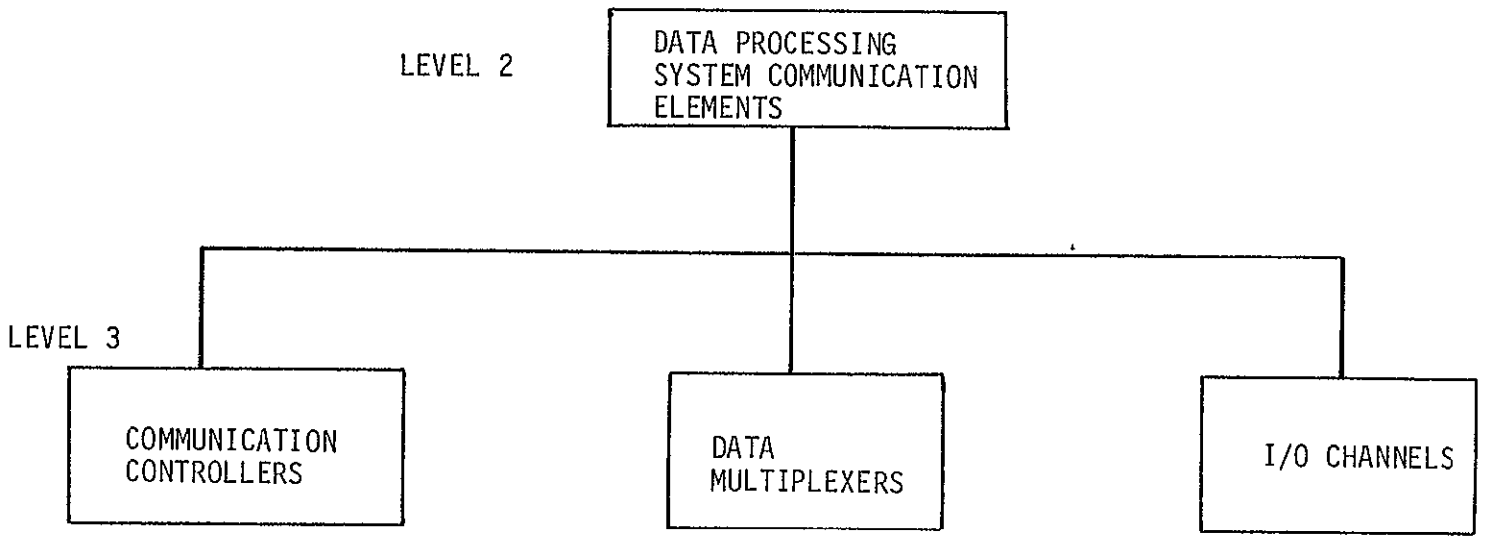

FIGURE 7-4. DATA PROCESSING SYSTEM COMMUNICATION ELEMENTS

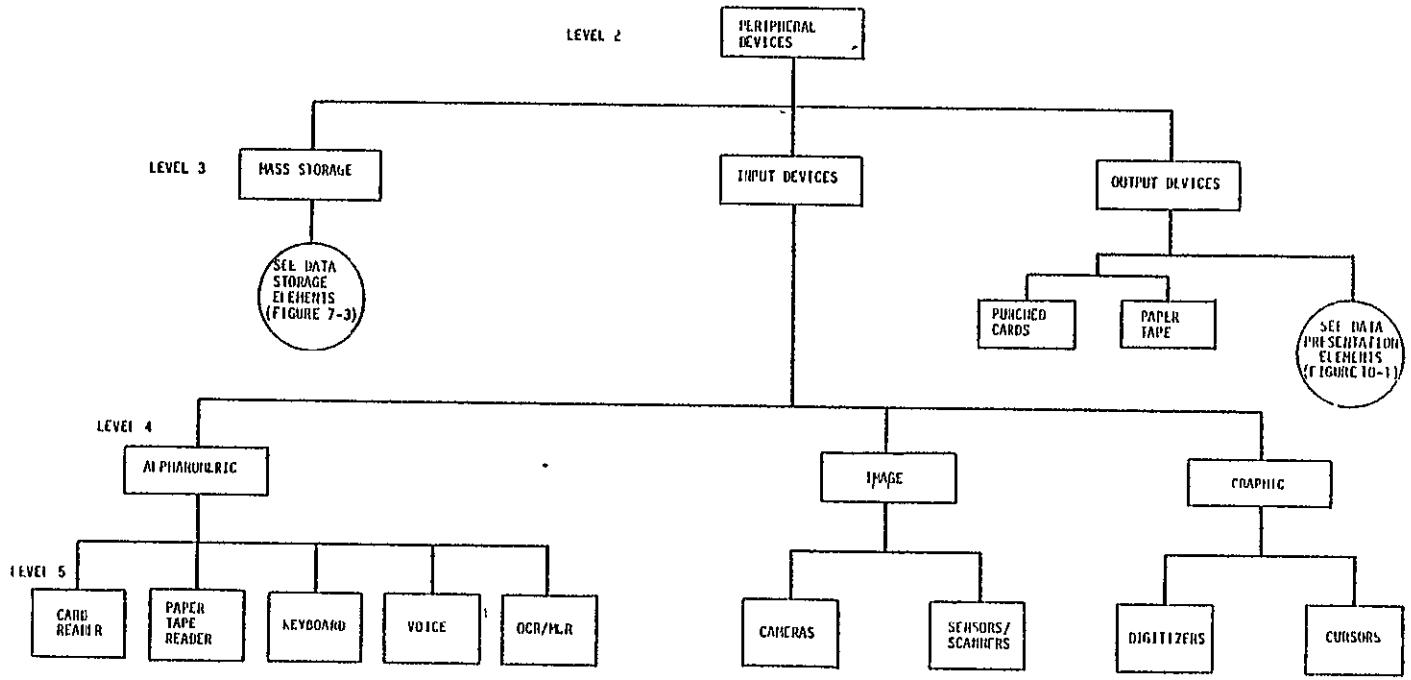

FIGURE 7-5 PERIPHERAL DEVICES

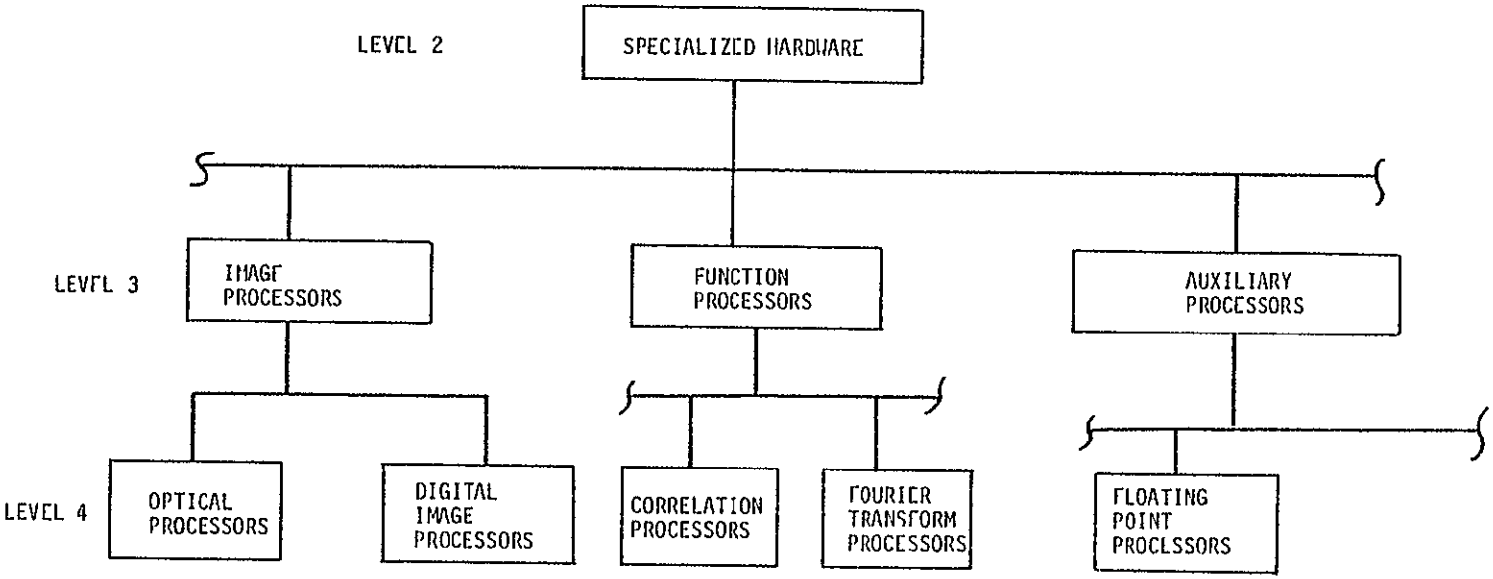

FIGURE 7-6 SPECIALIZED HARDWARE ELEMENTS

7.1.2 Minicomputers

7.1 2.1 State of the Art in Minicomputers - The capabilities of today's minicomputers cover a very broad range in terms of the size and speed of CPU and memory, software capabilities, instruction sets, and related areas. In view of the wide range of capabilities offered, the summary of the basic characteristics of state-of-the-art minicomputers presented in Table 7.1.2.1-1 includes one listing for average or typical minicomputers and one listing for super-minicomputers. The cost of a minicomputer system ranges anywhere from under $1,000 to over $100,000, with computing power increasing rapidly with increasing cost. Many of the super-minicomputers take advantage of bipolar integrated logic circuits, bipolar cache memories, and/or memory interleaving to achieve high performance levels. The average minicomputer uses NMOS technology, sacrificing some speed for lower cost.

Both core and MOS main memories are used in minicomputer systems, with neither technology dominating the other at the present time. Bipolar main memories are optionally available on some systems, providing faster main memories, but the technique is too costly for widespread use. Currently, only a few of the super-minicomputers offer virtual memory capabilities.

Bipolar cache memories and/or memory interleaving are included in several super-minicomputer systems for the purpose of increasing speed by decreasing average memory cycle time. The use of these techniques is particularly significant for those systems still using the slower core main memory. Examples of the effectiveness of these techniques are:

- The 240-nsec bipolar cache memory on the PDP-11/70 reduces the 980-nsec core memory cycle time to an average of 400 nsec.
- Memory interleaving and dual instruction look-ahead on the Interdata 8/32 reduce the 750-nsec core memory cycle time to an average of 300 nsec.

TABLE 7.1.2 1-1. STATE OF THE ART IN MINICOMPUTERS

CHARACTERISTICS	AVERAGE MINICOMPUTER	SUPER-MINICOMPUTER
CPU		
Word Length (bits)	16	16 or 32
Type	NMOS	TTL
Cycle Time (μsec)	0.250 to 0.400	0.160 to 0.300
Number of Directly Addressable Words	256 to 32K	32K to 1,024K
Add Time (μsec)	1 to 3	0.3 to 0.7
Main Memory		
Type	Core or NMOS	Core or NMOS
Cycle Time (μsec)	0.8 to 1.2, 0.5 to 0.7	0.5 to 0.98, 0.2 to 0.7
Minimum Capacity (words)	4K to 32K	16K to 64K
Maximum Capacity (words)	64K to 256K	128K to 4M
I/O Maximum Rate (words/sec)	1M to 2M	1M to 6.67M
Software		
Assemblers	Assembler	Assembler, macroassembler
Compilers	FORTRAN, BASIC	FORTRAN, BASIC, COBOL, RPG
Operating Systems	Batch, real-time	Batch, real-time, time-sharing, interactive
Number of Instructions	100 to 150	120 to 300
Cost of Basic System (CPU, power supply, front panel, and minimum memory in a chassis)	$5,000 to $20,000	$20,000 to $60,000
MIPS	0.17 to 0.50	0.7 to 1.5

TABLE 7 1.2 1-1 - Concluded

CHARACTERISTICS	AVERAGE MINICOMPUTER	SUPER-MINICOMPUTER
Physical Characteristics		
Volume (in^3)	4500	50,000
Voltage (Vac)	115 at 60 Hz or 220 at 50 Hz	115 at 60 Hz or 220 at 50 Hz
Operating Temperature Range (°C)	0 to 50	0 to 50
Humidity Tolerance (%)	0 to 95	0 to 95
MTBF (hr)	NA	NA
Comments		Many newer systems use bipolar cache memories or memory interleaving.

System reliability is enhanced through the use of memory parity checking, storage protection, and LSI logic circuits. LSI circuits, used in a majority of minicomputers, make the CPUs smaller, faster, and inherently more reliable. Parity checking of memory words and storage protection are either optional or standard on most of the super-minicomputers and on many of the smaller ones. A few systems even include an error-correcting capability for their main memory.

The instruction sets available on the minicomputers vary greatly, both in size and complexity. The instruction sets of most of the super-minicomputers now include hardware multiply/divide and hardware floating point arithmetic, either as optional or standard equipment. Availability of control storage on super-minicomputer systems in the form of ROM, PROM, or WCS (writable control storage) is also widespread, allowing the vendor and/or user to tailor the minicomputer's internal processing capabilities to better meet his needs. User-accessible microprogrammability through WCS greatly increases the flexibility of the system.

7.1.2.2 Trends in Minicomputers - During the past decade, the capabilities of minicomputers have increased steadily while their costs per MIPS have decreased. Technological and manufacturing innovations will continue these trends over the next decade, as illustrated graphically in Figures 7.1.2.2-1 through 7.1.2.2-3. Super-minicomputers will rival far more costly medium-scale computers in terms of power and flexibility. Increased use of microprogrammed logic will enhance the flexibility of minicomputers in general. As a result of these trends, there will be an ever-widening market for these small, economical, and surprisingly fast computers. Although most minicomputers are now used in process control and laboratory instrumentation, increasing emphasis is being placed on their use in distributed processing systems and in conventional business data processing applications. Primarily because of the lack of sophisticated software, minicomputers are really just beginning to make a significant impact in the business world. However, there is a definite movement by minicomputer manufacturers toward the development of overall systems, with the computer mainframe, peripherals, and sophisticated software all provided and working together to meet user needs effectively. This movement will attract the potentially very large market of business data processing users.

There is a clear-cut industry trend toward the use of LSI logic circuitry in minicomputers. NMOS and I^2L techniques are directly competitive and likely to coexist over the next decade for low- and medium-speed applications where a minimum number of chips and/or cost are of great importance (Ref. 7-2). Use of TTL and ECL circuits will be restricted to high-performance systems, where their cost can be justified.

The use of LSI logic circuits makes the CPUs smaller, faster, and inherently more reliable. The use of error correcting codes in minicomputer memory systems will expand during the next decade to further increase system reliability. Additionally, redundancy in installed systems will be utilized for the purpose of increased reliability.

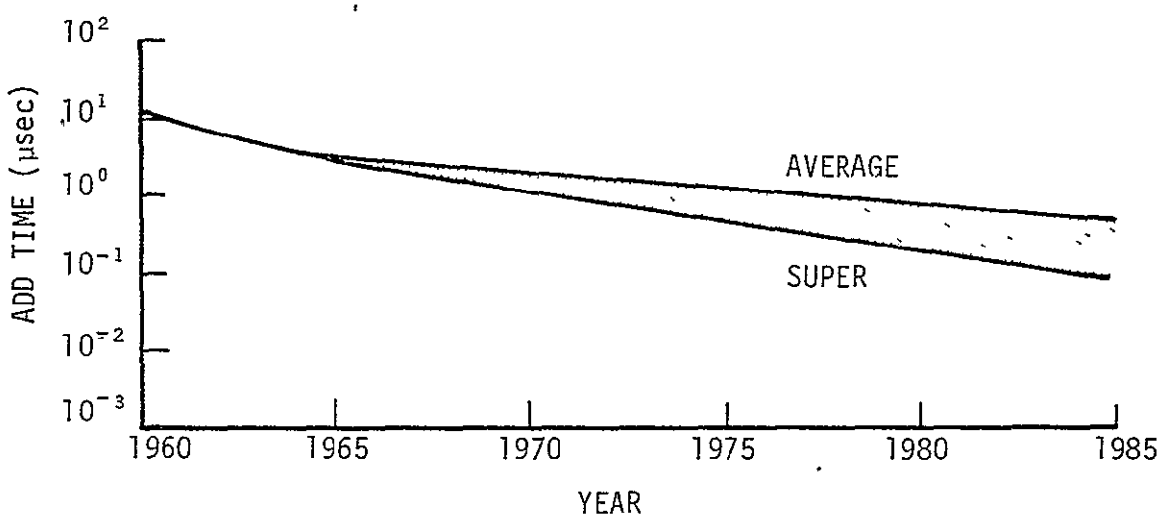

FIGURE 7.1.2.2-1. MINICOMPUTER ADD TIME TRENDS (REF. 7-1)

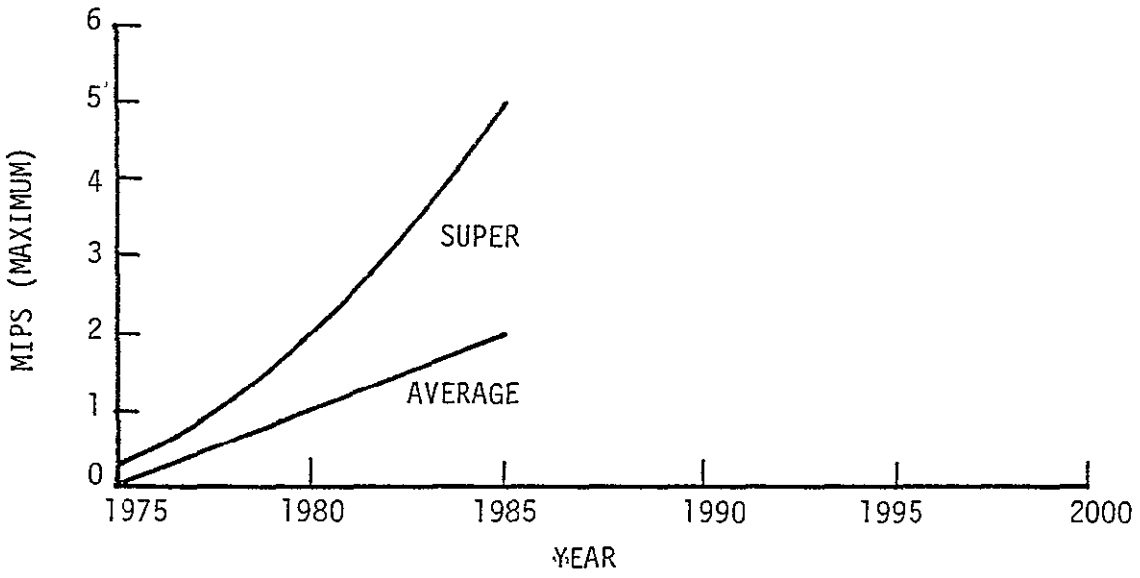

FIGURE 7.1 2 2-2. MINICOMPUTER INSTRUCTION EXECUTION RATE TRENDS

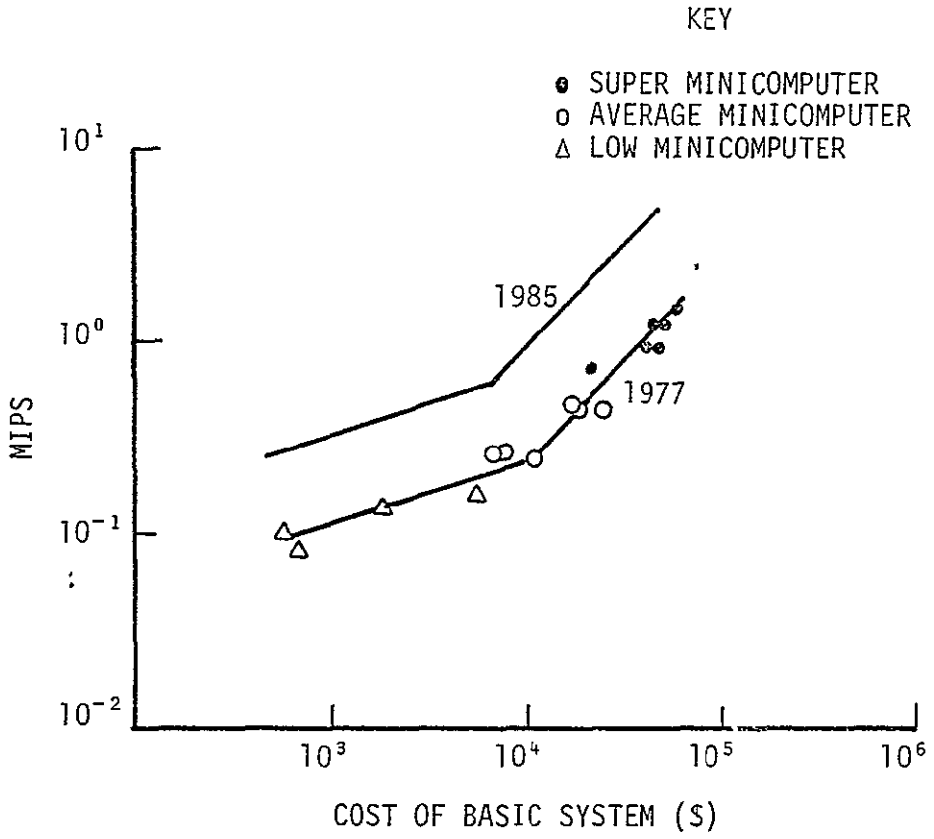

FIGURE 7.1 2.2-3. MINICOMPUTER COST TRENDS

Although bipolar main memories exist in some minicomputer systems and core main memories dominate the installed base of minicomputers, the trend is clearly toward the cheaper MOS technology. The continued demand for higher performance at a lower cost will bring MOS main memories into dominance. Main memory sizes will continue to increase. Virtual and cache memories will become standard on super-minicomputers and optional or standard on most average minicomputers.

7.1.2.3 Projected Developments in Minicomputers - Improvements in LSI logic circuits and semiconductor memories will occur during the next decade as a result of advancements in fabrication processes and photolithographic processes. Of major importance will be research into the use of electron beams. These improvements will be reflected in improvements in minicomputers in many areas, including:

- CPU speed
- Main memory size and speed
- Cost
- Physical size.

Tables 7.1.2.3-1 and 7.1.2.3-2 summarize the projected characteristics of minicomputers in 1980 and 1985, respectively. By the early 1980s, a complete minicomputer system chip will appear, including a 16-bit CPU, 32 kbits of memory, and simple I/O interfaces, with a manufacturing cost under $10 (Ref. 7-2). The cost of minicomputer systems utilizing these chips will be a function of the software capabilities provided with the system since the hardware cost will be practically negligible.

The minicomputer of 1980 and 1985 will be able to support a fully capable data processing system, with ease of use in interactive applications being the primary design consideration in many machines (Ref. 7-3). This will force the typical minicomputer of 1985 to have a large main memory and a virtual operating system. By the early 1980's, the use of hierarchical memory systems will be aided by the introduction of low-cost CCD-based or bubble memories between main memory and disk storage. Space and power requirements will drop by 1/100 in the 1980-1985 timeframe.

As the market addressed by minicomputers widens to include distributed processing and business data processing to a larger extent, greater flexibility of the basic minicomputer will be needed. The implementation of the instruction set in microprogrammed hardware rather than hardwired combinatorial logic will become more prevalent to provide this flexibility.

TABLE 7.1 2.3-1. PROJECTED TECHNOLOGY FOR MINICOMPUTERS, 1980

CHARACTERISTICS	AVERAGE MINICOMPUTER	SUPER-MINICOMPUTER
CPU		
Word Length (bits)	16	16 or 32
Type	NMOS, some I^2L	TTL or ECL
Cycle Time (μsec)	0.200 to 0.300	0.150 to 0.250
Number of Directly Addressable Words	NA	NA
Add Time (μsec)	0 85	0 22
Main Memory		
Type	Core or NMOS	NMOS
Cycle Time (μsec)	NA, 0.300 to 0.420	0.120 to 0.420
Minimum Capacity (words)	8K to 64K	32K to 128K
Maximum Capacity (words)	128K to 512K	256K to 8M
I/O Maximum Rate (words/sec)	NA	NA
Software		
Assemblers	Assembler, macroassembler	Assembler, macroassembler
Compilers	NA	NA
Operating Systems	NA	NA
Number of Instructions	NA	NA
Cost of Basic System (CPU, power supply, front panel, and minimum memory in a chassis)	$7,000 to $18,000	$28,000 to $56,000
MIPS	0 6 to 1.0	1.5 to 2

TABLE 7.1.2.3-1 - Concluded

CHARACTERISTICS	AVERAGE MINICOMPUTER	SUPER-MINICOMPUTER
Physical Characteristics		
Volume (in^3)	3,000	30,000
Voltage (Vac)	115 at 60 Hz or 220 at 50 Hz	115 at 60 Hz or 220 at 50 Hz
Operating Temperature Range (°C)	0 to 50	0 to 50
Humidity Tolerance (%)	0 to 95	0 to 95
MTBF (hr)	NA	NA
Comments	Virtual memory and cache memory on some systems	Virtual memory and cache memory on many systems

TABLE 7.1.2.3-2. PROJECTED TECHNOLOGY FOR MINICOMPUTERS, 1985

CHARACTERISTICS	AVERAGE MINICOMPUTER	SUPER-MINICOMPUTER
CPU		
Word Length (bits)	16 or 32	32
Type	NMOS or I^2L	TTL or ECL
Cycle Time (μsec)	0.150 to 0.200	0.100 to 0.150
Number of Directly Addressable Words	NA	NA
Add Time (μsec)	0.56	0.1
Main Memory		
Type	NMOS	NMOS or Bipolar
Cycle Time (μsec)	0.200 to 0 280	0 080 to 0.280, 0.055 to 0.085
Minimum Capacity (words)	16K to 128K	64K to 256K
Maximum Capacity (words)	256K to 1M	1M to 16M
I/O Maximum Rate (words/sec)	NA	NA
Software		
Assemblers	Assembler, macroassembler	Assembler, macroassembler
Compilers	NA	NA
Operating Systems	NA	NA
Number of Instructions	NA	NA
Cost of Basic System (CPU, power supply, front panel, and minimum memory in a chassis)	$10,000 to $15,000	$40,000 to $50,000
MIPS	1.0 to 1.5	4 to 5

TABLE 7.1.2.3-2. - Concluded

CHARACTERISTICS	AVERAGE MINICOMPUTER	SUPER-MINICOMPUTER
Physical Characteristics		
Volume (in^3)	50	500
Voltage (Vac)	115 at 60 Hz or 220 at 50 Hz	115 at 60 Hz or 220 at 50 Hz
Operating Temperature Range (°C)	0 to 50	0 to 50
Humidity Tolerance (%)	0 to 95	0 to 95
MTBF (hr)	10,000	10,000
Comments	Virtual memory and cache memory on many systems	Virtual memory and cache memory on most systems

7.1 3 Large-Scale Computers

7.1 3.1 State of the Art in Large-Scale Computers - A summary of the basic characteristics of the most powerful large-scale computers is given in Table 7.1.3.1-1. The cost of a basic system (CPU, I/O channels, system console, power distribution unit, and minimum amount of memory) varies between $3 million and $5 million, with cost generally increasing with increasing speed and computing power. The high performance levels of the current large-scale systems, especially their speeds, have been achieved through the use of integrated logic circuitry, semiconductor main memories, buffer or cache memories, instruction look-ahead, concurrent CPU and I/O processing, and multiprocessor systems. Advancements in these areas have reduced significantly the price/performance ratio for large-scale systems, as reflected in the low cost (0 5¢) to perform 100,000 computations.

Although discrete components still appear in a very few CPUs, most now utilize integrated circuits with ECL technology. The result has been smaller, faster, inherently more reliable CPUs. Some models incorporate microprogrammed control logic for added flexibility.

Core main memories have not been eliminated, but the use of semiconductor main memories is now predominant. As a result, the physical volume occupied by the main memory in a system has decreased greatly Although both bipolar and MOS techniques are used, for most applications the MOS technique is the more cost-effective The major advantage of bipolar over MOS is greater speed, but this is obtained at the expense of higher cost, greater power consumption, higher heat dissipation, and lower packing densities. The current large-scale computers have maximum main memory capacities up to 16 Mbytes. Virtual storage capabilities, available in about half of these computers, further enlarge the memory capacity, from the user's viewpoint.

Buffer or cache memories are included in many of the large-scale computers. This relatively small amount of very fast memory is provided

TABLE 7 1.3 1-1 STATE OF THE ART IN LARGE-SCALE COMPUTERS

CHARACTERISTICS	
CPU	
Word Length (bits)	32 or 48 or 60
Type of Logic Circuitry	ECL
Cycle Time (nsec)	25 to 80
Add Time:	
Fixed Point (μsec)	0.055 to 0 13
Floating Point (μsec)	0.110 to 0.7
MIPS	10 to 25
Main Memory	
Type	MOS or Core
Cycle Time (nsec)	300 to 500, 750 to 900
Minimum Capacity (bytes)	1M to 2M
Maximum Capacity (bytes)	4M to 16M
Volume (ft^3/Mbyte - MOS)	0.063
Cache Memory	
Type	TTL or ECL
Cycle Time (nsec)	32 to 80
Capacity (bytes)	16K to 32K
Virtual Memory	Some systems
Maximum I/O Transfer Rate (bytes/sec)	4M to 18M
Cost of Basic System (CPU, I/O channels, system console, power distribution unit, and minimum memory)	$3M to $5M
MTBF (hr)	150 to 250
Number of Instructions*	100 to 200
Cost per 100,000 Computations (¢)	0.5

*Instruction sets are very comprehensive, including capabilities for fixed and floating point decimal and integer arithmetic and string manipulations, among others.

to increase the speed of the computer. The most frequently referenced memory items are kept in this fast memory, which causes a decrease in the average memory reference time. For the same purpose, instruction look-ahead is used, either in conjunction with or instead of buffer memory. It increases CPU utilization by minimizing the number of memory references required to access sequences of instructions.

All of the state-of-the-art, large-scale computers have separate I/O processors that operate independently of the CPU. This allows concurrent data transmission and CPU execution, yielding an increase in system speed. Multiprocessing, the use of more than one CPU in the system, achieves even greater increases through concurrent execution by multiple CPUs. Several of the current large-scale computers are designed to operate in a multiprocessing environment. The pipeline structure found in some CPUs lies at an intermediate level, allowing several instructions to be in some phase of execution concurrently within a single CPU.

More emphasis has been placed on reliability in the current large-scale systems. The use of integrated circuits makes the logic circuitry inherently more reliable. Algebraic codes incorporated in the data stream increase the reliability of data transmissions. Code bits within each memory word allow correction of all single-bit errors and detection of all double-bit errors, as well as most other multiple-bit errors. Extensive parity checking is performed on instructions and I/O data. Most systems have an automatic instruction re-try to correct transient errors. Fail-soft capabilities are being emphasized, enabling a system to remain in operation at a reduced level of performance when failures occur. As a result, system MTBF of 150 to 250 hr is now typical.

The instruction sets of the large-scale computers are generally very comprehensive. Most repertoires include instructions for data movement, shifting, logic and control operations, binary arithmetic, variable-length fixed and floating point decimal arithmetic, and bit and byte

string manipulation. The most powerful computers permit floating point and integer operands of single and double precision to be combined freely, and also include vector mode operations

7.1.3.2 Trends in Large-Scale Computers - During the past decade, the capabilities or large-scale computers have increased rapidly while their costs per MIPS have decreased. Technological and manufacturing innovations will continue these trends over the next decade, as illustrated graphically in Figures 7.1 3.2-1 and 7.1.3.2-2 Although the graph depicting MIPS as a function of year (Figure 7.1.3 2-1) was originally produced in 1972, its predictions for current large-scale computers are very accurate, and those for large-scale computers of the 1980's are consistent with more recent predictions. The historical 12 to 15% annual price/performance improvement will continue as the result of achievements in logic circuits, main memories, and mass storage (Ref. 7-5). Reflecting this trend, the cost to perform 100,000 computations will continue to decline, as illustrated graphically in Figure 7.1.3.2-3

There is a definite trend toward the use of integrated logic circuitry in large-scale computers. In the future, increasing numbers of systems will incorporate CPUs built with integrated circuits, especially ECL and CML circuits. Denser logic chips will be achieved during the next decade through research into scanning techniques, projection techniques using electron beam technology, and X-rays. Improved system speed and reduced system power dissipation will be achieved through the use of these denser chips. The use of microprogrammed control logic will become more pronounced and more sophisticated.

During the next decade emphasis on system reliability will increase. Fault-tolerant design with redundancy at the module level will be aided by the increasing availability of larger and larger LSI devices. There will be continued widespread use of on-line monitoring and diagnostic capabilities with automatic re-try and path switching. The use of error correcting codes in memory systems will grow.

Although core main memories still exist in some large-scale computers, the trend is clearly toward semiconductor main memories. Over the next decade, main memory capacities will continue to increase while their physical dimensions will continue to decrease. These trends are illustrated graphically in Figures 7.1.3 2-4 and 7 1.3.2-5.

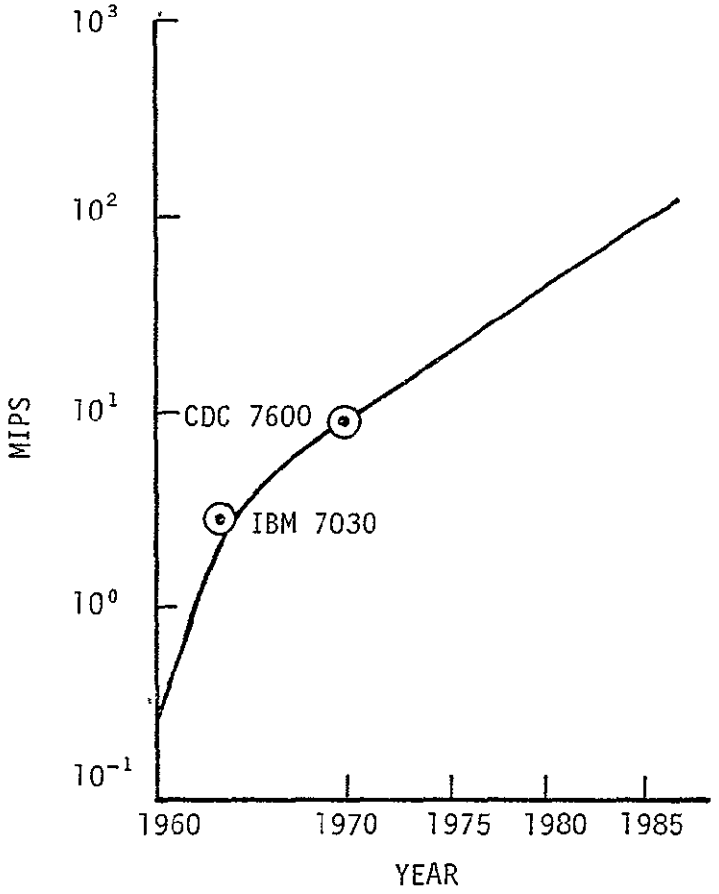

FIGURE 7.1 3.2-1. LARGE-SCALE COMPUTER INSTRUCTION EXECUTION RATE TRENDS (Ref. 7-59)

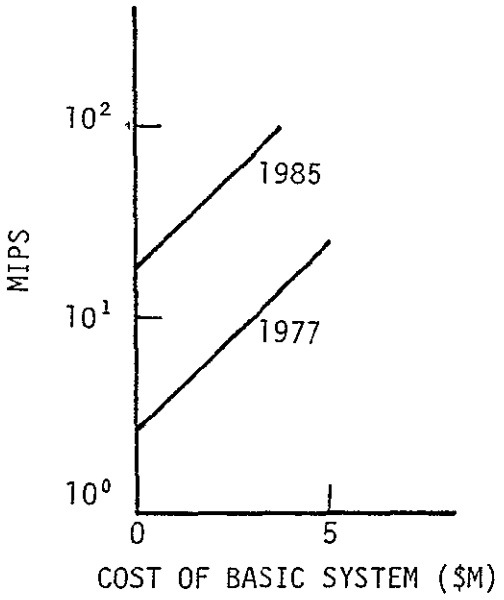

FIGURE 7.1.3 2-2. LARGE-SCALE COMPUTER COST TRENDS

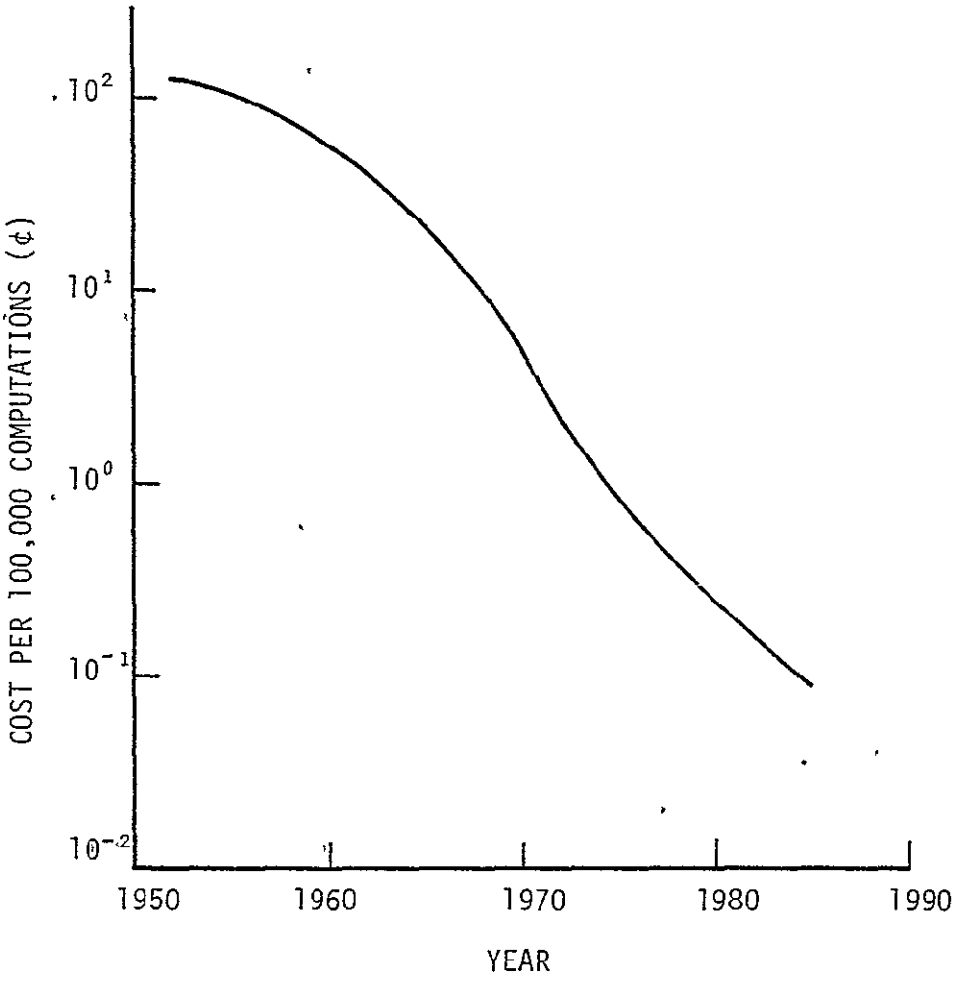

FIGURE 7.1.3.2-3. LARGE-SCALE COMPUTER COST PER 100,000 COMPUTATIONS TRENDS (Ref. 7-4)

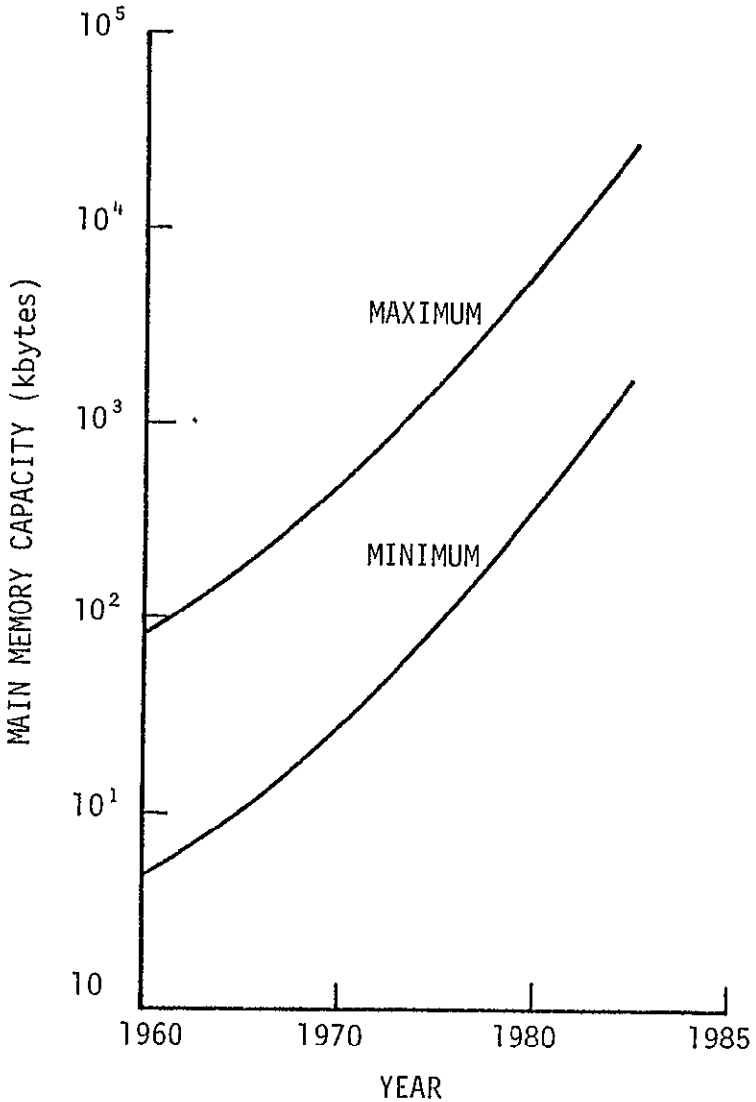

FIGURE 7.1.3 2-4 LARGE-SCALE COMPUTER MAIN MEMORY CAPACITY TRENDS

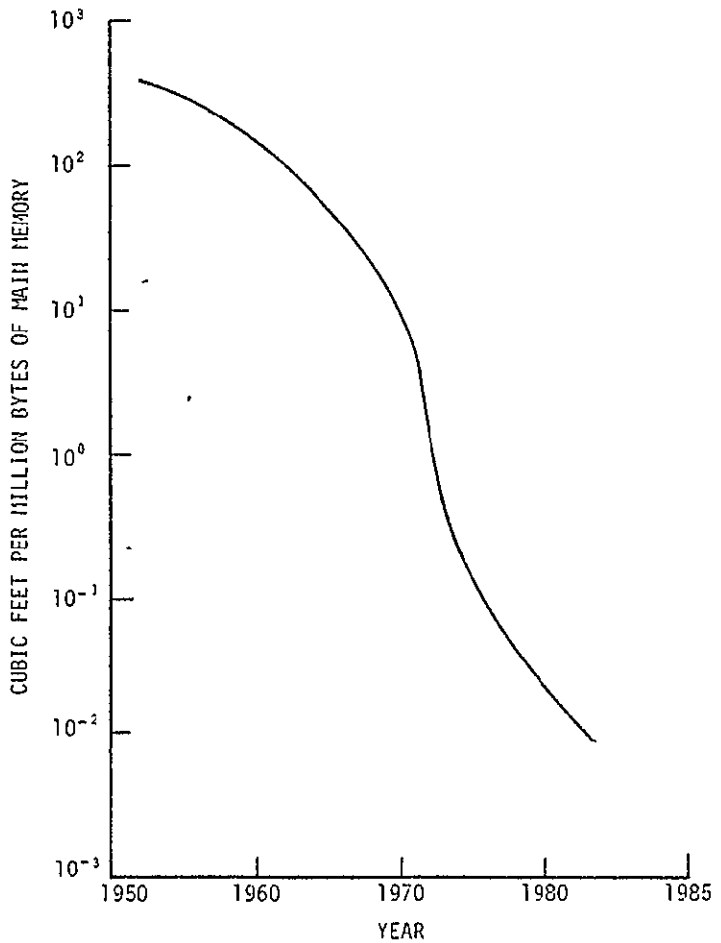

FIGURE 7.1.3 2-5 LARGE-SCALE COMPUTER MAIN MEMORY VOLUME TRENDS (Ref. 7-4)

The desire for ever greater speed will force the continued growth of multilevel hierarchical storage systems. In particular, buffer memories will be included in more large-scale computers and will have larger capacities and smaller cycle times. Virtual storage will become dominant.

The trends in large-scale computing include a move in some applications from single-machine computers toward distributed processing, where dedicated, interconnected processors work on each segment of a task (Ref. 7-6). Much research is being done in this area. Such systems are projected by many experts for applications having specific problems such as speed or data organization. As support for their positions, these experts cite the increasing complexity of the large computer systems, particularly the software required to utilize their vast array of features, and the decreasing cost and increasing capabilities of minicomputers and microprocessors. Although distributed processing currently has progressed only to the first stage, where a small amount of processing has been taken away from the central processing unit, a greater degree of offloading of the CPU can be expected (Ref. 7-7).

7.1.3.3 Projected Developments in Large-Scale Computers - Improvements in LSI logic circuits and semiconductor memories will occur during the next decade (see Section 7.2.1). These improvements will be reflected in improvements in large-scale computers in many areas, including.

- CPU speed
- Main memory size and speed
- Cache memory size and speed
- Cost.

Tables 7.1.3.3-1 and 7.1.3.3-2 summarize the projected characteristics of large-scale computers in 1980 and 1985, respectively. Bipolar logic circuits will continue to be dominant in the CPUs of large-scale computers because speed is more critical than packing density for these machines. Microcoded instruction sets will be used extensively in the 1980's for the purposes of flexibility and protection against plug-compatible devices.

Hierarchical storage systems with larger and faster bipolar buffer memories will be dominant in the large-scale systems of the next decade to aid in achieving desired system performance. The semiconductor main memories of the hierarchy will have capacities up to 256 Mbytes in 1985, while virtual address spaces of 10^{12} bytes are likely by that time. By the early 1980's, low-cost CCD-based or bubble memories will appear in the hierarchy.

Error detection and error correction in memory systems and fault-tolerant circuitry will be used over the next decade to increase the reliability of large-scale systems. Multiple-bit error correction in memory systems will become standard. Dual processors will be included in some systems primarily for the purpose of increased system reliability.

Distributed processing systems will increase in number during the next decade, with increasing amounts of the processing load shifted from the CPU. By 1980, the distributed processing network era will have

TABLE 7 1.3.3-1. PROJECTED TECHNOLOGY FOR LARGE-SCALE COMPUTERS, 1980

CHARACTERISTICS	
CPU	
Word Length (bits)	32 or 48 or 60
Type of Logic Circuitry	ECL
Cycle Time (nsec)	18 to 58
Add Time.	
Fixed Point (μsec)	0.04 to 0.09
Floating Point (μsec)	0.08 to 0 51
MIPS	40 to 45
Main Memory	
Type	MOS
Cycle Time (nsec)	180 to 300
Minimum Capacity (bytes)	3 9M
Maximum Capacity (bytes)	61.6M
Volume (ft^3/Mbyte)	0 024
Cache Memory	
Type	TTL or ECL
Cycle Time (nsec)	26 to 64
Capacity (bytes)	32K to 64K
Virtual Memory	Some systems
Maximum I/O Transfer Rate (words/sec)	NA
Cost of Basic System (CPU, I/O channels, system console, power distribution unit, and minimum memory)	$2.6M to $4 5M
MTBF (hr)	350 to 650
Number of Instructions	NA
Cost per 100,000 Computations (¢)	0.22

TABLE 7.1.3 3-2. PROJECTED TECHNOLOGY FOR LARGE-SCALE COMPUTERS, 1985 (REF. 7-8, 7-9)

CHARACTERISTICS	
CPU	
Word Length (bits)	32 or 48 or 60
Type of Logic Circuitry	ECL
Cycle Time (nsec)	10 to 32
Add Time.	
Fixed Point (μsec)	0 02 to 0.05
Floating Point (μsec)	0.04 to 0.28
MIPS	90 to 100
Main Memory	
Type	MOS or Bipolar
Cycle Time (nsec)	120 to 200, 50 to 100
Minimum Capacity (bytes)	17.4M
Maximum Capacity (bytes)	256M
Volume (ft^3/Mbyte)	0 008
Cache Memory	
Type	ECL
Cycle Time (nsec)	20
Capacity (bytes)	128K to 256K
Virtual Memory	Many systems
Maximum I/O Transfer Rate (words/sec)	NA
Cost of Basic System (CPU, I/O channels, system console, power distribution unit, and minimum memory)	$1.8M to $3 75M
MTBF (hr)	1,500 to 2,500
Number of Instructions	NA
Cost per 100,000 Computations (¢)	0.08

arrived (Ref. 7-4). However, this progress will be in conjunction with, rather than instead of, the evolution of large-scale computers. In addition, many large-scale systems of the next decade will be geared to large data base management operations.

7.1.4 Super-Scale Computers

7.1.4.1 State of the Art in Super-Scale Computers - Computers that execute 50 MIPS or more are generally classified as super-scale computers at the present time. The super-scale computer state of the art encompasses three basic designs. vector or pipeline processors, parallel array processors, and associative array processors. All three types are designed primarily to solve problems that throughput large amounts of data and in which computations are highly parallel, such as weather forecasting, sonar processing, aircraft and missile tracking, air traffic control, and image processing. Although some state-of-the-art multiprocessor systems configured from a small number of large-scale computers might be able to approach the computational power of the super-scale computers, they are better suited to the needs of users with mixed processing needs because of their designs. In these systems, floating point operations are more of an afterthought than a design consideration.

Vector super-scale computers are characterized by a single data stream which passes through a pipeline of sequentially connected processing units. Each processing unit operates on the elements of the data stream sequentially. Once results are first obtained from the pipe, they will be produced at the rate at which it takes a single processor of the pipe to perform one operation. Thus the high instruction execution rates claimed for these computers are based on the assumptions that there is a long string of data, a vector, which needs to be processed by the same sequence of operations, and that these data items can be fetched from memory at speeds corresponding to the processor speed.

A summary of the basic characteristics of state-of-the-art vector super-scale computers is presented in Table 7.1.4.1-1. Although scalar processing capabilities are included in these systems, emphasis is placed on vector processing. It is through the utilization of the vector capabilities that the high instruction execution rates are achieved. The rates included in Table 7.1.4.1-1 are the maximum rates possible. In

TABLE 7.1.4.1-1. STATE OF THE ART IN VECTOR SUPER-SCALE COMPUTERS

CHARACTERISTICS	
CPU	
Word Length (bits)	32 or 64
Type of Logic Circuitry	TTL or ECL
Cycle Time (nsec)	12.5 to 40
Minimum Computation Times.	
64-bit Add (nsec)	12 5 to 20
64-bit Multiply (nsec)	12.5 to 48
64-bit Divide (nsec)	40 to 80
Maximum Vector Result Rate (nsec)	12.5 to 40
MIPS	50 to 80
Memory	
Type	TTL or ECL
Cycle Time (nsec)	50 to 160
Maximum Capacity (words)	1M
Bandwidth (Mwords/sec)	80 to 400
Error Correction	Single error correction on some systems
Virtual Memory	Only on a few systems
Number of Instructions	
Scalar	64 to 177
Vector	64 to 70
Volume (ft^3)	170 to 450
Mainframe Weight (tons)	5 to 20
Cost ($M)	7 5 to 12.5
MTBF (hr)	2.5 to 5 (no memory error correction) 40 to 60 (memory error correction)
Maximum Number of Pipelines	1, 2, or 4

actual applications the rates achieved are one-third to one-half of these maximums. To enable the system to operate near the high vector rates, the vector super-scale computers contain the following features

- Bipolar integrated logic circuits
- Bipolar main memories
- Instruction stack with look-ahead hardware
- Independent I/O processors
- I/O channel buffering capabilities.

The newest systems use ECL logic circuits and memories because of the speed advantage of this technology over other semiconductor technologies. The high main memory speeds and large main memory capacities enable these systems to handle the large amounts of data inherent in the problems they address at rates commensurate with the vector rates. Virtual storage is not included in most of the vector super-scale computers because of its cost in terms of memory speed and addressing overhead All of these systems do include separate I/O processors operating independently of the CPU. This feature allows concurrent data transmission and CPU execution, yielding an increase in system speed. In addition, these systems usually have a separate large-scale mainframe acting as a host to the vector super-scale computer. This configuration off-loads most of the control tasks and some of the sequential tasks from the vector computer, allowing the vector computer to execute primarily in its fast vector mode.

A parallel array processor is a single-instruction-stream, multiple-data-stream computer. It contains many independent identical processing elements, each operating on a separate data stream but all under control of the single instruction stream. An associative array processor is just a special class of parallel array processor in which the processing elements are simple, serial-by-bit units connected to an associative memory, one unit per row of memory. Parallelism is achieved by performing the same operation on all words of the associative memory concurrently. The high instruction execution rates claimed for array processor super-scale computers are based on the concurrent operation of all processing elements, which in turn is dependent on the availability of very large

amounts of data requiring identical processing. To an even greater extent than in vector super-scale computers, the performance of these computers is seriously degraded by the need for scalar processing.

A summary of the basic characteristics of state-of-the-art parallel and associative array processors is presented in Table 7.1.4 1-2. The instruction execution rates included in the table are the maximum rates possible. In actual applications, the rates achieved are one-third to one-half of these maximums. The newest systems use ECL logic circuits and processing element memories because of the speed advantage of this technology over other semiconductor technologies. However, the individual processing elements are not extremely powerful and do not have large amounts of memory. It is the concurrent operation of these processing elements that yields a high performance system. A large-scale mainframe is included in the system to execute control tasks and many of the sequential tasks, allowing the processing elements to operate in parallel as much as possible.

Super-scale computers are relatively unreliable because they include massive amounts of hardware concentrated in one place. A number of features have been included in both types of systems to aid reliability, including

- Error-correcting memories
- Error correction on data transfers
- Automatic instruction re-try
- Integrated logic circuits

Array processors have the added advantage that an element failure can usually be tolerated and frequently even ignored in the kinds of problems addressed by them.

Software support for the super-scale computers is fairly limited. It generally includes an operating system, an assembly language, FORTRAN or a FORTRAN-like higher-level language, a library of mathematical routines, and a general utilities package. The operating system overhead is kept as low as possible because computers designed for heavy computational

TABLE 7 1 4.1-2 STATE OF THE ART IN ARRAY SUPER-SCALE COMPUTERS

CHARACTERISTICS	PARALLEL	ASSOCIATIVE
Processing Elements		
Number per System	64 to 288	256 per module, up to 32 modules
Word Length (bits)	32 or 64	32
Type of Logic Circuitry	ECL	NA
Cycle Time (nsec)	75 to 80	NA
Processing Element Data Memory		
Maximum Capacity	2K words	256 bits/processing element; 64 kbits/module
Type	NMOS or ECL	NMOS
Cycle Time (nsec)	100 to 240	200
Error Correction	Yes	Yes
MIPS	1 to 4	NA
Program and Data Memory*		
Maximum Capacity (words)	32K	4K**
Type	NMOS	NMOS
Cycle Time (nsec)	200	200
Error Correction	Yes	Yes
System MIPS	100 to 500	53.3/module***
System Up-Time (hr/5-day wk)	60	NA
System Cost ($M)	10	0.7 to 3 5

*On some machines
**Also 32K words of bulk core memory
***Word search operations

workloads function most efficiently under these circumstances Much work is needed in the area of software support, especially support to allow better utilization of the vector or parallel capabilities of the super-scale computers.

7.1.4 2 Trends in Super-Scale Computers - Historically, the performance levels of super-scale computers have increased rapidly while their costs have increased at a slower rate, resulting in a continuous price/performance improvement. Technological and manufacturing innovations in the areas of logic circuits, main memories, and mass storage will continue these trends over the next decade, as illustrated graphically in Figures 7.1.4.2-1 through 7.1.4.2-4. The curves in these figures, as well as all other curves contained in this section, are intended to illustrate trends only and should not be used to extract numbers for any particular year. Because of the limited market for super-scale computers and their high cost and level of complexity, the lead time for the production of a new system is long. As a result, improvements occur in jumps spaced several years apart rather than in small increments every year or so. For a given year, the curves indicate what the capabilities would probably be if a new system were to be introduced that year. It is probable that only one new generation of array super-scale computers will appear during the 1980-1985 timeframe.

Emphasis will be placed on larger memories and faster execution in the super-scale computers of the next decade, because the same problems will continue to be addressed and the quality of their solution depends on the number of data points considered and the number of computations performed. Figures 7.1.4.2-5 and 7.1.4.2-6 illustrate graphically the expected growth in memory capacities. ECL technology will continue to be used for both memories and logic circuits because of its speed advantage. Current Mode Logic (CML) circuits will also be utilized. Denser logic chips and memory chips will be achieved during the next decade through research into scanning techniques, projection techniques using electron beam technology, and X-rays. Improved logic and memory speeds will be achieved through the use of these denser chips, yielding improved system performance. Array processor systems will include larger numbers of processing elements to further increase system performance.

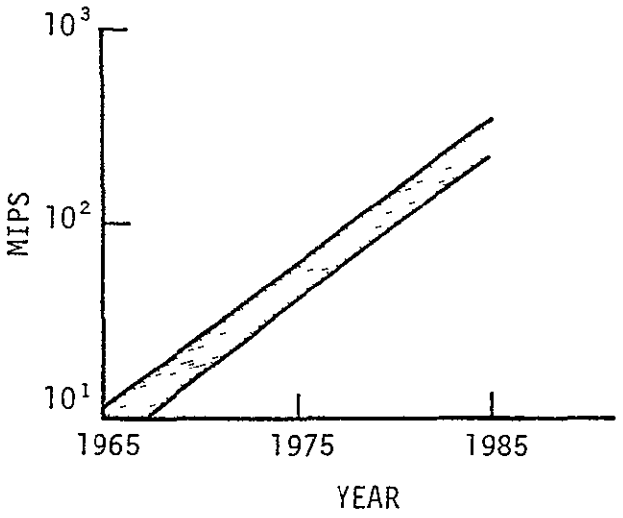

FIGURE 7 1.4 2-1. VECTOR SUPER-SCALE COMPUTER INSTRUCTION EXECUTION RATE TREND

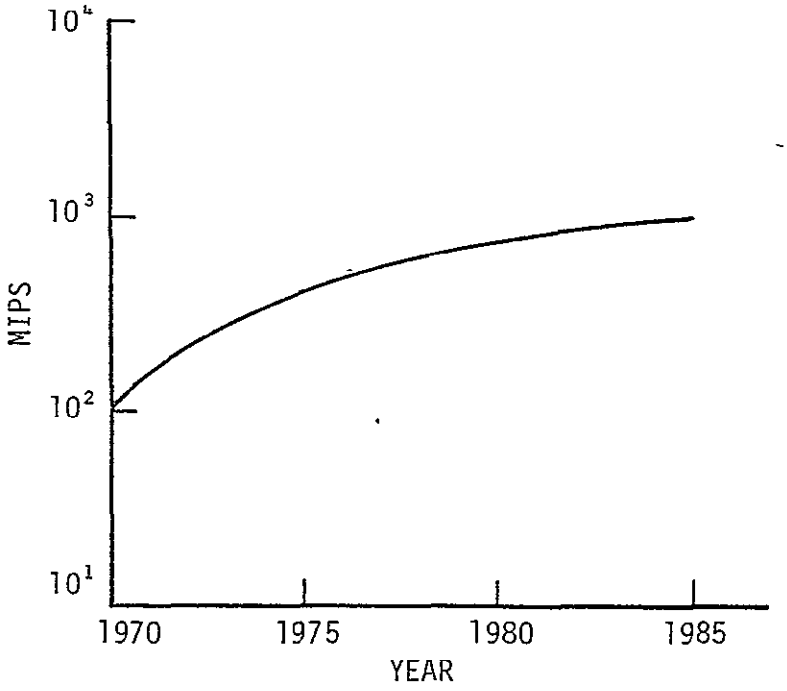

FIGURE 7.1 4 2-2 ARRAY SUPER-SCALE COMPUTER INSTRUCTION EXECUTION RATE TREND

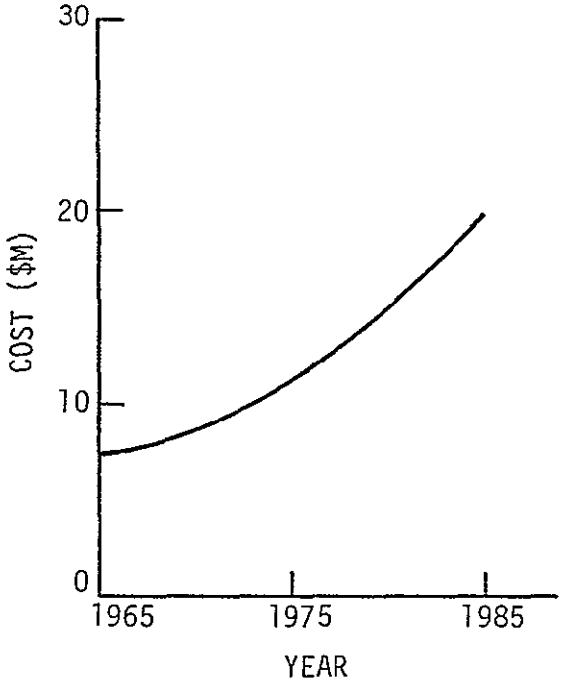

FIGURE 7 1 4 2-3 VECTOR SUPER-SCALE COMPUTER COST TREND

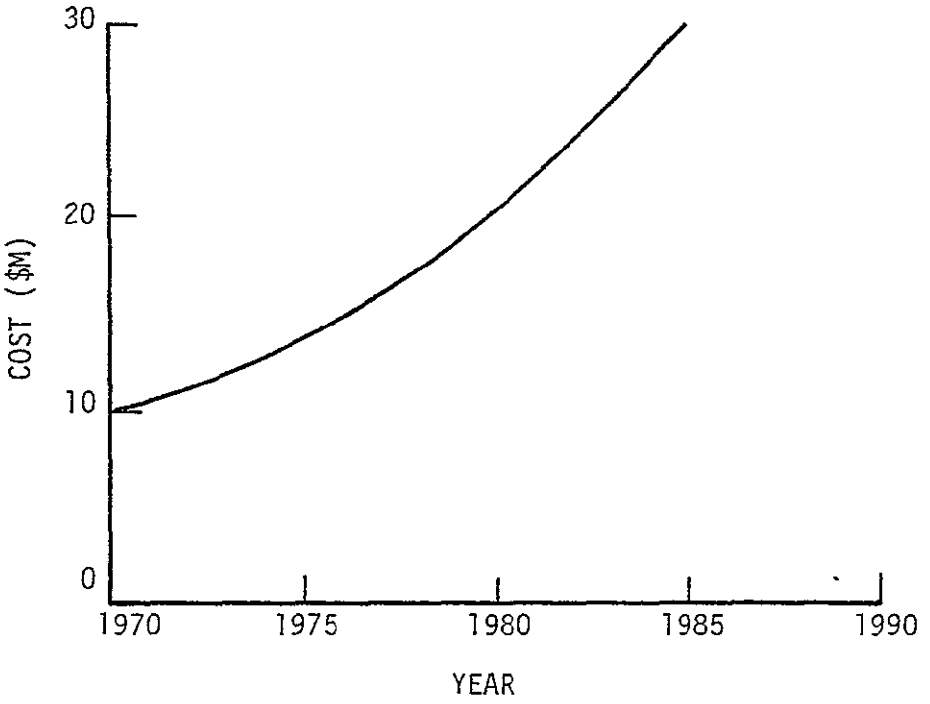

FIGURE 7.1.4.2-4. ARRAY SUPER-SCALE COMPUTER COST TREND

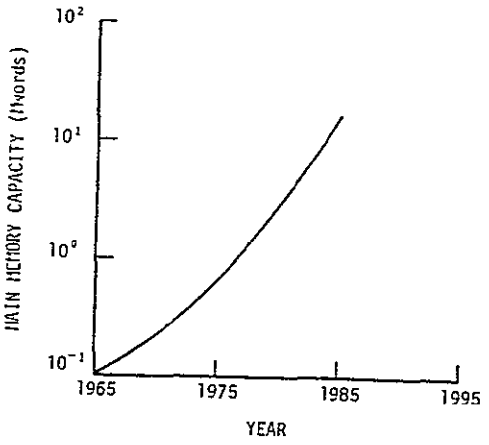

FIGURE 7.1.4 2-5. VECTOR SUPER-SCALE COMPUTER MAIN MEMORY CAPACITY TREND

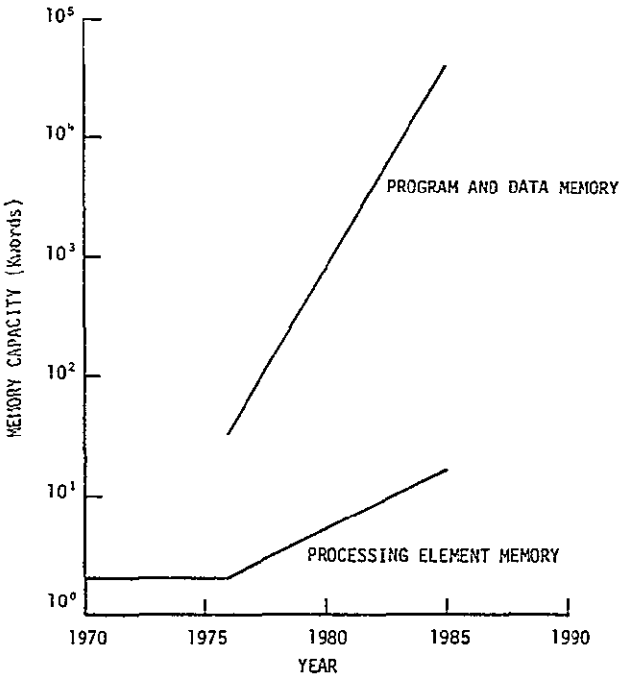

FIGURE 7.1.4.2-6. ARRAY SUPER-SCALE COMPUTER MEMORY CAPACITY TRENDS

During the next decade, emphasis on system reliability will increase. More sophisticated error correcting codes will be used. There will be widespread use of on-line monitoring and diagnostic capabilities with automatic re-try.

Major advances are needed in software support for super-scale computers Problem programming for a parallel or vector machine must be made reasonably straightforward and simple so that the system can be more fully utilized. For advances to occur, a better understanding of the hardware of the super-scale computers must be developed. Emphasis will be placed on the development of this understanding, and of software, during the next decade.

7.1.4.3 Projected Developments in Super-Scale Computers - Improvements in LSI logic circuits and semiconductor memories will occur during the next decade (see Section 7.2 1). These improvements will be reflected in improvements in super-scale computers in many areas, including

- Processing speed
- Memory capacity and speed
- Reliability
- Price/performance.

Tables 7.1.4.3-1 and 7.1.4.3-2 summarize the projected characteristics of vector super-scale computers in the early and mid 1980's, respectively. Table 7.1.4.3-3 summarizes the projected characteristics of array super-scale computers in the 1980-1985 timeframe. The instruction execution rates presented in these tables are conservative projections. The rates that will be achieved in super-scale computers of the next decade will depend on two things: on the extent to which the parallel or vector capabilities are increased, which depends primarily on hardware advances, and on the extent to which the parallel or vector capabilities are utilized, which depends primarily on software advances. Since software development is slower than hardware development, it will be the limiting factor, preventing the more optimistic projections made by some experts from being achieved.

Super-scale computers will continue to have a very limited market among installations with specialized applications that are highly parallel in nature. These applications require an ever increasing number of computations to be performed on an ever increasing amount of data. To meet these requirements, ECL and CML logic circuits and ECL memories with large capacities will be included in the super-scale computers of the next decade. System costs will be higher, since performance improvements will more than balance any lowering of component cost. The average computer installation will not be able to cost-justify the use of a super-scale computer.

TABLE 7.1 4.3-1. PROJECTED TECHNOLOGY FOR VECTOR SUPER-SCALE COMPUTERS, EARLY 1980'S

CHARACTERISTICS	
CPU	
Word Length (bits)	64
Type of Logic Circuitry	ECL or CML
Cycle Time (nsec)	10 to 30
Minimum Computation Times:	
64-bit Add (nsec)	10 to 15
64-bit Multiply (nsec)	10 to 35
64-bit Divide (nsec)	30 to 60
Maximum Vector Result Rate (nsec)	10 to 30
MIPS	100 to 150
Memory	
Type	TTL or ECL
Cycle Time (nsec)	110 to 40
Maximum Capacity (words)	2 5M
Bandwidth (Mwords/sec)	NA
Error Correction	Single error correcting
Virtual Memory	A few systems
Number of Instructions	
Scalar	NA
Vector	NA
Volume (ft^3)	NA
Mainframe Weight (tons)	NA
Cost ($M)	15
MTBF (hr)	100
Maximum Number of Pipelines	NA

TABLE 7.1 4.3-2. PROJECTED TECHNOLOGY FOR VECTOR SUPER-SCALE COMPUTERS, MID 1980'S

CHARACTERISTICS	
CPU	
Word Length (bits)	64
Type of Logic Circuitry	ECL or CML
Cycle Time (nsec)	5 to 15
Minimum Computation Times:	
64-bit Add (nsec)	5 to 10
64-bit Multiply (nsec)	5 to 20
64-bit Divide (nsec)	17 to 34
Maximum Vector Result Rate (nsec)	5 to 15
MIPS	200 to 300
Memory	
Type	ECL
Cycle Time (nsec)	30
Maximum Capacity (Words)	16M
Bandwidth (Mwords/sec)	NA
Error Correction	Double error correcting
Virtual Memory	A few systems
Number of Instructions	
Scalar	NA
Vector	NA
Volume (ft^3)	NA
Mainframe Weight (tons)	NA
Cost ($M)	20
MTBF (hr)	200
Maximum Number of Pipelines	NA

TABLE 7.1 4.3-3 PROJECTED TECHNOLOGY FOR ARRAY SUPER-SCALE COMPUTERS, 1980-1985 TIMEFRAME

CHARACTERISTICS	
Processing Elements	
Number per System	Up to 1,000
Word Length (bits)	64
Type of Logic Circuitry	ECL or CML
Cycle Time (nsec)	30
Processing Element Data Memory	
Maximum Capacity (words)	16K
Type	ECL
Cycle Time (nsec)	50
Error Correction	Yes
MIPS	NA
Program and Data Memory	
Maximum Capacity (words)	40M
Type	NMOS
Cycle Time (nsec)	80 to 120
Error Correction	Yes
System MIPS	500 to 1,000
System Up-Time (hr/5-day wk)	100
System Cost ($M)	30

7.2 DATA STORAGE ELEMENTS

Data storage elements are discussed in terms of two major categories considered to be representative of memory technology in general. The two categories, illustrated in Figure 7-3, are moving media memory and electronic/optical memory. The moving media category encompasses drum, disk, and tape storage. Drum and tape technology inputs (Subsections 7.2.5 and 7.2.6) will be provided in a later version of this report. The electronic/optical memory category encompasses semiconductor, core, film, and other electronic/optical memory. Core and film memory technology inputs (Subsections 7.2.3 and 7.2.7) will be provided in a later version of the report.

7 2.1 Semiconductor Memory

7.2.1.1 Bipolar Memory -

7.2.1.1.1 State of the Art in Bipolar Memory - TTL, ECL, and I^2L technologies are used to build bipolar memory chips. For each of these three technologies, Table 7.2.1.1.1-1 presents a summary of the characteristics of state-of-the-art RAM chips and of the memory systems built from these chips. TTL and ECL RAM chips are used to build memories for high-performance applications, such as scratchpad and buffer memories, control stores, and fast main memories, where operating speed is very important. ECL is the fastest bipolar technology but has the highest power dissipation. In general, for both TTL and ECL chips and memory systems, the fastest access and cycle times listed in Table 7.2.1.1.1-1 are associated with the highest cost per bit and the largest power dissipation. The packing of 1 kbit on TTL and ECL chips is opening the way for practical use of bipolar RAMs in larger systems because the ease of interfacing such RAMs allows the design of memory systems in which control and peripheral circuitry add little to the system's total access time.

I^2L, integration injection logic, is the newest bipolar technology. It is being used to design dynamic bipolar memory chips with more bits per chip than achieved using either TTL or ECL technology. I^2L is believed to have the density and low-cost advantage of the MOS process as well as speeds only slightly lower than those achieved with TTL technology. As in the case of the other bipolar technologies, the fastest access and cycle times listed in Table 7.2.1.1.1-1 are associated with the highest cost per bit and the largest power dissipation. Nearly every semiconductor manufacturer is either actively investigating or currently introducing I^2L memory products.

TABLE 7.2 1.1 1-1. STATE OF THE ART IN BIPOLAR MEMORIES

CHARACTERISTICS	TTL	ECL	I^2L
Chip			
Capacity (kbits)	1	1	4
Size (mil^2)	15,000	15,000	14,500
Maximum Access Time (nsec)	30 to 60	10 to 35	50 to 100
Minimum Cycle Time (nsec)	50 to 100	25 to 50	100 to 200
Maximum Power Dissipation (μW/bit)	500 to 200	812.5 to 500	122 to 12.2
Cost (¢/bit)	1 5 to 0.6	1.5 to 0 6	0.7 to 0.2
Type	Static	Static	Dynamic
MTBF (hr)	10^7 to 10^8	10^7 to 10^8	NA
System			
Capacity (bits)	Up to 64M	Up to 64M	Up to 128M
Physical Volume	NA	NA	NA
Maximum Access Time (nsec)	60 to 100	25 to 55	80 to 140
Minimum Cycle Time (nsec)	80 to 140	32 to 70	130 to 240
Maximum Power Dissipation (μW/bit)	512 to 212	836 to 524	134 to 24
Cost (¢/bit)	3.40 to 1.20	3.40 to 1.20	0.97 to 0 31
MTBF (hr) (with error correction on larger memories)	10^3 to 10^4	10^3 to 10^4	NA

7.2.1.1.2 Trends in Bipolar Memory - Many competent organizations are developing and producing bipolar RAM chips in a highly competitive market. This will assure continued improvements in all aspects of the three bipolar memory technologies. Chips will get both larger and denser, as illustrated in Figure 7.2 1.1.2-1 and Table 7.2.1.1.2-1, and the growth rate for chip density will continue to exceed the growth rate for physical chip size. As the chips become denser, chip and memory system speeds will increase, as illustrated in Figure 7.2.1.1.2-2. Improvements in manufacturing processes and yields should continue to result in cost per bit reductions, as illustrated in Figure 7.2.1.1.2-3. System-level cost per bit will decrease more rapidly than chip level cost per bit because when denser chips are used in a memory system the memory chip cost is a greater percentage of the total system cost. Although power dissipation per chip will increase slowly, power dissipation per bit should decline steadily, as illustrated in Figure 7.2.1.1 2-4. This trend will aid the development of denser chips because power consumption and removal of the heat generated by it are limiting factors to the growth in bipolar chip density.

As a more mature technology, bipolar RAMs will improve at a slower rate than MOS RAMs (see Section 7.2.1.2.2). They will continue to require about five times the chip area of MOS RAMs because of the complexity of circuitry and the need for passive components, to cost two to five times as much per bit, and to dissipate substantially more power.

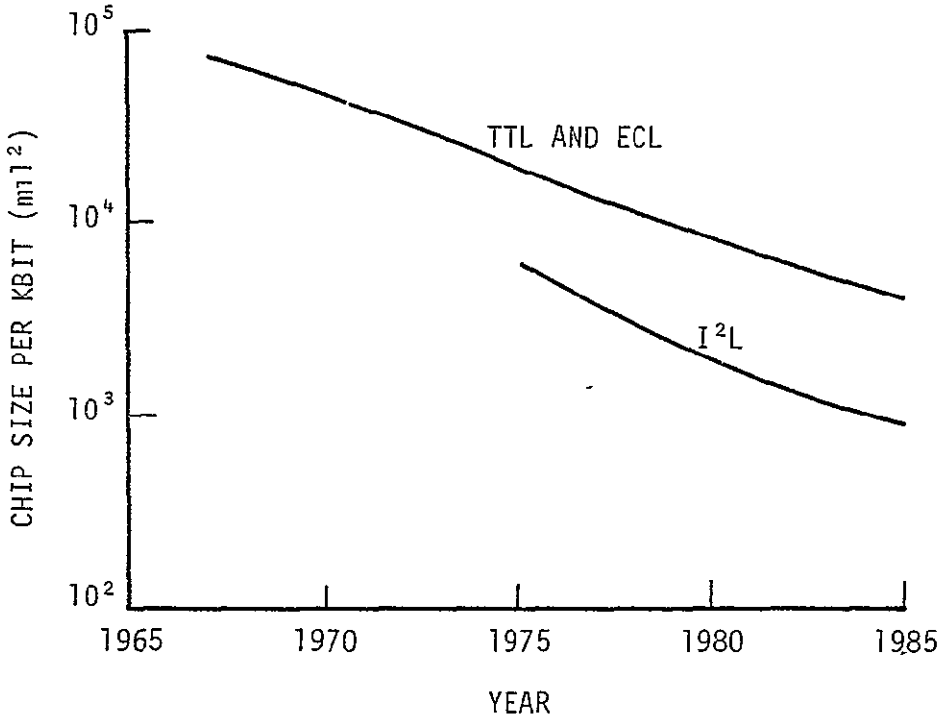

FIGURE 7 2.1.1 2-1. BIPOLAR MEMORY CHIP SIZE TRENDS

TABLE 7.2.1.1.2-1. BIPOLAR MEMORY CHIP DENSITY TRENDS

YEAR	TTL	ECL	I^2L
1965	16		
1966			
1967			
1968			
1969	64		
1970		256	
1971			
1972			
1973			
1974	1K		
1975		1K	
1976			
1977			4K
1978	4K		
1979		4K	16K
1980			
1981			
1982			
1983			64K
1984	16K		
1985		16K	

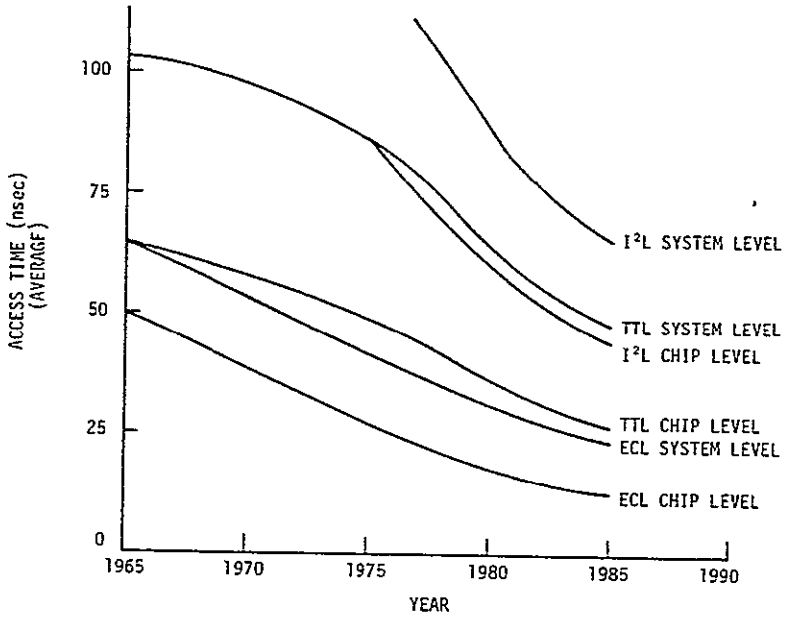

FIGURE 7.2.1.1.2-2 BIPOLAR MEMORY ACCESS TIME TRENDS

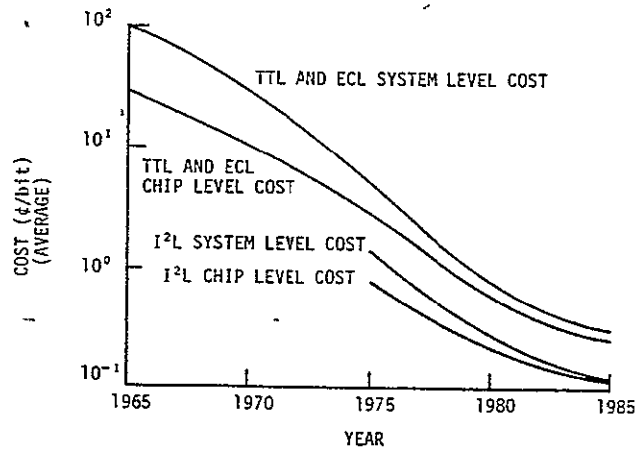

FIGURE 7.2.1.1.2-3 BIPOLAR MEMORY COST TRENDS

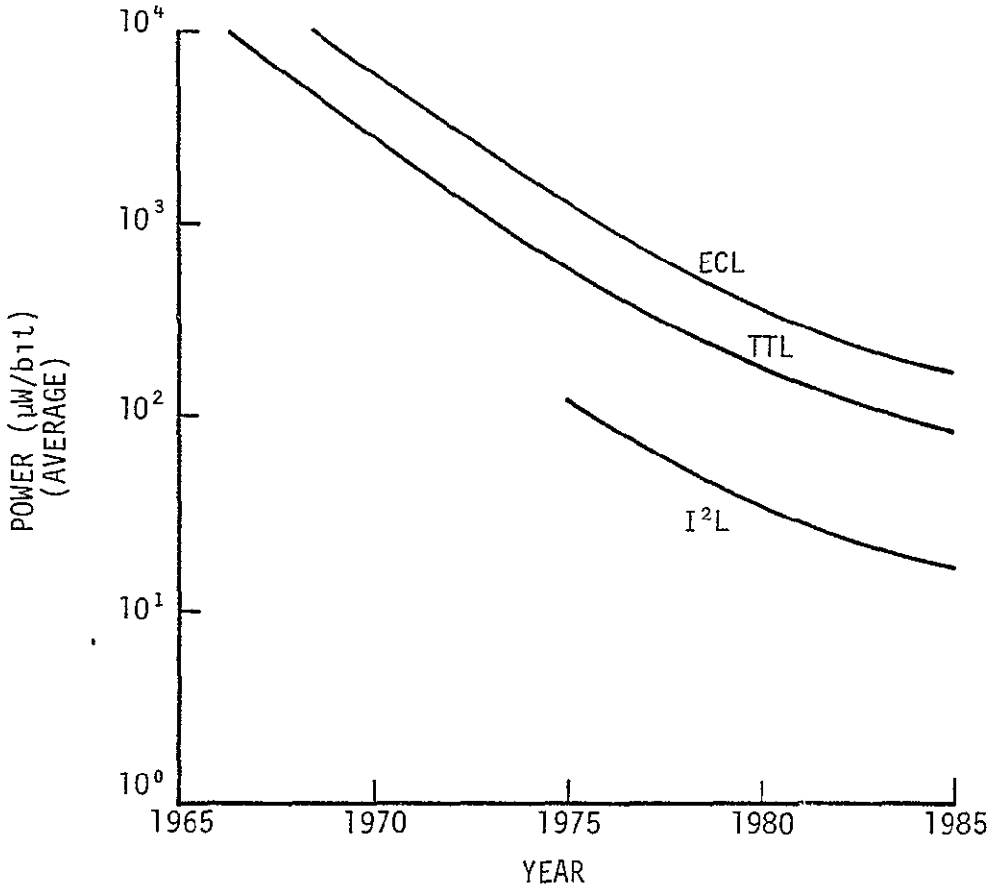

FIGURE 7 2.1.1.2-4. BIPOLAR MEMORY POWER DISSIPATION TRENDS

7 2.1.1.3 Projected Developments in Bipolar Memory - The trends in bipolar technology over the past decade and the assessment of several authorities in the field indicate that bipolar RAMs will be commercially available in 1980 and 1985 with the characteristics given in Tables 7.2.1.1.3-1 and 7.2.1.1.3-2, respectively. As with current RAM chips and memory systems, the fastest access and cycle times listed in these tables are associated with the highest cost per bit and the largest power dissipation. The 1980 and 1985 system-level access times, cycle times, and power dissipation figures were obtained by assuming that the same overhead circuitry will be needed in future systems that is needed in current systems and that improvements in the characteristics of this circuitry will occur at the same rate as improvements in these same characteristics on the chips themselves.

TTL and ECL RAMs will continue to be used to meet fast-access requirements, appearing both as buffer memory and as main memory when the cost can be justified. The fastest bipolar semiconductor memories can be expected to use ECL circuits. The newness of I^2L technology leaves a greater degree of uncertainty as to what its role will be in memory systems during the next decade. One group of experts believes that I^2L RAMs will be the next generation of high-density, low-cost components for main memories, competing with NMOS RAMs. Another group sees more use for I^2L RAMs and ROMs as elements for Programmable Logic Arrays (PLAs). As a new technology, I^2L is in need of refinements to achieve better production yields and higher speeds.

Improvements in chip-level reliability will occur during the next decade, with resultant increases in system-level reliability. However, the chips will not reach the degree of reliability required to enable large bipolar memory systems to reach the desired level of system reliability. To achieve high system reliability for these large memory systems, error correcting codes will be used.

TABLE 7.2 1 1.3-1 PROJECTED TECHNOLOGY IN BIPOLAR MEMORY, 1980

CHARACTERISTICS	TTL	ECL	I^2L
Chip			
Capacity (kbits)	4	4	16
Size (mil^2)	32,000	32,000	29,000
Maximum Access Time (nsec)	24 to 48	8 to 28	40 to 80
Minimum Cycle Time (nsec)	40 to 80	20 to 40	80 to 160
Maximum Power Dissipation (μW/bit)	250 to 100	406 to 250	61 to 6 2
Cost (¢/bit)	0.75 to 0.3	0.75 to 0.3	0 35 to 0 1
Type	Static	Static	Dynamic
MTBF (hr)	10^7 to 10^8	10^7 to 10^8	NA
System			
Capacity (bits)	Up to 160M	Up to 160M	Up to 492M
Physical Volume	NA	NA	NA
Maximum Access Time (nsec)	48 to 80	20 to 44	64 to 112
Minimum Cycle Time (nsec)	64 to 112	26 to 56	104 to 192
Maximum Power Dissipation (μW/bit)	256 to 106	418 to 262	67 to 12
Cost (¢/bit)	1 0 to 0 41	1 0 to 0 41	0 39 to 0.12
MTBF (hr) (with error correction on larger memories)	10^4	10^4	NA

TABLE 7.2.1.1.3-2 PROJECTED TECHNOLOGY IN BIPOLAR MEMORY, 1985

CHARACTERISTICS	TTL	ECL	I^2L
Chip			
Capacity (kbits)	16	16	64
Size (mil^2)	64,000	64,000	58,000
Maximum Access Time (nsec)	18 to 36	6 to 21	30 to 60
Minimum Cycle Time (nsec)	30 to 60	15 to 30	60 to 120
Maximum Power Dissipation (μW/bit)	125 to 50	203 to 125	30 to 3
Cost (¢/bit)	0 375 to 0 15	0.375 to 0.15	0 175 to 0.05
Type	Static	Static	Dynamic
MTBF (hr)	10^8 to 10^9	10^8 to 10^9	NA
System			
Capacity (bits)	Up to 1G	Up to 1G	Up to 2G
Physical Volume	NA	NA	NA
Maximum Access Time (nsec)	36 to 60	15 to 33	48 to 84
Minimum Cycle Time (nsec)	48 to 84	20 to 42	78 to 144
Maximum Power Dissipation (μW/bit)	128 to 53	209 to 131	33 to 6
Cost (¢/bit)	0.45 to 0.2	0.45 to 0 2	0 19 to 0 06
MTBF (hr) (with error correction on larger memories)	10^5	10^5	NA

7 2.1.2 MOS Memory -

7.2.1.2.1 State of the Art in MOS Memory - PMOS, NMOS, CMOS, and MNOS technologies are used to build MOS memory chips. For each of these technologies, Table 7.2.1.2.1-1 presents a summary of the characteristics of state-of-the-art RAM chips and of the memory systems built from these chips. For each of the chips and systems summarized, the fastest access and cycle times listed in this table are associated, in general, with the highest cost per bit and the largest power dissipation. Reduced cost per bit and reduced overhead circuit requirements have made semiconductor RAMs attractive for the replacement of magnetic core memories in computer mainframes. For most new developments, semiconductor RAMs are dominant up to 10^6 bits, which is 64K words in a 16-bit minicomputer system, and semiconductor memory systems have been built containing more than 10^8 bits. Currently, about 60% of the new main memory market belongs to semiconductor memories, with 40% belonging to MOS memories and 20% belonging to bipolar memories. MOS memories already play a strong role in large-scale memory systems. Although core technology still dominates the installed base of minicomputers, MOS technology dominates the new announcements. The principal advantages of MOS memories are higher speed, lower cost, reduced space requirements, lower power consumption, nondestructive readout, and simplified maintenance. The main disadvantage is volatility, and the newer MNOS technology is designed to offer nonvolatile semiconductor storage.

PMOS is the oldest MOS technology. The 4-kbit memory chips with the characteristics listed in Table 7.2.1.2.1-1 represent the state of the art for this technology. Since the newer NMOS technology offers nearly a factor of two increase in operating speeds because of lower capacitances and lower threshold voltage, PMOS is basically an obsolete technology.

NMOS is the MOS technology that offers the best combination of memory access time, chip density, power dissipation, and cost per bit. Both static and dynamic NMOS RAM chips are in widespread use today

TABLE 7.2.1.2.1-1 STATE OF THE ART IN MOS MEMORY

CHARACTERISTICS	PMOS	NMOS	NMOS	NMOS*	CMOS	MNOS
Chip						
Capacity (kbits)	4	4	4	16	1	4
Size (mil^2)	NA	30,000	17,000	30,000	11,200	37,000
Maximum Access Time (nsec)	300 to 400	45 to 250	100 to 250	150 to 250	60 to 300	1,600 (read) 100 msec (write)
Minimum Cycle Time (nsec)	500 to 600	130 to 320	150 to 365	375 to 410	450 to 600	NA
Maximum Power Dissipation (μW/bit)	100 active	160 to 90 active 160 to 5 standby	122 to 110 active 10 to 5 standby	45 to 30 active 1 2 to 0 6 standby	20 to 10 active 3 to 0 05 standby	75 to 100
Cost (¢/bit)	0 2	0 35 to 0 15	0 3 to 0 08	0 3 to 0 1	2 8 to 0 9	0 3
Type	dynamic	static	dynamic	dynamic	static	static
MTBF (hr)	NA	10^7 to 10^8	10^7 to 10^8	10^7 to 10^8	NA	NA
System						**
Capacity (bits)	up to 128M	up to 128M	up to 128M	up to 128M	NA	up to 18M
Physical Volume	NA	NA	NA	NA	NA	NA
Maximum Access Time (nsec)	330 to 440	85 to 290	130 to 290	180 to 290	100 to 350	2,000 per 1K block
Minimum Cycle Time (nsec)	530 to 640	160 to 450	180 to 450	400 to 450	480 to 640	4,000 per 1K block read 200 msec per 1K block write
Maximum Power Dissipation (μW/bit)	112	172 to 102 active 172 to 10 standby	134 to 122 active 15 to 10 standby	57 to 42 active 7 to 5 standby	32 to 22 active 8 to 5 standby	NA
COST (¢/bit)	0 31	0 50 to 0 25	0 44 to 0 16	0 34 to 0 12	4 60 to 1 60	NA
MTBF (hr)	NA	10^3 to 10^4	10^3 to 10^4	10^3 to 10^4	NA	NA

* Just beginning volume production, prices and speeds should drop during the next year
** BORAM (Block Organized RAM) systems

Dynamic chips store data as a capacitive charge and periodically refresh this charge before it can leak away, as opposed to static chips that store data in a bistable multivibrator and do not require periodic refresh. A dynamic cell requires only a fraction of the transistors needed by a static cell and also does not require a dc power component, although the sense amplifier may or may not dissipate dc power depending on the particular memory system design. The ac power dissipation of a dynamic cell is a function of the rate at which the memory is cycled, increasing as the cycle time increases. Obviously, density is greatly improved with a dynamic chip and power requirements are potentially much less. Dynamic chips are also less expensive and faster. However, they do require constant memory refreshing from additional support circuitry.

For small systems that cannot tolerate the additional support circuitry required by dynamic RAMs and for systems that cannot allocate time for memory refresh, static RAMs are essential. The state of the art for static NMOS RAMs is the 4-kbit chip, organized as either 4K × 1 bits or 1K × 4 bits, packaged in an 18-pin dual in-line package, and requiring a single +5-V supply. Chip and system characteristics are listed in Table 7.2.1.2.1-1. A few of the high-performance chips still use multiple power supplies. Static RAM chips are available in both static and quasi-static configurations. Both configurations employ a static memory array, but in the quasi-static configuration power applied to peripheral circuits can be switched off to conserve power, allowing standby power dissipation to be much lower than active power dissipation at the expense of circuit complexity. For the static configuration, standby and active power dissipation are the same, but this RAM chip is simpler to design into a memory system.

For main memory applications, one is primarily concerned with dynamic RAMs because of the power requirements of static RAMs. The state of the art for dynamic NMOS RAMs is the 4-kbit and 16-kbit chips, with the 16-kbit chips just now reaching full production status. Chip

and system characteristics are listed in Table 7 2.1.2.1-1. The large-board, dense RAM chip systems cost substantially less than their smaller counterparts because both the storage and the nonstorage costs per bit decrease with increasing chip density.

CMOS is the high-speed, low-power-dissipation, high-noise-immunity MOS technology. Its state of the art is the 1-kbit chip with the characteristics listed in Table 7.2.1.2.1-1. CMOS memory system characteristics are also listed in this table. CMOS chips utilizing SOS (silicon on sapphire) technology have the fastest access and cycle time but also cost the most per bit. Chips not using the SOS technology are available for under 1 ¢/bit but have access times greater than 100 nsec. Because of the very low power requirements, 1-kbit CMOS RAMs that operate from a small battery are available, thus providing a nonvolatile, portable memory package. Since CMOS is a static design that uses more silicon per cell than other technologies, it is generally agreed that the high cost of silicon will make CMOS useful for memories no larger than 1 kbit in capacity except for special applications.

MNOS is the MOS technology that attempts to overcome the volatility of semiconductor memories through the use of a double insulator layer structure. Its state of the art is the 4-kbit chip. Chip and system characteristics are listed in Table 7.2.1.2.1-1. Expected data-retention time quoted for state-of-the-art MNOS memory systems is 10 years, and researchers claim to have increased this time to 200 years in laboratory models. However, the long-term reliability of MNOS memory systems is still greatly debated. Because of the large access and write times, much improvement is needed for MNOS memories to become a viable alternative.

7.2.1.2.2 Trends in MOS Memory - Many competent organizations are developing and producing MOS memory chips in a highly competitive market. This will assure continued significant improvements in all aspects of MOS technology and will secure the position for MOS memories as the dominant processor memory technology, at least through 1985.

NMOS RAM chips will get both larger and denser, as illustrated in Figure 7.2.1.2.2-1 and Table 7.2.1.2 2-1, and the growth rate for chip density will continue to exceed the growth rate for physical chip size. These improvements will be the result of continued improvements in lithography, fabrication, and packaging. The historic factor of four improvement in NMOS RAM chip density every 2 years will slow down during the next decade because photolithographic limits will be reached with the 64-kbit NMOS RAM chip. The next step in chip density, to the 256-kbit chip, will require direct electron beam die etching. In the opinion of most experts, cost-effective use of this technique is at least 5 years away. CMOS RAM chips will probably get smaller, with the chip density maintained at 1 kbit because of the high cost of silicon.

As the chips become denser, chip and memory system speeds will increase, as illustrated in Figures 7.2.1.2.2-2 and 7.2.1.2.2-3. Since semiconductor memories generally rely on increasing chip density to reduce cost per bit, the growth in chip density, aided by improvements in manufacturing processes and yields, will allow the trend of a 30 to 35% cost per bit reduction each year to continue (Ref. 7-10), as illustrated in Figure 7.2.1 2.2-4. System-level cost per bit will decrease more rapidly than chip level cost per bit, because when denser chips are used in a memory system the memory chip cost is a greater percentage of the total system cost. Although power dissipation per chip will increase slowly during the next decade, power dissipation per bit should decline steadily, as illustrated in Figure 7.2.1.2.2-5. This trend will aid the development of denser chips. Reliability at the chip level will continue to increase as denser chips and improved fabrication processes are developed.

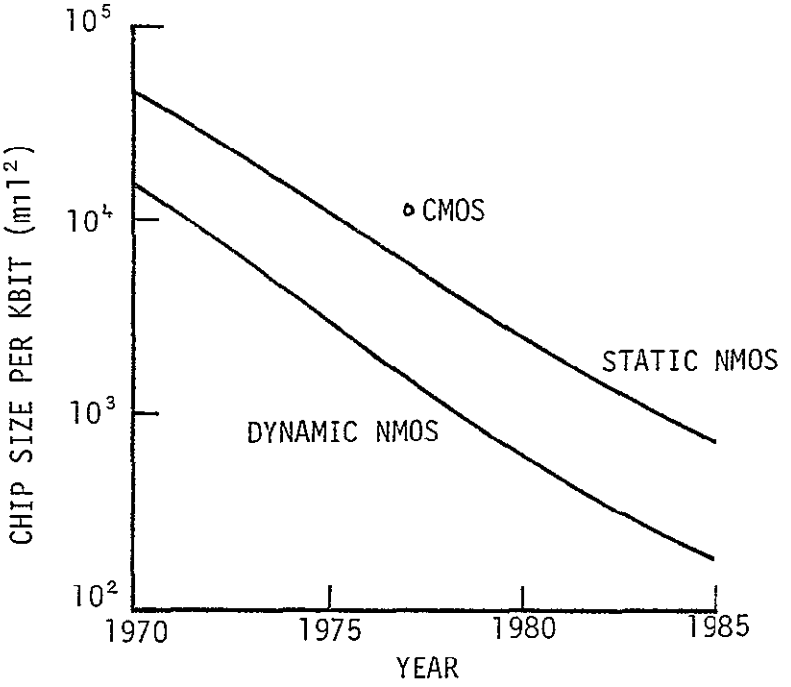

FIGURE 7.2 1.2.2-1 MOS MEMORY CHIP SIZE TRENDS

TABLE 7.2 1.2.2-1. MOS MEMORY CHIP DENSITY TRENDS

YEAR	STATIC NMOS	DYNAMIC NMOS
1969	256	
1970		1K
1971		
1972	1K	
1973		4K
1974		
1975		
1976	4K	16K
1977		
1978		64K
1979	16K	
1980		
1981		
1982		
1983	64K	256K
1984		
1985		

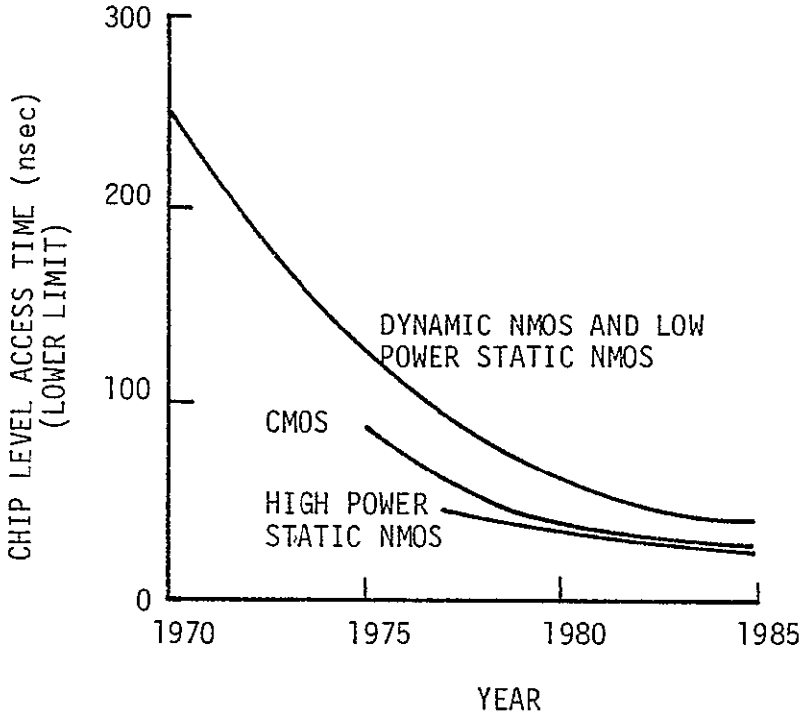

FIGURE 7.2 1.2.2-2. MOS MEMORY CHIP LEVEL ACCESS TIME TRENDS

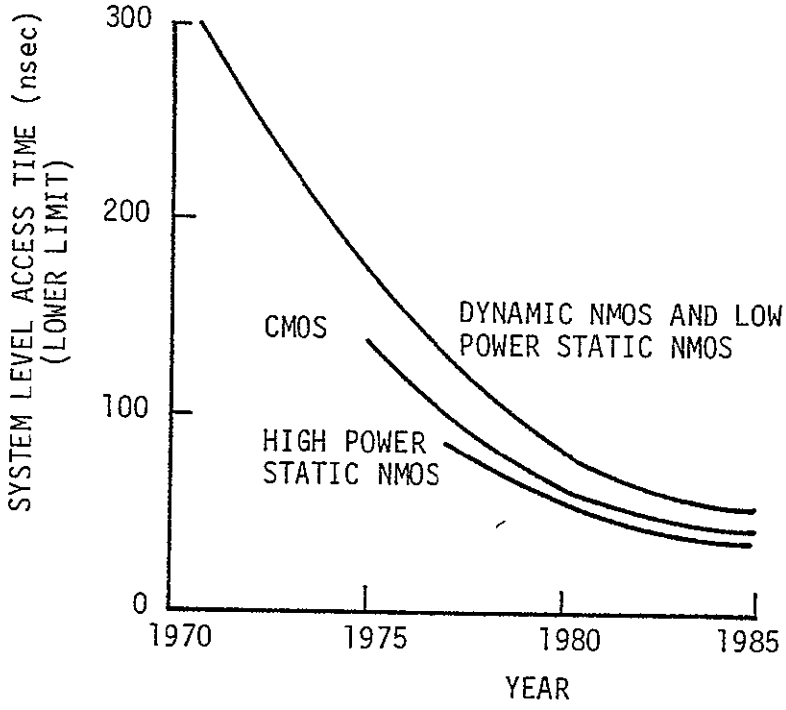

FIGURE 7.2.1.2.2-3 MOS MEMORY SYSTEM LEVEL ACCESS TIME TRENDS

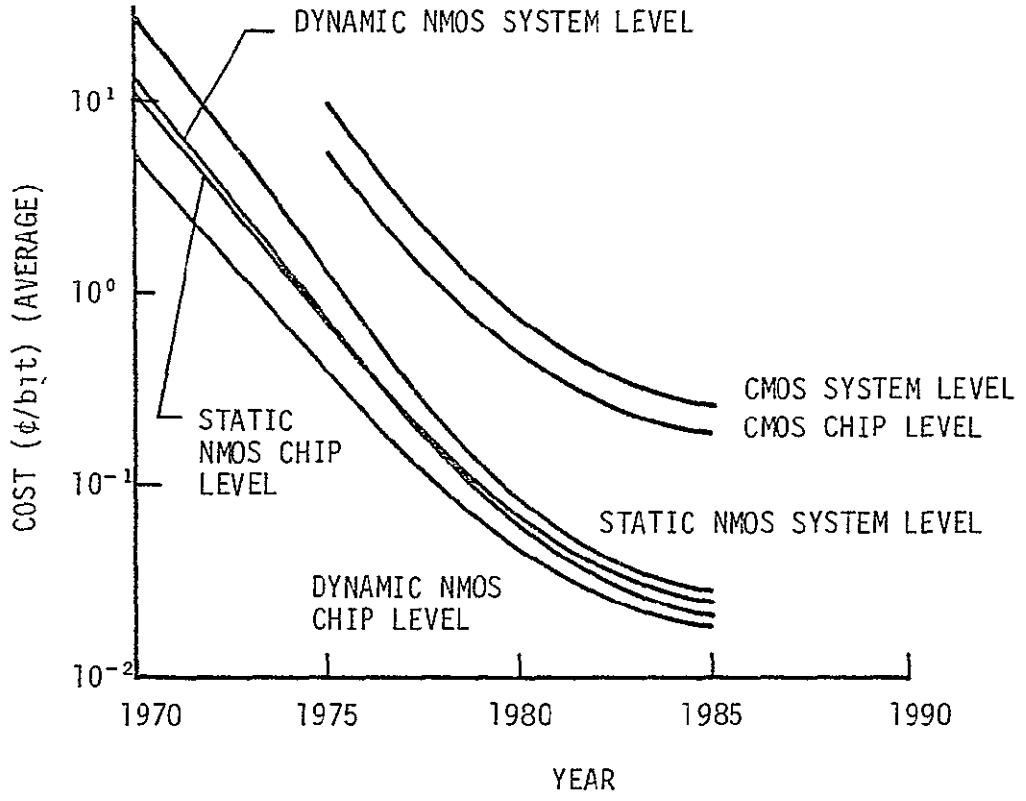

FIGURE 7 2.1 2.2-4 MOS MEMORY COST TRENDS

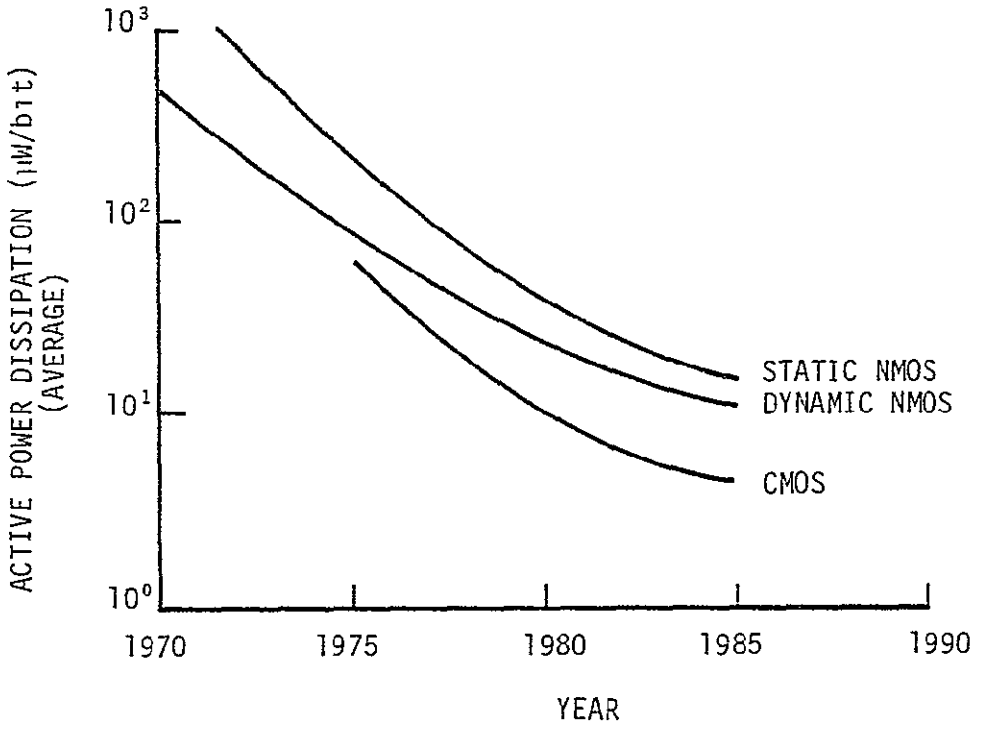

FIGURE 7 2 1.2 2-5. MOS MEMORY ACTIVE POWER DISSIPATION TRENDS

7.2.1.2.3 Projected Developments in MOS Memory - The trends in MOS technology over the past decade and the assessment of several authorities in the field indicate that NMOS and CMOS RAMs will be commercially available in 1980 and 1985 with the characteristics given in Tables 7.2.1.2.3-1 and 7.2.1 2.3-2, respectively. As with current RAM chips and memory systems, the fastest access and cycle times listed in these tables are associated with the highest cost per bit and the largest power dissipation. The 1980 and 1985 system-level access times, cycle times, and power dissipation figures were obtained by assuming that the same overhead circuitry will be needed in the future systems that is needed in current systems and that improvements in the characteristics of this circuitry will occur at the same rate as improvements in these same characteristics on the chips themselves.

MOS RAMs will be the dominant main memory technology during the next decade. However, the highest speed devices typically will not be used in the largest capacity systems because of their power requirements. The portable file storage area, now dominated by floppy and fixed-head disks, will be penetrated by MOS memories as the result of better MOS memory reliability and the achievement of higher densities and lower costs (Ref. 7-11). Continued improvements in fixed-head and moving-head disk and drum systems will block MOS memories from entering the mass storage area.

Improvements in chip-level reliability will occur during the next decade, with resultant increases in system-level reliability. However, the chips will not reach the degree of reliability required to enable large MOS memory systems to reach the desired level of system reliability. As MOS memories are used in larger-capacity memory systems, the use of error correcting codes will expand to achieve high system reliability. As the cost per bit continues to decline, the extra bits and associated logic required for error correcting codes become insignificant when compared with the cost of emergency service.

TABLE 7.2.1.2.3-1. PROJECTED TECHNOLOGY IN MOS MEMORY, 1980

CHARACTERISTICS		NMOS	NMOS	CMOS
Chip				
Capacity (kbits)		16	64	1
Size (mil^2)		40,000	40,000	NA
Maximum Access Time (nsec)		35 to 150	60 to 150	36 to 180
Minimum Cycle Time (nsec)		78 to 192	90 to 219	270 to 360
Maximum Power Dissipation (μW/bit)	active	40 to 23	20 to 15	5 to 2.5
	standby	40 to 2	1 5 to 0 7	0 75 to 0 0125
Cost (¢/bit)		0 09 to 0 04	0 08 to 0.02	0.7 to 0 23
Type		static	dynamic	static
MTBF (hr)		10^7 to 10^8	10^7 to 10^8	NA
System				
Capacity (bits)		up to 492M	up to 492M	NA
Physical Volume		NA	NA	NA
Maximum Access Time (nsec)		54 to 174	78 to 174	60 to 210
Minimum Cycle Time (nsec)		96 to 270	108 to 270	288 to 384
Maximum Power Dissipation (μW/bit)	active	46 to 29	26 to 21	11 to 8
	standby	46 to 5	5 to 4	4 to 3
Cost (¢/bit)		0.1 to 0.05	0.09 to 0.026	1 2 to 0.14
MTBF (hr)		10^4	10^4	NA

TABLE 7.2.1.2.3-2. PROJECTED TECHNOLOGY IN MOS MEMORY, 1985

CHARACTERISTICS		NMOS	NMOS	CMOS
Chip				
Capacity (kbits)		64	256	1
Size (mil^2)		48,000	48,000	NA
Maximum Access Time (nsec)		25 to 100	40 to 100	24 to 120
Minimum Cycle time (nsec)		52 to 128	60 to 146	180 to 240
Maximum Power Dissipation (μW/bit)	active	16 to 9	9 to 7	2 to 1
	standby	16 to 0.5	0.56 to 0.28	0 3 to 0.005
Cost (¢/bit)		0 035 to 0 015	0 03 to 0.008	0 28 to 0.09
Type		static	dynamic	static
MTBF (hr)		10^8 to 10^9	10^8 to 10^9	NA
System				
Capacity (bits)		up to 2G	up to 2G	NA
Physical Volume		NA	NA	NA
Maximum Access Time (nsec)		36 to 116	52 to 116	40 to 140
Minimum Cycle Time (nsec)		64 to 180	72 to 180	192 to 256
Maximum Power Dissipation (μW/Bit)	active	19 to 12	12 to 10	5 to 4
	standby	19 to 2	2	2 to 1.5
Cost (¢/bit)		0.038 to 0.017	0.032 to 0.009	0.47 to 0 07
MTBF (hr)		10^5	10^5	NA

7.2.1.3 CCD Memory - (Not available for Phase I)

7.2.2 Other Electronic/Optical Memory

7 2 2.1 Electron Beam Addressed Memory -

7.2.2.1.1 State of the Art in Electron Beam Addressed Memory - The use of electron beams for accessing memory has been under investigation for a number of years, principally by Stanford Research Institute, General Electric, and Micro-Bit Corporation Such memories are called either Electron Beam Addressable Memories (EBAM) or Beam Addressable MOS Memories (BEAMOS). The technology is based on the use of an electon beam to read and write data on a simple, unstructured MOS chip. Addressing of the two-dimensional array of data is accomplished by deflection of the electron beam. Data are stored on the MOS target as the presence or absence of positive charge in the oxide near the oxide-silicon interface. Charge storage is accomplished by the application of a bias voltage to the target while the beam is swept along a track during a write or erase cycle. In a subsequent read cycle, the beam is swept over the same track, and where a charge is present a current is produced in a sense circuit. If no charge is present, no significant current is produced

A complete BEAMOS or EBAM memory system consists of one or more tubes, address and interface logic, control circuits, and power supplies. The tube contains the MOS target and electron beam addressing system enclosed in a sealed evacuated envelope. Tubes are being designed with both one and two lens-deflector fields. The number of bits that can be accessed in a one-stage tube is limited by aberrations in the deflector and by inaccuracies and instabilities of the deflection eletronics. These limitations can be pushed outward by several orders of magnitude through the use of two-stage deflection and an array of lenses known as the fly's eye configuration.

Development of BEAMOS or EBAM technology has progressed to the prototype stage, with units scheduled to be commercially available this year. Table 7.2.2.1.1-1 summarizes the characteristics of the prototype units and memory systems. A memory access that invokes an operation change (e.g , read to write) requires a change in the bias of the oxide. Therefore, as indicated in the table, this type of access takes more time than

TABLE 7.2.2 1.1-1. STATE OF THE ART IN ELECTRON BEAM ADDRESSED MEMORY

CHARACTERISTICS*	ONE-STAGE	TWO-STAGE
Tube		
Dimensions (length by diameter)	26 by 5.5 cm	42 by 10 cm
Capacity	4 Mbits	32 Mbits
Storage Density	8.3×10^5 bits/cm^2	4.2×10^6 bits/cm^2
Cost	0 005 ¢/bit	0.005 ¢/bit
System		
Capacity	Up to 64×10^6 bits	Up to 6×10^8 bits
Access Time - No Operation Change	5 µsec	5 µsec
Access Time - Operation Change	10 to 20 µsec	20 to 30 µsec
Service Time	440 µsec	440 µsec
Recording Data Rate**	0.5 to 5 Mpbs	5 to 10 Mbps
Power	250 W	250 W
Temperature Range	-50 to +70°C	-50 to +70°C
Radiation Tolerance	10^5 rad	10^5 rad
MTBF	8,000 hr	8,000 hr
Cost***	0.1 ¢/bit	0 1 ¢/bit

*Laboratory models, first systems to be delivered late 1977.

**Higher read rate possible; higher write rate if tubes are operated in parallel.

***Upon entry into market; will fall to 0 02 to 0.05 ¢/bit as volume increases; cost listed is for large, multitube system.

successive calls of the same operation, which are limited primarily by the switching and settling time of the deflection amplifier. The service time listed in the table is the average time between the acceptance by the memory of a new command and the earliest time that the next command can be accepted. The recording data rate for a tube is determined by the beam current available. Because considerably less beam current is required for a read operation, reading can be performed at a higher rate than writing.

Electron beam memories require very stable and highly regulated power supplies and a very fast and accurate deflection electronics system, both of which contribute significantly to the overall system cost. For this reason it is highly desirable to build multitube systems in which a large portion of this electronics is shared. Only by sharing the electronics is the cost per bit reduced to acceptable levels.

The nonstructured nature of the storage plane and the flexibility of electron beam addressing allow the MOS target to be formatted in a wide variety of ways. BEAMOS or EBAM systems can be used to access a single bit at a time by allowing the deflection system to settle at a particular location and then turning on the beam to interrogate the charge stored at that target position. However, it is highly probable that most systems will be used in a block-oriented mode in which information is written as an encoded string of transitions along a continuous path. Random access to the start of the block is achieved digitally, and the block itself is scanned on the fly with the beam on continuously. This is a more efficient organization because access time is primarily dependent on the deflection settling time, which in the block organization is incurred only for the starting location of a block. The block length can vary over wide limits and there are no built-in restrictions on word length. Therefore, redundancy can be included easily within each block for error control to enhance system reliability.

The MOS target is a relatively nonvolatile storage medium. It stores data for several weeks, even when power is off, but it does not store data permanently because of signal decay. Signal decay is very slow with the power off or with the power on and zero or negative oxide bias

values. With the power off, the measured signal is 90% of its initial value after five days of storage and about 80% after one month (Ref. 7-12). Decay is somewhat faster at positive bias. In addition, the signal is reduced slightly by each readout. As a result of these sources of decay, refreshing of the memory is required, even when the memory is not being used. When reading at 10 Mbps, a rewrite becomes necessary after 10 to 20 reads. At higher read data rates, the number of reads before rewrite decreases.

Because the electron beam is a source of radiation, it causes a gradual permanent degradation of the target. This degradation limits the lifetime in each location to the order of 10^7 write-erase cycles. To lessen the effects of this target fatigue, present BEAMOS or EBAM systems rotate or permute the data to average the usage of the target area. Only if the tube itself is replaced on a preventive maintenance schedule can the MTBF given in Table 7.2.2.1.1-1 be achieved.

BEAMOS or EBAM memories exhibit many characteristics required for military environment applications. A major advantage is the fact that the systems are all-electronic and completely sealed. No parts are especially sensitive to vibration and the section most important for beam positioning, the matrix lens/target assembly, is very rugged. Tests of the storage plane over the -50°C to +70°C temperature range indicate that charge storage is not greatly affected by temperature. In this temperature range there should be less than 0.1-μm variation in the position of the addressing beam. Although the memory requires a shield to protect against external fields, a shield weighing only 10 lb should protect against fields up to 10 g in strength. The memory plane is quite tolerant of ionizing radiation. Ionizing radiation of 10^5 rads causes no more than 10% reduction in signal level, while no permanent radiation damage has been observed up to 6×10^7 rads

7.2.2.1.2 Trends in Electron Beam Addressed Memory - While functional BEAMOS or EBAM memory systems exist today, they are not exactly "home free". To lower costs while increasing capacity and performance, three significant problem areas must be addressed. First, the MOS target life must be improved Second, electron optics must be upgraded to accomplish submicron beam diameters in production so that density goals can be realized. Third, cathode development must occur to increase beam brightness as the beam is made smaller to achieve greater density. Assuming that progress is made in these areas, the trends stated in the following paragraphs should be realized.

BEAMOS or EBAM memories offer great potential in terms of performance, cost per bit, and total capacity. System performance is expected to approach that of main memory with a capacity approaching and even exceeding that of the large moving-head disk files. Therefore, these memory systems have the potential not only of bridging the memory access gap but also of eliminating it and thus effecting a dramatic reduction in operating system software complexity and cost.

During the next decade BEAMOS or EBAM memories will benefit from research in both semiconductor and electron beam technologies. As the result of improvements in MOS target parameters, the use of two-stage deflection in the array optics configuration, and increases in the addressable target area of a single tube arising from advances in electron optics, storage densities will increase and access times will decrease, as illustrated in Figures 7.2.2 1.2-1 and 7.2.2.1.2-2, respectively. At the same time, recording data rates will increase, as illustrated in Figure 7.2.2.1.2-3. The increases in storage density and addressable target area will bring increases in tube capacity, as illustrated in Figure 7.2.2.1.2-4 As a result of these technology improvements, cost per bit will decline rapidly, as illustrated in Figure 7.2 2.1.2-5. In addition, signal decay and target degradation improvements will be realized.

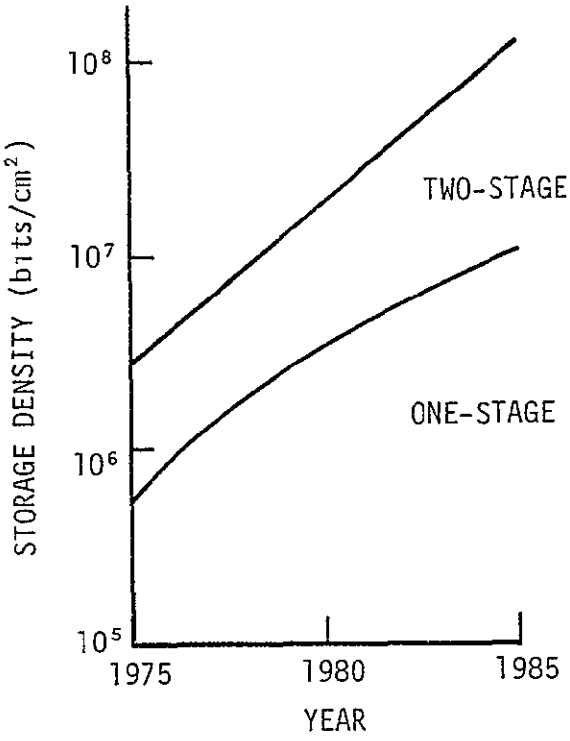

FIGURE 7.2.2.1.2-1. ELECTRON BEAM ADDRESSED MEMORY STORAGE DENSITY TRENDS

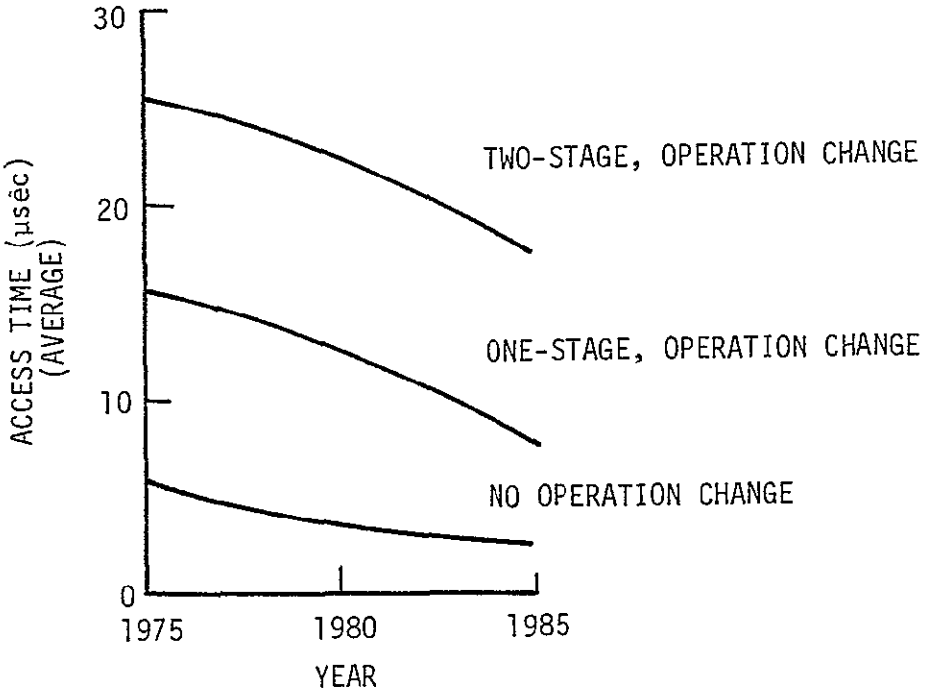

FIGURE 7.2.2.1.2-2. ELECTRON BEAM ADDRESSED MEMORY ACCESS TIME TRENDS

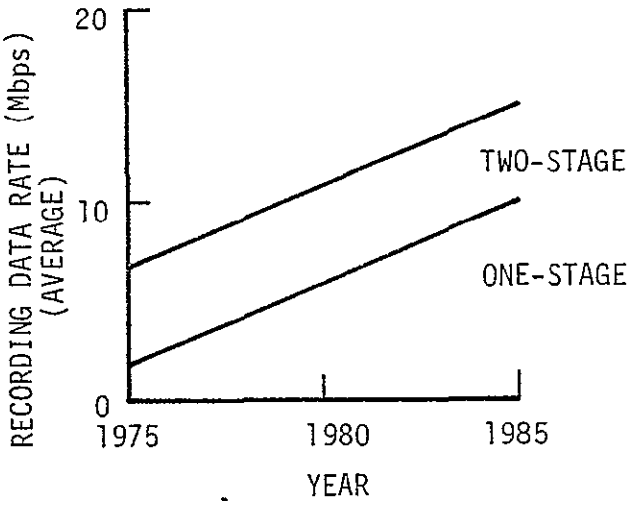

FIGURE 7.2.2.1.2-3 ELECTRON BEAM ADDRESSED MEMORY RECORDING DATA RATE TRENDS

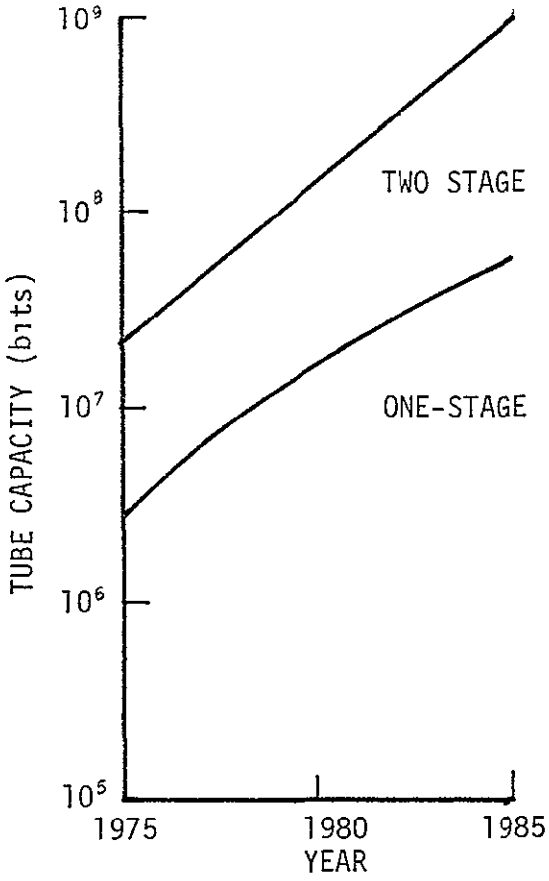

FIGURE 7.2.2 1.2-4 ELECTRON BEAM ADDRESSED MEMORY TUBE CAPACITY TRENDS

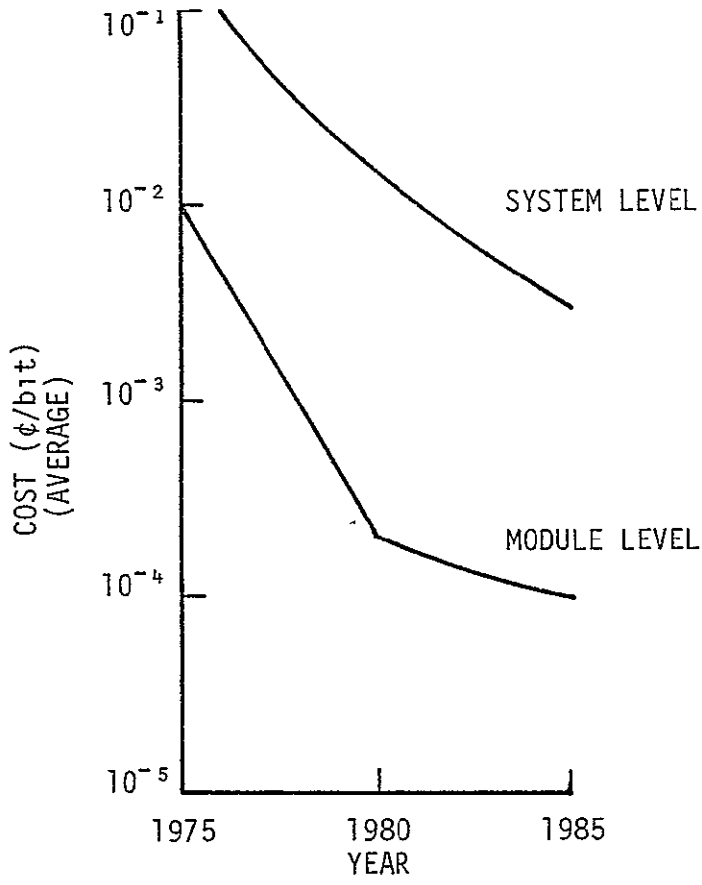

FIGURE 7.2 2.1.2-5. ELECTRON BEAM ADDRESSED MEMORY COST TRENDS

7.2.2.1.3 Projected Developments in Electron Beam Addressed Memory - Assuming that progress is made in the problem areas discussed under trends (Section 7.2.2.1.2), BEAMOS or EBAM memory systems should be commercially available in 1980 and 1985 with the characteristics presented in Tables 7.2.2.1.3-1 and 7.2.2.1.3-2, respectively. The minimum system capacity is equal to the tube capacity. Since system-level cost is dependent on the amount of sharing of electronics that is achieved, multitube systems will be dominant. The system costs given in the tables are for these multitube systems. Emphasis will be placed on utilizing two-stage deflection and an array of lenses known as the fly's eye configuration because of the improvement it offers in terms of addressable target area. The ultimate theoretical limit on packing density is approximately 10^{10} bits/cm^2 (Ref. 7-12). The development of tube capacities much greater than 10^9 bits will require the use of field-emitter cathodes that have three to five orders of magnitude greater brightness than the currently used thermal dispenser cathode. Such cathodes have been developed already as a result of the demand for higher-resolution scanning electron microscopy (Ref. 7-13)

The initial impact of the electron beam memory technology will be as a replacement for the fast-access auxiliary storage devices, currently dominated by fixed-head disks. The BEAMOS or EBAM systems are already cost-competitive with the high-performance fixed-head disks while offering significant performance improvement. Eventually these systems will be cost-competitive with all on-line random access peripheral memories but with far superior performance. Equally important is their potential use as main memory extensions, in combination with semiconductor cache, where they will have a large price advantage at comparable performance. Amdahl is on record as being willing to replace virtual disk memory, with its big loss of throughput, with electron beam memories, or at least electron beam cache, if they prove cost-effective.

TABLE 7.2.2.1.3-1. PROJECTED TECHNOLOGY IN ELECTRON BEAM ADDRESSED MEMORY, 1980

CHARACTERISTICS	ONE-STAGE	TWO-STAGE
Tube		
Dimensions (length by diameter)	26 by 5.5 cm	42 by 10 cm
Capacity	16 Mbits	128 Mbits
Storage Density	3 3 × 10^6 bits/ cm^2	1.7 × 10^7 bits/ cm^2
Cost	0.0002 ¢/bit	0.0002 ¢/bit
System		
Capacity	Up to 256 Mbits	Up to 2 Gbits
Access Time - No Operation Change	3 3 µsec	3.3 µsec
Access Time - Operation Change	10 to 15 µsec	20 to 25 µsec
Service Time	NA	NA
Recording Data Rate*	4 to 8 Mbps	10 to 12 Mbps
Power	NA	NA
Temperature Range	-50 to +70°C	-50 to +70°C
Radiation Tolerance	10^5 rads	10^5 rads
MTBF	NA	NA
Cost**	0.01 to 0.02 ¢/bit	0.01 to 0 02 ¢/bit

*Higher read rate possible; higher write rate if tubes are operated in parallel.

**For large, multitube system.

TABLE 7.2.2 1.3-2. PROJECTED TECHNOLOGY IN ELECTRON BEAM ADDRESSED MEMORY, 1985

CHARACTERISTICS	ONE-STAGE	TWO-STAGE
Tube		
Dimensions (length by diameter)	26 by 5.5 cm	42 by 10 cm
Capacity	53 Mbits	1 Gbit
Storage Density	1×10^7 bits/ cm^2	1.3×10^8 bits/ cm^2
Cost	0 0001 ¢/bit	0.0001 ¢/bit
System		
Capacity	Up to 848 Mbits	Up to 8 Gbits
Access Time - No Operation Change	2.5 µsec	2.5 µsec
Access Time - Operation Change	5 to 10 µsec	15 to 20 µsec
Service Time	NA	NA
Recording Data Rate	10 Mbps	15 Mbps
Power	NA	NA
Temperature	-50 to +70°C	-50 to +70°C
Radiation Tolerance	10^5 rads	10^5 rads
MTBF	NA	NA
Cost**	0.001 to 0.005 ¢/bit	0 001 to 0.005 ¢/bit

*Higher read rate possible; higher write rate if tubes are operated in parallel.

**For large, multitube system.

7.2.2.2 Magnetic Bubble Memory - Magnetic Bubble Memory is discussed in Subsection 3.2.

7.2.2.3 Plated Wire Memory - (Not available for Phase I)

7.2.2.4 Laser/Holographic Memory - (Not available for Phase I)

7.2.3 Core

(Not available for Phase I)

7.2.4 Disks

7.2.4.1 Fixed-Head Disks - (Not available for Phase I)

7.2.4.2 Moving-Head Disks -

7.2.4.2.1 State of the Art in Moving-Head Disks - Over the past 12 to 15 years, disks have provided the bulk of on-line mass storage Moving-head disk technology is the dominant disk storage technology today A disk storage system is configured from disk drives and controllers. A moving-head disk drive consists of a stack of rigid magnetic disks addressed by positionable read-write heads that are mounted on arms attached to a voice coil actuator. The actuator moves the heads from track to track so that each head covers a large number of concentric tracks, thereby reducing the cost of access to large amounts of data since the read-write heads contribute a major portion of the overall cost. Until recently, the majority of the drives incorporated removable disk packs. However, non-removable packs are appearing in many of the newest drives. Table 7.2.4.2.1.-1 summarizes the characteristics of state-of-the-art moving-head disk systems. The largest system capacities are associated with the largest spindle capacities, which in turn are associated with the largest track and linear densities. The drives with the largest spindle capacities generally allow the highest transfer rates. Because the larger spindle capacities are achieved by packing bits more closely together, the physical dimensions of systems are not proportional to their capacities. Some of the largest capacity systems occupy the least amount of space and have the smallest weight.

As a magnetic recording type of storage, moving-head disks have the advantages of nonvolatility; low cost; allocation flexibility; a simple, reliable recording process, and update in place. Their major disadvantage is that they involve mechanical motion and thus cannot achieve the speeds that all-electronic storage can achieve. In several of the newest disk systems, fixed-head storage is being combined with moving-head storage on the same spindle to reduce the average access time, albeit at an increased cost. This technique is particularly useful when multiple seeks are required, such as for indexing on the disk.

TABLE 7.2.4.2.1-1. STATE OF THE ART IN MOVING-HEAD DISKS

SYSTEM CHARACTERISTICS	REMOVABLE PACK	NONREMOVABLE PACK
Track Density	192 to 402 tracks/in.	402 to 480 tracks/in.
Linear Density	Up to 6,425 bpi	Up to 6,425 bpi
Areal Density	Up to 3 Mbits/in.^{2}	Up to 3 Mbits/in.^{2}
Spindle Capacity	69.8 to 317.5 Mbytes	300 to 400 Mbytes
Maximum System Capacity	800 to 6,400 Gbytes	5,000 to 12,800 Gbytes
Typical Physical Characteristics of Minimum-Capacity System.		
Width by Depth by Height	19 by 34 by 38 to 44 by 32 by 47 in.	20 by 34 by 40 to 50 by 42 by 33 in
Weight	480 to 1,100 lb	500 to 1,100 lb
Temperature Range	60 to 90°F	60 to 90°F
Humidity Tolerance	20 to 80%	20 to 80%
Head Movement:		
Minimum	7 or 10 msec	7 or 10 msec
Average	25 to 30 msec	25 or 27 msec
Maximum	50 or 55 msec	50 msec
Rotation Time	16.7 msec	16.7 msec
Average Access Time	34.3 to 38.3 msec	33.4 to 35.3 msec
Transfer Rate	806,000 or 885,000 or 1,198,000 bytes/sec	806,000 or 1,198,000 bytes/sec
Cost	0.001 ¢/bit	0.0007 ¢/bit
MTBF	NA	NA

Moving-head disk storage is used primarily as on-line bulk memory, providing large quantities of reliable, low-cost storage. The cost per bit of this storage is heavily dependent on the overall system capacity. The cost per bit figures given in Table 7.2.4 2.1-1 are for large-capacity systems, those with at least 100 Mbytes of storage. Cost per bit in small-capacity systems can be 0.04¢ and higher.

The achievement of higher storage densities has required improvement in magnetic recording resolution, which has been achieved through improvements in head gap, head-disk spacing, and medium thickness. Improved track densities have followed from the advent of the voice coil actuator and closed-loop track-following systems. Present track-following systems contain a servo head in a multiple-head array to supply feedback information on head positioning. Since all heads move together, if the servo head is maintained on its track, then all other heads will be on their tracks.

High recording densities and medium flaws have made the use of error-correcting codes a standard procedure in state-of-the-art disk systems for improved system reliability. The most common codes in use are cyclic codes that have burst error detection and correction capabilities. Relatively short codes in conjunction with logical means for skipping defective surface areas can provide the desired error-rate levels. Increased reliability has also been gained through the use of the Winchester design, in which the recording disks, moving arm, and read-write heads are contained in environmentally sealed data modules. The reliability advantages of this technique include reading of data by the same head that writes the data, low contamination by airborne particles, and light head loading.

7.2.4.2.2 Trends in Moving-Head Disks - Moving-head disk storage is still an evolving and viable technology. There is widespread belief that during the next decade the use of disk storage will expand and technical advances will continue at the same rate as in the past, providing further major improvements in most performance categories, with as much as an order of magnitude advance in many categories. Moving-head disk storage will continue to be the dominant technology for on-line bulk storage, at least into the 1980's.

Most of the improvements in the next decade will be in the form of increased areal density resulting from more tracks per inch laterally and more bits per inch longitudinally, as illustrated in Figures 7.2.4.2.2-1 through 7.2.4.2.2-3. Increased densities will be achieved through improvements in recording resolution, as a result of decreased medium thickness, head-gap and head-disk spacing, and through improved head performance. An areal density improvement factor of at least 40 appears theoretically possible. Although advances in track density will be less dramatic, further gains can be anticipated from improvements in head-positioning accuracy resulting from the incorporation of servo information within the data along each track, to be sensed by the same head that performs the reading and writing, to reduce all possible mechanical tolerances. In addition, disk systems will continue to be designed for ever larger capacity per arm, thereby reducing the access rate per unit of capacity Increasing arm capacity has been the basis for the trend toward reduced cost per bit. The 20 to 25% annual reduction in cost per bit will continue through the next decade, as illustrated in Figure 7 2.4.2.2-4.

Removable disk technology became attractive as a way of keeping drive costs down while increasing system storage capacity. With today's large-capacity drives, the need to remove packs during daily operation has been minimized. Fixed-disk packs are becoming desirable once again to achieve the tighter mechanical tolerances needed to achieve ever higher densities at the least cost.

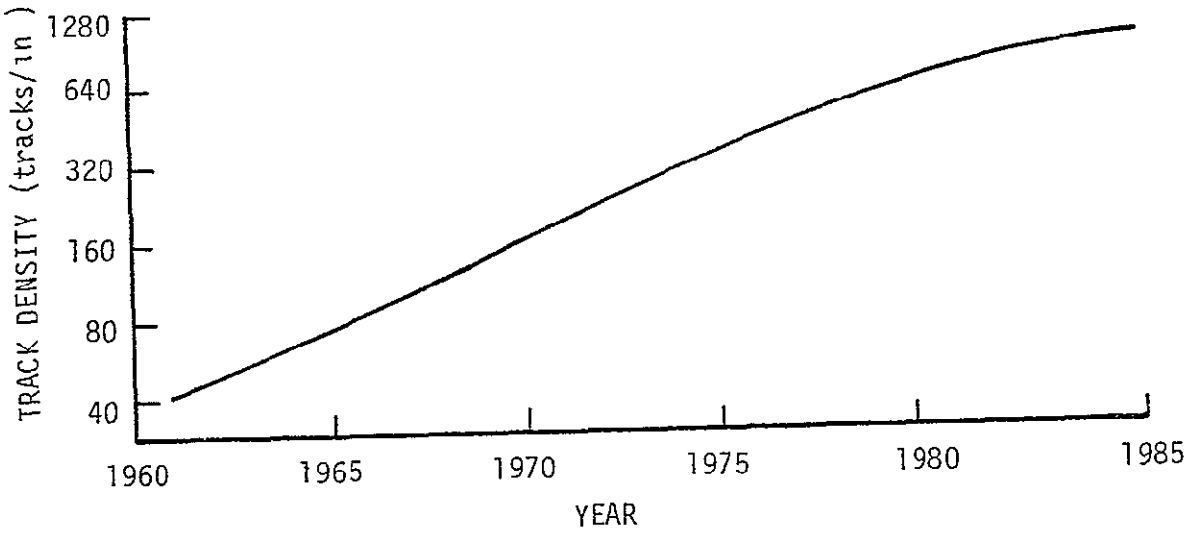

FIGURE 7.2.4.2.2-1 MOVING-HEAD DISK TRACK DENSITY TRENDS

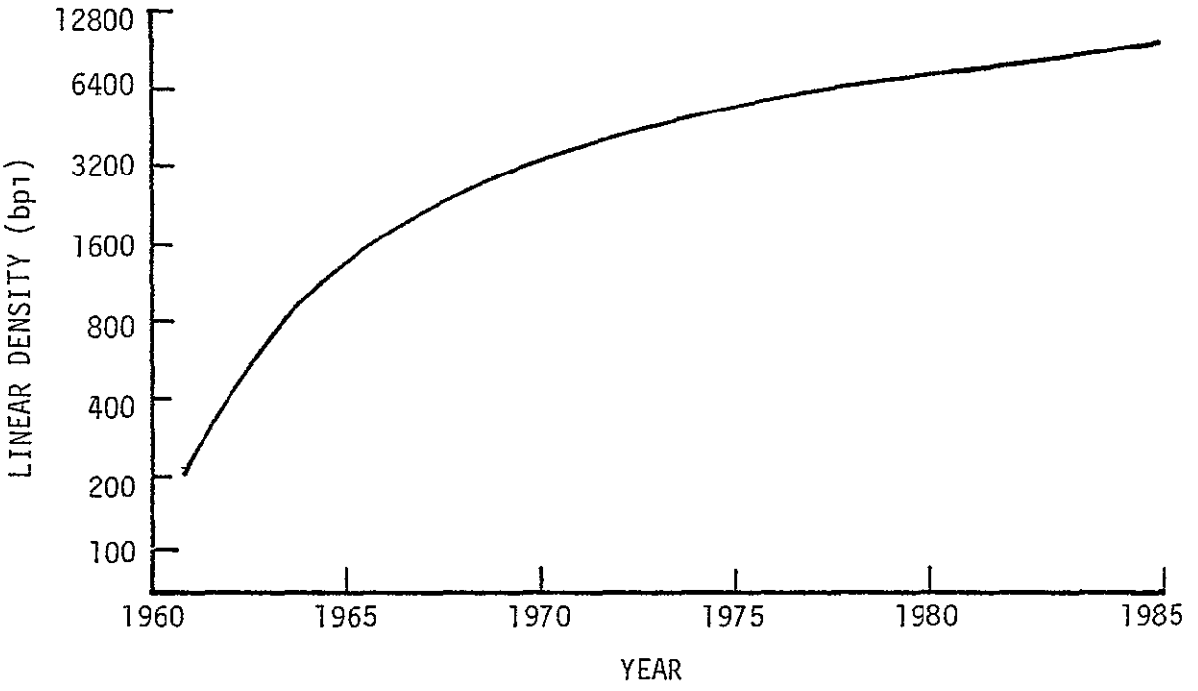

FIGURE 7.2.4.2.2-2. MOVING-HEAD DISK LINEAR DENSITY TRENDS

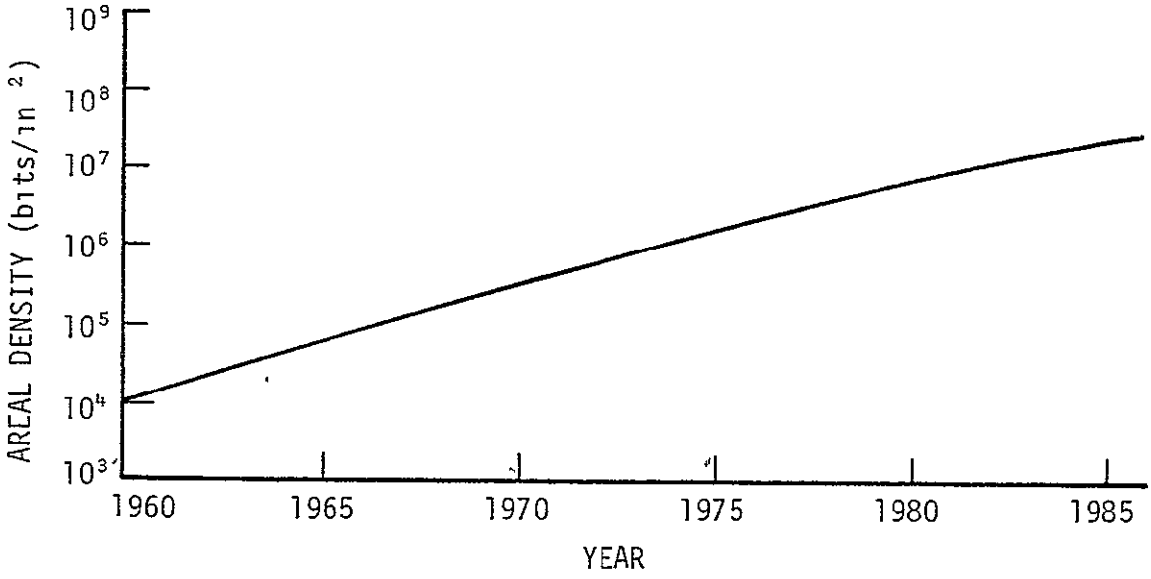

FIGURE 7.2.4.2.2-3. MOVING HEAD DISK AREAL DENSITY TRENDS

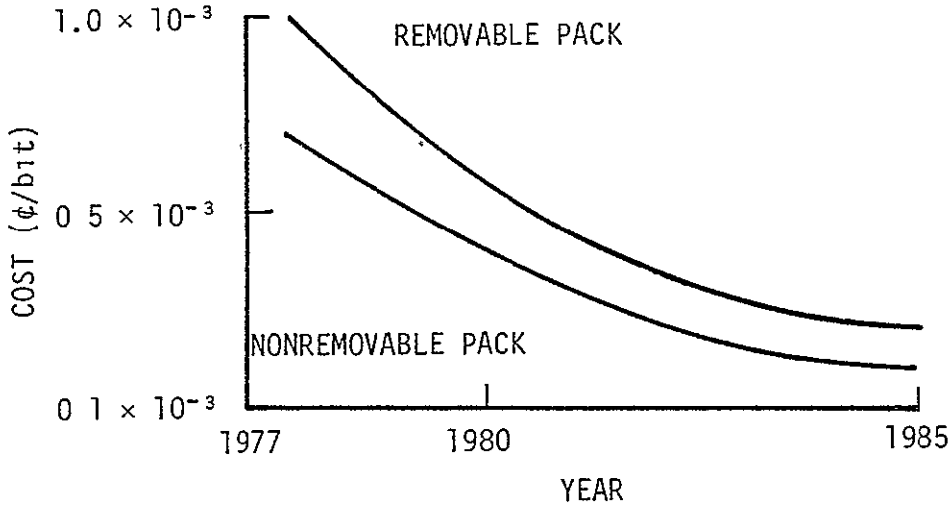

FIGURE 7.2.4.2.2-4. MOVING HEAD DISK COST TRENDS

7.2.4.2.3 Projected Developments in Moving-Head Disks - The trends in moving-head disk technology over the past 15 years and the assessments of several authorities in the field indicate that moving-head disk systems will be commercially available in 1980 and 1985 with the characteristics given in Tables 7.2.4 2.3-1 and 7.2.4.2.3-2, respectively. As discussed under trends (Section 7.2.4.2.2), the progress in storage densities will be achieved in the next decade through improved recording resolution. The advances will require a scaling down of all recording dimensions. Medium-base coatings will be thinner, with better dispersal and orientation of the particles. Read-write heads will be spaced more closely and will have improved performance, with minimized adjacent track pickup, minimized head misregistration, and increased longitudinal head resolution. Utilization of these storage density advances to increase the storage capacity per drive will cause a decrease in cost per bit and average access time without changing the physical characteristics of the system. The cost per bit of moving-head disk storage will continue to depend heavily on the overall system capacity. The cost per bit figures given in Tables 7 2.4 2 3-1 and 7.2.4.2.3-2 are for large-capacity systems

Increasing positioner motor force constants by the use of rare-earth magnet motors will aid the development of faster access times during the next decade. In addition, effective positioner speed will be improved through the use of multitrack heads in some systems. They will be used in fixed-head files, as fixed-head additions to moving-head files, and as moving multitrack heads in a hybrid design. An added benefit of this approach is that it increases the size of a cylinder, thereby improving performance in the case of sequential operations

Improvements in system reliability will be aided by several factors during the next decade. The use of error-correcting codes will expand since, as a rule of thumb, data integrity is improved by three orders of magnitude by the use of these codes. As electronic costs decline, error correcting codes will be built into the drives, making them transparent to the channel. Defect skipping will continue to be used, allowing the drive to locate magnetic surface flaws, to catalog them, and then, by the use of buffers, to skip over them during write and subsequent read operations. Redundancy

TABLE 7.2.4.2.3-1. PROJECTED TECHNOLOGY FOR MOVING-HEAD DISKS, 1980

SYSTEM CHARACTERISTICS	
Track Density	800 tracks/in
Linear Density	7,000 bits/in
Areal Density	9.4 Mbits/in^2
Spindle Capacity	600 Mbytes
Maximum System Capacity	19.2 Gbytes
Typical Physical Characteristics of Minimum-Capacity System:	
Width by Depth by Height	NA
Weight	NA
Temperature Range	60 to 90°F
Humidity Tolerance	20 to 80%
Head Movement.	
Minimum	6 to 10 msec
Average	23 msec
Maximum	45 msec
Rotation Time	16 7 msec
Average Access Time	30 msec
Transfer Rate	1.5 Mbytes/sec
Cost:	
Removable Pack	0.0005 ¢/bit
Nonremovable Pack	0 00036 ¢/bit
MTBF	NA

TABLE 7 2.4 2.3-2. PROJECTED TECHNOLOGY FOR MOVING-HEAD DISKS, 1985

SYSTEM CHARACTERISTICS	
Track Density	1,000 tracks/in
Linear Density	10,000 bits/in
Areal Density	25 4 Mbits/in^2
Spindle Capacity	1,000 Mbytes
Maximum System Capacity	32 Gbytes
Typical Physical Characteristics of Mimimum Capacity System:	
Width by Depth by Height	NA
Weight	NA
Temperature Range	60 to 90°F
Humidity Tolerance	20 to 80%
Head Movement	
Minimum	5 to 8 msec
Average	20 msec
Maximum	40 msec
Rotation Time	16.7 msec
Average Access Time	27 msec
Transfer Rate	4 5 Mbytes/sec
Cost:	
Removable Pack	0.0002 ¢/bit
Nonremovable Pack	0.0001 ¢/bit
MTBF	NA

of electronics-and tracks will be included in more systems. The use of fixed packs will expand, allowing greater control over possible damage caused by airborne particle contamination.

Moving-head disk technology is relatively mature. It should continue to be a reliable, cost-effective mass storage device during the 1980-1985 timeframe Although other emerging technologies such as CCD and bubble memories will challenge some applications of these disks, their biggest threat during the next decade seems to be to the smaller disk systems that have a higher cost per bit.

7.2.5 Drum

(Not available for Phase I)

7.2.6 Tape

(Not available for Phase I)

7.2.7 Film

(Not available for Phase I)

7.3 DATA PROCESSING SYSTEM COMMUNICATION ELEMENTS

(Not available for Phase I)

7.4 PERIPHERAL DEVICES

(Not available for Phase I)

7.5 SPECIALIZED HARDWARE

(Not available for Phase I)

7.6 SOFTWARE

(Not available for Phase I)

7.7 FIRMWARE

(Not available for Phase I)

LIST OF SYMBOLS - SECTION 7

BEAMOS	Beam Addressable MOS Memory
CCD	Charge-Coupled Device
CML	Current Mode Logic
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
EBAM	Electron Beam Addressable Memory
ECC	Error Correcting Code
ECL	Emitter Coupled Logic
I^2L	Integration Injection Logic
I/O	Input/Output
LSI	Large-Scale Integration
MIPS	Million Instructions Per Second
MNOS	Metal-Nitride-Oxide Semiconductor
MOS	Metal-Oxide Semiconductor
MTBF	Mean Time Between Failure
NMOS	N-channel Metal-Oxide Semiconductor
PLA	Programmable Logic Array
PMOS	P-channel Metal-Oxide Semiconductor
PROM	Programmable Read Only Memory
RAM	Random Access Memory
ROM	Read Only Memory
SOS	Silicon On Sapphire
TTL	Transistor Transistor Logic
WCS	Writable Control Storage

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8. DATA BASE SYSTEMS ELEMENTS (GROUND)

Data base systems elements include all the Level 1 elements presented in Figure 8-1. This section discusses only one of the Level 1 elements identified in the referenced figure: i.e., Data Base Management System (DBMS). Processing and data storage elements are discussed in Section 7; telecommunication elements are presented in Section 9, and system software, application software, and file management system elements will be included in this section for future program phases.

Figure 8-2 presents a detailed breakdown of DBMS elements in terms of features and functions that are generally used to characterize a DBMS. Subsequent paragraphs are organized along the lines of the breakout presented in this figure.

DBMS represents perhaps the most complex data processing technology in the industry today This is attributable to the several disciplines that are crossed to develop, assess, or even understand DBMSs as they exist today. As a result, two constraints or ground rules were established to effect a meaningful technology assessment within the limitations of this contract effort.

The first constraint is related to the scope of the subject matter. One alternative is to cover all aspects of DBMSs but restrict the level of detail and thereby produce little quantitative results. Another alternative is to concentrate the investigative effort on selected areas considered to be key DBMS issues. This latter approach was taken to assess the technology from the present time through 1985. Although a reasonably comprehensive outline of DBMS issues is contained in this section, not all of these issues were selected for in-depth investigation and assessment.

Second, to provide consistency and commonality to this effort and to enhance communication with experts and authorities in the field, DBMSs were limited to those that are, or will be, commercially available and general-purpose. In the evaluation and assessment of DBMS functions,

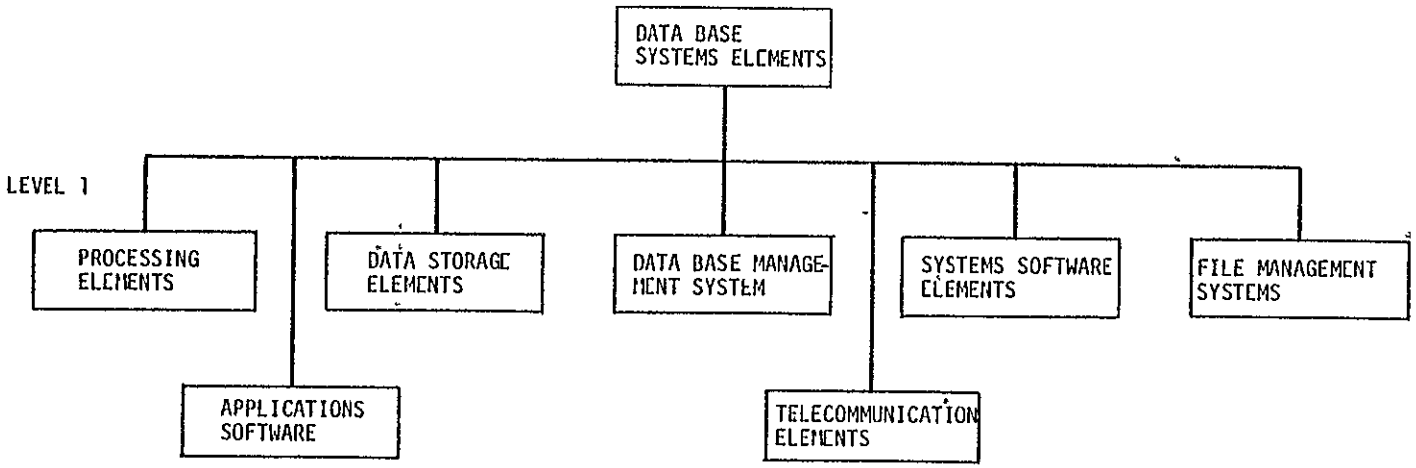


FIGURE 8-1 DATA BASE SYSTEMS ELEMENTS

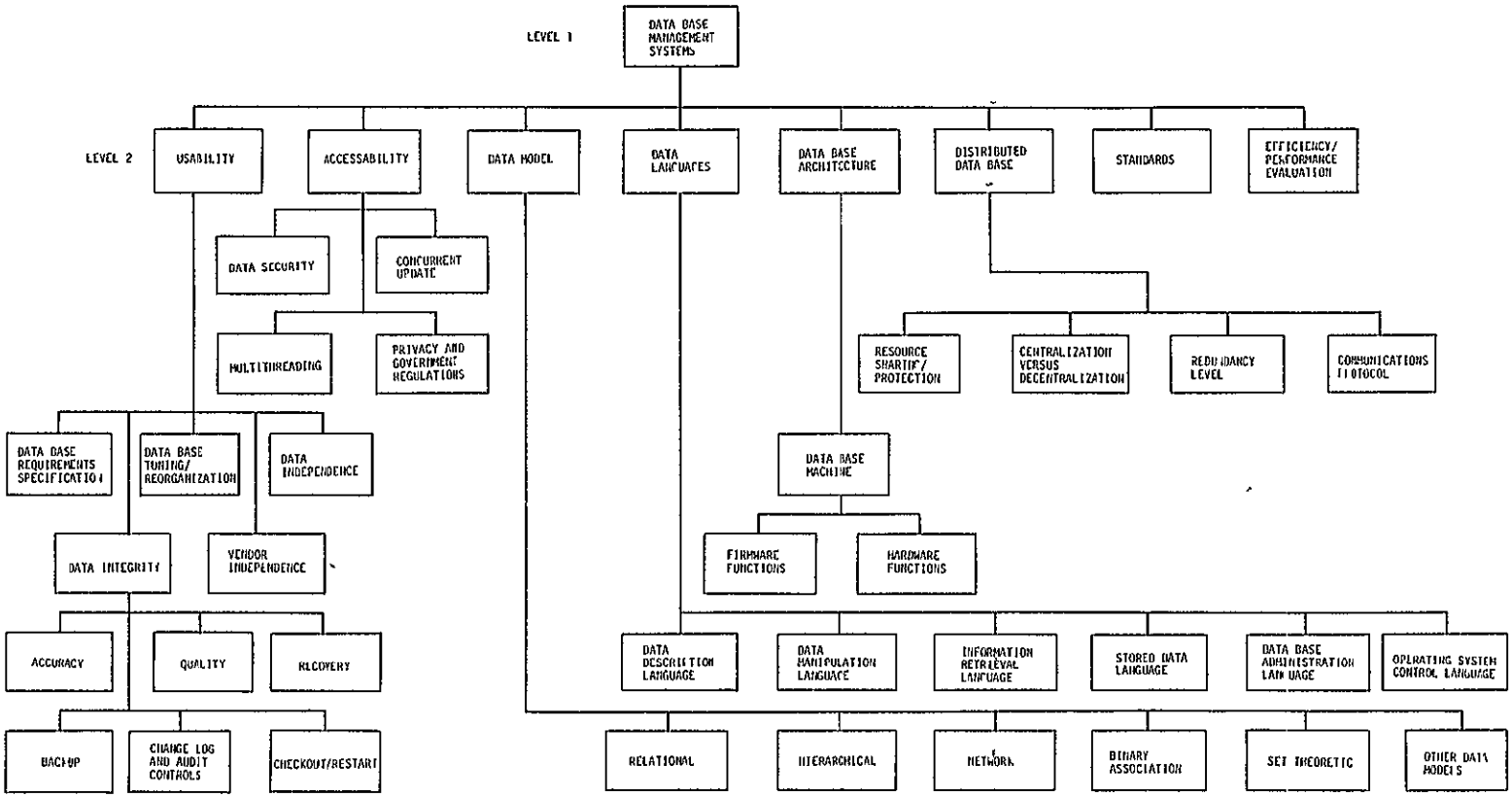


FIGURE 8-2. DATA BASE MANAGEMENT SYSTEM FEATURES AND FUNCTIONS

the results are taken to represent those functions and capabilities that are, or will be, common to the majority of commercially available, general-purpose DBMSs

The investigation/assessment process incorporated the following activities.

- Surveying and analyzing current periodicals and trade journals
- Conducting surveys and interviews of recognized authorities and experts in the field of DBMS
- Referring to system descriptions as supplied by independent agencies such as Datapro Research Corporation
- Referring to current textbooks describing methodology and trends.

All literature was restricted to 1975 or later.

Insofar as possible, terms will be defined in the appropriate sections where they are used.

8.1 USABILITY

The term usability is intended to represent a class of functions that enable the Data Base Administrator's (DBA) staff to effectively maintain, alter, and access the data base to ensure availability of meaningful data to end users. As such, usability entails several aspects which are considered in the following paragraphs.

8.1.1 Data Base Tuning/Reorganization

The purpose of data tuning and/or reorganization is to provide cost-effective performance of both the DBMS software and the set of applications programs that utilize it.

8.1 1.1 State of the Art in Data Base Tuning/Reorganization - Most DBMSs today have a Data Description Language that provides some capacity for logically restructuring the data base. At present, however, the DBMS maintains statistics on use, but the DBA must use the statistics in the reorganization decision-making process.

8.1 1.2 Trends in Data Base Tuning/Reorganization - The whole problem area of which statistics to gather and how often to gather them is also an integral part of the question of performance evaluation (Section 8.8). Much work is under way to identify those operating parameters affecting DBMS performance (Ref. 8.1), but there is little evidence to indicate that sufficient emphasis has been placed on incorporating advanced techniques in commercially available DBMSs Although there are trends toward continued development in this area, there appears to be insufficient market pressure to warrant a rapid development pace.

8.1.1.3 Projected Developments in Data Base Tuning/Reorganization - In terms of capabilities, it is envisioned that by 1985 (and no sooner) the DBMS and the DBA will jointly use the DBMS in the sense that the DBA can define a utilization statistics data base in much the same manner as any other data base might be defined. The DBA, as user, would then access and analyze these data, which are automatically maintained by the DBMS. Because of the obvious magnitude of resources required, this capability will be provided only on the largest installations for some time after initial development

8.1.2 Data Independence

Data independence is considered one of the key DBMS issues today Independence means the ability to make a change to the data base (whether logical or physical) without significantly affecting the programs that access it. The degree to which the programs must be changed represents the degree of data dependence (i.e., more change implies greater data dependence).

For this effort, data independence was classified into two general categories The first category is termed relative independence. A collection of application programs is said to be relatively data-independent with respect to a change if the only required changes are in those programs that directly access the changed view or structure of the data base. The second category is termed absolute independence. A collection of applications programs is said to be absolutely data-independent with respect to a change if it is not necessary to change or recompile any of the existing applications programs to enable their execution. To do this, in the case of data item deletion, for example, it is necessary for the DBMS to recognize an undefined data item and use some type of algorithm to substitute a default value upon accessing the data base to provide the application program an executable environment. Obviously, the long-term ramifications of such a capability imply a level of sophistication not readily achievable in the immediate future.

8.1.2.1 State of the Art in Data Independence - Tables 8 1.2.1-1 and 8.1.2.1-2 provide a summary of the present capabilities with respect to data independence. These tables exhibit different types of data base changes and the corresponding timeframe in which the designated type of independence will exist. Table 8.1.2.1-1 shows that there is a high degree of relative data independence in the present state of the art. Table 8.1.2.1-2, on the other hand, shows that there is need for significant development to achieve the same degree of absolute data independence.

TABLE 8 1 2.1-1. RELATIVE DATA INDEPENDENCE

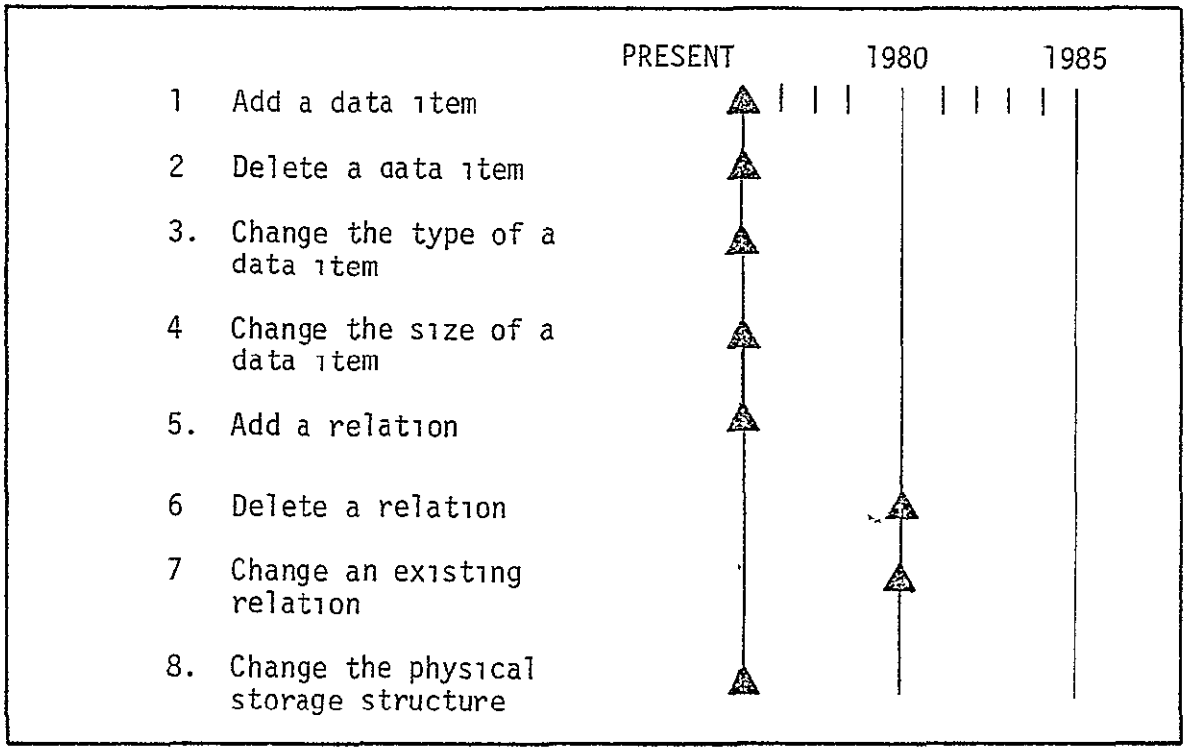
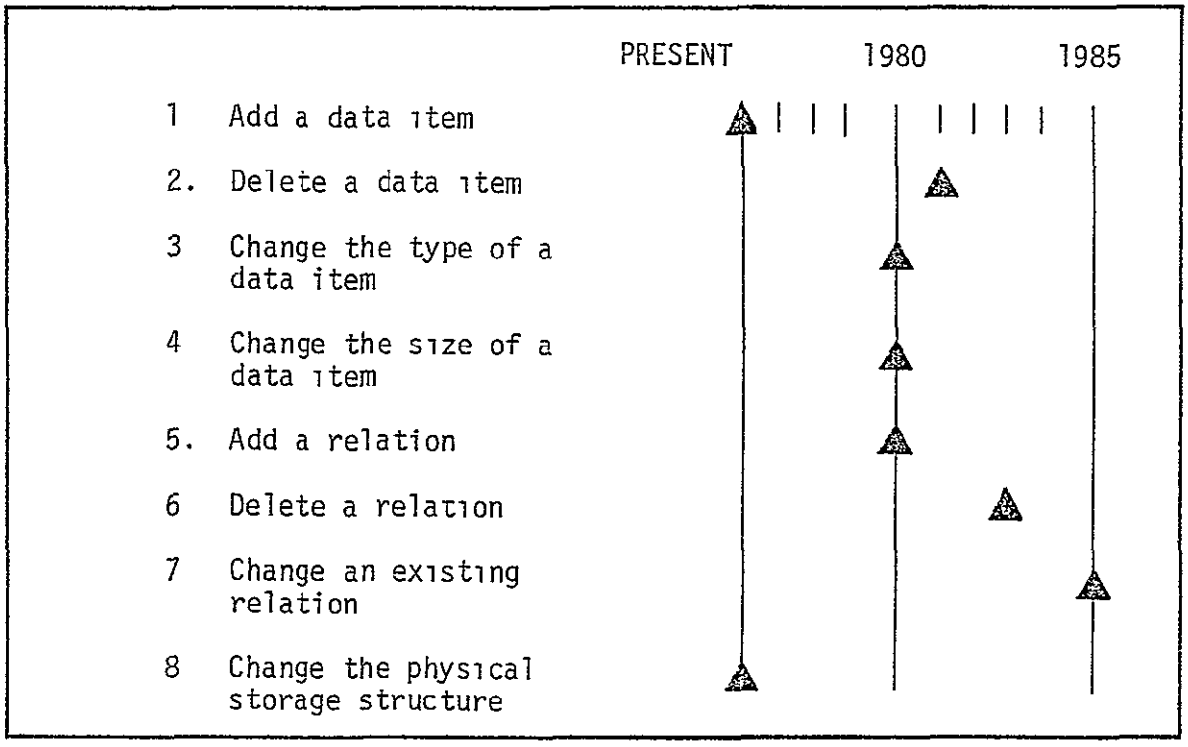


TABLE 8 1.2 1-2. ABSOLUTE DATA INDEPENDENCE



8.1 2.2 Trends in Data Independence - By comparing Tables 8.1 2 1-1 and 8.1.2.1-2, it can be seen that current development trends are much stronger in favor of changes affecting data items as opposed to changes affecting logical data relations. This applies to both relative and absolute data independence. Also, due to the less complex technological considerations, the trend toward comprehensive relative data independence is evidenced by Table 8.1.2.1-1.

8.1.2.3 Projected Developments in Data Independence - It is expected that by 1982 existing application programs will essentially be "immune" to data item changes, as well as to adding a relation Absolute data independence with respect to data relations is projected to be feasible by 1985. However, as a result of the more extensive ramifications associated with altering relations, it is uncertain at present as to what degree such relational changes can be performed and still accomplish meaningful processing. (An extreme example is the deletion of all relations, in which case any processing by existing applications programs would be meaningless unless for testing/checkout purposes or unless processing is performed on unconnected data.)

8.1.3 Data Base Requirements Specification/Definition

Requirements placed on a data base by an end user are funneled through a central data processing staff such as that of the DBA. The DBA then establishes additional requirements on the data base organization and access to meet the end user requirements as well as provide effective execution of corresponding applications programs. The technology under consideration here is the method of specifying these requirements.

8.1.3.1 State of the Art in Data Base Requirements Specification/Definition - At present, there is no single standard or widespread technique employed for such specification. Tools currently in use for activities of this type are discussed in Section 8.4. More general requirements languages and tools are presently being investigated and developed (Ref. 8-27).

8.1.3.2 Trends in Data Base Requirements Specificaton/Definition -

(Not available for Phase I)

8.1.3.3 Projected Developments in Data Base Requirements Specification/Definition -

(Not available for Phase I)

8.1.4 Data Integrity

(Not available for Phase I)

8.1 5 Vendor Independence

(Not available for Phase I)

8.2 ACCESSIBILITY

Accessibility includes both manual and automated procedures affecting an individual's or organization's ability to look at or alter data. This further means that procedures may vary depending on the mode of access (e.g., batch versus on-line), as well as on the nature of the various data items. The following paragraphs discuss the various aspects of accessibility in the context of DBMS

8.2.1 Data Security

Data security is considered to be the protection of data against unauthorized dissemination or tampering, whether it be accidental or intentional. Typically, attention is focused on the relationship between the data and users of this data (both authorized and unauthorized).

8.2.1 1 State of the Art in Data Security - One technique employed to discourage unauthorized comprehension of data in a data base is the use of data enciphering/deciphering. Presently, this is not a widespread feature of DBMS (e.g., only one or two DBMSs offer such a feature).

Another technique employed by DBMS to accomplish some degree of data security is the use of various passwords, algorithms, and identifications to lock DBMS resources. In this context, a resource is both the data and the operation performed on that data Table 8.2.1.1-1 depicts the timeframe when it is predicted that the various DBMS resource levels will be protected from unauthorized access. As shown in this table, the data base and file levels presently have reasonably comprehensive lockout capability. To date, the processing and management of lockout features resides in the DBMS software.

TABLE 8 2 1 1-1. PROJECTION OF DBMS RESOURCE PROTECTION

OPERATION / DATA LEVEL	"LOOK AT" (READ ONLY)	MODIFY	DELETE	ADD
Data Base	Present	Present	Present	Present
File	Present	Present	Present	Present
Record	1980	1980	1980	1980
Data Aggregate	1983	1983	1983	1983
Data Item	1984	1984	1984	1984

8.2 1.2 Trends in Data Security - The trend in data security is two-fold. 1) greater protection at lower resource levels and 2) the use of hardware to enhance prevention of unauthorized access to data. The use of technological advances in hardware will make the use of enciphering/deciphering, multi-level resource lockout, etc., not only feasible but economically practical as well.

8.2.1.3 Projected Developments in Data Security - As shown in Table 8.2 1.1-1, protection at the record level will be commonplace by 1980. At the lower data levels of data aggregate and data item, development will continue so that by 1984 these data levels may also be locked. Almost all of the resource locking capabilities will be in the DBMS software for the immediate future, since widespread use of hardware/firmware to replace current and anticipated DBMS software functions is not envisioned prior to the 1983-1985 timeframe.

With rapid hardware developments and the Federal Government's recent development of an enciphering/deciphering standard, it is believed that by 1985 such a feature will be widespread, but as an extra-purchase option.

8.2 2 Concurrent Update

A classic problem, which must be solved for any multiprogramming or multiuser environment, is the protection of data against simultaneous modification by two or more users or applications programs.

8.2.2.1 State of the Art in Concurrent Update - Presently, DBMS provides concurrent update protection at the data base and file levels. This is provided in the DBMS software, which is typically reentrant in nature.

8.2.2.2 Trends in Concurrent Update - The trend in this area is to develop techniques that enable protection of the data at the lowest level possible. This frees the remaining data for use by others. A major consideration in this assessment is when and at what level concurrent update protection is expected to be economically practical

8.2 2.3 Projected Developments in Concurrent Update - By 1979, this protection will be a common feature at the record level However, concurrent update protection at the data aggregate and data item levels is not expected to be available until 1985

8.2.3 Multithreading

Multithreading allows multiple users to access the data base in parallel. The current software technologies most responsible for this capability are reentrant code and multitasking. The basic concept of multithreading is to allow processing to continue on user B until the completion of I/O for user A.

8.2.3.1 State of the Art in Multithreading - This area was not treated comprehensively as a part of Phase I, however, multithreading does exist in DBMS today on a limited basis.

8.2 3.2 Trends in Multithreading - Although this capability exists today, availability as a common DBMS feature is not expected until 1980. Since there are some unique requirements associated with the DBMS/operating system interface that provides multithreading, the development of multithreading will continue to be accomplished on a "vendor-at-a-time" basis

8.2.3.3 Projected Developments in Multithreading -

(Not available for Phase I)

8.2.4 Privacy and Government Regulations

The Privacy Act of 1974 and other privacy legislation currently pending have a definite impact on the development and trends in DBMS. Since the area of privacy and Government regulations is not technological in nature, it is not included in this effort. However, it is recommended that this area be included in future assessment efforts.

8.3 DATA MODEL

A "data model" is the logical structure with which the user interrelates data items of interest to represent the "real world". DBMSs are typically characterized by the type of data model that they support. For assessing DBMS technology for the future, a DBMS is labeled "network" if the network data model is the primary model around which the DBMS was conceived and designed. For example, INQUIRE might be considered today to be a relational DBMS in light of some of its capabilities. However, literature to date indicates that INQUIRE's present capabilities as a DBMS have evolved from what was originally an information retrieval system. Thus INQUIRE would not be counted among the relational DBMSs projected to be developed in the future.

8.3.1 State of the Art in Data Models

Table 8.3.1-1 gives the distribution of data models among commercially available DBMSs, Table 8.3.1-2 gives the expected distribution among DBMS users. Although there are potentially many structural models into which data may logically fit, these tables show that the three most popular at present are hierarchical, network, and relational.

TABLE 8.3.1-1. DATA MODEL DISTRIBUTION AMONG DBMSs

DATA MODEL	PRESENT	1980	1985
Relational	2%	18%	25%
Network	36%	39%	42%
Hierarchical	58%	40%	28%
Binary Association	2%	1%	1%
Set-Theoretic	1%	2%	3%
Other	1%	0%	1%
	100%	100%	100%

TABLE 8.3.1-2. DATA MODEL DISTRIBUTION AMONG DBMS USERS

DATA MODEL	PRESENT	1980	1985
Relational	2%	14%	21%
Network	34%	36%	39%
Hierarchical	60%	47%	36%
Binary Association	4%	2%	2%
Set-Theoretic	0%	1%	2%
Other	0%	0%	0%
	100%	100%	100%

8.3.2 Trends in Data Models

Tables 8.3.1-1 and 8.3.1-2 illustrate a gradual trend away from hierarchical and other models in favor of the relational and network models.

8.3.3 Projected Developments in Data Models

Although Tables 8.3.1-1 and 8.3.1-2 indicate increasing development and use of the relational model, network is expected to be the primary data model available and in use through 1985. The information in these tables is based on an assessment of responses received from authorities in the field who were asked to predict the future data model distributions.

Some additional notes are necessary to further qualify these projections. First, 0% does not mean "not at all". Rather, 0% is intended to mean either that the number making up the percentage is so small as to be negligible (e.g , less than 1%) or that it reflects special DBMSs or users not considered in this assignment. Second, there is currently a distinct trend towards an increasing number of DBMSs designed around the network model (e.g., CODASYL). Also not shown in the tables is the expectation among experts that DBMSs of the future will support multiple data models. Exactly when such a DBMS might appear on the market is not clear, but prototypes are anticipated to be in development by 1985 Third, the trend away from hierarchical models to network models raises the question of translating a data base from one model to another. To facilitate this process, at least one high-level translation language is expected to exist by 1983. It will be specialized (e.g., to translate IMS to IDMS on IBM), and such translation languages when they exist will continue to be specialized through 1985 and perhaps beyond.

8.4 DATA LANGUAGES

(Not available for Phase I)

8.5 DATA BASE ARCHITECTURE (HARDWARE)

A number of varied advances in the hardware technology will definitely impact the trends in DBMSs of the future. As a result of the increased prominence of DBMSs in the industry and the many computer-consuming functions in DBMSs, experts are anticipating the imminent development of a data base machine.

8.5.1 Data Base Machines

8.5.1.1 State of the Art in Data Base Machines - There are presently computers oriented toward DBMS, such as Datacomputer developed by Computer Corporation of America. This is basically a minicomputer operating as a "back-end" processor to perform data access and organization functions. A similar development is being undertaken by Cullinane. Reference 8-3 provides a summary of the use of dedicated DBMS processors in ongoing work. If these qualify as data machines, then data machines are already available or certainly will be in the very near future. However, since these examples demonstrate new uses for current general-purpose hardware technology rather than a new development in the hardware itself, the "back-end" processor systems being developed today do not qualify as data base machines for this assessment effort. Thus a data base machine does not exist today.

8.5.1.2 Trends in Data Base Machines - In a recent article, Baum and Hsiao (Ref 8-4) provide an excellent summary of current research and anticipated hardware technology trends which will significantly influence the characteristics of a data base machine. To summarize their view, the data base machine will have electronic mass storage (in conjunction with disk) and multiple, specialized processors and/or memory to perform DBMS functions (e.g., security checks). Other authorities consulted as a part of this effort further indicate that initially the specialized processors will perform conventional distinct functions that can be readily identified in present software. Examples include searching, sorting, security checking, data base accessing by key, hashing, and some editing of data. After a period of development, the machine described by Baum and Hsiao (Ref. 8-4) exhibiting hierarchical memory, sophisticated data clustering, and a full complement of subsidiary DBMS processors will emerge.

8.5 1.3 Projected Developments in Data Base Machines - Exactly when the first data base machine will exist is not clear because of the vague idea of what characterizes such a machine. However, as qualified in Sections 8 5 1.1 and 8.5.1.2, the first data base machine is not expected to appear on the market before 1982. Also, historical data indicate that only the largest mainframe vendors have the resources to introduce such a potentially radical development and succeed at generating widespread interest.

8.5.2 Other Hardware

(Not available for Phase I)

8.6 DISTRIBUTED DATA BASES

Since there is a diversity of opinion as to what is required for distributed data bases, an attempt was made to define those DBMS features that are considered to be minimal to support distributed data base processing, and then to project when a DBMS with those features will exist.

In assessing distributed data base processing, the following DBMS characteristics were considered to be minimal:

- Concurrent update protection at the record level
- Security protection at the data item level
- Multilevel access authority controls
- Redundancy controls
- Transaction switching/routing
- Global data base dictionary with centralized control
- Distributed recovery capability (plus some degree of centralized recovery).

Other features that might be desirable include: support of multiple data models, reentrant software, multithreading, standard communciations interfaces and protocols, monitoring of data usage, dynamic file allocation, retrieval by content, and modular hardware architecture.

8.6.1 State of the Art in Distributed Data Bases - There is not a commercially available, general-purpose DBMS in existence today that is designed to fulfill the minimal requirements of a distributed data base.

8 6.2 Trends in Distributed Data Bases

Current trends indicate that a variety of efforts will be devoted to developing the individual features described above without particular consideration of integrating all of them in a single DBMS.

8.6.3 Projected Developments in Distributed Data Bases

The results of the survey of experts indicate that a DBMS possessing all of those features considered minimal to support distributed data base processing will not appear before 1985. Isolated systems with partial capabilities will begin to appear, however, in the 1980-1982 timeframe.

8.7 STANDARDS

In the proceedings of the workshop co-sponsored by NBS and ACM (Ref. 8-5), the working panel on standardization reported four prominent areas related to DBMS for which standards are needed: terminology, criteria for evaluation of standards, components (e.g., data description language), and usage.

8.7.1 State of the Art in Standards

To date, the only viable DBMS standards proposal has been that of the CODASYL Data Base Task Group (DBTG). The DBTG report of April 1971 contains the specification of a schema langauge, a COBOL subschema language, and a COBOL data manipulation language oriented toward the network data model.

8.7.2 Trends in Standards

As a general rule, the next 5 years are expected to demonstrate an increasing interest in DBMS standards developments. In addition to the DBTG, there is also an ANSI subcommittee developing similar subschema and data manipulation capabilities for FORTRAN The status of this committee is not presently known.

8.7.3 Projected Developments in Standards

Many experts expect the proposed standards of the DBTG (or a moderately revised version thereof) to receive ANSI approval by 1980.

8.8 EFFICIENCY/PERFORMANCE EVALUATION

In the area of DBMS efficiency and performance evaluation, two aspects are considered: evaluation tools/techniques and evaluation results.

Reference 8-6 presents a survey of evaluation techniques. Although there are a number of analytical techniques under investigation, comparison of features and capabilities continues to be the most widely used technique for DBMS evaluation. As a result of the broad diversity of parameters influencing DBMS performance, simulation is expected to be the most useful tool for the near future.

Three of the most important performance parameters are storage overhead, CPU time, and data access time. Storage overhead is a ratio of storage consumed by the DBMS for retention and access of data (including the data, compressed or uncompressed) to storage consumed by the uncompressed data. Data access time reflects the non-CPU time consumed to retrieve requested data.

8.8.1 State of the Art in Efficiency/Performance

Storage overhead is primarily compressed disk overhead and varies widely from 50% to 400%. While data compression could be used to decrease storage overhead, it is presently used in only one or two DBMSs.

8.8.2 Trends in Efficiency/Performance

Since trends indicate utilization of large amounts of electronic storage in the future, storage overhead should not be limited to disks, as is typically done today. It is expected that any storage overhead that might be diminished because of hardware advances will be essentially reinstated via incorporation of new or additional capabilities not previously available.

With the use of additional subsidiary processors and or reentrant code, both CPU time and data access time consumed by DBMS will continue to decrease through 1985. It is anticipated that DBMS will exhibit the most significant decreases in CPU time in the 1980-1985 timeframe.

8.8.3 Projected Developments in Efficiency/Performance

Due to the recapturing of storage overhead by the addition of capabilities as described above, storage overhead is not expected to change appreciably by 1980, and perhaps may even increase by 1985. Due to projections in hardware technology, the period between 1980 and 1985 will exhibit the most significant decreases in CPU and data access times.

While other parameters may be of interest to specific installations, the above parameters are considered common to a wide variety of interests and applications for evaluation purposes. These and other identifiable DBMS performance parameters will be analyzed in more depth during subsequent program phases.

REFERENCES - SECTION 8

8-1 "Study of Systems and Techniques for Data Base Management", Teledyne Brown Engineering, March 1977

8-2. "Introduction to Input/Output Requirements Language (IORL)", Teledyne Brown Engineering, March 1977

8-3. "Data Base Directions -- The Next Steps", Data Base, ACM Special Interest Group on Business Data Processing, Vol 8, No 2, Fall 1976

8-4. Baum and Hsiao, "Database Computers -- A Step Toward Data Utilities", IEEE Transactions on Computers, Vol. C-25, No. 12, December 1976

8-5. A Survey of Existing Techniques for Evaluating Data Base Management Systems, CSC Field Services Division, Huntsville, Alabama, May 1975

8-6 "A Buyer's Guide to Data Base Management Systems", Datapro Research Corporation, May 1976

8-7. "Evaluation of Data-Base Management Systems", ACM Computing Surveys, Vol 8, No. 1, March 1976

8-8. R. Turn and W. H. Ware, "Privacy and Security Issues in Information Systems", IEEE Transactions on Computers, Vol. C-25, No. 12, December 1976

8-9. R. M. Curtice, "The Outlook for Data Base Management", Datamation, Vol. 22, No. 4, April 1976

8-10. V. Chvalovsky, "Anything New in Data Base Technology?", Datamation, Vol 22, No. 4, April 1976

9. INFORMATION DISTRIBUTION ELEMENTS

Information distribution elements may be considered in terms of the Level 1 physical distribution elements and electronic distribution elements presented in Figure 9-1. Physical distribution elements (messengers, mail, etc.) may be used to distribute data stored on physical media such as magnetic tape, disks, etc., as well as hardcopy presentations that include printouts, film, photographs, microfilm, and other hardcopy items. Physical distribution elements are not covered in this study, but physical distribution media are covered under data storage elements (Subsection 7.2) and information presentation elements (Section 10). Electronic distribution elements are covered in Subsection 9.1 (Telecommunication Networks) and Subsection 9.2 (Telecommunication Hardware). These Level 2 elements are further broken down (Figure 9-1) to include all elements that make up the interface between either two computers that are communicating with each other or a user and computer that are interacting.

The state of the art in telecommunications technology is discussed first in terms of capabilities offered by specific types of telecommunications networks. Although many of these capabilities are not pushing the state of the art in terms of what could be achieved, they are what is practical from an availability and cost viewpoint. Technology items that offer potential for increasing the capabilities available to users are assessed with emphasis on those techniques that offer potential for relatively low-cost wideband (video) data transfer.

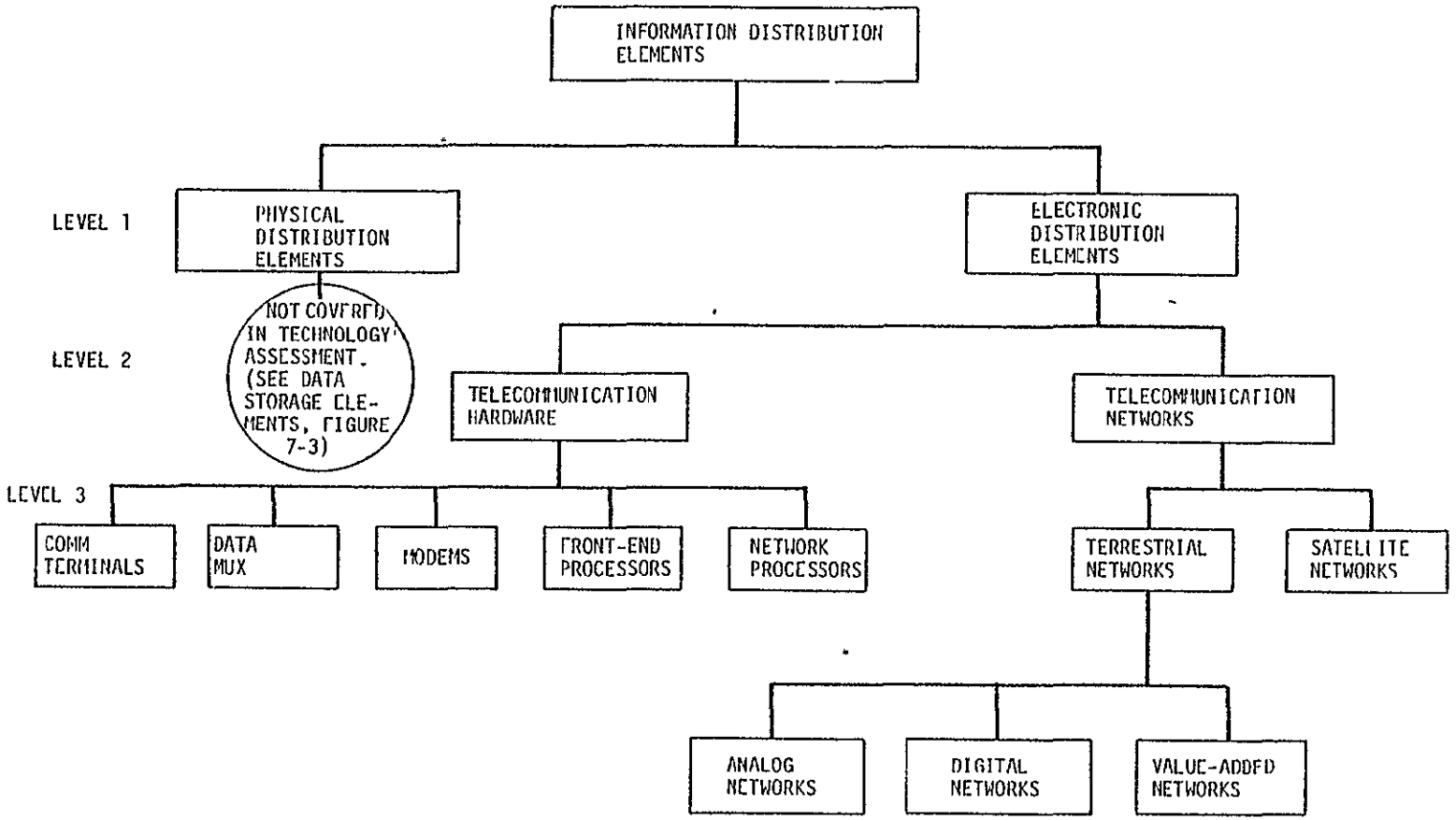


FIGURE 9-1. INFORMATION DISTRIBUTION ELEMENTS

9.1 TELECOMMUNICATION NETWORKS

Telecommunication networks may be characterized in a number of ways. The characterization in terms of terrestrial and satellite networks and the subsequent characterization of terrestrial networks into analog, digital, and value-added networks appears to be the most appropriate breakout for technology assessment purposes.

The capabilities and/or the technology are presented in terms of performance and cost for different types of networks, independent of whether they are common carrier networks, specialized common carrier networks, or private networks, except in instances where a carrier offers a special cost or performance advantage Subsequent efforts should establish a data bank on the specific services and tariffs offered by the different carriers.

Terrestrial networks will continue to provide the dominant method of interconnection for data communications in the early to mid 1980's, although long-haul links will tend to use more and more satellite channels. The average user, however, will interface to the satellite via a telephone line in lieu of having a satellite terminal. Also, the use of small satellite terminals, particularly for reception of wideband data, will grow at a rapid rate.

9.1.1 Terrestrial Networks

Terrestrial networks are generally characterized as analog or digital. Analog and digital networks are available from AT&T and a number of independent telephone companies (e.g., GTE) and from the specialized common carriers (MCI Telecommunications Corporation, Nebraska Consolidated Communications Company, Southern Pacific Communications Company, and a host of other companies. A third classification, which is generally digital in nature but which deserves separate coverage because of the services offered and the uniqueness of the service, is value-added networks. Subsequent subsections describe the services and the performance provided by the different types of networks. Cost data are discussed in relative terms where appropriate The complex nature and the changing status of tariffs require more detailed analysis than could be readily provided in this Phase I effort.

Although analog networks are the primary types of networks available at present, the trends and new technology developments are primarily related to digital networks. Also, much work is being performed in the area of satellite relay systems and value-added networks. The major developments in the area of analog networks is occurring in the equipment and techniques for interfacing to the network. As a result of the above facts, the major emphasis in this section of the study is on areas other than analog networks, although they still play a major role in telecommunications and probably will continue in this capacity into the mid-1980's.

9.1.1.1 State of the Art in Analog Networks - The primary networks available within the United States today (the public switched network, Type 3002 leased lines and equivalent, etc.) are analog in nature and offer 3-kHz bandwidth in the frequency range from 300 to 3,300 Hz. These 3-kHz channels are available as either dial-up or leased lines, depending on the type of service subscribed to. Table 9.1.1.1-1 lists the basic types of service available (the list is not comprehensive, but is representative) via analog networks and the bit-rate capability for each service. The information is presented without regard to whether the channel is provided via a hardwire (open wires or coaxial cable) or a microwave link. Although this subsection is intended to cover terrestrial networks, the services listed in this table could be provided by a satellite link.

All digital services via analog networks require the use of modems. Modem technology, which is primarily responsible for the high bit rates achievable via voice-grade lines, is discussed in Subsection 9.2.1.

TABLE 9.1.1.1-1. TYPICAL ANALOG NETWORK SERVICES WITHIN THE UNITED STATES

TYPE SERVICE	BANDWIDTH (kHz)	MAXIMUM BIT RATES (bps)	OFFERED BY	COMMENTS
Dial Up Lines				
Subvoice Grade		To 180	Western Union	
Direct Distance Dialed (DDD) Network	3	To 4,800	AT&T, GTE, and Others	
Wide Area Telephone Service (WATS)	3	To 4,800	AT&T	Leased
BEX Service		To 38,400*	Western Union	Switched service Available in certain areas only
Leased Lines				
Subvoice Grade		To 180	AT&T and WU	
Voice Grade Lines	3	To 9,600	AT&T, WU, and Specialized Common Carriers	C1, C2, and C4 conditioning available
Wideband	To 240	To 230,400	AT&T and Specialized Common Carriers	Available in Groups (12 voice-grade lines), Super Groups (60 voice-grade lines) and Master Groups (240 voice-grade lines)

*Dependent on modems Higher rates may be achieved.

9.1.1.2 State of the Art in Digital Networks - Digital networks offer a number of advantages over analog networks for transmitting digital data, but at the same time they present some unique problems. Probably chief on the list of advantages is the ability for virtually error-free transmission through the use of regenerators at periodic intervals along the transmission path. Among the unique problems is the need for the regenerators, which dictates the need for a network that is especially constructed to handle digital data. Analog data that are transmitted on the network must be digitized and transmitted as digital bits This type of conversion is being performed on voice data using a device designated as a Codec, which stands for coder/decoder. Voice data are sampled at a rate of 8,000 samples/sec, and the samples are coded using an 8-bit code Thus the bit rate for one voice channel is 64 kbps. In spite of the apparent high bit rate, the telephone company saves significant amounts of money through the use of the large capacity and smaller size digital switches, compared with existing analog equipment. The increased throughput per unit size means fewer buildings to house equipment, less power consumption, more efficient use of transmission trunks, and more economic expansion. In view of these increased savings, telephone companies are increasing their digital networks at the rate of tens of millions of circuit miles per year

Although digital data networks are growing at a rapid rate and a number of the specialized common carrier and private networks offer digital services, the principal digital network and the one that is in the forefront from the standpoint of digital technology is AT&T's DataPhone Digital Service (DDS). This network currently serves 24 cities [plans call for offering the service to more than 100 cities (see Table 9.1.1.2-1)], offering services at data rates from 2.4 to 1.544 Mbps.

The DDS user is multiplexed onto a T1 (1.544-Mbps) line, and eventually multiplexed onto the higher-data-rate links via the digital hierarchy used by the Bell system. The digital hierarchy for North America, Western Europe, and Japan is presented in Figure 9 1.1.2-1.

TABLE 9.1 1.2-1. CITIES TO BE SERVED BY DDS

Boston, New York, Washington, D C , Philadelphia, Chicago
Baltimore, Pittsburgh
St. Louis
Cleveland
Newark
Detroit
Kansas City
Dallas
New Haven, Denver
Hartford, Los Angeles
Atlanta
Milwaukee, San Francisco
Houston, Miami
Portland, Minneapolis
Camden, Seattle, Indianapolis, Mercerville (Trenton), Salt Lake City, White Plains
Wilmington, Memphis, Springfield, Massachusetts
Inglewood, California, East Bay, California, Omaha
Anaheim, California, Mountain View, California, Albany, Orlando, Buffalo
Charlotte, Phoenix, Columbus, Akron, Oklahoma City, Syracuse, Rochester
Des Moines, Sacramento, Dayton, San Diego
Tulsa, Cincinnati, Providence, Harrisburg, New Orleans
Birmingham, Toledo, Worcester, Allentown
Jacksonville, Louisville, Huntsville, Raleigh, Nashville
Greenville, Tampa, Richmond, Youngstown
Spokane, Reno, Shreveport, Colorado Springs
Greensboro, North Carolina, Norfolk, Fresno, Knoxville, South Bend
Wichita, Ventura, Albuquerque, Las Vegas, Lansing
Fort Wayne, El Paso, Lincoln, Chattanooga, Reading
Grand Rapids, Peoria, San Antonio, Baton Rouge, Madison
Flint, E. Moline, Little Rock, Roanoke, Cedar Rapids

(First 24 cities already in service. Remaining service to be provided in approximate order of listing)

NOTES

NUMBERS IN PARENTHESES REPRESENT THE NUMBER OF 64-kbps TIME SLOTS. FIRST NUMBER IS THE BIT RATE IN kbps

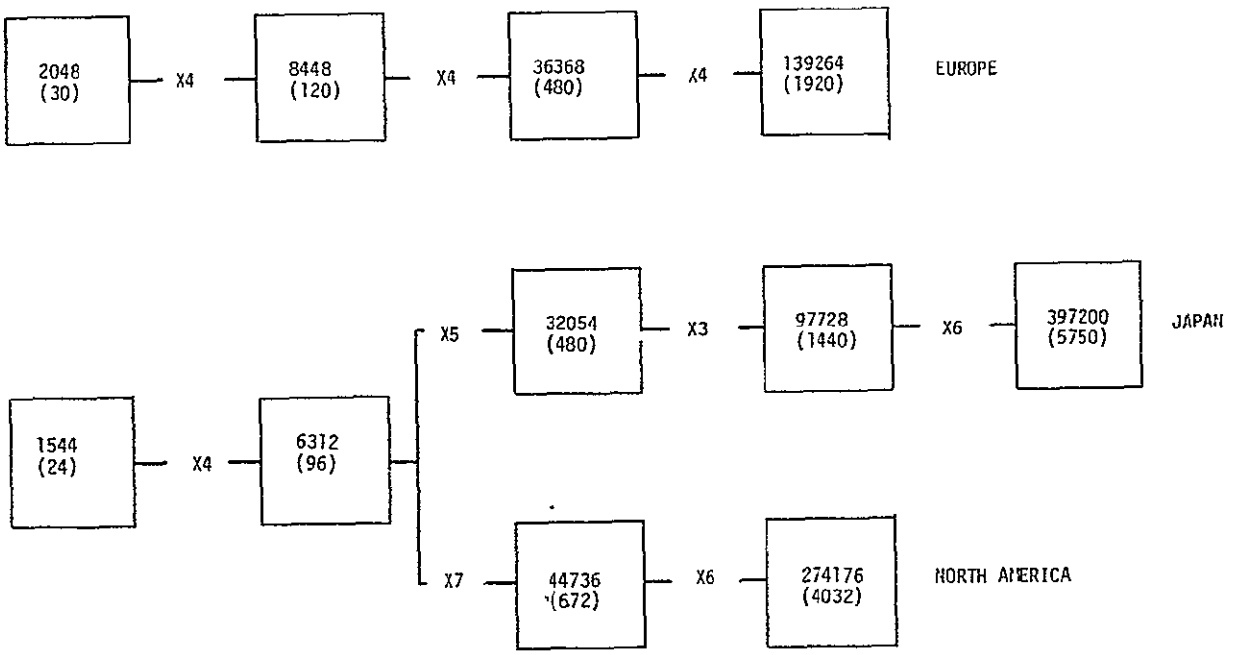


FIGURE 9.1.1 2-1. DIGITAL COMMUNICATION NETWORK HIERARCHY

The present telephone networks utilize the four lower levels of the hierarchy At this time, the fifth level has not been implemented.

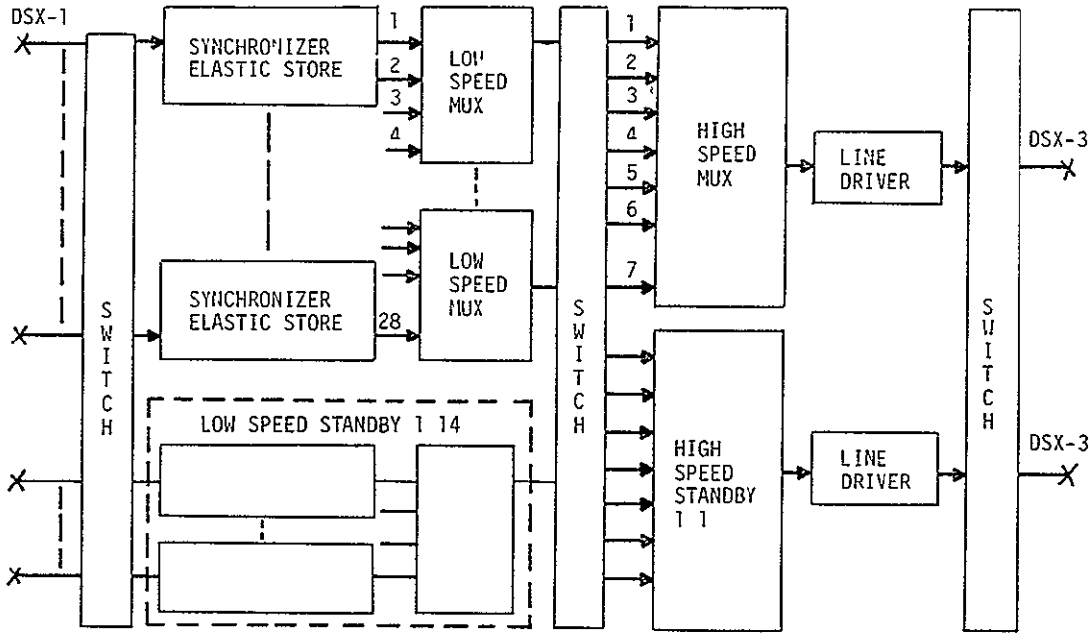
A number of technology developments are ongoing to better utilize and extend the capabilities of the digital networks. Among these developments are work to increase the throughput rate of digital multiplexers and work to provide higher performance channels using digital radio, various improved cable systems, waveguide system, and optical fibers.

Multiplexer technology was discussed in Section 4 (Space Data Handling), and the same technology is being applied to ground networks. Extensive use of integrated circuit devices, particularly ECL and Schottky TTL logic, are enabling the development of high-speed multiplexers that will extend the hierarchy by as much as a factor of four The use of these devices on terrestrial networks is not as constrained in power, size, etc., as it is for space data handling systems. Thus operational, commercially available, high-rate systems can be expected much sooner than in space.

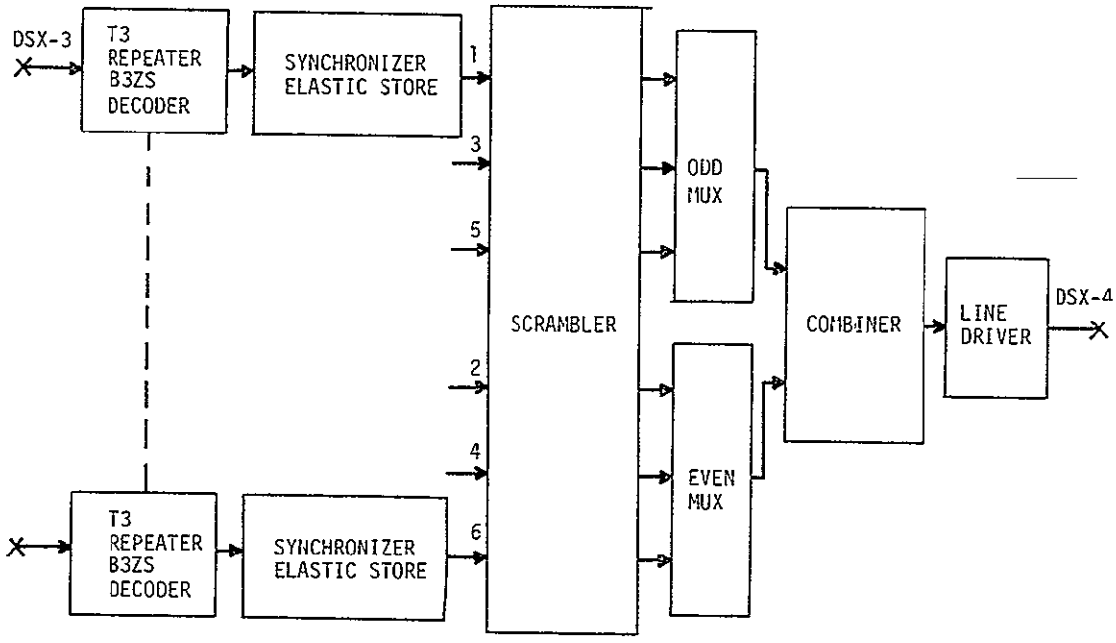
The state of the art in operational multiplexers is considered by some to be approximately 140 Mbps (Ref. 9-1), although AT&T has had a 274.176-Mbps system (the M34 digital multiplexer) in operation between Newark, New Jersey, and New York City since early 1975. The system is a limited-availability system and was under test initially. The performance has been excellent and the system may be available soon for widespread use, if this has not already taken place.

The M34 system configuration is illustrated in Figure 9.1.1.2-2, along with the M13 digital multiplexer, which is a 44.736-Mbps system. The multiplexer characteristics and frame and stuffing performance are presented in Table 9.1.1.2-2.

The majority of the circuits in the M13 multiplexer used low-power TTL logic DIPs. The M34 circuits required high-speed ECL devices. However, by multiplexing in two stages and interleaving the two 137-Mbps bit streams at the last instant, it was possible to limit the very high-speed (approximately 1-nsec) logic to as little as 4% of the total number of DIPs For more information on either or both of these multiplexers, refer to Reference 9-2.



a M13 Multiplexer Configuration



b M34 Multiplexer Configuration

FIGURE 9 1.1.2-2. M13 AND M34 MULTIPLEXER CONFIGURATIONS (Ref. 9-2)

TABLE 9.1.1.2-2 M13 AND M34 MULTIPLEXER CHARACTERISTICS AND PERFORMANCE (Ref 9-2)

MULTIPLEXER CHARACTERISTIC	M13		M34
	LS MUX	HS MUX	
Output Rate (Mbps)	6 312	44 736	274 176
Stability (ppm)	±20	±20	±10
Frame Length	294	680	196
Superframe Length	1,176	4,760	4,704
Average Maximum Reframe Time (μsec)	7,050	1,280	120
Nominal Stuff Rate (Hz)	1,800	3,655	27,429
Maximum Stuff Rate (Hz)	5,367	9,398	58,286
Stuff Ratio (%)	33.5	38.9	47.1

PERFORMANCE / ERROR RATE	MEAN TIME BETWEEN MISFRAMES (sec)		MEAN TIME BETWEEN IMPROPER DESTUFFS PER CHANNEL (sec)	
	M13	M34	M13	M34
10^{-6}	2×10^{12}	1.2×10^{9}	2.2×10^{7}	$4\ 7 \times 10^{9}$
10^{-3}	3.4×10^{3}	$4\ 5 \times 10^{1}$	$2\ 4 \times 10^{1}$	$1\ 7 \times 10^{3}$

In the area of laboratory systems, at least one European Company (Ref. 9-1) is working on a multiplexer capable of throughputting 565.148 Mbps to handle the fifth level of the digital hierarchy in Europe. The system under investigation consists of a pure digital chain and a 2.6- to 9.5-mm coaxial cable.

The digital network that uses the M34 multiplexer discussed above is designated as the T4 digital transmission system. The system is capable of accepting 168 DS1 (1.544 Mbps) signals over one pair of coaxial tubes designated as the T4M line. This line requires regenerators at distances no greater than 5,700 ft along the transmission path. A T4M line consists of maintenance spans up to 111 mi. in length, which may be connected in tandem for a total system length up to 500 mi. Future plans call for implementation of DS4 carriers via WT4 millimeter waveguide systems and via the DR-18 digital radio system.

Another important area of ongoing research and development in digital network technology is optical transmission of voice and data Fiber-optic transmission systems offer significant advantages over coaxial cable and metallic wire, including increased bandwidth, smaller diameter, lower weight, lack of crosstalk, and immunity to inductive interference. In addition, the cost is significantly less than wire/coaxial systems.

Bell Laboratories recently (in 1976) installed two experimental fiber-optic cables in underground ducts in Atlanta, Georgia, and ran tests that simulate a typical urban communications environment (Ref. 9-3). The system used GaAs injection lasers to convert digital signals into light pulses. On the receiving end, avalanche photodiodes convert the light into electrical signals, while timing and decision circuits regenerate clean output pulses.

An article in the February 1977 issue of IEEE Spectrum entitled "Optical Transmission of Voice and Data" by Ira Jacobs and Stewart E. Miller of Bell Laboratories states that the allowable pulse rate via optical fibers is inversely proportional to fiber length and that modal

dispersion in a step-index fiber with a 1% index difference permits a pulse-rate/length product of 18 Mbps/km. Seventy-five times that figure has been realized in the laboratory for graded-index fibers, and another factor of ten is theoretically achievable The same article states that if the installed cost of fiber were five times that of a wire pair, at a capacity of 1,000 circuits, optical fiber would still be ten times less expensive than video cable.

9.1.1.3 State of the Art in Value-Added Networks - Value-added networks, sometimes referred to as packet-switching networks, represent a dynamic force in the area of data communications. Since the implementation of the first such network by the Advanced Research Projects Agency, known as the ARPANET, this method of data transmission has received wide attention. Today, such networks are either available or being implemented on a worldwide basis. A recent listing (Ref. 9-4) included TELENET's Intelligent network in the United States, DATAPAC in Canada, TRANSPAC in France, CYCLADES also in France, EPSS in the United Kingdom, the European Integrated Network across Europe, TIDAS in Sweden, and a number of others currently being considered (e.g., the U.S. Autodin II net).

ARPANET, the oldest of the packet-switching networks, now interconnects approximately 100 computers in the CONUS, Hawaii, and Europe. TELENET currently serves some 250 users in 47 cities in the CONUS and Canada. TELENET expects to add another 38 cities in 1977.

TELENET Corporation and RCA Global Communications, Inc., have recently entered into an agreement whereby RCS Globcom provides the overseas data transmission facilities and the gateway switching equipment linking the TELENET network and its users in the United States with packet-switching facilities in the United Kingdom and Western European countries. In addition, TELENET has primarily entered into an agreement with Teleinformatica de Mexico to provide a computer communication service between the United States and Mexico. The rates filed with the FCC for this latter service are $5.30 per kilopacket (128K characters) regardless of distance.

TYMNET, another U.S. network, is providing service to 61 cities in CONUS. This should be expanded to 105 cities by 1979.

Typical value-added networks operate with 1,024 bit packets. The data rate between user and network terminal is 9.6 kbps or less with a 56-kbps rate within the network.

9.1.1.4 Trends in Terrestrial Networks - The trend in terrestrial networks is clearly toward an all-digital network for better or worse The existing investment in analog networks and the advancements in modem technology will have an effect on when or if digital networks will overtake analog networks in terms of numbers of channels. Other trends include higher rates of multiplexing in the digital hierarchy around the world, the probable use of fiber-optics in new trunks in the immediate future, and a continued proliferation of value-added or packet-switching networks, including the interconnection of packet-switched networks on a worldwide basis. Also, the use of combined terrestrial and satellite networks will grow significantly, where low-rate users are tied into satellite networks via local ground networks (analog, digital, and value-added) that feed into satellite ground stations.

9.1.1.5 Projected Developments in Terrestrial Networks - All authorities agree that networks will still be primarily analog in 1980 with a continued strong trend toward digital networks. By 1985, the major long-haul networks will probably be digital with continued dominance of analog circuits to subscribers, but with trends still toward an all-digital network.

There appears to be general agreement that data rates over voice-grade lines will increase in the 1980-1985 timeframe (possibly by 1980), but the increase will be the result of improvements that result from software techniques and modem hardware. Authorities tend to agree that baud rates of 9,600 bps should be achievable on multipoint lines in the 1980-1985 timeframe, primarily because of the reduction in acquisition time within the modems. Further, the opinions are that point-to-point communication lines will exceed 9,600 bps, but not by a factor of more than 1.5 by 1980. Rome Air Development Center recently (February or March 1977) awarded a contract to Harris Radiation Laboratories to build a 16-kbit modem. When or if such units would be available commercially is not known.

The general feeling among the authorities is that it will be reasonable to transmit at least 9,600 bps over switched voice-grade lines (e.g., the DDD network) in the 1980-1985 timeframe. The rate could potentially exceed this if the links are digital between the AT&T switches.

Responses from authorities in the telecommunications field indicate that optical fibers will begin to be used extensively in communication networks in the 1980-1985 time period. A number of European PTT organizations, as well as the United States Bell System, are currently implementing trial systems. Further, a number of authorities foresee limited operational usage of optical fibers for communications in ships, airplanes, and possibly spacecraft as early as the end of this decade. By 1980, optical fiber will be used for moderate systems requiring no repeaters, systems for which size and weight are important parameters, and systems well-suited to digital techniques. By 1985, optical fibers will be used for prototype systems on a long-haul basis.

9.1.2 Satellite Networks

This section addresses satellite network technology from the viewpoint of the availability and characteristics of satellite networks for telecommunications. Other aspects of satellite technology, such as orbiting spacecraft-to-ground communications and hardware components (transmitters, receivers, antennas, etc) were presented in Section 5.

9.1.2.1 State of the Art in Satellite Networks - Satellite networks for telecommunications have been in existence since 1965 when the first Intelsat was placed in orbit to provide communications coverage between the United States and Western Europe. Since that time, both the number of communication satellites and the number of satellite networks have grown rapidly. The number of satellites is less than the number of networks since a number of networks lease satellite channels and provide a network via these leased channels in lieu of having their own satellite. The state of the art in telecommunications satellite technology and the known future plans for telecommunications satellites were presented in a March 1977 article in the IEEE Proceedings entitled "Satellite Communications - An Overview of the Problems and Programs", by W. S. Prichard (Ref. 9-5). Tables 9.1.2.1-1 through 9.1.2.1-3, which were extracted from this article, identify the existing and planned systems and their characteristics. Specifically, Table 9.1.2.1-1 identifies the existing and planned telecommunication satellite network programs along with their class, coverage, status, planned or actual operational dates, and operational frequency bands. Table 9.1.2.1-2 presents the system characteristics for key systems with emphasis on modulation and multiple-access characteristics, ground antenna size, and throughput capacity. Finally, Table 9.1.2.1-3 presents the U.S. domestic satellite systems, along with Earth station locations, services offered, the satellite being used, and the status. Table 9.1.2 1-4 expands the key acronyms that are used in the preceding tables.

TABLE 9.1.2 1-1 SATELLITE NETWORK PROGRAMS

	Program	Class						Coverage		Status				First Operational Date -- Actual or Planning	Frequency Bands (GHz)	
		Fixed	Mobile	Broadcast	Experimental	Military	Proposed	Regional	Domestic	Operational	Under Construction	In planning	Under Construction			
1	INTELSAT	X						X		X				1965	5925 - 6425 up	3700 - 4200 down (C Band)
2	USSR	X						X	X	X				1965	5725 - 6225 up	3400 - 3900, 800 - 1000 down
3	TELESAT - Canada	X							X	X				1973	5927 - 6403	3702 - 4178
4	Western Union	X							X	X				1974	5925 - 6425	3700 - 4200
5	RCA SATCOM	X							X	X	X			1974	Same as WESTAR	
6	AMERICAN SATELLITE CORP.*	X							X	X				1974	WESTAR Transponder	
7	COMSAT/ATT (COMSTAR)	X							X	X				1976	5925 - 6425	3700 - 4200
8	ESA (OTS/ECS)	X						X			X			1977	14152 5 - 14192 5	11490 - 11530
															14242 5 - 14362 5	11580 - 11700
															14455 0 - 14460	11792 5 - 11797 5
9	ALGERIA*	X							X	X				1975	INTELSAT Transponder	
10	INDONESIA	X							X	X				1976	5925 - 6425	3700 - 4200
11	NORWAY/NORTH SEA	X						X			X			1975	INTELSAT Transponder	
12	SBS	X							X			X		1978	14000 - 14500	11700 - 12200 Ku Band
13	PHILIPPINES*	X							X				X	1976	5925 - 6425	3700 - 4200
14	INDIA	X		X					X				X	?	C or Ku	2500 B'cast
15	ARAB SYSTEM	X						X					X	1980-90	C Band	2500 B'cast
16	COMSAT GENERAL (MARISAT)		X					X	X					1975	Satellite - Ship	Satellite - Shore
															300 - 312 1638 5 - 1642 5 up	6174 5 - 6425 up
															248 - 260 1537 - 1541 down	3945 4 - 4199 0 down
17	ESA/COMSAT GENERAL (AEROSAT)		X					X				X		1979	Satellite - Plane	Satellite - Ground
															1645 - 1660	131 425 - 131 975 up 5000 - 5125 up
															1543 5 - 1558 5	125 425 - 125 975 down 5125 - 5250 down
18	ESA (MAROTS)		X					X			X			1977	Satellite - Ship	Satellite - Shore
															1641 5 - 1644 5 up	14490 - 14500 up
															1540 - 1542 5 down	11690 - 11700 down
19	IMCO (INMARSAT)		X					X					X	1980+	Satellite - Ship	Satellite Shore
															L Band	C or Ku Band
20	EUROPEAN BROADCASTING UNION			X				X					X	1980+	Ku Band	
21	FEDERAL REPUBLIC OF GERMANY			X					X				X	~1985	Ku Band	
22	SYMPHONIE				X			X		X				1975	5926 - 6424 up	3700 - 4200 down
23	ATS-6				X				X	X				1974	Wide variety of experiments in K, C, S, UHF, and VHF Bands	
24	JAPAN - COMMUNICATION	X			X				X		X			1977	5925 - 6425	3700 - 4200
															30 000	20 000
25	JAPAN - BROADCAST			X	X				X		X			1978	14 000	12 000
26	CTS				X			X			X			1975	14 000	12 000
27	SERIO				X				X		X			1977	17009 - 17782	11331 - 11862
28	DSCS	X	X			X		X		X	X			1966	7900 - 8400	7250 - 7750
29	SKYNET	X	X			X				X				1969	7976 - 8005	7257 - 7286
30	NATO	X	X			X				X				1970	7975 - 8162	7250 - 7437
31	FLTSATCOM	X	X			X		X			X			1977	Satellite - Ship	Satellite - Shore
															225 - 400	7900 - 8400
32	LES SERIES	X	X		X	X		X		X				1965	Wide variety of experiments at UHF and X Bands	
33	ANDEAN NATIONS*	X					X	*	?				X	?	INTELSAT Transponder	
34	ARGENTINA*	X					X		X				X	?	INTELSAT Transponder	
35	AUSTRALIA	X					X		X				X	1980's	C Band, Au, S Band	
36	BRAZIL	X		?		?	X		X			X		1978	5925 - 6425	3700 - 4200
37	DENMARK*	X					X		X				X	?	INTELSAT Transponder	
38	IRAN	X		?		?	X		X				X	?	--	
39	MALAYSIA*	X					X		X				X	1975	INTELSAT Transponder	
40	UNITED KINGDOM						*						*		--	
41	SYSTEMS USING INTELSAT*	X	X				X			X	X		X	Various	INTELSAT Transponder	
42	ASEAN NATIONS	X					X	?	X				X			

* Earth Stations Only

From Wilbur L. Pritchard, "Satellite Communications - An Overview of the Problems and Programs", Reference 9-5

TABLE 9 1.2 1-2 SATELLITE NETWORK SYSTEM CHARACTERISTICS

	SYSTEM	MODULATION AND MULTIPLE ACCESS	EARTH STATION ANTENNA DIAMETER	CAPACITY PER SATELLITE
1	INTELSAT IV INTELSAT IV-A	FM/Video FDM/FM/FDMA	29 5 M for Std A 13 M for Std B 29 5 M	7500 channels + SPADE + T, 12 000 channels + SPADE + TV
2	U S S R - MOLNIA	FM	12 M 25 M	1 TV channel + unspecified telephones
3	TELESAT - Canada	Single carrier FM Multi carrier FM Single channel/ carrier Delta modulation PSK TDMA	Heavy Route - 30M Network TV - 10 1 M Northern 10 1 M Tele-communications Remote TV 8 1M / 4 7M Thin Route 8 1M / 4 7M	12 transponders of 36 MHz bandwidth
4	WESTERN UNION - (WESTAR)	• SSB/FM/FDM Single & Multiple Access Video SCPC: PSK/TDM/TDMA	15 5M	12 Video channels (one way) or 14 400 FDM Voice channels (one way)
5	RCA SATCOM	FDMA FDM/FM & PCM/PSK for voice data 4 PSK for digital data, FM for monochrome or color TV TDMA PCM/PSK for voice/ data	10M	24 Video channels w/34 MHz bandwidth 9000 channels/transponder
7	COMSAT/ATT- (COMSTAR)	FDM/FM Digital Transmission 4PSK	30M	28 800 one-way tele-phony channels or >1 000 mb/s data
8	ESA (OTS/ECS)	4-Phase PSK FM Video TDMA	Eurobeam A 13M + Spot Beam Eurobeam B 3M	1-120 MHz Transponder 1-40 MHz Transponder 1-5 MHz Transponder
10	INDONESIA	FDM/FM Multiple carriers per transponder SCPC/FM demand-assigned	9 8M 7 3M 4 0M	
16	COMSAT GENERAL (MARISAT)	Voice SCPC-FM Data 2-Phase coherent PSK	1 22M mobile terminals 12 8M shore terminals	9 voice channels (both ways) 110 teleprinter channels (both ways)
17	ESA/COMSAT GENERAL (AEROSAT)	Voice NBFM PDM and/or VSDM Data PSK/FSK	Low gain airborne antennas	5-80 kHz comm ch for ground-to-air and surveillance 15-40 kHz comm ch for air-to-ground 2-80 kHz comm ch for ground-to-ground 1-400 kHz or 10 MHz experimental channels
18	ESA (MAROTS)	FDM TDM FDMA TDMA	About 1M	Shore-to-ship Up to 50 voice/high-speed data channels Ship-to-shore: Up to 60 voice/high-speed data channels Shore-to-shore Up to 3 voice/high-speed data channels

TABLE 9.1.2.1-3. DOMESTIC SATELLITE SYSTEMS

COMPANY	EARTH STATION LOCATIONS	SERVICES	SATELLITES	STATUS
Western Union	New York Chicago Los Angeles Dallas Atlanta Honolulu	Data, voice, and video leased private line	Two 12-channel HS-333's (WESTAR) satellites built by Hughes Aircraft Company	Operational July 1974
American Satellite (A S C)	New York Los Angeles Dallas Fairchild AFB, WA Loring AFB, ME Centerville Beach, CA Moffett Field, CA Offutt AFB, NB Monterrey, CA Chicopee, MA Orlando, FL San Francisco	Data, voice, and video leased private line	Phase 1 Lease of 3 channels in WESTAR Phase 2 12-channel HS-333's	Operational July 1974
RCA Global Communications RCA Alaska Communications (RCA)	New York Los Angeles San Francisco Juneau, AK Honolulu Washington, DC San Juan, PR Houston Prudhoe Bay, AK Cordova, AK Nome, AK Valdez, AK Talkeetna, AK Bethel, AK Yakutat, AK	Data voice, and video leased private line plus MTT within Alaska and between Alaska and CONUS	Phase 1 Lease of 2 channels in ANIK (or WESTAR) Phase 2 Two 24-channel satellites built by RCA Astro-Electronics	Operational January 1974
AT&T and GTE Satellite	New York Chicago San Francisco Atlanta Los Angeles Tampa Honolulu	MTT (no private line except to the U S Government for three years)	Leased from Comsat General by AT&T	Earth station authorizations granted
Comsat General	TT&C only (Santa Paula, CA and Southbury, CT	Lease of transponders to AT&T	Three 24-channel satellites (modification of INTELSAT IV) built by Hughes Aircraft Company	Leased to AT&T
General Electric Company	Valley Forge, PA Daytona Beach, FL	Company communications, equipment and system development	Transponders leased from Western Union	Operational

TABLE 9 1.2.1-4 ACRONYMS

DPSK	Differential Phase Shift Keyed
QPSK	Quadriphase Shift Keyed
FDMA	Frequency Division Multiple Access
TDMA	Time Division Multiple Access
SCPC	Signal Channel Per Carrier
SPADE	Single-channel-per-carrier PCM Multiple Access Demand-Assigned Equipment

9.1.2.2 Trends in Satellite Networks - The general trend in data systems is to transmit more data in less time. Future satellites will increase in capability for a number of reasons. Frequency re-use will become common as a scheme to double the transmission capacity at any one frequency by using orthogonal polarization to keep two different data signals separate. This frequency re-use scheme will be used in the 4- to 6-GHz band and at higher frequencies.

The 11- to 14-GHz band will be used to provide more channels and greater bandwidth. Later, the 20- to 30-GHz band will be used. Transmitting power in both 4- to 6- and 11- to 14-GHz bands will increase. This power increase will be made possible by 1) better TWTs capable of higher power and higher efficiency (the Canadian CTS satellite has developed a 200-W TWT operating at 12 GHz with 50% efficiency), 2) increased prime power collection capability, and 3) more directive antenna patterns. As with all systems, cost is a major factor. The launch costs of future satellites launched from the Space Shuttle will be an estimated 40% less than current costs. This will allow more of the system budget to be spent on the spacecraft itself. Also, heavier spacecraft will be used.

Multiple antenna feed systems will have lower loss and greater ability to point a spot beam where it is needed. This is consistent with a greater use of demand assignment systems. These systems will be used more because they make greater use of the system capability and minimize idle time on the links. The beam selection will be controlled by the network controller.

Changes in the ground stations will also occur. Because of the higher frequencies and/or higher power, smaller ground station antennas will be used. Depending on the type of signal, antennas will range from 10 m for high-rate digital data down to 0.6 m for TV reception from high-power satellites. Receivers will also be smaller because of better semiconductor components (See Section 5.5, Microwave Receivers). Uncooled low-noise amplifiers will become common because of advances in GaAs FETs and IMPATT devices.

9.1 2.3 Projected Developments in Satellite Networks - While the 4- to 6-GHz band will continue to be used, the 11- to 14-GHz band will become widely used. RF bandwidths of 85 MHz (versus current bandwidths of 36 MHz) will be common, with some systems having a few links with 250-MHz bandwidth Transmitted powers of 200 W will be common, with some systems capable of 500 W.

Ground stations for the 11- to 14-GHz band will use 5-m antennas for the most part. Some receive-only stations for TV will use 1- to 2-m antennas. Small terminals can be configured for transmission of wideband space data via links such as these Although the cost for use of a wideband channel is relatively high, the per-user cost could be low if transmissions were scheduled ahead of time and if multiple users received the data that are transmitted in a broadcast mode.

Satellite antenna beamwidths will be narrower and beam shape and beam pointing will be controlled by the data link controller for demand assignment.

By 1980 some systems will be expanding into the 20/30 GHz band with RF bandwidths of 500 MHz being common.

9 2 TELECOMMUNICATIONS HARDWARE

Telecommunications hardware includes all the terminal and interface equipment, except the long lines or radio links, that make up a communications network. These include terminals, data multiplexers, modems, front-end processors, and network processors. Modems and network processors are covered briefly in this report Limited coverage of certain types of terminals is provided in Section 10. Future reports will provide more extensive coverage of modem and network processor technology and will be expanded to cover areas not included in this first program phase.

9.2.1 Modems

Modems (short for modulator/demodulator) are used to interface digital bitstreams onto analog communication channels. Thus modems provide a translation of digital data from a baseband pulse train to a modulated carrier that fits within the 300- to 3 3-kHz bandpass of voice-grade telecommunication channels. In the process, modems use sophisticated modulation and equalization schemes to achieve bit rates that would exceed the channel capacity under normal conditions. Indeed, advances in modem technology account for most of the major improvements in telecommunication channel performance during recent years.

9.2.1.1 State of the Art in Modems - Modems are classified as either synchronous or asynchronous depending on whether the receiving terminal is in phase with the sending terminal or whether the two terminals do not require synchronization. Asynchronous modems operate in a stop-start mode and typically are restricted to data rates of 1,200 bps or less. Frequency-shift-keyed modulation is normally used with asynchronous modems and detection is performed nonsynchronously.

Data rates in excess of 2 kbps require synchronous modems. Sophisticated m-ary modulation techniques are used on these modems ranging from quadriphase modulation for 2,400 bps to 16-phase modulation for 9,600 bps. Multiline modems are available that are capable of handling 19.2 kbps over two voice-grade lines.

Until recently, line equalization was accomplished with passive filters in both the transmitter and the receiver Newer modems are using both active and digital filters, and the higher-data-rate modems are using adaptive digital equalizers.

9 2 1.2 - Trends and Projected Developments in Modem Technology - Trends in modem technology are based on the use of LSI circuitry to reduce power consumption, size, and cost as a function of performance (actual cost may increase) while at the same time increasing bit-rates, reliability, and error performance. The advances in network technology projected advances in modem technology. Baud rates of 9,600 bps should be achievable on multipoint lines, including the switched network, and point-to-point communications should be capable of rates to 14,000 bps within the projected timeframe. Custom-designed, very-high-cost systems may be available at rates to 16 kpbs. Error performance will be better than for equivalent circuits today, but the projected error performance for these higher-data-rate circuits is not available.

9.2.2 Front-End Processors

A front-end processor, by definition, is located with the host computer Its primary functions are to control and monitor the interface between the communication network and the host computer. It may function to conserve the host computer's resources by assuming all or part of the communication network management. Commonly the front-end processor functions include code conversion, data speed and code recognition, message assembly, error control and recovery, compilation of system statistics, message validation, auto dialing, and polling.

9.2.2.1 State of the Art in Front-End Processors - Front-end processors can be divided into two basic types hardwired and programmable. These types range from single channels to complex, self-actuated network systems.

Hardwired controllers are designed to accommodate a wide variety of asynchronous and synchronous terminals over a braod range of data rates with a variety of codes. One disadvantage of the hardwired controller is the number of lines that can be handled. Another limitation is a general inflexibility as well as difficulty in changing the network interfaces. With the advent of the programmable front-end processor, hardwired units were supposed to fall by the wayside. However, since many IBM 360 systems are not only still in use but still in demand, many hardwired front-ends will be around from some time.

The programmable front-end differs from the hardwired unit in having a programmable processor between the host interface and the line interface hardware. A typical programmable front-end will consist of a host computer interface, a communications multiplexer, a number of line adaptors, and the processor. Processors are primarily minicomputers with 4 to 256 kbytes of memory. Programmable front-ends will eventually account for over half of all future communications processing equipment activity because the host computer can be relieved of significant burdens Table 9 2.2.1-1 shows the current capabilities of some representative front-end processors

TABLE 9.2.4-1. FRONT-END PROCESSOR CHARACTERISTICS

MANUFACTURER AND MODEL	YEAR INTRODUCED	LINES		MEMORY SIZE (kbytes)	NUMBER OF HOSTS	WORD SIZE (bits)	COST ($K)	STORAGE MEDIUM	MEMORY SIZE (kbits)	OTHER FEATURES
		NUMBER	RATE (kbps)							
Computer Communications, Inc										
CC-8	1975	64	230	128	2	16	88 9	MOS	16 to 128	Peripherals card reader, line printer, fixed-head disc, movable-head disc
CC-80	1975	960	230	512	7	16	117 8	MOS	16 to 512	
Counter 3670	1972	384	230	3 2	4	16	70 + options	Core	16 to 512	Dynamic line/subchannel assignment, automatic baud rate detection, full-duplex BSC can be used as concentrator or concentrator/controller
Honeywell 6670	N/A	N/A	50	64	6	18	190	Semiconductor	N/A	Any combination of duplex or full duplex operation
IBM 3705-II	1976	352	56	252	2	16/32	N/A	Monolithic FET	32 to 256	Can be used as line concentrator
Memorex 1380	1976	240	230	32	4	16	154	MOS	32 to 512	Direct replacement for IBM 3704/3705 Block-level synchronous scanners and block-level channel adaptors are standard
Modular Computer Systems, Inc IV/CP	1975	256	250	128	1	16	29 5	-	512	Accommodates any type of peripheral
Paradyne Corporation PIX II	1976	N/A	56	32	N/A	16	15 8	MOS	32	Features include voice adaptor and line switch

9 2.2.2 Trends and Projected Developments in Front-End Processors - As with other areas of data handling equipment, the dividing line between front-end processors and other communications network hardware is not rigidly defined. The processors, then, will take on the functions required for the particular host computer and data network. They may take on functions usually assigned to modems, concentrators, and switches. Flexibility will be the key word for future units. This flexibility will be achieved through greater utilization of LSI, microprocessor control, and improved software.

In general, the trends and developments in front-end processor technology will follow the trends and developments for processors and memory presented in Section 7.

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10. INFORMATION PRESENTATION ELEMENTS

Information presentation elements are discussed in this section in terms of the dynamic or real-time presentation elements and the hard-copy presentation elements that are depicted in Figure 10-1 Dynamic presentation elements are those that are capable of being driven and/or changed in real time, in contrast to the hardcopy elements, which are permanent in nature once they are produced. For purposes of classification, dynamic presentation elements include certain classes of projection systems that use hardcopy media (e.g., film) as the image source. Thus, for this example, the systems that generate the hardcopy image source are classified as hardcopy presentation elements, and systems that project the image are classified as dynamic presentation elements.

For more than a decade, the information presentation/display market has been projected as ready to explode Indeed, the market has "exploded" in the area of alphanumeric terminal devices, but has been less successful in the area of graphics than forecasted To a certain extent, advancements in technology have been reflected by this market. Many of the most significant advances that have occurred in displays recently have been the result of advances in supporting technologies, primarily integrated circuit technology. Among the significant advances that have occurred as a result of IC technology are the intelligent terminals, graphic displays that are refreshed from solid-state memories, and digital control of graphic functions

Display devices still employ the CRT as the dominant display medium, and indications are that this will not change significantly during the next several years; however, other technologies are beginning to emerge as technically feasible approaches. The application of these technologies will probably be limited for the foreseeable future to special requirements that can justify the additional cost over that for a CRT-based system. At present, no technology is cost-competitive with the CRT, although certain classes of plasma panels are showing progress in that direction.

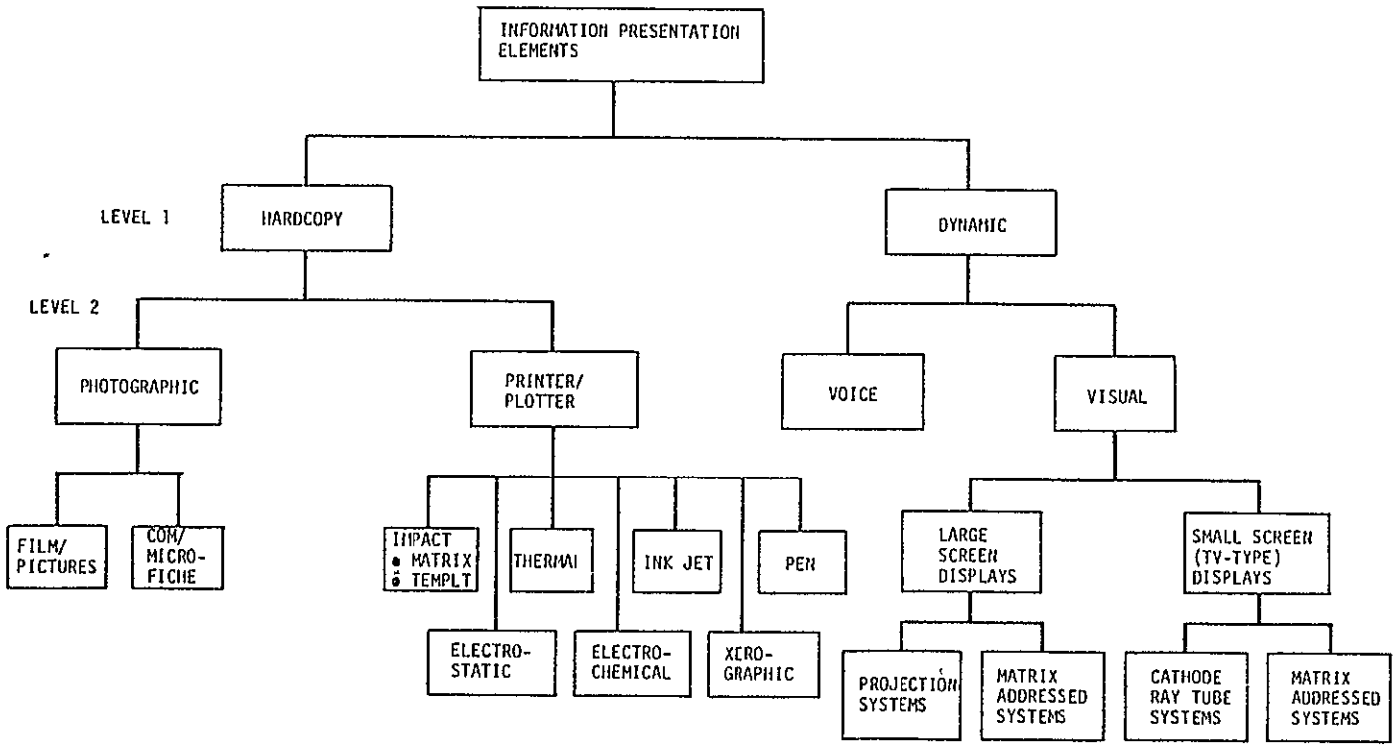

FIGURE 10-1. INFORMATION PRESENTATION ELEMENTS

Research is going on in many areas of display technology at the present time. In fact, so many areas are being investigated that the efforts appear to be fragmented. This fragmentation clearly disperses the available funding to the point that it probably restricts technology development. The one factor that places the most pressure on manufacturers to improve display media technology is the search for higher-performance home television/home entertainment displays to replace the current CRT systems. A breakthrough in one or more areas may result in more funding being diverted to that area, which could conceivably produce a system that is cost- and performance-competitive with the CRT However, most authorities are not presently willing to commit themselves as to which display technology will experience this first breakthrough, or indeed if such a breakthrough occurs, whether that technology will win the final competition as the predominant display medium for computer-generated data, home television, and other information presentation functions.

10.1 DYNAMIC INFORMATION PRESENTATION ELEMENTS

Dynamic information presentation elements include both visual and voice presentation systems. Visual systems only are covered in this Phase I report because these represent the most important method for presenting data; however, voice systems will take on added significance as both an input and an output method for data in the near future. Visual systems are classified as either small-screen (TV-type) or large-screen systems. Small-screen systems have typically been 25 in. or less in diagonal measurement. This limitation has been primarily the result of practical limitations on the size of cathode ray tubes, which is the principal dynamic display medium. This distinction between large- and small-screen displays may change as technology advances.

Technology is discussed in the following sections in terms of two specific aspects of display technology: (1) features that are provided independent of the display medium (e.g., intelligent terminal features) and (2) the display medium. Many of the features available on terminal devices are not limited by technology but are functions of human factors and cost.

10.1.1 State of the Art in Small-Screen Displays

The state of the art in small-screen (TV-type) dynamic information presentation elements is discussed first in terms of features available on alphanumeric terminals, graphic display terminals, and image presentation devices The specific display device technologies (CRTs, Plasma Panels, etc.) are discussed and compared in subsequent paragraphs

Alphanumeric display terminals perform in the capacity of remote communication terminals (similar to the hardcopy teletype devices) and as local terminals for interactive operations (editing, data base access, etc.) with computers As such, these devices are available as intelligent terminals (possess memory and limited processing capability) and as dumb terminals (strictly dependent on the host processor for all intelligence). The dumb terminal has been in use since the mid-sixties, and although it still serves the needs of numerous users, many of the newer terminals are incorporating microprocessor-based intelligence. Datapro Research Corporation (Ref. 10-1) reported that microprocessor-based terminals accounted for only 10% of the installed display terminal base at the beginning of 1975, but that 25% of the display terminals shipped in 1975 contained microprocessors. Similar statistics for 1976 and 1977 to date are not available, but the trend has not slowed

A characterization of the state of the art for alphanumeric displays, excluding the display medium itself, is difficult to accomplish because certain characteristics are more a function of human factors and cost than of technology. The primary technology items are features of intelligent terminals such as edit capabilities, memory size, stand-alone processing capabilities, etc. Tables 10.1.1-1 and 10.1.1-2 present the characteristics and features, respectively, for typical alphanumeric terminals available on today's market. These capabilities and features are not considered to be the limit of technology, but are representative of the features and capabilities that are available at a cost that the market will bear.

TABLE 10 1.1-1 CHARACTERISTICS OF TYPICAL ALPHANUMERIC DISPLAY TERMINALS

CHARACTERISTIC	RANGE
Display Screen Viewing Area	50 to 80 in^2
Number of Display lines	24 typical, up to 40
Number of Characters/Line	80
Maximum Viewable Characters	1,920 typical; up to 3,200
Character Set	64, 96, 128
Character Code	ASCII
Symbol Formation	5 × 7 dot matrix
Keyboard	Typewriter
Transmission Mode	Half/full duplex
Transmission Rate	2,400 to 9,600 bps
Transmission Technique	Synchronous or Asynchronous
Communication Protocol	ASCII/BSC/SDLC
Message Format	Character or Block
Interface	EIA RS-232C
Display Monitor	CRT

TABLE 10.1.1-2. TYPICAL ALPHANUMERIC DISPLAY TERMINAL FEATURES

FEATURE	COMMENT
Memory	Available to 64K words
Microprocessor Control	Widely available
Edit Features	
Cursor Positioning	U, D, L, R, H on most
Cursor Blinking	Available on most
Character insert/delete	Available on most
Line insert/delete	Widely available
Erase	Character, line, screen common
Roll	Limited availability
Paging	Limited availability
Color	Limited availability
Auxiliary Storage	Limited availability
Light Pen/Other Select Modes	Limited availability
Selectable Brightness	Up to 2 levels fairly common
Compatible With One or More Standard Devices	Generally available
Internal Refresh	Trends in direction of Internal Refresh

The CRT is the principal display medium for alphanumeric display terminals. Plasma panels are beginning to see limited use for special applications, but they are not cost-competitive with the CRT Other technologies (LEDs, liquid crystals, etc.) are seeing limited use in applications that are generally for a limited number of characters (e.g , time displays) that are no more than one line One company has announced a 6- by 6-in. TV-type display using liquid crystals, but the system has limited application as it presently exists.

The cathode ray tube is also the primary medium for graphic displays Display size is a more important factor in graphic displays than for alphanumeric displays, and systems to 25 in. diagonal measurement are available. Displays are available in black and white, shades of gray (up to 64 levels), and color, with resolution typically to 1,024 lines. At least three companies (Adage, Vector General, and Evans and Sutherland) build graphic display systems that produce dynamic perspective drawings of complete three-dimensional objects. These systems are capable of maneuvering and/or manipulating the displayed picture through offsets, rotation, translation, scaling up, scaling down, windowing, clipping, and zooming. Most of the newer systems perform these functions digitally, using integrated circuits. Prior to the past two or three years, these functions were performed using analog circuits.

As pointed out above, display monitors in use today are primarily CRT devices. CRTs typically have to be refreshed about 30 times per second; otherwise the image will fade or perhaps flicker, depending on the refresh rate. The need to provide the refresh function has in the past placed a relatively heavy processing load on the host computer. Two technological developments have enabled a significant reduction in refresh requirements. The first such development was the direct view storage tube (DVST) which does not have to be refreshed regularly (a DVST will store an image for minutes or hours without being refreshed), but which is limited in its dynamic capability (i.e., its ability to incorporate changes without erasing the entire picture and rewriting it). Some commercially available systems have combined the advantages of the storage tube with the advantages of a refresh system so as to

permit change and/or apparent motion The most innovative approach for achieving the desired result is accomplished through beam intensity control techniques. Another approach that permits changes but lacks the flexibility of the beam intensity control technique is to use the DVST as an image source for a raster scan converter, which presents the output to a standard raster TV monitor Some of the systems that use this latter approach experience degradation in resolution in order to achieve the desired flexibility. The storage tube and the scan converter combination produces an output resolution that is far below the quoted resolution for the system, which in some cases is quoted as high as 1,024 TV lines.

A second technological development that is gaining widespread acceptance in graphic display devices and which offers even greater potential for the future is the use of internal solid-state memory (mostly MOS) refresh systems. Systems in existence at present offer up to 480 × 640 addressable points for color displays. Each addressable point can be encoded as one of seven colors.

Table 10.1.1-3 presents state-of-the-art capabilities for graphic display systems. No one system provides all of these features and capabilities, but they are available in various combinations.

Information presentation devices that display images in lieu of alphanumerics or graphics play at least two roles for presenting high resolution images. The traditional role is that of the direct-view monitor, similar to the home television set. This type of monitor is available commercially in either color or shades of gray with display screen sizes to 25 in. diagonally and 1,024 TV lines resolution. The limitation on this type system is one of bandwidth, which is a function of the scan and refresh rates. Increasing the resolution by a factor of two increases the bandwidth by a factor of four, which soon becomes prohibitive unless the refresh rate can be reduced, which causes flicker. Thus, to take full advantage of the potential resolution capabilities of the CRTs that are presently available, the CRT should be used in a manner that eliminates the need for refreshing, and thus direct viewing The

TABLE 10.1 1-3 STATE-OF-THE-ART GRAPHIC DISPLAY SYSTEM CHARACTERISTICS/FEATURES

CHARACTERISTICS	COMMENTS
Display Media	CRT
Maximum Viewable Area	208 in^2
Addressable Matrix	4,096 × 4,096 typical, 8,192 × 8,192 maximum
Viewable Matrix	1,024 × 1,024 typical, 4,096 × 4,096 maximum
Word Length	16 bits
Points/sec	10^6
Vectors/sec	10^6 in/sec
Characters/sec	330,000
Character set	127 character ASCII set typical
FEATURES	**COMMENTS**
Color	Available on some units
Intensity/Shades of Grey	Available on some units
Perspective (3-D) Views	Available from 3 vendors
Translation/Rotation/Offset	Widely available
Line Texturing	Generally available
Windowing/Zoom	Generally available
Conics	Available on some units
Refresh Mode	Trend to internal refresh
Internal Processor	Trend to internal processor
Source Language	Wide use of FORTRAN

approach is to scan the CRT in a slow mode and let the light created by each scan line expose a film where the image is recorded. One commercially available system produces a 70-mm film from a 4,600-line CRT with a 3- by 3-in. raster. The CRT uses a 0.0006-in. CRT light source. Linearity of the system is 0.05%, short-term stability is 0 001%, and long-term stability is 0.0005%

10.1.1.1 Cathode Ray Tubes (CRTs) - Since the development of the CRT in the early 1930's, it has been the dominant (and until recently, the only) medium for display applications requiring a large number of picture elements. In the approximately 45 years of its existence, the CRT has advanced from its original application as an oscilloscope display to the capability for high-resolution color TV systems, and is used extensively for displaying computer-generated images, graphics, and alphanumerics.

CRTs are widely available in color, black and white, and shades of gray. The largest color CRTs produced commercially have a display screen that measures approximately 25 in. diagonally with a viewing area of approximately 315 in^2. J. W. Schwartz (Ref. 10-2) points out that although this is not the limit achievable in size, it is a practical limit because of rapid increases in volume, weight, and cost for even modest increases in size beyond 25 in. Beyond this, equivalent brightness and resolution are extremely difficult, if not impossible, to achieve. Table 10.1.1.1-1 presents representative characteristics of state-of-the-art color picture tubes, using 25-in. diagonal tubes as the basis for size-dependent characteristics.

CRT development is advanced to the point that most viewers cannot discern improvements in performance other than size. The one characteristic (Ref. 10-2) other than size which is discernible is resolution, particularly in picture highlight areas. The highest resolution systems that are commercially available are 1,024 lines (at 30 frames/sec refresh), and many of these systems fail to meet this specification on the fringes and in the picture corners. The area is receiving considerable attention by a number of vendors, and improvements

TABLE 10.1 1.1-1 TYPICAL SHADOW MASK COLOR TUBE CHARACTERISTICS (REF. 10-2)

Maximum Picture Area	315 in^2 (2,032 cm^2)
Peak Brightness	1,000 ft-L
Average Brightness (1.5 mA)	150 ft-L
Luminous Efficiency (Tri-Color White)	
Light Out/High Voltage Power	8 lm/W
Light Out/Total Display Power	3 lm/W
Contrast	50 1
Resolution	
Low Current	400 to 500 TV lines
High Current	100 to 200 TV lines
Minimum Number of Electrical Inputs	8
Total Power Input	100 W
Display Volume (Tube, Yoke, etc.)	0 8 ft^3 (23 liters)
Display Weight	50 lb (23 kg)
Display Cost (OEM)	$90

can be expected in the near future The preceding paragraph pointed out one system that is capable of much higher resolution for the special purpose of exposing high-resolution film images. Systems with 5,000 lines resolution are available for applications of this type.

10.1.1.2 Matrix-Addressed Pannels - Almost all flat-panel displays, excluding projection sytems which are classified as large-screen displays herein, use a matrix of display elements (Ref 10-3). The matrix-addressed devices discussed in this section are classified as small-screen displays since all such systems are currently in the size range of the CRT. However, some of the technologies discussed may achieve the size of large-screen displays in the future Also, some existing large-screen displays are matrix-addressed panels.

Three of the matrix-addressed techniques that appear to offer high potential for use as TV-type displays are plasma panels, electroluminescent panels, and thin-film transistor panels Many other technologies are being investigated and cannot be ruled out. Future reports will address these other technologies.

10.1.1.2.1 Plasma Panels - Plasma panels (sometimes referred to as gas discharge panels) are the most advanced display devices at present for competing with the CRT for computer-driven displays Plasma displays are classified as either dc gas discharge devices or ac gas discharge devices. Flat panels that employ both these techniques are commercially available and are receiving attention from a number of companies.

The dc plasma panels are driven by unidirectional pulses between two electrodes. The pulses may be modulated in intensity and pulse width to control glow intensity and pulse duration. When the electrodes are energized, light can be extracted from either the glow that is created near the cathode or the positive column of light that extends between the cathode glow and the anode. The positive column is more efficient (efficiencies of 3.4 lm/W have been achieved), but the cathode-glow system is more advanced. The dc plasma panels are capable of generating color displays by using the ultraviolet component of light generated by the glow to excite phosphors that give a choice of colors.

The ac plasma panels are energized with bidirectional pulses. When an element is energized by a starting pulse, it will emit light until the glow is quenched by an erase pulse. Thus, these panels have an inherent memory and do not impose a refresh requirement on the host computer. The ac plasma panel is basically a two-level device with a high contrast ratio, but progress is being made toward modulating the outputs for gray-scale applications. Owens-Illinois has developed a self-scanning technique, designated the "Digivue", that is capable of moving light spots around on the panel. This system is capable of displaying 512 × 512 addressable points and is commercially available. Larger systems have been built, but none are commercially available at this time.

10.1.1.2.2 Electroluminescent Display Panels - Electroluminescent panels produce light by exciting an electroluminescent phosphor with an electric field. These panels offer an excellent chance for building thin-film panels Some thin-film, ac-driven electroluminescent panels have full frame storage and can combine this with stored gray scale. The current limitations on this approach are relatively low luminescence and efficiency and high voltage requirements that are difficult to achieve with integrated circuits.

Both ac and dc excited panels exist, and both types can be matrixed in arrays with as many as 50,000 elements, but neither the non-linearity nor the color gamut is good enough for TV applications.

Westinghouse Research Laboratories (Ref. 10-4) has reported the development of a 12,000-element (6 × 6 in.) electroluminescent panel that consists of a 6 × 6-in. thin-film integrated circuit containing 24,000 transistors (two for each element) overlayed by a sprayed electroluminescent phosphor layer. This technique offers promise for achieving the desired nonlinearity, however, the luminescence is quite low (30 ft-L) The required voltage levels were lower than normally required for electro-luminescent panels, and several gray-scale levels were achieved.

10 1 1.2.3 Thın-Fılm Transıstor Panels - Thın-fılm transıstors (TFTs) were mentıoned ın conjunctıon wıth powder electrolumınescent panels ın the precedıng paragraph. Actually, thın-fılm transıstors offer potentıal for use in a number of areas, ıncludıng deposıts of TFTs on glass. TFTs have been used ın conjunctıon wıth a number of other technologıes ıncludıng electrolumınescent phosphors, lıquıd crystals, and gas dıscharge or plasma devıces. TFTs can be used to enhance the capabılıtıes of these other technologıes by provıdıng storage capabılity for technologıes that do not have storage and by provıdıng the nonlınearıty that ıs not achıevable ın electrolumınescent arrays or lıquıd crystals.

In addıtıon to the above advantages, TFT arrays offer the potentıal for physıcally large dısplays, up to a few feet across, and the TFTs can handle the hıgher voltages that lımıt the use of gas dıscharge and electrolumınescent panels. In vıew of the potentıal number of applıcatıons for TFTs and the flexıbılıtıes provıded, ıt appears almost certaın that they wıll be used extensıvely ın dısplay systems of the future.

10.1.2 Trends and Projected Developments in Small-Screen Displays

Small-screen displays discussed herein include alphanumeric displays, graphic displays, and imaging systems. Trends and projected developments are presented first in terms of available features and second in terms of the display medium As with other areas of data systems, the technology will be reflected largely by market demand, and feasibility does not necessarily imply availability.

Advances in the capabilities of available features in display devices can be expected to continue at an accelerated pace as a result of advances in the state of the art in integrated circuit technology, processing, communications, and different types of memories, including both semiconductor memories and magnetic bubbles For more details on these related technologies, refer to Sections 3, 4, 7, and 9

Recent advances that have resulted from the supporting technologies mentioned above include the introduction and growth of the intelligent terminal, the replacement of analog circuits with digital circuitry for graphics manipulation, and the increased use of MOS memories for storing and refreshing relatively high-resolution color graphic displays, such as the RAMTEC display system. The improvements in IC technology speed, packing density, power dissipation characteristics, and packaging that is forecast in previous sections (primarily Section 7) will be reflected on almost a one-for-one basis in future terminals. Alphanumeric terminals will be capable of incorporating increased processing capabilities and will have both random-access and high-speed auxiliary storage, probably in the form of magnetic bubbles. In the 1980 to 1985 timeframe, terminals with the processing capabilities of today's small minicomputer will be available at costs that rival a medium-capability intelligent terminal today. Random access storage of 64 kbits should be standard, with capabilities to 64 kbytes being common (Technology will support higher capacities, but the availability will be a function of market demand.) Bubble memory systems of about 4 to 16 Mbits can be expected. Internal refresh (via high-speed semiconductor memory) of high-resolution (1,576 × 2,048 pixels) color graphic displays and/or images will be feasible

from both a cost and a performance viewpoint. The added processing and/or storage capacity in display devices will provide almost all required processing capabilities within the graphics or image processing terminal, thus leaving the host processor free to perform more important functions.

As the display medium, the CRT will continue to be dominant for the foreseeable future Plasma devices will become more economical and will be used for specific applications. Also, other technologies, such as electroluminescent displays, will see limited use in the early 1980's. Thin-film transistor arrays will be used in conjunction with other technologies to produce larger displays than are currently available with CRTs; however, the cost of all new technologies will be higher than for CRT displays for the foreseeable future.

10.2 HARDCOPY INFORMATION PRESENTATION ELEMENTS

Hardcopy information presentation elements include the photographic and the printer/plotter elements depicted in Figure 10-1. This report presents information on the state of the art for computer output microfilm devices.

10.2.1 State of the Art in Computer Output Microfilm

Computer output microfilm (COM) systems are available as both on-line and off-line equipment, with the off-line systems normally using magnetic tape recorders for input. These systems are capable of producing alphanumeric and graphic data at rates to 30,000 lines/min for alphanumerics and 400,000 points/sec for graphics.

Available COM devices may be configured in many different ways Some manufacturers provide interfaces to only the IBM 360/370 series; others provide interfaces to any third-generation computer, and still others claim compatibility with any computer. Many of the newer systems are interfaced via front-end processors that increase the flexibility but may require user-provided software. Available features on COM equipment vary widely, ranging from multiple fonts, the presence or absence of graphic capability, different reduction ratios, etc. The details and implications of some of these features are discussed in subsequent paragraphs.

The majority of the COM equipment on the market today uses a CRT to expose the film. As the technology improves in dynamic displays, different types of image generation systems are being employed. Two of the more innovative systems use lasers and light-emitting diodes The 3M Company uses both an Electron Beam Recorder and a Laser Beam Recorder to write data directly onto the film. Memorex composes the output onto a bank of light-emitting diodes (LEDs) through a character-translation matrix. The light from these diodes is transmitted to the film through fiber optic strands to form a character image. One difficulty in this latter approach is that the image is generated a line at a time (CRT imaging systems generate a frame before the film is advanced, although the film may be exposed character-by-character). This imaging method has limited capabilities for producing graphics because of the difficulties in controlling movement of the film. Use of the LED approach also restricts the generation of microfiche because of inability to control the film. This latter difficulty may be a greater limitation on the use of this technique than the limited graphics capability because more

users appear to be using microfiche than microfilm in today's market. One major advantage of LEDs is that they produce up to a thousand times more light energy than a CRT and thereby lessen the effects of film sensitivity Thus, it appears likely that attempts will be made to overcome the problems identified above to enable the use of this technique on future COM devices.

Reductions in size of 42X to 48X appear to represent the state of the art. Some vendors are unable to overcome the resolution problem in going to 48X reductions. Silver halide films typically have resolutions that range from 100 to 190 lines per millimeter, and films with resolutions of 190 lines per millimeter or higher are required to accomplish reductions of 48.1. Silver halide film is considered the industry standard for the recorder master copy. One of the highest grade films available for COM applications is Kodak AHU, and the price is reflected accordingly. The most widely used film for duplicating is designated diazo. It is less expensive to purchase and to process. A relatively recent introduction is vesicular film, which is replacing diazo in many installations because of the simpler processing chemistry that eliminates the need for ammonia.

As mentioned above, the introduction of front-end processors on many COM systems has increased the flexibility of these systems. These processors not only relieve the host processor of its processing load and provide DMA-to-DMA interfaces to speed up the data throughput, but they also provide capabilities for handling standard print tapes that reduce the operator burden and/or the need for operating system modifications within the host processor. These front-end processors perform a number of functions that otherwise have to be performed by the host processor or deleted. Among current functions being performed are formatting, graphics generation, control functions, character selection, software translation, and film indexing. These functions can be expected to increase as the costs and capabilities of such processors continue to decline

10.2.2 Trends and Projected Developments in Computer Output Microfilm

Computer output microfilm is another area of technology that has failed to grow as rapidly as many experts projected in the 1960's In spite of this lack of rapid growth, the technology has followed a relatively steady increase in capabilities. The most important recent improvements in COM systems is the introduction of the front-end processor to increase system flexibility. Front-end processors will be used more and more to enhance the capability and flexibility of COM equipment. Also, advances in the area of image-generation devices will continue to be reflected in the COM systems of the future.

Datapro Research Corporation (Ref. 10-5) feels that COM prices will not decline in the foreseeable future. Instead, any reduction in component prices will be reflected in greater sophistication and flexibility.

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