EXTENDED PERFORMANCE SOLAR ELECTRIC PROPULSION THRUST SYSTEM STUDY

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16 Abstract

Ion-thruster technology has progressed during the past decade to the point that it is considered ready for application. During this study, several thrust system design concepts were evaluated and compared using the specifications of the most advanced 30-cm engineering model thruster as the technology base. Emphasis was placed on relatively high-power missions (60 to 100 kW) such as a Halley's comet rendezvous. The extensions in thruster performance required for the Halley's comet mission were defined and alternative thrust system concepts were designed in sufficient detail for comparing mass, efficiency, reliability, structure, and thermal characteristics. Confirmation testing and analysis of thruster and power-processing components were performed, and the feasibility of satisfying extended performance requirements was verified. A baseline design was selected from the alternatives considered, and the design analysis and documentation were refined. The baseline thrust system design features modular construction, "conventional" power processing, and a "concentrator" solar array concept and is designed to interface with the Space Shuttle. A program development plan was formulated that outlines the work structure considered necessary for developing, qualifying, and fabricating the flight hardware for the baseline thrust system within the time frame of a project to rendezvous with Halley's comet during December 1985. An assessment was made of the costs and risks associated with a baseline thrust system as provided to the mission project under this plan. Critical procurements and interfaces were identified and defined. The results of this study are presented in the five volumes of this report.

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FOREWORD

The work described herein was performed by the coordinated efforts of personnel within two divisions of the Hughes Aircraft Company. Responsibility for the study resided in the Ion Physics Department of the Research Laboratories Division. This department is managed by Mr. J.H. Molitor. A major portion of the thrust system design activity was performed by a team of individuals assembled from the Technology Division of the Space and Communications Group and coordinated and directed by Dr. E.I. Hawthorne. The work was funded under contract NAS3-20395 and monitored by Mr. James E. Cake of the NASA Lewis Research Center. The key technical contributors were

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SUMMARY

The primary objective of this study was to provide a data base for a program plan for the development of the ion-propulsion thrust system for the Halley's comet mission spacecraft. This data base was to include: the definition of a design concept, selected from among alternate candidate configurations; the identification of required supporting technology, including the definition of critical areas and potential technical risks; the definition of a program development plan, including a development schedule and an assessment of potential schedule risks; and a preliminary estimate of yearly and total program costs.

A concurrent objective of the study was to conduct a hardware "approach confirmation" technology effort to evaluate the ion thruster's performance and lifetime at the power level required for the Halley's comet mission, to design and evaluate the thruster isolator required for operation at the higher power level, and to evaluate the design of a capacitor-diode voltage multiplier.

A thrust system baseline configuration was identified for the 30-cm extended-performance mercury ion thruster that can perform the Halley's comet rendezvous mission. The configuration is comprised of 10 thrusters configured with a power management and control system and a structure and thermal control system in a modular thrust system design. The power management and control system uses conventional power processing. Power is provided to the thrust system with an 85 kW concentrating solar array. The thrust system mass is 1010 kg (including 15% contingency), the average system efficiency is 70%, and the estimated reliability upper bound is 72%.

Adaptability of the 900-series 30-cm thruster design to the 6 to 7 kW range required for the Halley's comet mission was demonstrated with only minor design modification required, and an acceptable high-voltage isolator design was validated by laboratory tests. The design and performance of an alternate power management and control system design approach utilizing the capacitor-diode voltage multiplier was successfully demonstrated by laboratory model tests in excess of 1 kW.

The technology efforts mentioned above assisted in the identification of the level of technical risks associated with the thrust system design. These risks have been found amenable to resolution through normal engineering development and, therefore, judged to be acceptable for mission application.

The program plan, which includes the procurement plan generated for the baseline configuration is a viable plan that provides for delivery in May 1981 of the flight thrust system to be integrated with the mission module and solar array. The cost of the thrust system development program is projected to be 54 million dollars (in fiscal year 1977 dollars) excluding contractor fee, of which approximately 13.5 million dollars will be required in fiscal year 1978.

In contrast to the low technical risk, the schedule risk for initiating this program development is of particular concern. Timely approval of the authorization of 13.5 million dollars for fiscal year 1978 must be granted so that the pre-project, or advanced development, activities can be initiated.

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SECTION 1

INTRODUCTION

This report summarizes the results of a six-month study to define the design, program plan, and costs of the ion-propulsion thrust system for the Halley's comet mission spacecraft. The modular characteristics of the design developed during this study also make it applicable as the prime space propulsion system for other potential missions.

This study, which is based on an initial system characterization (completed 7 February 1977) performed by the National Aeronautics and Space Administration's Lewis Research Center (NASA LeRC),was performed in three parts:

- Design tradeoff studies (14 February to 15 April 1977) to define and compare alternate design approaches.
- Conceptual design definition, program plan, and costs of a selected design approach (15 April to 15 June 1977).
- Approach confirmation of supporting technology in selected areas.

The results of this study are presented in five volumes. Volume I summarizes the results of the entire program. Volume II discusses the conceptual design, program development plan, and cost estimates for the selected baseline thrust system design. Volume III describes the design tradeoff studies performed to compare alternate design approaches. Volume IV describes the evaluation of thruster technology for extended performance applications. This volume, Volume V, presents the details of the capacitor-diode voltage multiplier (CDVM) circuit analysis and experimental evaluation. The results reported in these volumes have also been presented in briefings at NASA LeRC.

A. BACKGROUND

In the fall of 1976, the Office of Aeronautics and Space Technology (OAST) was given the responsibility of assessing the capability of the electric propulsion technology under development at NASA LeRC and of the

solar array technology under development at Marshall Space Flight Center (MSFC) and the Jet Propulsion Laboratory (JPL) to perform the Halley's comet rendezvous mission proposed by JPL. OAST established an "August Project" team from members of the three organizations to develop a preliminary program plan to support a fiscal year (FY) 1979 new start.

The August Project consisted of parallel efforts by JPL, NASA LeRC, and MSFC to define the design approach, program plan, costs, and risks of the Halley's comet mission. Three areas were considered: the spacecraft (including the science payload), the ion propulsion subsystem (referred to as the thrust system in this report), and the solar array. The NASA LeRC program was conducted in two phases. First, initialization studies (completed 15 February 1977) were conducted to define requirements and to identify preliminary design characteristics. Second, during the 15 February to 15 July period, the design of the thrust system was defined, the program plan and projected costs were generated, and a risk assessment was made. The results of the second phase of the program are reported in this volume. The design selection process included tradeoff studies among alternate design approaches, followed by a refinement of the conceptual design that had been selected. Iteration with design data available from the parallel activities at JPL and MSFC, and concurrent approach confirmation tests and analyses included in this study, serve to strengthen the conclusions of the thrust system study.

NASA directed us to begin the study by identifying two candidate solar array configurations (flat or concentrator), three candidate power management and control (PMaC) approaches (conventional, direct drive, or voltage multiplier), and two structural design approaches (modular or integrated). A comparative assessment of the various configurations possible from combinations of these design choices was desired in terms of performance, mass, efficiency, reliability, and technical and schedule risks.

The thrust systems being considered are based on the electric propulsion technology that NASA LeRC has been developing for over a decade. The technical baseline for this application is the most recent operational engineering model thruster (EMT), the 900-series 30-cm

mercury ion EMT. This thruster is a scaled-up version of the 15-cm thruster developed and flight tested during the 1960-1969 period for the SERT II program. The EMT operates at a 3 kW power level with a specific impulse of 3,000 sec. By making minor modifications in the existing thruster design, extended performance at approximately 6 kW power level, 4,800 sec specific impulse, and 15,000 hr pre-wearout life (as required for a Halley's comet mission) was believed to be achievable at a low technical risk. This supposition was evaluated as part of this study.

In addition to the extended-performance thruster, the key elements of the thrust system for this extended-performance application are the PMaC subsystem, gimbal system, propellant storage and distribution system, thermal control system, and supporting structure. The background of extensive development in power-processing technology for mercury ion thrusters and technology developments in the other areas were the basis for the high level of confidence that the required extended performance levels could be achieved.

B. SCOPE

The scope of this study included: the development of conceptual designs for various candidate systems; the selection, definition, and evaluation of a baseline design concept and its critical interfaces; an evaluation of the sensitivity of the baseline design to critical data base and design parameters; the generation of a development program plan for the baseline concept; estimation of costs and fiscal year funding requirements; fabrication of a demonstration scale model; and the conduct of supporting technology studies (including fabrication and testing of critical hardware components) to estimate the physical and electrical performance and to provide a baseline for subsequent work.

The design characteristics, program plan, and costs of the baseline system were defined in parallel with the supporting technology effort. Design definition was carried out in two consecutive phases:

- Phase 1: Definition and comparison of alternate configurations, leading to baseline selection.

- Phase 2: Design definition and evaluation of the baseline configuration, culminating in the generation of a program plan and cost estimates.

The concurrent technology effort comprised thruster performance and lifetime evaluation, thruster isolator design and evaluation, and the design and evaluation of a CDVM breadboard that operates at 1 kW.

This volume describes our approach to designing the CDVM circuit, the details of the CDVM, the component selection process, and the test results. The design principles of a multiphase CDVM concept were applied to design, fabricate, and test a breadboard model circuit to operate at a 1-kW power level. Verifying the successful operation of a CDVM scaled to 1 kW confirms the projections for the 6-kW design that were made during the study of alternative thrust system configurations (described in Volume III).

SECTION 2

1-kW CAPACITOR-DIODE VOLTAGE MULTIPLIER

The goal of the work described in this volume was to design, fabricate, and test a 1-kW CDVM for the purpose of demonstrating the feasibility of high-power CDVMs and of verifying the analytical techniques that had been used to predict the performance characteristics of a 6-kW CDVM (discussed in Volume III). The result of this task was the successful operation of a 1-kW CDVM circuit over various input line, load current, and load fault conditions. High efficiency (96.2%), a low ratio of component weight to power (0.55 kg/kW), and low output ripple voltage (<1%, peak to peak) were obtained.

A. DESIGN APPROACH

The 1-kW CDVM was designed using a novel approach. This approach yields a device with fewer components than would be in a multiphase system composed of several single-phase systems run out of phase. (The basic operation of single-phase CDVMs has been covered in the recent literature.[1])

Figure 1 shows a conventional single-phase multiplier with output voltage V_{out} equal to $V_1 + 3\ (V_1 + V_2)$. The figure also shows the dc voltages on the capacitors. Figure 2 shows two of these multipliers operating 180 deg out of phase. Except for the ripple voltages (which are equal and out of phase), V_3 equals V'_3, V_4 equals V'_4, V_5 equals V'_5, and V_{out} equals V'_{out}. Tying the equipotential junctions together and replacing the parallel capacitors with single capacitors yields the circuit shown in Figure 3. This method of connecting single phases can be extended to N phases, each run 360 deg/N out of phase with respect to the next phase. This configuration does not result in the minimum

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[1] W.T. Harrigill, Jr., I.T. Meyers, "Efficiency and Weight of Voltage Multiplier Type Ultra Lightweight DC-DC Converters," NASA TMX-71735, W.T. Harrigill, Jr., I.T. Meyers, "High Performance DC-DC Conversion with Voltage Multipliers," NASA TMX-71566.

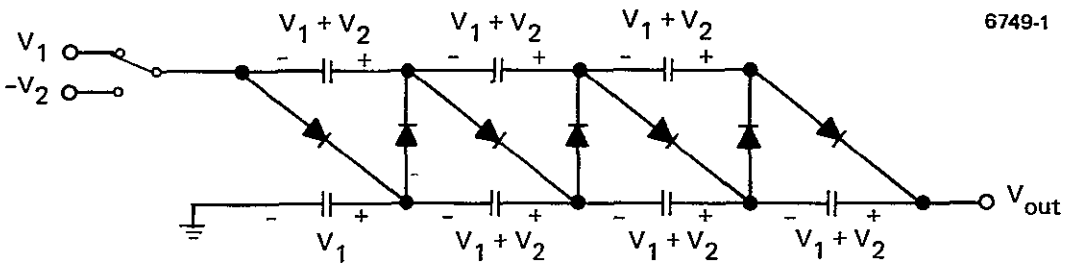


Figure 1. Conventional single-phase CDVM.

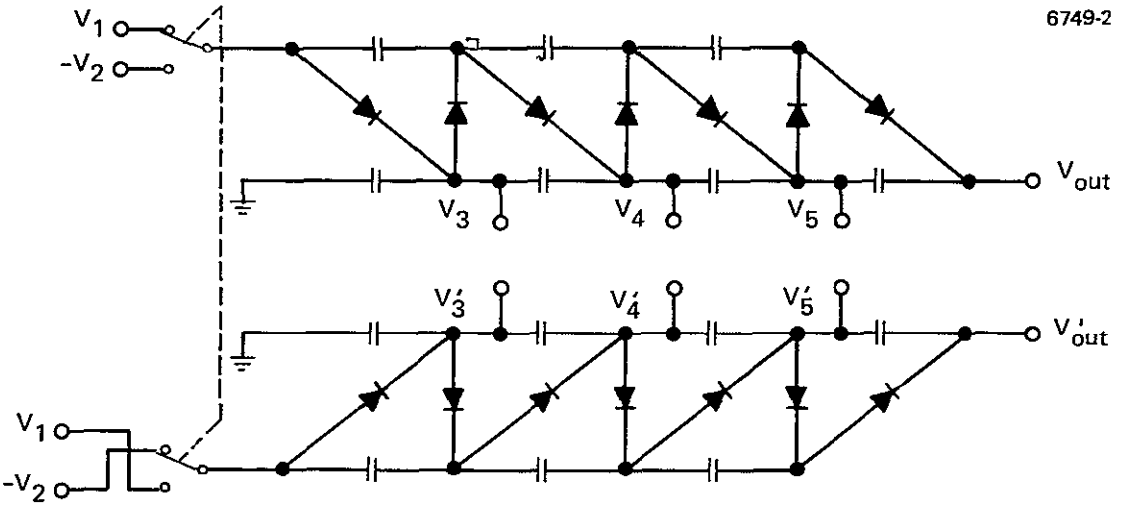


Figure 2. Two conventional single-phase CDVMs operated 180 deg out of phase.

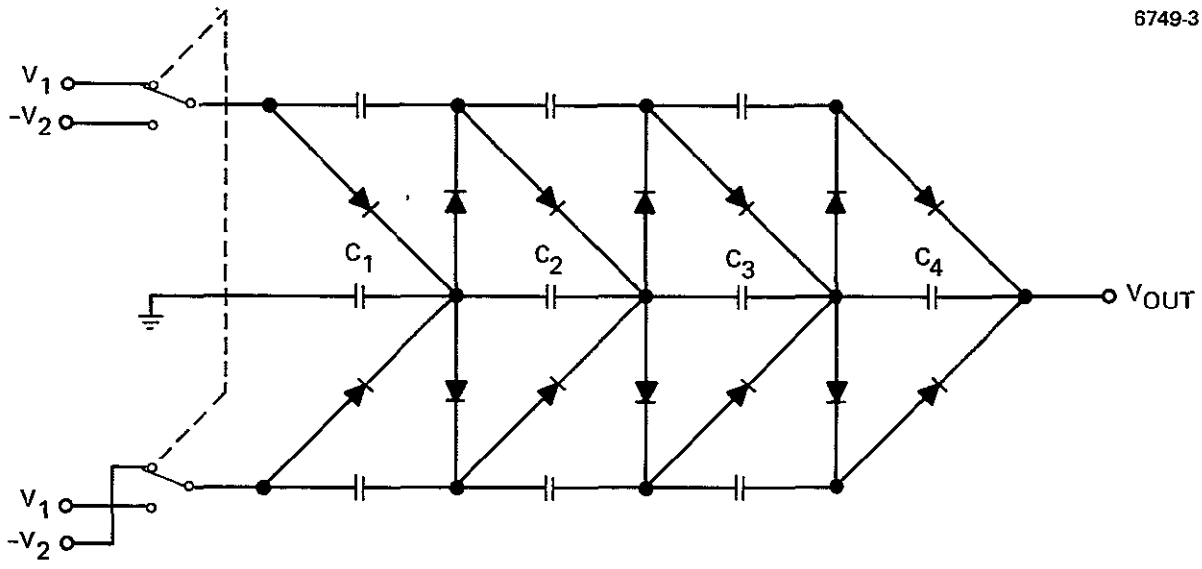


Figure 3. Circuit shown in Figure 2 after the equipotential points have been connected.

number of capacitors and diodes. Capacitors C_1, C_2, C_3, and C_4 in Figure 3 may be deleted, which results in the circuit shown in Figure 4. The diodes always conduct in series pairs; for instance, rectifiers CR1 and CR8 conduct, or CR7 and CR2 conduct. Also, series diodes across a capacitor never conduct simultaneously (except during the recovery time of the diode). The circuit in Figure 4 is shown reconfigured in Figure 5; this reconfiguration saves six diodes.

Figure 6 extends the two-phase system to a three-phase system. The input phases are run 120 deg out of phase. Extending this type CDVM to multiphase versions results in ring-shaped configurations (see Figure 7). The voltage multiplication (assuming positive input voltage, $V_{in} > 0$) is approximately equal to M + 1 times the input voltage, where M is the number of capacitor stages.

The phasing sequence of the CDVM is important. To operate efficiently, the capacitance charging period must be as long as possible to keep the peak currents in the transistor switch to a minimum. Figure 8 demonstrates the optimum phasing arrangement for a five-phase system. If the inductance values are properly selected, this configuration allows charging current to flow for nearly four-fifths of the half cycle.

Experience at Hughes has shown that efficiency is improved by connecting the input inductors in series with each phase. This improvement can be explained by considering a capacitor charged through a series resistor and diode or charged through a series-resistor, diode, and inductor combination.

In Figure 9(a), a capacitor is shown being charged through a resistor. The total energy dissipated in the resistor is found by integrating with respect to time the product of the resistance and the square of the current (assume an ideal diode: $V_f = 0$, $R_{Reverse} = \infty$). The current, i(t), through a resistor, R, is given by

$$i(t) = \frac{V_o}{R} e^{-t/\tau} \quad ,$$

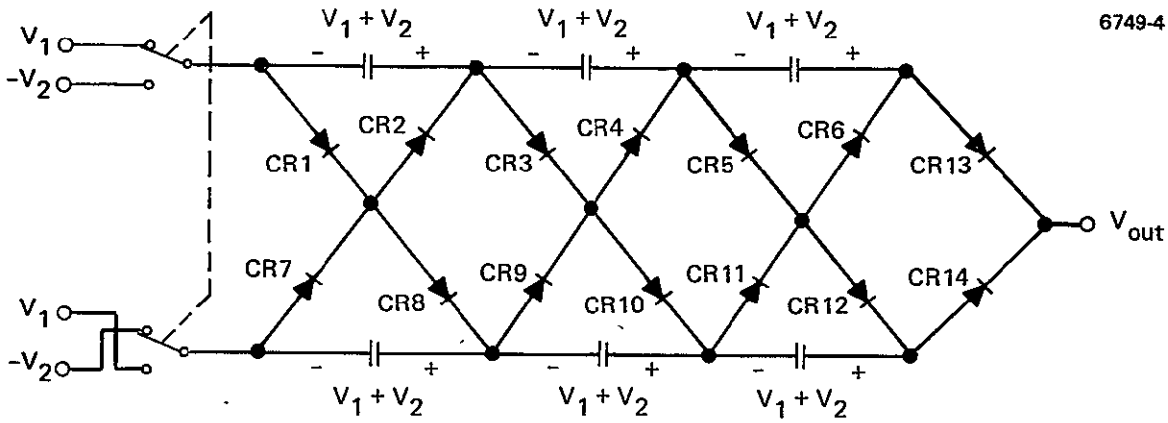


Figure 4. Circuit shown in Figure 3 after capacitors C_1, C_2, C_3, and C_4 have been eliminated.

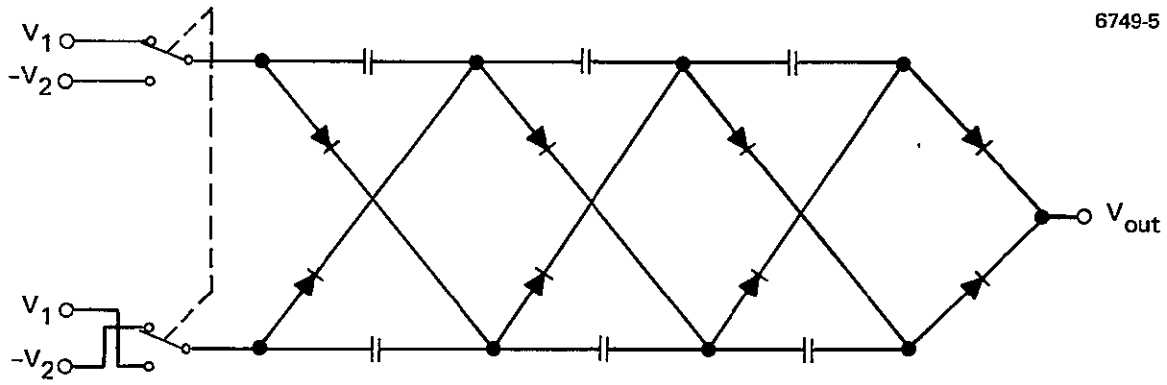


Figure 5. Circuit shown in Figure 4 reconfigured to eliminate six diodes.

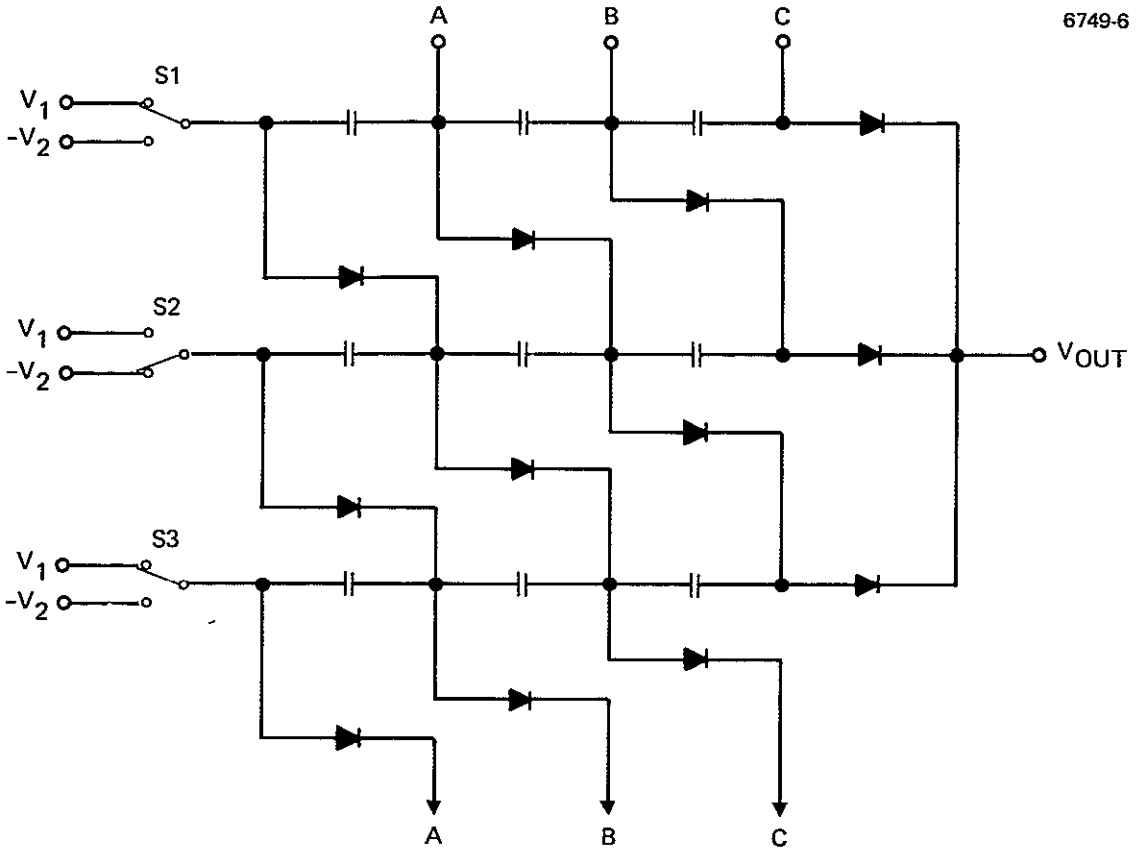


Figure 6. Circuit shown in Figure 5 extended to a three-phase system with input phases operated 120 deg out of phase.

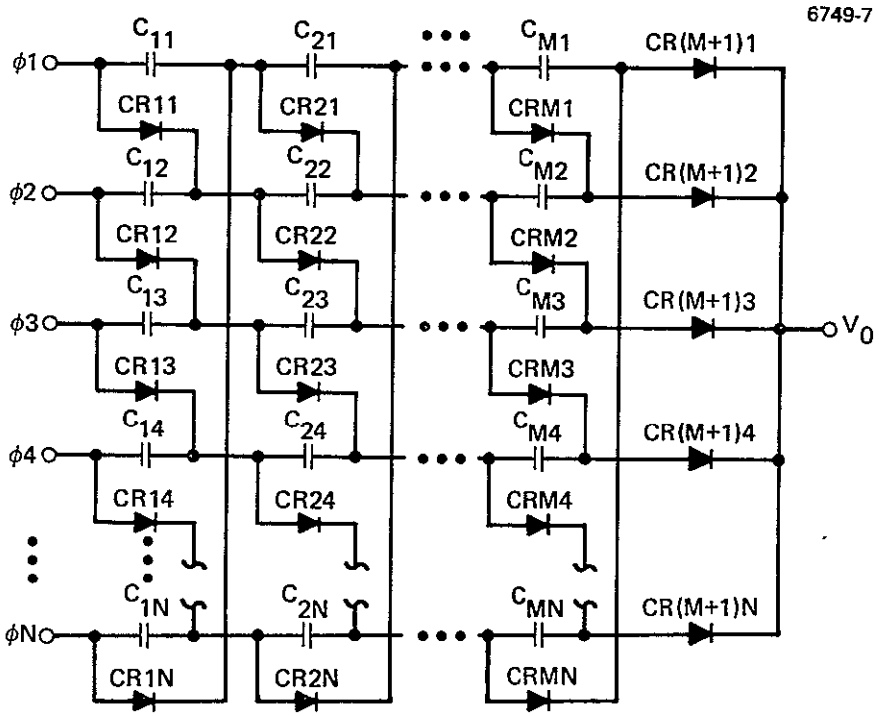


Figure 7. M-stage, N-phase ring (partial matrix) connection.

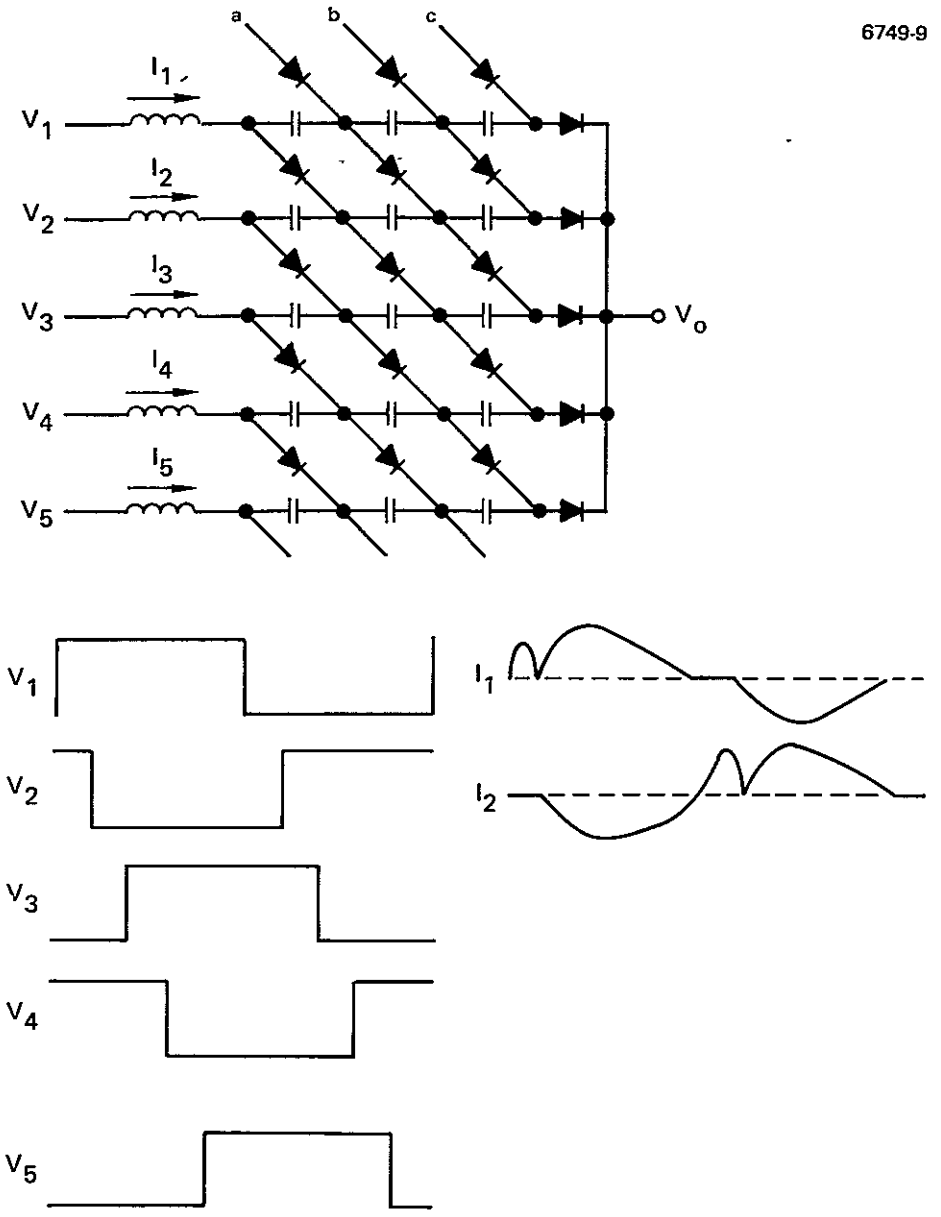
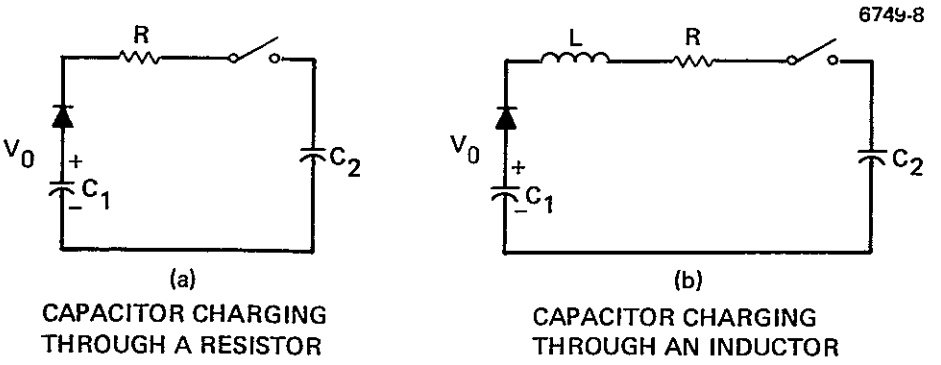


Figure 8. Proper input phasing for a five-phase system.



(a)
CAPACITOR CHARGING THROUGH A RESISTOR

(b)
CAPACITOR CHARGING THROUGH AN INDUCTOR

Figure 9. Options for a capacitor charging circuit.

where V_o is the initial voltage and

$$\tau = R\left(\frac{C_1 C_2}{C_1 + C_2}\right) .$$

Therefore, the power dissipated in the resistor, $W_{R,C}$, is

$$W_{R,C} = \int_0^\infty R\left(\frac{V_o}{R} e^{-t/\tau}\right)^2 dt$$

$$= \frac{V_o^2}{R} \int_0^\infty e^{-2/\tau}\, dt$$

$$= \frac{V_o^2}{R} \left[\frac{\tau}{2} e^{-2t/\tau}\right] \Bigg|_0^\infty$$

$$= \frac{V_o^2}{R} \frac{\tau}{2}$$

$$\boxed{W_{R,C} = \frac{1}{2}\left(\frac{C_1 C_2}{C_1 + C_2}\right) V_o^2 .}$$

Charging a capacitor through an inductor (as with the circuit shown in Figure 9(b)) radically changes the situation. If the system is highly underdamped (the normal situation in a CDVM), the current, i(t), will be given by

$$i(t) = \frac{Vo}{\omega L} e^{-\omega t} \sin(\omega t) \quad 0 \leq t \leq \pi/\omega$$

$$i(t) = 0 \qquad\qquad \pi/\omega \leq t \leq \infty \ ,$$

where

$$\omega = \sqrt{\frac{1}{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)} - \frac{R^2}{4L^2}} \quad .$$

Since the system is underdamped, the frequency, ω, can be approximated by i.e.,

$$\frac{1}{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)} >> \frac{R^2}{4L^2}$$

$$\omega \approx \sqrt{\frac{1}{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}}$$

$$i(t) \leq \frac{Vo}{\omega L} \sin(\omega t), \text{for } 0 \leq t \leq \pi/\omega \ .$$

Integrating $i^2(t)$ R results in

$$W_{R,L,C} = \int_o^{\pi/\omega} \left[\frac{Vo}{\omega L} \sin(\omega t)\right]^2 R \, dt$$

$$= \frac{Vo^2 R}{\omega^2 L^2} \int_o^{\pi/\omega} \sin^2 \omega t \, dt$$

$$= \frac{V_o{}^2 R}{\omega^2 L^2} \left[\frac{1}{\omega} \ \frac{\pi}{2}\right] \quad .$$

But, since

$$\omega \approx \frac{1}{\sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}} \quad ,$$

it follows that

$$W_{R,L,C} = \frac{V_o^2 R}{\omega^3 L^2} \quad \frac{\pi}{2}$$

$$= \frac{V_o^2 R}{2L^2} \left[L\left(\frac{C_1 C_2}{C_1 + C_2}\right)\right]^{3/2}$$

$$\boxed{W_{R,L,C} = \frac{1}{2}\left(\frac{C_1 C_2}{C_1 + C_2}\right) V_o^2 \left[\pi R \sqrt{\frac{C_1 C_2}{(C_1 + C_2)L}}\right] .}$$

In the first case, loss was independent of resistance. But in the second case, loss was a function of inductance, capacitance, and resistance:

$$W_{L,R,C} = W_{RC}\left(\pi R \sqrt{\frac{C_1 C_2}{(C_1 + C_2)L}}\right) .$$

For a typical multiplier with R = 0.03 , L = 10 x 10^{-6}H, and $C_1 = C_2$ = 2 x 10^{-6}:

$$W_{L,R,C} = W_{R,C}\,(\pi \times 0.03)\sqrt{\frac{(2 \times 10^{-6})^2}{(4 \times 10^{-6})\,(10 \times 10^{-6})}}$$

$$= W_{R,C}\,(0.0298) \quad .$$

The inductance in the circuit reduces the capacitance charging losses dramatically, by a factor of ≈33.6.

The value of the inductor, L, in the charging circuit is chosen so that the equivalent input capacitance of the CDVM and the inductance will resonate at the switching frequency. This results in a quasi-sine-wave current in which the current is approximately zero during the switching interval. Therefore, switching losses in the transistors are nearly eliminated. Switching losses still remain to the extent that the transistors must charge junction capacitance, rectifier reverse capacitance, and stray capacitance.

The particular configuration of a CDVM circuit is a function of the desired multiplication factor, load current, and the maximum ratings of available components. Since the output voltage of a multiphase CDVM is approximately equal to M + 1 times the input voltage (where M is the number of capacitor stages in the multiplier), the number of stages is easy to determine from the input/output requirements. Since the number of phases must be chosen to keep all components (transistors, diodes, capacitors) within their maximum current ratings, it is necessary to know the currents in all components as a function of the load current.

In the four-stage N-phase CDVM shown in Figure 10, the average current in each diode can be determined as a function of the number of phases and of the load current. Over a full cycle, the average current in each CDVM rectifier is the load current divided by the number of phases (I_L/N). Since the rectifiers conduct only during one-half of the cycle, the average current during the conduction period is $2\ I_L/N$. For example, consider the single-phase CDVM shown in Figure 11. Since there is only a single path to the output, the average current in all of the rectifiers in that path must be equal in the steady state. Since any rectifier must on average have the load current flowing in it during the half cycle it conducts, each will carry $2\ I_L$. For a two-phase system, there are two paths to the output; therefore, the average rectifier current during conduction will be I_L.

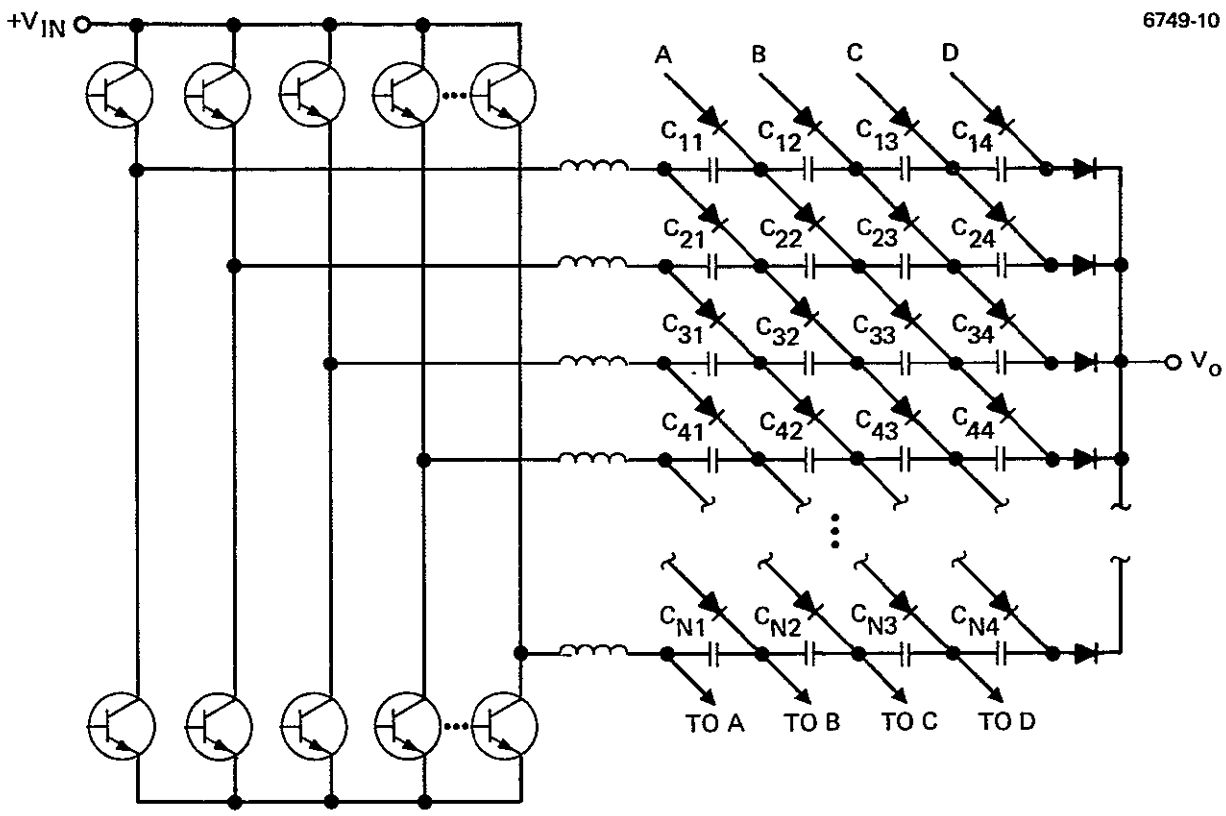


Figure 10. N-phase CDVM circuit.

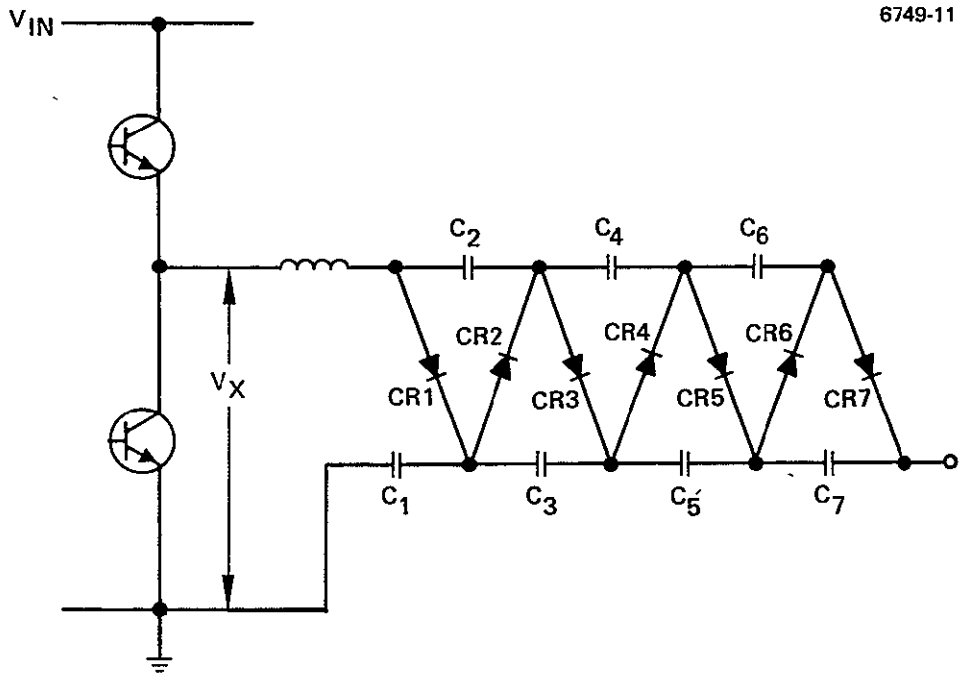


Figure 11. Single-phase multiplier.

Any transistor in the power stage will see an average current of $M/N(I_L)$ over a full cycle where I_L is the dc load current. However, the transistor does not conduct current over a full cycle. Figure 12 demonstrates a typical half-cycle where the Φ_j capacitors are transferring charge to $\Phi_j + 1$ capacitors. The period t_o to t_1 is a dead time in the drive current for the $\Phi_J + 1$ transistors. This prevents shoot-through currents from occurring as a result of stored charge in the "on" transistor. Between t_1 and t_2, the Φ_J input supplies load current while the $\Phi_j + 1$ transistor junctions are cleared. Between t_3 and t_4, the Φ_j capacitors provide charge to the $\Phi_J + 1$ capacitors. The average current during the capacitor charging period is

$$I_{avg} = \frac{M}{N} I_L \left(\frac{T}{t_4 - t_3} \right) \quad ,$$

where $T = 1/f_{sw}$, f_{sw} is the switching frequency of the chopper, and $(t_4 - t_3)$ is a function of the number of phases and of the dead time in the drive current. Assuming that the current waveform is approximately sinusoidal, the peak current I_{pk} in the transistor will be

$$I_{pk} = I_{avg} \frac{\pi}{2}$$

$$\boxed{I_{pk} = \frac{\pi}{2} \frac{M}{N} \frac{T}{(t_4 - t_3)} I_L = \frac{\pi M}{NK} I_L \quad ,}$$

where K is the maximum possible duty cycle.

The rms current in the capacitors is calculated assuming that each rectifier conducts current for approximately the same time interval and that the current in each capacitor is approximately sinusoidal. If C_{xj} is a capacitor in an N-phase, M-stage CDVM (see Figure 10), the average current in that capacitor during conduction will be

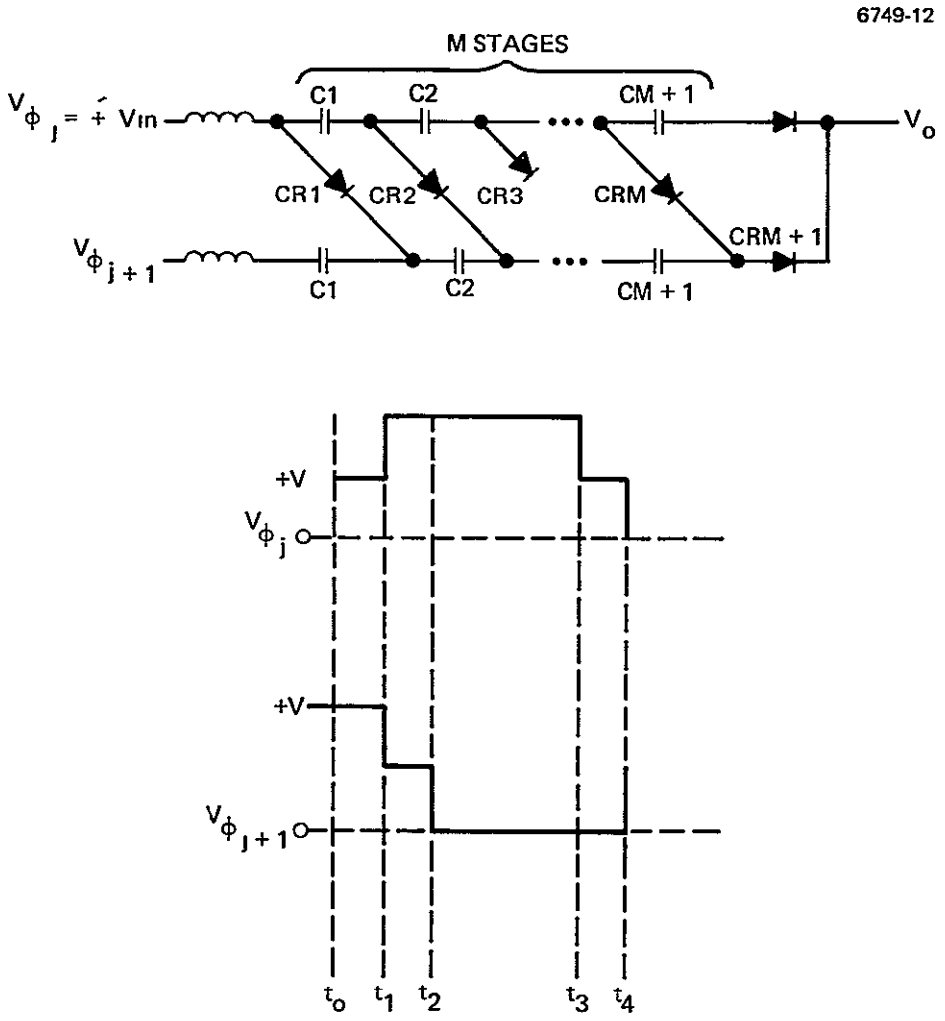


Figure 12. Typical input voltage to a CDVM.

$$\boxed{I_A(C_{xj}) = (M + 1 - j)\,\frac{2I_L}{N}\,,}$$

where j is the capacitor stage number, and x is the capacitor phase number.

If K is the maximum possible ratio of the conduction period to the half cycle (including the effect of drive current dead time), the maximum conduction duty cycle D for C_{xj} is

$$D\,(C_{xj}) = K\,\frac{(M + 1 - j)}{M}\quad .$$

Using the sinusoidal waveform assumption, the peak current I_p in each capacitor is

$$I_p\,(C_{xj}) = I_A\,(C_{xj})\,\frac{\pi}{2}\,\frac{1}{D}$$

$$= (M + 1 - j)\,2\,\frac{I_L}{N}\;\;\frac{\pi}{2}\,\frac{M}{K\,(M + 1 - j)}$$

$$\boxed{I_p\,(C_{xj}) = \frac{\pi}{K}\,\frac{M}{N}\,I_L\quad .}$$

The rms current I_{rms} is then

$$I_{rms}\,(C_{xj}) = I_p\,(C_{xj})\left(\frac{\sqrt{2}}{2}\right)\sqrt{D}$$

$$= \frac{\pi M}{NK}\,\frac{L}{\pi\sqrt{2}}{2}\sqrt{\frac{K\,(M + 1 - j)}{M}}\quad .$$

$$\boxed{I_{rms}\,(C_{xj}) = \frac{\pi\sqrt{2}}{2N}\,\sqrt{\frac{M}{K}\,(m + 1 - j)}\;I_L\,.}$$

The upper bound for the output ripple voltage may be determined by considering the maximum ΔV for a single phase. The ΔV on each capacitor C_{xj} (see Figure 7) of an M-stage, N-phase capacitor is found from the equation

$$\Delta V(C_{xj}) = I_A(C_{xj}) \frac{1}{C_{xj}} \Delta t$$

$$= \frac{2\,(M + 1 - j)\, I_L}{N} \left(\frac{1}{C_{xj}}\right) \frac{1}{2f}$$

$$\boxed{V(C_{xj}) = \frac{(M + 1 - j)\, I_L}{Nf\, C_{xj}} \quad .}$$

The total ΔV on a given phase is the sum of all the capacitor ΔV's:

$$\boxed{\Delta V_{TOT} = \sum_{j=1}^{M} \Delta V(C_{xj}) \quad .}$$

The actual output ripple voltage for an N-phase CDVM will be some fraction of ΔV_{TOT} since load current will normally commutate to the next conducting phase before all capacitors in the string have discharged to their lower bound.

The output voltage is a function of the number of stages, transistors, and rectifier forward drops and of ΔV_{TOT}. In general, assuming a positive supply only, the output voltage is

$$V_o = V_{C1} + V_{C2} + \ldots + V_{CM} + (V_{in} - V_{ce}(on))$$

$$- \left(\frac{1}{2} \Delta V_{TOT}\right)$$

$$V_o = M\,(V_{in} - 2V_{ce}(on) - V_{fwd}) + V_{in} - V_{ce}(on) - \frac{1}{2}\,\Delta V_{TOT}\ ,$$

where

V_{in} = the input bus voltage

$V_{ce}(on)$ = the transistor collector-emitter "on" voltage

V_{fwd} = rectifier toward voltage

ΔV_{TOT} = calculated output ripple voltage.

In their approximate order of importance, the loss terms are

- Transistor drive and logic power — $P_D(TOT)$
- Transistor switching losses (capacitance charging) — P_{sw}
- Rectifier forward losses — P_{fwd}
- Transistor "on" losses — $P_{"on"}$
- Capacitor equivalent series resistance (ESR) losses — P_{ESR}
- Miscellaneous (wire resistance, inductor series resistance losses (0.5%)). — P_{MSC}

The transistor drive current is intended to provide adequate base drive for the peak collector current condition. Effectively, each phase requires a constant amount of drive current because, at any given time, either the upper or the lower transistor is "on." If, as previously defined, the peak collector current is $(\pi/K)\,(M/N) \cdot I_L$, then required base drive current is

$$I_b = \frac{\pi}{K}\,\frac{M}{N}\,\frac{I_L}{h_{FE}}\ ,$$

where h_{FE} is the minimum expected transistor common emitter current gain. The drive power P_B into the base of the transistor is

$$P_B = I_b \, V_{BE} \quad ,$$

where V_{BE} is the base-to-emitter voltage of the power transistor. The total drive power (P_B (TOT)) is

$$P_B \text{ (TOT)} = n \, P_B/\eta_D$$

$$= \frac{\pi M I_L}{K \, h_{fe}} V_{BE} \frac{1}{\eta_D} \quad ,$$

where η_D is the efficiency of the drive/logic circuit. η_D is dependent on the particular drive circuit used and must be derived in terms of that specific circuit. A typical drive circuit will operate between 15 and 30% efficiency.

The three components of transistor switching losses are transistor junction capacitance charging, rectifier junction capacitance charging, and stray capacitance charging. The transistor switching losses in a single phase are

$$P_{sw} = (C_{Qj} + M \, C_{RJ} + C_{stray}) \, V_{in}^2 \quad ,$$

where C_{Qj} is the equivalent transistor junction capacitance, C_{Rj} is the reverse rectifier junction capacitance, and C_{stray} is the stray capacitance to ground from the transistor chopper output.

The total number of rectifiers carrying current is (M + 1)N. The average current in each rectifier over a full cycle is I_L/N. The total rectifier dissipation is then

$$P_{fwd} = \frac{I_L}{N} V_{fwd} \left[(M + 1) N\right]$$

$$\boxed{P_{fwd} = I_L V_{fwd} (M + 1) \quad ,}$$

where V_{fwd} = average rectifier forward voltage.

The transistor forward losses can be estimated by assuming that essentially the whole bus current must be handled by two transistors:

$$P_{"on"} = I_{in} V_{ce}(on)\ 2 \quad .$$

But, since the input current is $I_{in} = M I_L$, it follows that

$$\boxed{P_{"on"} = 2M I_L V_{ce}(on) \quad .}$$

The capacitor ESR losses are

$$P_{ESR} = \sum_{x=1}^{N} \sum_{j=1}^{M} I_{rms}^{\ 2} (C_{xj})\ ESR\ (C_{xj})$$

$$\boxed{P_{ESR} = N \sum_{j=1}^{M} I_{rms}^{\ 2} (C_{xj})\ ESR\ (C_{xj}) \quad ,}$$

where

$I_{rms}\ (C_{xj})$ = rms current in C_{xj}

$ESR\ (C_{xj})$ = equivalent series resistance in C_{xj} .

The miscellaneous losses (estimated to be ≈0.5% of total output power) are primarily a function of wiring resistance, inductor series resistance, and dc leakage currents in semiconductors. The efficiency of the CDVM converter is

$$N = \frac{P_o}{P_o + P_D(TOT) + P_{sw} + P_{fwd} + P_{on} + P_{ESR} + P_{MSC}}$$

During a load fault, an output inductor limits the peak current in the CDVM rectifiers and capacitors. Because the transistors can be turned off within a single cycle, the peak current in the inductor will be determined primarily by the amount of stored energy in the CDVM capacitors and by the size of the inductor. The peak inductor current is

$$I_p^2 \approx \frac{C_{TOT}}{L} (V_{in})^2$$

where

$$C_{TOT} = \sum_{x=1}^{N} \sum_{j=1}^{M} C_{xj} \quad .$$

The rectifier peak currents during a fault will be

$$I_p \text{ (rect)} = \frac{I_p}{N} = \sqrt{\frac{C_{TOT}}{L}} \left(\frac{V_{in}}{N}\right) \quad .$$

The capacitor peak current will be less than or equal to the rectifier peak in all cases. Since the capacitors are generally capable of much higher peak currents than are the rectifiers, the capacitors will not be damaged during a fault.

To protect the transistors during a fault, the devices must be turned off before the maximum rating is exceeded. Usually, the worst case dissipation in the transistor does not occur during the fault because the transistors are turned off before their collector current becomes excessive. The worst case for the transistors occurs during turn-on when all CDVM capacitors must be recharged. During the first few cycles, the transistors are forced out of the saturation region where the peak dissipation is very high. Proof of operation within tolerable limits during start-up is best demonstrated by testing

rather than by analysis. As a first approximation, the energy (W_Q) in the power transistor can be assumed to not exceed the losses associated with fully charging the first capacitor stage:

$$W_Q \leq \frac{1}{2} C_{x1} V_{in}^2 \quad .$$

If ≈5 cycles are required to charge the capacitor, the average power will be

$$P_{avg} \text{ (start-up)} = \frac{f_{sw}}{5} W_Q \quad .$$

Since the maximum collector current is limited by the base drive current, the effective voltage and current during startup is approximated by

$$I_Q = h_{FE} I_b$$

$$V_{ce} \approx \frac{P_{avg} \text{ (start-up)}}{I_Q} \quad .$$

Once these are calculated, they can be compared with the published operating range.

B. DETAILED CIRCUIT CONFIGURATION

The design goals for the high-power CDVM were

- V_{in} = 200 to 300 Vdc
- Voltage multiplication (M + 1) = 5
- Output current = 0.80 A
- Short-circuit protected .

The voltage multiplication ratio requirement determines the number of capacitance stages to be four. For M = 4, Table 1 lists the required component ratings as a function of load current. Transistor peak currents are better utilized if the number of phases is odd. Also, three-phase systems utilize the transistors poorly because they yield a low duty cycle, K.

Given a transistor current rating of 10 A and a rectifier current rating of 1 A, the 2-phase CDVM would just meet the design requirement. The peak transistor current would be 6.32 A, and the average rectifier current would be 0.80 A. Because peak currents in the rectifiers are significantly higher than are the average currents, the rectifiers should be derated by 50%. Since three- and four-phase systems result in high peak currents in the transistors, a five-phase CDVM was selected for the design.

Table 1. Comparison of Multiphase CDVM Circuits for N = 1 to 9

Number of Phases (N)	Maximum Duty Cycle (K)	Rectifier Average Current during Conduction	Transistor Peak Current (I_{pk})	RMS Capacitor Current (I_{rms} (C_{xJ}))			
				C_{x1}	C_{x2}	C_{x3}	C_{x4}
1	0.8	2 I_L	16 I_L	9 9 I_L	8 6 I_L	7 9 I_L	5 6 I_L
2	0 8	I_L	7 9 I_L	5 0 I_L	4 3 I_L	3 9 I_L	2 8 I_L
3	0 47	0 67 I_L	8 9 I_L	4.3 I_L	3 7 I_L	3 1 I_L	2.2 I_L
4	0.3	0 50 I_L	11 0 I_L	4 1 I_L	3 5 I_L	2 9 I_L	2 0 I_L
5	0 60	0 40 I_L	4 2 I_L	2 3 I_L	2 0 I_L	1 6 I_L	1 1 I_L
6	0 47	0 33 I_L	4 5 I_L	2 2 I_L	1 9 I_L	1 5 I_L	1 1 I_L
7	0 63	0.29 I_L	2 9 I_L	1.6 I_L	1 4 I_L	1 1 I_L	0 80 I_L
8	0 55	0 25 I_L	2 9 I_L	1 5 I_L	1 3 I_L	1 1 I_L	0.75 I_L
9	0 69	0.22 I_L	2 0 I_L	1.2 I_L	1.0 I_L	0 84 I_L	0.59 I_L

A block diagram of the complete CDVM circuit is shown in Figure 13. A 700 kHz astable multivibrator provides a clock signal to a five-phase capacitor metal oxide semiconductor (CMOS) logic circuit. The five-phase generator outputs two drive signals, V_{G1} and V_{G2}, for each phase (see Figures 14 and 15). The five-phase power stage drives the capacitor-diode matrix through small air-core inductors. The inductors, by limiting the peak currents in the transistors and rectifiers, cause the capacitors to be charged efficiently. The primary function of the output filter (a π filter) is to limit the peak currents in the CDVM with an inductor during load faults. If it is necessary to reduce ripple voltage reduction, the output capacitance can be increased. The output current is sensed through a 1 Ω resistor in the return path. When an over-current is sensed, the protection circuit turns off drive current to all the upper transistors in the power stage. When there is a continuous load fault, a one-shot multivibrator sets the time between restart intervals.

The logic circuit for a five-phase circuit is composed of a decade counter and three four-bit shift registers. The circuit shown in Figure 16 produces 10 signals, each shifted $1/f_{clock}$ from the other (see Figure 17). A_j and A_{J+5} (J = 0, 1, ... 4) are the two inputs to the phase j driver. During a load fault, the overcurrent signal goes high as long as the current exceeds the trip level. With the overcurrent signal high, a prescribed order of "1"s and "0"s are parallel loaded into the shift registers, which immediately turn off all upper transistors.

The drive circuit (shown in Figure 15) consists of a current-source-driven transformer. One or both of the drive transistors are always on. When V_{G1} is high, the upper transistor turns on. When V_{G2} is high, the lower transistor is on. When V_{G1} and V_{G2} are both high, the stored charge is removed from the base region of the transistor that has been on. The output from the five-phase power stage drives a five-phase CDVM.

A five-phase capacitor-diode matrix is shown in Figure 18. All rectifiers are series redundant (which improves the reliability of the

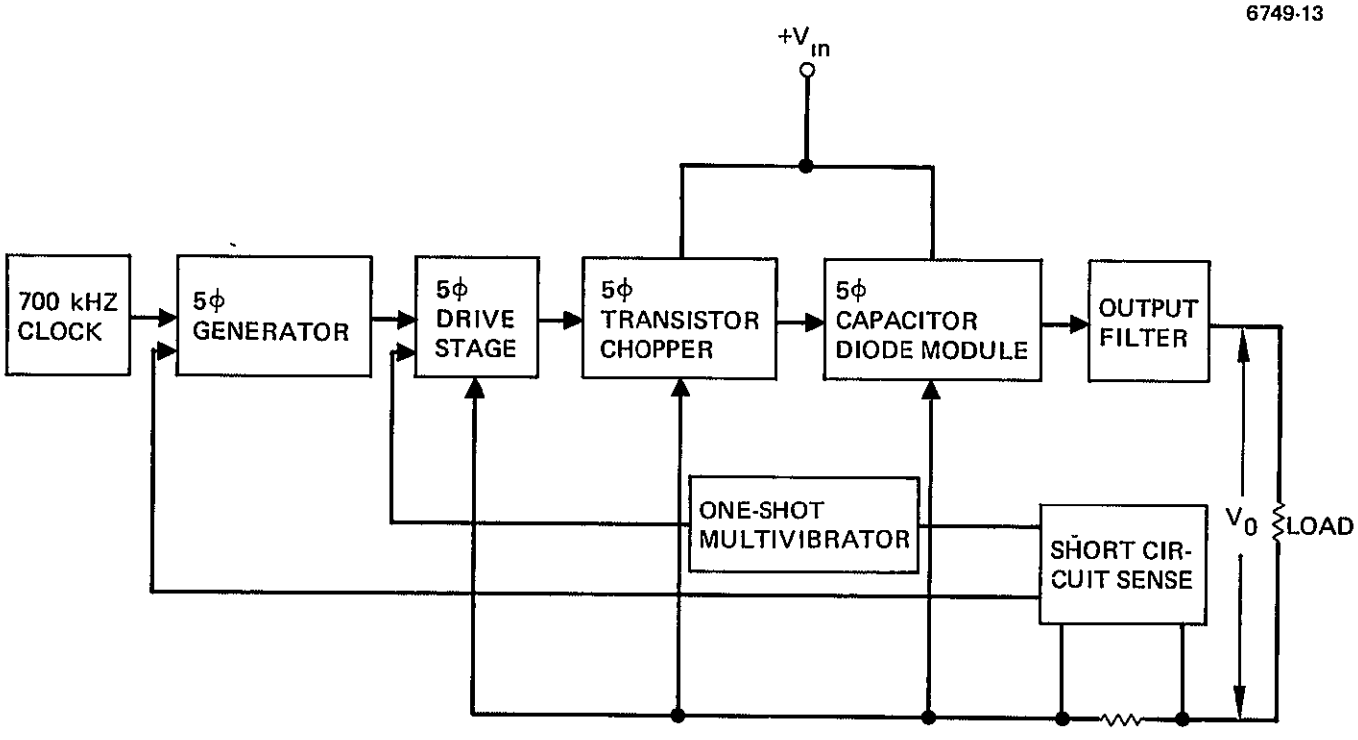


Figure 13. CDVM block diagram.

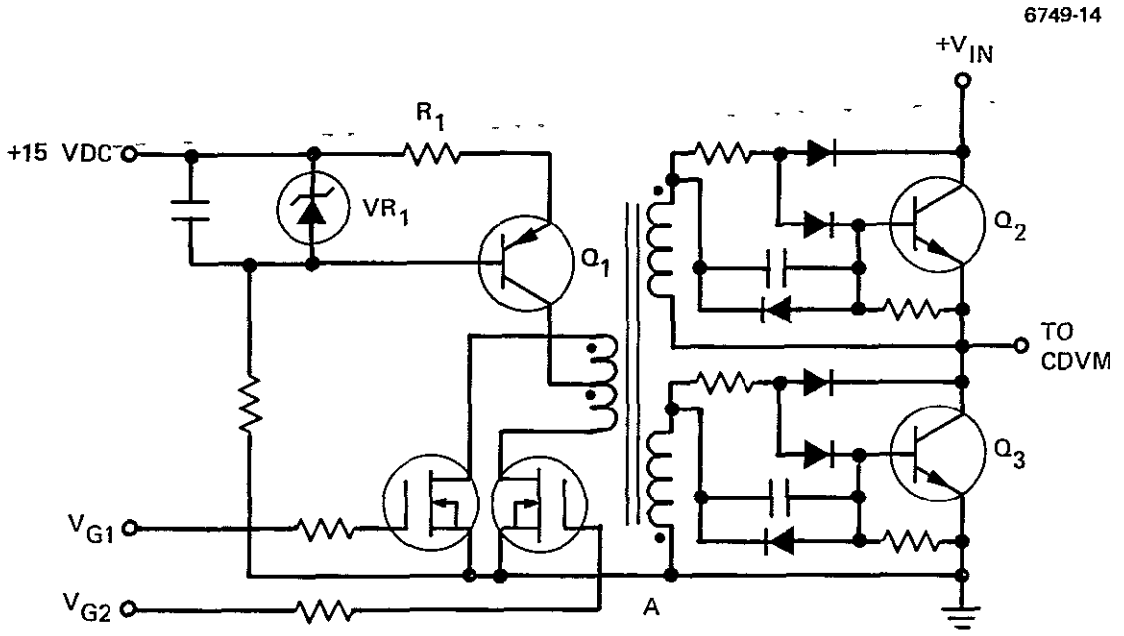


Figure 14. CDVM power stage.

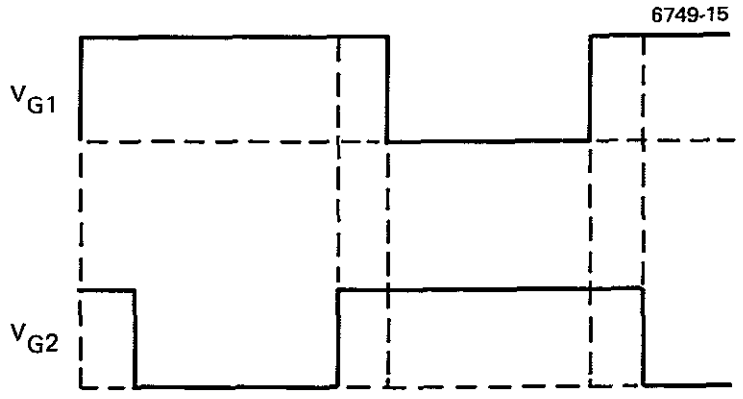


Figure 15. Typical inputs to the CDVM power stage.

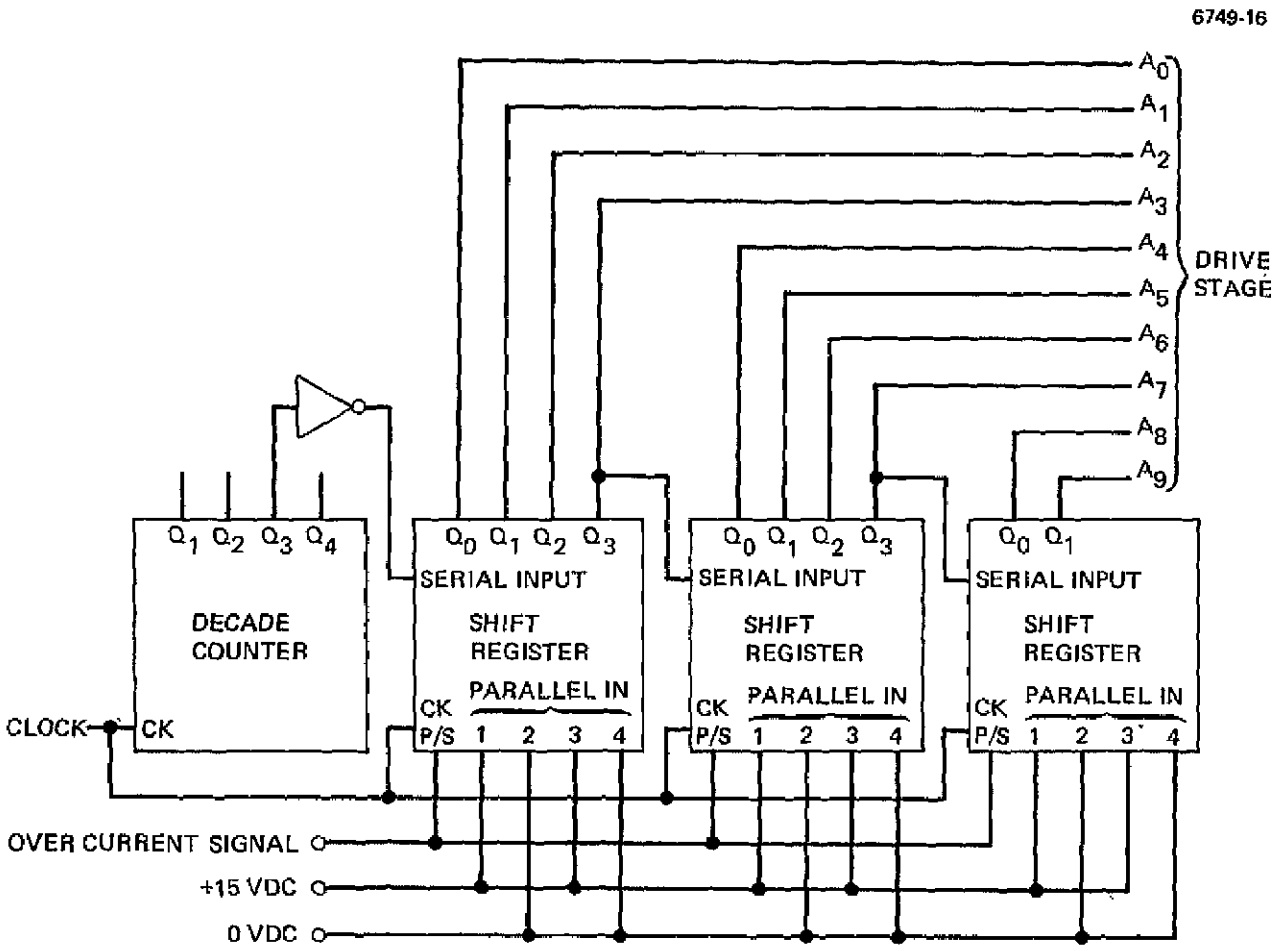


Figure 16. Five-phase logic circuit.

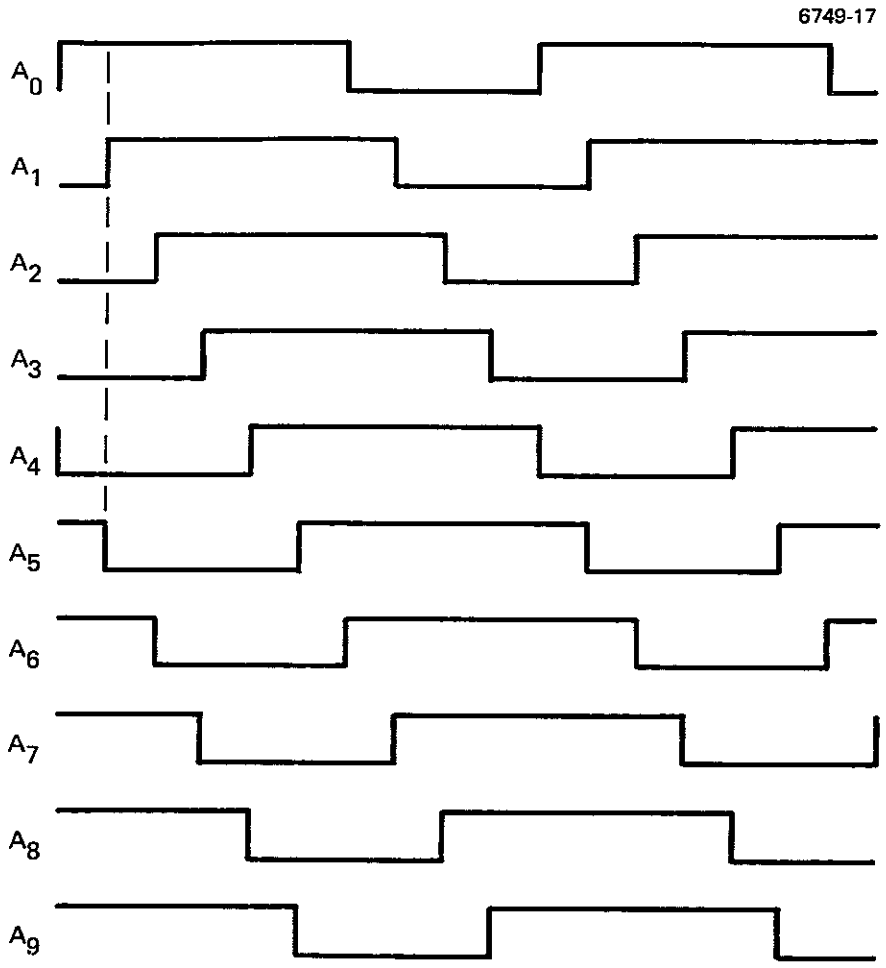


Figure 17. Logic circuit outputs.

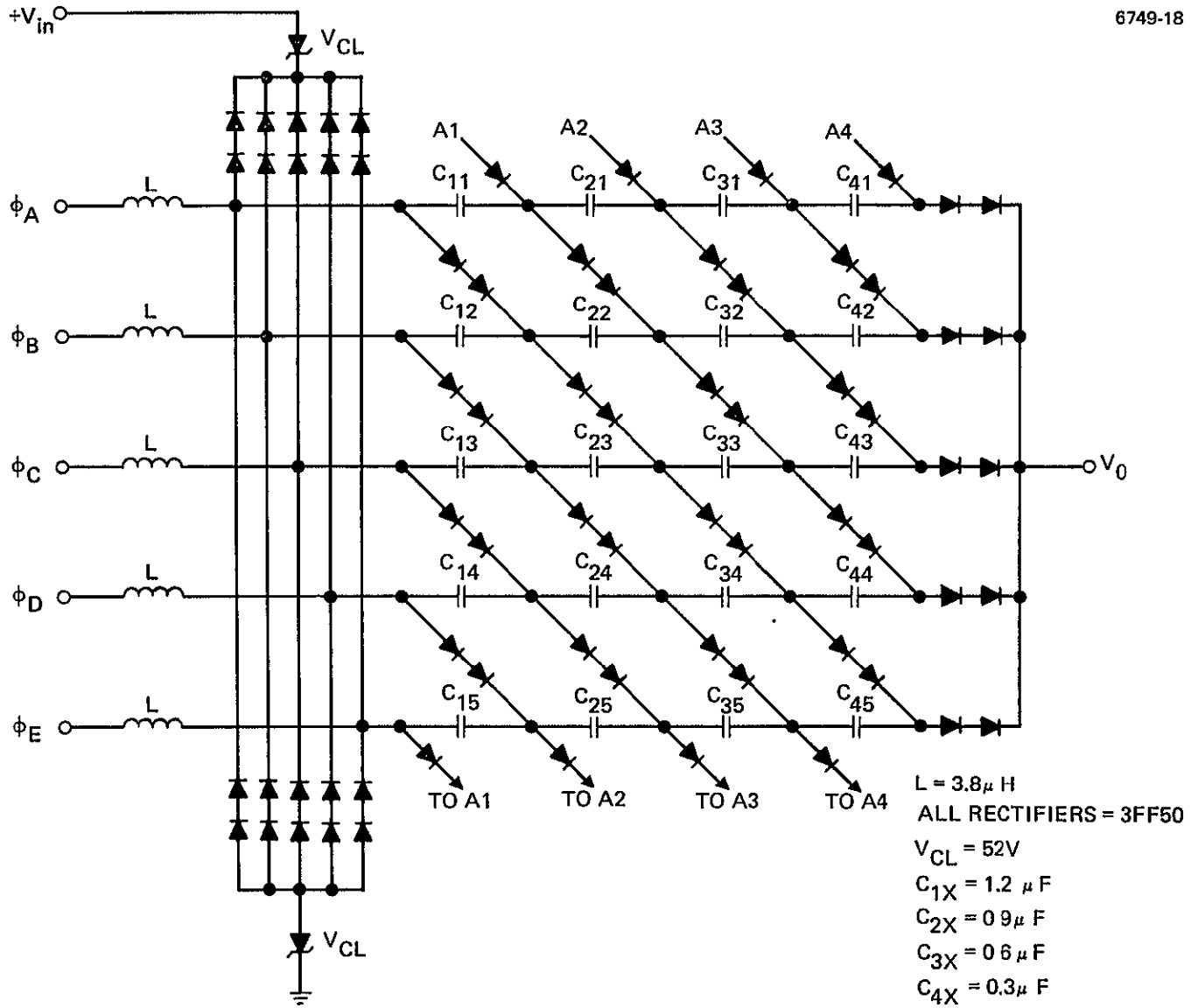


Figure 18. Capacitor-diode matrix.

CDVM), and each phase input is clamped so that the voltage across any rectifier cannot exceed $V_{in} + 2V_{CL}$ during a start-up or a load-fault transient. Since the inductor was chosen to resonate with the average input capacitance of the CDVM at approximately 90 kHz, the current will be approximately zero in the inductor (also in the transistor) when the transistor switches. The correct phasing for a five-phase CDVM is shown in Figure 19. This particular phasing allows the conduction duty cycle to be maximized in the transistors.

The output inductor has been selected to limit the peak output current to approximately 55 A during a load fault. Using an expression previously derived, it follows that

$$I_p^2 = \frac{C_{TOT}}{L} (V_{in})^2$$

$$L = \frac{V_{in}^2}{I_p^2} (C_{TOT}) = \frac{300^2}{(55)^2} (12\ \mu F) = 357\ \mu H\ .$$

$$\boxed{L = 357\ \mu H\ .}$$

Because the choke requires a high volt-second product and a low inductance, an air-core inductor is used.

The overcurrent sense circuit consists of a sense resistor, a comparator, and a one-shot multivibrator. When the current exceeds a predetermined trip point, the comparator output will go low, start the one-shot multivibrator, and parallel load the shift registers. The output of the one-shot multivibrator immediately disables all current sources in the drive circuit. When the output current decays below the trip point, the comparator output will go high and allow the shift registers to begin running in the serial mode. After ≈1 msec, the one-shot multivibrator returns to its normal state and allows the current sources to turn "on." If a continuous fault is applied to the output, the circuit will attempt to restart every 1 msec until the fault is removed. For the overcurrent sense circuit to function properly, the power source return must be isolated from the CDVM output return; if it is not, current will not flow through the sense resistor.

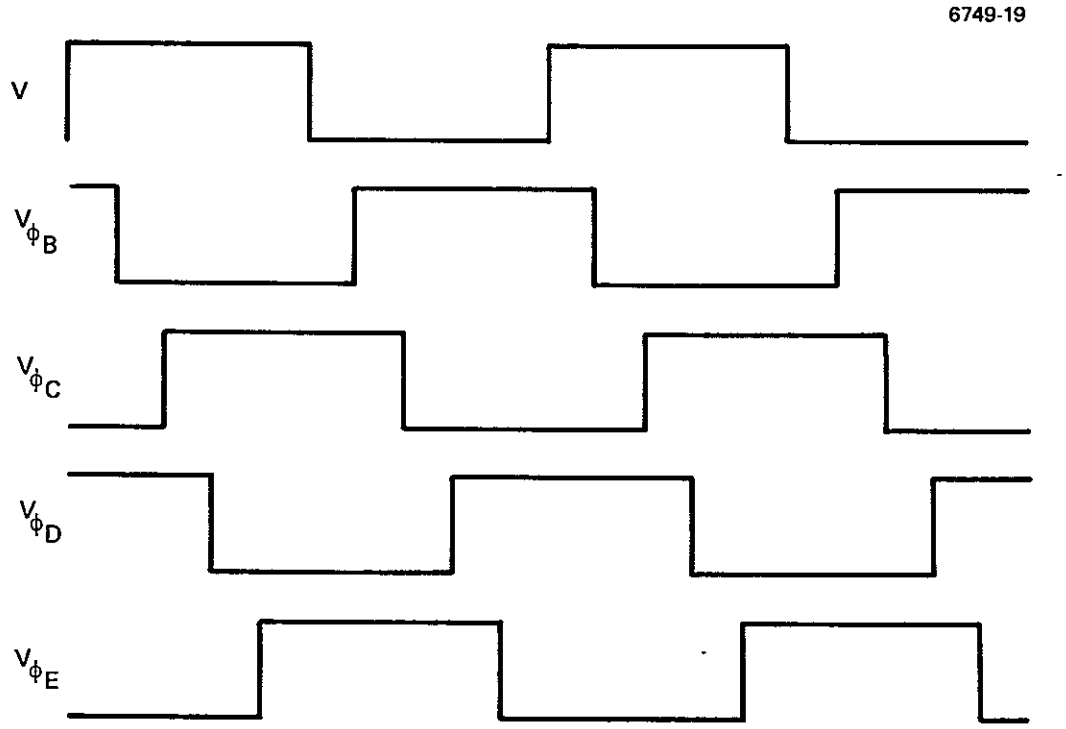


Figure 19. Correct phasing for a five-phase CDVM.

C. COMPONENTS

When inductors are used in series with the CDVM, losses are a function of the resistance in series with the capacitors. Since efficiency is of prime importance, the capacitor should have very low dissipation factors. Three capacitor films have been considered for this application: polysulfone, polyvinylfluoride (PVF2), and polycarbonate. We chose a polysulfone film; it has an extremely low dissipation factor and a high service temperature (≈150°C with no derating required).

A PVF2 film is considered a strong second choice because its high dielectric constant would yield a lighter capacitor. However, the dissipation factor of PVF2 is not accurately known. Measurements performed at Hughes during a study (performed for NASA LeRC under Contract NAS 3-18925) of high-energy density capacitors indicated a dissipation factor at 100 kHz of 35%.

In the same study, a dissipation factor of the polysulfone film capacitor was reported at 0.7%. However, since the dissipation factor of a 2-μF capacitor is extremely difficult to measure at 100 kHz, further study of the PVF2 capacitor might show that a much lower dissipation factor could be attained by better termination techniques.

Polycarbonate film capacitors compare favorably with polysulfone capacitors. However, their limited temperature range (they must be derated for temperature above 85°C) restrict their use somewhat. In spite of the temperature restriction, polycarbonate capacitors are another viable alternative, and they are commercially available.

Polysulfone capacitors can be reliably fabricated for voltage ratings between 300 and 1,000 Vdc and for capacitance values between 0.1 and 5 μF. For voltages less than 300 Vdc, the film becomes too thin to handle. Capacitances above 5 μF result in yield problems because of large-film surface error and the probability of flaws in the film. Capacitors with capacitances less than 0.1 μF are difficult to fabricate because the end termination area is very small.

With the voltage multiplier operating at 100 kHz, the reverse recovery time and reverse capacitance of the rectifiers are of prime importance. Several rectifiers in the 1 to 3 A range have 100 to 200 nsec

recovery times. The fastest reverse recovery time presently available is ≈30 nsec. The Semtech 3FF50 rectifier has 30 nsec recovery times, a 500 Vdc reverse blocking voltage, and a 1 A forward current rating. The surge rating (60 Hz half cycle rating) is 25 A peak.

High-speed, high-voltage transistors are becoming more readily available. There are several transistors capable of handling 8 to 15 A and 400 to 500 Vdc. The Motorola MJ7261 transistor is representative of the type of device required to drive a multiphase voltage multiplier operating from a 300 V bus. The V_{ceo} (sustained) is 400 V and the continuous collector current rating is 15 A. Rise and fall times of this device are typically 150 nsec.

SECTION 3

BREADBOARD MODEL TEST RESULTS

Table 2 lists the basic assumptions and the specific equations used to predict the input to output voltage transfer ratio. These equations assume that the drops in transistor and rectifier forward voltages remain constant with respect to load current. The transfer ratio then is a simple function of input voltage and load current:

$$\frac{V_o}{V_{in}} = \frac{5\ V_{in} - 14.4 - 19\ I_L}{V_{in}}$$

As shown by Figure 20, the test data corresponds very well with the predicted performance. The largest discrepancy (which occurs at 200 Vdc input line and 0.275 A) is .

$$\text{Maximum Error} = \frac{4.924 - 4.900}{4.924} \times 100 = 0.49\%$$

The predicted output voltage is

$$V_o = 5\ V_{in} - 14.4 - 19\ I_L \quad .$$

If the current went from 0.2 A to 0.8 A, the predicted change in the output voltage would be

$$\Delta V_o = \left[5\ V_{in} - 14.4 - 19\ (0.8)\right] - \left[5\ V_{in} - 14.4 - 19\ (0.2)\right]$$

$$= 19\ (0.2 - 0.8)$$

$$= 11.4 \text{ Vdc} \quad .$$

Table 2. Calculation of the Voltage Transfer Ratio

Assumptions

M = 4	C_{x1} = 1.2 μF
N = 5	C_{x2} = 0.9 μF
f = 70 kHz	
$V_{ce}(oh)$ = 0.8 V	C_{x3} = 0.6 μF
V_{fwd} = 2.0 V	C_{x4} = 0.3 μF

Equations

$$\Delta V_{TOT} = 38.1\ I_L$$

$$V_o = 5\ V_{in} - 14.4 - 19.0\ I_L$$

$$\frac{V_o}{V_{in}} = \frac{5\ V_{in} - 14.4 - 19\ I_L}{V_{in}}$$

The predicted load regulation for a change in current from 0.2 A to 0.8 A is

$$\text{Load Regulation} = \frac{11.4\ \text{Vdc}}{1500\ \text{Vdc}} \times 100 = 0.76\%\ (V_{in} = 300\ \text{Vdc})$$

and

$$\text{Load Regulation} = \frac{11.4\ \text{Vdc}}{1000} \times 100 = 1.14\%\ (V_{in} = 200\ \text{Vdc})\ .$$

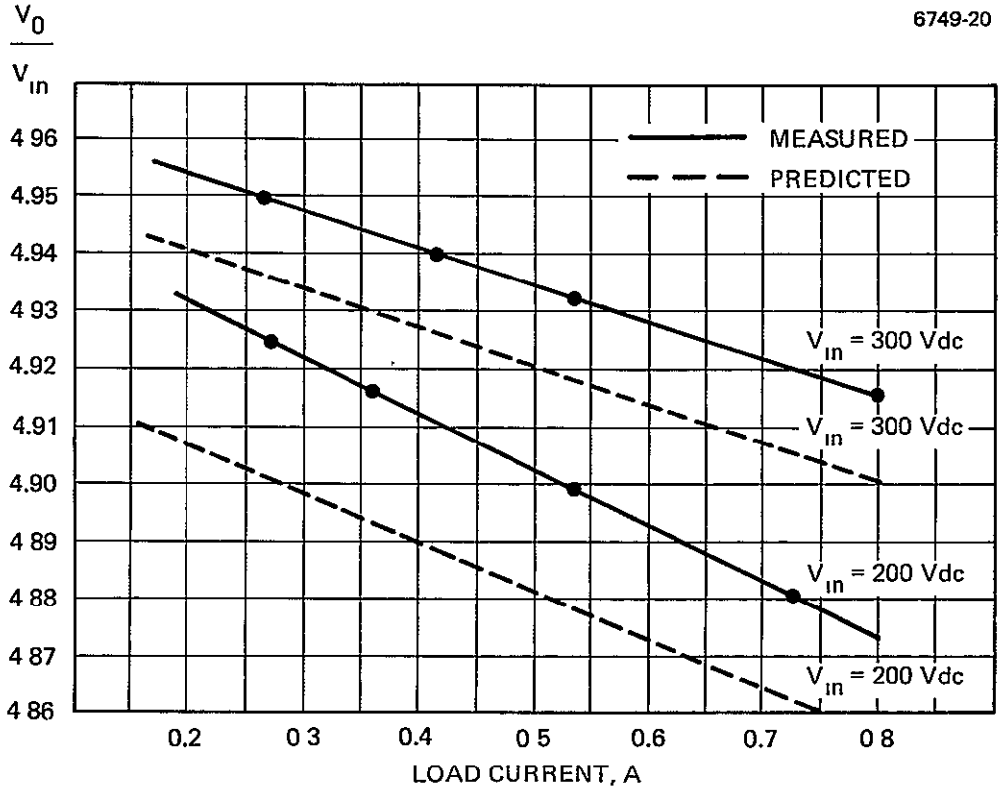


Figure 20. Voltage transfer ratio.

Using the data in Figure 20, the output regulation for I_L in the range of 0.2 A to 0.8 A is

$$\text{Output Regulation} = \frac{4.954 - 4.915}{4.915} = 0.793\% \quad (V_{in} = 300 \text{ Vdc})$$

$$\text{Output Regulation} = \frac{4.932 - 4.873}{4.873} \times 100 = 1.2\% \quad (V_{in} = 200 \text{ Vdc}) .$$

The loss equations for a five-phase, four-stage CDVM are summarized in Table 3. The predicted efficiencies and measured efficiencies for V_{in} = 200 Vdc and V_{in} = 300 Vdc are summarized in Figure 21. Although the predicted efficiencies are slightly higher than the actual efficiencies, they generally differ by less than 0.5%.

Many photographs were taken to demonstrate the operation of the CDVM. Since the photographs were identical for all five phases, only photographs from one representative phase have been included in this report.

Figures 22 and 23 show the time relationship between the phase voltages and the phase currents. For a given phase, the input current is zero when the voltage transition occurs. Also, when a phase first goes high, it will immediately supply current to the output filter. Slightly later, when the next phase goes low, charging currents will begin to flow.

The transistor waveforms for phase A (as defined in Figure 18) are shown in Figures 24 and 25. The predicted peak current in the transistors was

$$I_p = \frac{\pi M}{NK} I_L = \frac{4(3.142)}{5(0.6)} (0.8) = 3.35 \text{ A} .$$

The observed peak current was 3.5 A. I_D is the output current from the drive transformer; I_B is the actual current into the base of the transistor. Near the end of the half cycle, the drive current is shunted through the clamp diode, and the transistor base current is practically zero. This low base current results in low stored charge in the base of

Table 3. Efficiency Calculation

Assumptions

$V_{ce}(on) = 0.9$ V

$V_{fwd} = 2.0$ V (2 rectifiers)

$C_{QJ} = 80$ pF

$C_{Rj} = 8$ pF

$C_{stray} = 150$ pF

f = 70 kHz

M = 4

N = 5

ESR (C_{x1}) = 0.010 Ω

ESR (C_{x2}) = 0.020 Ω

ESR (C_{x3}) = 0.030 Ω

ESR (C_{x4}) = 0.040 Ω

Loss Equations

$P_D = 12$ W (measured)

$P_{sw} = 9.45 \times 10^{-5} V_{in}^2$

$P_{fwd} = 10 I_L$

$P_{"on"} = 9 I_L$

$P_{esr} = (1.316) I_L^2$

$P_{mso} = 0.005 P_o = 0.025 V_{in} I_L$

Efficiency Equation

$$\text{Efficiency} = \frac{P_o}{P_o + P_D + P_{sw} + P_{fwd} + P_{"on"} + P_{esr} + P_{mso}}$$

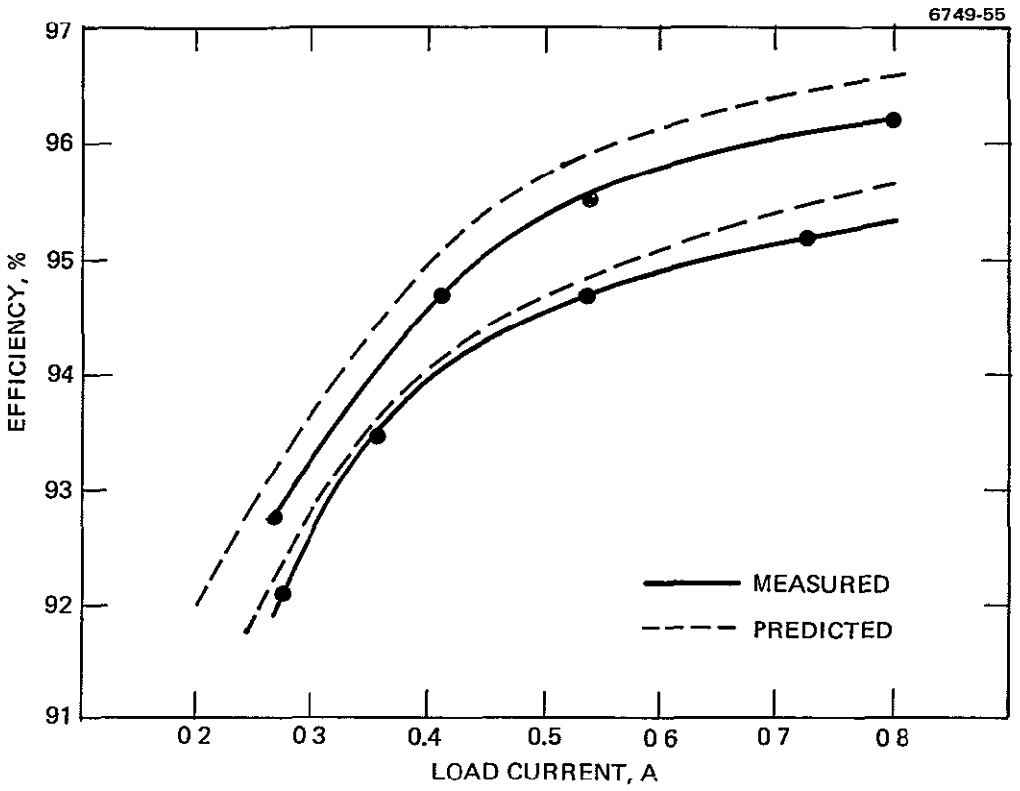


Figure 21. Efficiency versus load current.

6749-21

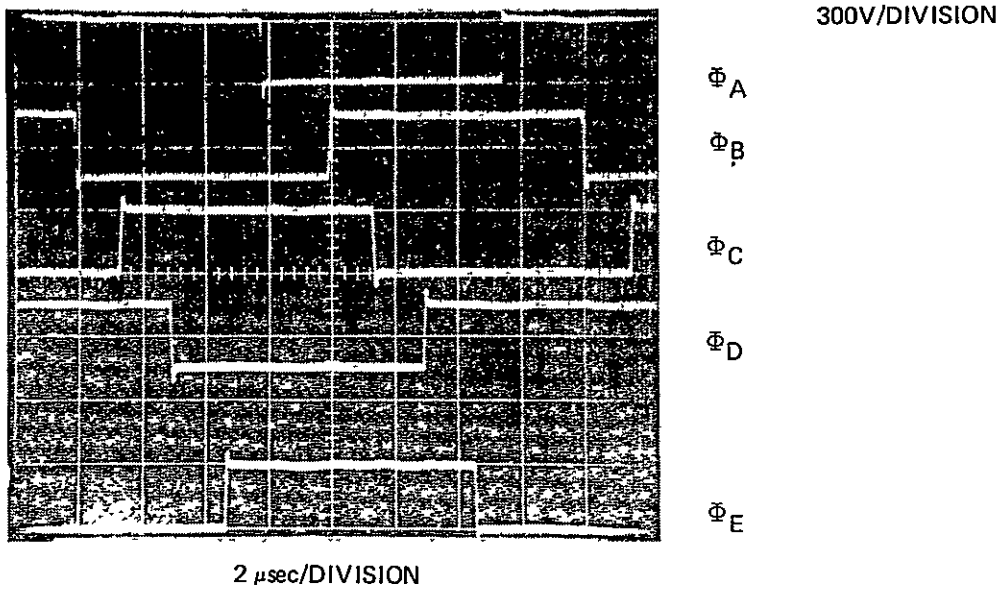


Figure 22. CDVM input voltages (I_L = 0.8 A, V_{in} = 300 Vdc).

6749-22

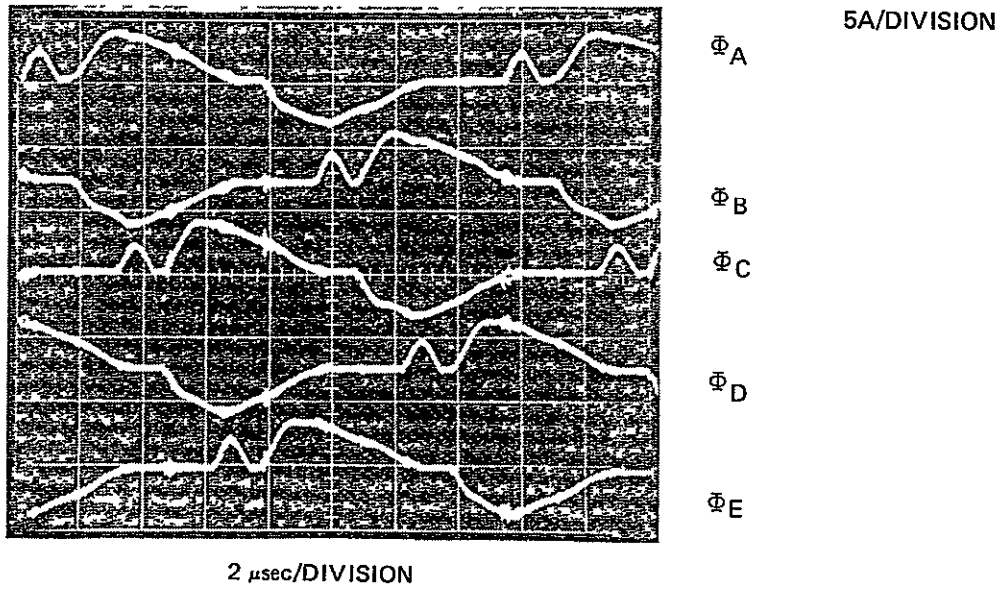


Figure 23. CDVM input currents (I_L = 0.8 A, V_{in} = 300 Vdc).

6749-23

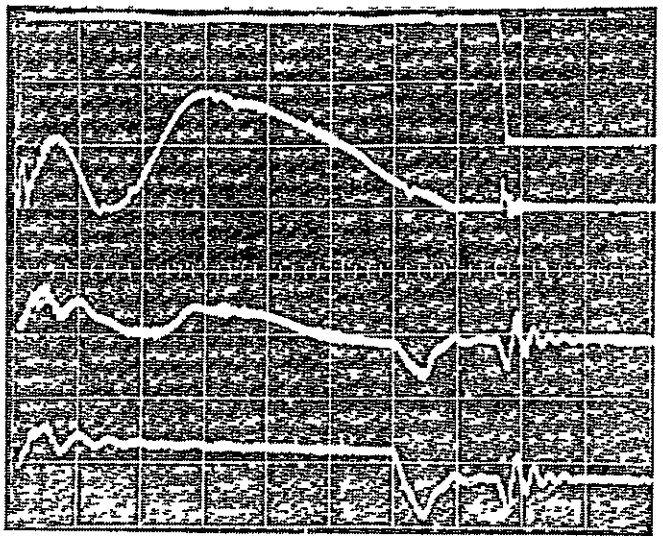


Figure 24. Upper transistor currents (I_L = 0.8 A, V_{in} = 300 Vdc).

6749-24

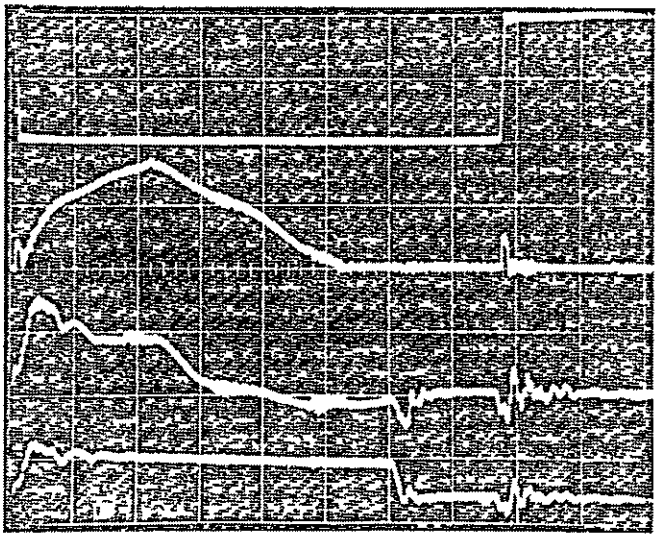


Figure 25. Lower transistor currents (I_L = 0.8 A, V_{in} = 300 Vdc).

the transistor and prevents shoot-through currents. Figures 26 through 31 demonstrate typical "on" voltages and switching waveforms of the transistor power stage.

Figure 32 is a multiple exposure photograph indicating how all the rectifier currents sum to the phase input current. Figures 33 through 37 show the phasing and relative magnitude of all rectifier currents.

The phase A capacitor currents (as defined in Figure 18) are shown in Figure 38. Comparing the rectifier currents during the positive half cycle, C_{4A} carries the same current as CR_{5A}, and C_{3A} carries the sum of the currents in C_{4A} and CR_{4A}. Ultimately, all of the rectifier currents except CR_{1A} sum up in the first capacitor C_{1A}.

The input current is shown in Figure 39. A 10-Ω resistor has been placed in series with the power supply to simulate the solar panel impedance; this, in conjunction with the 3.2-μF capacitor, results in essentially a dc input current (I_3).

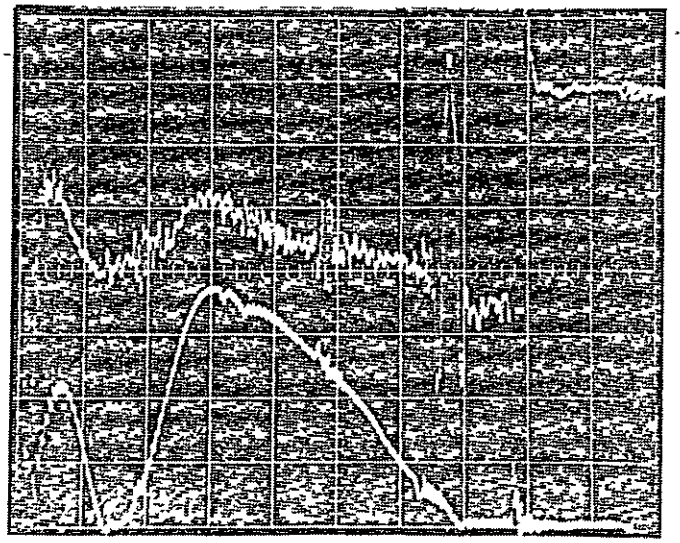
The output ripple voltage for I_L = 0.8 A and I_L = 0.4 A is shown in Figures 40 and 41. Unfortunately, the voltage scale is probably wrong for one of the photographs; this was not discovered before the breadboard was shipped. The equation for output (before the inductor) ripple voltage indicates that the maximum ΔV should be

$$\Delta V_{TOT} = 38.1\ I_L \quad .$$

For I_L of 0.8 A, ΔV_{TOT} will equal 30.5 V. The peak-to-peak output ripple voltage in Figure 40 is 24 V_{pp}, which correlates well with the calculation. The maximum output ripple voltage for I_L = 0.4 A should be less than 15.3 V_{pp}; it was, however, measured at 24 V_{pp}. The output ripple voltage measurements, because of the uncertainty in voltage scale, cannot be used to prove or disprove the output ripple equation. The total peak-to-peak ripple voltage would at most be (V_{in} = 300 Vdc) 3%, which could be easily filtered to less than 1% peak-to-peak.

Tests were performed to determine the transient response characteristics of the CDVM to transients in load and line conditions. Because of the long time constant of the 10-Ω resistor and of the

6749-25



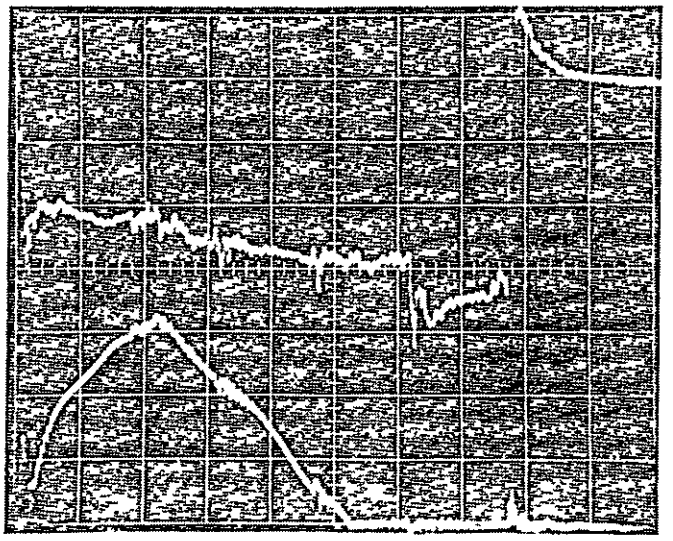
V_{CE} (on) 1 V/DIVISION

I_C 1 A/DIVISION

1 μsec/DIVISION

Figure 26. V_{ce} (on) for the upper transistor (V_{in} = 300 Vdc I_L = 0.8 A).

6749-26



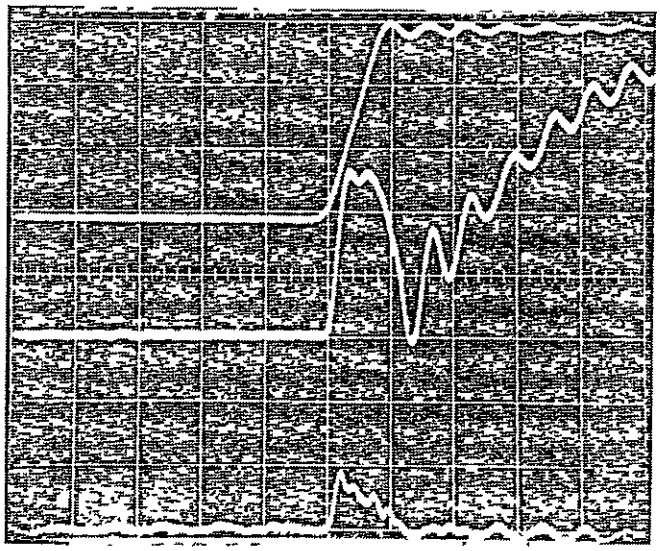
V_{ce} (on) 1V/DIVISION

I_L 1 A/DIVISION

1 μsec/DIVISION

Figure 27. V_{ce} (on) for the lower transistor (V_{in} = 300 Vdc I_L = 0.8 A).

6749-27

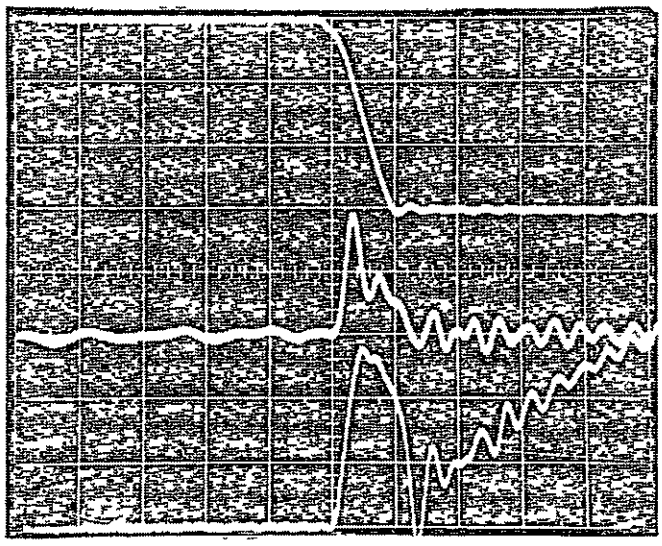


V (Φ_A) 100 V/DIVISION
I_C (UPPER) 0.5 A/DIVISION
I_E (LOWER) 0 5 A/DIVISION

100 nsec/cm

Figure 28. Transistor switching waveforms (I_L = 0.8 A).

6749-28

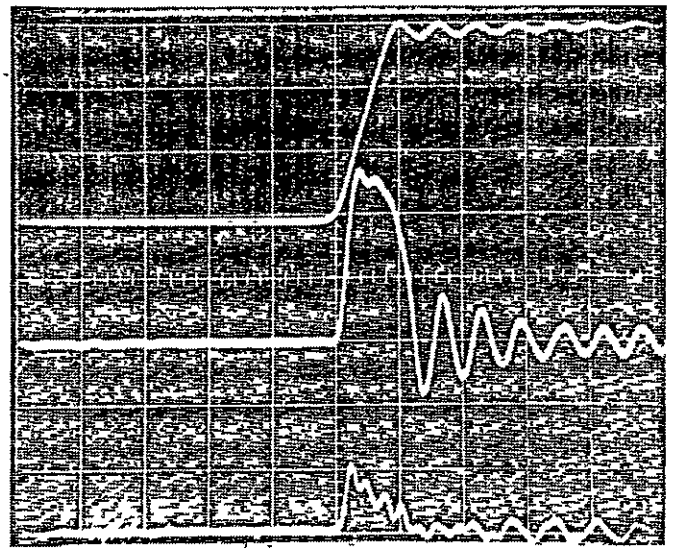


V (Φ_A) 100 V/DIVISION
I_C (UPPER) 0 5 A/DIVISION
I_E (LOWER) 0.5 A/DIVISION

100 nsec/cm

Figure 29. Transistor switching waveforms (I_L = 0.8 A).

6749-29



V (Φ_A) 100 V/DIVISION

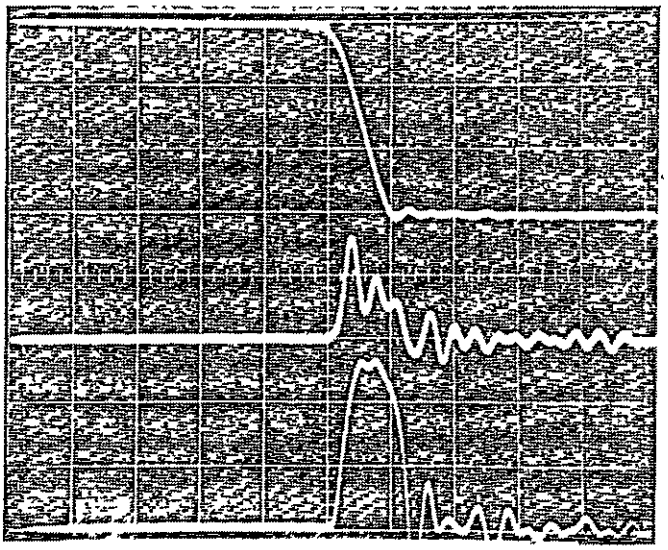
I_C (UPPER) 0.5 A/DIVISION

I_E (LOWER) 0 5 A/DIVISION

100 nsec/cm

Figure 30. Transistor switching waveforms (I_L = 0 A).

6739-30



V (Φ_A) 100 V/DIVISION

I_C (UPPER) 0.5 A/DIVISION

I_E (LOWER) 0.5 A/DIVISION

100 nsec/cm

Figure 31. Transistor switching waveforms (I_L = 0 A).

6749-31

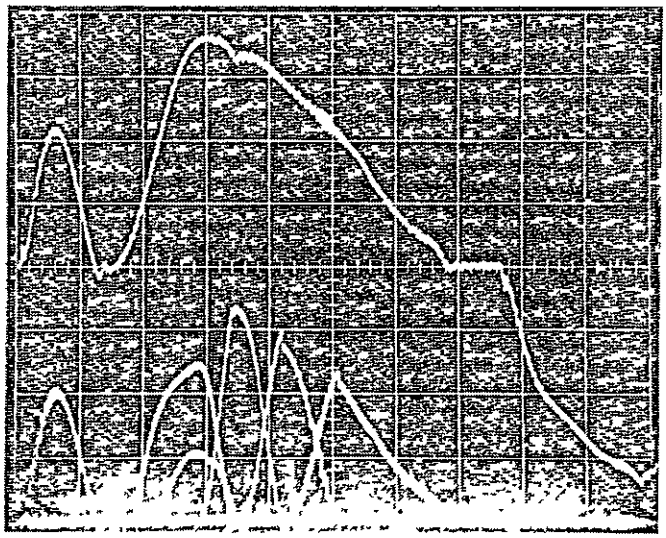


Figure 32. Multi-exposure of rectifier currents showing summation to phase current.

6749-32

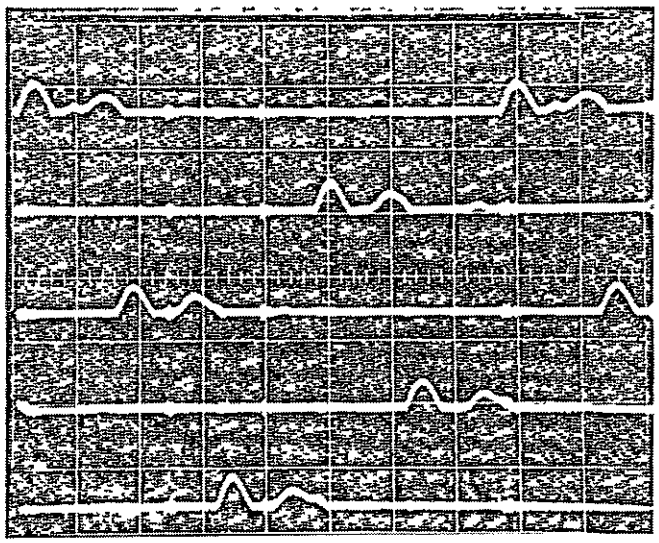
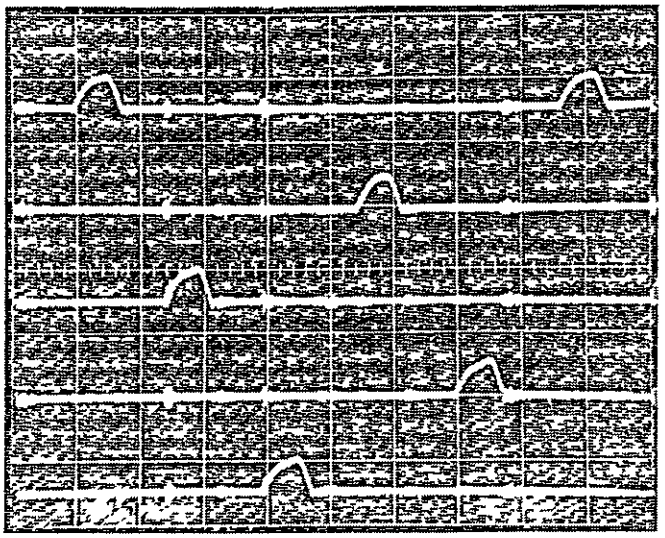


Figure 33. CDVM rectifier currents (I_L = 0.8 A).

6749-33



5 A/DIVISION

I_{R4} (Φ_A)

I_{R4} (Φ_B)

I_{R4} (Φ_C)

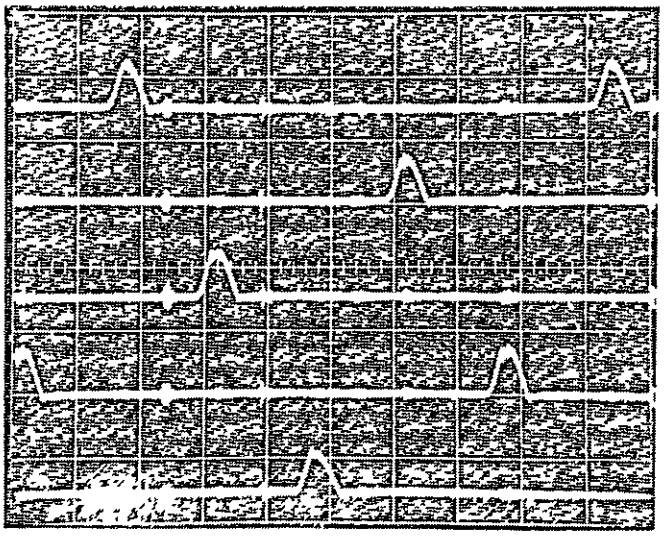
I_{R4} (Φ_D)

I_{R4} (Φ_E)

2 μsec/DIVISION

Figure 34. CDVM rectifier currents.

6749-34



5 A/DIVISION

I_{R3} (Φ_A)

I_{R3} (Φ_B)

I_{R3} (Φ_C)

I_{R3} (Φ_D)

I_{R3} (Φ_E)

2 μsec/DIVISION

Figure 35. CDVM rectifier currents.

6749-35

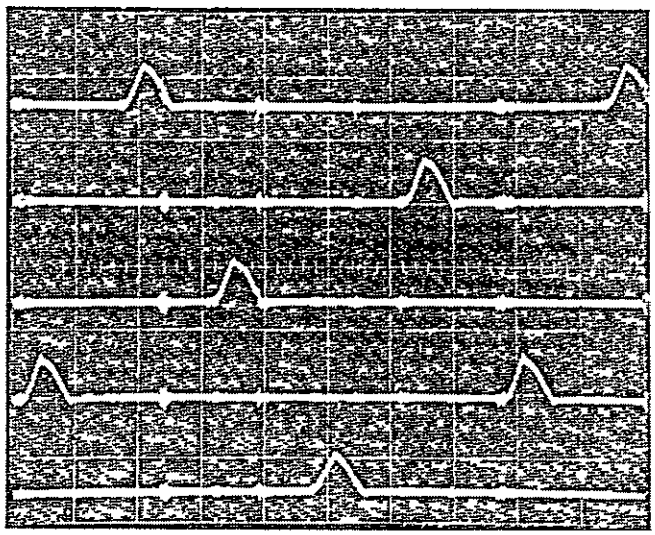


Figure 36. CDVM rectifier currents.

6749-36

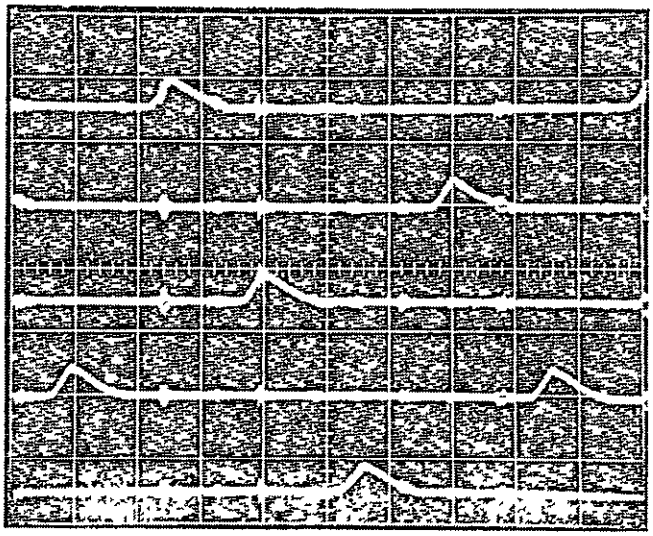


Figure 37. CDVM rectifier currents.

6749-37

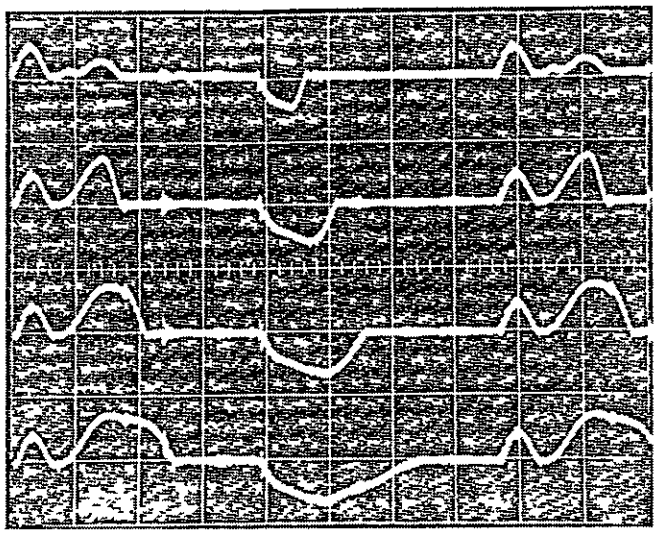
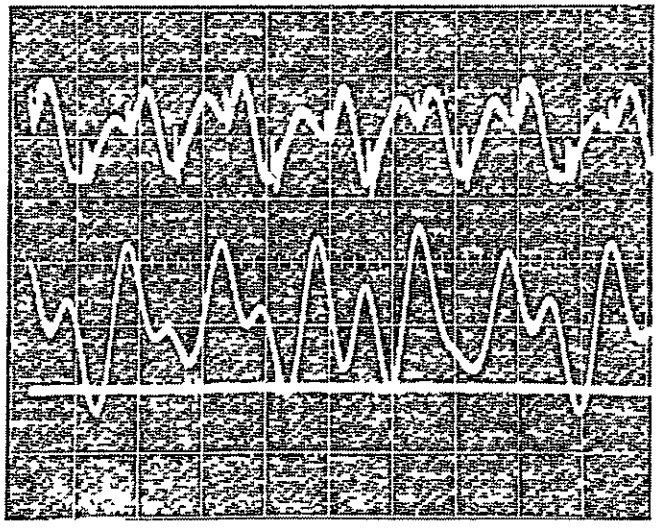


Figure 38. CDVM capacitor currents.

6749-39



6749-38

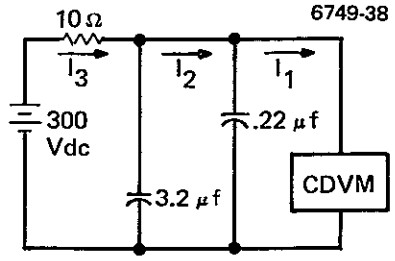
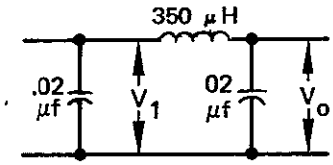
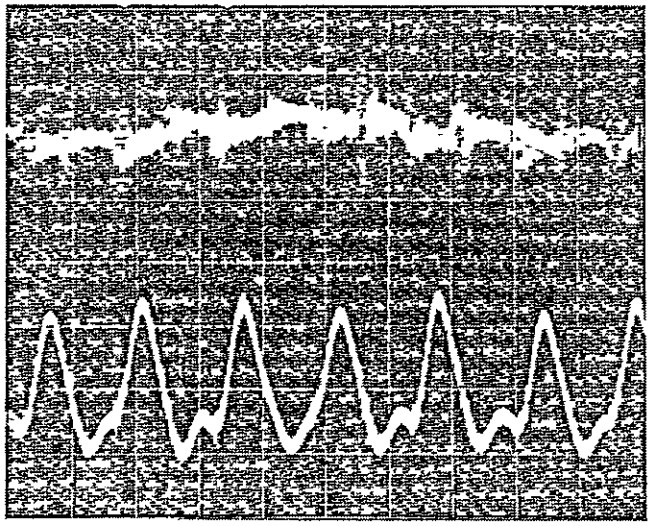


Figure 39. Input current.

6749-40

6749-41





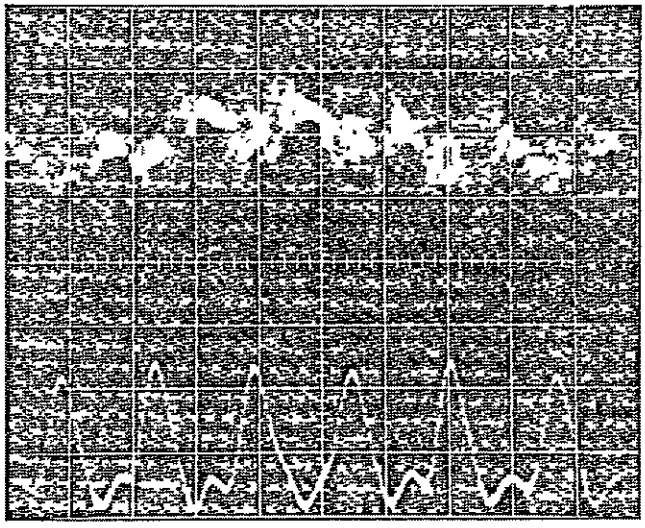
V_0 5 V/DIVISION

V_1 10 V/DIVISION

2 μsec/DIVISION

Figure 40. Output ripple voltage (I_L = 0.8 A).

6749-42



V_0 5 V/DIVISION

V_1 10 V/DIVISION

2 μsec/DIVISION

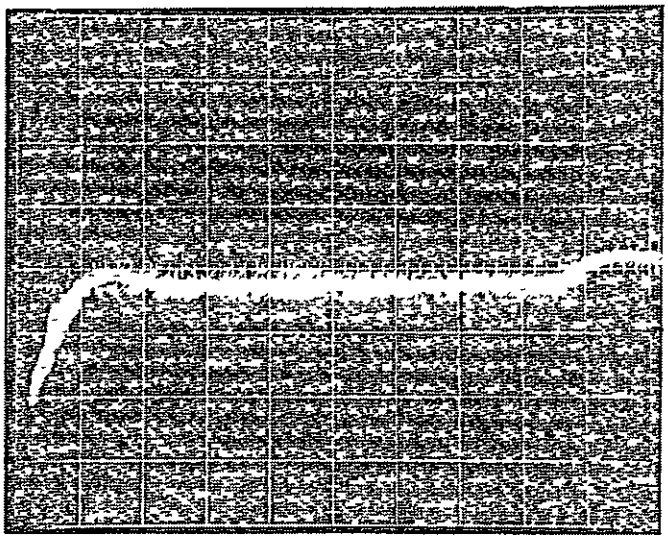
Figure 41. Output ripple voltage (I_L = 0.4 A).

3.2-μF CDVM input capacitor filter, it is difficult to determine the CDVM response time. Figure 42 shows the circuit used and the output response to a 50-V input voltage change. The first portion of the waveform corresponds to the CDVM response time (≈0.2 msec). The second transient is a result of the transient response of the 200-Vdc supply to a load current change. Figures 43 and 44 show the circuit and waveforms used to demonstrate the transient response to a transient load change. The extreme difficulty in separating the input filter response from the CDVM load response is illustrated by comparing the input and output voltages during the load transient. Without the 10-Ω resistor in series with the bus, the output voltage change would be ≈10 V and would settle within 0.2 to 0.4 msec. The transient response of any dc-dc converter to a load change depends on the source impedance.

Figure 45 shows the output voltage of the CDVM during start-up. To demonstrate that a CDVM circuit can withstand a load fault requires as a precondition that it be shown that the transistors can withstand the start-up surge currents. Figure 46 shows the voltage and current of a typical transistor during start-up. The transistor pulls 50 V out of saturation during the first few cycles. With 50 V across the transistors, the MJ7261 is capable of carrying 30 A for 200 μsec. Since the peak current stays below 20 A and the transistors easily saturate within 200 μsec, the transistor operates in the safe operating area during start-up.

Figure 47 shows the inductor current immediately after a load fault. As predicted, the peak current in the inductor is less than 55 A. Figures 48 through 50 show the resulting CDVM rectifier currents in a single phase. The rectifiers are not overstressed during the fault: they are capable of withstanding 25 A peak currents, but the actual peak current was in all cases less than 12 A.

6749-43



V_0 100 V/DIVISION

0 1 msec/DIVISION

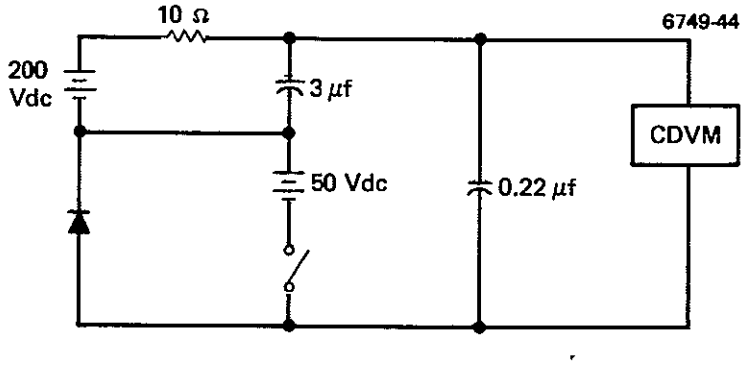
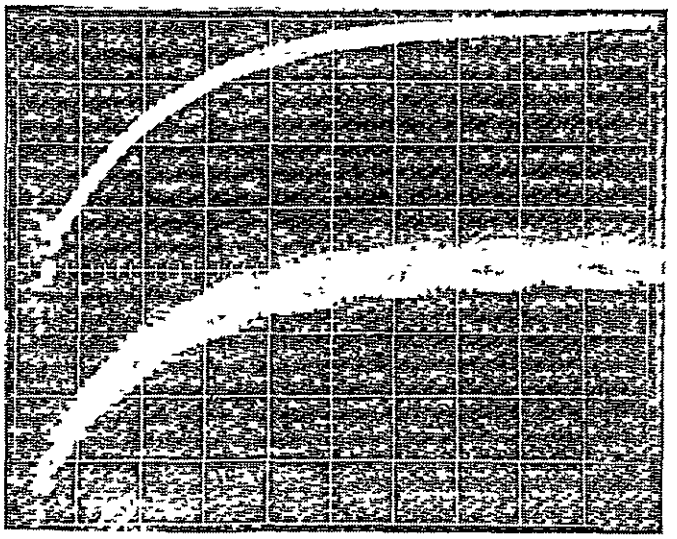


Figure 42. Transient line test (200 to 250 Vdc, I_L - 0.8 A).

6749-45



V_0 20 V/DIVISION

V_{in} 5 V/DIVISION

0 1 msec/DIVISION

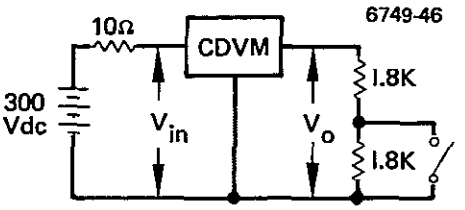


Figure 43. Load transient test (load current increased from I_L = 0.48 A to 0.84 A).

6749-47

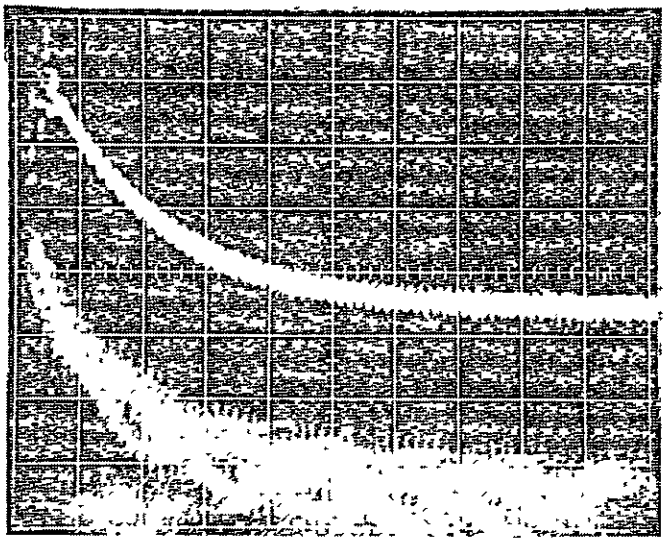
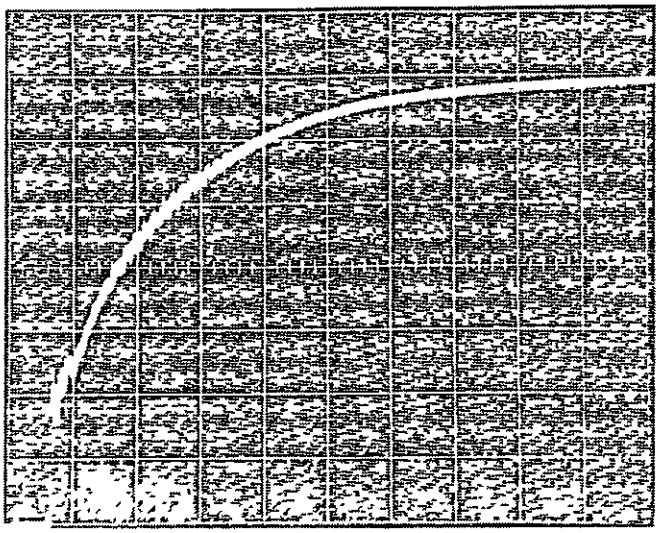


Figure 44. Load transient test; load current decreased from I_L = 0.84 A to 0.48 A.

6749-48

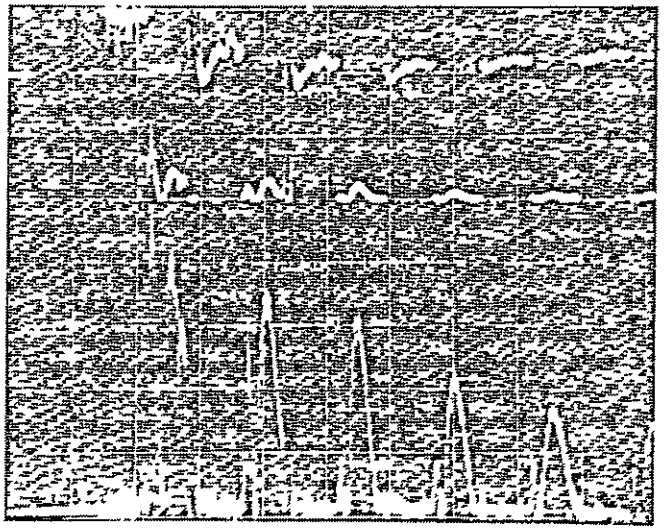


V_0 200 V/DIVISION

0 1 msec/DIVISION

Figure 45. Output voltage during start-up.

6749-49



V (Φ) 100 V/DIVISION

I_C 5 A/DIVISION

10 μsec/DIVISION

Figure 46. Typical transistor voltage/current during start-up.

6749-50

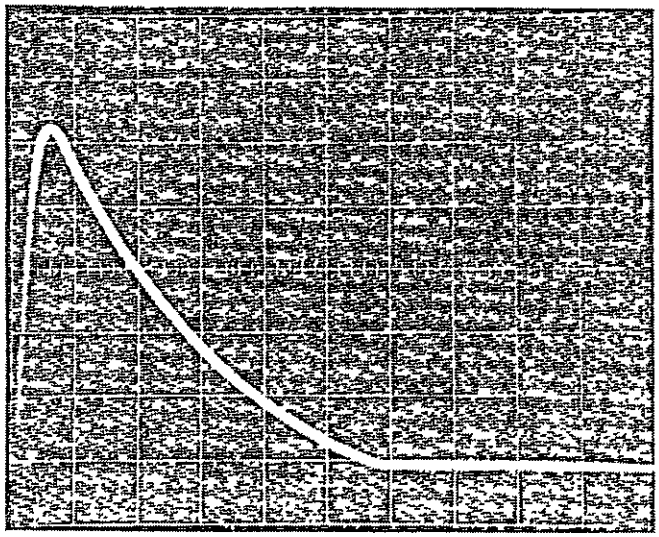


Figure 47. Inductor current during a fault.

6749-51

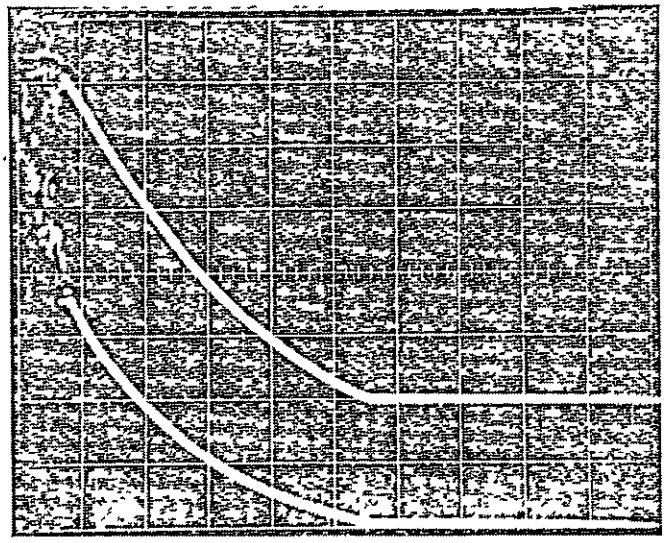


Figure 48. Rectifier currents during a fault.

6749-52

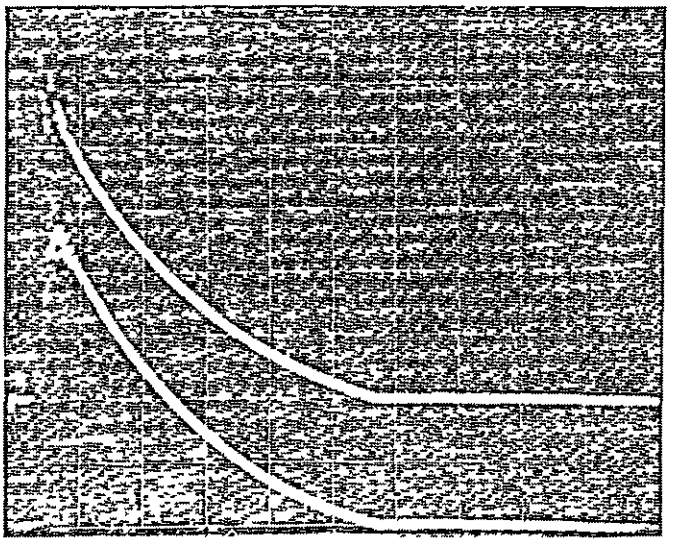


Figure 49. Rectifier currents during a fault.

6749-53

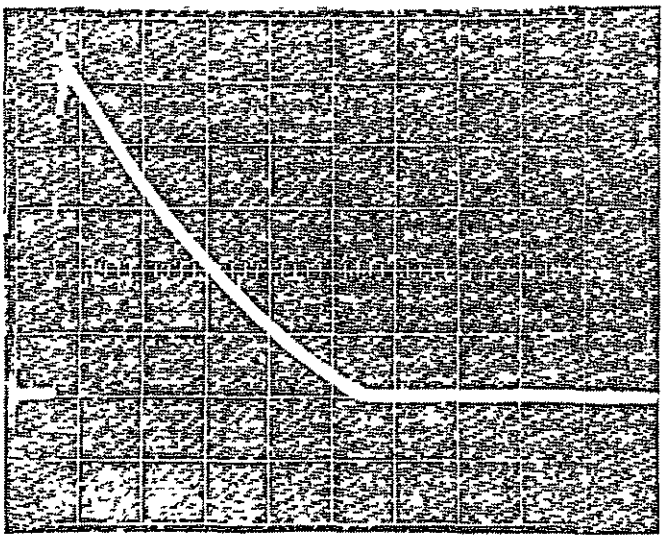
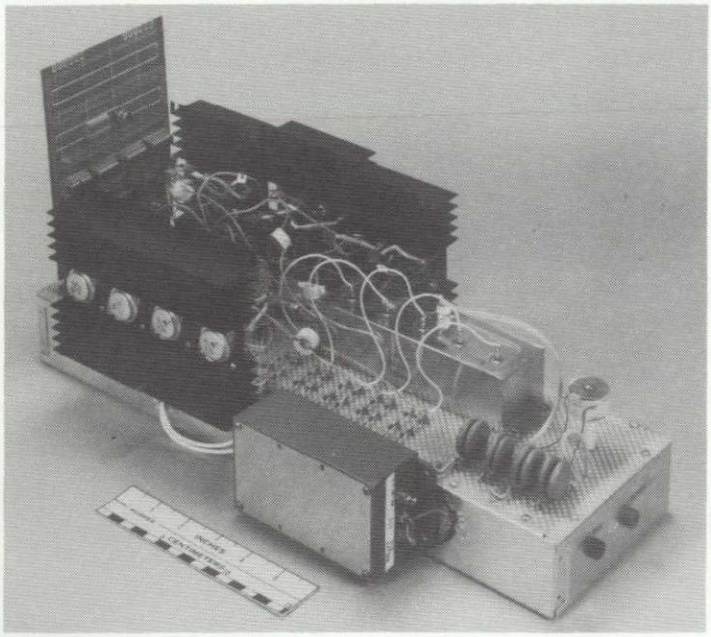
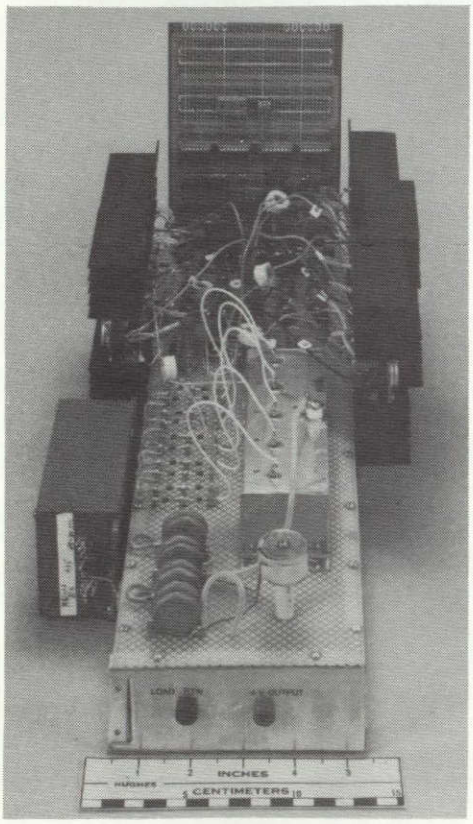


Figure 50. Rectifier currents during a fault.

A photograph of the breadboard model CDVM circuit is shown in Figure 51. On the basis of the components used in this circuit, the mass of a flight-packaged circuit can be projected as shown in Table 4. Table 5 gives the mass breakdown for a state-of-the-art transistorized transformer-coupled dc-dc converter. Since the power level for the transformer-coupled circuit is only 600 W, its specific mass (kg/kW) is greater than is that of the transformer-coupled circuit.

6749-54





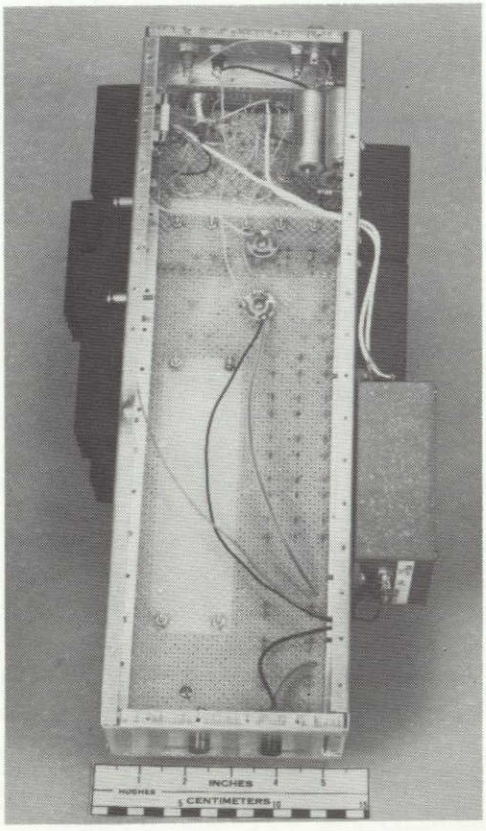


Figure 51. CDVM breadboard model.

SECTION 5

CONCLUSIONS

The feasibility of a high-power CDVM has been demonstrated by the design, fabrication, and testing of a 1.2-kW unit. Because of the high operating frequency and the unique properties of the multiphase CDVM converter, a very low component mass-to-power ratio and high efficiency have been simultaneously achieved. The CDVM has a 1.8-to-1 mass advantage over the conventional dc-dc converter. The two converters will be nearly indistinguishable in terms of efficiency: the transformer-coupled transistor is projected to have no more than a 0.5% advantage over the CDVM converter.

Generalized equations describing the operation of an N-phase, M-stage CDVM were used to design a five-phase CDVM and to predict its performance characteristics. Excellent correlation between test data and predicted values for output voltage, peak currents, and efficiency demonstrated the accuracy of the generalized equations. Since the same equations were used to design the 6-kW ion thruster screen supply for the thrust system trade-off study described in Volume III, the predicted voltages, efficiency, and weight have been validated.

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